# DIGITAL DC MOTOR SPEED CONTROL WITH PHASE LOCKED LOOP REGULATION

by

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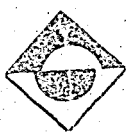

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# ABSTRACT

The object of the thesis is to study the speed control of direct current motor by using phase locked loop principle and compare alternative methods applied in practice.

The operation of phase locked servo systems is described and a linear discrete model is developed to describe their behavior. This model explains the observed phenomenon that the system becomes unstable at low speeds. Also discussed are the design problems, speed variations, and the extension of lock range by lag-lead networks.

A phase locked loop speed control system incorporating a digitally controlled single-phase thyristor bridge is described and the experimental results are given for the case of a separately excited d.c. motor.

# ÖZET

Bu tez çalışmasında bir doğru akım motorunun sayısal evre kilitlemeli çevrim prensibine göre hız denetimi ele alınmış ve uygulamada kullanılan diğer yöntemlerle karşılaştırılmıştır.

Evre kilitlemeli çevrim düzeneklerinin çalışması anlatılmış ve davranışını belirleyen doğrusal ayrık modeli geliştirilmiştir. Bu modelin düzeneğin düşük hızlarda niye kararsız olduğunu açıkladığı gösterilmiştir. Ayrıca tasarım sorunları, hız değişimleri ve ileri-geri (lag-lead) süzme devreleriyle kilitleme aralığının genişletilmesi de incelenmiştir.

Denetimli silisyumlu doğrultmaçlardan oluşan tek evreli tam dalga köprü ile serbest uyarmalı bir doğru akım motorunun hız denetiminin tasarımı, uygulaması ve denenmesi evre kilitlemeli çevrim prensibine göre yapılmış, deney sonuçları varilmiştir.

# TABLE OF CONTENTS

# INTRODUCTION

Speed control of electric motors is a common requirement in industrial processes. Various analog techniques are proposed from time to time and many of them are now in common use. The general procedure is to sense the angular speed, compare it with the desired one and develop some control signal which acts to bring the actual speed to the desired speed.

With the recent advances in digital technology, digital techniques are replacing the analog techniques with respect to measurement of speed and production of error. Speed control of motors by Phase Locked Loop (PLL) servo systems is becoming increasingly popular. Most of the methods use phase locked loop in which an encoder mounted to the motor shaft provides a pulse train signal, representing its speed. A reference pulse train and encoder signal are applied to a phase detector, the output of which drives the power amplifier and the motor, which, in this way, behave like a voltage controlled oscillator (VCO).

This thesis reports the work carried out for the development of a motor control circuitry for a dc motor using phase locked loop techniques. The purpose of such a control loop is to provide very accurate speed control, repeatability and synchronability.

The proposed circuit is based on the PLL principle. The effects of discrete phase detector output are explained and the stability limits on speed are predicted. Compared to a analog system; this system is simpler, cheaper and provides speed control with extreme precision. The scheme is especially suited for applications where a number of motors are to run in synchronism without any mechanical interconnections.

The system is basically made up of the following units:

a. A phase detector which compares the phase and frequency of the reference signal with those of the encoder signal,
b. A lag-lead filtering unit which filters the PFD output and extends the lock range,
c. A thyristor bridge whose output is varied in accordance with the filter output using pulse width modulation techniques.
d. A separately excited d.c. motor coupled to a d.c. generator for loading purposes.

In Chapter 1, a survey of dc motor speed control techniques is given and PLL servo system is introduced.

In Chapter 2, the theory of PLL systems is developed and using the z-transform analysis, the system stability and lock range is related to the system parameters.

In Chapter 3, the implementation of the system is presented, the design of various units are described.

Finally, in Chapter 4, the experimental results are given and compared with the theoretical expectations of Chapter 2.

# CHAPTER 1

# DIRECT CURRENT MOTOR CONTROL

The ability to be able to control its speed by variation of the armature voltage or by change in its fields current gives the dc motor great flexibility of operation. The fact that its torque is dependent on armature current and air-gap flux enables it to perform satisfactorily even under the most arduous duty cycles.

As a result, dc motor has been extensively used in all industries and in all environments wherever variable speed rotational drives have been required; to drive factory machines, trains, printing presses, mine hoists pumps, cranes, steel mills, ships, fans, paper making machines, conveyors.

## 1.1. DIRECT CURRENT MOTORS

Since its invention in the late 19th century the dc motor has been recognized as an ideal means of obtaining controlled

rotational motion and great numbers of dc motors are still made today because their characteristics are so well suited to many variable speed drives. Their inherent characteristics lend themselves to high starting torques, which are required for traction drives. Their speed range is large both above and below the rated values. Finally, the methods of control are in most cases simpler and less costly than the method of control of ac motors to obtain the same performance.

The equivalent circuit of the armature from the supply point of view is shown in Figure 1.1 in which $R_a$ is the total armature circuit resistance and $L_a$ is the total armature circuit inductance.

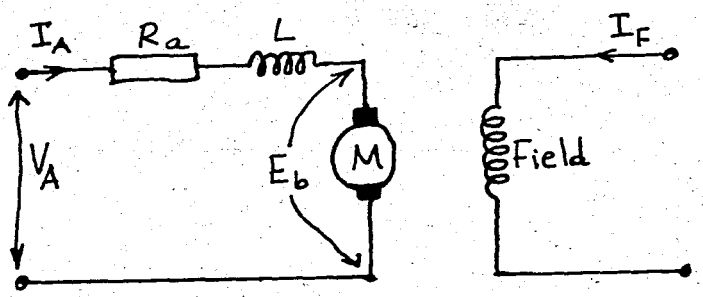



FIGURE 1.1. Schematic Representation of a Separately Excited Motor.

The back e.m.f., $E_b$ will be generated by the rotation of armature in the field flux.

Total armature circuit voltage is,

$$V_a = E_b + I_a \cdot R_a$$

The back e.m.f. $E_b$ is proportionality to the speed of rotation of armature and the field flux can be represented by

$$E_b = K_E \cdot \phi_f \cdot N$$

The torque developed by a dc motor is directly proportional to the armature current $I_a$ and the flux per pole $\phi$ (or $\phi_f$); that is

$$T = K_T \cdot \phi_f \cdot I_a$$

The simultaneous solution of the three equations yield for the speed

$$N = \frac{V_a - T\,(R_a/K_T\phi_f)}{K_E \cdot \phi_f}$$

where $V_a$ = supply voltage

$E_b$ = armature induced e.m.f.

$I_a$ = armature current

$R_a$ = armature resistance

$K_E$ = armature voltage constant

$\phi_f$ = field flux

$N$ = armature speed (rps)

$T$ = produced torque

$K_T$ = motor torque constant

The second term in the numerator is usually small. The speed equation shows that the speed of the motor can be controlled in three ways. They are:

1. by the armature circuit voltage $V_a$ which is nearly proportional to speed;
2. by the magnetic field, which is inversely proportional to speed; and
3. by the armature circuit resistance R, which is proportional to the speed drop.

The separately excited motor can be controlled by either field current or armature voltage. Field current control has its limitations however; reduction in field current (to increase speed) reduces the torque and in addition it cannot be changed quickly owing to the high inductance of the field windings. Hence, field control is suited for applications where constant power is required as speed increases. Armature voltage control suffers from neither of these limitations and when used with a fixed field allows very rapid changes of speed and torque to take place. Finally, armature resistance control is not practical except in small motors because of the power dissipation.

It can be seen that when the field flux is held constant at its rated value, variations of the applied voltage will result in variations of speed from zero to base speed, and the motor is said to be operating as a constant torque drive. When

the applied armature voltage is at the rated value, then reducing the field flux results in the above base speed being produced, and the motor is said to be operating as a constant horse power drive. These conditions are illustrated in Figure 1.2.

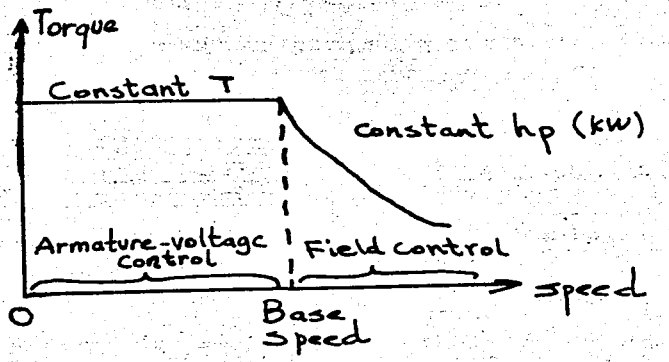



FIGURE 1.2. Torque-speed Characteristics of a Separately Excited dc Motor with Variable Armature Voltage and Field Control.

## 1.2. SPEED CONTROL TECHNIQUES OF DC MOTORS

D.C. motor control using Ward-Leonard sets required the use of three electrical machines: a three phase induction motor, a dc generator, and a dc motor. This can now be replaced by a solid-state controller employing only one electric machine, the dc motor. Changing from electro-mechanical control systems to electronic control systems generally provides a reduction in efficiency. With recent advances in power electronic components and integrated circuits it is now achievable with both cost and quality comparable to that of alternative systems.

In constant torque applications the motor field excitation remains constant, and as a result the excitation voltage is usually obtained from an uncontrolled rectifier connected across the ac supply lines.

In order that the motor will operate at the desired speed, it is necessary that a signal accurately represents the actual speed. There are three basic methods: First, to sense the e.m.f. of the armature circuit and reduce the voltage level by a voltage divider network, or second, to couple a tachogenerator to the output shaft of the motor. In all motor speed control techniques, motor will never remain constant at the set speed, but will vary slightly about the desired speed; the amount of the variation is a mreasure of the speed regulation capability of the drive control system. Armature voltage speed sensing techniques usually produces a speed regulation capability of $\pm$ 2 percent a.c. or d.c. tachogenerator speed sensor will provide a speed regulating capability of $\pm$ 0.1 percent. If improved speed regulation is required, then digital speed sensing tenchiques are used.

The most common available electronic systems in d.c. motor speed constrol methods are phase control and chopper control methods. Phase control methods use controlled rectifier circuits which are the simplest form of electronic motor control because the thyristors are naturally mains commutated

or line commutated from the three-phase or single phase a.c. source. In this case, motor voltage control is achieved by varying the phase angle at which the thyristors are fired relative to the incoming mains voltage supply waveform. This provides an output voltage ranging from zero to a value equal to that provided by a full-wave diode rectifying bridge.

All phase control systems use line commutation which imposes a controller bandwidth limited by the mains supply frequency, and for improved performance other systems are required.

The limitations of phase control may be overcome by using chopper control. In the principle of chopper control, the motor average voltage is controlled by varying the on-to-off time ratio for which the dc supply is applied to the load, and thyristors turn off is now achieved by forced commutation. Forced commutation, as the name implies forces the thyristor to turn off by using an auxilary circuit (the commutation circuit) consisting of an auxilary or commutation thyristor and a series resonant LC circuit. In the chopper circuit, the thyristor is used as a switch. The output of the chopper is a series of unidirectional voltage pulses that are applied to the load. These explanations are illustrated in Figure 1.3.

The mean load voltage over a cycle is given by

$$V_{do} = \frac{t_{ON}}{t_{ON} + t_{OFF}} \cdot V_d = \frac{t_{ON}}{T} \cdot V_d$$

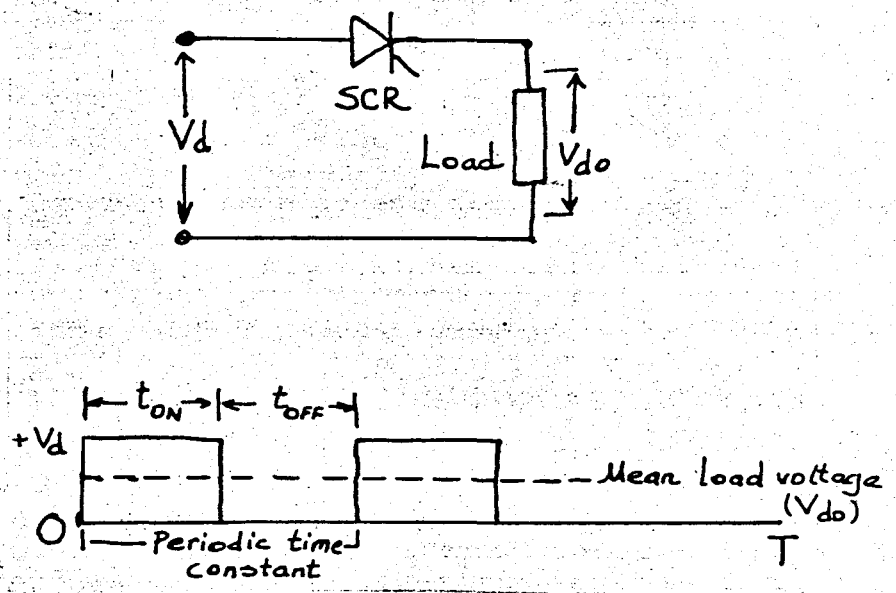



FIGURE 1.3. DC Chopper, Basic Principle.

where T = the periodic time.

Choppers provide an excellent means of controlling dc traction motors, since they eliminate the energy losses in starting and control resistances.

The degree of speed control required in the industrial drives depends on the application. In some applications the open-loop regulation of the drive motor is adequate. In others feedback control is required for better performance. Conventionally, this is achieved by an analog feedback system which any change in speed is sensed by an analog speed transducer and compared with a fixed reference voltage to generate a correction signal. However, this analog feedback system is not satisfactory in some applications where excellent speed regulation and fast dynamic response are required.

Conventional analog control methods have disadvantages

on several accounts. These methods include nonlinearity in the analog speed transducer and difficulty in accurately transmitting the analog signal after it has been obtained from the transducer |1|. In addition, error signal is subjected to temperature variations, component changes or noise |2|.

The block diagram shown in Figure 1.4 shows a typical closed-loop armature voltage analog dc motor speed control system. There are two requirements that must be met by the system: first, to limit the in-rush starting currents, and second, to control the motor speed at whatever speed setting has been designated.

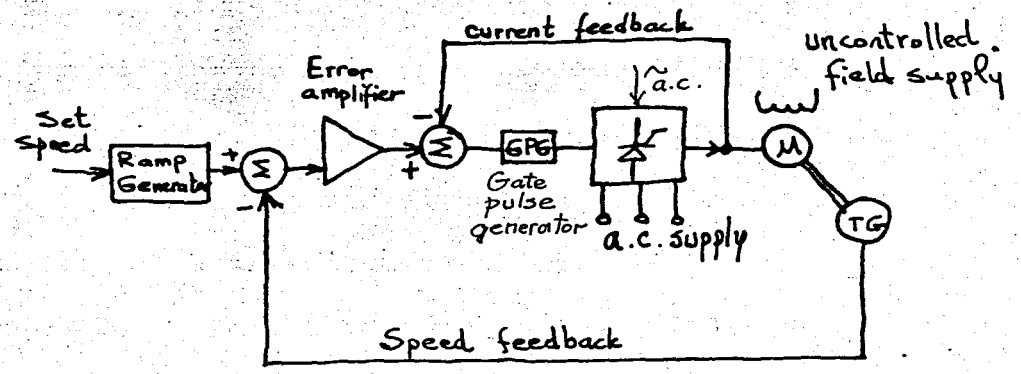



FIGURE 1.4. Block Diagram of a Phase-controlled DC Motor Analog Speed Control System.

In traditional electromagnetic dc motor control, the starting current is reduced by means of added resistance in series with the armature. In a solid-state controller the starting current

is limited by regulating the rate of advance of the firing angle by means of a ramp generator. The function of a ramp generator is to provide a controlled accelleration of the dc motor when starting the drive, irrespective of the set speed desired.

As can be seen, the drive will start with the firing angle fully retarded, and therefore a minimum voltage is applied to the armature circuit. The rate of increase of the applied armature voltage is controlled by the slope of the ramp output. As an added safeguard, a current limit signal is also generated. If the rate of acceleration of the connected load produces currents in excess of a predetermined amount, a signal is generated which will cause the firing angle to be retarded and the output voltage of the converter to be reduced to bring the armature current back within the prescribed limits. The current limit signal can be obtained either by using a dc shunt in series with the armature circuit, which will produce a voltage proportional to the armature current, or by the use of current transformer in the ac supply lines to the converter. The secondary outputs of the current transformers are rectified and once again a dc voltage signal proportional to the armature current is generated. The current feedback signal is compared against the dc signal from the error amplifier.

The disadvantages of an analog control system can be

overcome by using a digital control system. By using a digital speed control system, the speed regulation can be as good as the accuracy of the reference signal. The resulting speed will not drift due to temperature or component wear. In addition, a digital speed control system is adequate in systems where motors must be precisely synchronized to each other or to a clock signal such as conveyors, textile, paper mills, or computer peripheral drives.

A general description of digital motor speed control system has been given by Maloney and Alvarado |3|. In this work, the actual and desired speeds in the forms of pulse numbers are compared and the error is fed to an up-down counter, the output of a counter after passing through a D-A Converter and suitable amplifier, is fed to the motor armature to control its speed. The system is not continuous but measures and corrects motor speed at discrete intervals. This method was not fully digitized.

Another digital method is to use phase-locked method. PLL method provides accurate efficient dc motor speed control. PLL's were developed in the 1930's and have been extensively used in communication system |4|.

## 1.3. PHASE-LOCKED LOOP MOTOR SPEED CONTROL

In this section, the basic theory of the PLL will be

presented first, followed by an introduction of PLL motor speed control system.

Phase-locked loops have been intensively used in communication systems where accurate frequency synchronization is required. In its basic form a phase locked loop consists of a phase detector, a low-pass filter and a voltage-controlled oscillator (VCO) as shown in Figure 1.5.

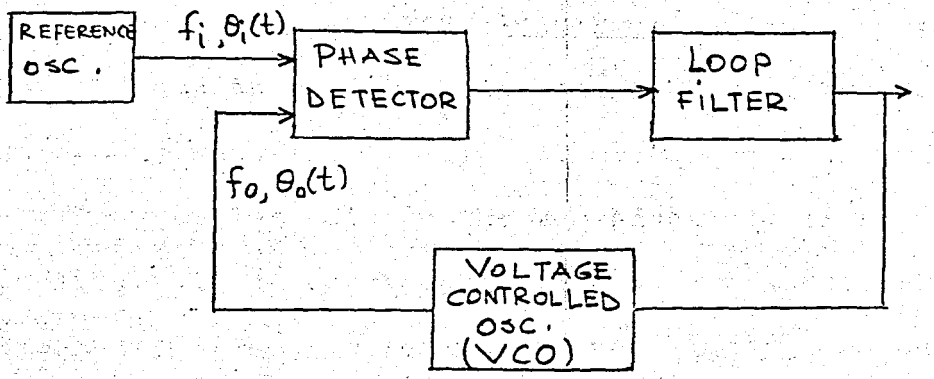



FIGURE 1.5. PLL Basic Form.

A phase detector measures the phase difference between an input voltage $v_i(t)$ and an output voltage $v_o(t)$ to give an output

$$v_d(t) = k_d(\theta_i - \theta_o)$$

where $\theta_i(t)$ is the instantaneous phase of $v_i(t)$ and $\theta_o(t)$ is the instantaneous phase of $v_o(t)$. This error voltage is passed

through a low-pass filter to reduce noise and extraneous high frequency components. The filtered voltage drives a VCO and alters its frequency in such a direction as will minimize the phase error. The output frequency of the VCO is inversely proportional to its input voltage.

If the VCO output is lower in frequency or lags in phase with that of the reference oscillator, the error voltage appearing at the output of the phase detector will decrease. The output frequency of the VCO will then increase (or gain in phase) to compensate for the original error. The error voltage is zero only when the two signals are exactly in phase. A slight lead or lag between the two signals will result in a corrective voltage and compensation will automatically occur. In this way, with a properly designed filter, the output frequency of the VCO can be made to phase-lock with, and therefore track with extreme precision, the frequency of the reference oscillator.

The accuracy with which the VCO output frequency tracks the reference is dependent on the dynamic characteristics of the feedback loop and limited ultimately only by the stability of the reference oscillator. The loop is said to be locked when the error voltage remains steady and the frequency of the reference oscillator is exactly equal to that of VCO output frequency. By inserting a frequency divider (usually a digital

counter) in the feedback path the VCO frequency can be synchronized to a multiple of the reference frequency. Such a configuration is called a frequency synthetiser, which usually is used to generate precise frequencies.

A phase-locked loop applied to dc motor speed control is similar to basic PLL loop technique except that the motor, encoder, and motor driver (thyristor bridge converter or chopper) replace the VCO. A basic form of PLL motor control is shown in Figure 1.6.

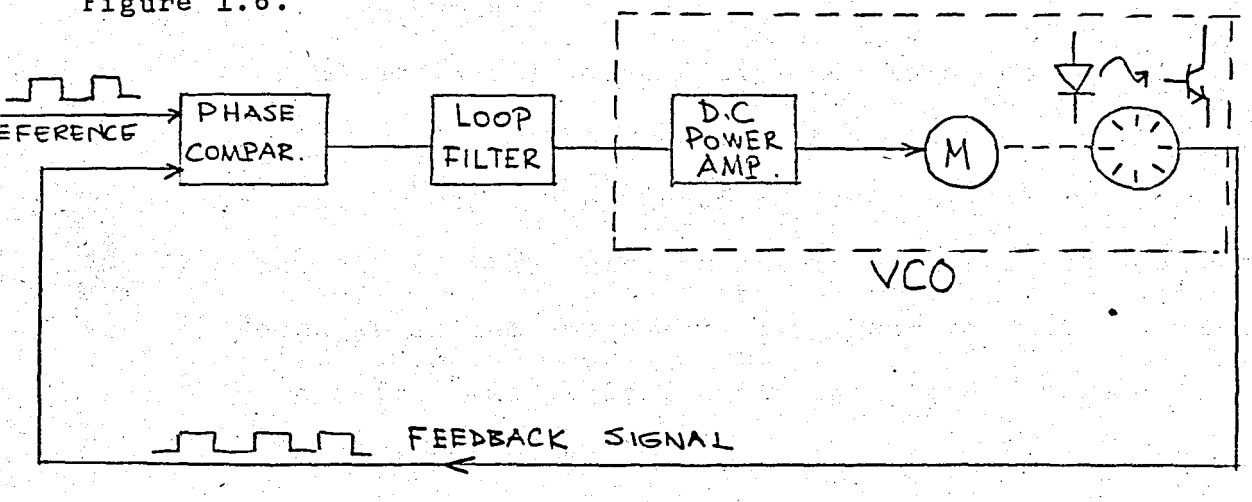



FIGURE 1.6. A Basic Form of PLL Motor Control.

The motor speed can be controlled by varying the reference input frequency or by changing the counter modulus which is inserted in the feedback path.

The use of a dc motor as the voltage controlled oscillator in a PLL increases the complexity of the loop design. In electronic PLL design it is assumed that the VCO responds in-

stantaneously to changes in the input voltage. A motor, on the other hand, has a much longer response time due mostly to the mechanical inertia of the system. This response delay affects the stability of the PLL and places much more stringent requirements on the phase detector.

The most important parameters of motor PLL control are the frequency capture range, the frequency lock range, and the ability of the phase detector to avoid locking on harmonics. The frequency lock range is the range of frequencies over which the PLL can maintain a locked condition. This determines the range of motor speeds. The frequency capture range is the range over which lock can be acquired if it has been lost. This is important because the motor cannot respond instantaneously to rapid changes in the speed set point, and the motor will lose "lock" for a short time period. With the proper phase detector, "lock" may be reacquired quickly For the same reason, the ability to "lock" only on the fundamental frequency is also necessary. Large changes in set-point could result in incorrect motor speed if the loop locked onto a harmonic of the reference signal.

An alternative approach to PLL speed control of a dc motor is by the use of VCO which is used as a reference signal. The VCO is basically an external R-C astable multivibrator whose frequency is set by an external R-C combination to the center

or free running frequency. The desired speed is set by varying the center frequency of the VCO. The block diagram of the system is given in Figure 1.7.

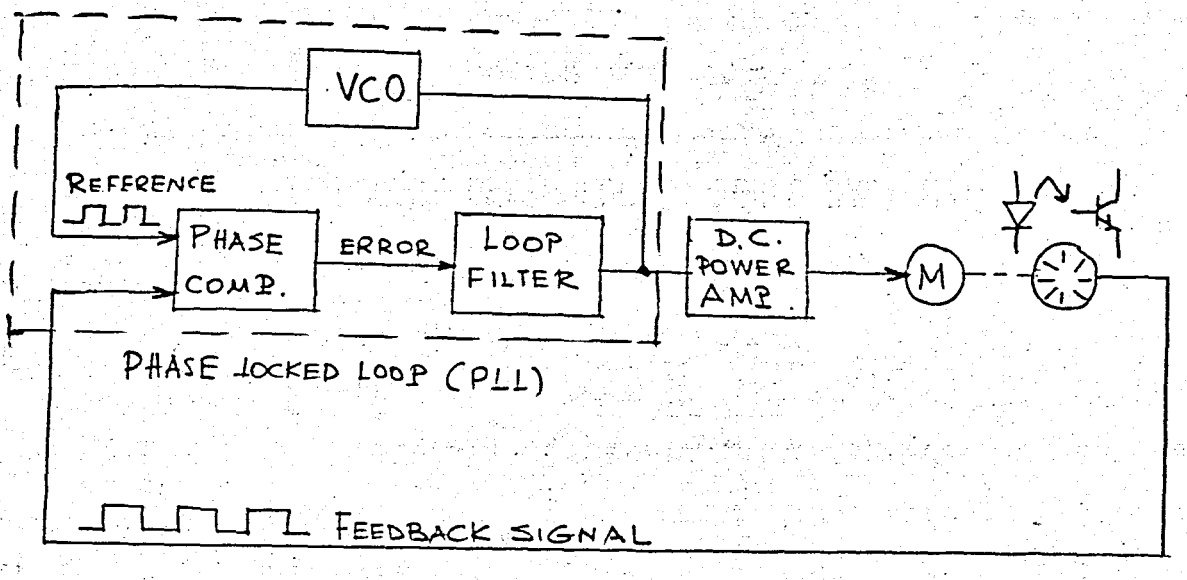



FIGURE 1.7. Block Diagram of the PLL Motor Control System.

The feedback signal from encoder representing actual speed is locked to the VCO frequency, provided that it is within the capture range. Any drift of the VCO frequency caused by aging, noise, or temperature variations will be followed by the motor. If there is a deviation of motor speed, this deviation will be detected by the comparator and a error signal will be produced by the low-pass filter, which will cause the VCO frequency to stay in phase with the encoder signal, and also supply a corrective signal to the dc amplifier, whose output will be varied to opposite the change in the motor speed. As a result, the motor is forced to maintain the speed set by the center frequency of the VCO.

# CHAPTER 2

# SPEED CONTROL BY PHASE-LOCKED SERVO SYSTEMS

In this chapter, the analysis and design of PLS systems are discussed. A model is derived for the phase frequency detector. This model explains why PLS becomes unstable at some defined speeds. Also, the design requirements and the main problems encountered in the implementation are discussed. These include the system bandwidth, the lock range and the speed variations of the motor.

## 2.1. PHASE-LOCKED SERVO SYSTEM

Phase-locked loop principle can be applied to servo systems in order to regulate the motor speed. The VCO is replaced by an power amplifier , a motor, an encoder which generates a pulse-train signal that accurately represents the actual motor speed. The resulting system is the phase-locked servo system (PLS) shown in Figure 2.1.

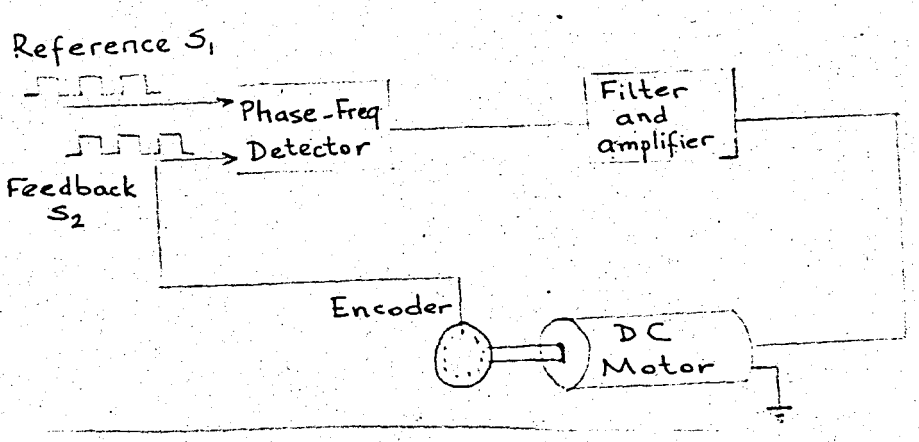



FIGURE 2.1. Phase-Locked Servo System.

When the system in Figure 2.1 is locked, the reference and feedback signals have the same frequency and a constant phase difference. Any deviation from this condition is detected, filtered, amplified and fed back to the motor for speed correction.

Zhile the fundamentals of PLL and PLS are the same, there are several important differences. These differences give rise to different design requirements and system components. The main differences between PLL and PLS are:

1. Frequency Range

The frequency of the input signal in PLL is usually high and its range is narrow. In contrast, the input frequency of PLS is much lower and its range is wide, up to 1000:1.

2. Loop Components

The feedback signal is generated in the PLL by VCO, which responds instantly to changes in command. In PLS, the

generation of the feedback signal is done by the motor and an amplifier which have considerably longer response time, thereby introducing additional lag in the loop.

3. Noise

The main source for noise in PLL is the input signal which is usually corrupted. In contrast, the noise in PLS is generated primarily by the loop components.

## 2.2. SYSTEM MODEL

In this section, we develop a model for the PLS depicted in Figure 2.1. As a first step, we combine all the linear continuous components, namely the filter, the power amplifier, trigger circuit and the motor. The transfer function of this combination of components is the ratio of the Laplace transform of motor angular speed $\omega$ to the Laplace transform of the phase comparator output x.

$$F(s) = \frac{\omega(s)}{x(s)}$$

Next, we consider the optical encoder and the waveforms $s_1(t)$ and $s_2(t)$ by $\theta_1(t)$ and $\theta_2(t)$ respectively. Since $s_2(t)$ is a nonlinear function of $\theta_2$, we prefer to regard $\theta_1$ and $\theta_2$ as the basic variables. Since the encoder produces n pulses per shaft revolution, the phase $\theta_2$ is n times the angular shaft position. The encoder transfer function can be expressed as

$$H(s) = \frac{\theta_2(s)}{\omega(s)} = \frac{n}{s}$$

The last component to be considered is the PFD. This is a digital circuit which senses the leading edges of the input signals and changes accordingly. In spite of the variety of detectors, most of them can be described by a three state model where transistions are caused by leading edges of $s_1$ or $s_2$.

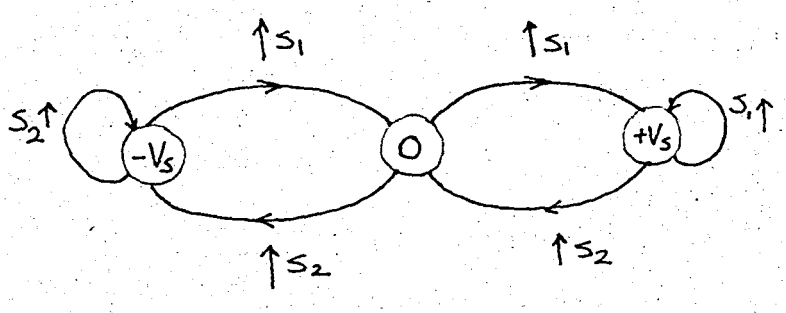



FIGURE 2.2. Three-State Model of PFD.

When the frequencies of $s_1$ and $s_2$, $f_1$ and $f_2$ respectively, are the same and $s_1$ leads, the output switches between 0 and $V_s$. If $s_1$ lags, the output switches between 0 and $-V_s$, it can be seen that the output will be between 0 and $V_s$ when $f_1 < f_2$ and between 0 and $-V_s$ when $f_1 > f_2$.

It is clear that such a component is quite complex to describe by a transfer function, and the development of the mode

needs to be tailored to its behavior. Accordingly, several models were developed.

a. Average output under lock condition -- When $f_1 = f_2$ and the phase difference is constant, the output x will be stationary, with a pulse width proportional to the phase difference. Therefore, the average output signal is proportional to the phase difference $\theta$, where $\theta = \theta_1 - \theta_2$. This model was suggested by Moore [5].

b. Average output under frequency difference -- When $f_1 > f_2$, the output switches between 0 and $+V_s$. When the two frequencies are nearly the same, the output stays for equal times in the two states, resulting in an average of $V_s/2$. As $f_1$ increases, the output will remain in the $+V_s$ state for longer times than in the 0 state, resulting in an increased average. Consequently, the average output increases with the frequency, as shown in Figure 2.3. This model was suggested by R. Schmidt [6]. It is useful in understanding the acquistion mechanism of PLS.

These two models describe the average of the output, and therefore cannot be used for stability analysis. For this purpose, a linearized model is developed. The mathematical details are given in Appendix A, and the summary is shown below.

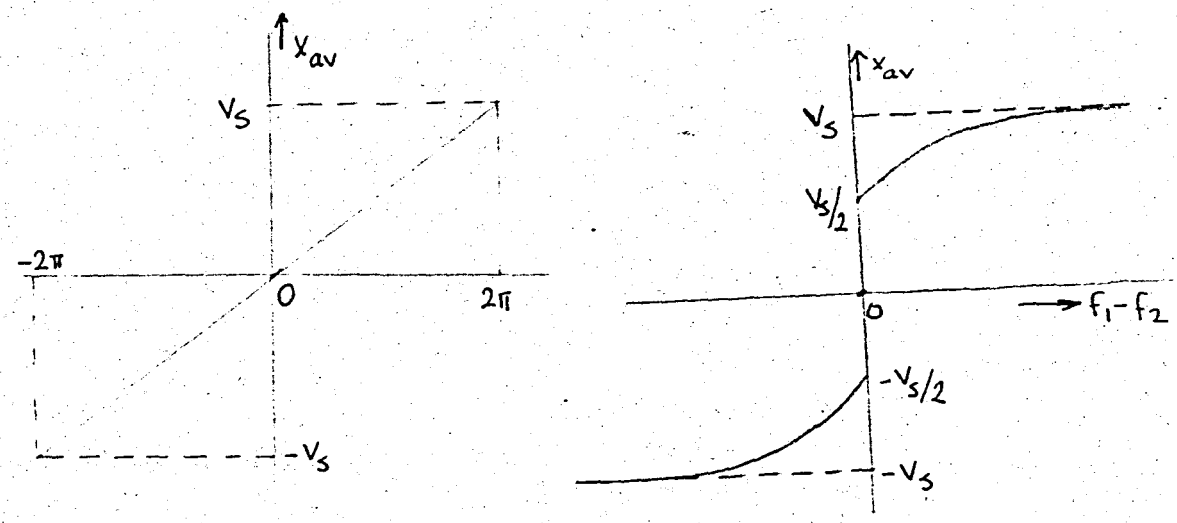



FIGURE 2.3. Average Output Under Lock and Linearized Model.

c. Linearized model -- The linearized model for PFD, when the reference signal has a period T, is that the output x is obtained by sampling the phase difference, $\theta$, by a train of impulses of weight $V_s T/2\pi$

$$x_t = \frac{V_s T}{2\Pi} \sum_{k=0}^{\infty} \theta(t)\ \delta(t-kT)$$

When the PLS components are combined together, they form the linearized model shown in Figure 2.4. This model is a basis for the analysis and understanding of the system.

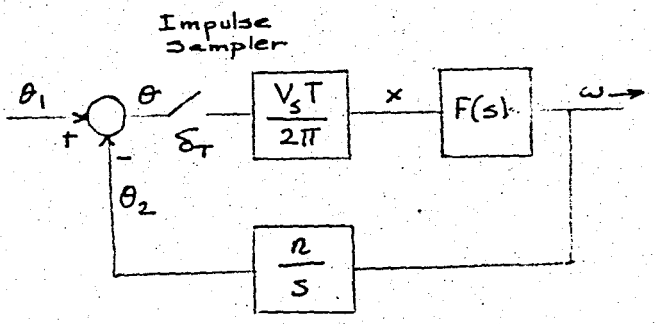



FIGURE 2.4. Linearized Model of PLS.

## 2.3. DISCRETE SYSTEM ANALYSIS

In this section, we use the models depicted in Figure 2.4 to analyse the stability of PLS. The analysis of the discrete system is more complex as it involves determining the aharacteristics roots of the loop using techniques of discrete-time system analysis. Analysis of this discrete model is most easily done in the z-domain where root locus methods can again be applied. This involves the z-transform which is described in most sampled data control texts |7|, |8| and will not be detailed here.

Consider the system shown in Figure 2.4 and define the transfer function H(s) as:

$$H(s) = \frac{n\ V_s\ T\ F(s)}{2\Pi_g s} \qquad (1)$$

The stability of the loop is determined by the characteristic equation

$$1 + H(z) = 0 \tag{2}$$

where H(z) is the discrete transfer function which corresponds to H(s). The system is stable as long as all the roots of (2) are within the unit circule. Furthermore, roots close to the origin result in rapid response while roots close to the unit circle result in slow response.

As an illustration of the analysis, consider a system with F(s) of the form

$$F(s) = \frac{k}{s\tau + 1} \tag{3}$$

Although the combined transfer function of the power amplifier, filter and motor is typically of the third and fourth order, Equation (3) is valid only an approximation for mechanical time constant of the motor is often the dominant factor.

The resultant open-loop transfer function is

$$H(s) = \frac{C}{s(s\tau + 1)} \tag{4}$$

where

$$C = \frac{n\ k\ T\ V_s}{2\Pi} \tag{5}$$

The corresponding transfer discrete transfer function is |8|

$$H(z) = \frac{Cz}{z-1} - \frac{Cz}{z - e^{-T/\tau}} \tag{6}$$

The characteristic equation becomes

$$1 + C\left|\frac{z}{z-1} - \frac{z}{z - e^{-T/\tau}}\right| = 0 \tag{7}$$

denote

$$B = e^{-T/\tau} \tag{8}$$

then characteristic equation becomes

$$z^2 + z(-1-B-BC + C) + B = 0 \tag{9}$$

The stability of the system is examined to determine the conditions under which the roots of Equation (9) will be within the unit circle. In order to determine the stability, use the transformation

$$z = \frac{\lambda + 1}{\lambda - 1} \tag{10}$$

This transforms the inside of unit circle, $|z|<|$ into the LHP of the complex variable $\lambda$, thus enabling us to apply the Routh-

Hurowitz criterion to

$$C(1-B)\lambda^2 + 2(1-B)\lambda + 2(2 + 2B + BC - C) = 0 \qquad (11)$$

In order for the roots of Equation (11) to be in the LHP, all the coefficients in Equation (11) must have the same sign. Furthermore, as (1-B) is always positive we require the last term to be positive too.

$$2 + 2B + BC - C > 0 \qquad (12)$$

This can be written as

$$C(1-B) < 2\ (1+B) \qquad (13)$$

or

$$C < \frac{2(1+B)}{1-B} \qquad (14)$$

The resulting condition for stability is

$$C < 2\ \frac{1+B}{1-B} \qquad (15)$$

Combining Equation (14) with Equations (5) and (8) gives the following explicit condition

$$k < \frac{4\Pi\ (e^{T/z} + 1)}{nV_s\ T\ (e^{T/z} - 1)} \qquad (16)$$

Equation (16) is the key to understanding the stability problems of a PLS. Since n is a large number, typically equals 500, the allowed gain is usually small.

In order to evaluate the minimum velocity of n Equation (16) may be written as follows:

$$n\, k\tau\, V_s < \frac{4\Pi\tau\,(e^{T/\tau} + 1)}{T\,(e^{T/\tau} - 1)} \qquad (17)$$

Equation (17) represents a limit for $nk\tau V_s$ as a function of $T/\tau$. It is shown in Appendix C that for the range of interesting, where $T/\tau \ll 1$, this expression must be accurately approximated by

$$n\, k\tau\, V_s < \frac{8\Pi\tau^2}{T^2} \qquad (18)$$

Equation (18)sets an upper limit for T, the period of the reference signal

$$T_{max} = \left(\frac{8\Pi\,\tau}{nkV_s}\right)^{\frac{1}{2}} \qquad (19)$$

This can be translated to an equivalent motor velocity

$$\Omega_{min} = \frac{1}{nT_{max}} = \left(\frac{kV_s}{8\Pi n\tau}\right)^{\frac{1}{2}} \quad |\text{rev/sec}| \qquad (20)$$

## 2.4. SYSTEM DESIGN

In this section, we review several important problems which arise in connection with the design of PLS systems. Indeed, systems may be different, and they may have some special specifications; however, there are some basic requirements to all PLS which are discussed here. The first requirement is the system bandwidth, $\omega_B$, which determines the speed of system response to variations in input or load. This may vary between 0.1 and 300 rad/s, according to the system parameters.

The second requirement describes the range of velocities which the PLS can follow. This range is called the lock range. It is characterized by the lower limit $\Omega_L$ and an upper one, $\Omega_H$, of the motor speed measured in rev/s. The last requirement refers to the speed variations. Although this is usually the most important requirement of the PLS, there is little that can be said about it in general, except that we want to keep the speed variations as small as possible. These requirements are studied below.

### 2.4.1. PLS Bandwidth

In order to study the bandwidth of the loop, we need an equivalent continuous model for it. It is shown in Appendix B that if the sampling time, T, is much smaller than the time constant, t, the impulse sampling may be approximated by a gain

of . Accordingly, the equivalent model is as shown in Figure 2.5.

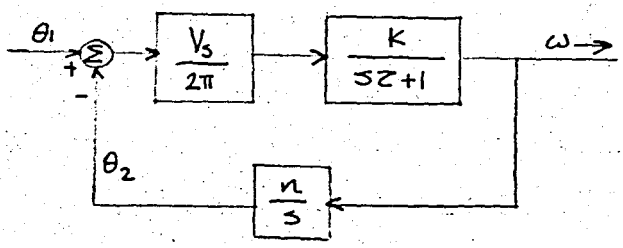



FIGURE 2.5. A Continuous Model for PLS under the Assumption $T << \tau$.

The characteristic equation of the system is given in Equation (21)

$$1 + \frac{C}{s(s\tau + 1)} = 0 \qquad (21)$$

where C, the equivalent gain is

$$C = \frac{n\ V_s\ k}{2\Pi} \qquad (22)$$

The loop poles, as derived from Equation (21), are:

$$P_{1,2} = \frac{-1 \pm j\sqrt{4C\tau - 1}}{2\tau} \qquad (23)$$

If we design the system damping to be critical,

$$P_{1,2} = -\omega_B \pm j\omega_B \tag{24}$$

This requires the gain, C, and the time constant

$$C = \omega_B \tag{25}$$

$$\tau = \frac{1}{2\omega_B} \tag{26}$$

Equation (26) indicates the first difficulty in the design. If you want to have a certain bandwidth, you must start with a motor which has the right time constant, $\tau$. Clearly, if the motor time constant is too short, one can always generate a longer time constant by a filter. Unfortunately, in most cases, $\tau$, is too long and the problem is to reduce it.

This can be done by adding a velocity feedback, a current feedback or several methods which reduce the effective time constant of the motor. Assuming that this requirement can be satisfied, we are ready to discuss the lock range problem. For simplicity, we discuss the two limits separetely.

### 2.4.2 Lower Speed Limit $\Omega_L$

It was previously shown that a PLS system will be unstable at low speeds. The design problem is to choose the parameters of the system such that it will be stable at the desired lower limit $\Omega_L$.

Recall Equation (20) and combine it with Equation (22) to give the lower speed limit

$$\Omega_{min} = \frac{1}{n} \left(\frac{C}{4\tau}\right)^{\frac{1}{2}} \tag{27}$$

Next, substitute Equations (25) and (26) in Equation (27) to give

$$\Omega_{min} = \frac{\omega_B}{n\sqrt{2}} \tag{28}$$

This relates the lower limit, $\Omega_{min}$, to the system bandwidth, $\omega_B$. It is clear from Equation (28) that if we want to lower $\Omega_{min}$, we must increqse n. However, there is a practical limit to increasing n due to cost and size. The common values of n are 500 and 1000. One can double n by sensing the zero-crossing times of the encoder signal, or increase it futher by having separate snesors, but this adds to the circuit complexity.

### 2.4.3. Upper Speed Limit $\Omega_H$

In order for the loop to follow speeds in the lock range, the gain has to be such that when the PFD output varies between the extremes, the motor speed will change the lock range. Thus, we want

$$\Delta\Omega = \frac{2V_s k}{2\Pi} \geq \Omega_H - \Omega_L \tag{29}$$

On the other hand, we can combine Equation (29) with Equations (22) and (25) to express

$$\Delta\Omega = \frac{2C}{n} = \frac{2\omega_B}{n} \tag{30}$$

Thus, once we selected $\omega_B$ and n, $\Delta\Omega$ is determined, and it may or may not satisfy Equation (29).

Note that we are concerned only with the magnitude of $\Delta\Omega$ as compared with $(\Omega_H - \Omega_L)$, and not about the actual velocities. The reason that the speed can always be shifted by adding a bias voltage to the amplifier.

The lock range problem, when $\Delta\Omega$ is obtained by Equation (30) does not satisfy Equation (29), is a serious one, and it can be solved in one of two ways. The first method is to divide the desired lock range into several bands, each being narrower than $\Delta\Omega$, as given by Equation (30). A band selector switch provides the desirable bias to the amplifier, to shift the speed to the desired band, and the PFD can vary the speed within the band. While this solution is relatively simple, it is not acceptable in cases where a continuous speed variation is required. In those cases, one can use the second method. This method is based on the idea of keeping F(s) to be the same as in Equation (3) in the range of frequencies which affect stability, but increase the low frequency gain by the addition of

lag-lead network G(s) of the form

$$G(s) = \frac{s + ma}{s + a} \qquad (31)$$

The lag frequency, a, is selected to be much smaller than $\omega_B$. Consequently, $G(s) \approx 1$ for frequencies about $\omega_B$. So the actual filter transfer function, $F_1(s)$, equals

$$F_1(s) = G(s)\, F(s) = \frac{s + ma}{s + a} \quad \frac{k}{s\zeta + 1}$$

The bode plots of $F(j\omega)$ and $F_1(j\omega)$ are shown in Figure 2.6.

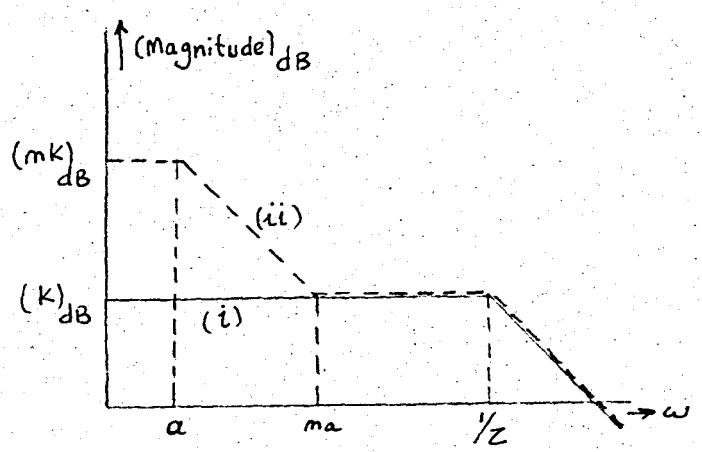



FIGURE 2.6. Bode Plot of the Original Function, $F(j\omega)$, Curve (i); Curve (ii) the Compensated Function $F_1(j\omega)$.

Note that at higher frequencies, the two functions are actually the same. On the other hand, the dc gain of $F_1(s)$ is

is $F_1(0) = mk$ whereas $F(0) = k$. Thus, the lag-lead network allows a gain increase in $\Delta\Omega$. This allows us to extend $\Delta\Omega$ as much as necessary, so the lock range is limited on the lower end by $\Omega_{min}$, and on the higher end by the maximum allowed velocity of the motor, or by the amplifier saturation voltage.

# CHAPTER 3

# THE IMPLEMENTATION

In this chapter, the design of a thyristor firing angle generator which uses a pulse width modulator to convert the analog error voltage into the digital word and the associated circuitry to make up a complete system are described. The digital word is translated into the timing of a thyristor trigger pulses so as to provide proportional control of the dc component of the load voltage.

Figure 3.1 shows the block diagram of the complete speed control system. The system employs digital phase locked loop control where the motor speed is controlled in precision with a command from a reference frequency. An auxiliary PLL frequency synthesizer is also provided to generate line synchronized clock pulses for the reference wave of the converter.

The speed of the motor is measured with a digital tachometer which consists of a slotted disk mounted on the rotor

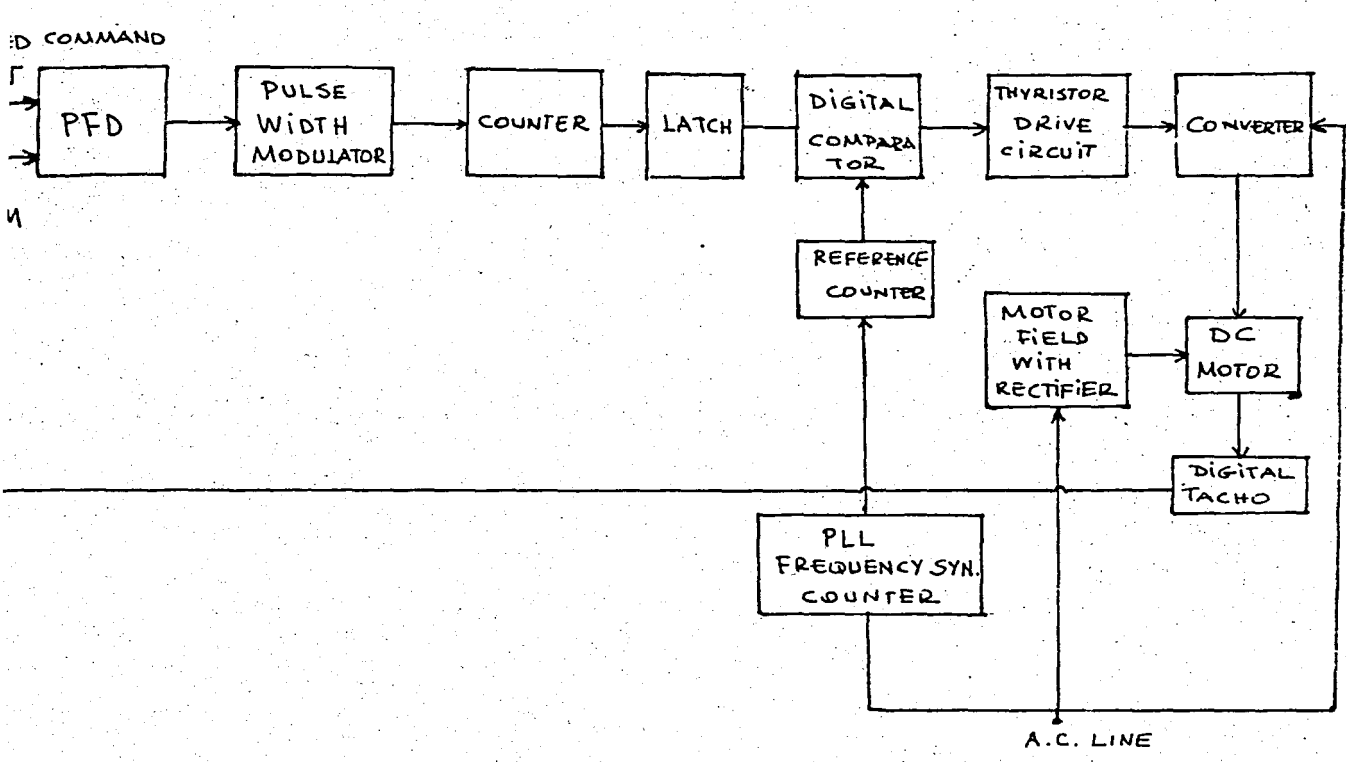



FIGURE 3.1. Control System Block Diagram.

shaft and opto-interruptur sensor. A Schmitt trigger is used to produce a square pulse from the photo detector assembly output.

The speed command frequency $f_R$ and the actual speed frequency $f_M$ are compared in PFD to generate a frequency and phase-sensitive error for actuating the converter. The present circuit used the MC4344 type PFD which has error characteristic as a function of phase difference Ø and is shown in Figure 3.2.

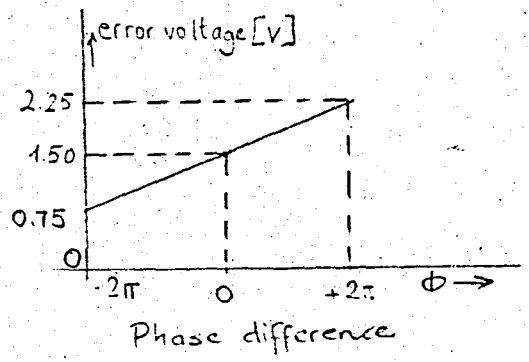



FIGURE 3.2. Error Characteristic of PFD MC4344.

## 3.1. PLL FREQUENCY SYNTHESIZER

The function of PLL frequency synthesizer is to generate line-synchronized clock pulses for the reference wave of the converter. In the analog control system, the reference wave is derived from the ac supply. The distortion and transients in the main ac supply cause changes in the reference signal waveform. This effects the timing of trigger pulses. PLL frequency synthesizer circuit produces a firing pulse for the thyristor at the same point on the mains cycle, regardless of the variation in the mains frequency.

A block diagram of frequency synthesizer is shown in Figure 3.3. It generates an output frequency $f_o = Nf_i$ which can be programmed either by varying the input frequency $f_i$ or by setting the modulus N of the counter. Essentially it is a digital feedback system in which the reference frequency and

feedback frequency are compared in the phase-frequency and analog error signal, proportional to the phase difference of the input waves, is generated at the output of the loop filter. The amplified error signals actuates a voltage controlled oscillator (VCO) to generate the desired frequency. If the output wave tends to fall back in phase (or frequency), the error voltage builds up to correct the VCO output such that the reference and feedback waves always lock together in phase under stable condition.

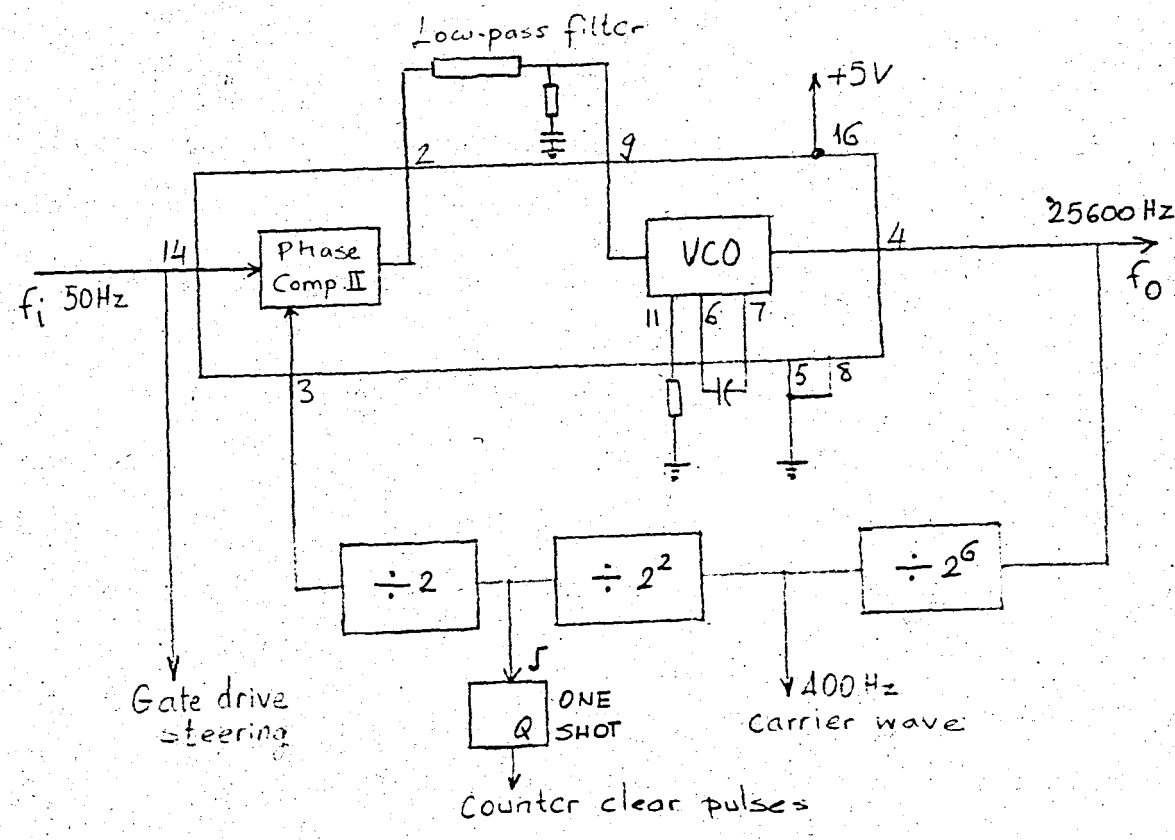



FIGURE 3.3. Phase Locked Loop Frequency Synthesizer.

In this circuit, PLL system can function as a frequency-selective frequency multiplier. When a frequency divider or counter is inserted into the feedback loop between the VCO output and the comparator input. In the circuit of Figure 3.3 an external frequency divider consisting of CD 4040.

Phase Comparator II of MC 4344 is used in this application because it will not lock on harmonics of the signal input reference frequency.

## 3.2. PULSEWIDTH MODULATOR

PFD generates an analog error voltage which is proportional to the difference in frequency or phase between the inputs. This error voltage is converted to digital error word in pulse-width modulator shown in Figure 3.4(a) and (b).

The comparator requires two input signals. One signal is a triangular wave of fixed frequency and amplitude. The other signal is a variable dc voltage that comes from a phase-frequency detector. Operation is shown in Figure 3.5.

In situation 1, the direct voltage is higher at all times than the triangular wave level, and the output is a continuously high signal.

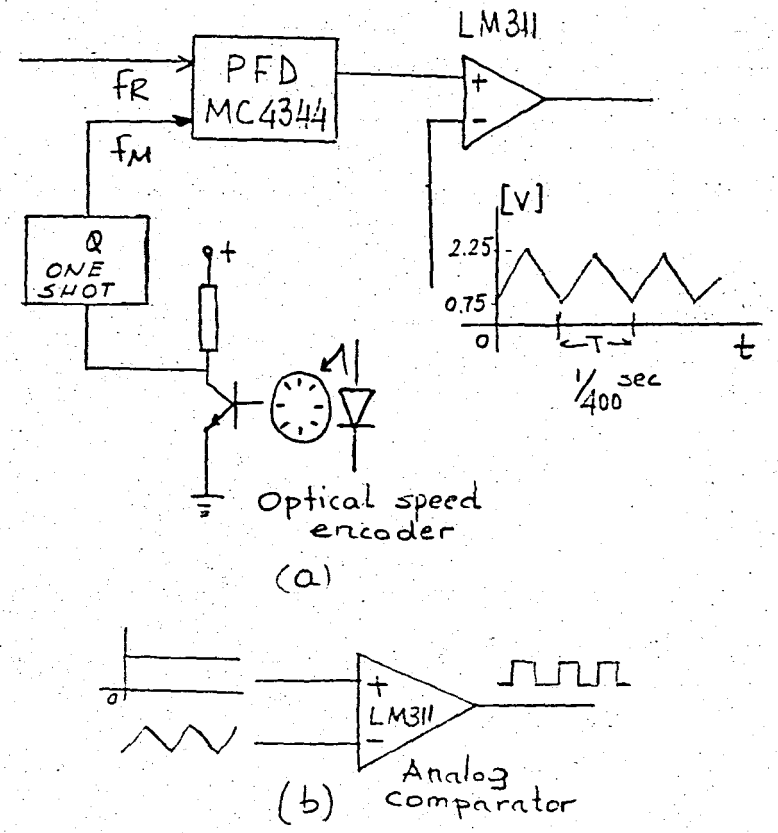



FIGURE 3.4. The Basic Explanation of the Pulsewidth Modulator.

In situation 2, the triangular wave exceeds the dc input for only a very short period, and thus produces a narrow, low volatage pulse on the output waveform. In situation 3, the dc level is below the average triangular wave. Thus, the low period of the output signal is greater than the high period. In situation 4, the reference level is below the triangular wave level in all times, thus giving low comparator output. The comparator circuit can control pulse widths from full-on to full-off.

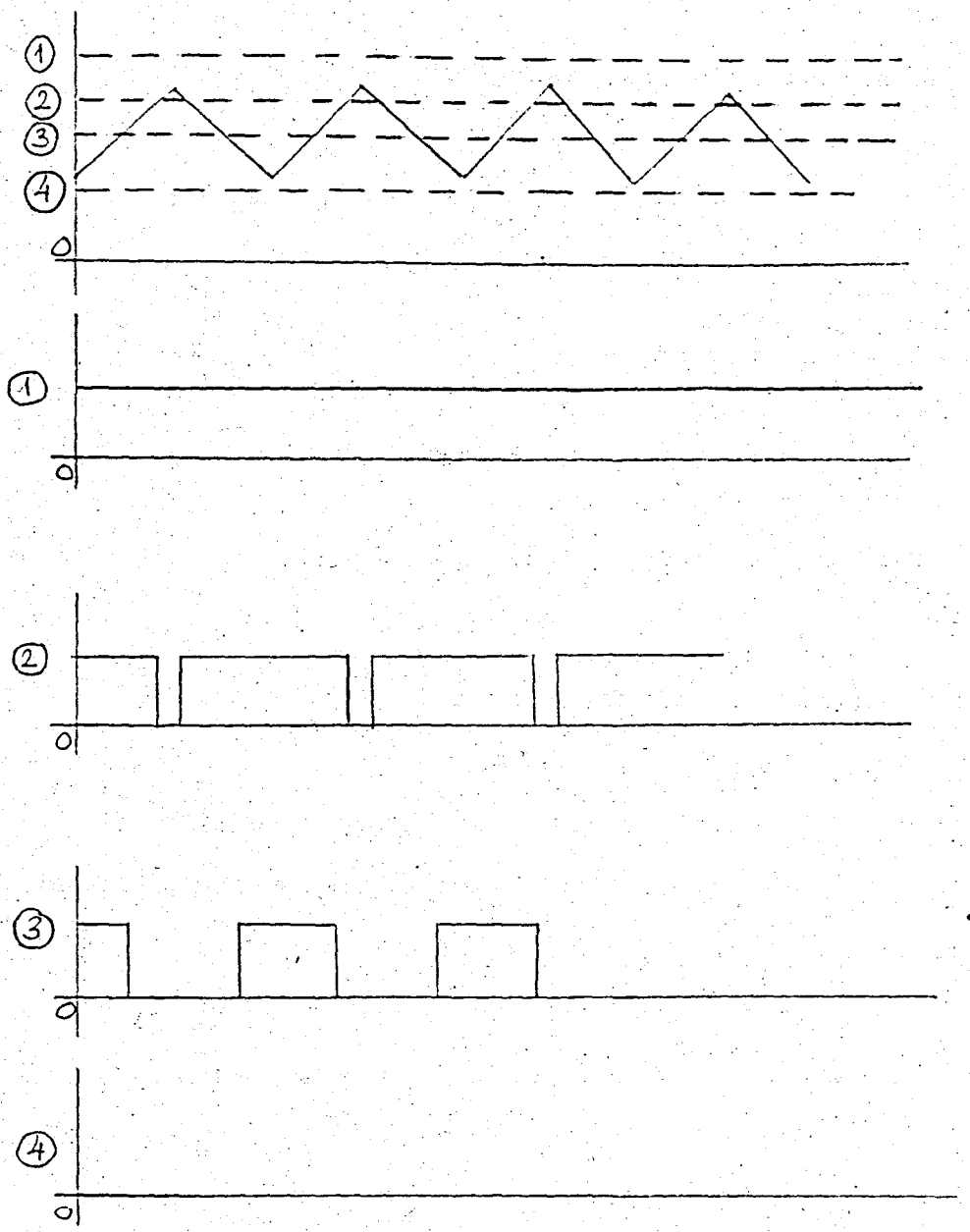



FIGURE 3.5. The Operation of the Pulse-Width Modulator.

The triangular wave is derived from one of the PLL frequency synthesizer outputs, (400 Hz carrier). A 400 Hz square wave which is derived from PLL is integrated to transform to a triangular wave and is then biased such that its maximum and minimum values correspond to these of the error voltage.

Figure 3.6 shows the generation of triangle wave from square wave.

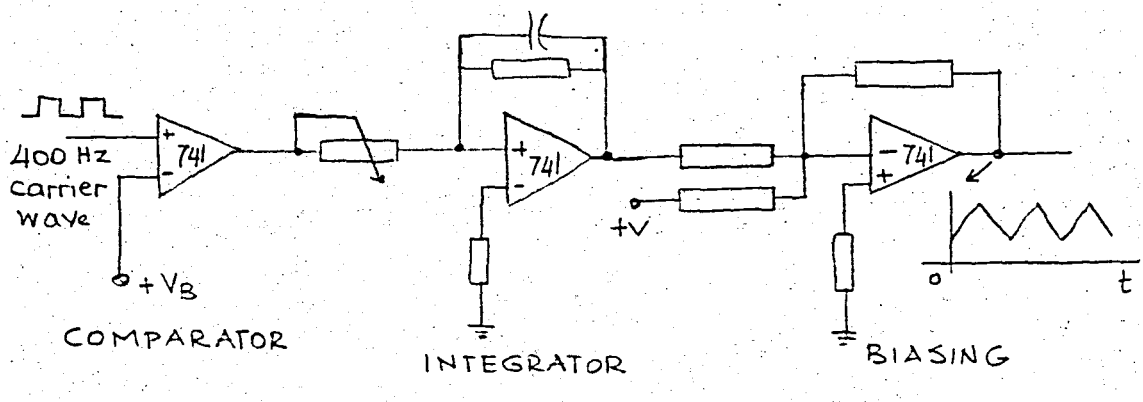



FIGURE 3.6. The Generation of Triangle Wave from Square Wave.

The analog signal (the output of the PFD) is compared to the triangular carrier wave and the output gates an oscillator. The pulse train is counted on a counter which corresponds to a digital word. At the trailing edge of the pulse train, monostable pulses load the counter content to the latch and clear the counter in sequence.

The error signal in the latch is refreshed four times every half.cycle of line wave and is compared to the reference counter. The thyristor firing pulses are generated at the crossover points. Figure 3.7 explains its waveforms.

The details of the pulsewidth modulator circuit are shown in Figure 3.8.

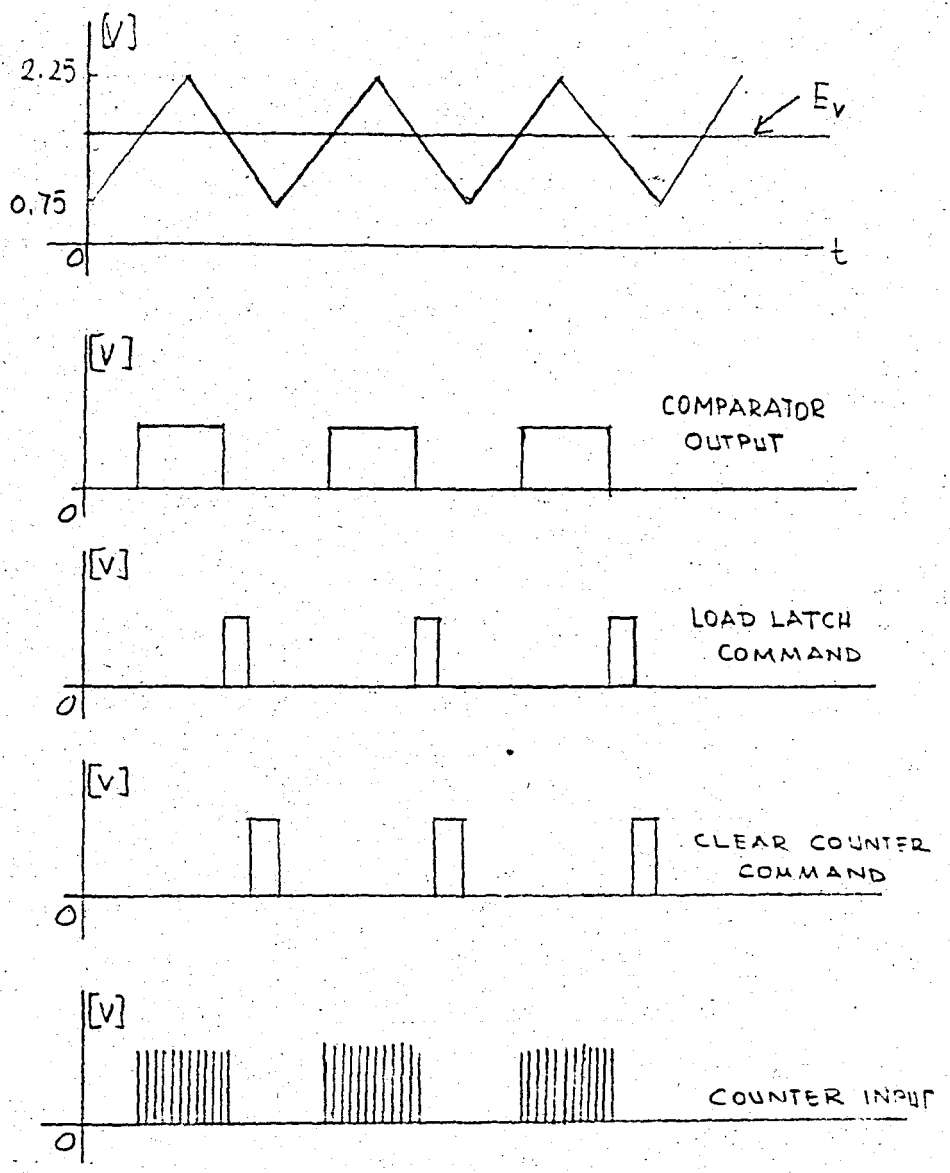



FIGURE 3.7. Pulsewidth Modulator Waves.

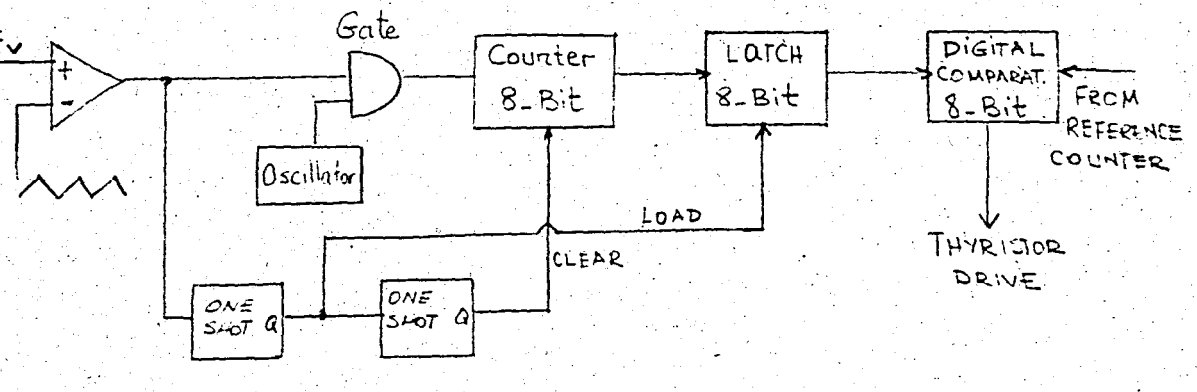



FIGURE 3.8. Complete Circuit of PWM.

In this circuit, error word is modified four times every half-cycle of line wave. Latch is used for storing these four values. The binary comparator compares the counter and the latch outputs and generates a pulse at the crossover point which corresponds to the delay angle.

The reference counter curcuit waveforms are shown in Figure 3.9.

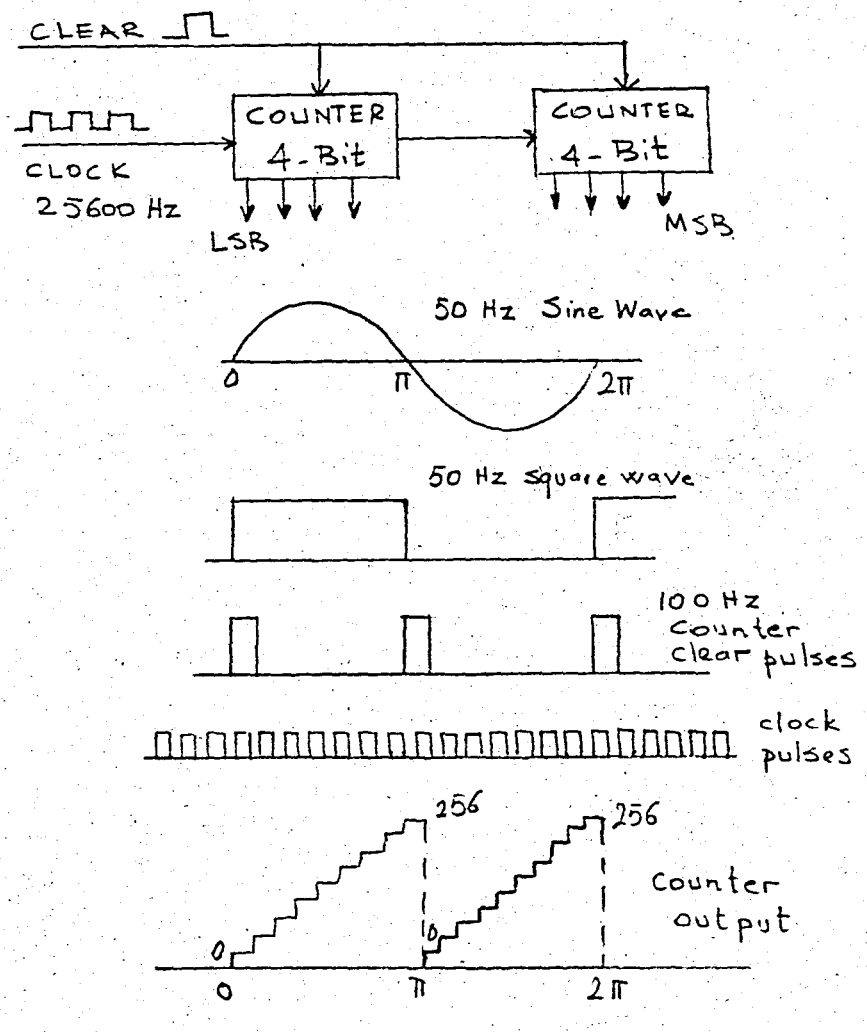



FIGURE 3.9. The Reference Counter.

## 3.3. THYRISTOR DRIVE CIRCUIT

The output of the comparator extends from $\alpha_1$ to II. This output is gated by a pulse train from an oscillator. These pulses are coupled to the steering circuit. The steering circuit directs firing pulses to the SCR's which have positive anodes, i.e., $Q_1$ and $Q_2$ in the positive half cycle and $Q_3$ and $Q_4$ in the negatif half-cycle.

The details of the thyristors drive circuit are shown in Figure 3.10.

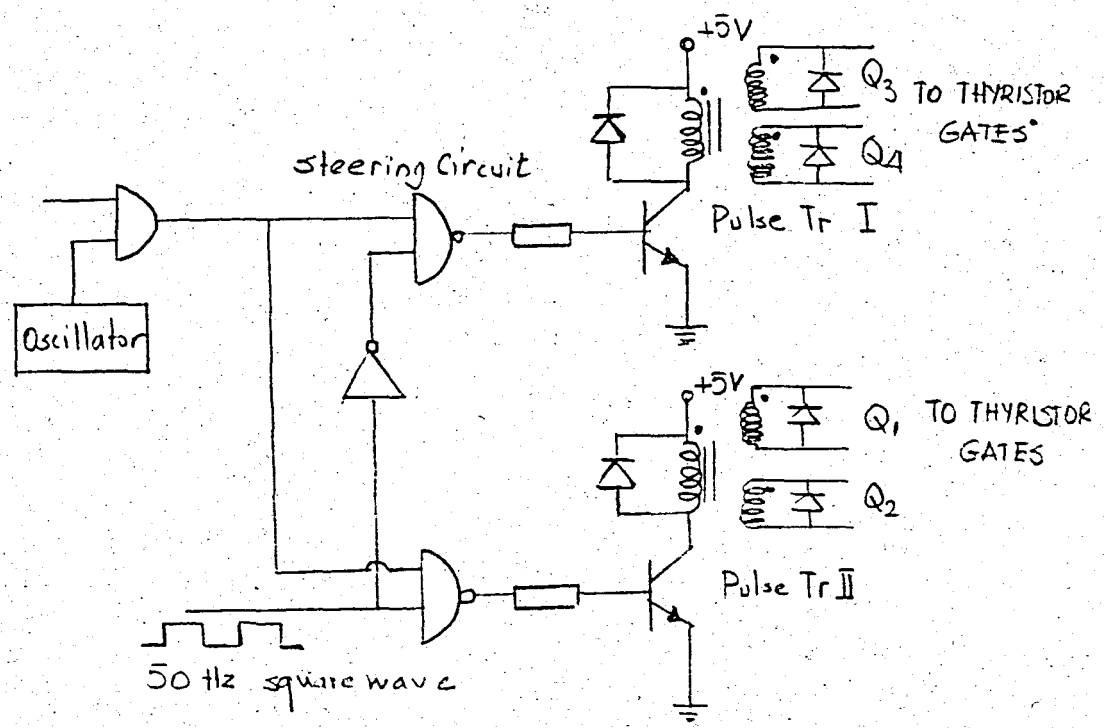



FIGURE 3.10. Thyristor Drive Circuit.

## 3.4. CONVERTER

Converter regulates the amount of power transferred from an ac supply to a dc load. D.C. motors controlled by thyristor converters have become the most popular form of industrial variable speed drive. The thyristor converter has the advantages of high reliability, efficiency and power gain coupled with its small size and fast response.

The speed control system described in this thesis employs a single phase full-bridge converter and is shown in Figure 3.11.

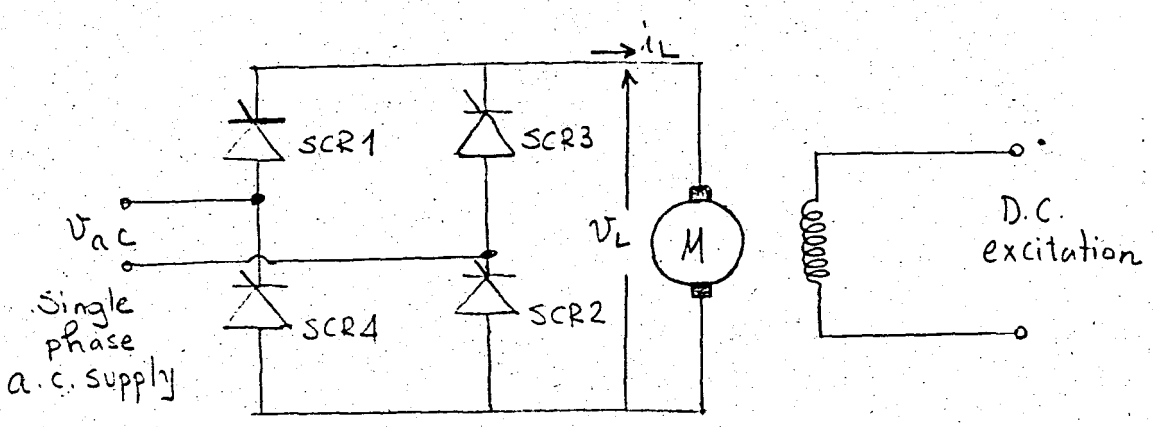



FIGURE 3.11.

The field current supplied through a diode bridge rectifier, is maintained constant but can be reversed for speed reversal of the motor.

The basic principle of the single phase bridge converter can be explained as follows: The load impedance can be a pure resistive load or a resistive inductive load (for example motor). Figure 3.12 shows the ac source voltage waveform. Figure 3.13 shows the load voltage waveform for a pure resistive load.

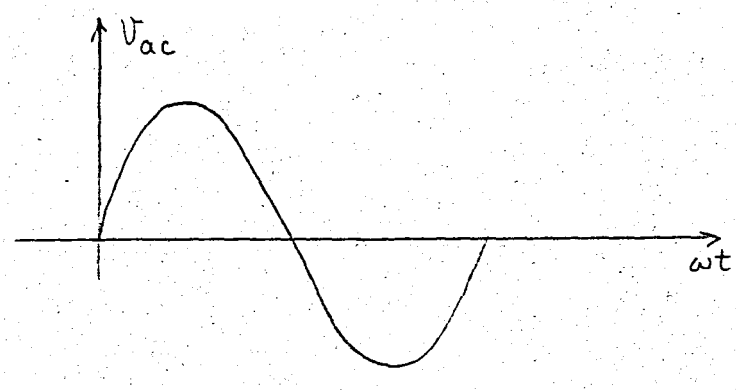



Fig 3.12 a.c. source voltage waveform

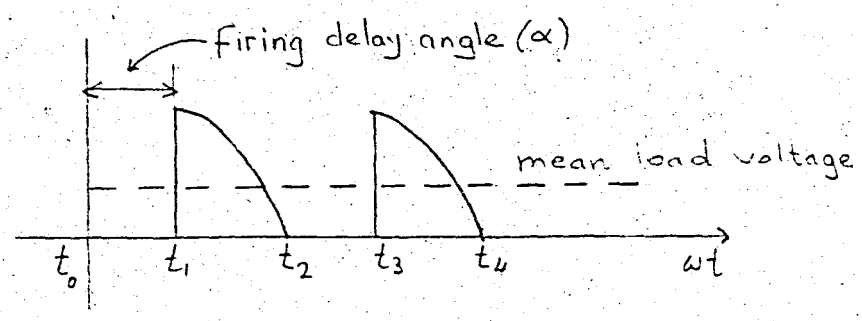



Fig. 3.13. Load voltage waveform

At time SCR's 1 and 2 are turned on simultaneously, and the voltage supplied to the load is the ac source voltage less the device voltage drops. At time $t_2$ SCR's 1 and 2 are reversed biased and turn off and load current ceases. At time $t_3$, SCR's 3 and 4 are turned on and even though the ac source voltage has reversed, the voltage applied to the load has the same polarity as when SCR's 1 and 2 are conducting. That is, the load voltage is unidirectional, and has a mean amplitude $V_{d\alpha}$. The interval $t_o$ to $t_1$ is known as the firing delay angle .

Increasing the firing delay angle $\alpha$ reduces the mean output voltage, as is shown in Figure 3.14.

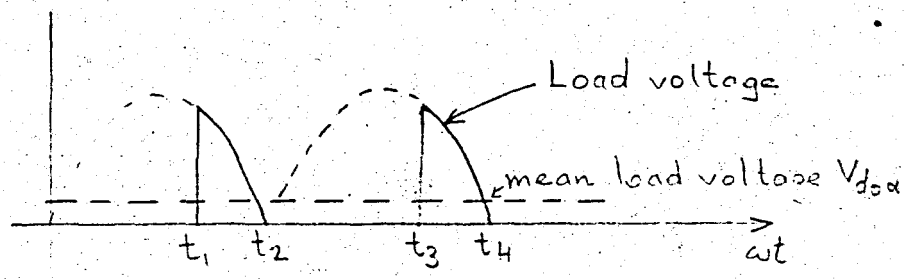



FIGURE 3.14.

By varying the firing delay angle $\alpha$ from 0 degree to 180 degree the mean output voltage is varied from its maximum to zero.

In this study, the converter uses the digital version of

cosine wave corssing method. As we know, the cosine wave crossing method is commonly used for generating gate firing signals of the thyristors. A conventional method consists of comparing a cosine wave generated from an synchronized to the a.c. source, with a variable d.c. reference voltage by means of a comparator as shown in Figure 3.15.

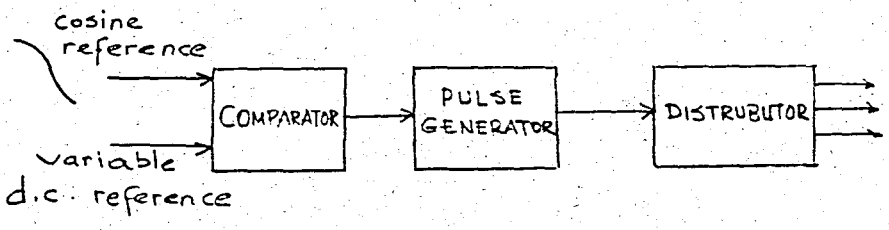



FIGURE 3.15. The Concept of Cosine-Crossing Firing Control.

As the amplitude of the d.c. reference signal is varied the point of intersection with the cosine timing curve will vary, and a firing signal can be generated corresponding to the point of intersection and a result the firing delay angle can be varied as desired. However, unless the d.c. reference signal is varying, the mean output voltage will remain constant.

In the digital version of the method, cosine reference wave is the output of the reference counter. This output is approximately ramp function. The ramp function defines the timing of the firing pulse in the point of intersection with the 8-bit control input. The intersection is done is the digi-

tal comparator. The output of the digital comparator drives the thyristor drive circuit. The control method of firing pulses in the converter is shown in Figure 3.16 (a) and (b).

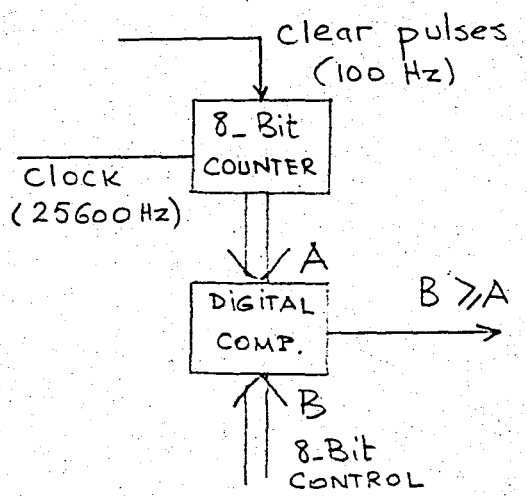



FIGURE 3.16(a). The Block Diagram of the Timing of the Firing Pulses.

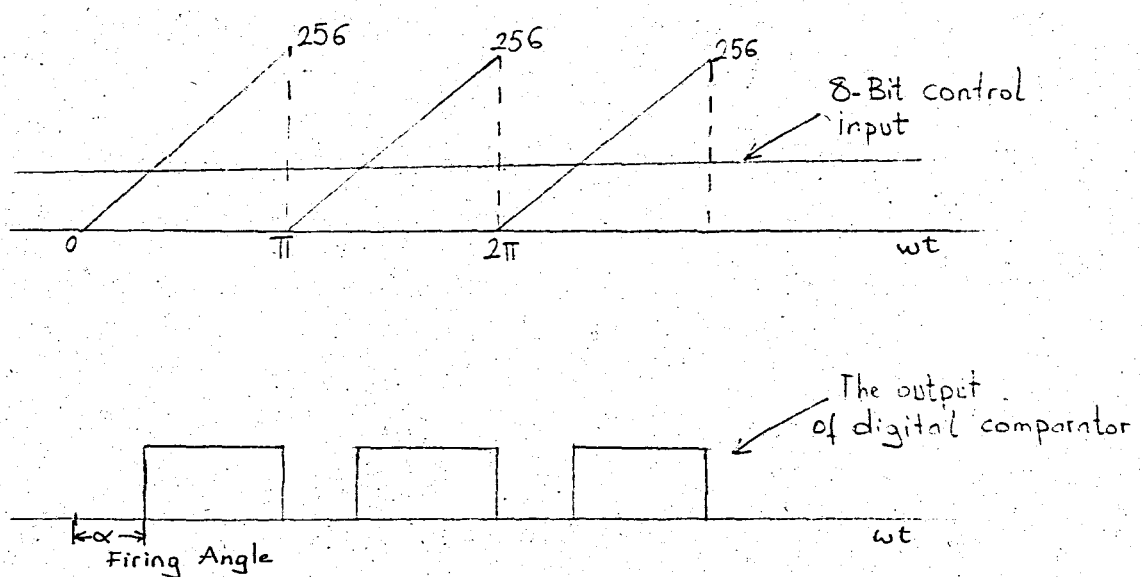



FIGURE 3.16(b). The Waveforms of the Timing Firing Pulses.

## 3.5. AN ALTERNATIVE METHOD TO THE TIMING OF FIRING PULSES

In application where the linear relationship between the average voltage and the control input is desired, EPROM can be used. The delay angle in our proposed circuit was proportional to the control input. In this case, we have a non-linear relationship between the average voltage and the control input. By adding a PROM, the depay angle can be made proportional to the arc-cosine of the control input. PROM is programmed to convert the linear digital ramp to a cosine ramp to the counter output.

The block diagram and waveforms of this approach is shown in Figure 3.17 (a) and (b).

## 3.6. DIGITAL TACHOMETER

Digital tachometer is the optical speed encoder. The disc is shown in Figure 3.18(a) and the complete assembly for measuring rev/sec (revolution per second) is shown in Figure 3.18(b).

Assume that the total number of holes, evenly spaced around the circumference of the disc as shown, is N. For every complete revolution, N holes will pass through the pickup head, consisting of the light source and the photo sensor. The number

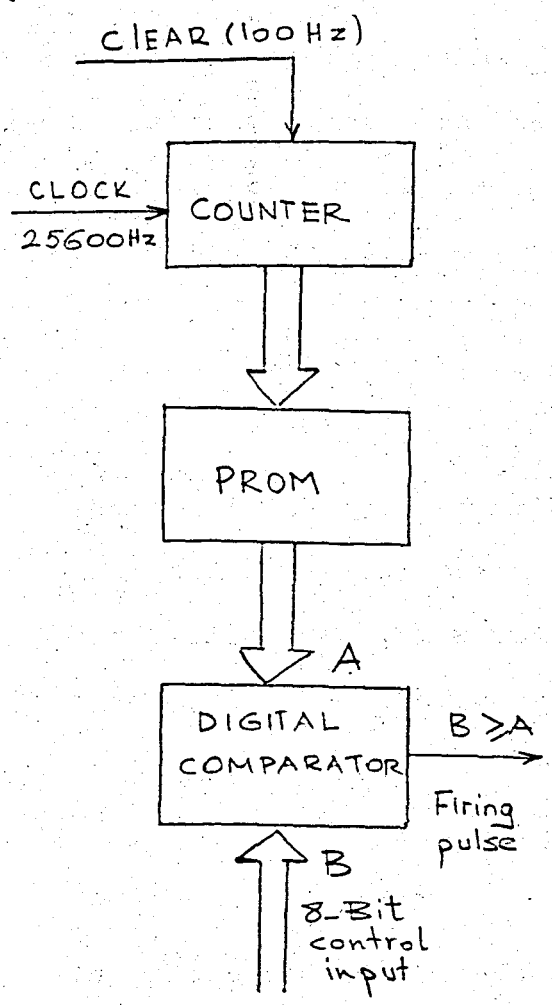



FIGURE 3.17(a). The Block Diagram.

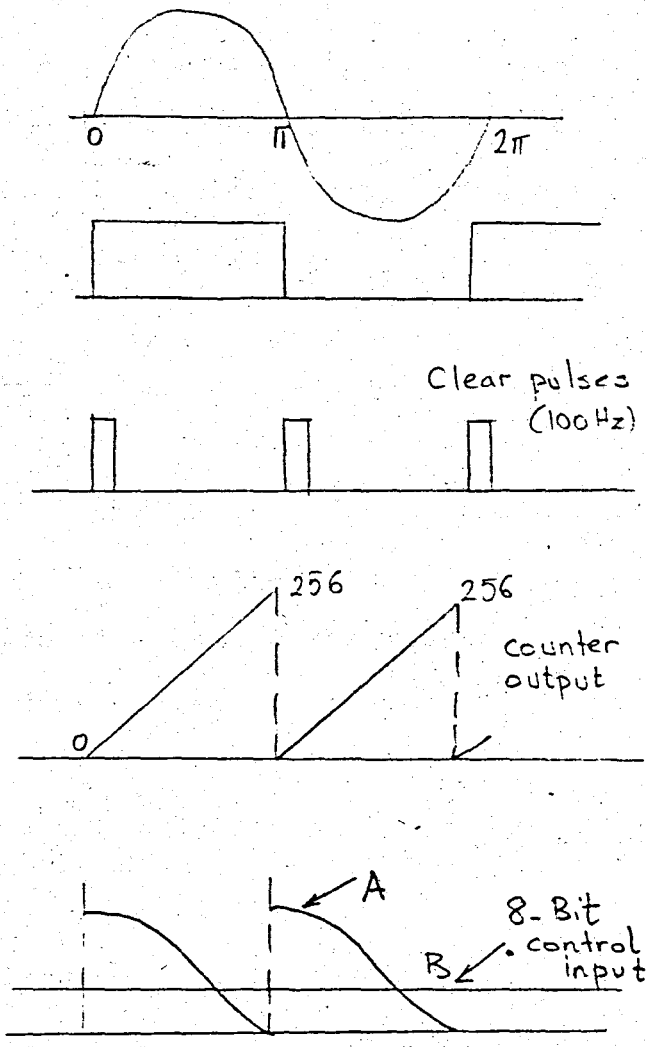



Figure 3.17(b). Waveforms.

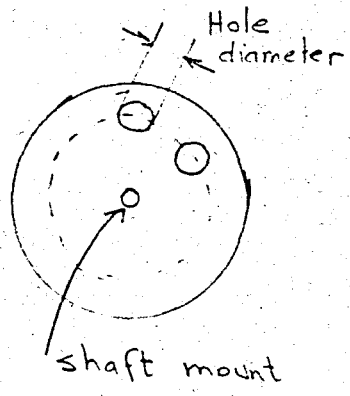



FIGURE 3.18(a). Photo Disc.

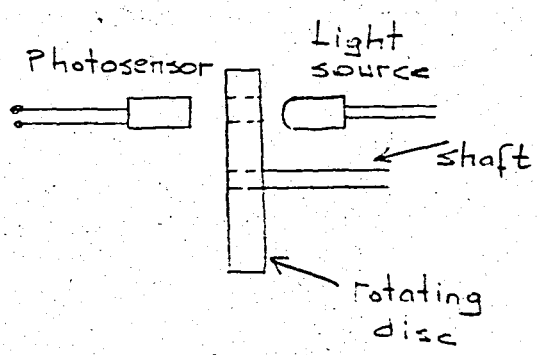



Figure 3.18(b). Basic Assembly.

of holes passing the head in 1 second is a direct measure of the speed of rotation, rev/sec = n/N. One electrical cycle consists of a hole and space. The optical speed encoder generates a pulse train of frequency equal to

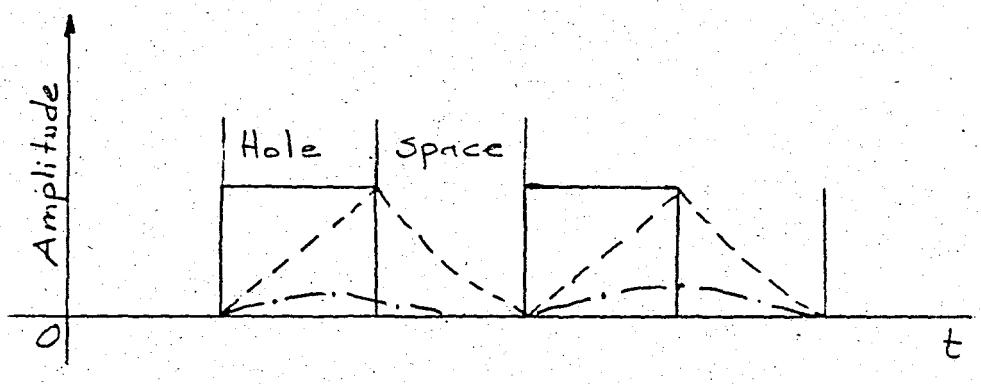
$$f_m = \frac{N \cdot \omega_m}{2\Pi}$$

where N is the number of holes on the perimeter of the encoder disc and $\omega_m$ is the motor speed (radian/second). Since the motor shaft encoder angular position is equal to the integral of its speed, the encoder transfer function can be expressed to

$$H_t(s) = \frac{\theta_m(s)}{\Omega_m(s)} = N/s$$

The photo sensor will be selected to yield a waveform as shown in Figure 3.18(c). The rise time of the sensor must be such that the signal will reach about full value during the time the photo sensor is exposed to the light source as a hole passes through the head. The fall time must permit a substantial decay to the dark state during the time a space passes through the head.

The pulse train which generates digital tachometer is shaped through a Schmitt trigger and fed to the phase-frequency detector input.




——— Ideal waveform

------- Slow response - acceptable

—·—·—·— Very slow response - unacceptable

FIGURE 3.18(c). Electrical Waveforms.

# CHAPTER 4

## 4.1. DIRECT CURRENT MOTOR

The ratings of the d.c. motor used are 3/4 KW, 125V, 6A and 1450 rpm. Starting from the differential equations governing the operation of a separately excited d.c. motor with constant field excitation, the transfer function is developed. Equations are simplified by making the following assumptions:

1. The static friction is negligible.
2. Armature reaction is negligible.
3. The armature resistance and inductance can be regarded as constant.
4. Armature inductance is much larger than the source inductance.
5. Brush and thyristor voltage drop is negligible.

With these simplifications and assumptions the following set

of differential equations are obtained:

$$V = L_a \frac{di_a}{dt} + R_a i_a + E$$

$$J = \frac{dw}{dt} = T - T_L$$

$$E = K_E \cdot W$$

$$T = K_T i_a$$

Assuming all initial conditions are zero and taking Laplac transforms, we obtain the following block diagram:

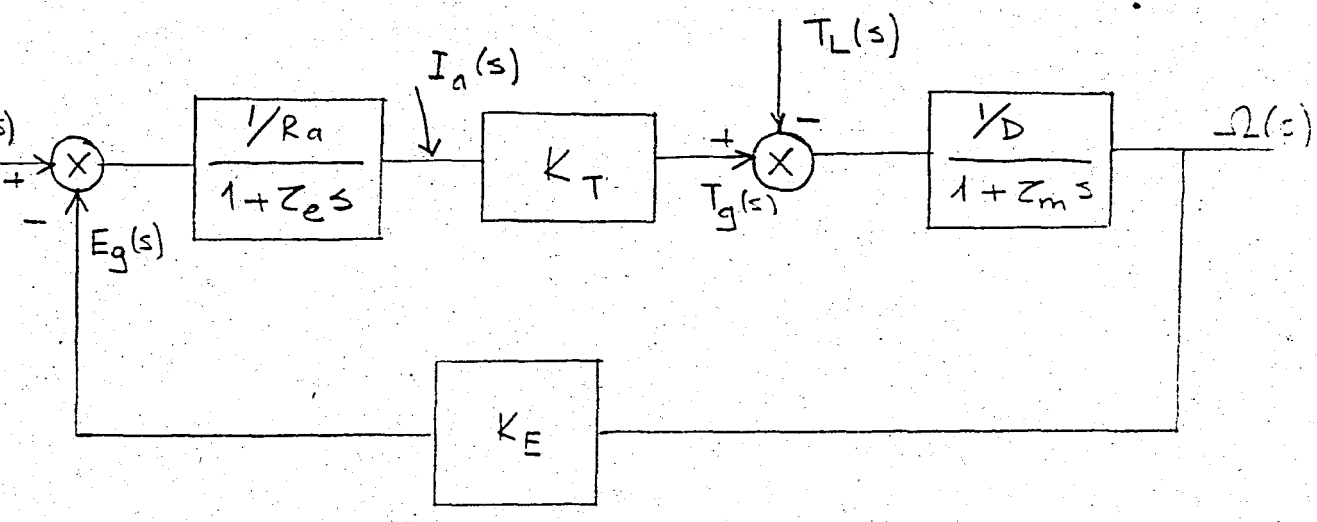



Fig. 4.1.1

The motor transfer function for $T_L = 0$ can be expressed as

$$H_m(s) = \frac{\Omega(s)}{V(s)} = \frac{k_T}{(R_a + L_a s)(D + Js) + k_E k_T}$$

where $R_a$, $L_a$, J, D, $k_E$ and $k_T$ are motor parameters. For most cases, the motor electric time constant $\tau_e = L_a/R_a$ is negligible compared to the mechanical time constant $\tau_m = J/D$, so that the motor transfer function can be written as

$$H_m(s) = \frac{k_T}{R_a J s + k_E k_T + R_a D} = \frac{k_T}{R_a J} \frac{1}{s + 1/\tau_{m1}}$$

where

$$\tau_{m1} = \frac{R_a J}{k_E k_T + R_a D}$$

If the viscous friction torques are neglected (D = 0) the motor transfer function becomes

$$H_m(s) = k_m \, 1/(s + 1/\tau_{m1})$$

where

$$k_m = 1/k_E \tau_{m1}$$

By substituting experimentally determined circuit and motor parameters (Appendix D)

$$k_m = \frac{1}{k_E \, \tau_{m1}}$$

$$\tau_{m1} = \frac{R_a \, J}{k_T k_E} = 0.45 \text{ sec.}$$

$$k_m = \frac{1}{1 \cdot 0.45} = 2.22 \quad \text{Motor gain constant}$$

$$H_m(s) = \frac{2.22}{s + 2.22}$$

## 4.2. EXPERIMENTAL RESULTS

In Chapter 2, it was found that the stability of the PLS is related to the system gain K. The relation was

$$K < \frac{4\Pi\,(e^{T/\tau} + 1)}{nV_s T(e^{T/\tau} - 1)}$$

If the speed is lowered further, instability may result and it is desirable to define these limits analytically. It is obviously difficult to evaluate a limit on T in this expression in closed form. For a specific speed, this expression can be solved for the maximum stable gain and such results are presented in Table 1.

Referring to Figure 4.11., the sampling rate T is speed dependent and its expression is:

$$T = \frac{1}{n \cdot \Omega} \quad |\text{sec}|$$

n - the number of holes in speed encoder |Hz/rev/sec|

$\Omega$ - the speed of the motor |rev/sec|.

TABLE 1

Stability Limit of Gain for a Specific Speed

| Speed (rpm) | Maximum Stable Gain |
|---|---|
| 5 | 5 |
| 10 | 20 |
| 20 | 80 |
| 30 | No limit |
| 40 | No limit |

The system gain K is measured for a specific operation point. This value is 100.

For a system gain K = 100

$$\Omega_{min} = \left(\frac{K\ V_s}{8\Pi n x \tau}\right)^{\frac{1}{2}} = \left(\frac{100 \cdot 0.75}{8\Pi x 48 x 0.453}\right)^{\frac{1}{2}} = 22 \text{ rpm}$$

$$\text{Lock range} = \frac{KV_s}{\Pi} = \frac{0.75 \times 100}{3.14} = 1433 \text{ rpm.}$$

Experimental results obtained with a prototype system intended for a separately excited 3/4 KW d.c. motor are given below:

$$\Omega_{min} \cong 15 \text{ rpm}$$

$$\text{Lock range} \cong 700 \text{ rpm}$$

The reason for these results can be explained by the fact that the approximate model developed previously is no longer valid for high speeds.

An alternator supplying a resistance bank was used as a load for the motor. Therefore, the load torque is proportional to the motor speed.

With heavy loads and at high speeds, synchronous control was obtained with predicted performance. However, with light loads and at low speeds, speed hunting was observed. When this happens, the motor speed oscillates about the desired value with a noticeable amplitude. It was observed that with light loads the motor armature current was discontinuous. This can be explained by the fact that the approximate model developed is no longer valid for discontinuous motor current operation. Another reason for this is the mechanical errors in the speed encoder. Mechanical irregularities in the encoder produce an error which is applied to the phase detector. If the frequency of this error is out of the system bandwidth, it will not cause speed variations. However, when the error frequency is sufficiently low, speed disturbances result. Further study is therefore needed to better predict system behaviour for this condition and to eliminate the speed hunting problem.

Motor is loaded by a d.c. generator feeding a resistive

load from no load to full load torque of 5.5 N.m.

Performance of the system to step change in load torque from 1 N.m to 2 N.m is shown in Figure 4.1.

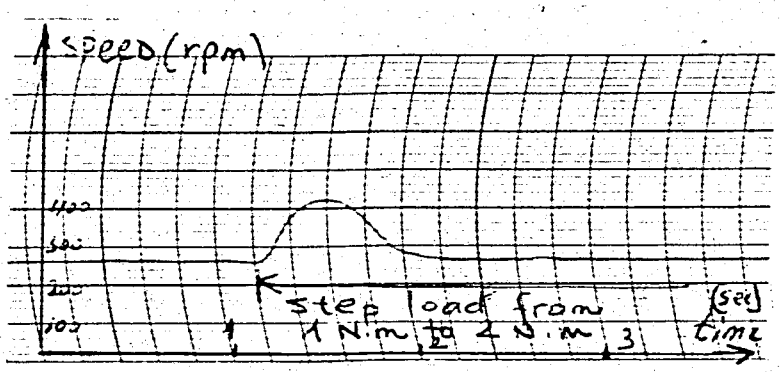



FIGURE 4.1. Load Torque Change from 1 N.m to 2 N.m.

Response of the system to a step change in trigger angle or step change in applied voltage is shown in Figure 4.2.

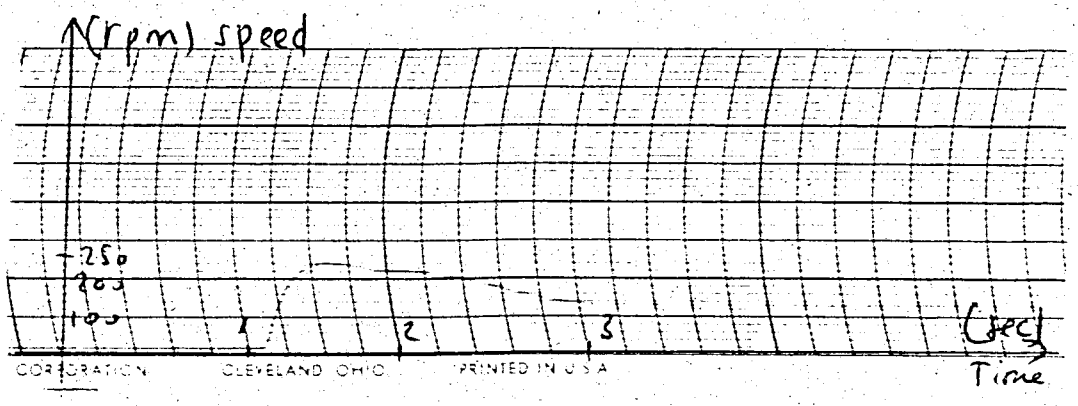



FIGURE 4.2. Step Change in Applied Voltage.

## 4.3. CONCLUSIONS

A digital speed control has been described in this thesis which provides the advantages of freedom from drift and offset errors, immunity of the control from transients and distortion of supply voltage, and permits integration of the control circuit. In addition, phase locked loop (PLL) control is provided which permits speed control with high degree of precision.

A complete speed control system employing a d.c. separately excited 3/4 KW motor has been described and analysed. Although the actual system is a nonlinear sampled data one, a linear sample data model developed represents the system performance accurately. However, in experiments carried out it was seen that the lock range was lower than predicted and speed hunting was experienced especially under light load conditions. These could be due to discontinuity in the armature current and to non-linear gain of the power amplifier which was assumed to be linear. The speed encoder mechanical irregularities also might be the cause of these problems. With 48 holes used, the range frequencies which the filter needs to act upon is very large and it is difficult to design a filter with constant gain throughout the range. The use of professionally produced encoders giving up to 1000 pulses per revolution is bound to improve the

system performance.

In spite of the above shortcomings, the advantages obtained with respect to accuracy, synchronization capability for sectional drives, low cost and integrated nature of the circuit justifies further work on the subject preferrably with a three-phase fully-controlled bridge using digital cosine wave crossing method to obtain a linear gain.

# APPENDIX A

## LINEARIZED MODEL FOR PFD

The objective of this section is to derive a linearized model for the PFD under locked condition and constant reference frequency.

Assume, with no losses of generality, that the reference signal leads the feedback. The output x of the PFD will be $V_s$ during the time interval between the leading edges $s_1$ and $s_2$ as illustrated in Figure A1.

The phase $\theta_1$ and $\theta_2$ of $s_1$ and $s_2$, respectively are:

$$\theta_1(kT) = 2\Pi k \tag{A1}$$

$$\theta_2(kT + t_k) = 2\Pi k \tag{A2}$$

Denote

$$\theta = \theta_1 - \theta_2 \tag{A3}$$

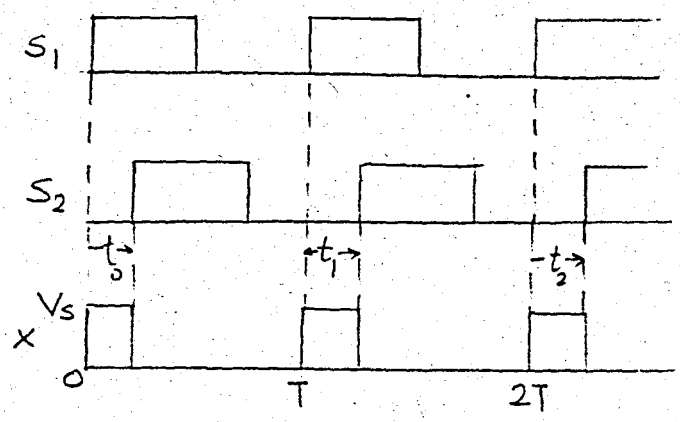



FIGURE A1. The Input $s_1$ and $s_2$ of PFD and the Output x.

The PFD output is

$$x = \begin{cases} V_s & kT < t \leq kT + t_k \\ 0 & \text{elsewhere} \end{cases} \qquad (A4)$$

Now suppose that the system operates around a nominal value of $\theta$, but that some small variations occur. Thus, $\theta$ will become $\theta + \delta\theta$.

$$\theta \rightarrow \theta + \delta\theta \qquad (A5)$$

Since the reference frequency is constant, (A5) can occur only if a change occurred in $\theta_2$:

$$\theta_2 \rightarrow \theta_2 - \delta\theta \tag{A6}$$

This will result in a change in the duration of the output pulses,

$$t_k \rightarrow t_k + \delta t_k \tag{A7}$$

and a change in the output

$$x \rightarrow x + \delta x \tag{A8}$$

The method to be used here is to determine the relationship between $\delta x$ and $\delta\theta$. This relationship constitutes the linearized model of the system. Note that the new pulse durations are such that (A2) must hold. Thus,

$$\theta_2(kT + t_k + \delta t_k) - \delta\theta(kT + t_k + \delta t_k) = 2\Pi k \tag{A9}$$

Since $\delta\theta$ and $\delta t$ are very small, we can expand (A9) by the Taylor series and retain the first order terms.

$$\theta_2(kT + t_k) + \frac{d\theta_2}{dt}(kT + t_k)\delta t_k - \delta\theta(kT + t_k) = 2\Pi k \tag{A10}$$

Simplify according to (A2), and note that

$$\frac{d\theta_2}{dt} = \omega \tag{A11}$$

Equation (A10) becomes

$$\omega(kT + t_k)\delta t_k - \delta\theta(kT + t_k) = 0 \tag{A12}$$

$$\delta t_k = \frac{\delta\theta(kT + t_k)}{\omega(kT + t_k)} \tag{A13}$$

Since the frequency is nearly constant, we can write

$$\delta t_k = \frac{1}{\omega}\ \delta\theta(kT + t_k) \tag{A14}$$

Then the resulting change in x is a pulse of duration $\delta t_k$.

$$\delta x = \begin{cases} V_s & kT + t_k < t \leq kT + t_k + \delta t_k \\ 0 & \text{elsewhere} \end{cases} \tag{A15}$$

Since $\delta t_k$ is very small, we can approximate the series of pulses of (A15) by a series of impulses of the same area. Note that the area, A of each pulse is:

$$A = V_s\ \delta t_k = \frac{V_s}{\omega}\ \delta\theta(kT + t_k) \tag{A16}$$

This is equivalent to the product of $\delta\theta$ and a series of impulses of weight $V_s/\omega$. Thus,

$$\delta x = \frac{V_s}{\omega} \sum_{k=0}^{\infty} \delta\theta(kT + t_k)\ \delta(t - kT - t_k) \tag{A17}$$

Note that if the frequency is constant, $t_k$ is constant, and we can shift t to eliminate $t_k$ in (A17). Also note that $\omega = \frac{2\Pi}{T}$. Therefore,

$$\delta x = \frac{V_s T}{2\Pi} \sum_{k=0}^{\infty} \delta\theta(kT)\ \delta(t - kT) \qquad \text{(A18)}$$

Thus, the linearized model of the PFD is the sampling of by a train of impulses of weight $V_s T/2\Pi$.

# APPENDIX B

## CONTINUOUS APPROXIMATION OF THE SAMPLING PROCESS

Consider a system with an impulse sampler and a low pass filter, as shown in Figure B1.

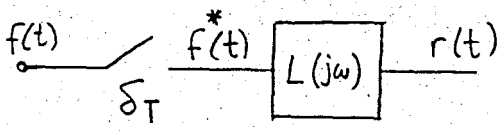



FIGURE B1. A Sampler Followed by a Filter.

Let the sampling period be T and define $\omega_s$ as

$$\omega_s = \frac{2\Pi}{T} \tag{B1}$$

The impulse-sampled signal, f*(t), is given by

$$f^*(t) = f(t) \sum_{k=-\infty}^{\infty} \delta(t - kT) \qquad (B2)$$

We can replace the summation in B2 by its Fourier series representation. This results in

$$f^*(t) = f(t) \sum_{k=-\infty}^{\infty} \frac{1}{T} e^{-jk\omega_s t} \qquad (B3)$$

Now assume that $F(j\omega)$ is the Fourier transform of $f(t)$.

$$f(t) \leftrightarrow F(j\omega) \qquad (B4)$$

Recall the frequency-shift theorem,

$$e^{\lambda t} f(t) \leftrightarrow F(j\omega - \lambda) \qquad (B5)$$

In view of B4 and B5, the Fourier transform of $f^*(t)$, $F^*(j\omega)$ equals

$$f^*(t) \leftrightarrow F^*(j\omega) = \frac{1}{T} \sum_{k=-\infty}^{\infty} F(j\omega - jk\omega_s) \qquad (B6)$$

Thus, $F^*(j\omega)$ is periodic in $\omega$, as shown in Figure B2.

However, if the bandwidth of the low-pass filter, $L(j\omega)$ is much lower than $\omega_s$, the side lobes will be attenuated and will not affect the system. Therefore, they may be ignored and $F^*(j\ )$ may be approximated by the center lobe.

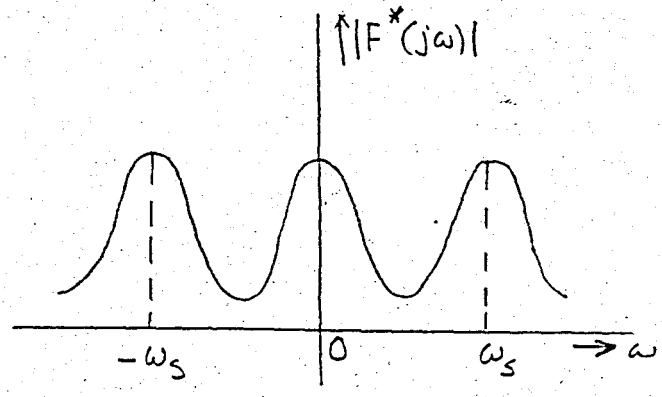



FIGURE B2. Magnitude of F*(jω) Versus ω.

$$F^*(j\omega) \cong \frac{1}{T} F(j\omega) \tag{B7}$$

and therefore,

$$f^*(t) \cong \frac{1}{T} f(t) \tag{B8}$$

Thus, if an impulse sampler is followed by a low-pass filter whose bandwidth is much narrower than $\omega_s$, the sampler may be approximated by a gain of 1/T.

# APPENDIX C

## AN APPROXIMATION FOR EQUATION (17)

Consider the function f(x)

$$f(x) = \frac{x(e^x + 1)}{e^x - 1} \tag{C1}$$

This function may be represented by its Taylor series. Since the function f(x) is even, the series contains only even powers of x.

$$f(x) = 2 + \frac{1}{6} x^2 \ldots \tag{C2}$$

Next, consider the interval $0 < \varepsilon \leq x$, and define there a function

$$g(x) = \frac{f(x)}{x^2} \tag{C3}$$

In view of (C2), this equals

$$g(x) = \frac{(e^x + 1)}{x(e^x - 1)} = \frac{2}{x^2} + \frac{1}{6} + \ldots \qquad (C4)$$

For small values of x, g(x) may be approximated by the first term of the series.

$$\frac{e^x + 1}{x(e^x - 1)} \cong \frac{2}{x^2} \qquad (C5)$$

Noz substitute $x = T/\tau$ and multiply both sides of (C5) by $4\Pi$

$$\frac{4\Pi\tau(e^{T/\tau} + 1)}{T(e^{T/\tau} - 1)} \simeq \frac{8\Pi\tau^2}{T^2} \qquad (C6)$$

Equation (C6) is the approximation suggested by (17). Clearly, this approximation introduces an error which increases as $T/\tau$ grows. Some values of the approximation error are given in Table C1.

TABLE C1

Approximation Error

| $T/\tau$ | 0.1 | 0.2 | 0.5 | 1.0 |
|---|---|---|---|---|
| Approximation Error | 0.08% | 0.3% | 2% | 8% |

It can be seen that the errors are small when $T/\tau << 1$.

# APPENDIX D

## MEASUREMENTS OF MOTOR PARAMETERS

The armature resistance $R_a$ is measuring applying different armature voltages and having corresponding current values. The average value is found to be 3 ohms.

Armature inductance $L_a$ measurement is made by an a.c. bridge and measured to be

$$L_a = 24 \text{ mH}$$

The back e.m.f. constant $K_E$ of the motor is obtained by running the machine as a generator at a rated field current and calculating the ratio of generated voltage to speed which is found to be 1.06 V/rad/sec.

The motor torque constant $K_T$ of the motor is measured to be 1 N.m/A. In ideal, it must be equal to $K_E$.

The total motor armature, generator and tachogenerator inertia is calulated from

$$\Sigma T = J \alpha$$

where $\alpha$ is the acceleration obtained from acceleration recordings, J is the total inertia of the motor and load and T is the sum of the produced torques. The total motor, generator and tachogenerator inertia is found to be 0.15 $kg.m^2$.

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