TIME MULTIPLEXED VIDEO TRANSMISSION

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CONTENTS

Part ONE

Introduction

I have always been attracted by the idea of multichannel and multidirectional information communication on the same path .

As an engineer working since two years in the TV domain , I wished to see how such a system can be applied to the television.

In the books concerning TV engineering time multiplexed video systems are not mentioned . Big companies producing professional TV equipment such as Bosh-Fernseh , Ampex , Thomson ,RCA did not include time multiplexers in their production list.

This Project provided me a good opportunity to work on the field of time multiplexing and to develop my knowledge about the different aspects of the system .

The principles of the time multiplexing are visible in the block diagrams of the sending and receiving ends .

The way I had to fallow is determined by technological limitations and the restrictions coming from the performance of the devices .

1 a) Functional description of the sending end .

This unit receives two different video signals and sends the multiplexed signal .

The inputs and the outputs of the system should be compatible with standart video cable impedance (75Ω) and insure a proper termination of the previous stages .

On the receiving end , the two video input amplifiers are arrenged to have good impedance matching . Input amplifiers provide a gain of 3-4 to compensate the attenuation of the cable and the insertion loss of the analog switch.

Analog switches are controlled by ϕ_1 and ϕ_2 control pulses. They have a phase differance of 180° . So the analog switches are switched ON and OF alternataly.When the analog switch 1 is ON , the second switch is OFF .

The ON resistance value of the switches varies from one to another . The amplifier of the channels present also small gain differences due to the tolerances of the elements . To compensate the differences balancing is necessary for each channel .

A second amplification stage is designed to compensate the loss of the adder and output buffer . This stage preemphesizes high frequency side of the video spectrum to compensate the high frequency

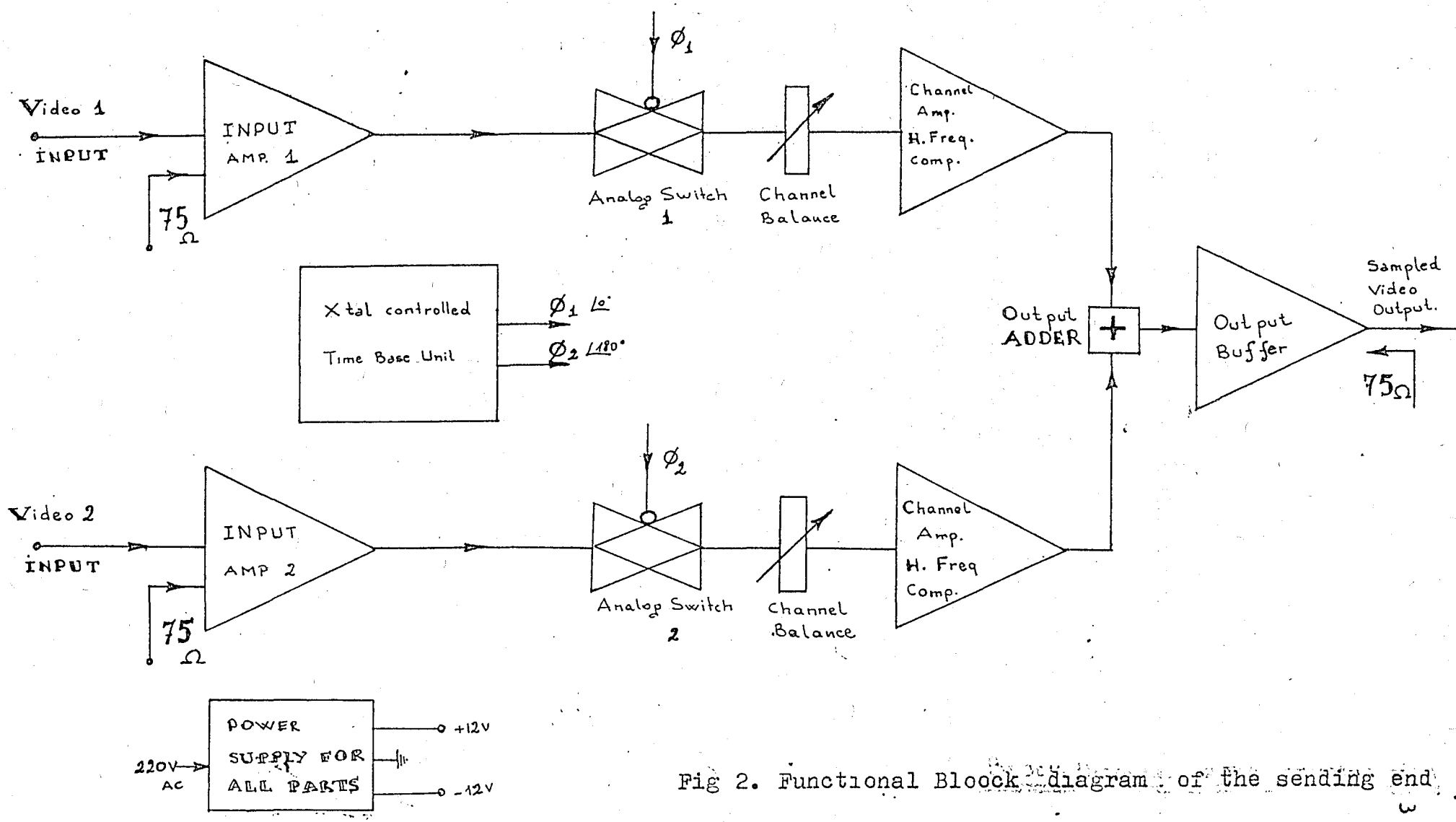


Fig 2. Functional Bloock diagram of the sending end

side of the video spectrum to compensate the high frequency losses of the transmission cable between the sending end and the receiving end .

The output buffer consists of an emitter fallower wich matches the output impedance to 75Ω and clamps the black level of the out going video to O V . Double power supply (± 12V) is necessary for this stage

2 phase control voltage (V_c) ϕ_1 and ϕ_2 are generated by a quartz controlled oscillator or by a H'/2 pulse generator which takes the horizontal pulse referance from the studio and halves the frequency to form ϕ_1 and ϕ_2 .

1 b) Functional description of the receiving end .

The unit receives the multiplexed video signal and gives the two video signals after demultiplexing .

The incoming signal is applied to the input amplifier wich is similar to the input amplifier of the sending end . This amplifier feeds the analog switches .

The sampling pulses are formed by a circuit which regerates the sampling pulses $\emptyset_1$ and $\emptyset_2$ are again out of phase .

When H'/2 sampling is used (see H'/2 circuit description) the sampling pulses are regenerated from the sync of the incoming signal or externally applied .

After proper timing , analog switch 1 is switched ON when the informations coming from the first channel of the sending end reach the output of the input amplifier .

The same sequences are valide for the operation of the second analog switch . The channels are again balanced after the switches The channel amplifier realizes the final amplification and the final frequency compensation around 3,5 - 4 MHz .

The last stage is a buffer to provide 1 V_{pp} standart video on 75 Ω load with proper clamping . The circuits of the second channel are similar .

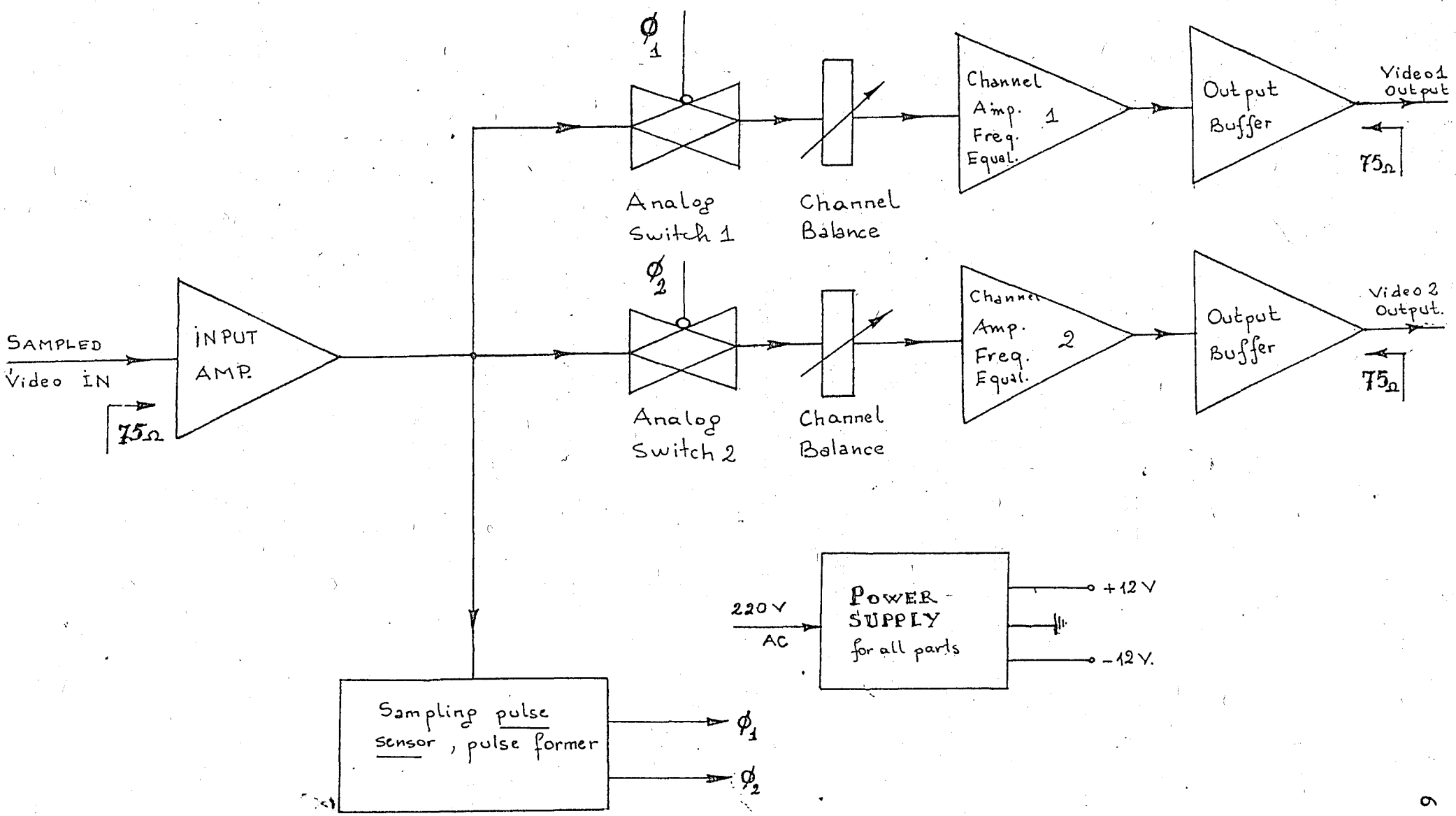


Fig 3. Functional block diagram of the receiving end

SENDING END

Input Amplifier And Analog Switches

The main problem is to match the impedance of the incoming video line (75Ω) to the circuits and to provide gain to compensate the insertion loss of the analog switches (A.S.) .
To have a low impedance at the input a grounded base configuration where the signal is applied to the emitter was preferred.

Base voltage $V_B = 12 \times \frac{0,47}{3,77} = 1,5$ V $\quad V_E = 1,5 - 0,6 = 0,9$V

$$I_E = \frac{0,9}{82} = 0,011 \text{ A} = 11 \text{ mA} \qquad h_{ie} = \frac{25}{11} = 2,26\ \Omega$$

$\overline{R_B}$ = equivalent of base voltage divider

$$\overline{R_B} = \frac{3,3 \times 0,47}{3,77} = 0,412 \text{ k} = 412\ \Omega$$

$\overline{R_B}$ reflected to the emitter ($h_{fe} \simeq 150$) $= \frac{412}{150} = 2,74\ \Omega$

The diagram of the input amplifier is given in figure 4.
The impedance that we see from A is $2,74 + 2,26 // 82 = 4,65\ \Omega$
So very low impedance is obtained . To insure a proper matching

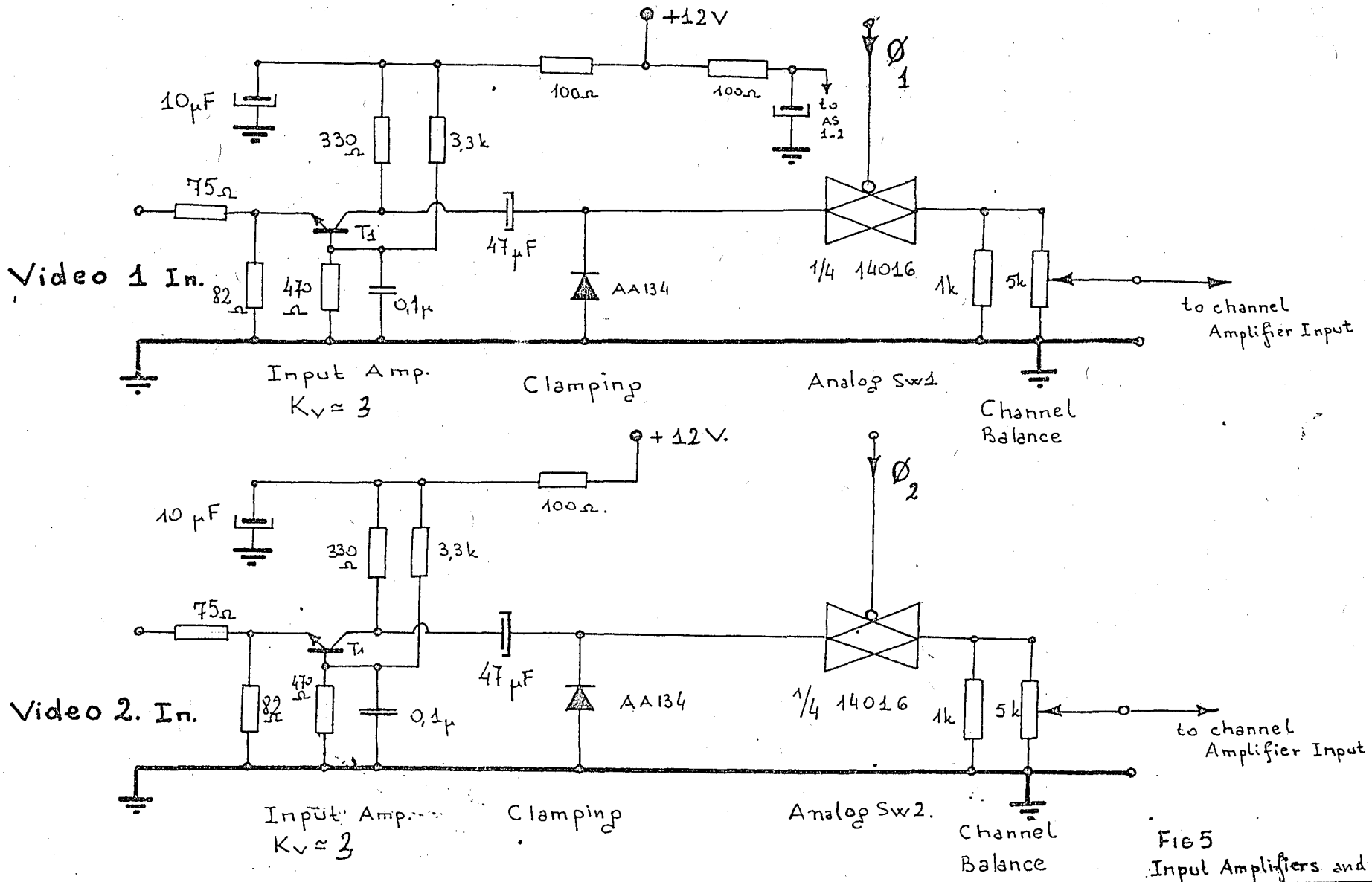


Fig 5
Input Amplifiers and Analog Switches of the sending side

a resistor of 86 is placed in series to the input of the circuit.

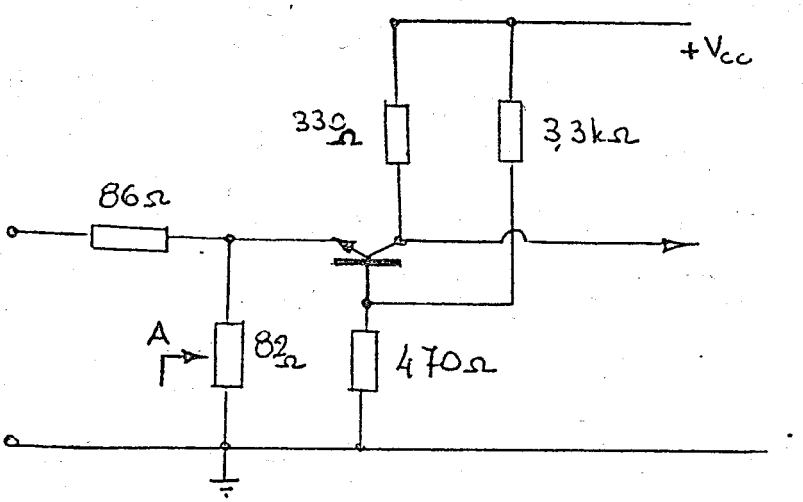


Fig 4 . Input amplifier .

To keep the band width for video signal one generally sets the gain of each individual stage to value between I,5 and 4 (Ref I a) .

The elements determining the gain of this stage are shown in fig 6 .

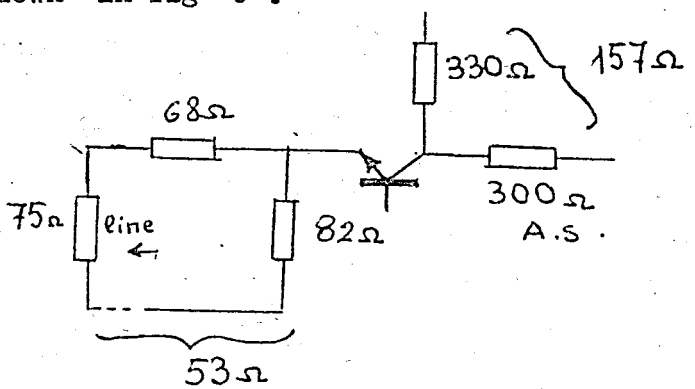


Fig 6 .

$$\text{Voltage gain } K_V = \frac{R_c \text{ equivalent}}{R_e \text{ equivalent}} = \frac{157}{53} \simeq 3$$

The amplified signal that we have at the output (collector of the transistor) has a DC component . To clamp the bottom of the sync to ground we use a simple clamping circuit (Ref 3 b)

The "ON" resistance of the A.S. is about 300 Ω. So , a good matching is established from the collector of Q_I (330Ω) to the A.S. (300 Ω)

The output of the analog switche should be terminated with a resistor of I kΩ for a proper operation of the switch . For loading resistors $>$ I kΩ the electrical charge accumulated in the switch during one period can not be discharged (the output can not swing from the maximum positive value to the ground) I kΩ is an optimum value for f= 8,3 MHz (sampling frequency) In the technical sheet of I40I6 B the value of the optimum resistor was not specified .

5 kΩ variable resistor (in paralel with I kΩ load) is for the compensation of the ΔR_{on} resistance of the A.S. of each channel (see fig 22) . The gain differance of the amplifiers due to the element tolerances is also balanced with the same resistor .

Sending End Channel Amplifiers And Output Buffer .

This board consists of two channel amplifiers for the samled video signals .

Each channel amplifier has two gain stages (T_I , T_2) . T_3 is an emitter fallower . The signals coming from the amplifiers are added on the resistors and then applied to the base of T_4 .

T_4 is the output buffer .Because of the special form of the video signal , the variable resistor R_v is to be adjusted in order to have the emitter of T_4 exactly at ground potential. In this case the base potential of T_4 is about 0,65V .)

Fig. 8 shows the components of one line positive video signal .

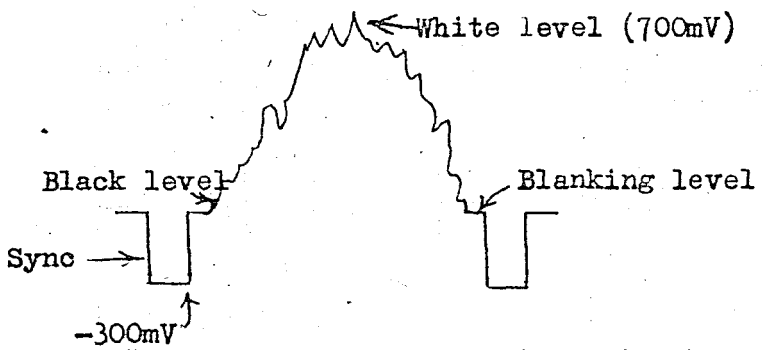
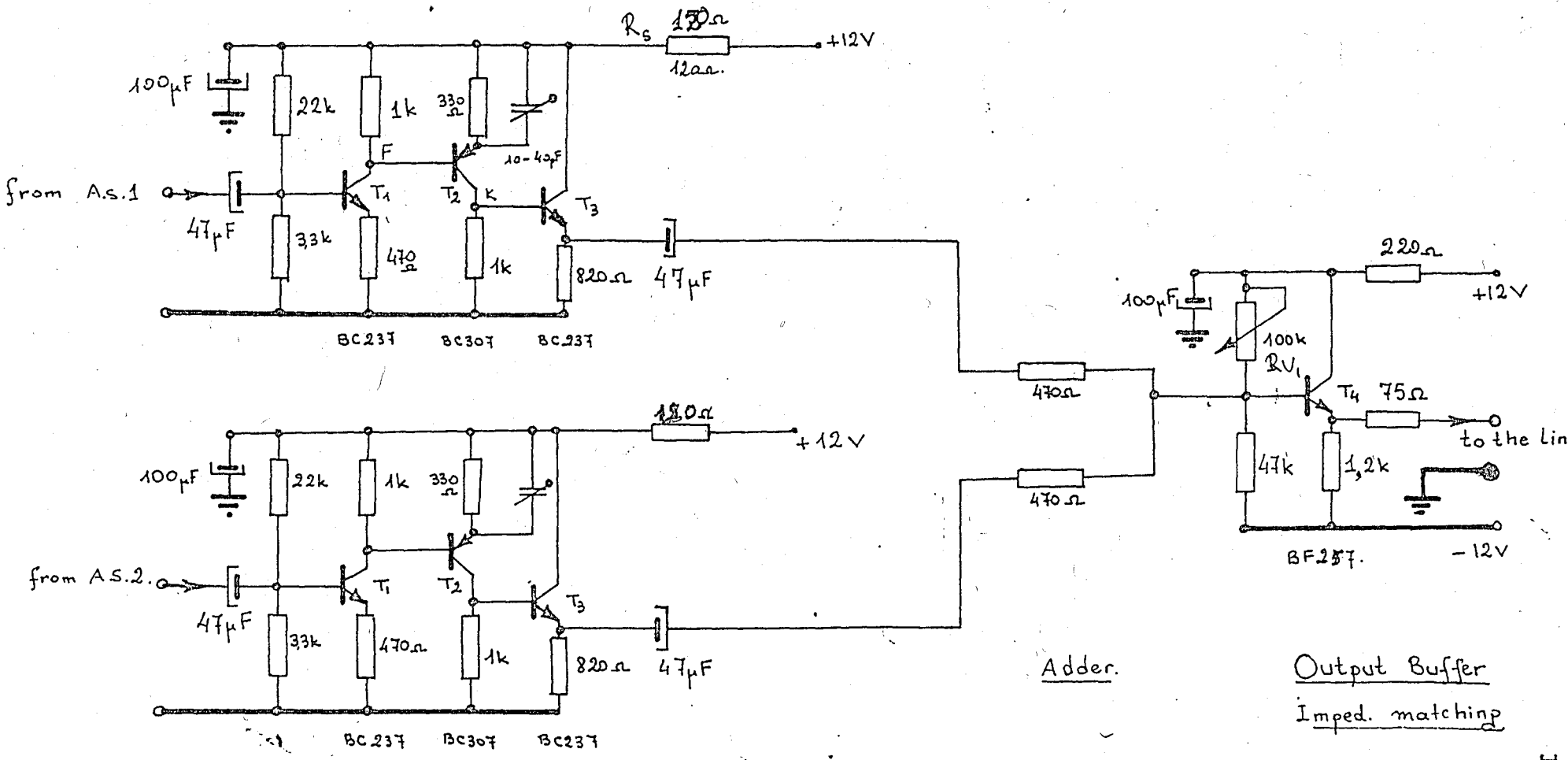


Fig.8 . One line positive video signal .

Blanking level corresponds to zero volts , syncronisation pulse bottom to - 300 mV and maximum white level to+700 mV.Thus using T_4 , proper clamping of the video signal is done .



Channel Amplifiers.

Adder.

Output Buffer

Imped. matching

FIG 7

Sending Side Channel Amp. And Output Buffer.

The collector current of T_I is selected around I,6 mA .

The base voltage is $V_{T_I B} = \frac{3,3}{22\ 3,3} \times 11 = 1,435$ V

(Assuming that we have I V drop on the resistor R_s in series with the +I2 V supply line) I2-I= I1 V = V_{cc}

$V_{T_I E} = 1,435 - 0,6 = 0,835$ V $\qquad I_{T_I E} = \frac{0,835}{0,47} = 1,77$ mA

$V_{T_I C} = 11 - 0,77 \times 1k = 9,23$ V $= V_{T_2 B}$

$V_{T_2 E} = 9,23 + 0,6 = 9,83$ V $\qquad I_{T_2 E} = \frac{11 - 9,83}{0,33} = 3,54$ mA

$V_{T_2 C} = 3,54 \times 1 = 3,54$ V $\qquad I_{T_2 E} = \frac{(3,54 - 0,6)\ V}{(0,82)\ k\Omega} = 3,58$mA

$\sum I \simeq I_{E_1} + I_{E_2} + I_{E_3} = 8,89$ mA

$\frac{1}{8,89\ 10^{-3}} \simeq 112\ \Omega = R_s$

The gain of the first stage is :

$$K_{V_1} = \frac{1k \,/\!/\, h_{fe2} \cdot (h_{ie2} + R_{E2})}{R_{E_1}}$$

$h_{fe2} = 150$

$h_{ie2} = \frac{25}{3,58} = 7,06\ \Omega$

$h_{fe2} \cdot (h_{ie2} + R_{E2}) = 150 \cdot (7,06 + 330) \simeq 51\ k\Omega$

$1\ k \,/\!/\, 51\ k = 0,98\ k\Omega$

$$K_{V_1} = -\frac{0,98}{0,47} \simeq -2,085$$

$$\left(K_{V_2}\right)_{\text{low freq.}} = -\frac{1k \,/\!/ (h_{ie3} + R_{E3})\, h_{fe3}}{R_{E2}} \qquad h_{ie3} = \frac{25}{3,58} = 6,98\ \Omega$$

$$(h_{ie3} + R_{E3}).h_{fe2} = 150 \cdot (6,98 + 820) = 124\ k\Omega$$

$$1\ k \,/\!/ 124k = 0,98\ k$$

$$\left(K_{V2}\right)_{\text{low freq}} = -\frac{0,992}{0,33} \simeq -3 \qquad K_V = K_{V1} \times K_{V2} = (-2,85)x(-3) = 8,55$$

Because of the trimmer capacitor shunting the emitter resistor of T_2 (330Ω) the gain of T_2 increases with frequency . The parallel equivalent of 330Ω and this capacitor of 40 pF at 5 MHz is :

$$\left(R_{E_{T2}}\right)_{equi} = 330 \,/\!/ \frac{1}{C\omega} \qquad \frac{1}{C\omega} = \frac{1}{40x10^{-12} x 2x\Pi x 5x10^{6}} = 795\ \Omega$$

for $f = 5MHz$.

$$\left(R_{E_{T2}}\right)_{equi} = \frac{330x795}{330+795} = 233\ \Omega$$

$$\left(K_{V2}\right)_{5MHz} = -\frac{0,992}{0,233} = -4,257$$

$$20 \log \frac{\left(K_{V2}\right)_{5MHz}}{\left(K_{V2}\right)_{\text{low frq}}} = 20 \log \frac{4,257}{3} = 3,106 \text{ dB} .$$

The timmer capacitor at the collector of T_2 is used to compensate the loss of high frequency compponents of the video signal on the circuits and the cables .

The final stage transistor T_4 has low output impedance . An additional resistor is placed in series with the load to realise good matching and to avoid reflections from the cable.

The inputs of the circuits are RC coupled . The time constant of the input circuit is selected in such a way that the largest pulses (vertical pulses) are passed without distortion.

X-tal Controlled Sampling Pulse Generator .

T_1 is used as oscillator . The LC network placed at the collector of T_1 is tuned to the frequency of the quartz cristal(x-tal) wich is placed on a feedback path from the collector to the base . At the frequency of the cristal the LC tank circuit has high impedance and the circuit of T_1 provides high gain . Thus at the collector of T_1 we obtain a sinusoidal oscillation at the X-tal frequency . This frequency is the sampling frequency . Due to the caracteristics of the analog switches f is selected as 8,3 MHz . In the resonnance frequency of the LC network is shifted from X-tal ffequency then the amplitude of the oscillations is reduced .

C should be selected larger than the distributed capacitance of the inductors (otherwise it will not have any adjusting effect) C is selected around 300pF and the value of the equivalent induc - tance is :

$$f = \frac{1}{2\sqrt{LC}} \qquad L = \frac{1}{f^2 . 4\pi^2 C}$$

$$L = \frac{1}{(8,3\text{x}10^6)^2 \text{x} 4 \text{x} \pi^2 \text{x}\ 300 \text{ x } 10^{-12}} = 1,22\text{x}10^{-6}\ \text{H.}$$

$$L = 1.22\,\mu\text{H.}$$

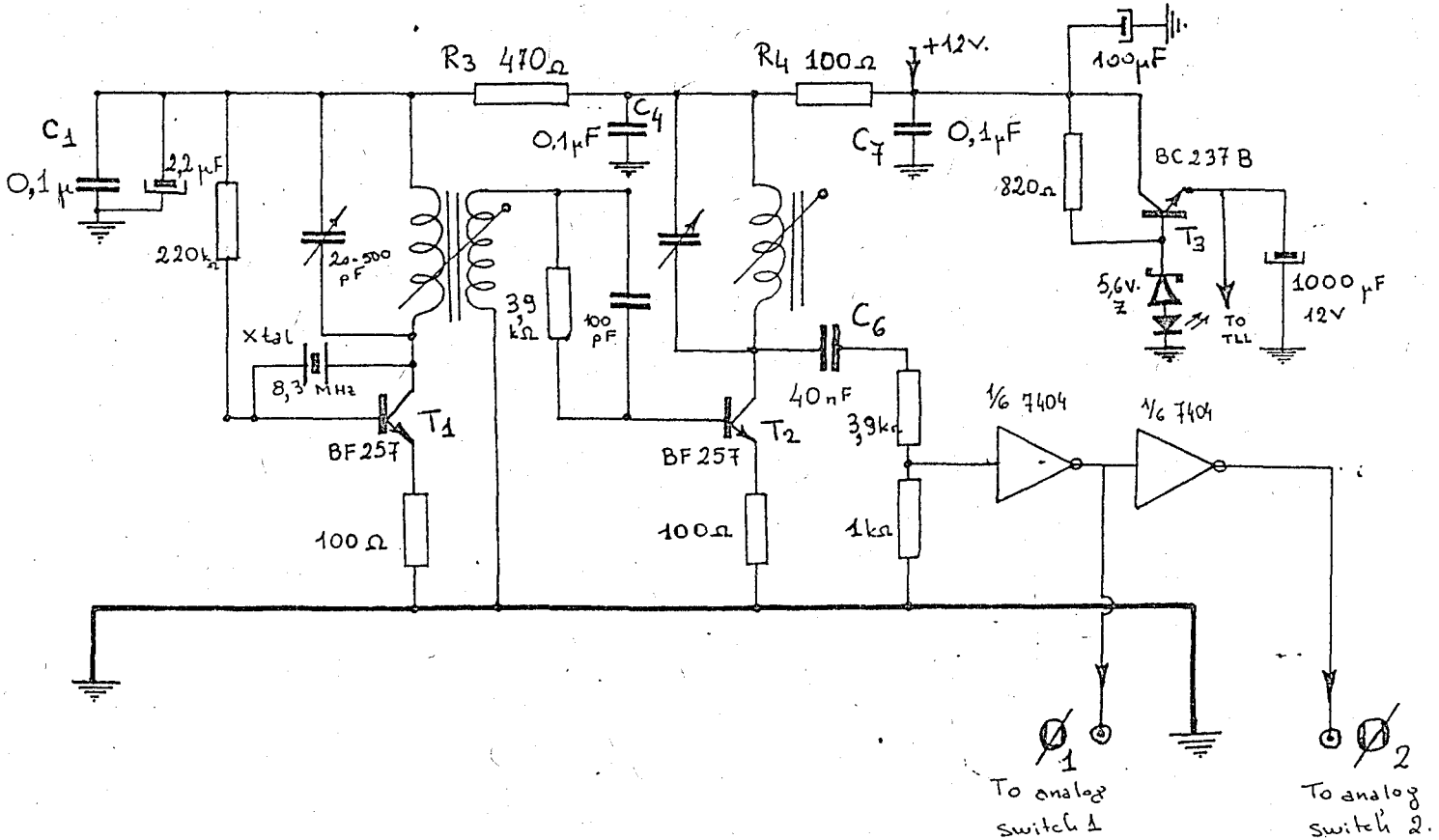


FIG 9

Time Base for sampling Pulses.

The inductor is obtained with 20 turns of 0,1 mm wire on a magnetic core of 5 mm diameter .Secondary side consists of 8 turns of the same wire . So $n = \frac{N_1}{N_2} = \frac{8}{20} = 0,4$. Then transfer ratio n is set to 0,4 to minimize the reflection of the capacitance and inductance of the secondary side and to reduce the influence of the second stage to the lc collector load .The loss of voltage due to low n is compensated by the gain of the second stage .

100Ω resistor at the emitter provides negative feedback and decreases the output voltage but improves thermal stability .

T_2 is used as a buffer amplifier . The LC circuit of the collector is again tuned at x-tal frequency .

The voltage of the collector of T_2 is applied to a voltage divider (1k/4,7k) not to give more than 5V to the input of theTTL.

C_6 of 40 nF is for the DC isolation of T_2 from the divider and is essentially short circuit at the frequency of the x-tal :

$$\frac{1}{C\omega} = \frac{1}{40\times10^{-9} \times 2\times\pi\times8,3\times10^{6}} = 0,479$$

The signal is applied to the inverting gates of a TTL hex-inverter (H 7404) to obtain two clock pulses ϕ_1 and ϕ_2 . The characteristics of this IC are in Ref 6.

The analog switbhes are controlled with ϕ_1 and ϕ_2 .The propagation delay time of the inverter is of the order of 10 ns. ϕ_1 is delayed in an inductor to obtain an exact phase differance of 180 ° .

T_3 is a voltage regulator to supply +5V to the TTL dividing down the positive voltage (+12 V) of the board .

R_1 , R_2 , C_1 , C_4 , C_7 form a network wich removes the ripples of the + supply and prevent RF contamination of the circuits connected to the same power supply .

The details of the tuned circuits are in Ref 4 .

Power Supply PS 01 , PS 02

The analogy between the sending and receiving ends allowed us to use the same power supply for both sides . The voltages required for the operation are +12 V, -12 V .

The circuit should supply 100mA to the +12 V line and 15mA to the -12 V line . -12v is used only for the emitter voltage of the final stage transistor .

Since +12V supplies a large number of stages , the probability of failure is higher ; a short circuit protection is added to the circuit .

A standart 4W; 220 V / 2x12 V transformer is used .The center tap and bridge rectifier configuration is selected to obtain (+) and (-) voltages from the same bridge .

These voltages are smouthed with electrolitic capacitors of 1000 μF and high frequency parasitic signals coming from mains are filtered with ceramic capacitors of 0,1 μF .

+12 V side : The base of the Darlington configuration (T_1 and T_2) receives the voltage of the collector of T_3 . The emitter of T_3 is at a fixed potential because of the stabilized voltage of D_2

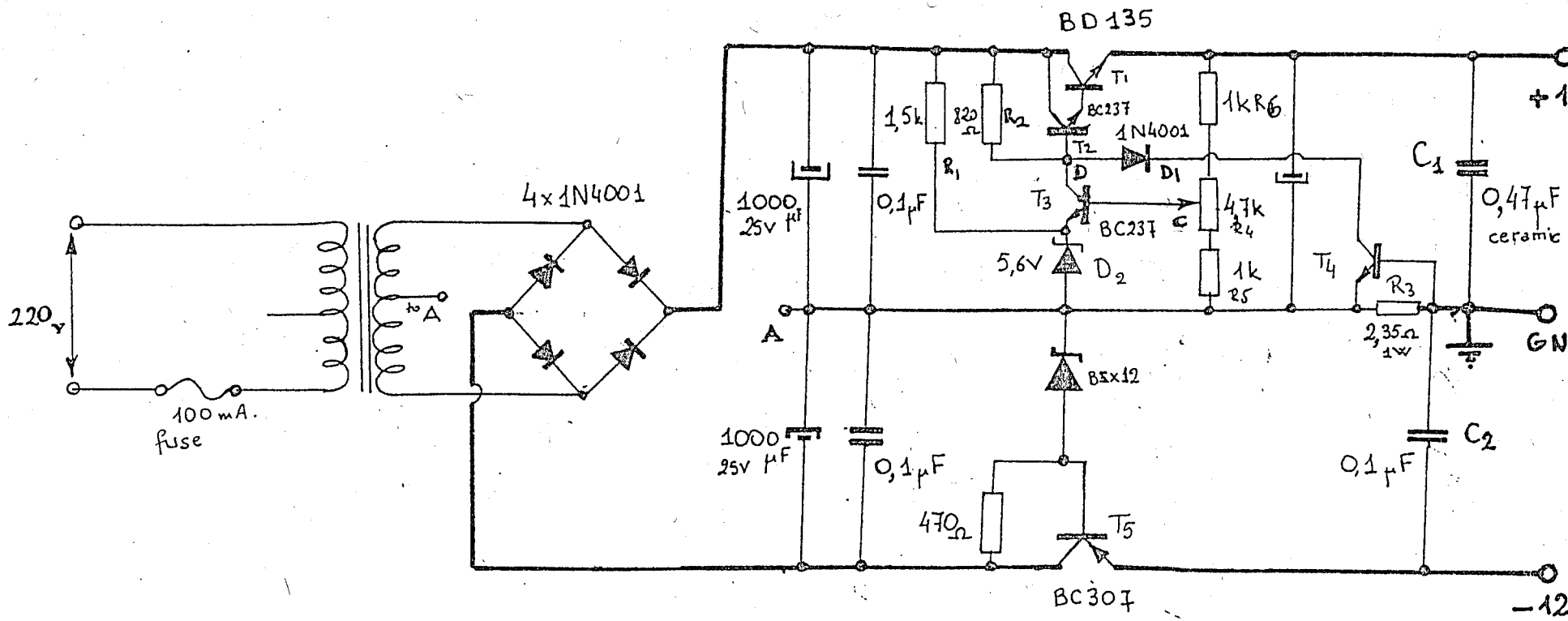


FIG 10

POWER SUPPLY UNIT

PS01 AND PS02

(Sending " Receiving)

The voltage divider (R_4 , R_5 , R_6) wich determines the base voltage of T_3 controls the output voltage. By setting the value of the variable resistor, T_3 is more or less conductive. Thus , the voltage of point D and consequently that of the output point are controlled .

Any drop of the output voltage makes T_3 less conductive and the voltage of point D is increased .

R_3 of 2,35Ω(I W) is used for sensing the output current of the power supply .

The currents supplied by the circuit are as indicated in fig II .

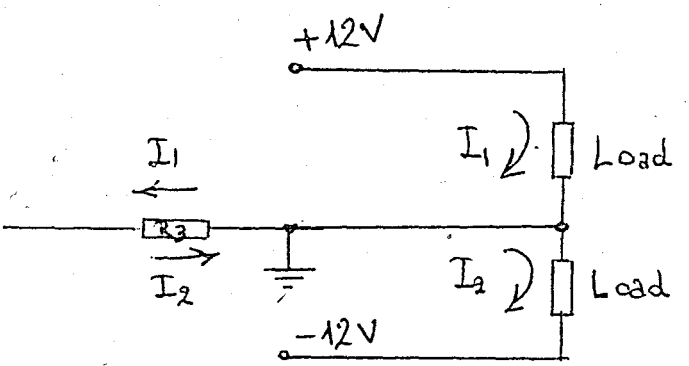


Fig II. Currents of the power supply .

A maximum value of 270 mA is adopted for I_I .I_2 is of the order of I5 mA . So , $I_I - I_2 = 255$ mA .

The voltage across R_3 is $U = 0,255 \times 2,35 = 0,6$ V . This voltage is applied to the base of T_4 . And , when the net current reaches 255mA T_4 is in conduction ; the point D is grounded via the diode D_I .

The output voltage decreases to limit the current .This simple method of protection is useful for circuits where the power does not exceed 4–5 Watts .

Negative power supply has no particularity . C_I , C_2 are ceramic capacitors used to remove high frequency noise components coming from circuits .

Receiving End Main Board

The essential function of this board is demultiplexing the incoming video signal. It amplifies the output of the analog switches. The circuit provides frequency compensation. The output is matched to 75 Ω and the blanking level of the video signal is clamped to 0 V.

The input amplifier Q_I is operated in common base mode. The signal is applied to the emitter and the input impedance is matched to 75 Ω. This stage has the same characteristics as the input amplifier of the sending end (Voltage gain $\simeq$ 3-4)

The amplified signal is fed to the analog switche and to the sampling pulse sensor circuit via resistors (R_1, R_2, R_3)

The capacitor of 480 pF are used to remove high frequency parasitic components (of the order of few hundred kHz) that may be induced on the line.

Since A. S. have low treshold voltage any parasitic pulse can trigger them. So, resistors of 5.6 kΩ are shunting the control inputs ϕ_1, ϕ_2 to keep them at ground potential when no voltage is applied.

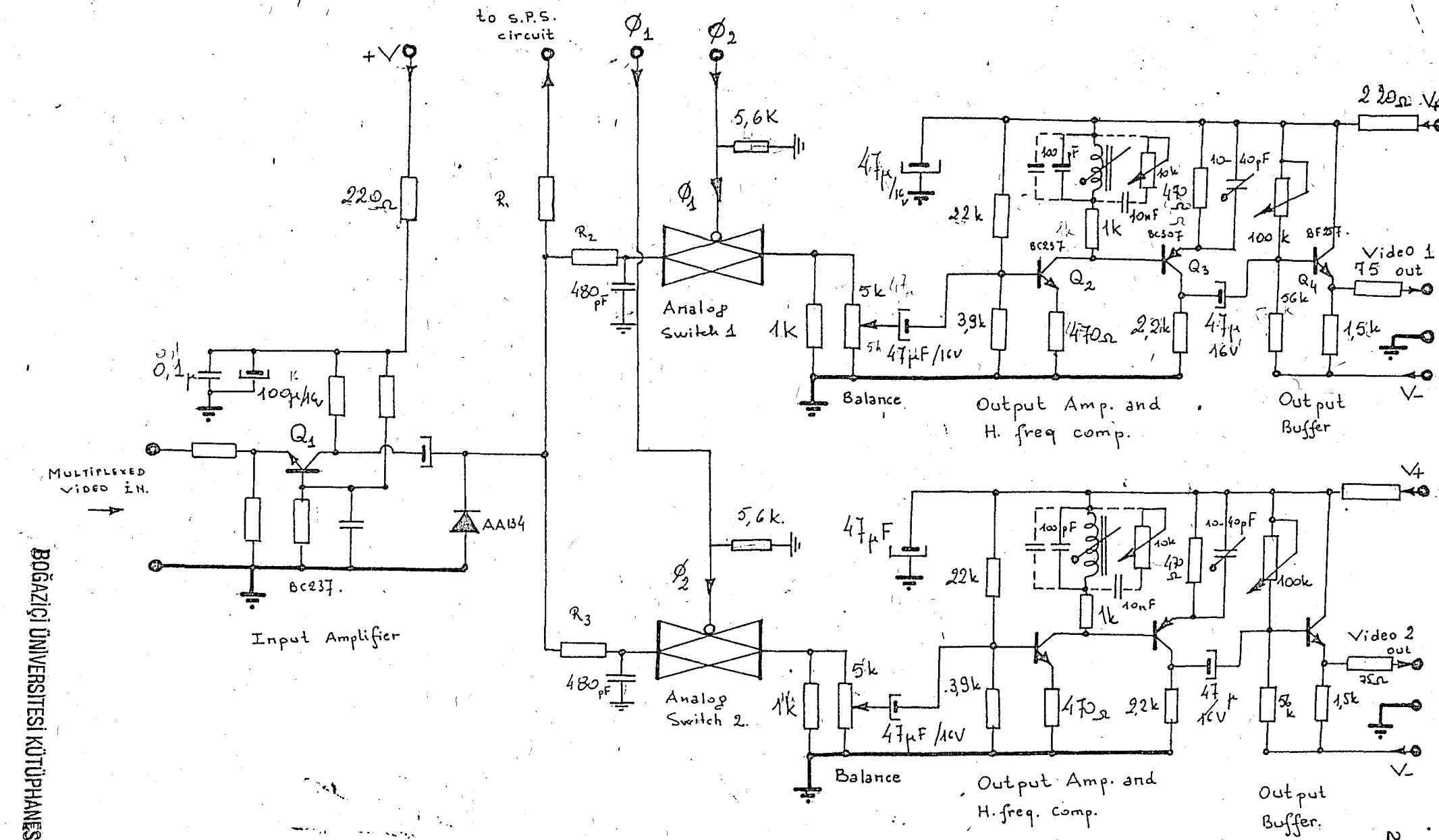


FIG 12 Receiving side main board.

The output of the A. S. is properly terminated and capacitive coupling is preferred. The capacitor is selected large enough (47 μF) to insure the transmission of the lowest frequency signals (such as the fundamentals of the syncronisation pulses).

The output amplifier consists of Q_2, Q_3. Q_2 is a pnp small signal transistor. The collector load of this transistor has a resistor of IkΩ in series with a LC circuit. The LC circuit is tuned to a frequency of 3.5-4 MHz to compensate the losses of the circuits at high frequency side of the video spectrum.

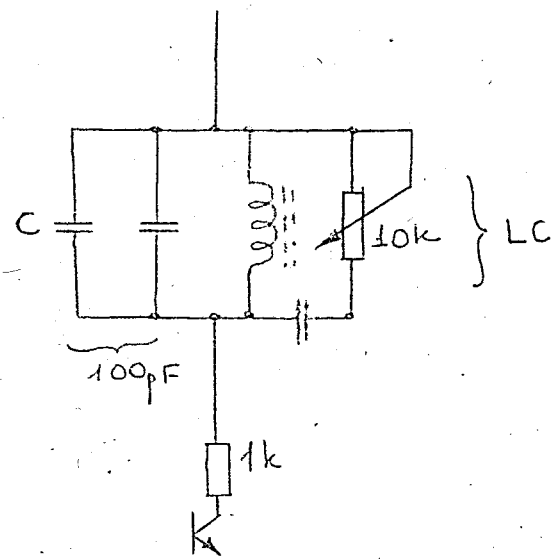


Fig I3. LC compensation network

I00 pF= C+ distributed capacitance of the inductor.

$$f = \frac{I}{2\pi\sqrt{LC}} \qquad L = \frac{I}{4\pi^2 f\ c} = \frac{I}{4.\pi^2.I6.I0^{I2}.\ I00.I0^{-2}}$$

$$L = I,6\ .\ I0^{-5} = I,6\ \mu H.$$

The collector load varies as described below :

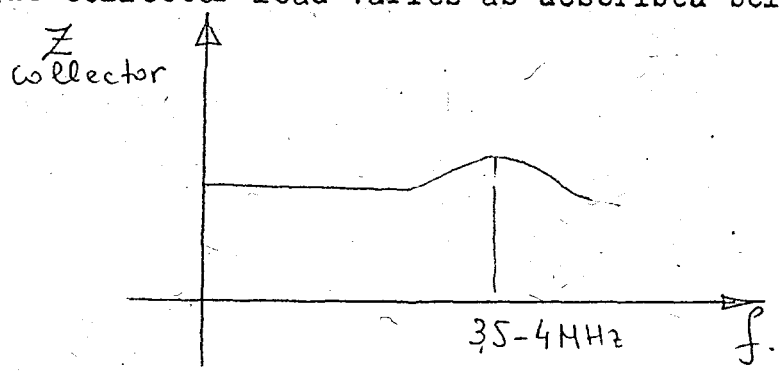


Fig I4 Variation of Z_c

The gain of Q_2 is approximatively equal to : $\frac{\text{coll,load}}{\text{emitt load}}$

Consequently, the gain exhibits a maximum at a frequency around 3,5-4 MHz . Q_3 is also a load for Q_2 but the reflection of the emitter load of Q_3 is $(Z_c /\!/ R_{E3}) x h_{fe3}$

$$Z_c = \frac{I}{C\omega} = \frac{I}{2\pi.40.I0^{-I2}\ 4.I0^6} \simeq I000\ \Omega$$

$I000 /\!/ 470 \longrightarrow 3I9\ \Omega$, let $h_{fe2} = I50$

$\rightarrow \left(Z_{E_{Q3}}\right)_{\text{reflected to base}} = 3I9 \times I50 = 47,8\ k\Omega$

$\left(Z_{E_{Q3}}\right)_{\text{reflected to base}}$ decreases with frequency but it has no

appreciable influence on the gain variation of Q_2 since it is much larger than $(Z_{42})_{collector}$.

This stage with a special frequency response is designed to compensate the frequency losses of the cicuits and of the cable

A variable resistor is placed across the LC network (10 nF can be considered as a short circuit element at 4 MHz.) The variable resistor is loading the LC circuit and damping the effective Q factor. The variable resistor is to be set according to the amount of losses at high frequencies.

Q_3 is a pnp transistor which has frequency dependent characteristics. The emitter load varies between 470 and 319 (trimming capacitor shunts the emitter resistor of Q_3 when the frequency is high) So, the gain of Q_3 increases with frequency. The resulting frequency is:

$$R = \frac{I}{C.\omega} \qquad 470 = \frac{I}{C.2.\pi.f} \qquad f = \frac{I}{40.10^{-12}.2..470} = 8,4\,MHz$$

The gain of Q_3 varies as in fig :

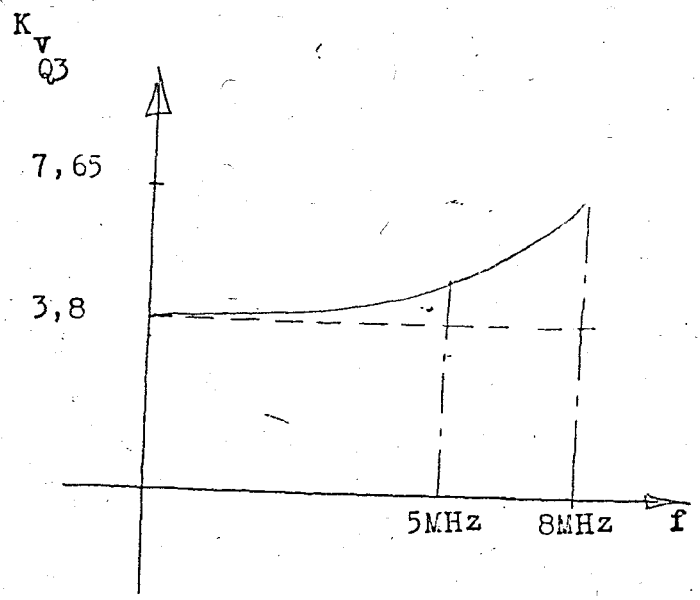


Fig I5 Characteristics of high frequency compensator.

Q_4 is the final stage for impedance matching and for the clamping of the blanking level to 0 V.

At the output a standart video signal is obtained. The circuits of the second channel are similar.

In this section reference Ia is used for video amplifiers and ref. 3b for clamping. The details of the compensators are in ref. 4.

Sampling Pulse Sensor and ϕ_1 , ϕ_2 Generator .

This circuit consists of two LC stages tuned to the frequency of the sampling pulse .

Q_1 and Q_2 are small signal RF transistors (BF294). Inductive coupling is done between the first and the second stage using RF transformer T_1 .

Q_1 is oparated in class A and Q_2 in class B . The signal obtained at the collector of Q_2 is applied to the inverters to form ϕ_1 and ϕ_2 .

The phase differance of ϕ_1 and ϕ_2 is not exactly 180° at the output of the inverters.There is a shift of 10 - 12 ns due to the propagaton delay time of the signal in the inverting . ϕ_1 is fed to the gate of the AS via the inductor B_1 to compensate the time error .

Negative supply voltage is not necessary for the operation of the board . +5 V for the TTL inverters is divided from the+12 V supply using a voltage regulator .

In the spectrum of the incoming signal the sampling pulse frequency is present.The circuit selects this signal and amplifies it. Because of the problems described in the other sections this board is not used;it has been replaced by H/2 generator circuit .

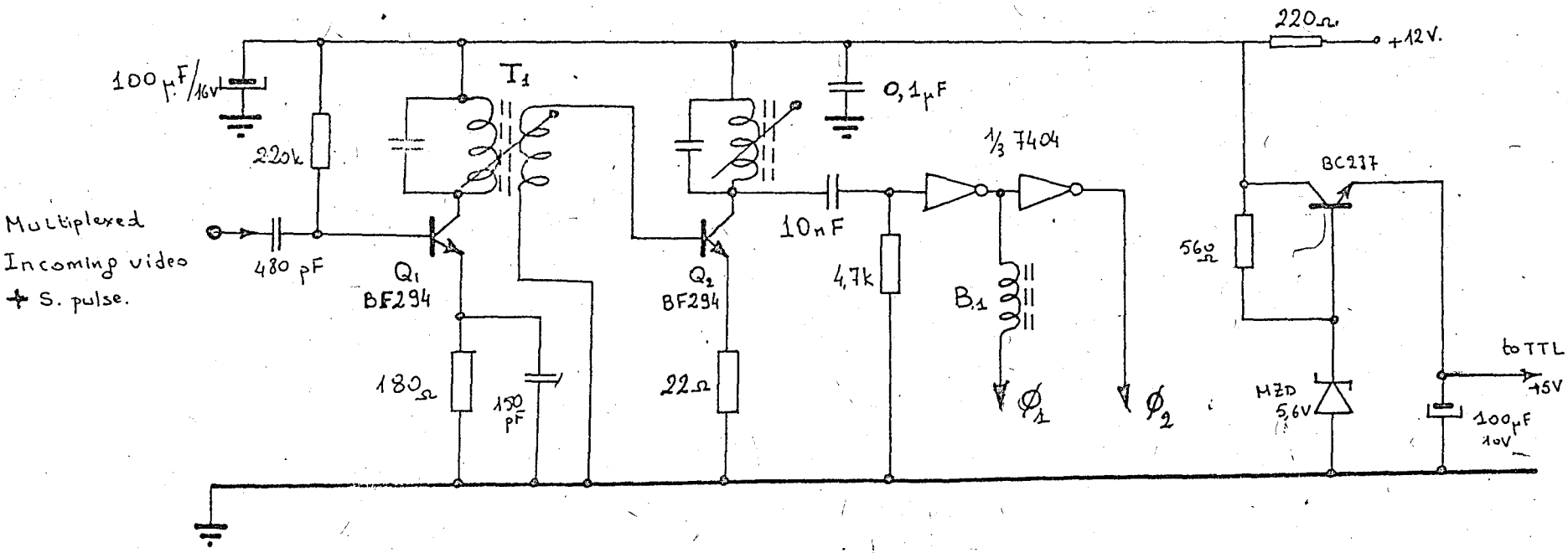


FIG 16

Sampling Pulse Sensor and ϕ_1, ϕ_2 generator.

H/2 Control Pulse Generator

Standart horizontal pulse (H) of the studio is a negative going pulse of 4 V_{pp} on 75 Ω load. To insure a proper termination of the H output, the input resister of the circuit is selected as 75 Ω .

Q_1, Q_2 and Q_3 are used to change the voltage levels of H pulse and to make them TTL compatible. The differential amplifier (Q_1 and Q_2) shifts the bottom of the pulses to ground potential. The waveform obtained at the point B (after the voltage dividers R_1, R_2) is a positive pulse of 5 V_{pp}. The signal is applied to Q_3 which operates in emitter follower mode to supply the pulses to the TTL counter.

Only the first Flip-Flop of 7490 (Decade counter) is used to perform " divide by two " operation. This counter is triggered at the negative-going edge of the pulse.

The output of 7490 is used as the first control phase (ϕ_1). ϕ_1 is also applied to an inverting gate to form ϕ_2 which is the control voltage of the second phase . ϕ_1 and ϕ_2 are out of phase by 180°.

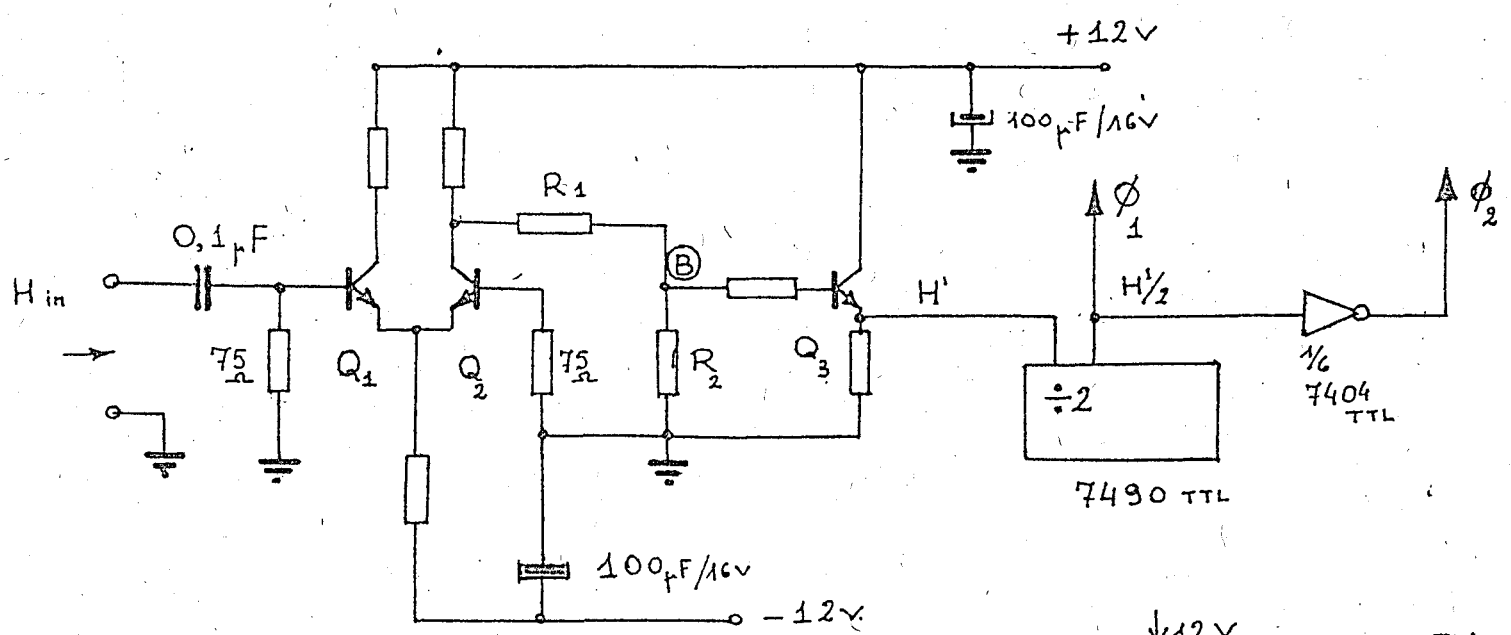
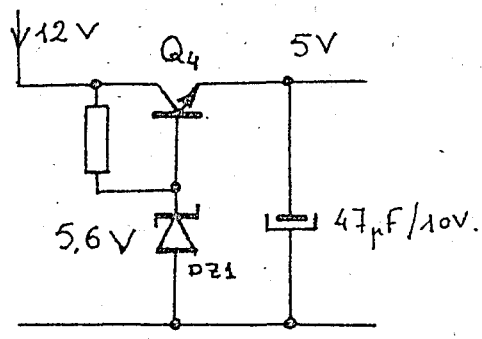


FIG 17

H/2 Control Pulse Generator.



When ϕ_1 is high ϕ_2 is low and vise versa . ϕ_1 activates the first channel , ϕ_2 activates the second channel.

+5 V supply voltage necessary for the TTL circuits is ob - tained from +12 V supply via a voltage regulator consisting of Q_4 and Dz_1 .

This board is used instead of the X-tal controlled sampling pulse generator .

The sequences of the control and the states of the analog switches are given in the following diagrem . (Fig 18)

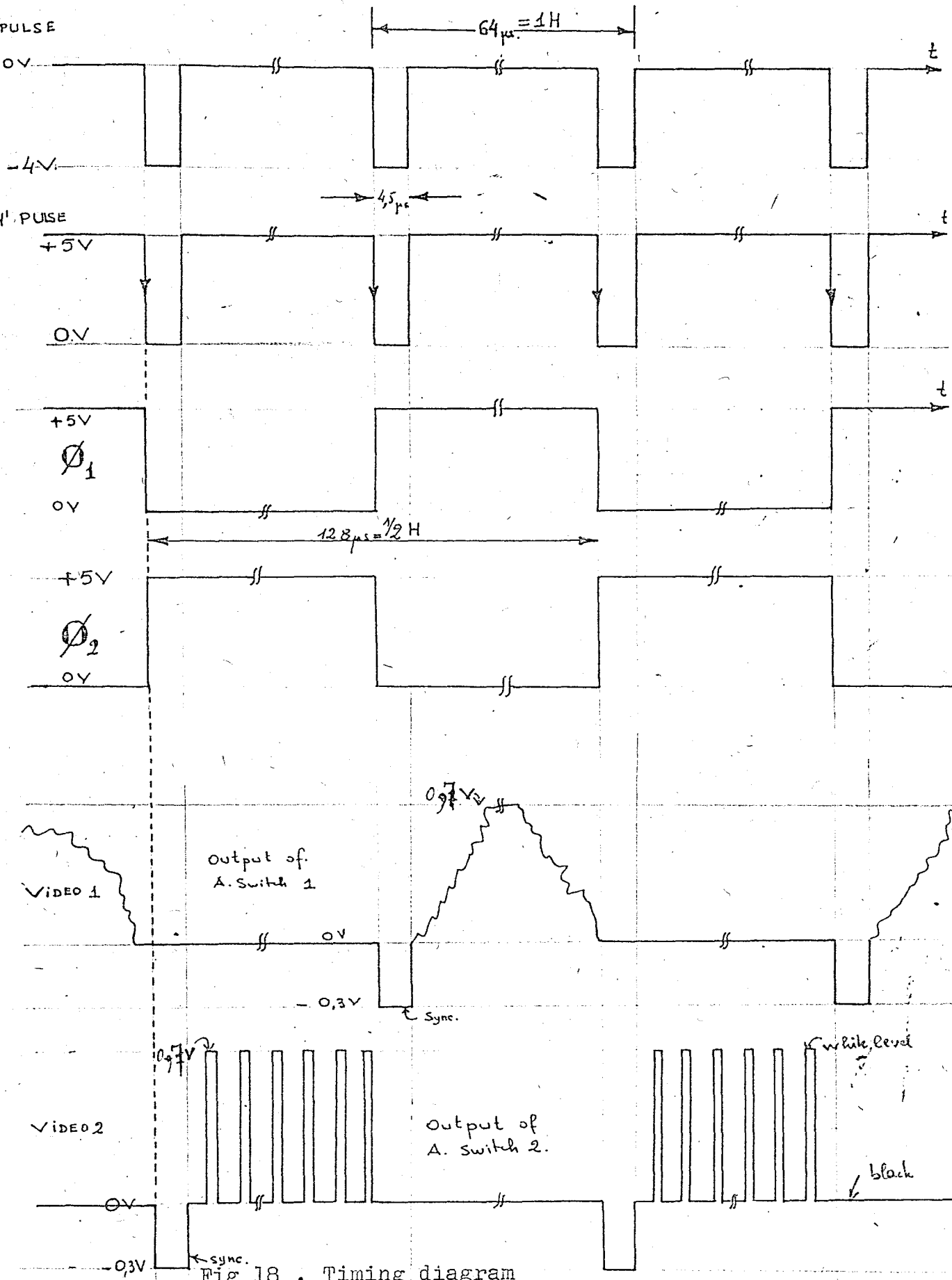


Fig 18 . Timing diagram

Characteristics of the Analog Switches (A.S.) and Selection of the Sampling Pulse Frequency

The only analog switche (AS) avialable was MC 14016 quad analog switch/multiplexer .

The techical data sheet (fig 22) shows that the switch has a corner frequency (-3dB)point) near 20 MHz for the transmitted signal . The propagation delay time(V_{in} to V_{out}) for V_{DD}= 10 V. is given as 7 to 15 ns after the establishment of the control voltage .

The propagation delay time from $V_{control}$ _ to V_{out} is 20-45 ns . These values are for the transmission of a constant DC level applied to the input .As a result of the measurements I observed that high frequency signal are delayed (1.5 times more) much longer than yhe DC componenbs of the signal . This is bringing a phase distortion (chroma - lumina delay) for the composite video signal which contains components from DC up to 5 MHz .

A sampling frequency of 8,3 MHz corresponds to a sampling time of $\frac{1}{8,3x10^{6}x2} = 60,24$ ns . The switch should be activated only during one alternance of the period .

According to the data sheet, in the test measurements for

the "delay time" and " turn-no time" (fig 23) a control voltage with 20 ns rise time is used . No information is given about the capacitance of the control input , but it is clear that this value is not very small.As a matter of fact, in the circuits designed for driving the control inputs , the control inputs were reacting as a load having a capacitive part which was causing a decrease of the slope of the rising edge of the control pulse .

Figure 24 indicates the variation of the insertion loss (dB) of the AS with load resistance . When the AS is terminated high - resistive load (such as 1MΩ- 100 kΩ) there is no loss; but in this cass, at high control frequencies the charge accumulated in the switch can not be removed completely .The output of the AS can not swing properly between V_{in} and ground potential.I observed that to insure a complete discharge the load resistor should be around 1k Such a low resistor increases the insertion loss of the A.S. (-2dB). This loss is compensated by the amplifiers of the succesive amplification stages .

My first approach was to select 60 ns as sampling time (20ns for rise time, 20 ns for max value of the pulse and 20 ns for the fall time). 60 ns corresponds to $f = \frac{1}{60 \times 2 \times 10^{-9}} = 8{,}33$ MHz .

I used a quartz cristal of 8,3 MHz to generate the control pulses .

The analog switch has a quite low trshold voltage; as V_c reaches 1V it starts to conduct .When two switches are operated for multiplexing purposes we meet another problem because of the rise times of ϕ_1 and ϕ_2. They have the fallowing shape:

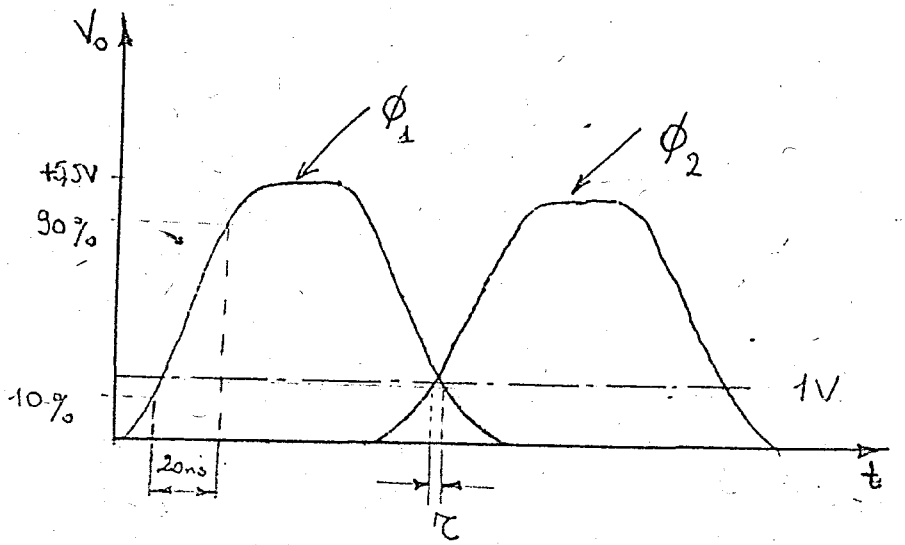


Fig 19 : Sampling pulses shape .

During τ both of the switches are slightly conducting . To overcome this difficulty I had the idea of clamping the bottom of the pulses to a negative voltage and thus the common part of the two signals was minimized .

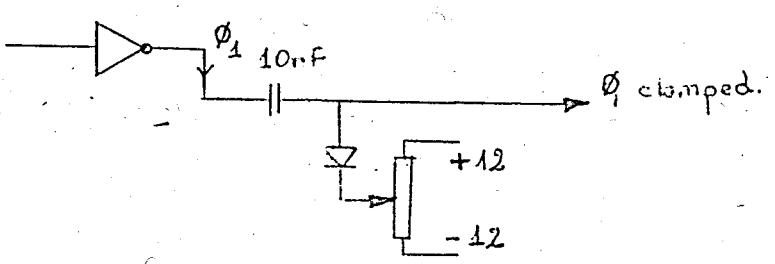


Fig 20 : Clamping of the sampling pulses .

The same clamping is used for ϕ_2 .

Another disturbing factor is the insertion of the clock pulses to the conduction channel at high clock frequencies even with grounded input .

R_{ON} resistance of the AS changes from Mega ohms to 300 Ω when V_C varies from 0 V to $V_{C\ max}$ .This variation is not very abrupt; especially at the negative going edge of the pulse the resistance of the channel increases as V_C deceases.This fact brings additional delay for the high frequencies . The delays are not negligibile when they are compared with the multiplexing time .

Because of the diffusion of the informations of AS_1 into the informations of AS_2 in time , it is not possible to recognise them completely at the receiving end even after an accurate time compensation of the regenerated sampling pulse .

Especially , high frequency components coming from the sharp edges of the picture are appearing as peaks on the other channel . This interaction of the two channels is a serious disturbing factor. To minimize this effect , the sampling frequency is lowered to 7,2 MHz, 5,950 MHz and 4,8 MHz .The effect of the interaction decreased gradually but remained in a innactable range .

As the essential idea is to send two pictures simultaneously on the same video path without using frequency multiplexing I. had

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Propagation Delay Time (V_{SS} = 0 Vdc)	7	tPLH, tPHL	5.0	15	30	45	ns
V_{in} to V_{out}			10	7.0	10	15	
(V_C = V_{DD}, R_L = 1.0 kΩ)			15	6.0	7.5	12	
Control to Output	8		5.0	34	60	90	ns
(V_{in} < 10 Vdc, R_L = 1.0 kΩ)			10	20	30	45	
			15	15	23	35	
Crosstalk, Control to Output (V_{SS} = 0 Vdc)	9	–	5.0	30	–	–	mV
(V_C = V_{DD}, R_{in} = 1.0 kΩ, R_{out} = 10 kΩ)			10	50	–	–	
			15	100	–	–	
Crosstalk between any two switches (V_{SS} = 0 Vdc)	–	–	5.0	–80	–	–	dB
(R_L = 1.0 kΩ, f = 1.0 MHz, crosstalk = $20 \log_{10} \frac{V_{out1}}{V_{out2}}$)							
Maximum Control Input Pulse Frequency (V_{SS} = 0 Vdc)	–	–	5.0	5.0	–	–	MHz
(R_L = 1.0 kΩ)			10	10	–	–	
			15	12	–	–	
Noise Voltage (V_{SS} = 0 Vdc)	10,11	–	5.0	24	–	–	nV/√Cycle
(V_C = V_{DD}, f = 100 Hz)			10	25	–	–	
			15	30	–	–	
(V_C = V_{DD}, f = 100 kHz)			5.0	12	–	–	
			10	12	–	–	
			15	15	–	–	
Sine Wave (Distortion) (V_{SS} = -5 Vdc)	–	–	5.0	0.16	–	–	%
(V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)							
Power Loss (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = –5 Vdc,	12	–	5.0				dB
RMS centered @ 0.0 Vdc, f = 1.0 MHz)							
loss = $20 \log_{10} \frac{V_{out}}{V_{in}}$)							
(R_L = 1.0 kΩ)				2.3	–	–	
(R_L = 10 kΩ)				0.2	–	–	
(R_L = 100 kΩ)				0.1	–	–	
(R_L = 1.0 MΩ)				0.05	–	–	
Bandwidth (–3 dB)	12,13	BW	5.0				MHz
(V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = –5 Vdc, RMS centered @ 0.0 Vdc)							
(R_L = 1.0 kΩ)				84	–	–	
(R_L = 10 kΩ)				60	–	–	
(R_L = 100 kΩ)				37	–	–	
(R_L = 1.0 MΩ)				37	–	–	
Control Input (V_{SS} = –5 Vdc)	–	–	5.0				kHz
(V_C = V_{SS}, 20 $\log_{10} \frac{V_{out}}{V_{in}}$ = –50 dB)							
(R_L = 1.0 kΩ)				1200	–	–	
(R_L = 10 kΩ)				180	–	–	
(R_L = 100 kΩ)				16	–	–	
(R_L = 1.0 MΩ)				2.0	–	–	

*The formula is for the typical characteristics only.

TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 4 – V_{SS} = –5.0 V AND –7.5 V

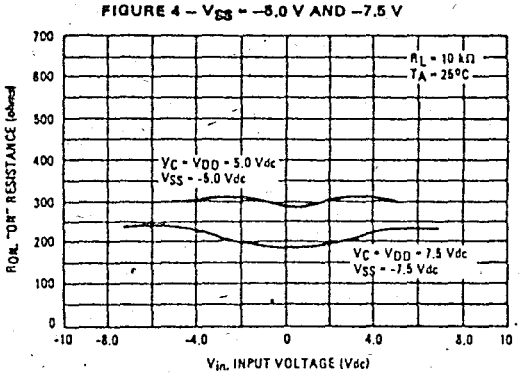


FIGURE 5 – V_{SS} = 0 V

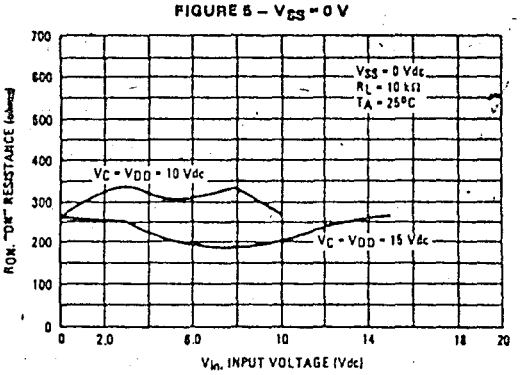


Fig 21

ELECTRICAL CHARACTERISTICS

Characteristics	Figure	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage# Control Input	1	V_{IL}	5.0	–	–	–	1.5	0.9	–	–	Vdc
			10	–	–	–	1.5	0.9	–	–	
			15	–	–	–	1.5	0.9	–	–	
		V_{IH}	5.0	–	–	2.0	3.0	–	–	–	Vdc
			10	–	–	6.0	8.0	–	–	–	
			15	–	–	11	13	–	–	–	
Input Current (AL Device) Control	–	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device) Control	–	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance	–	C_{in}									pF
Control			–	–	–	–	5.0	–	–	–	
Switch Input			–	–	–	–	5.0	–	–	–	
Switch Output			–	–	–	–	5.0	–	–	–	
Feed Through			–	–	–	–	0.2	–	–	–	
Quiescent Current (AL Device)	2,3	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)			10	–	0.50	–	0.0010	0.50	–	15	
			15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	2,3	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)			10	–	2.0	–	0.0010	2.0	–	15	
			15	–	4.0	–	0.0015	4.0	–	30	
"ON" Resistance (AL Device)	4,5,6	R_{ON}									Ohms
(V_C = V_{DD}, R_L = 10 kΩ)											
(V_{in} = +5.0 Vdc)			5.0	–	600	–	300	660	–	960	
(V_{in} = −5.0 Vdc) V_{SS} = −5 Vdc				–	600	–	300	660	–	960	
(V_{in} = ±0.25 Vdc)				–	600	–	280	660	–	960	
(V_{in} = +7.5 Vdc)			7.5	–	360	–	240	400	–	600	
(V_{in} = −7.5 Vdc) V_{SS} = −7.5 Vdc				–	360	–	240	400	–	600	
(V_{in} = ±0.25 Vdc)				–	360	–	180	400	–	600	
(V_{in} = +10 Vdc)			10	–	600	–	260	660	–	960	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	600	–	310	660	–	960	
(V_{in} = +5.6 Vdc)				–	600	–	310	660	–	960	
(V_{in} = +15 Vdc)			15	–	360	–	260	400	–	600	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	360	–	260	400	–	600	
(V_{in} = +9.3 Vdc)				–	360	–	300	400	–	600	
"ON" Resistance (CL/CP Device)	4,5,6	R_{ON}									Ohms
(V_C = V_{DD}, R_L = 10 kΩ)											
(V_{in} = +5.0 Vdc)			5.0	–	610	–	300	660	–	840	
(V_{in} = −5.0 Vdc) V_{SS} = −5 Vdc				–	610	–	300	660	–	840	
(V_{in} = ±0.25 Vdc)				–	610	–	280	660	–	840	
(V_{in} = +7.5 Vdc)			7.5	–	370	–	240	400	–	520	
(V_{in} = −7.5 Vdc) V_{SS} = −7.5 Vdc				–	370	–	240	400	–	520	
(V_{in} = ±0.25 Vdc)				–	370	–	180	400	–	520	
(V_{in} = +10 Vdc)			10	–	610	–	260	660	–	840	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	610	–	260	660	–	840	
(V_{in} = +5.6 Vdc)				–	610	–	310	660	–	840	
(V_{in} = +15 Vdc)			15	–	370	–	260	400	–	520	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	370	–	260	400	–	520	
(V_{in} = +9.3 Vdc)				–	370	–	300	400	–	520	
Δ"ON" Resistance	–	ΔR_{ON}									Ohms
Between any 2 circuits in a common package											
(V_C = V_{DD})											
(V_{in} = ±5.0 Vdc) V_{SS} = −5 Vdc			5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc) V_{SS} = −7.5 Vdc			7.5	–	–	–	10	–	–	–	
Input/Output Leakage Current (V_C = V_{SS})	–	–									nAdc
(V_{in} = +5.0, V_{out} = −5.0 Vdc)			5.0	–	±125	–	±0.001	±125	–	–	
(V_{in} = −5.0, V_{out} = +5.0 Vdc)			5.0	–	±125	–	±0.001	±125	–	–	
(V_{in} = +7.5, V_{out} = −7.5 Vdc)			7.5	–	±250	–	±0.0015	±250	–	–	
(V_{in} = −7.5, V_{out} = +7.5 Vdc)			7.5	–	±250	–	±0.0015	±250	–	–	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
*T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Input Voltage Specified as the voltage required at the Control Input for a 10 μA current through the transmission gate with an Input-to-output stress of V_{DD}−V_{SS} for V_{IL} and V_{IH}.

NOTE: All unused control inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

Fig 22 •

FIGURE 6 – R_{ON} CHARACTERISTICS TEST CIRCUIT

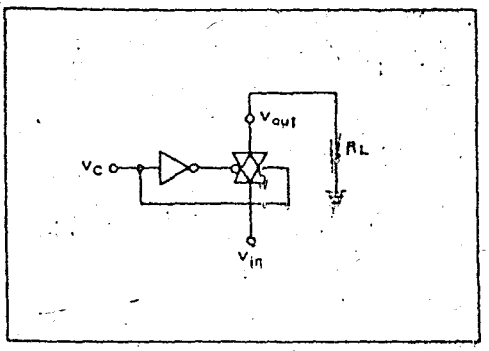


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

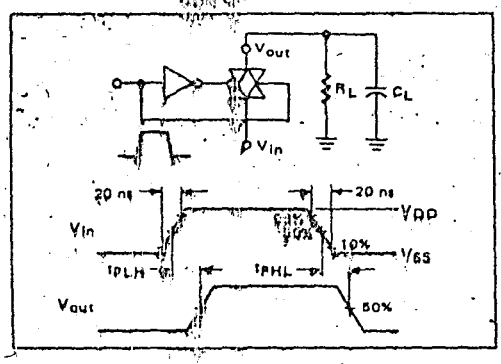


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

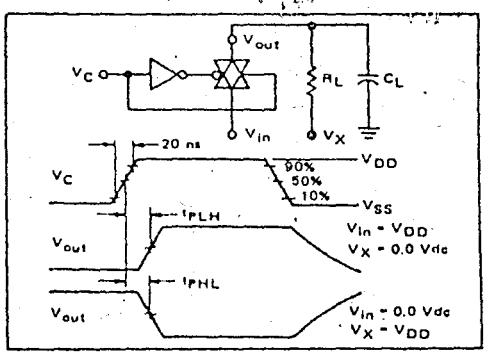


FIGURE 9 – CROSSTALK TEST CIRCUIT

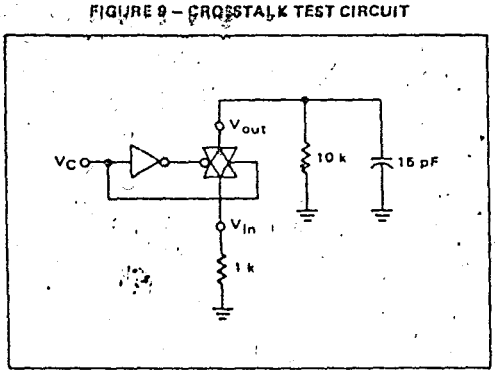


FIGURE 12 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS

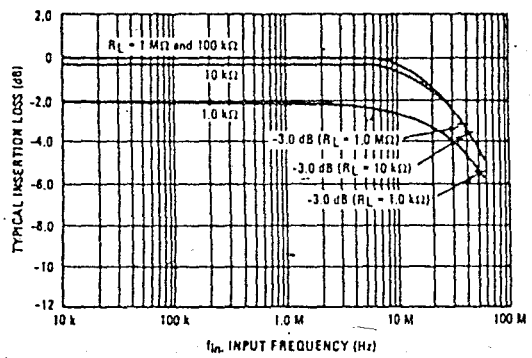


Fig 23 .

the idea of doing that at the beginning of each line . Thus , only $\frac{1}{2}$ of the lines of a picture are sent.The vertical detail is reduced but the picture is still visible and there is no interaction between the channels . 3I2,5 lines of picture A and other 3I2,5 lines($\frac{625}{2}$) of the picture of of channel B are active .

As the AS is in ON position during 1 horizontal line period (64μs) the frequency band width is not limited ; all the details of the line are transmitted.The delay has no disturbing effect since the times involved now are of the order of μs . Two consecutive informations are separated by the horizontal blanking interval of 4,5μs which is very large with respect to the delays (10-30 ns)

The ON resistance (R_{ON}) of the analog switch depends on the control voltage but varies also with the amplitude of the incoming signal . Fig 21 illustrates the variation of R_{ON} with V_{IN} . For $V_{DD} = V_C = 10$ V R_{ON} varies from 270Ω to 320Ω. We can say that $R_{ON} = 295\Omega \pm 25\Omega$.

$$\frac{\Delta R_{ON}}{R_{ON}} = 0,084$$

The variation of R_{ON} with V_{IN} introduces an amplitude distortion, a nonlinearity of the video signal (max luminance distortion of 8,4 %.

In TV engineering it is desirable to have linear circuits however this is not always possible . To overcome the nonlinearity correction circuits (such as γ correctors) are inserted all along the video path . Since the system will be used only for monitoring purposes (and not for broadcasting) this amount of nonlinearity is acceptable .

Consequences of the characteristics of the AS :

It can be used as a single high seed sampling gate where the sampled signal does not change appreciabbly during the sampling period . This switch can be used as the Switching element for video trick mixers.

It is suitable for multiplexed telephone switch board inter junction circuits . But , it can not be used for high speed video multiplexing becaeuse of the delays .

Part Three

Results And Application Areas

The original idea was to send two video signal in the same frequency spectrum .Thus , the frequency multiplexing division methode was rejected .In this case the only solution was to use time multiplexing division .

The most elegant application would be high speed sampling and multiplexing ; the characteristics of the analog switches were not satisfactory .

According to the sampling theorem the sampling frequency f_s should satisfy :

$$f_s \geqslant 2xf_{max}$$

f_{max} is the highest frequency component that one wishes to have in the spectrum after sampling . As the video information contains components up to 5MHz f_s should be 10 MHz .Because of the factors explained in the AS characteristics section f_s was selected to be 8,3 MHz , accepting a decrease of amplitude of 5MHz components . But , asa a result of the problems mentioned in the previous sections a switching at horizontal line frequency is adopted .

In this sampling method only half of the lines are sent; the vertical resolution is deceased. The picture has less vertical detail

but horizontal wise it has the complete spectrum from very low frequencies to 5MHz .The two pictures are properly separated ; no inter action exists.

This picture is certainly not for broadcasting purposes but it can be used in several areas :

a) In a professional TV studio the cameras are connected to the central commend unit (CCU) via a cable which contains conductors for the DC remote controls and coaxial cables for pulses and video signals .One of the coaxial cables brings back the composite video to the viewfinder of the camera . As there is only one return video path the cameraman see only the picture of his camera . When special effects are used the cameraman wishes to see the output of the mixer to adjust properly the relative position of his camera . This system can be inserted in the camera and in the CCU allowing the cameraman to see (to select) the two pictures .

The horizontal pulse exists in the camera head as well as in CCU .This brings an additional facility for syncronisation of the sending and receiving ends. 12 V supply voltages also are generally present in the camera units. So the system can be reduced to one board which can be inserted in the camera units .

b) To control large industrial complexes , closed circuit TV (CCTV) is widely used .Cheap vidicon cameras are prefered for CCTV

The multiplexed signal can be sent by radio link and demultiplexed at the output of the receiver .

The multiplexed signal can be recorded on Video Tape Recorder (VTR) . Since only the video above the black level (BA) is switched , the syncronisation pulses are present at the multiplexed output; no syncronisation problem occurs for the control track of the VTR .

The multiplexing operation can be bypassed by appling continuous DC to one of the control phase on both ends .

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