THESIS

FOR REFERENCE

NOT ... THIS ROOM

ROM-RAM PROGRAMMABLE

DIGITAL IC TESTER

by

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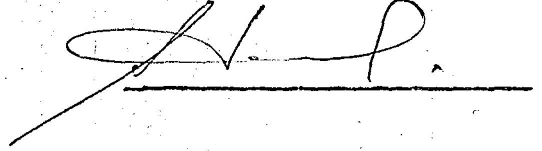

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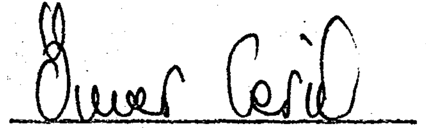

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ABSTRACT

In this thesis, the design of a ROM-RAM programmable digital IC tester by using a microcomputer system has been investigated.

The tester is a compact automatic test instrument that interrogates the parametric and functional performance of a wide variety of digital ICs.

However, the hardware design of the microcomputer part of the tester is excluded from the study, because of economical considerations. A microcomputer system, which was constructed beforehand, has been employed.

ÖZET

Bu tezde, mikroişlemci kullanılarak lojik entegre devreleri test edebilen bir cihaz tasarımı araştırılmıştır. Test programları ROM veya RAM hafıza elemanlarına yazılabilmektedir.

Test cihazı birçok lojik entegre devreleri test edebilmektedir. Test esnasında fonksiyonel ve parametrik değerler otomatik olarak kontrol edilmektedir.

Cihazın bir bölümünü teşkil eden mikroişlemcinin meydana getirilmesi, ekonomik düşünceyle tez çalışmasına dahil edilmemiştir. Daha önceden yapılmış bulunan bir mikroişlemci kullanılmıştır.

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INTRODUCTION

When a component fails in a piece of electronic equipment, locating and replacing it can be a costly process requiring a skilled technician. To reduce the possibility of such failures, components are subjected to various tests before they are assembled into equipment. However, no matter how complete a manufacturer's production tests are, a certain percentage of the components shipped will be found to be defective when they arrive at their destination. Therefore an IC tester becomes an essential test equipment to avoid such failures.

Besides performing the appropriate logical function, digital integrated circuits must meet input, output, and power supply voltage and current specifications, and propagation, rise, and fall time specifications. Although there are automatic systems that test all of these parameters, they are too complex and costly for most equipment manufacturers' incoming inspection departments. Less costly is the approach most often taken: each circuit is tested functionlly and its voltage and current parameters are checked.

Tester that do this kind of inspection are usually programmed to test different types of integrated circuits in one of two ways. Some use interchangeable printed circuit boards

or cards. Others are programmed by setting limit voltages and currents on thumbwheel switches and making connections to the device under test by means of a pushbutton matrix. The former method has the disadvantage that with the many thousands of different integrated circuits available today the program card library can become large and expensive. The latter method isn't well suited for use by unskilled personnel on a production basis. Also, a number of different tests can't be made easily on the same device.

Software programming can eliminate all of these disadvantages. Testers that are fully software programmed are only now becoming available.

In this thesis, a microcomputer controlled ROM-RAM programmable digital IC tester has been realised. An external microcomputer has been used as a part of the whole system. The microcomputer part was designed and built by Dr. Ömer CERİD.

A broad spectrum of logic families, including ECL, CMOS, TTL, RTL and DTL can be tested. Maximum test voltage is 5 volts, and maximum 16-pin capability is available. Testing is performed automatically according to the test program. Each IC is tested functionally, and its voltage and current parameters are checked.

Testing starts with the user informing the identity of the Unit Under Test (UUT) to the tester. The tester will then find the proper test program from the ROM memories for that UUT. If the proper test program is not available in the ROM, the program

must be written into the RAM memories with the teletypewriter. Once, the proper test program is ready, the IC to be tested is plugged into the socket and the start button is pressed. Then, the test system will read and interpret the instructions for the first test. If the first test is within the limits specified for that test the microcomputer will instruct the system to seek the next test in the "go-chain" sequence. If the test result is beyond the specified limits, a failure signal on the tester is produced, and the testing will end. As long as the results of each test are within limits, the tester will continue its operation until every test in the go-chain sequence has been performed. At this time the testing will terminate and a pass signal on the tester is produced.

In Chapter 1, a detailed information about automatic test systems used in industry is given. Chapter 2 introduces information about digital integrated circuits. Chapter 3 gives some economic considerations of IC testing. In Chapter 4, the implementation of the tester is described. Chapter 5 introduces the programming and testing process. The conclusion is given in the last chapter.

CHAPTER 1

AUTOMATIC TEST SYSTEMS USED IN INDUSTRY[8]

An automatic test system is composed of parts that are basically measurement and test instruments. The instruments used in the automatic test system must be automatically programmable. Another characteristic of an automatic test system is that it requires its test instruments to be capable of being connected in any desirable electrical configuration by the test systems switching matrix. The final requirement of a test system is that it have some type of man-machine interface such as a printer or visual display.

1.1 TEST SYSTEM DECISIONS

The user or developer of an automatic test system (ATS) must make two major decisions. First, he must decide if he will perform the necessary testing manually or automatically. Second, he must decide upon a specific test approach or method.

The first decision, manual or automatic, is usually easier to arrive at than the second and is related to characteristics of the tested item. There already exists a large body of data describing the advantages of automatic testing as compared to manual testing. These include 1) greater speed in performing tests 2) decrease in operator skill levels required to perform testing

with commensurate reduction in training costs, 3) test results independent of individual operator skills, 4) test sequence and tolerances more consistently performed and increasing confidence in test results.

Assuming that the user is attracted enough by these advantages to select the automatic test, he must then determine the type of ATS he will use. This decision is no less crucial than the first, not only because this decision will play a significant part in determining the magnitude of the investment that is necessary, but more importantly because selection of the proper test system determines the ultimate utility and satisfaction the user will derive.

1.2 WHAT IS AUTOMATIC TESTING?

The simplest way to describe automatic testing is to compare it to manual testing. Manual testing is usually performed by collecting individual pieces of test equipment, including measurement devices, special-purpose signal generators, power supplies, decade boxes, and a collection of clip leads. The test technician must plug in, set up, and connect all of this equipment to the unit under test (UUT) to make the tests. Other manual test equipment may interconnect the individual components in such a way that the operator performs these functions with simple switches. Normally, numerous tests are involved requiring the configurations and connections to be changed many times. Some sort of manual or set of ins-

tructions will normally be available to help the technician perform the tests. However, these instructions may not be complete or clear and usually will not be all inclusive. For example, the procedures or operations required to isolate a failure are too varied to allow specific instructions for every possibility, thereby lending uncertainty to the test and/or repair process.

In order to alleviate the multiple problems engendered by manual test procedures, the electronics industry's attention turned to automating the testing process. A typical ATS block diagram is shown in Fig.1. It can be noted that the major ingredients required to

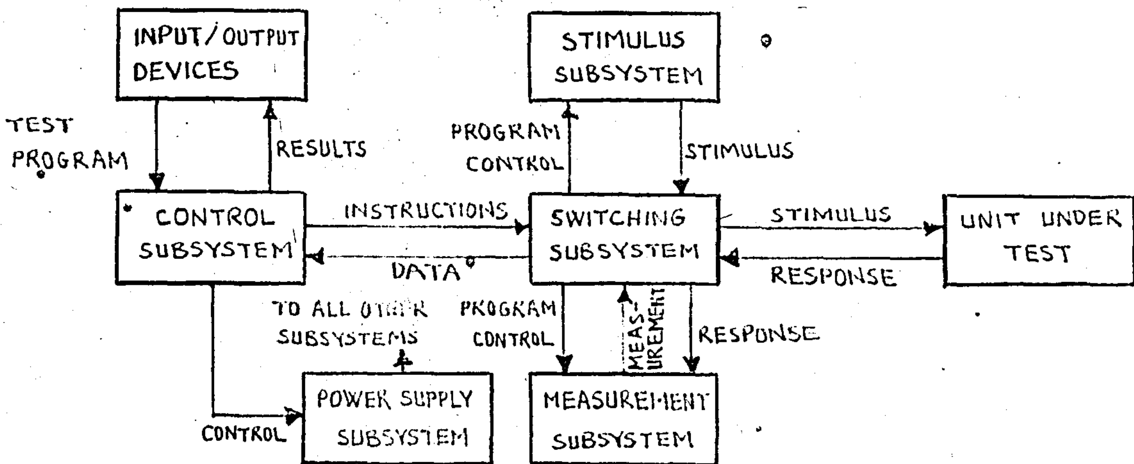

Fig.1. Block diagram of a typical ATS.

perfom manual testing are available within the ATS. There are power supplies, stimuli, measurement devices, and a switching system to allow the equipment to be arranged in desirable cofigurations. The instruction manual is replaced by a program tape that instructs the computer to carry out test instructions in the proper sequence, judge test results, and perform calculations. The requirement for

writing test results is performed by a printer. The keyboard and test results display have two functions: 1)to provide a means for man-machine communication within the testing process and 2) to provide the functional flexibility required in validating new test system programs. It is often necessary to use the test system operator to adjust a potentiometer, recognize if a lamp is on or off, or change the position of a switch. The printer is used to inform the operator of the action required, the display to indicate the parameter he must adjust to, and the keyboard to allow the operator to inform the test system that he has performed a necessary operation or to make a positive or negative response.

1.3 TEST SYSTEM OPERATION

Generally, operation of an ATS starts with the operator informing the test system of the identity of the UUT either on the keyboard or by control switches. The test system will then seek the proper test program for that UUT and (usually) verify through keying or other means that the UUT has been correctly identified. This is necessary to avoid damage to the test system and UUT due to operator error.

Once the UUT identity is verified, testing will begin. The test system will read and interpret the instructions for the first test. These instructions will set up switching to connect stimulus and power to proper points on the UUT; they will also set up connections between a measurement point and measurement device. Control signals on the test tape automatically program the measure-

ment devices to the proper scales and set the stimuli to the requ-ired voltage, frequency, slope, etc. A measurement command then will cause a measurement at the UUT test point. This measurement is transferred to the computer and compared against predetermined mea-surement criteria, which are also part of the test information. If the measurement is within the limits specified for that test the computer will instruct the system to seek the next test in the "go -chain" sequence. If the measurement is beyond the specified limits the computer will instruct the system to either halt and print that the UUT is defective, or direct the system to branch to a fault-isolation test sequence associated with that failure. In the case of a fault-isolation branch, testing will continue until some requ-ired fault-isolation level has been reached. As long as the results of each test are within limits, the test system will continue to rearrange switching, vary stimulus, change measurements, and eva-luate the results of each test in the go-chain sequence has been performed. At this time the testing will terminate and the test system will print out that the UUT is good. Thus the basic requ-irements for configuring an ATS are as follows.

1) A computer or controller to direct and control the testing process as well as interpret and evaluate test results.

2) Stimulus devices such as power supplies, signal generators, or pulse generators that can be automatically programmed to pro-vide required amplitudes, pulsewidths, frequencies, and other in-puts required to perform testing.

3) Measurement devices that can be programmed for the required

ranges and scales needed to carry out testing.

4) A switching device to interconnect (under program control) the UUT to the proper stimulus and measurement devices.

5) Peripheral devices such as printers and displays to provide a man-machine interface to the degree required by the user. The sophistication of the peripheral devices will depend greatly upon the use for which the test system is planned.

6) Tape reader or equivalent device for loading the UUT program into memory. The requirements for and size of this unit are also dependent upon the test system's use. If the system is required to test a small number of UUTs it may be possible to keep all the UUT programs resident in memory. As the number and size of the UUTs grow larger it becomes necessary to store these programs on some medium and read them into the test system as they are required.

7) Computer programs to direct the testing operations.

8) Accessories and signal conditioners as required for specific test problems.

1.4 INTEGRATED TEST SYSTEMS

An integrated test system is composed of separable functional elements. For example, if the test system multimeter were removed from the system, the multimeter could still perform its function

of making measurements under manual control; similarly the pulse generator could be removed and used in a manual test situation if necessary. Each element can operate independently of the remaining system elements as an entity.

This type of test system is quite common and is usually configured under two basic concepts. Either separate programmable test system entities are selected and modified to operate on a common data bus, or separate device controllers are used to act as an interface between the devices and data bus making them appear compatible to each other. In developing an integrated ATS it is desirable and sometimes possible to select devices from various suppliers that are already compatible and that meet the system test capability requirements. However, this fortuitous opportunity seldom presents itself; usually the compatibility and capability necessary for a dependable, accurate system must be engineered. An integrated system offers the following advantages to the user.

Advantages:

1. Wide Selection of Vendors from Whom to Select the Test System Building Block Components: The wide selection of vendors allows the user/developer configuring an integrated ATS to carefully select the elements of their system to optimally meet the requirements indicated by test requirement analysis and tradeoffs.

2. Expandable Capability Through Addition or Deletion of Building Block Components: The nature of an integrated ATS can

often make modification or expansion of its parameter envelope less difficult than what would be required in attempting this change on a dedicated system.

3. <u>The Initial Engineering Design and Development Costs May Be Lower</u>: This advantage refers to hardware rather than software expense.

Some of the disadvantages of the integrated automatic test system are the following:

1. <u>Hidden Development Cost</u>: Development of the integrated ATS includes an initial engineering outlay for integration. The size of this expense is seldom predicted accurately because the problems that will be encountered when attempting to join the individual elements into a single operational system cannot be easily identified in advance.

2. <u>Inefficient Utilization of Components</u>: The building blocks selected for incorporation into an integrated ATS usually are designed for general purpose applications and thus will have capabilities beyond the requirements of the test system itself. The inefficiency of unused capability as well as reduced system reliability due to the presence of unnecessary failure mode cadidates can prove troublesome.

3. <u>System Size Is Greatly Increased</u>: Because the packaging of the integrated ATS building blocks is not specifically designed for use in a system environment, a great deal of additional space is required.

4. <u>Increased Maintenance Requirements</u>: Maintenance considerations of an integrated ATS is a drawback because the self-diag-

nostic capability of an ATS is somewhat circumvented when the system is composed of individual programmable components.

1.5 DEDICATED TEST SYSTEMS

A dedicated test system is one that is specifically designed for a given task or class of tasks. The elements of this type of system, when separated from the system itself, cannot be used to provide characteristic system functions as they do when connected within the test system.

Normally, the system functions are configured from some type of standard modular devices arranged and connected for desired characteristics. The dedicated ATS has all the test characteristics of the integrated ATS. It is usually built about some selected computer that provides control and analysis, and it contains standard man-machine interface such as visual display, printer, and keyboard.

Advantages of This Type of System:

1. Greatly Reduced Size When Compared to Integrated Systems: The dedicated test system will usually occupy less than half the space required by an integrated ATS. When the space available for test and/or maintenance is limited, a dedicated ATS is often the only alternative.

2. Efficiency and Reliability Are Increased: The efficiency of a dedicated ATS is high because it contains only those functions required for the testing process; whereas, the integrated ATS will be configured from parts that usually possess capabilities and pa-

rameters well beyond the requirements of the test system itself. The reliability as defined by its mean time between failures may also be increased merely through elimination of failure modes in superfluous circuitry.

3. Maintenance Is Simplified: By its nature the design of the dedicated test system lends itself to automated maintenance techniques. Development of stimulus measurement and switching subsystems through modularized elements designed for specific tasks allows recognition and isolation of failures with greater precision. This is because the modular design inherently has a large number of internal monitoring points available for self-diagnosis. The availability of these additional test points allows the designer of the self-test program to isolate a test system failure to a single or small number of modules.

4. Availability Is Higher: The mean time to repair for the dedicated system is shorter and hence, availability is greater than that of the integrated system due not only to the precision with which the failure can be identified but also due to the ease with which the failure can be corrected. The modular nature of the dedicated ATS lends itself to rapid removal and replacement of the suspect element or elements. This rapid repair is not possible with the integrated ATS because removal tends to be difficult and it is too expensive to carry replacement spares on a building block basis.

5. Special Testing: Often when requirements are unique or when testing is necessary to check uncommon UUT parameters, a dedicated system is the only ATS solution.

Dedicated Test System Disadvantages:

1. Cost: The development cost of a dedicated ATS tends to be greater than that of an integrated system. The difference between the two will be less than that implied by comparing the component acquisition costs of an integrated ATS with design and development costs of dedicated ATS. There are subtle and somewhat hidden engineering expenses associated with developing an integrated ATS, such as the costs for compatibility devices and modification of the ATS building block elements, and the added expense to develop a more complex software package able to drive the diverse elements of the integrated system.

If the dedicated ATS is to be purchased rather than developed, the cost difference in acquiring the two types of system could become smaller.

2. In-House Requirements: Developing a dedicated ATS requires a broader pool of expertise and knowledge than is required of the purchaser of an integrated ATS. That is, the skill required for the design of the test system must be available within the developer organization. The risk is high that troublesome or inadequate design approaches could become incorporated into the test system unless the design group is carefully chosen and supervised. Errors so incorporated must slowly be modified out again as experience with the test system is gained. This process can prove costly, painful, and is not always entirely successful.

3. Limited Test Set Capability: The developer of a dedicated ATS must be very clear about what the system test capability must; the typical dedicated ATS will be especially designed for optimum

performance of a given task or class of tasks. This can be serious constraint if an error or miscalculation occurs when specifying system requirements. Modification of the dedicated system is of course possible, but the redesign tends to be expensive and sufficient space may not be available to incorporate necessary changes without mechanical redesign.

1.6 OTHER FACTORS

ATS are applied to many types of testing. Among these are: military and commercial test, production and support test, qualification and diagnostic test.

Military and Commercial Testing: Military test system must meet many criteria of reliability and maintainability that need not be considered when developing or purchasing a commercial system. Aside from the criticality of the military mission there are a number of unique logistics and training problems, which have no parallel in the commercial test world. The constraints imposed by the military test environment have led military procurement activities to depend heavily upon the dedicated ATS. This is due to the dedicated system's smaller size, ease of maintenance, and amenability to closely specified and controlled tolerances that can be oriented toward the military misson.

Commercial test systems cover a scope nearly as broad as military system. These systems range from the very simple to the very complex and from direct comparison techniques utilizing the 'known

good unit' to comparison based upon detailed circuit analysis. Generalities regarding commercial test system are difficult to formulate. However, it can be said that commercial tests systems tend to be more task oriented than general purpose.

Production Versus Support Testing: Production or factory testing is performed as part of the quality control function at interim stages or at the end of a production line. This type of testing becomes part of the production process and production efficiency.

The factory test system is usually an integrated ATS, often configured in large part from available factory test equipment. The length of the production run and the test precision required are critical factors when determining the test system requirements. In many cases only slight modification, electrical or mechanical, is necessary to adapt a previously used test system to a new production run.

The repetitive nature of production line tests allows use of components that need not be as software flexible as those in a test environment where the testing requirements vary. The test process on the production line can use a relatively simple device designed to solve a single well-defined test problem. Often manual test equipment with minor modification and appropriate computer or controller interface can be used to configure this type of tester.

The reliability of the factory ATS must be high and the mean time to repair relatively low to avoid shutdown of the production process due to an inability to test. Thus, this type of system must be designed to allow for rapid identification of failed components,

easy replacement, i.e., repairability, and with an adequate number of spare building blocks so that production need not be delayed.

The requirement that factory ATS have high reliability and be easily maintainable sound very much like the requirements listed for the military ATS. The difference between the two are matters of approach and degree. The factory ATS is configured to less stringent environmental standards than the military ATS.

Support testing usually takes place at remote or field locations. It is used to provide secondary level maintenance on prime hardware, reducing the repair time required and thereby lowering the spares level necessary for any given hardware item. The consequence of a failure is less immediate for a support ATS than it is for a factory ATS because the support ATS is not part of the on-line process it is supporting. That is, the factory ATS is often part of the production process and can stop this process in a relatively short period of time if it is not available. The reliability requirements will depend upon the specific support needs of the ATS user. The support ATS often must test many different types of equipment as well as be able to provide support for various versions of similar units. This requires broad test capability as well as a flexible software package. In addition the support ATS should be designed to store many programs either as resident memory or in some convenient protective device that can be used to load programs easily into the system as they are required.

ATS characteristics for support testing are not easily categorized into the dedicated/integrated classification. The field site constraints, the type of equipment supported, the capability of

maintenance personnel, and the scope of the support misson all must be considered. Often hybrid systems are found where the concept of the integrated and dedicated system have been incorporated to meet optimally the specific support required.

Qualification and Diagnostic Testing: Qualification, go-no-go, or acceptance testing all refer to a test philosophy in which the UUT is examined only to determine if it is capable of meeting its specified performance parameters. No further testing is performed if the UUT fails to fall within the limits required by its performance criteria. It is either thrown away or moved to another test area where the cause of the malfunction is identified and corrected. Qualification testing is usually used for high-volume testing of low-value UUTs. The user/developer of an ATS for qualification test is usually primarily concerned with test speed and accuracy. This type of testing is often performed on large numbers of identical UUTs over long periods of time. Therefore, programming simplicity rather than flexibility is sought. Other desired qualities for this type of testing are a fairly sophisticated mechanical interface between the test system and the UUT. Finally, qualification testing allows utilization of a simple man— machine interface.

Diagnostic testing is required for more complex UUTs. The lowest level of these is the small printed-circuit board or a small assembly of only two or three components. The philosophy of this type of testing is to identify and replace a failed component to a level required in an established maintenance plan. For a printed-circuit board, this may be one or a number of component parts. For

an assembly, it may be a chassis or a printed-circuit board. Often an ATS will be required to provide both qualification and diagnostic capability.

Test system requirements for diagnostic testing call for a sophisticated software/hardware combination allowing for a flexible interactive man-machine interface. Communication between man and machine by a printer and keyboard is usually a minimum. Many times photo displays are required and the industry is now considering computer-controlled video terminals that can be used in conjuntion with light pencils and other operator-control devices to allow greater diagnostic capability and flexibility.

1.7 FUTURE TRENDS

Certain trends are becoming obvious for both the integrated and dedicated ATS. The system's size is decreasing . This decrease in size has been accompanied by an increase in system complexity, capability, and interactive characteristics of the test system elements.

The general purpose microcomputer is increasingly found at the heart of ATS. The availability of resident memory and utility of the software package appear to be the major factors in selecting the test system computer.

Multistation ATS in which microcomputers interface with and are controlled by large computers on a real time basis are presently being used very successfully in factory test of TV and computer circuitry. Other successful applications of this technique are found in monitoring of multiple remote phenomena at a centralized

station.

Configuration of test system and application of the test process is more and more becoming a system engineering problem in which entire subsystems rather than individual system elements are considered.

CHAPTER 2

INFORMATION ABOUT DIGITAL INTEGRATED CIRCUITS [1,2,3,4,5,9,10]

Almost all modern digital systems utilize digital integrated circuits (ICs) because they result in an increase in reliability and a reduction in weight and size. Digital IC technology has advanced rapidly from small-scale integration (SSI), with less than 13 equivalent logic gates per chip, through medium-scale integration (MSI), with between 13 and 99 equivalent logic gates per chip, to large-scale integration (LSI), which covers the range beyond 100 gates per chip. With the widespread use of ICs comes the necessity for becoming familiar with the characteristics of the most commonly used logic familes. (A logic family refers to a specific class of logic circuits that are manufactured using the same manufacturing techniques.) In this chapter we will examine the DTL, TTL, ECL, RTL, DCTL, I^2L, N-MOS, P-MOS, CMOS and SOS logic families.

The various logic families can be placed into two broad categories according to the IC fabrication process: bipolar and unipolar. The bipolar familes utilize the bipolar transistor (NPN and PNP) as their principle circuit element. DTL, TTL, ECL, RTL DCTL and I^2L are bipolar families. The unipolar families use MOS field-effect transistors (MOSFETs) as their principal circuit element. N-MOS, P-MOS, CMOS, and SOS are all unipolar logic families. The unipolar logic families are also called as MOS fami-

lies.

In general, the MOS families tend to be well suited for MSI and LSI devices because the MOS families require less chip area and consume less power than their bipolar counterparts. On the other hand, MOS families tend to operate at slower speeds than bipolar and require special handling and storage precautions.

2.1 DIGITAL IC TERMINOLOGY

Although there are many digital IC manufacturers, much of the nomenclature and terminology is fairly standardized. The most useful terms are defined and discussed below.

Current and Voltage Parameters

V_{IH} high-level input voltage: The voltage level required for a logical 1 at an input. Any voltage below this level will not be accepted as a HIGH by the logic circuit.

V_{IL} low-level input voltage: The voltage level required for a logical 0 at an input. Any voltage above this level will not be accepted as a LOW by the logic circuit.

V_{OH} high-level output voltage: The voltage level at a logic circuit output in the logical 1 state. The minimum value of V_{OH} is usually specified.

V_{OL} low-level output voltage: The voltage level at a logic circuit output in the logical 0 state. The maximum value of V_{OL} is usually specified.

I_{IH} high-level input current: The current that flows into an input when a specified high-level voltage is applied to that input.

I_{IL} low-level input current: The current that flows into an input when a specified low-level voltage is applied to that input.

I_{OH} high-level output current: The current that flows from an output in the logical 1 state under specified load conditions.

I_{OL} low-level output current: The current that flows from an output in the logical 0 state under specified load conditions.

Fan-Out

In general, a logic-circuit output is required to drive several logic inputs. The fan-out (also called loading factor) is defined as the maximum number of standard logic inputs that an output can drive reliably. For example, a logic gate that is specified to have a fan-out of 10 can drive 10 standard logic inputs. If this number is exceeded, the output logic-level voltages cannot be guaranteed.

Transition Times

Some digital circuits respond to logic levels at their inputs, but others are activated by the rapid change in voltage. In the latter circuit type it is essential that the input signals have sufficiently fast level transitions or the circuit may not respond properly. For this reason the rise time t_R and fall time t_F of a logic output is often specified. The values of t_R and t_F are not necessarily equal, and both are dependent on the amount of loading placed on a logic output.

Propagation Delays

A logic signal always experiences a delay in going through a circuit. The two propagation delay times are defined as

t_{PLH} :- delay time in going from logical 0 to logical 1 state (LOW to HIGH).

t_{PHL} ; delay time in going from logical 1 to logical 0 state (HIGH to LOW).

Figure 2.1 illustrates these propagation delays. Note that t_{PHL} is the delay in the output's response as it goes to the 0 state, and vice versa for t_{PLH}.

In general, t_{PHL} and t_{PLH} are not the same value, and both will vary depending on loading conditions. The values of propagation times are used as a measure of the relative speed of logic circuits. For example, a logic circuit with values of 10 ns is a faster logic circuit than one with values of 20 ns.

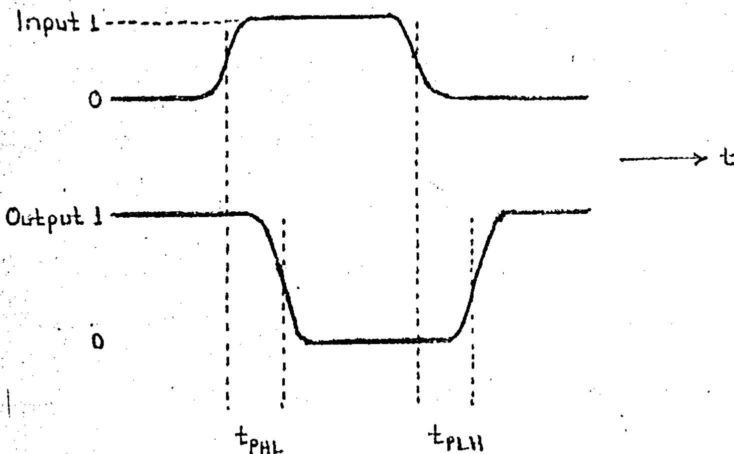

Figure 2.1 Propagation delays.

Power Requirements

The amount of power required by an IC is an important characteristic and is always specified on the manufacturer's data sheet. Sometimes it is given directly as average power dissipation P_D. More often it is indirectly specified in terms of the current drain from the IC power supply. This current is typically symbolized as I_{CC}. When the value for I_{CC} is known, the power drawn by the supply is obtained simply by multiplying I_{CC} by the power supply voltage.

For some ICs the value of supply current I_{CC} will be different for the two logic states. In such cases two values for I_{CC} are specified. I_{CCH} is the supply current when all outputs on the IC chip are HIGH; I_{CCL} is the supply current when all outputs are LOW.

Noise Immunity

Stray electrical and magnetic fields can induce voltages on the connecting wires between logic circuits. These unwanted, spurious signals are called noise and can sometimes cause the voltage at the input to a logic circuit to drop below V_{IH} (min) or rise above V_{IL} (max), which could produce unreliable operation. The noise immunity of a logic circuit refers to the circuit's ability to tolerate noise voltages on its inputs. A quantitative measure of noise immunity is called noise margin and is illustrated in Figure 2.2.

Figure 2.2(a) is a diagram showing the range of voltages that can occur at a logic circuit output. Any voltages greater than

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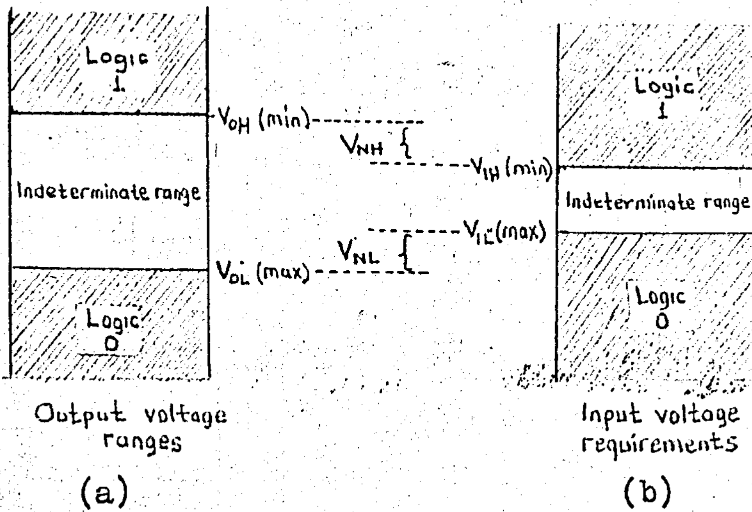


Figure 2.2 Noise margins.

V_{OH} (min) are considered a logic 1, and any voltages lower than V_{OL} (max) are considered a logic 0. Voltages in the indeterminate range should not appear at a logic circuit output under normal conditions. Figure 2.2(b) shows the voltage requirements at a logic circuit input. The logic circuit will respond to any input greater than V_{IH} (min) as a logic 1, and will respond to voltages lower than V_{IL} (max) as a logic 0. Voltages in the indeterminate range will produce an unpredictable response and should not be used.

The high-state noise margin V_{NH} is defined as

$$V_{NH} = V_{OH}(\text{min}) - V_{IH}(\text{min}) \tag{2.1}$$

as illustrated in Figure 2.2. V_{NH} is the difference between the lowest possible HIGH output and the minimum input voltage required for a HIGH. When a HIGH logic output is driving a logic circuit input, any negative noise spikes greater than V_{NH} appearing on

the signal line will cause the voltage to drop into the indeterminate range, where unpredictable operation can occur.

The low-state noise margin V_{NL} is defined as

$$V_{NL} = V_{IL}\,(max) - V_{OL}\,(max) \tag{2.2}$$

and it is the difference between the largest possible LOW output and the maximum input voltage required for a LOW. When a LOW logic output is driving a logic input, any positive noise spikes greater than V_{NH} will cause the voltage to rise into the indeterminate range.

AC Noise Margin

Strictly speaking, the noise margins predicted by expressions (2.1) and (2.2) are termed dc noise margins. The term "dc noise margin" might seem somewhat inappropriate when dealing with noise, which is generally thought of as an ac signal of the transient variety. However, in today's high-speed integrated circuits, a pulse width of 1 μs is extremely long and may be treated as dc as far as the response of a logic circuit is concerned. As pulse widths decrease to the low-nanosecond region, a limit is reached where the pulse duration is too short for the circuit to respond. At this point, the pulse amplitude would have to be increased to produce a change in the circuit output. What this means is that a logic circuit can tolerate a large noise amplitude if the noise is of a very short duration. In other words, a logic circuit's ac noise margins are generally substantially greater than its dc noise margins given by (2.1) and (2.2). Manufacturers generally

supply ac-noise-margin information in the form of a graph such as that in Figure 2.3. Note that the noise margins are constant for pulse widths greater than 10 ns but increase rapidly for narrower pulses.

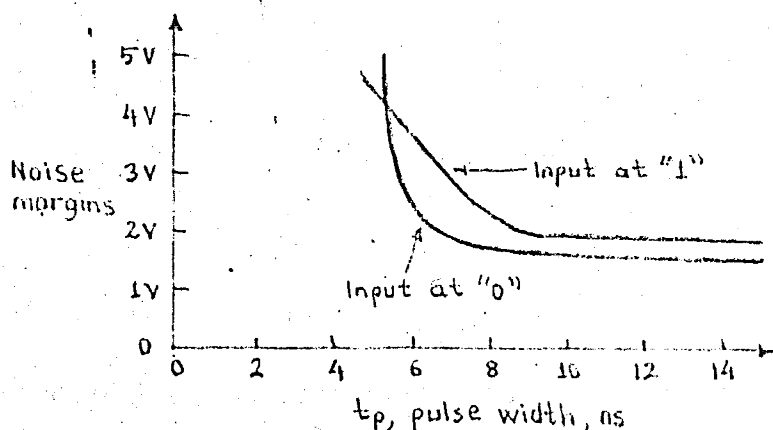
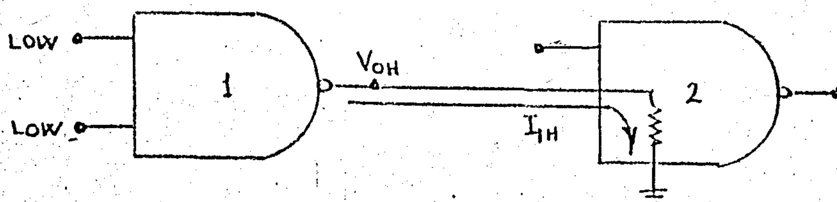


Figure 2.3 Typical ac noise-immunity graphs.

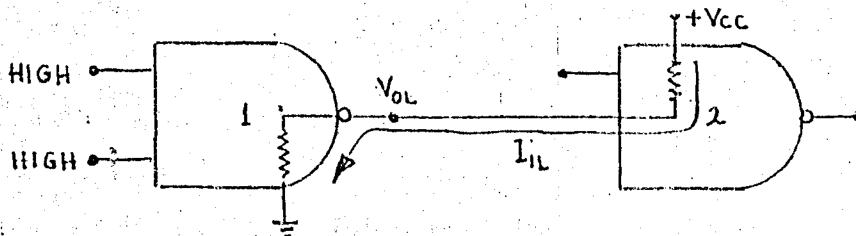
Current-Sourcing and Current-Sinking Logic

Logic families can be categorized according to how current flows from the output of one logic circuit to the input of another. Figure 2.4(a) illustrates current-sourcing logic. When the output of gate 1 is in the HIGH state, it supplies a current I_{IH} to the input of gate 2, which acts essentially as a resistance to ground. Thus, the output of gate 1 is acting as a source of current for gate 2 input.

Current-sinking logic is illustrated in Figure 2.4(b). Here the input circuitry of gate 2 is represented as a resistance tied to $+V_{CC}$, the positive terminal of a power supply. When the gate 1 output goes to its LOW state, current will flow in the direction



(a) Current sourcing.



(b) Current sinking.

Figure 2.4 Comparison of current-sourcing and current-sinking actions.

shown from the input circuit of gate 2 back through the output resistance of gate 1 to ground. In other words, in the LOW state the circuit driving an input of gate 2 must be able to sink a current, I_{IL}, coming from that input.

The distinction between current-sourcing and current-sinking logic circuits is an important one which will become more apparent as we examine the various logic families.

2.2 THE DTL LOGIC FAMILY

A typical DTL logic gate is depicted in Figure 2.5. This is called a DTL logic gate because it uses diodes at the inputs A and

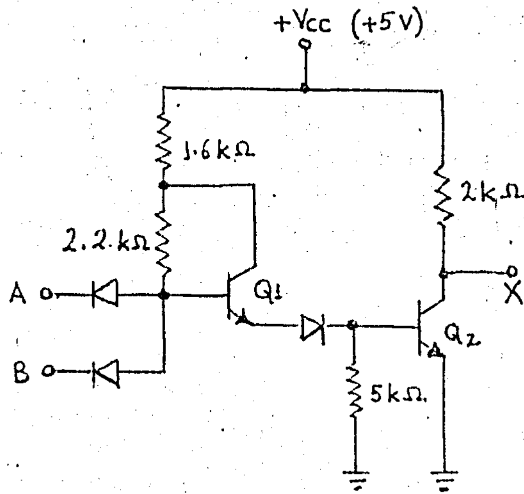


Figure 2.5 Basic DTL circuit.

B, and uses a transistor amplifier. This gate functions as a NAND gate for positive logic since all inputs must be HIGH in order to cause Q_2 to turn ON. If any input is LOW the base of Q_1 is clamped to a voltage near ground by the forward-biased diode. The drop across the emitter-base junction of Q_1 plus the drop across the following diode keeps the base of Q_2 negative and ensures that Q_2 is off for this condition. Typical levels for LOW state and HIGH state are 0.4 V and 2.4 V, respectively. The noise margins in either state are approximately 0.5 V. It has a fan-out of about 8. Typical power dissipation for a basic DTL gate is 10 mW. Propagation times are around 30 ns.

2.3 THE TTL LOGIC FAMILY

One of the most popular logic families at the present time is

the TTL family. Since the late 1960s this line has emerged as the most flexible and continues to be in great demand after the mid-1970s. This family possesses good fan-out figures and relatively high-speed switching. The Schottky-clamped TTL lowers switching times even further with propagation delay of gates in the area of two nanoseconds. The basic TTL gate is shown in Figure 2.6.

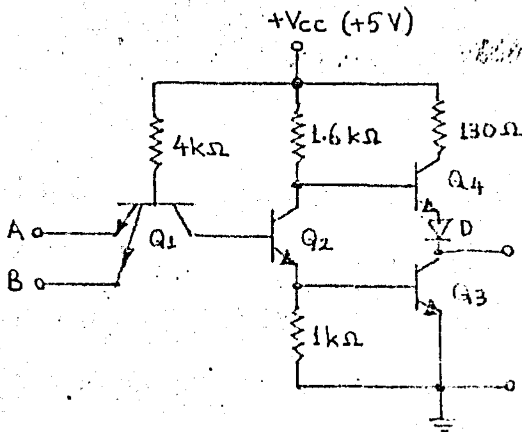


Figure 2.6 Basic TTL circuit.

The TTL family is based on the multiemitter construction of transistors which are easily and economically fabricated using integrated-circuit techniques. The operation of the input transistor can be visualized by the circuit of Figure 2.7, which shows the bases of the two transistors connected in parallel as are the collectors while the emitters are separate.

If all emitters are at ground level the transistors will be saturated due to the large base drive. The collector voltage will be only a few tenths of a volt above ground. The base voltage will equal $V_{BE(on)}$ which may be 0.5 V. If one of the emitter

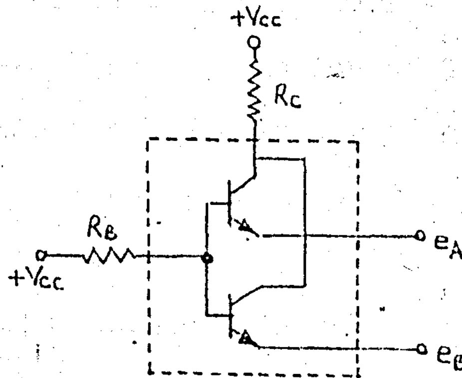


Figure 2.7 Discrete circuit equivalent
to the multiemitter transistor.

voltage is raised, the corresponding transistor will shut off. The transistor with an emitter voltage of zero volts still be saturated, however, and this will force the base voltage and collector voltage to remain low. If two emitters are raised to a higher level, the base and collector voltages will tend to follow this signal.

Returning to the basic gate of Figure 2.6 we see that the low logic level appears at one or more of the inputs, Q_1 will be saturated with a very small voltage appearing at the collector of this stage. Since at least $2V_{BE(on)}$ must appear at the base of Q_2 in order to turn Q_2 and Q_3 on, we can conclude that these transistors are off at this time. When Q_2 is off the current through the 1.6 kΩ resistance is diverted into the base of Q_4 which then drives the load as an emitter follower.

When all inputs are at the high voltage level, the collector of Q_1 attempts to rise to this level. This turns Q_2 and Q_3 on

which clamps the collector of Q_1 to a voltage of approximately $2V_{BE(on)}$. The base-collector junction of Q_1 appears as a forward-biased diode while the base-emitter junctions are reverse-biased diodes in this case. As Q_2 turns on the base voltage of Q_4 drops, decreasing the current through the load. The load current tends to decrease even faster than if only Q_4 were present, due to the fact that Q_3 is turning on to divert more current from the load. At the end of the transition Q_4 is off with Q_2 and Q_3 on. For positive logic the circuit behaves as a NAND gate.

This arrangement of the output transistors is called a totem pole. The output impedance of the emitter follower is asymmetrical with respect to emitter current. As the emitter follower turns on, the output impedance decreases. Turning the stage off increases the output impedance and can lead to distortion of the load voltage especially for capacitive loads. The totem pole output stage overcomes this problem as discussed in the preceding paragraph.

There are two standard methods of improving the high-speed switching characteristics of TTL. The first is to add clamping diodes to the input emitters of the gate to reduce transmission line effects by providing more symmetrical impedances. This improvement is shown in Figure 2.8 along with smaller resistors and a Darlington connection at the output. These gates exhibit a typical propagation delay time of 6 ns.

A very significant improvement in TTL switching speed results

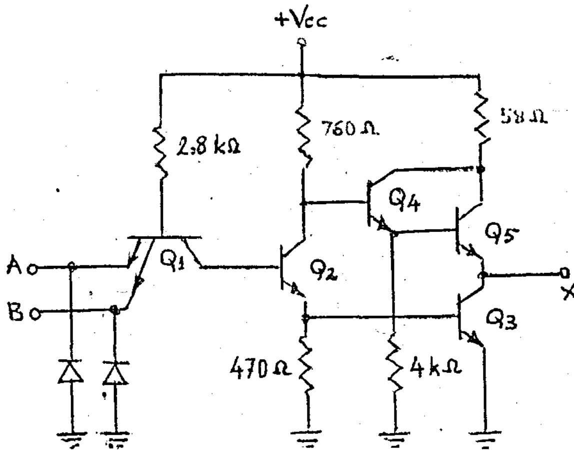


Figure 2.8 High-speed TTL gate.

from using Schottky barrier diodes to clamp the base-collector junctions of all transistors to avoid heavy saturation. Figure 2.9 shows the arrangement of the clamping diode.

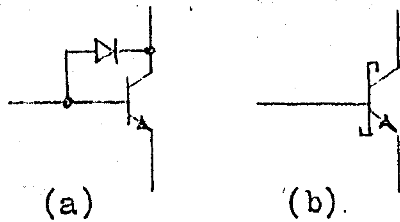


Figure 2.9 (a) Schottky-clamped transistor.
(b) Symbol for clamp.

The low forward voltage across the Schottky diode causes the diode to divert most of the excess base current around the base-collector junction. The transistor current can then decrease rapidly without the delay associated with excess base charge. The Schottky-clamped TTL gates exhibit propagation delay times of

two to three nanoseconds.

In 1964 Texas Instruments introduced the first standard product line of TTL circuits. The 5400/7400 series, as it is called, has been one of the most widely used families of IC logic. We will simply refer to it as the 7400 series since the only difference between the 5400 and 7400 versions is that the 5400 series is meant for military use and can operate over a wider temperature and power-supply range. Many IC manufacturers now produce the 7400 line of ICs, although some use their own identification numbers. For example, Fairchild has a series of TTL ICs, which uses numbers such as 9N00, 9300, 9600, and so on. However, on the Fairchild specification sheets the equivalent 7400 series number is usually indicated.

The 7400 series operates reliably over the temperature range 0-70° C and with a supply voltage (V_{CC}) of from 4.75 to 5.25 V. The 5400 series is somewhat more flexible since it can tolerate a -55 to -125° C temperature range and a supply variation of 4.5-5.5 V. Both series typically have a fan-out of 10, indicating that they can reliably drive 10 other inputs.

Table 2.1 lists the input and output voltage levels for the standard 7400 series. The minimum and maximum values shown are for worst-case conditions of power supply, temperature, and loading conditions. Inspection of the table reveals a guaranteed maximum logical 0 output $V_{OL} = 0.4$ V, which is 400 mV less than the logical 0 voltage needed at the input $V_{IL} = 0.8$ V. This means

Table 2.1 Standard 7400 Series Voltage Levels

	Minimum	Typical	Maximum
V_{OL}	-	0.2	0.4
V_{OH}	2.4	3.6	-
V_{IL}	-	-	0.8
V_{IH}	2.0	-	-

that the guaranteed LOW-state dc noise margin is 400 mV. That is,

$$V_{NL} = V_{IL}(max) - V_{OL}(max) = 0.8\ V - 0.4\ V = 0.4\ V = 400\ mV$$

Similarly, the logical 1 output V_{OH} is a guaranteed minimum of 2.4 V, which is 400 mV greater than the logical 1 voltage needed at the input $V_{IH} = 2.0$ V. Thus, the HIGH-state dc noise margin is 400 mV.

$$V_{NH} = V_{OH}(min) - V_{IH}(min) = 2.4\ V - 2.0\ V = 0.4\ V = 400\ mV$$

Thus, the guaranteed worst-case dc noise margins for the 7400 series are both 400 mV. In actual operation the typical dc noise margins are somewhat higher ($V_{NL} = 1$ V and $V_{NH} = 1.6$ V).

Standard TTL logic circuit draws an average supply current I_{CC} of 2 mA, resulting in a power dissipation of 2 mA $\times$ 5 V=10 mW. It has an average propagation delay of 9 ns.

Besides the standard 7400 series, several other TTL series have been developed to provide a wider choice of speed and power

dissipation characteristics. These are mentioned below.

Low-Power TTL, 74L00 Series

Low-power TTL circuits designated as the 74L00 series have essentially the same basic circuit as the standard 7400 series except that all the resistor values are increased. The larger resistors reduce the power requirements but at the expense of longer propagation delays. A typical NAND gate in this series has an average power dissipation of 1 mW and an average propagation delay of 33 ns.

The 74L00 series is ideal for applications in which power dissipation is more critical than speed. Low-frequency, battery-operated circuits such as calculators are well suited for this TTL series.

High-Speed TTL, 74H00 Series

The 74H00 series is a high-speed TTL series. The basic circuitry for this series is essentially the same as the standard 7400 series except that smaller resistor values are used and the emitter-follower transistor Q_4 is replaced by a Darlington pair. These differences result in a much faster switching speed with an average propagation delay of 6 ns. However, the increased speed is accomplished at the expense of increased power dissipation. The basic NAND gate in this series has an average P_D of 23 mW.

Schottky TTL, 74S00 Series

The 74S00 series has the highest speed available in the TTL

line. It achieves this performance by using a Schottky barrier diode connected as a clamp from base to collector of each circuit transistor. This reduces the average propagation delay to 3 ns for a typical NAND gate. The 74S00 series also uses smaller resistor values to increase switching speed. This produce an increase in average power dissipation to 23 mW per gate. Since it has essentially the same P_D as the 74H00 series while performing at a higher speed, it is the most widely used TTL series in applications where high speed is important.

Low-Power Schottky TTL, 74LS00 Series

Another Schottky-clamped TTL series uses larger resistor values to decrease power dissipation. The 74LS00 series has a typical P_D of only 2 mW per gate, which is the lowest for TTL except for the 74L00 series. The larger resistances cause an increase in propagation delay to approximately 9.5 ns. Thus, this series has about the same speed as the standard 7400 series while requiring much less power. This has resulted in the 74LS00 series starting to take over many of the applications areas previously dominated by the 7400 series. As the cost of 74LS00 devices continues to come down, it is probable that it will become the major TTL series.

2.4 THE ECL LOGIC FAMILY

The TTL logic family (with the exception of Schottky TTL)

uses transistor operating in the saturated mode. As a result, their switching speed is limited by the storage delay time associated with a transistor that is driven into saturation. Another bipolar logic family has been developed that prevents transistor saturation, thereby increasing overall switching speed. This logic family is called emitter-coupled logic (ECL), and it operates on the principle of current switching whereby a fixed bias current less than $I_{C(sat)}$ is switched from one transistor's collector to another. Because of this current-mode operation, this logic form is also referred to as current-mode logic (CML).

Figure 2.10 shows an ECL gate with two separate outputs. For positive logic X is the OR output while Y is the NOR output.

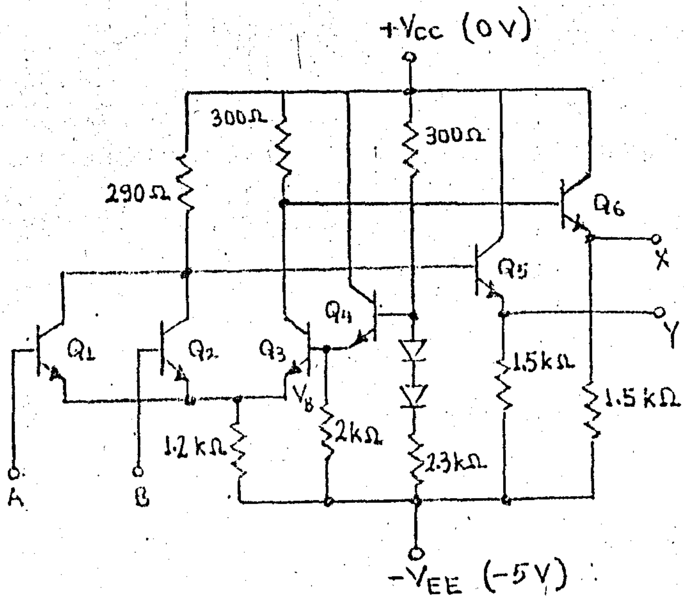


Figure 2.10 Basic ECL circuit.

Often the positive supply voltage is taken as zero volts and V_{EE} as -5 V. The diodes and emitter follower Q_4 establish a base reference voltage for Q_3. When inputs A, and B are less than the voltage V_B, Q_3 conducts while Q_1 and Q_2 are cut off. If any one of the inputs is switched to the 1 level which exceeds V_B, the transistor turns on and pulls the emitter of Q_3 positive enough to cut this transistor off. Under this condition output Y goes negative while X goes positive. The relativly large resistor common to the emitters of Q_1, Q_2, and Q_3 prevents these transistors from saturating. In fact, with nominal logic levels of -1.9 V and -1.1 V, the current through the emitter resistance is approximately equal before and after switching takes place. Thus, only the current path changes as the circuit switches.

The following are the most important characteristics of the ECL family of logic circuits:

1. The transistors never saturate, so switching speed is very high. Typical propagation delay time is 2 ns, which makes ECL a little faster than Schottky TTL (74S00 series). Although the 74S00 series is almost as fast as ECL, it requires a somewhat more complex fabrication process, so it is somewhat higher in cost.

2. The logic level are nominally -1.1 V and -1.9 V for the logic 1 and 0, respectively.

3. Worst-case ECL noise margins are approximately 250 mV. These low noise margins make ECL somewhat unreliable for use in heavy industrial environments.

4. An ECL logic block usually produces an output and its complement. This eliminates the need for inverters.

5. Fan-outs are typically around 25, owing to the low-impedance emitter-follower outputs.

6. Typical power dissipation for a basic ECL gate is 25 mW, just slightly higher than Schottky TTL.

7. The total current flow in an ECL circuit remains relatively constant regardless of its logic state. This helps to maintain an unvarying current drain on the circuit power supply even during switching transitions. Thus, no noise spikes will be internally generated like those produced by TTL totem-pole circuits.

Table 2.2 shows how ECL compares to the TTL logic families.

Table 2.2

Logic Family	t_{pd} (ns)	P_D (mW)	Worst-Case Noise Margin (mV)	Maximum Clock Rate (MHz)
7400	9	10	400	35
74L00	33	1	400	3
74H00	6	23	400	50
74S00	3	23	300	125
74LS00	9.5	2	300	45
ECL	2	25	250	200

2.5 THE RTL LOGIC FAMILY

A three-input RTL gate is shown in Figure 2.11. For positive logic the gate functions as a NOR gate. The RTL family is constructed in relatively simple configurations and is consequently one of the cheapest lines of logic. On the other hand, this family is more inflexible than other popular families. The fan-out specification is usually small with a typical value of four or five. The noise margin for RTL is low, as is the switching speed. Because of the disadvantages of RTL it finds limited application in digital system design.

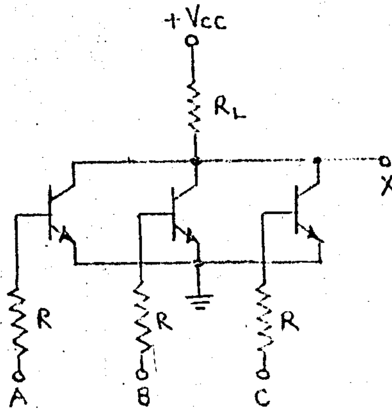


Figure 2.11 A three-input RTL gate.

The circuit operation is simple. If any input is HIGH, the corresponding transistor is driven into saturation and the output is LOW. However, if all inputs are LOW, then all input transistors are cut off and the output is HIGH. The preceding two statements confirm that the gate performs positive NOR logic. Levels for 1 state and 0 state are 1.2 V and 0.2 V, respectively.

2.6 THE DCTL LOGIC FAMILY

This configuration is the same as RTL, except that the base resistors are omitted. A three-input DCTL gate is shown in Figure 2.12. For positive logic the gate functions as a NOR gate. The characteristics of the DCTL family are similar to that of the RTL family. Typical levels for binary 0 and binary 1 are 0.2 V and 0.8 V, respectively.

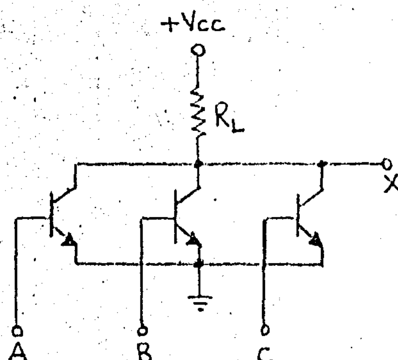


Figure 2.12 A three-input DCTL gate.

2.7 THE I^2L LOGIC FAMILY

This is the newest bipolar family. It has already made inroads in important application in games and watches, in chips for television tuning and control, and in memory and microprocessor chips. I^2L technology allows greater component densities on a chip (much greater than TTL and in some cases greater than MOS) and offers a variety of speed-power trade-offs. When operated at slow speeds (delays of 100 ns), I^2L dissipates less power (5 nW) than any logic family including CMOS. At high speeds (5 ns) it only dissi-

pates 5 mW per gate.

The basic I^2L circuit is shown in Figure 2.13(a). Transistor Q_1 is connected as a constant-current source which produces a current "I" dependent on the value of R_{ext}. This resistor is normally external to the IC chip and is chosen to produce the desired value of "I" typically between 1 nA and 1 mA. Transistor Q_2 acts as a switching transistor and has multiple collectors similar to the multiple emitters of TTL. Figure 2.13(b) shows the equivalent circuit model for this basic I^2L circuit with Q_1 replaced by a constant-current source.

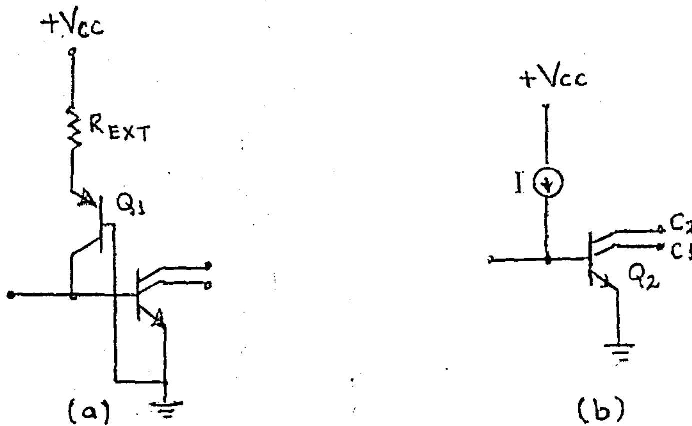


Figure 2.13 (a) Basic I^2L circuit: (b) equivalent circuit

The basic circuit operates as follows. If the input terminal is open-circuited, the current "I" flows into the base of Q_2 and turns it ON so that each collector is a low-resistance path to ground. If the input terminal is shorted to ground, the current "I" will be shunted away from Q_2's base and will flow through the shorted input terminal to ground. This will turn OFF Q_2 so that each of its collectors will be open circuits.

In practice, the input to this circuit is being driven by one or more collector outputs from similar circuits in order to produce the various logic operations. An example is shown in Figure 2.14. This circuit functions as an OR gate if we define our 0 and 1 levels as short circuit and open circuit, respectively. The output will be a 1 (open) when either or both inputs are a 1 (open). When both inputs are 0 (shorted to ground), Q_{2X} and Q_{2Y} will be OFF so that Q_{2Z} will be turned ON by "I", thereby producing an output of 0 (short).

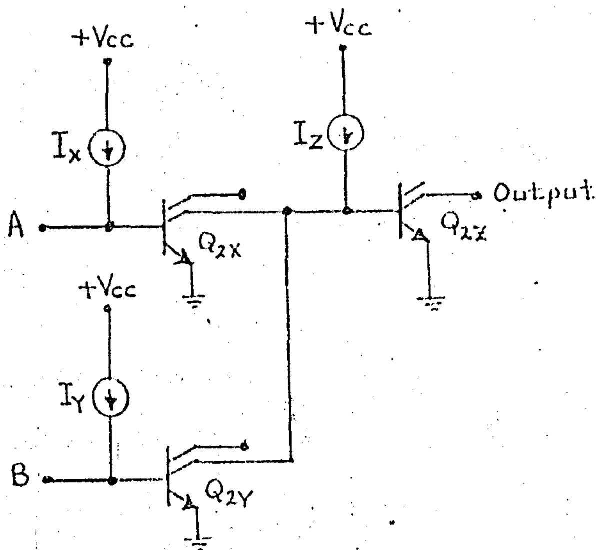


Figure 2.14 I^2L OR gate.

Looking at these I^2L circuits we can see a principal reason why they can achieve high component densities. It is the absence of resistors as part of the IC chip. Resistors represent a significant portion of the chip area, typically requiring ten times more space than a transistor.

In summary, the I^2L family is one of the more promising of the bipolar families. Because it is still in the development stage, the cost is still higher than other logic families, but this is gradually changing. It is reasonable to predict that I^2L will have a significant impact in the LSI field.

2.8 MOS DIGITAL INTEGRATED CIRCUITS

MOS (metal-oxide-semiconductor) technology derives its name from the basic MOS structure of a metal electrode over an oxide insulator over a semiconductor substrate. The transistors of MOS technology are field-effect transistors called MOSFETs. Most of the MOS digital ICs are constructed entirely of MOSFETs and no other components.

The chief advantages of the MOSFET are that it is relatively simple and inexpensive to fabricate, it is small in size, and it consumes very little power. Mos devices occupy much less space on a chip than bipolar transistors; typically, a MOSFET requires 1 square mil of chip area while a bipolar transistor requires about 50 square mils. More importantly, MOS digital ICs normally do not use the IC resistor elements.

The principal disadvantage of MOS ICs is their relatively slow operating speed when compared to the bipolar IC families. In many applications this is not a prime consideration, so MOS logic offers an often superior alternative to bipolar logic.

Digital circuits employing MOSFETs are broken down into three categories: (1) P-MOS, which uses only P-channel enhancement MOSFETs; (2) N-MOS, which uses only N-channel enhancement MOSFETs; and (3) CMOS (complementary MOS), which uses both P- and N-channel devices.

P-MOS and N-MOS digital ICs have a greater packing density than CMOS. N-MOS has about twice the packing density of P-MOS. In addition to its greater packing density, N-MOS is also about twice as fast as P-MOS, owing to the fact that free electrons are the current carrier in N-MOS while holes (slower-moving positive charges) are the current carriers for P-MOS. CMOS has the greatest complexity and lowest packing density of the MOS familes, but it possesses the important advantages of higher speed and much lower power dissipation.

Figure 2.15 shows the basic N-MOS logic circuit. The P-MOS circuits would be the same except for the voltage polarities. A typical N-MOS NAND gate has a propagation delay time of 50 ns. This is due to two factors: the relatively high output resistance in the HIGH state and the capacitive loading presented by the inputs of the logic circuits being driven. MOS logic inputs have very high input resistance ($>10^{12}\Omega$), but they have a high gate capacitance, typically 2-5 picofarads. This combination of large R_{OUT} and large C_{LOAD} serves to increase switching time. N-MOS noise margins are around 1 V, which is higher than TTL or ECL. Because of the extremely high input resistance at each

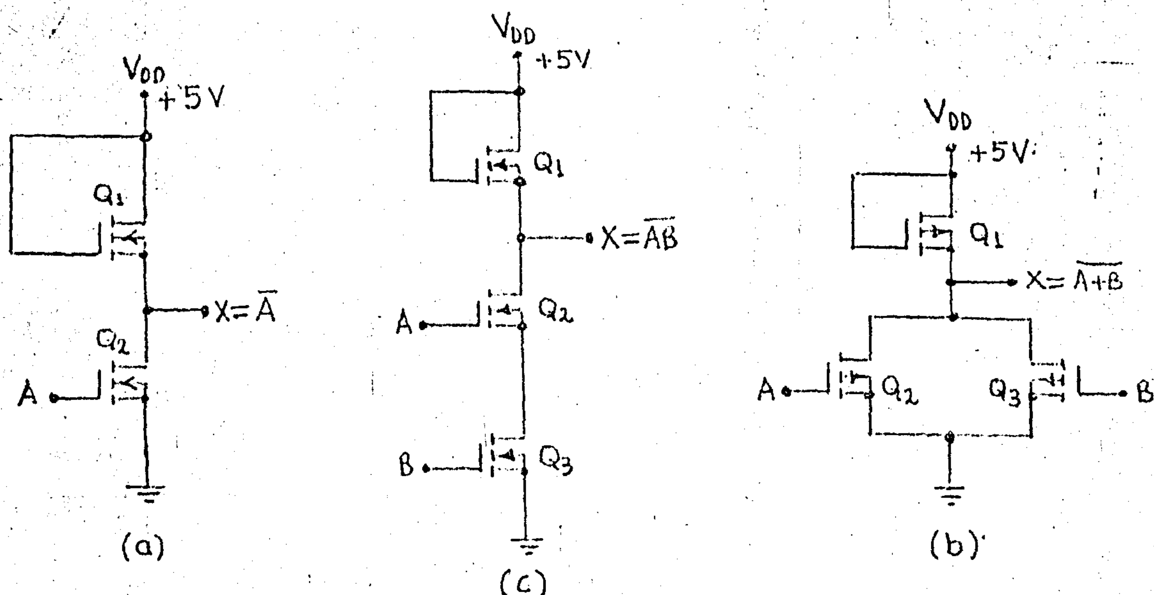


Figure 2.15 (a) N-MOS inverter; (b) NAND gate; (c) NOR gate.

MOSFET input, one would expect that the fan-out capabilities of MOS logic would be virtually unlimited. This is essentially true for dc or low-frequency operation. However, for frequencies greater than 100 kHz, the gate input capacitances cause a deterioratfon in switching time. Even so, MOS logic can easily operate at a fan-out of 50, which is somewhat better than the bipolar families. MOS logic circuits draw small amounts of power because of relatively large resistances being used.

2.9 COMPLEMENTARY MOS LOGIC

The complementary MOS (CMOS) logic family uses both P- and

N-channel MOSFETs in the same circuit to realize several advantages over the P-MOS and N-MOS families. Generally speaking, CMOS is faster and consumes less power than the other MOS families. These advantages are offset somewhat by the increased complexity of the IC fabrication process and a lower packing density.

Figure 2.16 shows the basic CMOS logic circuits.

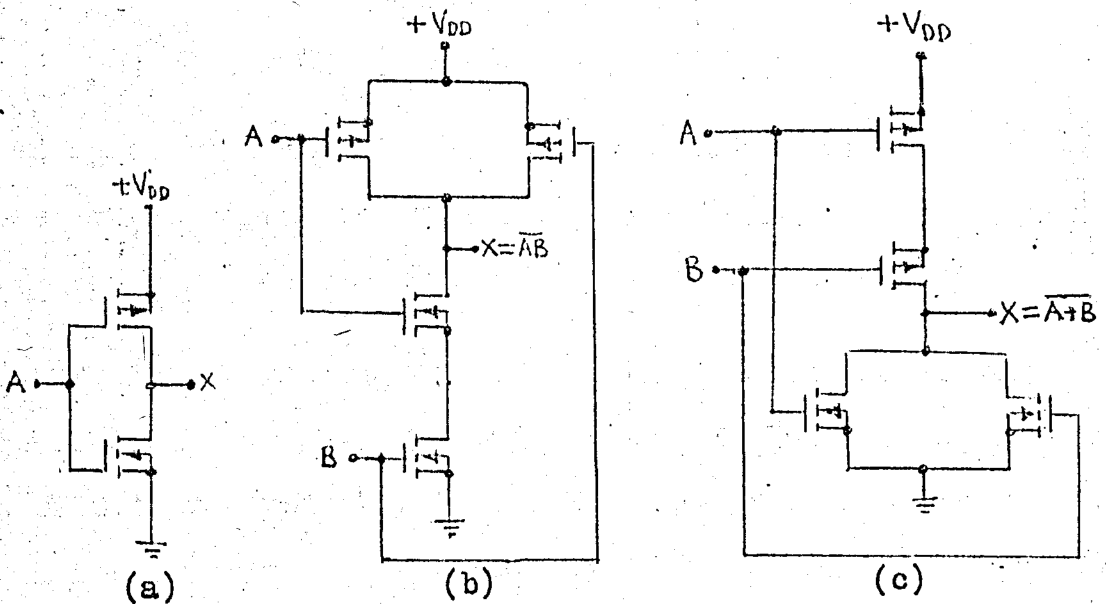


Figure 2.16 (a) CMOS inverter; (b) NAND gate; (c) NOR gate.

The quiescent (dc) power dissipation of CMOS logic circuits is extremely low. The reason for this can be seen by examining the circuits of Figure 2.16. For these circuits in either output state, there is never a low-resistance path from V_{DD} to ground: that is, for any input condition, there is always an OFF MOSFET in the current path. This fact results in typical CMOS dc power

dissipations of 10-20 nW per gate using $V_{DD} = 10$ V.

The CMOS logic levels are 0 V for logical 0 and $+V_{DD}$ for logical 1. The $+V_{DD}$ supply can range from 3 V to 15 V which means that power-supply regulation is not a serious consideration for CMOS.

The required CMOS input levels depend on V_{DD} as follows:

$$V_{IL}\ (max) = 30\% \times V_{DD}$$

$$V_{IH}\ (min) = 70\% \times V_{DD}$$

For example, with $V_{DD} = 5$ V, V_{IL} (max) is 1.5 V, which is the highest input voltage that is accepted as a LOW, and V_{IH} (min) = 3.5 V, which is the smallest voltage accepted as a HIGH input.

CMOS, like P-MOS and N-MOS, suffers from the relatively large load capacitances caused by the CMOS inputs being driven. each CMOS input typically is a 5-pF load. CMOS circuits, however, have a faster switching rate than MOS because of the lower output resistance in the HIGH state. The switching speed of the CMOS circuits will vary with supply voltage. A large V_{DD} produces lower values of R_{ON}, which produces faster switching, owing to faster charging of load capacitances.

When CMOS logic circuits are in a stable state for long periods of time or switching at very low frequencies, then the power dissipation will be extremely low. As the switching frequency of the CMOS circuits increases, however, the average po-

wer dissipation will increase proportionally. This is because each time the CMOS output switches HIGH, a transient charging current must be supplied to any load capacitance. These momentary pulses of current come from the V_{DD} supply. For example, a CMOS inverter gate with a dc dissipation of 10 nW will have an average dissipation of 0.1 mW at a frequency of 100 kHz. This increases to 1 mW at 1 MHz.

Because of the high dc input resistance of CMOS, there seems to be no practical limit on the number of CMOS inputs that can be driven by a CMOS output. However, the input capacitance of CMOS becomes a limiting factor when the total load capacitance becomes high enough to limit the switching speed of the circuit. Thus, the fan-out of CMOS is limited by capacitance of the inputs.

The CMOS series has the same noise margin in both the HIGH and LOW states. The values of V_{NL} and V_{NH} are guaranteed to be 30 per cent of the V_{DD} supply voltage. Thus, for $V_{DD} = 10$ V, the guaranteed noise margin is 3 V for either state.

All CMOS inputs must be tied to some voltage level, preferably ground or V_{DD}. Unused inputs cannot be left floating, because these inputs would be susceptible to noise which could bias both the P- and N-channel MOSFETs in the conducting state, resulting in excessive power dissipation.

The high input resistance of CMOS inputs makes them susceptible to static charge buildup, and voltages sufficient to cause electrical breakdown can result from simply handling the devices.

Some of the newer CMOS devices have protective diodes on each input to guard against breakdown due to static charges.

2.10 SILICON-ON-SAPPHIRE (SOS)

The SOS family is a modification of the CMOS family. It uses sapphire as an insulating material to reduce the capacitances associated with each MOSFET. SOS works just like CMOS except that it operates at a faster speed due to the reduction of these capacitances. However, it has a more complex fabrication process than the other MOS families and is therefore more expensive.

CHAPTER 3

SOME ECONOMIC CONSIDERATIONS OF IC TESTING[11]

Although integrated circuits are tested at several points in their manufacturing cycle, a certain percentage of the devices delivered to users are faulty. To eliminate all defective ICs, the manufacturer must test 100% of his devices before they are shipped. This is seldom true of any other manufactured product and is not true of integrated circuits. There seems to be a small percentage of defective devices that evade all controls. Unfortunately, this small percentage can cause serious trouble in systems where many ICs are used.

To see the effect of these defective devices, we can calculate the percentage of newly loaded printed circuit boards that will not function because they contain faulty devices. The probability of the total board working is the probability of all of its individual components working at the same time. This is derived by multiplying all the individual probabilities together. For example, a board containing 100 ICs, each with 99% probability of functioning correctly, would have a probability of functioning correctly of $(99\%)^{100}$, or 37%. This means that if only 1% of the ICs used are defective, only one out of three boards will work. Hence the rework costs, which is directly attributable to faulty ICs, can be quite sizable.

3.1 EQUIPMENT COSTS

Several types of test equipment are available to detect faulty digital integrated circuits. As one might expect, inexpensive testers may be used to catch some of the failures, whereas equipment designed to eliminate virtually all failures may be prohibitively expensive to all but extremely-high-volume users. Functional testing, or testing to see whether a device performs according to its truth table, can be done with equipment in the $ 1,000 price range. This type of testing catches an estimated 70% of all failures. The addition of dc parametric testing, or testing to see whether all input/output voltages and currents are correct and ascertaining that the device will operate under worst-case voltage and current conditions, catches greater than 95% of all faulty devices. A tester that performs both parametric and functional tests costs about $ 10,000.

To catch the last few faulty devices it is necessary to add pulse parametric or dynamic testing to the test repertoire. Addition of this test segregates those devices whose defects are slow rise times, long propagation delays, insensitivity to narrow clock pulses, or other timing-related phenomena. This type of tester costs typically over $ 100,000. For most IC users, the most cost-effective solution is a compromise between the two extremes: a bench-top digital IC tester capable of performing dc parametric and functional testing, thereby catching greater than 95% of all faulty devices.

3.2 SAMPLE TESTING OR 100% TESTING

Sample testing is designed to catch gross defects sush as high percentages of devices that do not meet specifications or devices that are mismarked. Small percentages of defective devices may not be detected. This type of testing is usually done when the lot of ICs is purchased as having an acceptable quality level. If a lot is rejected by the user because his sample testing reveal's excessive failures, the whole lot is returned to the vendor. This lot is then replaced by another lot that may pass the same sample test even though it contains a quite significant percentage of faulty devices.

100% testing is more expensive, since it typically involves automatic handling equipment and requires more of a labor investment. But it does have the advantage of catching not only the gross problems but also the small percentage of defects that are continuously present. Although the trend seems to be towards 100% incoming inspection of digital ICs, the user's decision must be based on a careful analysis of his individual situation.

3.3 THE COST OF 100% TESTING USING DC PARAMETRIC AND FUNCTIONAL TESTS

The cost of testing a digital IC depends primarily on two things: the cost of the test equipment involved and the cost of

the manpower required to operate the equipment. The cost of tes ting a single IC can then be determined according to the volume of ICs tested and the speed at which they are tested. For equip ment costs, let us assume that the IC tester costs $ 10,000 and the addition of automatic handling equipment to the tester cost $ 8,000. For labor costs, assume a $ 4/hour rate with 50% over- head for a total of $ 6/hour. The low-volume user of ICs, test- ing 50,000 ICs per year, would probably choose to insert the ICs into the tester manually. Using five-year straight-line dep- reciation, the annual equipment costs would be $ 2,000, or 0.04/IC. About 300 ICs can be tested per hour for $ 6 or 0.02/I The total testing cost is 0.06/IC. The high-volume user of ICs, testing 1,000,000 ICs per year, would require automatic handlin equipment in addition to the tester for a total of $ 18,000. Th annual equipment depreciation would be $ 3,600 or 0.0036/IC. About 4,000 ICs could be tested per hour for $ 6 or 0.0015/IC. The total testing cost is 0.0051/IC. For the assumptions stated the high-volume user could buy testing for each of his ICs at one-tenth the cost of the low-volume user. Even so, the cost to the low-volume user may prove to be a good investment.

3.4 THE COST OF FINDING A BAD IC

The cost to find a bad IC at incoming inspection depends on the cost of testing a single IC and the failure rate of the IC type. For a typical failure rate of 1% for room-temperature dc

parametric and functional testing (high-temperature testing usually produces more failures), 100 ICs must be tested to find a bad one. For the user of 50,000 ICs per year, the cost to find that bad IC is $ 6 (100×0.06). For the user of 1,000,000 ICs per year, the cost to find a bad IC is $ 0.51 (100×0.0051). These testing costs may now be compared to costs of finding and replacing a faulty IC once it is soldered into a circuit board. An estimate of $ 10 per board repair is representative of a typical cost.

For a company using 50,000 ICs per year the cost to find each bad IC is $ 6 for a 1% failure rate. With this failure rate, 500 faulty devices would be found per year, saving an estimated $ 5,000 in board repair costs. The cost to find these 500 bad ICs is $ 3,000 for a net savings of $ 2,000. Since the costs are fixed, higher failure rates than 1% mean more savings. For a company using 1,000,000 ICs per year, the cost to find each bad IC is $ 0.51 for a 1% failure rate. Testing the one million circuits yields 10,000 bad ICs for a savings of $ 100,000 in board repair costs. The cost to find these 10,000 bad ICs is $ 5,100 for a net savings of $ 94,900. For the two situations analyzed, the savings are then $ 2,000 and $ 94,900. Thus, the potential for cost savings is very great.

CHAPTER 4

IMPLEMENTATION OF CIRCUITRY[6,7]

4.1 GENERAL DESCRIPTION

The tester is a compact automatic test instrument that interrogates the parametric and functional performance of a wide variety of digital ICs, including DTL, TTL, ECL, RTL, DCTL, I^2L, CMOS and MOS. A microcomputer, which is part of the test system, directs and controls the testing process according to the test program. The microprocessor used is the M6800 which has an 8-bit data bus and a 16-bit address bus.

The tester has been specifically designed for testing digital ICs. Hence, it is a dedicated type test system. Advantages and disadvantages of this type of test system were given in Chapter 1.

During testing, a reference voltage is applied to each pin of the UUT, then the current flowing through each pin is measured and compared against predetermined limits. If the measurement taken from each pin is within the limits specified for that pin, the microcomputer will instruct the system to seek for the next test. If the measured current value at any pin is beyond the specified limits, the microcomputer will direct the

system to branch to a specific subroutine, and the LED corresponding to the failed pin is lit. At this time the current value at that particular pin can be read from the panel by pushing the proper switch. This procedure continues until the operator sends an END signal to the microcomputer.

Hence, the principle of the testing is to apply a reference voltage to each pin of the UUT and to measure the current for each pin, and then to compare it against predetermined current limits. The reference voltages and the current limits are held in the sample-and-hold circuits as voltage levels. For this reason, the value of the current flowing through each pin is converted to a voltage level. To compare the measured current against the current limits, only one voltage comparator for each pin is used.

4.2 BLOCK DIAGRAM OF THE TESTER

The complete block diagram of the tester is shown in Figure 4.1.

The pin driver circuit is the same for each pin of the UUT. Therefore, there are 16 pin driver circuits in the tester. Any pin can be an input, output, clock, ground, or power supply pin.

The reference voltage generator generates necessary voltage levels for pin driver circuits.

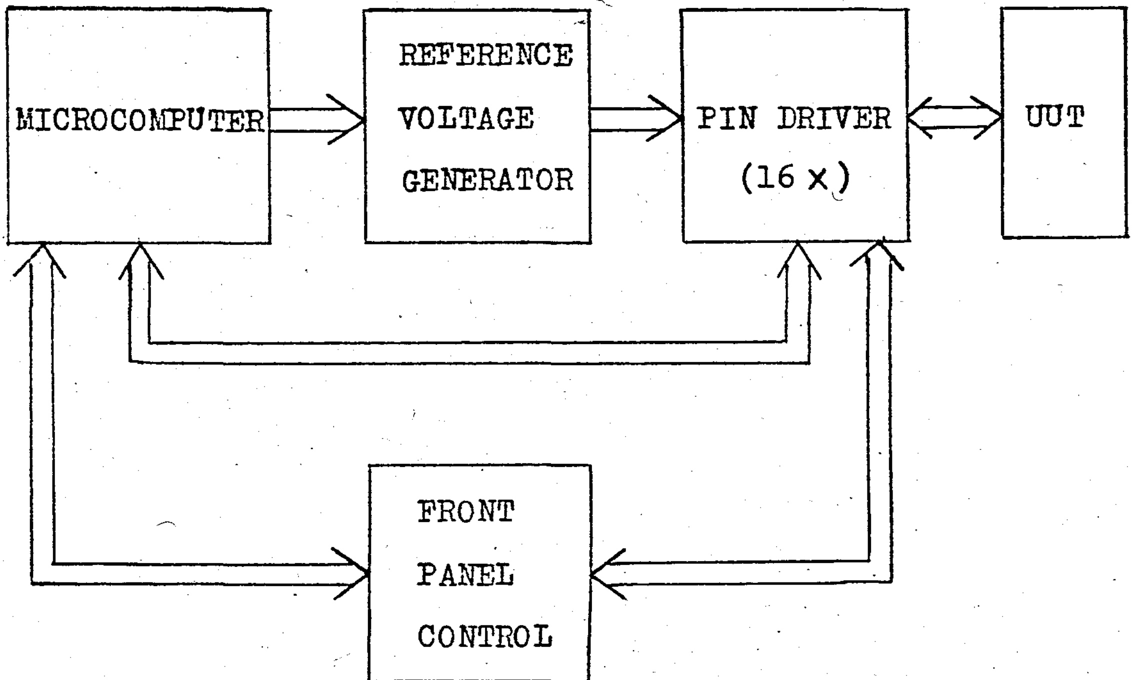


Figure 4.1 The block diagram of the tester.

The microcomputer directs and controls the testing process.

The front panel includes control switches, leds, and a current indicator.

4.3 PIN DRIVER

The pin driver circuit is the same for each pin of the UUT. A simplified circuit diagram for the pin driver is shown in Figure 4.2. Each pin driver has four reference voltages; V_1 ,

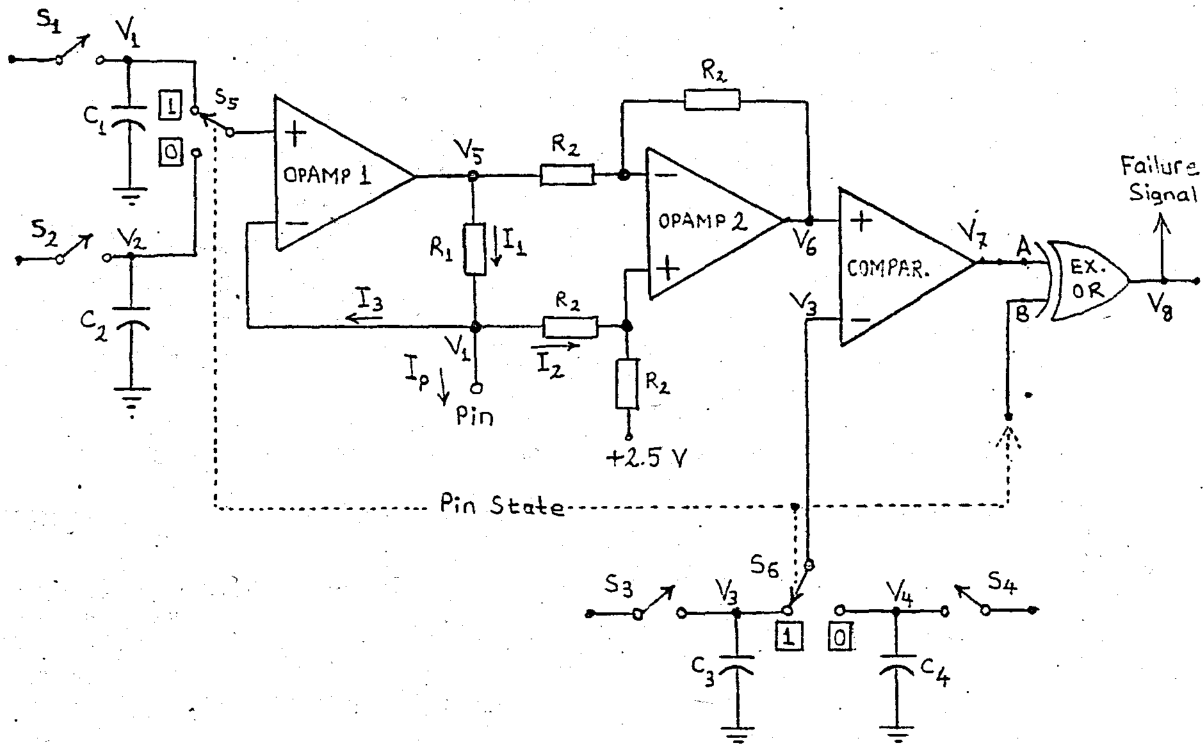


Figure 4.2 A simplified circuit diagram for the pin driver.

V_2, V_3, and V_4. These voltages are generated and applied to the corresponding capacitors by the reference voltage generator. To prevent the capacitors from discharging, they are refreshed periodically. Hence, V_1, V_2, V_3, and V_4 are held at their original values during testing.

V_1 is the "1" state voltage and V_2 is the "0" state voltage V_3 is the "1" state current limit and V_4 is the "0" state current limit.

S_1, S_2, S_3, and S_4 are CMOS analog bilateral switches. S_5 and S_6 are CMOS analog multiplexers/demultiplexers.

The pin driver can be either in the "1" state or in the "0" state. If it is in the "1" state, the noninverting terminal of the OPAMP-1 is connected to the capacitor C_1 via S_5 and the inverting terminal of the COMPARATOR is connected to the capacitor C_3 via S_6, and one of the inputs of the EXCLUSIVE OR gate, B, is put in the "1" logic level.

If the pin driver is in the "0" state, the noninverting terminal of the OPAMP-1 is connected to the capacitor C_2 via S_5, the inverting terminal of the COMPARATOR is connected to the capacitor C_4 via S_6, and the input B of the EXCLUSIVE OR gate is put in the "0" logic level.

As an example of "pin driver" operation, let us assume that the pin driver is in the "1" state. Then, the voltage of the noninverting terminal of the OPAMP-1 is V_1, the voltage of the inverting terminal of the COMPARATOR is V_3, and the input B of the EXCLUSIVE OR gate is in the "1" logic level. The OPAMP-1 makes the pin voltage equal to V_1. The OPAMP-2 and four R_2 resistors constitute a differential amplifier with unity gain. The output voltage of the OPAMP-2, V_6, can be calculated as

$$V_1 - V_5 = V_6 - 2.5\ \mathrm{V}$$

$$V_6 = 2.5\ \mathrm{V} - (V_5 - V_1) \qquad (4.1)$$

If we neglect the currents I_2 and I_3, then

$$I_1 = I_p \tag{4.2}$$

and

$$V_5 - V_1 = I_1 \times R_1 = I_p \times R_1 \tag{4.3}$$

and from Equation (4.1)

$$V_6 = 2.5\ V - I_p \times R_1 \tag{4.4}$$

If $V_6 > V_3$, then the output voltage of the COMPARATOR, V_7, will be in the "1" logic level. Since the output of the COMPARATOR is connected to the input A of the EXCLUSIVE OR gate, the output voltage, V_8, will be in the "0" logic level. This means that there is no failure.

However, if $V_6 < V_3$, then the output voltage of the COMPARATOR, V_7, will be in the "0" logic level, and the output voltage of the EXCLUSIVE OR gate, V_8, will be in the "1" logic level. "1" logic level for V_8 means that there is a failure.

The failure signal is not produced when $V_6 > V_3$. For this condition, we can calculate the limit value for the pin current I_p as

$$V_6 = 2.5\ V - I_p \times R_1 > V_3$$

$$I_p < \frac{2.5\ V - V_3}{R_1} \tag{4.5}$$

If the actual direction of the current I_p is in the same direction as that shown in Figure 4.2, then there is an upper limit for the current I_p, that is

$$I_{p_{max}} = \frac{2.5\ V - V_3}{R_1} \tag{4.6}$$

so that

$$I_p < I_{p_{max}} \tag{4.7}$$

On the other hand, if the actual direction of the current I_p is in the opposite direction of that shown in Figure 4.2, then there is a lower limit for the current I_p, that is

$$I_{p_{min}} = \frac{V_3 - 2.5\ V}{R_1} \tag{4.8}$$

so that

$$-I_p > I_{p_{min}} \tag{4.9}$$

When the pin driver (in the "1" state) is to drive an input pin or power supply pin of the UUT, it acts as a source. That is, the direction of the current I_p is in the same direction as that shown in Figure 4.2. When the pin driver is to drive an output pin of the UUT, it acts as a sink. That is, the direction of the current I_p is in the opposite direction of that shown in Figure 4.2. Hence, for an input pin or a power supply pin of the UUT, there is a current limit value of $I_{p_{max}}$, and for an output pin of the UUT, there is a current limit value of $I_{p_{min}}$.

Until now, we have assumed that the pin driver is in the "1" state. Now, let us assume that it is in the "0" state. When the pin driver is to drive an input pin or ground pin of the UUT, it acts as a sink, and there is a current limit value of $I_{P_{max}}$. When the pin driver is to drive an output pin of the UUT, it acts as a source. and there is a current limit value of $I_{P_{min}}$. These results come from the operation characteristics of the EXCLUSIVE OR gate.

The complete circuit diagram for the pin driver is shown in Figure 4.3. The transistors Q_2 and Q_4 are used to increase the output current of the OPAMP-1. The resistors r_5 and r_6, the diodes D_1 and D_2 constitute bias circuits for the transistors Q_2 and Q_4. The transistors Q_1 and the resistors r_1 and r_3 are used to limit the source current at 120 mA, while the transistor Q_3 and the resistors r_2 and r_4 limit the sink current at 120 mA. If a MOS or A CMOS device is to be tested, then the resistor r_7 is selected via the RELAY. If the UUT is not a MOS or a CMOS device, then the resistor r_8 is selected. The BUFFER-2 ~~is~~ is used to avoid discharging of the capacitors C_3 and C_4. The BUFFER-1 is used to decrease the current I_2. In the sample-and-hold circuits, the LF 13741 operational amplifiers are used Since the maximum input bias current for a LF 13741 operational amplifier is 50 pA, it follows that with a 1-nF capacitance the drift rate during the HOLD period would be less than 50 mV/s, if there were no other leakage current. But this is not true, because there are some leakage currents due to the CMOS switche

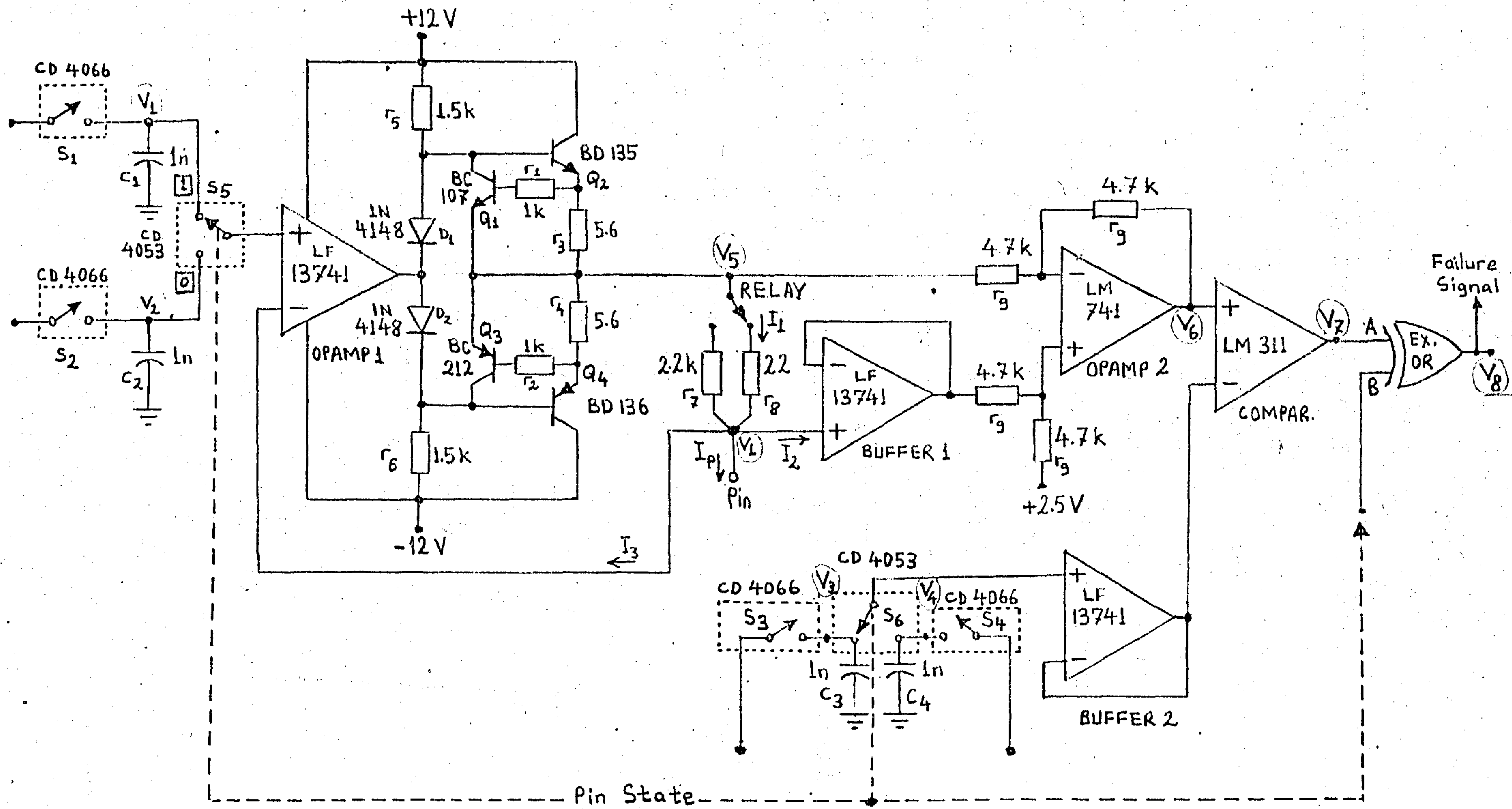


Figure 4.3 The complete circuit diagram for the pin driver.

4.4 REFERENCE VOLTAGE GENERATOR

Each pin driver requires four reference voltages. Each reference voltage can be set to different levels on all pins, therefore as many as $4 \times 16 = 64$ different voltages may be required. Figure 4.4 shows how these voltages are generated. The DAC 0808 is a current mode D/A converter. It has 8 bits for digital data. The OP-5 and the resistor R_5 constitute a current-to-voltage converter, so that the output current I_0 of the DAC 0808 is converted to a voltage which its proportional to the output current I_0. For a digital input of "11111111", the output voltage, V_{11}, becomes 5 V, while for a digital input of "00000001", it becomes 19 mV. The CD 4052 is a CMOS four-channel multiplexer/demultiplexer. The CD 4052 distributes the output line of the OP-5 to four sample-and-hold circuits. The control inputs,"a" and "b", determines to which sample-and-hold circuit the voltage V_{11} will be transmitted. The outputs of the sample-and-hold circuits are bussed to the pin drivers so that the reference voltages for each pin driver appear in sequence. At the appropriate time, each pin driver picks off its reference voltages by means of its sample-and-hold circuits. The CD 4514 is a CMOS line decoder. It has five control inputs: D, C, B, A, and "Inhibit". When the inhibit input is in the "1" logic level, all 16 pin selection lines become LOW. If the inhibit input is LOW, then one of the 16 lines becomes HIGH.

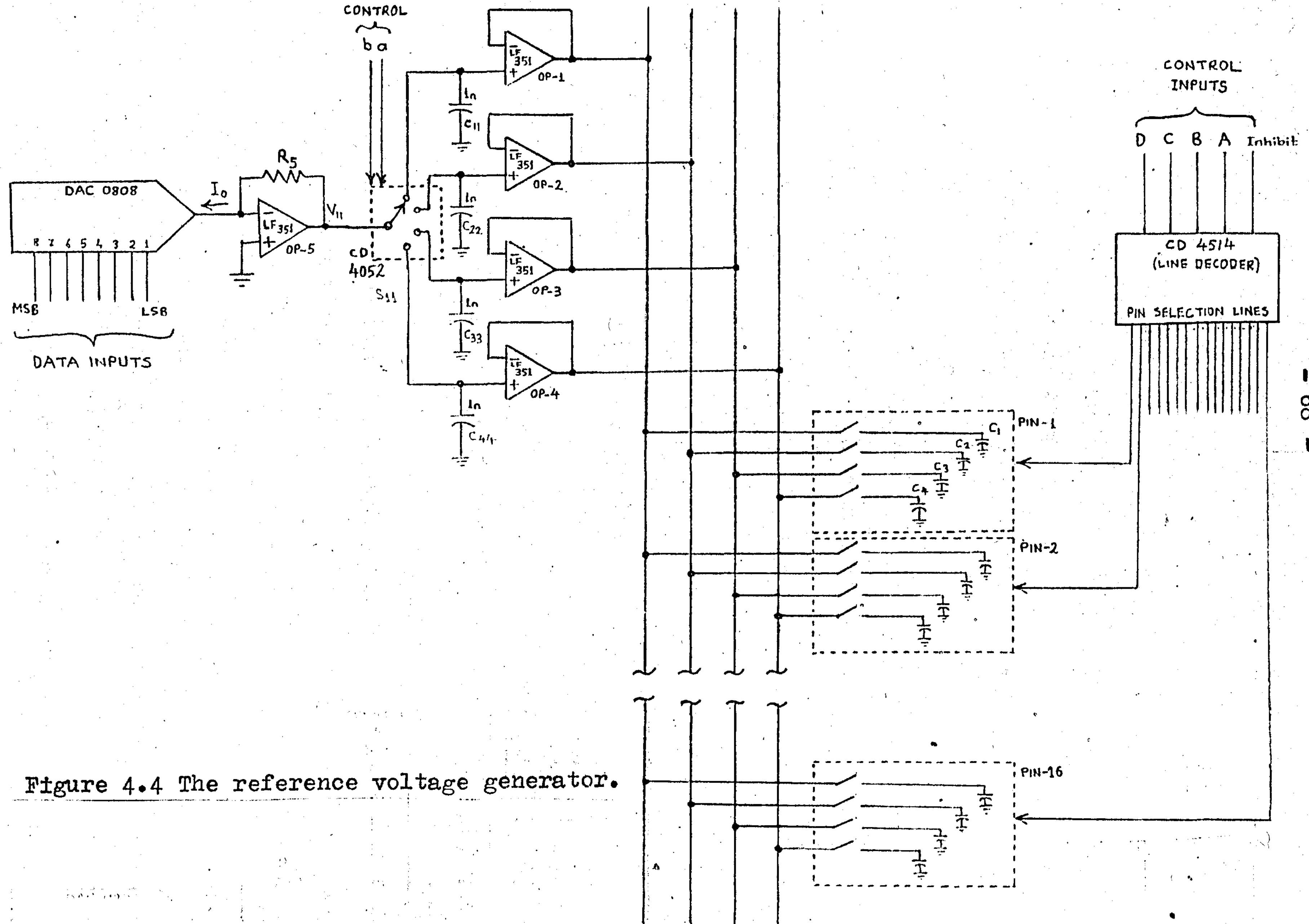


Figure 4.4 The reference voltage generator.

4.5 MICROCOMPUTER

The hardware design of the microcomputer has been excluded from the study, because of economical considerations. A microcomputer system, which was constructed beforehand, has been employed.

The microprocessor used is the M6800 which has an 8-bit data bus and a 16-bit address bus.

The microcomputer directs and controls the testing process.

4.6 FRONT PANEL CONTROL

The picture of the front panel is shown in Figure 4.5. It includes switches, LEDs, and a current indicator.

The LEDs L_1 through L_{16} are used to show failure at the corresponding pin. For example, if there is a failure in Pin 3 of the UUT, then the LED L_3 is lit. At this time the current value at that pin can be read from the current indicator by pushing the switch S^3. The LED L_F is used to show that the UUT is defective. Hence, if any of the LEDs L_1 through L_{16} is lit, the LED L_F is also lit. If the testing is completed without any failure, then the LED L_P is lit. S^{17} , S^{18} , and L_{17} are used to start and to end the testing process.

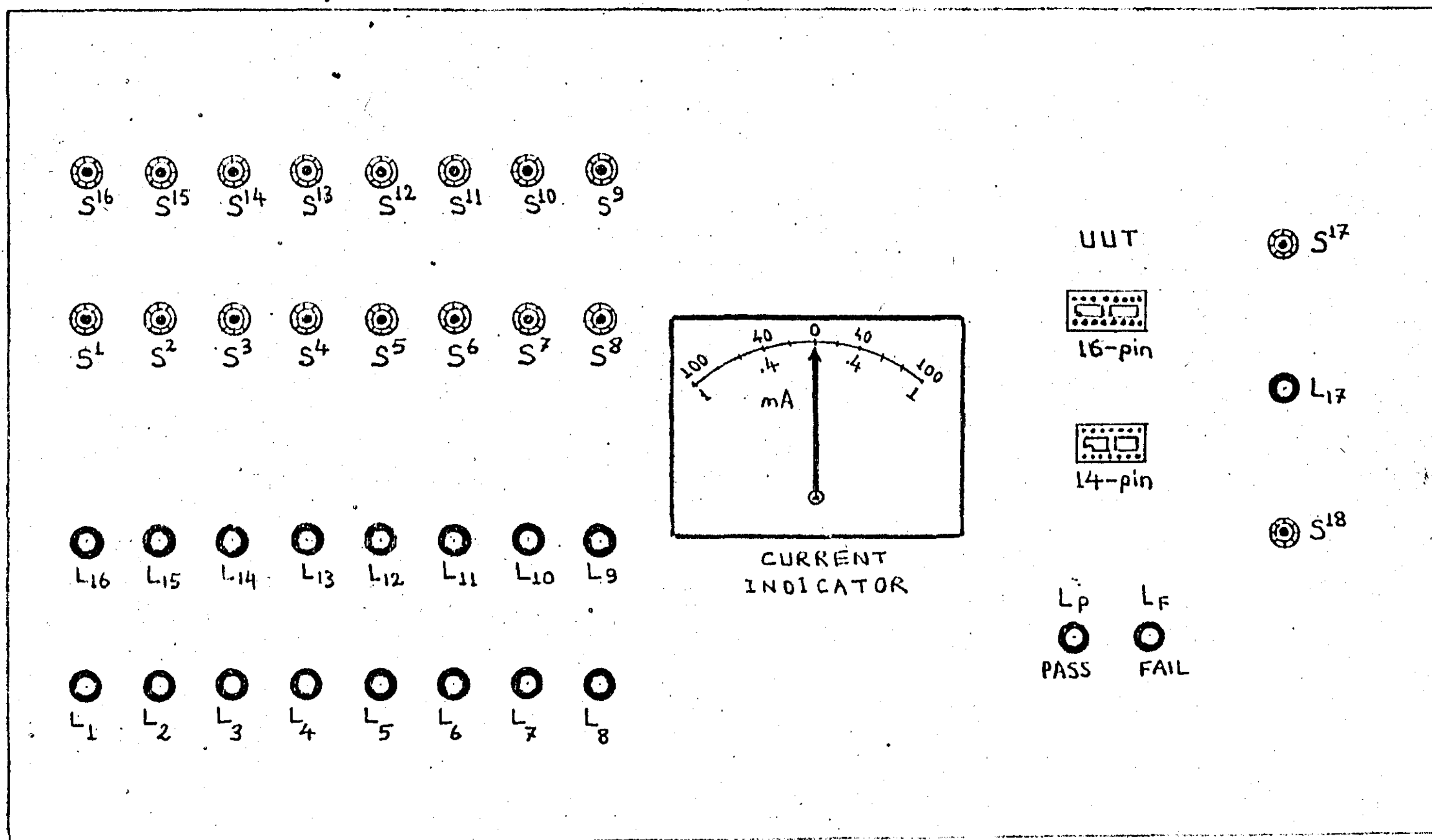


Figure 4.5 The picture of the front panel.

CHAPTER 5

PROGRAMMING AND TESTING PROCESS

The principle of testing is to apply a reference voltage to each pin of the UUT and to measure the current at each pin, and then to compare it against predetermined current limits. Any pin can be an input, output, ground, or power supply pin. If a pin is an input or an output, then two reference voltages are necessary: one for "1" state voltage, the other for "0" state voltage. Since however, the current limits in the circuit are controlled through comparison against reference voltages, we need two more additional reference voltages at the input and output pins. We therefore have to apply 4 reference voltages at each input and output pin. But since we cannot be sure which pins will be the input and output pins, we have to apply the four reference voltages to all the pins in the circuit.

The testing procedure is simple. The first thing is to set the reference voltages to the required levels. Then the truth table of the UUT is followed in steps.

5.1 FLOWCHART OF PROGRAM

The flowchart of the test program is shown in Figure 5.1. There are two subroutines in the program. The subroutines are

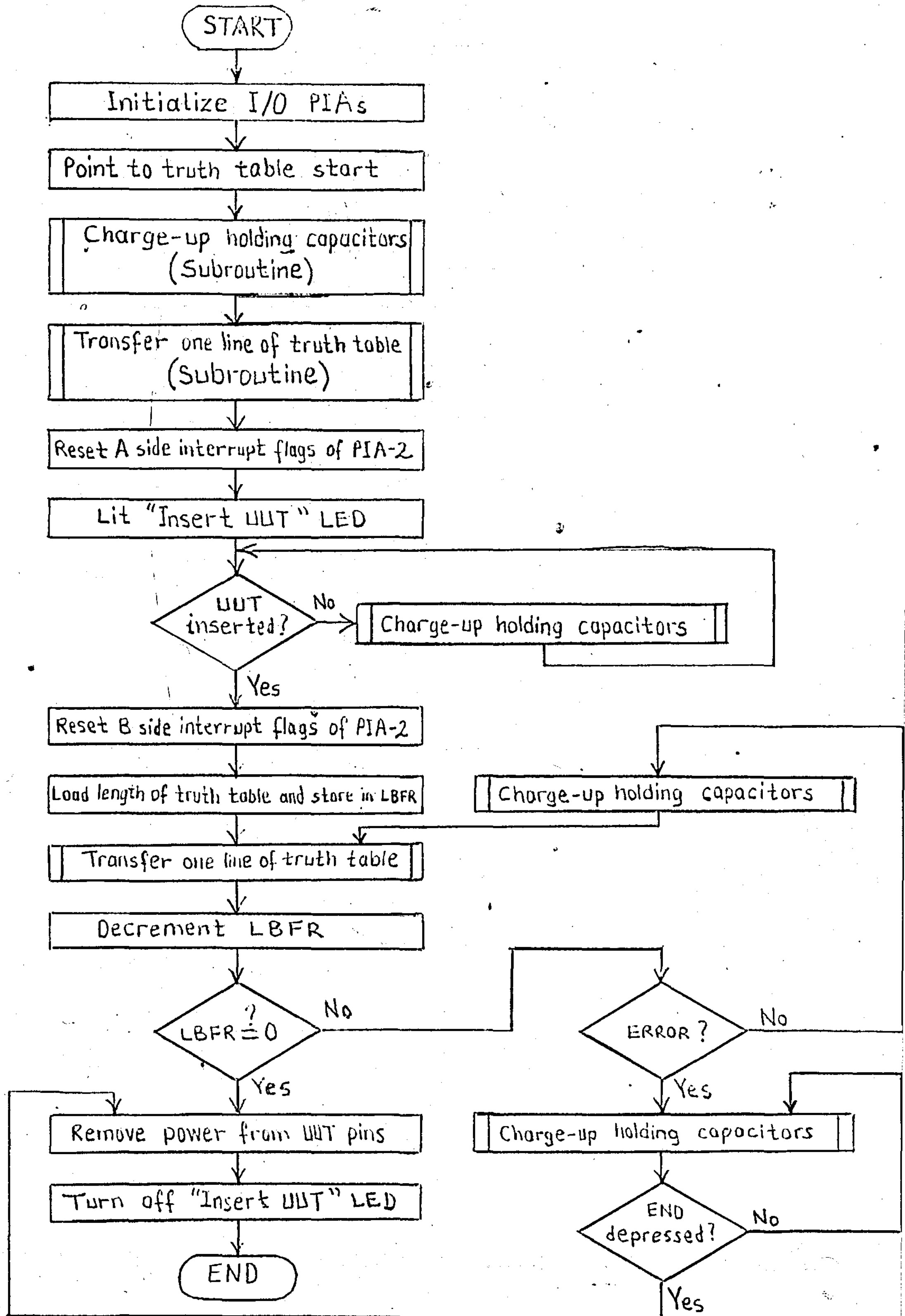


Figure 5.1 The flowchart of the test program.

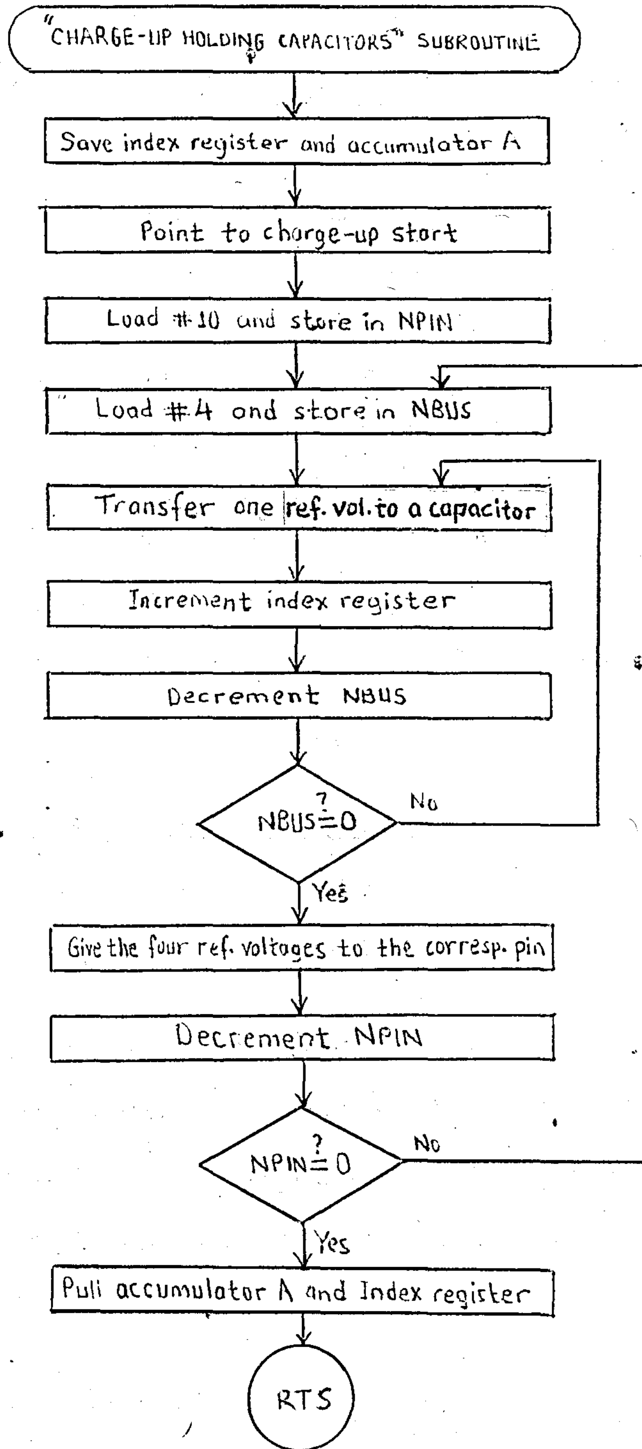


Figure 5.2 "Charge-up holding capacitors" subroutine.

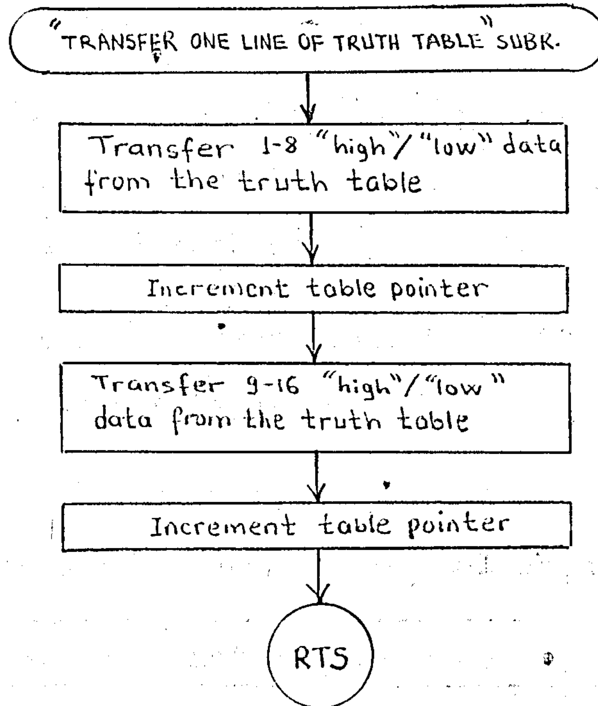


Figure 5.3 "Transfer one line of truth table" subroutine.

shown in Figures 5.2 and 5.3.

The program given in Figure 5.1 is applicable to all digital ICs. Of course each type of digital ICs require a differen set of reference voltages and "high"/"low" data. The "high"/ "low" data represents the "1s" and "0s" in a truth table.

5.2 PROGRAMMING

The reference voltage levels and "high"/"low" data for any

type of digital ICs are obtained from the data sheet for that particular digital IC.

In this thesis, the test program has been prepared for only the 7400, the quad 2-input NAND gate. The other digital ICs can be tested in the same fashion.

The required information about the 7400 for programming is given in Table 5.1 and Figure 5.4.

Table 5.1 The 7400 electrical characteristics.

Characteristic	Rating	Value	Condition
Input and output logic levels	V_{OH}	2.4 V	Minimum
	V_{OL}	0.4 V	Maximum
	V_{IH}	2.0 V	Minimum
	V_{IL}	0.8 V	Maximum
Input and output current levels	I_{OH}	-0.4 mA	Minimum
	I_{OL}	16 mA	Minimum
	I_{IH}	0.04 mA	Maximum
	I_{IL}	-1.6 mA	Maximum
Supply voltage	V_{CC}	4.75 V	Minimum
Supply current	I_{CC}	22 mA	Maximum

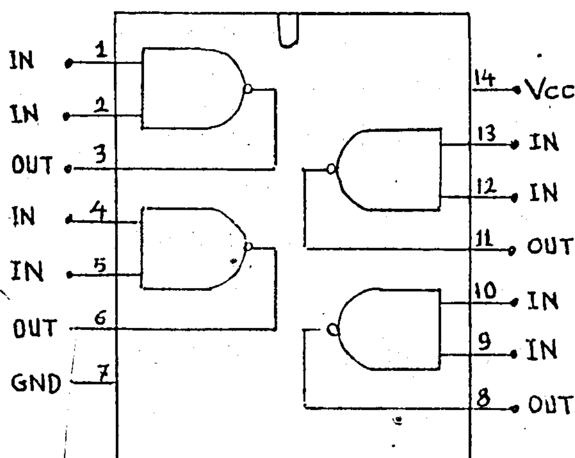


Figure 5.4 The 7400 pin layout.

At input pins, the reference voltage V_1 will be 2.0 V (V_{IH}) and the reference voltage V_2 will be 0.8 V (V_{IL}). At output pins, the reference voltage V_1 will be 2.4 V (V_{OH}) and the reference voltage V_2 will be 0.4 V (V_{OL}). At the supply pin, the reference voltage V_1 will be 4.75 V and the reference voltage V_2 will be 0 V. At the ground pin, the reference voltages V_1 and V_2 will be 0 V.

At input pins, the "1" state current limit, V_3, can be calculated as

$$V_3 = 2.5\ V - I_{IH} \times r_8$$

$$V_3 = 2.5\ V - (4 \times 10^{-5}) \times 22$$

$$V_3 = 2.49912\ V \qquad (5.1)$$

and the "0" state current limit, V_4, can be calculated as

$$V_4 = 2.5\ V + I_{IL} \times r_8$$

$$V_4 = 2.5\ V + (1.6 \times 10^{-3}) \times 22$$

$$V_4 = 2.5352\ V \tag{5.2}$$

At output pins, the "1" state current limit, V_3, can be calculated as

$$V_3 = 2.5\ V + I_{OH} \times r_8$$

$$V_3 = 2.5\ V + (0.4 \times 10^{-3}) \times 22$$

$$V_3 = 2.5088\ V \tag{5.3}$$

and the "0" state current limit, V_4, can be calculated as

$$V_4 = 2.5\ V - I_{OL} \times r_8$$

$$V_4 = 2.5\ V - (16 \times 10^{-3}) \times 22$$

$$V_4 = 2.148\ V \tag{5.4}$$

The supply current given in the data sheet is the no load current value. However, during the testing, the outputs of the UUT is always loaded. Therefore, the maximum value of the supply current is obtained by adding the I_{cc} given in the data sheet and the "1" state output currents. The maximum value of a "1" state output current is not given in the data sheet.

For that reason, we have to estimate the maximum value of a "1" state output current at 2.4 V. The experiments have shown that the maximum value of a "1" state output current is about 15 mA. Since there are four outputs in the 7400, the maximum value of the supply current can be calculated as

$$I_{CC_{max}} = I_{CC} + 4 \times I_{OH_{max}}$$

$$I_{CC_{max}} = 22 \text{ mA} + 4 \times 15 \text{ mA}$$

$$I_{CC_{max}} = 82 \text{ mA} . \qquad (5.5)$$

At the supply pin, the "1" state current limit, V_3, can be calculated as

$$V_3 = 2.5 \text{ V} - I_{CC_{max}} \times r_g$$

$$V_3 = 2.5 \text{ V} - (82 \times 10^{-3}) \times 22$$

$$V_3 = 0.696 \text{ V} \qquad (5.6)$$

When the supply pin is in the "0" state, there will be no current. To be on the safe side, we must set the "0" state current limit equal to 5 V.

The maximum value of the ground current is obtained by adding the supply current given in the data sheet and the "0" state output currents. Since the maximum value of a "0" state output current at 0.4 V is not given in the data sheet, we have estimated that it is about 40 mA. To avoid increasing the ground current, we have intentionally devised a truth table for the 7400, such that, at each line of the truth table, only one

output pin is in the "0" state. Therefore, the maximum value o the ground current will be

$$I_{G_{max}} = I_{CC} + I_{OL_{max}}$$

$$I_{G_{max}} = 22 \text{ mA} + 40 \text{ mA}$$

$$I_{G_{max}} = 62 \text{ mA} \qquad (5.7)$$

At the ground pin, the "0" state current limit, V_4, can be cal culated as

$$V_4 = 2.5 \text{ V} + I_{G_{max}} \times r_8$$

$$V_4 = 2.5 \text{ V} + (62 \times 10^{-3}) \times 22$$

$$V_4 = 3.864 \text{ V}$$

The ground pin is always in the "0" state. Therefore, the "1" state current limit, V_3, is never used during the testing.

The truth table for the 7400 is shown in Table 5.2. At the first line of the truth table, the supply pin is in the "0" state, that is, the voltage of the supply pin is 0 V. When the testing begins, the first line of the truth table is applied to the circuitry until the UUT is inserted in the place. This prevent the UUT from getting destroyed.

During the testing, the lines of the truth table is follow ed in sequence. To avoid making more than one output short cir cuit, only one output is changed from one state to the other,

Table 5.2 The truth table for the 7400.

Vcc 16	IN 15	IN 14	OUT 13	IN 12	IN 11	OUT 10	NC 9	NC 8	GRD 7	OUT 6	IN 5	IN 4	OUT 3	IN 2	IN 1
0	0	0	1	0	0	1	0	0	0	1	0	0	1	0	0
1	0	0	1	0	0	1	0	0	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0	0	0	1	0	1	1	0	1
1	1	0	1	1	0	1	0	0	0	1	1	0	1	1	0
1	1	0	1	1	0	1	0	0	0	1	1	0	0	1	1
1	1	0	1	1	0	1	0	0	0	1	1	0	1	1	0
1	1	0	1	1	0	1	0	0	0	0	1	1	1	1	0
1	1	0	1	1	0	1	0	0	0	1	1	0	1	1	0
1	1	0	1	1	1	0	0	0	0	1	1	0	1	1	0
1	1	0	1	1	0	1	0	0	0	1	1	0	1	1	0
1	1	1	0	1	0	1	0	0	0	1	1	0	1	1	0

when the tester goes from one line to the next line.

After calculating the reference voltages and preparing the truth table, we must convert each number to hexadecimal form, to write this data into the RAMs with the teletypewriter.

The complete test program and required tables in hexadecimal form are given in the appendix.

5.3 TESTING PROCESS

Testing starts with the user informing the identity of the UUT to the tester. The tester will then find the proper test program from the ROM memories for that UUT. If the proper test program is not available in the ROM memories, the program must be written into the RAM memories with the teletypewriter. Once the proper test program is ready, the reference voltage generator begins to apply the reference voltages to the corresponding capacitors. Charging the 64 capacitors takes 2,814 µs. Then, the first line of the truth table is applied to the circuitry until the UUT is inserted in the place. To avoid destroying the UUT, the voltage of the supply pin is set to 0 V before the UUT is inserted in the place. The user sends a signal by pushing the switch S^{17}, in order to inform the microcomputer that the UUT is inserted in the place. Then, the voltage of the supply pin is set to 4.75 V by applying the second line of the truth table. At this time the first test is performed. If there is no failure in the first test, the capacitors are charged again and then the second test is performed. As long as the results of each test are within limits, the tester will continue to charge the capacitors and then test the next line of the truth table until every test in the go-chain sequence has been performed. At this time the testing will terminate and the "PASS" LED will light. Testing one line of the truth table takes 49 µs.

However, if there is a failure in any test step, then the capacitors are charged repeatedly without going to the next step. At this time the LEDs corresponding to the failed pins are lit. The current values at the failed pins can be read from the front panel by pushing the proper switches. This procedure continues until the operator sends an END signal by pushing the switch S^{18} .

The time to test an UUT can be calculated as

$$t_{test} = 11\,\mu s + (LTT - 1) \times (49\,\mu s + 2{,}814\,\mu s) + 22\,\mu s\,.$$

LTT is the length of the truth table of the UUT considered. Since the length of the truth table for the 7400 is 11, then the testing time for the 7400 becomes

$$t_{test} = 11\,\mu s + (11 - 1) \times (49\,\mu s + 2{,}814\,\mu s) + 22\,\mu s$$

$$t_{test} = 11\,\mu s + 10 \times 2{,}863\,\mu s + 22\,us$$

$$t_{test} = 28{,}663\,\mu s$$

or

$$t_{test} = 28.663\ ms$$

CHAPTER 6

CONCLUSION

6.1 EXPERIMENTAL RESULTS

The program given in Figure 5.1 is applicable to all digital ICs, but each type of digital ICs require a different set of reference voltages and truth table. As described in the previous chapter the set of reference voltages and the truth table have been prepared for only the 7400, the quad 2-input NAND gate. Several 7400s have been tested with the built up tester. Testing a 7400 takes 28.663 ms.

Testing accuracy is determined by three factors: the resolution of the DAC, the tolerance of the resistors used in the unity gain differential amplifier (the four R_2 resistors in Figure 4.2), and the drift rate of the capacitors in the sample-and-hold circuits.

Resolution of a DAC is defined as the smallest change that can occur in the analog output as a result of a change in the digital input. Referring to Figure 4.4, the DAC 0808 and its auxiliary circuit have been so designed that the resolution is about 19 mV. This results from the fact that the DAC 0808 is a 8-bit converter and the analog output voltage, V_{11} , has a maximum value of 5 V.

To see the effect of the resolution of the DAC, let us consider the reference voltage V_2 for an output pin. Referring to Table 5.1, we see that the maximum voltage of an output pin in the "0" state, V_{OL}, is 0.4 V. Therefore, the "0" state voltage, V_2, for that pin must be 0.4 V. To load this data into the test program, it must be converted to binary form. Since the output voltage of the DAC is 5 V for a digital input of "11111111" (255 in decimal), to get an output voltage of 0.4 V the digital input must be

$$\frac{0.4}{5} \times 255 = 20.4 \qquad \text{(in decimal)}$$

$$20.4_{10} \cong 00010100.011_2 \qquad (6.1)$$

The binary number calculated in Equation (6.1) has an integer part and a fraction part. Since we cannot deal with the fraction part, we must take that binary number as "00010100" or "00010101". For a digital input of "00010100", the output voltage of the DAC becomes 0.392 V while for a digital input of "00010101", it becomes 0.412 V. Hence, if we take the binary number as "00010100", there will be an error of 8 mV. However, if we take that binary number as "00010101", then the error due to the resolution of the DAC will be 12 mV.

The tolerance of the resistors used in the unity gain differential amplifier effects the accuracy of testing directly. In the built up tester, these resistors are carefully se-

lected, and they have a tolerance of 0.5 %. Therefore, the error made in measurement due to these resistors is about 0.5 %.

Discharging of the capacitors in the sample-and-hold circuits is due to the bias currents of the operational amplifiers and the leakage currents of the CMOS switches. The LF 13741 has a maximum bias current of 50 pA while the leakage current of a CMOS switch may be as much as 5 nA. Therefore, the bias currents of the operational amplifiers can be neglected. Since the maximum hold period of the capacitors used in the sample-and-hold circuits is about 3 ms, we can calculate the maximum drift voltage as

$$\Delta V_{max} = \frac{t_h \times i_l}{C}$$

$$\Delta V_{max} = \frac{3.10^{-3} \times 5.10^{-9}}{10^{-9}}$$

$$\Delta V_{max} = 15.10^{-3} V = 15 \text{ mV} \qquad (6.2)$$

This calculated result has been confirmed experimentally.

The accuracy of the voltage applied to a pin is determined by adding the resolution of the DAC and the drift voltage of the capacitor. This makes 34 mV.

The accuracy of the current measurement at a particular

pin is determined by only the tolerance of the resistors used in the unity gain differential amplifier.

6.2 CONCLUDING REMARKS

Testing accuracy can be improved by decreasing the leakage current. This can be achieved by putting additional buffers in the circuitry.

The principle of testing was to apply a reference voltage to each pin of the UUT and to measure the current at each pin, and then to compare it against predetermined current limits. An alternative method is to apply a reference current to each pin of the UUT and to measure the voltage at each pin, and then to compare it against predetermined voltage limits. This alternative method has the advantage that the value of the current at each pin is known, so that we can calculate the currents at the supply pin and at the ground pin for any UUT without making any estimation. However, that kind of tester requires voltage-to-current converters that cost too much.

APPENDIX

1- MAIN PROGRAM

```
0000   CE 8004   LDX #8004
0003   6F 01     CLR 1, X
0005   6F 03     CLR 3, X
0007   6F 05     CLR 5, X
0009   6F 07     CLR 7, X
000B   86 FF     LDAA #FF
000D   A7 00     STAA 0, X
000F   A7 02     STAA 2, X
0011   A7 04     STAA 4, X
0013   A7 06     STAA 6, X
0015   86 04     LDAA #04
0017   A7 01     STAA 1, X
0019   A7 03     STAA 3, X
001B   86 34     LDAA  34
001D   A7 05     STAA 5, X
001[illegible]   86 06     LDAA #06
0021   A7 07     STAA 7, X
0023   CE 0200   LDX #0200
0026   BD 006F   JSR
0029   BD 009E   JSR
002C   B6 8008   LDAA
```

```
002F   86 3C     LDAA #3C
0031   B7 8009   STAA
0034   B6 8009   LDAA
0037   2B 05     BMI
0039   BD 006F   JSR
003C   20 F6     BRA
003E   86 0A     LDAA #0A
0040   B7 01FF   STAA
0043   BD 009E   JSR
0046   7A 01FF   DEC
0049   27 16     BEQ
004B   B6 800A   LDAA
004E   B6 800B   LDAA
0051   2B 05     BMI
0053   BD 006F   JSR
0056   20 EB     BRA
0058   BD 006F   JSR
005B   B6 800B   LDAA
005E   49        ROLA
005F   2A F7     BPL
0061   7F 8008   CLR
0064   7F 800A   CLR
0067   86 34     LDAA #34
0069   B7 8009   STAA
006C   7E F0E1   JUMP
```

2- "CHARGE-UP HOLDING CAPACITORS" SUBROUTINE

```
006F   FF 01FB    STX
0072   CE 0300    LDX #0300
0075   36         PUSHA
0076   86 10      LDAA #10
0078   B7 01FE    STAA
007B   86 04      LDAA #04
007D   B7 01FD    STAA
0080   A6 00      LDAA 0, X
0082   B7 8006    STAA
0085   08         INX
0086   A6 00      LDAA 0,X
0088   B7 8004    STAA
008B   08         INX
008C   7A01FD     DEC
008F   26 EF      BNE
0091   7A 8006    DEC
0094   7A 01FE    DEC
0097   26 E2      BNE
0099   32         PULA
009A   FE 01FB    LDX
009D   39         RTS
```

3- "TRANSFER ONE LINE OF TRUTH TABLE" SUBROUTINE

```
009E   A6 00     LDAA 0,X
00A0   B7 8008   STAA
00A3   08        INX
00A4   A6 00     LDAA 0,X
00A6   B7 800A   STAA
00A9   08        INX
00AA   39        RTS
```

4- TRUTH TABLE (For 7400, quad 2-input NANDggate.)

```
0200   2412
0202   2492
0204   2DB6
0206   36DA
0208   33DA
020A   36DA
020C   1EDA
020E   36DA
0210   36DC
0212   36DA
0214   36EA
```

5- ADDRESSES AND VOLTAGES OF HOLDING CAPACITORS (For 7400)

Address	Voltage
0300	0166
0302	2129
0304	4181
0306	617E
0308	0366
030A	2329
030C	4381
030E	637E
0310	057A
0312	2515
0314	456E
0316	657F
0318	0766
031A	2729
031C	4781
031E	677E
0320	0966
0322	2929
0324	4981
0326	697E
0328	0B7A
032A	2B15
032C	4B6E
032E	6B7F
0330	0D00
0332	2D00
0334	4DC0
0336	6D00
0338	0F00
033A	2F00
033C	4FFF
033E	6F00
0340	1100
0342	3100
0344	51FF
0346	7100
0348	137A
034A	3315
034C	536E
034E	737F
0350	1566
0352	3529
0354	5581
0356	757E
0358	1766
035A	3729
035C	5781
035E	777E
0360	197A
0362	3915
0364	596E
0366	797F
0368	1B66
036A	3B29
036C	5B81
036E	7B7E
0370	1D66
0372	3D29
0374	5D81
0376	7D7E
0378	1FF3
037A	3F00
037C	5FFF
037E	7F28

APPENDIX B

IC TESTER-MICROCOMPUTER INTERFACE

The IC tester cannot be used without a microcomputer. As far as the microcomputer is concerned, the IC tester has 32 input lines and 3 output lines. The line layout of the IC tester is shown in Figure B.1.

The inputs DAC-1 through DAC-8 to the IC tester are taken from the one side of the one of the PIA units of the microprocessor. The other side of the same PIA supplies the seven ADD inputs to the tester.

The second PIA supplies the 16 TT inputs to the tester. In this case, the two sides of that PIA are used for the TT inputs. The control lines of that same PIA are used for the input LED, and for the outputs FAIL, SW-1, and SW-2.

The input and output lines of the tester require voltages between 0 and 5 V. All the lines mentioned above have been marked on the tester.

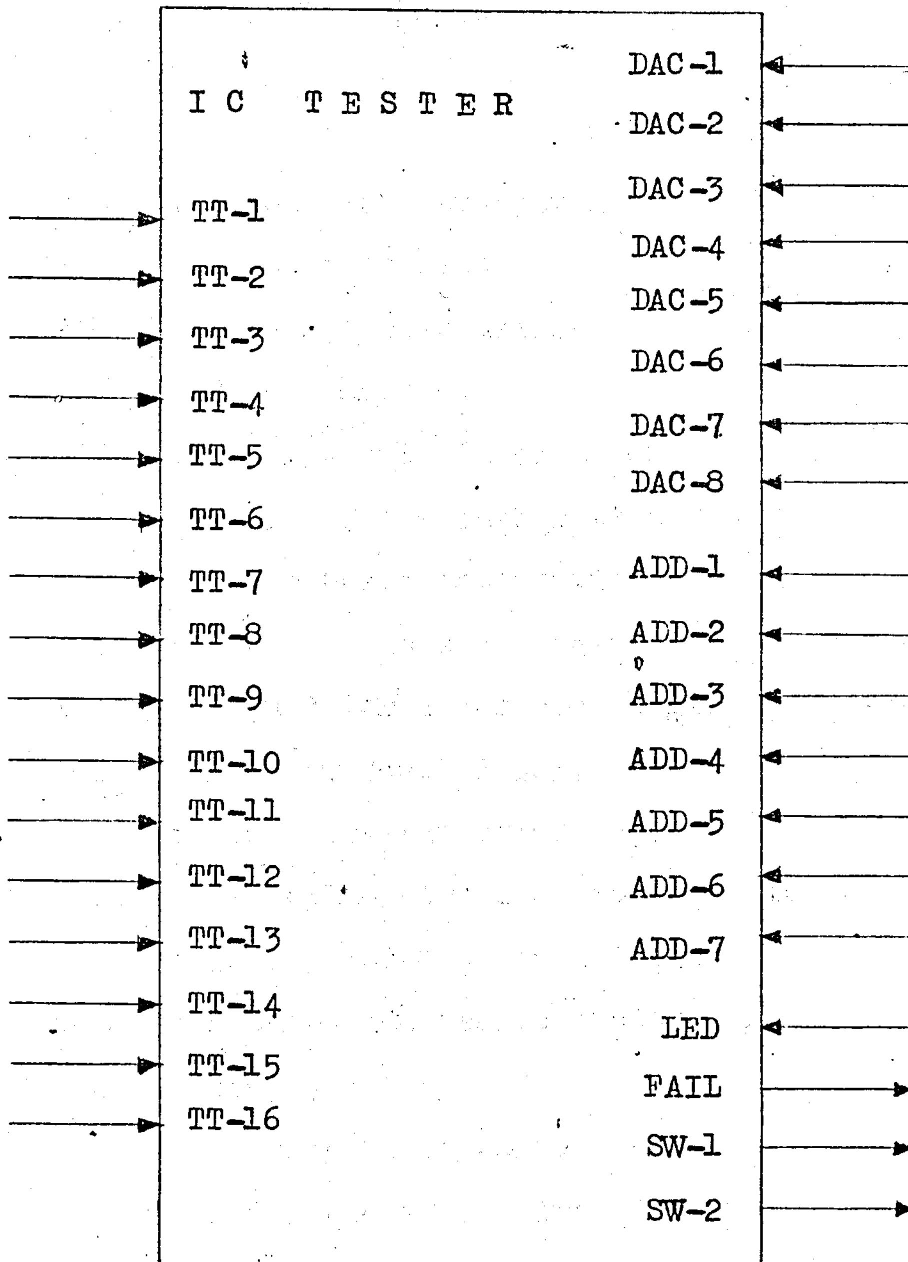


Figure B.1 The line layout of the IC tester.

NOMENCLATURE

ATS : Automatic Test System
UUT : Unit Under Test
RAM : Random Access Memory
ROM : Read-Only Memorl
SSI : Small -Scale Integration
MSI : Medium-Scale Integration
LSI : Large-Scale Integration
DTL : Diode-Transistor Logic
TTL : Transistor-Transistor Logic
ECL : Emitter-Coupled Logic
RTL : Resistor-Transistor Logic
DCTL : Direct-Coupled Transistor Logic
I L : Integrated-Injection Logic
MOS : Metal-Oxide-Semiconductor
CMOS : Complementary MOS
SOS : Silicon-On-Sapphire
MOSFET: MOS Field-Effect Transistor
IC : Integrated Circuit
CML : Current-Mode Logic
PIA : Peripheral Interface Adapter
LSB : Less Significant Bit
MSB : Most Significant Bit

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