A PORTABLE AND SENSITIVE ELECTROMETER AMPLIFIER FOR ASTRONOMICAL USE

by

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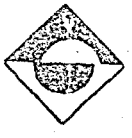

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ABSTRACT

In this thesis, a portable and sensitive electrometer amplifier which can measure the very small starlight and provide its supply from both the mains and the 12 V car-battery is built.

The design of the electrometer amplifier is described, and the theoretical and experimental values are given.

KISA ÖZET

Bu çalışmada, hem şehir şebekesinden hem de şehir dışında, 12 V luk bir doğru akım bataryasından beslenerek çok zayıf yıldız ışık seviyelerini ölçebilecek, taşınabilir ve duyarlı bir elektrometrik kuvvetlendirici yapılmıştır.

Elektrometrik kuvvetlendiricinin tasarımı ve uygulaması yapılarak teorik ve deneysel sonuçları verilmiştir.

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INTRODUCTION

Our understanding of the universe depends on the careful analysis of light reaching the earth. The intensity and spectral characteristics of the light gives us the knowledge about the regions of the space to which the space vehicles are not accessible. Thus, astronomers have great use for the electrometer amplifier, an instrument for measuring the apparent brightnesses of celestial objects in several wavelengths, usually by means of a photomultipier tube.

It is less difficult to determine accurate magnitudes by electrometric methods than by direct sky photography. Because the photographic process has the more complex nature. Moreover, photoelectric data are more readily reduced to numerical results.

Therefore, the electrometric methods are superior to other methods for the astronomic observations. The main advantages of the electrometer amplifier to be designed in this work are its low cost and relatively high sensitivity, its being portable and the possibility to power it from a d.c. supply (car battery) for field operation.

The electrometer amplifier which has these properties consists of two section:

a. Electronic section

b. Mechanical and optical sections

In this work, the electronic section is designed, and the mechanical and optical sections are available in the Astronomy Department of Faculty of Science of Istanbul University.

The electronic section consists of four parts:

1. Electrometer.
2. D.C. power suply for the photomultiplier tube.
3. 12 - 220 V Inverter for the field operation.
4. Photomultiplier tube.

The complete block diagram of the system is shown and each part is discussed in the following chapters.

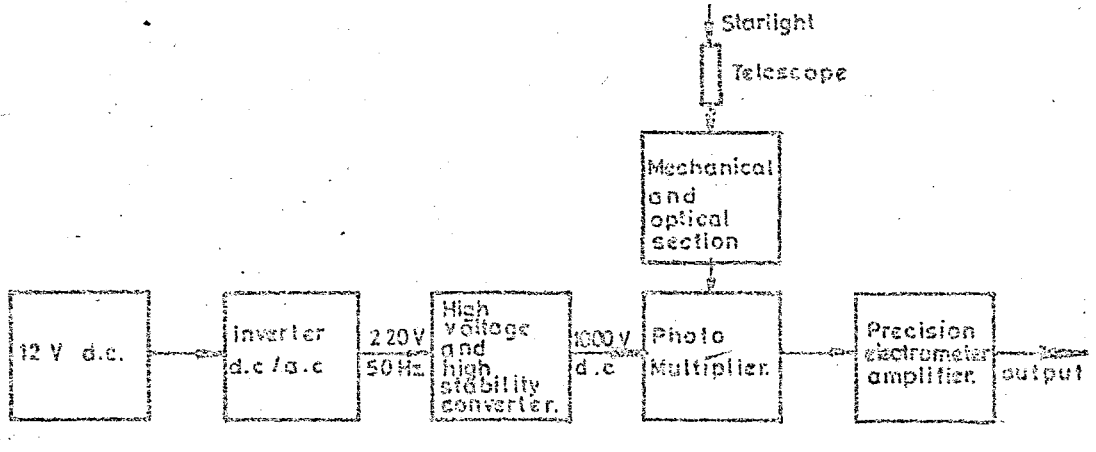

Fig. 1. The block diagram of the electrometer amplifier

CHAPTER I

E L E C T R O M E T E R S

An electrometer is an instrument which measures the very small currents, charges, voltages less than 10 V and sometimes resistance.

An electrometer is usually able to accept either a voltage input from source with a high internal impedance or a very low current such as the current from the photomultiplier tube, ionization chamber etc.

The electrometers can be classified as direct indicating electrometers or electronic electrometers. Whereas direct indicating electrometers rely for their operation on the electrostatic principle, electronic electrometers operate as voltage measuring amplifiers having such a high input resistance (usually above $10^{10}\Omega$).

1.1. DIRECT INDICATING (PASSIVE) ELECTROMETERS

These electrometers utilize the force of attraction or repulsion existing between to electrically charged bodies to produce a physical displacement of one or both members

of the system. Such movement serves as an indication of the presence of an electric change and, if calibrated, provides a measure of the magnitude of the charge.

The gold-leaf electroscope employs two thin strips of gold-leaf attached to a conducting rod which serves as support and as a means of imparting the electric charge to to the gold leaf(Fig. 2a). If an electric charge is placed on the metal ball (Fig. 2b), the charge distributes throughout the ball, rod, and leaves; for example if the charge is negative, each excess electron is repelled by all other excess electrons and assumes a position of equilibrium within the bounds of the conducting system. Since the charges on the two leaves are of like sign, the force between them causes them to stand apart. Some electrostatic voltmeters operate on the same principle as the gold-leaf electroscope and are used to measure voltages as low as millivolts and as high as hundreds of kilovolts.

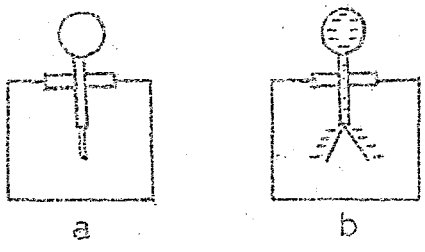

Fig. 2 Gold-leaf electroscope

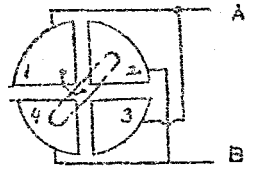

Fig. 3 Quadrant electrometer

The quadrant electrometer, (Fig. 3) utilizes both the force of attraction between charged bodies of like sign. A movable vane v, free to rotate against the torsion of a suspending wire, is connected to quadrant 1 and 3. If an electric potential is connected between terminals A and B

the vane is attracted toward quadrants 2 and 4 and is repelled by quadrant 1 and 3. A measure of the angular displacement of the vane indicates the magnitude of the potential.

1.2. ELECTRONIC ELECTROMETERS

Electronic electrometers exploit the ability of an electrostatic field to control a current flow either in a vacuum or in a solid, through a thermionic tube or a transistor respectively.

1.2.1. Vacuum tube electrometers

These electrometers detect and measure electric current by measuring the voltage drop produced by the current in a known resistance. In the basic circuit of Fig. 4, R_b is adjusted to balance the plate current of the vacuum tube to establish a zero reading on meter M with zero input current. An input current produces a change in grid voltage, $e_g = -i_{in} R_g$, and meter M reads the resulting change in plate current. If R_g is chosen as $10^{12}\Omega$ and the vacuum tube has a transconductance of 100μmhos, an input current of 10^{-13}A produces a meter reading of 10 μA. The circuit therefore provides a current gain of 10^8. However, only especially

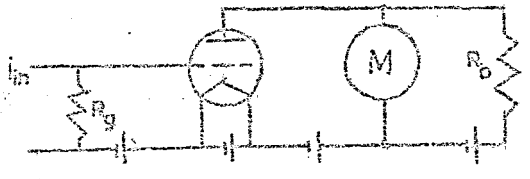

Fig. 4. Vacuum tube electrometer

designed vacuum tubes are capable of operation in electrometer applications.

1.2.2. Semiconductor electrometers (1)

Continuous development and revolutionary changes in transistor technology have led to the high-performance, reliable b.j.t. (bipolar junction transistor) devices of today. These developments have also facilitated the belated realisation of a range of f.e.t.s (field effect transistors).

Apart from an obvious disparity in size between tubes and semiconductors other advantages of semiconductors are freedom from microphony, potentially longer life and absence of heater supplies. In addition, the superior matching and temperature tracking of characteristics obtainable with two monolithic transistors have advantages if a balanced input stage is envisaged. On the other hand, semiconductors in general are more prone to damage when subjected to higher-than-rated currents and voltages, In the case of the i.g.f.e.t., the thin gate insulator in Fig. 5, which is typically 0.1 μm thick, is particularly prone to breakdown if spurious charges are induced on the gate, either during handling or subsequent circuit operation.

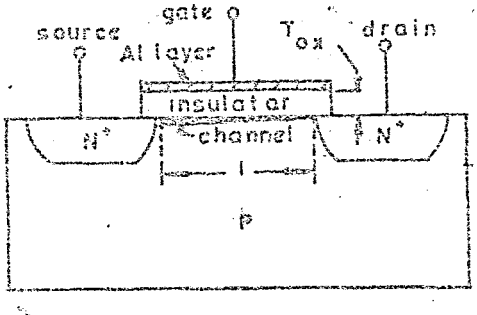

Fig. 5. Schematic representation of an N-channel i.g.f.e.t.

In the systems discussed in this section, the electrometer stage forms the input stage of a multistage voltage amplifier. In the case of the voltage-voltage convertor of Fig. 6, feedback (not shown explicitly) is assumed to give a closed-loop voltage gain A_v'. In the case of the current-voltage of Fig. 7, the measuring resistor R_F provides overall voltage feedback to the basic amplifier with an open-loop gain A_v.

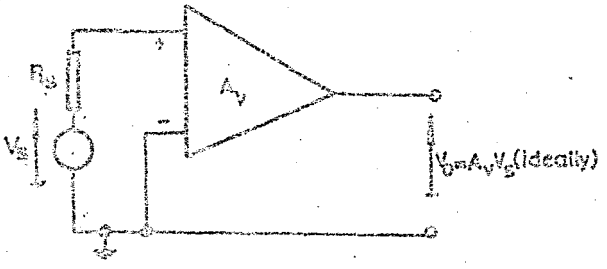

Fig. 6. Voltage-voltage convertor

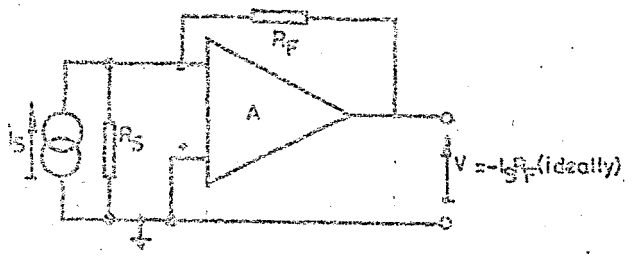

Fig. 7. Current-voltage convertor

In these convertors, the output is normally a voltage proportional to the input variable.

1.2.2.1. D.C. analysis of electrometer

It is shown in Appendix I that, for the case of the voltage voltage convertor, the fractional error occuring at the output of the electrometer due to the input leakage current i_1, input resistance R_i and offset voltage v_{os} is given by

$$\varepsilon_v = \frac{1}{(R_s + R_i)} \left(\frac{V_{os} R_i}{v_s} + \frac{i_1 R_s R_i}{v_s} - R_s \right) \qquad (1)$$

For the current-voltage convertor, the corresponding error is shown in Appendix I to be given by

$$\varepsilon_i \simeq \frac{i_1}{i_s} - \frac{v_{os}}{i_s R_i'} - \frac{1}{A_v} - \frac{R_f}{A_v} \left(\frac{1}{R_s} + \frac{1}{R_i} \right) \qquad (2)$$

where $R_i' = R_i /\!\!/ R_s$

For the case of the voltage voltage convertor, the effects of finite input resistance are clearly minimised by ensuring that $R_i \gg R_s$. With this condition, eqn. 1 approximates to

$$\varepsilon_v \simeq \frac{v_{os}}{v_s} + \frac{i_1 R_s}{v_s} \qquad (3)$$

From eqn. 3, the minimum voltage that can be measured for a given allowable error is determined by theamplifier offset voltage and leakage current, the latter in conjunction with the source resistance R_s. For $R_s > \frac{v_{os}}{i_1}$, leakage current is the dominant source of error, but for $R_s < \frac{v_{os}}{i_1}$, offset voltage dominates.

For the current-voltage convertor, the last three terms in eqn. 2 are minimised if $A_v \gg 1$, $R_s \gg \frac{R_f}{A_v}$, $R_i \gg \frac{R_f}{A_v}$. These conditions are usually met in most practical systems, resulting in

$$\mathcal{E}_i \approx \frac{i_1}{i_s} - \frac{v_{os}}{i_s R_f'} \qquad (4)$$

Once again, the minimum signal that can be measured for a given allowable error is determined by leakage current and offset voltage. For $R_f' > \frac{v_{os}}{i_1}$, leakage current dominates and for $R_f' < \frac{v_{os}}{i_1}$, offset voltage dominates. In many applications the condition $R_f \ll R_s$ is met and $R_f' \simeq R_f$.

To obviate these offset-voltage and leakage-current errors it is theoretically possible to set the quiescent conditions of an electrometer stage to effectively reduce v_{os} to zero (this type of procedure is commonly used to trim the offset voltage of standard operational amplifiers to zero). At same time it is possible to inject into the amplifier input terminal a small fixed current (2) to effectively cancel the effects of i_1. Another possibility is deliberately to set the electrometer quiescent conditions so that the offset voltage assumes a value that satisfies the conditions

$$v_{os} + i_1 R_s = 0 \qquad \text{and} \qquad v_{os} - i_1 R_f = 0 \qquad (5)$$

for the voltage-voltage and current-voltage convertors, respectively. In these cases, the offset voltage effect is used to balance the leakage-current effect, and a cancellation occurs in the error terms in eqns. 3 and 4.

In practice only marginal advantages are achieved by these measures, as both v_{os} and i_1 are generally temperature

dependent. Thus, although the effective error terms may be trimmed to zero, (dv_{os}/dT) and (di_1/dT) are nonzero and a change in ambient temperature will necessitate either a re-trimming of v_{os} or the presence of an error in the electrometer reading.

For these reasons it becomes apparent that when the electrometer is subjected to ambient-temperature fluctuations necessary conditions for maximum electrometer sensitivity are that v_{os}; $\frac{dv_{os}}{dT}$; and i_1; $\frac{di_1}{dT}$ should be minimized. The considerations effecting offset voltage and leakage current are considered in the next section.

1.2.3. OFFSET VOLTAGE AND LEAKAGE CURRENT

1.2.3.1. Offset voltage mechanisms in single-ended and balanced input stages

To illustrate the factors responsible for amplifier offset voltage, practical implementations of the schematic current-voltage convertor of Fig. 7 will be referred to. N-channel enhancement-mode i.g.f.e.t. devices are arbitrarily chosen it these circuits, but the conclusions arrived at apply also to similar circuits using the other i.g.f.e.t. variations as well as b.j.t.s, provided suitable bias changes are made. A single-ended i.g.f.e.t. input stage is shown in Fig. 8a and a balanced (long-tail pair) input stage is shown in Fig. 9. It is assumed that, in each case, the input stage alone produces insufficient voltage gain to

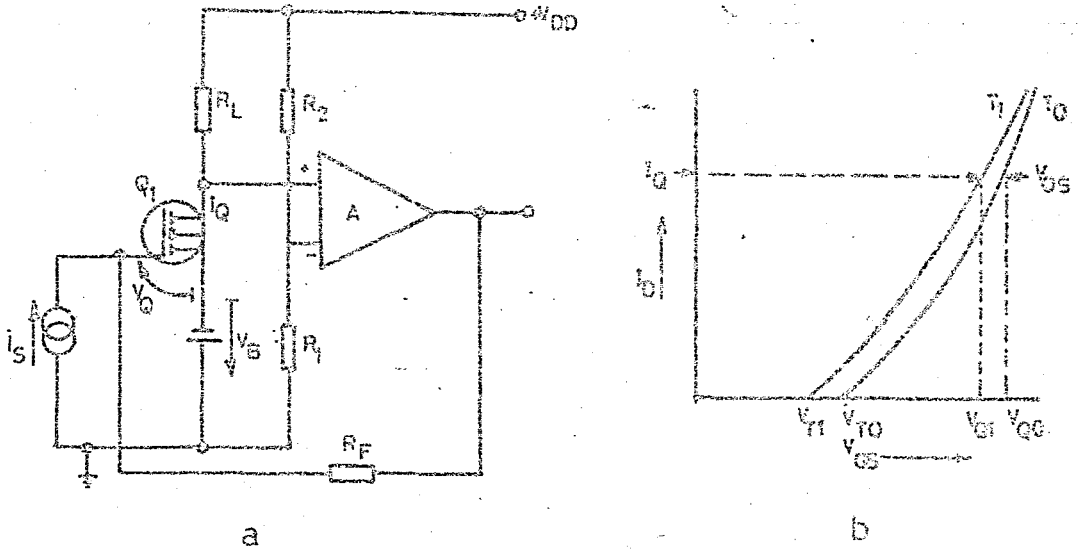

Fig. 8. a. Current-voltage convertor with a single-ended i.g.f.e.t. input stage

b. Mutual characterisitcs of an i.g.f.e.t. operating in the pinch-off region for two temperatures

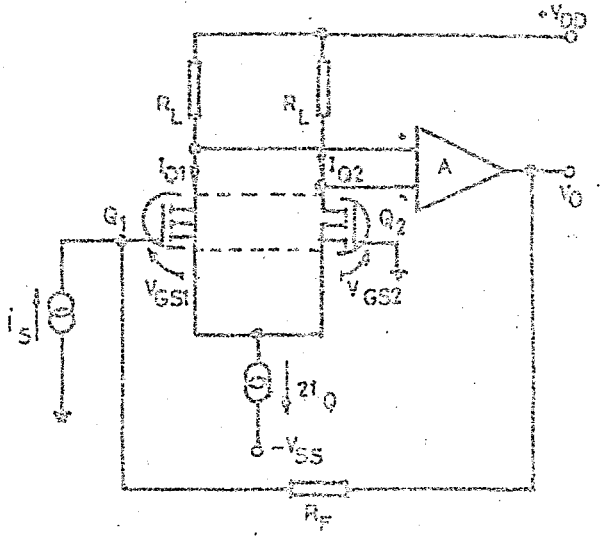

Fig. 9. Current-voltage convertor with a balanced (long-tail pair) i.g.f.e.t. input.

satisfy the conditions necessary for reducing the last three terms in eqn. 2 to negligible proportions, and the necessary additional voltage gain is produced by a high gain stage A. A, would typically be an op-amp. It is further

assumed that A is chosen with sufficiently low offsets for their effects to be negligible when referred to the gate terminal of the i.g.f.e.t.

For both types of input stage, the i.g.f.e.t.s involved operate under essentially constant-drain-current conditions by virtue of the high voltage gain of A. For Fig. 8a, the drain current will take the value necessary to bring the noninverting(+) terminal of A to the same potential as the inverting term terminal(-), i.e.

$$I_Q = \frac{V_{DD}\, R_2}{R_L\,(R_1 + R_2)} \qquad (6)$$

For the circuit of Fig. 9, the drain currents are determined by the source current $2I_Q$ which could be realised by a simple resistor of appropriate value or preferably by a b.j.t. common-base stage. If Q_1 and Q_2 are reasonably well matched, we have

$$I_{Q1} \simeq I_{Q2} = I_Q \qquad (7)$$

A typical 'mutual' characteristic for an i.g.f.e.t. operating in the normal pinch-off region (3) is shown in Fig.8b. To establish a drain current I_Q at a datum temperature T_o in the circuit of Fig. 8a, a gate-source bias V_{Qo} is required. The offset voltage is given for $T = T_o$ by

$$V_{os}(T_o) = (V_{Qo} - V_B) \qquad (8)$$

$v_{os}(T_o)$ can be set to zero if V_B is set equal to V_{Qo}. However, if the temperature changes to T_1, temperature drift mechanisms in the i.g.f.e.t. can cause V_{Qo} to shift to V_{Q1} as shown. If V_B is not readjusted to compensate, $v_{os}(T)$ is then given by

$$v_{os} = -(V_{Qo} - V_{Q1}) \qquad (9)$$

For the balanced input stage of Fig. 9, the offset voltage is given by $V_{GS1} = V_{GS2}$, and v_{os} is zero for all temperatures. In this case the matched i.g.f.e.t.s always maintained at similar temperatures, then V_{GS} variations of one device are compensated exactly by identical variations in the other device.

If a small mismatch exists in the I_D/V_{GS} characteristics of Q_1 and Q_2, then, in general, $V_{GS1} = V_{GS2}$ and v_{os} will be nonzero. (The action of the amplifier A ensures that, even for mismatched devices, the drain currents of Q_1 and Q_2 will be maintained at similar levels, and the mismatch between the two devices is absorbed by either an increase or a reduction in the gate-source bias of Q_1 relateve to Q_2. This produces a positive or negative v_{os}, respectively).

The nonzero v_{os} resulting from mismached devices can be artificielly trimmed to zero by, for example, adding resistors in series with the sources of either Q_1 or Q_2. However, as the temperature varies, the differential behaviour of the two V_{GS} bias potentials will again produce

a nonzero V_{os}. For the electrometer with the single-ended input stage, the offset-voltage uncertainty results from the temperature variations in V_{GS} of the input i.g.f.e.t. when it is operated at a constant drain current, i.e.

$$\left|\frac{dV_{os}}{dT}\right| = \left|\frac{dV_{GS}}{dT}\right|_{I_D} \tag{10}$$

For a balanced input stage, the offset-voltage uncertainty results from the differential temperature changes in the two gate-cource voltages when the two devices are operated under constant-drain-current conditions,

$$\left|\frac{dV_{os}}{dT}\right| = \left|\frac{d\,(V_{GS1} - V_{GS2})}{dT}\right|_{(I_{D1}, I_{D2})} \tag{11}$$

1.2.3.2. Offset-voltage temperature drift in f.e.t.s and b.j.t.s

In terpreting eqn.10 for the case of a single-ended b.j.t. stage gives

$$\frac{dV_{os}}{dT} = \left.\frac{dV_{BE}}{dT}\right|_{I_C} \tag{12}$$

It is well known that when a b.j.t. is operated at a fixed collector current and the temperature of the device is increased, the magnitude of the base-emitter bias potential decreases by approximately $2mV/^{o}C$. This is only weakly dependend on the collector current. A value of (dV_{os}/dT) of this magnitude would normally preclude the use of a single-

ended b.j.t. stage for most applications.

On the other hand, if a given j.f.e.t. or i.g.f.e.t. is operated at a fixed drain current, the corresponding variations in gate-source potential can be positive or negative depending on the drain current selected. For a unique drain current, the f.e.t. is capable of exhibiting zero drift of the gate-source voltage.

For a j.f.e.t., Honei and Weir (4) were first to discover two opposing temperature-dependent mechanisms which were responsible for this behaviour. The channel conductivity decreases whereas the barrier potential decreases with increasing temperature. The former mechanism (which causes the magnitude of the gate-source voltage to decrease when the drain current is constant and the tmperature increases) dominates at higher drain currents. Zero gate-source voltage drift occurs at the unique drain current where the two effects cancel exactly.

For an i.g.f.e.t., a zero-drift operating point similar to that of the j.f.e.t. also exists. In this case, threshold voltage temperature variations cancel channel conductivity variations at the zero drift point(5).

In principle, therefore, it is possible to employ a single f.e.t. in the input stage of an electrometer as in Fig. 8a. and achieve zero offset-voltage drift. This(6) approach suffers from two major drawbacks.(5). The zero-

drift operating point, being a point of inflection in the V_{GS} temperature plane, is valid only for a fixed temperature (7). A small error in establishing this operating point can give rise to significant additional V_{GS} drift. In the case of an i.g.f.e.t., for instance, temperature departures of 10% from the true zero drift-temperature would typically cause V_{GS} to drift by $\mp$ 0.2 mV. (5,7). If an error of only 1 % is made in biasing the i.g.f.e.t. drain current, causing the operating quiescent current to differ from the true current required for zero V_{GS} drift at a given temperature, the V_{GS} drift can exceed 0.4 mV for temperature departures of 10°C.

In practice, significant improvements in (dV_{os}/dT) can be achieved if a balanced electrometer stage such as Fig. 8a is used. Interpreting eqn. 11 for a balanced b.j.t. stage gives

$$\left| \frac{dV_{os}}{dT} \right| = \left| \frac{d\,(V_{BE2} - V_{BE1})}{dT} \right|_{I_{C1}, I_{C2}} \qquad (13)$$

Thus (dV_{os}/dT) represents the differential drift of the individual transistors, which should ideally be biased at equal currents. Clearly the resulting (dV_{os}/dT) that is possible is determined by the degree of matching of the constituent transistors. In this respect, b.j.t.s. are significantly superior to f.e.t.s.

The reasons for this situation are complex but are largely due to the superior mutual conductance of the b.j.t., which approaches the theoretical maximum of (qI_c/kT). This feature of the b.j.t. ensures that the various factors such as geometry variations due to imperfect photolithography, which account for mismatches in nominally identical devices result in smaller V_{BE} mismatches than the corresponding, V_{GS} mismatches in the case of f.e.t.s. For b.j.t. pairs, offset voltages and offset-voltage drifts of 1 mV and 3 $\mu V/^oC$ are routinely available, while precision-matched devices such as MAT-01 (PMI) and LM 94 (National Semiconductor) can offer corresponding figures approaching 25 μV and 30nV/^oC

In the case of f.e.t., the best v_{os} matching generally available in j.f.e.t.s is 5mV, corresponding with a (dv_{os}/dT) value of 5 $\mu V/^oC$, for the AD 840 (Analog Devices), 2N 5520 (Siliconix), BFQ 10 (Mullard).

Although a number of matched-i.g.f.e.t.-pair types available from various manufacturers are potentially suitable for electrometer applications the typical V_{GS} matching of 50 mV is relatively poor compared with j.f.e.t.s and no firm information an (dv_{os}/dT) is normally given. However, a selection procedure has been used to select devices with $(dv_{os}/dT) < 50\ \mu V/^oC$.(8)

1.2.3.3. Input leakage current

The input leakage current of electrometer input stages

of the type shown in Fig. 8a and Fig. 9 is normally the gate current or base current of the input transistor.

For a b.j.t., the base current is a composite term including the effects of recombination, back injection into the emitter and leakage across the collector-base junction. As the relative contributions of these mechanisms to the total base current vary with transistor type as well as in a given type with biasing conditions, no simple relationship exists which defines (dI_B/dT) for the general case. However, some idea of the lower limit for (dI_B/dT) can be obtained by considering the collector base leakage current component $I_{CBO}/dT = 0.07\ I_{CBO}$. At room temperature, I_{CBO} can be as low as 0.1 pA for devices such as the 2N 4044 when operated with V_{CB} = 1 V. This estimate suggests that (dI_B/dT) 10fA/°C. Normally however, (dI_B/dT) 10×10^{-15} A/°C.

In the case of a j.f.e.t. the situation is simpler, as almost the entire gate current is accounted for under normal operating conditions-by leakage current across a reverse-biased p-n junction. The temperature dependency is of the same form as that for I_{CBO} in a b.j.t.

For an i.g.f.e.t., represented schematically in Fig.5, the gate electrode is isolated from the channel region by a thin layer of silicon dioxide approximately 0.1 μm thick. The device or device pair is mounted in a header of the type shown in Fig. 10, with the gate (together with other electrodes) bonded to the leads protruding through the base of

the header. The resulting gate current of this arrangement consists of a number of components, including leakage across the silicon dioxide layer, through the bulk and across the surfaces of the header glass as a result of the bias potentials applied to the device leads. (These comments do not apply to i.g.f.e.t.s with integral protection diodes, which would normally not be considered for electrometer applications as their gate currents are relatively large).

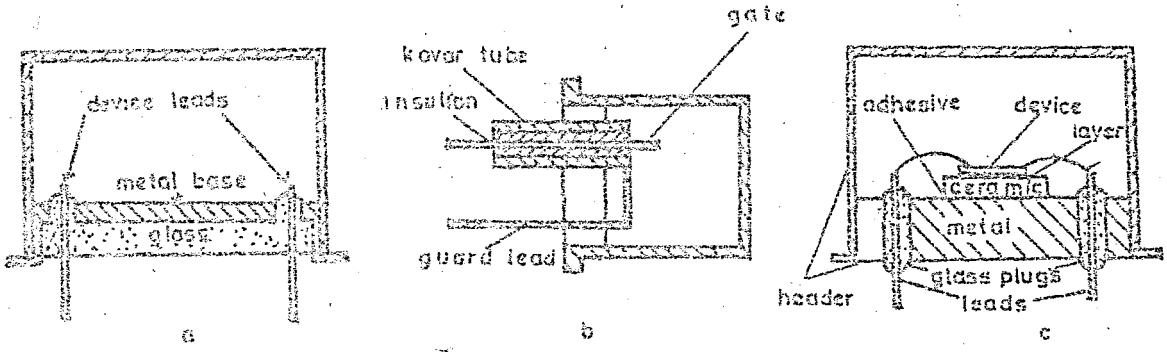

Fig. 10. a. Standard device header, b. Header providing a guarding facility for the gate lead, c. Header guard for gate lead

Typically, the gate current of small-signal i.g.f.e.t.s such as types MEM 551 and MT 102B is 10 fA ($\doteq 10^{-15}$A) but no reliable information on (dI_G/dT) can be given, as this dependent on the nature and composition of the various intrinsic and extrinsic leakage currents.

1.2.3.4. Minimising the effects of input leakage current

A common technique used with b.j.t. input operational amplifiers to minimise the effects of input currents on system accuracy is to arrange that the effective resistances

to earth for both inverting and noninverting inputs are equal. Under these circumstances, it is the input offset current $i_{os} = I_{B1} \sim I_{B2}$ and (di_{os}/dT) rather than I_{B1} and (dI_{B1}/dT) that is responsible for the input current errors discussed in former section. With the balanced input stage shown in Fig. 9, this approach may be implemented by placing an additional resistor of value R_F between the gate of Q_2 and earth.

For a significant improvement in input current error, this technique relies on the good matching of the input currents of Q_1 and Q_2. This requirement is more readily achievable in b.j.t. matched pairs than in f.e.t. pairs. In addition, for many applications R_F $10^{11}\Omega$, which gives rise to significant extra expense if R_F is duplicated particularly if good quality resistors are used and significant extra noise.

Another approach that has been used with some success for j.f.e.t. input stages is the use of similar magnitude and temperature dependency but of opposite polarity to the gate current. A reverse-biased collector-base junction of a b.j.t. or the gate current of a second j.f.e.t. has been used for this purpose (Fig. 11). This approach can be successful over a very limited temperature range but the differential behaviour of the two currents can reintroduce significant errors if an extended temperature range is considered.

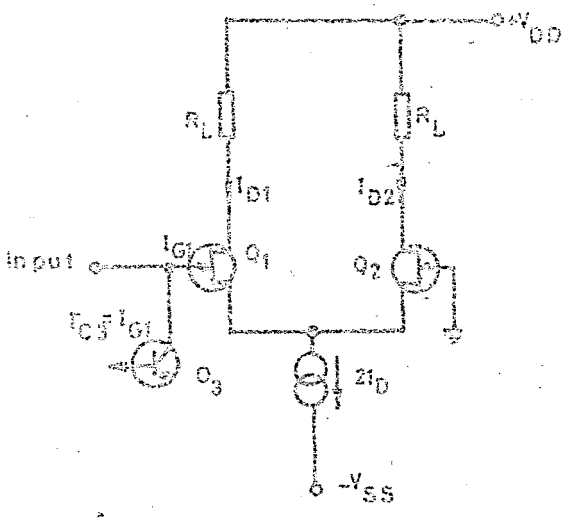

Fig. 11 Cancellation of the gate current of a j.f.e.t.

A significant feature of the gate current in i.g.f.e.t.s is the fact that its magnitude normally decays over a period of time from initial switch-on. This is associated with relaxation effects in the insulator which have long time constants. In the case of guarded gate i.g.f.e.t.s in particular, it is often advantageous to allow a warm-up time of about an hour before measurements are made to mimimize the effects of gate current.(9)

In all transistor types, input currents can be reduced if operating potentials are minimised and power dissipation kept to a minimum. All classes of transistor can, with careful selection of operating conditions, be arranged to operate with zero input current. In practice this approach suffers from the fact that the zero-input-current conditions -which may not always be attainable while at the same time keeping within the recommended ratings and achieving a good

performance as an amplifier- is normally very sensitive to small variations in operating conditions and temperature, and would therefore tend to drift.

1.2.3.5. Operational amplifiers for electrometer applications

It is sometimes possible to employ an operational amplifier with an electrometer input stage incorporated within it, effectively realising the compete function of Fig. 9, with the addition of R_F.

Such units, apart from varactor bridge types considered later, are usually hybrid arrangements incorporating an i.g.f.e.t. input stage. Typical units are 15A-36 (ANCOM) and 50200 (Keithly) which both have (dv_{os}/dT) = 150 $\mu V/^{o}C$ and input currents of 10 fA. These figures are similar to t those discussed earlier for an unguarded-gate input stage. More recently, fully integrated operational amplifiers in incorporating an i.g.f.e.t. input stage using a bipolar m.o.s. compatible process have been introduced, e.g. CA 3140 Series (RCA). Their potential in electrometer applications is, however, limited by the incorporation of integral-gate-protection diodes.

For some applications, operational amplifiers such as the the PM 156A (PMI) and 8007 (Intersil) which incorporate j.f.e.t. input stages can be used. Such devices have input offset currents of the order of 1 pA and (dv_{os}/dT) of the order of 5 $\mu V/^{o}C$.

Table 1 compares the performances of different transistor matched pairs as well as a number of operational amplifiers that may be suitable for electrometer applications.

Table 1

Input-offset-voltage drift and leakage current of matched pairs and operational amplifiers

Input stage	Type	dv_{os}/dT	I_1	dI_{i1}/dT
b.j.t. matched pair(I_C=10uA)	MAT-01	0.15 uV/°C	28nA	-
	LM 194	0.1	h_{FE}=450	-
b.j.t. op-amp	OP-07	0.2	0:7nA	8pA/°C
j.f.e.t.matched pair (I_D=200uA)	AD 840	5	≪100pA	-
	2N 5520	5	≪250pA	-
	BFQ 10	5	≪100pA	-
j.f.e.t. op-amp.	PM 156A	3	<10nA	-
	8007	5	50pA	-
i.g.f.e.t. matched pair (guarded gate)	MEM 551	50	10fA	
	MT 102B			
	MBH 1	50	1fA	0.1fA/°C
i.g.f.e.t. op-amp	50200	150	10fA	
	15A-36	150	10fA	-

1.2.4. NOISE IN ELECTROMETERS

In addition to the errors resulting from offset voltage and input current in the electrometer stage discussed earlier

additional limitations occur as a result of circuit noise. Normally this is mainly composed of noise generated in the electrometer input stage and noise generated in the high value range resistor in the case of the current-voltage convertor.

1.2.4.1. Johnson noise in R_F

Even with noise-free components in the remainder of the electrometer, a fundamental limit-under given conditions of temperature and system bandwidth-to the resolution of the electrometer is set by the Johnson noise contribution of R_F. Johnson-noise power, N, can be represented by the well known relationship

$$N = 4\ k\ T\ f_n \qquad (15)$$

where k is Boltzmann's constant (1.38×10^{-23} J/°K), T is absolute temperature and f_n is noise bandwidth in Hertz over which the measurement is being made. From the above equation, Johnson voltage and current noise developed in a resistor R_F can be found:

$$v_p = (4kTf_nR_F)^{1/2} \qquad i_p = (4kTf_n/R_F)^{1/2} \qquad (16)$$

The noise generated per $\sqrt{Hz}$ for a range of R_F commonly used in high sensitivity electrometers is given in columns 2 and 3 of Table 2. From column 3 of Table 2, it is clear that, on the basis of a fixed signal signal bandwidth, Johnson noise is minimised if R_F is maximized.

Table 2

Noise and bandwidth characteristics of high value resistors

R_F	v_p/ Hz	i_p/ Hz
Ω	mV	A
10^{11}	0.25	2.5×10^{-15}
10^{12}	0.80	0.8×10^{-15}
10^{13}	2.50	0.25×10^{-15}

In principle, it is possible to artificially restrict the electrometer bandwidth to the point where Johnson noise and other noise sources with a constant spectral density, become insignificant, compared with the drift errors. However, the excessive rise-times incurred as a result of the restricted bandwidth, together with the fact that low frequency noise mechanisms tend to dominate under these conditions, make anything other than a modest bandwidth reduction an unregarding exercise.

1.2.4.2. Transistor noise

Transistor noise in general can be modelled on a small signal basis by the addition of noise generators to the standard small signal models such as the hybrid-π model of a b.j.t. and the f.e.t. model shown in Fig. 12. (10) These noise generators represent the effects of individual noise mechanisms present in the transistor, which normally fall into one of three categories:Johnson noise, shot noise or low-frequency noise.

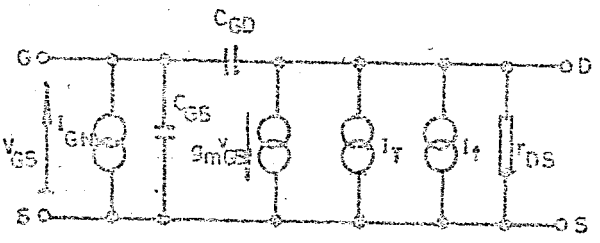

Fig. 12. Small signal model of a f.e.t. incorporating noise sources

Often it is convenient to regard the transistor amplifier as a noiseless two-port network with the transistor and other noise mechanisms lumped together as effective current and voltage generators i_n and v_n as shown in Fig. 13; this diagram, which is relevant for a current-voltage convertor also includes the noise generator e_f, relating to the noise generated in R_F.

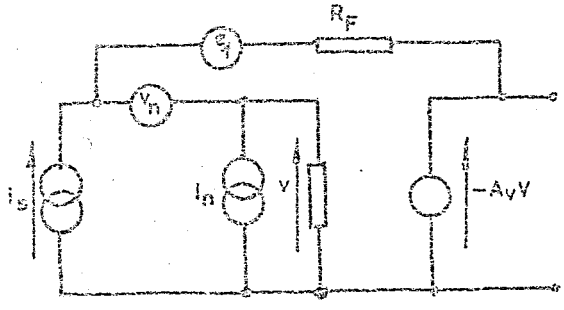

Fig. 13 Current-voltage convretor with noise mechanisms represented by current and voltage generators i_n and v_n:noise in R_F in represented by e_f.

In determining the overall noise of the electrometer a number of steps need to be taken:

a. The spectral density of each noise source must be identified.

b. the fact that each noise source can interact with the amplifier output through a frequency-sensitive network must be considered.

c. Some correlation can exist between the amplifier noise generators.

d. The effective bandwidth of the system must be known so that the correct limits can be applied when integrating the effective spectral densities of noise at the output.

e. The total r.m.s.noise is evaluated from the individual mean-square noise components at the output.

Most of the above points have been considered in some detail by various authors.(11-13)

1.2.4.3. Drift, noise, resolution and accuracy

In an electrometer, temperature and other drift mechanisms, together with noise, will be present at all times. These effects combine to give rise to various limitations in electrometer performance.

White noise becomes apparent if a wide bandwidth is required and relatively short-duration signals are being processed.

In a situation where a relatively static signal is being processed for a prolonged period, it would be possible to restrict significantly the electrometer bandwidth, thus removing white-noise effects to a large degree.

Under these circumstances, low-frequency noise becomes the dominant noise source.

With prolonged observation times, temperature-drift effects can add to the excursions produced by the low frequency noise. If the situation permits, it is beneficial to reset to zero the electrometer at intervals; this effectively reduces T.

Over a period of time, the combined effects of low-frequency noise and drift will cause a slow fluctuation in the output signal of the electrometer. In the case of current-voltage convertor, the output voltage will contain, in addition to the signal component ($i_s R_F$), an effective error component due to noise and drift.

The relative contributions of noise and drift are clearly dependent on many factors, including the choice of transistor type, range resistor etc. The electrometer with b.j.t. and j.f.e.t. sensitivities were limited by noise and drift, and the i.g.f.e.t. sensitivity was primarily limited by low frequency noise.(12)

In concluding this section some mention should be made of the nonideal behaviour of the high-value resistors used in electrometers. As well as exhibiting Johnson and excess noise, high-value resistors are characterised by relatively poor linearity, temperature drift and general stability,

Table 3 gives average values of voltage coefficient and temperature coefficient derived from published curves for Victoreen RX1 resistors.(14)

Table 3

Voltage and temperature coefficients of high value resistors

R	Voltage coefficient	Temperature coefficient
Ω	% / V	% / ^{o}C
10^{10}	-0.02	0.08
10^{11}	-0.03	0.10
10^{12}	-0.06	0.15
10^{13}	-0.13	0.22

1.2.5. Special Techniques

In addition to the standard electrometers discussed in the preceeding sections, a number of other techniques have been used to improve various aspects of electrometer performance.

1.2.5.1. Vibrating capacitor systems

The main features of a vibrating capacitor voltage-voltage convertor are illustrated in Fig. 14. C_v represents a periodically varying capacitor which varies in synchronism with the phase sensitive detector at a frequency f_m. The input voltage v_s charges C_v through R_1, the time constant C_vR_1 being large compared with the C_v variations but small

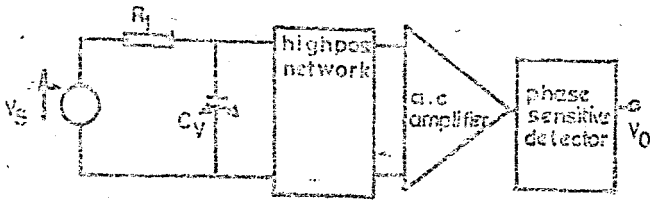

Fig. 14 Main features of a vibrating capacitor electrometer voltage-voltage convertor

compared with any signal components to be measured. An alternative voltage of amplitude $v_s(\Delta C_v/C_v)$ and fundamental frequency f_m is developed across C_v, where ΔC_v represents the fluctuation in C_v. This voltage is amplified by an a.c. amplifier tuned to amplify frequencies in the vicinity of f_m, and reconverted to d.c. by means of the phase-sensitive detector.

Various types of vibrating capacitor have been employed. (15). Normally, electromagnetic coupling is employed to vibrate the capacitor electrodes relative to each other. Frequencies up to 1 kHz are usually employed for this purpose. In some cases it is arranged that the moving element vibrates at its natural frequency, causing the movement to become sinusoidal and reducing the drive power.

Electromagnetic or electrostatic coupling can be employed to vibrate the capacitor electrodes relative to each other. In the absence of any polarisation (magnetic or electrostatic, respectively), both systems will cause the capacitor to oscillate at twice the drive frequency. Suitably polarised both systems will oscillate at the drive frequency.

As well as the voltage-voltage arrangement of Fig. 14, current-voltage and charge-voltage conversion can be obtained by means of a measuring resistor R_F or capacitor C_F, respectively, connected between input and output. The main advantage of a vibrating-capacitor system is that the effects of low-frequency noise and drift in the input stage of the amplifier are suppressed. This is due to the presence of the highpass filter between C_v and the amplifier input, which prevents modulation of C_v by low frequency noise and drift.

As with passive electrometers, a fundamental limitation on drift performance is due to contact potentials associated mainly with the vibrating capacitor.

The bandwidth of the system is limited by the presence of the relatively large time constant C_vR_1 at the input. Typically 5-10 cycles of vibration are needed for the system to respond adequately to a step function. This limitation is not normally important in maximum sensitivity applications, where the time constant C_FR_F of the current voltage convertor tends to dominate.

1.2.5.2. Varactor bridge systems

Varactor bridge systems use a principle similar to that of vibrating capacitor sytems. In this case, use is made of an element such as a semiconductor diode which exhibits a

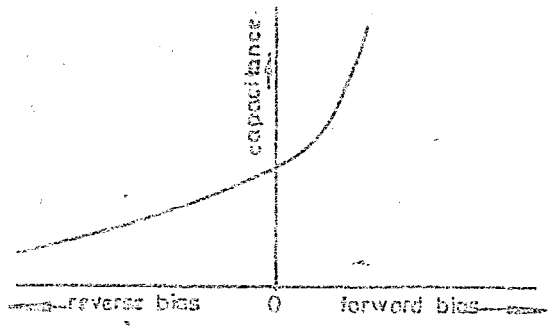

Fig. 15. Capacitance/voltage characteristic of a semiconductor diode

capacitance characteristic varying with applied voltage, as in Fig. 15.

Two diodes are normally employed in a bridge configuration as shown in Fig. 16, which illustrates the main features of the system. With no input signal, it is arranged that the bridge is balanced with $R_1C_{D1} = R_2C_{D2}$, where C_{D1} and C_{D2} are the capacitances of D_1 and D_2, respectively. Under these conditions, no signal appears at the input of the a.c. amplifier. When a voltage v_s is applied to the input, differential biasing is applied to D_1 and D_2, causing the bridge to become unbalanced. An alternating voltage related to the magnitude of v_s now appears at the input to the amplifier. This is amplified and detected in a manner similar to that of the vibrating-capacitor system.

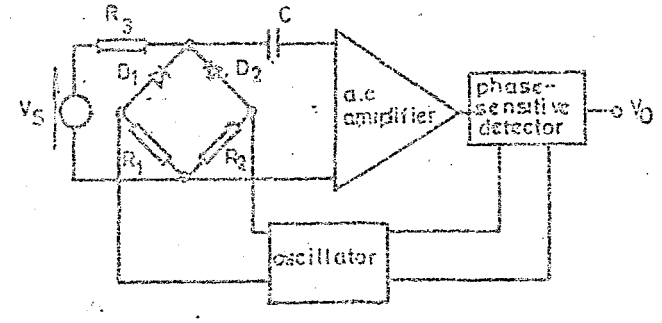

Fig. 16 Main features of a varactor-bridge voltage-voltage electrometer

As with vibrating-capacitor systems, low-frequency noise is low compared with i.g.f.e.t. d.c. electrometers. The input characteristics are determined mainly by the characteristics of the parallel combination of D_1 and D_2, which have only small polarising potentials applied to them. This results in input currents and resistances of the order of 10^{-14}A and 10^{12} respectively. This later figure can be increased by an order of magnitude if reverse polarisation is applied to the bridge diodes.(16) Since the input current doubles approximately every 10°C, the input-current temperature drift is approximately 1 fA/°C, offset voltage drift, typically 30 μV/°C, results from differential drift of the diode capacitances and the passive bridge components. Modulation frequencies of the order of 300kHz permit significantly higher bandwidths than are possible with vibrating capacitor systems. A voltage amplifier with a gain of 100 dB has a typical unity-gain bandwidth of 2 kHz.

1.2.6. Conclusions

For intermediate sensitivities, electrometers using b.j.t. j.f.e.t. and i.g.f.e.t. input stages can be used. For higher sensitivities, b.j.t. and j.f.e.t. input stages are limited by drift and noise effects. I.g.f.e.t. input stages are limited mainly by low-frequency noise at the higher sensitivities.

Vibrating-capacitor and varactor-bridge electrometers offer superior performance in terms of low-frequency noise but

have offset-voltage drifts of the order of 20-30 $\mu V/^{o}C$. The latter also has an input-current drift of the order of 1 $fA/^{o}C$. These details are summarised in Table 4.

Table 4

Comparison of parameters of main electrometer systems

	i.g.f.e.t.	varactor bridge	vibrating capacitor
input resistance	10^{14}	10^{12}-10^{14}	10^{16}
input current, I_1	1-10fA	10 fA	1 fA
dI_1/dT	0.1-1fA/^{o}C	1 fA/^{o}C	-
dv_{os}/dT	50-150uV/^{o}C	20 uV/^{o}C	30uV/^{o}C
long-term drift	poor	good	good

Recent developments in i.g.f.e.t. processing technolgy suggest that low-frequency noise performance can be improved by an order of magnitude, and that superior device matching shold be possible, which should reduce offset-voltage drift effects. With the general adoption of guarded-gate devices for electrometer applications, the i.g.f.e.t. input electrometer should become competitive in performance with the vibrating-capacitor and varactor bridge systems. Although gate-protection schemes (which tend to degrade the i.g.f.e.t. input characteristics) are normally necessary, the effects can be mitigated to a large degree.

Even with currently available i.g.f.e.t.s, improvements in low-frequencynoise can be achieved if the devices are

operated under subthreshold conditions. Additional advantages (17) of this type of operation are: a) the bias potentials and hence the gate current are minimised, b) the low drain current makes it feasible for the input stage to be left continuously on, powered by a battery. This avoids the undesirable initial drift effects that occur following switch on.

In terms of cost, it is likely that the i.g.f.e.t input electrometer will remain the simplest and cheapest system. The vibrating capacitor electrometer, involving delicate mechanical mechanisms in the capacitor unit, is likely to remain expensive. For a significantly superior performance, until new developments take place it may be necessary to resort to the use of a passive electrometer.

1.2.7. Circuit implementation;

The conversion of current-to-voltage is determined by the relation $V_s = - R_F I$, where R_F is the feedback resistance of a high-gain and high-input impedance amplifier. For the device implemented, a factor A has been introduced in this relation. Its value depends on the range selected.(18)

The gain of the amplifier in Fig. 17 may be shown to be

$$A = \frac{V_s}{E} = \frac{GB_e}{} \qquad \text{where } B_1 = \frac{R_1}{R_1+R_2} \text{ and } B_e = \frac{R_e}{R_3+R_e},$$

When $B_1 G \gg 1$, the gain will be: $A = \frac{B_e}{B_1}$

On the schematic shown in fig. 18, two switches have been added for the optional selection of resistors R_1 and R_5. In this way four possible values of gain are available.

1. Switch 1 closed, switch 2 open:

$$A_1 = \frac{B_e}{B_1} \qquad \text{where} \qquad B_e = \frac{R_4}{R_3+R_4}$$

2. Switches 1 and 2 open:

$$A_2 = B_e$$

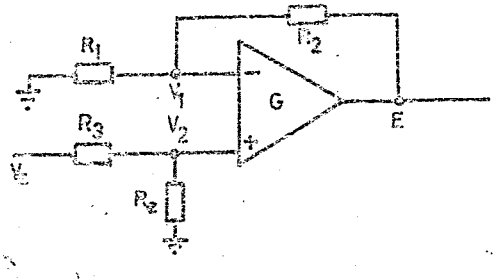

Fig. 17 Operational amplifier using fixed positive-voltage gain.

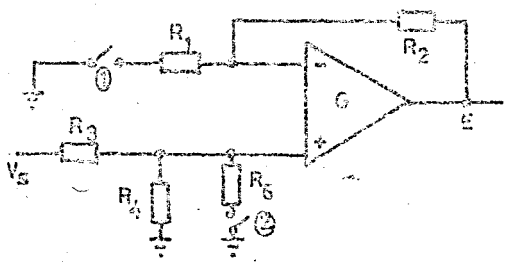

Fig. 18 Voltage amplifier of Fig. 17 with four possible values of gain

3. Switches 1 and 2 closed:

$$A_3 = \frac{B'_e}{B_1} \quad \text{where} \quad B'_e = \frac{R_4 R_5}{R_3 (R_4 + R_5) + R_4 R_5}$$

4. Switch 1 open , switch 2 closed:

$$A_4 = B'_e$$

From these relations, four decades of gain have been established:

$A_1 = 1 \quad B_e = B_1$

$A_2 = 1/10 \quad B_e = 1/10$

$A_3 = 1/100 \quad B'_e = 1/1000$

$A_4 = 1/1000$ verify the above relation.

In order to obtain the above values of gain the relations between the values of the resistors need to be:

$$R_2 = 9 R_1, \quad R_3 = 9 R_4, \quad R_4 = 110 R_5$$

The switches used are analog switches, the off resistance of

which can be considered to be infinite. However, the on resistance is significant and will be considered in the calculations as being in series with R_1 and R_5. From another point of view, the resistors R_1 and R_5 must be greater than the on resistance of the switches, as on resistance changes with temperature.

The resistor values were chosen as follows:

$R_1 = R_5 = 1500\Omega$, $R_4 = 168300\Omega$, $R_3 = 1515\ k$, $R_2 = 13770\Omega$

Fig. 19 shows the complete loop with the commuted gain amplifier which changes the voltage on the feedback resistor R_F.

The current to voltage conversion equation can be shown to be:

$$V_s = - \frac{G}{1 + G\,A} R_F\, I \ , \quad \text{and if } GA \gg 1, \ V_s = - \frac{R_F\, I}{A}$$

As described in the previous section, A takes the values 1, 1/10, 1/100, 1/1000, and the corresponding values of V_s are

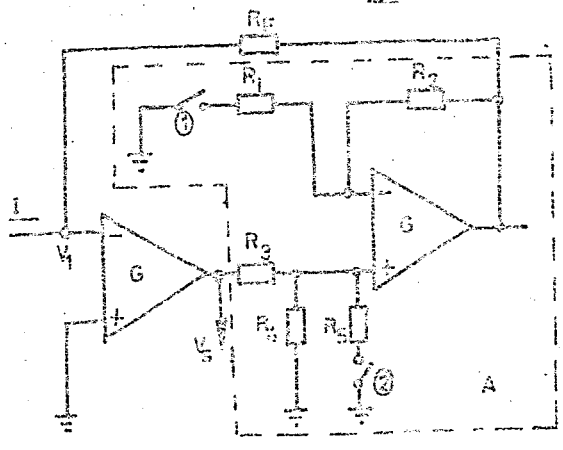

Fig. 19 Complete loop used to make current to voltage conversion in four ranges

$V_{s1} = -R_F I$, $V_{s2} = -10R_F I$, $V_{s3} = -100R_F I$, $V_{s4} = -1000R_F I$.

Thus, an electrometer with four decades has been obtained using only one feedback resistor, and it can detect a current one thousand times smaller than that detectable with the same feedback resistor in the conventional version.

The choice of the operational amplifier is very important. The electrometer operational amplifier of gain G must have very low input leakage current, while the amplifier of gain A must have very low offset voltage.

The feedback resistance used is 10 MΩ and allows current measurement from 10^{-10} A to 10^{-6} A.

The advantage of the automatic range switching is that it has wide dynamic range, and yet retains the high accuracy of a linear sytem. This system comparaed with others, has the foolowing advantages:

1. Better accuracy and smaller thermal drift; this results from an accurate and low-drift $10^7 \Omega$ resistor that is easier to obtain than a $10^{10} \Omega$ resistor;
2. Shorter time constant on higher sensitivities;
3. Mimimal size and weight;
4. Shorter switching time; and
5. Elimination of vibration or oscillation produced by relays.

The method for indicating the range in use at a given

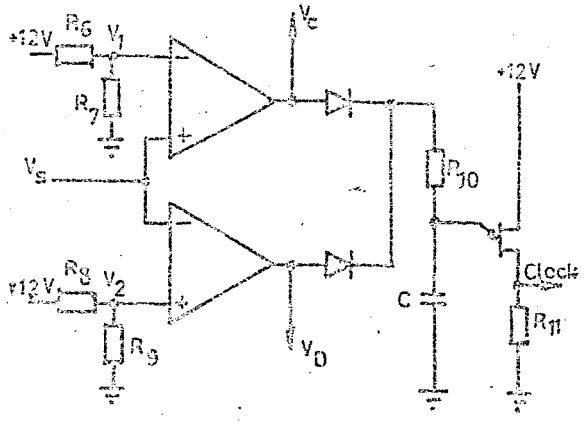

Fig. 20 Circuit providing pulses to logic circuits when signal is over-range or under-range.

time is shown in Fig. 20. Two operational amplifiers, used in on open-loop gain configuration, are employed together with a unijunction transistor which commands the logic circuits. The relationship is : $V_c = G(V_s - V_1)$ and $V_d = G(V_2 - V_s)$.

The amplifier has a large gain ($> 50\,000$) which can be considered to be infinite. (It would be possible to realize the infinite gain by using positive feedback, but it is not necessary in this case.) The sum of voltages V_c and V_d is applied to the unijunction transistor such that

a. If $V_2 < V_s < V_1$, V_c and V_d are at the negative saturation of -12V, the voltage on R_5 is zero and the unijunction transistor is off.

b. If $V_s > V_1$ or $V_s < V_2$, then V_c or V_d is at the positive saturation of +12V, which is applied to R_5, and the unijunction transistor will deliver one or several positive pulses, depending on the range to be selected, with a pulse rate proportional to R_5C.

The thresholds V_1 and V_2 have been chosen as 10.5 V and 0.95 V.

Two flip-flops are necessary to communicate the position required for each of the two switches. The truth table for the flip-flops is shown in Fig. 21a. From this table the two truth tables, increasing the gain and decreasing the gain , have been established in Fig. 21b. The system is locked to the corresponding state so that the gain increases if the input current is small and the gain increases if the input current is high.

These tables allow us to establish the following logic equations:

$$D_A = \bar{A} + \bar{B}C \ , \ D_B = BD\bar{A}, \ R_A = \bar{A}BD \ , \ R_B = \bar{B}C \ .$$

The connections are realised in the way shown in Fig. 22, where switches 1 and 2 are connected to A and B, respectively.

CD 4013

Cl.	D	R	Q	$\bar{Q}$
⌐	0	0	0	1
⌐	1	0	1	0
⌙	X	0	Q	$\bar{Q}$
X	X	1	0	1

a

Range	Switch 1	Switch 2	A	B	C=1 D_A	C=1 D_B	D=0 R_A	D=0 R_B	C=0 D_A	C=0 D_B	D=1 R_A	D=1 R_B
10^{-10}	0	1	0	1	1	1	0	0	X	1	1	0
10^{-9}	1	1	1	1	0	0	0	0	0	1	0	0
10^{-8}	0	0	0	0	1	X	0	1	1	1	0	0
10^{-7}	1	0	1	0	1	X	0	1	0	0	0	0

b

Fig. 21. a) Truth table of flip-flop.(CD 4013)

b) Truth table of logic circuits

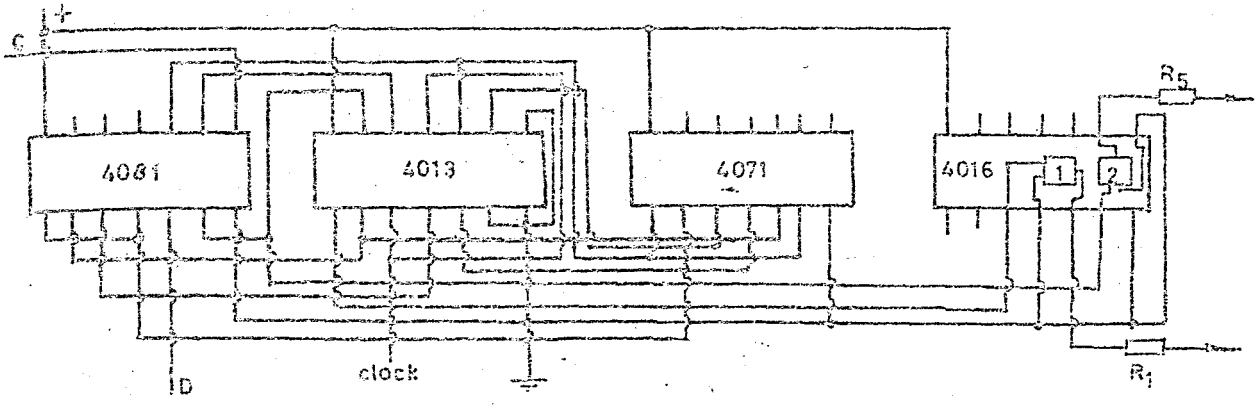

Fig. 22 Logic circuits used to select range

To facilitate the reading of the levels, it is added four indicating signals which consist of the LED s. These indicating signals are controlled by the logic circuit which consists of the NAND and AND gates and its diagram is given in the Fig. 23.

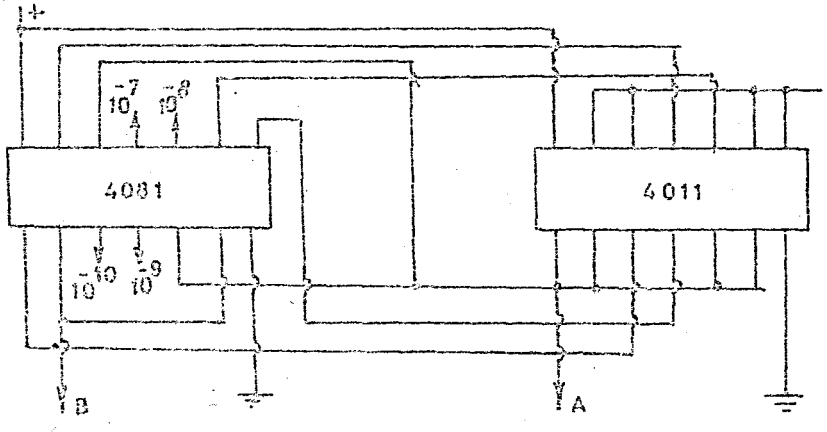

Fig. 23 Logic circuits used to read range.

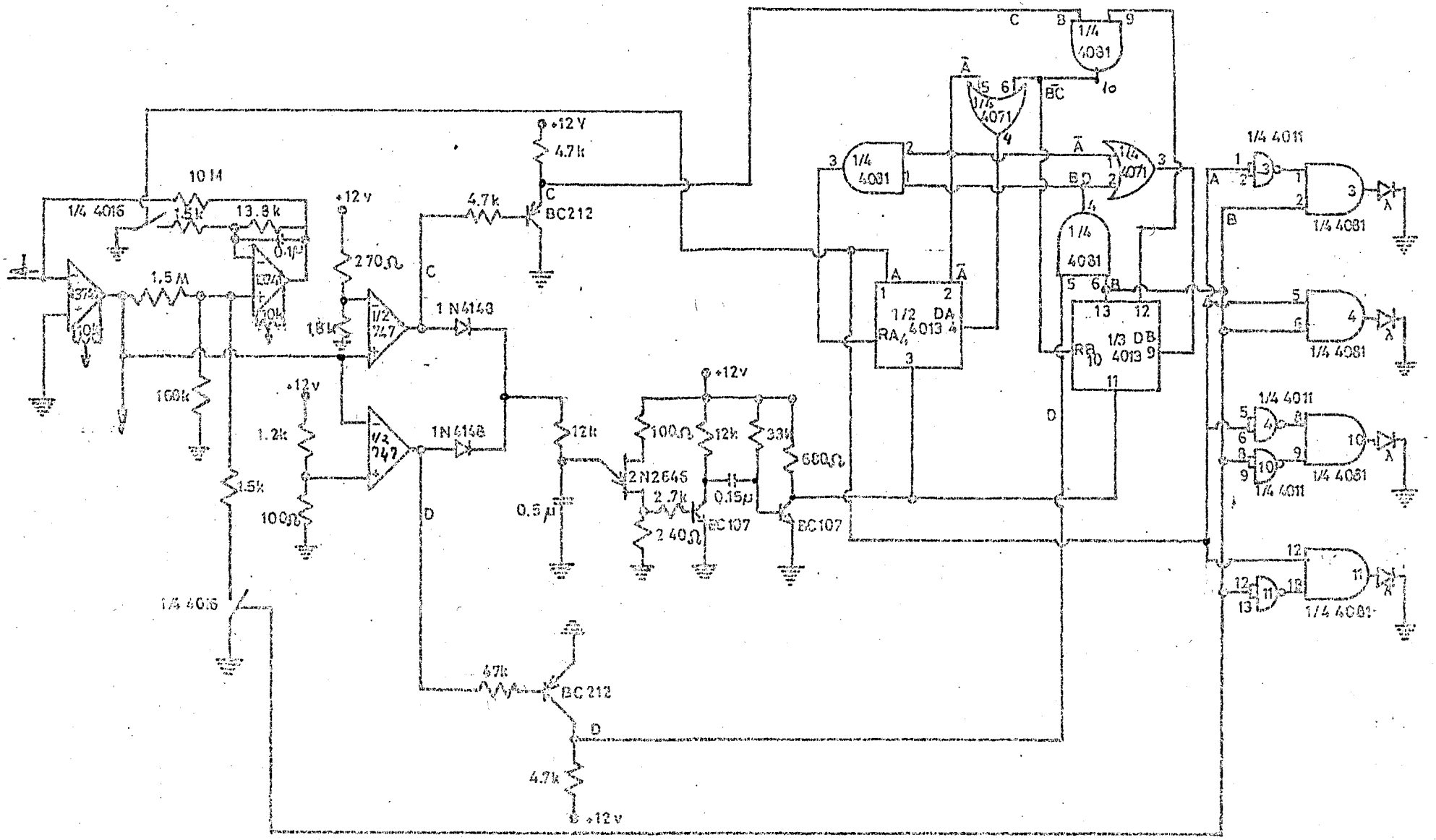

FIG. 24 Complete Circuit Diagram of the Electrometer

CHAPTER II

ELECTRONIC D.C. POWER SUPPLIES

Electronic equipment operates largely on d.c. power. The sources for this encompass many different types, including such prime sources as batteries and generators, as well as electronic converters, whose task it is to convert the output of a prime source to a useful form. We will concern ourselves with converters called the electronic d.c. power supplies designed for the purpose of changing a.c. utility-line electrical power to d.c..

2.1. Elements of an electronic d.c. power supply.

Electronic d.c. power supplies generally consist of the four sections a power transformer, a rectifier, a filter and a regulator.(Fig. 25)

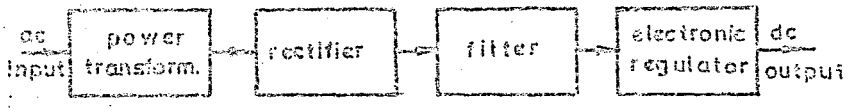

Fig. 25 Elements of a regulated a.c.-d.c. power supply

The power transformer converts the a.c. line voltage into a higher or lower (or sometimes equal) a.c. voltage, depending on the application, and isolates the remainder of the circuitry from the power line. The transformer output is applied to a rectifier, which converts the a.c. voltage into a d.c. voltage. Unfortunately, the conversion from a.c. into d.c. is not perfect, and a certain amount of a.c. residue or 'ripple' remains in the output of the rectifier. The rectifier is usually followed by a filter section, which reduces this residual a.c. component to produce a more nearly pure d.c. voltage. The filtered d.c. voltage is then applied to an electronic feedback or control circuit, called a regulator, which maintains the d.c. output voltage essentially constant for changes in load conditions or variations in line voltage.

Details of transformer, rectifier and filter construction and operation are treated in introductory books.(19,20) Therefore, the regulator details are explained in the following sections.

2.2. Basics of voltage regulation in d.c. supplies

In order to maintain a constant output voltage from a power supply two basic devices are necessary: a measuring unit and a regulating unit. The purpose of the measuring unit is to detect any departure in output voltage (or current, if it is a current stabilizer), from its correct

value. This then feeds a signal to the regulating unit, which makes the necessary correction to the output. The regulating unit may be placed in one of two positions and the measuring unit in one of three positions.(21)

2.2.1. Position of measuring unit

The three positions in which the measuring unit may be placed are as shown in Fig. 26, namely

a) Measuring unit across input

b) " " " output

c) " " in series with the output

In this diagram only one of the two possible positions of the regulating unit is shown. In order to explain the operation of these arrangements a factor called the regulator amplification, M, is introduced, this being given by.

$$M = \frac{\text{Change of voltage across regulating unit}}{\text{Change of voltage across measuring unit}} = \frac{dV_{RU}}{dV_{MU}}$$

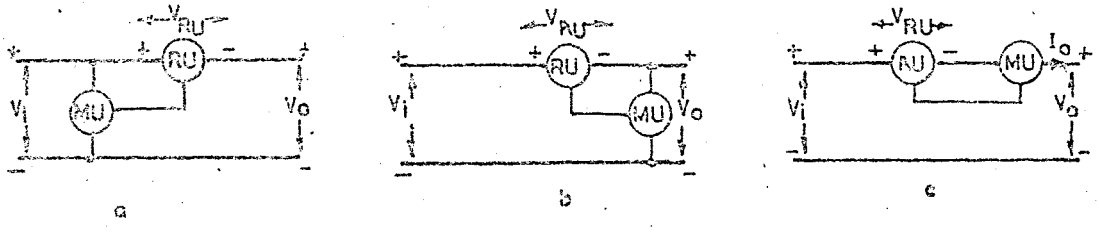

Fig. 26 Positions of measuring unit in voltage regulator
a) Across input b) Across output c) In series with load

2.2.1.1. Measuring unit across input

Consider Fig. 26a, where a change of input voltage dV_i occurs which results in a change of output voltage dV_o. From the circuit,

$$dV_o = dV_i - dV_{RU} \qquad (17)$$

where dV_{RU} is the change of voltage across the regulating unit. From the definition of regulator amplification, M, $dV_{RU} = MdV_{MU}$, and substituting in eqn.(17),

$$dV_o = dV_i - MdV_{MU}$$

But $dV_{MU} = dV_i$, since the measuring unit is connected across the input. Thus

$$dV_o = dV_i - MdV \quad \text{or} \quad \frac{dV_o}{dV_i} = 1 - M \qquad (18)$$

where $\frac{dV_o}{dV_i}$ is the regulation factor, R_f.

If M is made equal to unity then the regulation factor becomes zero and the output voltage is independent of changes of input voltage.

Although this may sound ideal the arrangement suffers from two disadvantages:

a) If R_f is to be zero then M must be exactly unity. If M changes by 10 per cent to 0.9 then R_f becomes 1-0.9=0.1 and the performance is poor. For ideal operation M must be exactly unity and must not vary with ambient temperature, ageing, etc.

It is impossible to satisfy this condition in practice.

b) Changes in load current will cause changes in output voltage since regulating unit will have some internal resistance. Since changes of current do not influence the measuring unit, no correction is made for load changes.

For these reasons this arrangement is rarely used. It is in fact an open loop control system.

2.2.1.2. Measuring unit across output

Consider the circuit of Fig. 26b. As previously,

$dV_o = dV_i - dV_{RU}$ and $dV_{RU} = MdV_{MU}$

but now the measuring unit is across the output, and hence

$dV_{MU} = dV_o$, Thus

$dV_o = dV_i - MdV_{MU} = dV_i - MdV_o$ or

$$\frac{dV_o}{dV_i} = \frac{1}{1 + M} \qquad (19)$$

The regulation factor is now made small by making M large, but it can not be made zero without making M infinite. In spite of this disadvantage the regulation factor is not critically dependent on M as in the last case. For example suppose M = 500. Then

$R_f = 1/(1+500) = 0.002$

Now suppose M changes by 10 per cent to 450; then

$$R_f = 1/(1+450) = 0.0022$$

and the stabilization is almost as good as previously.

This arrangement is really a negative feedback closed loop amplifier and that M is the loop gain.

2.2.1.3. Measuring unit in series with output

For the arrangement of Fig. 26c the definition of M has to be modified since the measuring unit is detecting changes of current and not voltage. Thus

$$M = \frac{\text{Change of voltage across regulating unit}}{\text{Change of current in measuring unit.}} = \frac{dV_{RU}}{dI_o}$$

The circuit has been redrawn in Fig. 27, where a resistance R has been added to represent the internal resistance of the regulating unit.

$$dV_o = dV_i - dI_o R + dV_{RU}$$

If the input voltage V_i is assumed constant, then

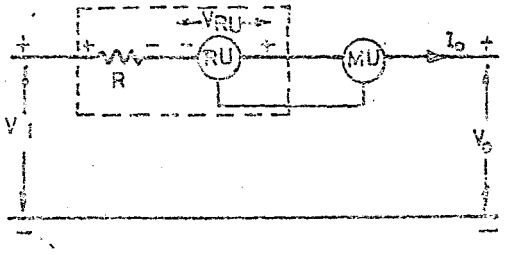

Fig. 27 Effect of measuring unit in series with load

$$dV_o = -dI_o R + dV_{RU}$$

But $dV_{RU} = MdI_o$; hence

$$dV_o = -dI_o R + MdI_o \qquad \text{or} \qquad -\frac{dV_o}{dI_o} = M - R$$

The effective internal resistance is

$$R_i = -\frac{dV_o}{dI_o}$$

the minus sign being required because an increase of I_o results in a decrease in V_o. Hence

$$R_i = R - M \tag{20}$$

Thus if M is made equal to R then the internal resistance $R_i = 0$. The arrangement has similar disadvantages to the circuit of Fig. 26a but may be used in conjunction with the circuit of Fig. 26b.

2.2.1.4. Measuring units across output and in series with load

In a similar way, if the circuits of Figs. 26 b and c are combined, the internal resistance is given by

$$R_i = \frac{R - M_s}{1 + M_o} \tag{21}$$

where M_s = Regulator amplification of measuring unit in series with output

M_o = Regulator amplification of measuring unit across output

Again any error due to M_s not being equal to R is divided

by the factor $1 + M_o$, and if $1 + M_o$ is large, good performance is obtained for change of output voltage due to change of current.

2.2.2. Position of Regulating unit

The two possible positions of the regulating unit are given in Fig 28, only one possible position of the measuring unit being shown. At (a) the regulating unit is in series with the load (series regulator systems), while at (b) it is in parallel with load together with a series resistor R_s (shunt regulator systems). In both these cases the regulating unit will dissipate the excess power. In (a) the power in the regulating unit is $(V_i - V_o)I_o$ and is a maximum under conditions of maximum load current (other factors being constant). Provided that the output voltage is not much less than the input voltage, the power to be dissipated in the regulating unit can be much less than the output power of the stabilizer.

Fig. 28 Positions of regulating unit

a) In series with load

b) Across output together with series resistor R_s.

Consider an example of a 50V,1A supply where the input voltage is 60V ∓ 10 per cent. The maximum dissipation occurs when the input voltage is a maximum, i.e. 66V, and the current is a maximum. It is then (66 - 50)x1 = 16W, whereas the output power is 50x1 = 50W.

In Fig. 28b the output voltage is maintained constant by varying the current through the regulating unit. If the input voltage increases then the current in the regulating unit must increase, so that the increase in voltage drop across the series resistor R_s just equals the increase in input voltage. If the load current changes, the current in the regulating unit must change by the same amount so that the current in R_s and the drop across it remain constant.

If the same power supply is considered but with a nominal input voltage of 75V then the normal drop across R_s is 25V. When the input voltage is a minimum, i.e. 75-7.5=67.5V (75V - 10per cent), the drop across R_s is 17.5V. The resistance R_s is therefore 17.5 assuming under these conditions that the load is 1A and that no current flows in the regulating unit. When the input voltage is a maximum, i.e. 75+7.5= 82.5V, the drop across R_s is 32.5V. For the same output voltage the current in R_s must now be 32.5/17.5 = 1.86A, and assuming the same load current, the current in the regulating unit is 0.86A. Thus if the load were constant at 1A the regulating unit would have to dissipate 0.86x50 = 43 W at maximum input voltage and nothing at minimum input voltage. Under the conditions of maximum input voltage and zero

load current (the worst conditions as regards the regulating unit) the current in R_s must still be 1.86A, and all this current must be passed by the regulating unit.

The maximum regulating unit dissipation is therefore 1.86x50 = 93W. Thus is greater than the maximum output power (50W) and much greater than that calculated for the case of the regulating unit in series with the load (16W). Obviously the exact figures will depend on the voltages used, but for Fig.28b the dissipation of the regulating unit must be greater than that of the load if the stabilizer is to operate down to zero load. It is important to note that in this arrangement the maximum dissipation in the regulating unit occurs at no load, whereas it is a maximum for Fig 28a under conditions of maximum load. Circuit (b) has the advantage that a short-circuit of the load does not overload the regulating unit, whereas in circuit (a) a short-circuit of the load causes full voltage to be applied to the regulating unit with a current equal to the short circuit current. Since the dissipation of the regulating unit (for a given output) is less in circuit (a) than in circuit (b), circuit (a) is more commonly used, but circuit (b) is sometimes used for low powers.

2.3. Linear and switched d.c. voltage regulators

D.C. voltage regulators can be classified as linear or switched.(22) In linear regulators which were discussed in

above sections, the regulating unit(seris or shunt) elements continuously dissipate some power in keeping the output voltage constant under varying input voltage and output load conditons.

The switching regulator gets round the low efficiency of the linear regulator by using controlled on-off switching of the power supplied to the load to keep the output voltage constent.

In series form of the switching regulator illustrated in Fig. 29a, the series on-off switching control element, A, (series regulating unit) inserted between the supply input and output is switched on and off by a controlled on-off duty-cycle switch circuit X. As a result, current from the input is released in pulses, which after smoothing, provide a controlled d.c. voltage output level. The switching duty cycle of X adjusts itself so that the mean output voltage remains constant irrespective of input voltage or load current variations.

The same principle of rapid on-off 'chopping' of the

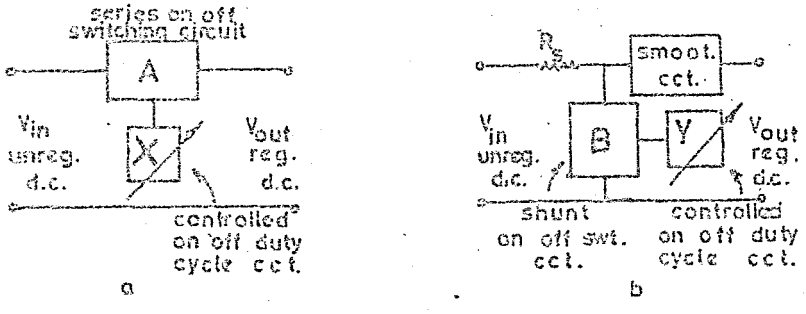

Fig. 29 Principles of switching regulators

a) switching series b) switching shunt

supply also appears in the shunt form of switching regulator shown in Fig. 29b. Here the controlled on-off duty cycle switching oscillator Y switches on and off the shunt switching circit B(shunt regulating unit) to bleed off current from the supply away from theload. Once again the chopped d.c. is smoothed and fed to the load. The duty cycle control of Y is such that the output voltage is held constant under varying input voltages and load currents.

Switching regulators can be more compact then equivalent linear ones because of the high efficiency of the switching mode. This efficiency has to be paid for in greater circuit complexity and in difficulties with r.f. (radio frequency) interference suppression.

2.4. Overload protection circuits in d.c. voltage regulators

Because voltage-regulated d.c. supply circuits depart from simple robust rectifiers into the area of more sophisticated, and thus more easily damaged, devices, protective circuits play a large part in the design of d.c. voltage regulators. Fig. 30 shows various point at which over-load protection circuits may commonly be found in a regulated d.c. supply system.

Protecting the basic voltage regulator, A in Fig. 30, against overload and fault conditions calls first of all

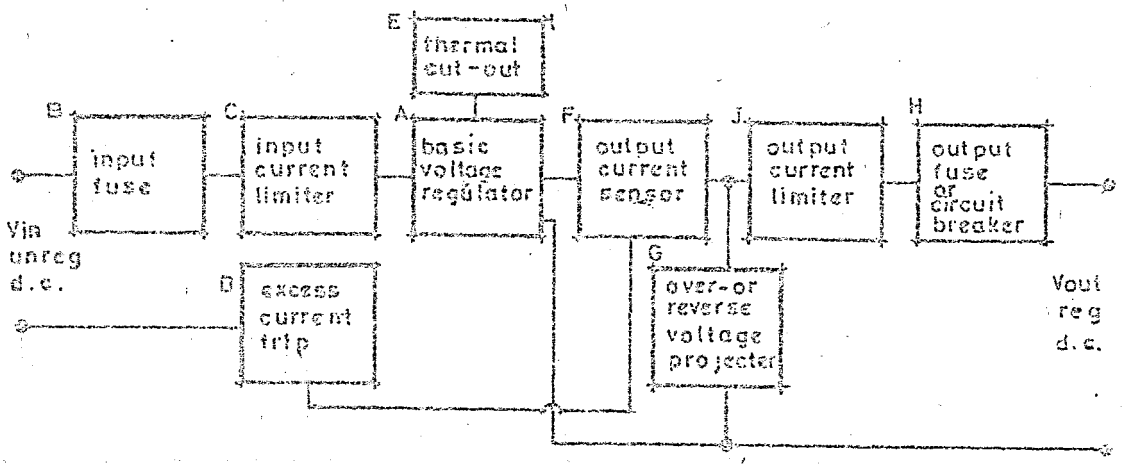

Fig. 30 Overload protection circuits

for adequate fusing, both on the input, as at B, and on the output, as at H, where a circuit-breaker is sometimes used.

A very common protective circuit is the input current limiter, C in Fig. 30, which can take as simple a form as a wirewound power resistor. Current limiting at the output, as at J in the diagram, is often used also. Frequently also some form of 'trip', as at D, is used, which switches the supply to a safety condition(off or low current only) when the load current, as sensed by F, exceeds a predetermined safety limit. Thermal cut-out, E, cuts off the supply when excess heat appears inside the equipment case, and the over- or reverse-voltage protector at G, prevents voltages of the wrong polarity, or above a predetermined level.

2.5. High voltage feedback-regulated d.c. supplies

The high voltages raise difficulties of their own. A shunt transistor in a d.c. regulator has to withstand the

full output rail voltage (often with a high resistance between base and emitter, under which condition a transistor has the lowest voltage rating). On the other hand, a series pass transistor has to withstand the difference between the unregulated input and the regulated output, which can be large in high-voltage power packs.

By careful control of input voltage range, the voltage drop across a series-pass transistor can be fairly limited easily. For this reason the most practical examples of high-voltage d.c. regulators are designed as series type. When it gets up into several hundred volts output, the costly special high-voltage transistors or some method of spreading the voltage in steps across a number of lower voltage units by stacking them in such a way that the voltage across each transistor is limited must be used.

Fig. 31(a) illustrates this in a linear series regulator. Transistors, $Q_1, Q_2, \ldots, Q_N$ are arranged in a series string with collector-to-emitter bias resistors of a suitable value to spread the high-voltage out across the individual transistors. Usually the voltage is divided equally by using a single value of resistance for R1, R2, etc. The design value of the resistor for the string is worked out on the basis of a resistance low enough so that a full output current, the base current demand of the transistors does not substantially alter the voltage drop between transistors. A useful rule of thumb is to bleed down the resistor chain

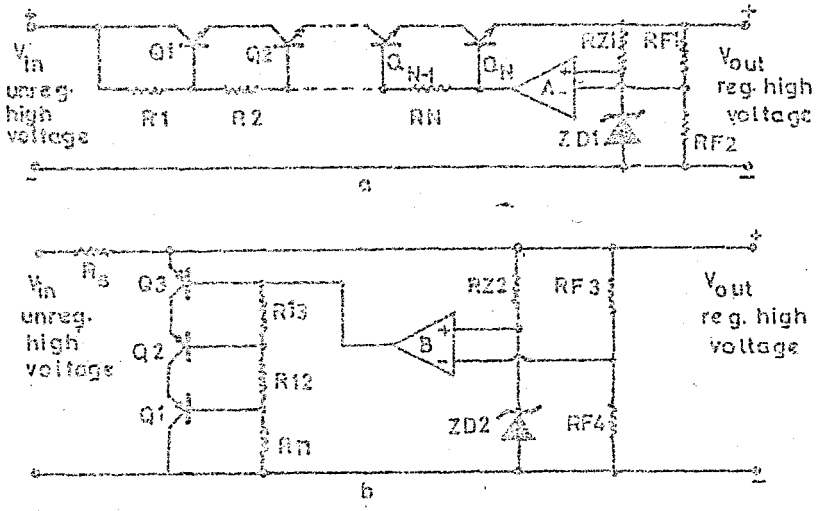

Fig. 31 Totem pole stacked composite high voltage transistors in high voltage linear feedbackd.c. regulators
a) Series b) shunt

a bias current of one-tenth of the full output current, on the basis that most modern transistors have a minimum current gain of 25, and a bias current means that at full output current the transistors will take not more than one-quarter of the available resistor bias current. As they will all be taking roughly equal base current, the voltages across the transistors will remain fairly constant.

The comparator feedback and drive is not shown in detail in Fig. 31a, but is merely indicated by output sample and reference voltage circuit feeding a comparator and phase-inverting driver amplifier, A.

An series-regulated supplies, under normal working, the series-pass element sees only the voltage difference between the input and output rails. This means, under normal working, a relatively small voltage drop. Of course, if the output

is short-circuited accidentally, the series transistor sees the full input rail voltage. This is why, in series regulators, the quite elaborate protection circuits to prevent this, will be very often found. Of cource, with the availability of suitable high-voltage transistors, the circuit can easily be designed to tolerate direct output short-circuit.

With shunt supplies, on the other hand, the shunt control element always sees the full output rail voltage, and this means that a suitable highly voltage-rated transistor must be used, or recourse made to a stacking of transistors to divide the voltage over a number of lower-voltage devices. Fig. 31b shows the approach that can be adopted for shunt regulation. Once again, the bases of the string of shunt transistors are clamped to lower voltage steps along a base bias chain indicated by R11, R12, R13 for three devices (although, of cource, any number of elements could be used).

The values of the bias resistors should be chosen to provide a resistor chain current of about one-tenth of the full shunt current designed for.

2.6. Circuit implementation

In this work, a high voltage d.c. power supply with high stability for a 9 dynode photomultiplier is proposed, which is in the form of series linear voltage regulator.

In this circuit, because the error signal is transmitted by an optical coupler to the control transistors in a high voltage circuit, high dielectric breakdown voltage is not required for most of the elements, and therefore the circuit becomes simplified and less expensive to build.

The built up circuit is shown in Fig. 33. Unregulated high voltage produced by two voltage doublers is connected to the output terminal to give a stabilized voltage V_o after passing through two control transistors Q_1 and Q_2 and a current detector. The output voltage is reduced by a resistive divider and compared with reference voltage that is realized by zener diode at the input of the op-amp. The voltage difference is then amplified by op-amp and is fed as an error signal to the optical coupler which is connected the bases of the series control transistors.

If the output voltage V_o increases beyond the initial setting voltage, an error signal from the error detect amplifier and current flowing through the optical coupler increases, the base current decreases and finally equivalent collector emitter resistance increases. As a result, the output voltage devreases to return to the original setting value and vice versa for the devrease of the output voltage.

In series regulator circuits the current which is fed to the junctions between the optical coupler (The comparator output) and the base of the control transistor must be stable. This one is provided by the circuit

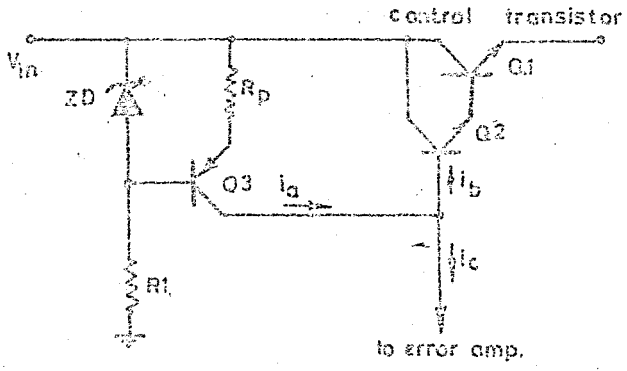

Fig. 32 Preregulator providing the base current of the control transistor

diagram shown in Fig. 32. In this circuit, the current through R1 is fixed by the constant voltage $V_Z - V_{EB}$ appearing across the resistor, and this current should be at least twice the maximum value of the base current, I_B.(23)

An accidental short circuit across the output of a regulator may destroy the control transistor(s). Fuse or circuit breakers are usually not fast-acting enough. Therefore to protect the control transistors(s) some form of current limiting is needed.(24)

A small resistance R inserted between the control transistor and load restricts the load current. Its value is selected to give a suitable voltage drop when the current approaches the maximum to be tolerated. For currents up to the level, op-amp is negative saturation and R has very little effect. When the load current exceeds a predetermined value, e.g. 10 mA in this circuit, op-amp turns positive, drawing current away from the base of the control transistor by the optical-coupler. Regulation is no longer (in the determined limits) effective and the output voltage drops.

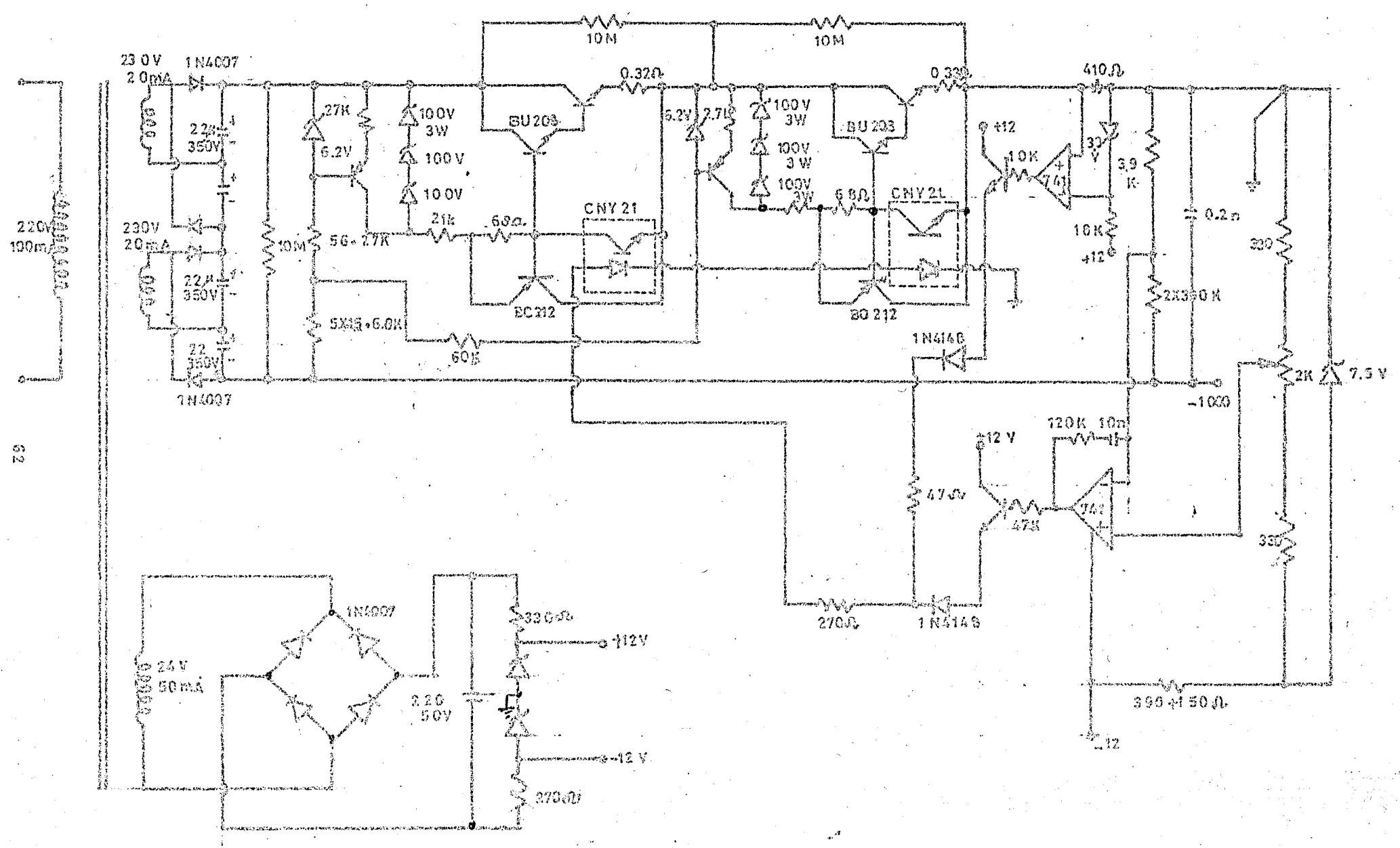

Fig. 33 Complete circuit diagram of photomultiplier power supply

CHAPTER III

I N V E R T E R S

It is often necessary to operate 220V AC equipment in an area where the mains supply is unavailable. This may include for example, electric hand tools, measurements in the field with laboratory equipment, or perhaps domestic appliances.

There are two alternatives: either an engine-driven alternator, or an inverter operating from a storage battery. If a large power output is required, an engine driven alternator is the obvious choice. But if energy requirements are relatively low an inverter has the advantages of quietness, efficiency, and the possibility of exact frequency control.

An inverter accepts d.c. and provides a.c. It can be designed in many configurations, but to be of any value an inverter must be efficient. Thus when d.c. is switched to produce a.c. the switches must be near ideal. Two semiconductors fall into this category, the transistor and the thyristor. The transistor can be switched on and off, that

is, from a conducting state to a non-conducting state, easily and at will. In the case of the thyristor, this can be easily switched on but switch off requires more complex circuitry, although the thyristor has greater power handling capacity than the transistor.

3.1. Transistor inverters

A transistor inverter can be either self-oscillating or driven. However, the low-cost and relative compactness of a self-excited inverter are outweighed by two disadvantages: frequency and output voltage are notoriously variable with changes in supply voltage and load. In addition, the transformer used in a self-excited invereter has to meet tight specifications on leakage inductance, mutual inductance, and winding resistance if the operating frequency is to stay within the design limits.

In a driven inverter on the other hand, these problems are eliminated. The output voltage can be controlled by pulse width modulation and if it is necessary to control the frequency precisely, then this can be done using a crystal oscillator. It is the drive circuitry which determines the characteristics of the driven inverter; the transformer is merely used for voltage conversion so its specifications are not critical.

For all these reasons, the driven transistor inverters are considered in the later sections.

Figures 34 to 37 show the basic circuits of most common ones of the driven transistor inverters. Fig. 34 shows the simplest transistor inverter; as can be seen, the transistor is used to switch the supply across the output transformer, thus a voltage of nV_s is impressed on the secondary. The mean output voltage can be controlled by varying the ratio of on to off time of the transistor, and hence, into some loads, the output power. The main drawback of the circuit is that the unidirectional current polarizes the transformer. Since each pulse applied to it is of the same polarity, it will saturate unless recovery is permitted. For the transformer to recover, its magnetizing current must be allowed to return to the starting point every cycle. This requires that the voltage across it must reverse, i.e. the transistor collector will become more positive than V_s. Furthermore, if the on time of the transistor has been t_1 then, since the flux swing in the transformer is proportional to $\int v dt$, it is also proportional to $V_s x t_1$ and as this must return to zero a reverse swing of this magnitude is required. Thus, if the on time and the off time are required to be equal, then a reverse amplitude of V_s is necessary and the transis-

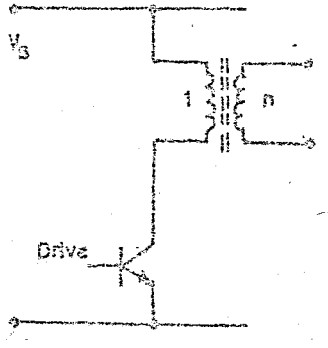

Fig. 34 Simple transistor inverter.

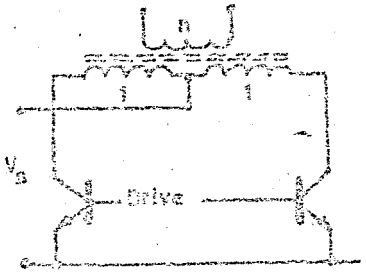

Fig. 35 Push-pull inverter

tor collector reaches $2V_s$. The result of this problem is that the operating power is limited, as a transistor capable of withstanding twice the supply voltage in its open circuit condition and current, is only switched for half the time.(25)

The circuit shown in Fig. 35 and known as a push-pull inverter is the logical extension of Fig. 34 ; a second transistor is added to form a push-pull arrangement.This gives two improvements, firstly current can now be switched during the whole cycle of operation, that is , in each transistor for half the time. This results in the second improvement which is that the transformer has bidirectional current. At least the major effects of saturation are overcome, but errors in switching characteristics can still result in some saturation difficulties. Although it has been stated that the full time can be utilised, this is not necessary and pulse duration modulation can be used as a control feature. As with Fig. 34, the voltage impressed on the transistors is double the supply voltage but this is only true for an ideal transformer, for any imperfections will result in rings taking the voltage higher.

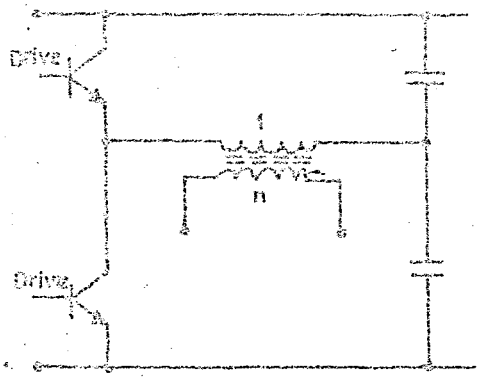

Fig. 36 Half-bridge inverter

Fig. 36 shows a non-symmetrical push-pull inverter, usually called a half-bridge inverter in which a point at $V_s/2$ is provided, usually by capacitive division from V_s. In this circuit, since one side of the transformer is fed by capacitors, no d.c. polarising current is possible and saturation is avoided. A further significant difference to the circuit of Fig. 35 is that the transistor voltage does not exceed V_s so if the same transistors were used the supply railcould be doubled without damage. This, unfortunately, does not mean greater power, as only half the supply is placed across the transformer, but greater freedom in supply rail choice is given.

An extension of Fig. 36 is shown in Fig. 37. This is the full bridge inverter in which the capacitors are replaced by two more transistors which are, in this arrangement, switched diagonally. The full supply voltage is placed on the transformer in alternating directions and the power is hus doubled. The advantage of transistor voltage not exceeding V_s is still effective, but lack of balance in

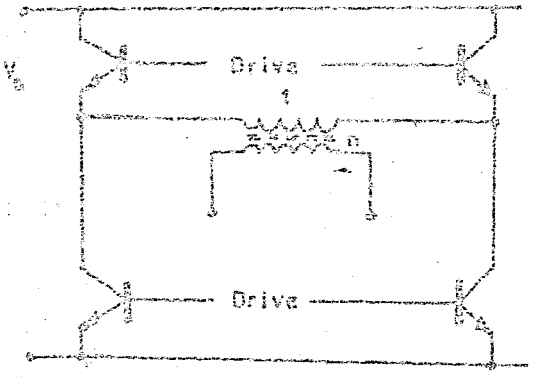

Fig. 37 Full-bridge inverter

the circuit can result in transformer polarising.

3.2 Thyristor inverters

The major reason for using thyristor inverters is their high-power capability and they are not usually used at at power levels obtainable with transistors.

In these inverter circuits, the pole changes required to turn out an a.c.voltage is performed by means of thyristors. In order that a thyristor may be used as a switch, it must be quenched at suitable instants determined by the frequency stipulated. Energy required for quenching is usually stored in capacitors (commutating capacitors). Quenching is performed by commutating circuits making use of of the energy stered.(26)

The basic connections are presented in Figs. 38 and 39. These connections involve commutating capacitor(s) C_c

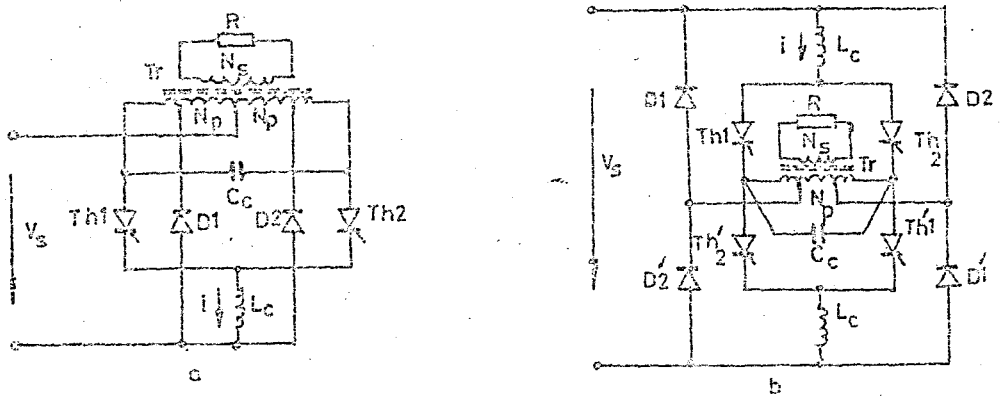

Fig. 38 Single-phase parallel quenched inverter.

a) Simple parallel quenched inverter

b) Bridge " " "

ensuring the quenching of the conducting thyristors, and (a) commutating inductance L_c ensuring the correct operation of the quenching circuit. This latter may be either of the coupled or of the uncoupled type. The quenching-circuit arrangement may be parallel-type (with the capacitor storing the quenching charge connected in parallel with the controllable element), or series-type (with the quenching

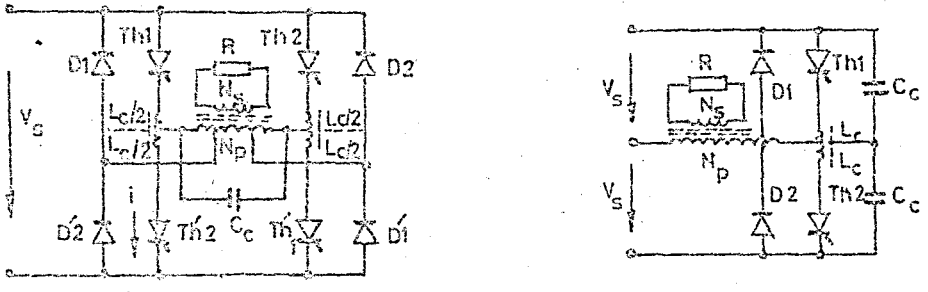

Fig. 39 Single-phase series quenched inverter

a) With single quenching capacitor

b) " two " "

capacitor connected in series at the time of commutation). Connections 38 feature parallel quenching, 39 feature series quenching.

Inverter connections usually incorporate feedback diodes ensure the operation of the inverter at no-load or under an inductance-type load by making possible the reverse flow of power between the inverter and the d.c. supply source. (27)

3.3. Circuit implementation

In this work a driven type of transistor inverter is built up which basically consists of a push-pull arrangement. Here the power amplifiers are driven by a crystal controlled oscillator and therefore the frequency is precisely fixed at 50 Hz. The output voltage is controlled by the pulse width modulation.

A conventional crystal oscillator CD 4017 decade dividers. The crystal frequency is 10 MHz so the resultant frequency is 100 Hz. This is then fed to a CD 4027 bistable wired in the divide-by-two bode to give two antiphase outputs. These outputs are fed via NAND gates to drivers consisting of two series-connected darlington pairs. The NAND gates are capacitively coupled to the drivers to prevent one driver conducting should the oscillator fail.

Three output transistors are used for each phase. These ensure adequate gain, the typical gain of a 2N5772 being 20 at 10A, and 10 at 20A. The use of the transistors also reduces the saturation voltage since the current in each transistor is divided. The saturation voltage when using one transistor is 2V. When the other transistors is connected, the saturation voltage drops to 0.9 V.

The ideal way of ensuring that three paralleled transistors take on equal current is to use emitter resistors chosen so that the voltage across each resistor is of the order of 0.5 V. This applies negative current feedback which reduces gain and saturation voltage variations between the three transistors. However, this is rather wasteful of energy when large currents are involved. To avoid this, base resistors R14, R15 and R16 along with R17, R18 and R19 were used to equalise transistor collector currents. Current sharing using this method has proved to be quite satisfactory.

Diodes D1 and D2 conduct the reactive current after their opposite transistor pairs have ceased conduction. The current pulse they have to pass is of the order of 30 A when the power factor is 0.2. However the conduction period is short and diode specifications indicate that a 2.5 A rating is sufficient.

The 100 Hz square wave is picked off the input of the CD 4027 and differentiated by C1 and C2 with R3 and R5

before being fed to the inputs of each phase driver. This slows the switching times of the drivers and therefore reduces the maximum possible pulse width of each phase to slightly less than 180°, ensuring that under conditions of maximum power transfer, the current in one branch begin to conduct. It also slows the switching time from 10 μs to 60 μs. At full power this results in a switching loss at only 0.6 W which is negligible.

The power output of the inverter is determined by the pulse width of the signal fed to the driver stages. This is controlled by error voltages derived from both the output voltage and current. A sample of the output voltage is obtained from secondary winding S1. This voltage is rectified by the full wave bridge D3, filtered, and applied to the inverting input of op-amp IC4(a) via the output voltage control potentiometer VR1. The resulting DC voltage is compared in the amplifier with a 5.6V reference from D5 to yield a voltage error signal.

To obtain a current error signal the supply current to the output transistors is passed through R20 to develop a voltage proportional to current. This is averaged and compared with a reference derived from diode D4, which is pre-regulated by D5.

Op-amp IC4(b), which amplifies the current error signal, has a lorge feedback capacitor to ensure stabilitly when

the inverter is in the current limited mode. The amplifier has, in this configuration, a large dc gain equal to the open loop gain of the amplifier-about 100 dB- and an ac gain of almost unity.

The outputs of IC4(a) and IC4(b) are fed via a diode OR gate to the inverting input of IC4(d). A delay circuit, consisting of R43, R42, and C12, controls the rate of change of voltage on this input. This is necessary bacuse the long time constant of the voltage sensing circuit would otherwise cause the output voltage to overshoot when the unit was switched on. R42 is included to allow a small rapid change to be made to the output voltage. IC4(d) is wired as a comparator.

The dc error signal applied to the inverting input is compared with a 100 Hz triangular wave fed to the non-inverting input. The triangular wave is generated by IC4(c), which integrates the 100 Hs square wave obtained from the CD 4027 input.

The result of the comparison in IC4(d) is a pulse-width modulated 100 Hz square wave. This signal is fed via an inverter to the NAND gates of each phase of the 50 Hz drive, the phasing being such that the off-time of each phase is proportional to the error signal. (Fig. 40)

A National LM 324 quad op-amp is specified for IC4. This

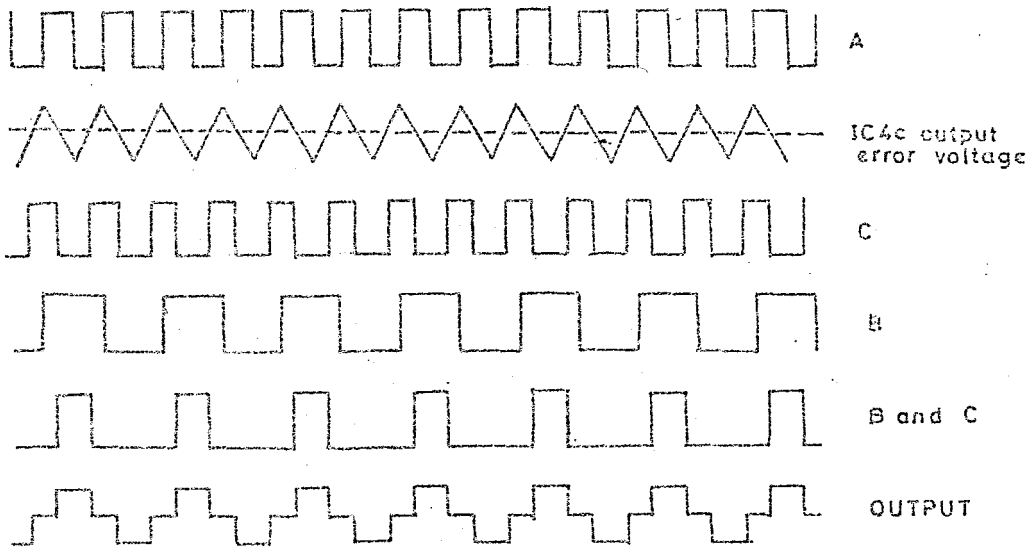

Fig. 40 The formation of the various waveforms

was chosen because, for the current error amplifier, the inputs are almost at zero volts. The LM 324 can be kept in the linear mode, even when the inputs are at ground potential.

The outputs of the error amplifiers are fed to discrete lamp drivers to indicate the running mode. Lamps were chosen because LEDs are difficult to see outdoors or under strong lights. The lamp driver transistors Q15 and Q16 each have a parallel resistor to keep a small current flowing through the lamp. This keeps the flament just less than red and its resistance somewhat greater than its value when cold. In addition, series resistors, R32 and R37, are used to ease the load on the BC 337 drivers, thus enhancing their reliability.

The current sensing resistor consists of about 100 mm

of 60 A fuse wire mounted on either a component board or between two tag-strips. This wire has a diameter of 1.3 mm but any copper wire with a diameter between 1 mm and 2 mm would be satisfactory.

Thermal overload sensing and protection is provided by NTC and SCR1.

The output transistors are mounted on 30 cm of extruded aluminium heat-sink. Although the heatsinking requirements are quite small in the normal operating mode, all the power is dissipated in the output transistors when the output is shorted, so an appropriate heatsink is required. NTC is thermally connected to one of the output transistors.

The transformer may have a specification similar to a mains transformer and can be specified by the VA rating and the turns ratio.

Suggested windings are;

Primary	10.5 - 0 - 10.5 V
Secondaries	12V, 0.1 A ; 220V, 1.5 A
Rating	300 VA

Ten-turn trimming potentiometers are used as they allow setting of the voltage and current limits.

The complete circuit diagram is shown in Fig. 41.

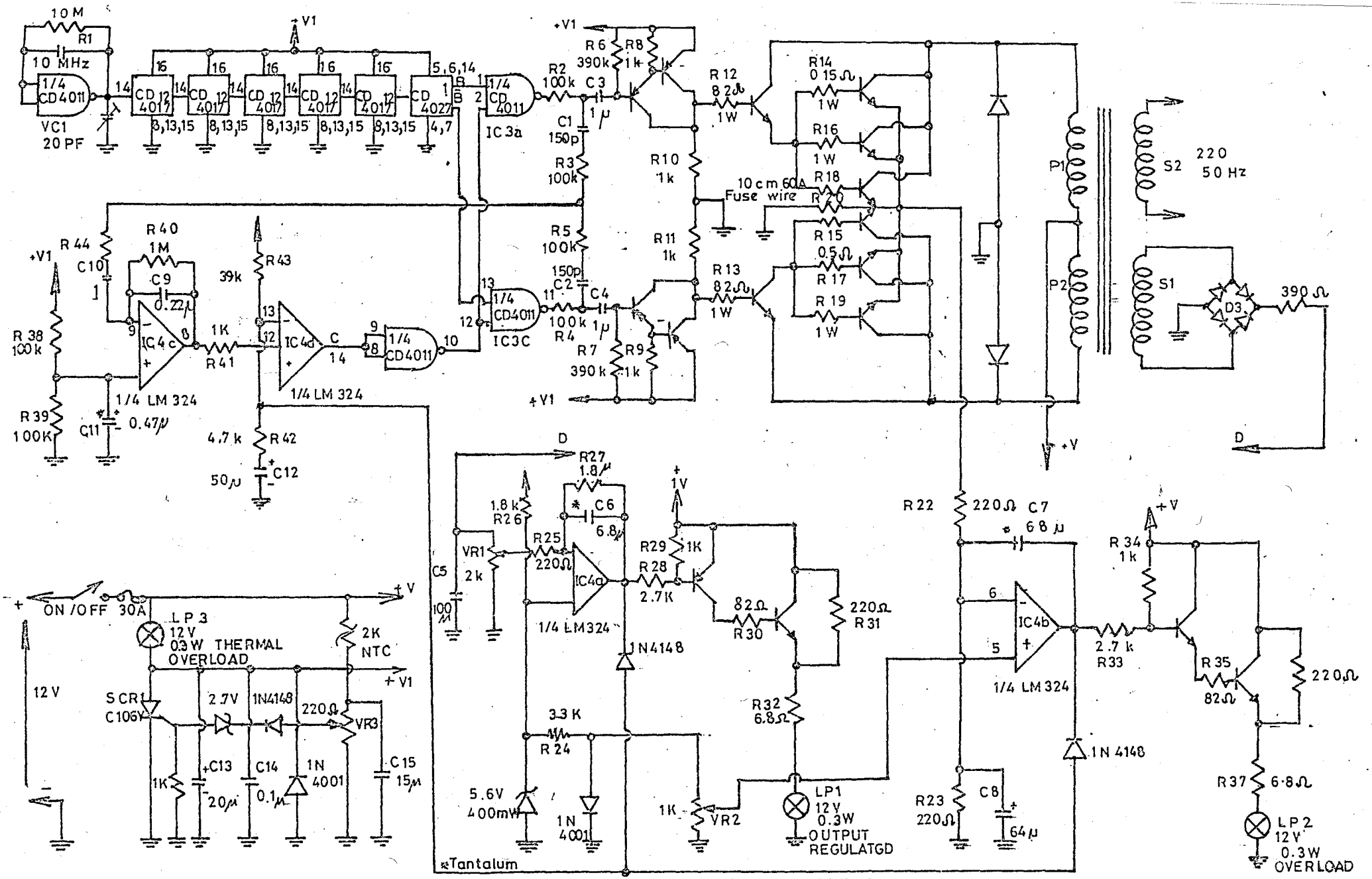

FIG. 41 Complete circuit diagram of the 12 – 220 V Inverter.

CHAPTER IV

PHOTOMULTIPLIER TUBES

The photomultiplier tube (PMT) is a common device for converting light (usually star light) energy to current through a process of photo emission. Unlike the simple phototube or photodiode, the PMT amplifies the current produced by photoemission making it far more sensitive than the simpler devices. Gains of up to 1 million are commonplace.

4.1. Photomultiplier structure

The photomultiplier tube consists of a light-sensitive cathode which emits electrons in proportion to the photons striking it. The electrons are then accelerated to a next stage where they impinge and cause emmission of 3-6 secondary electrons per primary electron. The process is continued throigh 6 to 14 stage (called 'dynodes') depending on the tube type.

Electrons are accelerated by making each successive

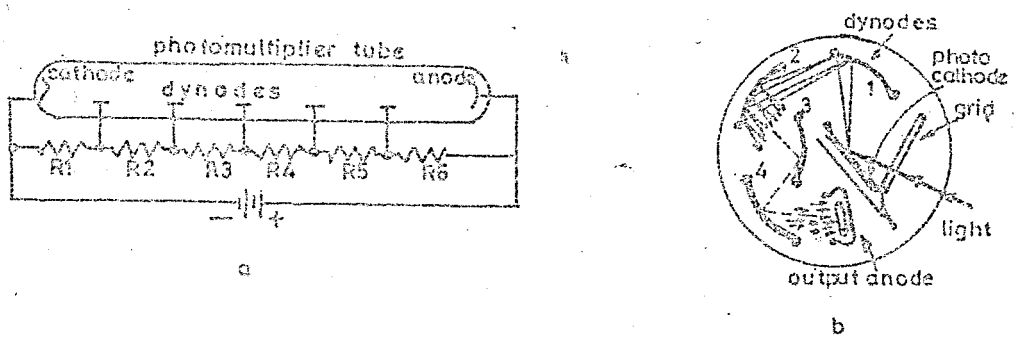

Fig. 42 Photomultiplier tube structure

a) Schematic diagram b) Cross section diagram

stage (dynode) of the tube more positive with respect to the previous one. This is most easily accomplished by applying a potential across the entire tube and tapping the dynode voltages off a voltage divider as shown in Fig. 42. (28)

The voltages that should be applied to each dynode are a function of PMT design and are specifed for each tube type.

The total resistance of the dynode resistors (also known as the 'dynode string') should be such that the current flowing through the series resistance is at least 100 times the expected anode current of thetube.

Most photomultiplier tubes require anode to cathode potentials of between 1000 and 3000 volts. Since the anode is the read-out point, it is usually advantageous to operate the anode at near ground potential and the cathode at high, negative potential.

The anode current of most photomultiplier tubes ranges from picoamperes up to a milliamp. The electrometer amplifier is commonly used as a readout because of its high sensitivity. The low input voltage drop of such a amplifier-when used in the feedback configuration-keeps the anode at virtually ground potential. A typical hook-up is shown in Fig. 43.

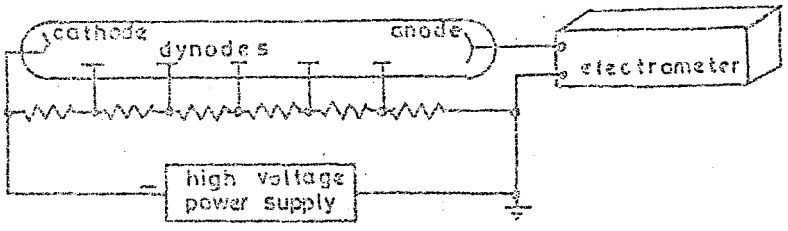

Fig. 43 The measurement of the anode current of PMT

4.2. The selection of the photomultiplier tube for astronomical use

A PMT usually has a small amount of current flowing even when the cathode is not illuminated. This phenomenon is known as 'dark current', and it is part of any signal measured. Its amount depends on the particular tube and temperature at which it is operated cooling tube thermoelectrically or with dry ice often reduces the dark current to an insignificant levels.

The following examples of the tubes shows the importance of dark current. In a selected and inexpensive EMI 9781A side window tube from Emitronics , the value of the dark

current is the half of the signal from the 11th magnitude* star by means of a 16 inches telescope.(29) For an uncooled and cheap RCA 1P21 or 931A side window tube the dark current maybbe greater than the signal from the same magnitude star. Because in these tubes the dark current is about 10^{-9}A.(30) However in a selected, cooled, EMI 6256 end window tube from Emitronics the dark current is a hundredth of the signal and it can detect the signal from the 13th magnitude star. Such high signal-to-noise ratios are important for accurate measurements, because the dark current of any PMT may change slightly during a set of observations.

Therefore the selection of PMT is very important in the astronomical usage.

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* Magnitude: A numerical designation of the brightness of a celestial object; by convention, the assigned number increases as the brightness decreases.

The scale of stellar magnitudes is logarithmic and takes into acount the fact that visual sensation varies logarithmically. For example, a two candlepower light will look proportionately as bright to the eye when compared with a one candlepower light as will a 100 candlepower 1 light, because the ratio in both cases is 2:1. The difference in magnitude (Δm) between two stars is expressed mathematically as follows.

$$\Delta m = 2{,}5 \log_{10} \frac{I_1}{I_2}$$

where I is the brightness of the source (candlepower)

CHAPTER V

OPERATING RESULTS AND CONCLUSIONS

5.1. Operating results

The operating results of each part of the system are given in the following sections.

5.1.1. Electrometer

In this work the built up electrometer is the configuration of the current-voltage converter.

The instrument uses mainly two operational amplifiers of type LF 13741, one feedback resistor of the range of $10^7\Omega$, and other control circuits. It can measure currents in the range 10^{-7}~10^{-10}A, i.e. four decades of the current using only one feedback resistor.

In the current-voltage converters the minimum current which can be measured is limited by the input leakage current and offset voltage of the amplifier. Therefore

the choice of the operational amplifiers is very important. The operational amplifier of gain G must have very low input leakage current while the operational amplifier of gain A must very low offset voltage. (Fig. 44)

In the built up design, the availcbel operational amplifiers of type LF 13741 (from National Semiconductors) had to be used. With these operational amplifiers used and the resistor of 10 % tolerance used, the current in the range 10^{-7}-10^{-9}A could be measured. But the range 10^{-10}A of current could not be measured, because these operational have a leakage current of 50 pA, offset voltage of 15 mV, and input resistance of $5\times10^{11}\Omega$. These put a limit to the lowest measurable current.

This is seen easily from the analysis of the circuit. From eqn. 2 the output error $\mathcal{E}_i$ which is due to the input leakage current, offset voltage and input resistance of operational amplifier, is given by

$$\mathcal{E}_i \cong \frac{i_1}{i_s} - \frac{V_{os}}{R_f i_s} - \frac{1}{A_v} - \frac{R_F}{A_v}\left(\frac{1}{R_s} + \frac{1}{R_i}\right)$$

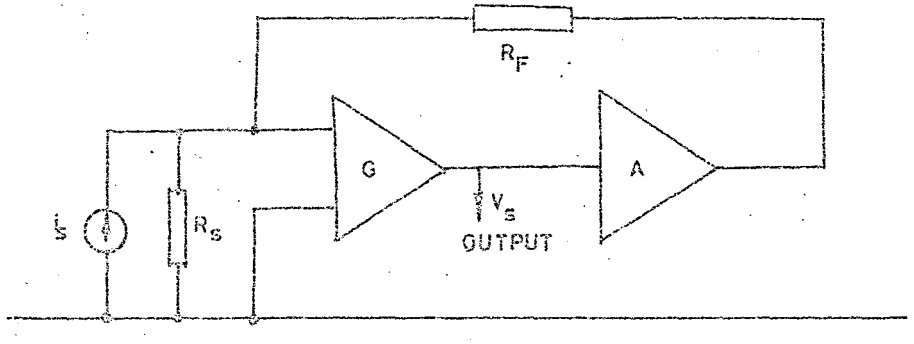


Fig. 44 The schematic diagram of the electrometer amplifier

where i_j = Input leakage current of op-amp.

V_{os} = Offset voltage of op-amp.

A_v = Open loop gain " " "

R_i = Input resistance " "

i_s = Source current

R_s = Source resistance

R_F = Feedback resistor

$R_f' = R_F \parallel R_s$

Let $i_s = 10^{-10}$A

The corresponding fractional error

$$\varepsilon_i = \frac{50\times10^{-12}}{10^{-10}} - \frac{15\times10^{-3}}{5\times10^{9}\times10^{-10}} - \frac{1}{50\times10^{3}} - \frac{10^{10}}{50\times10^{3}}\left(\frac{1}{10^{10}} - \frac{1}{5\times10^{9}}\right)$$

$$R_s = \frac{R_F \times R_i}{R_F + R_i} = \frac{10^{10}\times5\times10^{11}}{10^{10}+5\times10^{11}} = 10^{10}\Omega$$

$$R_f' = \frac{R_F \times R_s}{R_F + R_s} = \frac{10^{10}\times10^{10}}{10^{10}+10^{10}} = 5\times10^{9}\Omega$$

$$\varepsilon_i = 50\times10^{-2} - 3\times10^{-2} - 8\times10^{-5} = 0.47$$

The fractional error in the range 10^{-10}A is 47 %.

Therefore with these operational aplifiers the 10^{-10}A range can not be measured and the lowest current which can be measured by using these operational amplifiers can be calculated.

Let $i_s = 10^{-9}$A. The fractional error;

$$\varepsilon_i = \frac{50\times10^{-12}}{10^{-9}} - \frac{15\times10^{-3}}{5\times10^{8}\times10^{-9}} - \cdots\cdots$$

$$R_f' = \frac{10^9\times10^9}{10^9+10^9} = 5\times10^8\,\Omega \;; \qquad R_s' = \frac{10^9\times5\times10^{11}}{10^9+5\times10^{11}} = 10^9\,\Omega$$

$$_i = 0.05 - 0.03 = 0.02$$

The fractional error in the 10^{-9}A is 2 %.
This fact has been confirmed by our experimental results.

Thus, the operational amplifiers used in the electrometers must be very sensitive amplifiers and must have very low input leakage current and offset voltage such as PMI 156A from PMI, 8007 from Intersil etc. Once again resistors used must have the tight tolerance.

5.1.2. High voltage d.c. power supply

In this work a high voltage power supply is built up in the configuration of series linear feedback regulator. In this kind of the regulator the power dissipation is very low because of in the case of no load, the current drawn from the input rail is very low and under load, the small current drawn from the input..

This high voltage d.c. supply is capable of providing 5 mA current at the range 600-1200V, and it has ∓0.5 % stability for changes in load conditions or variations in

supply voltage range of 190-240 V. The long term stability is better than ∓ 0.1 % for 2 h-run.

5.1.3. Inverter

The inverter which forms the last part of the work is 300W capable and it is built for the general purposes. Therefore it accepts 12.8 V d.c. power and provides 220v, 50 Hz a.c. power for various instrument such as oscilloscope, test equipments etc.

The instrument operates excellent under the loads so that it is able to drive any instrument.

The instrument can handle power factors from zero to unity lagging or leading. The output voltage is within 5 % of 220 V except for zero load and power factors deviating too far from unity. This is due to the voltage sensing circuit which reads the average voltage rather than the RMS value.

It also has the temperature shutdown and overload protection. When the transistors cases reach $60^{o}C$, the temperature limiter circuit switches of the transistors. If the input current drawn from the supply exceeds 30A, the current control circuit cuts the power by going into overload state.

The inverter output wave shape is of the form shown.

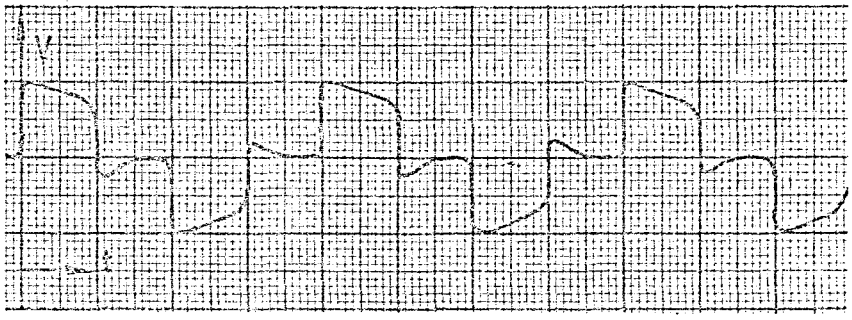


Fig. 45 The output wave shape of the inverter.

5.2. Conclusions and recommendations

This work is the beginning work on the electrometer amplifier for astronomical use in our state.

In the overall systems, the choice of the operational amplifiers in the electrometer section and the selection of photomultipiler tube is very important for measuring the signals from the 11th and so on magnitude stars.

In the electrometer, an f.e.t. input stage can be used, if the suitable op-amp can not be obtained. Also the high value resistors also must have tight tolerance.

The PC board must be designed so that it does not generate the additional noise. The leads of the op-amp must be guarded. At the same time the PC board should be as small as possible. The converter section of the electrometer and input rail must be shielded.

In the inverter, if the number of the power transistors can be decreased by ensuring and using the high power transistors, and the capacitors which are connected base and emitter of the power transistors can be removed then it may be allowed to reduce the input voltage from the car battery. In this case the protection of the transistors againg the voltage spikes must be provided by the high voltage zener diodes which are connected across the emitter and collector. Thus, the transistors switches on and off fast. For this reason they do not in the active region and the voltage on the transistors will be only saturation voltage. Therefore the input voltage may be reduced.

APPENDIX I

ELECTROMETER D.C. ANALYSIS

A - Voltage-voltage convertor

With reference to Fig.46 , the influence of the input voltage v_s, offset voltage v_{os} and input leakage current i_1 on the input terminal voltage v_1 are considered individually:

$$v_1(v_s) = \frac{v_s R_i}{(R_i + R_s)} \qquad v_1(v_{os}) = \frac{v_{os} R_i}{R_i + R_s}$$

$$v_1(i_1) = \frac{i_1 R_s R_i}{(R_i + R_s)}$$

where R_s is the source resistonce and R_i is the amplifier input resistance.

Applying superposition and $v_o = A_v (v_1 - v_{os})$,

$$v_o = A_v (v_1 (v_s) + v_1 (v_{os}) + v_1 (i_1) - v_{os})$$

Substituting and rearranging,

$$v_o = A_v v_s \left\{ \frac{R_i}{R_i+R_s} + \frac{R_s}{R_i+R_s}\,\frac{v_{os}}{v_s} + \frac{R_i R_s}{R_i+R_s}\,\frac{i_1}{v_s} - \frac{v_{os}}{v_s} \right\} \quad *$$

Eqn. (*) may be written in the form $v_o = A_v v_s (1 + \varepsilon_v)$

$$v_o = A_v\, v_s\, (\, 1 + \varepsilon_v\,)$$

where $A_v\, v_s$ represents the ideal output voltage, and ε_v represents the fractional output error given by

$$\varepsilon_v = \frac{1}{(\, R_i + R_s\,)} \left\{ \frac{v_{os}\, R_i}{v_s} + \frac{i_1\, R_s\, R_i}{v_s} - R_s \right\}$$

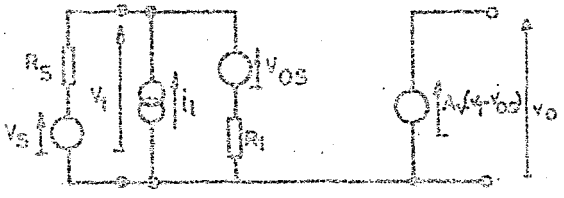


Fig. 46 Equivalent circuit of the voltage-voltage convertor

B - Current-voltage convertor

With reference to Fig. 47 , we have

$$i_f = i_1 + i_2$$

where $i_1 = \dfrac{(\, i_s R_s - v_1\,)}{R_s}$ $\qquad$ $i_2 = \dfrac{(\, v_{os} - v_1 + i_1 R_i\,)}{R_i}$

Also, $v_o = v_1 - i_f R_f$

From operational amplifier theory,

$$v_o = - A_v (v_1 - v_{os})$$

Solving for v_o we have

$$v_o = \frac{- R_f \left\{ i_s - \left[\frac{v_{os}}{R_s} \right] + i_1 \right\} + v_{os}}{1 + \frac{1}{A_v} + \frac{R_f}{A_v R_s} + \frac{R_f}{A_v R_i}}$$

Approximating and rearranging we have

$$v_o = - R_f i_s (1 + \mathcal{E}_i)$$

where $\mathcal{E}_i$ is the fractional output error, given by

$$\mathcal{E}_i \approx \frac{i_1}{i_s} - \frac{v_{os}}{i_s R_f'} - \frac{1}{A_v} - \frac{R_f}{A_v} \left(\frac{1}{R_s} + \frac{1}{R_i} \right)$$

where $R_f' = R_f \| R_s$.

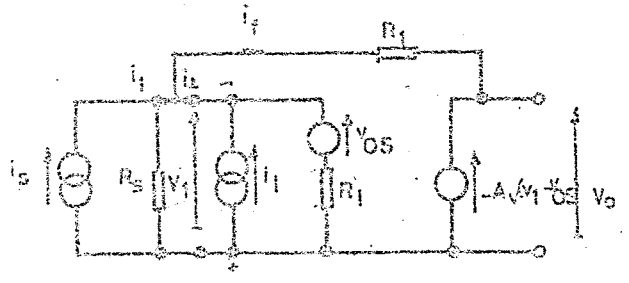
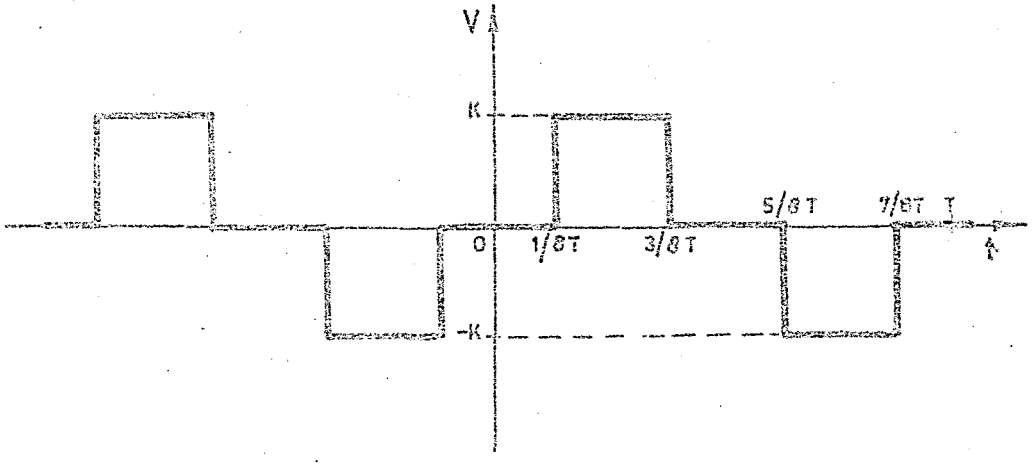


Fig. 47 Equivalent circuit of the current-voltage convertor

APPENDIX II

FOURIER ANALYSIS OF NON-SINUSOIDAL WAVEFORM



$$V(t) = Ku(t - \frac{1}{8}T) - Ku(t - \frac{3}{8}T) - Ku(t - \frac{5}{8}T)$$

$$+ Ku(t - \frac{7}{8}T)$$

where in the above equation $Ku(t - \tau)$ is defined as:

$$Ku(t - \tau) = \begin{cases} K & t \geq \tau \\ 0 & t < \tau \end{cases}$$

The Fourier series expansion of a function V(t) will be of the form.

$$V(t) = \frac{a_o}{2} + \sum_{n=1}^{\infty}\left[a_n.\text{Cos}(\frac{2\Pi n}{T}t) + b_n.\text{Sin}(\frac{2\Pi n}{T}t)\right]$$

where

$$a_n = \frac{2}{T}\int_0^T V(t).\text{Cos}(\frac{2\Pi n}{T}t).dt$$

$$b_n = \frac{2}{T}\int_0^T V(t).\text{Sin}(\frac{2\Pi n}{T}t).dt$$

From the above figure it is obvious that V(t) is an odd function. Therefore, we conclude the important result that all the a_n coefficients are identically equal to zero.

$$V(t).\text{Cos}(\frac{2\Pi n}{T}t) = \text{odd function}$$

(odd).(even)

$$\int_0^T \text{odd function}.dt = 0$$

Therefore it is only necessary to compute the b_n coefficients:

$$b_n = \frac{2}{T}\left[\int_0^T V(t).\text{Sin}(\frac{2\Pi n}{T}t).dt\right]$$

$$b_n = \frac{2}{T}\left[\int_{\frac{1}{8}T}^{\frac{3}{8}T} K\ \text{Sin}(\frac{2\Pi n}{T}t)dt + \int_{\frac{5}{8}T}^{\frac{7}{8}T}(-K)\ \text{Sin}(\frac{2\Pi n}{T}t)dt\right]$$

$$b_n = \frac{2}{T}\left[\left(-\frac{KT}{2n}\right)\text{Cos}(\frac{2\Pi n}{T}t)\Big|_{\frac{1}{8}T}^{\frac{3}{8}T} + \left(\frac{KT}{2n}\right)\text{Cos}(\frac{2\Pi n}{T}t)\Big|_{\frac{5}{8}T}^{\frac{7}{8}T}\right]$$

The above expression for b_n can be simplified:

$$b_n = -\frac{4K}{n}\,\mathrm{Sin}\left(\frac{\pi n}{4}\right)\,\mathrm{Cos}(\pi n)\,\mathrm{Sin}\left(\frac{\pi n}{2}\right)$$

If n = even $\qquad \mathrm{Sin}\left(\frac{\pi n}{2}\right) = 0 \quad \therefore \quad b_n = 0$

Thus

$$V(t) = b_1\,\mathrm{Sin}\left(\frac{2\pi}{T}t\right) + b_3\,\mathrm{Sin}\left(\frac{6\pi}{T}t\right) + b_5\,\mathrm{Sin}\left(\frac{10\pi}{T}t\right) + \ldots\ldots$$

and

$$V(t) = 0.9\,K\,\mathrm{Sin}\left(\frac{2\pi}{T}t\right) - 0.3\,K\,\mathrm{Sin}\left(\frac{6\pi}{T}t\right) - 0.18\,K\,\mathrm{Sin}\left(\frac{10\pi}{T}t\right)$$

$$+0.12\,K\,\mathrm{Sin}\left(\frac{14\pi}{T}t\right) + 0.1\,K\,\mathrm{Sin}\left(\frac{18\pi}{T}t\right) - \ldots\ldots$$

where K is the step voltage.

APPENDIX III

COST EVALUATION

The components used in the system and their costs are as follows;

A - Electrometer

1.	10xIC	1100 T.L.
2.	6xDiodes	50
3.	7xTransistors	400
4.	6xCapacitors	300
5.	Various resistors	200
6.	2xTrimmers	300
7.	1xScale(10V)	1000
8.	LEDs,fuse and switch	250
9.	1xTransformer(220-2x12V)	250
10.	Chasis and rubber feet	500
11.	10xIC Sockets	400
12.	Pc Board(150x200mm)	150
13.	Miscellaneous	100

B - High voltage d.c. power supply

1.	4xIC	500
2.	4xHigh voltage transistors	700

3.	12xZener Diodes	450
4.	10xDiodes	100
5.	6xTransistors	300
6.	1xTransformer (220-2x12, 2x230V)	1500
7.	Trimmers and resistors	550
8.	7xCapacitors	500
9.	Cord, plug, fuse and switch	450
10.	Chassis and rubber feet	500
11.	2xIC Sockets	100
12.	15cm extruded aluminium heat sink	350
13.	PC Board (100x300 mm)	150
14.	Miscellaneous	100

C.- Inverter

1.	4xIC	450
2.	8xTransistors	450
3.	6xPower transistors	1800
4.	1xNTC and 1xSCR	200
5.	7xDiodes	150
6.	Bridge rectifier	100
7.	2xTrimmers	300
8.	Resistors	350
9.	Capacitors	450
10.	4xIC Sockets	200
11.	Cord, plug, fuse, lamps and switch	750
12.	22 way PC Socket and PC Board	350
13.	Extruded aluminium heat sink (30 cm)	700
14.	Transformer	5000
15.	Chassis and rubber feet	750
	TOTAL	23,000 T.L.

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