MICROPROCESSOR BASED PULSE WIDTH MODULATED INVERTER

by

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ABSTRACT

Microprocessor control of variable voltage and variable frequency inverter drivers has many advantages over conventional analogue techniques; such as improved reliability, manufacture, maintanence and servicing, and increased control flexibility. In addition that, precise timing and sufficient harmonic elimination can be obtained. It also results from a reduction in the complex control circuitry since it is replaced by microprocessor software.

As conventional method, a desired sinousodial wave is modulated with a carrier triangular wave, however it has essentialy some defects such as:

(a) insufficient tolerance of temperature fluctuations.

(b) when the two waves are not synchronised, a short pulse can occur and causes commutation failure.

(c) if a precise control is desired, circuits become much complex, as a result, it increases cost substaintially.

(d) analogue method can do nothing for harmonic minimization.

The digital control can solve these problems, in addition posseses the following advantages.

(a) since data are calculated beforehand, the output waveform has high quality, for example of harmonic suppression.

(b) it is easy to add new functions or to modify them since they are under the software control of the microprocessor.

In this thesis, a software based pulse width modulated (PWM) inverter drive system is presented. Emphasis is placed on minimization of the hardware requirements. An additional critarion is that an efficient program structure is used in order to minimize the computation time required; hence increasing the operational speed considerably.

ÖZETÇE

Mikroişlemci denetimli değişken gerilim ve değişken frekanslı eviriciler klasik analog yöntemlerle tasarımlananlarla kıyaslandığında birçok üstünlüklere sahiptirler. Bunlar, güvenilirliğin artması, bakım, imalat ve hizmetlerin kolaylaşması ve denetim olanaklarının artması olarak sıralanabilir. Bunlara hassas zamanlama ve yeterli düzeyde harmoniklerin bastırılabilme olanağı da ilave edilebilir. Karmaşık denetim devrelerinin yerini ise mikroişlemcinin yazılım devresi aldığı için donanım devresinde bir azalma da görülür.

Klasik yöntemde, istenen sinüssel dalga bir taşıyıcı üçgen dalga ile modüle edilerek elde edilir. Fakat bu yöntem aşağıda sıralanan özellikler açısından yetersizdir:

(a) sıcaklık değişmelerine karşı hassastır.

(b) eğer iki dalga eşzamanlı değilse meydana gelebilecek kısa bir darbe aktarımda hata yaratır.

(c) hassas bir denetim isteniyorsa devreler çok karmaşık olmakta, bu ise maliyeti çok yükseltmektedir.

(d) analog yöntem harmonikleri bastırabilme özelliğine sahip değildir.

Sayısal denetim bütün bu sorunları çözdüğü gibi aşağıdaki özelliklere de sahiptir:

(a) aktarım darbeleri önceden hesaplandığı için çıkış dalga

şeklinin özelliklerini denetlemek mümkündür.

(b) eviriciye yeni işlevler ilave etmek ya da değiştirmek kolaydır, çünkü tüm işlevler mikroişlemcinin yazılım devresi tarafından kontrol edilir.

Bu tezde yazılım devresine dayalı darbe genişlik modülasyonlu evirici tasarımlanmıştır. Özellikle donanım devresinin en aza indirilmesine çalışılmıştır. Buna ilaveten etkin bir yazılım kullanılarak hesaplama zamanının kısaltılması sağlanmış, dolayısıyla da eviricinin çalışma hızı arttırılmıştır.

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LIST OF SYMBOLS

M	Modulation index
R	Carrier frequency/modulating frequency
T	Time period of carrier signal
C	Count number
f	Output frequency of the inverter
t_p	Width of modulated pulse
w	Angular velocity of modulating signal

I. GENERAL FEATURES OF INDUCTION MOTORS

Since d.c. motors give good control characteristics, they are widely used for the application of variable speed systems. However, they have some essential defects such as trouble on commutation or tedious maintanence over commutators and brushs. For this reason, induction motor speed control has gained importance in accordance with the progress in technology.

A. Introduction to Induction Motors:

Induction motor is one in which alternating current is supplied to the stator directly and to the rotor by induction. When excited from a balanced polyphase source, it will produce a magnetic field in the air-gap rotating at synchronous speed as determined by the number of poles and the applied stator frequency.

The rotor may be either wound rotor or squirrel cage type. A wound rotor has a polyphase winding smiliar to and wound for the same number of poles as the stator. The terminals of the rotor windings are connected to insulated slip rings mounted on the shaft. Carbon brushes bearing on these rings

make the rotor terminals availiable external to the motor. However, squirrel cage rotor has a winding consisting of conducting bars embadded in slots in the rotor iron and short-circuited at each end by conducting end rings. The extreme simplicity and the ruggedness of the squirrel cage construction are the outstanding advantages of the induction motor.

B. Equivalent Circuit of the Induction Motor:

The equivalent circuit of the induction motor is very similiar to the transformer equivalent circuit, since the induction motor is essentialy a transformer with a rotating secondery winding. In induction motors, the stator current establishes a mutual flux which links the rotor windings, and a leakage flux induces a primary e.m.f. which is proportional to the rate of change of stator current, and its effect may be represented by a series leakage reactactance X_1 in each stator phase. R_1 is the stator leakage impedance. The mutual flux in the air-gap induces slip frequency e.m.f.s in the rotor and the supply frequency e.m.f.s in the stator. The stator current, I_1 is composed of the exciting current and the load component of the stator current which cancel the mmf due to the rotor current. The exciting current I_ϕ consists of the magnetizing and core loss components I_m and I_c respectively. The stator terminal voltage differs from the counter e.m.f. by the voltage drop in the stator leakage

impedance. The phasor relation for the phase under consideration being:

$$V_1 = E_1 + I_1 (R_1 + jX_1) \qquad (1.1)$$

At standstill, the induced e.m.f. per phase in the equivalent rotor is equal to the stator e.m.f. E_1, and the rotor frequency equals to the supply frequency f_1. When the motor runs with a slip s, the rotor e.m.f. $E_2 = sE_1$, and the rotor frequency $f_2 = sf_1$. If R_2 is the equivalent rotor resistance per phase, and X_2 is the rotor leakage reactance per phase the rotor current is given by:

$$I_2 = \frac{E_2}{R_2 + jsX_2} = \frac{sE_1}{R_2 + jsX_2} \qquad (1.2)$$

$$I_2 = \frac{E_1}{R_2/s + jX_2} \qquad (1.3)$$

In Eq. (1.2), all rotor quantities are at slip frequency, but in equation (1.3), they are at supply frequency. This shows that if the rotor is brought to standstill and the resistance increased from R_2 to R_2/s the rotor current is unaltered. Therefore the rotor equivalent circuit may be joined directly to the stator circuit as in Fig. 1.2

The equivalent circuit shows that the total power P_g transfered across the air-gap from the stator is:

$$P_g = q_1 I_2^2 \frac{R_2}{s} \qquad (1.4)$$

where q_1 is the number of stator phases. The total copper loss is evidently:

$$P_c = q_1 I_2^2 R_2 \qquad (1.5)$$

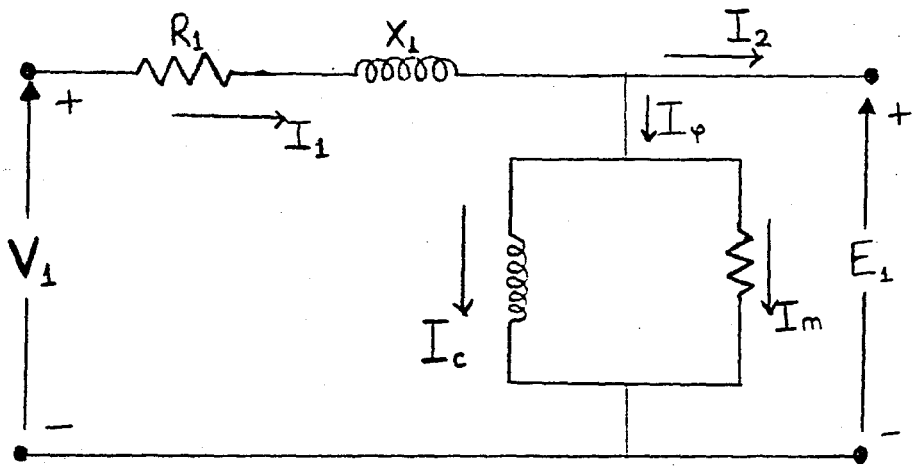


Fig. 1.1. Stator equivalent circuit for a polyphase induction motor.

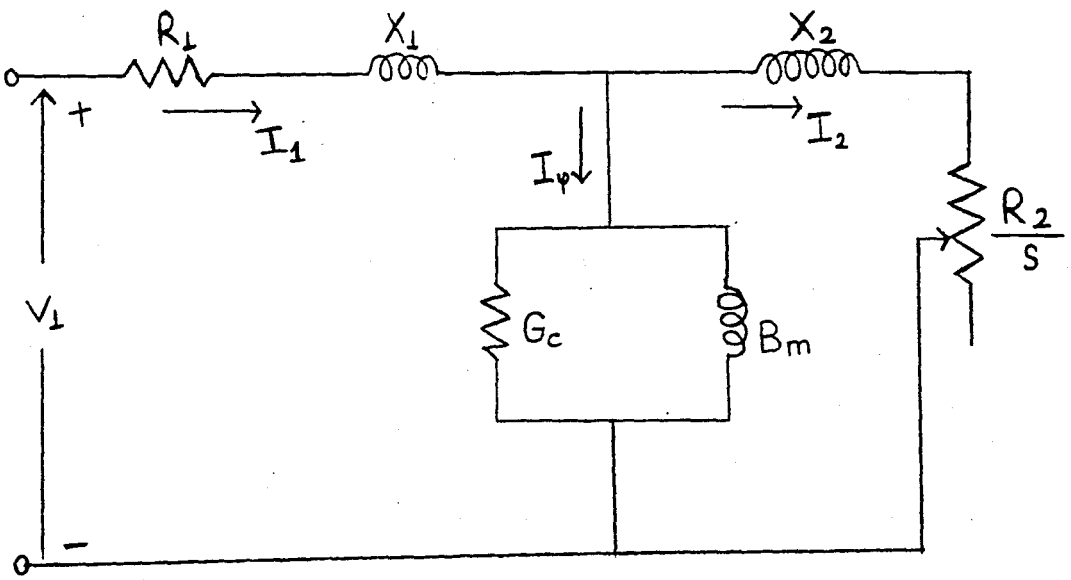


Fig. 1.2. Equivalent circuit of a polyphase induction motor.

The internal mechanical power P developed by the motor is therefore:

$$P = P_g - P_c = q_1 I_2^2 \frac{R_2}{s} - q_1 I_2^2 R_2 = q_1 I_2^2 R_2 \frac{1-s}{s} \qquad (1.6)$$

$$P = (1-s)\, P_g \qquad (1.7)$$

Equation (1.7) shows that only the fraction (1-s) of the total power delivered to the rotor is converted to mechenical power, and the fraction s is dissipated as rotor circuit copper loss. The internal electomagnetic torque T, corresponding to the internal power P will be:

$$P = (1-s)\, w\, T \qquad (1.8)$$

where w is the synchronous angular velocity of the rotor in mechanical radians per second. By using equation (1.6)

$$T = \frac{1}{w}\, q_1 I_2^2 \frac{R_2}{s} \qquad (1.9)$$

As can be seen from equation (1.9), the internal torque is a function of slip at any speed. Figure 1.3 shows the torque-slip curve in both motor and generator regions.

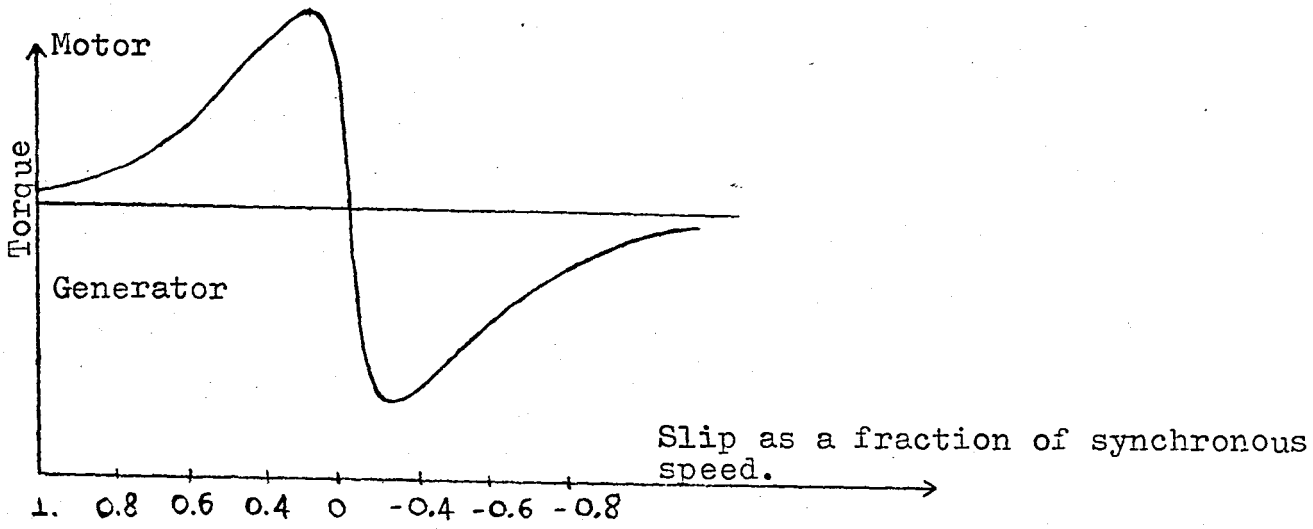


Fig.1.3. Induction motor torque-slip curve.

C. Speed Control Systems:

In a three phase machine, the windings of the individual phases are displaced from each other by 120 electrical degrees in space. If the symmetrical three phase windings are supplied from a balanced three phase power supply, a rotating field is produced. The synchronous speed of the induction machine is directly proportional with the applied frequency to the stator. If p denotes pole pairs and f is the applied frequency, the synchronous speed of the motor is defined as:

$$n_s = \frac{60\ f}{p} \quad \text{rev/min.} \qquad (1.10)$$

If s is the slip at any speed, the speed of an induction motor will be :

$$n = n_s(1-s) \qquad (1.11)$$

$$n = \frac{60\,f}{p}\,(1-s) \qquad (1.12)$$

Equation (1.12) shows that the speed of an induction motor can be controlled by :

(a) increasing slip

(b) changing pole pairs

(c) controlling stator voltage

(d) changing stator frequency by keeping V/f constant

For a wound-rotor motor, by changing external rotor circuit resistance causes the slip to increase. When slip increases the speed of the machine decreases. This method is rather inconvenient and also costly for large powers since it is achieved by dissipating power as heat in the external resistances. However, special auxilary machines can be used to convert the power at slip frequency and return it to the supply.

Changing pole pairs in order to control the speed of an induction motor is generally applied to the squirrel cage type motors. For this type of control, the stator windings are so designed that simple change in stator connections changes the number of poles.

The speed of an induction motor can also be controlled by changing only line voltage. The internal torque developed by an induction motor is proportional to the square of the applied voltage. In Figure 1.4 two different torque-speed characteristics are shown. If line voltage is changed, the speed of the machine is reduced from n_1 to n_2.

The principal disadvantages of both line voltage and slip-changing speed control are low efficiency at reduced speeds and poor speed regulations with respect to change in load.

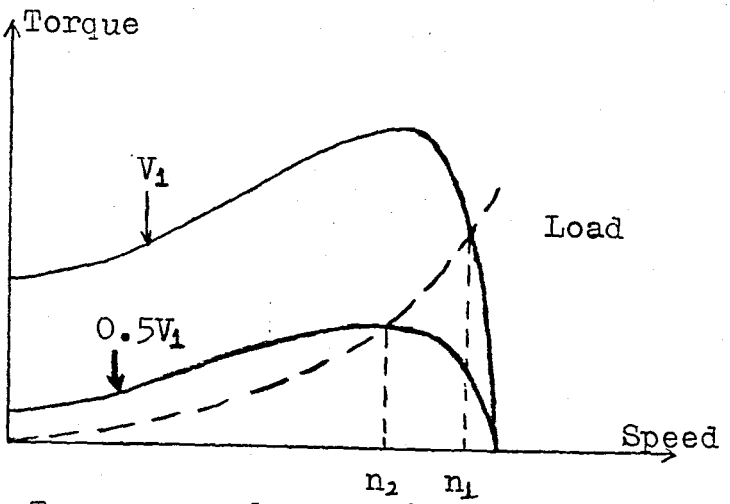


Figure 1.4. Torque-speed curve for different stator voltages.

The speed of an induction motor is directly proportional with the applied stator frequency. By changing applied frequency, the speed of an induction motor can be controlled in 1:100 range.

In general, when stator frequency changes, the internal torque of the motor also changes. However, in the industrial applications, varible drive systems are required to operate with either constant torque or constant power. For constant torque operation, stator voltage is decreased with decreasing stator frequency, keeping V/f ratio constant. In this way air-gap flux is kept constant. This is called "constant V/f operation mode." Above nominal frequency, when stator frequency increases the stator voltage is kept constant so that constant power operation is achieved. At very low frequencies, stator

leakage reactance becomes competible with the stator reactance so the stator e.m.f. E_1 is very much reduced. To keep air-gap flux constant, V_1 must be increased over its marked value so that the corresponding stator voltage curve will be that as shown in Fig 1.5. and corresponding torque-speed curve is shown in Fig. 1.6.

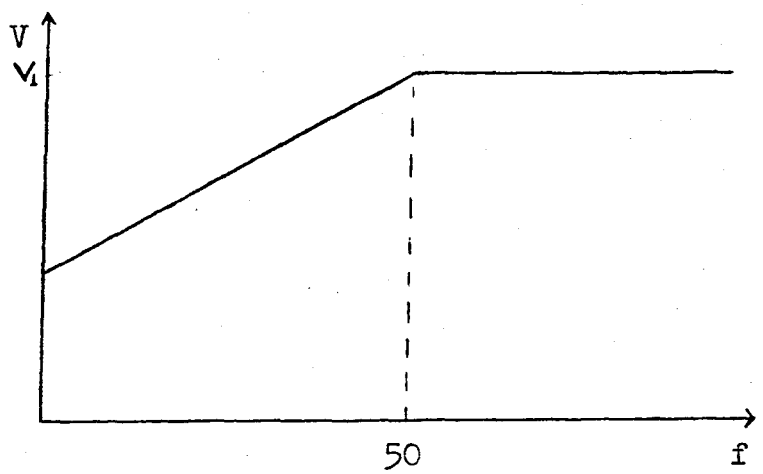


Figure 1.5. Stator voltage-frequency law for an induction motor.

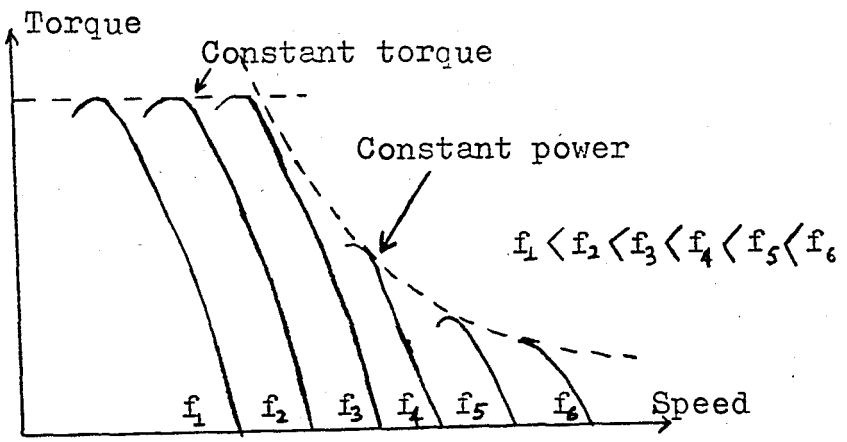


Figure 1.6. Torque-speed characteristics of operation with constant torque and power.

Figure 1.7. shows the starting torque and starting current in constant V/f mode of operation. It is evident that starting torque is increased and starting current is rather decreased. These are main advantages of operating at constant V/f mode.

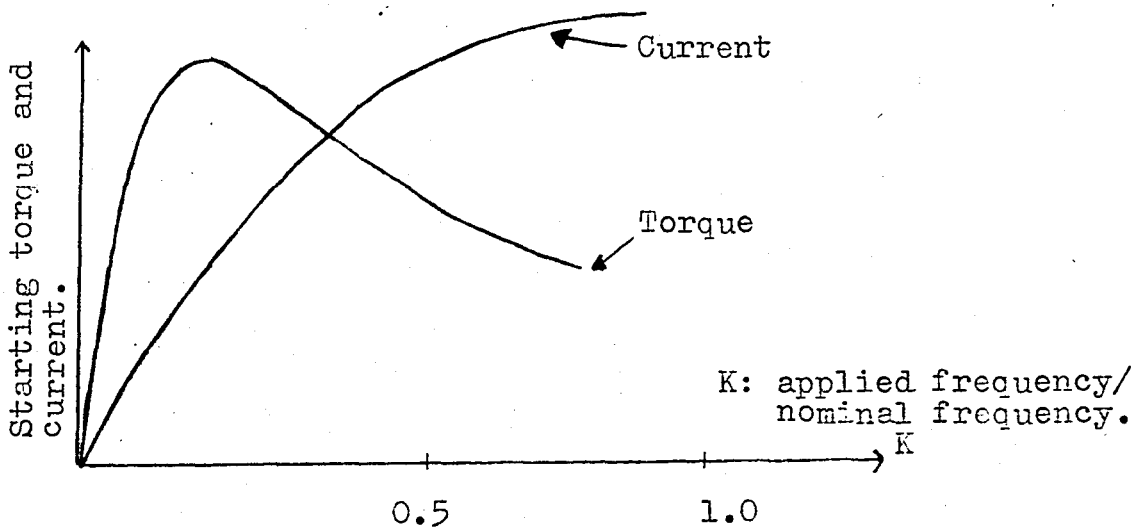


Figure 1.7. Starting torque and current at constant V/f mode of operation.

In general, to change the stator voltage and frequency under the constant V/f condition, pulse width modulation (PWM) is used. This technique will be explained in detail in chapter II.

II. PULSE WIDTH MODULATION

Pulse width modulation is widely used in variable voltage, variable frequency drive systems. Although it requires a much complex hardware circuitry in analogue implementation, improvement in digital technology has reduced the circuitry and increased the accuracy. Therefore, PWM inverter has become attractive in a.c. drives.

A. Switching Strategy in PWM:

The easiest and most widely used type of PWM is the "natural sampled PWM." Figure 2.1 shows the general features of this mode of sampling. As can be seen, the modulating sine wave is compared directly with the triangular carrier wave and the intersection points determine the resultant pulse widths. The most important characteristic in this mode of sampling is that the resultant pulse width is proportional with the amplitude of the modulating wave at the instant the switching occurs. Therefore, it is not possible to define the widths of the pulses using an analytic expression. The pulse widths can only be defined by the transcendental equation :

$$t_p = \frac{T}{2}\left[1 + \frac{M}{2}(\mathrm{Sin}wt_1 + \mathrm{Sin}wt_2)\right] \qquad (2.1)$$

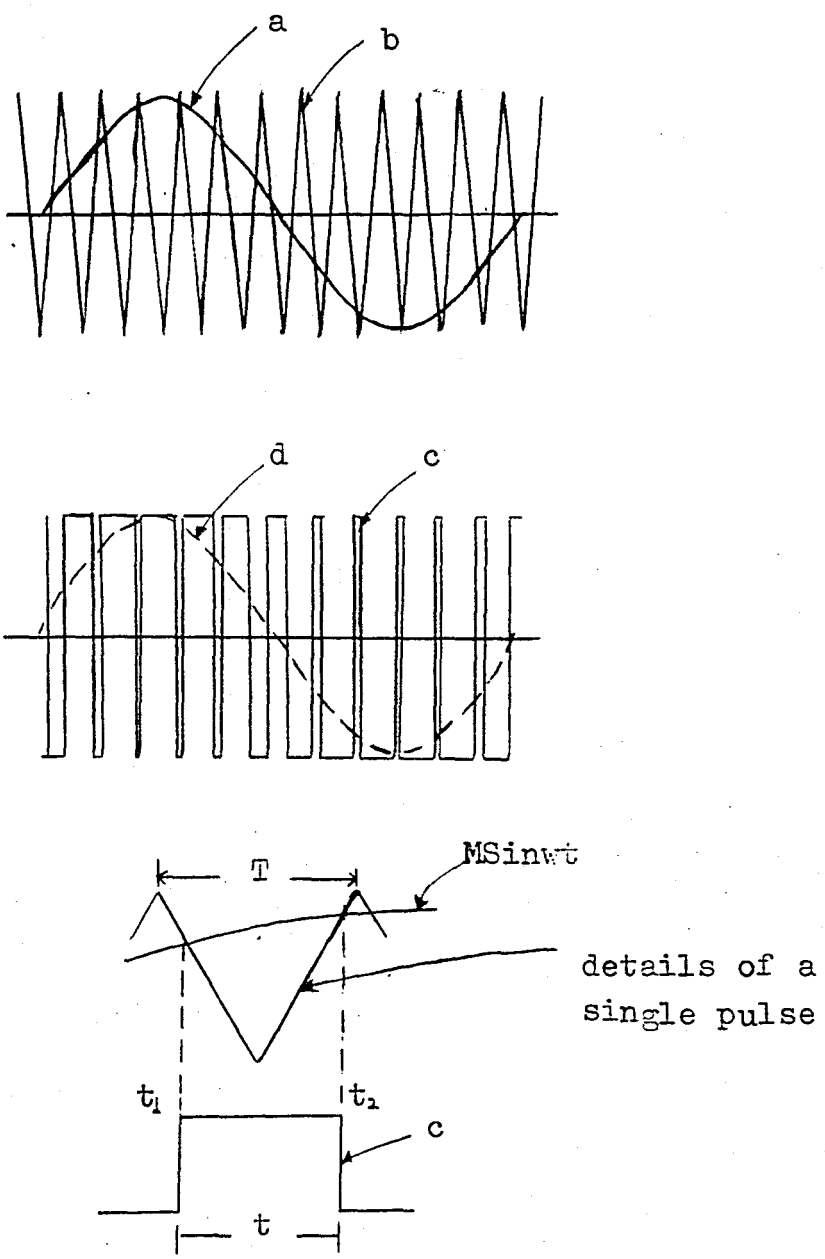


Figure 2.1 Natural sampled PWM
a. Reference modulating signal
b. Carrier signal
c. PWM voltage
d. Fundamental of PWM voltage.

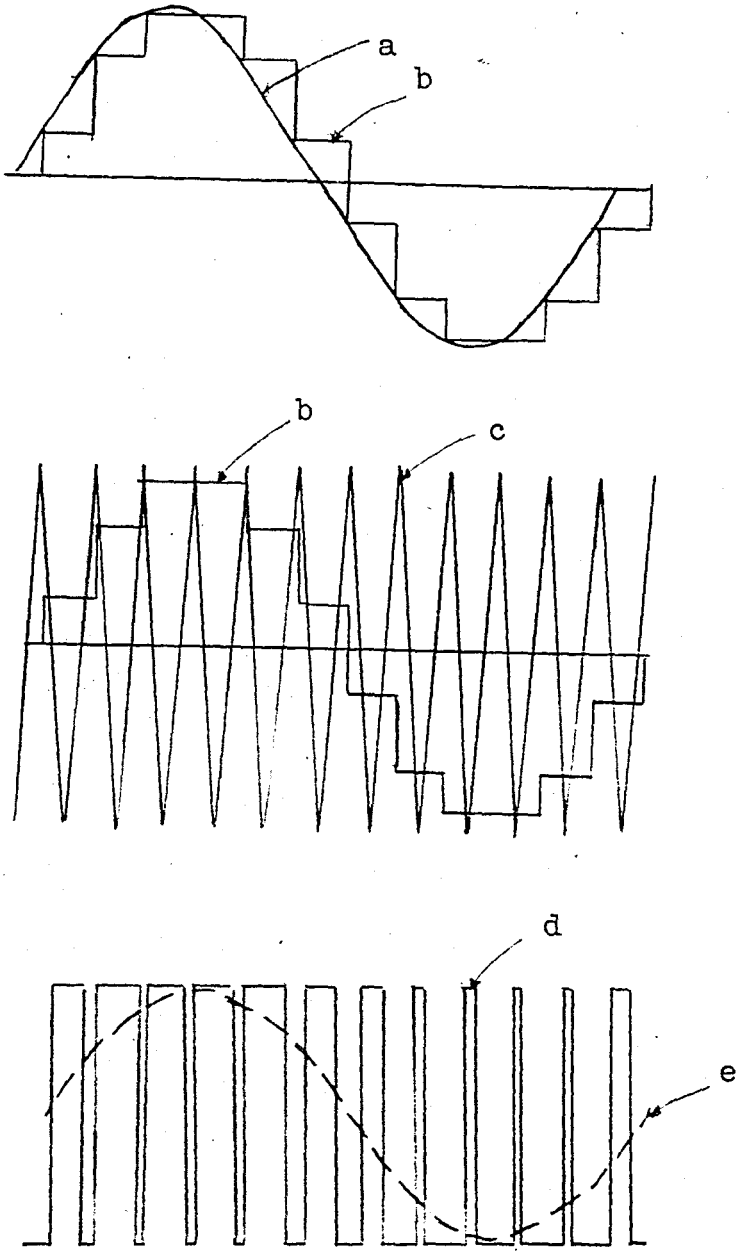


Figure 2.2 Regular sampled PWM
a. Reference modulating signal
b. Sample and hold modulating signal
c. Carrier signal
d. PWM waveform
e. Fundamental of PWM waveform.

For this reason, it is widely used in analogue implementation and it can be used in hardware based microcomputer systems.

Regular sampled PWM is another technique to determine the switching instants. It is more attractive for digital control systems, since it offers the possibility of defining the pulses analytically. Figure 2.2 shows the ragular sampled PWM waveform. To obtain regular sampled pulses, firstly the sine wave is sampled and held and then it is compared with the triangular carrier wave. Since the amplitude of the sine wave is constant during one period of the carrier wave, it is possible to define the pulses using an analytic expression, that is:

$$t_p = \frac{T}{2} \left(1 + M \sin w_m t_i \right) \qquad (2.2)$$

The sampling instants can be calculated directly using Eq (2.2) and it forms the basis of the software based microcomputer systems.

The third and the newest method is called "optimal PWM." This approach is based on the minimization of certain performance criteria; especially for minimization of harmonic content. The idea behind this statement is that such switching angles can be found so that the fundamental of the resultant waveform would be maximum and the low harmonics would be mininum. Computer algorithms to generate these optimised strategies are rather complex and complicated for main frame computers. However, at low frequency ratios (carrier frequency/modulating frequency) it is possible to write down the algorithms so that

microprocessor can utilize the solutions of the algorithms solved by the main frame computer for the inter-relations of the modulation index, frequency ratio and output frequency to obtain optimum waveforms.

If it is desired to analyse the harmonic spectrum and if quarter wave symmetry of the waveform is assumed, then only odd harmonics exist and these can be defined as:

$$V_n = \frac{4}{n\pi}\left(1+2\sum_{k=1}^{m}(-1)^k \mathrm{Cos}n\alpha_k \right) \qquad (2.3)$$

where n corresponds to the harmonic order and m equals the number of switching angles per quarter cycle. Figure 2.3 shows a typical optimized PWM waveform.

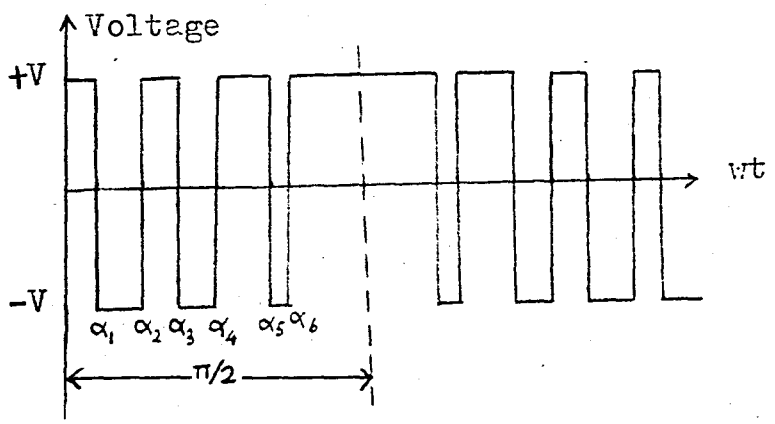


Figure 2.3. Typical optimised PWM waveform.

The weighted harmonic voltage distortion of the PWM votage is defined by the equation:

$$\sigma = \left[\sum_{n=1}^{30} \left(\frac{V}{n}\right)^2 \right]^{1/2} \Big/ V_1 \qquad (2.4)$$

B. PWM Control Functions:

Every microcomputer based PWM inverter must control three phase generation, frequency ratio, minumum pulse width, switching strategy and voltage per frequency.

To generate three phase waveform, it is sufficient to calculate the switching pattern of one quadrant of the waveform. With the aid of the symmetry, three phases are loaded to the memory just by shifting and / or inverting the calculated portion of the waveform.

To operate with constant torque, the fundamental component of the waveform must decrease when the output frequency decreases. This is achieved by decreasing the modulation index proportional with the frequency. Figure 2.4. shows the relation between fundamental voltage and the modulation index.

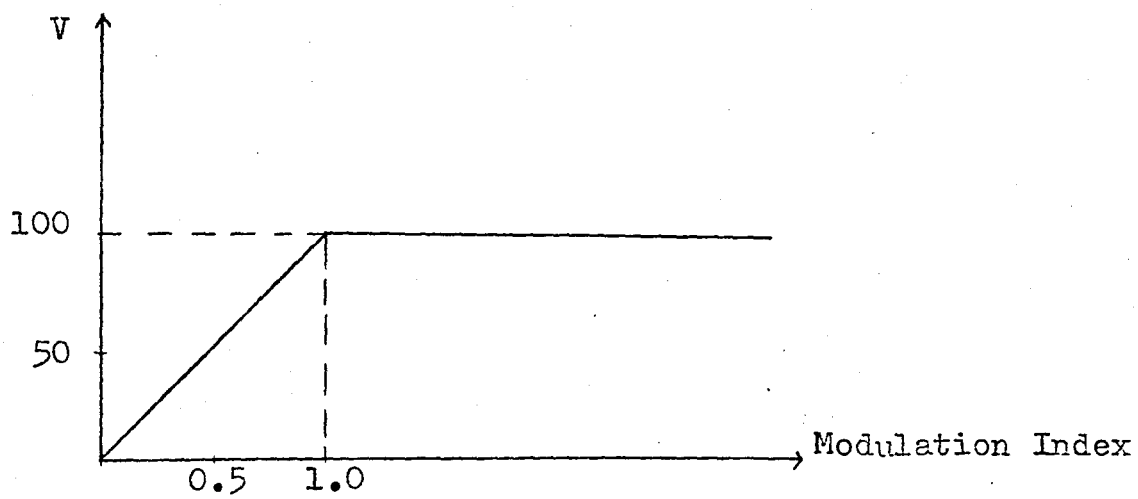


Figure 2.4. Fundamental versus modulation index

It is necessary to control the frequency ratio (carrier frequency/modulating frequency) in order to utilize fully the harmonic minimization capabilities of PWM. Fourier analysis of the PWM waveform shows us that the output voltage has a fundamental, some lower harmonics and a strong harmonic at the carrier frequency. To block out the strong harmonic component at the carrier frequency, carrier frequency should be much higher than the modulating frequency so that the stator windings accept the waveform as approximately modulating wave. On the other hand, microcomputer must calculate the output pattern during one period. Therefore, there is a trade-off between the frequency ratio and output frequency. Undoubtadly, it is desirable to operate the system at the maximum carrier frequency. However when the frequency ratio increases, the calculation time increases, so the maximum output frequency is reduced. The solution is called "discreate integer ratio adaptive mode." At this mode of control, the frequency ratio for maximum output frequency is determined, and frequency ratio is increased when the output frequency decreases. The frequency is changed in integer steps at discreate points in the output frequency range and therefore the corresponding carrier frequency varies between a maximum and a minimum value when ratio changes.

Minumum pulse width is restricted by the power elements of the inverter. Minumum pulse width is so chosen that the delay of the power element should be smaller than the minumum pulse width, therefore commutation failure is prevented. Commutation failure is generally known as a problem in the

natural sampled technique. In regular and optimum PWM techniques since the switching pattern is under the software control of the microcomputer, commutation failure does not occur. If the pulse width is smaller than the required one, pulse dropping is done.

C.Software Based PWM:

In general, the switching pattern of the PWM inverter is either calculated by software of the microcomputer or determined by external hardware. In the former, CPU is responsible of performing all control functions in addition to switching pattern. However in the latter, the only required thing by microprocessor is to generate variable frequency modulating wave. Figure 2.5 shows a typical hardware based scheme.

In hardware based system, memory contains sampled and held sine wave values. The output frequency is determined by variable frequency clock. Clock interrupts CPU and at each transition, CPU choose the corresponding sine wave value and sends it to the multiplier. CPU also determines the modulation index and puts it into multiplier. Multiplier multiplies modulation index with the corresponding sine wave value. It is then compared with a triangular carrier wave. For a three phase operation, multiplier is multiplexed and extra comparators are added. The advantage of the hardware based system is the operating speed of the inverter. The maximum switching frequency is only limited by the power circuit. The heart of the system is the

multiplier. In such a configuration, hardware multiplier should be used. If software multiplier is preferred, speed is reduced significantly, so the outstanding advantage of the hardware based system gets lost. The major disadvantage is the increased cost of the system. In addition to microcomputer, the configuration needs external hardware and it increases cost substantially. From the viewpoint of engineering, nothing can be done to obtain optimal PWM waveform.

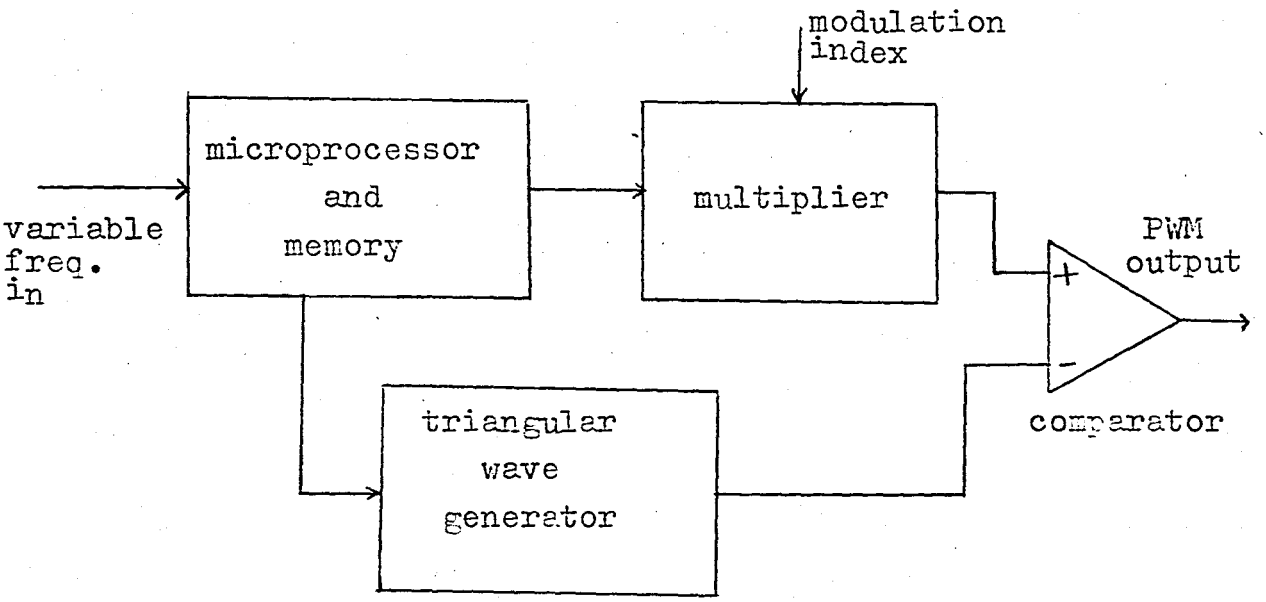


Figure 2.5. Hardware based scheme.

These disadvantages are eliminated by using a software based system. In this method, quarter wave of one hertz sine wave is sampled and held and stored in memory as a look-up table. Modulation index is also stored in memory in a desired resolution. When the required frequency is greater than 50 Hz., modulation index is unity, for the lower values of 50 Hz., modulation index decreases linearly. The pulse widths of the output waveform is

calculated by the equation (2.2). To minimize the computation time of the pulse widths, the second term of the equation (2.2) which is a multiplication operation is performed for all possible combinations on off-line and stored into RAM as look-up table. In the case of a frequency demand, microprocessor just selects the results of the multiplications from the look-up table corresponding to the current value of frequency.

In the design, the on-line computation time is always kept less than the output period. The first term of the equation (2.2) is always constant whatever the modulating frequency is. Since discreate integer ratio adaptive mode is adopted, frequency ratio changes in steps when the frequency changes. Therefore, since the period of the carrier wave T, is kept constant, when ratio changes total memory in which output pattern is stored changes. In other words, when output frequency decreases, the total memory increases. Memory increases step by step in order to increase the timing accuracy, to block out the beat frequency effect and to minimize harmonic distortion. Table 2.1. shows the output frequency range, frequency ratio, memory dimentions, carrier frequency and modulation index. Since the power transistors used in the inverter designed has a maximum collector-emiter breakdown voltage of 100 volts, inverter d.c. power supply was adjusted to 100 volts. Since tested squirrel cage induction motor has a nominal voltage 220 V, 100 volts corresponds to the 16 Hz. stator frequency when the modulation index is unity and decreases linearly when the modulation index decreases. Therefore, if the motor used has a 220 volts of nominal voltage, maximum allowable speed is 480 rev/min. for a four pole motor. However,

the frequency range of the inverter can be increased just by replacing the power transistors used in the inverter. System has an analogue to digital converter to set the reference speed. The flowchart of the PWM inverter is shown in Figure 2.6.

output freq.	r.p.m.	freq. ratio	modul. index	memory byte/180	carrier freq.
16-11	480-330	60	1-0.79	496	960-660
11-6	330-198	80	0.79-0.51	640	880-480
6-1	198-30	96	0.51-0.21	768	576-96

Table 2.1

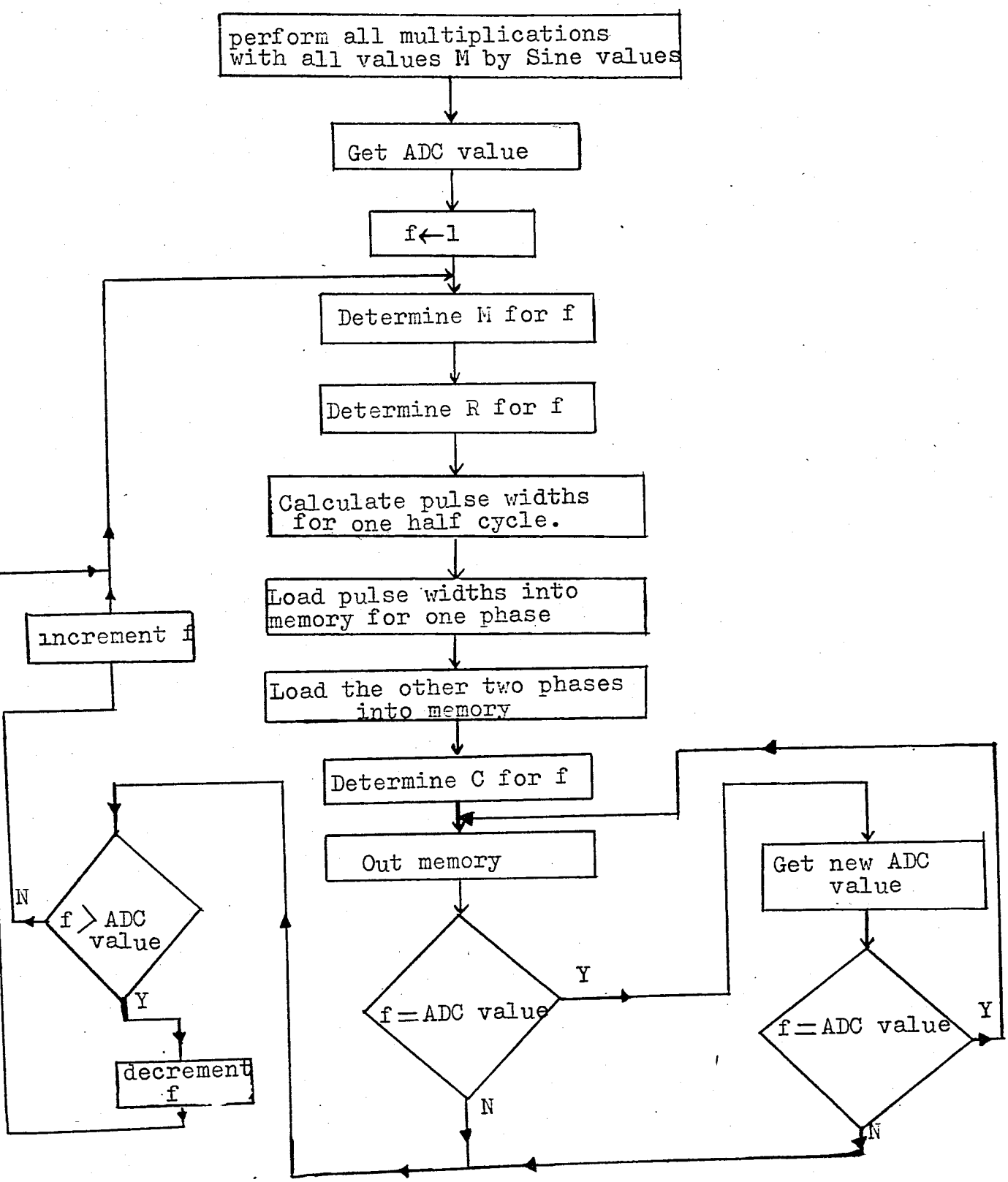


Figure 2.6 Flowchart of the PWM inverter schemes.

III. INVERTER

Inverters are used to transfer energy from a d.c. source to an a.c. load of arbitrary frequency and phase. In motor drive systems, inverters employ thyristors or power transistors as controlled switching elements to form the desired a.c. waveforms. Depending upon the applications, single phase inverters, three phase self-commutated or forced commutated inverters can be used.

A. Three Phase Inverters:

The three phase inverter has a minimum of six switching elements arranged in a bridge configuration; these elements are switched sequentially to synthesize at the a.c. terminals of the inverter bridge a set of three phase voltages which are applied to the motor. In the case of a thyristor inverter, the thyristors are turned off by commutating capacitors either by the on-coming thyristors or by auxiliary thyristors. Former is called "self commutation" and the other is called "forced commutation mode" With forced commutation, the conduction time of each thyristor can be controlled independently of frequency for purposes of waveform or voltage control. Figure 3.1 shows a thyristor inverter. This circuitry can be operated at either two thyristors in conduction at the same time or three thyristors in conduction. Table 3.1 shows the firing sequence of the thyristors for both

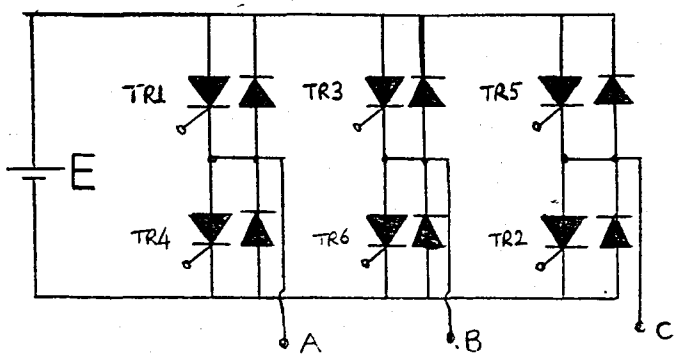


Figure 3.1 Three phase thyristor inverter.

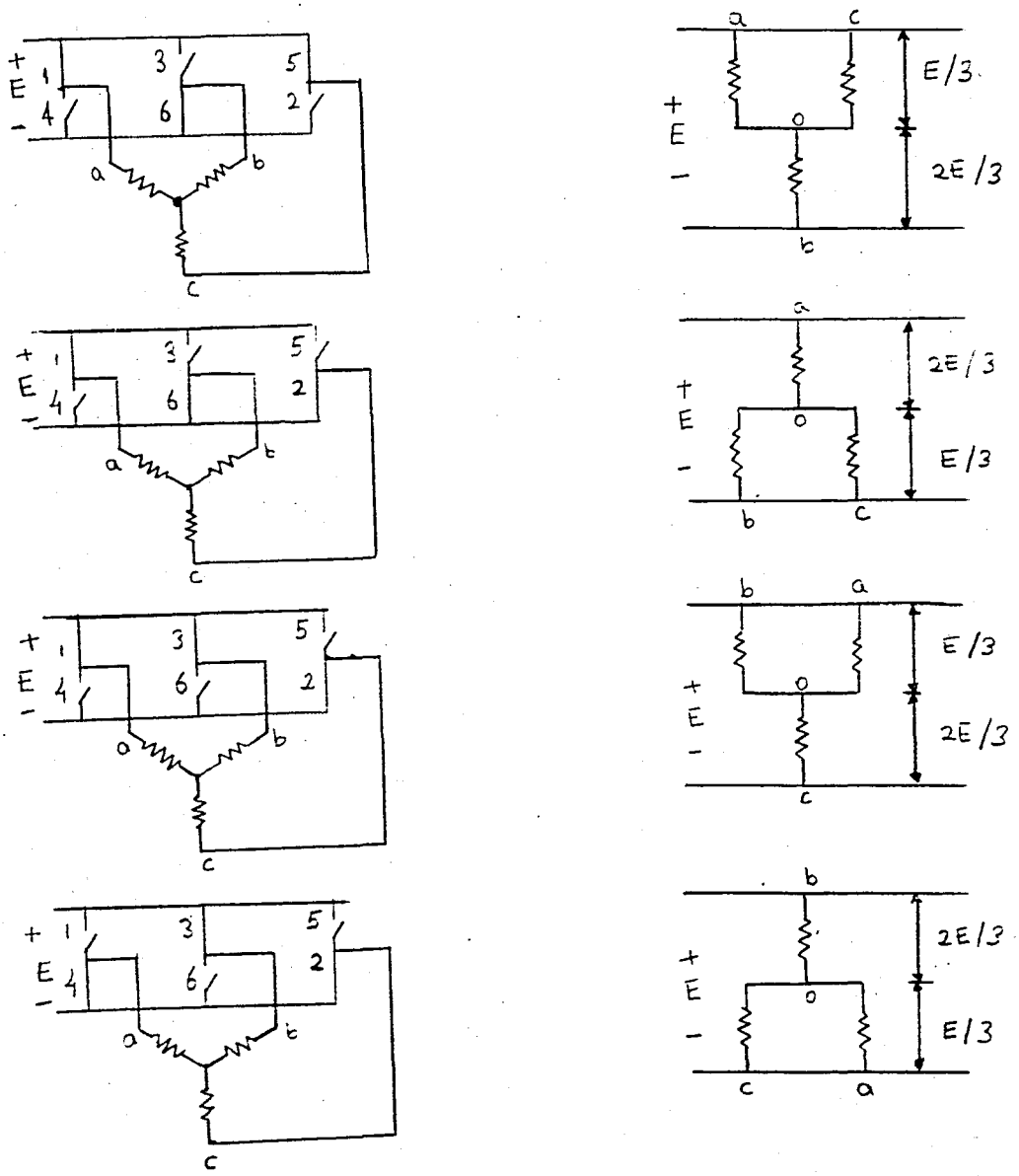


Figure 3.2 Basic operation of three phase inverter.

operation modes.

Operation by keeping three thyristors in conduction is generally preferred to the other since all three terminal voltages are predetermined. In other, only two terminal voltages are known, the third terminal voltage can not be determined.

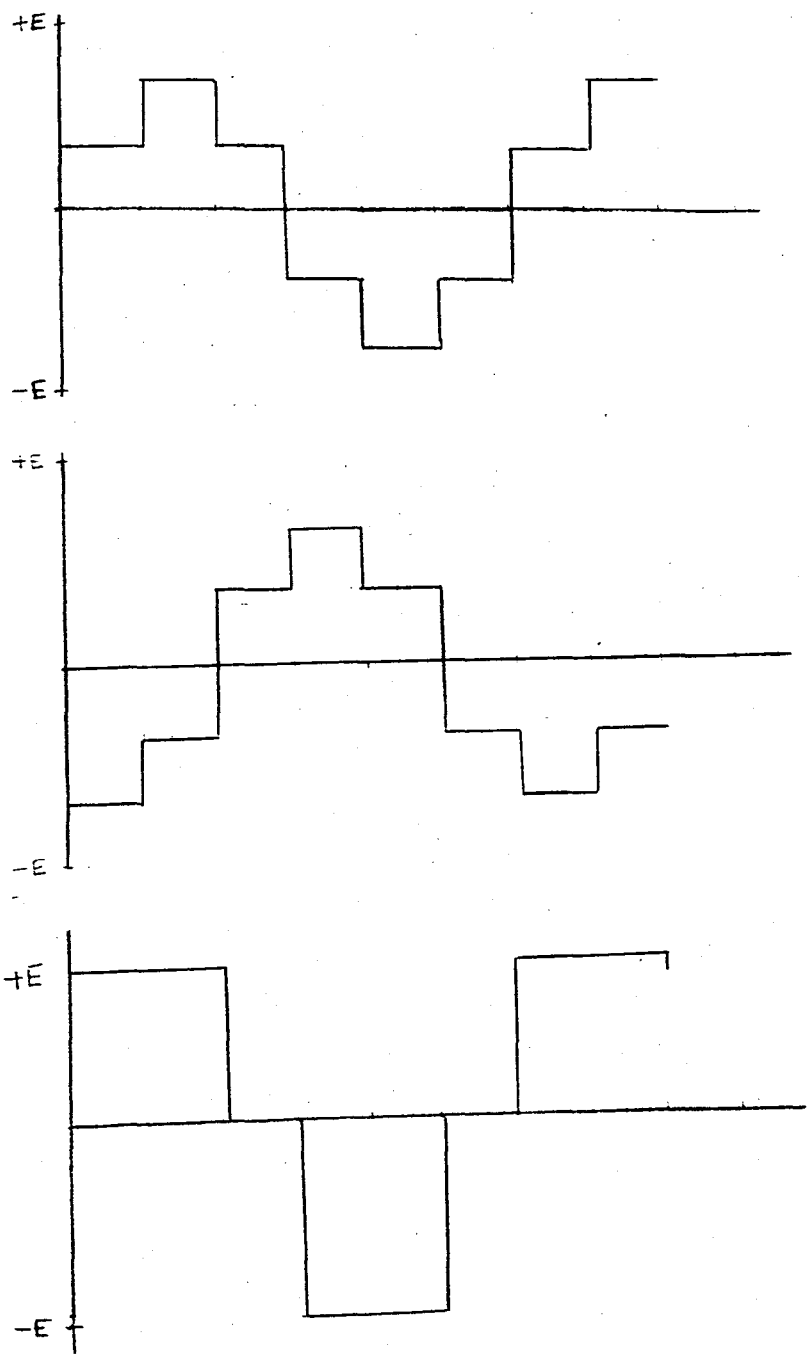
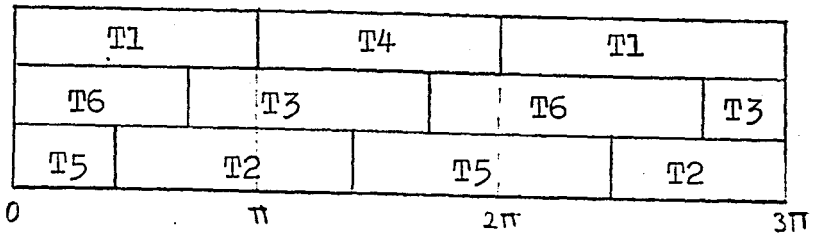
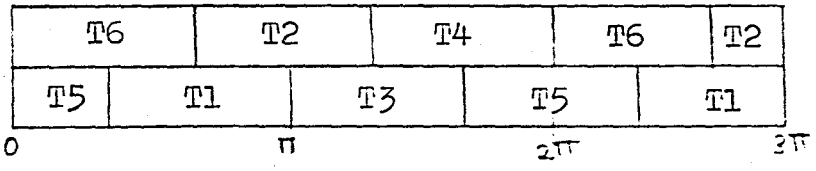


Figure 3.3. Output waveform of the inverter.



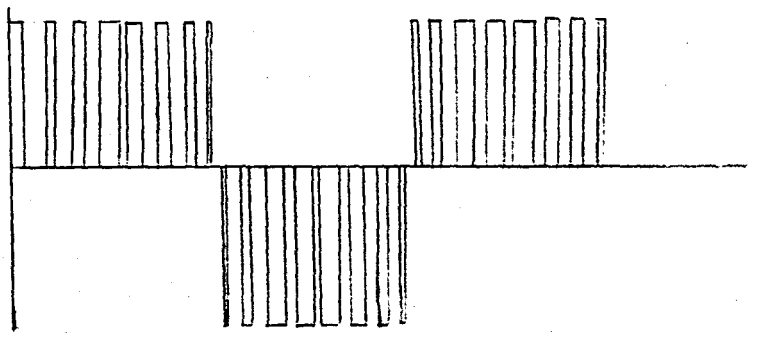
(a) Firing sequence for 180 degrees conduction.



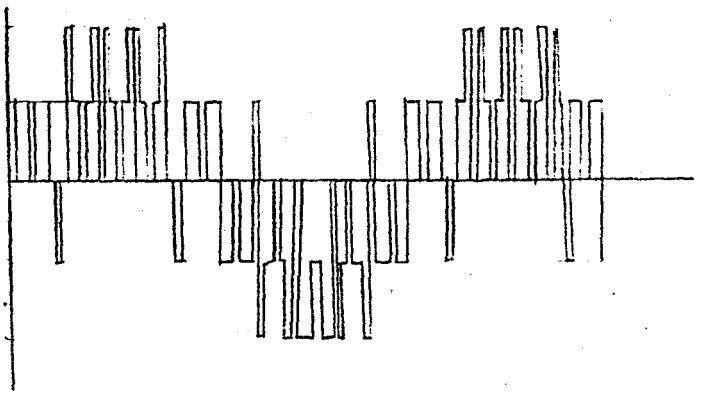
(b) Firing sequence for 120 degrees conduction.
Table 3.1 Firing sequence of the thyristors.

The sequence in which the thyristors of the inverter in Figure 3.1 operated to obtain three phase output waveform is shown in Fig. 3.2. if the thyristors are replaced with switchs and the load is represented by a Y connected set of impedances. Each step in the figure corresponds to 60 degrees on the output waveform. The waveforms of the phase and line voltages are shown in Fig. 3.3. In this mode of operation, relation between variable voltage and variable frequency is achieved by means of a voltage controlled oscillator, that is; when frequency decreases the supply voltage also decreases. However, in the case of PWM

inverter, there is no need to change the supply voltage of the inverter. D.C. Power supply is always constant whatever the output frequency is, the only thing that changes is the fundamental component of the output waveform. In this implementation, the amplitude of the fundamental component is determined by the microcomputer. Figure 3.4 shows the pulse-width modulated line and phase voltage waveforms.



(a) Inverter line voltage.



(b) Inverter phase voltage.
Figure 3.4 Inverter line and phase voltages for a Y connected load.

B. Transistor as Power Control Element in Inverters:

Transistors were considered as low power elements to produce and amplify some signals in analogue and digital systems in 1960s. The need for high power transistors to amplify the signals in the output stages of the audio amplifiers quickened the evolution of the power transistors. Today, power transistors are so improved that they have become alternative power control elements to thyristors due to their fast switching capabilities.

Figure C.3 is the block diagram of the three phase transistor inverter implemented in this thesis. Six power channels provide the required pulses to supply three phase energy to the motor. All power cnannels are identical. As a power transistor, BDX53G Darlington transistors were used. Their maximum collector current is eight amperes and maximum collector- emiter breakdown voltage is 100 volts.Therefore, the external d.c. power supply should be 100 volts and has a current capability of about 10 amperes. Such requirements are best served by a voltage regulated switching supply which minimizes power dissipation. In the design, optic isolators are employed to isolate the power circuit from the microcomputer kit.

IV. MICROCOMPUTER KIT

As the microcomputer of the inverter, an Intel 8085 A based general purpose microcomputer was designed and used to produce commutating pulses and to perform all the control functions of the inverter.

A. Specifications of the System:

A general purpose microcomputer kit contains CPU, volatile and non-volatile memory, keyboard and display peripherial units and serial and parellel ports for user. System is so designed that it can be seperately used as a microcomputer kit. The block diagram of the system is shown in Figure 4.1

Intel 8085 A is an eight bit processor which has seperately serial in and serial out capability directly with accumulator, and five seperate interrupt pins. In the system it is operated at maximum clock frequency; that is 6.144 MHz. and it can be easily replaced with a 10 MHz. version in order to increase the system speed.

The system contains one 2716 EPROM, two 2114 RAMs, one CPU 8085 A, one octal latch, two PPIs 8255 and the subroutines of the control program were stored in EPROM. Total memory of

the system is three kilobytes, which is sufficient for most practical applications. The octal latch is used for demultiplexing the data lines. One of the PPIs is used for communicating with keyboard and display, the other is reserved for user. The keyboard is organized as 4x7 matrix and display is considered as seven segment lines and six selecting lines.

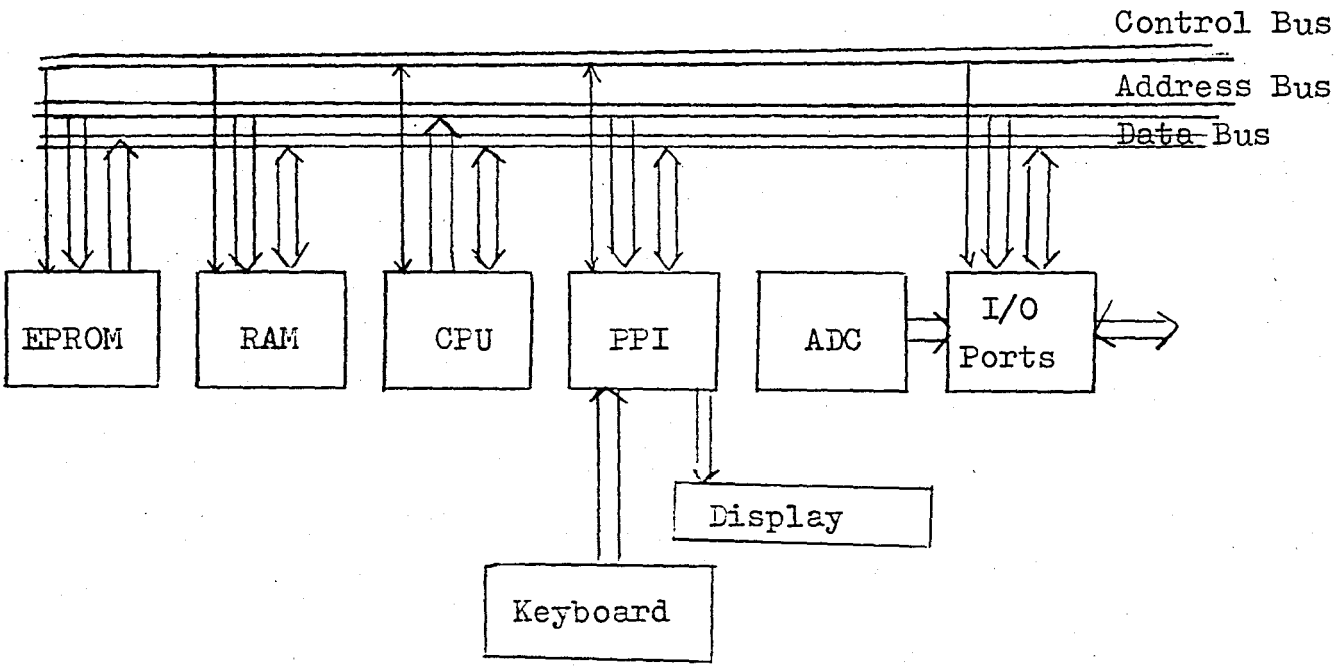


Figure 4.1 Block diagram of the system.

The memory map of the system is as follows:

0000H-07FFH : EPROM Addresses

0800H-0BFFH : RAM Addresses

The port organization of the system is as follows:

00 Display segment address

01 Keyboard row address

02 Upper part of port C is keyboard column address, lower part

is the display select lines

03 Address of control word

04 Port A of user PPI

05 Port B of user PPI

06 Port C of user PPI

07 Control address of user PPI

Since 8255 has two addressing lines, A_2 selects the chips, A_0 and A_1 specifies the address of selected ports.

Systems has 23 key keyboard in addition to reset key. Fig. 4.2 shows the key organisation.

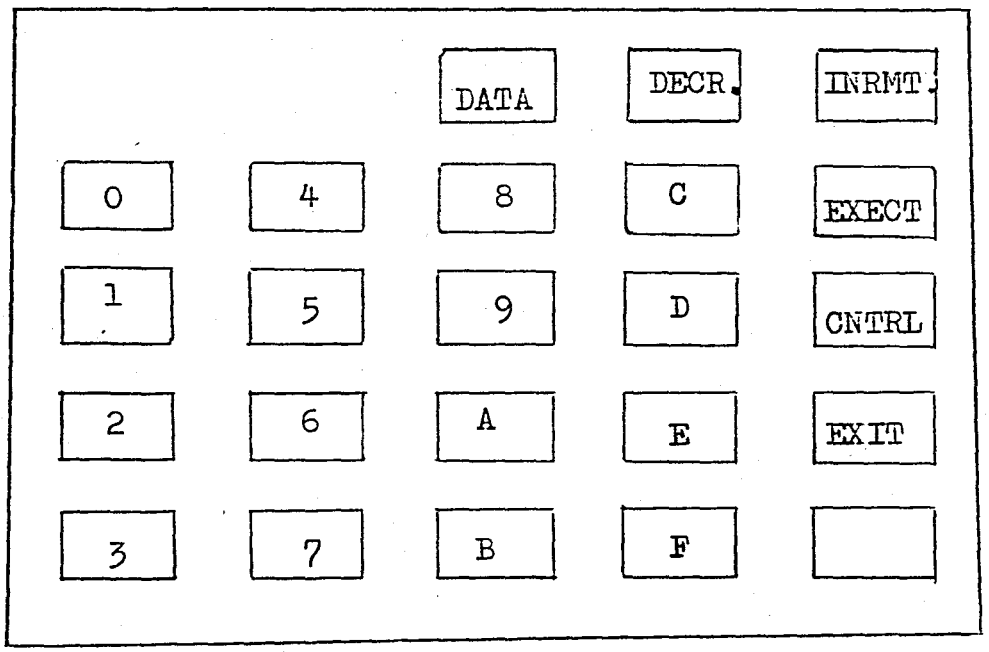


Figure 4.2 Key organisation.

B. Keyboard Organisation:

The keyboard is organised as 16 hexadecimal digits, and five control keys in addition to a reset key. The reset key is an individual push button which is connected directly to the

reset pin of the microprocessor. It gives a hardware reset to the over-all system. When applied, microprocessor goes to the first address location and executes the initialization program of the ports and makes the system ready to get data from the keyboard. Once the reset key has been pushed a slash is displayed at the leftmost display and all the others are blank. This shows that the incoming digit from the keyboard specifies the address to be inputted.

The data key acts as a cursor. When display contains an address and its content, if data key is pushed, slash is displayed. This enables the user to enter the address digits. After the address is entered, if this key is pushed it gives the control of the keyboard to data. In other words, during slash is being displayed if data key is pressed then incoming digits are accepted as data digits until it is pushed again. After address is entered, not only data key, but also increment and decrement keys give the control of digits to data.

If the increment key is pushed, the displayed address is incremented by one, and its contents are displayed. Likewise, it is decremented when the decrement key is pushed.

When the execute key is pressed, the system starts to execute the program from the displayed address location. The system monitor program specifies end instruction as FF in hexadecimal number. After the program is exacuted, system goes to warmstart and displays slash.

The control key is assigned to give the control of the keys to the PWM control application. The flowchart of the monitor program is shown in Fig. 4.3

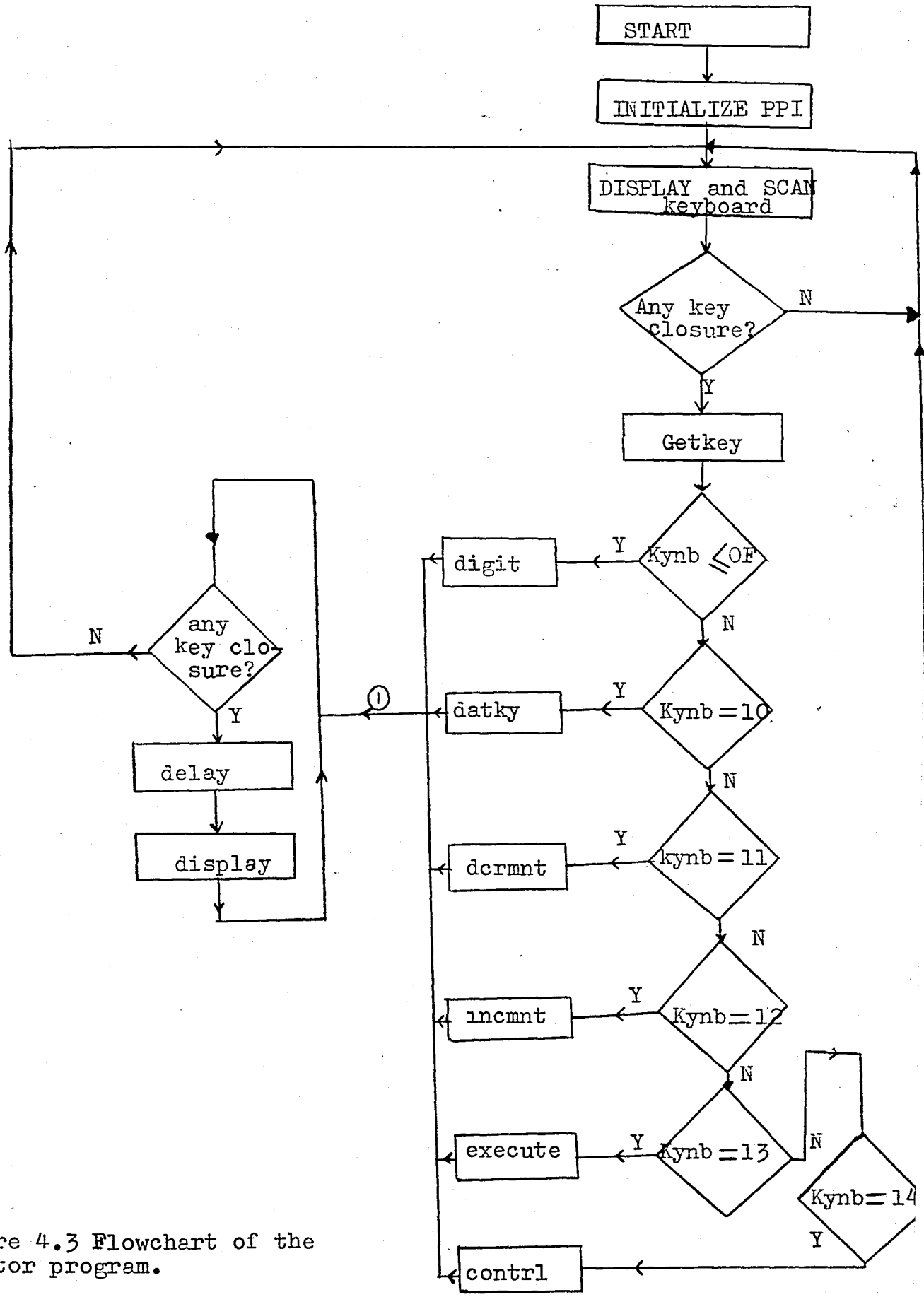


Figure 4.3 Flowchart of the monitor program.

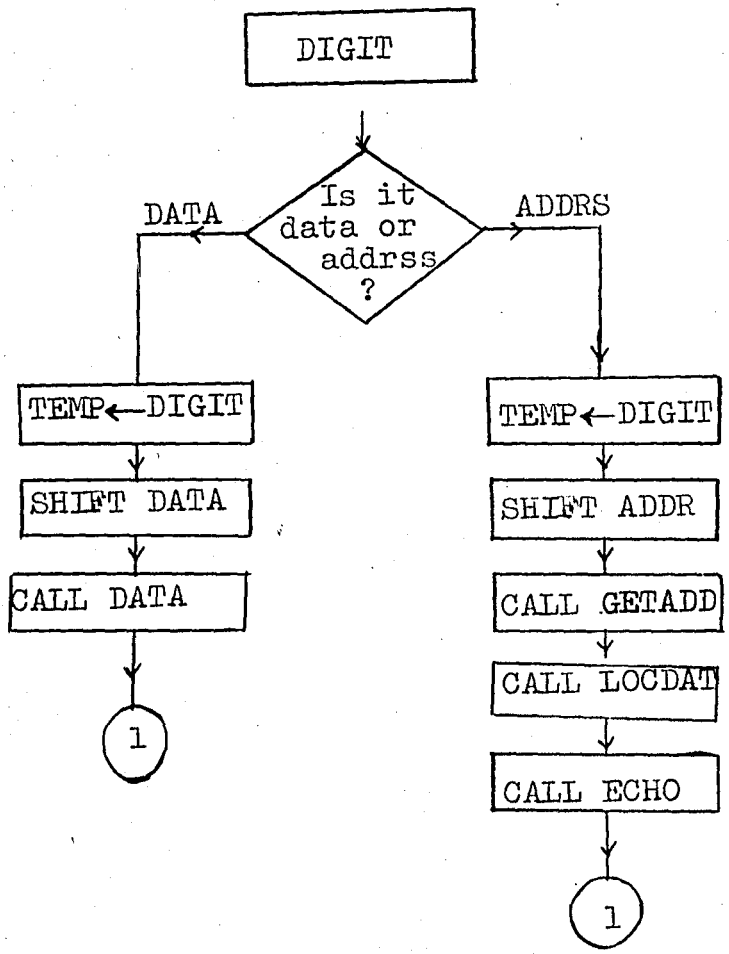


Figure 4.4 Flowchart of the DIGIT

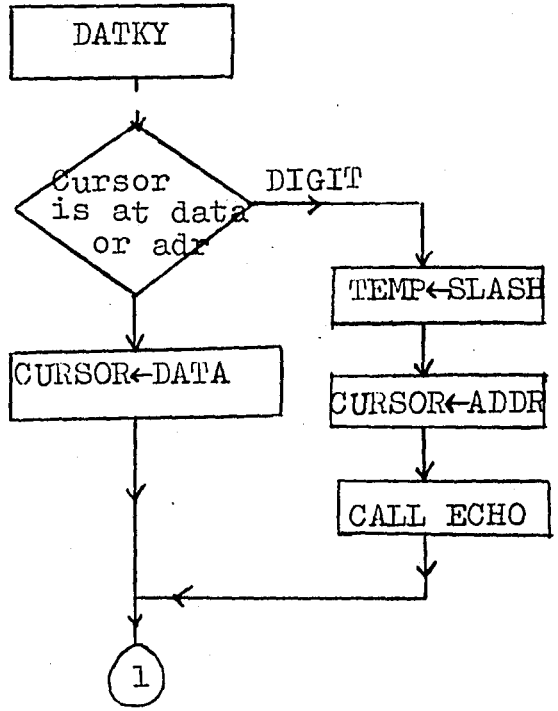


Figure 4.5 Flowchart of DATKY

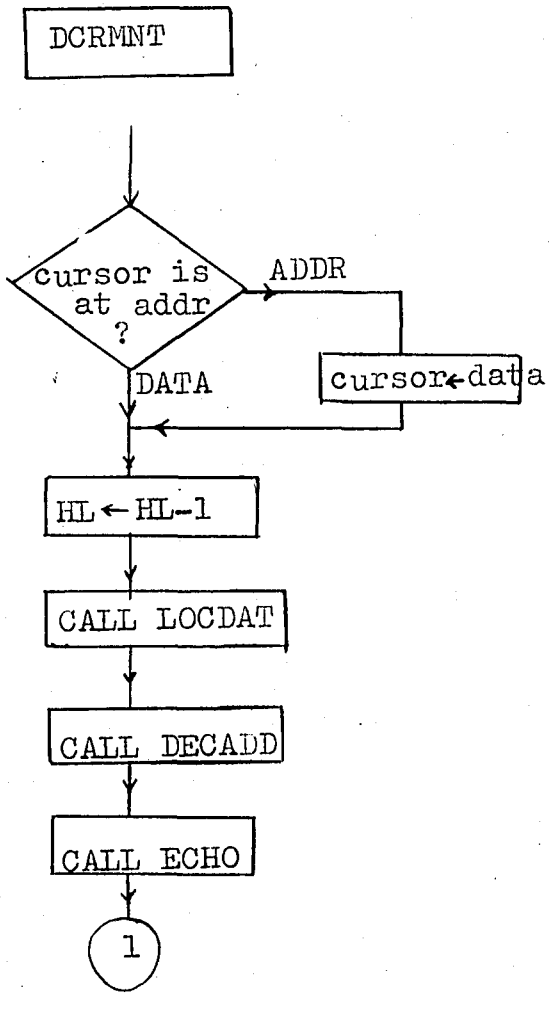


Figure 4.6 Flowchart of DCRMNT

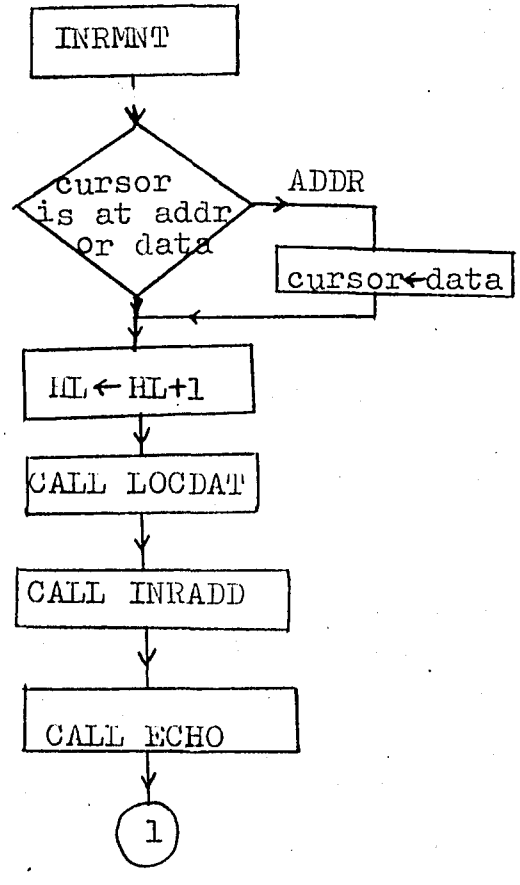


Figure 4.7 Flowchart of INRMNT

V.EXPERIMENTAL RESULTS AND CONCLUSIONS

A. Experimental Results:

The microprocessor based speed control circuitry was designed and built as explained in the above chapters. The connection diagrams of both the microprocessor kit and the inverter are shown in Appendix C.

The system was tested on different induction machines and it was verified that smooth control of speed was possible. The highest operating frequency is limited to 16 Hz. owing to the rating of the Darlington transistors used.

The relation between input voltage and the output frequency is obtained as that shown in Fig. 1.5. Since the modulation index is increased linearly, the linear relation between output frequency and expected stator voltage is achieved.

B. Conclusions:

In the thesis, by using PWM technique, microprocessor based inverter is implemented. The advantages of the system can be stated as follows:

(a) in conventional method, variable voltage is implemented by a controlled rectifier. However, in the PWM technique since the d.c. power supply of the inverter is always constant, Cosϕ is

always unity, therefore reactive power consumption is zero.

(b) since "discreate integer ratio adaptive mode" is used, harmonic minimization is achieved by keeping switching frequency as high as possible at the operating frequency.

(c) since the algorithm is essentially based on a type of modulation, all the system parameters can be changed by software.

It was demonstrated that the PWM technique can control the speed of an induction machine in a 100:1 range.

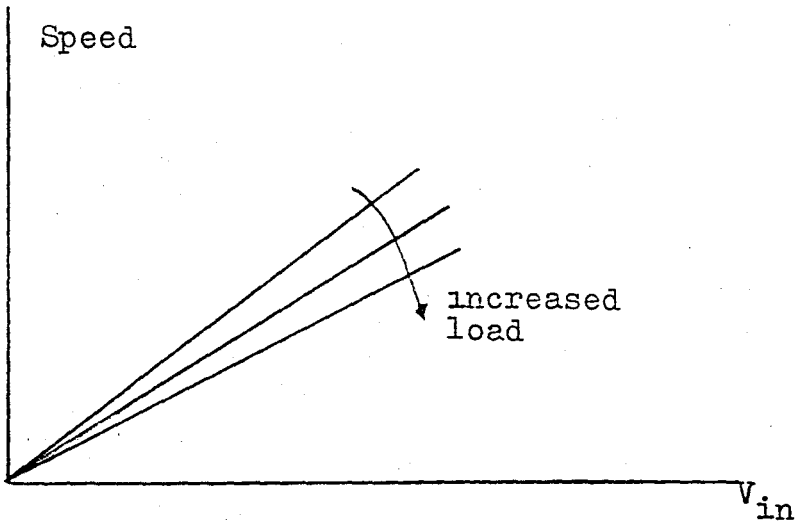


Figure 5.5 The input-output characteristic of an induction motor.

C. Suggestions:

System is essentially implemented as an inverter. If a closed loop operation is desired, it can be achieved with the modifications as explained below.

The ideal input output characteristics of an induction motor are shown in Fig. 5.5.

The system can be operated in closed loop as shown in Fig.5.6. The speed information is obtained from the output of the

tachogenerator. The current information is obtained from the load current.

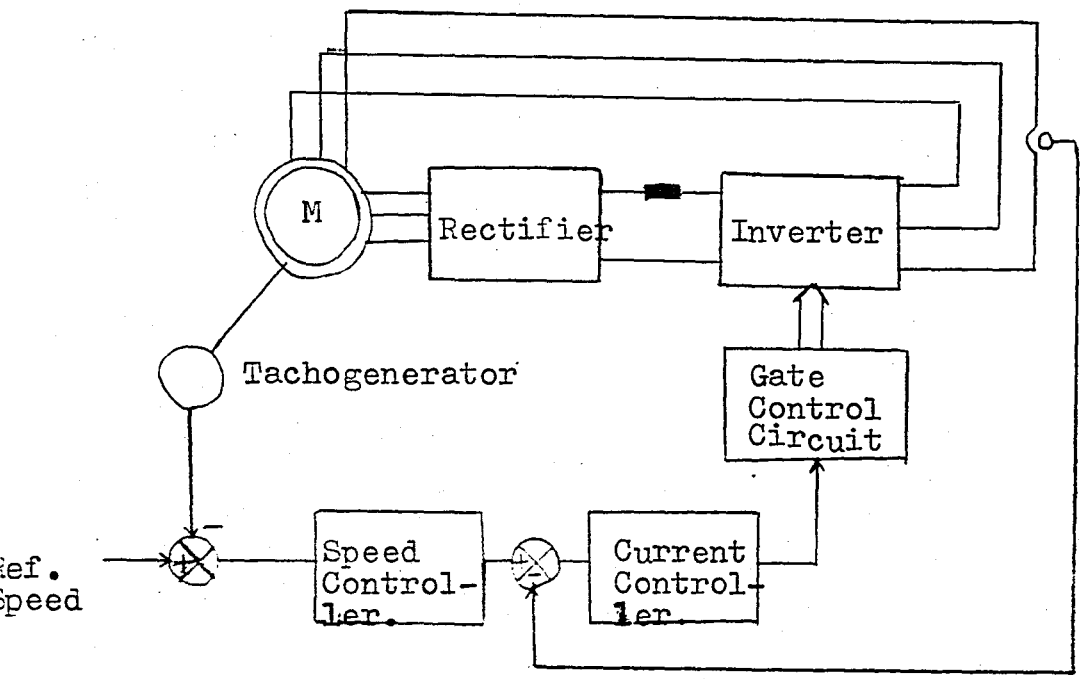


Figure 5.6 Closed loop operation of the induction motor.

In the case of any increase in reference speed, speed controller produces higher current output than the output of the inverter, so the output of the current controller increases. This also increases the modulation index and the output frequency. When the stator current increases, it causes the rotor current and the output speed to increase. Similiar argument holds in the case of any decrease in reference speed.

APPENDIX A

MONITOR PROGRAM OF THE MICROCOMPUTER

```
LOC.   OBJ. CODE   M STMT SOURCE STATEMENT

0000   3E 82        0000          MVI A, CNTWRD ;Initialization of
                    0001                        system PPI, port
                    0002                        A,C output, port
                    0003                        B input.
0002   D3 03        0004          OUT PORTC
0004   31 FF 0B     0005          LXI SP, STK   ;Initialize system
                    0006                        stack.
0007   3E 00        0007  L1      MVI A, 0      ;Initialize display
0009   21 D0 0B     0008          LXI H, TEMP
000C   06 06        0009          MVI B, 06
000E   77           0010  L2      MOV M,A
000F   23           0011          INX H
0010   05           0012          DCR B
0011   C2 0E 00     0013          JNZ L2
0014   3E FD        0014
0016   77           0015          MVI A, FD
0017   23           0016          MOV M,A
0018   06 05        0017          INX H
001A   3E FF        0018          MVI B,5
001C   77           0019          MVI A,FF
                    0020  L3      MOV M,A       ;Load display array
                    0021                        with the code of
001D   23           0022          INX H         slash.
001E   05           0023          DCR B
001F   C3 40 00     0024          JMP NEWADR    ;Continue at NEWADR
0040   C2 1C 00     0025  NEWADR  JNZ L3
0043   3E 00        0026          MVI A,0
0045   32 DE 0B     0027          STA TEMPP
                    0028  ;-------------------------------------------
                    0029  DISPLAY:
                    0030  continously refreshs the seven segment
                    0031  displays, and between two refreshings,
                    0032  checks whether any key closure occurs
                    0033  or not. In the case of closure, stops
                          refreshing and gets key value.
```

```
LOC.   OBJ. CODE     M STMT SOURCE STATEMENT

0048   1E 70         0034  DSPLY   MVI E,70
004A   21 D6 0B      0035          LXI H,ARRAY
004D   7B            0036  L4      MOV A,E
004E   D6 10         0037          SUI 10
0050   CA 3A 01      0038          JZ ENA
0053   D3 02         0039          OUT PORTC
0055   5F            0040          MOV E,A
0056   7E            0041          MOV A,M
0057   D3 00         0042          OUT PORTA
0059   3E 02         0043          MVI A,2        ;delay for refresh.
005B   06 BC         0044  L5      MVI B,BC
005D   05            0045  L6      DCR B
005E   C2 5D 00      0046          JNZ L6
0061   3D            0047          DCR A
0062   C2 5B 00      0048          JNZ L5
0065   3E FF         0049          MVI A,FF       ;blanks display.
0067   D3 00         0050          OUT PORTA
0069   C3 30 01      0051          JMP DEVAM      ;continue at DEVAM
                     0052 ;_____________________________________________
                     0053  LOCDAT:
                     0054 ;gets the content of the address stored in
                     0055 ;HL, breaks it into two digits, and stores
                     0056 ;them into TEMP4 and TEMP5. Destroys reg.
                     0057 ;A,B, and HL.
0070   7E            0058  LOCDAT  MOV A,M
0071   47            0059          MOV B,A
0072   07            0060          RLC
0073   07            0061          RLC
0074   07            0062          RLC
0075   07            0063          RLC
0076   E6 0F         0064          ANI 0F
0078   21 D4 0B      0065          LXI H,TEMP4
007B   77            0066          MOV M,A
007C   E6 0F         0067          ANI 0F
007E   23            0068          INX H
007F   77            0069          MOV M,A
0080   C9            0070          RET
                     0071 _____________________________________________
                     0072 ;DATA:
                     0073 ;gets the contents of TEMP4 and TEMP5, forms
                     0074 ;them as a datum, and stores it into address
                     0075 ;stored in HL. Destroys reg. A,HL.
0082   21 D4 0B      0076  DATA    LXI H,0BD4
0085   7E            0077          MOV A,M
0086   07            0078          RLC
0087   07            0079          RLC
0088   07            0080          RLC
0089   07            0081          RLC
008A   23            0082          INX H
008B   86            0083          ADD M
008C   2A DC 0B      0084          LHLD 0BDC
008F   77            0085          MOV M,A
0090   C9_           0086          RET
```

```
LOC.    OBJ. CODE       M STMT SOURCE STATEMENT

                        0087 ;INRADD:
                        0088 ;increments the address stored in TEMP
                        0089 ;locations. Format is as follows:
                        0090 ;  TEMP : contains MSD of the address
                        0091 ;  TEMP1: contains one of the digits
                        0092 ;  TEMP2:     "     "   "   "     "
                        0093 ;  TEMP3: contains LSD of the address
                        0094 ;  TEMP4: contains MSD of the data
                        0095 ;  TEMP5: contains LSD of the data.
                        0096 ;destroys reg. A,B,H,L.
0091    06 00           0097 ; INRADD MVI B,0
0093    21 D3 0B        0098          LXI H,TEMP3
0096    3E 0F           0099          MVI A,0F
0098    BE              0100          CMP M
0099    CA 9E 00        0101          JZ L1
009C    34              0102          INR M
009D    C9              0103          RET
009E    2B              0104   L1     DCX H
009F    BE              0105          CMP M
00A0    CA A7 00        0106          JZ L2
00A3    34              0107          INR M
00A4    23              0108          INX H
00A5    70              0109          MOV M,B
00A6    C9              0110          RET
00A7    2B              0111   L2     DCX H
00A8    34              0112          INR M
00A9    23              0113          INX H
00AA    70              0114          MOV M,B
00AB    23              0115          INX H
00AC    70              0116          MOV M,B
00AD    C9              0117          RET
                        0118:-----------------------------------------
                        0119;DECADD:
                        0120;decrements the address stored in TEMP
                        0121;locations. Destroys reg. A,B,H and L.
00AF    06 0F           0122   DECADD MVI B,0F
00B1    21 D3 0B        0123          LXI H,0BD3
00B4    3E 00           0124          MVI A,0
00B6    BE              0125          CMP M
00B7    CA BC 00        0126          JZ L1
00BA    35              0127          DCR M
00BB    C9              0128          RET
00BC    2B              0129   L1     DCX H
00BD    BE              0130          CMP M
00BE    CA C5 00        0131          JZ L2
00C1    35              0132          DCR M
00C2    23              0133          INX H
00C3    70              0134          MOV M,B
00C4    C9              0135          RET
00C5    2B              0136   L2     DCX H
00C6    35              0137          DCR M
00C7    23              0138          INX H
```

```
LOC.   OBJ. CODE     M STMT SOURCE STATEMENT

00C8   70              0139            MOV M,B
00C9   23              0140            INX H
00CA   70              0141            MOV M,B
00CB   C9              0142            RET
                       0143;-----------------------------------------------
                       0144;ECHO:
                       0145;converts the digits stored in TEMP
                       0146;locations to the seven segment display
                       0147;code,and stores into ARRAY locations.
                       0148;Destroys reg.A,B,C,D,E,H,L.
00CC   21 D0 0B        0149;  ECHO     LXI H,TEMP
00CF   01 D6 0B        0150            LXI B,ARRAY
00D2   16 06           0151            MVI D,6
00D4   5E              0152   L1       MOV E,M
00D5   E5              0153            PUSH H
00D6   3E 1D           0154            MVI A,1D
00D8   83              0155            ADD E
00D9   6F              0156            MOV L,A
00DA   26 01           0157            MVI H,1
00DC   7E              0158            MOV A,M
00DD   02              0159            STAX
00DE   E1              0160            POP H
00DF   23              0161            INX H
00E0   03              0162            INX B
00E1   15              0163            DCR D
00E2   C2 D4 00        0164            JNZ L1
00E5   C9              0165            RET
                       0166;-----------------------------------------------
                       0167;GETADD:
                       0168;combines the digits stored in TEMP
                       0169;locations and forms them as an address
                       0170;and puts the result into HL.
                       0171;Destroys reg. A,B,C,H,L.
00E6   21 D0 0B        0172   GETADD   LXI H,TEMP
00E9   0E 02           0173            MVI C,2
00EB   7E              0174   L2       MOV A,M
00EC   07              0175            RLC
00ED   07              0176            RLC
00EE   07              0177            RLC
00EF   07              0178            RLC
00F0   23              0179            INX H
00F1   46              0180            MOV B,M
00F2   80              0181            ADD B
00F3   0D              0182            DCR C
00F4   CA FC 00        0183            JZ L1
00F7   F5              0184            PUSH PSW
00F8   23              0185            INX H
00F9   C3 EB 00        0186            JMP L2
00FC   6F              0187   L1       MOV L,A
00FD   F1              0188            POP PSW
00FE   67              0189            MOV H,A
00FF   C9              0190            RET
```

```
LOC.   OBJ. CODE    M STMT SOURCE STATEMENT

0130   3E 21        0191   DEVAM   MVI A,21      ;delay for blank time
0132   3D           0192   L7      DCR A
0133   C2 32 01     0193           JNZ L7
0136   23           0194           INX H
0137   C3 4D 00     0195           JMP L4
013A   DB 01        0196   ENA     IN PORTB      ;checks whether any key
                    0197                          closure.
013C   E6 7F        0198           ANI 01        ;masks unused bit.
013E   FE 7F        0199           CPI 7F
0140   CA 48 00     0200           JZ DSPLY      ;jumps in the case of no
                    0201                          closure.
0143   CD 06 02     0202           CALL DDLY     ;calls delay subroutine
                    0203                          for debounce.
0146   DB 01        0204   KEY     IN PORTB
0148   E6 7F        0205           ANI 7F
014A   FE 7F        0206           CPI 7F
014C   CA 48 00     0207           JZ DSPLY      ;continues to refreshing
                    0208                          if key is released.
014F   06 00        0209           MVI B,0
0151   1E FE        0210           MVI E,FE      ;scans row, gets column
                    0211                          value, if gets a zero
                    0212                          stops scanning.
0153   16 04        0213           MVI D,4
0155   7B           0214   FROW    MOV A,E
0156   D3 02        0215           OUT PORTC
0158   07           0216           RLC
0159   5F           0218           MOV E,A
015A   DB 01        0219           IN PORTB
015C   E6 7F        0220           ANI 7F
015E   FE 7F        0221           CPI 7F
0160   C2 6E 01     0222           JNZ FCOL
0163   78           0223           MOV A,B
0164   C6 07        0224           ADI 07
0166   47           0225           MOV B,A
0167   15           0226           DCR D
0168   C2 55 01     0227           JNZ FROW
016B   C3 E5 01     0228           JMP KEY
016E   1F           0229   FCOL    RAR
016F   D2 76 01     0230           JNC DONE
0172   04           0231           INR B
0173   C3 6E 01     0232           JMP FCOL
0176   26 01        0233   DONE    MVI H,01      ;key number in reg.B
0178   68           0234           MOV L,B
0179   46           0235           MOV B,M       ;entered digit in reg.B
017A   3E 10        0236           MVI A,10
017C   B8           0237           CMP B
017D   F2 A6 01     0238           JP DIGIT      ;jumps if a digit is
                    0239                          entered.
0180   3C           0240           INR A
0181   B8           0241           CMP B
0182   CA 2F 02     0242           JZ DTKY       ;jumps if data key is
                    0243                          entered.
```

```
LOC.    OBJ. CODE    M STMT SOURCE STATEMENT

0185    3C           0244          INR A
0186    B8           0245          CMP B
0187    CA 47 02     0246          JZ DECRM      ;if decrement key is
                     0247                        entered, it jumps.
018A    3C           0248          INR A
018B    B8           0249          CMP B
018C    CA 66 02     0250          JZ INCRM      ;jumps if increment key
                     0251                        is entered.
018F    3C           0252          INR A
0190    B8           0253          CMP B
0191    CA 85 02     0254          JZ EXECT      ;starts to execute the
                     0255                        user program.
0194    3C           0256          INR A
0195    B8           0257          CMP B
0196    CA 91 02     0258          JZ COTRL      ;starts to execute the
                     0259                        PWM control program.
0199    3C           0260          INR A
019A    B8           0261          CMP B
019B    CA 00 00     0262          JZ EXIT       ;jumps to the warmstart
                     0263                        waits a new instruction.
019E    3C           0264          INR A
019F    B8           0265          CMP B
01A0    CA 00 00     0266          JZ ERROR      ;returns to monitor.
01A3    C3 E5 01     0267          JMP SON       ;means key is released.
01A6    3A DE 0B     0268  DIGIT   LDA OBDE
01A9    FE 00        0269          CPI 00
01AB    C2 D0 01     0270          JNZ ORA       ;jumps if data digits ar
                     0271                        entered.
01AE    21 DE 0B     0272          LXI H,OBDE
01B1    34           0273          INR M
01B2    21 D1 0B     0274  LL      LXI H,TEMP1   ;starts to shift the
                     0275                        address digits.
01B5    7E           0276          MOV A,M
01B6    23           0277          INX H
01B7    4E           0278          MOV C,M
01B8    23           0279          INX H
01B9    56           0280          MOV D,M
01BA    70           0281          MOV M,B
01BB    2B           0282          DCX H
01BC    72           0283          MOV M,D
01BD    2B           0284          DCX H
01BE    71           0285          MOV M,C
01BF    2B           0286          DCX H
01C0    77           0287          MOV M,A       ;address digits are
                     0289                        shifted in the TEMPs.
01C1    CD E6 00     0290          CALL GETADD   ;shifted address are
                     0291                        loaded into HL.
01C4    22 DC 0B     0292          SHLD TEMPP
01C7    CD 70 00     0293  LL1     CALL LOCDAT   ;TEMP4 and TEMP5 are loa
                     0294                        with the content of HL.
01CA    CD CC 00     0295  LLX     CALL ECHO     ;TEMPs are converted to
                     0296                        seven segment codes.
```

```
LOC.    OBJ. CODE    M STMT SOURCE STATEMENT

01CD    C3 E5 01     0296           JMP SON
01D0    FE 01        0297   ORA     CPI 01
01D2    CA B2 01     0298           JZ LL
01D5    21 D5 0B     0299           LXI H,TEMP5
01D8    7E           0300           MOV A,M
01D9    70           0301           MOV M,B
01DA    2B           0302           DCX H
01DB    77           0303           MOV M,A
01DC    CD 82 00     0304           CALL DATA
01DF    2A DC 0B     0305           LHLD 0BDC
01E2    C3 C7 01     0306           JMP LL1
01E5    DB 01        0307   SON     IN PORTB      ;waits until the key
                     0308                         is released.
01E7    E6 7F        0309           ANI 7F
01E9    FE 7F        0310           CPI 7F
01EB    C2 00 02     0311           JNZ LL3
01EE    CD 06 02     0312           CALL DDLY     ;delay for debounce.
01F1    CD 06 02     0313           CALL DDLY
01F4    DB 01        0314           IN PORTB      ;checks whether key is
                     0315                         released.
01F6    E6 7F        0316           ANI 7F
01F8    FE 7F        0317           CPI 7F
01FA    CA 48 00     0318           JZ DSPLY      ;jumps if key is release
01FD    C3 E5 01     0319           JMP SON
0200    CD 06 02     0320   LL3     CALL DDLY
0203    C3 E5 01     0321           JMP SON
022F    21 DE 0B     0322   DATKY   LXI H,0BDE    ;check if cursor is at
                     0323                         data or address digits.
0232    3E 00        0324           MVI A,00
0234    BE           0325           CMP M
0235    CA E5 01     0326           JZ SON
0238    3C           0327           INR A
0239    BE           0328           CMP M
023A    CA 42 02     0329           JZ LL4
023D    3C           0330           INR A
023E    77           0331           MOV M,A
023F    C3 E5 01     0332           JMP SON
0242    35           0333   LL4     DCR M
0243    35           0334           DCR M
0244    C3 00 00     0335           JMP ERROR
0247    21 DE 0B     0336   DCRMNT  LXI H,0BDE    ;decrements the current
                     0337                         address and displays th
                     0338                         content.
024A    3E 00        0339           MVI A,0
024C    BE           0340           CMP M
024D    CA E5 01     0341           JZ SON
0250    3C           0342           INR A
0251    BE           0343           CMP M
0252    C2 56 02     0344           JNZ LL5
0255    34           0345           INR M
0256    2A DC 0B     0346   LL5     LHLD 0BDC
0259    2B           0347           DCX H
025A    22 DC 0B     0348           SHLD 0BDC
```

```
LOC.    OBJ. CODE    M STMT SOURCE STATEMENT

025D    CD 70 00     0349           CALL LOCDAT
0260    CD AF 00     0350           CALL DECADD
0263    C3 CA 01     0351           JMP LLX
0266    21 DE 0B     0352  INCRM    LXI H,OBDE      ;increments the curre
                     0353                           address and displays
                     0354                           its content.
0269    3E 00        0355           MVI A,0
026B    BE           0356           CMP M
026C    CA E5 01     0357           JZ SON
026F    3C           0358           INR A
0270    BE           0359           CMP M
0271    C2 75 02     0360           JNZ LLY
0274    34           0361           INR M
0275    2A DC 0B     0362  LLY      LHLD OBDC
0278    23           0363           INX H
0279    22 DC 0B     0364           SHLD OBDC
027C    CD 70 00     0365           CALL LOCDAT
027F    CD 91 00     0366           CALL INRADD
0282    C3 CA 01     0367           JMP LLX
0285    3A DE 0B     0368  EXECT    LDA OBDE        ;executes the user
                     0369                           program from the
                     0370                           displayed address.
0288    FE 00        0371           CPI 0
028A    CA E5 01     0372           JZ SON
028D    CD E6 00     0373           CALL GETADD
0290    E9           0374           PCHL
                     0375  ---------------------------------------------
                     0376  ;DDLY:
                     0377  ;refreshs the display  10.6 msec. Destroys
                     0378  ;reg.A,B,D,H,L.
0206    06 70        0379   DDLY    MVI B,70
0208    21 D6 0B     0380           LXI H,ARRAY
020B    78           0381   L4      MOV A,B
020C    D6 10        0382           SUI 10
020E    C8           0383           RZ
020F    D3 02        0384           OUT PORTC
0211    47           0385           MOV B,A
0212    7E           0386           MOV A,M
0213    D3 00        0387           OUT PORTA
0215    3E 03        0388           MVI A,3
0217    16 F1        0389   L2      MVI D,F1
0219    15           0390   L1      DCR D
021A    C2 19 02     0391           JNZ L1
021D    3D           0392           DCR A
021E    C2 17 02     0393           JNZ L2
0221    3E FF        0394           MVI A,FF
0223    D3 00        0395           OUT PORTA
0225    3E 40        0396           MVI A,40
0227    3D           0397   L3      DCR A
0228    C2 27 02     0398           JNZ L3
022B    23           0399           INX H
022C    C3 0B 02     0400           JMP L4
```

```
LOC.  OBJ. CODE  M  STMT  SOURCE STATEMENT

                    0401    ;Key-position-code to key-internal-code
                    0402     conversion table.
0100  15            0403    DEFB        CONTROL KEY
0101  16            0404    DEFB        UNUSED
0102  12            0405    DEFB        DECREMENT KEY
0103  17            0406    DEFB        EXIT KEY
0104  0F            0407    DEFB        HEX-F
0105  13            0408    DEFB        INCREMENT KEY
0106  14            0409    DEFB        EXECUTE KEY
0107  FF            0410    DEFB        UNUSED
0108  00            0411    DEFB        HEX-0
0109  01            0412    DEFB        HEX-1
010A  03            0413    DEFB        HEX-3
010B  FF            0414    DEFB        UNUSED
010C  FF            0415    DEFB        UNUSED
010D  02            0416    DEFB        HEX-2
010E  0D            0417    DEFB        HEX-D
010F  04            0418    DEFB        HEX-4
0110  11            0419    DEFB        DATA KEY
0111  FF            0420    DEFB        UNUSED
0112  FF            0421    DEFB        UNUSED
0113  08            0422    DEFB        HEX-8
0114  0C            0423    DEFB        HEX-C
0115  0A            0424    DEFB        HEX-A
0116  0E            0425    DEFB        HEX-E
0117  05            0426    DEFB        HEX-5
0118  07            0427    DEFB        HEX-7
0119  0B            0428    DEFB        HEX-B
011A  09            0429    DEFB        HEX-9
011B  06            0430    DEFB        HEX-6
                    0431
                    0432
                    0433    ;Display code convertion table.
011D  02            0434    DEFB        HEX-0
011E  5B            0435    DEFB        HEX-1
011F  21            0436    DEFB        HEX-2
0120  11            0437    DEFB        HEX-3
0121  58            0438    DEFB        HEX-4
0122  14            0439    DEFB        HEX-5
0123  04            0440    DEFB        HEX-6
0124  1B            0441    DEFB        HEX-7
0125  00            0442    DEFB        HEX-8
0126  10            0443    DEFB        HEX-9
0127  08            0444    DEFB        HEX-A
0128  44            0445    DEFB        HEX-B
0129  26            0446    DEFB        HEX-C
012A  41            0447    DEFB        HEX-D
012B  24            0448    DEFB        HEX-E
012C  2C            0449    DEFB        HEX-F
```

APPENDIX B

SOFTWARE OF THE PWM INVERTER

```
LOC.   OBJ. CODE   M STMT SOURCE STATEMENT

                   0000;MULTPLY:
                   0001;multiplies modulation index by sampled and
                   0002;held sine values. Result in reg. HL.
                   0003;Destroys regs. A,B,C,D,E,H,L.
0291   21 00 00    0004  MULTPLY LXI H,0
0294   16 00       0005        MVI D,0
0296   0E 08       0006        MVI C,8      ;initialize regs.
0298   78          0007  L1    MOV A,B
0299   0F          0008        RRC
029A   47          0009        MOV B,A
029B   D2 9F 02    0010        JNC L2
029E   19          0011        DAD D
029F   7B          0012  L2    MOV A,E
02A0   17          0013        RAL
02A1   5F          0014        MOV E,A
02A2   7A          0015        MOV A,D
02A3   17          0016        RAL
02A4   57          0017        MOV D,A
02A5   0D          0018        DCR C
02A6   C2 98 02    0019        JNZ L1
02A9   0E 05       0020        MVI C,05     ;result in HL.
02AB   7C          0021        MOV A,H      ;determine decimal poi
02AC   37          0022  L11   STC
02AD   3F          0023        CMC
02AE   1F          0024        RAR
02AF   0D          0025        DCR C
02B0   C2 AC 02    0026        JNZ L11
02B3   D0          0027        RNC
02B4   3C          0028        INR A
02B5   C9          0029        RET
                   0030;-------------------------------------------
                   0031; PRFM :
                   0032;performs all necessary multiplications by
                   0033;using subroutine MULTPLY and stores the
                   0034;results as look-up table in memory location
                   0035;labelled TMP.
```

```
LOC.    OBJ. CODE    M STMT SOURCE STATEMENT

                     0036 ;TMP address locations:
                     0037           TMP1   -0800H
                     0038           TMP200 -08CFH
0300    3E 03        0039 PRFM      MVI A,NBR
0302    06 F5        0040           MVI B,MODX1      ;loads it with M valu
0304    11 00 08     0041           LXI D,TMP1
0307    21 C5 07     0042 L5        LXI H,TBLE       ;loads the address
                     0043                            of the Sin values
                     0044                            look-up table.
030A    0E 0F        0045           MVI C,SWNBR      ;loads reg C with the
                     0046                            number of Sin values
                     0047                            corresponding to
                     0048                            R=60.
030C    F5           0049           PUSH PSW         ;save registers.
030D    E5           0050 L1        PUSH H
030E    C5           0051           PUSH B
030F    D5           0052           PUSH D
0310    5E           0053           MOV E,M          ;loads reg.E with the
                     0054                            first Sine value.
0311    CD 91 02     0055           CALL MULTPLY
0314    D1           0056           POP D
0315    C1           0057           POP B
0316    E1           0058           POP H
0317    12           0059           STAX             ;stores the result
                     0060                            into TMP.
0318    13           0061           INX D
0319    23           0062           INX H
031A    0D           0063           DCR C
031B    C2 0D 03     0064           JNZ L1
031E    F1           0065           POP PSW
031F    3D           0066           DCR A
0320    CA 35 03     0067           JZ L3
0323    3D           0068           DCR A
0324    CA 2E 03     0069           JZ L4
0327    3E 02        0070           MVI A,NBR1
0329    06 DE        0071           MVI B,MODX2      ;loads the other M
                     0072                            value.
032B    C3 07 03     0073           JMP L5
032E    3E 01        0074 L4        MVI A,NBR2
0330    06 C9        0075           MVI B,MODX3
0332    C3 07 03     0076           JMP L5
0335    3E 03        0077 L3        MVI A,NBR3
0337    06 B0        0078           MVI B,MODX4
0339    21 D4 07     0079 L55       LXI H,TBLE1      ;loads HL with the
                     0080                            beginning of addrs.
                     0081                            into that Sin value
                     0082                            for R=80 are store
033C    0E 14        0083           MVI C,SWNBR1     ;loads reg.C with th
                     0084                            number of Sin value
                     0085                            for R=80.
033E    F5           0086           PUSH PSW         ;save registers.
033F    E5           0087 L11       PUSH H
0340    C5           0088           PUSH B
```

```
LOC.   OBJ. CODE    M STMT SOURCE STATEMENT

0341   D5           0089          PUSH D
0342   5E           0090          MOV E,M          ;loads reg.E with the
                    0091                            first Sin value
                    0092                            corresponding to
                    0093                            R=80.
0343   CD 91 02     0094          CALL MULTPLY
0346   D1           0095          POP D
0347   C1           0096          POP B
0348   E1           0097          POP H
0349   12           0098          STAX
034A   13           0099          INX D
034B   23           0100          INX H
034C   0D           0101          DCR C
034D   C2 3F 03     0102          JNZ L11
0350   F1           0103          POP PSW
0351   3D           0104          DCR A
0352   CA 67 03     0105          JZ L33
0355   3D           0106          DCR A
0356   CA 60 03     0107          JZ L44
0359   3E 02        0108          MVI A,NBR4
035B   06 99        0109          MVI B,MODX5
035D   C3 39 03     0110          JMP L55
0360   3E 01        0111  L44     MVI A,NBR5
0362   06 99        0112          MVI B,MODX6
0364   C3 39 03     0113          JMP L55
0367   3E 04        0114  L33     MVI A,NBR6
0369   06 6B        0115          MVI B,MODX7
036B   21 E8 07     0116          LXI H,TBLE2      ;loads HL with the
                    0117                            beginning of addrs.
                    0118                            of look-up table
                    0119                            into that Sin values
                    0120                            for R=96 are stored.
036E   0E 18        0121  L555    MVI C,SWNBR2     ;loads regC with the
                    0122                            number of Sin values
0370   F5           0123          PUSH PSW
0371   E5           0124  L111    PUSH H
0372   C5           0125          PUSH B
0373   D5           0126          PUSH D
0374   5E           0127          MOV E,M          ;loads regE with the
                    0128                            first Sin value
                    0129                            corresponding to
                    0130                            R=96.
0375   CD 91 02     0131          CALL MULTPLY
0378   D1           0132          POP D
0379   C1           0133          POPB
037A   E1           0134          POPH
037B   12           0135          STAX
037C   13           0136          INX D
037D   23           0137          INX H
037E   0D           0138          DCR C
037F   C2 71 03     0139          JNZ L111
0382   F1           0140          POP PSW
0383   FE 04        0141          CPI NBR6
```

```
LOC.   OBJ. CODE    M STMT SOURCE STATEMENT

0385   C2 8E 03      0142            JNZ LX
0388   3D            0143            DCR A
0389   06 5C         0144            MVI B,MODX8
038B   C3 6B 03      0145            JMP L555
038E   FE 03         0146   LX       CPI NBR3
0390   C2 99 03      0147            JNZ LXX
0393   3D            0148            DCR A
0394   06 4A         0149            MVI B,MODX9
0396   C3 6B 03      0150            JMP L555
0399   FE 02         0151   LXX      CPI NBR4
039B   C2 A4 03      0152            JNZ LXXX
039E   3D            0153            DCR A
039F   06 36         0154            MVI B,MODX10
03A1   C3 6B 03      0155            JMP L555          ;performed all
03A4   C9            0156   LXXX     RET               multiplications and
                     0157                              stored into TMPs.
                     0158 ;_____________________________________________
                     0159 ; LOAD:calculates tp values and loads into
                     0160 ;memory. The resultant tp values are stored into
                     0161 ;first three bits of the memory.Initially,regB
                     0162 ;should contain the current frequency value.
                     0163 ;Destroys all registers. Memory dimension
                     0164 ;depends upon R.
                     0165 ;            DEG0    DEG60   DEG90   DEG120 DEG180
                     0166 ;For R 60   08D0H   0970H   09C0H   0A10H   0AB0H
                     0167 ;For R 80   08D0H   09B5H   0A10H   0A7EH   0B50H
                     0168 ;For R 96   08D0H   09D0H   0A50H   0AD0H   0BD0H
03A5   78            0169 ; LOAD    MOV A,B
03A6   21 48 07      0170           LXI H,ADRS
03A9   85            0171           ADD L
03AA   6F            0172           MOV L,A           ;determined the TMP
                     0173                              location.
03AB   4E            0174           MOV C,M           ;gets the corresponding
                     0175                              MSin value.
03AC   21 D0 08      0176   CALC1   LXI H,DEG0
03AF   11 00 08      0177           LXI D,TMP1
03B2   59            0178           MOV E,C
03B3   78            0179           MOV A,B
03B4   FE 2E         0180           CPI R1            ;chose the proper R.
03B6   FA BE 03      0181           JM LK2
03B9   0E 0F         0182           MVI C,SWNBR       ;determined that R=60
03BB   C3 CA 03      0183           JMP LL3
03BE   FE 1C         0184   LK2     CPI R2
03C0   FA C8 03      0185           JM LK3
03C3   0E 14         0186           MVI C,SWNBR1      ;determined that R=80
03C5   C3 CA 03      0187           JMP LL3
03C8   0E 18         0188   LK3     MVI C,SWNBR2      ;determined that R=96
03CA   C5            0189   LL3     PUSH B            ;save frequency value.
03CB   1A            0190   LL33    LDAX
03CC   13            0191           INX D
03CD   47            0192           MOV B,A
03CE   3E 08         0193           MVI A,T/2
03D0   90            0194           SUB B
```

```
LOC.    OBJ. CODE    M STMT SOURCE STATEMENT

03D1    F5           0195          PUSH PSW
03D2    FE 00        0196          CPI 0
03D4    CA EC 03     0197          JZ L21
03D7    47           0198          MOV B,A
03D8    3E 00        0199          MVI A,0
03DA    77           0200 LL1      MOV M,A          ;loaded tp into memo
03DB    23           0201          INX H
03DC    05           0202          DCR B
03DD    C2 DA 03     0203          JNZ LL1
03E0    F1           0204 L21      POP PSW
03E1    47           0205          MOV B,A
03E2    3E 10        0206          MVI A,T
03E4    90           0207          SUB B
03E5    47           0208          MOV B,A
03E6    3E 01        0209          MVI A,1
03E8    77           0210 LL2      MOV M,A          ;loads logic ones in
                     0211                            memory.
03E9    23           0212          INX H
03EA    05           0213          DCR B
03EB    C2 E8 03     0214          JNZ LL2
03EE    0D           0215          DCR C
03EF    C2 CB 03     0216          JNZ LL33         ;loaded between DEG0
                     0217                            and DEG90 for phase
03F2    C1           0218 R1       POP B            ;restore frequency.
03F3    79           0219          MOV A,C
03F4    FE 0F        0220          CPI SWNBR
03F6    CA 1A 04     0221          JZ D1
03F9    FE 14        0222          CPI SWNBR1
03FB    CA 0C 04     0223          JZ D2
03FE    11 D0 0A     0224          LXI D,0AD0
0401    D5           0225          PUSH D
0402    11 D0 09     0226          LXI D,09D0
0405    D5           0227          PUSH D
0406    11 4F 0A     0228          LXI D,0A4F
0409    C3 25 04     0229          JMP CALLC        ;saved DEG120, DEG60
                     0230                            and DEG90 addresses
                     0231                            for R=96.
040C    11 7B 0A     0232 D2       LXI D,0A7B
040F    D5           0233          PUSH D
0410    11 B5 09     0234          LXI D,09B5
0413    D5           0235          PUSH D
0414    11 0F 0A     0236          LXI D,0A0F
0417    C3 25 04     0237          JMP CALLC        ;saved DEG120, DEG60
                     0238                            and DEG90 addresses
                     0239                            for R=80.
041A    11 10 0A     0240 D1       LXI D,0A10
041D    D5           0241          PUSH D
041E    11 70 09     0242          LXI D,0970
0421    D5           0243          PUSH D
0422    11 BF 09     0244          LXI D,09BF       ;saved DEG values for
                     0245                            R=60.
                     0246
```

```
LOC.    OBJ. CODE    M STMT SOURCE STATEMENT

0425    1A           0247  CALLC   LDAX
0426    0F           0248          RRC
0427    DA 3E 04     0249          JC L6
042A    3E 00        0250          MVI A,0
042C    77           0251  L7      MOV M,A
042D    23           0252          INX H
042E    1B           0253          DCX D
042F    3E CF        0254          MVI A,CF
0431    BB           0255          CMP E
0432    C2 25 04     0256          JNZ CALLC
0435    3E 08        0257          MVI A,08
0437    BA           0258          CMP D
0438    C2 25 04     0259          JNZ CALLC
043B    C3 43 04     0260          JMP LOADB1
043E    3E 01        0261  L6      MVI A,1
0440    C3 2C 04     0262          JMP L7          ;loaded memory between
                     0263                           DEG90 and DEG180 for
                     0264                           R phase.(bit zero)
0443    01 D0 08     0265  LOADB1  LXI B,DEG0
0446    E1           0266          POP H
0447    2B           0267          DCX H
0448    0A           0268  B1      LDAX
0449    0F           0269          RRC
044A    D2 62 04     0270          JNC L10
044D    3E 02        0271          MVI A,2
044F    B6           0272          ORA M
0450    77           0273          MOV M,A
0451    2B           0274          DCX H
0452    23           0275          INX B
0453    3E CF        0276          MVI A,CF
0455    BD           0277          CMP L
0456    C2 48 04     0278          JNZ B1
0459    3E 08        0279          MVI A,08
045B    BC           0280          CMP H
045C    C2 48 04     0281          JNZ B1
045F    C3 68 04     0282          JMP LOADY1
0462    3E FD        0283  L10     MVI A,FD
0464    A6           0284          ANA M
0465    C3 50 04     0285          JMP L11         ;loaded DEG0 to DEG60
                     0286                           for phase B.(bit 1)
0468    01 D0 08     0287  LOADY1  LXI B,DEG0
046B    E1           0288          POP H
046C    2B           0289          DCX H
046D    0A           0290          LDAX
046E    0F           0291          RRC
046F    DA 87 04     0292          JC L12
0472    3E 04        0293          MVI A,4
0474    B6           0294          ORA M
0475    77           0295  L13     MOV M,A
0476    2B           0296          DCX H
0477    03           0297          INX B
0478    3E CF        0298          MVI A,CF
```

```
LOC.     OBJ. CODE     M STMT SOURCE STATEMENT

047A     BD            0299          CMP L
047B     C2 6D 04      0300          JNZ Y1
047E     3E 08         0301          MVI A,08
0480     BC            0302          CMP H
0481     C2 6D 04      0303          JNZ Y1
0484     C3 8D 04      0304          JMP LOADB2
0487     3E FB         0305  L12     MVI A,FB
0489     A6            0306          ANA M
048A     C3 75 04      0307          JMP L13         ;loaded from DEG0 to
                       0308                           DEG120 for phaseY
                       0309                           (bit 2)
048D     3B            0310  LOADB2  DCX SP
048E     3B            0311          DCX SP
048F     3B            0312          DCX SP
0490     3B            0313          DCX SP
0491     E1            0314          POP H
0492     C1            0315          POP B
0493     0B            0316          DCX B
0494     0A            0317  B2      LDAX
0495     0F            0318          RRC
0496     0F            0319          RRC
0497     0F            0320          RRC
0498     DA B0 04      0321          JC L1
049B     3E FD         0322          MVI A,FD
049D     A6            0323          ANA M
049E     77            0324  L2      MOV M,A
049F     23            0325          INX H
04A0     0B            0326          DCX B
04A1     3E CF         0327          MVI A,CF
04A3     B9            0328          CMP C
04A4     C2 94 04      0329          JNZ B2
04A7     3E 08         0330          MVI A,8
04A9     B8            0331          CMP B
04AA     C2 94 04      0332          JNZ B2
04AD     C3 B6 04      0333          JMP LOADY2
04B0     3E 02         0334  L1      MVI A,2
04B2     B6            0335          ORA M
04B3     C3 9E 04      0336          JMP L2          ;loaded from DEG60 to
                       0337                           DEG180 for phaseB
                       0338                           (bit 1)
04B6     3B            0339          DCX SP
04B7     3B            0340          DCX SP
04B8     3B            0341          DCX SP
04B9     3B            0342          DCX SP
04BA     C1            0343          POP B
04BB     E1            0344          POP H
04BC     0B            0345          DCX B
04BD     0A            0346          LDAX
04BE     0F            0347          RRC
04BF     0F            0348          RRC
04C0     DA D8 04      0349          JC L1
04C3     3E FB         0350          MVI A,FB
```

```
LOC.    OBJ. CODE    M STMT SOURCE STATEMENT

04C5    A6           0351           ANA M
04C6    77           0352   L2      MOV M,A
04C7    23           0353           INX H
04C8    0B           0354           DCX B
04C9    3E CF        0355           MVI A,CF
04CB    B9           0356           CMP C
04CC    C2 BD 04     0357           JNZ Y2
04CF    3E 08        0358           MVI A,8
04D1    B8           0359           CMP B
04D2    C2 BD 04     0360           JNZ Y2
04D5    C3 DE 04     0361           JMP SON
04D8    3E 04        0362   L1      MVI A,4
04DA    B6           0363           ORA M
04DB    C3 C6 04     0364           JMP L2
04DE    C9           0365   SON     RET                ;loaded from DEG120 to
                     0366                               DEG180 for phase Y
                     0367                               (bit 2)
                     0368 ;-------------------------------------------------
                     0369 ; NEGTV :
                     0370 ;complements the switching pattern stored in
                     0371 ;the first three bits, and stores them into
                     0372 ;bit3, bit4 and bit5.
                     0373 ;destroys  registers A, H and L.
04DF    3E FF        0374  NEGTV    MVI A,FF
04E1    32 CF 08     0375           STA TMP200
04E4    78           0376           MOV A,B
04E5    FE 2E        0377           CPI R1
04E7    FA F0 04     0378           JM L2
04EA    21 AF 0A     0379           LXI H, DEG180   ;for R 96.
04ED    C3 FE 04     0380           JMP DONE
04F0    FE 1C        0381   L2      CPI R2
04F2    FA FB 04     0382           JM L3
04F5    21 4F 0B     0383           LXI H, DEG180   ;for R  80
04F8    C3 FE 04     0384           JMP DONE
04FB    21 CF 0B     0385   L3      LXI H, DEG180   ;for R 60
04FE    7E           0386   DONE    MOV A,M
04FF    FE FF        0387           CPI FF
0501    C8           0388           RZ
0502    07           0389           RLC
0503    07           0390           RLC
0504    07           0391           RLC
0505    B6           0392           ORA M
0506    77           0393           MOV M,A
0507    2B           0394           DCX H
0508    C3 FE 04     0395           JMP DONE
                     0396 ;-------------------------------------------------
                     0397 ;OUTPAT:
                     0398 ;outputs the switching pattern one cycle.
                     0399 ;destroys registers A,B,D,E,H,L.
0510    2A D2 0B     0400  OUTPAT   LHLD 0BD2       ;loads memory lenght
0513    EB           0401           XCHG
0514    21 D0 08     0402           LXI H,DEG0
```

```
LOC.    OBJ. CODE    M STMT SOURCE STATEMENT

0517    7E           0403  L7      MOV A,M
0518    23           0404          INX H
0519    BE           0405          CMP M
051A    C2 40 05     0406          JNZ LY          ;checks whether data
                     0407                           are changed or not.
051D    06 02        0408          MVI B,02
051F    05           0409  L       DCR B
0520    C2 1F 05     0410          JNZ L
0523    D3 04        0411  LA      OUT PORTA
0525    1B           0412          DCX D
0526    E5           0413          PUSH H
0527    2A D4 0B     0414          LHLD TEMP2
052A    EF           0415          RST
052B    E1           0416          POP H
052C    06 02        0417          MVI B,2
052E    05           0418  LL      DCR B
052F    C2 2E 05     0419          JNZ LL
0532    00           0420          NOP
0533    3E 00        0421          MVI A,0
0535    BB           0422          CMP E
0536    C2 17 05     0423          JNZ L7
0539    BA           0424          CMP D
053A    C2 17 05     0425          JNZ L7
053D    C3 49 05     0426          JMP L8
0540    00           0427  LY      NOP
0541    3E 38        0428          MVI A,TRIST
0543    D3 04        0429          OUT PORTA
0545    7E           0430          MOV A,M
0546    C3 23 05     0431          JMP LA
0549    2A D2 0B     0432  L8      LHLD TEMP1      ;outputs negative hal
                     0433                           cycle.
054C    EB           0434          XCHG
054D    21 CF 08     0435          LXI H,DEGO
0550    7E           0436  L10     MOV A,M
0551    23           0437          INX H
0552    BE           0438          CMP M
0553    C2 7B 05     0439          JNZ LYY
0556    00           0440          NOP
0557    06 01        0441          MVI B,1
0559    05           0442  LLL     DCR B
055A    C2 59 05     0443          JNZ LLL
055D    F6 80        0444  LA1     ORI 80
055F    2F           0445          CMA
0560    D3 04        0446          OUT PORTA
0562    1B           0447          DCX D
0563    E5           0448          PUSH H
0564    2A D4 0B     0449          LHLD TEMP2
0567    EF           0450          RST
0568    E1           0451          POP H
0569    06 02        0452          MVI B,2
056B    05           0453  LL1     DCR B
056C    C2 6B 05     0454          JNZ LL1
056F    00           0455          NOP
```

```
LOC.     OBJ. CODE     M STMT SOURCE STATEMENT

0570     3E 00          0456          MVI A,0
0572     BB             0457          CMP E
0573     C2 50 05       0458          JNZ L10
0576     BA             0459          CMP D
0577     C2 50 05       0460          JNZ L10
057A     C9             0461          RET
057B     00             0462    LYY   NOP
057C     3E 38          0463          MVI A,TRIST
057E     D3 04          0464          OUT PORTA
0580     7E             0465          MOV A,M
0581     C3 5D 05       0466          JMP LA1
                        0467;----------------------------------------
                        0468;MAINP:
                        0469;Gets the frequency value, determines the
                        0470;frequency ratio, memory dimension, and the
                        0471;count number. Outputs the switching pattern
                        0472;one cycle than checks whether the frequency
                        0473;changes or not. If changed, calculates new
                        0474;parameters.
062D     3E B8          0475          MVI A,STRTP
062F     D3 04          0476          OUT PORTA       ;gives start pulse
0631     3E 38          0477          MVI A,38         to ADC.
0633     D3 04          0478          OUT PORTA
0635     CD 00 03       0479          CALL PRFM       ;all multiplications
                        0480                           are performed offlir
0638     DB 05          0481    LAT   IN PORTB        ;gets frequency value
                        0482                           from ADC.
063A     FE 08          0483          CPI SMAL
063C     FA DB 06       0484          JM BASA         ;if f is smaller than
                        0485                          one Hz. jump to BASA.
063F     06 08          0486          MVI B,SMAL
0641     F5             0487          PUSH PSW
0642     E6 FC          0488          ANI FC
0644     F5             0489    L5    PUSH PSW
0645     C5             0490          PUSH B
0646     CD A5 03       0491          CALL LOAD
0649     C1             0492          POP B
064A     C5             0493          PUSH B
064B     CD DF 04       0494          CALL NEGTV
064E     78             0495          MOV A,B
064F     FE 2E          0496          CPI R1          ;determines memory
0651     FA 65 06       0497          JM L22          lenght.
0654     21 DF 01       0498          LXI H,DURTN
0657     22 D2 0B       0499          SHLD TEMP1
065A     21 59 07       0500          LXI H,TABLC
065D     85             0501          ADD L
065E     6F             0502          MOVL,A
065F     22 D4 0B       0503          SHLD TEMP2
0662     C3 8F 06       0504          JMP L2
0665     FE 1C          0505    L22   CPI R2
0667     FA 7B 06       0506          JM L33
066A     21 7F 02       0507          LXI H,DURTN1
```

```
LOC.    OBJ. CODE    M STMT SOURCE STATEMENT

066D    22 D2 0B     0508          SHLD TEMP1
0670    21 7E 07     0509          LXI H,TBLEC
0673    85           0510          ADD L
0674    6F           0511          MOV L,A
0675    22 D4 0B     0512          SHLD TEMP2
0678    C3 8F 06     0513          JMP L2
067B    21 FF 02     0514 L33      LXI H,DURTN2
067E    22 D2 0B     0515          SHLD TEMP1
0681    21 AA 07     0516          LXI H,TBLEC
0684    85           0517          ADD L
0685    6F           0518          MOV L,A
0686    C1           0519          POP B
0687    4E           0520          MOV C,M
0688    C5           0521          PUSH B
0689    21 20 06     0522          LXI H,DONGU
068C    22 D4 0B     0523          SHLD TEMP2      ;now, TEMP1 contains
                     0524                           memory lenght, TEMP2
                     0525                           contains addrs of
                     0526                           count number.
068F    3E B8        0527 L2       MVI A,STRTP
0691    D3 04        0528          OUT PORTA
0693    3E 38        0529          MVI A,38
0695    D3 04        0530          OUT PORTA
0697    CD 10 05     0531          CALL OUTPAT     ;output one cycle.
069A    3E 38        0532          MVI A,38
069C    D3 04        0533          OUT PORTA       ;inverter channels a
                     0534                           in tri-state.
069E    C1           0535          POP B
069F    F1           0536          POP A
06A0    B8           0537          CMP B
06A1    CA B5 06     0538          JZ NEWVL
06A4    FA AE 06     0539 LX       JM DUSUK        ;if f smaller than
                     0540                           desired freq. jump
                     0541                           DUSUK
06A7    04           0542          INR B
06A8    04           0543          INR B
06A9    04           0544          INR B
06AA    04           0546          INR B
06AB    C3 44 06     0547          JMP L5
06AE    05           0548 DUSUK    DCR B
06AF    05           0549          DCR B
06B0    05           0550          DCR B
06B1    C3 44 06     0551          JMP L5
06B5    F1           0552 NEWVL    POP PSW
06B6    F5           0553          PUSH PSW
06B7    B8           0554          CMP B
06B8    CA BF 06     0555          JZ NEW
06BB    47           0556          MOV B,A
06BC    C3 44 06     0557          JMP L5
06BF    DB 05        0558 NEW      IN PORTB        ;checks whether freq
                     0559                           changes.
06C1    B8           0560          CMP B
```

```
LOC.    OBJ. CODE     M STMT SOURCE STATEMENT

06C2    CA D6 06      0561          JZ L55
06C5    FE 08         0562          CPI  SMAL
06C7    FA DB 06      0563          JM BASA
06CA    D1            0564          POP D
06CB    F5            0565          PUSH PSW
06CC    E6 FC         0566          ANI FC
06CE    F5            0567          PUSH PSW
06CF    78            0568          MOV A,B
06D0    E6 FC         0569          ANI FC
06D2    47            0570          MOV B,A
06D3    C3 45 06      0571          JMP LLL
06D6    F5            0572 L55      PUSH PSW
06D7    C5            0573          PUSH B
06D8    C3 8F 06      0574          JMP L2
06DB    3E B8         0575 BASA     MVI A,STRTP     ;if ADC value is
                      0576                           smaller than on
                      0577                           Hz. waits here.
06DD    D3 04         0578          OUT PORTA
06DF    3E 38         0579          MVI A,38
06E1    D3 04         0580          OUT PORTA
06E3    3E 25         0581          MVI A,DLC
06E5    3D            0582 LIB      DCR A
06E6    C2 4A 06      0583          JNZ LIB
06E9    C3 38 06      0584          JMP LAT
```

```
LOC.    DEFB.

;Sine values table for R 60.
07C5    1B
07C6    35
07C7    4F
07C8    68
07C9    80
07CA    96
07CB    AB
07CC    BD
07CD    CE
07CE    DD
07CF    E9
07D0    F3
07D1    FA
07D2    FE
07D3    FF

;Sine values table for R 80.
07D4    14
07D5    28
07D6    3C
07D7    4F
07D8    62
07D9    74
07DA    85
07DB    96
07DC    A6
07DD    B4
07DE    C2
07DF    CE
07E0    D9
07E1    E3
07E2    EC
07E3    F3
07E4    F8
07E5    FC
07E6    FE
07E7    FF

;Sine values table for R 96.
07E8    11
07E9    21
07EA    32
07EB    42
07EC    52
07ED    62
07EE    71
07EF    80
07F0    8E
07F1    9B
07F2    A8
07F3    B4
07F4    C0
```

```
LOC.     DEFB.

07F5     CB
07F6     D4
07F7     DD
07F8     E5
07F9     EC
07FA     F1
07FB     F6
07FC     FA
07FD     FD
07FE     FE
07FF     FF
:
;Count number table for R  60
0789     3D
078A     00
078B     00
078C     00
078D     00
078E     00
078F     00
0790     00
0791     00
0792     00
0793     00
0794     00
0795     00
0796     00
0797     00
0798     C9

;Count number table for R 80
0799     19
079A     19
079B     19
079C     19
079D     19
079E     7E
079F     19
07A0     7E
07A1     7E
07A2     7E
07A3     7E
07A4     3D
07A5     7E
07A6     3D
07A7     3D
07A8     3D
07A9     3D
07AA     00
07AB     3D
07AC     00
07AD     C9
```

```
LOC.      DEFB.

;Count number table for R 96
07AE      78
07AF      5E
07B0      4B
07B1      3F
07B2      35
07B3      2E
07B4      28
07B5      23
07B6      1F
07B7      1C
07B8      16
07B9      14
07BA      12
07BB      10
07BC      0F
07BD      0D
07BE      0C
07BF      0B
07C0      0A
07C1      09
07C2      08
07C3      07
07C4      06

;Address convertion table
0748      B1
0749      B1
074A      B1
074B      B1
074C      B1
074D      B1
074E      B1
074F      B1
0750      B1
0751      B1
0752      99
0753      99
0754      99
0755      99
0756      99
0757      99
0758      81
0759      81
075A      81
075B      81
075C      81
075D      81
075E      69
075F      69
0760      69
0761      69
0762      69
```

LOC.	DEFB.
0763	69
0764	55
0765	55
0766	55
0767	55
0768	55
0769	55
076A	55
076B	41
076C	41
076D	41
076E	41
076F	41
0770	41
0771	2D
0772	2D
0773	2D
0774	2D
0775	2D
0776	2D
0777	1E
0778	1E
0779	1E
077A	1E
077B	1E
077C	1E
077D	0F
077E	0F
077F	0F
0780	0F
0781	0F
0782	0F
0783	00
0784	00
0785	00
0786	00
0787	00
0788	00

APPENDIX C

CONNECTION DIAGRAM OF BOTH MICROCOMPUTER KIT AND INVERTER

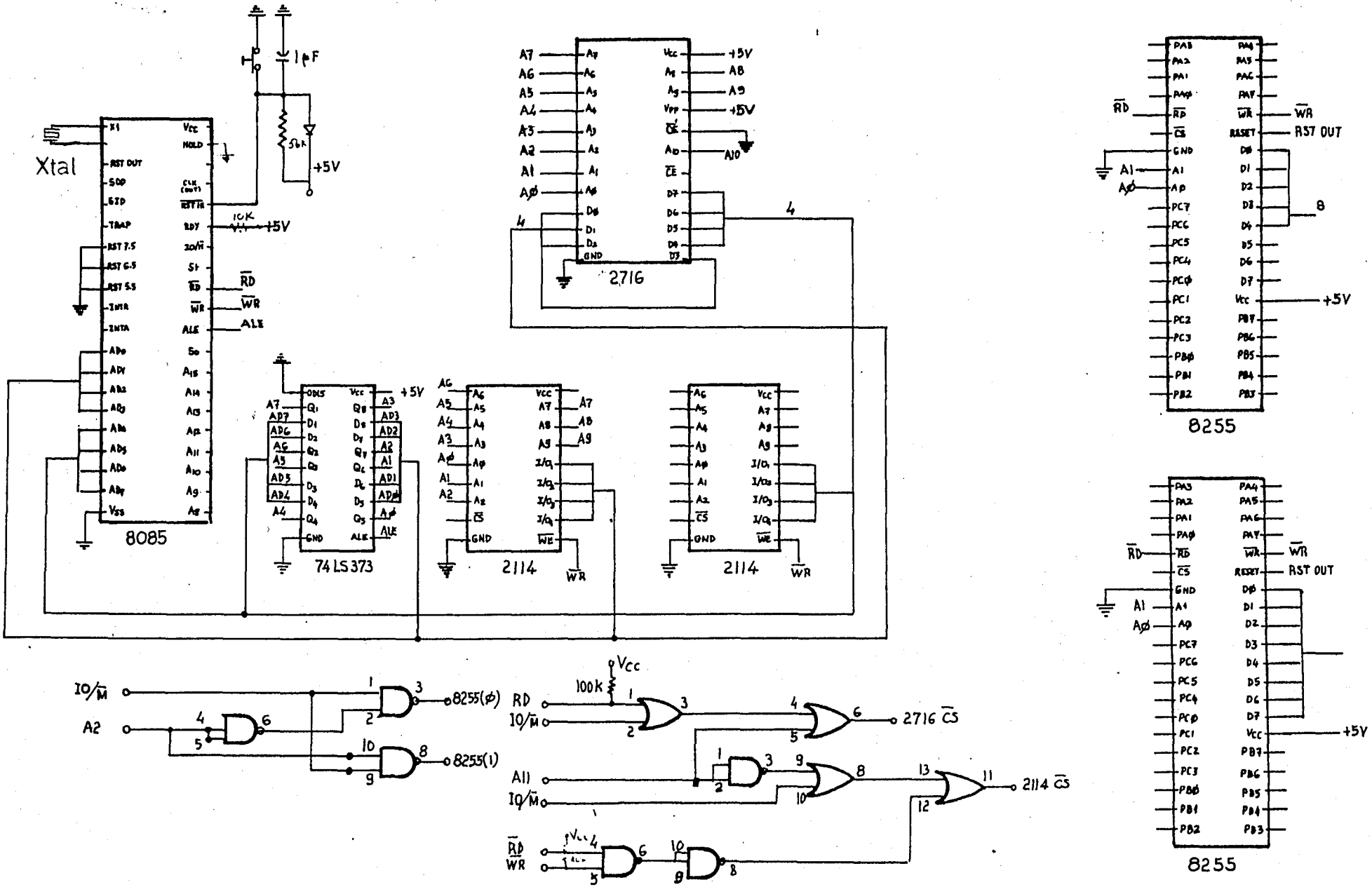

Xtal
1μF
10K
+5V
RD
WR
ALE
8085
74LS373
2114
2716
8255
IO/M
A2
8255(Ø)
8255(1)
Vcc
100k
2716 CS
A11
2114 CS

Figure C.1.

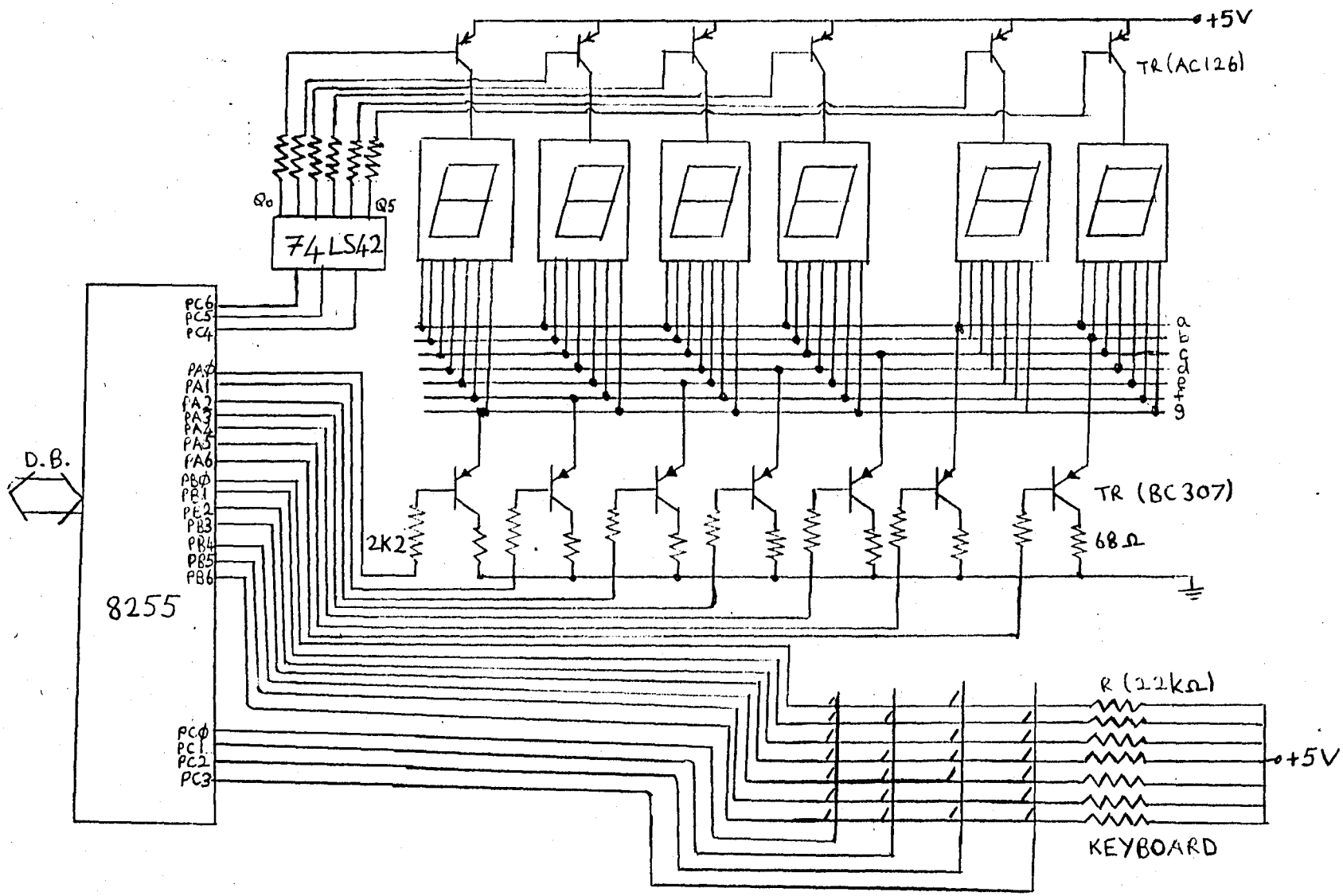


Figure C.2 Keyboard and display organization.

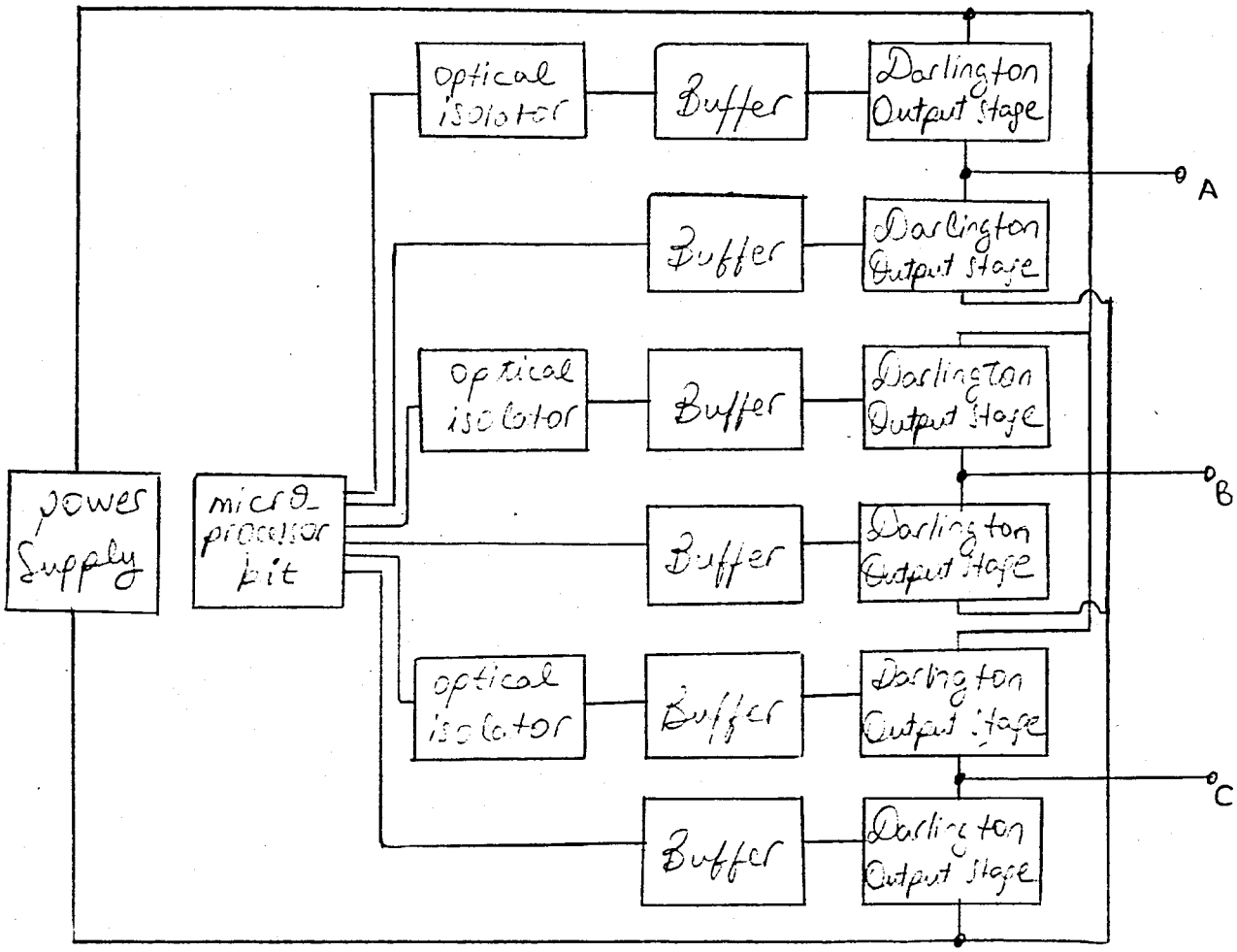


Figure C.3 Block diagram of the transistor inverter.

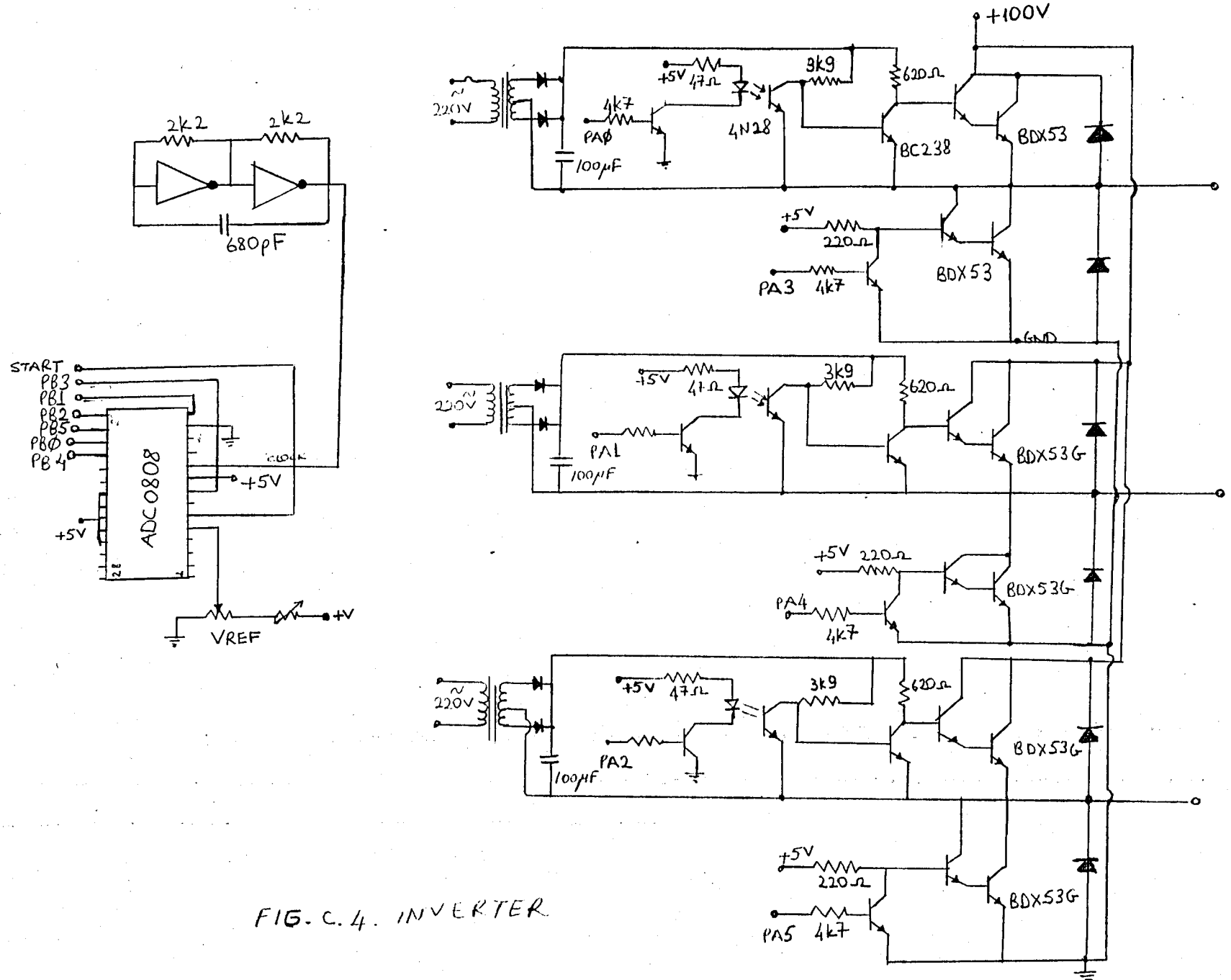


FIG. C.4. INVERTER

APPENDIX D

FOURIER ANALYSIS OF THE PWM WAVEFORM

PWM WAVEFORM HARMONIC ANALYSIS

```
Ready
LIST-180
 10 DIM T1(80),V(80)
 20 INPUT X1,M
 30 PRINT/P TAB(10);"[illegible]";X1
 35 PRINT/P TAB(10);"[illegible]";M
 37 PRINT/P
 40 X=2*π/M:X0=0:K=1
 50 T1(K)=X*(1+X1*SIN(X0))/2
 60 K=K+1:X0=X0+X:T1(K)=X0:K=K+1
 70 IF X0>=π/2 THEN 90
 80 GOTO 50
 90 K=1:X0=0
100 T1(K)=T1(K)+X0:X0=X0+X
110 IF X0>=π/2 THEN 130
120 K=K+2:GOTO 100
130 FOR N=1 TO 31 STEP 2
140 L=1:X2=0
150 FOR L=1 TO K-1
160 X2=((-1)^L)*COS(N*T1(L))+X2
170 NEXT
180 X2=2*X2:V(N)=(4/(N*π))*(1+X2)
Ready
COPY/P1

 180 X2=2*X2:V(N)=(4/(N*π))*(1+X2)
 190 PRINT/PTAB(10);"V(";N;")= ";V(N)
 200 NEXT
 210 S1=0
 220 FOR I=1 TO 31 STEP 2
 230 S1=S1+(V(I)/I)^2
 240 NEXT
 250 S2=SQR(S1)/V(1):PRINT/P:PRINT/P
 260 PRINT/PTAB(10);"[illegible]";S2:PRINT/P:PRINT/P"
     ----------":PRINT/P:PRINT/P
 Ready
```

RESULTS

Modulation index = 1
Frequency ratio = 60

V(1)= 0.94158258
V(3)= -0.043379699
V(5)= -.76408215E-02
V(7)= -0.012032389
V(9)= -.59636139E-02
V(11)= -.70448929E-02
V(13)= -.47760303E-02
V(15)= -.51260733E-02
V(17)= -.41013012E-02
V(19)= -.41906037E-02
V(21)= -.37209044E-02
V(23)= -.37130975E-02
V(25)= -.35317308E-02
V(27)= -.35117321E-02
V(29)= -.34905417E-02
V(31)= -.35241359E-02

Sigma = 1.0001216

Modulation index = 0.9
Frequency ratio = 60

V(1)= 0.84324571
V(3)= -0.031893363
V(5)= -0.013522946
V(7)= -.44268905E-02
V(9)= -0.011800861
V(11)= .23354374E-04
V(13)= -0.010708359
V(15)= .17686704E-02
V(17)= -0.010119364
V(19)= .26518928E-02
V(21)= -.98182453E-02
V(23)= .31416064E-02
V(25)= -.97091265E-02
V(27)= .34032841E-02
V(29)= -.97548323E-02
V(31)= .34983226E-02

Sigma = 1.0000872

Modulation index = 0.8
Frequency Ratio = 60

V(1)= 0.74509135
V(3)= -0.021233083
V(5)= -0.018686409
V(7)= .25239982E-02
V(9)= -0.016993282
V(11)= .64823565E-02
V(13)= -0.01604696
V(15)= .81058946E-02
V(17)= -0.015605797
V(19)= .90053108E-02
V(21)= -0.015464852
V(23)= .95979416E-02
V(25)= -0.015541902
V(27)= 0.010039651
V(29)= -0.015814401
V(31)= 0.010401017

Sigma = 1.0000654

Modulation index = 0.7
Frequency Ratio = 80

V(1)= 0.66065286
V(3)= -.88390168E-02
V(5)= -0.0173181
V(7)= .65435488E-02
V(9)= -0.016021475
V(11)= .91738424E-02
V(13)= -0.015340956
V(15)= 0.010297023
V(17)= -0.015013854
V(19)= 0.010959673
V(21)= -0.014886185
V(23)= 0.011436475
V(25)= -0.014892707
V(27)= 0.011832992
V(29)= -0.015005471
V(31)= 0.012200952

Sigma = 1.0000345

Modulation Index = 0.6
Frequency Ratio = 80

V(1)= 0.56225441
V(3)= -.20212334E-02
V(5)= -0.020090615
V(7)= 0.01075217
V(9)= -0.018898301
V(11)= 0.013017635
V(13)= -0.018345039
V(15)= 0.014037326
V(17)= -0.018132021
V(19)= 0.014691231
V(21)= -0.018119387
V(23)= 0.015214004
V(25)= -0.018251857
V(27)= 0.015699072
V(29)= -0.018509144
V(31)= 0.016195925

Sigma = 1.0000508

Modulation Index = 0.5
Frequency Ratio = 96

V(1)= 0.47008409
V(3)= .33951635E-02
V(5)= -0.018581649
V(7)= 0.012012494
V(9)= -0.017666566
V(11)= 0.013583387
V(13)= -0.017266234
V(15)= 0.014307979
V(17)= -0.017116434
V(19)= 0.014785597
V(21)= -0.017111155
V(23)= 0.015176544
V(25)= -0.017208297
V(27)= 0.01554418
V(29)= -0.017390589
V(31)= 0.015921088

Sigma = 1.0000684

Modulation index = 0.4
Frequency ratio = 96

V(1)= 0.3716448
V(3)= .80044596E-02
V(5)= -0.019966465
V(7)= 0.014660176
V(9)= -0.019197803
V(11)= 0.015932408
V(13)= -0.018907015
V(15)= 0.016558184
V(17)= -0.018841856
V(19)= 0.017007179
V(21)= -0.018913219
V(23)= 0.017407093
V(25)= -0.019087753
V(27)= 0.017810112
V(29)= -0.01935351
V(31)= 0.018244848

Sigma = 1.0001544

Modulation index = 0.33
Frequency ratio = 96

V(1)= 0.30281279
V(3)= 0.010899987
V(5)= -0.020661075
V(7)= 0.01625672
V(9)= -0.020012479
V(11)= 0.017324041
V(13)= -0.019800407
V(15)= 0.017879853
V(17)= -0.019793326
V(19)= 0.018306284
V(21)= -0.019915591
V(23)= 0.018708776
V(25)= -0.02014034
V(27)= 0.019131791
V(29)= -0.020459445
V(31)= 0.019601146

Sigma = 1.0002875

Modulation index = 0.27
Frequency ratio = 96

V(1)= 0.24386363
V(3)= 0.01316413
V(5)= -0.021076112
V(7)= 0.017456532
V(9)= -0.020541712
V(11)= 0.018350578
V(13)= -0.020397993
V(15)= 0.018845359
V(17)= -0.020439289
V(19)= 0.01925004
V(21)= -0.020602533
V(23)= 0.01965136
V(25)= -0.020866657
V(27)= 0.020087182
V(29)= -0.021226795
V(31)= 0.020580856

Sigma = 1.0005183

Modulation index = 0.18
Frequency ratio = 96

V(1)= 0.1555263
V(3)= 0.016182194
V(5)= -0.021386194
V(7)= 0.01896395
V(9)= -0.021042295
V(11)= 0.019601675
V(13)= -0.021002061
V(15)= 0.020002357
V(17)= -0.021112666
V(19)= 0.0203693
V(21)= -0.021331684
V(23)= 0.020761722
V(25)= -0.021647086
V(27)= 0.021207648
V(29)= -0.022058897
V(31)= 0.021726565

Sigma = 1.0015437

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