MODELS FOR VERY HIGH SPEED FETS

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MODELS FOR A VERY HIGH SPEED TRANSISTOR

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MODELS FOR VERY HIGH SPEED TRANSISTORS

In recent years,the semiconductor electronic industry has entered the Very Large Scale Integration(VLSI)era, in which individual integrated circuits are characterized by increasingly complex circuitry and technology.Progress in the microelectronics area will continue to be tied to the ability to continue to put ever increasing numbers of smaller devices on a chip. In the submicron device size range, it is expected that transport will be limited by the saturation velocity.Therefore, the devices should be very fast and be fabricated with very small dimensions.A new transistor which can meet these requirements has appeared on the scene. This transistor,called MODFET which is a device evolved from the work on GaAs-AlGaAs superlattices(thin alternating layers of different materials sharing the same crystalline lattice) shows some superior properties because of high mobilities achieved in GaAs since electrons transfer from the doped wider band gap AlGaAs to an adjacent undoped GaAs layer,a process now called modulation doping.

Models to predict the characteristics of MODFET are investigated and a new analytical model is introduced.This new model,called Mobility-Dependent Model and based on the field dependent velocity approximation, seems to be the best model for this type of device so far.

ÇOK HIZLI BİR TRANZİSTOR IÇİN MODELLER

Son yıllarda yarı iletken elektronik endüstrisi gittikçe karmaşık bir tümleşik devre ve teknoloji içeren çok büyük çapta tümleşik devreler (VLSI) çağına ulaşmıştır. Mikroelektronik alandaki bu hızlı gelişme her geçen gün daha çok sayıda küçük devre elemanını bir kırmığa yerleştirebilme gereksiniminden kaynaklanmaktadır.Mikron altı küçük boyutlara sahip elemanlarda,ulaşılabilecek en yüksek çalışma hızı doyma hızı ile sınırlıdır.O halde,geleceğin ihtiyaçlarını karşılayabilecek elemanların çok hızlı ve çok küçük boyutlarda olması gerekmektedir.Bu gereksinimleri karşılayacak GaAs-AlGaAs süperyapılar (aynı kristal yapı içinde ince tabakalar halinde farklı malzemelerin değişimli olarak yerleştirilmesiyle oluşmuş kristal yapı) teknolojisine dayalı yeni bir tranzistor üretilmeye başlanmıştır. Bu tranzistor bazı üstün özellikler göstermektedir çünkü kullandığı modülasyonlu katkılama teknolojisinin sonucu katkılanmış geniş enerji bantlı malzemedeki elektronların bitişikteki katkılanmamış dar bantlı malzemeye geçmesiyle çok yüksek elektron hareket kabiliyeti özelliğine sahiptir.

Bu tezde MODFET olarak isimlendirilen bu tranzistorun karakteristiklerini belirlemek için geliştirilen modeller

sırasıyla incelenecek ve Hareketliliğe-Bağımlı model diye isimlendirilen yeni bir analitik model önerilecektir.Bu model elektron sürüklenme hızının elektrik alanına bağımlılığı üzerine kurulmuştur ve şimdiye kadar,bu tip bir tranzistor için,geliştirilmiş en iyi model gibi görünmektedir.

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I. INTRODUCTION

Depending on their use,high speed devices can be grouped into two categories :analog and digital devices.In general the analog devices are much faster than the digital ones and both types have different applications.This thesis will be concerned with only special high speed field effect transistors which can be best fabricated by a special manufacturing technology,called molecular beam epitaxy(MBE).

Devices intended for high speed applications should have very short transit times between the input and the output.This can be obtained by choosing a semiconductor and/or a special structure which exhibits high carrier velocity and by reducing the distance that the carriers have to travel.In vertical devices,e.g.bipolar junction transistors,the important distance is the base thickness.This means that the control of the base thickness is very important.

Lateral three terminal devices,such as FETs,must have correspondingly small lateral dimensions.Small lateral dimensions also require small epitaxial layer thicknesses and larger doping. The drawback of very high carrier concentrations is that the electronic properties of semiconductor degrade with increased doping.The point should be made very clear that for current conduction one needs electrons or holes.In conventional structures, electrons and donors,and holes and acceptors are present in the same space.Using the heterojunction concept that can be achieved by MBE it is possible to separate the electrons needed for current conduction from donors,minimizing their adverse effects.

Electrons associated with donors placed in the $Al_xGa_{1-x}As$ layers of $Al_xGa_{1-x}As$/GaAs heterojunction structures transfer to the GaAs layers.The resulting space charge sets up a strong electric field at each interface and leads to the formation of a triangular potential well.Aided by the energy bandgap discontinuity,the electrons are confined to the heterointerface and are spatially separated from the donors.This is a very convenient way of obtaining electron concentrations of over 10^{18} cm^{-3} essentially in a plane.Since the donors are separated from the electrons the electron transport properties of undoped GaAs are preserved.This phenomenon is called modulation doping,the FET application of which will be the main topic of this thesis.

In the first chapter the two-dimensional phenomenon encountered in Si-SiO_2 interfaces and in heterointerfaces is summarized.Since the device operation of MOSFET and MODFET is based on the two-dimensional phenomenon,at least,having a general idea about this concept is necessary.Many aspects of the two-dimensional electron gas(2-DEG) cannot be explained properly yet,therefore,only general properties will be given. Since a thorough consideration of two-dimensional transport phenomenon is beyond the scope of this study.

In the second chapter,main properties which cause the differences between Si and GaAs characteristics and some physical material properties of them are given.Also,in this chapter,the devices fabricated utilizing the properties of compound semiconductors,especially the GaAs,and the devices incorporating heterojunctions are described and comparisons

between them are made.At the end of this chapter a comparison of today's available high-frequency,low-power device applications are given.

The third chapter is devoted to the MODFET.A thorough explanation of modulation doping technique,which is the basic principle of obtaining MODFETs as a result giving its name to the device,is given.Then the fabrication techniques are given briefly preceding to the investigation of the models.The models, which are proposed to estimate the device characteristics and to be used as guides in device designs,are given in the order in which they appear in the international literature.Comparisons between them and between experimental data are made.

In the last chapter we introduce a new model which is based on the field-dependent velocity formula of Lehovec and Zuleeg.At the beginning,high field transport conditions ,which are frequently encountered in the submicrometer devices, are investigated.Then the model predictions about the device behavior are given.It is shown that very good agreement with experimental data is obtained.The AC and DC characteristics of the MODFET are obtained using the proposed model.Comparisons of the results with the present models and the introduced model are made.The high frequency performance,switching properties and the circuit applications of the MODFET are discussed.At the very end,the noise performance of the device is given.

II. TWO-DIMENSIONAL ELECTRON GAS

Our main interest in this chapter is dynamically-two dimensional system in which electrons or holes have quantized energy levels for one spatial dimension,but are free to move in two spatial dimensions.Thus the wave vector is a good quantum number for two dimensions,but not for the third.

The best known two-dimensional systems are carriers confined to the vicinity of junctions between insulators and semiconductors,between layers of different semiconductors, and between vacuum and liquid helium.

The most important example of a two-dimensional system is a particular insulator-semiconductor heterojunction system- the metal-insulator-semiconductor (MIS) and more particularly the metal-oxide-semiconductor (MOS) structure.The silicon MOS field-effect transistor (MOSFET) developed in 1960s and 1970s as an amplifying and switching device used in integrated circui It is the most successful example of a device in which the cha on the plates of a capacitor is changed by the application of a voltage in order to modulate the conductance of one of the plates,and is now one of the major electronic components of memory and logic circuits used in computers.

The interest in MOS structures is enhanced because they show the electronic properties expected of a two-dimensional electron gas.It was postulated by Schrieffer (1) that the electrons confined in narrow potential well of an inversion layer would not behave classically.Quantization of the motion

in this direction into discrete levels is expected.When the free-electron behavior along the interface is included,the energy levels take the form

$$E = E_n + \hbar^2(k_x^2 + k_y^2)/2m \qquad (1.1)$$

where k_x and k_y are the wave vector components for the motion parallel to the surface and the E_n are the electric quantum levels arising from the confinement in the narrow potential well.Each value of E_n is the bottom of a two-dimensional continuum called a subband.

Fang and Howard (2) had observed a pronounce decrease in the electron mobility at high surface fields on a (100) surfa at 4.2K.They postulated that on a (100) surface the degenerac of the six silicon conduction band energy minima located alon the [100] axes in the Brillouin zone is removed by quantizati in the surface potential well.The four valleys for which the effective mass for motion perpendicular to the surface is the light mass m_t are expected to have higher values of the quant levels E_n of Equation(1.1) than the two valleys whose long ax corresponding to the heavy effective mass m_ℓ,is perpendicular to the surface.They assumed that the decrease in mobility appeared when the increasing carrier concentration carried the Fermi level into the subband associated with the higher energy levels,making scattering between the two set of valle energetically possible.This explanation was not a correct one for the decrease in mobility but it gave the basis for the models of quantization in these surfaces and its predictions as to the lifting of degeneracy of the valleys and of the

two-dimensional nature of the electrons were soon borne out by magnetoconductance measurements.

A. Magnetoconductance

A two-dimensional conduction band without spin or valley degeneracy has a constant density of states equal to $D=m/2\pi\hbar^2$, where m is the effective mass,assumed to be isotropic.If a magnetic field H perpendicular to the surface is applied,the two-dimensional free electron motion is converted to a set of quantized Landau levels with spacing $eH\hbar/mc$,(3) .Neglecting spin,the energy states of the free electrons in the presence of the magnetic field H is given by the expression

$$E=(p+ 1/2)\hbar\omega_c+ \hbar^2 k_z^2/2m^* \qquad (1.2) \qquad ,(4)$$

where p is a positive integer, $\omega_c= eH/mc$,is the cyclotron frequen and $k_z$is the component of the electron wave vector in the direction of the magnetic field,which has been assumed to be in direction perpendicular to the motion.The quantities m_c and m^* are the cyclotrcn mass and effective mass respectively.As one can see from Equation (1.2) ,p and k_z are quantum numbers that characterize the energy state of an electron in a magnetic field.The quantum number p can take only integral values or zero and characterizes which Landau level the electron belongs to,whereas,$k_z$varies continuosly. This situation, is illustrated in Figure 2,is startingly different from the uniform distribution of electrons in $\vec{k}$- space.

Viewed over a sufficiently large range of energy or $\vec{k}$-space,the average density of states is not grossly affected

by a magnetic field;but the detailed distribution is certainly changed.It is this detailed distribution which explains various phenomena that show an oscillatory dependence on B_z.The density of states given by a seriesof δ-functions is $eH/mc\hbar(p+1/2)\pm g\beta H/2$, where H is the magnetic field,p is the order,g the Lande g-factor,c the speed of light,and β is the Bohr magneton,(5). Each Landau level has to conserve the states available in an energy interval equal to the Landau energy at zero field.

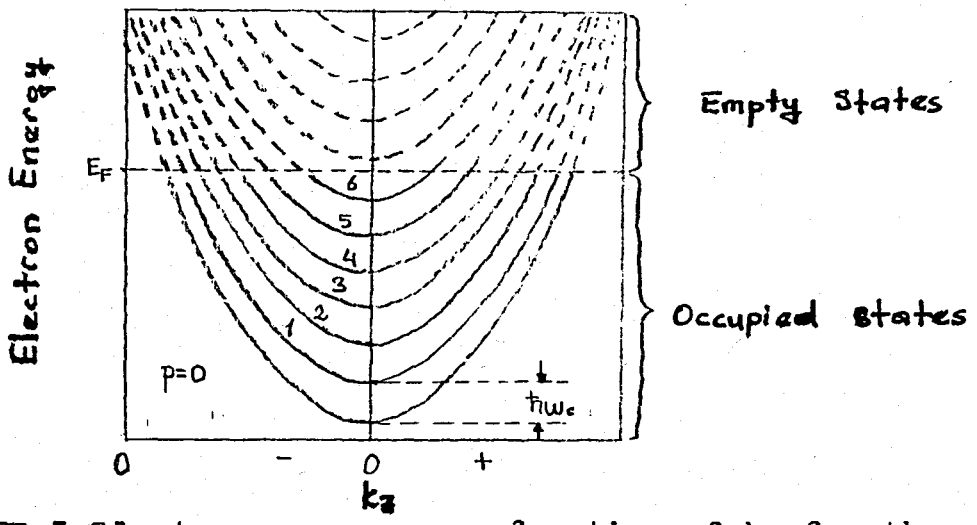


FIGURE 1 Electron energy as a function of k_z for the magnetic subbands,when the magnetic induction is B_z,(6).

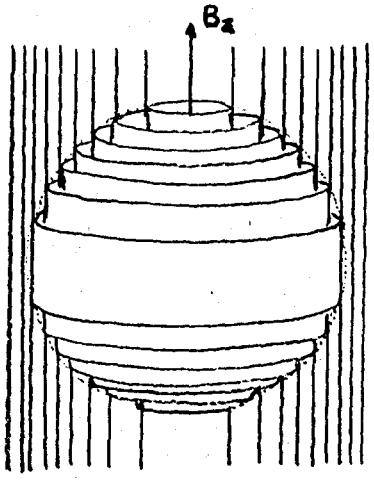


FIGURE 2 The effect of magnetic field H_z on the regions of $\vec{k}$-space which can be occupiedby electrons,according to Landau's model.

So long as ω_c is small, so is the magnetic field, there is no important consequence of this stratification of the electron states. But if, $\Delta E = \hbar\omega_c > kT$ so that the spacing is greater than the thickness of the thermal layer, we may expect various phenomena to occur as we alter the magnetic field. As H changes, the ladder of levels passes through the Fermi level; we might expect the transport properties to depend on the exact position of the ring which is nearest to the Fermi surface. For example, the conductivity is suppressed if there were happened to be no allowed level within easy reach of where the Fermi surface would normally to come.

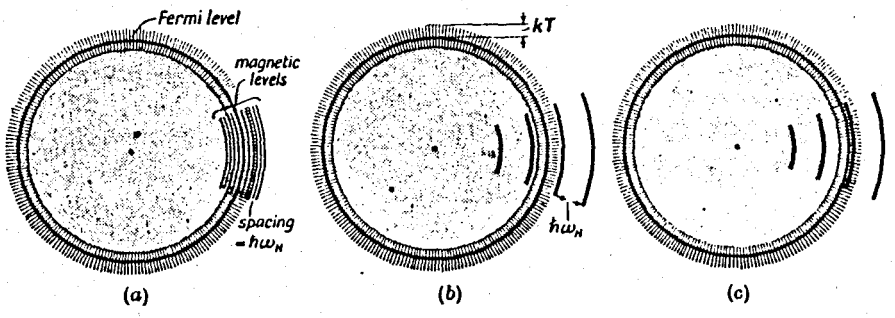


FIGURE 3 Effects of quantization of orbits (a) $\hbar\omega_c \ll kT$; (b) $\hbar\omega_c > kT$ Fermi level between the orbits; (c) $\hbar\omega_c > kT$, Fermi level near the allowed state.

It is easy to see, qualitatively, that we should expect any such phenomena to repeat themselves for successive integral values of p, where

$$p = E_F/\hbar\omega_c = E_F m^*/\hbar eH \qquad (1.3)$$

in the effective mass approximation. If this is not smeared out by temperature effects, we should expect the conductivity or resistivity to show oscillations as the field is increased. As the strength ($B_z = \mu H$) of magnetic induction increases, the

set of Landau levels depicted as cylinders in Figure 3 expands outwards.At a series of critical B_z values,these threshold energies for sub-bands coincide with the Fermi energy.Thus the Fermi energy oscillates as a function of magnetic field in response to the discontinuities in the density of states.

The Shubnikov-de Haas (SdH) effect is an oscillatory dependence of electrical resistance on magnetic induction.

Magnetoconductance oscillations in inversion layers are unique that the number of electrons can be varied and counted by changing the gate voltage.Number of free carriers in the inversion layer

$$N = k(V_G - V_T)/4\pi t_{ox}e \qquad (1.4) \quad ,(7)$$

where,k is the SiO_2 dielectric constant,V_G and V_T are the gate and threshold gate voltage for free carrier induction,respectively and t_{ox} is the oxide thickness.In the usual Shubnikov-de Haas experiments,oscillatory magnetoconductance is measured by varying the magnetic field with a fixed carrier concentration. In the inversion layer case,variation of gate voltage,thus the the carrier concentration at fixed magnetic field leads to periodic changes in conductance.In Figure 4 the constant period was prima facie evidence of two-dimensionality.In the three-dimensional systems each successively higher Landau level contains more electronic states,because the average density of states is preserved when the distribution is perturbed by magnetic field.In three-dimensional systems the density of states function is proportional to the energy in such a way that $D \propto E^{1/2}$;in one-dimensional systems the density of states

function depends on energy as well, by $D \propto E^{-1/2}$; the two-dimensional systems are the only having constant density of states function. Therefore, the constant period in magnetoconductance oscillations with respect to gate voltage is an indication of two-dimensionality.

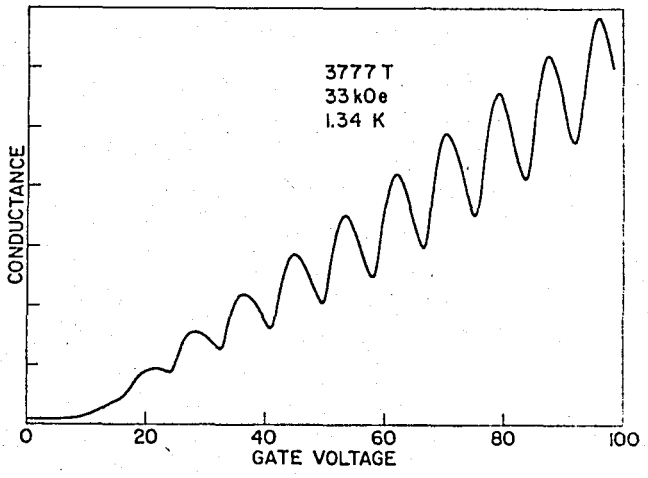


FIGURE 4 Conduction on a (100) surface of an n-channel MOSFET in the presence of a magnetic field perpendicular to the interface.

The magnetoconductance experiment made a two-dimensional model a necessity, at least at low temperatures.

B. Properties of a Two-Dimensional Electron Gas

1. Density of States

Because the density of states in n-dimensional wave vector space is $(2\pi)^{-n}$, the two-dimensional density of electron states per unit area and unit energy is

$$D(E) = 2g_v \frac{1}{(2\pi)^2} 2\pi k \frac{dk}{dE} \qquad (1.5)$$

where g_v is the valley degeneracy factor which gives the number of equivalent energy bands and where we have included a factor 2 for spin degeneracy. If the electron excitation

spectrum is given by

$$E = E_o + \hbar^2 k^2 / 2m \qquad (1.6)$$

where m is the effective mass, here assumed to be isotropic, we obtain

$$\begin{aligned} D(E) &= g_s m / \pi \hbar^2 \quad , \text{ for } E > E_o \\ D(E) &= 0 \quad , \text{ for } E < E_o \end{aligned} \qquad (1.7)$$

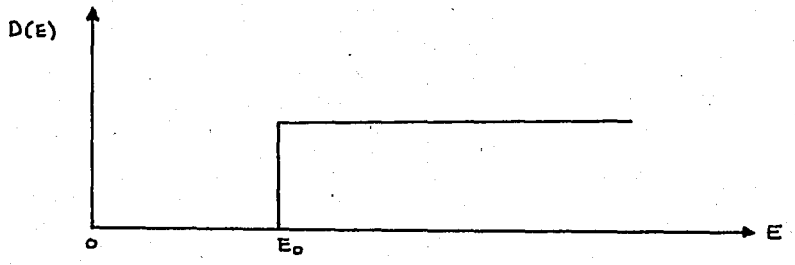


FIGURE 5 Density of states for a two-dimensional system

There will be additional step increases in the density of states if there are two-dimensional bands at higher energies. When only the lowest band is occupied, the number of electrons per unit area at absolute zero temperature is

$$N_s = \frac{g_v m}{\pi \hbar^2} (E_F - E_o) \qquad (1.8)$$

where E_F is the Fermi energy. The Fermi surface for the two-dimensional electron system is a curve, also called the Fermi line. In the simplest case of isotropic effective mass, it is a circle whose radius is the Fermi wave-vector

$$k_F = (2\pi N_s / g_s)^{1/2}. \qquad (1.9)$$

2. Polarizability and Screening

The another important aspect of a two-dimensional electron gas is its response to electromagnetic fields.

When the external charge is a point charge at the origin the screened Coulomb potential seen by the electrons is given for three-dimensional case as

$$\Phi = (Z\ e/\bar{\kappa}\ r)\ \exp(-Q_s\ r) \qquad (1.10)$$

where r is the distance between the free electron and the external charge.For the two-dimensional case,the average screened potential (8),

$$\Phi(r) \sim \frac{Z\ e(1+\bar{q}_s\ z_o)}{\bar{q}_s\ \bar{\kappa}\ r^3} \qquad (1.11)$$

This inverse-cube dependence of potential on distance is much slower than the exponential decay found in the three-dimensional case,and is one of the principle qualitative differences between two-dimensional and three-dimensional screening.

3. General Aspects of Transport in Two-Dimensional Systems

The basic machinery for transport properties of two-dimensional systems is quite similar to that used for three-dimensional systems,but some of the details are different.

A very instructive example of scattering in two-dimensions that the scattering of electrons by an unscreened Coulomb potential energy,$V(r)=-Z\ e^2/\bar{\kappa}r$,produced by a charge located in the electron plane can be solved exactly.The scattering cross sections,one of which is obtained by exact solution of the Schrödinger equation,the other which is obtained using Born approximation and the one which is obtained by classical methods,are different from each other.Each of them is valid according to the approaches used to obtain the solution. Whereas,the corresponding comparison cannot be made for three-dimensional Coulomb scattering;the Born approximation, classical,and exact cross sections all agree in that case.

C. Energy Levels and Wave Functions

1. Subband Structure

In this section we will deal with the energy levels and wave functions of electrons in semiconductor inversion and accumulation layers. In this system, after some approximations (9), the envelope function, $\zeta_i(z)$, is found to satisfy

$$\frac{\hbar^2}{2m_z}\frac{d^2\zeta_i(z)}{dz^2}+[E_i - V(z)]\zeta_i(z)=0 \qquad (1.12)$$

where m_z subject to the boundary conditions that $\zeta_i(z)$ goes to zero for $z=0$ and $z=\infty$, z being the direction perpendicular to the interface. The energy levels obtained are constant energy parabolas above an energy level. These energy levels are indicated as E_i in the Equation (1.12).

The energy levels E_i for a given value of m_z constitute a series of subband minima called a subband ladder. For differe orientations of the bulk constant energy surfaces with respect to the surface, there may be different values of m_z, and therefore different ladders. One way to name these levels is to number the lowest ladder $0,1,2,\ldots$, those of the second ladder $0',1',2',\ldots$, the third ladder $0'',1'',2'',\ldots$, and so on. If all conduction band valleys have the same orientation with respect to the surface there will be only one ladder. Because of the kinetic energy term in the Schrödinger equation the valleys giving the largest effective mass m_z for motion perpendicular to the surface will have the lowest energy.

The potential energy V(z) which enters in Equation (1.12) can be written as the sum of the three terms as

$$V(z)= V_d(z)+ V_S(z)+ V_I(z) \qquad (1.13)$$

which represent,respectively,the contributions from fixed space charges,from induced charges in the space charge layer.and from the image charges at the semiconductor-insulator interface.

Figure(6) shows the energy levels of a Si (100) inversion layer at absolute zero as the electron concentration is increased

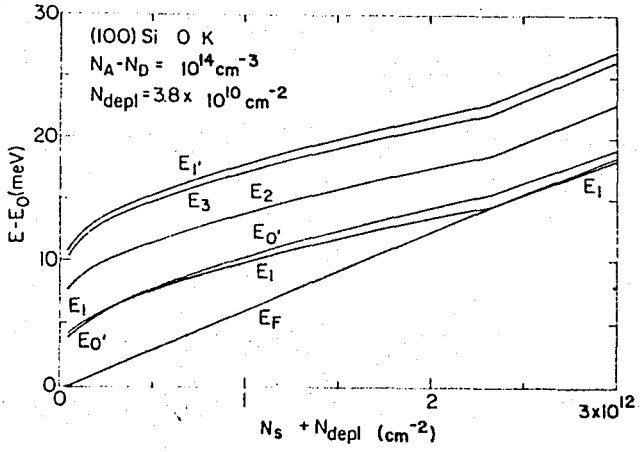


FIGURE 6 Energy level splittings and Fermi energy at 0°K for a (100) inversion layer on a p-type silicon.All energies are measured from the bottom of the lowest subband.

The energy level increase with increasing surface carrier concentration (N_s) shown in Figure(6) occurs because the average electric field in the inversion layer increases as the total space charge increases.Another important aspect of Figure(6) is the pinning of the Fermi level to the bottom of the first excited subband after they cross,accompanied by a discontinuity in their variation with N_s.The pinning is simply a consequence of the increased density of states after the second subband is occupied.

Quantum effects play an important role in the properties of the space cherge layer,especially at low temperatures and high concentrations.

One of the measures of the importance of quantum effects

is the population of subbands associated with the conduction band valleys. Classically all six valleys are equally occupied. The quantum model, on the other hand, predicts that at low temperatures, all the electrons are in the subbands associated with the two-valleys whose heavy mass is perpendicular to the interface provided N_s is not too large.

2. Triangular Potential Approximation

The potential energy $V(z)$ which entered in the Schrödinger equation (1.12) has been written as $V(z)=V_d(z)+V_s(z)+V_I(z)$. If the image potential is excluded, the remaining terms of the potential increase linearly at the semiconductor-insulator interface and then bend over to approach a constant value.

In the triangular well approximation, the potential energy is given by an infinite barrier for $z<0$, and for $z>0$ it increases linearly with z.

$$V(z)\to\infty \quad \text{for } z<0$$
$$V(z)=q\mathcal{E}z \quad \text{for } z>0, \text{where } \mathcal{E}=\frac{(N_{dep}+fN)\,q}{\epsilon_{sc}} \tag{1.14}$$

$\mathcal{E}$ is the electric field and f is a numerical coefficient. Choosing $f=1$ gives the field at the interface, $f=0$ gives the depletion contribution alone, and $f=1/2$ gives the average field in the inversion layer.

The Schrödinger equation is solved with the condition that the envelope wave function goes to zero at $z=0$ and at infinity. The solutions are called Airy functions

$$\gamma_i(z)=A_i\left\{\frac{2m_z q\mathcal{E}}{\hbar^2}\left[z-\frac{E_i}{q\mathcal{E}}\right]\right\} \tag{1.15}$$

where the eigenvalues E_i are given asymptotically for large i

by

$$E_i \cong \left[\frac{\hbar^2}{2m_z}\right]^{1/3}\left\{\frac{3\pi q\mathcal{E}}{2}\left[i+\frac{3}{4}\right]\right\}^{2/3} \quad ,i=0,1,2,.. \qquad (1.16)$$

3. Many-Body Effects

The Hartree approximation,for which each electron moves in the potential produced by all electrons neglecting many-body interactions,is valid when the electron concentration is sufficiently high,i.e.,when the average kinetic energy of electrons is much larger than the average interaction energy.

Exchange and correlation effects are the many-body effects which greatly reduce the effective repulsive potential for electrons.As a result,energies of the subbands are strongly lowered and the splitting between the lowest subband and the higher subbands is increased.The change in the density of states is also appreciable.

4. Intersubband Optical Transitions

Attempts have been made to measure the electron concentration at which a higher subband starts to be occupied by electrons.The best way to study the subband structure is to observe intersubband optical transitions.A resonance occurs when the energy of the far infrared light is equal to the subband separation.Three different methods have been employed to observe this phenomenon:infrared absorption,emission and photoconductivity.

In addition to the spectroscopic measurements of the intersubband transitions there is another way to get some information on the subband energy separations.In principle one can detect the threshold condition,at which a higher subband

starts to be populated by careful examination of the period of the Shubnikov-de Haas oscillation in magnetic fields perpendicular to the interface.Each period corresponds to the filling of one Landau level in the ground subband.When a higher subband starts to be populated the period is expected to change.Such a period change has been observed experimentally, but results do not agree with each other.

D. Transport:Extended States

1. Measurements

The problem is to derive the fundamental properties-free-carrier concentration,mobility,trap distributions,density of states,etc.-from the measured quantities-conductance,Hall-effect,field-effect mobility,magnetoresistance,capacitance,etc.

The simplest measurable quantity is the sheet conductivity,

$$\sigma = q\, N_s \mu = g_D L/W \qquad (1.17)$$

where q is the electronic charge,N_s is the areal free charge density,μ the mobility,g_D the source-drain conductance,L the length of the channel of the MOSFET structure,and W its gate width.

For inversion layers a drift mobility measurement cannot be made,but there is additional information available as compared to solids.The number of carriers can be estimated from the gate voltage dependence of the capacitance and the conductance.

Several mobilities are used to characterize MOSFETs.The effective mobility

$$\mu_{eff} = \frac{\sigma}{C_{ox}(V_G - V_T)} \tag{1.18}$$

where σ is the small signal conductivity, C_{ox} is the capacitance per unit area across the oxide, V_G is the gate voltage, and V_T is the threshold gate voltage. An overestimate of V_T results in low values for N_S and high values for μ_{eff} as compared to μ. The effective mobility can also differ from the mobility μ in the presence of trapping at the interface. A simple model gives

$$\mu_{eff} = f\mu \tag{1.19}$$

where f is the fraction of induced electrons that are free, i.e., not trapped or in the depletion charge. The field-effect mobility

$$\mu_{FE} = \frac{g_m}{C_{ox}V_D} \tag{1.20}$$

is derived from the transconductance $g_m = dI_D/dV_G\big|_{V_D}$ where I_D is the drain current and V_D the drain voltage, and g_m is normalized for geometric factors then

$$\mu_{FE} = \frac{g_m}{C_{ox}V_D} = f\mu + (V_G - V_T)\left[\mu \frac{df}{dV_G} + f \frac{d\mu}{dV_G}\right] \tag{1.21}$$

which illustrates the hazards of extracting information from the field-effect mobility. The Hall mobility also needs not equal the mobility μ.

$$\mu_H = r\mu = R_H c \sigma \tag{1.22}$$

where r is the Hall ratio, and R_H is the Hall constant. The Hall ratio needs not equal unity. It is expected to be unity for circular Fermi surfaces at low temperatures. Hall-effect measurements without an adequate theory of scattering cannot unambiguously give either the mobility or the carrier density.

In the absence of trapping the measured concentration

$$N = \frac{1}{eR_H c} = \frac{N_S}{r} \qquad (1.23)$$

can reasonably be used to define a threshold by extrapolation to zero carrier concentration.However Hall-effect measurements are moredifficult than conductance measurements,and the samples are more complex and larger.

The C-V curves-capacitance measured as a function of gate voltage can be used to measure free-carrier,depletion,and surface trapped carrier densities near threshold,at least above the temperature for freeze-out of the bulk(see,reference No 3 for excellent overview).The capacitance can be used to characterize the surface because the charge is not induced within a few angstroms of the silicon-insulator interface as it would be in a metal-insulator interface.

Another technique for counting the number of free-electrons as a function of gate voltage is to measure the Shubnikov-de Haas oscillations in the magnetoconductance at moderate fields as a function of V_G and magnetic field.Each oscillation contains the number of electrons in a Landau level which fortunately is independent of effective mass.The spacing of Landau levels gives a very accurate measurement of C_{ox}.When the nth Landau level is filled

$$n \hbar\omega_c D(E) = N_S = C_{ox}(V_G - V_T) \qquad (1.24)$$

where D(E) is the density of states function.

2. Experimental Results

In general at room temperature the electron mobility in the surface is less than in the bulk because of increased scat-

tering.However,at low temperatures it is higher,partly because the electrons are in the lowest subband so that the effective mass parallel to the surface is light and partly because they are separated from their compensating positive charge in the gate,so that Coulomb scattering ,which is effective at low temperatures is reduced.The general characteristics are illustrated in Figure(7).The differences between the samples are most striking at 4.2K,although the samples show the same general variation of mobility with N_S and T.

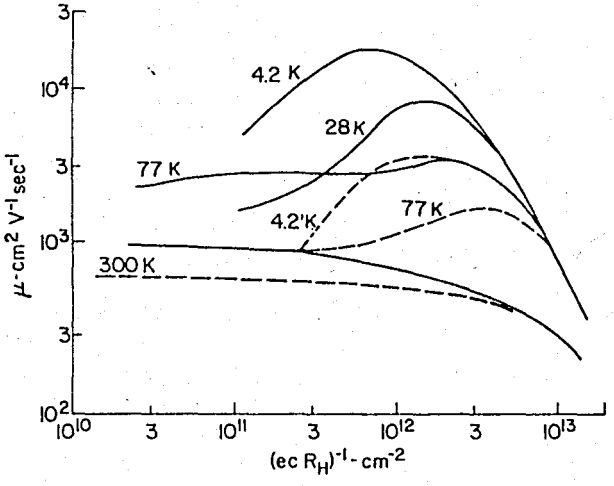


FIGURE 7 Hall mobility as a function of $N = 1/ecR_H$ for two samples.The solid curves for a sample of less oxide charge, the dashed curves for a sample of more oxide charge.

At 4.2 K there is a smooth rise in mobility.As N_s increase the mobility increases as well.This behavior can be ascribed to oxide charge scattering,which decreases as N_S increases.At high values of N_S the mobilities approach the same values and decrease as about N_S^{-2} ,this is due to the surface roughness scattering,which increases with N_S,although other mechanisms may affect the mobility to a lesser extent,especially near threshold.

3. Scattering Mechanisms at Low Temperatures

a. Coulomb Scattering

It is known that any attractive potential has a bound state in two-dimensions,in contrast to that in three-dimensional case.Thus the potential of charged centers can have a bound state after being screened by free electrons.

Many charged centers can contribute to scattering at low electron concentrations,but only a small number of charge centers,especially ones which are located near the interface, contribute to it at high electron concentrations.Usually the charged acceptors in the bulk play little role as scatterers except at extremely small electron concentrations.

The net effective mobility increases with the increase of electron concentration at low temperatures.

As has been shown before,the exchange-correlation effect is important in determining the subband structure.The same is expected to hold for the screening effect.If account is taken of the exchange and correlation,electrons do not experience so much repulsive force due to other electrons and consequently feel impurity potentials more strongly.Thus the mobility decreases.At extremely high electron concentrations like $N_s > 10^{13}\ cm^{-2}$,higher electric subbands are occupied by electrons and we have to consider the problem of multisubband transport.

b. Surface Roughness Scattering

Surface asperities at the interface are considered to be inherent to space charge layers and are expected to constitute a major cause of scattering,especially at high electron concentrations.The exact nature of this scattering is not yet known.

Figure(8) shows the mobility limited by the surface roughness scattering.The mobility decreases in proportion to N_s^{-2} at high electron concentrations.

If we include the two scattering mechanisms,charged centers in the oxide and the surface roughness,we can explain the overall behavior of experimental mobility at low temperatures.The mobility increases first,takes a maximum value around $N_s \sim 10^{12}$ cm^{-2},and then decreases with increase of electron concentration as shown in Figure(9).Quantitatively,however, the two mechanisms alone cannot reproduce the experimental behavior.The two mechanisms explain the behavior at both low and high electron concentrations,but are insufficient near the electron concantration where the mobility has a maximum.

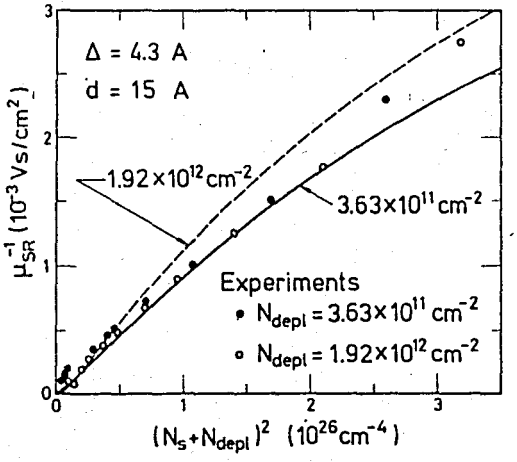
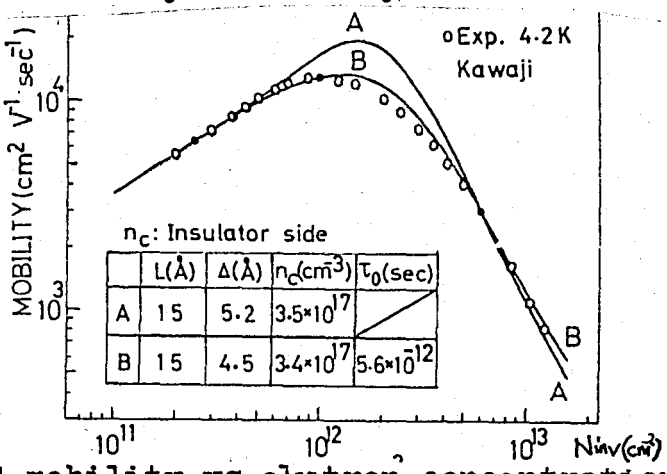


FIGURE (8) Calculated mobility limited by the surface roughness scattering.



	L(Å)	Δ(Å)	$n_c(cm^{-3})$	τ_0(sec)
A	15	5.2	3.5×10^{17}	
B	15	4.5	3.4×10^{17}	5.6×10^{-12}

FIGURE (9) Calculated mobility vs electron concentration.Curve A is obtained by combining oxide charge scattering and surface roughness scattering.Curve B by adding a third relaxation process,independent of electron concentration.

4. Multisubband Transport

So far we have mainly been concerned with the transport problem in the electric quantum limit,where only the ground subband is occupied by electrons.At high electron concentration or at nonzero temperatures,higher subbands can be populated, and we have to deal with the problem of multisubband transport. This is also true in the presence of appropriate uniaxial stresses,where subbands associated with other valleys can have the same or lower energies and electrons are transferred from the usual two valleys to other valleys.

Occupation of higher subbands leads to several effects. The transport now includes contributions from several subbands and one must also take into account intersubband scattering processes.Further,the screening effect becomes larger,since all the subbands contribute to the screening of scattering potentials.

At low temperatures intervalley scattering is expected to be sufficiently weak and can be neglected.In this case electrons in the different valleys can be regarded as independent current carriers,and there is no coupling between their distribution functions.Therefore,the mobility of i'th subband at zero temperature is given by

$$\mu_i = (e/m)\tau_i(E_F) \tag{1.25}$$

The effective mobility is given by

$$\bar{\mu} = \sum_i \mu_i \frac{N_i}{N_s} \tag{1.26}$$

where N_i is the electron concentration in the i'th subband.

So far we have assumed that there is only a single set

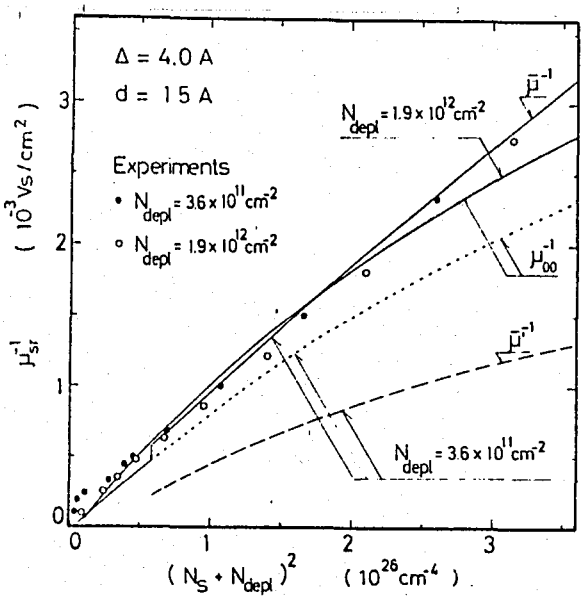
of subbands associated with equivalent valleys.If different set of subbands are occupied by electrons the total current becomes a sum of contributions of subbands of different valleys.

The mobility increases dramatically when the subband 0′ is occupied.When the excited subband is occupied,electrons in the subband have very high mobility values because effective potentials for the electrons in the excited subband become very weak.Further,the screening effect itself also becomes stronger,since electrons in both subbands contribute to the screening of scattering potentials.These two effects cause the abrupt increase of the mobility when the subband 0′ becomes occupied.

In the case of subbands 0 and 1 are occupied by electrons, we have to treat the intersubband scattering properly.In this case the mobility decreases discontinuously at some critical concentration and becomes smaller than that obtained by neglecting the occupation of excited subband;this is because the intersubband scattering is crucial and reduces the mobility especially for the excited subband considerably.

As we have seen,mobility behaves quite differently, depending on which subband is occupied by electrons first. Comparison with experimental results seems to show that subband 1 is usually the lower than the subband 0′ at high electron concentrations(in the absence of stresses).Mobility increases by more than one order of magnitude when the subbands of the different valleys are occupied by electrons at the same time.Experimentally such an anomalous increase of the mobility has not been observed,which seems to suggest the importance of other kinds of scattering mechanisms at

relatively low electron concentrations.



FİGURE(10) Calculated and experimental mobilities limited by surface roughness scattering for two different values of N_{dep}. The solid lines are obtained with two subbands, E_0 and E_1, included. The dotted line is the case in which only the lowest subband is assumed to be occupied for $N_{dep}=3.6\times10^{11}$ cm^{-2}. The dashed line is obtained if intersubband scattering is neglected.

By applying an appropriate uniaxial stress we can bring energies of bottoms of different valleys down and transfer electrons from the usual two valleys to the other set of valleys. This causes the Fermi level to come close to the bottom of subband 0, which is higher in energy than the subband 0′ at low electron concentrations under sufficiently large stresses. So far the experimental results seem to show that the valley degeneracy remains two in spite of the electron transfer effect.

5. Phonon Scattering at High Temperatures

Lattice vibrations are an inevitable source of scattering and can dominate the scattering near room temperature. In the range of electron concentrations $N_S \sim 0.5\text{-}5\times10^{12}$ cm^{-2} and around

room temperature, the mobility is known to behave like $\mu \propto N_s^{-(1/6-1/3)} T^{-(1-1.5)}$. This behavior is generally believed to be determined by phonon scattering.

Scattering by lattice vibrations can be expected to cause three different types of electonic transitions, i.e., transitions between states within a single valley via acoustic phonons (called intravalley acoustic-phonon scattering) and optical phonons (intravalley optical-phonon scattering), and transitions between different valleys (called intervalley scattering). The intravalley-acoustic phonon scattering involves phonons with low energies and almost is an elastic process. The intravalley optical phonon scattering is induced by optical phonons of low momentum and high energy. The intervalley scattering can be induced by the emission and absorption of high-momentum, high energy phonons, which can be of either acoustic or optical mode nature. Intervalley scattering can therefore be important only for temperatures high enough that an appreciable number of suitable phonons is excited or for hot electons which can emit high energy phonons.

Kawaji(10) calculated the electron mobility limited by acoustic phonons. Because of the two- dimensional energy-independent density of states, no additional temperature dependence appears in the mobility, in contrast to the usual result for three-dimensional systems. The phonon system was found to be essentially three-dimensional while the electron system is two-dimensional.

The existence of the interface does not play an important role in electron-phonon scattering in actual inversion layers e.g., a $Si-SiO_2$ system, except that the electron motion is two-dimensional, i.e., the change of direction of electrons after

collision wouldn't be in the direction perpendicular to the interface.

In general, theoretical results for phonon scattering turned out to be much larger than the experimental ones. This indicates the possibility that some other scattering mechanisms still contribute to the mobility even at room temperature and high electron concentrations. At room temperature excited subbands are occupied, intersubband scattering becomes very important and should be taken into account properly. Occupation of excited subbands associated with the two-valleys which are located in the [100] and [$\bar{1}$00] directions and which give the ground subband reduces the mobility because of the important intersubband scattering. The mobility of electrons occupying subbands associated with the other four valleys become smaller than that of electrons in the two valleys, because the decrease of scattering caused by a larger (z) is cancelled by the mass increase in the direction parallel to the surface. Consequently the mobility decreases with higher subband occupation. The effect is substantial and reduces the mobility to as low as the half of the value in the electric quantum limit and also the temperature dependence becomes steeper than the T^{-1} dependence found for the electric quantum limit. However the agreement becomes worst for N_s dependence; numerical calculations gave mobilities which were almost independent of N_s; in contrast to the $N_s^{-1/3}$ dependence in the electric quantum limit.

The theory of phonon scattering is at an unsatisfactory stage. The calculated mobility limited by acoustic-phonon scattering is not only much larger than experiments, but does not reproduce $\mu \propto N_s^{-1/3}$ behavior as well.

Intervalley phonon scattering is known to be necessary to

account for mobilities in the bulk at room temperature.As a matter of fact intervalley scattering reduces the mobility as much as a factor of three from the calculated only for acoustic phonon scattering in the bulk at 300 K.This mechanism is also important in the inversion layer and will reduce the discrepancy between the theory and the experiments discussed above.

At lower temperatures,the phonon scattering is not important to determine the resistivity.The charge and surface roughness scattering alone can approximately account for the most of the observed temperature dependence between 4.2 K and 50 K.Further,Matthiessen's rule is invalid at elevated temperatures,which casts doubt on the separation of various scattering contributions at such high temperatures.

E . Hot Electron Effects

It was observed very early that especially at low temperatures the conductance of electrons depended on the source-drain field $\mathcal{E}_D$.This result of electron heating adds the difficulty of making the conductivity or mobility measurements.

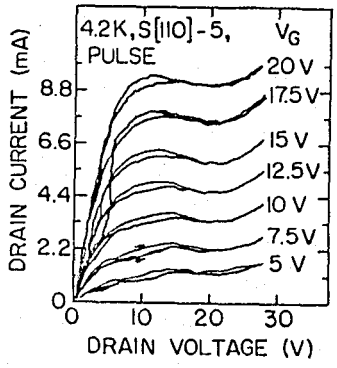
As the field increases the carrier at first can give up the energy acquired by the field by interacting with the lattice giving up a phonon.If the field continues to increase the energy acquired becomes more than the carrier can easily lose, therefore,it retains some energy.It finds a new equilibrium at a higher potential energy-in other words it has risen in the conduction band.It is now a hot electron.Further field increase causes to rise more,and one of two things happens: the carrier can ionize additional electron-hole pair,and eventually the semiconductor breaks down,or the carrier transfers to the other minima in the conduction band(11).

In GaAs,since the conduction band has a large curvature the effective mass is very low and electron mobility is high. Hence the electrons acquire a high drift momentum in an electrical field and there is a strong energy transfer to the electron ensemble leading to pronounced hot electron effects.In GaAs the hot electron phenomenon occurs at relatively low field values because of high mobility of electrons.

In silicon inversion layers,at very high electric fields even at 300 K,most of the electron energy is transferred to the lattice through optical phonons;eventually the electron velocity saturates as in the bulk.This has practical implications for device design and also allows for study of intervalley and intersubband scattering.

The saturation velocity($6x10^6$ cm/s) for the (100) surface of silicon inversion layer at 300 K is somewhat lower than the bulk value of about 10^7 cm/s.At first glance,this may seem surprising,because at high electron temperatures(~1000 K) near saturation the electrons might be expected to look almost bulklike,and they would be so far from the surface that surface effects should be minimal.Nonetheless,because of the varying potential perpendicular to the surface,the electron energy distribution averages perpendicular to the surface might be expected to be different than it would be in a constant potential.

Experiments were carried out by pulsing the drain voltage to avoid heating,and observing the drain current at a given time for different drain voltages ,asillustrated in Figure(11).



FIGURE(11) The drain current, I_D vs the drain voltage, V_D at 4.2 K on (100) Si sampled at 70 ns from the pulse front.

F. Heterojunctions Quantum Wells and Superlattices

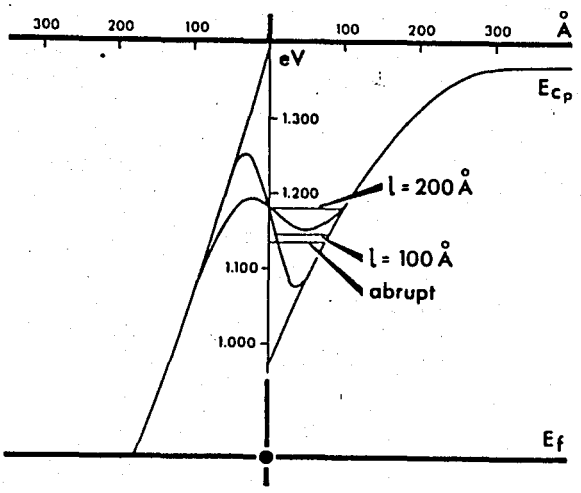
1. Structures

A superlattice arises when a periodic spatial modulation is imposed and lowers the effective dimensionality of a system. The simplest example relevant to the present discussion is the superposition of a periodic potential, as produced by a sound wave, a composition variation, or an impurity concentration modulation on an otherwise homogenous three-dimensional system.

The development of crystal growth techniques such as molecular beam epitaxy(MBE),(12),and metal organic chemical vapor deposition have made possible the growth of semiconductors with controlled changes of composition and doping on a very fine scale. Heterostructures which exhibit two-dimensional electron effects have also been made using liquid phase epitaxy, LPE,(13).

Figure(12) shows the energy-band diagram of a GaAs-AlGaAs heterojunction, with the band-gap discontinuity that arises in the presence of an abrupt composition change. The quasi-

triangular potential well can confine electrons and can lead to quantum effects similar to those seen in silicon inversion layers.



FIGURE(12) Schematic drawing of the conduction band edge at a GaAs-AlGaAs heterojunction with an abrupt composition change or a transition layer graded over 10 or 20 nm.The position of the lowest quantum level is indicated by the horizontal line for each of the three cases,(14).

The combinations of materials from which heterojunctions and therefore quantum wells and superlattices can be made is limited by material constraints such as reasonable matching of lattice parameters and absence of large densities of interface states.

2. Energy Levels

Energy levels can be calculated most easily for a quantum well-or for a thin film-if one assumes an abrupt interface and an infinite barrier height.Then,in effective-mass approximatio the energy levels are given by

$$E = \frac{\hbar^2 \pi^2}{2m_z d^2} n^2 + \frac{\hbar^2 k^2}{2m} \qquad (1.27)$$

where d is the well width, m_z is the effective mass for motion

perpendicular to the walls,k and m are the wave vector and effective mass for motion parallel to the walls.This spectrum shows increasing level spacing with increasing quantum number n,which is opposite to the behavior in a triangular well.

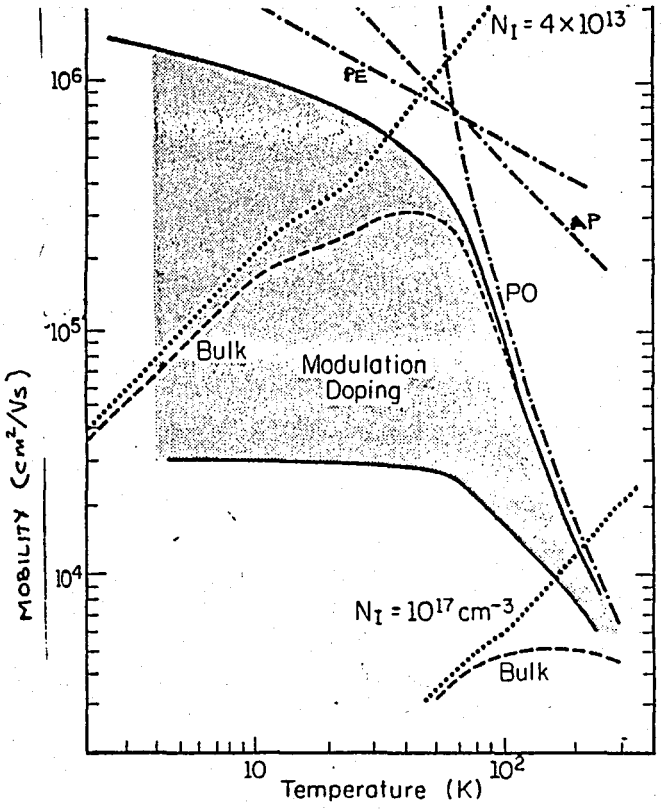
3. Transport Properties

Transport properties of carriers in superlattices are controlled in part by the same mechanisms that limit the mobility of electrons in silicon inversion layers.One important difference arises from the polar nature of most superlattice materials,such as gallium arsenide,which enhances phonon scattering.

Coulomb scattering by impurities can be reduced in superlattices,If the impurities are placed in the layers with the higher energy gap and the carriers are confined in the layers with the lower energy gap.This technique, called modulation doping(15),(16),(17),(18),allows the carriers and the impurities to be spatially separated and results in higher mobilities than would be obtained for uniform doping.Still higher mobilities can be obtained by separating the carriers from their parent ions by an undoped spacer layers,(19),(20).Low temperature mobilities considerably higher than those obtained for Si inversion layers have been obtained in this way.Part of the mobility increase can be attributed to the smaller mass of electrons in GaAs ($0.07m_o$) than in (001) Si inversion layers($0.19m_o$),where m_o is electroni rest mass.

Since the mobility is greatly enhanced by modulation doping,moreover by an undoped spacer layer,apparently to near

the ion-free values,above about 100 K,as illustrated in Figure (13).The limiting mobilities,thus,obtained by assuming that the scattering between the electron states is only that because of absorption or emission of a lattice phonon.



FIGURE(13) Electron mobility versus lattice temperature of modulation doped structures having equivalent electron concentrations larger than 10^{18} cm^{-3} in bulk GaAs.For comparison GaAs with ion concentration of $4x10^{13}$ cm^{-2} (lowest obtained)is also shown,(21).

For acoustic mode scattering the ratio of two-to-three dimensional mobility is given,(22),

$$\frac{\mu_{2D}}{\mu_{3D}} = (m^*\kappa T/2\pi)^{1/2}(3b/\hbar) \qquad (1.28)$$

where b=a/3,a being 10^{-6} cm.

The mobility is given by the relaxation time,

$$\tau' = \ell/\vec{v} \qquad (1.29)$$

where ℓ is the generalized mean free path,which is approximately parallel to $\vec{v}$,the electron velocity.The ohmic drift mobility μ and the Hall mobility are

$$\mu = (e/m^*) \langle \tau' E \rangle / \langle E \rangle \qquad (1.30)$$

$$\mu_H = (e/m^*) \langle (\tau')^2 E \rangle / \langle \tau' E \rangle \qquad (1.31)$$

where the angle brackets signify the thermal average.For two-dimensional case,(23),

$$\langle F(E) \rangle \equiv (1/kT) \int_0^\infty \exp(-E/kT)\, F\, dE \qquad (1.32)$$

In two-dimensions τ' is independent of energy E and consequently the mobilities μ_{2D} and μ_{2D}^H are equal;but in three-dimensions τ' is proportional to E,and hence μ_{3D}^H/μ_{3D} is equal to $3\pi/8$.

At low temperatures the phonon scattering consists of acoustic-mode scattering due to the deformation-coupling and to piezzoelectric-coupling.Since the acoustic-mode scattering is virtually elastic,then the mobility equals the sum of the values it would have from each of the scattering contribution alone:

$$\mu \cong \mu_{def}\mu_{piez} / (\mu_{def} + \mu_{piez}) \qquad (1.33)$$

Then we obtain an instance of Matthiessen's rule.

Intervalley scattering by optical phonons is very inelasti and ,in fact,provides the fundamental energy transfer mechanism between hot electrons and the lattice.Intervalley scattering occurs by the interaction with the large wave number phonons.

Some comparisions,especially on the role of modulation doping and the use of undoped spacer layers,have already been

made and show that phonon scattering is the limiting mechanism in the highest-mobility structures down to below 77 K,with Coulomb scattering dominance near liquid helium temperatures.

4. Magnetotransport

A magnetic field perpendicular to a layer of two-dimensional system quantizes the motion along the layer and leads to the characteristic Shubnikov-de Haas oscillations in conductance.Such experiments have been widely used to probe two-dimensionality of carriers in superlattices,(24).Note,however, that a gate voltage cannot be used to control carrier concentration as easily as in an inversion or accumulation layer of silicon system.Thus,oscillatory magnetotransport measurement have been made by varying the magnetic field rather than the carrier concentration.One of the key tests of two-dimensional character is the behavior of the oscillations as the field is tilted from the normal to the layers.A strictly two-dimensional system will have oscillations that follow the normal component of the field.

III. INTEGRATED CIRCUITS

Today, latest large-scale general purpose computers, using silicon-based technology, have already achieved speeds as high as 30 Million Instructions Per Second(MIPS). In 1990, the performance of 100 MIPS with the system delay per gate of 200 ps will be required. It may be difficult for Si-based technology to achive these values. GaAs Large Scale Integrated circuits (LSI) and Very Large Scale Integrated circuits(VLSI), however, seems the most promising device candidate for Central Processor Unit (CPU) and memory requirements for the main frames of future computers.

Therefore, the properties of GaAs and other compounds and devices designed by using these materials should be investigated and compared with one another; since they seem to be the most promising devices for the future high frequency electronic applications.

A. Compound Semiconductors Versus Silicon

1. Physics

Silicon is a remarkable material with many interesting properties. It can fulfill the requirements for most semiconductor devices, and is the material selected for the overwhelming majority of them. But, in fact, silicon is a rather poor semiconductor if judged on its physical properties alone, as shown in Table 2.1.

TABLE 2.1 A Comparison of Silicon and Gallium Arsenide

	Energy Gap (300K)	Electron Mobility
Silicon	1.12 eV	1500 cm^2/Vs
GaAs	1.40 eV	9000 cm^2/Vs

Silicon owes its predominant position to its developed technology.Many millions of dollars have been spent on devising methods of producing silicon slices and silicon devices,and it is more economic to try variations of this technology to produce new devices rather then to exploit new materials. Fortunately for those who find silicon a rather dull semiconductor there are a number of functions which it cannot fulfill.The exploitation of new semiconductors is always fascinating,but it is rewarding economically as well if we seek out these fields in which silicon operates poorly.

2. Band Structure

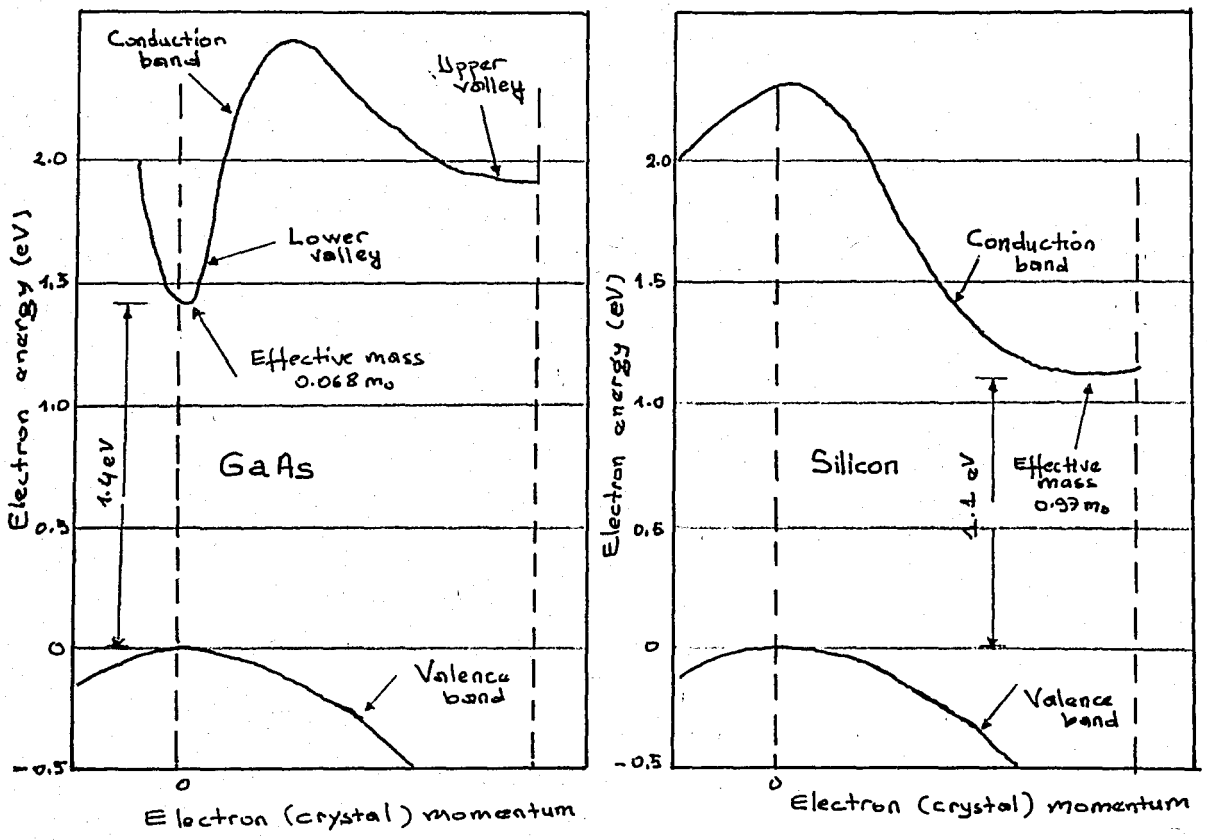
Most of the compound materials are direct gap materials, for example GaAs and InP,with valence band maximum and conduction band minimum being at the center of the Brillouin zone.

Electrons can travel through GaAs faster than they do through silicon because of the shapes of their conduction bands.The minimum point of gallium arsenide's conduction band is near the zero point of crystal-lattice momentum,as opposed to silicon,whose conduction band minimum is at high momentum.Furthermore,the rate at which the GaAs conduction-band energy increases with crystal momentum implies very high electron velocities because taking the slope of $(1/2mv^2)$

versus (mv) yields a constant times v .The curvature of energy-versus momentum profile determines the effective mass of electrons travelling through the crystal lattice,that is

$$\frac{1}{m^*_{ij}} = \frac{1}{\hbar^2}\frac{\partial^2 E(k)}{\partial k_i \partial k_j} \qquad (2.1)$$

where m^*_{ij} is the effective mass which,in general,is tensorial, and $\hbar$ is the reduced Planck constant.



FIGURE(14) Band structure of GaAs and Si,(25); GaAs is a direct gap semiconductor whereas Si is an indirect gap semiconductor.

3. Scattering Mechanisms

In a perfect lattice the carrier motion is determined by its mass and the carrier-lattice interaction.In compounds this interaction is particularly effective because the lattice is made up from charged dipoles.For example,the free gallium atom normally has three electrons with it,and the arsenic atom five. When these atoms are brought together to form GaAs there will be electron exchange.The electron cloud surrounding the molecule moves so that negative charge is passed to the gallium atom. The GaAs assembly now behaves as a dipole.We say that the compounds show polar scattering.

We should emphasize at this point the differences between an elemental semiconductor like Si and a compound like InP or GaAs.They can be summarized as in Table 2.2 .

TABLE 2.2 Summary of Features of GaAs and Si

	Mass	Transition	Scattering
Si	heavy	indirect	acoustic and polar
GaAs	light	direct	polar

4. Other Properties

The choices of properties made available by the use of compound semiconductors was broadened still further by the discovery that many compounds can be mixed in pairs to give properties intermediate between those of the two primary compounds.For example,a uniform material of composition $Al_xGa_{1-x}As$ with x controlled anywhere between 0 and 1,can be synthesized from the vapor phase.This ability to mix crystals is of particula

advantage in optical applications where one may wish to specify a wavelength accurately,as for example in a filter with a defined cut-off.

No account of compound semiconductors would be complete without some mentions of the problems of doping.The III-V compounds behave normally on the introduction of impurities. Elements from the second group dope p-type,and those from the sixth group act as donors.The fourth group elements behave in a more complex fashion since they can go on either lattice site.A good example of this is silicon which if introduced into the crystal at low temperature acts as an acceptor,while a high temperature doping gives donors.It is in fact possible to make a p-n junction in GaAs using Si as the sole dopant.

A different anomaly occurs in the doping of some III-V compounds,but this has proved extremely useful.A GaAs crystal that has less than about 5×10^{16} donors/cm^3 is readily converted to a high-resistivity condition by doping with oxygen or chromium.This material,though it contains over 10^{16} impurity centers/cm^3 ,behaves in many ways like intrinsic GaAs with a resistivity of over 10^6 ohm-cm,and a carrier concentration less than $10^7/cm^3$ .In this form it is called 'semi-insulating' GaAs.It is used as a substrate for the deposition of epitaxial layers,and finds application in certain device structures. Similar effects occur in InP.

5. Applications:Microwave Devices

It might be thought that high mobility could be exploited directly in transistors intended for operation at high frequenc A unipolar transistor(or JFET) has a certain spacing between

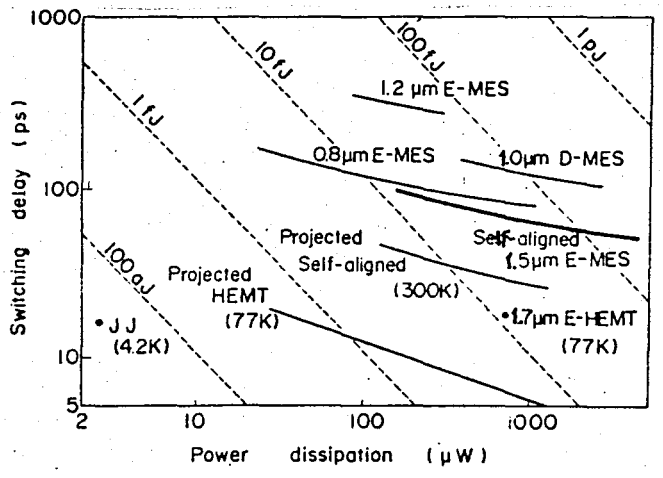
source and drain,and the frequency response is dominated by the transit time of carriers.Suitable materials are Si and GaAs and one might think that since carriers in GaAs are five or six times more mobile,the gap could be scaled accordingly. The assumption in this argument is that the carrier velocity is proportional to the electric field,and this is only true for velocities up to 10^6 cm/s.When we attempt to drive carriers in Si faster than this they meet extra resistance from lattice, and their incremental mobility falls.In direct gap compounds stranger things occur.

Since the conduction band mass at the center of the zone is low,the carriers can be accelerated to the velocities by easily attainable electric fields.As the field increases the carrier at first can give up the energy acquired by the field by interacting with the lattice,giving up a polar phonon.If the field continues to increase the carrier retains some energy. It rises in the conduction band and becomes a hot electron. Then either the semiconductor breaks down or the carriers transfer to the other minima in the conduction band if the energy separation between the lower minimum and the upper minimum is less than the energy gap of the semiconductor.Since in the GaAs ,the curvature of the upper valley is less than that of lower valley,that is,the effective mass of the electrons in the upper valley is heavier,the mobility of electrons drops after they transfer to the upper valley even thoughthe density of states increases.This causes the current,which is proportional to the carrier velocity,to decrease with increasing electric field,that is,the negative resistance.An application of this phenomenon is the Gunn diode,or Transferred Electron Oscillator.

B. GaAs Integrated Circuits

Because of its energy-band structure,gallium arsenide is an ideal medium for achieving blinding speed in electronic devices and circuits.The speed advantage of field-effect transistors(FETs) for GaAs over Si has long been recognized. Electron velocities measured in GaAs transistor structures range up to $5x10^{7}$m/s -about five times those achieved in Si devices.Furthermore,GaAs is readily available in a semi-insulating substrate form that substantially reduces parasitic capacitances,so its outstanding device speeds can be fully realized in integrated circuits.

The high speed,plus power dissipation that tends to be substantially lower than that of high-speed Si devices,accounts for the growing interest in GaAs.In a wide variety of applications,such as high data-rate communications,wide-bandwidth instrumentation,and high-speed computers,the principle focus is on the capability of GaAs ICs to operate in a speed range that is simply not available elsewhere.Cryogenic Josephson-junction technology,which offers speed comparable to those of GaAs,appears some years away from practical application.

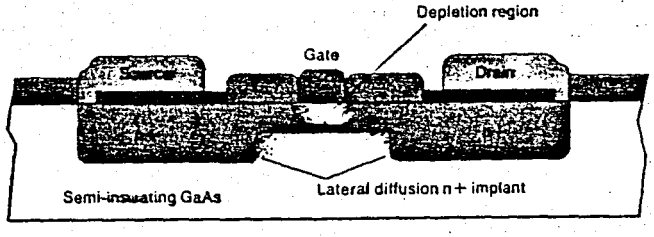


FIGURE(15) Speed and power performance of the GaAs devices.

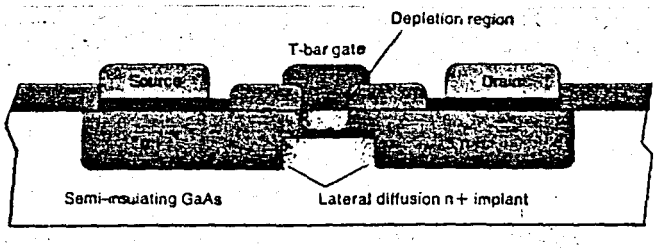
In addition,for some military and space applications,GaAs ICs offer exceptional radiation hardness.For applications with wide operating temperature ranges GaAs ICs made by standard processes can work between -200 to +200° C,and ranges up to 300° or 400° C may be possible.

1. Device Approaches

Researchers have investigated a number of different devices as the basis for building GaAs integrated circuits: the depletion-mode metal-semiconductor FET (D-MESFET),the enhancement-mode MESFET (E-MESFET),self-aligned GaAs MESFET (26), the insulated-gate GaAs FET (27),and the modulation-doped FET (MODFET),or high electron mobility transistor (HEMT), or two-dimensional electron gas FET (TEGFET),and hetero-junction bipolar transistor (HJBT).The most mature of these devices is the D-MESFET,which has been produced for ten years.



(a)



(b)

FIGURE(16) All GaAs MESFETs use ion implantation in their fabrication.a)the D-MESFET ,b) self-aligned gate E-MESFET.

In the D-MESFET (see Figure(16)-a)switching is controlled by the voltage on a one-micrometer-wide strip of gate metallization on the semiconductor passing between the source and drain regions of the device:as the gate voltage is increased the width of the depletion region under the metal gate increases and so the width of the channel,through which current flows, decreases;at the pinch- off voltage,current flow essentially stops.For logic circuits,typical pinch-off voltages are on the order of one volt.The most important difference between GaAs and Si FETs is that GaAs transconductance is very high, and the input capacitance is very low.As a result,GaAs MESFETs have a very high gain-bandwidth product,typically 15 to 20 gigahertz,leading to circuit-switching speeds in the 50ps range.

D-MESFETs have been used to build a number of different circuits,including buffered FET logic (BFL),Schottky-diode FET logic (SDFL),capacitor-coupled FET logic (CCFL),and source-coupled logic (SCL).Circuits as many as 1000 gates have been fabricated with SDFL.D-MESFET random-access memories with reported access times as short as one nanosecond and capacities of 256 bits have been fabricated using a three-FET cell.Efforts are in progress to build 1-,4-,and 16-kilobit versions. D-MESFET-based ICs give excellent performance,but they typically require two power supplies for proper operation,and they also must contain some kind of voltage-level shifting built into the logic gates to generate the negative voltages for switching from the positive drain voltages of the n-channel MESFETs.

The E-MESFET,usually used in direct-coupled FET logic circuits (DCFL),avoids the requirement for a dual power supply and level-shifting circuitry by having slightly positive pinch-

off voltages.Its structure is similar to that of the D-MESFET except that the implanted channel depth and n-type doping are designed so that the built-in potential of the metal-Schottky barrier gate normally cuts off the channel conduction.Thus,a positive gate potential of about 0.1V must be supplied for source-drain conduction to begin.

E-MESFETs are restricted to very limited logic voltage swings (typically about 0.5V) because they begin to draw excessive gate currents for gate voltages greater than about 0.7V.Because the difference between voltages representing logical 0 and 1 states must be 20 times the standard deviation of pinch-off(threshold) voltages to allow adequate margins for building LSI circuits,E-MESFET pinch-off voltage must be uniform to within 25 millivolts.This degree of control has proved exceedingly difficult to achieve consistently,particularly since the mean pinch-off voltage for each wafer must be correct within 50 or 100 mV as well.

The use of insulated-gate FET (IGFET) technology would eliminate this basic limitation and allows more flexibility in circuit design.A variety of dielectrics and techniques have been studied to find a suitable dielectric for the fabrication of GaAs IGFETs,including pyrolytically silicon dioxide,silicon nitride etc.But,because of high density of surface states, with a continuum of time constants the inversion-mode GaAs IGFETs are not feasible at present.Therefore,most development efforts on GaAs IGFETs are directed towards depletion-mode devices which operate in deep depletion-mode with a conducting bulk channel.The transconductance of GaAs IGFETs are frequency

dependent and this restricts the usefulness of deep depletion-mode GaAs IGFETs in certain applications.On the other hand the use of InP instead of GaAs proved that the InP-and InGaAsP based IGFETs can operate in inversion and/or deep depletion-modes,seeming to be superior to GaAs IGFETs for digital applications requiring full frequency response.

An additional complication in the manufacture of E-MESFETs is their need for more complex device processing than D-MESFETs. The problem is that the substantial depletion region at the surface of the GaAs,between the source or drain and gate regions,tends to pinch-off the very lightly doped channel. This leads to high-sometimes almost infinite-source resistances that degrade FET transconductance.One solution is to recess the gate slightly by etching down into thicker-than -usual channel,but this approach can reduce the uniformity of pinch-off voltages.Fujitsu Ltd. in Japan has demonstrated a self-aligned fully implanted planar GaAs MESFET approach for the source-gate and gate-drain regions,in which the gate metallization serves as a mask to define areas implanted with dopants to increase conductivity (see Figure(16)-b).The performance of such self-aligned implant device with short channel lengths is degraded by diffusion of some of the implanted atoms into the region under the gate,but a number of laboratories are working on programs to avoid this.

a. Manufacturing GaAs MESFETs

Planar implanted D-MESFETs are fabricated by implanted patterns of dopant ions directly into the semi-insulating

GaAs substrate.The substrate also provides electrical isolation between devices.Alternatively,devices can be isolated by local implants of protons, or boron or oxygen ions,which form high resistivity damaged regions near the surface of the GaAs. Metallizations are standard microwave-developed gold-germanium ohmic contacts and titanium-platinum-gold Schottky barriers.Circuits are fabricated using high-resolution photolithography,with dry etching and enhanced lift-off techniques to produce device patterns.

Because D-MESFETs have large logic voltage swings, adequate control of pinch-off voltages is not difficult in this technology.Furthermore,because the channel region is relatively thick compared with E-MESFETs,channel resistance between source and gate is not a serious problem,and so complex process steps to lower channel resistance are not required.The implanted regions of the source and drain can be placed sufficiently far from the gate electrode so that lateral diffusion does not extend under the gate depletion region,and thus the threshold voltage depends primarily on the characteristics of the channel active layer.Because of its simple processing requirements,D-MESFET technology has matured rapidly;GaAs LSI was first demonstrated with D-MESFETs in 1980.

D-MESFET circuits have high performance and large noise margins,both important for high-speed systems applications, but their power dissipation and device area are somewhat larger than those of E-MESFETs,which implies that the latter devices may form a better basis for GaAs VLSI circuits.The ultimate range of D-MESFET applications will depend on the

size of chips that can be economically fabricated and the acceptable power dissipation that can be achieved.Even though D-MESFET technology may not be universally applicable,its relative maturity ensures that it will be the basis for the first commercial GaAs ICs.

Although enhancement-mode MESFETs offer many advantages over depletion-mode devices-including the use of single power supply,simpler logic gates,and lower supply voltages that can ultimately lead to denser chips with lower power dissipation-they also require the development of complex,expensive process technology to make them work.The 'normally-off' condition of E-MESFETs requires an extremely thin,lightly doped channel region.Such thin active layers are extremely surface-sensitive, highly resistive,and difficult to control.

Probably the most serious problem is the high series resistance of the channel between the gate and the source or drain.Potential solutions include recessed gates-metal gates placed physically below the GaAs surface or junction-FET-like p-type gates below the surface-or regions of enhanced doping next to the edges of the gate.Early E-MESFET approaches, with the exception of JFETs,used etching to recess gates. This technique does not permit fine control of threshold voltages so it has not been successful in making ICs with significant scales of integration.

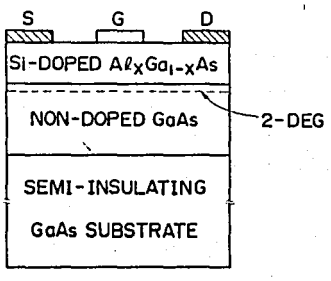
Recently many technologies have been developed to overcome these problems associated with GaAs MESFETs and so rapid these advances are that we can't mention all of them.

b. Heterojunction devices

The Modulation-doped FET (MODFET) (28),or High Electron Mobility Transistor (HEMT) (29),or Two-Dimensional Electron Gas FET (TEGFET) (30),are the different names of a device which is an alternative and seems to be superior to the GaAs MESFETs,is a lattice matched heterojunction structure and fabricated using the modulation doping technology.The mobility enhancement in Molecular Beam Epitaxy (MBE) grown modulation-doped GaAs/n-$Al_xGa_{1-x}As$ superlattice structure was first reported by Esaki and Tsui in 1969 (31),and experimentally observed by Dingle et al.(32) in 1978.

These structures consist of alternate layers of GaAs and AlGaAs with the $Al_xGa_{1-x}As$ layers selectively doped with donors.Free electrons in the $Al_xGa_{1-x}As$ layers are transferred to the undoped GaAs layers where they are confined in a quantum well about 100 Å wide because of the very high transverse electrical field.Since electrons are separated from their parent donor impurities,the GaAs layer having an interface sheet carrier density of about 10^{12} cm^{-2}.is virtually free of ionized impurities;therefore,electron mobilities are higher than those of uniformly doped GaAs of equivalent doping concentrations.Because of these properties,the modulation-doped FET technology offers substantially better performance than standard MESFET technology.Since donors are separated from free electrons,which are confined in the GaAs, the impurity scattering is greatly reduced;thus,the device offers even better performance particularly at lower temperatures where impurity scattering is efficient.this gives the MODFETs a fast turn-on characteristic-they develop

nearly their full transconductances with gate voltages only slightly above the threshold voltage.Furthermore,the thin gate insulator gives them comparatively high transconductances, and the effective electron velocities achieved are also higher than those of MESFETs at room temperature,so that potential clock speeds are also higher.Because of their speeds,MODFETs are excellent candidates for building high-performance VLSI, especially at low temperatures.



FIGURE(17) Schematic representation of a depletion-mode MODFET,where 2-DEG is for Two-dimensional Electron Gas.

These devices,which offer significant performance advantages over standard MESFETs,are usually fabricated by molecular beam epitaxy.A thin layer of AlGaAs is deposited over an undoped GaAs channel,and then the gate metallization is deposited over that layer.Processing of the MODFETs can be virtually identical to that of the standard D-MESFET, with the exception of the molecular beam epitaxy(MBE) layers and the fact that device isolation is provided by implant damage rather than by undoped semi-insulating GaAs.

The main drawback of this technology is,of course,the lack of production MBE equipment at present.Other,less obvious limitations also exist.As an enhancement technology,MODFETs

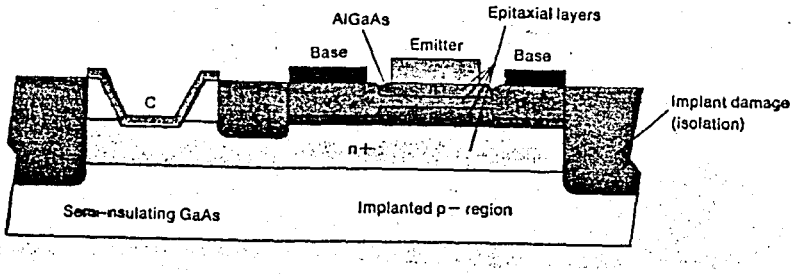
suffer from the problems of high channel resistance,threshold voltage uniformity,gate voltage swing limit,and so forth.The superior control over layer thickness offered by MBE may overcome these limitations,but that is not yet clear.

The main subject of this thesis is the modulation-doped field-effect transistors;therefore,the detailed theory of this device will be given in the next chapters.

Perhaps the most sophisticated GaAs device is the Heterojunction Bipolar Transistor (HJBT),based on very thin (approqimately 10 nm)layers of GaAs and AlGaAs,in which the proportions of Al and Ga are carefully controlled,leading to a wide energy bandgap.It holds promise for switching delays of less than ten picoseconds,even at high-current driving levels,and has the threshold immunity characteristic of all bipolar techniques.However,it has been demonstrated only in circuits of five to ten gates.

Because it is a vertical device,the HJBTs speed characteristics are dominated by the thin base region and the high electron mobility of GaAs and AlGaAs,rather than by the gate length as in FETs.

Because of the wide energy bandgap of the heterojunction emitter,base doping can be quite high without loosing current gain,and,therefore,a very thin base can be implemented,making possible potential gain-bandwidth products of 100 to 200 GHz. Another advantage is that the threshold voltage for the bipolar transistor is determined by the bandgap of the AlGaAs and GaAs layers,which are relatively constant,rather than by process parameters such as channel doping and layer thickness, as in MESFETs.



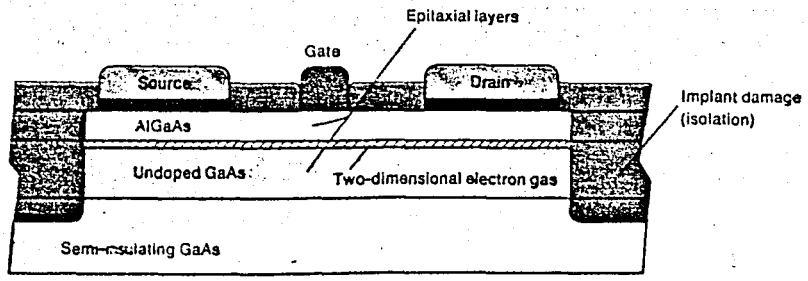
FIGURE(18) Heterojunction bipolar transistor;

The price for this performance advantage for the HJBT is the difficulty of fabrication:not only does fabrication require sophisticated MBE techniques to grow the heterojunction layers, but it also requires ion implantation both for making base region contacts and for damaging the crystal lattice to provide electrical isolation between devices.Bases must be less than 100 nm thick with carrier concentrations approaching 10^{19} cm^{-3}, and base contacts are extremely small.The width of emitter stripes must be on the order of one micrometer,and contact resistances must be kept very small to allow high-speed operation.HJBTs have all the lithographic difficulties of the MODFETs,their processing complexity is increased because both ion implantation and MBE layer growth techniques must be coordinated,and the very small,low resistance ohmic contacts of both p-and n-type are required.Although their potential performance advantages are large,process complexities will probably delay HJBT commercialization for a number of years.

A comparison summary of various high-speed technologies is shown in Table 2.3.As can be seen MODFET is superior to the other technologies.

TABLE 2.3 Device comparis on graded 1 (best) through 5.

	GaAs				Si	
	MODFET	MESFET	Vertical FET	HJBT	MOSFET	BJT
speed	1	3	1	2	5	4
power delay product	1	2	2	4	1	4
lithographic requirement	2	3	5	1	4	1
threshold control	4	4	4	1	2	1
processing complexity	2	1	4	5	3	5
material problems	4	3	3	4	1	2



FIGURE(19) Modulation-doped FET.

IV. MODELS FOR MODULATION-DOPED FETS

As we have mentioned in the preceding chapters,a new transistor has appeared on the scene,made of GaAs and AlGaAs, which now holds the record as the fastest logic switching device,switching at the speeds of ten picoseconds.The device, which is evolved from the work on GaAs-AlGaAs superlattices (thin alternating layers of differing materials sharing the same crystalline lattice),shows some superior properties because of high mobilities achieved in the GaAs due to the transfer of electrons from the doped and wider bandgap AlGaAs of higher electron affinity, to an adjacent undoped GaAs layer of lower electron affinity,a process now called modulation doping.

The topic of this chapter is this device,the MODFET; and the models developed to predict the characteristics of it.

Before describing the models a general background for MODFET is given,including modulation doping,structural paramet mobility and velocity consideration.Then models are given in the order that they appear in the international literature, and comparisons are made between them.

A. General Background

Electron devices with ever increasing speed are used either as switches or as amplifiers.The switching speed of the device is primarily determined by how fast an input

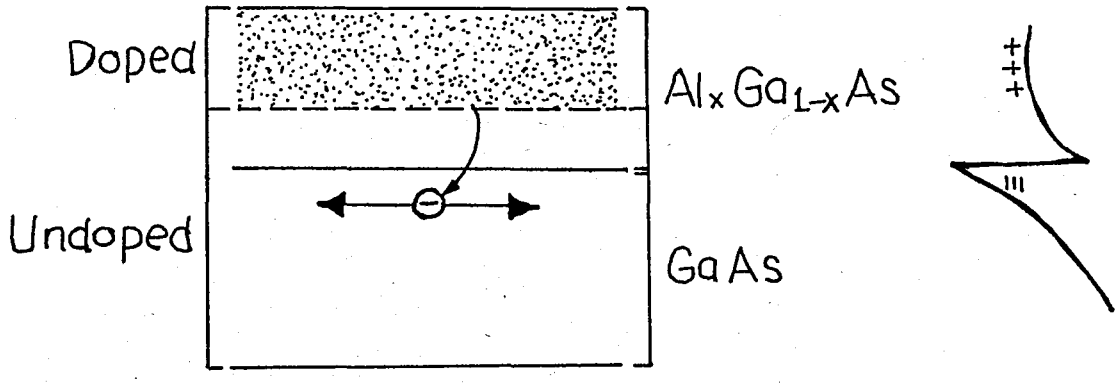
pulse can be transmitted to the output.To increase the switching speed,larger amount of current is desired,since it can charge and discharge the capacitances faster.The current path that carriers travel should be made smaller and/or somehow carriers should travel faster.This means a reduction in device geometry which in turn introduces high-field problems,i.e.,drift velocity saturation at easily attainable fields.Another way to increase current is to increase the number of carriers.

In conventional MESFETs the electrons are obtained by incorporating donor impurities which share the same space with electrons and interact with them.In general,as FETs become smaller,thinner channel layers and higher electron concentrations are required.The requirement for large electron concentration without the deleterious effects of donors can be met by novel heterojunctions.A heterojunction composed of AlGaAs and GaAs layers can be structured so that the donors are introduced only into the wider bandgap material(AlGaAs).The heterojunction line up is such that the energy of the electrons donated to the AlGaAs layer is higher in the AlGaAs than in the adjacent GaAs.

The electrons originally introduced into the AlGaAs layer then diffuse to the lower energy GaAs layer where they are confined due to the energy barrier at the heterointerface. This technique -modulation doping-is a perfect means of introducing electrons into the GaAs layer without the adverse effects of donors.Having the electrons confined at the heterointerface in a two-dimensional electron gas(2-DEG)

very close to the gate and a perfect interface leads to very high mobilities and large electron velocities at very small values of drain voltage.This,in turn,increases the switching speed.These advantages are enhanced by almost a factor of two when cooled to 77 K,which is conceivable for larger supercomputer systems.The principles of operation of MODFETs are similar to those of Si MOSFET and the models developed for MODFETs benefited greatly from Si MOSFET models.

The modulation-doped heterojunction structures are prepared by MBE.In the case of modulation-doped structures intended for FETs,single interface structures with larger layer thicknesses are used.



FIGURE(20) Single interface heterostructures used for MODFETs;

Even though the electrons and donors are separated spatially,their close proximity allows an electrostatic interaction called Coulomb scattering.By setting the donors away from the interface,Coulombic scattering by donors can be reduced.If the device is cooled to low temperatures, mobility doesn't drop as it does in other structures;because

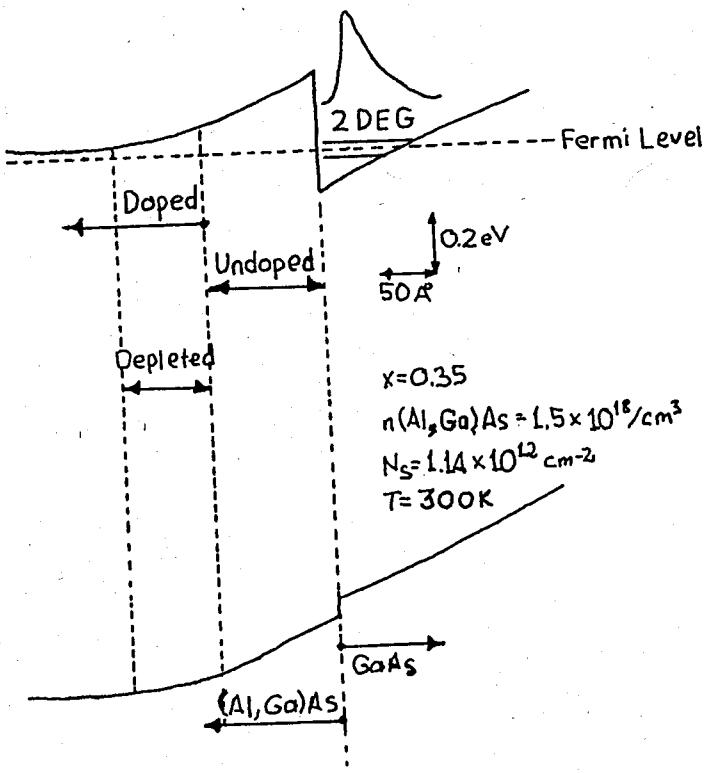
the electrons in the 2-DEG are free from ionized impurities. Only procedure that limits the mobility can be the ionized impurity scattering of bulk GaAs ionized ions at low temperatures.Although bulk impurities are present,they are so uneffective that they can hardly lower the electron mobilities because they are screened out by electrons in the 2-DEG.In fact,mobilities of 10^6 cm^2/Vs have been reported at low temperatures.Such high mobilities are not really essential for devices since the electron velocity is the dominant factor (33),(34).

Even though electrons and donors are separated,at room temperature,electrons interact with the phonons in the GaAs. The phonon scattering limited mobility in GaAs is 8500-9000 cm^2/Vs which sets an upper limit to the mobility obtainable in modulation-doped structures at 300 K.

While the basic principles of operation of MODFET and Si-MOSFET are similar,material system and details of device physics are different.The most striking difference,however, is the lack of interface states in MODFET structures.In MODFET the gate metal and the channel are separated by only about 400 Å.This,coupled with the large dielectric constant of AlGaAs as compared to SiO_2give rise to extremely large transconductances.In addition,large electron densities, about 10^{12} cm^{-2} ,can be achieved at the interface which leads to high current levels.The effective mass of electrons in GaAs is much smaller than Si and therefore electron concentrations under consideration raise the Fermi level up into the conduction band,which is not the case for Si MOSFETs.It is therefore necessary to develop a new model for the MODFET.

1. Structural Parameters

We have so far briefly discussed the multiple period and single period structures but did not address the question of which one is better for FETs.Even though the multiple period structures are a means of producing many parallel paths and thus a large conductance these structures are not used for devices.This is a result of assymetry between the properties of GaAs grown prior to and after AlGaAs growth (35).The heterointerface when the GaAs grown on AlGaAs is not of high quality which makes the inverted and multiple-period modulation-doping unattractive.

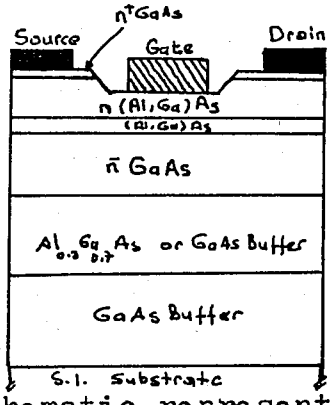


FIGURE(21) Band diagram (drawn to scale) of a single period modulation-doped heterostructure having an undoped AlGaAs spacer layer thickness of 100 Å.The electron concentration in the AlGaAs is 1.5×10^{18} cm^{-3}.

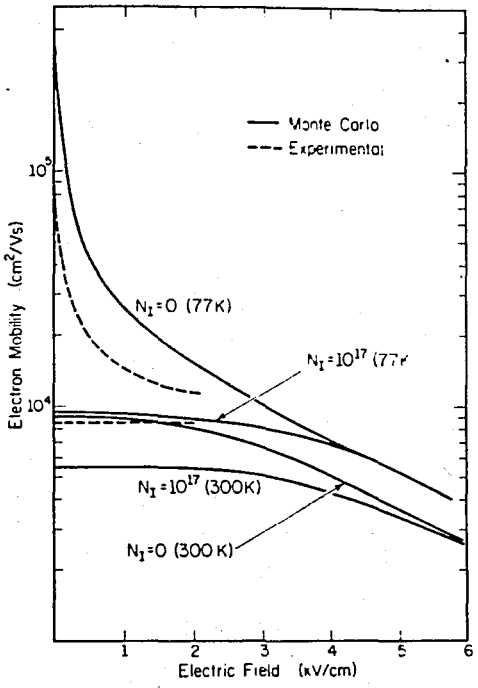
The band diagram of a normal modulation-doped structure is shown in Figure(21) where the electrons are confined at the interfacial triangular potential well have the characteristics of a 2-DEG.In addition ,higher order subbands formed in such a narrow quantum well may be populated if the electron concentration exceeds about high 10^{11} cm^{-2}.In such cases the electron mobility decreases,but improvements in the current carrying capability of the devices more than compensates for this reduction in mobility.

2. Mobility and Velocity Considerations

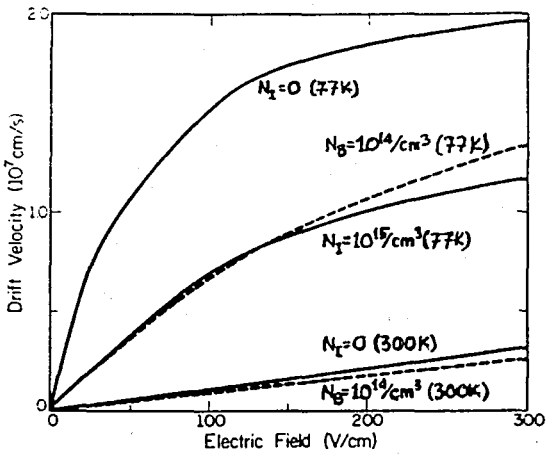
We have mentioned that the electric field in short channel devices can be very high.Since the device geometry is very small,the electric field at which the mobility is no longer a constant can be attained very easily with low bias voltages.A schematic representation of such a surface oriented device (FET) having a gate length of one micrometer is shown in Figure(22).For such short channel devices,the electric field is high,therefore the carrier drift velocity saturates and becomes the determining factor instead of the mobility.The mobility and electron velocity are given for these types of structures in Figure(23)and (24) respectively.



FIGURE(22) A schematic representation of a cross sectional view of a MODFET with the AlGaAs on top of the GaAs.



FIGURE(23) Electron mobility as a function of electric field.



FIGURE(24) Electron velocity versus electric field comparing a modulation-doped structure with undoped GaAs.

B. Modfet Models

1. HEMT (High Electron Mobility Transistor) Model

a. Device Structures and Fabrication Technologies

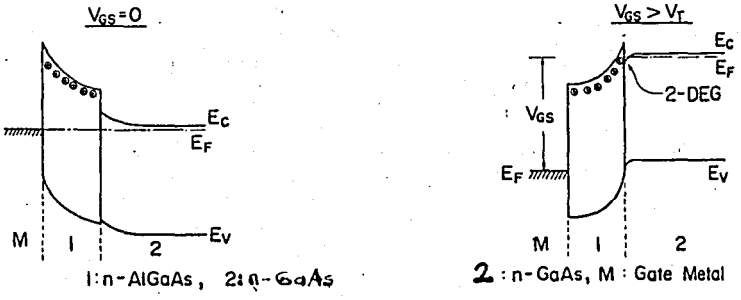
In 1980,Mimura (36) developed a transistor which they called HEMT based on the field effect control of the high mobility electrons in selectively doped GaAs/n-AlGaAs single heterojunction structures,offering new possibilities for high speed low power LSI circuits.A cross-sectional structure of Depletion-mode HEMT(D-HEMT) was illustrated in chapter 3(Figure (17)).The epilayer consisting of undoped GaAs

are grown on a (100) semi-insulating GaAs substrate by MBE. Some epilayers were grown with 6 nm thick undoped AlGaAs spacer layer inserted between the undoped GaAs and n-AlGaAs layers to enhance electron mobility (37).An AlAs mole fraction, denoted as x ,was tentatively selected as 0.3.It was expected that high AlAs exhibits crystal deterioration as a slight haze on the surface and an increase of deep traps,which make device fabrication difficult.The AlGaAs is doped with Si to the concentration of $2x10^{18}$ cm^{-3} ,the AlGaAs thickness is 600 Å and the n-GaAs thickness is 500 Å.

The process starts with etching mesa islands down to the undoped GaAs layer adjacent to the semi-insulating substrate to localize the active region.The source and drain are metallized with Au-Ge eutectic alloy and Au overlay alloying to form ohmic contact with the 2-DEG.Selective dry etching using an etching gas composed of CCl_2F_2 and 'He' was carried out to remove the the top epilayer of n-GaAs for fabrication of the recessed gate structure.Rectifying Schottky contact for the gate was provided by depositing of Ti-Pt-Au on the surface of n-AlGaAs.The n-AlGaAs layer is completely depleted by two depletion layers:the surface depletion layer produced by the gate Schottky barrier and the heterojunction interface depleti layer produced by the transfer of electrons into the adjacent undoped GaAs layer.

The basic device structure of the E-HEMT (Enhancement-mode HEMT) is similar to the D-HEMT,except that it has a thinner AlGaAs layer,even with the same doping concentration. As the AlGaAs layer thickness is reduced,the space charges

caused by donor ions in the AlGaAs layer will be insufficient to support the Schottky barrier potential.Therefore,the Schottky barrier depletion layer will be expected to extend into the undoped GaAs layer,causing upward band bending and diminishing the 2-DEG at the interface.The resultant energy band diagrams are shown in Figure(25).In this figure,the undoped GaAs is assumed be n-type.



a)in thermal equilibrium b)with positive metal gate voltag higher than the threshold voltage

FIGURE(25) Energy band diagram of an enhancement-mode HEMT.

Thus,in E-HEMT,donors in AlGaAs serve not to form the two-dimensional electron channel but to control the surface potential of the undoped GaAs layer.The positive metal gate voltage,which is higher than the threshold voltage,V_T,causes electrons to be attracted to the surface of the undoped GaAs layer,resulting in the bottom of the conduction band falling below the Fermi level,as illustrated in Figure(25).This electron accumulation layer acts as the current channel, resulting in the enhancement-mode operation.In depletion-mode operation,the two-dimensional channel already exists for zero metal gate voltage.

b. Device Modeling

(1). Carrier Concentration versus Gate Voltage

Joyce-Dixon approximation,(38),(39), is used for the Fermi energy in a degenerate heterojunction,neglecting quantum size effects.If $e\phi=E_F-E_c$ in the GaAs region, ϕ can be written in the Joyce-Dixon approximation as

$$e\phi/kT=\ln(n/N_c)+\sum_m A_m(n/N_c)^m \qquad (3.1)$$

where n denotes electron concentration and N_c is the effective density of states.The first four terms of A_m will be given by

$$A_1=1/\sqrt{8} \qquad A_2=-4.95009\times10^{-3}$$
$$A_3=1.48386\times10^{-4} \qquad A_4=-4.42563\times10^{-6} \qquad (3.2)$$

Differentiating Eqn(3.1) with respect to z,the distance from the heterojunction interface,and equating Poisson's equati

$$dE/dz=\left[e(n-N_D)\right]/\epsilon_{s2}$$

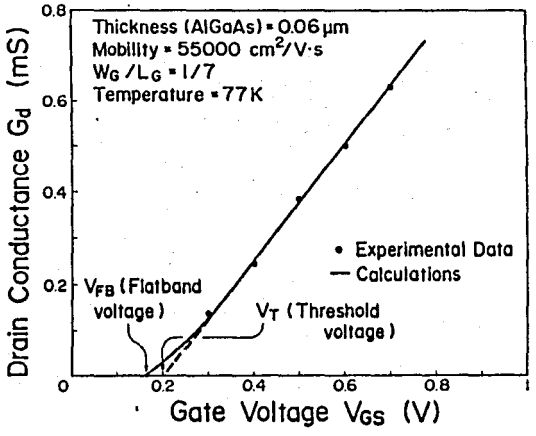
where N_D is the concentration of donors and ϵ_{s_2} is the dielectri constant of GaAs,an equation is obtained to express the relationship between the electric field E and n/N_c as

$$\frac{\epsilon_{s2}E^2}{2N_D kT}=\frac{N_c}{N_D}\sum_m B_m\left[\left(\frac{n}{N_c}\right)^m-\left(\frac{N_D}{N_c}\right)^m\right]-\ln(n/N_D) \qquad (3.3)$$

where B_m is given by

$$B_1=1-A_1(N_D/N_c),\quad B_m=A_{m-1}\left(\frac{m-1}{m}\right)-A_m(N_D/N_c) \qquad ,(m>1) \quad (3.4)$$

Equations(3.1)and(3.3) can be considered to express the fundamental equations which describe modulation of the drain conductance against gate voltage in HEMTs.From Equations (3.1) and(3.4) the relationship between E and ϕ at the heterojunction interface is obtained (z=0) with n(z=0)/N_c as a parameter.Figure(26) shows the experimental plots of the drain conductance against gate voltage at 77K.The solid line represents the result derived from assuming the effective mobility value to be 55,000 cm^2/Vs(observed Hall mobility of 2-DEG was 61,000 cm^2/Vs) and 0.16V flatband voltage value V_{FB} via Joyce-Dixon approximation.



FIGURE(26) The experimental plots of the drain conductance against gate voltage.A solid line represents the calculated results using the Joyce-Dixon approximation.

(2). Current-Voltage Characteristics(40)

The derivation of current-voltage characteristics begins with the well-known drain current expression for Si-MOSFETs:

$$I_D = -\mu_n W_G \, Q_n(x) \frac{dV(x)}{dx} \qquad (3.5)$$

where μ_n is the electron mobility, W_G is the gate width, $Q_n(x)$ is the electron charge per unit area, and $V(x)$ is the potential of the surface of the channel with respect to the source end of the gate ($x=0$). At the drain end of the gate, x becomes L_G, the gate length.

In equation(3.1), it is assumed that the electron mobility is independent of the electron concentration, which changes with the gate voltage. It was experimentally observed that the Hall mobility at 77K increases with the electron concentration over the measured concentration range. However, this dependence is fairly weak, especially for a high quality material with high electron mobility. For this reason the constant mobility approximation is used as a fairly accurate engineering approximation.

The electron charge Q_n is readily found from the charge neutrality condition expressed by

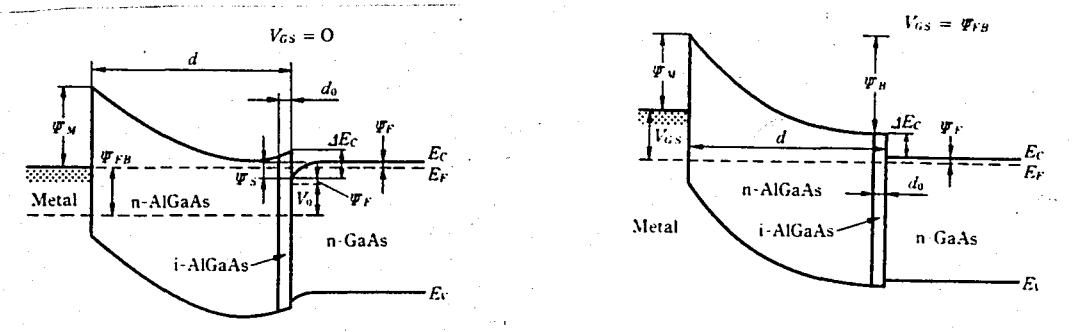
$$\Delta Q_g + \Delta Q_n = 0 \qquad (3.6)$$

where ΔQ_g and ΔQ_n represent induced charges on the metal gate and in the channel, respectively. Equation(3.6) assumes that the AlGaAs layer is completely depleted and no variation of charges in the AlGaAs takes place for any nonequilibrium conditions. The maximum AlGaAs layer thickness with respect to donor concentration is also calculated in reference (40).

The energy band diagrams used for device modeling are in Figure(27). Undoped GaAs grown in MBE was experimentally found to be lightly n-type and donor concentration was estimated to

be about $1x10^{15}$ cm^{-3}.The n-AlGaAs layer is assumed to be completel occupied with two depletion regions.The surface depletion regio results from trapping of the free electrons by surface states, and the interface depletion region results from the transfer of electrons into the adjacent undoped GaAs layer.Surface state are assumed to cause Fermi level pinning at the AlGaAs surface, and the Fermi level of the gate metal is matched to the pinning point.Here,the pinning point is assumed to be 1.2 eV below the conduction band in accordance with the empirical law(41).

The application of a voltage ($V_{GS} - \Psi_{FB}$) across the gate changes the potential across the AlGaAs layer by V_o and the surface potential by Ψ_S ,as shown in Figure(27)-a.



a)thermal equilibrium b)flatband condition

FIGURE(27) Energy band diagram used for HEMT modeling.

Hence,

$$V_{GS} - \Psi_{FB} = V_o + \Psi_S \qquad (3.7)$$

where Ψ_{FB} is the flatband potential.When $V_{GS} = \Psi_{FB}$, $Q_n(\Psi_{FB}) = 0$.

The flatband potential Ψ_{FB} can be found by noting that the quasi-Fermi level is constant throughout in Figure(27).Summing potentials,we have

$$\Psi_{FB} = \Psi_m - \left(\frac{\Delta E_c}{q} + \Psi_F + \Psi_B\right) \qquad (3.8)$$

where Ψ_m is the metal-semiconductor barrier potential, ΔE_c is the difference in the energy between the AlGaAs and GaAs conduction band edges, Ψ_F is the Fermi potential deep in the undoped GaAs bulk and Ψ_B is the built-in potential of AlGaAs at the flatband condition. Ψ_B is given by

$$\Psi_B = \frac{q n_D}{2\epsilon_{s1}} (d-d_o)^2 \qquad (3.9)$$

where n_D is the donor concentration in the AlGaAs layer, ϵ_{s1} is the permittivity of AlGaAs, d is the layer thickness and d_o is the thickness of undoped AlGaAs.

The induced incremental gate charge ΔQ_g can be expressed by

$$\Delta Q_g = C_o V_o = -\Delta Q_n \qquad (3.10)$$

where $C_o = \epsilon_y / d$ is the AlGaAs capacitance, V_o is the voltage drop across the AlGaAs layer. According to the definition, the induced electron charge ΔQ_n is given by

$$\Delta Q_n = Q_n(V_{GS}) - Q_n(V_{GS} = \Psi_{FB}) = Q_n(V_{GS}) \qquad (3.11)$$

Then, from Equations (3.10) and (3.11) we have

$$Q_n = -C_o V_o \qquad (3.12)$$

Substituting Eqn.(3.7) into Eqn.(3.12) yields

$$Q_n(x) = -C_o (V_{GS} - \Psi_{FB} - \Psi_S) \qquad (3.13)$$

Therefore, $Q_n(x)$ can be obtained as

$$Q_n(x) = -C_o \{ V_{GS} - V(x) - \Psi_{SS} - \Psi_{FB} \} \qquad (3.14)$$

where Ψ_{SS} is the surface potential at x=0, the source end of

the gate, or ($\Psi_{ss}+V(x)$) is the surface potential at any point x along the channel.

The surface potential Ψ_{ss} can be expressed by

$$\Psi_{ss} = \phi_s + \Psi_F \tag{3.15}$$

where ϕ_s denotes the surface Fermi potential. Substituting Eqns (3.8) and (3.15) into Eqn.(3.14) we have

$$Q_n(x) = -C_o\left\{V_{GS} - V(x) - \phi_s - \Psi_m + \frac{\Delta E_c}{q} + \Psi_B\right\} \tag{3.16}$$

since ϕ_s, which is a function of V_{GS}, is small compared to the other terms, Eqn.(3.13) can be approximated as

$$Q_n(x) = -C_o\left\{V_{GS} - V(x) - V_T\right\} \tag{3.17}$$

where

$$V_T = \Psi_m - \Psi_B - \frac{\Delta E_c}{q} \tag{3.18}$$

The absolute value of ϕ_s falls below one-tenth the $(V_{GS} - \Psi_{FB})$ value when $(V_{GS} - \Psi_{FB})$ becomes higher than 0.07 V at 77K for a 0.07 micrometer thick AlGaAs layer.

Substituting Eqn.(3.17) into Eqn.(3.5), the form of the integral of I_D from x=0 to $x=L_G$ with the boundary conditions $V(0)=0$ and $V(L_G)=V_{DS}$ becomes

$$\int_0^{L_G} I_D \, dx = \mu_n W_G \int_0^{V_{DS}} C_o \left\{ V_{GS} - V(x) - V_T \right\} dV(x) \tag{3.19}$$

Carrying out the integration, the drain current is obtained the

$$I_D = \frac{\mu_n W_G C_o}{L_G}\left\{(V_{GS} - V_T)\, V_{DS} - 1/2\, V_{DS}^2\right\} \tag{3.20}$$

The last term of Eqn.(3.20) can become negligible compare to the others, especially for small V_{DS}. Under these conditions

Eqn.(3.20) reduces to

$$I_D \cong \frac{\mu_n W_G C_o}{L_G} (V_{GS} - V_T) V_{DS} \qquad (3.21)$$
$$V_{DS} \to 0$$

It is noted in the Eqn.(3.21) that I_D becomes zero for a small but finite V_{DS} when V_{GS} is equal to V_T, the threshold voltage.

According to Shockley's gradual channel approximation(42) I_D saturates at the pinch-off voltage V'_{DS}, which can be given by

$$(dI_D/dV_{DS})_{V_{DS}=V'_{DS}} = 0 \qquad (3.22)$$

It can be found that

$$V_{DS} = V_{GS} - V_T \qquad (3.23)$$

and then under saturation conditions

$$I_{DS} = \frac{\mu_n W_G C_o}{2L_G} (V_{GS} - V_T)^2 \qquad (3.24)$$

Thus, a HEMT exhibits the so-called square-low characteristics.

After this point the short-channel effects are taken into account because of the electric field values which cause the velocity saturation, in such a short channel device. In the HEMT modeling the results of Turner-Wilson analysis, in which saturation is assumed to occur when the drain field reaches E_m, (43), are used and the saturation current is calculated by imposing the boundary condition that the field at the drain be equal to E_m, the critical field at which the velocity saturation is assumed to occur.

Then, the common-gate configuration is considered to simplify the analysis, and the V_{DS}

$$V_{DS} = V_{GS} - V_{GD} \tag{3.25}$$

Then, Eqn.(3.20) can be written as

$$I_D = I_o(\eta^2 - \zeta^2) \tag{3.26}$$

where,

$$I_o = \frac{\mu_n W_G C_o V_T^2}{2L_G} \tag{3.27}$$

$$\eta^2 = \left(\frac{V_S' - V_G' - V_T'}{V_T}\right)^2 \tag{3.28}$$

$$\zeta^2 = \left(\frac{V_D' - V_G' - V_T}{V_T}\right)^2 \tag{3.29}$$

where

$$V_G' = V_G - I_D R_S$$

$$V_D' = V_D - I_D(R_S + R_d) \quad \text{and} \quad V_S' = I_D R_S \tag{3.30}$$

where R_S and R_d are source and drain resistances, respectively. The quantities η and ζ denote the normalized potential differences at the source and drain respectively.

The current saturation condition is given by the boundary condition, $dU/dx = E_m$ at $x = L_G$, where U is the electrostatic potential difference between the gate and channel. The drain saturation current I_{DS} is then given by

$$I_{DS} = -\frac{2 I_o E_m L_G \zeta_{sat}}{V_T} \tag{2.31}$$

where ζ_{sat} is the value of ζ at the saturation of I_D and must also satisfy Eqn.(3.26). That is,

$$I_{DS} = I_o(\eta^2 - \zeta_{sat}^2) \tag{3.32}$$

Then, I_{DS} can be calculated from Eqns.(3.31)and(3.32) by using ζ_{sat}. If $V_T=0$,(3.20) can be written as

$$I_{DS}=\frac{\mu_n W_G C_o}{2 L_G}(V_{GS}^2 - V_{GD}^2) \tag{3.33}$$

and then I_{DS} can be expressed as

$$I_{DS} = -E_m W_G \mu_n C_o V_{GDsat} \tag{3.34}$$

where V_{GDsat} is the value of V_{GD} at the saturation of I_D and must also satisfy Eqn.(3.33) yielding

$$I_{DS}=\frac{\mu_n W_G C_o}{2 L_G}(V_{GS}^2 - V_{GDsat}^2) \tag{3.35}$$

The expression for I_{DS} can be obtained from Eqn.(3.34) and (3.35) as

$$I_{DS}=\frac{W_G \mu_n C_o}{2 L_G}\left\{ V_{GS}^2 - \left(\frac{I_{DS}}{E_m W_G \mu_n C_o}\right)^2 \right\} \tag{3.36}$$

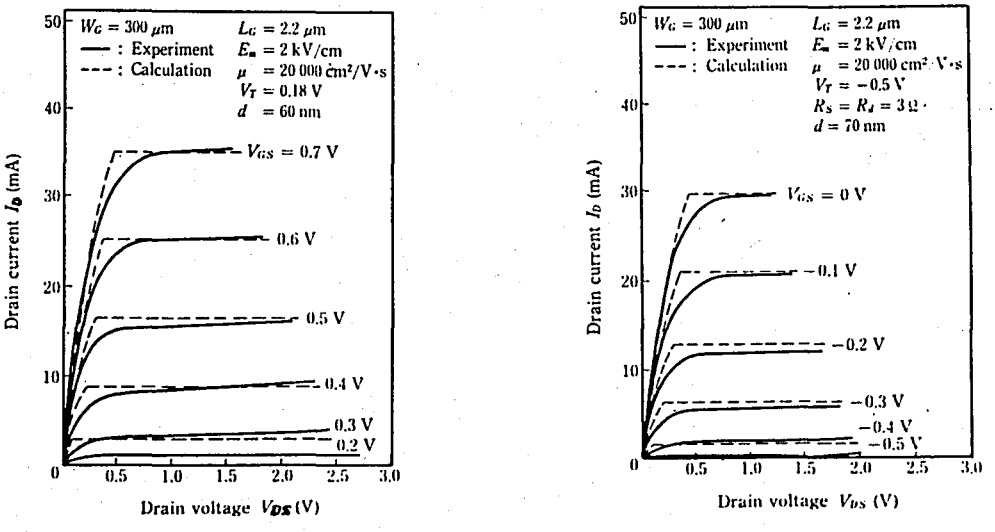
From Eqns.(3.26) amd (3.36) the current-voltage characteristics of the HEMT can be obtained.The measured drain current-voltage characteristics obtained for the short-channel (L_G =2.2 μm) D-MODE and E-MODE HEMTs are shown in Figure(28).

It is to be noted that,in the Figure(28) the short channel D-and E-HEMTs operating in the high field regime exhibit the square-law,$I_{DS}= K (V_{GS} - V_T)^2$ characteristics.

As can be seen in the Figure(28),smooth decrease in I_D about the current saturation region cannot be seen in theoretic calculations because the model assumes constant mobility below the critical electric field,which makes the electron velocity saturate.The usage of common-gate configuration in the

modeling casts some doubt on the generalization of the model into every configuration.

An overestimation of drain current in saturation region is observed;this also may be caused by neglecting the field-dependent mobility.Therefore, a very precise knowledge of scattering phenomena that limit the mobility of electrons in the 2-DEG should be known and taken into account in calculating the current-voltage characteristics.Beyond these,reasonable agreement between experimental and calculated results is observed.



a)enhancement-mode HEMT b) depletion-mode HEMT

FIGURE(28) Drain current-voltage characteristics of the HEMTs at 77K.

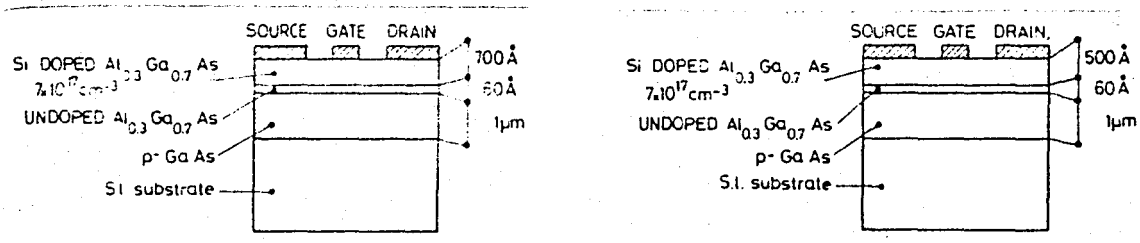
2. Two-dimensional Electron Gas FET (TEGFET) Model

a. Device Structures and Fabrication Technologies

In 1981, P.Delescluse et al. reported their first results on transport properties in GaAs-AlGaAs structures and some heterostructure FET applications working at 11 GHz, and give an 8 dB gain (44).These structures were actually modulation-doped FETs or HEMTs,but due to the high contact resistance and low material quality their results were not so successful.Shortly after,the same group published the letter about their first normally-on(D-mode) modulation-doped FET which they called as TEGFET (45).A transistor which has a noise figure of 2.3 dB,and a maximum gain of 13.2 dB at 10 GHz was reported there.A gain increase about 4dB was realized at 77K,but the characteristics of the TEGFET were found to be very sensitive to the light radiation.These instabilities in MODFETs were also reported (46), where the threshold voltage shift in MODFETs at 77K was also investigated.The causes were reported to be the traps in the AlGaAs,especially donor-complex centers which give rise to a persistent photo-conductivity effect in both bulk AlGaAs (48) and in AlGaAs/GaAs modulation-doped structures. At low temperatures,this trap has large barriers to both emission and capture of electrons due to a large lattice relaxation.At low temperatures,when the device is illuminated,the ionized donor impurity density(N_d^+) increases because of excitation of electrons from these traps lowering the threshold voltage.Under illumination,the threshold voltage lowering is partially due to steady-state generation of carrier

Thus,as the illumination is removed,the threshold voltage increases slightly.In part,the threshold voltage change with temperature is explained by a simple model based on the temperature-dependent occupation of deep donor traps in the AlGaAs layer (49).

Then,low-noise normally-on and normally-off TEGFETs, which were fabricated with source,drain and gate being directl deposited on the Si-doped AlGaAs top layer without any recess, were reported (50). A noise figure of 2.3 dB is obtained for both types with an associated gain of 10.3 and 7.7 dB for normally-on and normally-off device,respectively at 10 GHz. The planar(without any recess gate) normally-off transistor is the first enhancement-mode modulation-doped FET obtained with unrecessed gate planar structure.



a) normally-on b)normally-off

FIGURE(29) Schematic cross-sectional view of normally-on and normally-off TEGFETs,(only difference is in Si-doped AlGaAs thickness).Note that there is no recessed gate structure.

The obtention of this low-noise normally-off transistor in a nonrecess structure is surprising.In the conventional GaAs MESFET which does not have a recessed gate,the source and drain resistances were very high due to the surface

depletion of carriers;the built-in potential of the free GaAs surface is almost equal to the Schottky barrier height.It is shown that the situation is not the same with AlGaAs since very low source resistance has been obtained,such as 4Ω for a gate-to-source distance of 1.5μm. It seems that a certain aspect of the achievement of the high-performance planar E-mode TEGFET is related to low access resistance R_S.The high electron mobility in the 2-DEG certainly has a strong contribution in the reduction of R_S.On several TEGFET structures having a thin AlGaAs top layer(400-500 Å) it was noted that the ungated transistors presented a large drain current(40 mA for 300μm gate width) but became E-mode transistors once the gate was deposited.The conclusion is that there is a large difference in the free surface potential and the Schottky barrier height.The Schottky barrier height has been found to be 1 eV.The surface potential of AlGaAs was determined as 0.33 ± 0.04 eV.This shows that the surface depletion for AlGaAs is not a severe problem with the Schottky barrier gate potential of 1 eV and therefore,normally-off operation with planar structure can be obtained.Since a recessed gate involves increased device processing complexity,planar, unrecessed gate structure is important in achieving high level of integration.Recently,a wafer which has approximately zero threshold voltage entirely was reported(51),(52).This zero threshold voltage,together with the unrecessed gate structure make the logic circuit applications feasible in LSI level.

The fabrication process begins with growing epitaxial layer of p-type GaAs of 1μm thick by MBE on a Cr-doped semi-

insulating substrate.All epitaxial layers are grown by molecular beam epitaxy(MBE).Then an undoped $Al_{0.3}Ga_{0.7}As$ spacer layer of 60 Å thick And Si-doped $Al_{0.3}Ga_{0.7}As$ layer($n=7x10^{17}$ cm^{-3}) of 700 Å thick are deposited successively.The wafer is cut into two parts:the first is processed in the state as received,and the second is given a slight chemical etching to remove approximately 200 Å,before device processing.Both parts are identically treated:AuGe:Ni are first deposited and annealed to form source and drain contacts.After mesa definition and etching,Al or Au gate is deposited directly on the AlGaAs top layer without any recess.Source and drain spacing is 4μm, gate length and width are 0.8 and 300μm,respectively.All the tested transistors which were fabricated the first part of the the wafer were of the normally-on type whereas all those on the other half were normally-off.

b. TEGFET Model (53)

In this model,the subband splitting in the 2-DEG is taken into account.The analytical treatment given in the model is valid for both p-type and n-type GaAs cases.

(1). Treatment of the 2-DEG Layer

The object of this section is the calculation of the Fermi level position in the 2-DEG,the free electron surface density,and the electric field at the interface.

The calculation starts from the assumption of a quasi-constant electric field $\mathcal{E}$ in the potential well(triangular well approximation),and takes two subbands into account.Figure (30) gives the used notations (a p-type small gap semiconductor

is assumed).

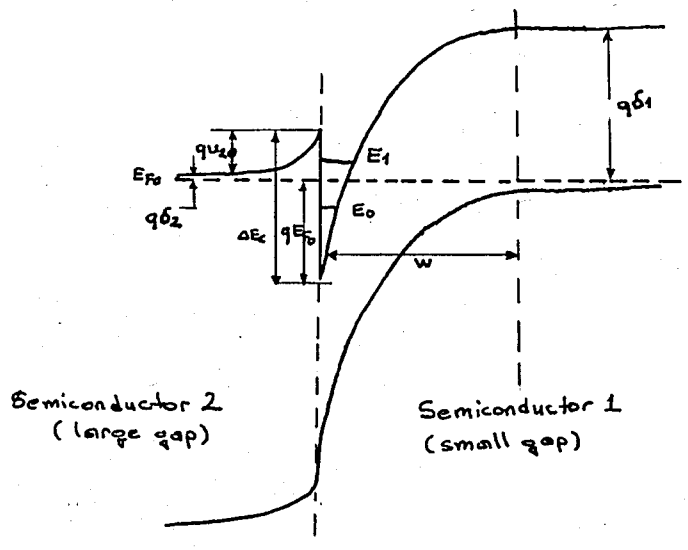
The solution for the longitudinal quantized energy is then well approximated by the formula

$$E_n(eV) \cong \left(\frac{\hbar^2}{2m_\ell^*}\right)^{1/3} \left(\frac{3}{2}\pi q \mathcal{E}\right)^{2/3} \left(n+\frac{3}{4}\right)^{2/3} \qquad (3.37)$$

where m_ℓ^* is the longitudinal effective mass. For GaAs and considering only the lower and excited subbands, one obtains

$$\begin{aligned} E_o &= 1.83\times10^{-6}\ \mathcal{E}^{2/3} \quad (eV) \\ E_1 &= 3.23\times10^{-6}\ \mathcal{E}^{2/3} \quad (eV) \end{aligned} \qquad (3.38)$$

where $\mathcal{E}$ is in V/m. The numerical coefficients of Eqn.(3.38) are modified to be in agreement with the most important published experimental results.



FIGURE(30) Al Ga As-GaAs(p) heterojunction at equilibrium and isolated.

First a relation between the interface electric field $\mathcal{E}_{i1}$ and the electron sheet concentration is established.

(a). p-type Case

In the small gap semiconductor, the electric field obeys the Poisson equation

$$\frac{d\mathcal{E}_1}{dx} = -\frac{q}{\epsilon_1}\left(n(x)+N_{A1}\right) \qquad (3.39)$$

n(x) being the bulk free electron concentration and N_{A1} the ionized acceptor density in the small gap semiconductor. Integration between the limit of the depletion region ($\mathcal{E}_1=0$) and the interface ($\mathcal{E}_1=\mathcal{E}_{i1}$) gives

$$\epsilon_1\mathcal{E}_{i1} = q\, n_s + q\, N_{A1} w_1 \qquad (3.40)$$

where ϵ_1 is the dielectric permittivity in the small gap semiconductor, n_s the 2-DEG electron density, and w_1 the space charge region width. For MESFET applications, where a good mobility is required, N_{A1} is chosen very low to reduce the impurity scattering in the 2-DEG layer. Then, as a good approximation

$$\epsilon_1\mathcal{E}_{i1} \cong q\, n_s \qquad (3.41)$$

(b). n-type Case

$$\frac{d\mathcal{E}_1}{dx} = -\frac{q}{\epsilon_1}\left(n(x)-N_{D1}\right) \qquad (3.42)$$

where N_{D1} is the ionized donor density in the GaAs. If d_1 is the small gap semiconductor layer width and if $\mathcal{E}(d_1)\approx 0$ (neutrality at d_1) the integration of (3.42) gives

$$\epsilon_1\mathcal{E}_{i1} = q\, n_s - q\, N_{D1}\, d_1 \qquad (3.43)$$

If N_{D1} and d_1 are chosen sufficiently small

$$\epsilon_1\mathcal{E}_{i1} \cong q\, n_s \qquad (3.44)$$

that is the same result as for the p-type case.

From these assumptions and (3.38),(3.41)and(3.44) the subband positions are given by the relations

$$E_o \approx \gamma_o (n_s)^{2/3}$$
$$E_1 \approx \gamma_1 (n_s)^{2/3} \qquad (3.45)$$

where γ_o and γ_1 are adjustable parameters which otherwise would be given by

$$\gamma_o = 2.26 \times 10^{-12}$$
$$\gamma_1 = 4 \times 10^{-12} \qquad \text{(systeme international- SI)} \qquad (3.46)$$

The treatment of the 2-DEG layer will be complete when a relation between n_s and Fermi level position is established. The density of states(associated with a single quantized energy level)for a two-dimensional system is a constant

$$D = \frac{q\, m^*}{\pi \hbar^2} \qquad (3.47)$$

(spin degeneracy-two,valley degeneracy-one).For a two-dimensional density of states D between E_o and E_1 ,and equal to 2 D for energies greater than E_1,using the Fermi statistics

$$n_s = D \int_{E_o}^{E_1} \frac{dE}{1+\exp(\frac{E-E_F}{kT})} + 2D \int_{E_1}^{\infty} \frac{dE}{1+\exp(\frac{E-E_F}{kT})} \qquad (3.48$$

applying the easily verifiable formula $\int \frac{dx}{1+\exp(x)} = -\ln(1+e^{-x})$, n_s is obtained

$$n_s = DkT \ln\left[(1+\exp(\frac{E_F-E_o}{kT})) \; (1+\exp(\frac{E_F-E_1}{kT}) \;) \right] \qquad (3.49)$$

which at low temperatures, reduces to

$$n_s = D(E_F - E_o) \quad \text{or,} \tag{3.50}$$

$$n_s = D(E_1 - E_o) + 2D(E_F - E_1) \tag{3.51}$$

when the second subband is, respectively, unoccupied or occupied. From the published results performed at low temperatures by Shubnikov-deHaas or cyclotron resonance experiments, an estimation of γ_o and γ_1 can be done. In the p-type case they are found as

$$\gamma_o = 2.5 \times 10^{-12}$$

$$\gamma_1 = 3.2 \times 10^{-12} \quad \text{(SI)} \tag{3.52}$$

and from the measured cyclotron mass

$$D = 3.24 \times 10^{17} \ m^{-2} V^{-1} \tag{3.53}$$

(2). Equilibrium-Isolated case

Figure (30) shows the band diagram of the studied heterostructure in the p-type case at equilibrium and isolated from the influence of any external contacts. Two of the subbands E_o, E_1 are shown but their position is only illustrative. In the calculation the presence of undoped AlGaAs spacer layer of thickness e is taken into account. Electric displacement vector at the interface in the large gap semiconductor is computed by assuming the total depletion approximation in its space charge layer.

The voltage $V_2(x)$ in the space charge region of the semiconductor 2 obeys the Poisson equation

$$\frac{d^2V_2}{dx^2} = -\frac{q}{\epsilon_2} N_2(x) \tag{3.54}$$

Taking the heterojunction interface as origin, the conditions

$$V_2(0)=0$$

$$\left(\frac{dV_2}{dx}\right)_{x=-w_2}=0$$

$$\left(\frac{dV_2}{dx}\right)_{x=0}=-\mathcal{E}_{i2}$$

where w_2 is the space charge layer width, one obtains successively

$$\mathcal{E}_{i2} = -\frac{q}{\epsilon_2}\int_0^{-w_2} N_2(x)\,dx$$

$$V_2(-w_2)=V_{20}=\mathcal{E}_{i2}w_2-q/\epsilon_2\int_0^{-w_2}dx\int_0^{x} N_2(x')\,dx' \qquad (3.55)$$

For our case

$$N_2(x)=0 \quad ,\text{for} \quad -e<x<0$$

$$N_2(x)=N_2 \quad ,\text{for} \quad x<-e \quad \text{then,}$$

$$\epsilon_2\mathcal{E}_{i2}=qN_2(w_2-e) \qquad (3.56)$$

$$V_{20}=\frac{qN_2}{2\epsilon_2}(w_2^2-e^2) \qquad (3.57)$$

$$\epsilon_2\mathcal{E}_{i2}=\sqrt{2q\epsilon_2N_2V_{20}+q^2N_2^2e^2}-qN_2e \qquad (3.58)$$

By examination of Figure(30),

$$V_{20}=\Delta E_c/q-\zeta_2-E_{FD}/q \qquad (3.59)$$

neglecting interface states we have, according to Gauss's law,

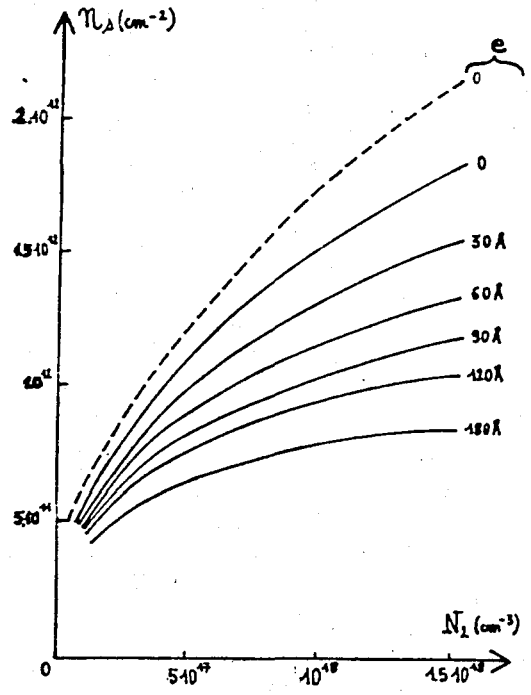
$$\epsilon_2\mathcal{E}_{i2}\cong\epsilon_1\mathcal{E}_{i1}\cong qn_S \qquad (3.60)$$

then from (3.41),(3.49),(3.58),and(3.60) we must solve

$$\sqrt{2q\epsilon_2N_2V_{20}+q^2N_2^2e^2}-qN_2e=qn_S=qDkT\ln\left[\frac{(1+\exp(\frac{E_{F0}-E_{c0}}{kT}))}{(1+\exp(\frac{E_{F0}-E_{i1}}{kT}))}\right] \qquad (3.61$$

The solution is obtained numerically according to the following procedure.It starts from an arbitrary low value of E_{Fo}(which can be negative),from(3.58),(3.59),and(3.60) n_s is deduced and E_o and E_1 computed with(3.45).The deduced value for n_s must also satisfy (3.49) and,if it is not the case,E_{Fo} is increased until (3.61) is verified.The result in the p-type case (using the and values given by (3.46)),x=0.3,and various values of e is shown as a function N_2(AlGaAs doping density) at T=300K in Figure(31).In this figure,the curve, which corresponds to the case where two-dimensional behavior is ignored,is also reported.

The observed decrease in n_s at low temperatures is attribute to carrier freeze-out in AlGaAs (reduction of the number of ionized impurities).But as shown before,this is not the only mechanism responsible for temperature dependence of n_s.



FIGURE(31) Sheet concentration of the 2-DEG.GaAs is taken p-type ($N_{A_1}=10^{14}$ cm^{-3}) and Al concentration is 0.3 in AlGaAs.Full curves correspond to various thicknesses e ,dash curve to the case e=0 but ignore the two-dimensional character of the electron sheet.

(3). Charge Control by a Schottky Gate on AlGaAs Layer

Figure(32) shows the band diagram of the heterostructure submitted to influence of a Schottky gate in contact with the large bandgap semiconductor.It is supposed that the interpenetration of the two depletion layers is as effective as in the HEMT model.With the notations used in the Figure(32) the electrostatic potential obeys the Poisson equation with

$$N_2(x)=0 \quad , \text{ for } -e<x<0$$
$$N_2(x)=N_2 \quad , \text{ for } -d_2<x<-e$$

The origin is also taken at the interface and $V_2(0)=0$ is arbitrarily chosen.A double integration gives

$$V_2(-d_2) = -v_2 = \mathcal{E}_{i_2} d_2 - \frac{q}{\epsilon_2}\int_o^{-d_2} dx \int_o^{x} N_2(x')\, dx'$$

that is,

$$v_2 = \frac{q N_2}{2\epsilon_2}(d_2-e)^2 - \mathcal{E}_{i_2} d_2$$

$$\epsilon_2 \mathcal{E}_{i_2} = \frac{\epsilon_2}{d_2}(V_{P_2} - v_2) \qquad (3.62)$$

where

$$V_{P2} = \frac{qN_2}{2\epsilon_2}(d_2-e)^2 \qquad (3.63)$$

By examination of Figure(32) the relation,

$$v_2 = \phi_m - V_G + \frac{E_F}{q} - \frac{\Delta E_c}{q} \qquad (3.64)$$

then

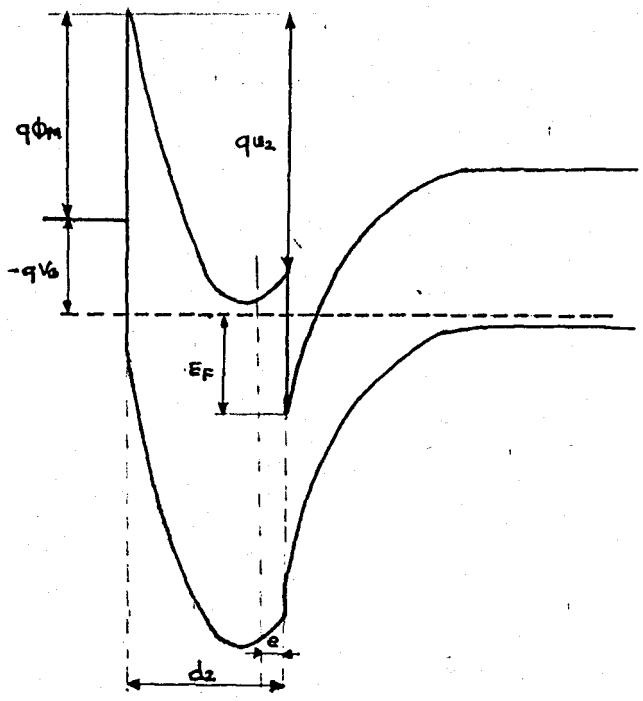
$$\epsilon_2 \mathcal{E}_{i_2} = \frac{\epsilon_2}{d_2}\left(V_{P_2} - \phi_m - \frac{E_F}{q} + \frac{\Delta E_c}{q} + V_G\right) \qquad (3.65)$$

In the absence of interface states we have then,according

to (3.60),

$$Q_S = qn_S = \frac{\epsilon_2}{d_2}\left(V_{p_2} - \phi_m - \frac{E_F}{q} + \frac{\Delta E_c}{q} + V_G \right) \qquad (3.66)$$

Here, as in HEMT model, the E_F/q term, which is a function of V_G, is neglected because of the reason that it is small when compared with the other terms. As can be recalled in the HEMT model the E_F/q term was represented by the term ϕ_s.



FIGURE(32) AlGaAs-GaAs(p-type) heterojunction in the 2-DEG control regime by a Schottky gate.

then, the approximate result is obtained as

$$Q_S \cong \frac{\epsilon_2}{d_2}(V_G - V_{off}) \qquad (3.67)$$

where

$$V_{off} = \phi_m - \frac{\Delta E_c}{q} - V_{p_2} \qquad (3.68)$$

is called the 'off voltage' which annihilates the 2-DEG. Having neglected the E_F/q to obtain these results, it is realized that

(3.67)and (3.68) are insensitive to the exact positions of the subbands.

If the interface charges Q_i cannot be neglected,(3.67) remains valid but (3.68) becomes

$$V_{eff} = \phi_m - \Delta E_c/q - V_{p_2} - (d_2/\epsilon_2) Q_i \qquad (3.69)$$

For a given large semiconductor layer width,there exists a threshold voltage V_{Gth} separating the charge control regime from the equilibrium state.It was obtained by equilizing the two expressions of $\epsilon_2 \mathcal{E}_{i2}$ (3.58) and (3.65) for the equilibrium value E_{F_o} of the Fermi energy.The result can be put in the form

$$V_{Gth} = \phi_m - \delta_2 - \left(\sqrt{\frac{qN_2 d_2^2}{2\epsilon_2}} - \sqrt{(\Delta E_c/q - \delta_2 - E_{Fo}/q) + \frac{qN_2 e^2}{2\epsilon_2}} \right)^2 \qquad (3.70)$$

where (3.59) has also been used.

(4). FET Applications

If $V_c(y)$ is the channel voltage under the gate at abscissa y (y is the direction parallel to the current flow), and V_G the gate voltage,the effective voltage for charge control at y is

$$V_{eff}(y) = V_G - V_c(y) \qquad (3.71)$$

and(3.67) must be written as

$$Q_s(y) \cong \frac{\epsilon_2}{d_2} (V_G - V_c(y) - V_{off}) \qquad (3.72)$$

The channel current expression at y is

$$I_D = Q_S(y) Z\, v(y) \tag{3.73}$$

where Z is the gate width, and v(y) the electron velocity at y.

Then, because of the lack of knowledge of the limiting mechanisms of the electron velocity in such systems, it was only assumed that the electron velocity saturates at a critical field, $\mathcal{E}_c$, up to which the electron mobility was assumed to be constant (using Turner-Wilson approximation).

According to Turner-Wilson approximation,

$$\begin{aligned} v &= \mu \mathcal{E} \quad \text{, for} \quad \mathcal{E} < \mathcal{E}_c \\ v &= v_S \quad \text{, for} \quad \mathcal{E} \geqslant \mathcal{E}_c \end{aligned} \tag{3.74}$$

where v_S is the electron saturation velocity. At field values less than $\mathcal{E}_c$,

$$I_D = \mu Z \frac{\epsilon_2}{d_2} (V_G - V_c(y) - V_{off}) \frac{dV_c}{dy} \tag{3.75}$$

where $dV_c/dy = \mathcal{E}$ is the electric field.

The current I_D being conservative and the channel voltage $V_c(y)$ increasing from source to drain, the electric field is maximum close to the drain and the velocity saturation will occur first at the drain side of the gate region. First the case of very small drain voltage V_D (linear region of I_D-V_D characteristics) is considered. From (3.75),

$$I_D = \mu Z \frac{\epsilon_2}{d_2} (V_G - V_{off}) \frac{V_c(L) - V_c(0)}{L} \tag{3.76}$$

where L is the gate length. At this point R_S and R_D, being respectively the source and drain access resistances, are incorporated.

$$V_c(0)=R_S I_D$$
$$V_c(L)=V_D-R_D I_D \qquad (3.77)$$

Then, from (3.76) and (3.77),

$$\frac{V_D}{I_D}= R_S+R_D+\frac{L\, d_2}{\mu Z \epsilon_2 (V_G-V_{off})} \qquad (3.78)$$

and the FET acts as a pure controllable resistor.

At drain voltages such that the drain side electric field is less than $\mathcal{E}_c$, the integration of (3.75) gives

$$V_c(y)=V_G-V_{off}-\sqrt{(V_G-V_{off}-V_c(0))^2-\frac{2d_2 I\, y}{\mu Z \epsilon_2}} \qquad (3.79)$$

The electric field at y, $\mathcal{E}(y)= dV_c/dy$ is then easily obtained. Expressing the condition $\mathcal{E}(L)=\mathcal{E}_c$ one obtains the saturation current:

$$I_S=\frac{Z \epsilon_2 v_S}{d_2}\left(\sqrt{\mathcal{E}_c^2 L^2+(V_G-V_{off}-R_S I_S)^2}-\mathcal{E}_c L\right) \qquad (3.80)$$

For a long-gate FET, i.e., $\mathcal{E}_c L \gg (V_G-V_{off}-R_S I_S)$, (3.80) reduces to

$$I_S=\frac{\mu Z \epsilon_2}{2d_2 L}(V_G-V_{off}-R_S I_S)^2 \qquad (3.81)$$

and for a short-gate FET, i.e., $\mathcal{E}_c L \ll (V_G-V_{off}-R_S I_S)$, the control is linear

$$I_S=\frac{Z \epsilon_2 v_S}{d_2}(V_G-V_{off}-R_S I_S-\mathcal{E}_c L) \qquad (3.82)$$

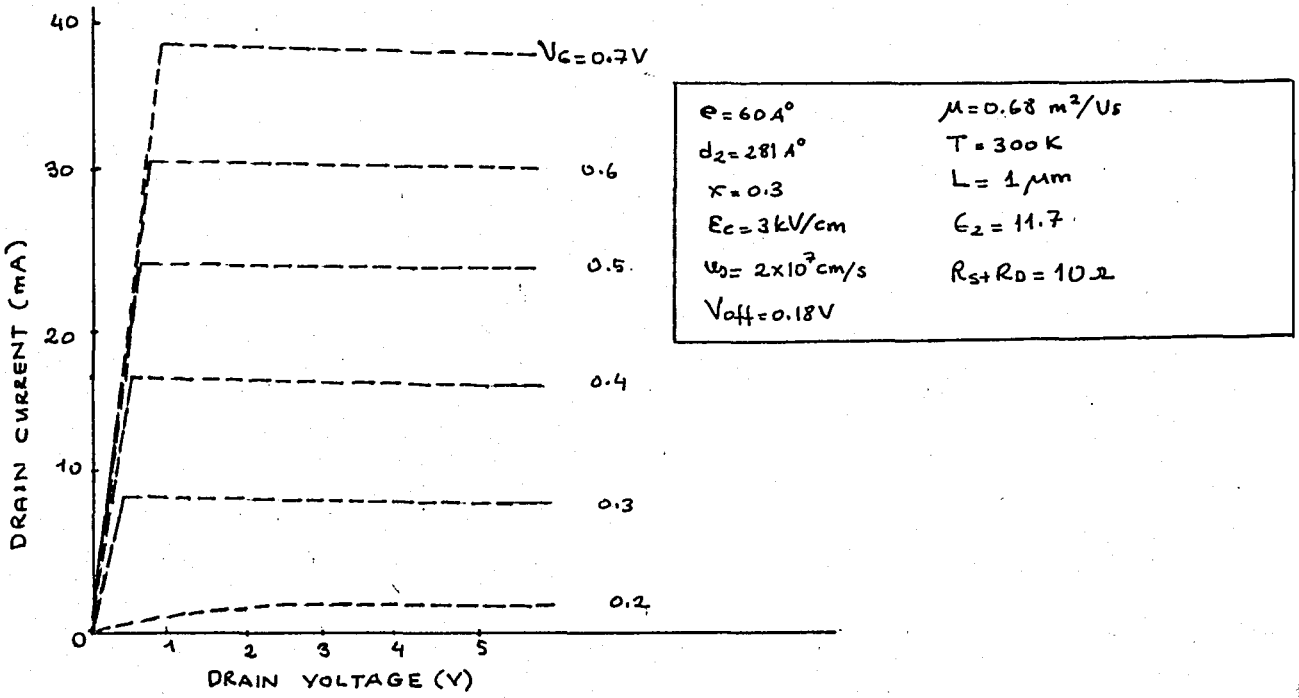
In that case, the linearity between I_S and V_G for a short-channel FET has been experimentally verified (54).

Using this model and data shown in the Figure(33),we obtain the I_D-V_D curve for a normally-off TEGFET.As can be seen the current is overestimated.This is partly due to neglecting E_F/q term which causes the overestimation of 2-DEG charge $Q_s(y)$ and eventually overestimation of the current,and partly due to the inherent insufficiency of the Turner-Wilson approximation which assumes constant mobility at the electric field values below the critical field and pins the occurance of critical field value to the plane at the drain end of the gate.

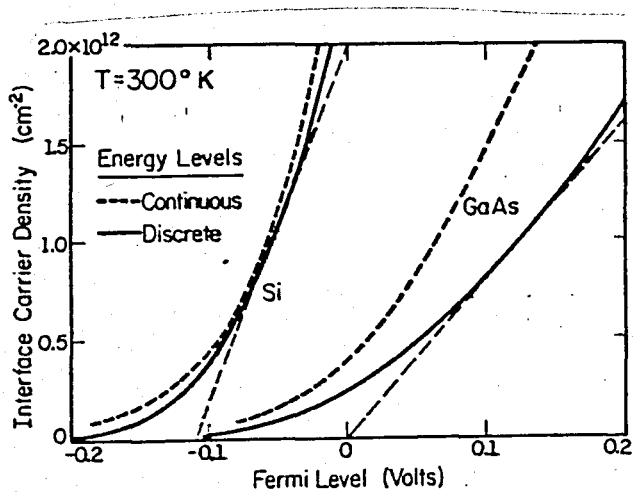
In the TEGFET model the subband splitting in the 2-DEG is taken into account,and the triangular-well approximation is used to calculate the subband energies for the first time for these types of structures.In this 2-dimensional system it is a necessity to take the quantization into account,since in GaAs,the density of states is smaller(or the effective mass is smaller)and the quantization of electron population at the heterointerface cannot be neglected as done in Si where the conduction band density of states is very large,the Fermi level even for the largest carrier concentration,2×10^{12} cm^{-2},is still below the conduction band and predictions are reasonably accurate when the problem is treated like a three-dimensional(3-D) and quantization is neglected(for instance,using Joyce-Dixon approximation).Therefore,as illustrated in Figure(34),the Joyce-Dixon approximation which was used in the HEMT model is not a good approximation in these heterostructures.

As a result,this model is not sufficient to predict the device behavior and,therefore,it should be improved.The E_F/q

term shouldn't be neglected,since it is a function of gate voltage,and it has contribution to the threshold gate voltage.



FIGURE(33) I -V characteristics of a normally-off TEGFET obtained using the TEGFET model,and the parameter values in the inset.



FIGURE(34) Variation of the electron density with Fermi level as measured from the bottom of the conduction band in GaAs.

3. The MODFET Model

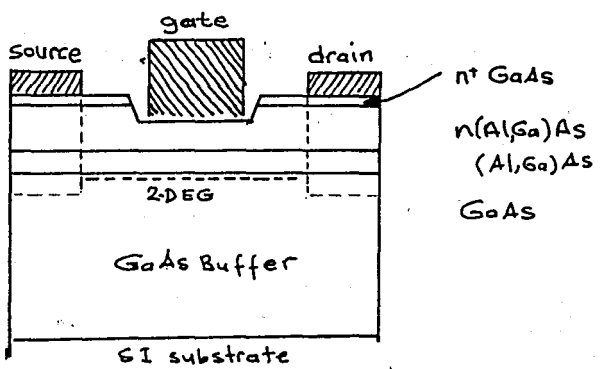
a. Device Structures and Fabrication Technologies

T.J.Drummond and H.Morkoç et al. published their first paper about high mobility structures which were fabricated using modulation-doped AlGaAs-GaAs heterostructures(56). These single-period modulation-doped heterojunctions have been prepared by MBE.The AlGaAs,grown with x=0.25 or x=0.33,was doped to a level $N_D \cong 3x10^{17}$ cm^{-3} with Si.Maximum mobilities of 74200 cm^2/Vs at 78 K and 6930 cm^2/Vs at 300K were observed in different structures and it is predicted that,these structures,if used for normally-off and/or pseudonormally-off FET channel layers in high-speed integrated circuits,can provide improved performance.In this paper,the FET device applications were also discussed by using a MESFET model given by S.M.Sze.

In 1982,the model for modulation-doped FET (MODFET) was introduced,(57).This model is nearly same with the TEGFET model;only difference is that in the MODFET model the variation of the Fermi level with the gate voltage was not neglected as it was done in both the HEMT and the TEGFET models.Shortly after,same group presented their three-piece model in which a three-piece linear approximation is used for the velocity-field characteristics (58).We will investigate these models but,prior to this,fabrication techniques of MODFETs are given.

The heterojunction structures needed for MODFETs are grown by MBE on semi-insulating substrates.First a nominally 1μm thick undoped GaAs layer is grown on the semi-insulating substrate.This followed by the growth of the AlGaAs layer,

about 20-60 Å of which is not doped near the heterointerface. The doped AlGaAs layer,about 600 Å thick,may be capped with a doped GaAs layer(200-300 Å thick)or the mole fraction may be graded down to GaAs towards the surface.Device isolation is in most cases done by chemically etching mesas down to the undoped GaAs layer or to the semi-insulating substrate, or by an isolating implant.The source and drain areas are then defined in positive photoresist and typically AuGe/Ni/Au metallization is evaporated.Following the lift-off,the source-drain metallization is alloyed at or above 400°C to obtain ohmic contacts.During this process Ge diffuses down past the heterointerface,thus making contact to the sheet of electrons. The gate is then defined and a very small amount of recessing is done.The extent of recess is dependent upon whether depletion or enhancement mode devices are desired.In depletion-mode devices,the remaining doped layer should be just the thickness to be depleted by the gate Schottky barrier.In enhancement-mode devices,the remaining doped AlGaAs is much thinner and thus the Schottky barrier depletes the electron gas as well.Finally,the aluminum gate metallization (3000 Å thick) was evaporated by an electron gun and lifted-off. Figure(35) shows the cross-section of a normally-off MODFET.



FIGURE(35) Cross-section of a normally-off MODFET.The dimensions are,3,1,and 290μm for the channel length,gate length and gate width,respectively.

b. The MODFET Model

(1). Interface Sheet Carrier Concentration

This model is greatly benefited from the TEGFET model; thus,it also considers the subband splittings in the interface potential well.It takes the undoped spacer layer into account, as well.

The charge accumulated in the potential well is similarly obtained as in the TEGFET model.

$$n_s = DkT \ln\left[\left(1+\exp\left(\frac{E_{Fi}-E_0}{kT}\right)\right)\left(1+\exp\left(\frac{E_{Fi}-E_1}{kT}\right)\right)\right] \qquad (3.83)$$

The interface sheet-carrier concentration just calculated is said to be provided by the larger bandgap semiconductor.Under equilibrium,the charge depleted from the larger bandgap material must be equal the interface carrier density.A solution is then found such that the Fermi level is constant across the heterointerface.The depletion approximation is not used because of the reason that the doping level in the AlGaAs layer is quite large (approaching the density of states).Then a charge approach,where charge is a function of distance even with a constant doping,is taken.Therefore,the modified Poisson's equation becomes

$$\frac{d^2V}{dx^2} = \frac{-\rho(x)}{\epsilon_2} \qquad (3.84)$$

here,V is the electostatic potential and x is the perpendicular distance away from the heterointerface.The space charge density $\rho(x)$ is given by

$$\rho(x)=q\left[N_d^+(x)-n(x)\right] \tag{3.85}$$

where n(x) is the free-electron concentration, and

$$N_d^+(x)=\frac{N_d}{1+g\exp\left[(E_d+qV)/kT\right]} \tag{3.86}$$

is the ionized donor concentration. Here Nd is the total donor density, g is the degeneracy factor of the donor level, and E_d is the donor activation energy; on the other hand,

$$n(x)=N_c\frac{\exp(qV/kT)}{1+\frac{1}{4}\exp(qV/kT)} \tag{3.87}$$

where N_c is the density of states in the conduction band in the AlGaAs, and the Fermi level E_F is chosen as the origin of the energy scale (E_F=0) as shown in Figure(36). Combining Eqns.(3.84) through (3.87), we obtain

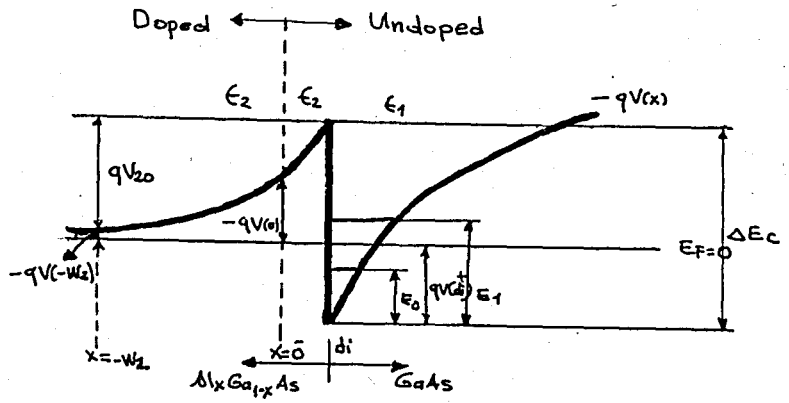
$$\frac{d^2V}{dx^2}=-\frac{q\,N_c}{\epsilon_2}\left\{\frac{N_d'}{1+g'\exp(qV/kT)}-\frac{\exp(qV/kT)}{1+\frac{1}{4}\exp(qV/kT)}\right\} \tag{3.88}$$

where

$$N_d'=N_d/N_c \qquad \text{and} \qquad g'=g\exp(qV/kT) \tag{3.89}$$

The integration of Eqn.(3.88) from $V(-w_2)$ to V(0) with respect to V using the boundary condition $\mathcal{E}_2(-w_2)=0$, where $\mathcal{E}_2$ is the electric field in the AlGaAs layer as shown in Figure(36), and w_2 is the edge of the depletion region, yields

$$\mathcal{E}_2^2(0)=\frac{2kTN_c}{\epsilon_2}\left\{N_d'\ln\frac{g'+\exp(-qV(0)/kT)}{g'+\exp(-qV(-w_1)/kT)}+4\ln\frac{4+\exp(qV(0)/kT)}{4+\exp(qV(-w_2)/kT)}\right\} \tag{3.90}$$



FIGURE(36) Conduction band edge diagram of a single period modulation-doped structure.

The constant $V(-W_2)$ can be found from the space charge neutrality that exists at $x=-W_2$,i.e.,

$$\rho(-W_2)=-\frac{qN_c}{\epsilon_2}\left\{\frac{N_d'}{1+g'\exp(qV(-W_2)/kT)}-\frac{\exp(qV(-W_2)/kT)}{1+\frac{1}{4}\exp(qV(-W_2)/kT)}\right\}=0 \qquad (3.91$$

This equation is a quadratic equation with respect to $\exp(qV(-W_2)/kT)$.The solution is obtained that

$$y=\exp(qV(-W_2)/kT)=\frac{-(1-\frac{N_d'}{4})+\sqrt{(1-\frac{N_d'}{4})^2+4g'N_d'}}{2g'} \qquad (3.92)$$

The equilibrium interface density is determined by the interface electric field as

$$n_{so}=\frac{\epsilon_2\mathcal{E}_2(0)}{q}=\frac{\epsilon_2\mathcal{E}_2(\bar{d}_i)}{q} \qquad (3.93)$$

Eqn.(3.93) follows from Gauss's law,if the doping density in

the GaAs layer is small enough so that the bulk charge in the depletion layer of the GaAs is much smaller than qn_{so}. The expression for $\mathcal{E}_2(0)$ is given by Eqn.(3.90) which may be simplified when the inequality $\exp(-qV(0)/kT) \gg 1$ is taken into account, that is,

$$\mathcal{E}_2^2(0) = \frac{2qN_d}{\epsilon_2}\left\{-V(0)+V(-w_2)-\frac{kT}{q}\left[\ln(1+g'y)+\frac{4}{N_d'}\ln(1+y/4)\right]\right\} \qquad (3.94)$$

Substituting Eqn.(3.94) into Eqn.(3.93) yields

$$n_{so} = \sqrt{\frac{2\epsilon_2 N_d}{q}\left[-V(\bar{d}_i)+V(-w_2)+\delta+N_d^2\, d_i^2\right]} - N_d\, d_i \qquad (3.95)$$

where

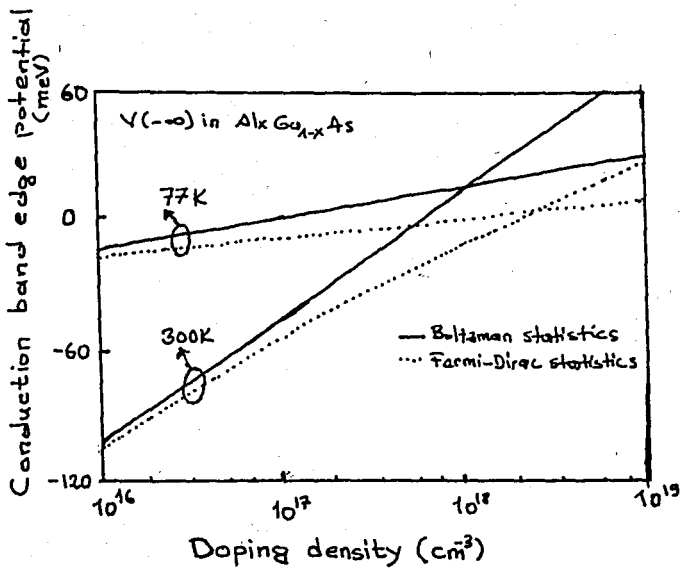
$$\delta = -\frac{kT}{q}\left\{\ln(1+g'y)+\frac{4}{N_d'}\ln(1+y/4)\right\} \qquad (3.96)$$

The relationship

$$V(\bar{d}_i) = V(0) - \mathcal{E}_2(0)\, d_i \qquad (3.97)$$

has been incorporated to derive Eqn.(3.95). The coordinate $x=\bar{d}_i$ corresponds to the AlGaAs side of the heterointerface.

Eqn.(3.95) differs from the depletion approximation case by δ in the right hand side which is substracted from the total band bending (total band bending $= -V(\bar{d}_i) - (-V(-w_2)) = -V(\bar{d}_i) + V(-w_2)$). This contribution to the band bending is shown in Figure(37) as a function of doping density, N_d, in AlGaAs for 77 and 300K,(59). As can be seen from this figure, the correction is quite important because it is comparable to ΔE_c, the conduction band discontinuity at the heterointerface.



FIGURE(37).The energy correction term arising from the degeneracy in the AlGaAs(without depletion approximation)as a function of the donor concentration in the AlGaAs layer.

In order to determine n_{so} ,the same method as that used in the TEGFET model is used.The Eqns.(3.83),(3.95) with (3.96),(3.97) and $V(\overset{+}{d_i}) = \frac{1}{q}\Delta E_c + V(\overset{-}{d_i})$ are used.However,an accurate analytical approximation is obtained by linearizing the Eqn.(3.83) with respect to $V(\overset{+}{d_i})$,which can be expressed as E_{Fi}/q and depicts the difference between the Fermi level (taken as reference)and the bottom of the conduction band in the GaAs at the heterointerface.

Repeating Eqn(3.83) with this replacement,

$$n_{so} = DkT \ln \left[\left(1+\exp\left(\frac{E_{Fi}' - E_o}{kT}\right)\right)\left(1+\exp\left(\frac{E_{Fi}' - E_1}{kT}\right)\right) \right] \qquad (3.98)$$

For large values of n_{so} ,

$$-\frac{1}{q}E_{Fi}' = \frac{1}{q}\Delta E_{Fo}(T) + an_{so} \qquad (3.99)$$

where $a = 0.125 \times 10^{-16}$ (Vm^{-2}) ,and $\Delta E_{Fo} = 0$ at 300K and 25 meV at

77K and below. Noting $qV(\bar{d}_i) = \Delta E_c - E_{Fi}$, Eqn.(3.95) leads to the following simple formula for n_{so}:

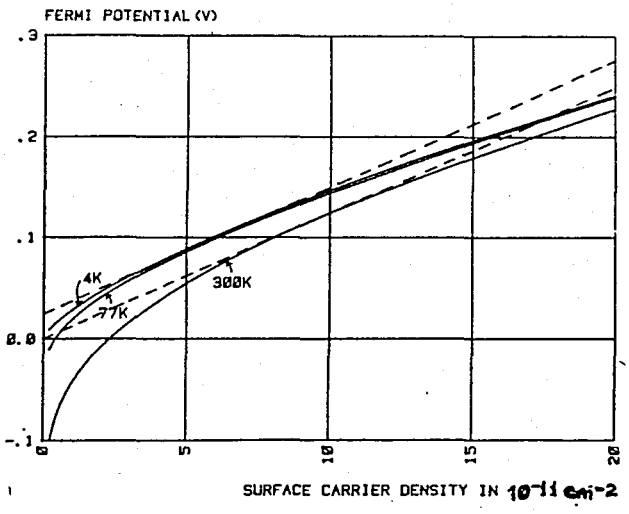
$$n_{so} = \sqrt{\frac{2\epsilon_2 N_d}{q}\left[\frac{\Delta E_c + \Delta E_{Fo}(T)}{q} + \delta + V(-w_2)\right] + N_d^2(d_i+\Delta d)^2} - N_d(d_i+\Delta d) \qquad (3.100)$$

where $\Delta d = \frac{a\epsilon_2}{q} \approx 80$ Å

The depletion approximation can be arrived by setting $\delta = 0$ in Eqn.(3.100), then

$$n_{so} = \sqrt{\frac{2\epsilon_2 N_d}{q}(V_{2o}) + N_d^2(d_i+\Delta d)^2} - N_d(d_i+\Delta d) \qquad (3.101)$$

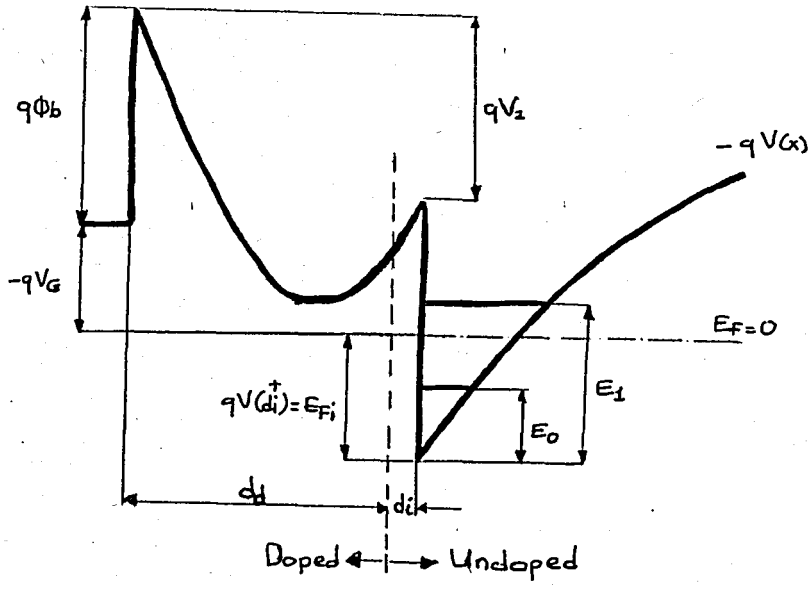
where $V_{2o} = V(-w_2) - V(\bar{d}_i)$, at 77K and 300K, the depletion approximation underestimates the voltage term by 25 mV and zero both respectively.



FIGURE(38) Interface Fermi Potential (E_{Fi}/q) versus the sheet carrier concentration.

(2). Charge Voltage Relation

The main purpose of this section is to derive the necessary expressions showing how n_{so} is modulated by applied gate bias.A band diagram of such a heterojunction with a Schottky barrier(biased negatively) is shown in Figure(39).Here as had been assumed in the two models given before this model, there are two depletion regions,one of which is caused by the heterojunction and the other by Schottky barrier which will be referred to as the gate.A completely depleted doped AlGaAs layer as shown in the figure can be achieved by a combination of a sufficiently large gate voltage and/or a sufficiently thin doped AlGaAs layer.



FIGURE(39) Conduction band edge diagram of a single period modulation-doped structure with a Schottky barrier deposited on the AlGaAs layer.

Using Eqns.(3.93) and(3.95),and assuming that the depletion approximation is accurate enough,it can be found that

$$qn_{so} = \epsilon_2 \mathcal{E}_2(0) = \sqrt{2q\epsilon_2 N_d \left[-V(\bar{d}i) + V(-W_2) \right] + q^2 N_d^2 \, di^2} - qN_d \, di \qquad (3.102)$$

which,in turn can be used to calculate the electric field strength at the heterointerface.

Since the transport through AlGaAs is not as good as it is through GaAs,the structure and operational parameters are chosen such that the AlGaAs layer is depleted entirely.The electostatic potential in such a case can be calculated by integrating the area under the electric-field curve.One must, however,remember that the electric field is constant in the undoped spacer layer.Using Figure(39),

$$V_2 = \frac{qN_d}{2\epsilon_2} d_d^2 - \mathcal{E}_2(0)\, d \qquad (3.103)$$

can be obtained,where d_d is the doped AlGaAs thickness, $d = d_d + d_i$ and

$$\epsilon_2 \mathcal{E}_2(\bar{d}) = \epsilon_2 \mathcal{E}_2(0) = qn_{so} = \frac{\epsilon_2}{d}(V_{P_2} - V_2) \qquad (3.104)$$

where

$$V_{P_2} = \frac{qN_d}{2\epsilon_2} d_d^2 \qquad (3.105)$$

is the voltage necessary to pinch off the doped AlGaAs layer. Examination of Figure(39) reveals that

$$V_2 = \phi_b - V_G + \frac{1}{q}(E_{Fi} - \Delta E_c) \qquad (3.106)$$

Combining Eqns.(3.104)and(3.106)leads to

$$n_{so} = \frac{\epsilon_2}{q\, d}\left[V_G - (\phi_b - V_{P_2} + E_{Fi}/q - \Delta E_c/q) \right] \qquad (3.107)$$

Substituting (3.99) into (3.107)

$$n_{so} = \frac{\epsilon_2}{q\, d}\left[V_G - (\phi_b - V_{P_2} - \Delta E_c/q + \Delta E_{Fo}(T)/q + a\, n_{so}) \right] \qquad (3.108)$$

or,

$$n_{so}=\frac{\epsilon_2}{q(d+\Delta d)}(V_G-V_{off}) \qquad (3.109)$$

where

$$V_{off}\equiv\phi_b-(\Delta E_c/q)-V_{p2}+(\Delta E_{Fo}/q) \qquad (3.110)$$

and

$$\Delta d=\frac{\epsilon_2 a'}{q}\approx 80\ \text{Å}$$

The charge is then given by

$$Q_s=qn_{so}=\frac{\epsilon_2}{(d+\Delta d)}\quad(V_G-V_{off}) \qquad (3.111)$$

The correction term Δd comes from E_{Fi} which is a function of gate voltage. Since the thickness of the AlGaAs layer is about 300 Å, Δd, which is approximately 80 Å, gives an important correction factor and dropping it can lead to overestimation of n_{so} for a particular V_G and thus the overestimation of current.

(3). Current-Voltage Relation

In an FET configuration, such as Figure(40), application of drain voltage in addition to gate voltage gives rise to a potential distribution varying from zero at the source end to V_D' at the drain end. This potential, then, leads to an effective charge control voltage which is different from the applied gate voltage and now is a function of distance under the gate. The potential distribution shown in the Figure(40) is obtained when the ohmic drop across the source and drain resistances are neglected. Later on these resistances will be incorporated.

At a distance y from the source, the effective voltage controlling the charge is

$$V_{eff}(y) = V_G - V_c(y) \qquad (3.112)$$

where V_G and $V_c(y)$ are the external applied gate voltage, and the channel voltage respectively. Then, using the current equation

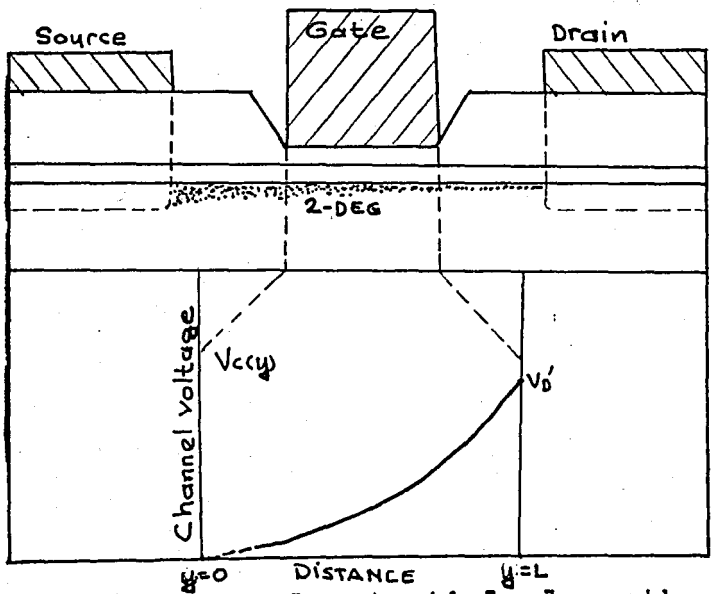
$$I = Q_s(y) Z v(y) \qquad (3.113)$$

where

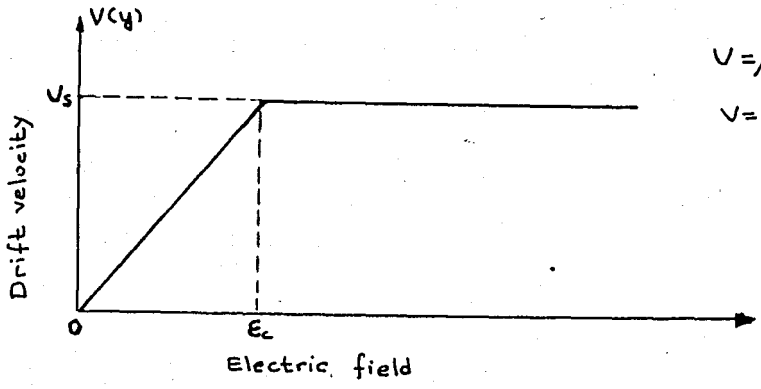
$$Q_s(y) = qn_{so} = \frac{\epsilon_2}{(d+\Delta d)} (V_G - V_c(y) - V_{off}) \qquad (3.114)$$

and Z denotes the gate width, v(y) is the electron velocity at y, y being the direction parallel to the electron motion.

Then the Turner-Wilson approximation is used to simulate the velocity-field characteristics of such a small device. The two-piece linear approximation given by Turner and Wilson is shown in Figure(41).



FIGURE(40) Channel potential along the gate of an FET.



FIGURE(41) Two-piece linear approximation of the velocity-field characteristic of GaAs FETs(Turner and Wilson approximation

At fields less than $\mathcal{E}_c$,from Eqns.(3.112)and(3.114),

$$I=\mu Z \frac{\epsilon_2}{(d+\Delta d)} (V_G-V_c(y)-V_{off}) \frac{dV_c}{dy} \qquad (3.115)$$

where $-dV_c/dy=\mathcal{E}(y)$ is the electric field.For the case where $\mathcal{E}<\mathcal{E}_c$,integration of Eqn.(3.115) with the use of

$$\begin{aligned} V_c(y=0)&=R_S I \\ V_D'=V_c(y=L)&=V_D-(R_S+R_D)I \end{aligned} \qquad (3.116)$$

where L is the gate length,R_S and R_D denote the source and drain parasitic resistances and V_D depicts the external drain voltage,leads to

$$V_c(y)=V_G'-\sqrt{(V_G'-R_S I)^2-2\frac{(d+\Delta d)Iy}{\epsilon_2\mu Z}} \qquad (3.117)$$

where

$$V_G'=V_G-V_{off} \qquad (3.118)$$

Differentiation of Eqn.(3.117) with respect to y results in the electric field

$$\mathcal{E}(y) = -\frac{dV_c(y)}{dy} = \frac{(d+\Delta d)I}{\mu Z \epsilon_2}\left[(V_G' - R_S I)^2 - 2\frac{(d+\Delta d)I\, y}{\epsilon_2 \mu Z}\right]^{-1/2} \quad (3.119)$$

As the drain voltage is increased, the electric field near the drain end at $(y=L)$ will reach the critical value first, called $\mathcal{E}_c$ or $\mathcal{E}_s$.

$$\mathcal{E}(y)\Big|_{y=L} = \mathcal{E}_c = \left(\frac{I_s}{\beta L}\right)\left[(V_G' - R_S I_s)^2 - 2\frac{I_s}{\beta}\right]^{-1/2} \quad (3.120)$$

where $\beta = \frac{\mu \epsilon_2 Z}{(d+\Delta d)L}$ and I_s is the saturation current. Letting

$$V_{s\ell} = \mathcal{E}_c L = \left(\frac{I_s}{\beta}\right)\left[(V_G' - R_S I_s)^2 - 2\frac{I_s}{\beta}\right]^{-1/2} \quad (3.121)$$

then

$$\left(\frac{I_s}{\beta}\right)^2\left[(V_G' - R_S I_s)^2 - 2\frac{I_s}{\beta}\right]^{-1} - V_{s\ell}^2 = 0 \quad (3.122)$$

or,

$$\left(\frac{I_s}{\beta}\right) - V_{s\ell}^2\left[(V_G' - R_S I_s)^2 - 2\frac{I_s}{\beta}\right] = 0 \quad (3.123)$$

Solving for I_s leads to

$$I_s = \frac{\beta V_{s\ell}^2}{1-(\beta R_S V_{s\ell})^2}\left[\sqrt{1+2\beta R_S V_G' + (V_G'/V_{s\ell})^2} - (1+\beta R_S V_G')\right] \quad (3.124)$$

If R_S were to be set to 0, then

$$I_S = \beta V_{s\ell}^2\left[\sqrt{1+(V_G'/V_{s\ell})^2} - 1\right] \quad (3.125)$$

or

$$I_s = \frac{\mu \epsilon_2 Z}{(d+\Delta d)L} V_{s\ell}\left[\sqrt{(V_G')^2 + V_{s\ell}^2} - V_{s\ell}\right] \quad (3.126)$$

using $V_{s\ell} = \mathcal{E}_c L$, $\mu \mathcal{E}_c = v_s$, one finds

$$I_s = \frac{Z \epsilon_2 v_s}{(d+\Delta d)}\left[\sqrt{(V_G')^2 + V_{s\ell}^2} - V_{s\ell}\right] \quad (3.127)$$

From Eqn. (3.117) with $R_s = 0$ and $y = L$

$$V_c(L)=V'_G - \sqrt{(V_G')^2 - 2\frac{I_S L(d+\Delta d)}{\mu \epsilon_2 Z}} \qquad (3.128)$$

On the other hand

$$I_S = \frac{Z\epsilon_2 v_s}{(d+\Delta d)}\ (V'_G - V'_{DS}) \qquad (3.129)$$

where V'_{DS} denotes the intrinsic drain to source voltage. Using Eqns.(3.127) and (3.129), it can be found

$$V'_{DS} = V'_G + V_{S\ell} - \sqrt{(V'_G)^2 + V_{S\ell}^2} \qquad (3.130)$$

Extrinsic drain to source voltage is then given by

$$V_{DS} = V'_G + V_{S\ell} - \sqrt{(V_G')^2 + V_{S\ell}^2} + I_S(R_S+R_D) \qquad (3.131)$$

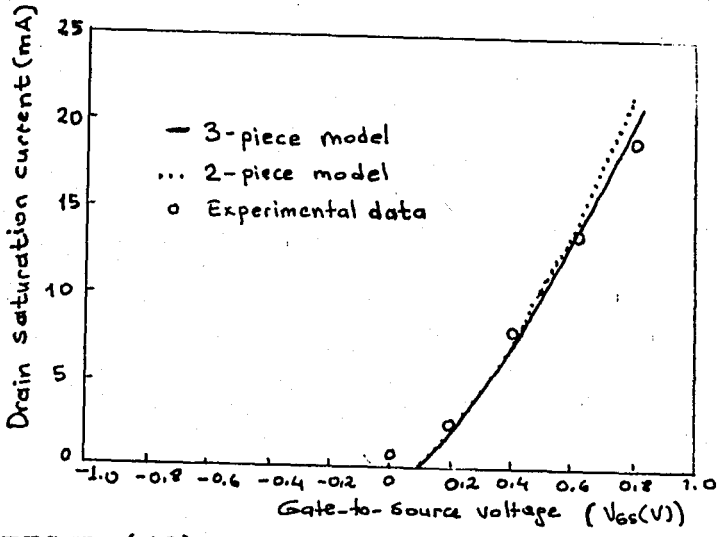
The two equations, if we repeat them together give the I-V characteristics of the device,

$$V_{DS} = V'_G + V_{S\ell} - \sqrt{(V'_G)^2 + V_{S\ell}^2} + I_S(R_S+R_D)$$

$$I_{DS} = \beta V_{S\ell}^2 \frac{\sqrt{1+2\beta R_S V'_G + V'^2_G/V^2_{S\ell}} - (1+\beta R_S V'_G)}{1-\beta^2 R_S^2 V_{S\ell}^2}$$

To test the accuracy of the model, a normally-off modulation-doped FET is fabricated and characterized. The low field mobility μ was obtained from the Van der Pauw-Hall measurements of the particular wafer from which the FET was fabricated. The gate length is 1 μm and the gate width is 145 μm. For x=0.3 $N_d = 1\times10^{18}\ cm^{-3}$, and d_i=100 Å, the doped AlGaAs remaining beneath the gate should be about 300 Å and 450 Å thick to obtain normally-off and normally-on devices respectively. The calculated and experimental drain saturation currents at room temperature

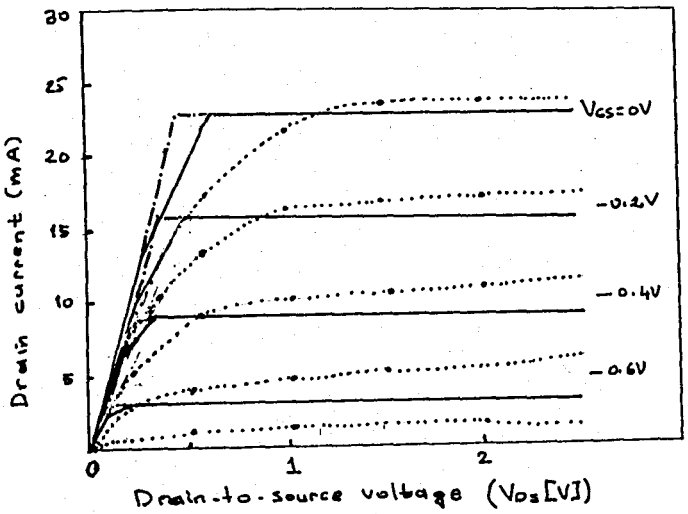
as a function of gate voltage are shown in Figure(42). $N_d = 1 \times 10^{18}$ cm^{-3}, $\mu = 0.68$ m^2/Vs and $R_S = 12\Omega$ are measured. In this particular device, a value of $v_s = 2 \times 10^5$ m/s was used for best fit for gate voltages below +0.74V.

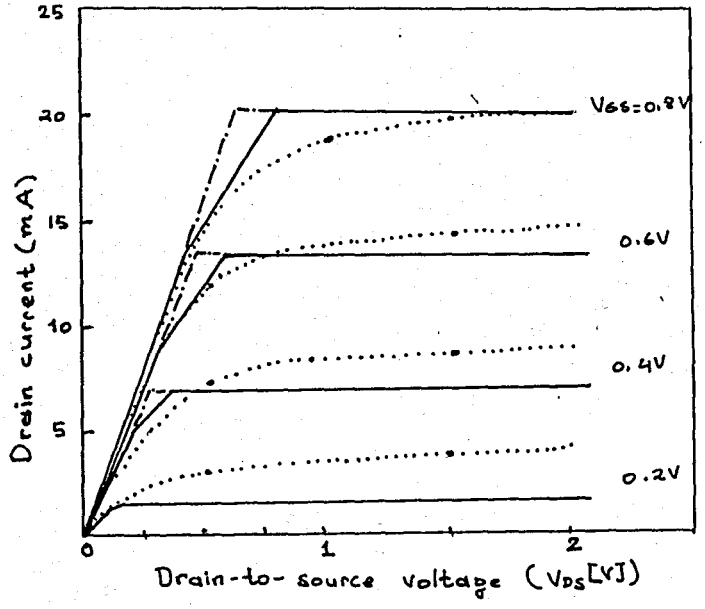


FIGURE(42) Saturation current versus gate voltage for a normally-off MODFET. Measured points are superimposed on the calculated curve.

Even though 10Ω is measured as R_S for the normally-off FET, 12Ω is used in the model to have the best fit to the experimental data. The justification given as follows: the fabrication FET has $1\mu m$ spacing between source and gate. This region is thought of as ungated FET indicating that R_S increases as the current increases. This effect should be more pronounced for normally-off FETs even though the surface potential for AlGaAs was reported to be substantially smaller than the Schottky barrier height.

The I_D-V_D characteristics obtained using the MODFET model for normally-on and normally-off FETs are shown in Figure(43).





—·—2-piece model

——3-piece model

····· experimental data

FIGURE(43) Three terminal output characteristics of the normally-on and normally-off MODFETs.

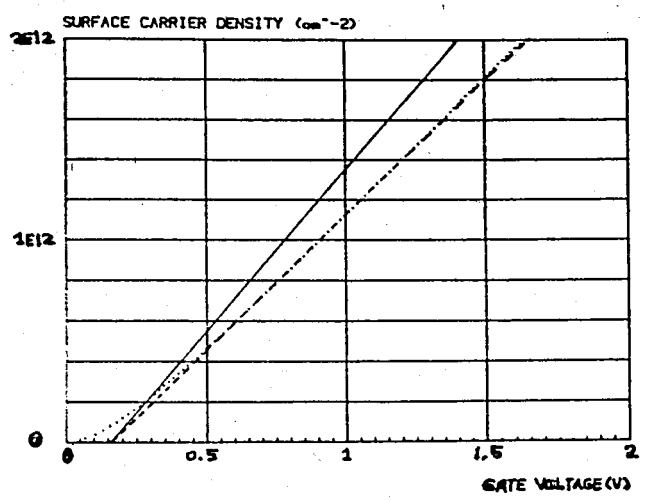
As seen in Figure(43),the drain current is still overestimated in this model,and a smooth decrease around saturation current levels cannot be seen in this model as well. These sharp corners on I_D-V_D curves suggest that the two-piece linear approximation(The Turner-Wilson approximation) is not a good approximation to make exact predictions about

device behavior.Nevertheless,the model approximately predict the saturation currents although its predictions of saturation voltages are not so good.

The only difference between the TEGFET model and the MODFET model is that in the former the total charge in the 2-DEG was found neglecting the variation of the Fermi level, E_{Fi} ,with the gate voltage.In a typically normally-off MODFET,however, E_{Fi} can be larger than 0,14 V when the device is fully on,causing the charge to be significantly over-estimated.The Fermi level,E_{Fi} ,determines the width of the potential well at the interface.As the Fermi level drops, the well becomes wider and the spatial distribution of the electrons changes.This effect leads to an increase of about 80 Å in the effective distance from the 2-DEG to the gate, to a small change in the threshold voltage,to a very pronounced decrease of the transconductance near the threshold, and to a subthreshold current.

The HEMT model,on the other hand,not only neglects the E_{Fi} ,but it neglects the quantization in the potential well and uses the less accurate Joyce-Dixon approximation as well.The calculated electron density,n_s, at 300K is about half of that predicted by this less accurate three- dimensional electron gas model.In the HEMT model,the apparent mobility for the 2-DEG,calculated from the drain conductance versus gate voltage was 55,000 cm^2/Vs at 77K.The measured mobility was 61,000 cm^2/Vs;the value of Δd (correction term due to E_{Fi}) required to explain this difference is 100 Å, which is in good agreement with the Δd value calculated in the MODFET model.

The implications of the MODFET model are shown in Figure (44).



FIGURE(44) Surface carrier density versus voltage difference between gate and the channel.

The exact solution of Equations

$$n_s = DkT \ \ln\left[\left(1+\exp\left(\frac{E_{Fi}-E_0}{kT}\right)\right)\left(1+\exp\left(\frac{E_{Fi}-E_1}{kT}\right)\right)\right]$$

and

$$n_s = \frac{\epsilon_2}{qd}\left[V_G - (\phi_b - V_{p2} + E_{Fi}/q - \Delta E_c/q)\right]$$

is shown by the dotted line.This can be compared with the solution of

$$n_s = \frac{\epsilon_2}{q(d+\Delta d)}\ (V_G - V_{off})$$

using the linearized E_{Fi} versus n_s relation ($E_{Fi} = \Delta E_{Fo}(T) + aqn_{so}$), is shown by the dashed line and the charge control of the TEGFET model where E_{Fi} set equal to zero(solid line).Since E_{Fi} is zero at 300K,the difference between the two approximations is due to the Δd increase in the effective gate-to-two-dimensional electron gas spacing.

The slightly smaller current measured at V_{GS} =0.8 V (see Figure(42)) is due to the invalidity of the model at

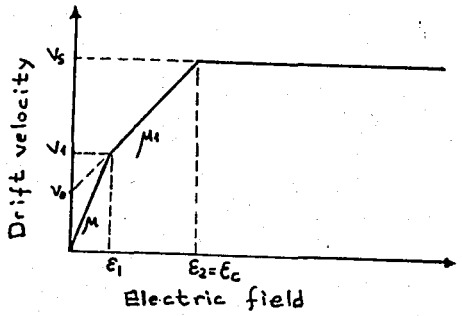
high gate voltages.The same reasoning was given for the TEGFET model,in which the decrease in current and therefore in transconductance at high gate voltage levels were found to be due to another current path formed in the AlGaAs layer,that is,a parasitic MESFET action starts.Since the transport properties of AlGaAs is inferior to that of 2-DEG whichtakes place in GaAs,the transconductance decreases. Device parameters and gate voltage level should be arranged in such a way that an additional current path in the AlGaAs layer would never occur.

Near the threshold voltage(see Figure(42)),the measured current is larger than predicted by the MODFET model,because this region is not taken into account in all the models we have seen so far.

Even though the model incorporates the Δd correction term,it still overestimates the current and underestimates the drain voltages,as shown in Figure(43).These suggest that the velocity-field approximation should be reviewed. As seen in Figure(23) and (24),the mobility of 2-DEG becomes field-dependent even though the electric field is substantially less than the field values required to saturate the drift velocity.The electron mobility becomes more field-dependent at low temperatures.Therefore,a linear three-piece approximation of the drift velocity-electric field curve is used to take the field-dependence of mobility into account,since the electron mobility decreases very abruptly even at 200V/cm.

(4). Field-Dependent Mobility

Three-piece linear approximation for the velocity-field characteristics is used to obtain the drain saturation currents, especially at low temperatures where the mobility is extremely field-dependent.



FIGURE(45) Three-piece linear approximation for the velocity-field characteristics of the MODFETs.

When the drain-to-source voltage is small the Shockley model applies, leading to

$$I_{DS} = \beta \left(V_G' V_{DS} - \frac{1}{2} V_{DS}^2 \right) \qquad (3.132)$$

where $\beta = \dfrac{\epsilon \mu Z}{(d+\Delta d)L}$, $V_G' = V_G - V_{off}$, V_{DS} is the drain-to-source voltage.

For,

$$V_{DS} < V_G' + V_0 - \sqrt{V_G'^2 + V_0^2} \equiv V_{1S} \qquad (3.133)$$

Here $V_0 = \mathcal{E}_1 L$. At higher V_{DS}

$$V_{1S} < V_{DS} < V_{DS}^S \qquad (3.134)$$

where V_{DS}^S is the drain voltage at the saturation. There are two regions with different differential mobilities under the gate.

The first region

$$0 < y < L_1 \tag{3.135}$$

where L_1 is defined as the point where $\mathcal{E} = \mathcal{E}_1$. In this region the mobility is equal to the low field mobility μ. In the second region

$$L_1 < y < L \tag{3.136}$$

the differential mobility is equal to μ_1. In region-I the current is given by

$$I_{DS} = C_o (V_G' - V_1) v_1 \tag{3.137}$$

where $v_1 = v(\mathcal{E}_1)$ (see Figure (45)).

$C_o = \dfrac{\epsilon Z}{(d + \Delta d)}$ and $V_1 = V_G' + \mathcal{E}_1 L_1 - \sqrt{V_G'^2 + (\mathcal{E}_1 L_1)^2}$

In region-II

$$I_{DS} = C_o (V_G' - V)\left(\mu_1 \frac{dV}{dy} + v_o\right) \tag{3.138}$$

Integrating (3.138) with respect to y,

$$L - L_1 = \frac{\mu_1}{v_o}\left[(V_1 - V_{DS}) + \frac{I_{ds}}{C_o v_o} \ln\left(\frac{1 - \frac{C_o v_o}{I_{ds}}(V_G' - V_{DS})}{1 - \frac{C_o v_o}{I_{ds}}(V_G' - V_1)}\right)\right] \tag{3.139}$$

Eqns.(3.138) and(3.139) were solved numerically to yield L_1 and I_{DS} ,the drain current.

At the saturation voltage $V_{DS}=V_{DS}^{s}$ the analytical solution may be found using the following equation

$$I_{DS}^{s} = C_o (V_G' - V_{DS}^{s})\, v_s \qquad (3.140)$$

The result of the solution for (3.137),(3.139),(3.140),after the source resistance R_S and drain resistance R_D are included, is given by

$$I_{DS}^{s} = \frac{\beta V_o^2}{b} \frac{\sqrt{1+2\beta R_S V_G' + b(V_G'/V_o)^2} - (1+\beta R_S V_G')}{1-(\beta R_S V_o)^2/b} \qquad (3.141)$$

and

$$V_{DS}^{s} = V_G' + \frac{V_1}{V_s} \frac{1-\sqrt{1+b(V_G''/V_o)^2}}{b} V_o + I_{DS}^{s}(R_s+R_D)$$

where

$$b = 1 - 2\frac{V_1}{V_s}\left(\frac{V_1 - V_o}{V_o}\right)\left(1 - \frac{V_s}{V_1} + \frac{V_s}{V_o} \ln \frac{1 - V_o/V_s}{1 - V_o/V_1}\right) \qquad (3.142)$$

The resulting Equations(3,141) look quite similar to the simpler equations of the linear two-piece MODFET model.

As can be seen from Figure(43) the agreement between the three-piece model and the experimental data is the best so far.Nevertheless,a smooth saturation cannot be observed.Its predictions are not so good to make it worth using;because

the calculations of current and voltage based on this model need much time,if numerical procedure is chosen.But,if analytical solutions are preferred,the results obtained using this model wouldn't be much different from the results arrived using the two-piece linear MODFET model ,as can be seen in Figure(43).

Since mobility below a critical field ($\mathcal{E}_1$) is assumed constant and after a critical field value($\mathcal{E}_c$) a sharp velocity saturation is taken,this model also shows the insufficiencies of the other models we have investigated so far,such as predicting higher saturation currents at lower drain saturation voltages.

V. NEW MODEL-MOBILITY DEPENDENT MODEL FOR THE MODFET

All the models we have seen have used the Turner-Wilson approximation to simulate the velocity-field characteristics for current-voltage calculations. In the Turner-Wilson approximation drift velocity is assumed to saturate when the drain field reaches $\mathcal{E}_c$ (a critical field), and the saturation current is calculated by imposing the boundary condition that the field at the drain end is equal to $\mathcal{E}_c$. This solution yields an abrupt saturation and, because of the rounding of v_{dr} characteristics in the vicinity of $\mathcal{E}_c$ it cannot be expected to give accurate results just prior to the saturation point. These models predict a larger drain current and a smaller saturation voltage. These results are expected, since the effective mobility introduced in these models, in fact, decreases as the electric field increases, while they assume constant mobility up to $\mathcal{E}_c$.

Turner and Wilson were the first attempting to analyze velocity saturation effects in GaAs. To account for a velocity saturated electron flow, they postulated a finite channel openning at the drain end of the gate at the onset of the drain current saturation. Saturation current levels corresponding to different gate bias voltages could be accomodated by a widening or narrowing of the channel openning at the drain end. Lehovec and Zuleeg(60) modified this model by replacing the constant mobility with the approximate field-dependent expression proposed earlier by Trofimenkoff(61).

These two analyses of GaAs FET both use Shockley's gradual channel approximation, but differ in the approximation used for electron drift velocity, v_{dr}. In the Lehovec and Zuleeg analysis v_{dr} is approximated by

$$v_{dr} = \frac{\mu_o \mathcal{E}}{1+\mu_o \mathcal{E}/v_s} \qquad (4.1)$$

where μ_o is the low field mobility, $\mathcal{E}$ is the electric field, v_s is the saturation velocity.

For short channel silicon FETs the Lehovec and Zuleeg analysis was used successfully and good fits of theoretical values to experimental data were obtained. For GaAs FETs, since the analytical formula(4.1) doesn't seem to be in agreement with the velocity field characteristics(see Figure(46)), Turner-Wilson analysis has been used. In this chapter we will try to show that the Lehovec and Zuleeg analysis can be applied to short channel GaAs MESFETs, particularly to the MODFET.

A. Field-Dependent Mobility

The Lehovec and Zuleeg analysis has not been used for GaAs FETs due to the reason that although it can give good results for silicon FETs, it shouldn't be used for GaAs FETs since GaAs velocity-field characteristics are completely different from the silicon, as shown in Figure(46). This figure shows that velocity-field characteristics of GaAs and Si are completely different at first sight. But, these curves are obtained at uniform electric field conditions and on the semiconductor wafers, not on the practical FET device structure

For instance,these curves predict a negative resistance region for GaAs after some field values,but this is not the case for a GaAs FET.Therefore,these curves shouldn't be taken strictly to simulate the real phenomena happen in the channel of the GaAs FETs.

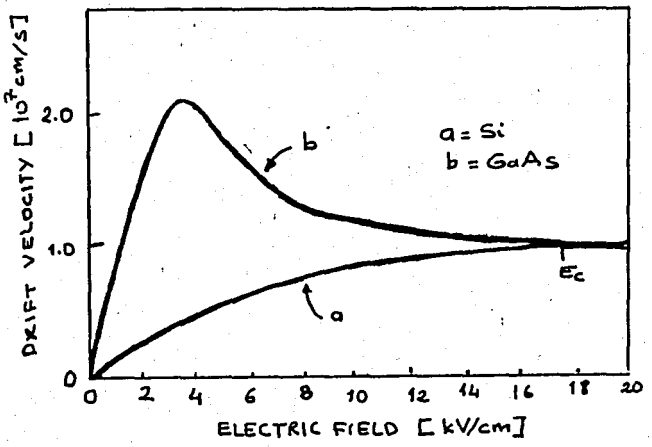
B. Velocity-Field Characteristics of the MODFETs

We have seen so far,in modulation-doped heterostructures a mobility enhancement is observed.This phenomenon results from a separation of mobile carriers from their parent donor impurities.Mobility increases considerably over conduction in bulk material of equivalent carrier concentration mostly due to the reduction of the ionized impurity scattering.Consequently the modulation doping advantage is predominantly present at low temperatures where in regularly doped semiconductors carrier scattering by ionized impurity prevails.At higher temperature where phonon scattering dominates,the modulation-doping advantage is reduced,though still present even at room temperature.

Mobilities of over $1x10^{6}$ cm^{2}/Vs at 4K have been achieved(62), indicating the effective screening of the ionized impurities and that the electron mobilities are limited almost only by piezoelectric scattering.

These mobilities are observed at zero field.When an electric field is applied,the extremely high cryogenic mobilities decrease rapidly.The decrease is due to the emission of polar optical phonons.At room temperature,the mobility is independent of electric field up to at least 2 kV/cm.In short channel FETs

the electric field can reach tens of kV/cm,it is,therefore, not possible to predict FET performance at moderately high fields by extrapolations based on the zero field mobility, particularly at cryogenic temperatures.Thus,the extremely high mobilities obtained at very low electric fields have only a secondary effect on device performance.The higher mobilities at low fields can help give the device a low saturation voltage and a small on-resistance.



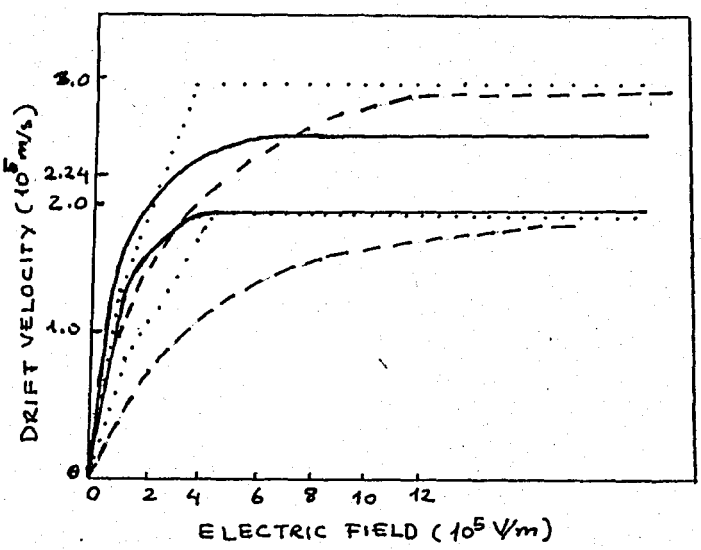
FIGURE(46) Drift velocity versus electric field for Si and GaAs.

Since the properties of the pure GaAs are maintained, electron peak velocities over $2x10^7$ cm/s and $3x10^7$ cm/s at 300K and 77K,respectively,can be obtained.We will use these velocity values in our calculations.

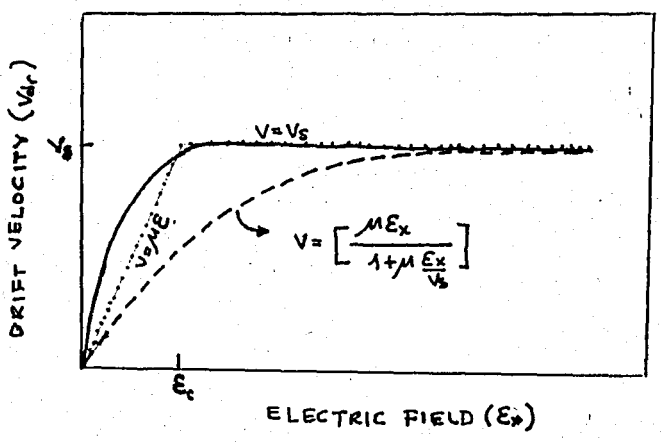
The velocity vs field characteristics in Figure(47) are obtained by using the data given in(33) up to 300V/cm,beyond that a constant increase of drift velocity is assumed.At 300K a velocity of $1.7x10^5$ m/s at 2 kV/cm was measured,at 77K the largest measured velocity was $2.24x10^5$ m/s.In these measurements between 0 and 200V/cm,the velocity-field characteristics were

obtained under dc conditions,since the lattice heating effects are negligible.Pulse technique,however,was used between 200 V/cm and 2kV/cm to avoid heating and any change in carrier concentration.

Differences between real data,piecewise linear models, and mobility-dependent model are shown in Figure(47).



FIGURE(47) Experimental and approximated drift velocity vs electric field curves for the MODFET.In all models low field mobility of 0.68 m^2/Vs,2 m^2/Vs for 300 and 77K respectively,and saturation velocities of $2x10^5$ m/s ,$3x10^5$ m/s for 300 and 77K, respectively,are used.



FIGURE(48) Approximations for the velocity-field curves (used for Si-FETs).

The analytical model of Lehovec and Zuleeg for drift velocity can agree to this level.The agreement seems to be not so good,but this may be misleading.If one reminds the case for silicon FETs (see Figure(48)),which had given very good results this disagreement in the MODFET velocity-field characteristics is found to be not worse than that obtained for silicon.Therefore,the mobility-dependent model(the Lehovec and Zuleeg analysis)can be used in MODFET also.Moreover,the experimental curves in Figure(47) are obtained by extrapolating linearly beyond 300 V/cm,because no experimental data are found in the literature beyond this field value for these type of structures. We feel that the rate of increase of electron velocity with electric field decreases with increasing electric field.The agreement between the measured data and our model based on the mobility dependent analysis of Lehovec and Zuleeg leads us to conclude that the velocity-field characteristics beyond very low field values are closer to the curves obtained using the empirical formula(4.1).

In all these analytical models,the current beyond saturation point is assumed to be constant.Therefore,they are valid only up to the knee of the current-voltage characteristics.They all predict an infinite drain resistance beyond the knee.

Our assumption of a saturation field above which carriers travel at a constant velocity disregards the negative mobility in the actual velocity-field characteristics and the possibility of electron accumulation near the drain.

Although the negative mobility is responsible for domain formations and rf oscillations in Gunn diodes,only limited

evidence of such instabilities in GaAs FETs has been demonstrated (63) and only for doping levels an order of magnitude lower than that used for practical conventional GaAs FETs. Indeed the computer solutions of Himsworth(64) point to the possibility of negative resistance effects for lightly-doped epi-layers.The apparent minor role played by the negative resistance region in practical short-gate FETs suggest that rf instabilities due to this region,if they exist,occur at frequencies far above the normal frequency regime of microwave FETs,or alternatively the domain formation is inhibited by the two-dimensional character of the field configurations within the FET.These results are for FETs having highly doped epi-layers.But since the transport in MODFET occurs in undoped GaAs layers,why cannot the velocity overshoot be observed in these devices?It should be possible,in such submicrometer devices,to apply sufficiently low voltages to effectively confine the electrons to the high-mobility central valley while in the same device creating a large electric field.After a threshold electric field,under such conditions,it should be possible to produce average velocities exceeding the maximum steady state drift velocity.But we have no experimental data to indicate this in the MODFET.Lets see the reasons of not obtaining the negative resistance in the MODFET.

We have seen that the velocity-field characteristic of GaAs shows a dropback region.Velocity increases linearly with electric field,reaches a peak value then decreases again and saturates at a critical field(ε_H).

In any FET device the electric field in the device shows two-dimensional character.That is, the carriers are under the effect of both the longitudinal field,i.e.,from source

to drain,and transverse electric field,i.e.,from gate to substrate,And the latter is always much higher than the former.

If one reminds the current transport equation in the semiconductor,

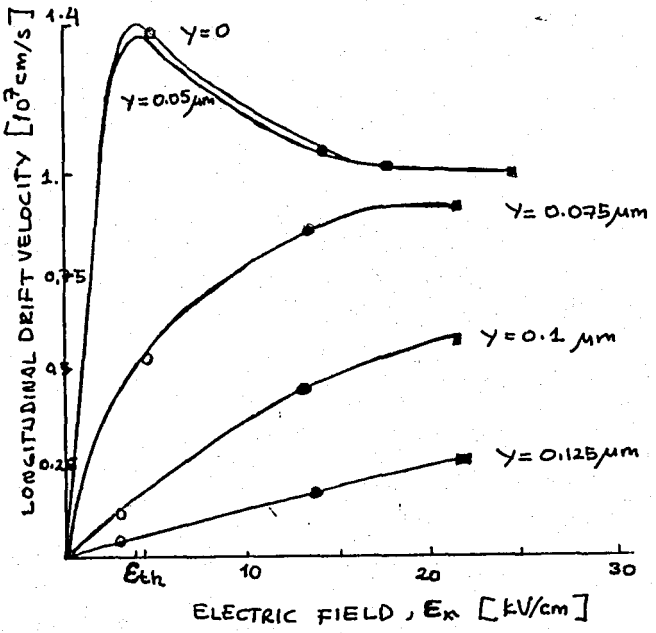
$$J_x = q\ v_x\ n + q\ D \frac{\partial n}{\partial x}$$
$$J_y = q\ v_y n + q\ D \frac{\partial n}{\partial y} \qquad (4.2)$$

where,J is the current density,q the eletronic charge,x represents the longitudinal direction,y the transverse direction, v is the drift velocity, D is the diffusion constant, and n the number of free electrons.These equations show that the resultant I/V characteristics do not depend on the longitudinal drift velocity alone,but depends also upon the mobile carrier density associated with the drift velocity.The longitudinal electron velocity,on the other hand,depends both the longitudinal and transverse electric field also.

Figure(49) shows the variation of longitudinal velocity v(x) with longitudinal field $\mathcal{E}(x)$ for an unsubstrated GaAs MESFET device,as a function of y(transverse direction) at 0.75μm from source end of gate for different values of V_{DS} and $V_{GS}=0$,where y=0 corresponds to the bottom of the device.

As can be seen from the Figure(49),since the transverse electric field exceeds the threshold electric field $\mathcal{E}_{th}$,under the gate electrode (y=0.125μm) velocity overshoot effect doesn't occur,whereas at the bottom of the device(y=0)most of the carriers are free to move since the gate depletion region doesn't reach here,therefore,the transverse electric

field is low enough here that the carriers can be accelerated to overshoot values by an increase in longitudinal electric field.As a result,a dropback in the I/V characteristics may occur.



FIGURE(49) Variation of longitudinal velocity v_x with longitudinal field $\mathcal{E}(x)$ for a GaAs MESFET without a substrate layer. o = V_{DS} =1V, • = V_{DS} =3V, ▪ = V_{DS} =5V.(63)

After this point lets see what would occur if there were a substrate layer below the epitaxial layer of the device. Since the epi-layer is highly doped in comparison with the semi-insulating substrate,the epilayer/substrate boundary is,therefore,a high/low junction in which the electrons diffuse from the highly doped epilayer into the low doped substrate.In this structure there are two factors which determine the resultant electric field at any point,the field opposing the diffusion across the high/low junction and the field set up by the gate electrode.Therefore,majority of the mobile carriers,whether in the active layer itself or in the substrate, are in the situation that the transverse field is large enough

to suppress the velocity dropback in the $v/\mathcal{E}$ characteristic.

This leads directly to two clear differences in the properties of devices with and without substrate .The first is that the carrier accumulation which had taken place in the unsubstrated device does not occur for the substrated device.The second is that the overall I/V characteristic shows no current dropback.

The current through a given epitaxial layer is reduced by the presence of the substrate because of the carrier injection from the active layer into substrate.This decrease in the channel current is compensated by the current which flows in the parallel path through the substrate.

As a result,the negative resistance property can be suppressed by either sufficient reduction of the epilayer thickness(therefore,extending the gate depletion region effect through most of the active channel) or by addition of a relatively high-resistance substrate.The situation can be simply explained by the fact that,if an electron moves in combined longitudinal and transverse fields,there is no velocity drop in the longitudinal-velocity/longitudinal-electric field relation,provided that the transverse electric field is big enough.

Therefore,in simulating GaAs MESFET,theoretically calculated I/V characteristic using a velocity-field formula which takes into account the velocity dropback behavior as in (65)is likely to give inconsistent results,because in real GaAs MESFETs this velocity dropback may never occur.

Our empirical formula,fortunately with the help of ever-present substrate layer,approximates the state of affairs

happening in the real device and according to the predictions based on the model using this velocity-field formula,one can say that this approximation simulates the phenomenon in the MODFETs accurately.

C. Mobility-dependent Model for the MODFET

Since the MODFET is a short channel device the mobility of carriers (here electrons are used,since electrons are more mobile than holes)in the channel becomes field dependent.

The charge control mechanisms through the gate voltage is taken as in the MODFET model,where the quantization effect in the heterointerface triangular potential well,and the gate voltage dependence of Fermi energy in the potential well are taken into account.We will try to model the FET application of these heterostructures.

In obtaining the drain current,we use the empirical formula introduced by Lehovec and Zuleeg.In that analysis the field-dependent velocity was given by,repeating again,

$$v(x)=\frac{\mu\mathcal{E}(x)}{1+\frac{\mu\mathcal{E}(x)}{v_s}}$$

As seen in the formula,this model predicts electron velocity saturation at infinite electric field values.

The drain current of the FET is given

$$I_D = Q_n(x)\ Z\ v(x) \qquad (4.3)$$

where $Q_n(x)$ is the interface charge which is determined as in the MODFET model, Z the gate width, v(x) the drift velocity. $Q_n(x)$ has been calculated in the MODFET model as

$$Q_n(x) = \frac{\epsilon}{(d+\Delta d)} (V_G' - V_x) \qquad (4.4)$$

where ϵ is the dielectric constant of the AlGaAs layer, d the total distance between the 2-DEG and the gate, V_G' is the effective gate voltage, i.e., $V_G' = V_G - V_{off}$, V_{off} being the threshold voltage, V_x is the channel voltage, Δd is the correction factor.

If we use (4.1), (4.4) in(4.3),

$$I_D = \frac{Z \epsilon}{(d+\Delta d)} (V_G' - V_x) \frac{\mu \, dV/dx}{1 + \frac{dV/dx}{v_s} \mu} \qquad (4.5)$$

let $u = V_G' - V_x$ and $\frac{dV(x)}{dx} = -\frac{du}{dx}$

$$I_D = \frac{-Z \epsilon \mu}{(d+\Delta d)} u \frac{du/dx}{1 - \mu \frac{du/dx}{v_s}} \qquad (4.6)$$

$$I_D \, dx = -\frac{Z \epsilon \mu}{(d+\Delta d)} u \, du + I_D \frac{\mu \, du}{v_s} \qquad (4.7)$$

If we integrate (4.6) from x=0 to x=L and from $u=u_1$ to $u=u_2$, where $u_1 = V_G - V_{off} - V_S$, and $u_2 = V_G - V_{off} - V_D$, V_S and V_D being, respectively the intrinsic source and drain voltage.

$$I_D \int_0^L dx = -\frac{Z \epsilon \mu}{(d+\Delta d)} \int_{u_1}^{u_2} u \, du + I_D \frac{\mu}{v_s} \int_{u_1}^{u_2} du \qquad (4.8)$$

then

$$I_D = \frac{\frac{Z\epsilon\mu}{2L(d+\Delta d)}(u_1^2-u_2^2)}{1-\frac{\mu}{v_s L}(u_1-u_2)} \qquad (4.9)$$

If we put u_1 and u_2 here

$$I_D = \frac{Z\epsilon\mu}{2L(d+\Delta d)} \frac{\left[(V_G')^2-(V_G'-V_D)^2\right]}{1+\frac{\mu}{v_s L}V_D} \qquad (4.10)$$

Here we use $V_S=0$ (the source is at the reference potential).

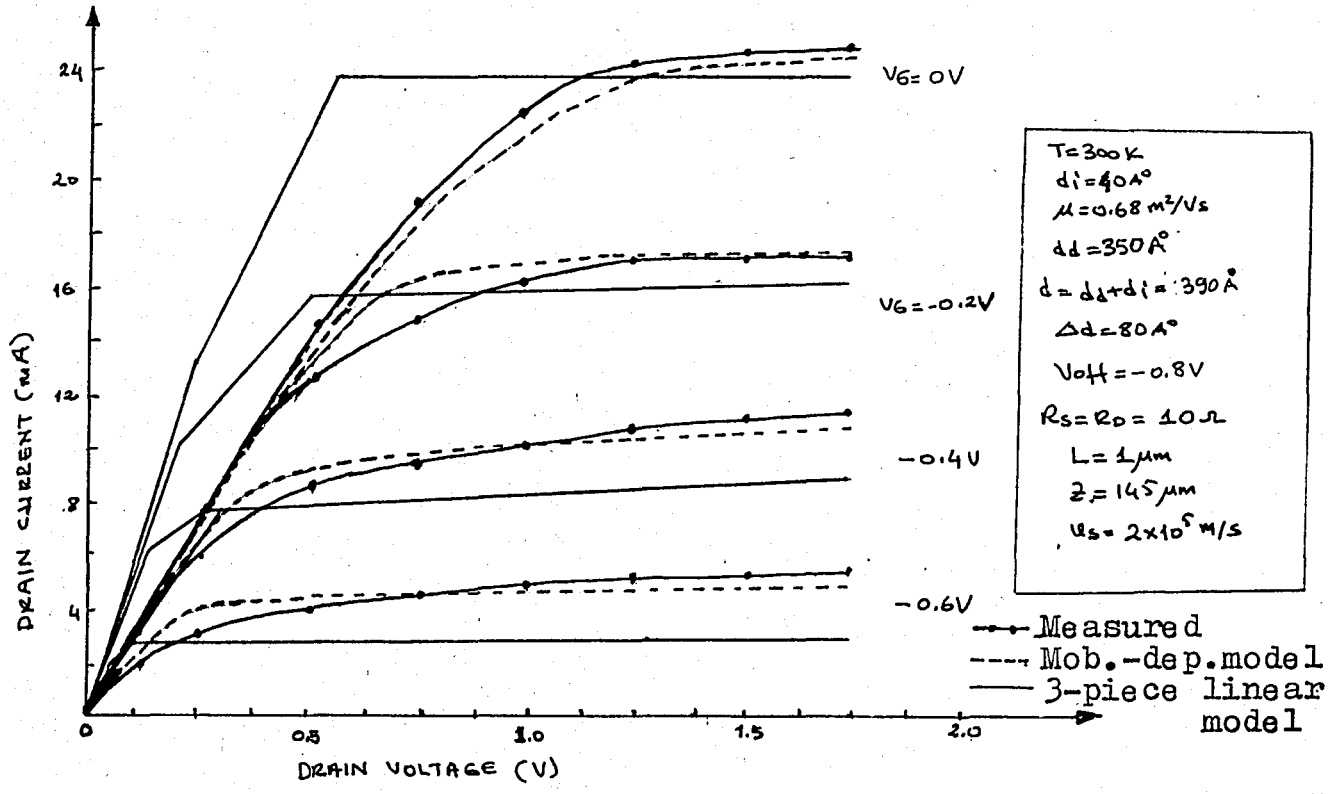
The results obtained with this formula,(4.10),with changing V_G' and V_D are shown in the Figure(51) for normally-on and in the Figure(52) for the normally-off MODFETs.Also in these figures,comparisons between the new model and the best three-piece linear model are made.In Figure(53),the results using Eqn.(4.10) are shown for an E-HEMT with comparisons between the present model and the HEMT model.

Since the MODFET is a short channel device,its epitaxial layer is very thin also.This,inherently introduces a resistance.

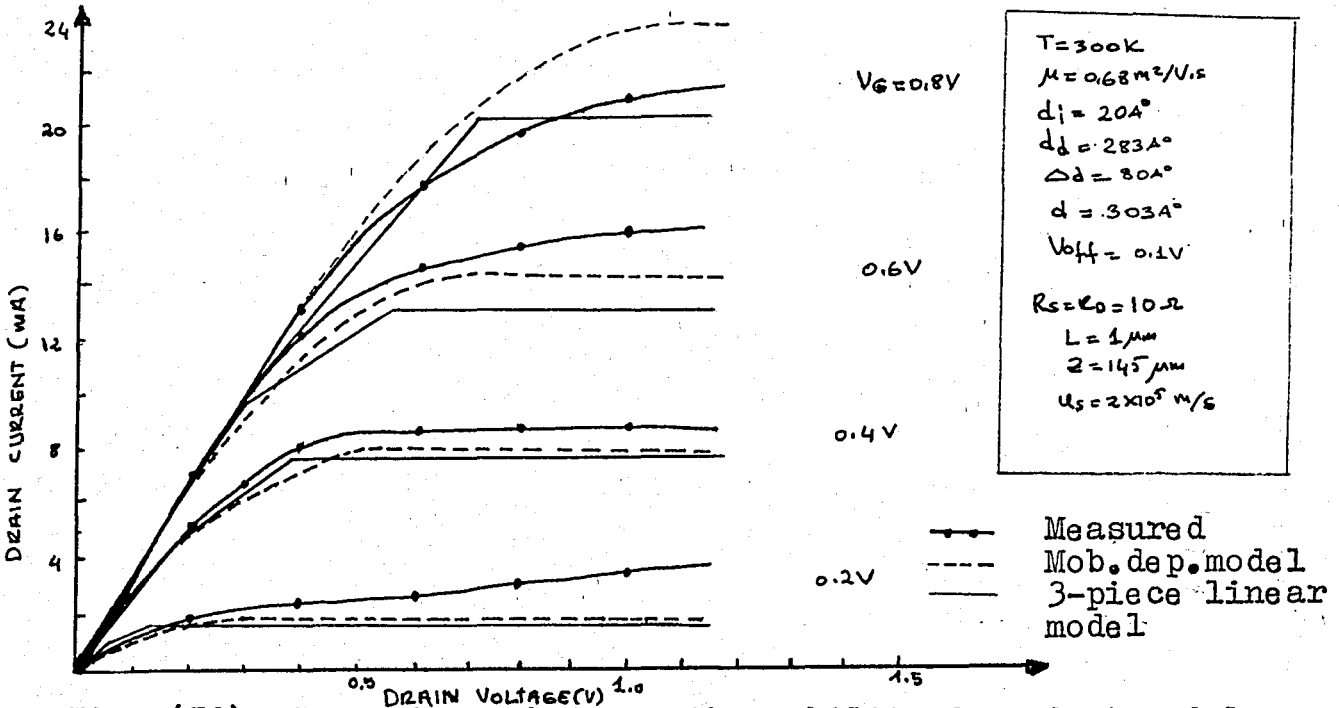
Therefore,to calculate the terminal voltages,we have to use the source and drain resistances (R_S and R_D).Thus,

$$V_{DS_{ext}} = V_{DS_{int}} + I_{DS}(R_S+R_D) \qquad (4.11)$$

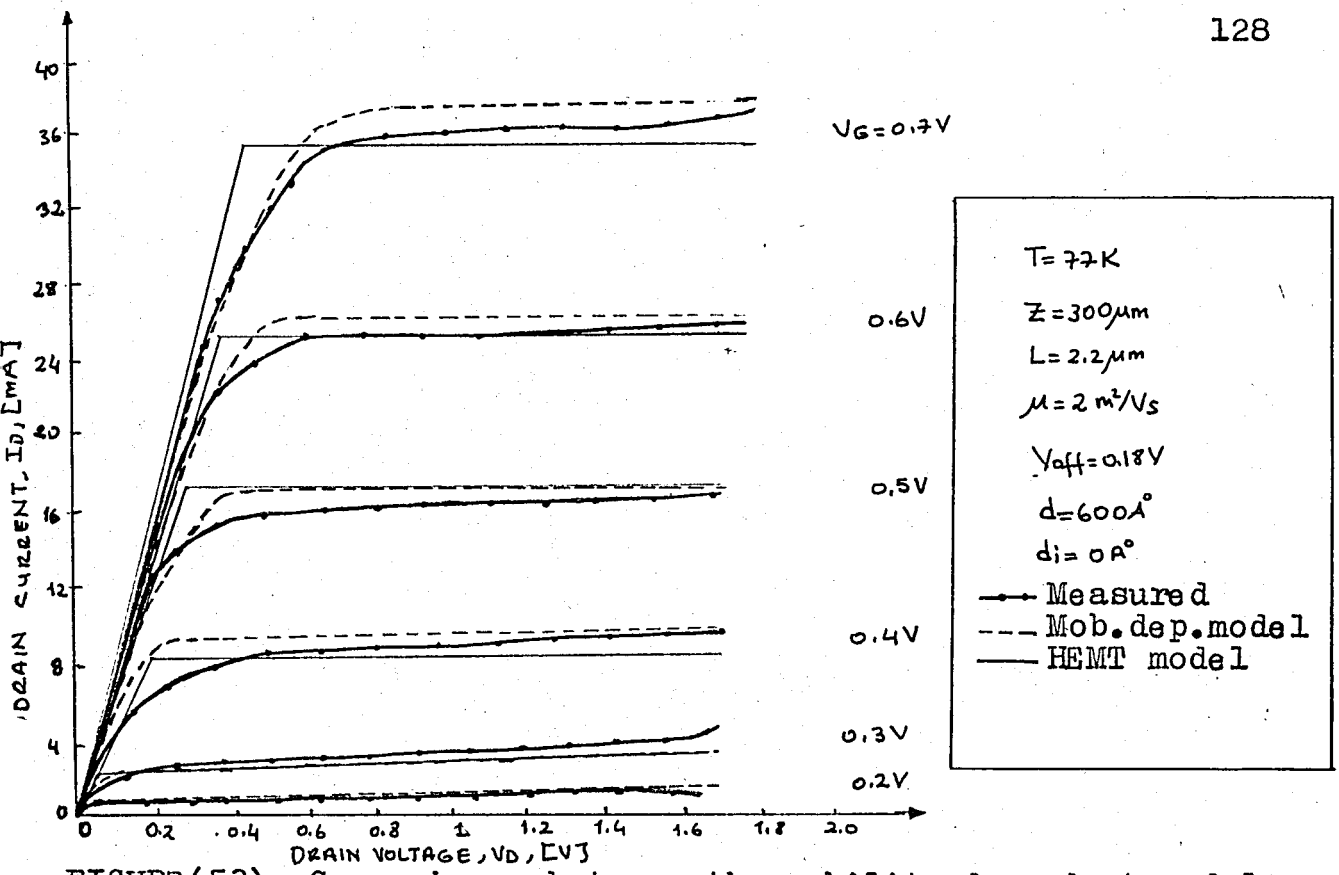
Although 7Ω is obtained from the experimental MODFET I/V characteristics,R_S and R_D are taken as 10Ω,to obtain best fit to the experimental data,as done in the MODFET and the HEMT models.



FIGURE(51) I_D-V_D characteristics of a normally-on MODFET with the parameters given in the inset. Comparisons of the mobility-dependent model, three-piece linear model and the experimental data.



FIGURE(52) Comparisons between the mobility-dependent model and three-piece linear model and experimental data for a normally-off MODFET whose parameters are given in the inset.



FIGURE(53) Comparisons between the mobility-dependent model, and the HEMT model,and the experimental data of an E-HEMT whose parameters are given in the inset.

D. Saturation Voltage and Current

We have obtained the drain current as

$$I_D = -\frac{\mu Z \epsilon}{2(d+\Delta d)L}\left\{\frac{[(V_G'-V_D)^2 - V_G'^2]}{1+zV_D}\right\}$$

where $z=\frac{\mu}{V_S L}$ is the saturation factor.The condition

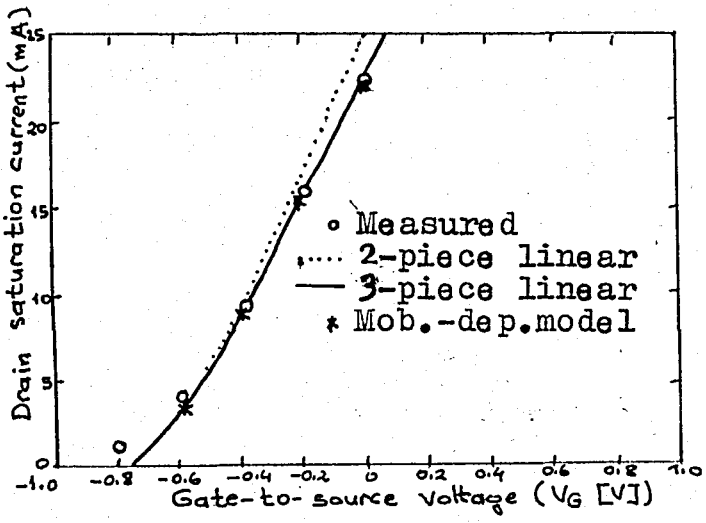
$$\frac{\partial I_D}{\partial V_D}_{V_G'=\text{constant}} = 0$$

gives the drain saturation voltage, V_{DS}, which is obtained as

$$V_{DS} = \frac{v_s L}{\mu} \left[(1+2\ z\ V_G')^{1/2} - 1 \right] \qquad (4.12)$$

Using Eqn.(4.12) in(4.10) in place of V_D ,we obtain the drain saturation current that

$$I_{DS} = -\frac{Z\ v_s \epsilon}{(d+\Delta d)} \left\{ \frac{\frac{v_s L}{\mu} \left[1-(1+2\frac{\mu}{v_s L} V_G')^{1/2} \right] + V_G' \left[2-(1+2\frac{\mu}{v_s L}\ V_G')^{1/2} \right]}{(\ 1+2\ \frac{\mu}{v_s L}\ V_G')^{1/2}} \right\} \qquad (4.13)$$



FIGURE(54) Drain saturation current versus gate voltage for a normally-on MODFET.

As can be seen from the figure,the agreement with experimental data is very good except that near the subthreshold region,which is not included in the model.

E. Transconductance

The transconductance of an FET is defined as

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_G'} \right|_{V_D = \text{constant}} \qquad (4.14)$$

using Eqn.(4.13),the transconductance for the MODFET is obtained that

$$g_m = \frac{Z \epsilon v_s}{(d+\Delta d)} \left(1 - \frac{1}{\sqrt{1+2\frac{\mu}{v_s L} V_G'}} \right) \qquad (4.15)$$

As can be seen from Eqn.(4.15) that,transconductance is directly proportional to the saturation velocity,the gate width,dielectric constant of the AlGaAs layer,and inversely proportional to the distance of the 2-DEG from the gate.

Maximum transconductance,g_{max},is obtained at $V_{G\,max}'$,which is the pinch-off voltage of the 2-DEG.

$$V_{G\,max}' = V_{po}\Big|_{2D} = q\,\frac{n_{so}(d+\Delta d)}{\epsilon} \qquad (4.16)$$

If we substitute Eqn.(4.16) into Eqn.(4.15),we can obtain the g_{max},

$$g_{max} = \frac{Z \epsilon v_s}{(d+\Delta d)} \left\{ 1 - \left[1 + \frac{2\,q\,n_{so}\mu\,(d+\Delta d)}{\epsilon\, v_s L} \right]^{-1/2} \right\} \qquad (4.17)$$

Our model predicts a g_{max} of 256 mS/mm gate width,for a normally-on MODFET,whose parameters were given in Figure(51), at V_G'=0V.This transconductance is 7 percent different from the experimental data given in(28),where the transconductance for the same device was 275 mS/mm gate width,whereas the MODFET model using the same parameter estimates a maximum transconductance of 460 mS/mm gate width,nearly two times higher than the experimental result.

a. Effect of Donor-electron Separation

From Eqn.(4.17) it is clear that any reduction in the thickness of the AlGaAs layer under the gate leads to increased transconductances.This can either be done by increasing the doping in AlGaAs (thereby reducing the thickness under the gate) and/or reducing the undoped AlGaAs spacer layer.Reduction of spacer layer thickness also has the added advantage of leading to increased two-dimensional electron concentrations.The resulting increased current carrying capability leads to a faster charging time of device and parasitic capacitances and thus to higher speeds.High speeds can be obtained at small voltage swings and thus at low power consumption.This argument basically leads to the conclusion that the doping level in the AlGaAs layer should be increased as much as possible and the spacer layer should be as small as possible.Schottky barriers are difficult to obtain with a doping level greater than about $2\times10^{18}\ cm^{-3}$ which sets the practical limit.

The second parameter,the spacer layer,can be made as thick or as thin as one desires,that is there is no technological limit by the MBE process.The electron velocity in undoped GaAs and doped($10^{17}\ cm^{-3}$)GaAs layers is 2×10^{7} cm/s and 1.8×10^{7} cm/s respectively.This means that advantage gained in reducing spacer layer thickness must be weighted against the degradation in the electron velocity.

We had Eqn.(4.17) for the maximum transconductance,and

$$d=d_i+\left[\,2\epsilon_2(V_{bi}-V_{off})/qN_d\,\right]^{1/2} \qquad (4.18)$$

where d_i is the thickness of the undoped AlGaAs layer, N_d is the dopant density in the AlGaAs, and

$$V_{bi} \cong \phi_b - \Delta E_c/q \qquad (4.19)$$

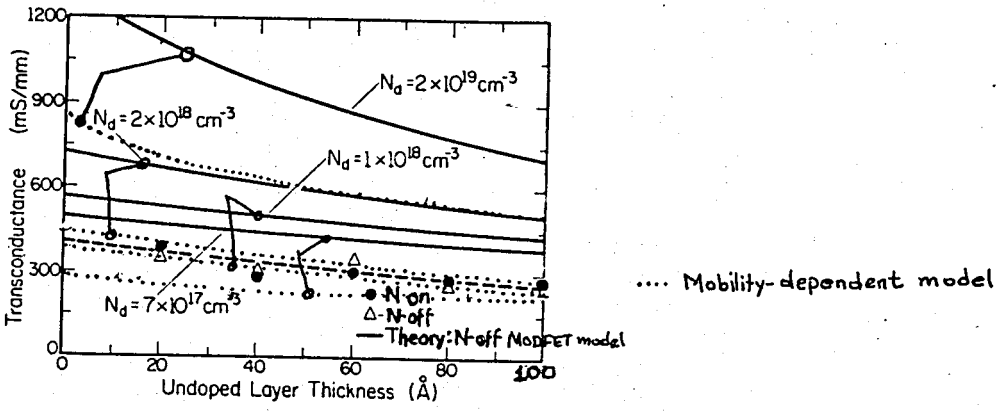
is the effective built-in voltage, where ϕ_b is the Al/AlGaAs Schottky barrier height, ΔE_c is the conduction band discontinuity at the heterointerface.

As can be seen from Eqn.(4.18), increasing doping density reduces d, leading to higher transconductances.

At room temperature when μ is only a weak function of d_i, the transconductance should increase with a decrease in d_i. This reduction in d_i has two effects: first, it increases both the capacitance and the transconductance, second, it increases the sheet carrier concentration, n_s, the maximum voltage swing(Eqn.(4.16)), and the maximum drain saturation current.

Assuming V_{bi} =0.7V, d_i=80 Å, μ=7000cm^2/Vs and independent of d_i at room temperature, we calculate g_{max} as a function of d_i for different doping levels in AlGaAs layer, for a device having gate length of 1μm, and a gate width of 145 μm, and V_{off}=0.2V, using Eqns.(4.17),(4.18), and(4.19). The results are shown in Figure(55).

As seen from the figure, the theoretical calculations using the mobility-dependent model agree very well with the experimental data. Figure(55) also shows that the transconductance is nearly insensitive to the undoped layer thickness for low doping levels.



FIGURE(55) Maximum transconductance per mm gate width as a function of the undoped layer thickness, d_i, for various doping concentrations of AlGaAs layer. Black dotes are experimental values given in (28).

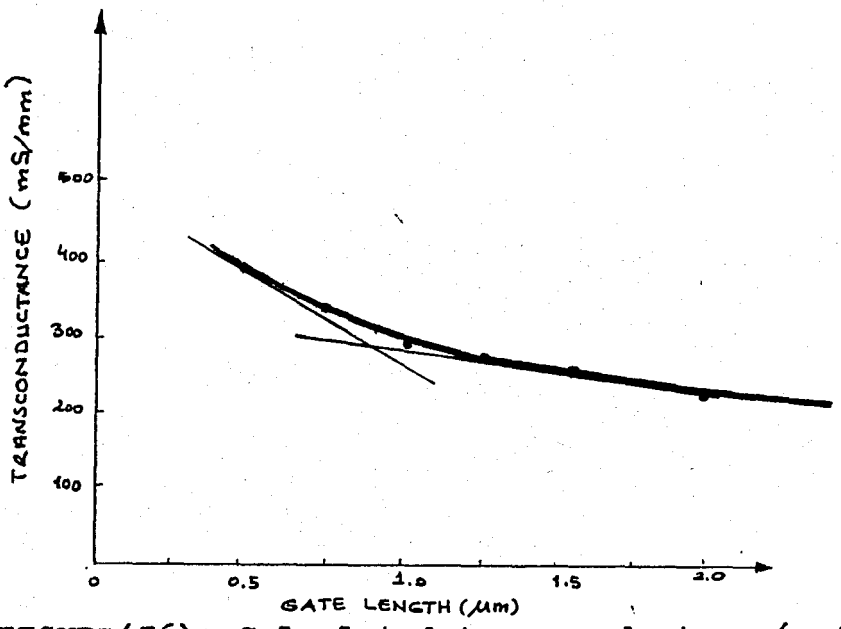
Agreement of our model to the experimental data is the best so far. Other models given before overestimate the transconductance, especially at high doping levels.

In our model the transconductance is dependent on the saturation velocity not on the electron mobility. This is also a good prediction for a short channel(1 μm or less) device,(66).

b. Effect of the Gate Length and the Saturation Velocity

The calculated transconductance values as a function of the gate length are shown in Figure(56). We note from this figure that, the transconductance decreases with increasing

gate length; although beyond L=1μm, the transconductance becomes very weak function of the gate length. Decreasing the gate length not only increases the transconductance but decreases the gate capacitance as well. As a result high frequency performance of the device increases, since f_T is defined as $g_m/2\pi C_{gs}$ where C_{gs} is the gate-to-source capacitance, f_T is the gain-bandwidth product.

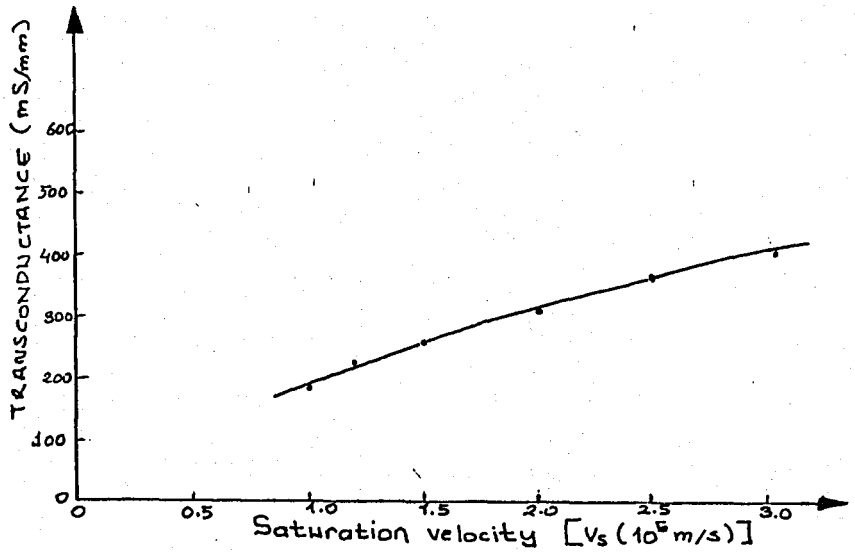


FIGURE(56) Calculated transconductance (using mobility-dependent model) versus gate length for a normally-off MODFET at 300K, at $V_G'=0.6V$ for device with $Z=145\mu m$, $d_d=250$ Å, $d_i=60$ Å, $N_d=1\times10^{18}$ cm^{-3}, $V_{off}=0.2V$.

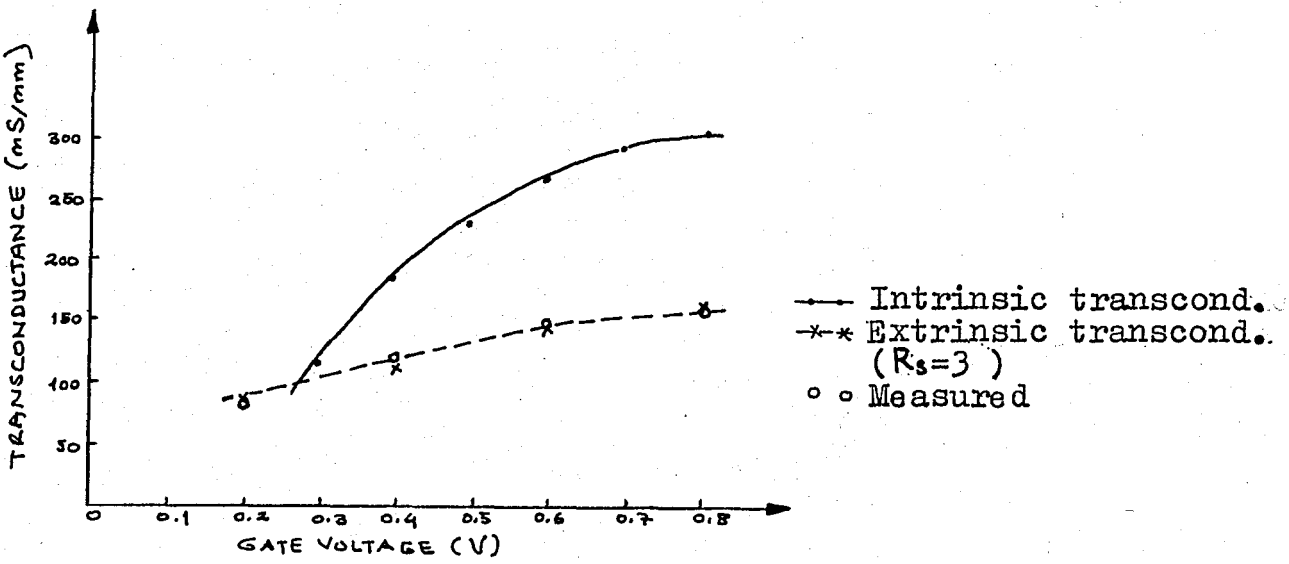
Our model predicts that the transconductance increases with the saturation velocity, but the rate of increase of the transconductance decreases as we go to the higher electron saturation velocities. The results are shown in Figure(57).

Figure(58) shows that the extrinsic transconductances (transconductance in which the source resistance is taken into account) agree very well with the experimental

data,which are nearly constant for gate voltage changes.The theoretically calculated values using $R_s=3\Omega$,which was given as measured source resistance of the device in(28),fit very well to the experimental data.This proves the validity of the model.



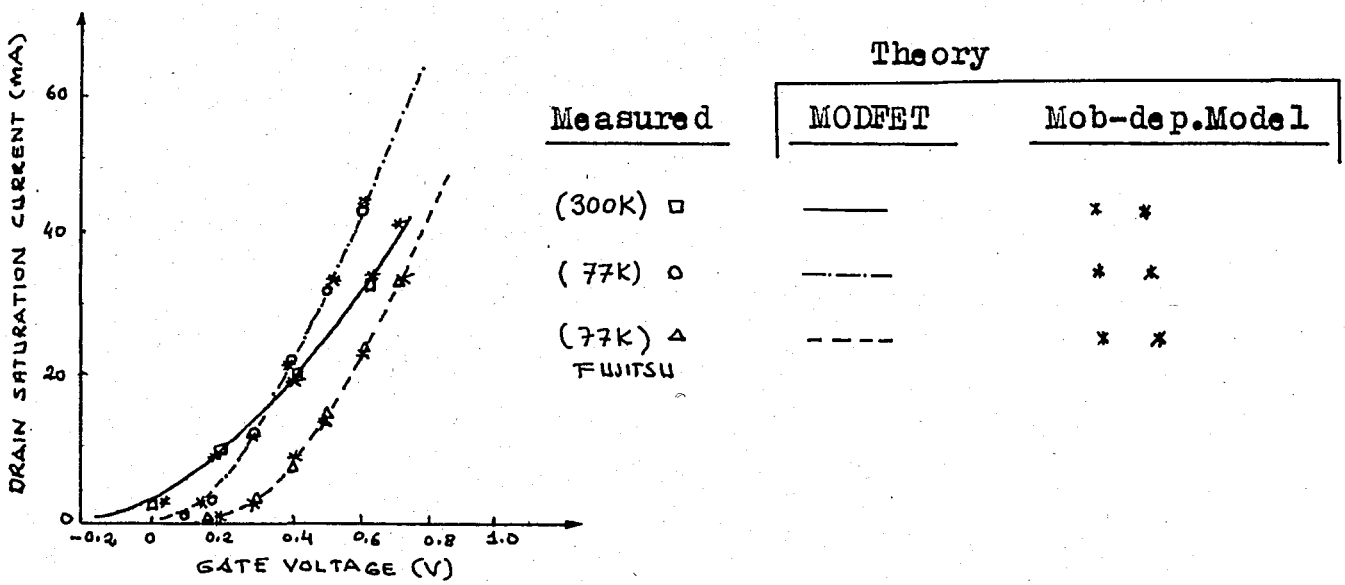
FIGURE(57) Transconductance versus saturation velocity for a MODFET having the same parameters as in Figure(56),and the gate length is 1/mm.



FIGURE(58) Transconductance versus gate voltage for the same device,in comparison with the experimental data given by(28).

F. Cryogenic Temperature Performance

The electron mobility and velocity register an enhancement when cooled to 77K.This is the result of the reduced ionized impurity scattering.Using the mobility-dependent model,the drain saturation currents with respect to gate voltage were calculated at 300 and 77K,and plotted in Figure(59),also shown the experimental data for the MODFET and the HEMT and theoretical calculations using the MODFET model as well.At 300K a saturation velocity of 2×10^5 m/s were used.At 77K v_s is increased to 3×10^5 m/s.The results are in extremely good agreement with the predictions based on pulse measurements(67). Also characterized in Figure(59) is the HEMT operating at 77K.The data,represented as triangles were taken from published Fujitsu drain I-V characteristics given in(27).The dotted line is then calculated using the MODFET model,and the stars are obtained using the mobility-dependent model. The Fujitsu device had a gate length of 2.2μm, d_d=400 Å, d_i=0 Å, Z=300μm, V_{off}=0.18V.To model the device at 77K the reported mobility of 20000cm^2/Vs was used with $v_s=3\times10^7$ cm/s.



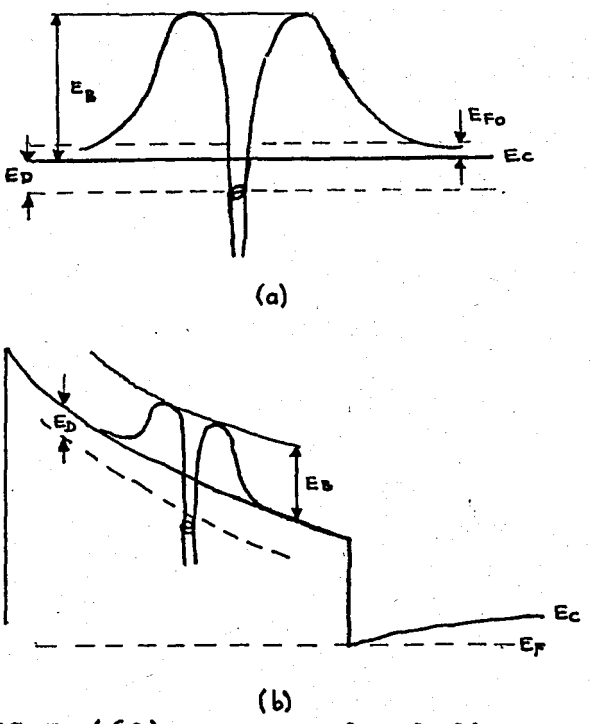
FIGURE(59) Drain saturation current as a function of gate voltage for two devices.

In Figure(59),we have used Z=290μm,d_d=305 Å,d_i=20 Å, V_{off}=-0.03V(at 300K),and V_{off}=0.13V(at 77K) for the MODFET.Our model overestimates the current at high gate voltages about four percent,because at high gate voltages another current path in the AlGaAs layer may form.Since this parasitic MESFET has inferior transport properties comparison with the transport in the undoped GaAs layer,saturation current decreases. This parasitic MESFET action is not modelled here.

We note from Figure(59)that a threshold shift about 0.2V occurs when the device is cooled down to the 77K.In all devices,it was assumed that 25 percent of the electrons in the AlGaAs layer are frozen out at 77K.Hall Measurements(68) on modulation-doped heterostructures,indeed,show that sheet electron concentration decreases with temperature if the sample is not illuminated.This reduction had to be included in the model to account for the observed shift in the threshold voltage as the device was cooled to 77K.

The variation of the threshold voltage of the MODFET with the temperature was modelled(69).It was shown that $V_{off}(T)$ may result from the temperature-dependent occupation of electron traps located in the AlGaAs layer.The freeze-out of electrons was found to be not responsible for the observed shift in V_{off}. The Fermi level shift with temperature and/or the change in occupation of any traps present in the AlGaAs layer,GaAs layer, or at the heterojunction interface are found to be not the causes of the shift in the threshold voltage.Calculations of the Fermi level shift with temperature showed that most of the shift occurs at higher temperatures(at or above 300K) and that the magnitude of the shift(about 25-35 mV)is much

smaller than the observed variation in V_{off}. Thus the conclusion was, at low temperatures, that the shift in V_{off} may be caused by deep traps in the MBE AlGaAs layer; such traps had been revealed by previous studies of a persistent photoconductivity which occurs at low temperatures(70). It had been demonstrated that deep donor traps exist at an energy (E_D) of the order of 50-100 meV below the bottom of the conduction band, in addition, have an energy barrier (E_B) for electron capture of the order of 0.2 eV(see Figure(60)). The value of the activation energy for carrier emission was estimated to be 450 meV.



FIGURE(60) Energy band diagram of AlGaAs with deep donor traps characterized by capture energy E_B and emission energy $E_D + E_B$. a) at equilibrium with E_{F_o} = Fermi level, b) in an AlGaAs/GaAs heterojunction FET near threshold.

This model for threshold voltage shift does not explain the relatively large shift in the threshold voltage at high temperatures(300-400K) even when the variation of the Fermi

level with temperature is included.This may indicate that other types of traps may exist in these structures.More detailed studies are needed to check this hypothesis.More detailed information about the traps,in particular,the value of the barrier energy of capture (E_B),may be obtained from transient capacitance measurements.

G. Capacitance-Voltage Characteristics

In order to find the various device capacitances the total charge under the gate should be calculated.In the Shockley approximation the total charge is given by

$$Q_T = Z\int_0^L q\, n_{so}\, dx = Z\int_{V_S'}^{V_D'} q\, n_{so}\frac{dx}{dV_c}\, dV_c \qquad (4.20)$$

where n_{so} is the maximum carriers per unit area in the 2-DEG. Using the current equation,

$$I=\frac{Z\epsilon\mu}{2(d+\Delta d)L}\,\frac{(u_1^2-u_2^2)}{1-\frac{\mu}{v_s L}(u_1-u_2)} \qquad (4.21)$$

where, $u_1 = V_G'-V_D'$ and $u_2=V_G'-V_S'$, V_G' is the effective gate voltage, V_D' is the drain-to-source voltage, V_S' is the source-to-bulk voltage.Then we have

$$I=\frac{Z\epsilon\mu}{2(d+\Delta d)L}\,\frac{\left[(V_G'-V_S')^2-(V_G'-V_D')^2\right]}{1-\frac{\mu}{v_s L}\left[(V_G'-V_D')-(V_G'-V_S')\right]} = Zq\mu\, n_{so}\frac{dV_c}{dx} \qquad (4.22)$$

$$I = Zq\mu n_{so}\frac{dV_c}{dx} = \frac{Z\mu\epsilon}{(d+\Delta d)}(V_G'-V_c)\frac{\frac{dV_c}{dx}}{1+\frac{\mu}{v_s}dV_c/dx} \tag{4.23}$$

$$qn_{so} = \frac{\epsilon}{(d+\Delta d)}(V_G'-V_c)\frac{1}{1+\frac{\mu}{v_s}dV_c/dx} \tag{4.24}$$

since

$$Q_T = Z\int_{V_s'}^{V_D'} qn_{so}\frac{dx}{dV_c}dV_c \tag{4.25}$$

using Eqn.(4.22)

$$Q_T = Z\int_{V_s'}^{V_D'} Z\mu\frac{(qn_{so})^2}{I}\,dV_c \tag{4.26}$$

Combining Eqns.(4.22),(4.25),and(4.26),

$$Q_T = Z\int_{V_s'}^{V_D'} \frac{Z\mu\left[\frac{\epsilon}{(d+\Delta d)}\frac{(V_G'-V_c)}{1+\frac{\mu}{v_s}\partial V_c/\partial x}\right]}{\frac{Z\epsilon\mu}{2(d+\Delta d)L}\frac{\left[(V_{GS}')^2-(V_{GD}')^2\right]}{1-\frac{\mu}{v_s L}(V_{GD}'-V_{GS}')}}dV_c \tag{4.27}$$

where $V_{GS}' = V_G' - V_S'$

$V_{GD}' = V_G' - V_D'$

$$Q_T = 2ZL\frac{\epsilon}{(d+\Delta d)}\frac{\left[1-\frac{\mu}{v_s L}(V_{GD}'-V_{GS}')\right]}{\left[(V_{GS}')^2-(V_{GD}')^2\right]}\int_{V_s'}^{V_D'}\frac{(V_G'-V_c)^2}{(1+\frac{\mu}{v_s}dV_c/dx)^2}dV_c \tag{4.28}$$

Since $\frac{\mu}{v_s}\epsilon(x) \ll 1$ we can neglect the term which comes from the field dependence to obtain the approximate formula

$$Q_T \cong 2\,Z\,L\,\frac{\epsilon}{(d+\Delta d)}\,\frac{\left[1-\frac{\mu}{v_s L}(V_{GD}'-V_{GS}')\right]}{\left[(V_{GS}')^2-(V_{GD}')^2\right]}\int_{V_S'}^{V_D'}(V_G'-V_c)^2\,dV_c \qquad (4.29)$$

$$Q_T \cong \frac{2}{3}C\left[1-\frac{\mu}{v_s L}(V_{GD}'-V_{GS}')\right]\frac{(V_{GS}')^3-(V_{GD}')^3}{(V_{GS}')^2-(V_{GD}')^2} \qquad (4.30)$$

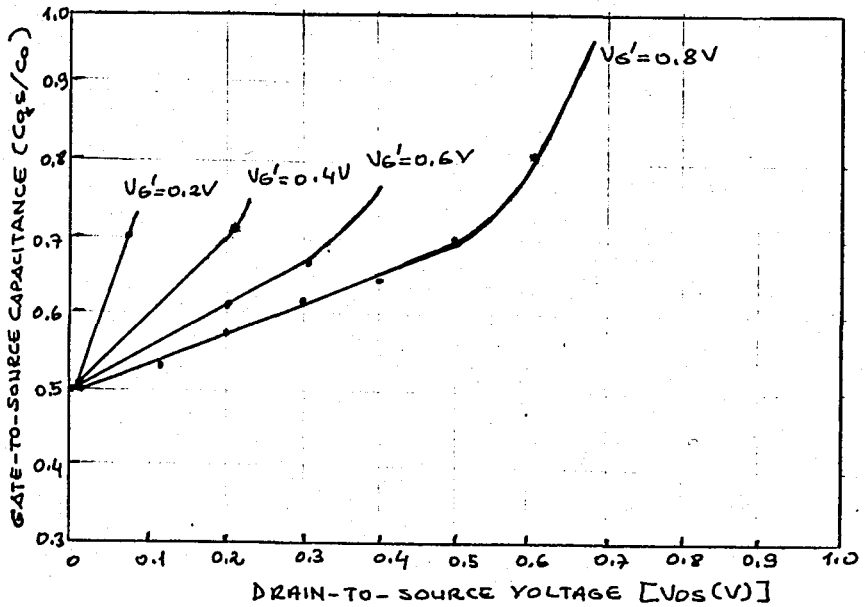
where $C_o = \dfrac{Z\,L\,\epsilon}{d+\Delta d}$

Then, for the gate-to-source capacitance,

$$C_{gs} = \frac{\partial Q_T}{\partial V_{GS}}$$

$$C_{gs} \cong \frac{2}{3}C_o\,(V_{GS}'+V_{GD}')^{-2}\left[\frac{\mu}{v_s L}V_{GD}'(V_{GD}'^2-V_{GS}'^2)+V_{GS}'(V_{GS}'+2\,V_{GD}')\right] \qquad (4.31)$$

In Figure(61), the normalized gate-to-source capacitance C_{gs}/C_o is plotted against the drain-to-source voltage, using the gate voltage as the parameter. These capacitance values are calculated for the region below current saturation. Above saturation, gate capacitance stays constant at about C_o.



FIGURE(61) The normalized gate-to-source capacitance vs. the drain voltage for the same MODFET as in Figure(56).

H. High Frequency Performance

Under high frequency operations, two factors limit the frequency response of an FET: the transit time and the RC time constant. The transit time effect is the result of finite time being required for carriers to travel from source to drain. For the constant mobility case and the saturated velocity case, the transit time is given by

$$\tau = \frac{L}{\mu \mathcal{E}_x} \cong \frac{L^2}{\mu V_D} \qquad (4.32)$$

and

$$\tau = L/v_s$$

respectively. According to this formula, $\tau = 5$ ps at 300K, and $\tau = 3.3$ ps at 77K for a MODFET having gate length of 1μm.

This transit time is usually small compared to the RC time constant resulting from the input capacitance and the transconductance.

It is of interest to assess the gain-bandwidth product, f_T, of the MODFET, since high speed microwave capability depends crucially on the f_T value of the device. The intrinsic gain-bandwidth product f_T of 1μm gate-length MODFET is calculated to be 18 GHz using the device parameters of $Z = 145\mu$m, $d_d = 250$ Å, $d_i = 60$ Å, $V_{off} = 0.2$V, $\mu = 0.68$ m²/Vs, $v_s = 2 \times 10^5$ m/s (at 300K). Here

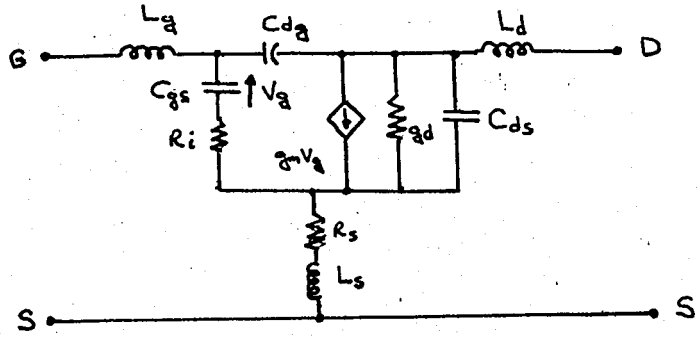
$$f_T = \frac{g_m}{2\pi C_{gs}} \qquad (4.33)$$

where g_m is the intrinsic transconductance of the device. For a 1.4μm-gate HEMT with parameters $V_{off} = -1.5$V, $\mu = 0.65$m²/Vs,

Z=300μm, d_d=1500 Å, d_i=0 Å, the intrinsic gain-bandwidth product is calculated to be 21.5 GHz

To confirm the validity of the calculations, we compare them with the measured common-source s-parameters of the 1.4 μm-gate HEMT given in (40), in the freqency range of 2 GHz to 12 GHz at room temperature. The s-parameters were used to determine the equivalent circuit elements and to derive the the current gain $|h_{21}|$. The equivalent circuit model used to describe the small-signal characteristics of the MODFET is shown in Figure(62). The equivalent circuit includes the intrinsic elements and the extrinsic elements. The intrinsic device consists of low-frequency transconductance g_m, drain conductance g_d, channel resistance R_i, gate-to-source capacitance C_{gs}, and gate-drain feedback capacitance C_{gd}. The extrinsic elements are parasitic source resistance R_s, drain-source capacitance C_{ds}, and source, drain, and gate lead inductance L_s, L_g, and L_d respectively.

The equivalent circuit element values were determined by matching the frequency dependence of s-parameters simulated from the equivalent circuit and are listed in Table 4.1.



FIGURE(62) Equivalent circuit model used to describe the small signal characteristics of the MODFET.

TABLE 4.1 Equivalent circuit parameters of the HEMT

intrinsic elements	extrinsic elements
g_m=37.9 mS	C_{ds}=0.01 pF
C_{gs}=0.3 pF	R_s =20.0 Ω
C_{dg}=0.021 pF	L_s =0.012 nH
R_i=14.1 Ω	L_g =0.56 nH
g_d=5mS	L_d =0.39 nH

The gain-bandwidth product at which $|h_{21}|$=0dB was found to be 17 GHz.The intrinsic gain-bandwidth product f_T was derived to be 20 GHz,which is in good agreement with our theoretically calculated value of 21.5 GHz.

Since $f_T = g_m/2\pi C_{gs}$,increasing the transconductance and decreasing the C_{gs} will improve the f_T.These can be done by decreasing the gate length.As can be seen from Eqns.(4.15) and (4.31),the shorter the gate length,the higher the transconductance and the smaller the C_{gs} .Eqn.(4.31) implies that, an increase in electron saturation velocity will cause the g_m to increase ,hence improves f_T.

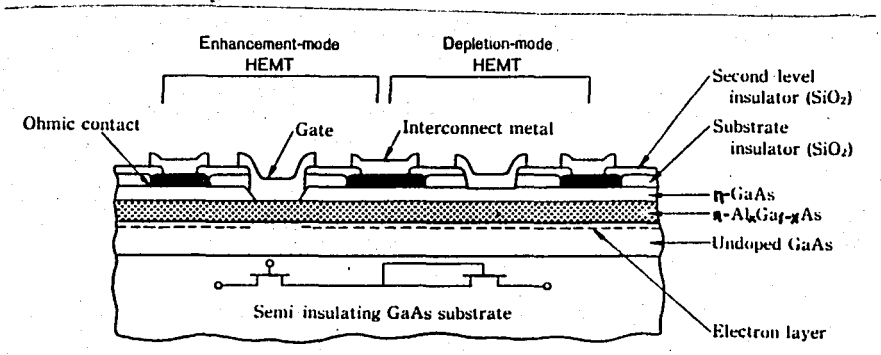
I. Switching Performance

So far,using the MODFET technology,ring oscillators have been fabricated and their performances have been reported in the references(52),and(71).The best propagation delay time obtained is 17 ps at 300K with a power dissipation of slightly under 1 mW per gate with a gate length of 0.7 μm.

At 77K,the best performance is 12 ps with a power dissipation of about 10 mW per gate,which must be trimmed down to about 1 mW to make refrigeration to 77K practical.

Ring oscillators are no-function circuits,having fan-in and fan-out of one;therefore they connot be used to estimate the device performance properly with adequate noise margins. Nevertheless,due to its high electron mobility and high intrinsic gain-bandwidth product,MODFET technology is expected to result in high performance integrated circuits.

Figure (63) shows a cross-sectional view of an experimental inverter structure with enhancement-mode switching and depletion -mode load HEMTs.The doping concentration in the n-AlGaAs and n-GaAs is 2×10^{18} cm^{-3}.The n-GaAs layer of the top epilayer is removed by etching to fabricate an enhancement-mode switching device.

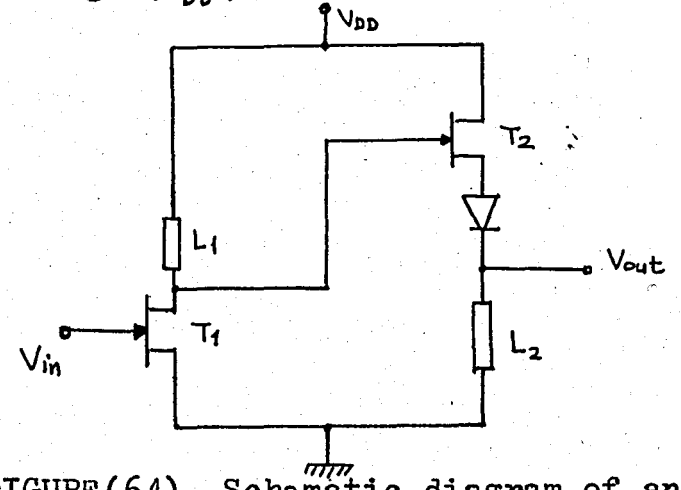


FIGURE(63) Cross-sectional view of the experimental inverter structure with enhancement-mode switching and depletion-mode load HEMTs.

The propagation delay time obtained is 56.5 ps at 300K is encouraging,although the heterostructure used has a complicated epitaxial layer profile and the enhancement-mode

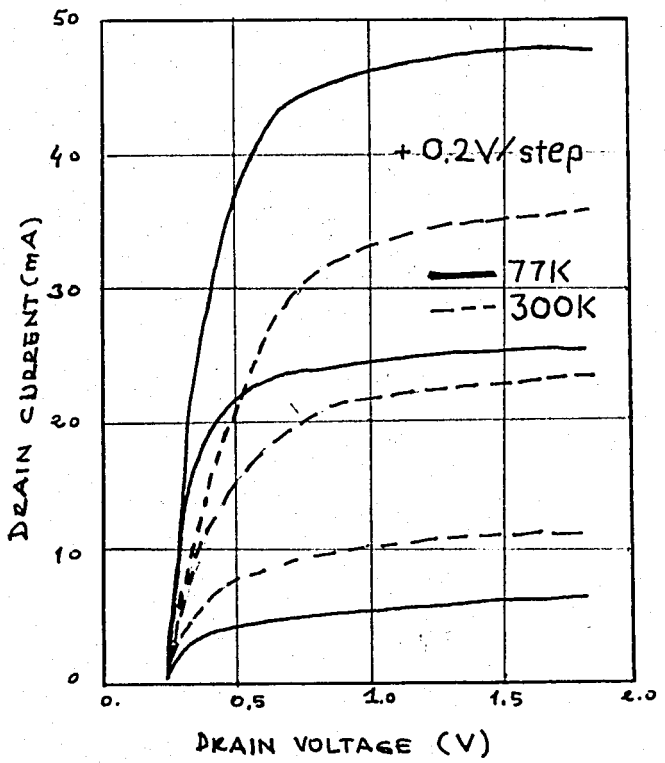
transistor has a recessed gate,which increases the device processing complexity.

We have seen in Chapter four that high performance enhancement-mode TEGFETs can be fabricated in a planar unrecessed gate structure.This advantage of enhancement-mode (E-MODE) TEGFETs has been used to achieve planar high-speed logic circuits,as given in reference(52). A schematic diagram of inverter circuit,which includes unrecessed gate E-TEGFETs as drivers and ungated transistors(TEGFETs) as loads,is shown in the Figure(64).The driver T_1 and the follower T_2 are E-TEGFETs.They were obtained by depositing source,drain,and gate contacts directly on the AlGaAs uppermost layer.The commonly used loads are depletion-mode transistors,but because of their low capacitance,ungated transistors are also appropriate.Ungated transistors have been used in Figure(64).The Direct Coupled FET logic(DCFL) would be possible,since,as we have mentioned before,the threshold voltage is approximately zero across the entire wafer,therefore,the voltage shift of the diode is unnecessary.Elimination of Schottky diode improves the delay time of the inverter.A propagation delay time of 22.6 ps was obtained at room temperature for a supply voltage (V_{DD}) of 3.5V.



FIGURE(64) Schematic diagram of an inverter circuit.

For good switching and amplifier devices,a good saturation, low differential conductance in the current saturation region, and a low saturation voltage are needed.These are obtained quite well in MODFETs particularly at 77K as shown in Figure (65).



FIGURE(65) Drain I-V characteristics of a MODFET with a 300 μm gate width at 300 and 77K (from reference(28)).

To optimize the transistor for use in normally-off logic, the main parameters to be determined are the Al concentration in the AlGaAs,the thickness and the doping of the AlGaAs layer.

(1) Increasing the Al concentration in the AlGaAs increases both the Schottky barrier height of the gate,and the heterojunction interface barrier.These permit higher forward gate voltages on the device,reduced hot carrier injection from the GaAs into the AlGaAs,

and permit higher electron concentrations in the channel without conduction in the AlGaAs.The concentration of Al in the AlGaAs should therefore be as high as possible consistent with obtaining low ionization energies for the donors,good ohmic contacts, and minimum traps.

(2) Maximum voltages on the gate,limited by Schottky diode leakage or by conduction in the AlGaAs,are about 0.8V at room temperature and about 1V at liquid nitrogen temperature.Threshold voltages should be about 0.1V for good noise margins and tolerances.

(3) To maximize transconductance,the AlGaAs layer should be as thin as possible.Thinner AlGaAs implies higher doping to achieve the desired threshold voltage.

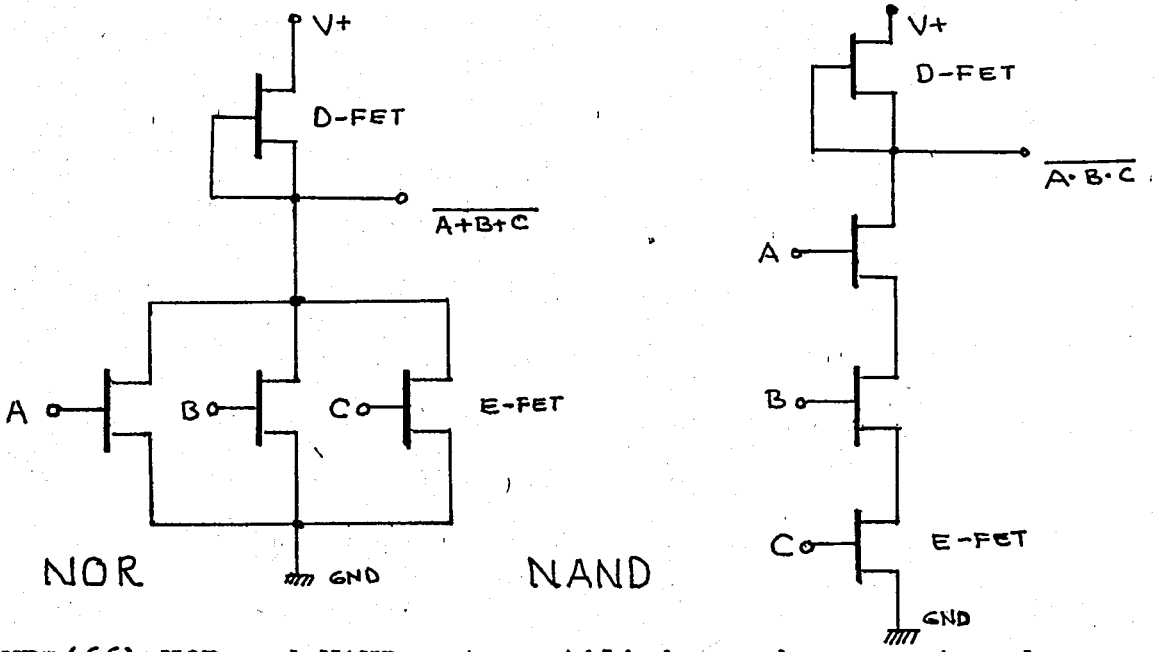
(4) The undoped AlGaAs layer should be as narrow as possible.

A simplified delay equation for the NOR and NAND gates of Figure(66) is given by

$$\text{delay} = (C_D + C_L)V_L / 2\ I_L$$

where I_L is the load current,V_L is the logic voltage,C_D the device capacitance,and C_L the load capacitance which includes the wiring capacitance.To achieve high speeds one needs to develop a high current to voltage ratio.This means that a high transconductance is necessary.The transconductance-gate voltage characteristic should also have a sharp knee so that little of the valuable voltage swing is lost traversing the low transconductance region.The sharp turn-on of the MODFET maximizes the load current of the NOR gate for a given

noise margin and therefore maximizes speed.The maximum transconductance is mainly a function of the saturation carrier velocity,but the sharpness of the knee depends strongly on the lower field part of the velocity vs electric field characteristic and it is the both areas the MODFET excels.



FIGURE(66) NOR and NAND gates utilizing enhancement-mode drivers and depletion-mode loads with gate shorted to source.

Low voltages are the key to low power operation,since the switching energy of the circuit is proportional to CV^2;however operation at low power supply voltages would require a very tight control over the turn-on characteristic of the device. Good uniformity of threshold has been achieved over the distances of a few cm,the best number being about a 10 mV standard deviation,achieved by Fujitsu Laboratories(72).

The higher the mobility and hence low on-resistance of the MODFET make it ideal for circuits where logic is performed by serial connection of devices,as illustrated in Figure(66) for the NAND gate.

In the logic application area,using 1μm gate technology

18.4 ps with a power dissipation of P_d=0.9 mW/stage at 300K was reported .

MODFETs have recently progressed from no-function circuits, e.g.,ring oscillators to frequency dividers.A single-clocked divide-by-two circuit based on the master-slave flip-flop consisting of eight DCFL NOR gates,one inverter,and four output buffers was fabricated(73).This circuit is shown in Figure(67).The circuit has a fan-out of up to three and 0.5μm-long interconnects giving a more meaningful indication of the overall performance of the MODFET integrated circuits than that obtained with a simple ring oscillator.

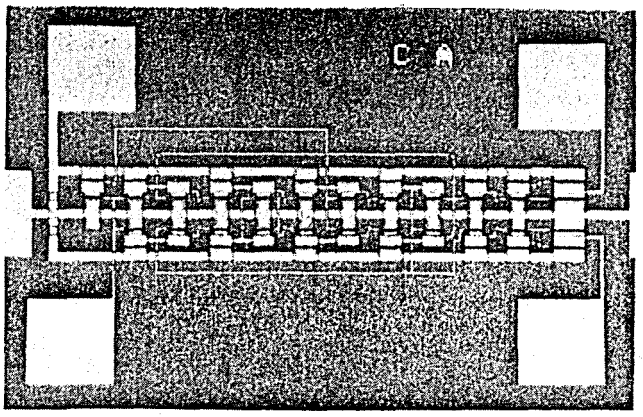
The basic gate consists of 0.5μmX20μm gate enhancement-mode MODFET and saturated resistors as loads.Direct writting electron-beam lithography and lift-off techniques were used throughout the fabrication process.

The maximum clock frequency achieved with these circuits is 8.9 GHz with a power dissipation of 36.8 mW.Oscillope traces of 8.9 GHz input and divide-by-two circuit are shown in Figure(68),(74).

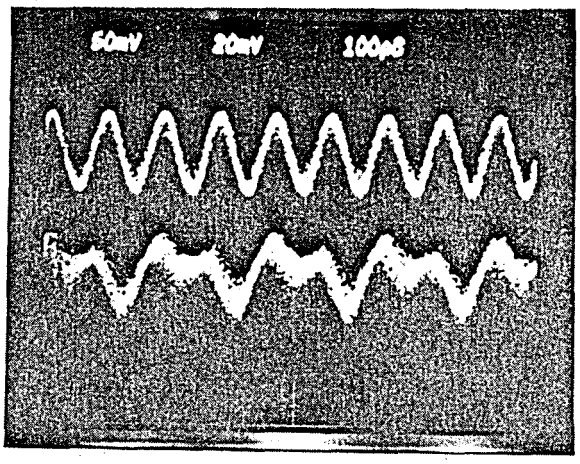
At room temperature,the maximum clock frequency is 5.5 GHz with a supply voltage of 1.31V and with 38.2 mW power dissipation.The logic delays determined from the dividing frequencies are 22 ps per gate with a 2.8 mW per gate power dissipation at 77K,and 36 ps per gate with a 2.9 mW per gate power dissipation at room temperature.

The maximum clock frequency achieved with MODFET technology is roughly two times as high as that of its GaAs MESFET counterpart with comparable geometry.By using complementary-clocked circuits maximum clock frequencies higher than 10 GHz

will be achievable at 77K.



FIGURE(67) Photomicrograph of single-clocked divide-by-two circuit fabricated with electron-beam lithography.

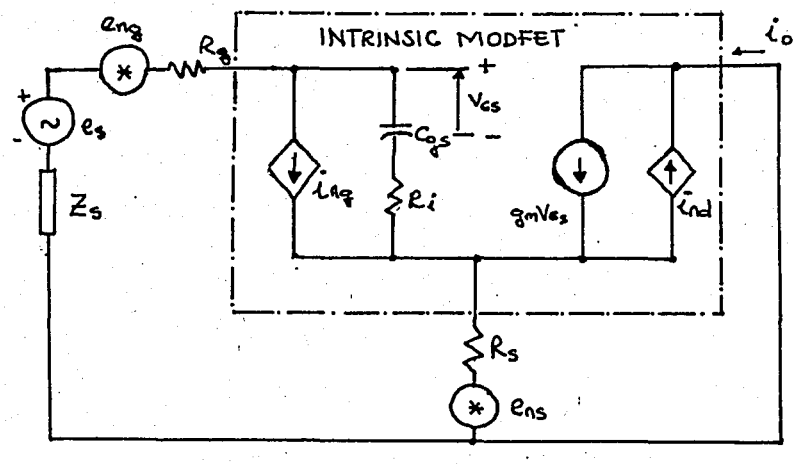


FIGURE(68) Oscilloscope traces of 8.9 GHz input(upper)and divide-by-two output waveforms of the circuit.

K. Noise Characteristic of the MODFET

As an FET,MODFET is a low-noise device,because only majority carriers participate in its operations.However,in practical devices,extrinsic resistances are unavoidable and the parasitic resistances are mainly responsible for the noise behavior.

The equivalent circuit used for noise analysis is same that for GaAs MESFET,illustrated in Figure(69),(75).Noise sources i_{ng},i_{nd},e_{ng},and e_{ns} represent the induced gate noise, drain circuit noise,thermal noise of the gate metallization resistance R_g,and thermal noise of the source series resistance R_s,respectively.The e_s and Z_s are the signal source voltage and the source impedance.The circuit within the semi-dashed lines corresponds to the intrinsic MODFET.



FIGURE(69) Equivalent circuit of the MODFET for the noise analysis.

The MODFET is assumed to operate in the microwave region below the cut-off frequency at room temperature here.The optimal value of the minimum noise figure is designated as F_o has been empirically found for MESFETs(76),and can be used also for the MODFET is given that

$$F_o = 1 + K_f \frac{f}{f_T} g_m(R_g+R_s) \qquad (4.34)$$

where f_T is the gain-bandwidth product and equals to $g_m/2\pi C_{gs}$, K_f is a fitting factor of approximately 2.5,representing the quality of the channel materials,g_m is the transconductance, R_g is the ac series gate resistance in ohms,R_s is the source series resistance in ohms,f is the frequency in Hertz.

For a MODFET with L=1.7μm,f_T =21 GHz,R_s=20Ω,R_g=1Ω, g_m=39 mS,at f=10 GHz we obtained an optimal noise figure of 3 dB,which is very close to the experimental values,justifying the use of the Eqn.(4.34) for this type of device.

In the microwave low-noise FET area,using a 0.55μm gate technology,noise -figures of 1.26 dB,1.7 dB,and 2.5 dB at 10,12,and 17.5 GHz with associated gains of 12,10.3, and 6.6 dB,respectively were obtained ,given by reference (45).

Three stage amplifiers for satellite communications operating at 20 GHz were constructed with a 300K (L=0.5μm) overall noise-figure of 3.9 dB and gain of 30 dB were reported in (72).

The source resistance,R_s,mainly affects the noise performance of the device.If the state of the art source resistance were obtained,almost a two-fold improvement over

GaAs MESFET could be expected as far as the noise performance is considered.

MODFET is a very low-noise device at high frequencies; since at high frequencies dominant noise is the thermal noise generated by the finite resistance of the channel.At this point the superiority of the MODFET appears: since the transport takes place through a 2-DEG,because of reduced scattering processes,nearly no noise is generated at very high frequencies,where the device is normally desired to be used.Moreover,cooling the device down to the liquid nitrogen temperature enhances the noise performance of the MODFET;whereas in conventional FETs operating at low temperatures doesn't make much difference in their operations.

The situations are not the same for the low frequencies where the 1/f noise is effective.MODFET,like MOSFET,suffers from the trap centers in the AlGaAs layer(as trap centers in SiO_2 and at the Si-SiO_2 interface),and hot electron injection to the AlGaAs layer.

When the electrons are heated by the electric field across the channel,they can surmount the energy barrier and transfer into the AlGaAs layer where they may be captured by deep and shallow trap centers.These traps reduce the carrier concentration and mobility and increase the noise. Generation-recombination noise (1/f noise) is caused by the fluctuations in the number of the free electrons.These traps increase the channel resistance by causing depletion layers in the channel and consequently increase the thermal noise.

The 1/f noise contribution at low frequencies is so effective that,the 1/f noise measurement is used to estimate

trap centers in the AlGaAs layer (77).

Therefore,the MODFET,like MOSFETs is noisier than MESFETs at low-frequencies.Nevertheless since the 1/f noise is effective below 1 kHz,it is not very critical in determining the noise performance of the device because the MODFET is a superfast transistor and designed in particular to operate at very high frequencies.

VI. CONCLUSION

In this thesis we have tried to give a general insight enough to understand the state of affairs underlying the FET operation.Heterojunction interfaces,modulation doping concept, and device applications utilizing these structures are described in detail.

The two-dimensional electron gas concept was summarized, and a summary of compound semiconductors was also given. Heterojunction concept and its treatment in theoretical calculations were shown.

New device applications in very fast switching device area were given and their operation principles and features which make them inferior or superior to one another were pointed out.

Future devices,undoubtedly much faster than today's devices,will be the devices fabricated using new materials, because the operation limits are nearly reached in silicon based technology.The new materials,most probably,will be the compound semiconductors.Therefore,those interested in device applications should know some features of compound semiconductors.The other concept that should be understood is the high electric field effects due to reduced device dimensions. Device dimensions are reduced to make drain-source distance shorter,thus, to reduce the time it takes for a carrier to travel from one terminal to the other.Another way to increase the speed of the carriers is to make them less susceptible to scattering mechanisms.The modulation doping technique was presented for this purpose.Using this technique,Coulomb scattering at low temperatures due to the ionized donors

is eliminated and nearly undoped bulk semiconductor conditions are reached with an electron density of 10^{12} cm^{-2} available for current.Therefore,the modulation doping concept was given in detail.

Then the models for the MODFET were given.Comparisons are made.At the end,a new model,called Mobility-Dependent Model was introduced.This new model,introduced in the thesis, uses Lehovec and Zuleeg empirical formula to simulate the velocity-field characteristics of the device.To test the accuracy of the model,measured data of a normally-off and a normally-on MODFET and HEMT were selected and comparisons between measured data and the predictions of the model were made. The agreement between the model and the measured data is the best so far.Better agreement with measured data than those of MODFET and HEMT models for different devices fabricated in the laboratories in the U.S. and in Japan proves the validity of the model.These lead us to conclude that,in such small GaAs FETs,velocity overshoot effect is not likely to happen.We pointed out the reasons for not obtaining velocity overshoot were presence of the substrate layer and two-dimensional character of the channel electric field.

All the models we have seen,including our model,pin the velocity saturation point to the plane at the drain end of the channel.In fact,this plane moves toward the source as the channel field increases.To include this effect,current continuit condition should be established somehow.This can easily be done for MESFETs,where current is controlled by arranging the opening of the channel with gate voltage;whereas in MODFETs,like MOSFETs the current is modulated by increasing or decreasing ban

bending at the interface,thereby modulating the carrier density with the gate voltage.Therefore,assuming a constant opening for current continuity is enough for MESFETs.But an assumption like that couldn't be taken for the MODFET.

All the models assume constant current beyond the saturation point,that is ,they are valid up to the saturation point.Constant current after saturation point means infinite output resistance.In fact,every FET has a finite output conductance.To make the model valid in two regions,the region up to the saturation point and the region beyond the saturation point,a model which can solve the Poisson,Current and Continuity equations numerically in a two-dimensional approach is necessary.Moreover,the two-dimensional character of the electric field in such a small device necessitates this. Solving these equations by finite difference or finite element method is a very hard task since the heterojunction concept makes the mesh generation and determination of boundary conditions very difficult.

Like the other models,our model is invalid at higher gate voltages.Since at high gate voltages another current path forms in the AlGaAs layer and a parasitic MESFET action starts.This was not modeled,because we believe that this phenomenon is a parasitic action of the device and as the improvements in manufacturing techniques and very tight control on the AlGaAs layer thickness and on the doping density in AlGaAs are achieved,this parasitic MESFET action will disappear.

Also,like the other models,the threshold region is not included in this model.Since the two-dimensional gas is a

highly degenerate system,Fermi statistics must be used instead of Boltzman statistics in calculating the electron densities at the heterointerface.Then,to calculate the interface potentials by taking into account the quasi Fermi levels becomes very difficult,making the model unpractical. To consider the weak inversion and the accumulation phenomena thereby to investigate the threshold region, a new model should be introduced.This can be the topic of another study.

Our model,nevertheless,appears to give the best agreeement so far.Its predictions about device performance are quite reasonable.Therefore,it can effectively be used in designing MODFETs.

This study proves that the Lehovec and Zuleeg analysis can be applied to devices made up of GaAs as well.

This thesis is a complete characterization of an FET, including derivation of every FET characteristic,therefore it can also be used as a reference for GaAs FET devices.

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APPENDIX

CALCULATION AND DRAWING THE OUTPUT CHARACTERISTICS OF A NORMALLY-OFF MODFET

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  1 REM MOBILITY DEPENDENT MODE
  2 REM THIS PROGRAM CALCULATES
THE OUTPUT CHARACTERISTICS OF A
MODULATION DOPED FET(MODFET)
  3 REM THE PARAMETERS THAT CAN
BE OPTIMIZED IN MANUFACTURING A
: THE SOURCE RESISTANCE (Rs),TH
THRESHOLD VOLTAGE(Voff),THE AlG
aSTHICKNESS(d),AND THE UNDOPED
lGaAs THICKNESS(di).
  4 REM Rs,Voff ARE ENTERED BY
 DATA STATEMENT,d AND di ARE EN
ERED ANOTHER DATA STATEMENT
  5 REM THIS PROGRAM DRAWS THE
UTPUT CHARACTERISTICS.
 10 PLOT 16,16: DRAW 200,0: DRA
 -2,2: DRAW 2,-2: DRAW -2,-2: D
AW 2,2: PLOT 16,16: DRAW 0,120:
DRAW -2,-2: DRAW 2,2: DRAW 2,-2
 DRAW -2,2: PLOT 16,16
 20 PLOT 16,32: DRAW 2,0: PLOT
5,48: DRAW 2,0: PLOT 16,64: DRA
 2,0: PLOT 16,80: DRAW 2,0: PLO
 16,96: DRAW 2,0: PLOT 16,112:
RAW 2,0: PLOT 16,16
 30 FOR n=1 TO 6
 40 PRINT AT (19-2*n),0;4*n
 50 NEXT n
 60 FOR i=1 TO 4
 70 PRINT AT 20,(1+5*i);0.5*i
 80 NEXT i
 82 PLOT 56,16: DRAW 0,2: PLOT
6,16: DRAW 0,2: PLOT 136,16: DR
W 0,2: PLOT 176,16: DRAW 0,2: P
OT 16,16
 84 PRINT AT 4,0;"Id(mA)"
 86 PRINT AT 21,26;"Vds(V)"
100 READ z,l,m,Vs,e,dd,di,delD
200 DATA 145E-6,1E-6,0.68,2E5,1
.3,370E-10,40E-10,80E-10
300 READ Rs,Rd,Voff
400 DATA 10,10,0.1
410 FOR k=2 TO 8
420 LET Vg=0.1*k
500 LET Eps=e*8.8542E-12
500 LET Vg1=Vg-Voff
550 LET d=dd+di
700 LET x=(z*Eps*m)/(2*l*(d+delD
)
800 LET Id=0
900 FOR n=0 TO 160
000 LET Vd=n*2/160
100 LET y=((m*Vd)/(Vs*l))+1
200 LET Ids=Id
300 LET iD=(x/y)*(Vg1↑2-(Vg1-Vd
↑2)
400 IF Id<Ids THEN GO TO 3000
500 GO SUB 2000
700 NEXT n
750 NEXT k
770 STOP
000 LET Vdsext=Vd+Id*(Rs+Rd)
100 GO SUB 4900
150 RETURN
000 FOR n=n TO 160
200 LET Id=Ids
300 LET Vd=n*2/160
400 GO SUB 2000
500 NEXT n
550 NEXT k
900 PLOT (Vdsext*80+16),(16+Id*
000)
100 RETURN
```