MICROWAVE DIODE SWITCHES

by

Cevat KARAKAYALI

B.S. in E.E., Boğaziçi University, 1981

Submitted to the Institute for Graduate Studies in Science and Engineering in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL ENGINEERING

Boğaziçi University

1984

MICROWAVE DIODE SWITCHES

APPROVED BY

Prof. Dr. Adnan ATAMAN
(Thesis Supervisor) _____

Doç. Dr. Haluk BEKER _____

Y. Doç. Dr. Ömer CERİD _____

DATE OF APPROVAL : January 18, 1984

ACKNOWLEDGEMENTS

This thesis has been prepared for the partial fulfillment of the requirements of Boğaziçi University, School of Engineering for the degree of Master of Science in Electrical Engineering.

I would like to express my sincere gratitude to those who have helped me during the development of this study, especially to my thesis advisor Prof. Dr. Adnan ATAMAN for his invaluable aid.

I also wish to thank Dr. Ömer Cerid for his help.

ABSTRACT

In this study, S-band microstrip stub switch, using PIN diode such as HP 5082-3005 series for the switching element, is designed in the SPST configuration at the central frequency of 2.5 GHz. The design procedure for multiport switches is given.

The theory of PIN diode and microstrip line are presented for the design of the microwave diode switch. Different types of switches are investigated. An experimental results are reported for the purpose of supporting theory.

A microstrip line stub switch has been constructed in which PIN diode provides 24 dB isolation and 1.5 dB insertion loss at the central frequency of 2.65 GHz.

ÖZET

Bu çalışmada, S-bandında 2.5 GHz merkez frekansında, HP 5082-3005 PIN diyodu kullanarak şerit hatlı bir anahtar devresi tasarlanmıştır. Ayrıca çok kapılı anahtar devrelerini tasarlama yöntemi verilmiştir.

Mikrodalga diyodlu anahtar devresini tasarlamak için, PIN diyodunun ve şerit hatların teorisi sunulmuştur. Ayrıca çeşitli anahtar devreleri incelenmiştir. Anahtar devrenin performansını göstermek için deney sonuçları da verilmiştir.

PIN diyodu şerit hattın üzerine yerleştirerek elde edilen anahtar devre, 2.65 GHz merkez frekansında 24 dB isolasyon ve 1.5 dB araya girme kaybı sağlamıştır.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

a	Depletion region width (cm)
A	Area (cm^2)
c	Speed of light (cm/sec)
C_d	Diffusion capacitance (F)
C_f	Fringing capacitance (F)
C_i	Capacitance of the portion of the I layer exclusive of the swept out regions (F)
C_j	Junction capacitance (F)
C_p	Package capacitance (F)
C_T	Total capacitance (F), $C_T = C_j + C_p$
D	Ambipolar diffusion coefficient (cm^2/sec)
D_n, D_p	Diffusion coefficient for electrons, holes (cm^2/sec)
E	Electric field strength (V/cm)
I_d	Diode current (A)
I_F	Forward current (A)
I_o	Bias current (A)
I_R	Reverse current (A)
J_n, J_p	Current density for electron, holes (A/cm^2)
ℓ_{DF}	Effective length of diode for forward bias case (cm)
ℓ_{DR}	Effective length of diode for reverse bias case (cm)
ℓ_{S1}	Length of lower stub (cm)

ℓ_{S2}	Length of upper stub (cm)
L_s	Series inductance (H)
n	Electron density distribution (cm^{-3})
N+	Heavily doped n-type material
n_i	Intrinsic concentration of electrons (cm^{-3})
N_a, N_d	Concentration of acceptors, donors (cm^{-3})
p_i	Intrinsic hole concentration (cm^{-3})
P_a	Absorbed power (W)
P_{cw}	C·W power (W)
$\overline{P}_o$	Power dissipation (W)
$\hat{P}_i$	Peak incident power (W)
P_i	Incident power (W)
P_r	Reflected power (W)
P_t	Transmitted power (W)
q	Magnitude of the electronic charge (C)
q_o	Effective filling fraction charge
Q	Quality factor
R_i	Resistance of the portion of the I layer exclusive of the swept out regions (Ω)
R_I	Intrinsic layer resistance (Ω)
R_s	Series resistance (Ω)
S	VSWR, Voltage standing wave ratio
t	Time (sec)
t_{rr}	Reverse recovery time (sec)
T_A	Ambient temperature (^oC)
V	Voltage (V)
V_{BR}	Breakdown voltage (V)
V_{pT}	Punch-through voltage (V)
V_R	Reverse bias voltage (V)

V_p	Pulse voltage (V)
w	Microstrip transmission line width (cm)
W	Intrinsic layer width (cm)
x	Distance from N-type surface (cm)
x_j	Distance of junction from N-type surface (cm)
X_o	Diode reactance for forward bias
X_s	Diode reactance for reverse bias
Y	Admittance $(\Omega)^{-1}$
Y_o	Characteristic admittance
Z	Impedance (Ω)
Z_o	Characteristic impedance (Ω)
Z_{01}	Characteristic impedance of free space (Ω)
Z_{os}	Stub characteristic impedance (Ω)
α	Attenuation (dB)
Γ	Voltage reflection coefficient
δ	Insertion loss (dB)
ε	Permittivity (F/cm) $\varepsilon = \varepsilon_o \varepsilon_r$
ε_{eff}	Effective dielectric constant
ε_o	Permittivity of free space (F/cm)
ε_r	Relative dielectric constant
η	Isolation (dB)
λ_o	Wave-length of free space (cm)
λ_g	Transmission line wave-length (cm)
μ	Ambipolar mobility (cm^2/V-sec)
μ_n, μ_p	Mobility for electrons, holes (cm^2/V-sec)
ν_o	Propagation velocity (cm/sec)
ν	Lightly doped N-type material

π	Lightly doped p-type material
ρ_I	Resistivity (Ω-cm)
σ	Conductivity $(\Omega\text{-cm})^{-1}$
τ	Life time (sec)
τ_n, τ_p	Recombination life time for electrons, holes (sec)
Φ	Transmission line phase shift
ϕ	Built-in potential (V)
ψ	Potential (V)
ω	Angular grequency (rad/sec)

INTRODUCTION

Microwave switches, which their operations depend on the action of diodes, are used increasingly in microwave systems because of their valuable advantages of light weight, and low driving (or bias) power. Typical applications are transmit-receive (T-R) switches for pulsed radars and digital phase shifter for phased-array antennas.

Microwave transmission lines are usually coaxial, stripline, or wave-guide. For some years a technique for a switching microwaves in x-band wave-guide with semiconductor diode has been in use (1). But using microstrip line for switching element can be fabricated at a substantially lower cost than wave-guide or coaxial circuit configurations. This thesis includes a theoretical background on the PIN diode, microstrip transmission line, theoretical and practical design of the microwave switch.

The switching action of the PIN diode results from the variation of the I-layer resistance with applied signal level. At zero bias, the I-layer has a high resistance and hence the diode acts as a fairly high Q capacitance at microwave frequencies. This effect is very beneficial for a diode which is intended for use as a microwave switch because the

lower the capacitance the higher the impedance of the diode under reverse bias, and the more effective the device is as an "open circuit". In the forward bias state, the I-layer resistance is considerably lower due to conductivity modulation and the diode acts as a low resistance. Such conductivity modulation can be produced by the dc bias.

Chapter 1 is concerned with an analysis of the properties of the PIN diode in both the forward and reverse state. The I-layer resistance for dc injection is calculated here in elementary fashion using the stored charge method. We also point out the advantages of the PIN diode for the microwave switch.

In Chapter 2, we introduce the basic concepts on the microwave switch. Diodes modes are discussed. The power handling capacity is given.

In Chapter 3, the properties of microstrip transmission lines are investigated. We also point out the advantages of microstrip transmission lines. Microstrip transmission line design chart is given.

In Chapter 4, we introduce different types of switches. We also design the microstrip stub switch in SPST configuration. The design procedure for multiport switches is given.

Chapter 5 is concerned with the driver circuit consideration for PIN diode RF switch. High speed driver cir-

cuit configurations are given.

Chapter 6 summarizes the experimental results and the conclusions of this study.

CHAPTER 1

PIN DIODES AND THEORY OF MICROWAVE OPERATION

1.1. INTRODUCTION

The PIN diode should not be thought of as something physically different from the PN junction (2), but its structure is somewhat different. We know that with the abrupt junction the width of the depletion zone is inversely proportional to the resistivity of P or N region, whichever has the lesser impurity doping concentration. Under zero and reverse bias, the diode has very high impedance at microwave frequencies, whereas at moderate forward currents it has a very low impedance. This permits the use of a PIN diode as a switch in a microwave transmission line.

1.2. STRUCTURE AND PUNCH-THROUGH VOLTAGE

In a PIN diode, the semiconductor wafer has a heavily doped P region and a heavily doped N region separated by a layer of high-resistivity material that is nearly intrinsic. Often the thickness of the high-resistivity layer lies in the range between 10 and 200 μm. Electrical contact is made to the two heavily doped regions. The dopping profile for the

wafer is illustrated in Figure 1.1. The dopping profile is achieved by diffusing an N-type dopant from one side of the wafer and a P-type dopant from the other side, the wafer being initially of high-resistivity P-type (π) material (see Fig. 1.1, broken curve). N-type material can be treated as well by making appropriate changes in the sign of the concentration and using the appropriate values of mobility for the majority carriers.

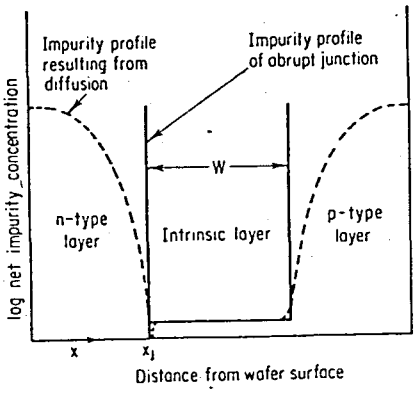


FIGURE 1.1. Doping profiles for PIN structure.

Ideally it would be desirable for the I-layer material of the diode to be intrinsic. With an intrinsic I-layer, the RF loss of the PIN diode under reverse bias would be minimized, and its capacitance would vary least with reverse-bias voltage. In practice, a truly intrinsic layer does not exist in a PIN diode, because it has not been technologically feasible to maintain intrinsic resistivity in the I-layer through the processing of a diode. Thus the concept of P+ and N+ layers

separated by an intrinsic region is somewhat artificial. To distinquish unusually heavily or lightly doped material, special nomenclature has evolved. Heavily doped P and N material are referred to as P+ and N+, respectively, the Greek letters are used; thus high-resistivity P material is called π-type and high-resistivity N material is called ν-type. Typically the I-layer has a resistivity of 1000 Ω-cm and is either π-type or ν-type.

Now the question arises as to the differences between the ideal PIN diode having a truly intrinsic layer and a practical PIN diode, in which the I-layer is actually, for example, a π layer. Let us consider what happens to the space charge and electric field for the ideal and the practical diode as we applied reverse bias (P+ layer negative). Figure 1.2 illustrates the comparison. At zero bias, the diffusion of the holes and electrons across the junction causes space-charge regions of thickness inversely proportional to the impurity concentration to form in the P+ and N+ layers adjacent to the I-layer. The ideal PIN diode which actually does have so high a resistivity I-layer, that it is depleted at zero bias is called a zero punch-through diode, because the depletion region has "punched through" to the high conductivity region even before bias is applied. Thus we have a region of fixed negative charge in the P+ layer and a region of fixed positive charge in the N+ layer, with equal charge in the two layers but no charge in the I-layer. As Fig. 1.2 shows, a uniform electric field appears in the I-layer, dropping linearly to zero through the depletion regions in the N+ and P+ layers

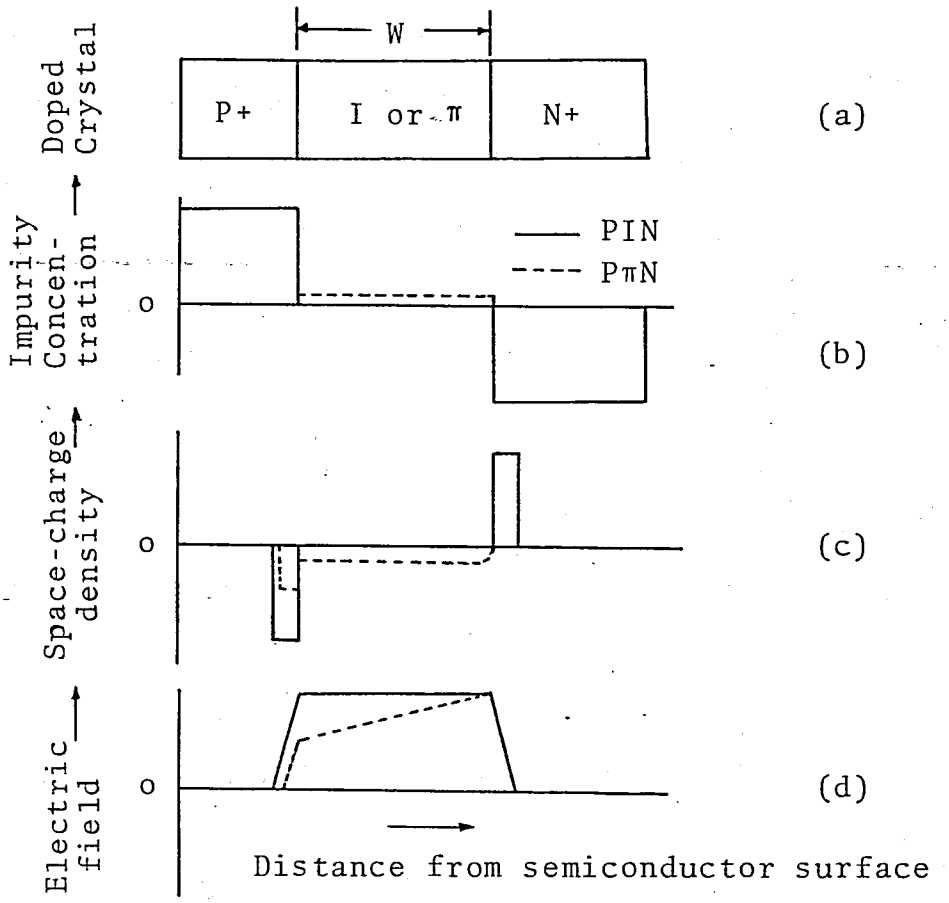


FIGURE 1.2. Doped crystal, impurity, charge and field distributions in PIN and PπN junctions.

If the high-resistivity layer were actually a π layer, the situation would be somewhat different. Figure 1.3 shows schematically a practical PIN diode with ionized impurity profiles at zero bias and punch-through. At zero bias a large portion, but not necessarily all, of the I region impurities have been ionized and the depletion region, a(o), may be somewhat less than the I layer width, W. As reverse bias voltage is applied to this diode, depletion region spreading occurs. At this voltage the depletion region width, $a(V_{pT})$, is appro-

ximately equal to W. Further spreading of the depletion layer into the low resistivity P+ and N+ regions, is for most applications, negligible. The voltage at which the depletion region just reaches the P+ contact is the punch-though voltage or swept-out voltage, V_{pT}.

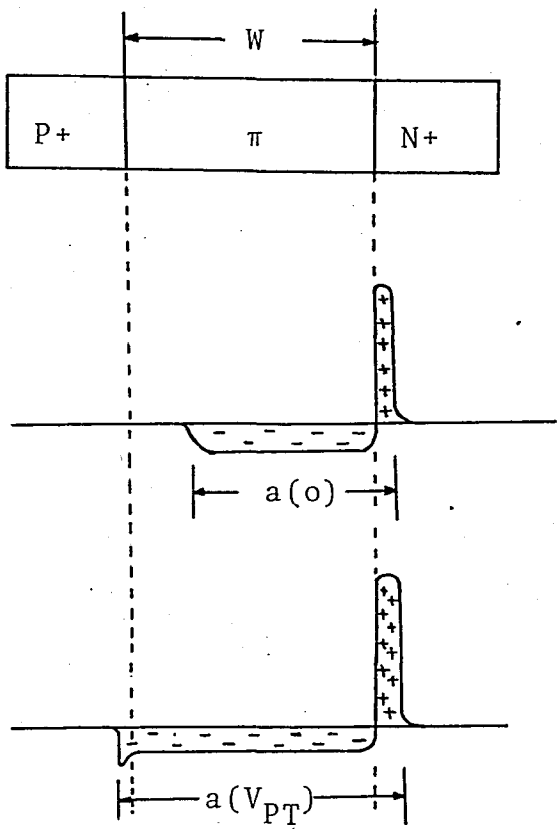


FIGURE 1.3. Practical PIN with ionized impurity profiles at zero bias and punch-through.

It is important in many microwave applications to have the π region swept-out, lest the current flow by mobile carriers in the resistive π region constitute an undue source of signal loss. Hence, when PIN diodes are used as microwave switches and they are biased in the OFF condition, the bias

is usually well beyond the swept-out voltage. With increasing bias, beyond that required to sweep out the π layer, a thin depletion region appears in the P+ layer. The electric field rises steeply in the N+ depletion region, decays slowly across the π layer, and drops steeply to zero in the P+ depletion region. Figure 1.2d shows a comparison of the electric field profiles for the cases of an ideal intrinsic layer and a practial π layer. The comparison is made assuming equal peak values of electric field for two cases. The voltage across each diode is proportional to the area under the electric field profile. As is apparent, the voltages for the two cases illustrated are not the same.

In summary, the I-layer of the ideal diode is swept-out at zero bias or any reverse bias, whereas in a practical diode a small bias must be used if the assumption of an ideal diode is appropriate if we restrict ourselves to bias voltages sufficient to sweep-out the I-layer.

1.3. THE EQUIVALENT NETWORK

The analysis of microwave structure containing PIN diodes is done most readily if the diodes are represented by lumped-element networks. This is justified by the fact that a diode is ordinarily small compared with the wavelengths of the applied fields. The network shown in Figure 1.4 is a rather detailed representation of a typical diode. This representation is quite general, being applicable at low and

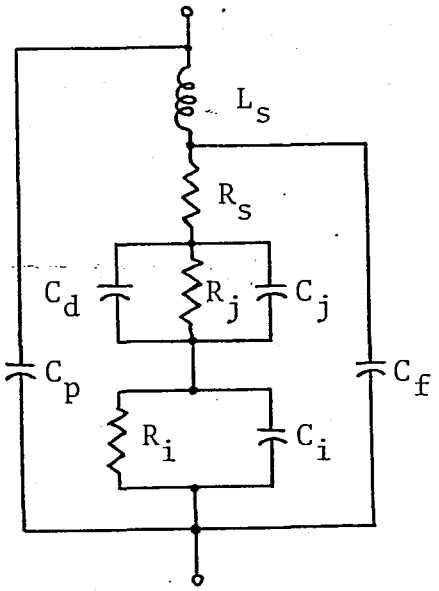


FIGURE 1.4. Equivalent network of PIN diode.

high frequencies and under various bias conditions. For most analyses, certain elements of this network can be disregarded without serious loss of accuracy. We shall say more about simplifying the network shortly. But first it is important to identify each element of this generalized network with specific parts of the diode and to consider how the individual resistances and reactances arise.

The elements L_S, C_p and C_f results from the connection of leads to the semiconductor wafer and the packaging of the wafer. L_S is the total series inductance, concentrated in the leads; C_p represents the stray capacitance shunted across the wafer by the package or encapsulation; C_f, referred to as the fringing capacitance, is the stray capacitance shunted across the wafer from the leads. The remaining elements in Fig. 1.4 are disposed within the semiconductor wafer itself.

The depletion region in the wafer exhibits reactance and resistance. The capacitance C_j arises because of the charge storage at the boundaries of the depletion region. The resistance R_j is the reciprocal of the conductance caused by carriers generated within the region. Another contribution to the capacitance of this region is called the diffusion capacitance C_d. It represents charge storage as current flows through the depletion region. That is, under forward bias, mobile carriers are injected into the I-layer during the forward portion of the rf cycle, and some of these carriers are subsequently extracted during the other half of the cycle. This storage of charge is accounted for by the diffusion capacitance.

R_i and C_i represent simply the resistance and capacitance of the portion of the I-layer exclusive of the swept-out regions. R_s is the sum of the P+ and N+ layers and any resistance associated with the contacts to these layers.

Table 1.1 lists the values of the elements of Fig. 1.4 for a typical PIN diode under three different bias conditions and at 1.3 GHz.

The following sections describe the action of a diode under reverse bias and forward bias and demonstrate what happens in switching from one bias condition to another.

Diode Element	Bias		
	0V	50V reverse	25 mA forward
C_j	0.8 pF	0.17pF	>> 10pF
C_d	Negligible		> 3pF
C_i	0.25pF	∞	>0.25pF
C_f	0.02pF	0.02pF	0.02pF
C_p	0.3 pF	0.3 pF	0.3 pF
L_S	0.3 nH	0.3 nH	0.3 nH
R_S	0.3 Ω	0.3 Ω	0.3 Ω
R_j	$>10^9\Omega$	$>10^9\Omega$	<0.1 Ω
R_i	2.500Ω	0.0	0.5 Ω

TABLE 1.1. Typical equivalent network values.

1.4. BEHAVIOR UNDER REVERSE BIAS

The simplified equivalent circuit for a PIN wafer (idealized profile of Fig. 1.1 with parasitics neglected) under sufficient reverse bias to partially sweep-out the I-layer is simply that of Figure 1.5a. Since the resistance of the depletion layer R_j is orders of magnitude higher than the reactance of the depletion layer $-1/\omega C_j$, we can neglect R_j. With an I-layer of reasonably high-resistivity material, the resistance of the undepleted portion of the I-layer R_i will be considerably larger than $1/\omega C_i$. Although we are not justified in neglecting the R_i entirely, we can transform the circuit into that of Fig. 1.5b without appreciable loss of ac-

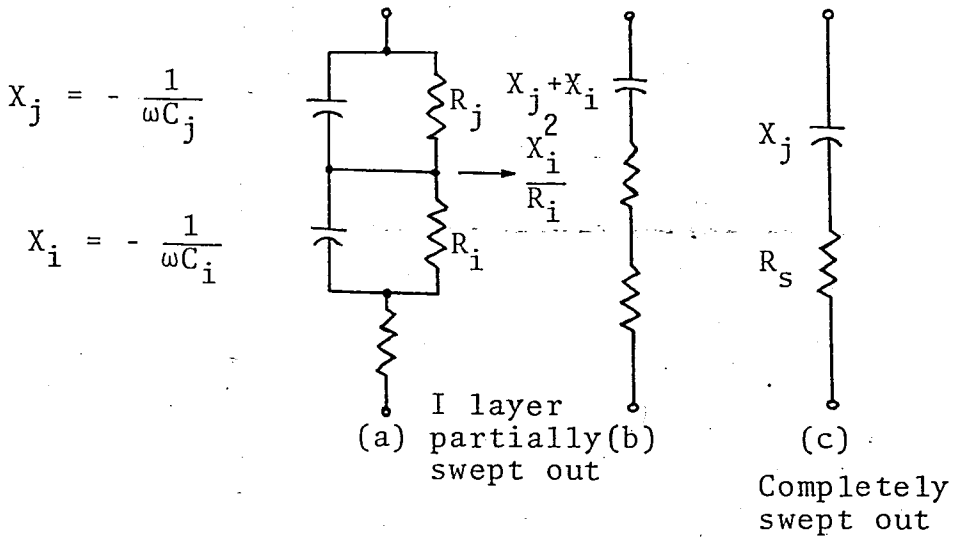


FIGURE 1.5. Approximate equivalent networks for PIN diodes under reverse bias at microwave frequencies.

curacy. The total reactance $X_j + X_i$ is essentially that of the capacitance between the N+ and P+ layers and is independent of bias. Thus, the PIN diode is virtually a constant-capacitance device with respect to bias variations.

If the bias is enough to sweep-out the I-layer, R_i and X_i in Fig. 1.5 become zero, and we have simply R_S in a series with the diode capacitance, as in Fig. 1.5c. Since, with care in fabrication, R_S can be made quite small, a PIN diode with moderate reverse bias will act as an almost lossless constant capacitance in a microwave circuit.

1.5. BEHAVIOR UNDER FORWARD BIAS

At zero bias, the resistance X_i^2/R_i in series with the diode capacitance (Fig. 1.5b) is relatively large, because most of the I-layer is not depleted of mobile carriers. As increasing forward bias is applied to the diode, carrier injection into the I-layer becomes significant. Electrons are injected into the I-layer from the N+ layer, and holes are injected from the P+ layer. The carriers diffuse into the I-layer because of recombinations, as shown in Figure 1.6. This results in the carrier concentrations in the I-layer becoming raised above their equilibrium levels, and the resistivity drops as forward bias is increased. The hole and electron concentrations are about equal throughout the I-layer. If the carrier life times in the I-layer are relatively long and the I-layer is not too thick, the I layer becomes flooded with carriers at reasonable forward-bias levels. When this happens, the diode exhibits low resistance and, in fact, appears as a virtual short circuit across a microwave transmission line. Even if the microwave signal is very large, with substantial forward bias the diode impedance remains low because of the large amount of charge stored in the I-layer.

The effect of controlling the carrier density, and hence the resistance in the I-layer, by varying the forward bias is known as "conductivity modulation".

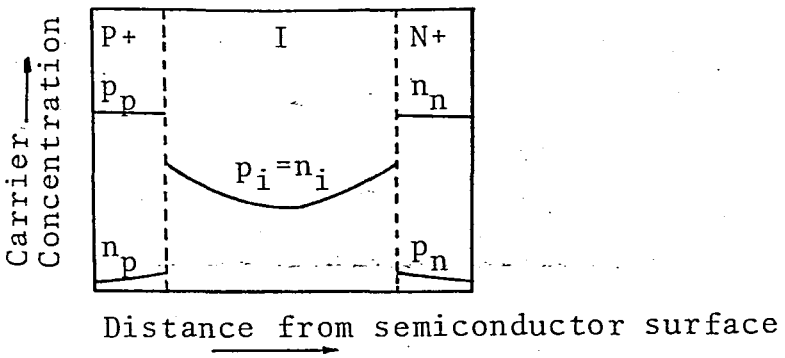


FIGURE 1.6. Typical carrier distribution in I-layer of PIN diode under forward bias.

1.6. SWITCHING FROM ONE BIAS STATE TO ANOTHER

Since one of the important uses of a PIN diode is as a microwave switch, we need to consider also the behavior of the diode during the switching process. First, let us examine the behavior of a reverse-biased diode when a forward-bias voltage is suddenly applied. Assuming that I-layer was entirely depleted of mobile carriers, the depletion region collapses almost instantly. The injection of carriers begins immediately, although some finite interval is required before the I-layer can fill up with carriers to its equilibrium value. During this charge-storage interval, the distribution of carriers in the I-layer is quite uniform, since the transit time for carriers in the I-layer is ordinarily short compared with the time required to reach equilibrium, and the carrier lifetime is long compared with the transit time.

One might expect that the diode impedance during turn-on (forward to reverse bias) would retrace the turn-on curve of impedance vs time. This is not the case, however, because the distribution of carriers in the I-layer is different for two cases. When a reverse voltage is applied to the diode, the electroncs leave the I region as a wall of carriers heading back to the N+ side. The holes are similarly moving back toward the P+ side with a widening depleted I region. The depletion region form at the boundaries of the I-layer, as shown in Figure 1.7.

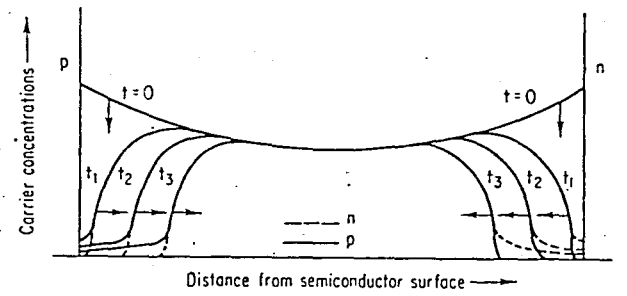


FIGURE 1.7. Sweeping out of I-layer and widening of space-charge regions after switching from forward to reverse bias.

The forward biased transient of a PIN diode is resistive (3), the RF admittance going across the middle of the Smith Chart as shown by curve A in Figure 1.8. The reverse biased transient is quite different. Thus, rapdily going from the forward conduction to the reverse bias state, the PIN diode behaves like a capacitor going from $C=\infty$ to $C=C_{MIN}$ and gives the admittance shown as curve B in Fig. 1.8. Figure

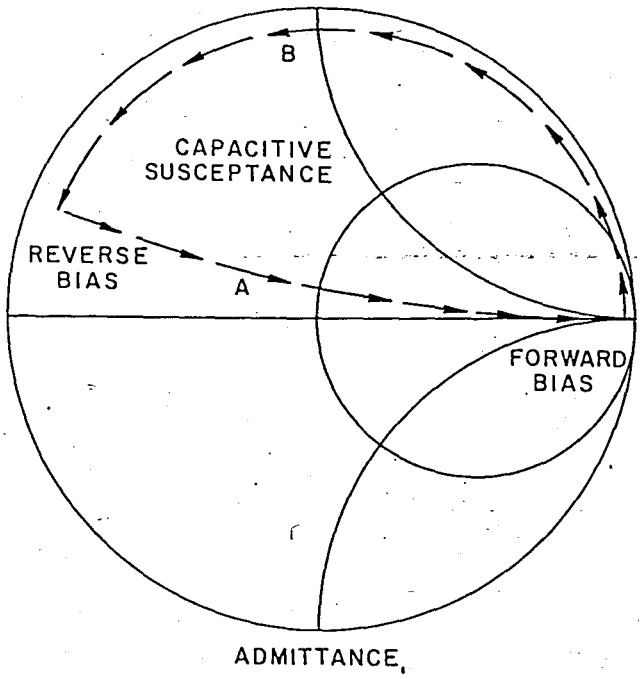


FIGURE 1.8. Diode admittance for turn-on (A) and turn-off (B) transients.

1.9 illustrates the change in impedance with time after reversing the applied bias in order to turn the diode on and off. The switching speed with which charge is removed from the diode during turn-off depends on the rise time and amplitude of the switching-voltage pulse applied to the diode.

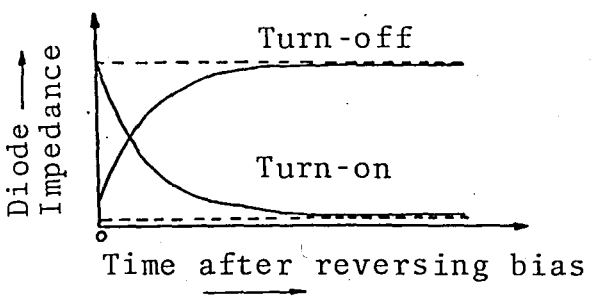


FIGURE 1.9. Switching transients for PIN diodes.

1.7. CALCULATIONS OF DIODE IMPEDANCE

We shall use very simple models to calculate the impedance of a PIN diode under forward and reverse bias. First, let us consider reverse bias. We shall assume the impurity profile of the diode to be that of the abrupt junction shown in Fig. 1.1. As will be seen, this model does not give accurate values of the reverse-bias series resistance for most diodes. However, besides keeping the mathematics simple, it does demostrate two important features of diode behavior: (1) the decrease of series resistance with increasing bias voltage and (2) the invariance of diode capacitance with bias voltage. We assume that the I-layer consists of π-type material and that the P+ and N+ layers are very heavily doped. The analysis is similar to that for the abrupt junction. Because of our assumption about doping, the depletion region in the N+ layer will be so thin that we can neglect it and assume that the entire sum of the applied and built-in voltages appears across the depletion region in the I-layer.

We start with Poisson's equation

$$\frac{dE}{dx} = -\frac{d^2\psi}{dx^2} = 0 \qquad x < x_j \text{ amd } x > x_j + a \qquad (1.1)$$

$$\frac{dE}{dx} = -\frac{d^2\psi}{dx^2} = -\frac{q}{\epsilon} N_a \qquad x_j < x < x_j + a \qquad (1.2)$$

where

ψ - potential, V

ε - permitivity, ($\varepsilon = \varepsilon_o \varepsilon_r$), farad cm^{-1}

q - charge of the electron, coulombs

E - electric field, volts cm^{-1}

N_a - number of acceptors per cm^3

a - the thickness of depletion region in the I-layer, cm

x - distance from N-type surface, cm

x_j - distance of junction from N-type surface, cm

Integrating Eq (1.1) and applying the boundary condition that the electric field E vanishes at $x=x_j+a$ and is zero outside the depletion region gives us

$$E = \frac{q}{\varepsilon} N_a (x_j + a - x) \qquad x_j < x < x_j + a \qquad (1.3)$$

We integrate the electric field over the depletion region and equate the integral to the algebraic difference between the applied voltage V (negative for reverse bias) and the built-in voltage ,

$$- V + \phi = \int_{x_j}^{x_j + a} E \, dx = \frac{q}{\varepsilon} N_a \frac{a^2}{2} \qquad (1.4)$$

We can solve this relation for the thickness of the depletion region,

$$a = \left[\frac{2\varepsilon}{qN_a} (-V + \phi)\right]^{\frac{1}{2}} = \left[2\varepsilon\mu_p \rho(-V + \phi)\right]^{\frac{1}{2}} \qquad (1.5)$$

where the I-layer resistivity $\rho = 1/\mu_p \, qN_a$, μ_p being the hole mobility.

We can calculate the values of C_j, C_i, X_j, X_i and R_i in Fig. 1.5.

$$C_j = \frac{\varepsilon A}{a} \qquad C_i = \frac{\varepsilon A}{W-a} \qquad R_i = \frac{\rho}{A}(W-a) \tag{1.6}$$

where W is the thickness of the I-layer.

Since R_j is very large in comparison with X_j, we can approximate the total impedance of the I-layer by

$$Z = R + jX \approx j\left(X_j + \frac{X_i R_i}{R_i + jX_i}\right) \tag{1.7}$$

substituting the expressions for C_j, C_i and R_i from Eq. (1.6) gives series resistance and reactance of the I-layer:

$$R = \frac{\rho(W-a)}{A(\rho^2\omega^2\varepsilon^2+1)} \quad \text{and} \quad X = \frac{-\rho^2\omega\varepsilon}{A(\rho^2\omega^2\varepsilon^2+1)}\left(W + \frac{a}{\rho^2\omega^2\varepsilon^2}\right) \tag{1.8}$$

If $\rho\omega\varepsilon >> 1$, we can approximate the resistance and reactance as

$$R \approx \frac{W - \left[2\varepsilon\mu\rho(-V+\phi)\right]^{\frac{1}{2}}}{\rho\omega^2\varepsilon^2 A} \qquad 0 \geq V \geq \phi - \frac{W^2}{2\varepsilon\mu\rho}$$

$$R = 0 \qquad V < \phi - \frac{W^2}{2\varepsilon\mu\rho}$$

$$X \approx \frac{-W}{\omega\varepsilon A} \tag{1.9}$$

where we have substituted for a the expression given in Eq.

(1.5). We have shown that if the operating frequency and the I-layer resistivity are high, the capacitance of the I-layer is independent of the bias voltage and is equal to that of a parallel-plate capacitor of separation W and plate area A. These conditions are well satisfied for PIN diode used at microwave frequencies. We have shown also that the resistance of the I-layer decreases with increasing bias voltage V, as well as with increasing operating frequency and I-layer resistivity and permitivity.

Now the steady-state microwave impedance of a PIN diode with high carrier injection levels in the I region resulting from a dc forward bias is calculated. It is assumed that the major portion of this impedance is the resistance of I-layer; thus, the resistance of the contacts or of the heavily doped P+ and N+ regions and junction impedance which have been negligible effect at microwave frequencies, or parasitics of the encapsulation shall not be considered. The I-layer resistance for dc injection is calculated here in elementary fashion using the stored charge method; in Appendix B, a more exact expression is obtained by solving the diffusion equation to determine carrier distribution in the I-layer.

Let us consider again the abrupt-junction model of Fig. 1.1. Under forward bias, the injection into the I-layer of holes from P+ layer and electrons from the N+ layer will take place. Let us assume that the I-layer doping is sufficiently light that the carrier concentrations without injec-

tion are negligible in comparison with the injected carrier concentrations and that all carrier recombination takes place within the I-layer. With highly doped P+ and N+ layers, the injection of holes into the N+ layer and of electrons into the P+ layer will be negligible. In the steady state, then, the dc bias current will be exactly the current needed to replace the carriers lost by recombination. We shall also assume that the I-layer thickness is small compared with the diffusion legnths for holes and electrons in the I-layer. This implies that the hole and electron concentrations may be assumed uniform throughout the I-layer. The current crossing the boundary between the P+ and I-layers will be entirely hole current and will be equal to the total hole charge Q_p in the I-layer divided by the hole lifetime τ_p.

$$I_o = \frac{Q_p}{\tau_p} = \frac{qpAW}{\tau_p} \tag{1.10}$$

where A and W are the area and thickness of the I-layer, respectively. Similarly, at the other I-layer boundary, I_o will be entirely electron current:

$$I_o = \frac{Q_n}{\tau_n} = \frac{qnAW}{\tau_n} \tag{1.11}$$

where τ_n is the electron lifetime in the I-layer. It is also reasonable to assume that there will be no unneutralized charge in the I-layer. Therefore, p=n; and as a further consequence, $\tau_p = \tau_n$. The uniformity of carrier concentrations means that the resistivity ρ_I of the layer will also be uni-

form.

$$\rho_I = \frac{1}{(q\mu_p p + q\mu_n n)} = \frac{1}{2q\mu n} \qquad (1.12)$$

assuming the mobility of both carrier types are equal to the ambipolar mobility, $\mu = 2\mu_p\mu_n/(\mu_p+\mu_n)$.

The resistance of the I-layer then will be,

$$R_I = \frac{\rho_I W}{A} \qquad (1.13)$$

Combining Eqs. (1.11), (1.12) and (1.13), we obtain as the final result,

$$R_I = \frac{W^2}{2\mu} \cdot \frac{1}{I_o \tau} \qquad (1.14)$$

This expression is applied frequently. We note from it that R_I is theoretically independent of I region area, being proportional to the square of I region width and varying inversely with mobility, lifetime, and bias current. However, care must be taken in the application of Eq. (1.14) to practical solutions. In particular, the following generalizations should be qualified:

1. Holding all process steps the same except for varying A produces a selection of diodes with different capacitances but the same R_I for a given bias current. This situation is true only if τ

remains constant; but generally, τ decreases with a decrease in A, since I region carriers are then nearer to the periphery where recombination can occur more rapidly.

2. R_I decreases as $(1/I_o)$. Again, this statement holds true only so long as τ remains constant. However, as I_o increases, the carrier density increases, and the recombination probability increases, decreasing τ. Furthermore, a saturation is reached when p and n increase sufficiently that substantial injection (holes into the N+ region and electrons into the P+ region) become significant, in violation of the above assumption used to derive Eq. (1.14).

Despite these limitations Eq. (1.14) is very useful and is typically invoked to estimate I region resistance at microwave frequencies.

1.8. EFFECTS OF DIODE MATERIALS AND DESIGN ON CHARACTERISTICS

In this section we shall consider the design trade-offs and compromises which must be made in achieving a set of characteristics for a practical PIN diode. The design variables are the thicknesses of the layers, the diode area, the resistivity or dopping concentrations of the layers, and the minority-carrier lifetime of the I-layer. In using the diode

as a switch, for example, the characteristics we want to control are the series resistance R_s and capacitance C under reverse bias, the forward bias series resistance R_f and the switching speed.

Table 1.2 shows in which direction it is desirable to shift the design variables in order to achieve the characteristics needed for a good switch. Notice that one wants to have as high an I-layer resistivity as possible and as low resistivities as possible for the P+ and N+ layers. Also, the P+ and N+ layers should be as thin as possible. Achieving these objects is entirely as the matter of the technological limits. On the other hand, there are conflicting requirements on the diode area, the I-layer thickness, and the minority carrier lifetime. For the two of these, one must compromise between achieving low series and low capacitance. For the lifetime, one must compromise between low forward resistance and rapid switching. The lifetime is, at best, usually rather difficult to control, so that lifetime is a design variable in a limited sense only.

Design Variable	Low R_s	Low C	Low R_f	Fast Switching
Area	Large	Small	Large	Small
I-layer thickness	Thin	Thick	Thin	Thin
P+ and N+ layer thickness	Thin	...	Thin	Thin
Lifetime	...	...	Long	Short
I-layer Resistivity	High	High		
P+ and N+ layer resistivity	Low	...	Low	Low

TABLE 1.2. Design variables to achieve the characteristics needed for a good switch.

CHAPTER 2

BASIC CONCEPTS

2.1. INTRODUCTION

The switch is the simple device that serves as the basic building block for these other control devices. A diode variable attenuator is a switch that goes continuously and smoothly from its low loss, "on" state to its high loss, "off" state. A limiter is a switch that is normally "on" at low level incedent power and turns itself "off" at high level incedent power by rectifying its own "off" biasing current. In other words, a limiter is a self-activating switch having the proper switching polarity and activated by high-level incident power. Thus a conceptual derivation that begins with the diode switch will provide a good foundation for understanding the other devices.

A light switch is closed to ideal. A knife switch is even closer to ideal. When the knife switch is closed, the high pressure over the large contact area provides a very low resistance, for all practical purposes zero ohms. When the knife switch is open, the resistance is extremely high, practically infinite. The switch is usually placed in series between a voltage source and light bulb so that when it is open

no current flows, etc. The house current or battery normally used provides a constant voltage, i.e., the source has a very low output impedance, much lower than the resistance of the load (light bulb).

A switch in a transmission, line is different from a light switch in that the voltage source is replaced by a generator having an output impedance equal to that of the load. In order to operate efficiently the source and load impedances are equal to the transmission line impedance. Microwave transmission lines are usually coacial, stripline, or waveguide, all of which may be represented by the parallel line Letcher model. Note that in a transmission line the alternative scheme of having the switch in shunt with the load becomes a possibility. In Figure 2.1, the first $Z_o(Y_o)$ is the generator output impedance and the second $Z_o(Y_o)$, designated by L, is the matched load terminating the transmission line.

A useful concept in transmission lines is traveling waves. A well matched transmission line has only a forward traveling wave, going from generator to matched load. This is called incident power and denoted by P_i. When the wave hits a discontinuity some power is absorbed in the discontinuity, denoted by P_a, some is reflected by the discontinuity, denoted by P_r, and some is transmitted past it, denoted by P_t.

When discussing diode switching it is necessary to define certain terms. RF power incident on an ideal attenua-

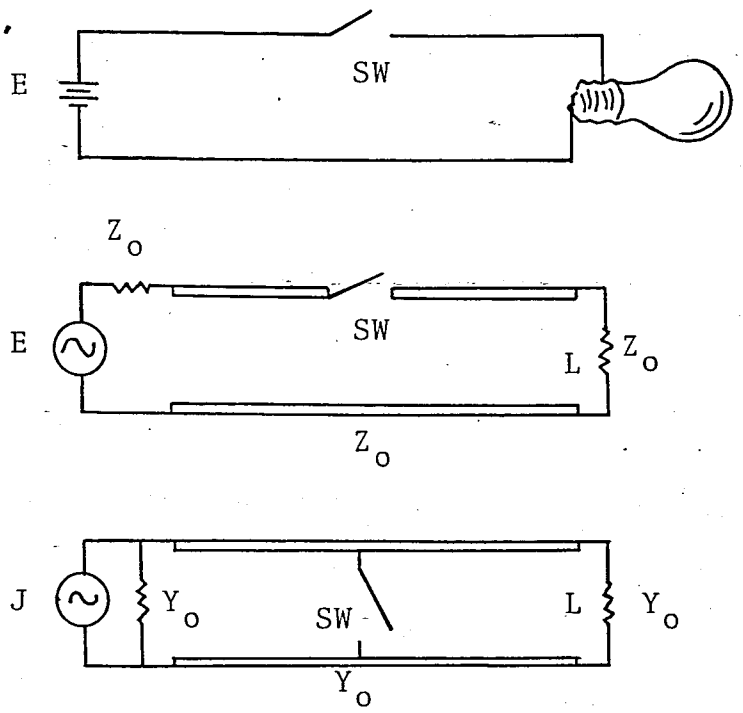


FIGURE 2.1. Basic switch operation.

ting device is either absorbed in or transmitted past the device, with no power reflected. The attenuation α of the device is defined as the ratio in decibels of the incident power to the transmitted power. If the attenuation of the device can be changed from some low value to some high value the device is called a switch. The insertion loss δ is defined as the minimum attenuation, and the isolation η is defined as the maximum attenuation.

When a diode is inserted in series or in shunt in a transmission line, EF power incident on the diode is reflected by, absorbed in, or transmitted past the diode. A diode is different from an attenuating device in that most of the incident RF power not transmitted is reflected rather than

absorbed. In fact, in an ideal diode switch, the incident power is either completely reflected or completely transmitted.

2.2. IN-LINE SWITCHES

To obtain attenuation by use of a single diode element in a TEM wave transmission line, the diode is mounted either in series with the center conductor or in shunt across the center and outer conductors. The RF power transmitted past the diode is, in all cases, the power delivered to the matched load. For the purpose of deriving the attenuation resulting from diode impedance and admittance, the diode is visualized as a two-terminal device whose RF impedance can be varied by changing the applied voltage. The equivalent circuits are shown in Figure 2.2. If the diode is considered to be of zero thickness and in bilaterally matched transmission line, then the equivalent circuits are valid for most applications.

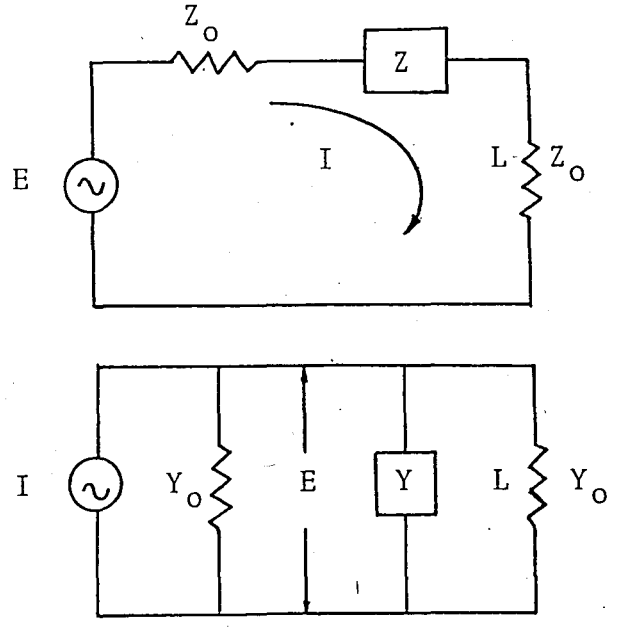


FIGURE 2.2. The equivalent circuits of a diode impedance Z in series and admittance Y in shunt in a transmission line.

In the equivalent circuit of a series-connected diode (Fig. 2.2), V is the peak amplitude of the sinusoidal voltage source which is assumed to have an output impedance Z_o; Z represents the diode, and L(=Z_o) is the matched load behind it. I is the peak amplitude of the resulting sinusoidal current. The power P_L in L is given by

$$P_L = \frac{1}{2} I I^* Z_o \tag{2.1}$$

Using the series circuit first,

$$I = \frac{V}{2Z_o + Z} \tag{2.2}$$

If Z = R + jX then

$$P_L = \frac{1}{2} \frac{V^2 Z_o}{(R+2Z_o)^2 + X^2} \tag{2.3}$$

in which P_L is the power absorbed by L. The attenuation, α of a diode inserted in a transmission line is defined as the ratio in decibels of power incident to the diode, P_i, to power transmitted past the diode P_t(P_t=P_L).

$$\alpha = 10 \log \frac{P_i}{P_t} \tag{2.4}$$

The power P_i incident on the diode is the power in the forward traveling wave going toward L. This is attained in the series equivalent circuit by setting Z equal to zero. So

$$P_i = P_L \qquad \text{for } Z = 0 \tag{2.5}$$

using Eq. (2.3)

$$P_i = \frac{V^2}{8Z_o} \tag{2.6}$$

Normally the diode impedance will not be zero ohms, but some finite value, and will cause the power transmitted past it to be some reduced value $P_t=P_L$ for $Z=Z$.

Using Eqs (2.3, 2.4 and 2.6) and the resulting attenuation is

$$\alpha = 10 \log \frac{P_i}{P_t} = 10 \log \frac{(\frac{R}{Z_o} + 1)^2 + (\frac{X}{Z_o})^2}{4} \tag{2.7}$$

For a diode in shunt having an admittance Y=G+jB, the derivation of attenuation is the same as above with the substitution of Y for Z, I for V, etc. Thus,

$$P_L = \frac{1}{2} V V^* Y_o \tag{2.8}$$

and

$$\alpha = 10 \log \frac{(\frac{G}{Y_o} + 1)^2 + (\frac{B}{Y_o})^2}{4} \tag{2.9}$$

The same equations may be derived using matrices (Appendix C). Given a matrix of the form

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{2.10}$$

a series impedance in a transmission line is represented by

$$\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \tag{2.11a}$$

a shunt admittance, by

$$\begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \tag{2.11b}$$

and the equation for attenuation in a transmisstion line is

$$\alpha = 10 \log \frac{1}{4} \left[A + \frac{B}{Z_o} + Z_o C + D\right]^2 \tag{2.12}$$

substituing Eq. 2.11 into Eq. 2.12 gives

$$\alpha = 10 \log \frac{1}{4} \left|2 + \frac{Z}{Z_o}\right|^2 \tag{2.13}$$

which reduces to Eq. (2.7), etc.

Eq. (2.7 and 2.9) give circular arcs of equi-attenuation curves on a rectangular grid polt of normalized impedance or admittance.

Circle centers are at -2 + jo and radii are $2 \times 10^{\alpha/20}$. The equi-attenuation curves are also circles on the Smith Chart as shown in Figure 2.3.

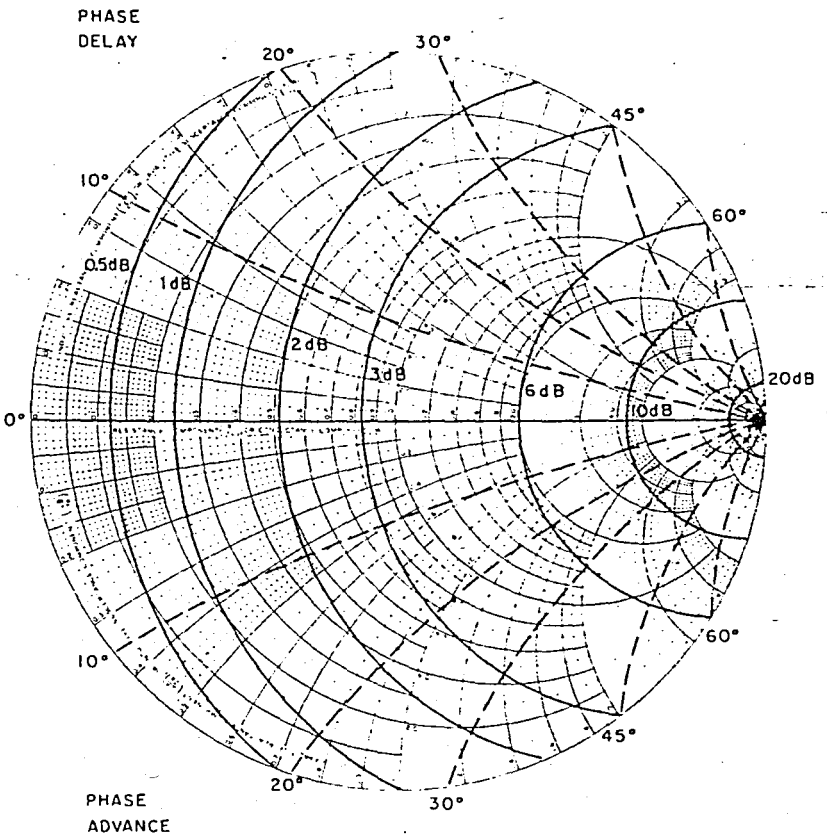


FIGURE 2.3. Transmission loss and phase from normalized diode impedance or admittance.

Plotting the impedance or admittance of a diode at the frequency of interest normalized to transmission line impedance on Figure 2.3 indicates directly the switching properties to be expected from the diode.

The phase shift of a network represented by an ABCD matrix (ref. Appendix C) is given by (4)

$$\phi = \tan^{-1}\left[\frac{I_m(A+B/Z_o + CZ_o + D)}{R_e(A+B/Z_o + CZ_o + D)}\right] \qquad (2.14)$$

Substituting Eq (2.11) into Eq. (2.14) the phase shift from

an impedance in series in a transmission line given by

$$\phi = \tan^{-1} \frac{X/Z_o}{2 + R/Z_o} \qquad (2.15)$$

These are shown as equi-phase arcs on the Smith Chart of Fig. 2.3. The utility of these curves may be demonstrated by viewing the normalized impedance and admittance of a typical PIN diode.

Consider an HP 5082-3001 PIN junction diode measured at 1GHz and normalized to 50 ohm transmission line characteristic impedance superimposed on the attenuation Smith Chart as shown in Figure 2.4. Note that for this diode L_s = 3.7nH R_s = 2Ω $C_p + C_j$ = 0.2pF. As illustrated in Fig. 2.4 and 2.5 placing this diode in series in a 50 ohm transmission line would provide < 1/2 dB insertion loss (δ) and 18 dB isolation (η). Shunting a 50 ohm transmission line it would provide 0.12 dB insertion loss and 4 dB isolation.

Note that this diode functions are better in series than in shunt. The required impedance range of a diode giving 1 dB to 20 dB switching is calculated by using Eq. (2.13).

$$\alpha = 10 \log \left| 1 + \frac{Z}{2Z_o} \right|^2 \qquad (2.16)$$

which can be approximated by

$$\alpha \approx 20 \log \left(1 + \frac{|Z|}{2Z_o} \right) \qquad (2.17)$$

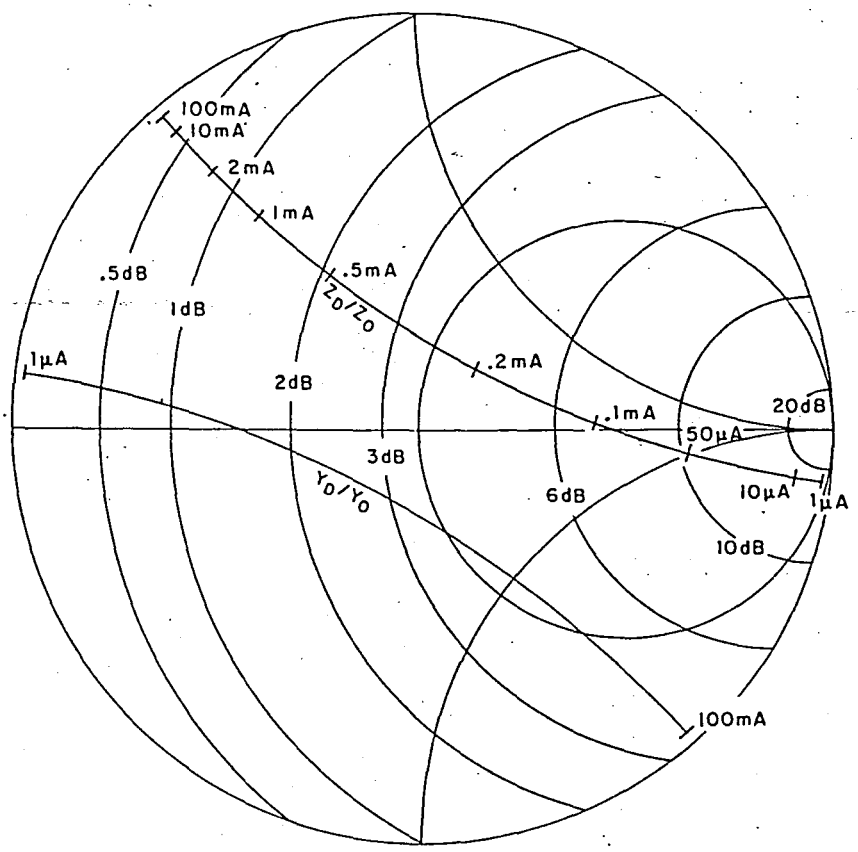


FIGURE 2.4. Attenuation of HP 3001 PIN diode at 1GHz in series (Z_o/Z_o) and shunt (Y_o/Y_o) in a Z_o = 50 ohms transmission line.

and provide

$$\frac{|Z|}{2Z_o} = 9 \text{ for } 20 \text{ dB}$$

or approximately,

$$\frac{|Z|}{2Z_o} = 20 \qquad (2.18)$$

Similarly for a shunt diode

$$\frac{|Y|}{Y_o} \approx 20 \approx \left(\frac{|Z|}{Z_o}\right)^{-i} \tag{2.19}$$

$$\frac{|Z|}{Z_o} = 0.05 \tag{2.20}$$

For the low loss state (1 dB)

$$\frac{|Z|}{2Z_o} = .13$$

$$\frac{|Z|}{Z_o} \approx .25 \text{ for series} \tag{2.21}$$

and

$$\frac{|Z|}{Z_o} \approx 4 \text{ for shunt} \tag{2.22}$$

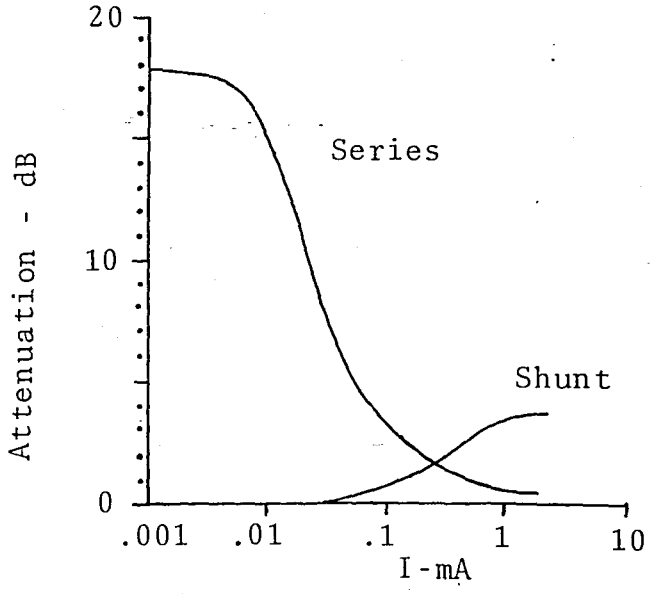


FIGURE 2.5. Attenuation as a function of current of PIN Diode switch of Figure 2.4.

Therefore if the diode normalized impedance varies between .25 and 20 the series configuration is favored and if it varies between .05 and 4 the shunt configuration is favored. Figure 2.6 illustrates this point.

Using Eqs. (2.8) and (2.9)

$$\alpha = 20 \log \left(\frac{R}{2Z_o} + 1\right) \quad \text{for } \frac{R}{Z_o} \text{ curves} \tag{2.23}$$

and

$$\alpha = 10 \log \left[1 + \left(\frac{X}{2Z_o}\right)^2\right] \text{ for } \frac{X}{Z_o} \text{ curves, etc.} \tag{2.24}$$

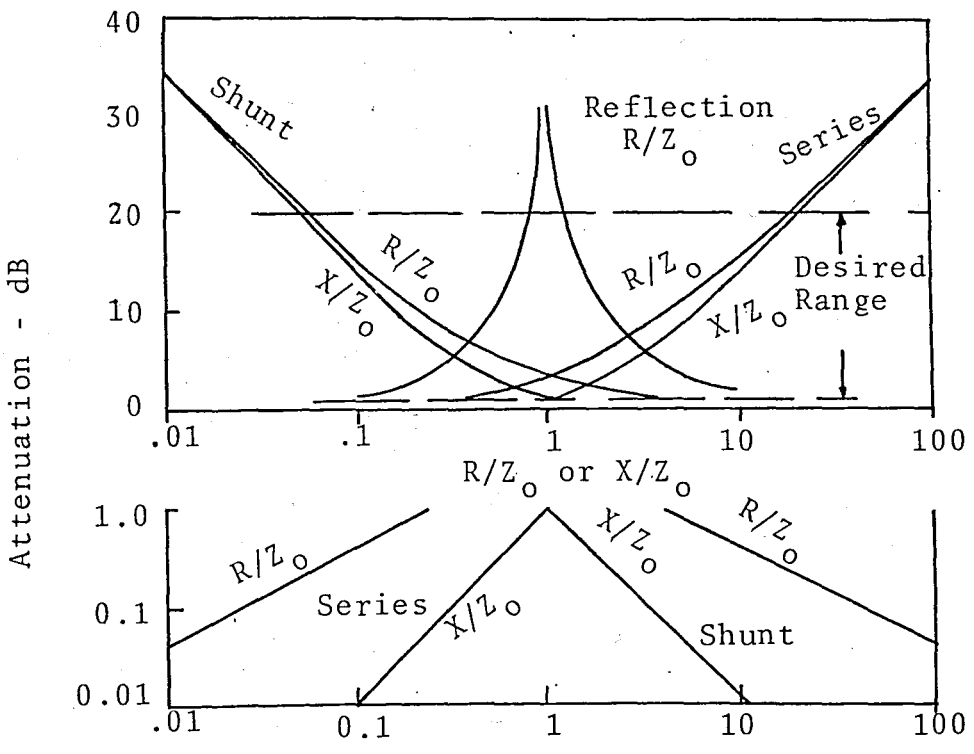


FIGURE 2.6. Attenuation as a function of normalized diode impedance or admittance. Insertion loss is shown expanded on a log scale.

2.3. DIODE MODES

Due to reactive elements in the diode equivalent circuit shown in Figure 2.7 the diode impedance goes through various resonances as frequency is changed. These resonances when controlled can provide useful switching at higher frequencies (5).

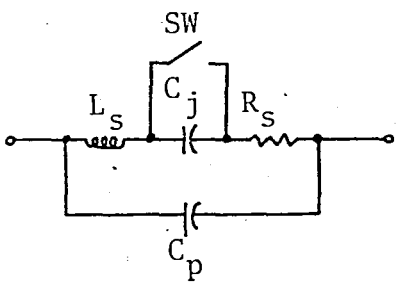


FIGURE 2.7. Diode equivalent circuit.

2.3.1. SERIES DIODE

As a function of frequency, the computed attenuation of a series diode in a 50 ohm transmission line is shown in Figure 2.8. The equivalent circuit parameters are C_p=0.2pf, L_s=5nH, C_j=0.2pf, and R_s = 5 ohms. It is assumed that these parameters do not change drastically with frequency. From Fig. 2.8 it is seen that high isolation is available at three frequencies, which are labeled Mode 1, 2 and 3. Mode 1 is the baseband mode; Mode 2 is the resonant diode mode; and

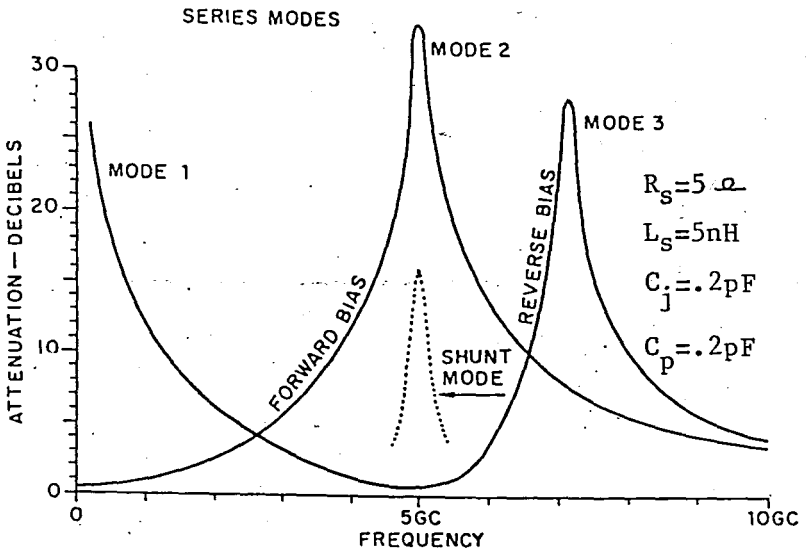


FIGURE 2.8. Attenuation of series diode switching modes.

Mode 3, the higher order diode resonance mode. Referring to Figure 2.9, the high isolation of Mode 1 is due to the high series reactance of the reverse bias diode capacitance at low frequencies which impedes the flow of current in the load L. The low insertion loss of Mode 1 is attributed to the low series impedance of R_s and L_s at low frequencies. As frequency is increased, the parallel resonance between L_s and C_p is encountered at forward bias which presents a high series impedance again impeding the flow of current to L and providing the isolation peak labeled Mode 2. Mode 3 is caused by the reverse bias parallel resonance C_p and L_s in combination with C_j.

1. Mode 1: Expanded curves for Mode 1 are shown in Figure 2.10. Here it is assumed for the C_p+C_j curves that the diode is at reverse bias and $R_s = L_s = 0$. For the L_s curves

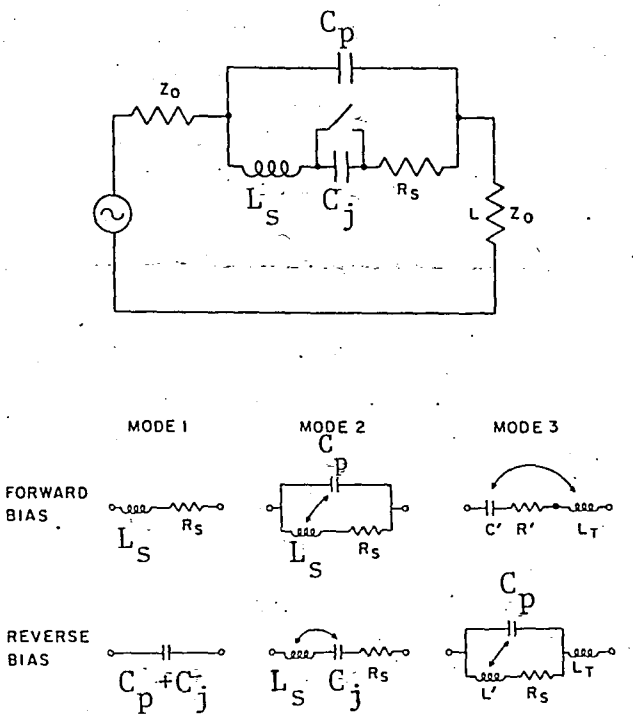


FIGURE 2.9. Diode element producing the switching modes.

it is assumed that the diode is at forward bias and C_p=0 and R_s=5 ohms. One sees that the combination of C_p+C_j = 0.2pF and L_s = 5nH allows for 10 dB or greater switching up to 2 GC. It is also seen how with a given C_p+C_j the isolation increases with decreasing frequency.

With Mode 1 operation, the insertion loss becomes undesirably large at higher frequencies due to L_s; at 2GC, 5nH already results in 2 dB insertion loss. For the "C_p+C_j" curves it is assumed that the diode is at reverse bias and that $R_s = L_s = 0$. For the "L_s" curves it is assumed that C_p=0 and R_s = 5 ohms. These same curves describe the bandwidth of the isolation and insertion loss of the diode operating in the

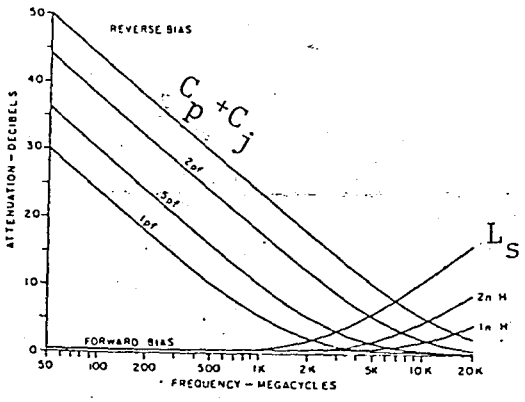


FIGURE 2.10. Detailed presentation of Mode 1 operation.

other series modes.

2. Mode 2: Mode 2 will normally exist for most diodes, but the maximum isolation and minimum insertion loss may not occur at the same frequency. By picking $C_p = C_j$, these resonances are made to occur at the same frequency so that Mode 2 has a low insertion loss.

3. Mode 3: As frequency is increased further on the reverse biased diode the series L_s-C_j combination becomes inductive and soon parallel resonates with C_p giving the high isolation peak labeled Mode 3. The forward biased diode is capacitive above Mode 2 which by itself does not present a low insertion loss for Mode 3, but, with the addition of a series inductance L_T, could be made to provide low insertion loss, see Fig. 2.9. L_T may be realized by including a short section of high impedance transmission line adjacent to the

diode.

Note that the high isolation and low insertion loss occur at the same frequency in Fig. 2.8 for Mode 2 because C_p and C_j are equal. At the forward bias L_s parallel resonates with C_p and at reverse bias it series resonates with C_j, therefore when $C_p=C_j$ these occur at the same frequency. Note also that the center frequency of Mode 3 is $\sqrt{2}$ times the frequency of Mode 2.

In Fig. 2.9 the terms C', R' and L' are simply derived and are given by

$$C' = \frac{(1-\omega^2 L_s C_p^2)^2 + (\omega R_s C_p)^2}{\omega^2 [C_p (R_s^2 + \omega^2 L_s^2) - L_s]} \tag{2.25}$$

$$R' = \frac{R_s}{(1-\omega^2 L_s C_p)^2 + (\omega R_s C_p)^2} \tag{2.26}$$

$$L' = L_s - \frac{1}{\omega^2 C_j} \tag{2.27}$$

To find the frequency of Mode 3 set

$$\omega_3 L' = \frac{1}{\omega_3 C_p} \tag{2.28}$$

in which ω_3 is the angular frequency of Mode 3. Recalling $C_p=C_j$, defining $\omega_2 = (C_p L_s)^{-\frac{1}{2}}$, and using Eq. (2.27) with $\omega=\omega_3$ the expression can be obtained

$$\omega_3 = \sqrt{2}\,\omega_2 \qquad (2.29)$$

2.3.2. SHUNT DIODE

Figure 2.11 shows the computed attenuation of a shunt diode in a 50 ohm transmission line as a function of frequency. The diode equivalent circuit parameters are the same as those for the series diode of Fig. 2.8. At forward bias, high isolation occurs only at low frequencies. At reverse bias, high isolation occurs only at the frequency corresponding to the series resonance between L_s and C_j.

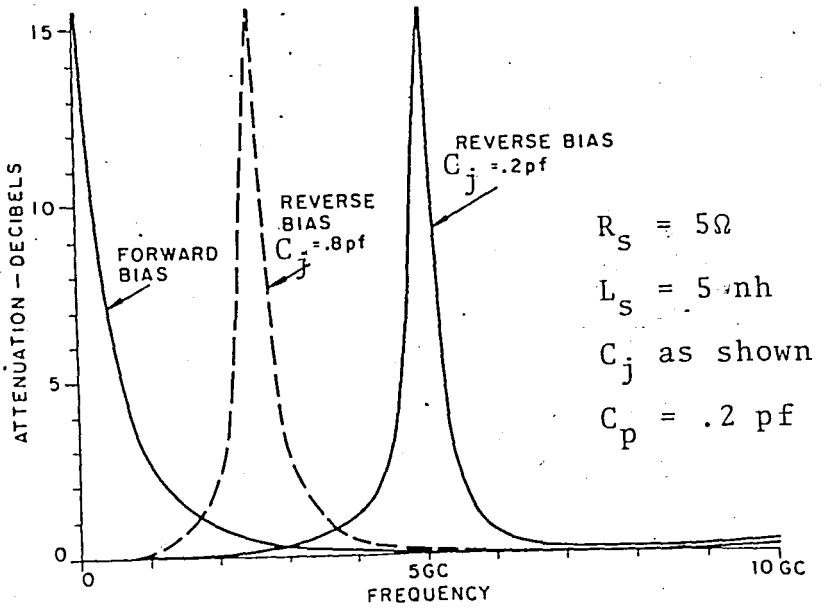


FIGURE 2.11. Attenuation of shunt diodes modes.

A very efficient switch can be made using a varactor as a shunt diode. If it is assumed that the varactor capacitance C_j can increase to 0.8 pF before conduction starts, then the resonant shunt mode will appear as shown by a dashed curve in Figure 2.11.

2.3.3. BANDWIDTH

1. Isolation

The isolation of a series diode switch results from the high reactive impedance of the diode. In a 50 ohm transmission line, when $R/Z_o << 1$ and $X/Z_o \geq 6$, the isolation given by Eq. (2.7) reduces to

$$\eta \approx 20 \log \frac{|X|}{100} \qquad (2.30)$$

with an error of less than 5 per cent. This relation is valid for isolation greater than 10 dB and frequencies slightly away from any resonances. Thus, for a specified isolation, the required series reactance is

$$|X| = 100 \times 10^{\eta/20} \qquad (2.31)$$

if X is due to a parallel combination of L and C, the susceptance of the pair is

$$\frac{1}{X} = 2\pi f C - \frac{1}{2\pi f L} \qquad (2.32)$$

solving for f:

$$f = \frac{1}{4\pi CX} + \frac{1}{2\pi}\sqrt{\frac{1}{4C^2X^2} + \frac{1}{LC}} \qquad (2.33)$$

Given a value of X, the isolation will increase as the parallel resonant frequency is approached and then decrease to the same isolation as -X is approached. The bandwidth is the difference between the frequencies that correspond to X and -X. Over the bandwidth, the isolation is maximum at parallel resonance and minimum at the extremes which correspond to X and -X. Substituting -X for X in Eq. (2.33) and then subtracting from the same, the bandwidth is obtained:

$$\Delta f = f(X) - f(-X) = \frac{1}{2\pi C|X|} = \left[200\pi C \times 10^{\eta/20}\right]^{-1} \qquad (2.34)$$

Note that L does not appear in the equation and that the isolation bandwidth is a function of specified isolation and C (and Z_o) only.

For Mode 1, L assumed to be infinite. The isolation results from a capacitor alone in series in the transmission line. Thus Fig. 2.10 shows not only an extended plot of Mode 1 operation, but also shows the plot of isolation bandwidth, Eq. (2.34).

The resonance causing Mode 2 isolation is between C_p and L_s (Fig. 2.9). In this case C_p rather than C_p+C_j determines the bandwidth. If $C_p=C_j$, Mode 2 bandwidth is twice that of Mode 1 (Fig. 2.8).

Mode 3 is the results of a series-parallel antiresonance of C_p, L_s and C_j, which occurs at $\sqrt{2}$ times the center frequency of Mode 2 when $C_p=C_j$, and has the same bandwidth as Mode 1.

The bandwidth of a diode switch shunting the transmission line is similar in derivation to that of the series diode. The isolation results from the low impedance of a series resonance between an L and a C. Isolations above 10 dB in a 50 ohm transmission line are given approximately by

$$\eta = 20 \log \left(\frac{25}{|X|}\right) \tag{2.35}$$

where X is the shunting reactance.

Solving for $|X|$

$$|X| = 25 \times 10^{-\eta/20}$$

The reactance of the shunting series LC is

$$X = 2\pi fL - \frac{1}{2\pi fC} \tag{2.37}$$

solving for f,

$$f = \frac{X}{4\pi L} + \frac{1}{2\pi}\sqrt{\frac{X^2}{4L^2} + \frac{1}{LC}} \tag{2.38}$$

substituting -X for X as before, and subtracting:

$$\Delta f = f(X) - f(-X) = \frac{|X|}{2\pi L} = \frac{25}{2\pi L} \times 10^{-\eta/20} \qquad (2.39)$$

It is seen here that the bandwidth is dependent only on L and η (and Z_o).

2. Insertion Loss

The insertion loss of a series diode switch results either from the low impedance of R_s and L_s for Mode 1, or a series resonance between C_j and L_s for Mode 2.

$$Z = R_s + j(2\pi f L_s - \frac{1}{2\pi f C_j}) = R_s + jX \qquad (2.40)$$

From Section 2.2, the insertion loss in a 50 ohm transmission line is given by the relation

$$\delta = 10 \log \left[(1 + \frac{R_s}{100})^2 + (\frac{X}{100})^2\right] \qquad (2.41).$$

solving for X:

$$|X| = 100 \left[10^{\delta/10} - (1 + \frac{R_s}{100})^2\right]^{\frac{1}{2}} \qquad (2.42)$$

Solving for the bandwidth as before:

$$\Delta f = \frac{|X|}{2\pi L_s} = \frac{50}{\pi L_s} \left[10^{\delta/10} - (1 + \frac{R_s}{100})^2\right]^{\frac{1}{2}} \qquad (2.43)$$

The insertion loss bandwidth is not a function of C_j and is also plotted in Fig. 2.10.

The insertion loss of a shunting diode in the frequency range of interest (Fig. 2.11) is less than some maximum value δ from zero to a maximum frequency fmax at reverse bias; at forward bias it is below δ for frequencies above a minimum frequency fmin. The insertion loss of a shunting diode comes from low susceptance and negligible conductance. From Eq. (2.9):

$$\delta = 10 \log \left[1 + \left(\frac{B}{2Y_o}\right)^2\right] \qquad (2.44)$$

$\log(1+X) = 0.435X$ for $X \leq 0.1$. So.

$$\delta \approx 4.35 \left(\frac{B}{2Y_o}\right) \qquad (2.45)$$

Solving for B in a 50 ohm transmission line:

$$B = \frac{\sqrt{\delta}}{52} \qquad (2.46)$$

At reverse bias:

$$B = 2\pi fC \,, \quad \text{and} \quad fmax = \frac{\sqrt{\delta}}{327C} \qquad (2.47)$$

The insertion loss is less than δ up to fmax. At forward bias:

$$B = \frac{1}{2\pi fL_s} \qquad (2.48)$$

and

$$fmin = \frac{1}{2\pi BL_s} = \frac{8.28}{\sqrt{\delta}\ L_s} \qquad (2.49)$$

The insertion loss is less than δ above fmin.

2.4. REFLECTION SWITCHES

The possible circuits for making switches discussed thus far have included mounting the diode in series or shunting the transmission line and operating in Mode 1 or Mode 2. Mode 3 has never been used practically. Another basic method of making switches is to use the absorbing properties of the diode at intermediate bias. For example, a diode biased to 50 ohms and terminating a 50 ohm transmission line would absorb all power incident upon it. When this diode is connected to a circulator of when two of them are connected to a 90^{o} 3 dB coupler as shown in Figure 2.12 the combination becomes an absorption diode switch. Power entering Port 1 of the circulator is directed to Port 2 by circulator action. When the impedance connected to Port 2 is a perfect match then no power is reflected to re-enter Port 2 and emerge from Port 3. The result is high isolation from Port 1 to Port 3. When the termination on Port 2 has a high VSWR, as an impedance does which is near the outside edge of the Smith Chart, then most power emerging from Port 2 of the circulator is reflected by the impedance on Port 2 only to re-enter the circulator at Port 2 and be directed to Port 3 having a low insertion loss from Ports 1 to 3. That power which is reflected from the termination on Port 2 emerges from Port 3. It can be seen from Fig. 2.4 that a bias of 0.2 mA on the HP 3001 PIN diode will produce a high attenuation when the diode is connected

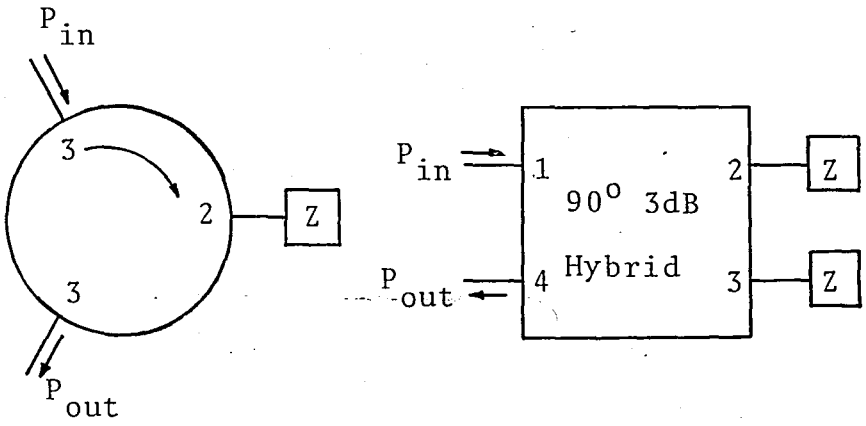


FIGURE 2.12. Absorption diode switches.

to Port 2 of a circulator and a low insertion loss at 0 mA or 100 mA bias. The VSWR (S) at 0.2 mA is 1.2. This produces a voltage reflection coefficient given by

$$|\Gamma| = \frac{S-1}{S+1} = \frac{.2}{2.2} = .0909 \tag{2.50}$$

The power reflection coefficient is given by

$$\frac{P_i}{P_t} = |\Gamma|^2 = 0.008263 \tag{2.51}$$

The attenuation is given by

$$\alpha = 10 \log \frac{P_i}{P_t} = 10 \log \frac{P_i}{P_r} = 10 \log \frac{1}{|\Gamma|^2}$$

$$= 20.8 \text{ dB} \tag{2.52}$$

In general when Z or Y terminate a transmission line having characteristic impedance Z_o or admittance Y_o the voltage re-

flection coefficient is given by (6)

$$\Gamma = \frac{Z_T - Z_o}{Z_T + Z_o} = \frac{Y_o - Y_T}{Y_o + Y_T} \tag{2.53}$$

$$\Gamma = \frac{(R - Z_o) + jX}{(R + Z_o) + jX} \tag{2.54}$$

$$\alpha = 10 \log \frac{1}{|\Gamma|^2} = 10 \log \left[\frac{(R+Z_o)^2 + X^2}{(R-Z_o)^2 + X^2} \right] \tag{2.55}$$

when $R \approx Z_o$ and $X \approx 0$ very high attenuation is possible. Assuming X_T is very small, Fig. 2.6 shows how R/Z_o contributes to attenuation for a reflection type diode switch. Note that when a PIN diode is used to absorb the power then all of the incident power is absorbed by the diode. The maximum average power a PIN diode can absorb is usually in the 1 watt to 10 watt range, thus incident power levels must be below this limit. Power handling capability may be increased by putting a power absorbing resistance in series or shunt with the switching diode.

Also shown in Figure 2.12 is a 90^o 3-dB hybrid with two identical impedances connected to it. These couplers have the property that power into Port 1 is split equally between Ports 2 and 3 with none emerging from Port 4. When perfect identical reflectors are attached to Ports 2 and 3, the power reflected by them recombines in the coupler in such a manner that their phases add at Port 4 and cancel at Port 1. Thus power perfected by the impedances emerges from Port 4 just as it emerged from Port 3 of the circulator. This form of

matched switches has advantages in that,

(1) it is reciprocal (the circulator gives no variable attenuation for the wave traveling Port 3 to Port 1),

(2) these hybrid junctions can be made over extreme bandwidth (10 to 1),

(3) they are less expensive and smaller volume and weight than circulator,

(4) the power is divided between two diodes, increasing power capability by a factor two. Their disadvantage is that they require twice as many diodes as the circulator type.

2.5. POWER LIMITATIONS

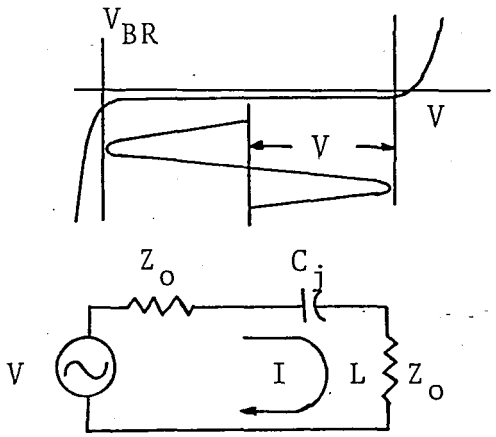
Different factors limit the incident peak power $\hat{P}_i$ and incident average power $\overline{P}_i$ that a diode can control. The $\hat{P}_i$ is determined by the diode breakdown voltage V_{BR}, the characteristic impedance of the transmission line in which it is mounted Z_o, and circuit used for switching (whether the diode is series mounted or shunt mounted for the most practical circuits). The average power is determined by the forward biased series resistance R_S, the average power the diode can dissipate $\overline{P}_o$, the Z_o and the circuit, when the diode is required to control c.w. power ($\hat{P}_i = \overline{P}_i$), then the maximum limit P_{cw} is not determined by Z_o and the circuit but only by V_{BR}, R_S, and $\overline{P}_o$. (The circuit and Z_o for P_{cw} are determined

by V_{BR}, R_S, and $\overline{P}_o$.)

2.5.1. PEAK POWER

To maintain isolation with a series diode it is important that no conduction current flow during the RF cycle. The RF voltage thus must be positioned between 0 volts and the breakdown voltage V_{BR} as shown in Figure 2.13. When the diode is providing high isolation all of the generator voltage across the high impedance of C_j, which is the reverse biased diode. When a diode is biased to $V_{BR}/2$, as shown in Fig. 2.13, the magnitude of the generator voltage may be as large as $V_{BR}/2$.

MAXIMUM PEAK POWER



MAXIMUM AVERAGE POWER

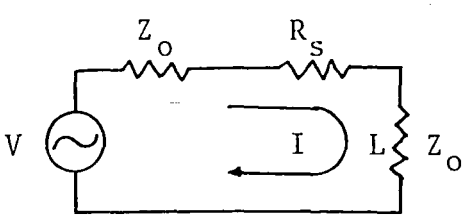


FIGURE 2.13. Voltage-current characteristic of a diode and series equivalent circuits for determining maximum peak and average power the diode can switch.

Using Eq. (2.6) the incident power is given by

$$P_i = \frac{V^2}{8Z_o} \tag{2.56}$$

which gives a maximum incident peak power P_i for a series diode of

$$\hat{P}_i = \frac{V_{BR}^2}{32\ Z_o} \tag{2.57}$$

since the highest V_{BR} available (in HP 3001 PIN diode) is about 200 volts, such a diode can isolate a peak incident power of 25 watts in a 50 ohm transmission line, provided the power dissipated in the diode under these conditions is within the dissipation rating of the diode.

A shunt diode in the low loss state will have half of the generator voltage dropped across it; thus the maximum incident power $\hat{P}_i'$ for a shunt diode is given by

$$\hat{P}_i' = 4\hat{P}_i = \frac{V_{BR}^2}{8Z_o} \tag{2.58}$$

A 200 volt shunt diode in 50 ohm transmission line can switch 100 watts of incident peak power in this configuration.

2.5.2. AVERAGE POWER

The current shown in Fig. 2.13b is given by

$$I = V/(R_S + 2Z_o) \tag{2.59}$$

The power dissipated in the diode $\overline{P}_o$ is given by

$$\overline{P}_o = \frac{1}{2} I^2 R_S = \frac{V^2 R_S}{2(R_S + 2Z_o)^2} \tag{2.60}$$

solving for V^2

$$V^2 = 2(R_S + 2Z_o)^2 \overline{P}_o/R_S \tag{2.61}$$

Recalling from Eq. (2.6) the incident power is given by

$$P_i = \frac{V^2}{8Z_o} \tag{2.62}$$

Combining Eqs. (2.61) and (2.62) gives the average incident power $\overline{P}_i$ the series diode can control:

$$\overline{P}_i = \frac{\overline{P}_o Z_o}{R_S} \left(1 + \frac{R_S}{2Z_o}\right)^2 \approx \overline{P}_o \frac{Z_o}{R_S} \tag{2.63}$$

The dissipating rating of available switching diodes range from 0.08-0.25 watts. For example, assuming that $\overline{P}_o = 0.1$ watt, $Z_o = 50$ ohms, and $R_S = 2$ ohms, results in $\overline{P}_i = 2.6$ watts.

Substituting G_s for R_S and Y_o for Z_o gives the average incident power $\overline{P}_i'$ a shunt diode can control:

$$\overline{P}_i' = \frac{\overline{P}_o Y_o}{G_s}\left(1 + \frac{G_s}{2Y_o}\right)^2 = \frac{\overline{P}_o Z_o}{4R_S}\left(1 + \frac{2R_S}{Z_o}\right)^2 \approx \overline{P}_o \frac{Z_o}{4R_S} \qquad (2.64)$$

In a 50-ohm transmission line, a 2-ohm, HP 3001 PIN diode can switch average power of about 0.7 watts in this configuration.

2.5.3. C.W. POWER

To determine the highest CW power that a diode can switch, the transmission line impedance is varied so that the peak power rating of the diode and average power rating of the diode are equal. Assuming for the shunt diode that

$$\hat{P}_i' = \frac{V_{BR}}{8Z_o} \quad \text{and} \quad \overline{P}_i' = \overline{P}_o \frac{Z_o}{4R_S}$$

for the series diode that

$$\hat{P}_i = \frac{V_{BR}^2}{32Z_o} \quad \text{and} \quad \overline{P}_i = \overline{P}_o \frac{Z_o}{R_S}$$

and that the optimum characteristic impedance is used in each case, then both the diode configurations can switch the same amount of CW power

$$\overline{P}_{cw} = V_{BR}\sqrt{\frac{\overline{P}_d}{32R_S}} \qquad (2.65)$$

A 2 ohm, 200 watt, HP 3001 PIN diode can switch 7.9 watts CW power in a 180-ohm transmission line.

CHAPTER 3

PROPERTIES OF MICROSTRIP TRANSMISSION LINES

3.1. INTRODUCTION

Transmission lines and passive lumped or distributed elements, which are manufactured and assembled from metal conductor or conducting stripes on insulating substrates, are essential basic elements in microwave and millimeter wave hybrid integrated circuits. The metal strips or microstrips are deposited by thin-film or thick-film technology on dielectric substrates; the processing steps are substantially different compared to conventional coaxial and waveguide circuit technology. Circuits built with microstrip transmission lines or microstrip components have three important advantages:

i. The complete conductor pattern can be deposited and processed on a single dielectric substrate which is supported by a single metal ground plane. Such a circuit can be fabricated at a substantially lower cost than waveguide or coaxial circuit configurations.

ii. Beam-leaded active and passive devices can be bonded directly to metal strips on the dielectric

substrate.

iii. Devices and components incorporated into hybrid integrated circuits are accessible for probing and circuit measurements (with some limitations imposed by external shielding requirements).

3.2. DEFINITION AND CLASSIFICATION

A strip line or microstrip line is a parallel two-conductor line made of at least one flat strip of small thickness. For mechanical stability the strip is deposited on a dielectric substrate which is usually supported by a metal ground plane. This basic configuration is shown in Figure 3.1a.

A parallel two-conductor line of this type may need modifications because:

i. A radio frequency shield may be required to eliminate radiation losses. The shield dimensions or the sheet conductivity of the shielding have to be chosen in such a way that excitation of traverse electric modes, traverse magnetic modes, and box resonance is suppressed.

ii. Proximity of the air-dielectric interface with the strip conductor can be lead to excitation of plane-trapped surface waves. This problem can be solved by using a substrate with a low dielec-

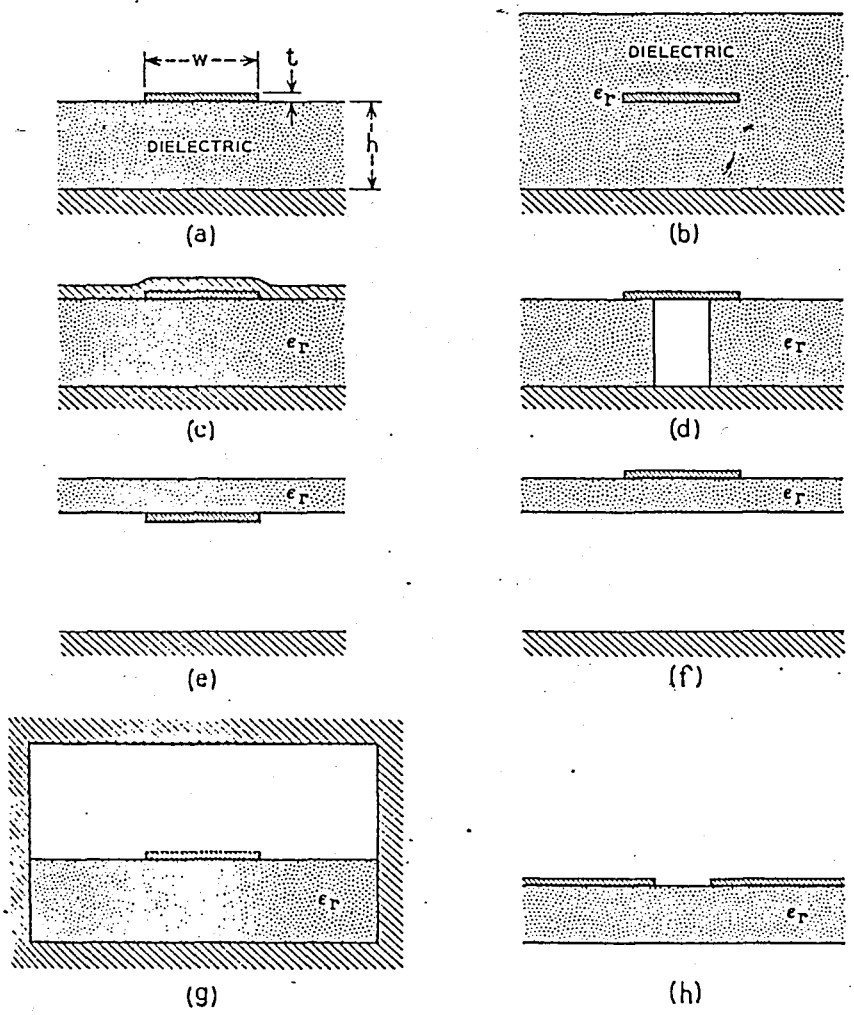


FIGURE 3.1. Basic types of microstrip transmission lines with one strip conductor supported by a dielectric substrate: (a) standard microstrip, (b) embedded microstrip, (c) microstrip with overlay, (d) microstrip with hole, (e) standard inverted microstrip, (f) suspended microstrip, (g) shielded microstrip, (h) slot transmission line.

tric constant or by choosing a sufficiently small frequency-thickness product for the microstrip. It can also be solved by removing the air-dielectric interface into the far field region as shown in Fig. 3.1b.

iii. If the substrate is a semiconductor, surface passivation may be necessary to protect against atmospheric contanminants. This can be achieved by a thin dielectric film as shown in Fig. 3.1c.

iv. Solid-state devices with substantial heat dissipation such as IMPATT, and GUNN diodes as well as high-power varactor diodes have to be shunt mounted in the microstrip in order to achieve a small thermal spreading resistance in the ground plane. A hole in the dielectric is required in Fig. 3.1d for mounting a solid state device between the two microstrip conductors.

IMPATT and high-power varactors are typical examples of solid-state devices which are usually shunt mounted in transmission line circuits. Other solid-state devices or materials which require shunt mounting are ferrites for circulators and isolators and high-Q dielectric resonantors for microwave band-pass filters. Shunt mounting is facilitated in inverted microstrips and suspended microstrips shown in Fig. 3.1e and 3.1f. Solid-state devices which require a dc bias or a dc return have to be mounted by means of a pressure contact or bonded contacts between the ground plane and the

strip conductor in Fig. 3.1e. Complete shielding of such a line is essential because fringe field effects are enhanced by increased electric field intensities in the dielectric support material. An attractive solution is to suspend the substrate symmetrically between the ground plane and the top shield. A major advantage of all microstrip configurations with an air gap is that the effective dielectric constants is small. This means that the effective dielectric loss tangent is substantially reduced, also, all circuit dimensions can be increased, which leads to less stringent mechanical tolerances; better circuit reproducibility, and therefore lower production cost.

Figure 3.1g shows a completely shielded standard micropstrip and Fig. 3.1h a schematic diagram of a slot line which consists of two conductors deposited on the same side of a high permittivity substrate. The slot line can be tightly coupled to the lines of Fig. 3.1a through g by depositing the slot line metalization on one side of the substrate and the microstrip conductor on the opposite side of the same substrate.

3.3. IMPEDANCE, ATTENUATION AND UNLOADED Q

The electrical parameters of the microstrips of Fig. 3.1a through g which are required for circuit design are impedance, attenuation, unloaded Q, wavelength, and propagation constant. These parameters are interrelated for all micro-

strips of Fig. 3.1a through g assuming that:

i. the propagating mode is a traverse electromagnetic mode, or it can be approximated by a traverse electromagnetic mode;

ii. conductor losses in the metal strips are predominant, which means dielectric losses can be neglected;

iii. the relative magnetic permeability of the substrate material is $\mu_r = 1$.

The basic reason for the subsequently explained relationship of the line parameters is that of the inductance per unit length depends only upon the conductor geometry and is absolutely independent of the geometry and the dielectric properties of the supporting structure. The relationship between line parameters is shown in Fig. 3.2.

Let us assume in Fig. 3.2a that the conductor geometry is defined by a stripe width w_o, a ground plane spacing h_o, and a small stripe thickness t_o. Let us also assume that this is an air line with characteristic impedance Z_{o1}, a wavelength λ_o, an attenuation per unit length α_o, and an unloaded Q_o. If the conductor dimensions remain, the same, and if the micrstrip is fully embedded in the dielectric medium with dielectric constant ε_r, one obtains the new line parameters given in Fig. 3.2b. If the line is only partially filled with dielectric support material with a relative dielectric constant ε_r, one obtains for the line parameters of

Fig. 3.2c.

$$Z = \frac{Z_{o1}}{\sqrt{\varepsilon_{eff}}} \qquad \text{impedance} \qquad (3.1)$$

$$\lambda = \frac{\lambda_o}{\sqrt{\varepsilon_{eff}}} \qquad \text{wavelength} \qquad (3.2)$$

$$\alpha = \alpha_o \sqrt{\varepsilon_{eff}} \qquad \text{attenuation} \qquad (3.3)$$

$$Q = Q_o = \frac{20\pi}{\ell n 10} \frac{1}{\alpha_o \lambda_o} \qquad \alpha_o\lambda_o \text{ in dB} \qquad (3.4)$$

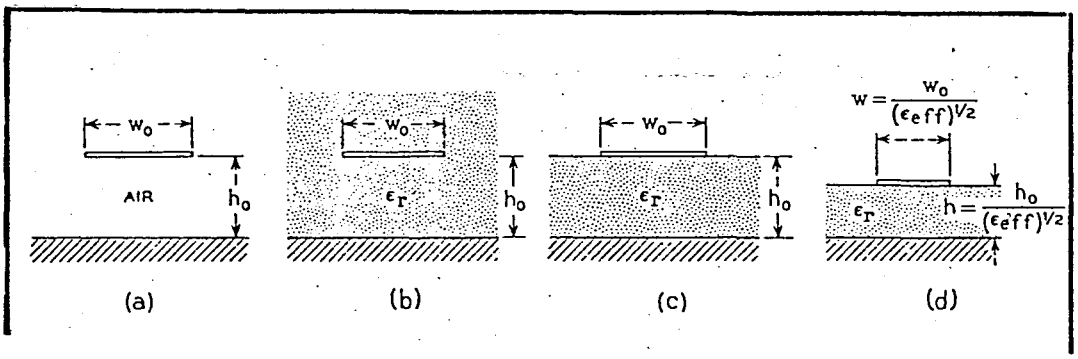
The effective dielectric constant ε_{eff} has to be computed or measured as discussed in Section 3.3. The following inequalities are valid for the standard microstrip in Fig. 3.1a and the inverted microstrip in Fig. 3.1e are given by

$$\frac{1+\varepsilon_r}{2} \leq \varepsilon_{eff} \leq \varepsilon_r \qquad \text{standard microstrip} \qquad (3.5)$$

$$1 \leq \varepsilon_{eff} \leq \frac{1+\varepsilon_r}{2} \qquad \text{inverted microstrip} \qquad (3.6)$$

If one has to compare the attenuation or the quality factor Q of different microstrips one has to consider lines which have the same impedance level. Fig. 3.2d gives the line parameters for partial dielectric filling with reduced dimensions $w_1 = w_o/\sqrt{\varepsilon_{eff}}$ and $h_1 = h_o/\sqrt{\varepsilon_{eff}}$. This insures that the electrical dimension of the two basic line parame-

ters is the same as the electrical dimension of the air of Fig. 3.2a.



Z_o Impedance	$\frac{Z_{o1}}{\sqrt{\epsilon_r}}$	$\frac{Z_{o1}}{\sqrt{\epsilon_{eff}}}$	$\frac{Z_{o1}}{\sqrt{\epsilon_{eff}}}$
λ_o Wavelength	$\lambda = \frac{\lambda_o}{\sqrt{\epsilon_r}}$	$\lambda = \frac{\lambda_o}{\sqrt{\epsilon_{eff}}}$	$\lambda = \frac{\lambda_o}{\sqrt{\epsilon_{eff}}}$
α_o Attenuation	$\alpha = \alpha_o \sqrt{\epsilon_r}$	$\alpha = \alpha_o \sqrt{\epsilon_{eff}}$	$\alpha = \alpha_o \cdot \epsilon_{eff}$
$Q_o = \frac{20\pi}{\ell n 10} \frac{1}{\alpha_o \lambda_o}$	$Q = Q_o$	$Q = Q_o$	$Q = \frac{Q_o}{\sqrt{\epsilon_{eff}}}$

FIGURE 3.2. Impedance, wavelength, attenuation and quality factor Q of microstrip transmission lines.

3.4. COMPUTATION AND MEASUREMENT OF EFFECTIVE DIELECTRIC CONSTANT (7)

The electrical parameters of any microstrip can be computed if the characteristic impedance Z_{o1} of corresponding

air line and the dielectric constant $\sqrt{\varepsilon_{eff}}$ are known. The basic equations required for this computation are listed in Fig. 3.2.

The effective dielectric ε_{eff} is a function of the ratio w/h, the relative dielectric constant, and geometrical shape of the boundary between air and the dielectric support material. In order to find a function which approximates the set-up of Figure 3.3 over the total range $0 \leq w/h < \infty$ and $1 \leq \varepsilon_r < \infty$ we define a function $F(\varepsilon_r, w/h)$ by

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2} \; F(\varepsilon_r, \frac{w}{h}) \tag{3.7}$$

From Eq. (3.5) we find for the standard microstrip of Fig. 3.1a:

$$0 \leq F(\varepsilon_r, \frac{w}{h}) \leq 1 \tag{3.8}$$

One class of functions which fulfills this requirement is the class of irrational functions

$$F(\varepsilon_r, \frac{w}{h}) = \left[1 + \sum_{n=1}^{N} c_n \left(\frac{h}{w}\right)^n\right]^m \tag{3.9}$$

with c_n being functions of ε_r and $m \leq 0$. The set of curves of Fig. 3.3 can be approximated with m = -0.5 and one side term of the series by

$$F(\varepsilon_r, \frac{w}{h}) = \left(1 + \frac{10h}{w}\right)^{-\frac{1}{2}} \tag{3.10}$$

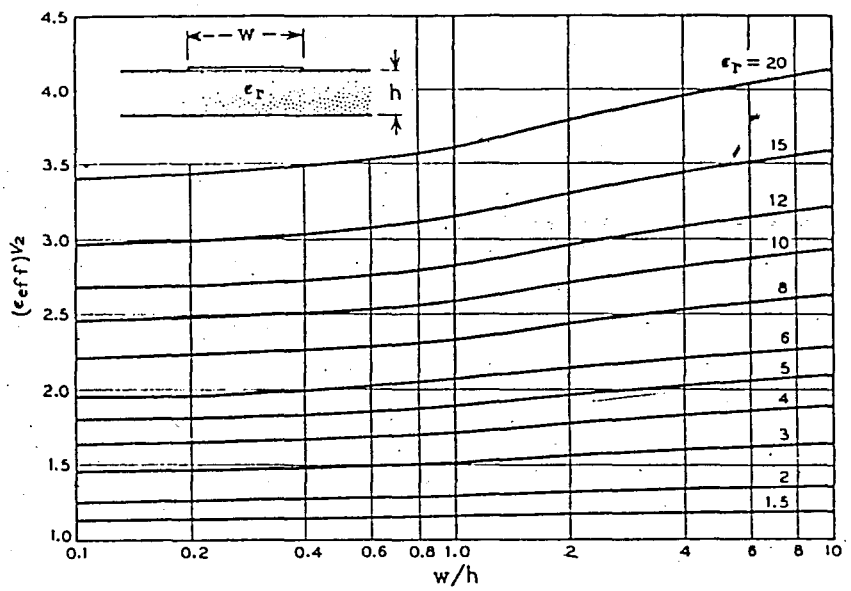


FIGURE 3.3. Square root of the effective dielectric constant for a standard microstrip. $(\varepsilon_{eff})^{\frac{1}{2}}$ plotted as a function of w/h with ε_r as parameter.

The final result with an accuracy of ± 2 per cent for ε_{eff} and an accuracy of ± 1 percent for $(\varepsilon_{eff})^{\frac{1}{2}}$ is

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left(1 + \frac{10h}{w}\right)^{-\frac{1}{2}} \qquad (3.11)$$

Effective dielectric constants can also be obtained by static capacitance measurement or time domain reflectometer measurements. If the static capacitance per unit length is C with partial dielectric filling and C_o with the dielectric removed, one obtains $\varepsilon_{eff} = C/C_o$ and from $Z = (L/C)^{\frac{1}{2}}$ with $L = \frac{Z_o}{C}$

$$Z = \frac{Z_{o1}}{\sqrt{\varepsilon_{eff}}} = \frac{1}{c\sqrt{c\ c_o}} \tag{3.12}$$

where c is the velocity of light in vacuum, $c = 3x10^{10}$ cm per second.

3.5. IMPEDANCE DESIGN FORMULAS

Wheeler showed that for the zero-thickness dielectric microstrip line (8)

$$Z_o = \frac{188.5}{\pi\sqrt{\frac{\varepsilon_r+1}{2}}}\left[\ell n\left(\frac{8}{w/h}\right) + \frac{1}{8}\left(\frac{w/h}{2}\right)^2 - \frac{1}{2}\left(\frac{\varepsilon_r-1}{\varepsilon_r+1}\right)\left(\ell n\ \frac{\pi}{2} + \frac{1}{\varepsilon_r}\ \ell n\ \frac{4}{\pi}\right)\right] \tag{3.13}$$

is valid for narrow strips $(w/h) < 1$, and

$$Z_o = \frac{188.5}{\sqrt{\varepsilon_r}}\left[\frac{w}{2h} + 0.441 + 0.082\left(\frac{\varepsilon_r-1}{\varepsilon_r^2}\right) + \frac{\varepsilon_r+1}{2\pi\varepsilon_r}\left[1.45 + \ell n\left(\frac{w}{2h} + 0.94\right)\right]\right]^{-1} \tag{3.14}$$

is valid for wide strips $w/h > 1$. These characteristic impedance equations are in good agreement with experiment for very thin strips $(t/h < 0.005)$ when the substrate dielectric constant ε_r is the range from 2 to 10 and $0.1 < \frac{w}{h} < 5$.

Figure 3.3 is a plot of the characteristic impedance of dielectric microstrip as a function of the w/h ratio for dielectric constants corresponding to several important substrate materials. Note that for the 50 ohm characteristic impedance which is popular in coaxial transmission line, (w/h) = 1 on an alumina substrate.

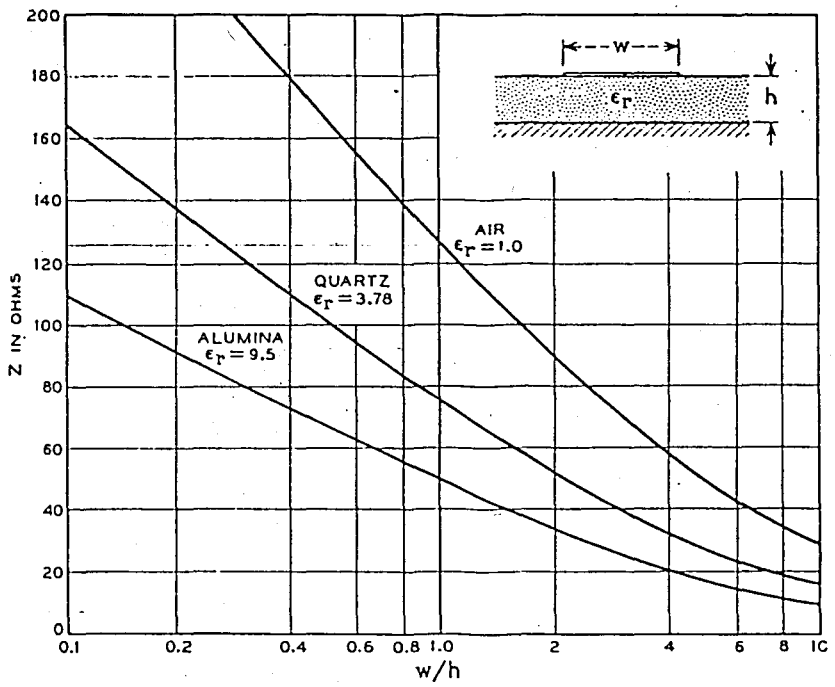


FIGURE 3.4. Characteristic impedance of a standard microstrip for ε_r = 1 and impedance of the standard microstrip for ε_r = 3.78 (quartz) and ε_r = 9.5 (alumina) as a function of w/h.

There exists a relationship between the effective filling fraction q_o and the effective dielectric constant defined as:

$$q_o = \frac{\varepsilon_{eff} - 1}{\varepsilon_r - 1} \tag{3.15}$$

with an aid of a computer, the set of curves presented in Fig. 3.4 was generated (9).

If the shape of w/h of the microstrip line is known, the free-space characteristic impedance Z_{o1} and the effective filling fraction q_o can be read directly from the curve denoted $\varepsilon_r = 1$. The characteristic impedance Z_o can be read directly from the curve corresponding to the associated dielectric constant ε_r of the substrate. The effective dielectric constant (ε_{eff}) can be computed by Eq. (3.15).

If the characteristic impedance Z_o is known, the shape ratio and the effective filling fraction can be read directly from the curve corresponding to the associated dielectric constant ε_r of the substrate. A wide variety of the dielectric substrates is available, with typical properties shown in Appendix A.

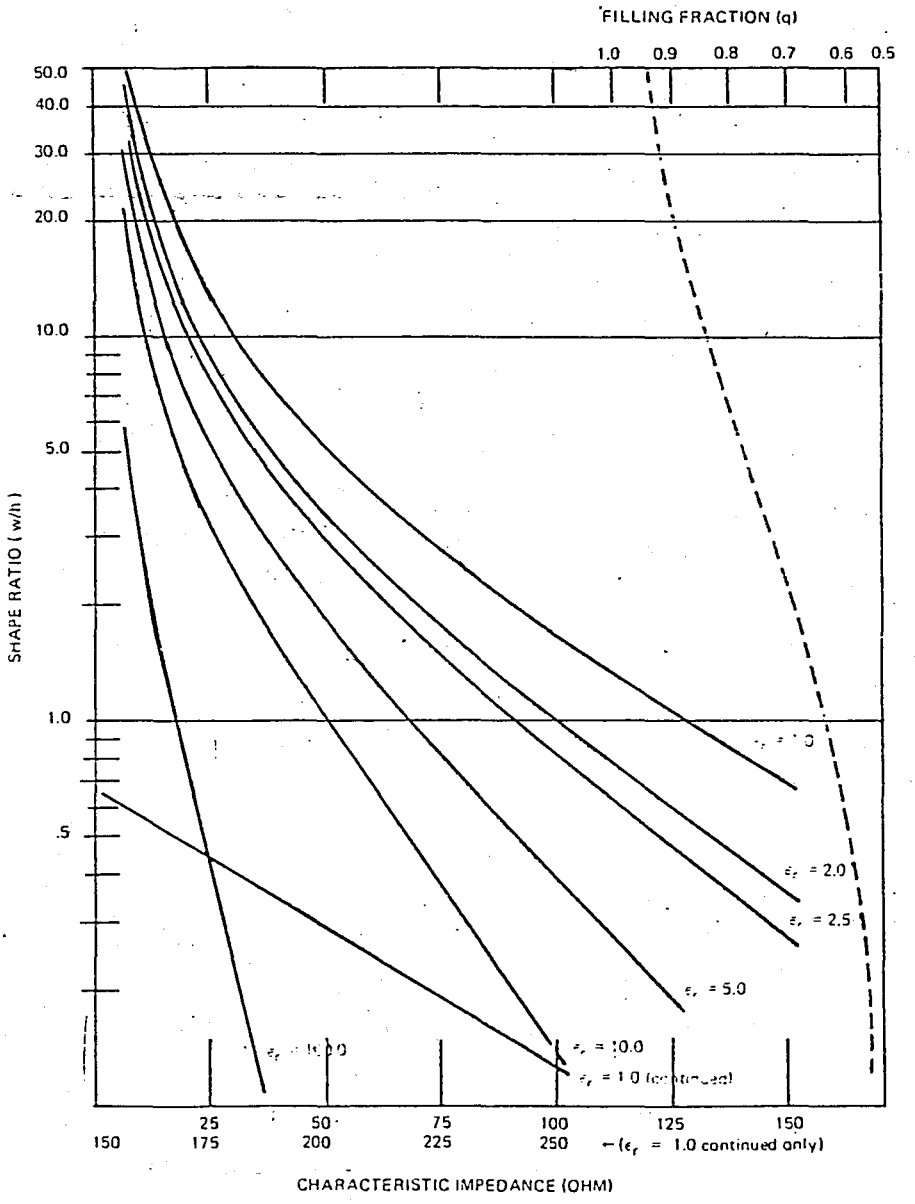


FIGURE 3.5. Microstrip transmission line design chart.

CHAPTER 4

DESIGN OF MICROWAVE SWITCHES USING MICROSTRIP LINES

4.1. INTRODUCTION

Many switching requirements can be met simply by using the concepts developed in Chapter 2. Packaged diodes work quite well in Mode 1, without any tuning up to about 4 GHz. Unpackaged diodes work well in miniaturized microstrip up to about 20 GHz.

There is a wide variety of ways of combining diodes with transmission lines to obtain good switching. Every diode switch must include a diode and the bias circuit. When both bias circuit and diode are considered together, it frequently becomes possible to use the elements of the bias circuit to optimize the diode insertion loss and/or isolation at the design frequency.

4.2. SWITCHES

The selected optimum configurations for mounting diodes in microstrip line to make switches are shown in Figure 4.1.

In most cases the bias circuit elements are chosen to work in conjunction with the diode reactances to provide optimum insertion loss or isolation at the design frequency. A typical requirement on a diode switch is to provide less than 1 dB insertion loss and more than 20 dB isolation. Wide strips indicate characteristic impedance $Z_o \leq 50$ ohms, while thin strips indicate $Z_o \geq 50$ ohms.

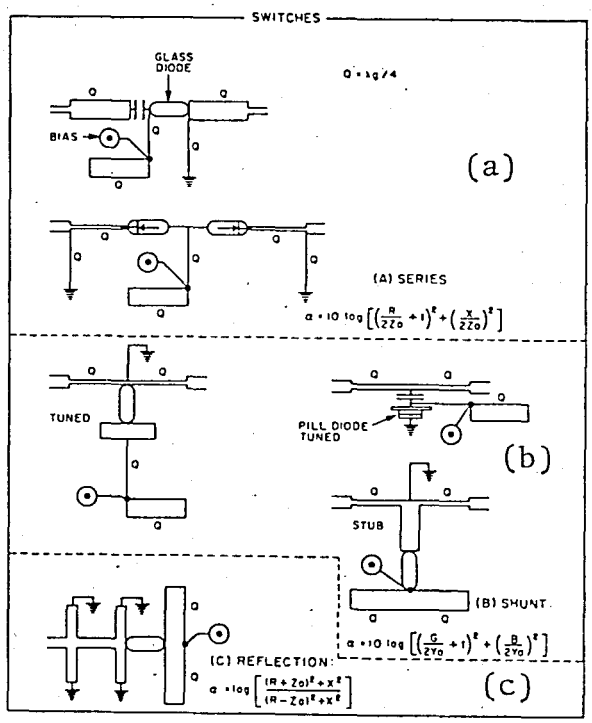


FIGURE 4.1. Circuits for microstrip line switches.

4.2.1. SERIES DIODE

When a series diode has a low impedance, most of the RF current passes through it into the terminating load behind it. It then provides a low insertion loss, δ. When it has a high impedance, practically no RF current passes through

it, and the device demonstrates high attenuation termed isolation, η. Since a capacitor must be put in series with the series diode to isolate the bias voltage from the other parts of the system, the same capacitor can be made to series resonate with the inductance of the forward-biased diode to provide a low impedance (and thus low insertion loss) at the design frequency. Putting an inductor in parallel with a diode to parallel resonate with the reverse bias capacitance to obtain high impedance (and thus high isolation) is practical only when the required inductance is small, so that it is comprised of a short length of high-impedance transmission line connecting the quarter-wavelength sections on both sides of the diode. Normally such an inductor will not be used, dictating that the series configureation be used only when the diode reverse bias impedance is high enough to provide the desired isolation by itself.

Since minimum insertion loss is easily obtained by tuning the series capacitance, the isolation is the only switching state difficult to satisfy. The isolation is dictated by the impedance of the diode at reverse bias, which must be high compared to Z_o. The Z_o in which the diode is mounted can be lowered by putting quarter-wavelength transformers before and after the diode. Allowing the transformer stripline characteristic impedance to be as low as 25 ohms permits the diode to be mounted in a region transformed to 12.5 ohms. This gives the series diode curbe on Figure 4.2 defining the impedance region of a diode measured in 50 ohm

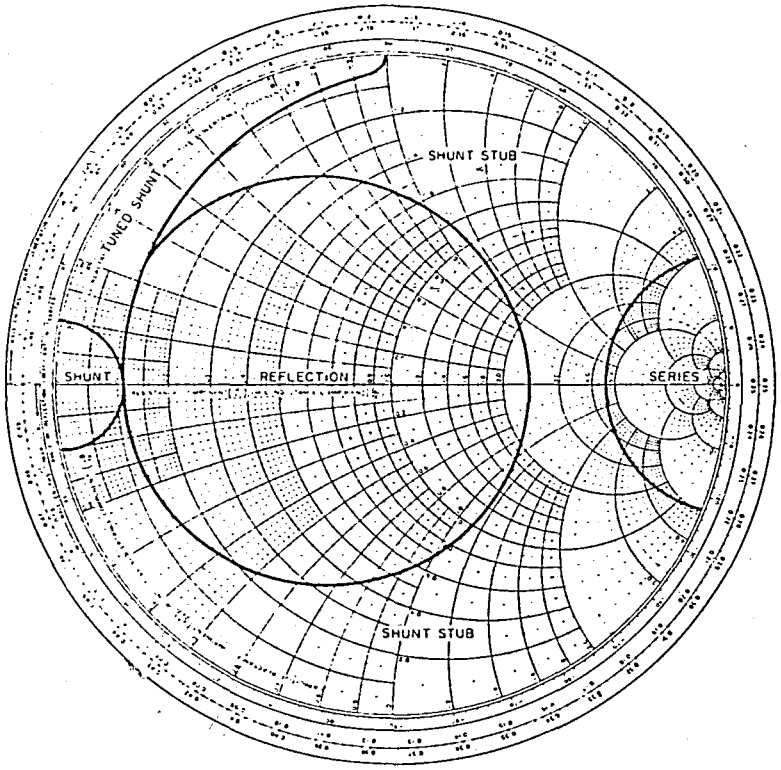


FIGURE 4.2. Normalized impedance plot for selecting the most suitable circuit.

transmission line that will provide at least 20-dB isolation.

Using Eq. (2.7) and assuming R = 0, Z_o = 12.5 ohms, the reactance X corresponding to an isolation of 20 dB is $\pm$250 ohms, or $\pm$5 normalized to a 50-ohm line.

The remainder of the circuit shown in the upper portion of Figure 4.1a is for biasing. The high Z_o quarter-wavelength line to ground provides a d-c ground return for bias with very little contribution to insertion loss over a wide bandwidth. The high Z_o quarter-wavelength line section from the bias point similarly provides wide bandwidth. The

open-circuit low-Z_o quarter-wavelength line from the bias point provies an RF ground at the point and prevents RF from being coupled to the external biasing circuit.

Another circuit is shown in Fig. 4.1a that uses two diodes and has the advantage that no series tunign capacitor is required. The reflections of two identical discontinuities cancel when their electrical separation ℓ/λ_g satisfies the equation

$$\frac{\ell}{\lambda_g} = \frac{1}{2\pi} \tan^{-1} \left(\frac{2}{X/Z_o}\right) \qquad (4.1)$$

where ℓ = the distance between diode centers.

A spacing of $\ell/\lambda_g = 0.2$ is approximately correct for tuning out the inductive reactance of most forward-bias diodes. This same spacing also increases the isolation. For example, if one diode in a given Z_o provides only 10 dB, then two of them properly spaced in series and in the same Z_o will provide 26 dB. Although this lower circuit of Fig. 4.1a could permit the region for series diode isolation on Fig. 4.2. to be expanded, it is not expanded making Fig. 4.2 a conservative guideline. In this circuit the transformers in series with the diodes may be needed to reduce the insertion loss contributed by a series resistance of the forward bias diodes by transforming the series resistance to lower effective values.

4.2.2. SHUNT DIODES

Lead-type or pill-packaged diodes may be used for making shunt diode switches as shown in Fig. 4.1b. A shunt diode must have low impedance to provide high isolation and high impedance for low insertion loss. The insertion loss of the lead-type shunt diode switch may be reduced by making the d-c ground return shorter than $\lambda_g/4$.

The isolation of the lead-type diode is maximized by adjusting the lengths of the shunt capacitive stubs on the bias end of the diode. Since the forward-bias impedance of the diode is usually inductive, these open-circuit stubs are made shorter than $\lambda_g/4$ to provide the series capacitance for resonance.

The maximum isolation of the pill diode is obtained by varying the capacitor between the diode and the center strip of the stripline. These two circuits perform well as diode switches when their impedance normalized to 50 ohms falls within the region labelled "shunt" and "tuned shunt" in Fig. 4.2.

A large portion of the outer edge of the Smith Chart lies outside the region so far defined in Fig. 4.2 by the circuits. This unclaimed region is easily within range of the shunt stub configuration.

When a diode at forward bias has inductance L and at reverse bias capacitance C, it has the same impedance as a shorted or opened length of transmission line of characteristic impedance

$$Z_o' = \sqrt{L/C} \tag{4.2}$$

and length

$$\ell' = \frac{\lambda_g}{2\pi} \tan^{-1} \omega\sqrt{LC} \tag{4.3}$$

By adding more length in front of the diode of characteristic impedance Z_o', the line can be made $\lambda_g/4$ long and perform as a switch having optimized isolation and insertion loss.

The requirement may be stated more generally in terms of diode reactance. For forward conduction, the diode reactance is X_s, and for reverse bias the reactance is X_o.

Then

$$Z_o' = \sqrt{-X_s X_o} \tag{4.4}$$

and

$$\ell' = (\lambda_g/2\pi)\tan^{-1} \sqrt{-X_s X_o} \tag{4.5}$$

Note that X_s and X_o must have opposite signs to provide real values. In the event Z_o' is too high or too low for practical construction, or if both the reactances have the same sign, the d-c ground return may be adjusted to a length other than

$\lambda_g/4$ to provide the desired tuning for optimum insertion loss, the stub having been adjusted for high isolation.

When the Z_o' for any diode is out of the range 12.5 to 100-ohm range, the impedance level of the diode is such that 10-percent bandwidth becomes very difficult to obtain in any switching circuit.

4.2.3. REFLECTION DIODE

When the impedance of the diode is close to 50 ohms in one bias state, none of the circuits discussed thus far will provide satisfactory switching. Good switching may be obtained by connecting the diode to the second port of a circulator. Then power in the first port is absorbed by the diode in the 50-ohm impedance state and does not come out of port 3. In the other bias state the diode is presumed to be a better reflector, incident power is reflected from it, emerging from port 3 with low insertion loss. The 50-ohm stubs shown in Fig. 4.1c are for improving the match of a diode that is not exactly 50 ohms.

Reflection switches may also be made using 90-deg 3-dB couplers. A reflection-type diode is put on each of the normal output arms of the 3-dB coupler. Then power reflected from them adds in phase at normally isolated arm of the 3-dB coupler.

4.3. SPECIAL MODEL FOR SHUNT DIODE STUBS

Normally the switching diode is represented by the equivalent circuit shown in Fig. 4.3a. The new model for the switching diode is a length of two-wire transmission line as shown in Fig. 4.3b. The characteristic impedance of the transmission line representing the switching diode can be defined to be equal to the square root of the product of the input impedances when the diode junction is conducting and when it is non-conducting (as in Eq. (4.4)). The effective length of the line is defined by the reactance at either bias state and is then the same for both bias states. Alternatively, the diode can be represented with equal accuracy by a line of any characteristic impedance when the effective lengths are properly chosen for conduction and non-conduction. In general, these lengths vary with frequency. It is more

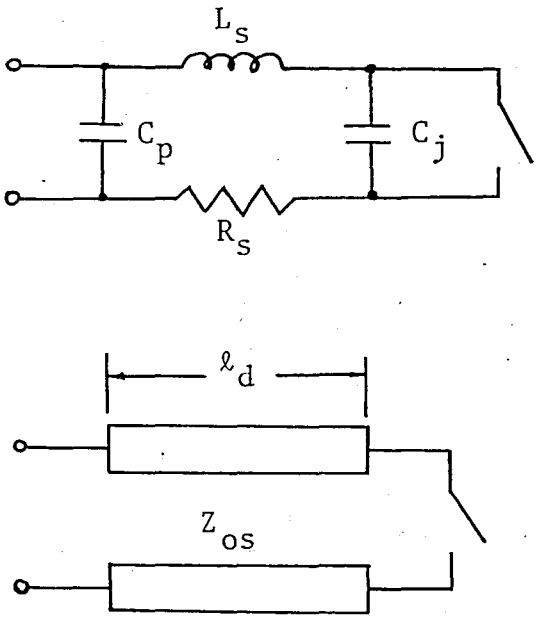


FIGURE 4.3. Equivalent circuits of switching diodes (a) old, (b) new.

convenient to fix the characteristic impedance and allow only the effective lengths to vary. This approach is taken here because it facilitates measurement and design. When the diode is forward biased, it is considered to be a length of short-circuit-terminated transmission line. When the diode is reverse biased, it is considered to be different lengths of open-circuit-terminated transmission line. The effective lengths of a diode are obviously a function of the assumed Z_o. The effective length of several HP 3001 PIN diodes (Z_{os}=50) is shown in Figure 4.4.

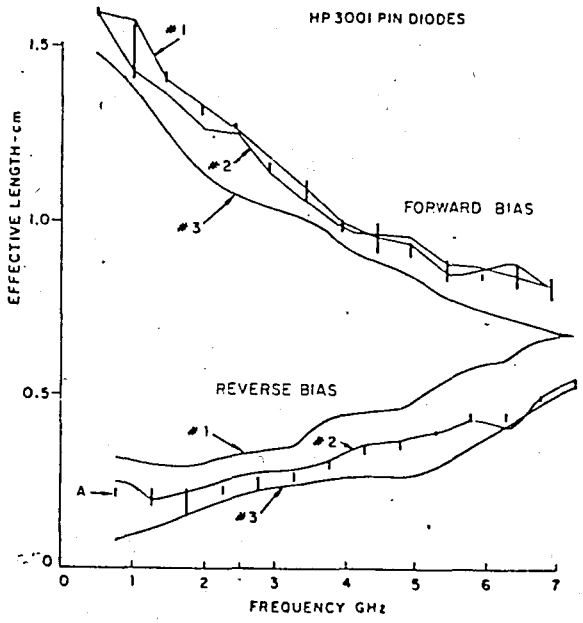


FIGURE 4.4. Effective length of several HP 3001 PIN diodes (Z_{os} = 50).

4.4. DESIGN OF STUB SWITCH (10)

The microstrip stub switch, using PIN diode such as HP 5082-3005 series for the switching element, is designed in the SPST configuration at the central frequency of 2.5 GHz, as shown in Figure 4.5.

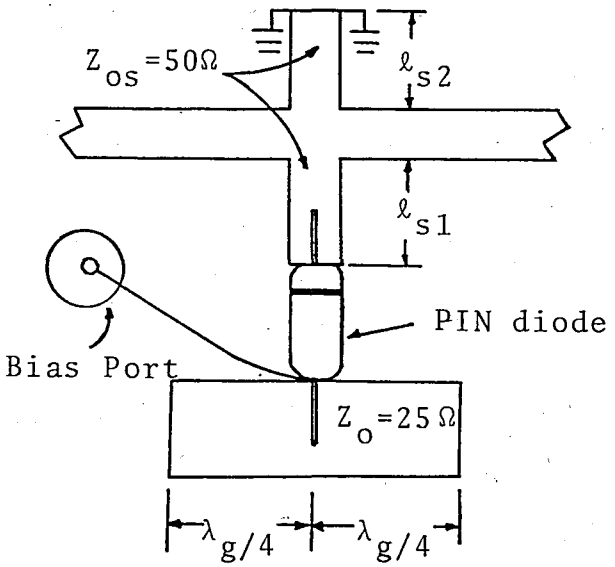


FIGURE 4.5. The stub switch.

We use DUROID 5870 for the microstrip transmission line. The dielectric constant of Duroid 5870 is 2.33 (see Appendix A). It has a thickness of 0.7379 mm. In order to find the diode stub length, we should calculate the propagation velocity.

$$v_o = \frac{C}{\sqrt{\epsilon_{eff}}} = 2.126 \times 10^{10} \text{ cm/sec} \qquad (4.6)$$

where $C = 2.998 \times 10^{10}$ cm/sec and ε_{eff} is calculated using Eq. (3.11) and Fig. 3.5 for 50Ω transmission line, then $\varepsilon_{eff} = 1.988$.

Hence, the transmission line wavelength is

$$\lambda_g = \frac{\nu_o}{f_c} = 8.504 \text{ cm} \qquad (4.7)$$

where $f_c = 2.5$ GHz.

When the diode is reversed-biased, the length of the stub between the main line and the diode is calculated so that it and the diode length add up to $\lambda_g/4$ at 2.5 GHz. Hence,

$$\ell_{s1} + \ell_{DR} = \lambda_g/4 \qquad (4.8)$$

where ℓ_{DR} is the effective length of the diode for reverse biase case.

Using Fig. 4.4. and $\ell_{DR} = 0.26$ cm, hence,

$$\ell_{s1} = \lambda_g/4 - \ell_{DR} = 1.866 \text{ cm}$$

An open circuit at the diode junction is thus transformed to a short circuit across the main transmission line, which results in high isolation.

When the diode is forward biased, the RF current goes to ground via the two parallel 25 ohm, $\lambda_g/4$ open-circuit stubs so that the diode stub appears as a short-circuit terminated stub slightly greater than $\lambda_g/4$ long as shown in Figure 4.6 and the length of the diode stub increases as ΔL.

$$\Delta \ell = \ell_{DF} - \ell_{DR} \tag{4.9}$$

where ℓ_{DF} is the effective length of the diode at forward bias.

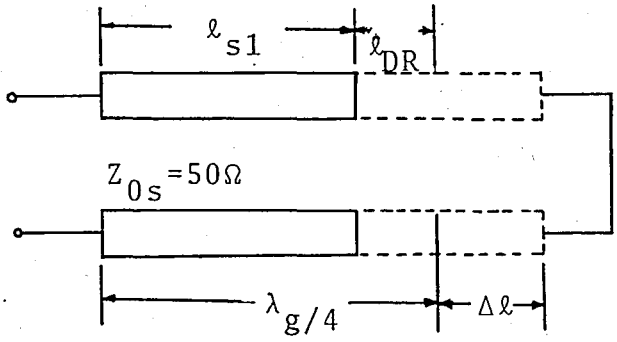


FIGURE 4.6. Influence of the effective length of the diode on the stub.

Using Fig. 4.4, and $\ell_{DF} = 1.244$ cm, hence,

$$\Delta L = 1.244 - 0.26 = 0.984 \text{ cm}$$

$$\lambda_g/4 + \Delta\ell = 3.11 = 0.3657\ \lambda_g$$

Thus it appears as a capacitor across the main transmission line. The reactance of the capacitance can be calculated using the transmission line (or Smith Chart).

$$Z_{s.c} = j\, Z_{os} \tan 2\pi \frac{\ell}{\lambda_g} \tag{4.10}$$

Using the Eq. (4.3), then

$$Z_{s.c} = -\, j56.2$$

$$\frac{1}{\omega C} = 56.2 \qquad \text{and} \qquad C = \frac{1}{\omega 56.2} \tag{4.11}$$

and C = 1.132 pf at the frequency of 2.5 GHz.

This capacitance is tuned out by the inductance of the upper stub, which is less than $\lambda_g/4$, and terminated in a short-circuit. Therefore, using the definition of the resonance,

$$\omega = \frac{1}{\sqrt{LC}} \tag{4.12}$$

and inductance,

$$L = \frac{56.2}{\omega} \tag{4.13}$$

L = 3.577 nH at the frequency of 2.5 GHz.

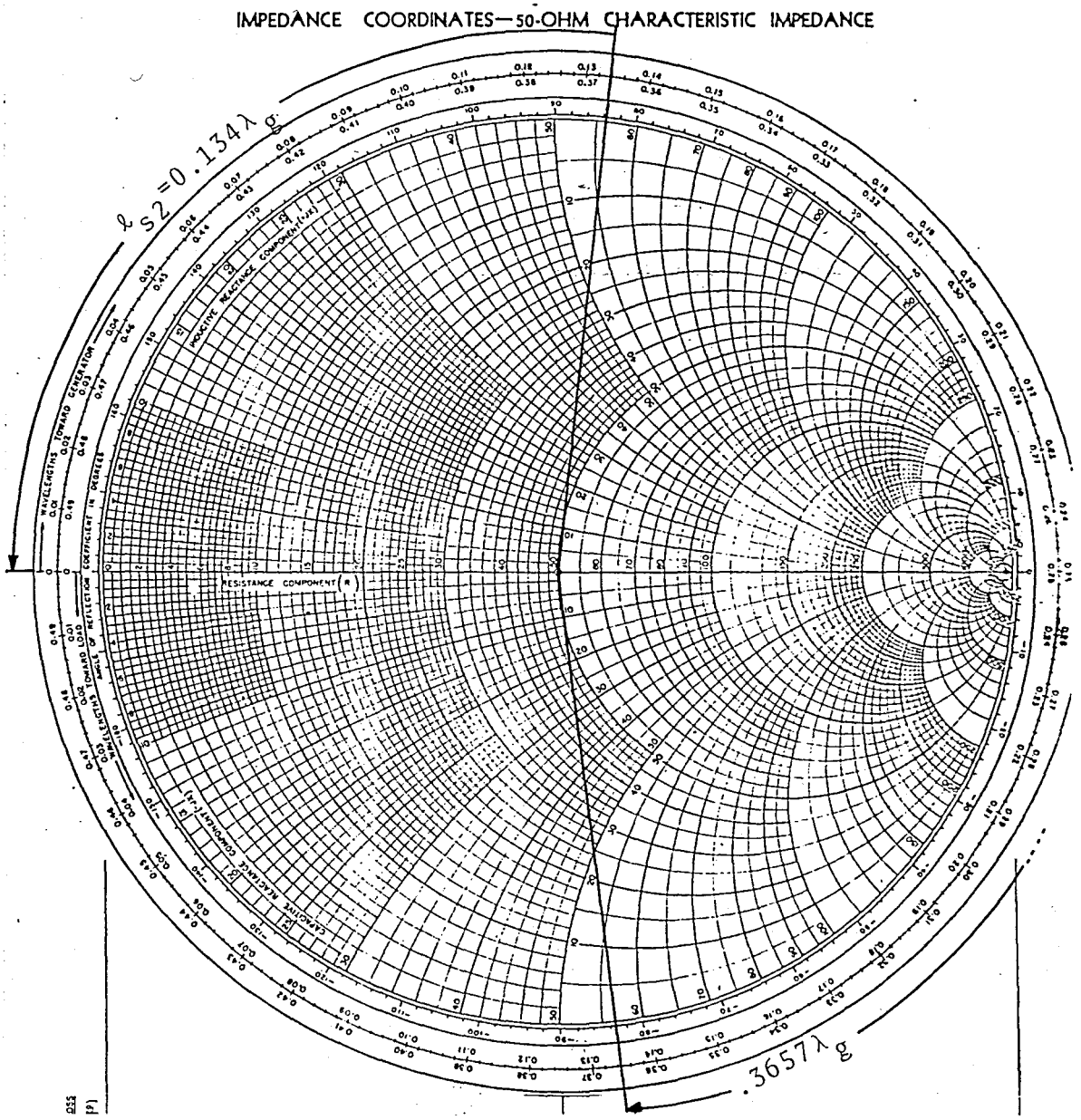


FIGURE 4.7. Calculation of the length of upper stub using the Smith Chart.

Now, the length of the upper stub can be calculated using Eq- (4.10)

$$\ell_{s2} = \frac{\lambda_g}{2\pi} \tan^{-1} \frac{56.2}{50}$$

$$\ell_{s2} = 0.134\ \lambda_g$$

$$\ell_{s2} = 1.142 \text{ cm}$$

The same results are obtained using the Smith Chart as shown in Figure 4.7. The upper stub provides dc return for the bias current.

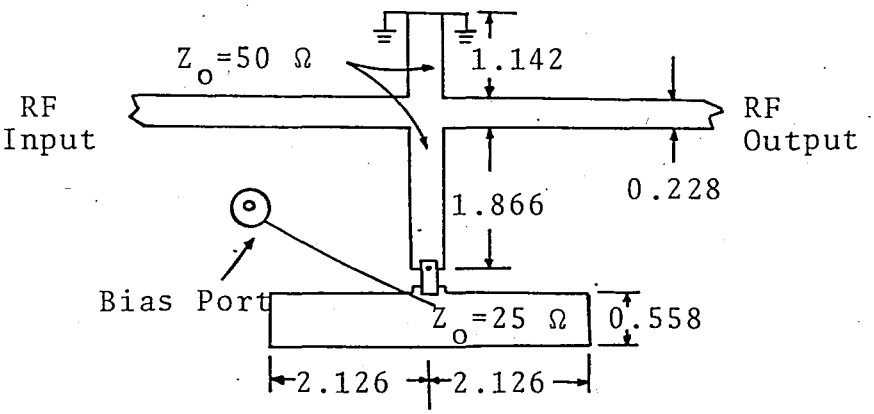


FIGURE 4.8. The 2.5 GHz stub switch using HP 3005 PIN diode. All dimensions in centimeters. Drawing is not to scale.

4.5. DESIGN PROCEDURE FOR MULTIPORT SWITCHES

Fisher (11) has proposed a design procedure for multiport switches based on the characteristics of quarter-wavelength-stub bandpass filters. Such filters of a number of quarter-wavelength stubs on a transmission line spaced at quarter-length intervals. An example of a three-stub maximally flat filter is shown in Figure 4.9.

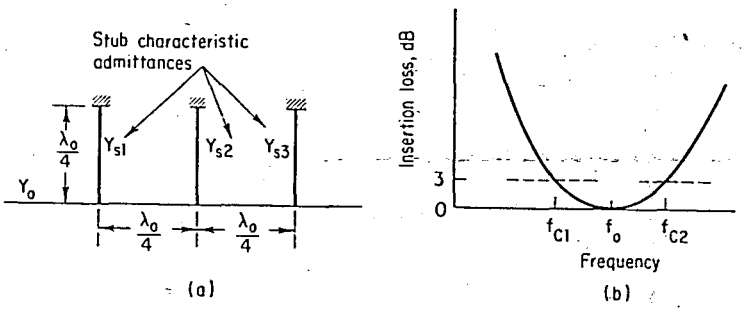


FIGURE 4.9. Three-stub maximally flat bandpass filter. (a) Schematic diagram showing stub length and spacing for maximally flat characteristic, $Y_{s1}=Y_{s3}=Y_{s2/2}$; (b) attenuation characteristic.

The basis of the Fisher procedure is the substitution of a so-called "quasi-lumped" stub for one of the stubs. A quasi-lumped stub consists of a lumped capacitance C across the main transmission line, in parallel with a short-circuited stub of characteristic: admittance Y_1 and length d_1, as shown in Figure 4.10. One method, found to give good practical results, is to equate the mid-band susceptance slope of the quasi-lumped stub to that of an actual $\lambda_o/4$ stub characteristic admittance Y_1. This may be done by considering Figure 4.10, where

$$B = j\omega C - jY_1 \cot \frac{\omega d_1}{\nu} \qquad (4.14)$$

where

$$\nu = \frac{3x10^{10}}{\sqrt{\dot{\epsilon}_{eff}}} \text{ cm/sec}$$

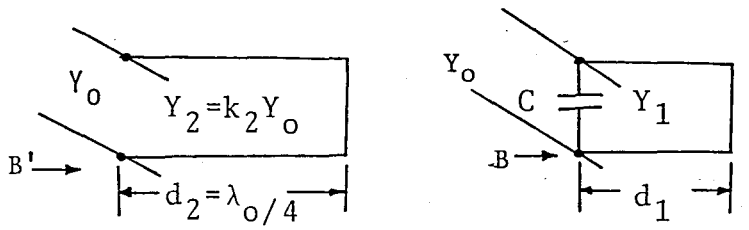


FIGURE 4.10. Stub equivalences (a) original quarter-wave short-circuited stub, (b) quasi-lumped stub approximation.

The corresponding radian frequency derivatives are then

$$\frac{dB}{d\omega} = j \left(C + Y_1 \frac{d_1}{\nu} \csc^2 \frac{\omega d_1}{\nu}\right) \tag{4.15}$$

Also, for the quarter wave stub

$$B' = -j\, Y_2 \cot \frac{\omega d_2}{\nu} \tag{4.16}$$

$$\frac{dB'}{d\omega} = j\, Y_2 \frac{d_2}{\nu} \csc^2 \frac{\omega d_2}{\nu} \tag{4.17}$$

Equating the two derivatives since we wish the selectivities to be equal near ω_o.

$$C + Y_1 \frac{d_1}{\nu} \csc^2 \frac{\omega d_1}{\nu} = Y_2 \frac{d_2}{\nu} \csc^2 \frac{\omega d_2}{\nu} \tag{4.18}$$

Let $\omega = \omega_o$ $\quad d_2 = \dfrac{\lambda_o}{4}$ $\quad k_2 = \dfrac{Y_2}{Y_o}$

then $$\csc^2 \frac{\omega_o d_2}{\nu} = 1$$

and

$$k_2 = \frac{4}{\pi}\frac{\omega_o C}{2Y_o} + \frac{4}{\pi}\frac{\omega_o d_1}{2\nu}\cdot\frac{Y_1}{Y_o}\csc^2\frac{\omega_o d_1}{\nu} \qquad (4.19)$$

also for $B = 0$ at $\omega = \omega_o$

$$\omega_o C = Y_1 \cot\frac{\omega_o d_1}{\nu} \qquad (4.20)$$

hence

$$d_1 = \frac{\nu}{\omega_o}\,\text{arc cot}\,\frac{\omega_o C}{Y_1} \qquad (4.21)$$

hence

$$k_2 = \frac{2}{\pi Y_o}\left\{\omega_o C + Y_1\left[\text{arc cot}\,\frac{\omega_o C}{Y_1}\right]\left[1 + \left(\frac{\omega_o C}{Y_1}\right)^2\right]\right\} \qquad (4.22)$$

An SPDT (Single Pole Double Throw) switch is realized by using two such filters connected together as shown in Figure 4.11. This diagram illustrates the reason for using multistub filters: If it is desired to direct power from

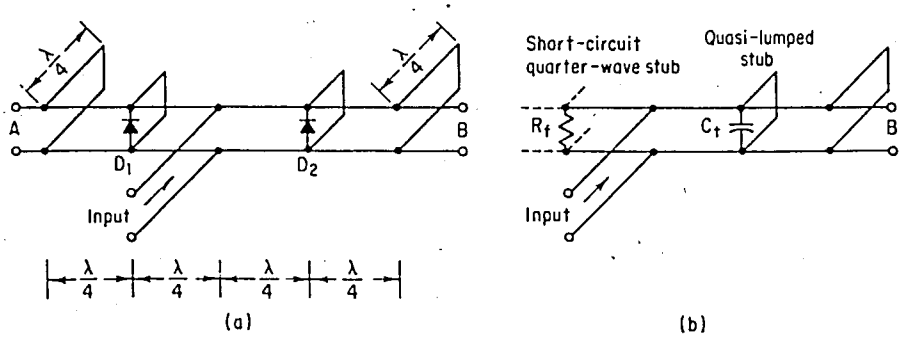


FIGURE 4.11. (a) SPDT switch configuration; (b) schematic diagram illustrating switch setting for transmission from input to port B.

the input to port B and isolate port A, the diode D_1 is forward biased, thus producing a quarter-wavelength short-circuit stub. The other two stubs, the quasi-lumped stub incorporating a reverse-biased diode D_2 and the final short-circuited quarter-wavelength stub, are designed to yield the required low-loss characteristic. The characteristic admittance of the first short-circuited stub (from the junction to D_1) in these configurations must be Y_o, the characteristic admittance of the main transmission line.

CHAPTER 5

BIASING AND DRIVING CONSIDERATIONS FOR PIN DIODE OF SWITCHES

5.1. BASIC RF SWITCHING BEHAVIOR OF PIN DIODES

Basically, a PIN diode switch consists of one or more PIN diodes usually shunted across an RF transmission line in such a way that dc, low frequency, or pulsed bias can be applied to them. These diodes have an approximate RF equivalent circuit consisting of a junction capacitance, C_j, shunted by an adjustable conductance, G (see Figure 5.1).

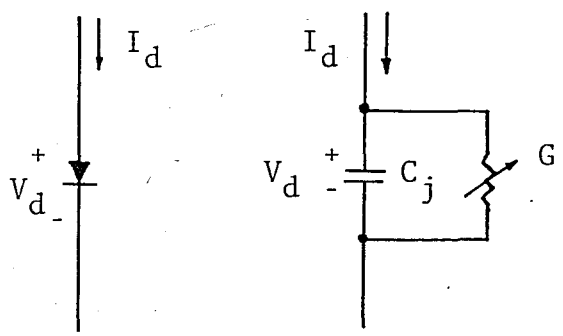


FIGURE 5.1. PIN diode and RF equivalent circuit.

The junction capacitance is fairly constant. The junction conductance is approximately proportional to the

charge stored within the diode, which is a function of diode current and time according to these equations:

$$i_d = \frac{d(Q_d)}{dt} + \frac{Q_d}{\tau} \quad \text{for } Q_d > 0 \tag{5.1}$$

$$i_d = C \frac{d(V_d)}{dt} \quad \text{for } Q_d < 0 \tag{5.2}$$

where

i_d = diode current

Q_d = charge stored in diode

τ = diode recombination time (typically in the range of 0.3 to 500 ns)

The case for $Q_d < 0$ is clearly just the back-bias capacitance effect of the diode. Therefore, $G \approx 0$ for $Q_d < 0$. The case for $Q_d > 0$ will be considered here.

Taking the Laplace transform of Eq. (5.1):

$$i_d(s) = s\, Q_d(s) + \frac{Q_d(s)}{\tau} \tag{5.3}$$

$$Q_d(s) = \frac{\tau\, i_d(s)}{(1 + s\tau)} \tag{5.4}$$

$$Q_d(s) = \frac{\tau\, i_d(j\omega)}{(1 + j\omega\tau)} \tag{5.5}$$

For constant ac current versus frequency, the ac charge storage component $Q_d(\omega)$ follows curve of Figure 5.2.

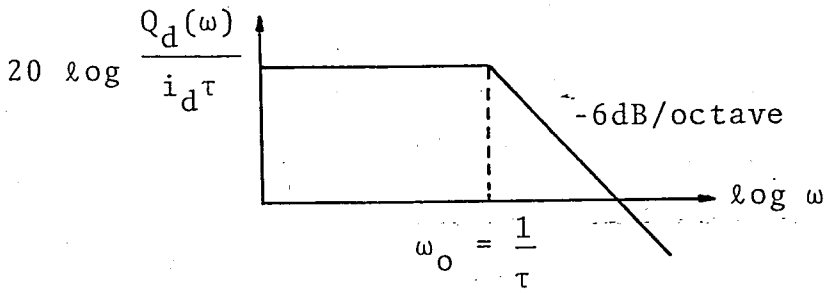


FIGURE 5.2. PIN behavior as a function of frequency.

For, a PIN diode with a life time of 100 nsec, $\omega_o = 10^7 sec^{-1}$ and $f_o \approx 1.6$ MHz.

Modulation frequency components up to about f_o have more or less the same effect as dc drive. Above f_o, however modulation efficiency decreases by -6 dB/octave as suggested by Fig. 5.2.

To reach a high value of G, a high value of Q_d must be reached. In Eq. (5.4) it is seen that the time response of Q_d to a step of forward diode current, I is:

$$Q_d(t) = L^{-1}|Q_d(s)| = I\,\tau\,(1 - e^{-t/\tau}) \qquad (5.6)$$

and the stored charge will follow the function of in Figure 5.3.

The rise time for stored charge, for G, and for the attenuation, will be several times τ, several hundred nano-

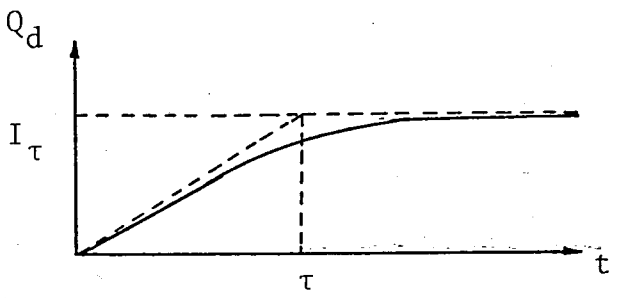


FIGURE 5.3. Charge stored response for constant drive current. Relatively slow rise fo response in the PIN diode for such drive limits switching speed.

seconds for a PIN diode of 100 ns liftime.

This time, however, can be shortened by using a shaped drive current pulse with initial overshoot, as shown in Figure 5.4. For perfect compensation, the area (current X time) of the initial spike should be $I\tau$, where I is the steady state value of the diode current pulse.

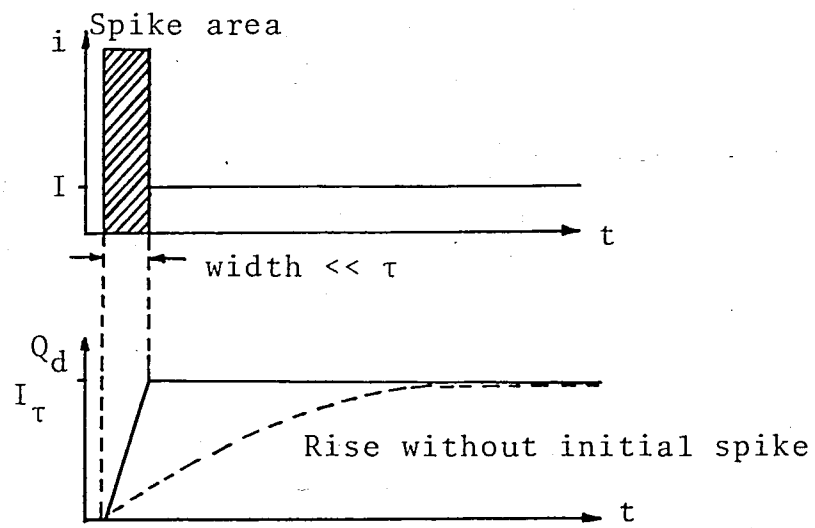


FIGURE 5.4. Spiked current drive accelerates charge storage in PIN diode with consequently faster switching.

5.2. CHARGE REMOVAL

The dynamics of the charge removal are similar to the dynamics of charge storage. A reduction of forward current instaneously to zero causes an exponentially decaying waveform of stored charge. Therefore a spiked reverse current waveform is also necessary for fast charge removal, as shown in Figure 5.5.

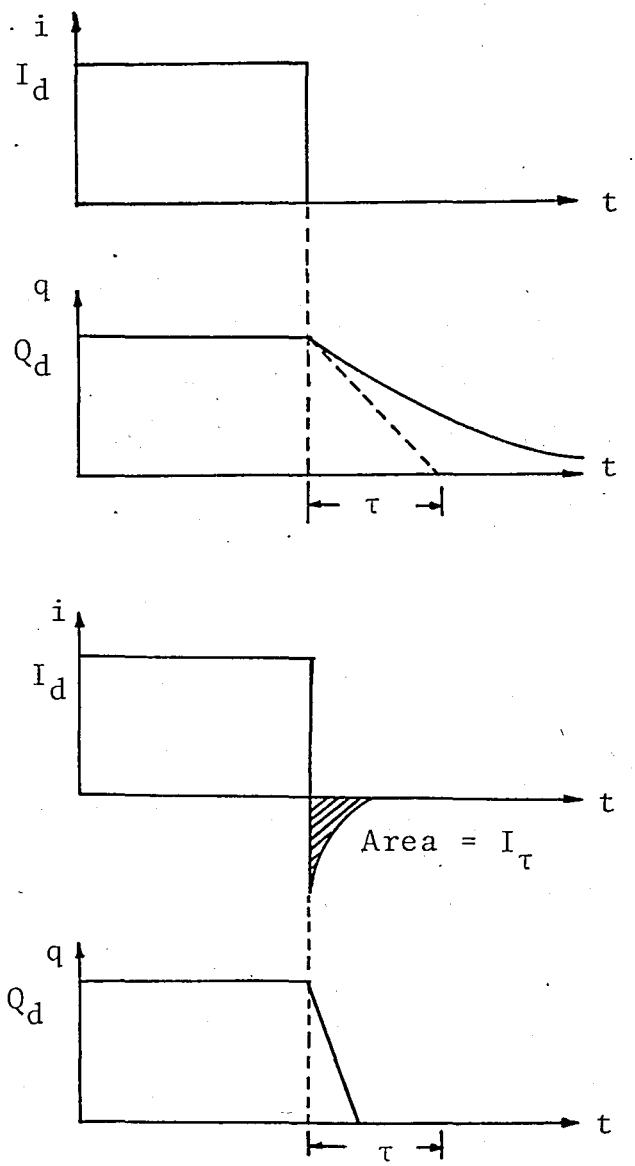


FIGURE 5.5. A reduction of forward current instaneously to zero causes an exponentially decaying waveform of stored charge.

5.3. PULSE DRIVE CIRCUIT CONSIDERATIONS FOR HIGH SPEED SWITCHING

For best performance a diode switch should be biased in both sates. Under most conditions PIN diodes are reverse biased only enough to hold off rectificed current (10V - 100V). But when harmonic generation, intermodulation products, or insertion loss must be low then the PIN diode must be biased to half the breakdown voltage V_{BR}. The reverse bias voltage V_R would be

$$V_R = \frac{V_{BR}}{2} \tag{5.7}$$

For lower power the bias need not be as high, but is a function of the incident peak power $\hat{P}_i$ as follows:

$$V_R = 2\sqrt{2P_i Z_o} \qquad \text{for series diodes} \tag{5.8}$$

$$V_R = \sqrt{2P_i Z_o} \qquad \text{for shunt diodes} \tag{5.9}$$

Although the PIN diode responds to current, the switch designer must achieve the driving source voltage swing needed to produce the desired bias current waveforms. To good approximation at the usual bias frequencies, the PIN diode has a forward V-I characteristic typical of silicon diodes, as shown in Figure 5.6. The voltage drop is approximately 1V and the forward bias current is I_F.

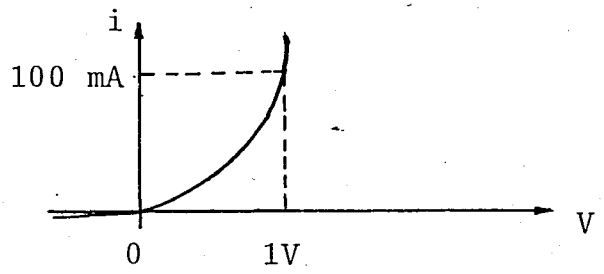


FIGURE 5.6. V-I characteristic of typical PIN diode.

The simplest bias circuit is shown in Figure 5.7. The series resistor is determined by

$$R = \frac{V_R - 1}{I_F} \qquad (5.10)$$

Nominal values of V_R and I_F are 20V and 100 mA respectively. Under these conditions, the battery has to be able to supply 2W power and R has to be able to dissipate it.

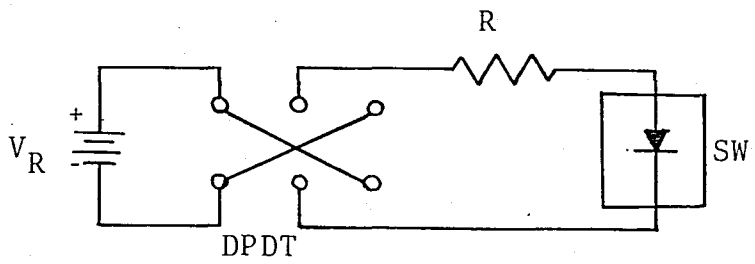


FIGURE 5.7. Manual switching driver circuit.

In many applications, the diode is normally in one state and put into the other state only for short periods of

time (pulsed). It is most efficient to arrange the switch so that it is reversed biased normally and pulsed into conduction. Figure 5.8 shows the circuit for a pulse driver. The pulse voltage must be large enough to overcome the 1V forward drop of the diode. Therefore, the pulse voltage must satisfy

$$V_P \geq V_R + 1 \tag{5.11}$$

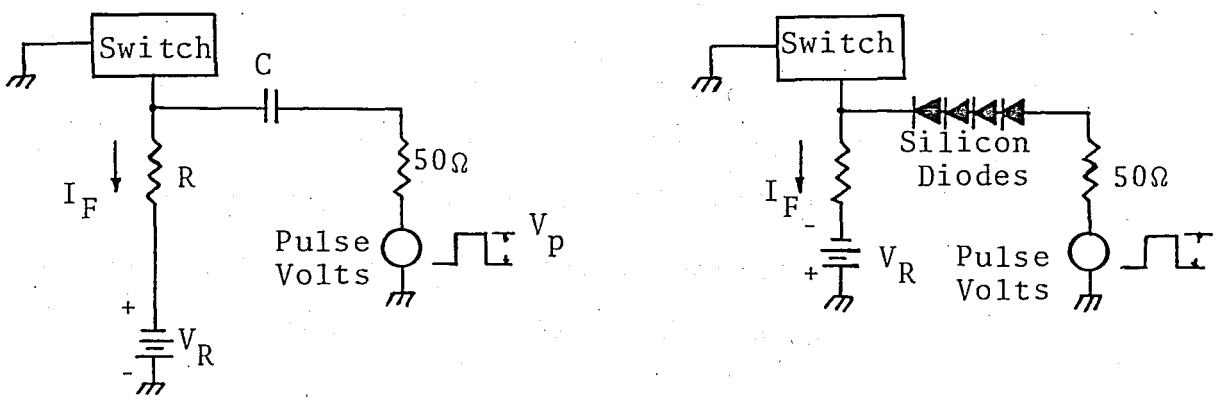


FIGURE 5.8. High-speed pulseing driver circuit.

The series capacitor should be part of an RC time constant longer than the pulse length t_p to prevent pulse sag (integration). The resistive part of the time constant is made up of the 50 ohm pulse generator impedance and the 10 ohm diode resistance. The series capacitor should satisfy

$$C > \frac{t_p}{60} \tag{5.12}$$

The mismatch of the conducting diode causes the pulse to be reflected back into the pulse generator. This pulse can be prevented from having undesirable transients either by making sure that the pulse generator has 50 ohm output impedance, or by using a long cable so that reflections appear after the diode switch has gone into the non-conducting state. A resistor may have to be put across the capacitor if the duty factor is high because the rectification of the switching diode will add to V_R and require V_P to be even larger.

If the diode is to be biased into conduction and pulsed into non-conduction, the circuit of Figure 5.8 will be adequate provided V_R and R are adjusted to give I_F. If R is greater than 500 ohms, the pulse voltage on the diode will be $2V_p$. The requirement on C is also relaxed as follows:

$$C > \frac{t_p}{50+R} \qquad (5.13)$$

For this polarity of switching, C can also be replaced by a diode (or multiple diode in series to assure that their forward drop is greater than that of the switching diode as shown in Fig. 5.8b). With a diode there is no limit to the pulse length.

When switching is done with a PIN the diode tends to slow the swtiching. The carriers take time after they are injected into the I region before they begin to recombine and charge the I region conductivity. Time is also necessary to

pull the carriers out of the I region when going to the non-conduction state. The charge stored in the I region Q_d os proportional to the forward current I_F and minority carrier lifetime τ.

$$Q_d = I_F \cdot \tau \tag{5.14}$$

To have rapid switching of a PIN diode, this charge must be rapidly injected and removed. The slow switching causes the waveform to be partially integrated. Partial differentiation of the drive pulse will compensate for the slow switching. A circuit to accomplish this is shown in Figure 5.9. The charge stored in C_τ is given by

$$Q_C = C_\tau V \tag{5.15}$$

in which V is the voltage across C_τ. This is the same voltage as appears across R_τ.

$$V = I_F \cdot R_\tau \tag{5.16}$$

For the complete initial charging of the diode to its final value:

$$Q_C = Q_d \quad \text{or} \quad C_\tau V = \frac{V}{R_\tau} \tau \quad \text{and} \quad R_\tau C_\tau = \tau \tag{5.17}$$

In other words, the time constant of the parallel $R_\tau C_\tau$ drive should be equal to the diode minority carrier re-

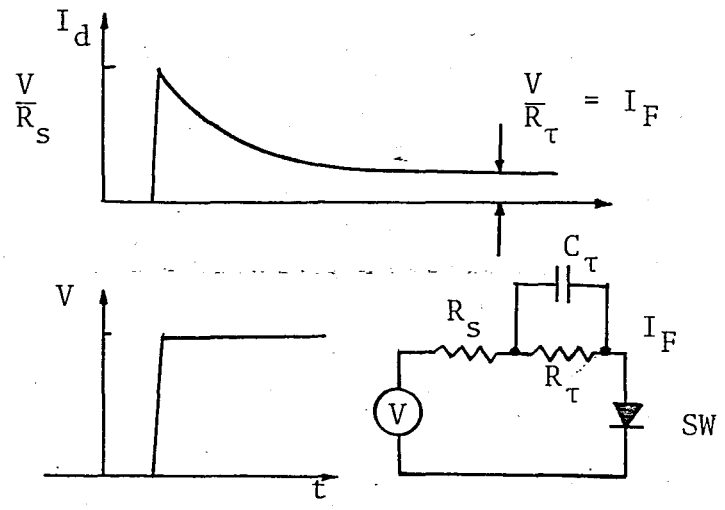


FIGURE 5.9. Capacitor (C_τ) allows initial current overshoot pulse with a high impedance source.

combination lifetime τ, for perfect compensation.

For Eq. (5.17) all of the charge in C_τ was assumed to be transferred to the I region. C_τ discharges through R_τ directly and has the resistance of external pulse circuit in series with the switching diode. Thus R_τ should be large and the external pulse circuit resistance, R_S should be low. Normally, it is reasonable to allow these resistance to be moderate, and to adjust $R_\tau C_\tau$ such that $Q_c > Q_d$. The extra current causes no problem in diode turn-on. Only if the reverse bias is near V_{BR} does it cause a problem in the breakdown current which may flow after the charge is cleared out of the I region.

When R_τ and C_τ are used, diode turn-on is limited by the RC time constant C_τ and the R_S composed of R_τ. For fast switching time diode turn-off is sped up by the circuit, but there is a limit to the speed with which it can be turned-off. The circuit pulls most of the free carriers out of the I region quickly, but to have high resistance the I region must be free of all carriers.

If a transistor is to be used as a driver, its collector current can be "spiked" by applying a step voltage to its base and using a parallel RC circuit in the emitter as shown in Figure 5.10.

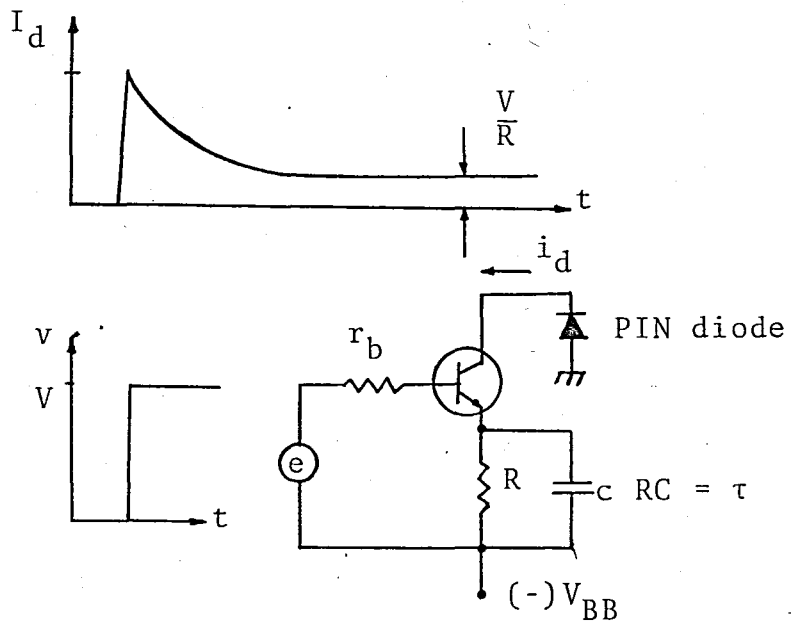


FIGURE 5.10. Current overshoot circuit for a transistor driver.

Of course, such a driver as the above cannot pass the reverse current that is necessary to quickly clear the stored charge out of the PIN diode. Therefore, following removal of the drive, the charge would exponentially decay as shown in Fig. 5.5, giving a slow switching in the reverse bias direction. The obvious answer to this problem is to make the drive circuit symmetrical about ground such that it can be caused by a spiked current waveform in either direction. Such a circuit is shown in Figure 5.11.

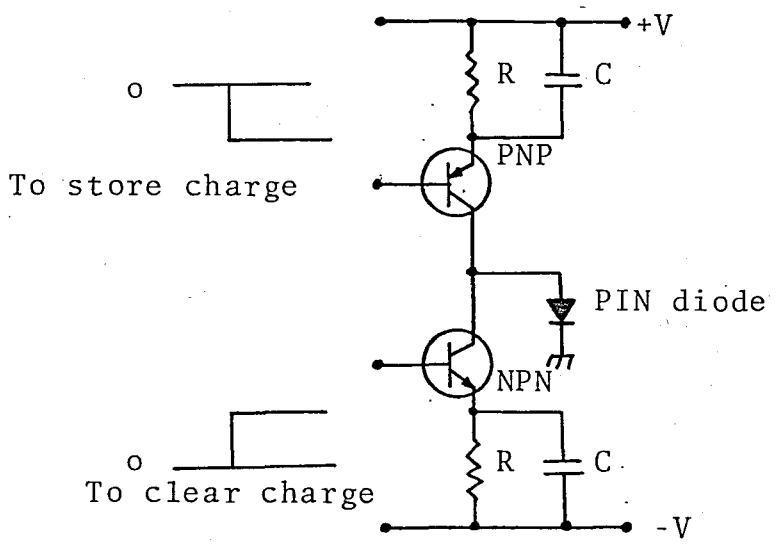


FIGURE 5.11. Symmetrical transistor driver for PIN diode switch allows fast pulsing in both the forward- and the reverse current directions.

The transistor stage that back biases the PIN diode faces somewhat different conditions from the one that forward biases does. Under forward bias, the PIN diode presents quite a low impedance associated with a low voltage drop; therefore, almost any desired current magnitude can be forced through it, even from a low supply voltage. In the reverse

current direction, however, the diode starts becoming a high impedance before all of its stored charge is cleared out, thus the reverse current becomes limited and a longer time is necessary to get the remaining charge out. The transient reverse current waveform becomes limited by the high impedance of the diodes for instaneous reverse voltages above approximately 40 volts. The result is that the reverse current is independent of diode reverse voltage, and hence the rate of decrease of stored charge can not be further increased. This effect limits the minimum possible time that is required to get the diode to its RF open (zero conductance) state. For typical 400 ns, 200-volt diodes, this minimum time is 70-100 ns for 40 volts reverse bias, and no amount of reverse drive will reduce the RF conductance significantly faster. This time is a function of diode breakdown voltage and lifetime, and can be made less than 1ns for certain diode types.

CHAPTER 6

EXPERIMENTAL RESULTS AND CONCLUSIONS

Figure 6.1 shows the test set-up used to measure the isolation and the insertion loss of the microwave diode switch. This measurement technique is known as the "substitution method". The crystal detector is connected to the SWR meter by 50 ohm cable. Table 6.1 presents the results of the measurement of the characteristics for the switch ranging from 2.4 GHz to 2.8 GHz. The performance of this switch is shown in Figure 6.2. Peak solution occurred at 2.6 GHz which is 4 percent higher than the design frequency of 2.5 GHz. Some of the error in design frequency was caused by finite fabrication tolerances in the lengths of the stub to the diode.

An analysis of the PIN diode has shown that this device will usually give much better performance as a microwave switch when used in dc bias operation. The PIN diode has several advantages over the other types of diodes.

1. Its characteristics are quite insensitive to bias over a large positive or negative voltage range. In the small range about zero bias, the series resistance and reactance vary rapidly with change

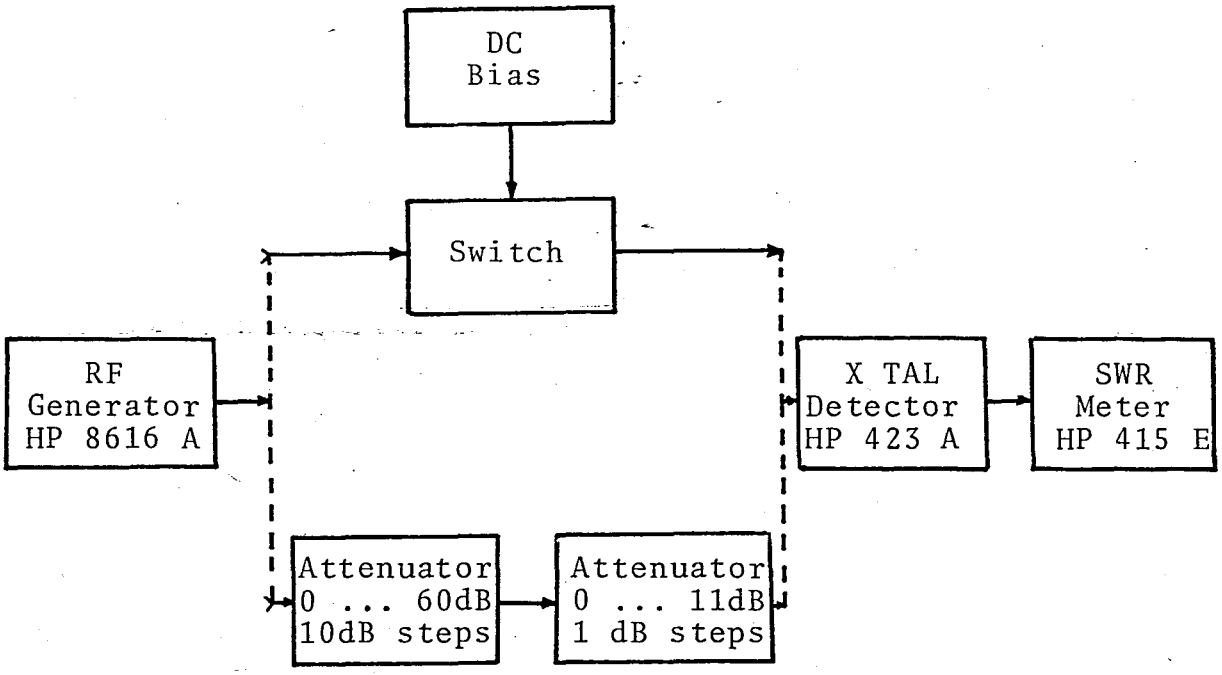


FIGURE 6.1. The setup for measuring isolation and insertion loss.

Frequency (GHz)	Bias	
	Isolation - dB -5V	Insertion Loss + 10 mA
2.40	19.5	7.5
2.45	20	6
2.50	23	5
2.55	25	3.5
2.60	25.5	3
2.65	24	1.5
2.70	21	3
2.75	18.5	6
2.80	18	7

TABLE 6.1. Experimental results for the microwave diode switch. Isolation at -5V, insertion loss at + 10 mA.

in the bias.

2. The series resistance in both states is lower than for other types of diodes presently available.

3. It exhibits a lower capacitance.

PIN diodes with lower R and C are available in a standard package, hermetically sealed, and consisting of a ceramic body bonded to gold-plated metal lugs.

For the transmission line, a microstrip line is preferable to a coaxial line or a waveguide as discussed in Chapter 3. Complete shielding is essential for most applications in order to reduce radiation loss and the coupling between different circuits.

Microwave diode switch is developed in the SPST configuration which has good characteristics at the single frequency in S-band region. Its measured characteristics is indicated in Figure 6.2 and Table 6.1. With moderate bias of + 10 mA, minimum insertion loss 1.5 dB and with -5V reverse bias, maximum isolation 25.5 dB are obtained.

The switching speed of a PIN diode may be defined in a number of ways. Ideally, the time it takes the device to make the transition from the minimum insertion loss to the maximum isolation or vice versa. To switch a shunt diode

circuit from on to off we must inject a charge into the diode; to switch it from off to on, we must completely remove this charge. When the fastest off to on switching speed is required, one should use the lowest steady state bias current that is consistent with the required isolation level. The less charge, the faster it can be removed. The switching speed of a PIN diode is a function of τ.

In summary, the designer must consider two major points which affect the speed of a switching circuit: the lifetime of the diodes and the magnitude and rise time of the switching pulse.

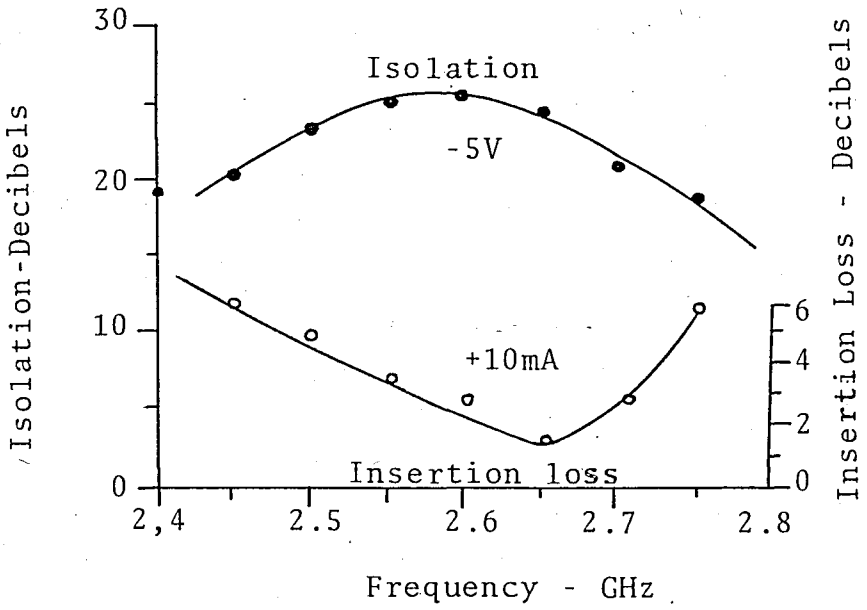


FIGURE 6.2. Performance of the stub switch.

APPENDIX A

PHYSICAL CONSTANTS AND OTHER DATA

A.1. PHYSICAL CONSTANTS (12)

Permittivity of free space	$\varepsilon_o = 8.85 \times 10^{-14}$ F/cm
Permeability of free space	$\mu_o = 4\pi \times 10^{-9}$ H/cm
Impedance of free space	$Z_o = 376.7 \approx 120\pi\ \Omega$
Velocity of light	$C = 2.998 \times 10^{10}$ cm/sec
Charge of electron	$q = 1.602 \times 10^{-19}$ C
Electronic rest mass	$m_o = 9.11 \times 10^{-31}$ kg
Plank's constant	$h = 6.63 \times 10^{-34}$ J.sec
1 Å (angstrom) = 10^{-8} cm	milli-, m- = 10^{-3}
1 μm (micron) = 10^{-4} cm	micro-. μ- = 10^{-4}
1 mil = 10^{-3} in.	nano-, n- = 10^{-9}
2.54 cm = 1 in.	pico-, p- = 10^{-12}
1 eV = 1.6×10^{-19} J	kilo-, k- = 10^{3}
	mega-, M- = 10^{6}
	giga-, G = 10^{9}

A.2. DIELECTRIC MATERIALS USED FOR MICROSTRIPS LINES (13)

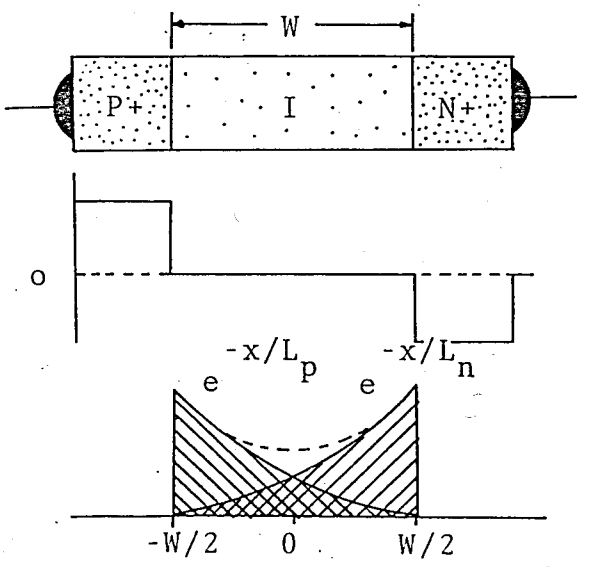
Material	Dielectric Constant	Loss Factor	Useful Temp range, ^{o}C
Woven	2.55	.0015	-60 to +200
Microfiber TFG Duroid 5870	2.33	.0005	-60 to +200
Duroid 5880	2.2	.0006	-60 to +200
Polystyrene	2.53	.0003	-60 to +200
Reinforced	2.62	.002	-60 to +200
Polyphenelene oxide, PPO	2.55	.0016	-60 to +200
Polyolefin	2.32	.00015	-60 to +200
Quartz Teflon	2.47	.0006	-60 to +200
Polymide, Micaply 5032	4.8	.01	-60 to +250
Epsilam -10	10.0	.002	-60 to +150
99.5% alumina	9.9	.00008	up to 500
Quartz (fused silica)	3.78	.0001	up to 500
Sapphire	9.4	.00008	up to 500
99.5% Be O	6.6	.0004	up to 500
Boron nitrid	4.4	.0003	up to 500

APPENDIX B

SEMIRIOGOROUS SOLUTIONS FOR I LAYER RESISTANCE

The derivation is similiar to that given by Leenov (14). The parameters are derived from an abrupt junction model shown in Figure B.1. The resistance of the I layer can vary over a wide range depending on the densities of injected carriers throughout the I region at forward bias. Before attempting a solution for this resistance, let us first state the simplifying assumptions to be used:

(1) the same diffusion coefficient for holes and electrons in the I layer ($D = 2 D_p D_n / D_p + D_n$ = ambipolar diffusion coefficient) and $\tau_n = \tau_p = \tau$.



$$p(x) = n(x) \ldots$$

$$\sigma(x) = q\left[\mu_p \cdot p(x) + \mu_n \cdot n(n)\right]$$

$$R_I = \frac{1}{A} \int_{-W/2}^{+W/2} \frac{dx}{\sigma(x)}$$

FIGURE B.1. Abrupt junction model.

(2) Quasi-neutrality, i.e., $p(x) = n(x)$, and hence $\partial_n/\partial_x = \partial_p/\partial_x$;

(3) The hole current at the P+I interface consists entirely of hole current and a similarly situation occurs for electrons at the N+I interface; and

(4) injection of electrons into the P+ region and holes into the N+ region may be neglected (this is a requirement of 3).

The equations for the continuity of hole and electron current are given by

$$\frac{1}{q}\frac{\partial J_p}{\partial x} + \frac{p-p_i}{\tau_p} = -\frac{\partial p}{\partial t} \qquad \text{(B.1)}$$

$$-\frac{1}{q}\frac{\partial J_n}{\partial x} + \frac{n-n_i}{\tau_n} = -\frac{\partial n}{\partial t} \qquad \text{(B.2)}$$

where $p = p(x)$ - hole density distribution

$n = n(x)$ - electron density distribution

J_p, J_n = hole, electron current, respectively

p_i, n_i = intrinsic carrier concentration

The components I_p and I_n are related to the carrier concentration,

$$J_p = \frac{I_p}{A} = q\left(\mu_p\, p\, E - D_p \frac{dp}{dx}\right) \qquad (B.3)$$

$$J_n = \frac{I_n}{A} = q\left(\mu_n\, n\, E + D_n \frac{dn}{dx}\right) \qquad (B.4)$$

where E = electric field and $D = 2D_pD_n/D_p+D_n$ (a result of assumption (1) above).

Combining Eq. (B.1) to (B.4), we can write,

$$\frac{\partial n}{\partial t} + \frac{\partial p}{\partial t} = -\frac{(n-n_i)}{\tau} - \frac{(p-p_i)}{\tau} + D\frac{\partial^2 n}{\partial x^2} + D\frac{\partial^2 p}{\partial x^2} + \mu\frac{\partial}{\partial x}\left[(n-p)\,E\right] \qquad (B.5)$$

Since E will be small in a heavily injected region and also since n=p, the last term on the R.H.S. of Eqs. (B.5) may be dropped. Since n=p we can also convert Eq. (B.5) to:

$$\frac{\partial n}{\partial t} = -\frac{n-n_i}{\tau} + D\frac{\partial^2 n}{\partial x^2} \qquad (B.6a)$$

or

$$\frac{\partial p}{\partial t} = -\frac{p-p_i}{\tau} + D\frac{\partial^2 p}{\partial x^2} \qquad (B.6b)$$

and, in the dc steady state, $\partial n/\partial t = \partial p/\partial t = 0$. Hence, and if n and p are much larger than n_i and p_i (which is the definition of conductivity modulation), we can write:

$$\frac{\partial^2 n}{\partial x^2} - \frac{n}{L^2} = 0 \qquad (B.7a)$$

$$\frac{\partial^2 p}{\partial x^2} - \frac{p}{L^2} = 0 \qquad \text{(B.7b)}$$

where $L = \sqrt{D\tau}$ = diffusion length. Equations (B.7a) and (B.7b) are the so called steady-state diffusion equations, and their solution (satisfying a given set of boundary conditions) defines the carrier distributions in the I region. The coordinate system to be used is shown in Figure B.1. Since $n(x) = p(x)$, it is sufficient to solve either Eqs. (B.7a) or (B.7b). The equation is a simple second-order differential equation, and the solution is known to be of the form:

$$n(x) = A_1 \exp\left(+\frac{x}{L}\right) + A_2 \exp\left(-\frac{x}{L}\right) \qquad \text{(B.8)}$$

Due to the double injection, finite diffusion length, and assumption (1), we expect $n(x)$ to be minimum at $x=0$, i.e.,

$$\left.\frac{dn(x)}{dx}\right|_{x=0} = 0 \qquad \text{(b.9)}$$

This requires that $A_1 = A_2$. Therefore, Eq. (B.8) can be written

$$n(x) = 2 A_1 \cosh\left(\frac{x}{L}\right) \qquad \text{(B.10)}$$

At $x = W/2$ we require

$$n(x)\Big|_{x=W/2} = n\left(\frac{W}{2}\right)$$

a boundary condition. Applying this boundary condition to Eq. (B.10), we get:

$$n(x) = \frac{n(W/2) \cdot \cosh(x/L)}{\cosh(W/2L)} \tag{B.11}$$

Therefore, once the value of n at x=W/2 (N+I interface) is known the carrier distribution in the I-region will be given by Eq. (B.11).

The solution for n(W/2) proceeds as follows, at $x = + W/2$, $J_p=0$ (assumption 3). Hence, from Eq. (B.3)

$$J_p = 0 = q(\mu\, p\, E - D\, \frac{dp}{dx}) \tag{B.12}$$

or

$$\mu\, p\, E = D\, \frac{dp}{dx} \tag{B.13}$$

From Eq. (B.13) and (B.4), the continuity current, and recalling that p(x) = n(x), it follows that

$$I_o = J_n \cdot A\Big|_{x=W/2} = 2\, q\, D\, A\, \frac{dn}{dx} \tag{B.14}$$

where I_o = bias current and A = area of the I layer. Differentiating Eq. (B.11) to get dn/dx and solving Eq. (B.14) for n(W/2), we get

$$n(\frac{W}{2}) = \frac{I_o \, L \cosh (W/2L)}{2 \, q \, D \, A \sinh(W/2L)} \qquad (B.15)$$

Substituting this result into Eq. (B.11), we have

$$p(x) = n(x) = \frac{I_o \, L \cosh (x/L)}{2 \, q \, D \, A \sinh (W/2L)} \qquad (B.16)$$

This is the carrier distribution we have been seeking. The carrier densities are seen to depend on the bias current density, I_o/A, and the ratio W/2L (I-region width divided by twice diffusion length).

The resistance of the I layer may be calculated from

$$R_I = \frac{1}{A} \int_{-W/2}^{+W/2} \frac{dx}{\sigma(x)} \qquad (B.17)$$

where

$$\sigma(x) = q \, \mu \, [n(x) + p(x)] = 2 \, q \, \mu \, n(x) \qquad (B.18)$$

R_I may be found by substituting Eq. (B.17) into Eq. (B.18) and carrying out the integration (15). The result is:

$$R_I = \frac{2(kT/q)}{I_o} \cdot \sinh (\frac{W}{2L}) \cdot \tan^{-1}[\sinh (\frac{W}{2L})] \qquad (B.19)$$

when W/L < 1, Eq. (B.19) approaches form previously obtained,

$$R_I = \frac{W^2}{2\mu} \cdot \frac{1}{I_o \tau} \qquad (1.14)$$

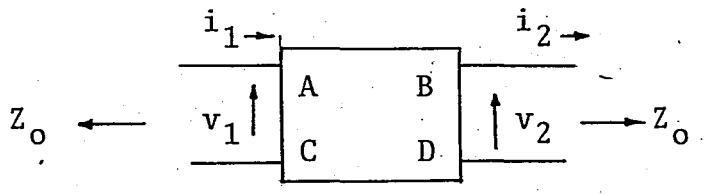
APPENDIX C

ABCD - MATRICES

Conventional loop and nodal analyses are convenient for circuits comprised of all lumped elements. However, when distributed elements (transmission line elements) become mixed with elements, method of calculation using matrices are more convenient. The well-known matrix methods are impedance matrix (Z), admittance matrix (Y), wave cascading coefficient matrix (r), generalized circuit constant matrix (ABCD), and scattering matrix (S). Of these types of matrices, two stand out as most useful for microwave circuits. Measurements are most often made in terms of S parameters. S_{11} is identical to Γ, the voltage reflection coefficient, and the basic parameter of the Smith Chart. Calculations are most easily made using ABCD matrices, because: (a) lumped elements and transmission line elements are related to the matrix elements quite simply; and (b) elements are cascaded simply by multiplying their matrices.

Beaty and Kerns (16) give the definitions of and interrelationships between the various matrices even when input and output impedances are equal. The more restrictive case given here is adequate for most problems and is all that is

required for the derivations presented in this section. The overall input and output impedances are assumed to be equal. The terms of the ABCD matrix are defined in Figure C.1. A is the voltage transforming term; D, current transformer; B, a series impedance term; and C, shunt admittance.



$$v_1 = A\, v_2 + B\, i_2 \qquad \text{(C.1)}$$

$$i_1 = C\, v_2 + D\, i_2 \qquad \text{(C.2)}$$

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \qquad \text{(C.3)}$$

SUMMETRICAL: $A = D$ (C.4)

RECIPROCAL: $AD - BC = 1$ (C.5)

LOSSLESS RECIPROCAL: A and D - REAL,
B and C - IMAGINARY

FIGURE C.1. ABCD matrix definition.

The representation of various elements by ABCD matrices is given in the upper half of Figure C.2. Z and Y are complex numbers. A Lossey transmission line may be represented either by using hyperbolic functions or by putting the appropriate attenuator next to each lossless line.

The relationships permitting SBCD to be converted to S parameters are given in the lower portion of Figure C.2. The main terms of interest are S_{21} and S_{11}. Attenuation is given by

$$\alpha = 20 \log \left|\frac{1}{S_{21}}\right| = 20 \log \left|\frac{A+B+C+D}{2}\right| \qquad (C.10)$$

Using normalized ABCD. The transmission phase shift is given by

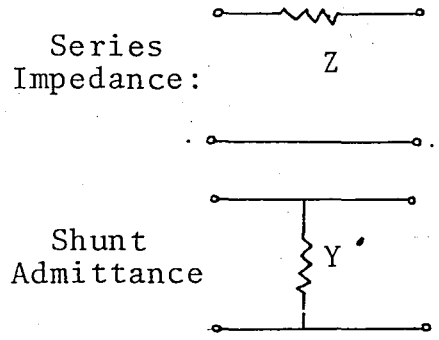
$$\Phi = - \tan^{-1} \left[\frac{I_m(A+B+C+D)}{R_e(A+B+C+D)}\right] \qquad (C.11)$$

The reflection coefficient is given by S_{11}

$$\Gamma = S_{11} \qquad (C.12)$$

From this can be calculated the VSWR,

$$s = \frac{1 + |\Gamma|}{1 - |\Gamma|} = \frac{1 + |S_{11}|}{1 - |S_{11}|} \qquad (C.13)$$



	General ABCD	Normalized ABCD
Series Impedance:	$\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & Z/Z_o \\ 0 & 1 \end{bmatrix}$
Shunt Admittance	$\begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ Y/Y_o & 1 \end{bmatrix}$

INPUT REFLECTION COEFFICIENT

$$S_{11} = \frac{A+BY_o-CZ_o-D}{A+BY_o+CZ_o+D} \qquad \frac{A+B-C-D}{A+B+C+D} \qquad (C.6)$$

REVERSE VOLTAGE TRANSFER COEFFICIENT

$$S_{12} = \frac{2(AD-BC)}{A+BY_o+CZ_o+D} \qquad \frac{2(AD-BC)}{A+B+C+D} \qquad (C.7)$$

FORWARD VOLTAGE TRANSFER COEFFICIENT

$$S_{21} = \frac{2}{A+BY_o+CZ_o+D} \qquad \frac{2}{A+B+C+D} \qquad (C.8)$$

OUTPUT REFLECTION COEFFICIENT

$$S_{22} = \frac{-A+BY_o-CZ_o+D}{A+BY_o+CZ_o+D} \qquad \frac{-A+B-C+D}{A+B+C+D} \qquad (C.9)$$

FIGURE C.2. ABCD matrix relationships.

APPENDIX D

GENERAL PURPOSE DIODES ELECTRICAL SPECIFICATIONS AT $T_A = 25^{o}C$ (17)

Part Number 5082	Maximum Total Capacitance C_T(pF)	Minimum Breakdown Voltage V_{BR}(V)	Maximum Series Resistance R_s (Ω)	Minimum Effective Carrier Lifetime τ(ns)	Maximum Reverse Recovery Time t_{rr}(ns)
GENERAL PURPOSE SWITCHING					
3001	0.25	200	1.0	100	100
3002	0.2	300	1.0	100	100
3005	0.25	150	0.8	400	100
SOLDERING CONDITIONS			250°C 5 sec		
FAST SWITCHING					
3040	0.30*	70	0.8	15	5
3041	0.30*	70	0.8	15	5
3042	0.4*	70	1.0*	15	5
3043	0.4*	50	1.5*	15	10
SOLDERING CONDITIONS			230°C 5 sec		
Test Conditions	VR=50 *VR=20 f=1MHz	$V_R=V_{BR}$ Measure $I_R \leq 10\mu A$	I_F=100mA *I_F=20mA f=100MHz	I_F=50mA I_R=250mA	I_F=20mA V_R=10V

TYPICAL PARAMETERS

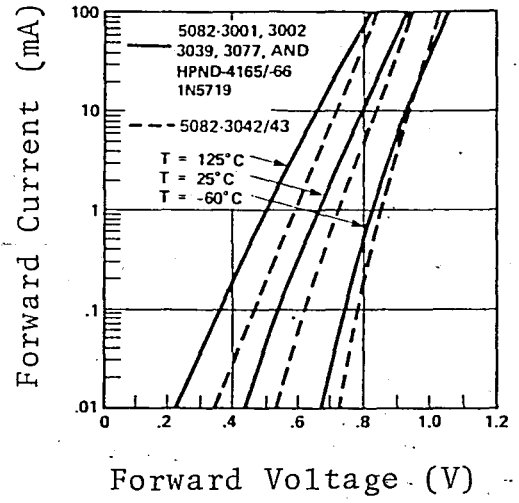


Fig. D.1. Typical forward current ve. forward voltage.

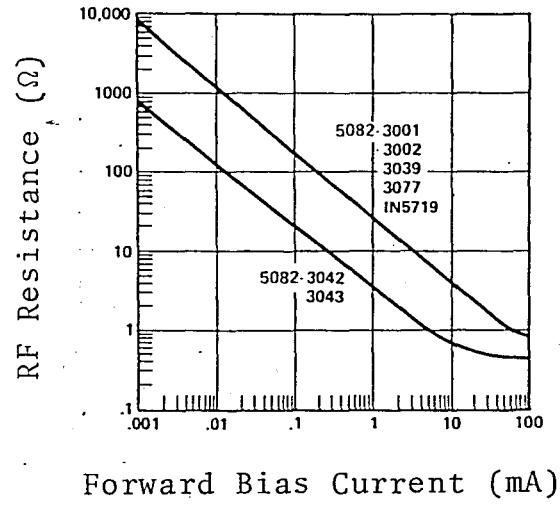


Fig. D.2. Typical RF resistance vs forward bias current.

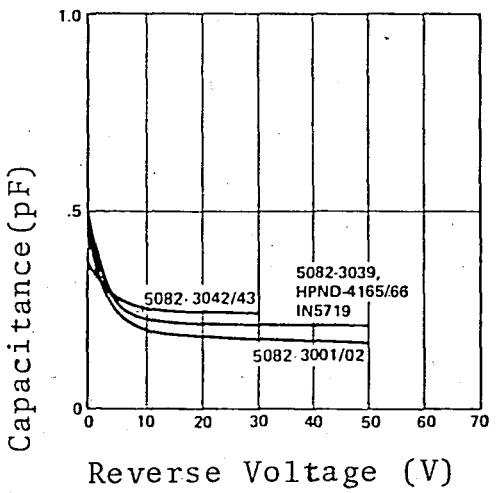


Fig. D.3. Typical capacitance vs reverse voltage.

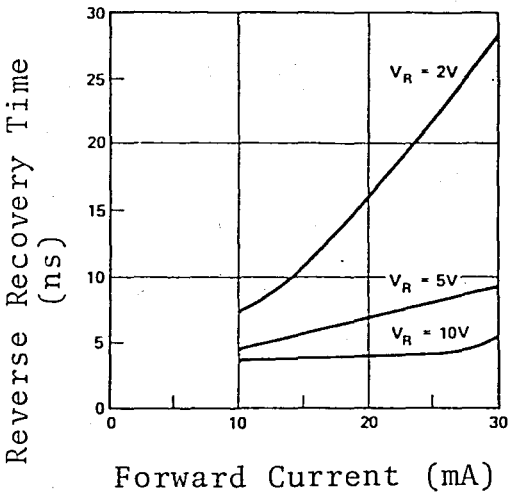


Fig. D.4. Typical reverse recovery time vs forward current for various reverse driving voltages, 5082, 3042, 3043

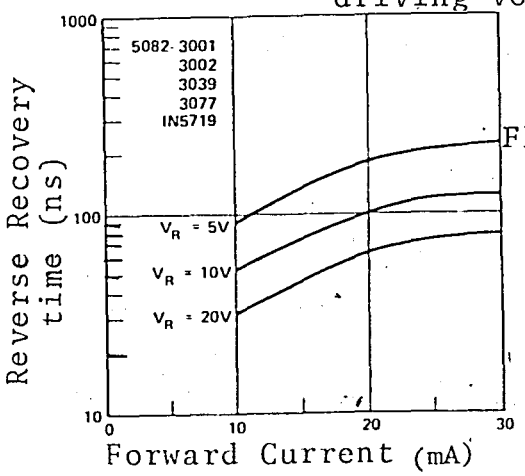
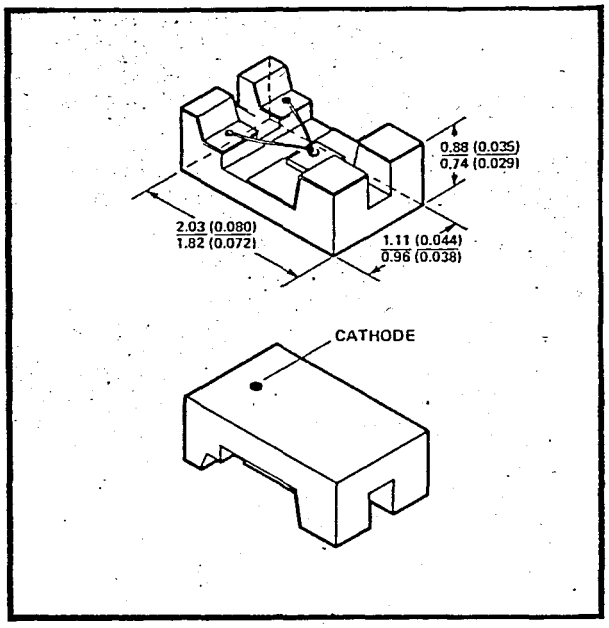
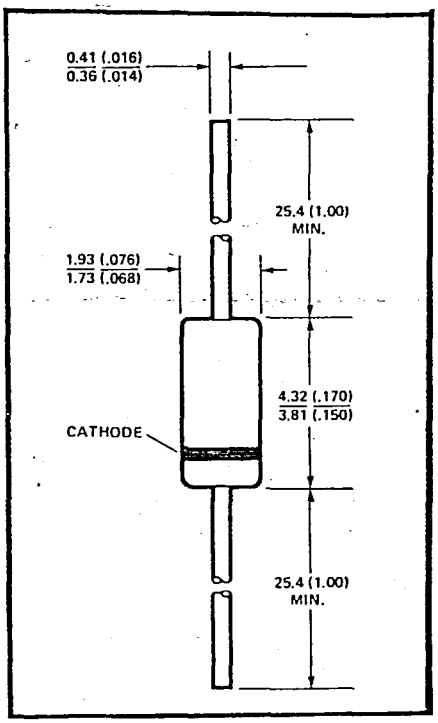


FIG. D.5. Typical Reverse Recovery Time vs Forward Current.

PACKAGE OUTLINES



Outline 50
HP 3005



Outline 15
HP 3001

All Dimensions in Millimeters and (inches)
Drawings are not to Scale

NOTES:

1. Handle with grounded tweezers and grounded bonding equipment. These diodes are pulse sensitive and may be damaged by electrostatic charges.
2. Use standard thermocompression bonding techniques. Ultrasonic bonding is not recommended.
3. Either ultrasonic or thermocompression bonding techniques can be employed.
4. Reverse polarity. Anode is the bottom contact and the cathrode is the top contact.

BIBLIOGRAPHY

1. M.A. Armisted, E.G. Spencer and R.D. Hatcher, "Microwave Semiconductor Switch," PRO. IRE, Vol. 44, pp. 1875; December, 1956.

2. E.S. Yang, Fundamentals of Semiconductor Devices, New York: McGraw-Hill, pp. 83-89, 1978.

3. R. Galvin and A. Uhlir, Jr., "Transient Microwave Impedance of PIN Switching Diode," IEEE Trans. on Electron Devices, Vol. ED-11, pp. 441, September, 1964.

4. Robert V. Garver, Microwave Diode Control Devices, Massachusetts: Artech House, pp. 22, 1978.

5. R.V. Garver, "Theory of TEM Diode Switching," IRE Trans. on Microwave Theory and Techniques, Vol. MTT-9, pp. 224-228, May 1961.

6. Hewlett Packard Components. Diode and Transistor Designer's Catalog, California: Hewlett-Packard, pp. 242, 1980.

7. Schneider, M.V., "Microstrips Lines for Microwave Integrated Circuits," Bell System Tech. Journal, pp. 1432-1434, May-June, 1969.

8. G. Subak-Sharpe, Integrated Circuit Engineering, Reading, Massachusetts: Addison-Wesley, pp. 137, 1979.

9. Andrew H. Kwon, "Design of Microstrip Transmission Line," Microwave Journal, Vol. 19, No. 1, pp. 61-63, January, 1976.

10. Robert V. Garver, Microwave Diode Control Devices, Massachusetts: Artech House, pp. 143-145, 1978.

11. R.E. Fisher, "Broadbanding Microwaves Diode Switches," IEEE Trans. Microwave Theory Tech., :TT-13, pp. 706, 1965.

12. Ben G. Streetman, Solid State Electronic Devices, Englewood Cliffs, N.J.: Prentice-Hall, pp. 442, 1980.

13. Donald G. Fink and Donald Christionsen, Electronics Engineers' Handbook, New York: McGraw-Hill, pp. 9-12, 1982.

14. D. Leenov, "The Silicon PIN Diode as a Microwave Radar Protector at Megawatt Levels," IEEE Trans. PGED, Ed-11, pp. 53-61, 1964.

15. Jan J. Tuma, Engineering Mathematics Handbook, New York: McGraw-Hill, pp. 323, 1979.

16. R.W. Beaty and D.M. Kerns, "Relationship between Different Kinds of Network Parameters, Not Assuming Reciprocity or Equality of the Waveguide or Transmission Line Characteristic Impedance," Proc. IEEE, Vol. 52, pp. 84, January, 1964.

17. Hewlett Packard Components Diode and Transistor Designers' Catalog, California: Hewlett-Packard, pp. 189-192.

REFERENCES NOT CITED

S.M. Sze Physics of Semiconductor Devices, New York: John Wiley and Sons, 1969.

H.A. Watson Microwave Semiconductor Devices and Their Circuit Applications. New York: McGraw-Hill, 1969.

R.J. Chaffin Microwave Semiconductor Devices. John Wiley and Sons, 1973.

J. White Semiconductor Control. Dedham, MA: Artech House, 1977.

H.V. Shurmer Microwave Semiconductor Devices. New York: Wiley Interscience, 1971.

M. Caulton "PIN Diodes for Low-Frequency High-Power Switching Applications", IEEE Trans. on Microwave Theory and Techniques, Vol. MTT.30, pp. 875-881, 1982.

R.V. Garver, E.G. Spencer and M.A. Harper, "Microwave Semiconductor Switching Techniques," IRE Tran. on Microwaves Theory and Techniques, Vol. MMT.6, October 1958, pp. 378-583.

D. Leenov "PIN Diode Microwave Switches and Modulators," Solid State Design, Vol. 6, pp. 37-40, April 1965, pp. 33-37, May 1965.

L.S. Senhouse, Jr., "Reverse Biased PIN Diode Equivalent Circuit Parameters at Microwave Frequencies", IEEE Trans. on Electron Devices, Vol. ED-13,pp. 314-322, March 1966.

C.J. Georgopoulos, "PIN-Driver Design Saves Time," Microwaves, pp. 50-55, August 1972.

Annon "Biasing and Driving Considerations for PIN Diode RF Switches and Modulators," Hewlett Packard Application Note 914, January 1967.

Forge, Churck "Driving the PIN Diode Switch," Microwaves, pp. 30-36, April 1967.

Catalog 105, Newark Electronics, Chicago: Enterprise of Premier Industrial Corporation, 1981.