TIME-VARIANT LINEAR TRANSISTOR MODEL TO BE USED IN SWITCHING CIRCUITS

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TIME-VARIANT LINEAR TRANSISTOR MODEL TO BE USED IN SWITCHING CIRCUITS

The aim of this thesis is to apply a time-variant linear large signal transistor model (15) to the Bipolar Junction Transistors (BJTs) and Vertical V-groove Metal Oxide Semiconductor Transistors (VVMOSTs),to analyse basic three transistor switching circuits by using this model,and to compare the results of analyses with the experimental results.

The time-variant linear large-signal BJT model includes the time-variant equivalent output resistance and capacitance and the D.C. voltage source which represents the saturation voltage.In this model the equivalent output capacitance is connected in parallel with the equivalent output resistance and the D.C. voltage source which are connected in series with one another.This model which is applied to the bipolar transistor is also used as the output side of the VVMOS transistor model beyond the saturation voltage.The input side of the VVMOS model includes only an input capacitance between the gate and the source.The related model parameters are determined separately for the BJTs and VVMOS transistors.

The equivalent output resistance and capacitance of the new BJT model are changed only in the transient regions as an exponential function.They are taken as a constant value in the other regions.

In the VVMOS transistor model the equivalent output resistance

is considered as a function of input voltage in the resistive and pinch-off regions.For the turn-on delay and cut-off regions,the equivalent output resistance is taken as a constant value which is equal to the transistor maximum drain to source resistance.The equivalent output capacitance is considered as a function of the output voltage for all regions.

The model related to the VVMOS transistors can also be used for the Vertical Double-diffused Metal Oxide Semiconductor (VDMOS) transistor.Useful formulas and necessary explanations for this purpose and the related model parameters are also considered as the subject of this thesis.

As an application,the analysis of three basic transistor switching circuits,switching circuits with resistive,resistive-inductive and resistive-inductive-capacitive loads,and the Complementary VDMOS (CVDMOS) inverter are done by using the proposed models.The accuracy of the models is evaluated by a detailed comparison of simulated and measured switching characteristics on the experimental high-speed switching circuits.

This new model which is applied to the transistor switching circuits can be considered as the best one which provides an optimum combinetion of accuracy,ease of parameter acquisition,simplicity, and less computational costs,so far.

ANAHTARLAMA DEVRELERİNDE KULLANILACAK ZAMANLA DEĞİŞEN LİNEER TRANZİSTOR MODELLERİ

Bu tezin gayesi bipolar tranzistorlar için geliştirilmiş modeli VVMOS tranzistorlara uygulamak,bu model yardımı ile tranzistorlu üç temel anahtarlama devresinin analizlerini yapmak ve elde edilen analiz sonuçlarını deneysel sonuçlarla mukayese etmektir.

Bipolar tranzistorun lineer zamanla değişen büyük işaret modeli, zamanla değişen eşdeğer çıkış direnç ve kapasitesi ile doyma gerilimini temsil eden bir doğru gerilim kaynağından oluşur.Bu modelde, eşdeğer çıkış kapasitesi,seri olarak birbirine bağlanmış olan eşdeğer çıkış direnci ve doyma gerilim kaynağı ile paralel bağlı olarak düşünülmüştür.Bipolar tranzistor için geliştirilen bu model kollektör emetör doyma gerilimi dışında VVMOS tranzistor modelinin çıkış kısmı olarak da kullanılmıştır.VVMOS tranzistor modelinin giriş kısmı ise sadece tranzistorun kapı ve kaynak terminalleri arasındaki giriş kapasitesinden oluşmuştur.İlgili model parametreleri herbir tranzistor için ayrı ayrı belirlenmiştir.

Bipolar tranzistorlar için geliştirilen yeni modelin eşdeğer çıkış direnç ve kapasitesi sadece geçiş bölgelerinde üstel fonksiyon şeklinde değiştirilmiş diğer bölgelerde sabit olarak düşünülmüştür.

VVMOS tranzistor modelinde eşdeğer çıkış direnci direnç ve geçiş bölgelerinde giriş geriliminin bir fonksiyonu olarak düşünülmüştür.Kesimde ise eşdeger çıkış direnci maksimum tranzistor savak-kaynak direncine eşit olan sabit bir değer olarak alınmıştır.Eşdeğer

Çıkış kapasitesi ise tüm bölgelerde çıkış geriliminin bir fonksiyonu olarak ifade edilmiştir.

VVMOS tranzistorlar için geliştirilen model VDMOS tranzistorların modellenmesinde de kullanılabilir.Bunun için gerekli formül ve açıklamalar ile model parametrelerinin elde edilmesi bu tezin konuları arasındadır.

Uygulama olarak tranzistorlu üç temel anahtarlama devresi olan rezistif,rezistif-indüktif,rezistif-indüktif-kapasitif yüklü anahtarlama devrelerinin ve CVDMOS eviricinin analizleri bu model yardımı ile yapılmıştır.Modelin doğruluğu,yüksek hızlı anahtarlama devreleri üzerinde ölçmeyle ve teorik olarak da bilgisayar çalışması sonucu elde edilen anahtarlama karekteristiklerinin teferruatlı bir mukayesesi ile incelenmiştir.

Tranzistorlu anahtarlama devrelerinin çalışmasını açıklamak ve göstermek için geliştirilen bu model şimdiye kadar yapılan modeller içinde basitlik,doğruluk,parametre verme kolaylığı ve devre analizlerinde daha az bilgisayar zamanı gerektirmesi gibi hususların en iyi birleşimini sağlayan bir model olarak düşünülebilir.

TABLE OF CONTENTS

LIST OF FIGURES

Page

LIST OF TABLES

LIST OF SYMBOLS

A	Total area of VVMOST within groove
C	Bipolar transistor collector to emitter time-variant non-linear capacitance
Cl	Load capacitance
C_{DS}	Drain to source junction capacitance
C_{DSO}	Drain to source junction capacitance at $V_{DS}=0$
C_{GD}	Gate to drain capacitance
C_{GS}	Gate to source capacitance
C_{IN}	MOS transistor input capacitance
C_{MAX}	Maximum value of collector to emitter time-variant non-linear capacitance
C_{MIN}	Minimum value of collector to emitter time-variant non-linear capacitance
C_P	Stray capacitance for VDMOSTs
DELT	Timing interval
E_{OFF}	Low value of the square wave applied to the input of the switching circuit
E_{ON}	High value of the square wave applied to the input of the switching circuit
F	Ringing frequency
H	Grading coefficient $0.3 \leqslant H \leqslant 0.5$
I_D	Load current for MOS transistors
I_G	Gate current
I_L	Load current for bipolar transistors
I_{Ol}	Initial condition of load inductance
Ll	Load inductance
R	Bipolar transistor collector to emitter time-variant non-linear resistance

RI	Load resistance
R_B	Bipolar transistor base to emitter time-variant non-linear resistance
R_{BT}	Series combination of base spreading resistance and external base resistance
R_D	Drain resistance
R_{DS}	Drain to source time-variant non-linear resistance
R_{DSMAX}	Maximum value of the drain to source time-variant non-linear resistance
R_G	Gate resistance
R_I	Input voltage source impedance in MOS switching circuit
R_{MAX}	Maximum value of collector to emitter time-variant non-linear resistance
R_{MIN}	Minimum value of collector to emitter time-variant non-linear resistance
R_N	N(-) drift layer resistance in VVMOST
R_S	Source resistance
tdoff	Turn-off delay time
tdon	Turn-on delay time
tf	Fall time
T_{OFF}	Off time
T_{ON}	On time
tr	Rise time
troff	Turn-off transient time
tron	Turn-on transient time
T_S	Storage time
TT	Operating period
V_{BE}	Base to emitter output voltage
V_{CC}	Supply voltage for BJT switching circuits

V_{CES}	Collector to emitter saturation voltage
V_{DD}	Supply voltage for MOS transistor switching circuits
V_{DS}	Drain to source voltage
V_G	Cut-in voltage of bipolar transistors
V_{GS}	Gate to source voltage
V_O	Output voltage
V_{O1}	Initial voltage across the collector to emitter or drain to source time-variant non-linear capacitance by depending on the type of the switching circuit to be used
V_{O2}	Initial voltage across the load capacitance
V_T	Threshold voltage of MOS transistors
XN	Total number of steps
Za	VVMOS area occupied by the grooves at the P-N(-) interface
β	Constant related to MOS transistor
ϕ	Transistor junction potential

I. INTRODUCTION

Most transistor models are aimed either toward portraying the interaction of the device with an external circuit or toward relating device behavior to device physics,and most models involve some degree of approximation.In the former case,the primary interest is the specification of performance;just as it is sometimes convenient to use only the two-port parameters of an electric network to describe its terminal behavior,so it is sometimes convenient to prescribe a particular set of terminal measurements as parameters which characterize transistor behavior.In the latter case,the primary concern is the analysis of device behavior in terms of physical processes.Either case,when carried to its extreme,is unsatisfactory from a model point of view.On one hand,the terminal properties,while conveniently measured, do not themselves elucidate the reasons for device behavior.On the other hand,consideration of physical processes alone generally leads to cumbersome results which obscure dominant tendencies and inhibit qualitative interpretation of the relationship between processes and terminal behavior.

An ideal model may be regarded as one which

1) involves parameters which maintain a one-to-one correspondence with physical processes.
2) lends itself well to analysis of circuit problems.
3) involves a degree of approximation sufficient to enhance qualitative understanding and interpretation while maintaining reasonable quantitative accuracy.
4) cuts computer costs with sufficient accuracy for practical application.

Large-signal models for transistors are necessary tools for the device engineer,who must specify device performance,and the circuit designer,who must be equipped for both the analysis and design of transistor circuits.Over the past few years,a number of models have been proposed.The non-linear models which have received the most attention are the Linvill lumped model(1),the Beaufoy-Sparkes charge-control model(2),and the Ebers-Moll model (3),(4),(5).

The classical method of analyzing high-power high-frequency transistor performance is to use the hybrid-Π model.To date,this model has been the most popular high-frequency equivalent circuit for a junction transistor.Because this model does not include a collector-base diode,it can accurately represent operation in the ACTIVE region,but not in the ON and OFF regions.

Although each of the hybrid-Π model parameters varies with instantaneous signal level and time,they are normally assumed to have fixed values which are a function of the average level of operation.With a judicious selection of parameter values,this model can be adjusted to predict small and even medium signal performance quite well over wide frequency ranges.It does not predict very well the characteristics of a transistor driven heavily into saturation. That's why a linear model more complete than the hybrid-Π type is necessary to represent and explain the operation of transistor switching circuit.

The purpose of this thesis is to apply a time-variant linear large-signal transistor model (15) to the bipolar transistors and VVMOS-or VDMOS-transistors,to analyse basic three transistor switching circuits by using the related model,and to compare the results of analysis with the experimentel results.

In the second chapter the new linear large-signal transistor

model is introduced.At the beginning a genaral information is given about the non-linear models.Then the Ebers-Moll model is preferred as a favorite model within non-linear models .But high-computer costs are seen as a disadvantage in the Ebers-Moll model.The new linear model which is more simple than the Ebers-Moll model is developed and it is considered as a linearized version of the Ebers-Moll model.This model is proposed separately for the bipolar and VVMOS-or VDMOS-transistors.After the model is presented,the necessary formulas and explanations for the related model parameters are given separately for each one of the transistors.

In the third chapter basic transistor switching circuits and their characteristics are explained and the analysis of all the switching circuits are made.For each one of the BJTs and VVMOST-or VDMOS-switching circuits only one analysis is made because they have the similar equivalent linear circuits when the proposed model is used instead of the related transistor.Then,as an application of the proposed VVMOST-or VDMOS-model,the analysis of a CVDMOS inverter is made.At the end of the chapter,for all the analyses, the related flowcharts are given.A general idea for the preparation of computer programs is also given.

The last chapter is devoted to the experimental studies. Profitting by the related references and the measurement techniques, the values of the parameters required to characterise the model are conveniently obtained.The application of the proposed time-variant linear large-signal model to the basic transistor switching circuits to compute transient switching characteristics is illustrated and the accuracy of the model is evaluated by a detailed comparison of computer simulations with experimental switching waveforms.

II. DESCRIPTION OF TIME-VARIANT LINEAR LARGE-SIGNAL TRANSISTOR MODELS AND THEIR PARAMETERS

Transistor models are tools which are used to facilitate the optimization of transistor design and performance.The degree of complexity of a model is always a compromise between accurate device representation and ease of analysis.Relatively simple linear models have traditionally been used to characterize high-frequency transistors with excellent results for low-signal levels.At large-signal levels,however,a transistor exhibits significant effects which can not be analyzed by means of the simpler models.These effects are generally caused by harmonic components of the voltages and currents generated by non-linear mechanisms within the transistor. To date, many large-signal non-linear models have been used to represent these mechanism.A general information is to be given about the non-linear large-signal models at the beginning in this chapter.

Our main interest in this chapter is to represent a new time-variant linear large-signal transistor model which provides an optimum combination of accuracy,ease of parameter acquisition and simplicity,(15).After developement of the model which is constructed for the bipolar and VVMOS-or VDMOS-transistors,parameter evaluation for this model is presented.

2.1. General Review to Non-Linear Models for Bipolar Transistors

Of the many large-signal models which have been proposed for the bipolar transistors,three have received the most attention. These are the Linville lumped model(1),the Beaufoy-Sparkes charge-control model (2),and the Ebers-Moll model (3),(4),(5).Each represents a different approach to solution of the relations describing the

distributed base region of a diffused transistor.

The Linville lumped model is obtained by solution of the continuity equation for current carriers at finite intervals in the base.The form of the solution leads naturally to a set of lumped elements which can be treated as a network.The accuracy of the representation depends on the number of sections into which the base is divided.Of the three models,this type provides the most accurate physical description of the transistor.The resulting representation,however,is quite cumbersome to analyse,(1).

The charge-control model focuses upon the relationship between the terminal currents and minority-carrier stored charge.The resulting equations can be represented by circuit elements.Although the elements are not the conventional type,they can be used in a circuit analysis,(2).

The Ebers-Moll model is based upon the concept of superimposing normal and inverse transistors in which the collector-base and emitter-base junctions are represented by diodes shunted with capacitors.This model is the easiest of the three types to use because it can be represented by conventional circuit elements. The biggest shortcoming of the model is that it does not accurately include the effect of the carrier storage.However,the errors incurred by this lack depend upon the frequency of operation,(3),(4),(5).

When these three models are to be compared with each other, the Ebers-Moll model is preferred as a favorite model because

1) its elements have meaning as a result of familiarity;
2) there is some easy way of getting data for the elements;
3) temperature changes and aging can be easily accounted in the model;
4) from past experience the model has given satisfied results;

5) the model provides insight to what is going on,(6).

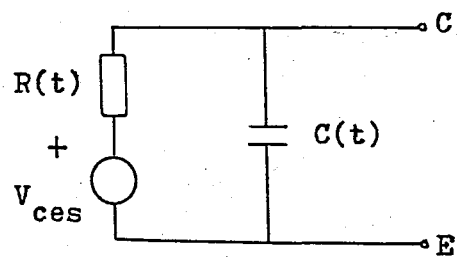
The Ebers-Moll model is explained in detail in Appendix A.

It must be further emphasized that a non-linear model such as the Ebers-Moll model is not always the best choice for large-signal problems,too.Far simpler linear time-variant large-signal models may cut computer costs with sufficient accuracy.For this purpose a new time-variant linear transistor model is developed to represent and explain the operation of transistor switching circuits,(15).

2.2. A Time-Variant Linear Large-Signal Modeling of Bipolar Transistors

A time-variant linear large-signal model for the bipolar transistors is developed in this section.This model,basically, includes the time-variant equivalent output resistance and capacitance and the D.C. voltage source which represents the transistor saturation voltage.In this model the equivalent output capacitance is connected in parallel with the equivalent output resistance and the D.C. voltage source which are connected in series with one another.The complete model is shown in Figure(2.1).

The equivalent output resistance and capacitance of this model are taken as a constant value in the cut-off and saturation regions. They are changed only in the transient regions.For determining the variations of the output resistance and capacitance versus time, their time-variant functions must be determined at the beginning. By means of the experimantal studies it is seen that if their variations versus time are taken as an exponential function the load current and output voltage waveforms which are closer to the real waveforms are obtained.The variations versus time of the output resistance and capacitance are shown in Figures(2.2.a) and (2.2.b), respectively.



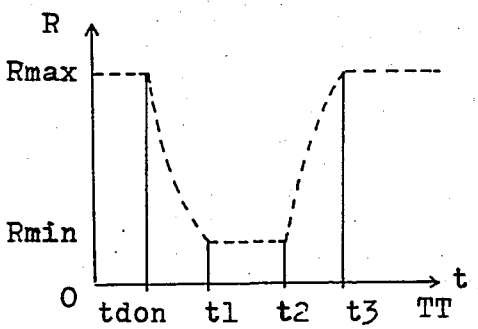
FIGURE(2.1) The new time-variant linear large-signal model for BJTs

In this model the number of calculating points within one period is considered as XN.One-step value within the timing range of one period is defined as

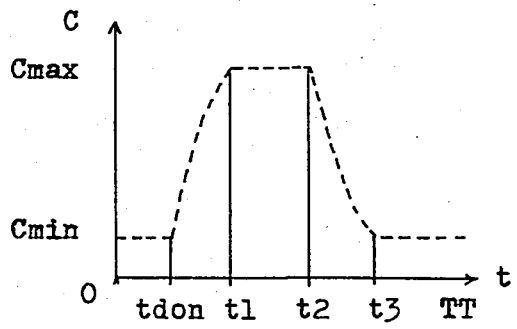
$$DELT = TT/XN \qquad (2.2.1)$$

where TT is the operating period.

In the turn-on and turn-off transient regions,the numbers of the equivalent output resistance and capacitance to be changed are considered,respectively,as



(a)



(b)

FIGURE(2.2) a) Variation of the BJT output resistance versus time
b) Variation of the BJT output capacitance versus time

$$XN1 = XN.(tron/TT) \qquad (2.2.2)$$

and

$$XN2 = XN.(troff/TT) \qquad (2.2.3)$$

where tron and troff are the rise and fall times for the load current, respectively.

In the consideration of the junction transistor as a switch the calculations must be made for five regions,separately.These regions can be defined as the turn-on delay region ,the turn-on transient region,the saturation region,the turn-off transient region,and the cut-off region.

For the turn-on delay and cut-off regions,the values of the equivalent output resistance and capacitance are Rmax and Cmin, respectively.Their time-variant functions in the turn-on transient regions are expressed as

$$R(t) = Rmax.e^{[((t-tdon)/tron).ln(Rmin/Rmax)]} \qquad (2.2.4)$$

and

$$C(t) = Cmin.e^{[((t-tdon)/tron).ln(Cmax/Cmin)]} \qquad (2.2.5)$$

where tdon is the turn-on delay time.

In the saturation regions,the output resistance and capacitance have the constant values of Rmin and Cmax.In the turn-off transient region their time-variant functions are given by

$$R(t) = Rmin.e^{[((t-t2)/troff).ln(Rmax/Rmin)]} \qquad (2.2.6)$$

and

$$C(t) = Cmax.e^{[((t-t2)/troff).ln(Cmin/Cmax)]} \qquad (2.2.7)$$

where t2 is the time passing up to the beginning of the turn-off transient.

2.3. Description of BJT Model Parameters

For using the proposed time-variant linear transistor model in the analysis of BJT switching circuits the model parameters must be determined at the beginning. The model parameters are the switching times, the off impedance and the on impedance of the transistor. For determining the model parameters, the parameters of

a) the forward common-emitter large-signal current gain, β_F,

b) the inverse common-emitter large-signal current gain, β_R,

c) the transistor saturation current, Is,

d) the temperature at which the parameters are obtained, Tnom,

e) the emitter ohmic resistance, R_{EE},

f) the collector ohmic resistance, R_{CC},

g) the base ohmic resistance, R_{BB},

h) the emitter-base junction capacitance at $V_{BE} = 0$, CjeO,

i) the collector-base junction capacitance at $V_{BC} = 0$, CjcO,

j) the emitter-base barrier potential, V_{ZE},

k) the collector-base barrier potential, V_{ZC},

l) the emitter-base capacitance gradient factor, N_E,

m) the collector-base capacitance gradient factor, N_C,

n) the normal-mode intrinsic gain-bandwidth product, Fn,

o) the inverted-mode intrinsic gain-bandwidth product, Fı,

p) the emitter-base junction ohmic leakage resistance, R_E,

q) the collector-base junction ohmic leakage resistance, R_C,

r) the emission constant for emitter-base diode, M_E,

s) the emission constant for collector-base diode, M_C,

must be determined at the beginning.The measurement techniques for obtaining these 19 transistor parameters are given in the related references(5),(7).Useful formulas and necessary explanations are to be given in detail in the following subsections.

2.3.1. Theoretical Explanations and Formulas for Switching Times

The time required to change the operating point of a junction transistor from the cut-off to the saturation,or vice-versa,is clearly of primary importance.It is the purpose of this section to show how switching-time is related to transistor parameters and circuit conditions.The switching time is easily calculated in terms of the normal active-region parameters of the transistor.Large-signal switching time includes the turn-on and turn-off times to be used as the model parameters.

a. Turn-on Time

When an input pulse (forward bias to emitter-base junction) is applied to a practical transistor switch,the transistor can not turn-on in zero time.Turn-on time is the time required for the collector current to change to 90 per cent of its saturated value. The turn-on time is made up of two parts.

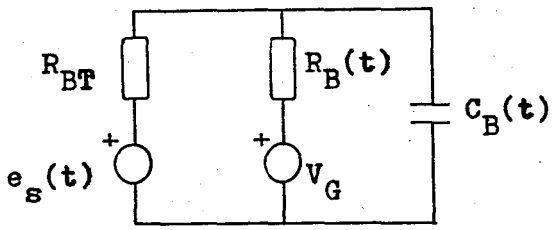
(1). The Delay Time

The delay time is the time required for the collector current to change to its 10 per cent of its saturated value.

When the transistor is switched from the OFF condition to ON condition,the emitter-base junction voltage must change from an applied reverse-bias voltage,$V_{BE}(off)$,to the forward voltage,V_{BE}, associated with the forward current being switched.The charge

associated with the emitter depletion layer and corresponding to a change in emitter-base voltage affects the response time of the transistor.In particular,emitter-base transition capacitance gives rise to an additional response time(8).

For determining the delay time,tdon,a linear model of the input side of the bipolar transistor is developed and it is shown in Figure(2.3).In this model,$R_B(t)$ and $C_B(t)$ represent the base to emitter non-linear resistance and capacitance.R_{BT} is the series combination of the base resistance,R_B,and the base ohmic resistance, RBB.$e_s(t)$ is used for representing the input sqare-wave generator. V_G is the base to emitter cut-in voltage.



FIGURE(2.3) Linear model developed for the input side of BJTs

For the turn-on delay region,the model parameters can be expressed as

$$R_B(t)=R_{Bmax} \qquad (2.3.1)$$

$$C_B(t)=C_{Bmin} \qquad (2.3.2)$$

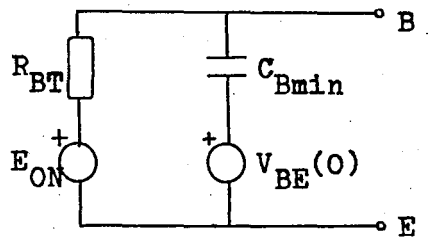
$$R_{BT} = R_B+R_{BB} \qquad (2.3.3)$$

and

$$e_s(t)=E_{ON} \qquad (2.3.4)$$

where E_{ON} is the positive value of the input square wave,R_{Bmax} is

the maximum value of the base to emitter time-variant resistance and C_{Bmin} is the minimum value of the base to emitter time-variant capacitance.The model shown in Figure(2.3) can be redrawn for the turn-on delay region and the base to emitter voltage can be



FIGURE(2.4) Equivalent circuit to be used in the calculation of tdon

calculated by means of this new model.The expression of the base to emitter voltage can be written as

$$V_{BE}=\left[E_{ON}-V_{BE}(0)\right].\left[1-\exp(-DELT/(R_{BT}.C_{Bmin}))\right]+V_{BE}(0) \qquad (2.3.5)$$

The calculation of V_{BE} must be repetead with the time intervals of DELT.Each time this equation is to be solved with the result of the previous calculation taken as the initial condition.The time which V_{BE} is equal to the cut-in voltage,V_G,is defined as the turn-on delay time,tdon.

(2). <u>The Rise Time</u>

The rise time,tron,is the time required for the load current to increase from 10 per cent of the saturated load current,I_L,to 90 per cent of I_L.It can be saturated as (3),(4)

$$tron=\frac{1}{\omega_N.(1-\alpha_N)}.\ln\left[\frac{1-0.1(Ic/Ib).(1-\alpha_N)/\alpha_N}{1-0.9(Ic/Ib).(1-\alpha_N)/\alpha_N}\right] \qquad (2.3.6)$$

where I_b is the base current after step is applied, I_C is the collector current at the edge of saturation region, α_N is the current gain, and ω_N is the cut-off frequency.

Turn-on time clearly depends on the amount of drive, current gain, and frequency response of the transistor.

b. Turn-off Time

The turn-off transient from the saturation region to the cut-off region differs materially from the turn-on transient in that the junction transistor suffers from carrier storage.

The succession of events during the turn-off transient (at the end of pulse) may be described as follows:

The base current is reduced from a value corresponding to operation in the saturation region to zero, or possibly to a reverse emitter-junction current. The excess carrier density in the base layer decays until the minority carrier density in the base layer at the collector junction reaches nearly zero. During this initial stage of the turn-off transient, the collector junction is a low impedance and the collector current remains very nearly constant, at a value determined by the external circuit resistance. When the minority carrier density in the base layer at the collector approaches zero, the collector junction rapidly becomes a high impedance. The turn-off transient, after the collector junction has recovered, is controlled by the normal active region parameters. We see that for junction transistors the turn-off transient can be conveniently divided into two times.

(1). The Storage Time

Storage time is the time interval between the reduction of

base current to a zero,or reverse value,and the active response of the collector current.Storage time has been related to transistor parameters and circuit conditions from the fundamental considerations. The saturation delay time is given by (7),(9),(10)

$$T_S = \tau_{sat} \cdot \ln \frac{I_{BF}+I_{BR}}{I_{CF}/B_F+I_{BR}} \qquad (2.3.7)$$

where I_{BF} is the forward base current,I_{BR} is the reverse base current, I_{CF} is the forward collector current and τ_{sat} is the saturation delay time constant. τ_{sat} can be determined easily with a measurement technique which is explained in the reference (7).

(2). Fall Time

The fall time is the time between the decrease of the load current,I_L,from 90 per cent of I_L(sat) to 10 per cent of I_L(sat) is

$$t_{roff} = \frac{1}{\omega_N \cdot (1-\alpha_N)} \cdot \ln \left[\frac{0.9I_{C1}-(\alpha_N \cdot I_{BR})/(1-\alpha_N)}{0.1I_{C1}-(\alpha_N \cdot I_{BR})/(1-\alpha_N)} \right] \qquad (2.3.8)$$

where I_{C1} is the initial collector current.

As shown in Figure(2.2),all the switching times to be used in the analyses of switching circuits can be defined as

$$t1 = t_{don}+t_{ron} \qquad (2.3.9)$$

$$t2 = TT/2+Ts \qquad (2.3.10)$$

$$t3 = t2+t_{roff} \qquad (2.3.11)$$

respectively.

2.3.2. Determination of Saturation Voltage and On and Off Impedances of Bipolar Transistors

The voltage drop between collector and emitter in the saturation region can be written as (7),(11)

$$V_{CE} = \frac{k.T}{q} \ln \frac{\alpha_I(1-I_C.(1-\alpha_N)/I_B.\alpha_N)}{1+I_C/I_B.(1-\alpha_I)} + I_E.R_{EE} + I_C.R_{CC} \quad (2.3.12)$$

As the model parameters,the value of V_{CES} can be obtained from Eq. (2.3.12) by neglecting the voltage drop on the emitter and collector ohmic resistances(3),(11)

$$V_{CES} = \frac{k.T}{q}.\ln \frac{\alpha_I(1-I_C.(1-\alpha_N)/I_B.\alpha_N)}{1+I_C/I_B.(1-\alpha_I)} \quad (2.3.13)$$

In this equation,since $k.T/q = 0.0026$ volt at room temperature this voltage can be as low as a few millivolts.As the collector current approaches $\beta_N.I_B$,this voltage approaches infinity,and the transistor goes from the saturation region into the transient region.

For determining the ON and OFF impedances,or Rmin,Rmax,Cmin, and Cmax,the A.C. impedance of the collector region in the closed condition,the emitter-base and collector-base junction ohmic leakage resistances,and the emitter-base and collector-base junction and diffusion capacitances must be determined.

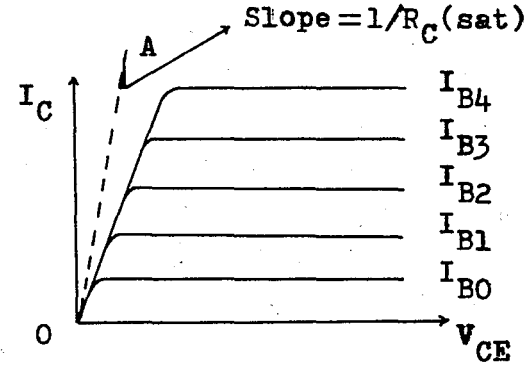
The A.C. impedance in the collector circuit in the closed condition can be obtained from both of Eq. (2.3.12) and the related measurement technique together.It is given by (7)

$$R_C(Sat) = \frac{1}{\text{Slope A}} - (1+1/B_F)R_{EE} - \frac{k.T}{q}\left[1/(B_F.I_B-I_C) + a\right] \quad (2.3.14)$$

where

$$a = 1/((1+B_R).I_B+I_C) \qquad (2.3.15)$$

In this expression a correction is taken into account the effects of R_{EE} and the finite slope in the I_C versus V_{CE} characteristics



FIGURE(2.5) Typical I_C versus V_{CE} characteristics at constant I_B

in the saturation region,Figure(2.5).Minimum equivalent output resistance or ON resistance can be expressed as(12)

$$R_{MIN} = R_C(sat)+R_{CC}+R_{EE} \qquad (2.3.16)$$

For determining the maximum equivalent output resistance we can use the related common emitter hybrid parameter,hoe,

$$R_{MAX} = 1/hoe \qquad (2.3.17)$$

or if the base current were set to zero,the collector current which remains flowing through the transistor in the OFF state would be

$$I_C = I_{CO}/(1-\alpha_N) = I_{CS}(1-\alpha_N.\alpha_I)/(1-\alpha_N) \qquad (2.3.18)$$

and

$$R_{MAX}=V_{CC}(1-\alpha_N)/I_{CS}\cdot(1-\alpha_N\cdot\alpha_I) \qquad (2.3.19)$$

There are two types of capacitances associated with the p-n junction. They are the junction and diffusion capacitances.The junction capacitance occurs as a consequence of the variation in the width of the depletion layer in a reverse -biased junction.An increase in reverse-bias causes majority carriers to move away from the junction and uncover fixed charges.This action causes a widening of the depletion region and because the charges moved from the depletion region must be pulled out of the diode terminals by the voltage source,the effect is that of a voltage variable capacitance.

The emitter-base and collector-base junction capacitances are expressed in the following expressions as (7),(13),(14)

$$C_{JE}=\frac{C_{JEO}}{(1-V_{EB}/V_{ZE})^{Ne}} \qquad (2.3.20)$$

and

$$C_{JC}=\frac{C_{JCO}}{(1-V_{BC}/V_{ZC})^{Nc}} \qquad (2.3.21)$$

where V_{EB} and V_{BC} are the junction voltages (negative),V_{ZE} and V_{ZC} are contact potentials,and Ne and Nc are junction grading constants.

The diffusion capacitance exists across a forward-biased junction. The following expressions for the emitter-base diffusion capacitance C_{DE},and the base-collector diffusion capacitance,C_{DC} can be written as(5), (7)

$$C_{DE}=\frac{q}{2.\pi.M_E.k.T.Fn}\cdot\left[I_{EF}+(I_{ES}/(1-\alpha_N\cdot\alpha_I))\right] \qquad (2.3.22)$$

and

$$C_{DC}=\frac{q}{2.\pi.M_C.k.T.Fi}\cdot\left[I_{CF}-(I_{CS}/(1-\alpha_N\cdot\alpha_I))\right] \qquad (2.3.23)$$

where

$$I_{EF}=(I_{ES}/(1-\alpha_N\cdot\alpha_I)\cdot\left[\exp(q\cdot V_{EB}/M_E\cdot k\cdot T)-1\right] \qquad (2.3.24)$$

$$I_{CF}=(I_{CS}/(1-\alpha_N\cdot\alpha_I)\cdot\left[\exp(q\cdot V_{BC}/M_C\cdot k\cdot T)-1\right] \qquad (2.3.25)$$

$$Is=\alpha_I\cdot I_{CS}=\alpha_N\cdot I_{ES} \qquad (2.3.26)$$

and Fn and Fi are the normal and inverted-mode gain-bandwidth products of the intrinsic transistor.

In the cut-off region the equivalent output capacitance can be taken as a value which is equal to the value of the collector to base junction capacitance for $V_{BC}=-V_{Cav}$.Because no current flows through the junction and we can not speak of the existence of the diffusion capacitance.Here the value of V_{Cav} is considered as the average value of the output voltage for an half period (15).The value of the output capacitance in the cut-off region is defined as the minimum equivalent output capacitance and it is given by

$$C_{MIN}=\frac{C_{JCO}}{(1+V_{Cav}/V_{ZC})^{Nc}} \qquad (2.3.27)$$

For the saturation region the equivalent output capacitance is taken as the additions of the values of the emitter-base junction for $V_{BE}=V_{BE}(sat)$ and the collector-base diffusion capacitance for $I_{CF}=I_{Cav}$. The value of I_{Cav} is considered as the average value of the load current for an half period.As a result the value of the output equivalent capacitance is defined as the maximum equivalent output capacitance and it is equal to

$$C_{MAX}=\frac{C_{JEO}}{(1+V_{BE}(sat)/V_{ZE})^{Ne}}+\frac{q}{2.\Pi.Mc.k.T.Fi}\cdot\left[I_{Cav}-(I_{CS}/(1-\alpha_N\cdot\alpha_I))\right] \qquad (2.3.28)$$

2.4. General Review to VVMOS Transistors

Vertical V-groove Metal Oxide Semiconductor Field Effect Transistors (VVMOSTs) uniquely combine the advantages of the power bipolar transistors with those of the MOSFETs.The result is a high power,high-voltage,high-gain power transistor with no minority-carrier storage time,no thermal runaway and a greatly inhibited secondary breakdown characteristic,all of which are contributing to the spectacular rise in the popularity of the VMOS power FET (16)

The vertical VMOS structure,like the power bipolar transistor, offers a large surface area for source metal and the entre backside of the chip for the drain.This is of great importance as it allows maximum current carrying capacity unavailable to a nonvertical structure.

Operationally,VVMOST is unique among power transistors.Channel conduction is proportional to gate voltage,not to any sort of injection current,typical of the bipolar transistor.Whatever input current that does exist beyond that attributed to leakage may be identified as the charging current necessary to overcome the input capacitance in very high-speed switching situations.Because the stea state gate current negligible,the familiar parameter,beta,is of litt importance.Consequently,VMOS exhibits a high input resistance that makes it ideal for many logic control applications.

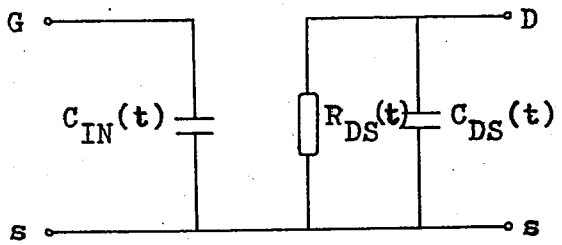
In the consideration of VVMOS transistor as a switch the calculations must be made for the five regions,separately.These regions can be defined as the turn-on delay region,the pinch-off region (off to on),the resistive region,the pinch-off region (on to off),and the cut-off region,respectively.For the turn-on delay and cut-off regions V_{GS} is below threshold,($V_{GS} < V_T$),and the VVMOST is

OFF.In the pinch-off region as V_{GS} exceeds V_T drain current begins to increase until V_{DS} saturation is reached,or $V_{GS}-V_T \geqslant V_{DS}$.In the resistive region V_{DS} is saturated and no further change in I_D or V_{DS} occurs.

Useful explanations and the comparison of VVMOS transistors with the other transistors are given in Appendix B.A time-variant linear large-signal model for the VVMOS transistors is to be developed in the following section and the related model parameters and useful formulas according to them are given in section(2.6).

2.5. A Time-Variant Linear Modeling of VVMOS Transistors for Switching Circuits

A time-variant linear large-signal model for the VVMOS transistor is developed in this section.This model,basically,is similar to the



FIGURE(2.6) A time-variant linear large-signal model for VVMOSTs

proposed new BJT model.This model includes an equivalent input capacitance between the gate and source for the input side and the parallel combination of the equivalent output resistance and capacitance for the output side.The complete model is shown in Figure(2.6).

The input side of this model consists of a FET equivalent time-variant input capacitance,C_{IN},only,that's why the D.C. input resistance of a VVMOS power FET is in excess of 10^{12} ohms.

The output side includes a time-variant drain to source resistance and capacitance.For the turn-on delay and cut-off regions the equivalent output resistance,or drain to source resistance,is considered as a constant value which is equal to the maximum drain to source resistance,R_{DMAX}.In the pinch-off and resistive regions this resistance is a function of the input voltage.The equivalent output capacitance,or drain to source capacitance,is a function of the output voltage for all regions in the VVMOS transistors.

For using this model in the analysis of the switching circuits, the VVMOS transistor model parameters must be determined at the beginning.Beyond the structural parameters,all the parameters can be obtained from the related DATA SHEETs.The structural parameters and related model parameters are explained in detail in the following section.

2.6. Description of VVMOST Model Parameters

For the VVMOST model to be used in the switching applications a careful analysis of the VVMOST switching parameters is required. The related switching parameters are the ON-resistance,OFF-resistance, PINCH-OFF resistance and the device capacitances.Necessary explanations for obtaining the switching times are given at the end of this section.

2.6.1. ON-Resistance

At low drain voltage and large-currents,the N^- layer acts as a simple resistance in series with the drain of a conventional MOST. The resistance of the N^- layer is (17)

$$R_{N^-} = \frac{2.g_{n^-}}{\pi.z} \cdot \ln \frac{4.d}{\pi.a} \qquad (2.6.1)$$

where g_{n^-} is the N^- layer resistivity,z is the total channel width

of the device,d is the thickness of the N^- layer,and a is the half of the groove opening at the P-N^- interface.

The total ON-resistance of the VVMOST is made up of the series combination of the channel resistance R_C,the N^- drift layer resistance R_{N^-},and the N^+ source and drain resistances as well as the metallization resistance.The channel and N^- region resistances are the dominant resistances to the ON resistance,$R_{DS}(ON)$,which can be expressed as (17),(18)

$$R_{DS}(ON) = R_C + R_{N^-} \tag{2.6.2}$$

$$= 1/\beta.(V_{GS}-V_T)^{-1} + R_{N^-} \tag{2.6.3}$$

where

$$\beta^{-1} = \frac{L}{\mu.C_0.z} \tag{2.6.4}$$

is a constant,L is the channel length in the VVMOS device,μ is the surface channel mobility,C_0 is the effective gate oxide capacitance per unit area.

2.6.2. OFF-Resistance

For the turn-on delay and the cut-off regions the maximum drain to source resistance can be calculated by using the related transistor parameters,the zero gate voltage drain current,I_{DSS},and the maximum drain source voltage,V_{DSMAX}.The expression for the maximum drain to source resistance is given by

$$R_{DSMAX} = V_{DSMAX}/I_{DSS} \tag{2.6.5}$$

2.6.3. PINCH-OFF Resistance

In the pinch-off regions,an internal transconductance that

initially rises with V_{GS} but eventually saturates at a constant maximum value can be written as

$$g_{mi} = 1/V_{DS} \cdot \beta \cdot (V_{GS} - V_T)^2 \qquad (2.6.6)$$

The presence of R_N^- and R_S results in the external pinch-off transconductance, g_m being reduced from its internal value. The drain to source resistance for this region can be written by using the external transconductance as

$$R_{DS} = \frac{V_{DS}}{\beta \cdot (V_{GS} - V_T)^2} + R_N^- \qquad (2.6.7)$$

2.6.4. Device Capacitances

Several capacitances affect the high-frequency and switching characteristics of the VVMOST. Figure(2.7) shows these capacitances schematically on the cross section of the VVMOST. C_{GS} and C_{GD} are MOS capacitances and C_{DS} is a junction capacitance.

An approximate expression for the maximum input capacitance of the VVMOST (neglecting overlap metallization on the planar non-grooved regions of the device and space-charge capacitance under gate oxide) is (17)

$$C_{IN} \cong C_O \cdot (1.23 \cdot Y_G \cdot 0.707) \cdot z \qquad (2.6.8)$$

$$\cong 0.86 C_O Y_G z \qquad (2.6.9)$$

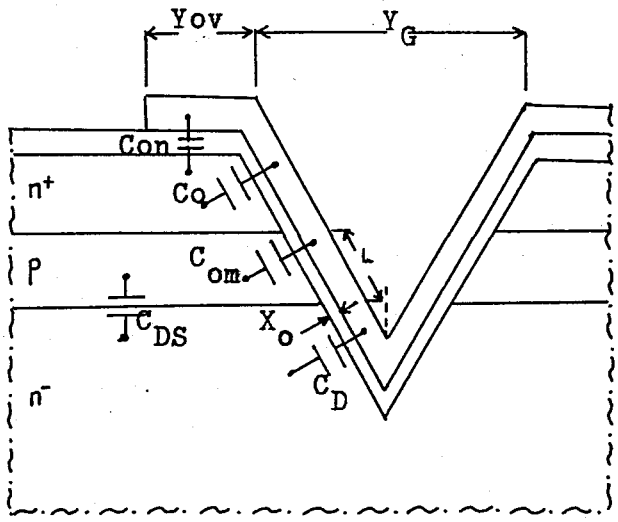
where Y_G is the length of the groove opening. To minimize the input capacitance Y_G must be kept as small as possible.

More accurate expressions for the individual capacitances including overlap and space-charge capacitances can be obtained from the geometry of the device. The gate to source capacitance is

made up of three components:a capacitance associated with gate overlap over the N source on the surface,and a gate to bulk capacitance component.The gate to source capacitance can be expressed as (17)

$$C_{GS} = 1.23 \cdot C_O \cdot X_N \cdot z + C_{on} \cdot Y_{ov} \cdot z + C_{om} \cdot L \cdot z \qquad (2.6.10)$$

where C_{on} is the capacitance per unit area of the field oxide over



FIGURE(2.7) Capacitances associated with the VVMOST structure

the N^+source,C_{om} is the voltage variable MOS capacitance of the channel region,Y_{ov} is the gate metallization overlap over the field oxide, and X_N is the source diffusion depth.In order to reduce C_{GS},the overlap capacitance component must be minimized.

The gate to drain capacitance at zero drain voltage is given by (17)

$$C_{GD} = 1.23 \cdot C_O (0.707 \cdot Y_G - X_P) \cdot z \qquad (2.6.11)$$

Since this capacitance is directly over the accumulated N^-region,

little variation in C_{GD} with gate voltage is expected.However,at higher drain voltages the increasing space-charge region in the N^- layer causes a reduction in this capacitance.In order to minimize C_{GD},the effective penetration of the groove into the N layer must be minimized.

The drain to source capacitance is given by (17)

$$C_{DS} = C_d.(A-Za) \qquad (2.6.12)$$

where C_d is the voltage variable space-charge region capacitance per unit area associated with the P-N^- junction,A is the total area of the device within groove ,and Za is the area occupied by the grooves at the P-N^- interface.To minimize C_{DS},C_d must be made as small as possible by using a high resistivity N^- region (17).The expression of C_d is given by

$$C_d = C_{DSO}.(1+V_{DS}/\phi)^{-H} \qquad (2.6.13)$$

where C_{DSO} is the junction capacitance at $V_{DS}= 0$,H is the grading coefficient $0.3<H<0.5$,ϕ is the junction potential (18).

The VVMOST equivalent input capacitance,C_{IN},is a function of V_{GS} and V_{GD}.In the switching applications,it changes during transition from the ON state to the OFF state or vice versa.Typically the capacity characteristics specified on the related data sheet are given for a fixed bias condition.This may present a problem in trying to estimate C_{IN}.

Driving VVMOS from logic requires an appreciation of the gate drive power needed to actuate,or turn-on,the VVMOS power transistor. First,the driver must be able to deliver sufficient current during the transition (from OFF to ON) to adequately charge the input capacitor in the desired time.As the driving voltage ramps upward

another phenomenon occurs called MILLER EFFECT.Once the threshold voltage of the VVMOS transistor is passed it begins to draw increasingly heavier drain current.As the drain current rises rapidly to saturation.Concurrent with this rise in transconductance is a proportional rise in gain and once low feedback capacitance now swells to enormous proportions appearing as an addition to the input capacitance

$$C_{IN} = C_{ISS} + (1-Av).C_{GD} \qquad (2.6.14)$$

where C_{ISS} is the common-source input capacitance, C_{GD} is the gate-drain capacity,and Av is the voltage gain.

The input capacitance, C_{IN}, in the cut-off region is fairly constant.It corresponds to the common-source input capacitance, C_{ISS}, and is approximately equal to

$$C_{IN1} = C_{ISS} + C_{GD} \qquad (2.6.15)$$

In the pinch-off region, C_{IN} increases because the VVMOST begins to turn-on and V_{DS} begins to change,thus increasing the rate of change of V_{GD}.The MILLER EFFECT on C_{GD} causes C_{IN} to increase.This effect stops after the device is fully ON and V_{DS} ceases to change. The approximate capacitance in this region is (16)

$$C_{IN2} = C_{ISS} + (1-Av).C_{GD} \qquad (2.6.16)$$

where Av is equal to

$$Av = \frac{\triangle V_{DS}}{\triangle V_{GS}} = \frac{V_{DS}(ON) - V_{DS}(OFF)}{V_{DS}(ON)} \qquad (2.6.17)$$

Substituting Eq.(2.6.17) into Eq.(2.6.16), C_{IN2} can be rewritten as

$$C_{IN2} \cong C_{ISS} - \frac{V_{DS}(ON)-V_{DS}(OFF)}{V_{DS}(ON)} \qquad (2.6.18)$$

In the resistive region V_{DS} is saturated at a low value and is no longer changing.The VVMOST channel is ON and C_{IN} is higher than it is in the cut-off region,but not as high as in the pinch-off region.No MILLER occurring and it also corresponds C_{ISS},and it is approximately equal to (16)

$$C_{IN3} = C_{ISS}+C_{GD} \qquad (2.6.19)$$

As a result C_{IN1} and C_{IN3} corresponds to C_{ISS} and are approximately equal to the addition of the gate to source and gate to drain capacitances.They differ in magnitude because of the differences in V_{DG} in the turn-on delay and the resistive regions.

There is a large change in the bias on C_{GD}.In the turn-on delay or cut-off regions the drain area under the gate is depleted of carriers,thus C_{GD} is greatly reduced.In the resistive region the drain region under the gate is flooded with carriers because the device is ON,that is much greater.

2.6.5. Switching Times

By using the input side of the VVMOST model the related switching times can be calculated.

A turn-on delay,tdon,occurs in the turn-on delay region while the gate is being charged up to threshold voltage,V_T.Then turn-on of the VVMOST channel starts and is completed when V_{DS} saturation occurs at $V_{GS} = V_T+V_{DS}(ON)$.This turn-on time is defined as the rise time,tr.

Overdrive is occurring in the resistive region.The excess charge

in the resistive region causes a turn-off delay,tdoff.This delay occurs until V_{GS} drops to the value of $V_T+V_{DS}(ON)$.The turn-on and turn-off delays could be decreased by pre-biasing the gate to a V_{GS} just below V_T and by avoiding overdriving into the resistive region.This,however,would decrease the switching circuit noise-margin and would require closer control of the gate drive voltage and the threshold voltage of the VVMOST.

For the value of V_{GS} just below $V_T+V_{DS}(ON)$,V_{DS} begins to come out of saturation,and the VVMOST will be completely OFF when V_{GS} drops below the threshold voltage,V_T.The time which is passed at this state is defined as the fall time,tf.

Finally ON and OFF times can be calculated by using these definitions,respectively

$$T_{ON} = (TT/2-tr-tdon)+tdoff \qquad (2.6.20)$$

and

$$T_{OFF} = tdon+(TT/2-tdoff-tf) \qquad (2.6.21)$$

Table(2.1) shows the approximate quantities to use in the equation for determining the switching times (16)

TABLE 2.1 Pertinent VVMOST switching relationships

Interval	Symbol	Gate Voltage Change	Capacitance
Turn-on Delay	tdon	$V_T-V_{GS}(OFF)$	C_{ISS}
Rise Time	tr	$V_{GSON1}-V_T$	$C_{ISS}+\frac{\Delta V_{DS}}{\Delta V_{GS}}.C_{RSS}$
Turn-off Delay	tdoff	$V_{GS}(ON)-V_{GSON2}$	C_{ISS}
Fall Time	tf	$V_{GSON2}-V_T$	$C_{ISS}+\frac{\Delta V_{DS}}{\Delta V_{GS}}.C_{RSS}$

Capacitance values used are the average values as V_{GS} varies over the ranges shown for the time interval of interest.Appropriate V_{DS} values must also be used to determine the capacitance.Key V_{GS} points are

$V_{GS}(OFF)$: OFF state gate voltage prior to turn-on

V_T : Threshold gate voltage

V_{GSON1} : V_{GS} corresponding to the peak value of drain current for capacitive or resistive loads or the value of drain current when the drain voltage enters the ohmic region for inductive loads.

$V_{GS}(ON)$: On-state gate voltage prior to turn-off

V_{GSON2} : V_{GS} corresponding to the value of drain current flowing prior to turn-off

2.7. General Review to VDMOS Transistors

Recent advances in processing technology and the introduction of new device structures have allowed dramatic improvements in the current,voltage,and power-handling capabilities of MOSFET devices. The impetus for much of this work is the faster switching ability of majority-carrier devices which do not suffer from the minority-carrier charge-storage problems inherent to bipolar transistors. A second primary motivation is the negative temperature coefficient of carrier mobility which greatly decreases problems of thermal runaway,secondary breakdown,and current hogging,all of which play important roles in the design and application of power bipolar transistors.The recent commercial availability of a variety of discrete-power MOS transistors has made possible a host of new applications for these devices including switching power supplies, linear audio and high-frequency amplifiers,and power control devices.

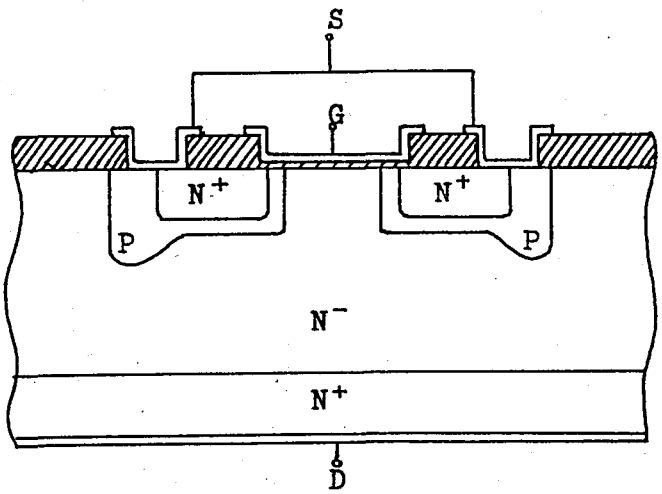
Two main changes in the basic MOSFET structure have been responsible for these advances.The first of these is the wide-spread use of double-diffusion techniques to achieve very short channels, although not all of the new power MOSFET's use double-diffusion. Sequential diffusion of p- and n-type impurities in a manner analogous to bipolar transistor fabrication processes yields channel lengths comparable in dimension to bipolar basewidths.Historically, this process has been difficult to control because the threshold voltage of the device is determined by diffused impurity profiles rather than by bulk substrate doping levels.The wide-spread use of ion implantation has,however,largely eliminated this difficulty.

The second major change in the basic MOSFET structure has been the incorporation of a lightly doped (usually n^-) drift region between the channel and the n^+ drain contact.This region largely supports the applied drain potential because its doping level is chosen to be much smaller than the p-channel region.These new structures,therefore,effectively separate the active portion of the device (channel) which determines device gain,from the region of the device which supports the applied voltage (drift region).This separation is exactly analogous to modern bipolar transistors in which a lightly doped collector region largely supports the applied potential and a narrow,more heavily doped base region largely determines device gain.

While most of the recently developed power MOS devices are based on these two principles,there exists substantial variation in the structures used to implement them,(18).The topology of the vertical double-diffused power MOSFET (VDMOS) is attractive,since it combines excellent performance with a planar,high-yield fabrication process.The VDMOS structure is shown in cross section in Figure(2.8).

An enlarged cross-section of a single cell of the VDMOS structure is shown in Figure(2.9).The channel region is covered by an insulating oxide layer,and polycrystalline silicon overlays this to form the gate electrode.The gate is insulated by a further oxide layer from the full surface-top metallisation which forms the source terminal and which contacts both the n^+ source region and the p well on the top surface.The drain region is an n^-n^+ sandwich with an ohmic metal contact at the bottom surface.

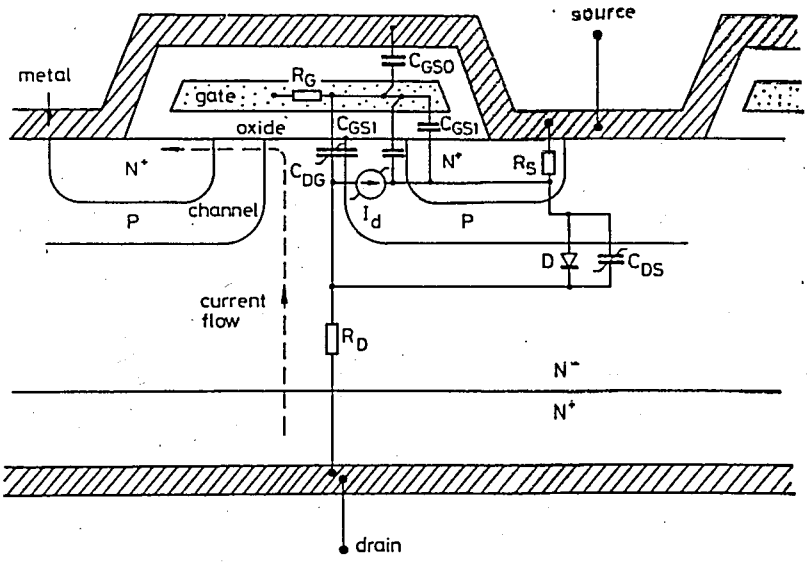
The path of conventional current flow through the inversion layer in the channel is shown on the left side of Figure(2.9). Current flows vertically from the drain through a drift region in the n^- layer,then horizontally through a surface inversion layer in the active channel and out of the source.The physical origins of the circuit elements in the model are indicated on the right side of Figure(2.9).



FIGURE(2.8) Cross section of the high-voltage VDMOS device

First,the D.C. aspect of the model is described.The non-linear voltage-controlled current generator I_d models the intrinsic field-effect action on channel conductivity.R_S and R_D model the access resistances (extrinsic) to the source and drain from the external device terminals.R_D is the principal contributor to the FET source-

drain 'ON' resistance,and consists of several additive components: (i) the resistance of the lightly doped n^- epitaxial layer drift region,(ii) a spreading resistance arising from the curvature of the current flow lines from vertical to horizontal,(iii) a resistance representing the pinching of current between adjacent p wells and (iv) a resistance corresponding to the surface accumulation layer which is formed in the drift region immediately under the gate (between the p wells),whose conductivity depends on the gate voltage. The latter two components are to some extent voltage dependent, however,in typical high-voltage devices which require low n^- doping, the resistance of the epi-layer,including spreading resistance, dominates,and R_D can be approximated by a constant resistance. Inherent in the VDMOS structure shown in Figure(2.9) is a parasitic n^+pn^- bipolar transistor (between the source-channel-drain regions).



FIGURE(2.9) Cross-section of single cell of power VDMOS structure

This transistor is kept inactive by shorting the base to the emitter directly on the die by means of the source metallisation which overlaps the p and n^+ regions on the surface.By appropriate design, the base resistance and β of the parasitic BJT are minimised,so

that the transistor can not be turned on.Neverthless,a pn^- diode remains at the channel-drain junction.This diode is normally reverse biased (forming the collector junction of the parasitic BJT),but it may conduct current if the source is biased positively with respect to the drain.The presence of this integral reverse rectifier is represented by the pn junction diode in Figure(2.9).

Next,the A.C. and charge storage aspects of the model are considered.The gate to source capacitance C_{GS} comprises several components,as shown in Figure(2.9).C_{GSi} expresses the fundamental intrinsic field control of charge storage in the inversion charge and space charge of the bulk channel region.The extrinsic component contributions to C_{GS} are represented by the constant capacitances: C_{GSO} which is due to the overlay of the source metallisation over the isolated gate electrode,and C_{GSl} which arises from the gate metal overlap onto the n^+ source region.The drain to gate feedback capacitor C_{DG} is a nonlinear element which arises from the effects of drain voltage on gate charge;it comprises an intrinsic element relating to charge storage at the drain end of the channel,together with a component owing to surface charge accumulation that can occur in the drift region directly under the gate between the P wells. The drain to source capacitance C_{DS} is a nonlinear element which models the depletion capacitance behaviour of the reverse-biased pn integral junction diode,as well as the effects of drain voltage on the channel space charge,and any extrinsic interelectrode drain-source capacitance.It is assumed that the parasitic bipolar transistor in the device structure is rendered inactive.so that its model elements are omitted (19)

The time-variant linear VDMOST model which is to be used in the analysis of switching circuits is similar to that of VVMOS transistors

which is given in section(2.5).The model is associated with the VDMOS device structure.The model consists of only three elements whose parameter values are directly determined from a series of D.C. and A.C. measurements.The description of the model parameters is given in the following section.

2.8. Description of VDMOST Model Parameters

For the VDMOST model to be used in the switching applications a careful analysis of the VDMOST switching parameters is required. The parameters required to characterise the model are the device resistances,the device capacitances,the threshold voltage,and a constant,B.All these parameters are conveniently obtained from D.C. and small signal measurements,(19)

2.8.1. D.C. Characterisation

The VDMOST D.C. characteristics are modelled by the resistances R_S and R_D.The relation between the external applied voltages V_{GS}, V_{DS} and the internal controlling modes V_{GSi},V_{DSi} is (19)

$$V_{GSi} = V_{GS} - I_D . R_S \qquad (2.8.1)$$

$$V_{DSi} = V_{DS} - I_D . (R_S + R_D) \qquad (2.8.2)$$

The equations for I_D in the cut-off,pinch-off and resistance regions are specified by

$$I_D = 0 \qquad V_{GSi} < V_T \qquad (2.8.3)$$

$$I_D = \beta . (V_{GSi} - V_T)^2 \qquad 0 < (V_{GSi} - V_T) < V_{DSi} \qquad (2.8.4)$$

$$I_D = \beta \left\{ 2 . V_{DSi} (V_{GSi} - V_T) - V_{DSi}^2 \right\} \qquad 0 < V_{DSi} < V_{GSi} - V_T \qquad (2.8.5)$$

where V_T is the device threshold voltage and β is a constant.Here the channel-length modulation term which leads to a finite output conductance in the pinch-off region has been omitted for simplicity, since this effect is not important for switching applications.

Power VDMOSTs have D.C. characteristics that deviate from the classical square-law equations in Eqs.(2.8.3)-(2.8.5),because of secondary effects in the short active-channel region.A more accurate D.C. model should incorporate mobility reduction,owing to the normal component of electric field in the channel,scattering limited velocity saturation of carriers and nonuniform impurity concentration in the channel.In the pinch-off region Eq.(2.8.4) predicts an internal transconductance as

$$g_{mi} = \frac{\beta.(V_{GSi}-V_T)^2}{V_{DSi}} \qquad (2.8.6)$$

whereas actual power VDMOSTs exhibit a transconductance that initially rises with V_{GSi} but eventually saturates at a constant maximum value. This is because of the high electric field along the short channel length between drain to source which causes the carriers to reach a scattering limited velocity.In the resistance region,Eq.(2.8.5) predicts a channel conductance

$$g_{oi} = 2.\beta.(V_{GSi}-V_T) \qquad (2.8.7)$$

whereas actual power VDMOSTs exhibit a drain-source conductance that approaches a constant value at high gate voltages.This is because of mobility reduction with normal electric field at high gate voltages.The reductions in the observed transconductance and output conductance at the device terminals are caused by a combination of the intrinsic secondary effects in the channel,as

discussed above,and extrinsic effects due to the voltage drops in the parasitic source and drain resistances R_S and R_D.With respect to the latter effect,the presence of R_S results in the measured external pinch-off transconductance g_m being reduced from its internal value g_{mi}

$$g_m = \frac{g_{mi}}{1+g_{mi}.R_S} \qquad (2.8.8)$$

By using this expression the pinch-off drain to source resistance can be obtained as

$$R_{DS}(\text{OFF to ON}) = 1/g_{mi}+R_S = \frac{V_{DSi}}{\beta.(V_{GSi}-V_T)^2} + R_S \qquad (2.8.9)$$

Similarly,the measured external drain to source output conductance in the resistance region g_0 is reduced from its internal value g_{oi}:

$$g_o \cong \frac{g_{oi}}{1+(R_S+R_D).g_{oi}} \qquad (2.8.10)$$

The ON-drain to source resistance can be obtained by using Eqs. (2.8.7) and (2.8.10) as shown below

$$R_{DS}(\text{ON}) = 1/g_{oi}+R_S+R_D = \frac{1}{2.\beta.(V_{GS}-V_T)} + R_S + R_D \qquad (2.8.11)$$

where the approximation $V_{GSi} = V_{GS}-I_d.R_S \cong V_{GS}$ applies to large V_{GS} and low V_{DS} in the resistance region.

In the present modeling approach all the resistances and the expressions which provide a relation between the cut-off,pinch-off and resistance regions require the determination of only four parameters V_T,B,R_S,R_D.This can be expressed as the very efficient data-acquisition and reduction procedure.

a. Determination of V_T and B

In the pinch-off region, using Eqs.(2.8.1) and (2.8.4), the drain current is given by

$$I_D = \beta.(V_{GS}-V_T-I_D.R_S)^2 \qquad (2.8.12)$$

For small R_S and for I_D chosen in the low range

$$V_{GS} = \frac{1}{\sqrt{\beta}}\sqrt{I_D} + V_T \qquad (2.8.13)$$

A plot of V_{GS} against $\sqrt{I_D}$ from measured characteristics in the pinch-off region for moderate I_D gives a straight line, for which the intercept gives V_T and the slope gives $1/\sqrt{\beta}$.

b. Determination of R_S

In the pinch-off region described by Eqs.(2.8.4), R_S may be determined from

$$R_S = \frac{V_{GS}-V_T}{I_D} - \frac{1}{\sqrt{\beta.I_D}} \qquad (2.8.14)$$

A suitable (V_{GS}, I_D) measurement must be substituted into Eq.(2.8.14). An appropriate measurement point is one where I_D is moderate, so the $I_D.R_S$ drop is significant, and which lies fairly centrally within the total I_D range to be modelled for the device.

c. Determination of R_D

In the resistance region for low V_{DS} the total drain to source resistance $R_{DS}(ON)$ is given in Eq.(2.8.11). Hence R_D may be evaluated from this expression

$$R_D = R_{DS}(ON) - \frac{1}{2.\beta.(V_{GS}-V_T)} - R_S \qquad (2.8.15)$$

The effective value of R_D obtained from Eq.(2.8.15) depends on the measurement point used in the resistance region.Since a good fit is more important at the drive levels used in practice for attaining minimum device 'ON' resistance,the (R_{DSON},V_{GS}) measurement is taken at high V_{GS} values.The information for determining R_D can be taken from the data sheet.

2.8.2. A.C. Characterisation

The values and behavior of the capacitance elements in the power VDMOST model have been determined by making small-signal measurements over a range of bias points.Measurements were taken along various constant V_{GS} contours over a range of V_{DS} from zero to 25 V.,encompassing the cut-off,pinch-off and resistance regions of operation,from which the voltage dependencies of C_{DG},C_{DS} and C_{GS} were deduced.Conventional small signal y parameters at one MHz were chosen for convenience,although some care is necessary when measuring the reverse parameters y_{12} and y_{22} in the resistance region where the drain-source resistance is low.

a. Determination of C_{DG}

The characteristics of C_{GD} are obtained from y_{12} measurements. For low parasitic resistances R_S,R_D, and R_G,the value of C_{DG} is given by

$$C_{DG} = -\frac{Im[y_{12}]}{\omega} = \frac{|y_{12}|}{\omega} \qquad (2.8.16)$$

The phase of y_{12} corresponds nearly to a pure reactance,indicating a capacitance element consistent with the model.C_{DG} has a single variable dependency,with the drain to gate voltage V_{DG} being the

controlling voltage.The $C_{GD}(V_{DG})$ behavior plays an important role in the switching characteristic.

b. Determination of C_{DS}-

The characteristics of the output capacitance C_{DS} is obtained from y_{22} measurements and is evaluated from

$$C_{DS}=\frac{Im(y_{22})}{\omega}-C_{DG} \qquad (2.8.17)$$

This capacitance exhibits a typical pn junction depletion capacitance behavior associated with the integral reverse diode at the drain. Some departure from this is evident when the device turns on, especially in the resistance region for low V_{DS},owing to a contribution from the intrinsic capacitance associated with the effects of draim voltage on channel-space charge.However,C_{DS} is well modelled by accounting for the primary dependence of depletion capacitance on V_{DS},using an expression of the form

$$C_{DSO}\cdot(1+V_{DS}/\phi)^{-H}+C_p \qquad (2.8.18)$$

where C_{DSO} is the junction capacitance at $V_{DS}=0$, H is a grading coefficient $0.3<H<0.5$, ϕ is the junction potential and C_p is the etray capacitance arising from the mounting of the VDMOST on a heatsink.

c. Determination of C_{GS}-

The characteristic of the input capacitance C_{GS} is obtained from y_{11} measurements and is evaluated from

$$C_{GS}=\frac{Im[y_{11}]}{\omega}-C_{DG} \qquad (2.8.19)$$

The phase of y_{11} corresponds nearly to a pure reactance,indicating a capacitance element.The gate to source capacitance,C_{GS},is independent of voltage and may be modelled by a constant value. This behavior can be explained on a physical basis.With regard to the intrinsic channel region,when the VDMOST is in cut-off,there is no inversion charge,however,there is a charge-storage component owing to space charge in the bulk-channel region.When the VDMOST enters the conducting region,either in the pinch-off or the resistance regions,the channel space charge stays fairly constant, however,the channel inversion charge rises approximately linearly with V_{GS}.This leads to a fairly constant overall intrinsic gate to source capacitance behavior,which is further linearised,in the case of the power VDMOST structure,by the presence of significant extrinsic constant capacitances C_{GSO} (source metal overlay over gate) and C_{GSl} (gate metal overlap onto source).

The model input capacitance can be obtained from the gate to source capacitance,C_{GS},and the gate to drain capacitance,C_{DG}, by using the related explanations and expressions which are given in section(2.6.4).

d. Determination of R_G

The value of the gate resistance is obtained by measuring the time constant of the step response of the gate voltage,when the VDMOS is operating in the cut-off region.The VDMOS is biased with a large drain voltage and a small gate pulse is applied from a generator with source resistance R_I.Under these conditions,V_{DG} is large so C_{DG} has a constant small value given by the lower plateau, and the time constant of the gate voltage response,in cut-off conditions for $V_{GS}(t) < V_T$,is given by

$$\tau = (R_G + R_I).(C_{GS} + C_{GD}) \qquad (2.8.20)$$

From a measurement of this time constant, R_G can be evaluated.

III. BASIC SWITCHING CIRCUITS ANALYSIS BY USING TIME-VARIANT LINEAR TRANSISTOR MODELS

The transistor is being used as a switch to connect and disconnect the load from the source.When a transistor is used as a switch,it is useful to divide its operation range into three regions.Whether the transistor is in the ON condition,the OFF condition,or the transient region between OFF and ON,the behavior can be calculated with considerable accuracy.

The junction transistor used as a non-regenerative switch,that is,a switch which can be maintained in an altered condition only by the continued application of sufficient control or stimulus can have a few hundred kiloohms impedance in the OFF condition and less than one ohm in the ON condition.The actual D.C. voltage across the transistor switch in the ON condition can be as low as a few hundred millivolts.Non-regenerative transistor switches can be switched from OFF to ON,or vice verca,in a relatively insignificant time.

In the common-emitter configuration the input switching signal current or voltage,is small in comparison with the switched output current or voltage.Hence,the common-emitter configuration is the most generally useful for a bipolar transistor switch.In most bipolar transistor switching circuits,the input voltages can be relatively large.The base resistance,R_B,must be large to limit base current to reasonable levels.

The type of drive of a transistor affects the shape of the current in the collector circuit.Current drive and voltage drive have different effects on the output current of the transistor with both small and large signals.

The type of the load of a transistor affects also the shape of

the signal received in the output circuit.To enable us to form a complete picture of the possible uses of a transistor with rectangular signals,it is very important that the effect of the loads should be discussed(20).

There are three basic types of load for a switching stage:

1) a purely resistive load;
2) an inductive and resistive load;
3) a capacitive,inductive,and resistive load.

A resistive load involves the use of a pure resistance in the output circuit of the transistor.A purely resistive load is rarely met with in industrial circuits.The actual load of a transistor often consists of a system of diodes feeding connecting units associated with the inputs of the stages immediately following the transistor under study.These different units,diodes and transistors which make up the load,may act inductively or capacitively.

In transistorized switching circuits the type of load which consists of an inductance and a resistance in series is often met. In order to determine the available energy at the output of the stage,the value of the collector current,or load current,and then the variations of the output voltage must be determined.

An inductance stores energy and restores it.For this reason with inductive loads we must differentiate between the following three possibilities:

1) under-damping
2) critical condition
3) over-damping

These three cases have a very important effect on the shape of the signals received at the output circuit.All necessary analyses to be used in the determination of the load current and output voltage

are to be made in this chapter.

One of the most serious problem in the operation of a power transistor with an inductive load is burn-out,which results in a short circuit between the collector and emitter.Burn-out is usually produced when the transistor is suddenly cut-off from its ON-condition. The secondary breakdown of the collector characteristics determines the susceptibility to this type of failure.The secondary breakdown is greatly influenced by the reverse base current.The reverse base bias voltage and impedance affect the reverse base current in a predictive manner.

For safe operation,the secondary breakdown current should be greater than the maximum operating current.When the reverse base current is minimized,the transistor is also protected.To protect against burn-out,it is also desirable to use transistors with lower breakdown voltage requirement,because lower voltage transistor absorbs less inductive energy(21).In switching circuits with inductive loads,the switching response time is lengthened if the voltage surge from the inductance is limited.In such circuits,lowering BV_{CEO} of the transistor is not desirable.

The operation of transistors which uses a resonant circuit formed from a resistance,an inductance,and a capacitance in parallel as load is also considered.The analysis to be made for this type of load is similar to that of the inductive-resistive load.

The recent advent of the VVMOS transistors has been a significant development in the field of semiconductor power-control devices.The reasons for this arise from the transistor's inherent features of high-speed response,voltage controlled drive,robust operation with absence of secondary breakdown and excellent thermal stability,which is because of its fundamental mechanism as a field-controlled majority

carrier device.

Freedom from secondary breakdown limitations makes driving highly inductive or capacitive loads a natural application for VVMOSTs.Inductive loads include transformers,solenoids or relays. High current inrush loads such as incandescent lamps,pulse forming networks,and motors also are generally handled easily.Some attention must be given to the load characteristics,however.

In common with bipolar semiconductor devices,VVMOS transistors can be damaged if their voltage rating are exceeded.Although their avalanche energy capability is much better than that of bipolar transistors,it is not good design practice to have the VVMOST absorb inductive energy unless the part is rated for this type of service. The spikes generated from inductive loads may have tremendous energy content and usually some means of limiting their amplitude must be provided.Highly inductive loads may generate significant power on turn-off,whereas capacitive-like loads cause power surges on turn-on.

Usually with inductive loads the peak voltage spike should be limited to a value below the breakdown rating of transistor.The safest and least expensive limiting technique is to use a zener diode as a peak-clipping (16).Resistive and capacitive loads usually require no auxiliary circuitry.

In this chapter the analyses of the transistor switching circuit with R-L-C load and CVDMOS inverter are made,separately.The linear equivalent circuits to be used in the analyses can be obtained by using the related time-variant linear large-signal transistor models which are presented in the second chapter.

For the VVMOST switching circuit the output side of the equivalent circuit to be obtained is similar to that of BJT.That's why the analysis which is made for the BJT switching circuit with R-L-C load

in section(3.1) is used for the VVMOST switching circuit.The expressions of the load current and output voltage of the VVMOST switching circuit can be obtained by using the parameters of R_{DS}, C_{DS},V_{DS},and V_{DD} instead of R,C,V_C,and V_{CC} and by equating V_{CES} to zero.The input side of the VVMOST switching circuit is used for determining the gate to source voltage,the gate current,the related switching times,and the relations between the switching regions.

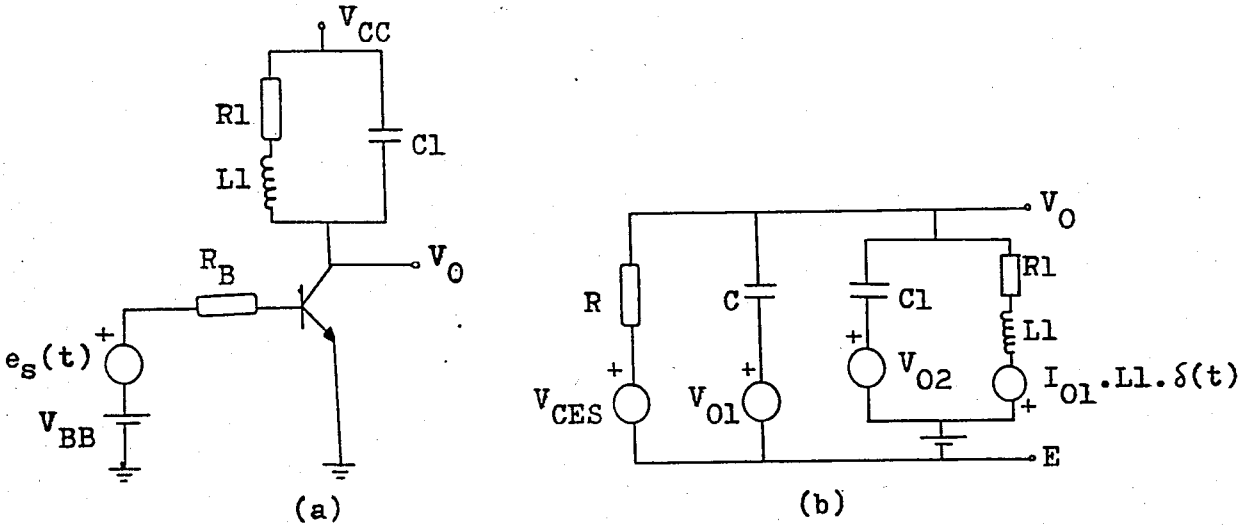
The analysis of the switching circuits with resistive and resistive-inductive loads can be obtained easily by taking the values of the load inductor and capacitor and the load capacitor as zero,respectively,in the expressions which are obtained as a result of the analysis which is given in section(3.1)

The analysis of the CVDMOS inverter which is considered as an application of VDMOST model is made in section(3.2).The inverter consists of a p-channel VDMOST connected in series with an n-channel VDMOST (drain to drain) with the gates tied together and driven from a common signal-hence,the name CVDMOS (Complementary VDMOS).When the input signal goes positive the p-channel VDMOST is essentially off and conducts only I_{DSS}(picoamperes).The n-channel unit is forward biased but since only I_{DSS} is available from the p-channel,V_{DS} is very low.Conversely,when the input goes low (zero),the p-channel device is turned full on,the n-channel device is off,and the output will be very near $-V_{DD}$.Since the current (without a load) is extremely small-the inverter dissipates almost no power in either stable-state;the only dissipated power of consequence occurs during the switching transitions as capacitances are charged.

For all the analysis,the related flowcharts are given in section (3.3).Some general and necessary explanations for the preparation of computer programs are given in this section,too.

3.1. Analysis of Switching Circuits with R-L-C Load

For the BJT switching circuit with R-L-C load,a linear equivalent circuit which contains the initial conditions of the load inductor,load capacitor,and the collector to emitter time-variant capacitor is obtained by using the time-variant linear model which is given in section(2.2),instead of the bipolar transistor.The switching circuit and its linear equivalent circuit related to the output part are shown in Figures (3.1.a) and (3.1.b),respectively.

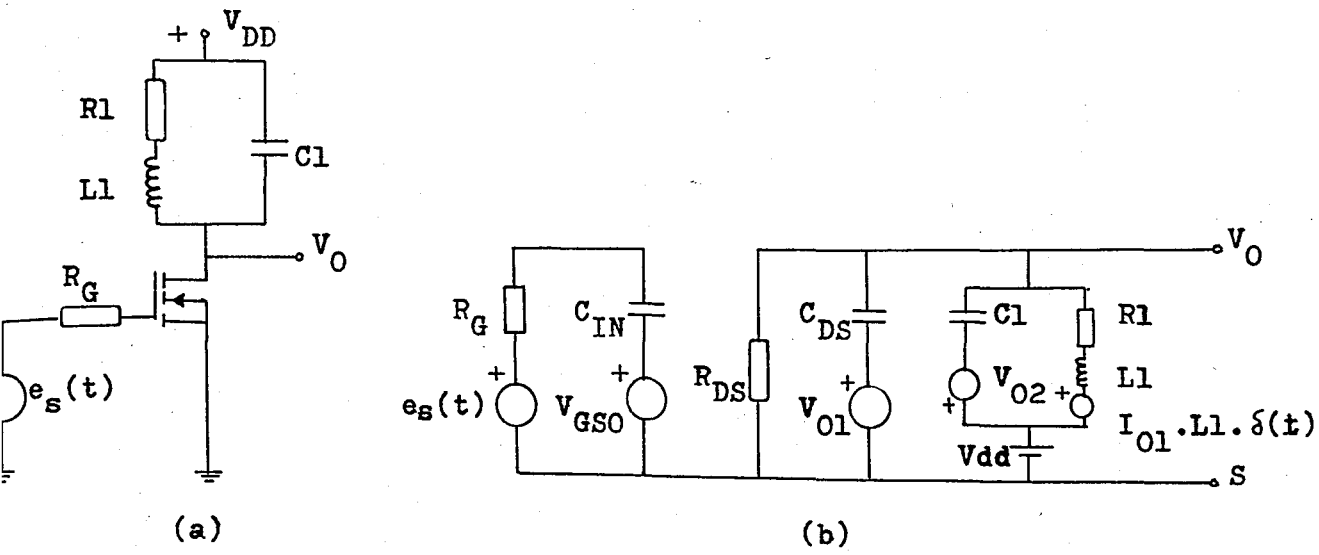


FIGURE(3.1) a) A BJT switching circuit with R-L-C load

b) The related linear equivalent circuit

Similarly,a linear equivalent circuit of the VVMOST switching circuit with R-L-C load is obtained by using the corresponding time-variant linear model instead of VVMOS transistor.This model is given in section(2.3).The related switching circuit and its equivalent circuit are shown in Figures (3.2.a) and (3.2.b),respectively.

For the VVMOST switching circuit,the expressions of the gate to source voltage and load current can be obtained by using the input side of the linear equivalent circuit which is shown in Figure(3.2.b). The input side of the equivalent circuit to be used in this analysis

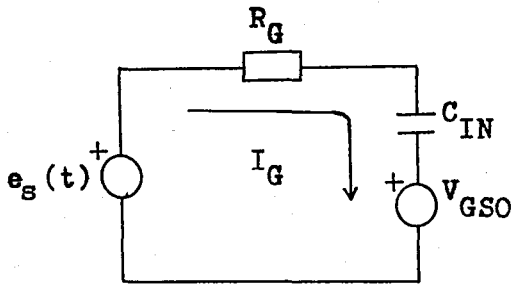


FIGURE(3.2) a) A VVMOST switching circuit with R-L-C load

b) The related linear equivalent circuit

is shown in Figure(3.3).

If the initial conditions of the equivalent circuit input capacitance, C_{IN}, is considered as the previous value of the gate to source voltage, the expression for the gate to source voltage can

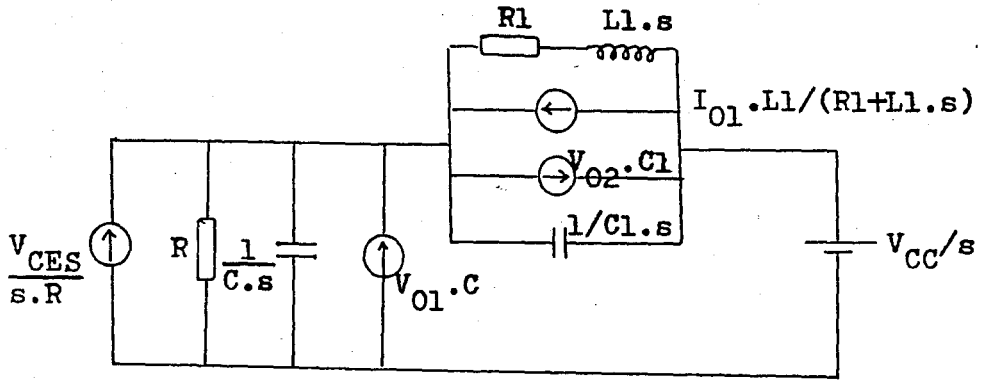


FIGURE(3.3) Input side of the equivalent circuit shown in Figure(3.2

be obtained as

$$V_{GS} = \left[e_s(t) - V_{GSO}\right] \cdot \left[1 - \exp(-DELT/(R_G \cdot C_{IN}))\right] + V_{GSO} \qquad (3.1.1)$$

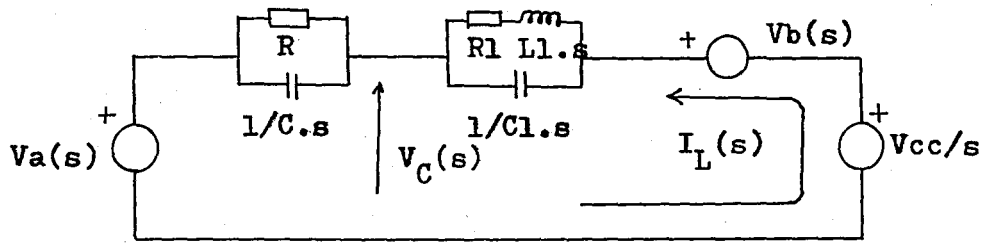
In this expression the value of C_{IN} changes by depending on the operating regions. The expression for the gate current can be obtained easily



FIGURE(3.4) The circuit obtained by using Laplace transform method and network theorems in the circuit shown in Figure(3.1.b).

$$I_G = \left[e_s(t) - V_{GSO}\right] / R_G \qquad (3.1.2)$$

As shown in Figures (3.1.b) and (3.2.b),the equivalent circuit of the BJT switching circuit with R-L-C load is similar to the output side of that of VVMOST.That's why only one analysis is to be made



FIGURE(3.5) The circuit to be used in the analysis

for obtaining the output voltages and load currents of these two kinds of switching circuits.

By using the equivalent circuit shown in Figure(3.1.b) a new circuit which contains the current equivalences of voltage sources and Laplace transforms of the circuit parameters is obtained and it is shown in Figure(3.4).

By using the voltage equivalences of the current sources in Figure(3.4),a circuit to be used in the analysis is obtained and it is shown in Figure(3.5).

The output voltage and load current of this switching circuit can be calculated by using the related equations which are obtained by the analysis which is made in this section.

In this analysis,the voltages of Va(s) and Vb(s) are defined as, respectively

$$Va(s)=(V_{CES}/s+V_{01}.C.R).\frac{1}{1+s.R.C} \tag{3.1.3}$$

$$Vb(s)=\frac{L1.I_{01}-V_{02}.C1(R1+L1.s)}{s^2.L1.C1+s.R1.C1+1} \tag{3.1.4}$$

The load current of this circuit can be calculated like that

$$I_L(s)=\frac{V_{CC}/s+Vb(s)-Va(s)}{\frac{R}{1+s.R.C}+\frac{R1+L1.s}{s^2.L1.C1+s.R1.C1+1}} \tag{3.1.5}$$

$$I_L(s)=\frac{\left[V_{CC}/s+Vb(s)-Va(s)\right](1+s.R.C)(s^2L1.C1+s.R1.C1+1)}{s^2(R.L1.C1+R.L1.C)+s(R.R1.C1+R.R1.C+L1)+R+R1} \tag{3.1.6}$$

By substituting Eqs.(3.1.3) and (3.1.4) into Eq.(3.1.6),and rearranging it according to the power of s,this expression can be obtained

$$I_L(s)=\frac{s^3.A1+s^2.A2+s.A3+A4}{s(s^2.A5+s.A6+A7)} \tag{3.1.7}$$

where

$$A1=R.L1.C.C1(V_{CC}-V_{02}-V_{01}) \tag{3.1.8}$$

$$A2=R.R1.C.C1(V_{CC}-V_{02}-V_{01})+L1.C1(V_{CC}-V_{02}-V_{CES})+I_{01}.R.L1.C \tag{3.1.9}$$

$$A3=R.C(V_{CC}-V_{01})+R1.C1(V_{CC}-V_{02}-V_{CES})+I_{01}.R.L1.C \tag{3.1.10}$$

$$A4=V_{CC}-V_{CES} \tag{3.1.11}$$

$$A5 = R.L1(C+C1) \tag{3.1.12}$$

$$A6 = R.R1(C+C1)+L1 \tag{3.1.13}$$

$$A7 = R+R1 \tag{3.1.14}$$

There are two types of solution of Eq.(3.1.7) by depending on the value of the load inductor which is equal to zero or not.

3.1.1. Case of $L1 = 0$

If the load inductor is not used in the circuit shown in Figure (3.5),Eq.(3.1.7) becomes

$$I_L(s) = \frac{s^2.A2+s.A3+A4}{s(s.A6+A7)} \tag{3.1.15}$$

If the numerator and denominator of Eq.(3.1.15) are divided by A6, the expression of $I_L(s)$ becomes

$$I_L(s) = \frac{s^2.A8+s.A9+A10}{s(s+A11)} \tag{3.1.16}$$

where

$$A8 = A2/A6 \tag{3.1.17}$$

$$A9 = A3/A6 \tag{3.1.18}$$

$$A10 = A4/A6 \tag{3.1.19}$$

$$A11 = A7/A6 \tag{3.1.20}$$

The output voltage can be obtained as

$$V_0(s) = I_L(s) \cdot \frac{R}{1+s.C.R} + Va(s) \tag{3.1.21}$$

For finding the solutions of these expressions in time-domain

once the partial fraction expansion of these expressions must be achieved, the corresponding residues must be determined, and their inverse Laplaces must be obtained by taking the inverse transform of each term in the partial fraction expansion.

If the denominator of these expressions has simple roots the i-th residues, k_i, can be obtained as (22)

$$k_i = (s-s_i).F(s)\Big|_{s=s_i} \qquad (3.1.22)$$

where F(s) is a function in s-domain and s_i is a pole of F(s).

If the denominator of these expressions has poles with multiplicities, the corresponding residues, K_{ij}, can be obtained from the following expression (22)

$$K_{ij} = \frac{1}{(r_i-j)!}\cdot\frac{d^{r_i-j}}{ds^{r_i-j}}\left[(s-s_i)^{r_i}.F(s)\right]\Big|_{s=s_i} \qquad (3.1.23)$$

where $i = 1,2,3,\ldots,t$ and $j = 1,2,3,\ldots,r_i$. Here t is the number of poles, r_i defines the multiplicities. The expression in Eq.(3.1.23) is in its most general form, too.

a. Determination of $I_L(t)$

By using Eq.(3.1.16), the current of $I_L(s)$ can be written in the form of the partial fraction expansion

$$I_L(s) = \frac{A12}{s} + \frac{A13}{s+A11} \qquad (3.1.24)$$

The corresponding residues of Eq.(3.1.24) can be calculated by means of Eq.(3.1.22) and by using Eq.(3.1.16) the residues, A12 and A13, are obtained as shown below

$$A12 = \left.\frac{s^2.A8+s.A9+A10}{s+A11}\right|_{s=0} = \frac{A10}{A11} \qquad (3.1.25)$$

$$A13 = \left.\frac{s^2.A8+s.A9+A10}{s}\right|_{s=-A11} = -\frac{A11^2.A8-A11.A9+A10}{A11} \qquad (3.1.26)$$

By using the corresponding residues, A12 and A13, the value of the load current in time domain can be calculated easily. The inverse Laplace transform of $I_L(s)$, Eq.(3.1.24), can be calculated as

$$I_L(t) = A12.u(t)+A13.\exp(-A11.t) \qquad (3.1.27)$$

b. Determination of $V_0(t)$

Substituting Eqs.(3.1.3) and (3.1.24) into Eq.(3.1.21), the expression of $V_0(s)$ can be obtained as

$$V_0(s) = \left(\frac{A12}{s} + \frac{A13}{s+A11}\right).\frac{R}{1+sCR} + \frac{V_{CES}}{s(1+sCR)} + \frac{V_{01}.CR}{1+sCR} \qquad (3.1.28)$$

The expression can be written in the form of the partial fraction expansion for taking the inverse Laplace transform

$$V_0(s) = \frac{A14}{s} + \frac{A15}{s+1/RC} + \frac{A16}{s+A11} + \frac{A17}{s+1/RC} + \frac{A18}{s} + \frac{A19}{s+1/RC} + \frac{V_{01}}{s+1/RC} \qquad (3.1.29)$$

The corresponding residues of Eq.(3.1.29) can be calculated by using Eq.(3.1.22) and (3.1.28) and they can be written as

$$A14 = \left.\frac{A12}{C(s+1/RC)}\right|_{s=0} = A12.R \qquad (3.1.30)$$

$$A15 = \left.\frac{A12}{C.s}\right|_{s=-1/RC} = -A14 \qquad (3.1.31)$$

$$A16 = \left.\frac{A13}{C(s+1/RC)}\right|_{s=-A11} = \frac{A13.R}{1-A11.RC} \tag{3.1.32}$$

$$A17 = \left.\frac{A13}{C(s+A11)}\right|_{s=-1/RC} = -A16 \tag{3.1.33}$$

$$A18 = \left.\frac{V_{CES}}{RC}.\frac{1}{s+1/RC}\right|_{s=0} = V_{CES} \tag{3.1.34}$$

$$A19 = \left.\frac{V_{CES}}{RC}.\frac{1}{s}\right|_{s=-1/RC} = -A18 \tag{3.1.35}$$

If the terms having a denominator with s and s+1/RC are added separately,their additions become

$$AT1 = A14+A18 \tag{3.1.36}$$

$$AT2 = A15+A17+A19+V_{01} \tag{3.1.37}$$

respectively.Finally $V_0(s)$ becomes

$$V_0(s) = \frac{AT1}{s} + \frac{AT2}{s+1/RC} + \frac{A16}{s+A11} \tag{3.1.38}$$

The inverse Laplace transform of $V_0(s)$ is equal to

$$V_0(t) = AT1.u(t)+AT2.e^{-t/RC}+A16.e^{-A11.t} \tag{3.1.39}$$

3.1.2. Case of $L1 \neq 0$

If the load inductor is used in the switching circuit shown in Figure(3.5),Eq.(3.1.7) can be used for obtaining the expression of the load current in time-domain.

If the numerator and denominator of Eq.(3.1.7) are divided by A5,the expression of $I_L(s)$ becomes

$$I_L(s)=\frac{s^3.AA1+s^2.AA2+s.AA3+AA4}{s(s^2+s.AB1+AB2)} \tag{3.1.40}$$

where

$$AA1=A1/A5 \tag{3.1.41}$$

$$AA2=A2/A5 \tag{3.1.42}$$

$$AA3=A3/A5 \tag{3.1.43}$$

$$AA4=A4/A5 \tag{3.1.44}$$

$$AB1=A6/A5 \tag{3.1.45}$$

$$AB2=A7/A5 \tag{3.1.46}$$

The denominator of Eq.(3.1.40) is a third order polynomial and its roots can be found like that

$$s(s^2+s.AB1+AB2)=0 \tag{3.1.47}$$

$$s_1=0 \tag{3.1.48}$$

$$s_{2,3}=\frac{-AB1\mp\sqrt{AB1^2-4.AB2}}{2} \tag{3.1.49}$$

Here

$$\triangle=AB1^2-4.AB2 \tag{3.1.50}$$

Depending on the value of $\triangle$,there are three types of solutions.

1) $\triangle=0$

For this case,there are three real roots.Two of them are equal each other.The roots can be obtained as

$$s_1=0 \tag{3.1.51}$$

$$s_2=s_3=-AB1/2 \tag{3.1.52}$$

2) $\Delta < 0$

Here, there are three roots. Only one of them is real, the others are imaginary. They can be written as

$$s_1 = 0 \tag{3.1.53}$$

$$s_2 = \frac{-AB1 + j\sqrt{4.AB2 - AB1^2}}{2} \tag{3.1.54}$$

$$s_3 = \frac{-AB1 - j\sqrt{4.AB2 - AB1^2}}{2} \tag{3.1.55}$$

3) $\Delta > 0$

There are three different real roots of the polynomial. Their roots can be obtained as

$$s_1 = 0 \tag{3.1.56}$$

$$s_2 = \frac{-AB1 + \sqrt{AB1^2 - 4.AB2}}{2} \tag{3.1.57}$$

$$s_3 = \frac{-AB1 - \sqrt{AB1^2 - 4.AB2}}{2} \tag{3.1.58}$$

Now, these three cases will be studied in detail and their analyses will be made, separately.

a. <u>The Case of $\Delta = 0$</u>

For this case the load current of $I_L(s)$, Eq.(3.1.40) can be written as

$$I_L(s) = \frac{s^3.AA1 + s^2.AA2 + s.AA3 + AA4}{s.(s + AB1/2)^2} \tag{3.1.59}$$

and the output voltage, $V_0(s)$, is shown in Eq.(3.1.21). For finding

the solutions of these expressions in time-domain, the method which is explained in section(3.1.1) is used here.

(1). Determination of $I_L(t)$

By using Eq.(3.1.59), the current of $I_L(s)$ can be written in the form of the partial fraction expansion as

$$I_L(s)=\frac{B1}{s}+\frac{B2}{s+AB1/2}+\frac{B3}{(s+AB1/2)^2} \qquad (3.1.60)$$

The corresponding residues of Eq.(3.1.60) can be calculated by means of Eqs.(3.1.22) and (3.1.23) and by using Eq.(3.1.59). The residues, B1, B2, and B3, are obtained as shown below

$$B1=\left.\frac{s^3.AA1+s^2.AA2+s.AA3+AA4}{(s+AB1/2)^2}\right|_{s=0}=\frac{4.AA4}{AB1^2} \qquad (3.1.61)$$

$$B2=\left.\frac{d}{ds}\cdot\left(\frac{s^3.AA1+s^2.AA2+s.AA3+AA4}{s}\right)\right|_{s=-AB1/2} \qquad (3.1.62)$$

$$B2=\frac{-AA1.AB1^3+AA2.AB1^2-4.AA4}{AB1^2} \qquad (3.1.63)$$

$$B3=\left.\frac{s^3.AA1+s^2.AA2+s.AA3+AA4}{s}\right|_{s=-AB1/2} \qquad (3.1.64)$$

$$B3=\frac{AA1.AB1^3-2.AA2.AB1^2+4.AA3.AB1-8.AA4}{4.AB1} \qquad (3.1.65)$$

By using the corresponding residues, B1, B2, and B3, the value of the load current in time-domain can be calculated easily. The inverse Laplace transform of $I_L(s)$, Eq.(3.1.60), can be obtained as

$$I_L(t) = B1.u(t) + B2.e^{-\frac{AB1.t}{2}} + B3.t.e^{-\frac{AB1.t}{2}} \qquad (3.1.66)$$

(2). Determination of $V_0(t)$

Substituting Eqs.(3.1.3) and (3.1.60),into Eq.(3.1.21) the expression of $V_0(s)$ can be obtained as

$$V_0(s) = 1/C.(B1+V_{CES}/R)\frac{1}{s(s+1/RC)} + B2/C.\frac{1}{(s+1/RC).(s+AB1/2)} +$$

$$B3/C\ \frac{1}{(s+1/RC).(s+AB1/2)^2} + \frac{V_{01}}{s+1/RC} \qquad (3.1.67)$$

This expression can be rewritten in the form of the partial fraction expansion for taking the inverse Laplace transform.

$$V_0(s) = \frac{BA11}{s} + \frac{BA12}{s+1/RC} + \frac{BA21}{s+1/RC} + \frac{BA22}{s+AB1/2} + \frac{BA31}{s+1/RC} +$$

$$\frac{BA32}{s+AB1/2} + \frac{BA33}{(s+AB1/2)^2} + \frac{V_{01}}{s+1/RC} \qquad (3.1.68)$$

The corresponding residues of Eq.(3.1.68) can be calculated by using Eqs.(3.1.22),(3.1.23),and (3.1.67) and they can be written as

$$BA11 = 1/C.(B1+V_{CES}/R)\ \frac{1}{s+1/RC}\Big|_{s=0} = B1.R+V_{CES} \qquad (3.1.69)$$

$$BA12 = 1/C.(B1+V_{CES}/R).\frac{1}{s}\Big|_{s=-1/RC} = -BA11 \qquad (3.1.70)$$

$$BA21 = B2/C.\frac{1}{s+AB1/2}\Big|_{s=-1/RC} = \frac{2.R.B2}{AB1.R.C-2} \qquad (3.1.71)$$

$$BA22 = B2/C \cdot \left.\frac{1}{s+1/RC}\right|_{s=-AB1/2} = -BA21 \qquad (3.1.72)$$

$$BA31 = B3/C \cdot \left.\frac{1}{(s+AB1/2)^2}\right|_{s=-1/RC} = \frac{4.B3.R^2.C}{(AB1.R.C-2)^2} \qquad (3.1.73)$$

$$BA32 = \frac{d}{ds} \cdot \left[B3/C \frac{1}{(s+1/RC)}\right]\Bigg|_{s=-AB1/2} = -BA31 \qquad (3.1.74)$$

$$BA33 = B3/C \cdot \left.\frac{1}{s+1/RC}\right|_{s=-AB1/2} = \frac{2.B3.R}{2-AB1.R.C} \qquad (3.1.75)$$

If the terms having a denominator with s+1/RC and S+AB1/2 are added, separately, their additions become

$$BB1 = BA12+BA21+BA31+V_{01} \qquad (3.1.76)$$

$$BB2 = BA22+BA32 \qquad (3.1.77)$$

respectively. Finally $V_0(s)$ becomes

$$V_0(s) = \frac{BA11}{s} + \frac{BB1}{s+1/RC} + \frac{BB2}{s+AB1/2} + \frac{BA33}{(s+AB1/2)^2} \qquad (3.1.78)$$

The inverse Laplace transform of $V_0(s)$ is equal to

$$V_0(t) = BA11.u(t)+BB1.e^{-\frac{t}{R.C}} +BB2.e^{-\frac{AB1.t}{2}} +BA33.t.e^{-\frac{AB1.t}{2}} \qquad (3.1.79)$$

b. The Case of $\Delta<0$

For this case, the current of $I_L(s)$, Eq.(3.1.40), can be written as

$$I_L(s)=\frac{s^3.AA1+s^2.AA2+s.AA3+AA4}{s.(s-s_2).(s-s_2^*)} \qquad (3.1.80)$$

and the output voltage, $V_0(s)$, is shown in Eq.(3.1.21). For finding the solutions of these expressions in time-domain, the method which is explained in section(3.1.1) is used here.

(1). Determination of $I_L(t)$

By using Eq.(3.1.80) the current of $I_L(s)$ can be written in the form of the partial fraction expansion as

$$I_L(s)=\frac{K_{11}}{s}+\frac{K_{12}}{s-s_2}+\frac{K_{13}}{s-s_2^*} \qquad (3.1.81)$$

By means of Eqs.(3.1.80) and (3.1.81) and using Eq.(3.1.22) the corresponding residues of $I_L(s)$ can be calculated like that

$$K_{11}=\left.\frac{s^3.AA1+s^2.AA2+s.AA3+AA4}{(s-s_2).(s-s_2^*)}\right|_{s=0}=\frac{AA4}{s_2.s_2^*} \qquad (3.1.82)$$

Here s_2 and s_2^* are the roots of the denominator polynomial and they are defined in Eqs.(3.1.54) and (3.1.55). Substituting them into Eq.(3.1.82)

$$K_{11}=\frac{AA4}{AB2} \qquad (3.1.83)$$

can be obtained easily.

$$K_{12}=\left.\frac{s^3.AA1+s^2.AA2+s.AA3+AA4}{s.(s-s_2^*)}\right|_{s=s_2} \qquad (3.1.84)$$

If this expression is solved and its real and imaginary parts are separated from each other, K_{12} can be obtained as

$$K_{12}=\frac{C1.AA1+C3.AA2+C5.AA3+AA4+j(C2.AA1-C4.AA2+C6.AA3)}{C7-j.C4} \qquad (3.1.85)$$

where

$$C0=1/2.\sqrt{4.AB2-AB1^2} \qquad (3.1.86)$$

$$C1=AB1/2.(3AB2-AB1^2) \qquad (3.1.87)$$

$$C2=C0.(AB1^2-AB2) \qquad (3.1.88)$$

$$C3=\frac{AB1^2}{2}-AB2 \qquad (3.1.89)$$

$$C4=C0.AB1 \qquad (3.1.90)$$

$$C5=-AB1/2 \qquad (3.1.91)$$

$$C6=C0 \qquad (3.1.92)$$

$$C7=\frac{AB1^2-4.AB2}{2} \qquad (3.1.93)$$

and then multiplying the numerator and the denominator of K_{12} by the complex conjugate of its denominator polynomial, K_{12} is rewritten as

$$K_{12}=C13+j.C14 \qquad (3.1.94)$$

where

$$C8=C1.AA1+C3.AA2+C5.AA3+AA4 \qquad (3.1.95)$$

$$C9 = C2.AA1 - C4.AA2 + C6.AA3 \qquad (3.1.96)$$

$$C10 = C7^2 + C4^2 \qquad (3.1.97)$$

$$C11 = C7.C8 - C4.C9 \qquad (3.1.98)$$

$$C12 = C7.C9 + C4.C8 \qquad (3.1.99)$$

$$C13 = C11/C10 \qquad (3.1.100)$$

$$C14 = C12/C10 \qquad (3.1.101)$$

can be determined easily.

$$K_{13} = K_{12}^{*} = C_{13} - j.C_{14} \qquad (3.1.102)$$

By using the corresponding residues, K_{11}, K_{12}, and K_{13}, Eq.(3.1.81) can be written as

$$I_L(s) = \frac{K_{11}}{s} + \frac{(C13+j.C14).(s-s_2^{*}) + (C13-j.C14).(s-s_2)}{(s-s_2).(s-s_2^{*})} \qquad (3.1.103)$$

In this expression, if the values of s_2 and s_2^{*} are substituted, Eq.(3.1.103) can be written as

$$I_L(s) \quad \frac{K_{11}}{s} + \frac{s(2.C13) + C13.AB1 - \sqrt{4.AB2 - AB1^2}.C14}{s^2 + AB1.s + AB2} \qquad (3.1.104)$$

Finding the roots of the denominator polynomial of the second term in Eq.(3.1.104) and rearranging this term, the current of $I_L(s)$ becomes

$$I_L(s) \quad \frac{K_{11}}{s} + \frac{2.C13(s+AB1/2)}{(s+AB1/2)^2 + \frac{4.AB2-AB1^2}{4}} - \frac{2.C14.1/2.\sqrt{4.AB2-AB1^2}}{(s+AB1/2)^2 + \frac{4.AB2-AB1^2}{4}} \qquad (3.1.105)$$

Taking the inverse Laplace transform of this expression we can obtain the load current in time-domain as

$$I_L(t) = AA4/AB2.u(t) + 2.C13.e^{-\frac{AB1.t}{2}}.Cos(CO.t) - 2.C14.e^{-\frac{AB1.t}{2}}.Sin(CO.t) \qquad (3.1.106)$$

(2). Determination of $V_0(t)$

If Eq.(3.1.3) and (3.1.105) are substituted into Eq.(3.1.21), the expression of $V_0(s)$ can be obtained as

$$V_0(s) = 1/C.\frac{1}{s-1/RC}\left\{\left[\frac{AA4}{AB2.s} + \frac{2.C13(s+AB1/2)}{(s+AB1/2)^2 + \frac{4.AB2-AB1^2}{4}} - \frac{2.C14.1/2.\sqrt{4.AB2-AB1^2}}{(s+AB1/2)^2 + \frac{4.AB2-AB1^2}{4}}\right] + \frac{V_{CES}}{s.R} + V_{01}.C\right\} \qquad (3.1.107)$$

$$V_0(s) = \left(\frac{AA4}{C.AB2} + \frac{V_{CES}}{R.C}\right).\frac{1}{s(s+1/RC)} + \frac{(C13.AB1)/C - \frac{C14}{C}\sqrt{4.AB2-AB1^2} + \frac{2C13.s}{C}}{(s+1/RC).\left[(s+AB1/2)^2 + \frac{4.AB2-AB1^2}{4}\right]} + \frac{V_{01}}{s+1/RC} \qquad (3.1.108)$$

The partial fraction expansion of this expression can be achieved easily and it is expressed as

$$V_0(s) = \frac{CA1}{s} + \frac{CA2}{s+1/RC} + \frac{CB1}{s+1/RC} + \frac{CB2.s+CB3}{s^2+AB1.s+AB2} + \frac{V_{01}}{s+1/RC} \qquad (3.1.109)$$

The corresponding residues of Eq.(3.1.109) can be calculated by means of Eq.(3.1.22) and by using Eq.(3.1.108).They can be written as

$$CA1=\left(\frac{AA4}{C.AB2}+\frac{V_{CES}}{R.C}\right).\frac{1}{s+1/RC}\Bigg|_{s=0}=\frac{AA4.R}{AB2}+V_{CES} \tag{3.1.110}$$

$$CA2=\left(\frac{AA4}{C.AB2}+\frac{V_{CES}}{R.C}\right).\frac{1}{s}\Bigg|_{s=-1/RC}=-CA1 \tag{3.1.111}$$

$$CB1=\frac{C13.AB1-C14.\sqrt{4.AB2-AB1^2}+2.C13.s}{C.\left[(s+AB1/2)^2+\frac{4.AB2-AB1^2}{4}\right]}\Bigg|_{s=-1/RC} \tag{3.1.112}$$

$$CB1=\frac{C13.R.(AB1.R.C-2)-2.C14.R^2.C.CO}{AB2.R^2.C^2-AB1.R.C+1} \tag{3.1.113}$$

$$CB2.s-CB3\Big|_{s=-AB1/2+j.CO}=\frac{C13.AB1-C14.2.CO+2.C13.s}{C.(s+1/RC)}\Bigg|_{s=-AB1/2+j.CO} \tag{3.1.114}$$

$$CB2.s-CB3\Big|_{s=-AB1/2-j.CO}=\frac{C13.AB1-C14.2.CO+2.C13.s}{C.(s+1/RC)}\Bigg|_{s=-AB1/2-j.CO} \tag{3.1.115}$$

These residues CB2 and CB3 can be calculated from Eqs.(3.1.114) and (3.1.115) as

$$CB2=-CB1 \tag{3.1.116}$$

$$CB3=\frac{2.CO.C14.R(RC.AB1-2)-4.R^2C.CO^2C13+AB1.CB2(AB2.R^2C^2-AB1.R.C+1)}{2.(AB2.R^2.C^2-AB1.R.C+1)} \tag{3.1.117}$$

If the terms having a denominator with S-1/RC are added, their addition becomes

$$CC = CA2+CB1+V_{01} \tag{3.1.118}$$

Using all the residues which are calculated above, the expression of the output voltage in time-domain can be written by taking the inverse Laplace transform of $V_0(s)$ which is to be obtained by rearranging Eq.(3.1.109). The new expression of $V_0(s)$ becomes

$$V_0(s) = \frac{CA1}{s} + \frac{CC}{s+1/RC} + \frac{CB2.s+CB3}{s^2+AB1.s+AB2} \tag{3.1.119}$$

and

$$V_0(s) = CA1.u(t)+CC.e^{-\frac{t}{R.C}} + \mathcal{L}^{-1}\left(\frac{CB2.s+CB3}{S^2+AB1.s+AB2}\right) \tag{3.1.120}$$

The inverse Laplace transform of the term of

$$\left(\frac{CB2.s+CB3}{s^2+AB1.s+AB2}\right) \tag{3.1.121}$$

can be found like that

At the beginning Eq.(3.1.121) can be written in the form of the partial fraction expansion by determining the roots of the denominator polynomial and it becomes

$$\frac{CB2.s+CB3}{(s+AB1/2+j.CO).(s+AB1/2-j.CO)} = \frac{X_{11}}{s+AB1/2+j.CO} + \frac{X_{12}}{s+AB1/2-j.CO} \tag{3.1.122}$$

The corresponding residues of Eq.(3.1.122) can be calculated by a

similar way which is used before and they can be written as

$$X11 = \left.\frac{CB2.s+CB3}{s+AB1/2-j.CO}\right|_{S=-AB1/2-j.CO} \qquad (3.1.123)$$

$$X11 = \frac{CB2}{2} + j\,\frac{1}{2.CO}\,(CB3-1/2.AB1.CB2) \qquad (3.1.124)$$

$$X12 = \left.\frac{CB2.s+CB3}{s+AB1/2+j.CO}\right|_{s=-AB1/2+j.CO} \qquad (3.1.125)$$

$$X12 = \frac{CB2}{2} - j\,\frac{1}{2.CO}\,(CB3-1/2.AB1.CB2) \qquad (3.1.126)$$

By using the corresponding residues, X_{11} and X_{12}, Eq.(3.1.122) becomes

$$\frac{CB2/2+j.\frac{1}{2.CO}\,(CB3-1/2.AB1.CB2)}{s+AB1/2+j.CO} + \frac{CB/2-j.\frac{1}{2.CO}\,(CB3-1/2.AB1.CB2)}{s+AB1/2-j.CO} \qquad (3.1.127)$$

By taking the inverse Laplace transform of Eq.(3.1.127) and substituting it into Eq.(3.1.120), this expression can be obtained

$$V_O(t) = CA1.u(t) + CC.e^{-t/RC} + \left[CB2/2+j\,\frac{1}{2.CO}(CB3-1/2.AB1.CB2)\right] e^{-(\frac{AB1}{2}+jCO)t}$$

$$+ \left[CB2/2-j\,\frac{1}{2.CO}\,(CB3-1/2.AB1.CB2)\right] e^{-(\frac{AB1}{2}-jCO)t} \qquad (3.1.128)$$

By rearranging Eq.(3.1.128), the load voltage becomes

$$V_0(t) = CA1.u(t) + CC.e^{-t/RC} + CB2.e^{-(AB1.t)/2}.Cos(CO.t) -$$

$$-1/CO.\left(\frac{AB1.CB2}{2} - CB3\right).e^{-(AB1.t)/2}.Sin(CO.t) \qquad (3.1.129)$$

c. The Case of $\triangle > 0$

For this case, the current of $I_L(s)$, Eq.(3.1.40), can be written as

$$I_L(s) = \frac{s^3.AA1 + s^2.AA2 + s.AA3 + AA4}{s.(s-s_2).(s-s_3)} \qquad (3.1.130)$$

Here s_2 and s_3 are the roots of the denominator polynomial and they are defined in Eqs.(3.1.57) and (3.1.58), respectively.

The output voltage, $V_0(s)$, is shown in Eq.(3.1.21). For finding the solutions of these expressions in time-domain, the method which is explained in section(3.1.1) is used here.

(1). Determination of $I_L(t)$

By using Eq.(3.1.130) the current of $I_L(s)$ can be written in the form of the partial fraction expansion as

$$I_L(s) = \frac{DB1}{s} + \frac{DB2}{s-s_2} + \frac{DB3}{s-s_3} \qquad (3.1.131)$$

The corresponding residues of Eq.(3.1.131) can be calculated by means of Eq.(3.1.22) and by using Eq.(3.1.130). The residues, DB1, DB2, and DB3, are obtained like that

$$DB1 \quad \left.\frac{s^3.AA1 + s^2.AA2 + s.AA3 + AA4}{(s-s_2).(s-s_3)}\right|_{s=0} = \frac{AA4}{s_2.s_3} \qquad (3.1.132)$$

By using Eqs.(3.1.57) and (3.1.58),

$$s_2.s_3 = AB2 \qquad (3.1.133)$$

can be found easily.From Eqs.(3.1.132) and (3.1.133)

$$DB1 = AA4/AB2 \tag{3.1.134}$$

can be obtained.

$$DB2 = \left.\frac{s^3.AA1+s^2.AA2+s.AA3+AA4}{s.(s-s_3)}\right|_{s=s_2} \tag{3.1.135}$$

$$DB2 = \frac{(D1+D2).AA1+D3.AA2+D4.AA3+AA4}{D4.D5} \tag{3.1.136}$$

where

$$D0 = 1/2.\sqrt{AB1^2-4.AB2} \tag{3.1.137}$$

$$D1 = AB1/2.(3.AB2-AB1^2) \tag{3.1.138}$$

$$D2 = (AB1^2-AB2).D0 \tag{3.1.139}$$

$$D3 = AB1^2/2-AB2-AB1.D0 \tag{3.1.140}$$

$$D4 = -AB1/2 + D0 \tag{3.1.141}$$

$$D5 = 2.D0 \tag{3.1.142}$$

$$DB3 = \left.\frac{s^3.AA1+s^2.AA2+s.AA3+AA4}{s.(s-s_2)}\right|_{s=s_3} \tag{3.1.143}$$

$$DB3 = -\frac{(D1-D2).AA1+DA2.AA2+DA1.AA3+AA4}{DA1.D5} \tag{3.1.144}$$

where

$$DA1 = -AB1/2-D0 \tag{3.1.145}$$

$$DA2 = AB1^2/2-AB2+AB1.D0 \tag{3.1.146}$$

By using all the residues which are calculated above, the expression of load current in time-domain can be written by taking the inverse Laplace transform of Eq.(3.1.131) as

$$I_L(t) = DB1.u(t)+DB2.e^{s_2.t}+DB3.e^{s_3.t} \qquad (3.1.147)$$

Substituting Eqs.(3.1.57) and (3.1.58) into Eq.(3.1.147) the load current in time-domain becomes

$$I_L(t) = DB1.u(t)+DB2.e^{D4.t}+DB3.e^{DA1.t} \qquad (3.1.148)$$

(2). Determination of $V_0(t)$

If Eq.(3.1.3) and Eq.(3.1.131) are substituted into Eq.(3.1.21), the expression of $V_0(s)$ can be obtained as

$$V_0(s) = \left(\frac{DB1}{s}+\frac{DB2}{s-s_2}+\frac{DB3}{s-s_3}\right).\frac{R}{1+s.C.R}+\left(\frac{V_{CES}}{s.R}+V_{01}.C\right)\frac{R}{1+s.C.R} \qquad (3.1.149)$$

$$V_0(s) = \frac{DB1}{C}\cdot\frac{1}{s.(s+1/RC)}+\frac{DB2}{C}\cdot\frac{1}{(s-s_2).(s+1/RC)}+\frac{DB3}{C}\cdot\frac{1}{(s-s_3).(s+1/RC)}$$

$$+\frac{V_{CES}}{R.C}\cdot\frac{1}{s.(s+1/RC)}+\frac{V_{01}}{s+1/RC} \qquad (3.1.150)$$

The partial fraction expansion of this expression can be achieved easily and it is expressed as

$$V_0(s) = \frac{DC11}{s}+\frac{DC12}{s+1/RC}+\frac{DC21}{s+1/RC}+\frac{DC22}{s-s_2}+\frac{DC31}{s+1/RC}+\frac{DC32}{s-s_3}+\frac{DC41}{s}+$$

$$\frac{DC42}{s+1/RC}+\frac{V_{01}}{S+1/RC} \qquad (3.1.151)$$

The corresponding residues of Eq.(3.1.151) can be calculated by

means of Eq.(3.1.22) and by using Eq.(3.1.150).They can be written as

$$DC11 = DB1.R \tag{3.1.152}$$

$$DC12 = -DC11 \tag{3.1.153}$$

$$DC21 = -\frac{DB2.R}{1+R.C.D4} \tag{3.1.154}$$

$$DC22 = -DC21 \tag{3.1.155}$$

$$DC31 = -\frac{DB3.R}{1+DA1.R.C} \tag{3.1.156}$$

$$DC32 = -DC31 \tag{3.1.157}$$

$$DC41 = V_{CES} \tag{3.1.158}$$

$$DC42 = -DC41 \tag{3.1.159}$$

If the terms having a denominator with s and s+1/RC are added , their additions become

$$DD1 = DC11+DC41 \tag{3.1.160}$$

$$DD2 = DC12+DC21+DC31+DC42+V_{01} \tag{3.1.161}$$

respectively.

By using all the residues which are calculated above and the related expressions,the expression of the output voltage in time-domai can be written by taking the inverse Laplace transform of $V_0(s)$ which is obtained by rearranging Eq.(3.1.151).The new expression of $V_0(s)$ becomes

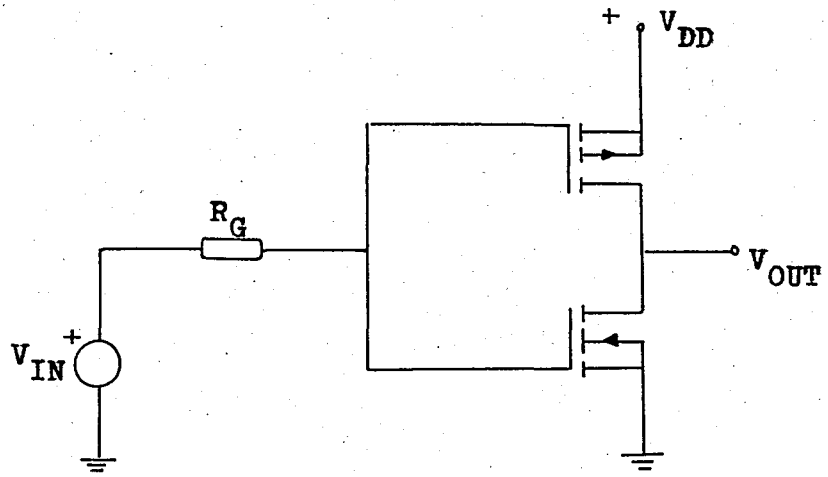
$$V_0(s) = \frac{DD1}{s} + \frac{DD2}{s+1/RC} + \frac{DC22}{s-s_2} + \frac{DC32}{s-s_3} \tag{3.1.162}$$

and

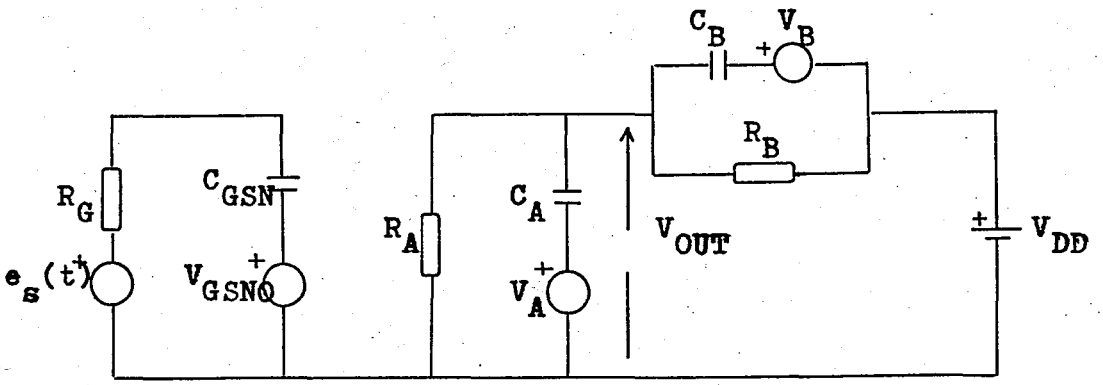
$$V_0(t) = DD1.u(t)+DD2.e^{-t/RC}+DC22.e^{D4.t}+DC32.e^{DA1.t} \tag{3.1.163}$$

3.2. Analysis of Complementary VDMOS Inverter

By using the time-variant linear models of the n-channel and p-channel VDMOS transistors in the complementary VDMOS inverter circuit which is shown in Figure(3.6),an equivalent circuit which contains the initial conditions of the gate to source and the drain to source time-variant capacitors of the n- and p- channel VDMOS transistors is obtained and it is shown in Figure(3.7).



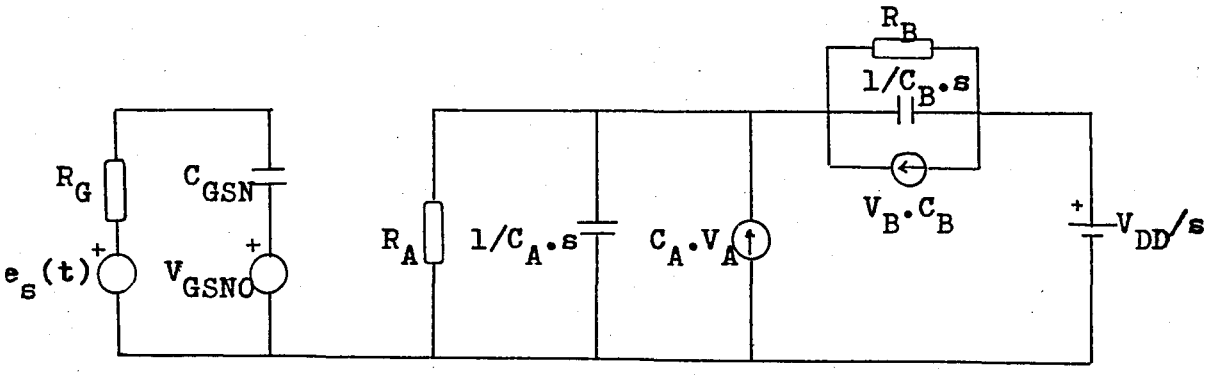
FIGURE(3.6) A complementary VDMOS inverter circuit



FIGURE(3.7) Equivalent linear model of the CVDMOS inverter circuit

A new circuit which is shown in Figure(3.8) can be obtained by using the current equivalences of the voltage sources and Laplace

transforms of the circuit parameters of the output side of the circuit which is shown in Figure(3.7).



FIGURE(3.8) Equivalent circuit which is obtained by using the Laplace transform method and network theorems in the circuit shown in Figure(3.7)

In the above circuits the meanings of the circuit parameters are explained in Table(3.1).

TABLE 3.1 Explanation of CVDMOS inverter equivalent circuit parameters

Parameter	Explanation
R_A	N-channel VDMOST drain to source resistance
R_B	P-channel VDMOST drain to source resistance
C_A	N-channel VDMOST drain to source capacitance
C_B	P-channel VDMOST drain to source capacitance
V_A	N-channel VDMOST previous drain to source voltage
V_B	P-channel VDMOST previous drain to source voltage

By using the voltage equivalences of the current sources at the output side of the circuit which is shown in Figure(3.8) the circuit to be used in the analysis is obtained and it is shown in Figure(3.9).

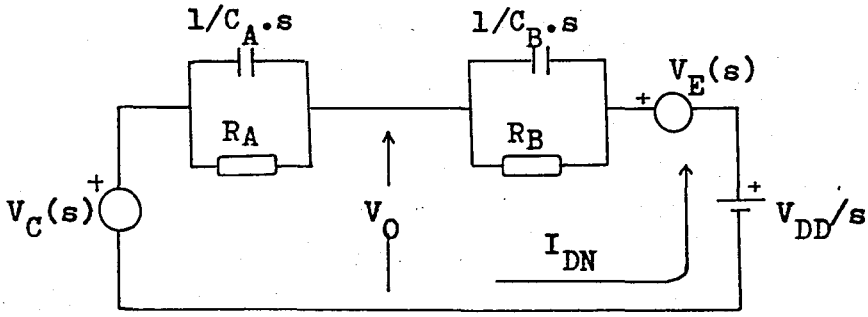
In this circuit,the voltages of $V_C(s)$ and $V_E(s)$ are defined as

$$V_C(s) = C_A \cdot V_A \frac{1}{1/R_A + C_A \cdot s} \tag{3.2.1}$$

and

$$V_E(s) = C_B \cdot V_B \frac{1}{1/R_B + C_B \cdot s} \tag{3.2.2}$$

respectively.



FIGURE(3.9) The circuit to be used in the analysis

The drain to source current and voltage of the n-channel VDMOST in this inverter are defined as the load current and output voltage, respectively.The expressions of the load current and output voltage in time-domain are obtained by means of this analysis.

The load current of this inverter can be calculated like that

$$I_{DN}(s) = \frac{V_{DD}/s + V_E(s) - V_C(s)}{\dfrac{1}{1/R_A + C_A \cdot s} + \dfrac{1}{1/R_B + C_B \cdot s}} \tag{3.2.3}$$

$$I_{DN}(s) = \frac{\left[V_{DD}/s + V_E(s) - V_C(s)\right] \cdot (s^2 C_A \cdot R_A \cdot C_B \cdot R_B + s(C_A \cdot R_A + C_B \cdot R_B) + 1)}{s \cdot (C_B \cdot R_B \cdot R_A + C_A \cdot R_A \cdot R_B) + (R_A + R_B)} \tag{3.2.4}$$

If Eq.(3.2.1) is rewritten,the expression of $V_C(s)$ becomes

$$V_C(s)=\frac{R_A.C_A.V_A}{1+s.R_A.C_A} \qquad (3.2.5)$$

If the denominator and numerator of Eq.(3.2.5) are divided by $R_A.C_A$, this expression can be obtained

$$V_C(s)=\frac{V_A}{s+1/(R_A.C_A)} \qquad (3.2.6)$$

Similarly,the expression of $V_E(s)$ can be written as

$$V_E(s)=\frac{V_B}{s+1/(R_B.C_B)} \qquad (3.2.7)$$

In Eqs.(3.2.6),(3.2.7),and (3.2.4) some abbreviations are used and they are given below.

$$A1=1/(R_A.C_A) \qquad (3.2.8)$$

$$A2=1/(R_B.C_B) \qquad (3.2.9)$$

$$A3=C_A.R_A.R_B+C_B.R_B.R_A \qquad (3.2.10)$$

$$A4=R_A+R_B \qquad (3.2.11)$$

$$A5=C_A.R_A+C_B.R_B \qquad (3.2.12)$$

$$A6=C_A.C_B.R_A.R_B \qquad (3.2.13)$$

$$A7=A4/A3 \qquad (3.2.14)$$

Substituting the abbreviations which are defined in Eqs.(3.2.8) to (3.2.14) into the related expressions,the load current can be written like that

$$I_{DN}(s)=\frac{V_{DD}/s+V_B\frac{1}{s+A2}-V_A\frac{1}{s+A1}\cdot(s^2.A6+s.A5+1)}{s.A3+A4} \quad (3.2.15)$$

By rearranging Eq.(3.2.15) and by using the related abbreviations for the constant terms,the expression of the load current can be obtained as

$$I_{DN}(s)=\frac{D4.s^4+D3.s^3+D2.s^2+D1.s+D0}{s.(s+A1).(s+A2).(s+A7)} \quad (3.2.16)$$

where

$$D0 = B0/A3 \quad (3.2.17)$$

$$B0 = V_{DD}.A1.A2 \quad (3.2.18)$$

$$D1 = B1/A3 \quad (3.2.19)$$

$$B1 = V_{DD}.(A1+A2+A1.A2.A5)+V_B.A1-V_A.A2 \quad (3.2.20)$$

$$D2 = B2/A3 \quad (3.2.21)$$

$$B2 = V_{DD}.(1+A2.A5+A1.A5+A1.A2.A6)+V_B(1+A1.A5)-V_A(1+A2.A5) \quad (3.2.22)$$

$$D3 = B3/A3 \quad (3.2.23)$$

$$B3 = V_{DD}.(A5+A1.A6+A2.A6)+V_B.(A5+A1.A6)-V_A.(A5+A2.A6) \quad (3.2.24)$$

$$D4 = B4/A3 \quad (3.2.25)$$

$$B4 = A6.(V_{DD}-V_A+V_B) \quad (3.2.26)$$

By means of Figure(3.9),the expression of the output voltage for CVDMOS inverter can be written as

$$V_O(s) = I_{DN}(s) \frac{1}{1/R_A + s.C_A} + V_C(s) \qquad (3.2.27)$$

If Eq.(3.2.27) is rewritten,the expression of the output voltage becomes

$$V_O(s) = I_{DN}(s).1/C_A \cdot \frac{1}{s+1/(R_A.C_A)} + V_C(s) \qquad (3.2.28)$$

3.2.1. Determination of $I_{DN}(t)$

Using Eq.(3.2.16) the current of $I_{DN}(s)$ can be written in the form of the partial fraction expansion as

$$I_{DN}(s) = \frac{F1}{s} + \frac{F2}{s+A1} + \frac{F3}{s+A2} + \frac{F4}{s+A7} \qquad (3.2.29)$$

By means of Eq.(3.2.16) and Eq.(3.2.29) and by using Eq.(3.1.22) the corresponding residues of $I_{DN}(s)$ can be obtained as shown below

$$F1 = DO/(A1.A2.A7) \qquad (3.2.30)$$

$$F2 = \frac{D4.A1^4 - D3.A1^3 + D2.A1^2 - D1.A1 + DO}{A1.(A1-A2).(A7-A1)} \qquad (3.2.31)$$

$$F3 = \frac{D4.A2^4 - D3.A2^3 + D2.A2^2 - D1.A2 + DO}{A2.(A2-A1).(A7-A2)} \qquad (3.2.32)$$

$$F4 = \frac{D4.A7^4 - D3.A7^3 + D2.A7^2 - D1.A7 + DO}{A7.(A7-A1).(A2-A7)} \qquad (3.2.33)$$

Using all the residues which are calculated above,the value of the load current in time-domain can be determined easily.The inverse Laplace transform of $I_{DN}(s)$ can be obtained as

$$I_{DN}(t) = F1.u(t) + F2.e^{-A1.t} + F3.e^{-A2.t} + F4.e^{-A7.t} \qquad (3.2.34)$$

3.2.2. Determination of $V_0(t)$

If Eqs.(3.2.6) and (3.2.16) are substituted into Eq.(3.2.28), the expression of $V_0(s)$ can be obtained as

$$V_0(s)=\frac{D4.s^4+D3.s^3+D2.s^2+D1.s+D0}{C_A.s.(s+A1).(s+A2).(s+A7).(s+1/(R_A.C_A))}+V_A\frac{1}{s+1/(R_A.C_A)} \qquad (3.2.35)$$

By using the related abbreviations in Eq.(3.2.35),the expression of $V_0(s)$ becomes

$$V_0(s)=\frac{E4.s^4+E3.s^3+E2.s^2+E1.s+E0}{s.(s+A1)^2.(s+A2).(s+A7)}+\frac{V_A}{s+A1} \qquad (3.2.36)$$

where

$$E0=D0/C_A \qquad (3.2.37)$$

$$E1=D1/C_A \qquad (3.2.38)$$

$$E2=D2/C_A \qquad (3.2.39)$$

$$E3=D3/C_A \qquad (3.2.40)$$

$$E4=D4/C_A \qquad (3.2.41)$$

Eq.(3.2.36) can be rewritten in the form of the partial fraction expansion for taking the inverse Laplace Transform.

$$V_0(s)=\frac{H1}{s}+\frac{H2}{s+A1}+\frac{H3}{(s+A1)^2}+\frac{H4}{s+A2}+\frac{H5}{s+A7}+\frac{V_A}{s+A1} \qquad (3.2.42)$$

The corresponding residues of Eq.(3.2.42) can be calculated by using

Eqs.(3.1.22) and (3.1.23) and Eq.(3.2.36).They are obtained as shown below

$$H1=\frac{E0}{A1^2.A2.A7} \tag{3.2.43}$$

$$H2=\frac{A1^6.E4-2.A1^5.E4.(A2+A7)+A1^4.\left[E3.(A2+A7)+3.E4.A2.A7-E2\right]}{-A1^3.(2.E3.A2.A7-2.E1)+A1^2\left[E2.A2.A7-E1.(A2+A7)-3.E0\right]}$$

$$\frac{+2.A1.E0.(A2+A7)-E0.A2.A7}{\left[A1.(A1-A2).(A7-A1)\right]^2} \tag{3.2.44}$$

$$H3=\frac{E4.A1^4-E3.A1^3+E2.A1^2-E1.A1+E0}{A1.(A1-A2).(A7-A1)} \tag{3.2.45}$$

$$H4=\frac{E4.A2^4-E3.A2^3+E2.A2^2-E1.A2+E0}{A2.(A1-A2)^2.(A2-A7)} \tag{3.2.46}$$

$$H5=\frac{E4.A7^4-E3.A7^3+E2.A7^2-E1.A7+E0}{A7.(A1-A7)^2.(A7-A2)} \tag{3.2.47}$$

If the terms having a denominator with s+A1 are added,their addition becomes

$$H6=H2+V_A \tag{3.2.48}$$

Finally $V_0(s)$ becomes

$$V_0(s)=\frac{H1}{s}+\frac{H6}{s+A1}+\frac{H3}{(s+A1)^2}+\frac{H4}{s+A2}+\frac{H5}{s+A7} \tag{3.2.49}$$

The inverse Laplace transform of $V_0(s)$ is equal to

$$V_0(t)=H1.u(t)+H6.e^{-A1.t}+H3.t.e^{-A1.t}+H4.e^{-A2.t}+H5.e^{-A7.t} \tag{3.2.50}$$

3.3. COMPUTER PROGRAM DESCRIPTION

The time-variant linear large-signal BJT,VVMOS,and VDMOS models and model parameters have been explained in the second chapter.The analyses of the transistor switching circuits with RLC load and CVDMOS inverter which are driven by the square wave signal source have been done for obtaining the expressions related to their load currents and output voltages in the third chapter.

By using the proposed transistor models,the model parameters, and the related expressions,one-period variations of the load currents and output voltages of the circuits which are expressed above can be calculated by changing the corresponding model elements with the time intervals of DELT as depending on the operating regions.At the beginning of all the calculations,the initial conditions which are related to the transistor parameters and circuit elements must be determined.The expressions of the load current and output voltage which are obtained in the third chapter and are used by putting DELT instead of t,can be solved each time with the results of their previous calculations taken as the initial conditions.The linear equivalent circuits of the transistor switching circuits which include the corresponding transistor models are the same formally in all the operating regions beyond the values of the model elements.

The number of calculations is equal to the number of points taken during the switching time.During the calculations one-step integration error must be controlled.If the error is high,the time interval,DELT,must be reduced,if not,by increasing the time interval time wasting can be prevented.

For determining the output voltage and load current of the BJT switching circuits the corresponding switching times and model

parameters which are expressed in sections (2.3.1) and (2.3.2), respectively,must be determined at the beginning.For all the operating regions the time-variant functions of the BJT output resistance and capacitance are given in section (2.2).One-period variations of the load currents and output voltages of the BJT switching circuits can be calculated by using the expressions of the model elements and the switching times corresponding to the every operating region.

For determining the output voltages and load currents of the VVMOS and VDMOS switching circuits the corresponding transistor and model parameters which are explained in sections (2.6) and (2.8), respectively,must be determined at the beginning.The input side of the model which is developed for the VVMOS and VDMOS transistors in section (2.5) is used for determining the operating region and the value of the drain to source resistance beyond the cut-off region. The variations of the load currents and output voltages can be obtained for every region,separatively,by using the adequate values of the model elements.

For determining one-period variations of the drain to source currents and voltages of a CVDMOS inverter both of the n- and p-channel enhancement mode VDMOS transistor models are used together. The drain to source voltage and current expressions have been obtained in section (3.2).The computer program description is similar to that of VVMOS-or VDMOS-switching circuit in general.

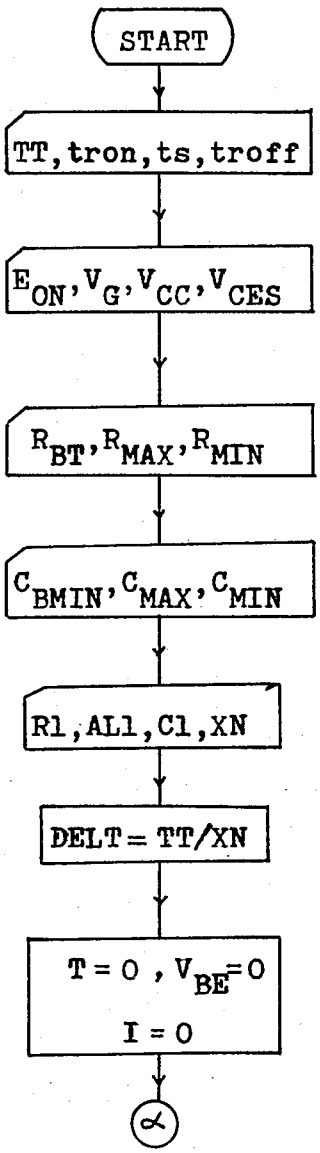
The switching times of the VVMOS-or VDMOS- switching circuit and CVDMOS inverter can be calculated easily from the time values at which it passes from one region to the other region within one-period interval.

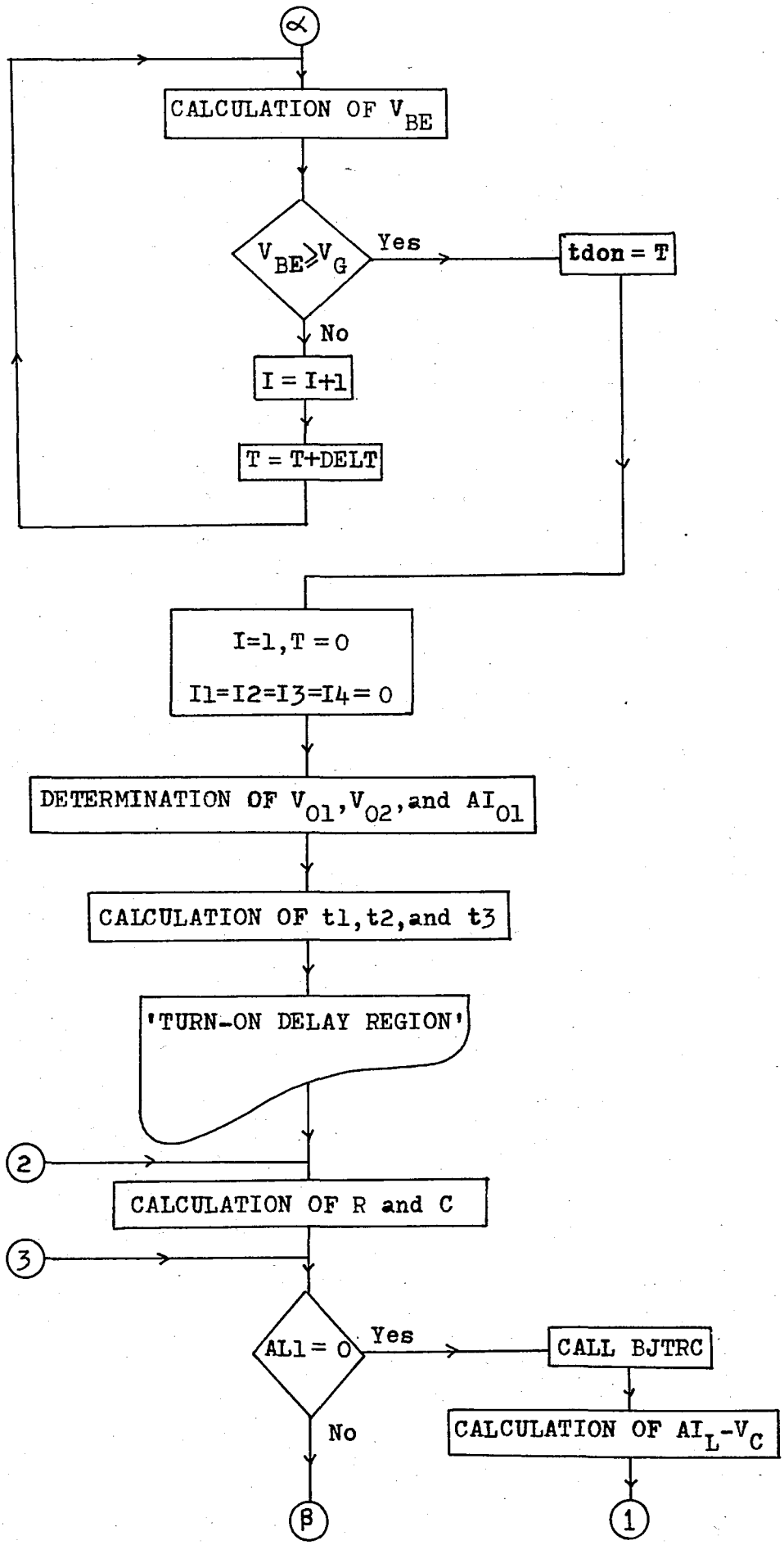
In the computer programs,only resulting curves or both the

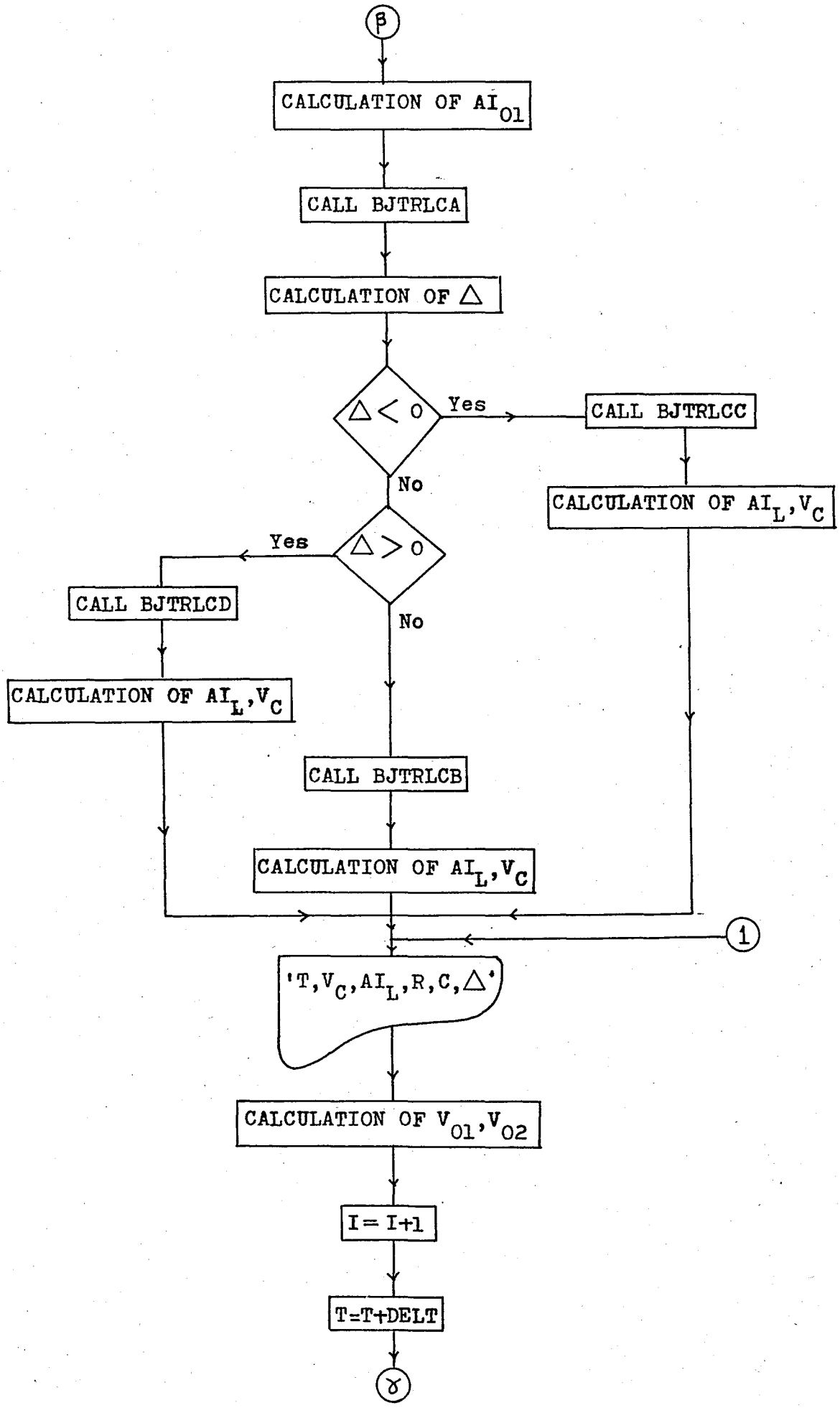
related values and curves can be obtained at the output as depending on the state of switch,SW,which is used for this purpose.

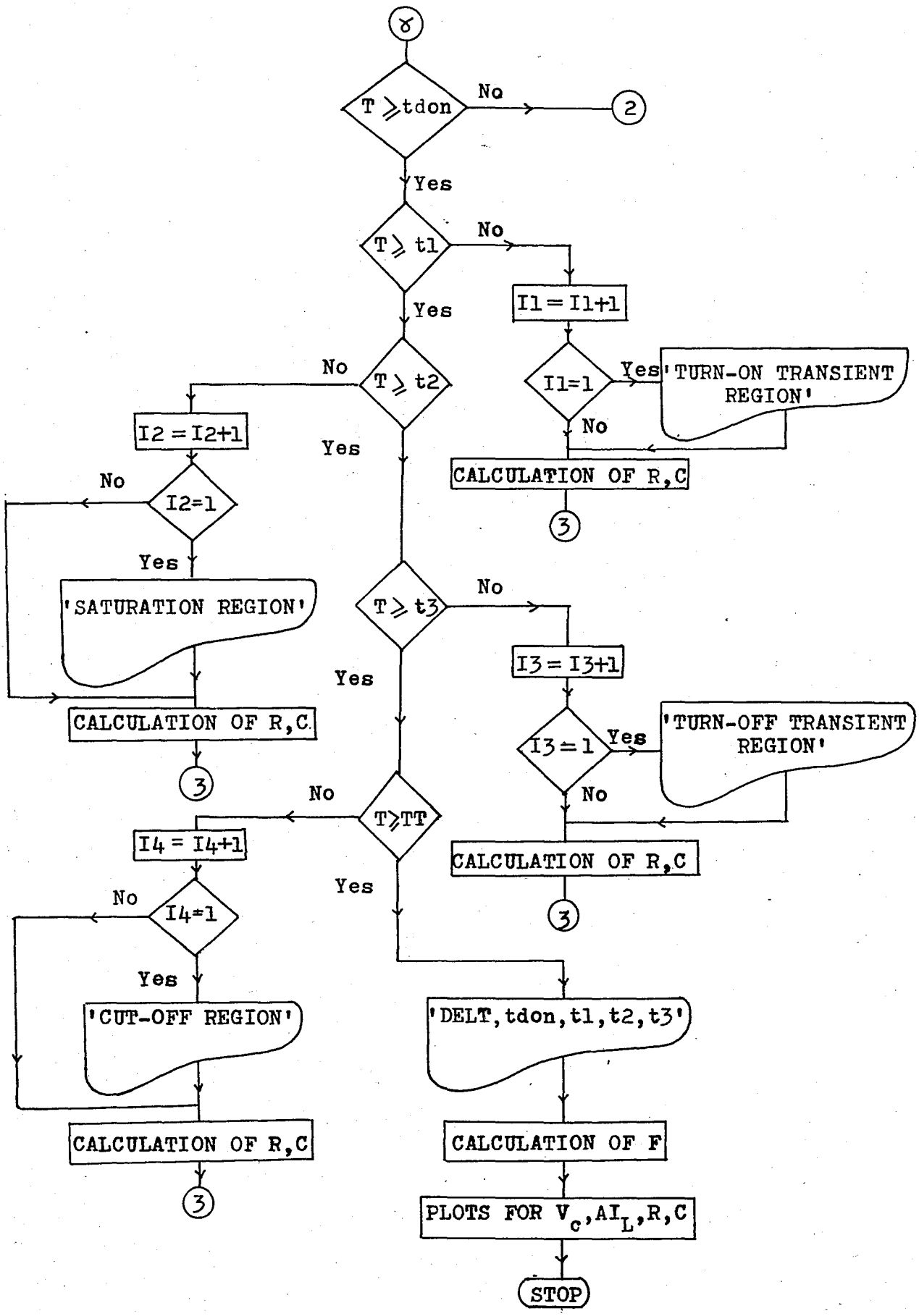
The flowcharts related to the computer programs of the BJT and VVMOS-or VDMOS- switching circuits and CVDMOS inverter are given, separately,in the following sections.Flowcharts for the subroutines are not prepared but all subroutines are given in Appendix-C together with the computer programs.

3.3.1. Flowchart Related to the Computer Simulation of BJT Switching Circuit with RLC Load

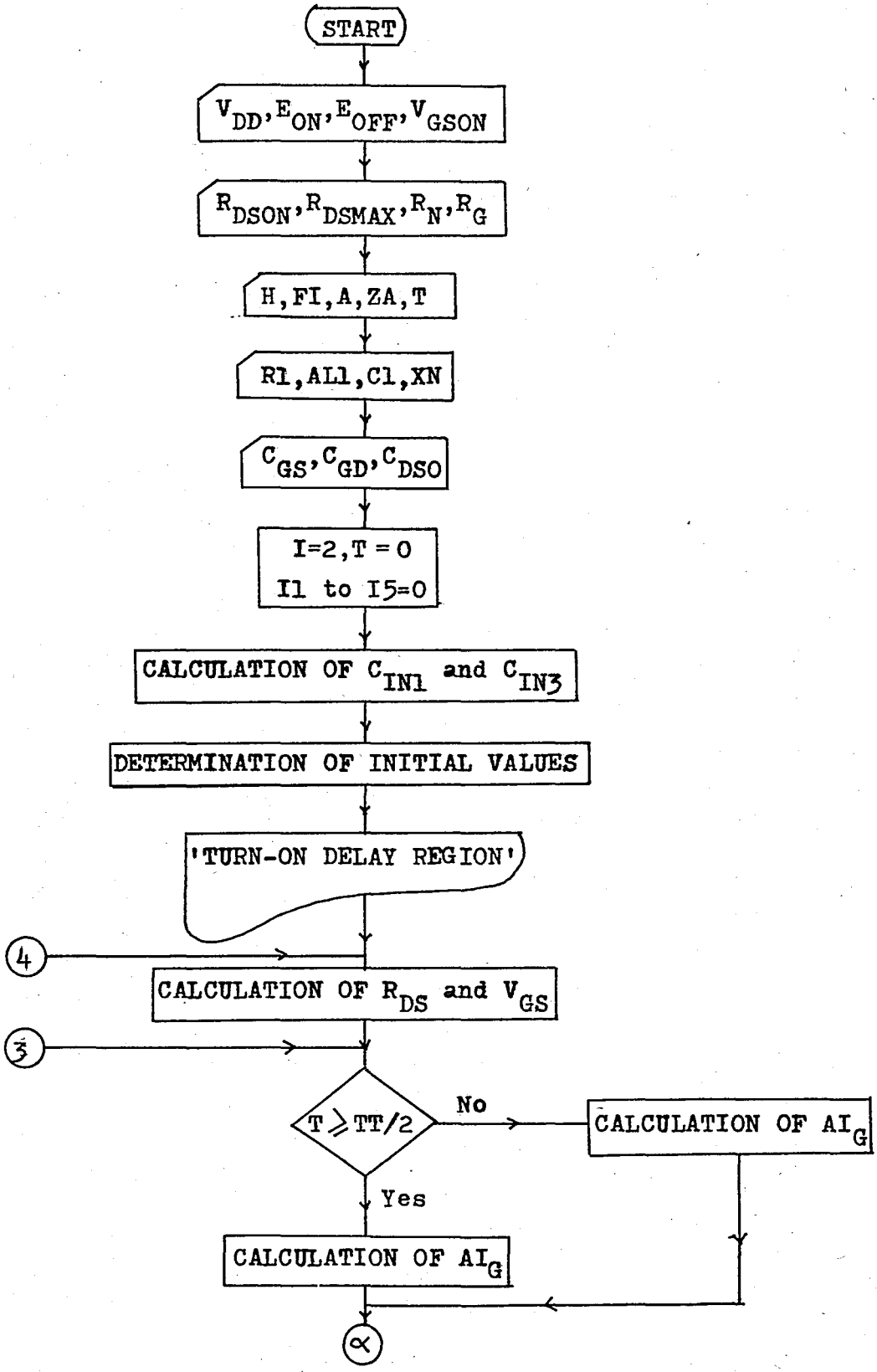


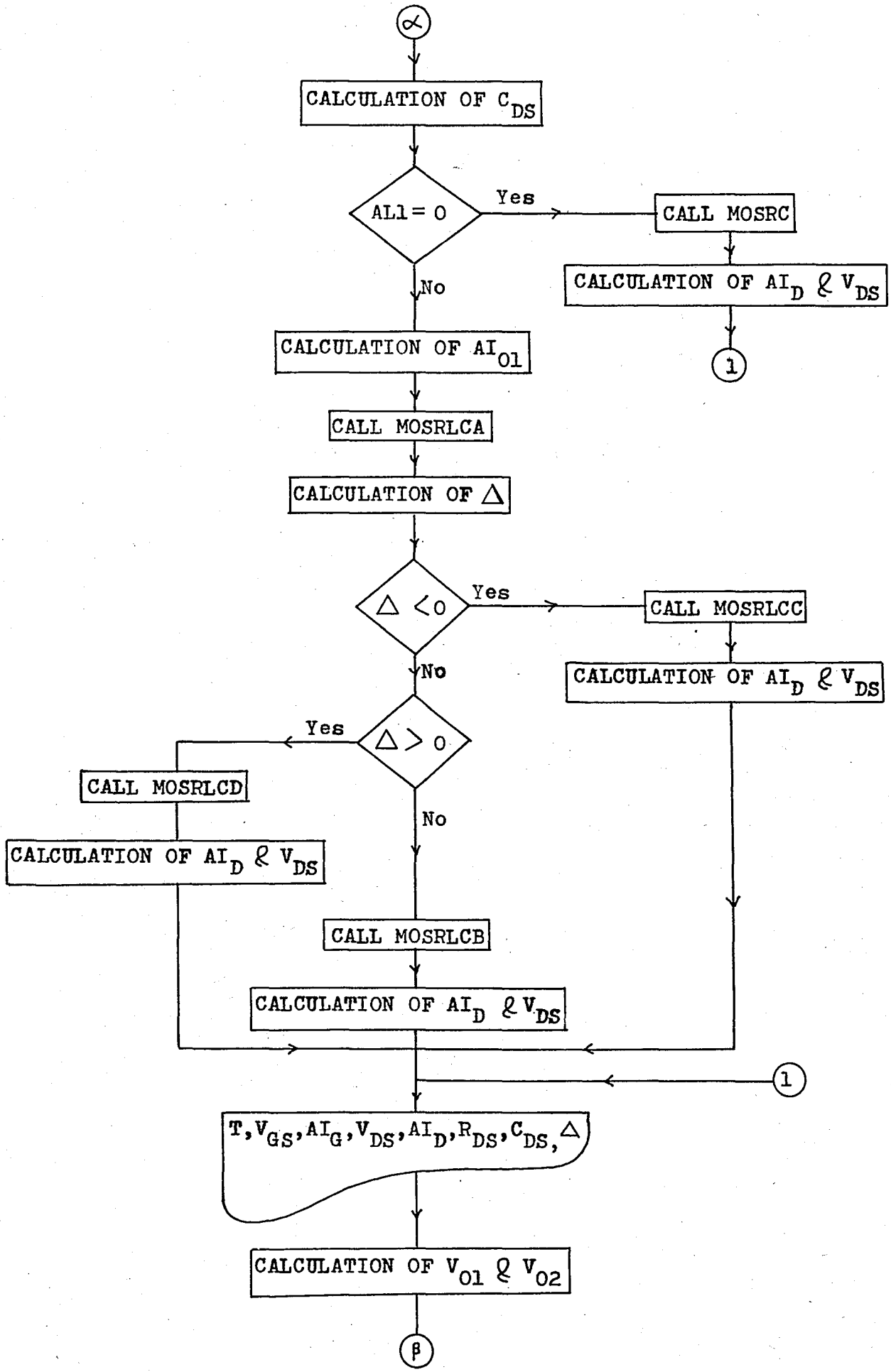

∝
CALCULATION OF V_{BE}
$V_{BE} \geq V_G$
Yes
tdon = T
No
I = I+1
T = T+DELT
I=1, T = 0
I1=I2=I3=I4= 0
DETERMINATION OF V_{O1}, V_{O2}, and AI_{O1}
CALCULATION OF t1, t2, and t3
'TURN-ON DELAY REGION'
2
CALCULATION OF R and C
3
AL1 = 0
Yes
CALL BJTRC
CALCULATION OF AI_L-V_C
No
β
1

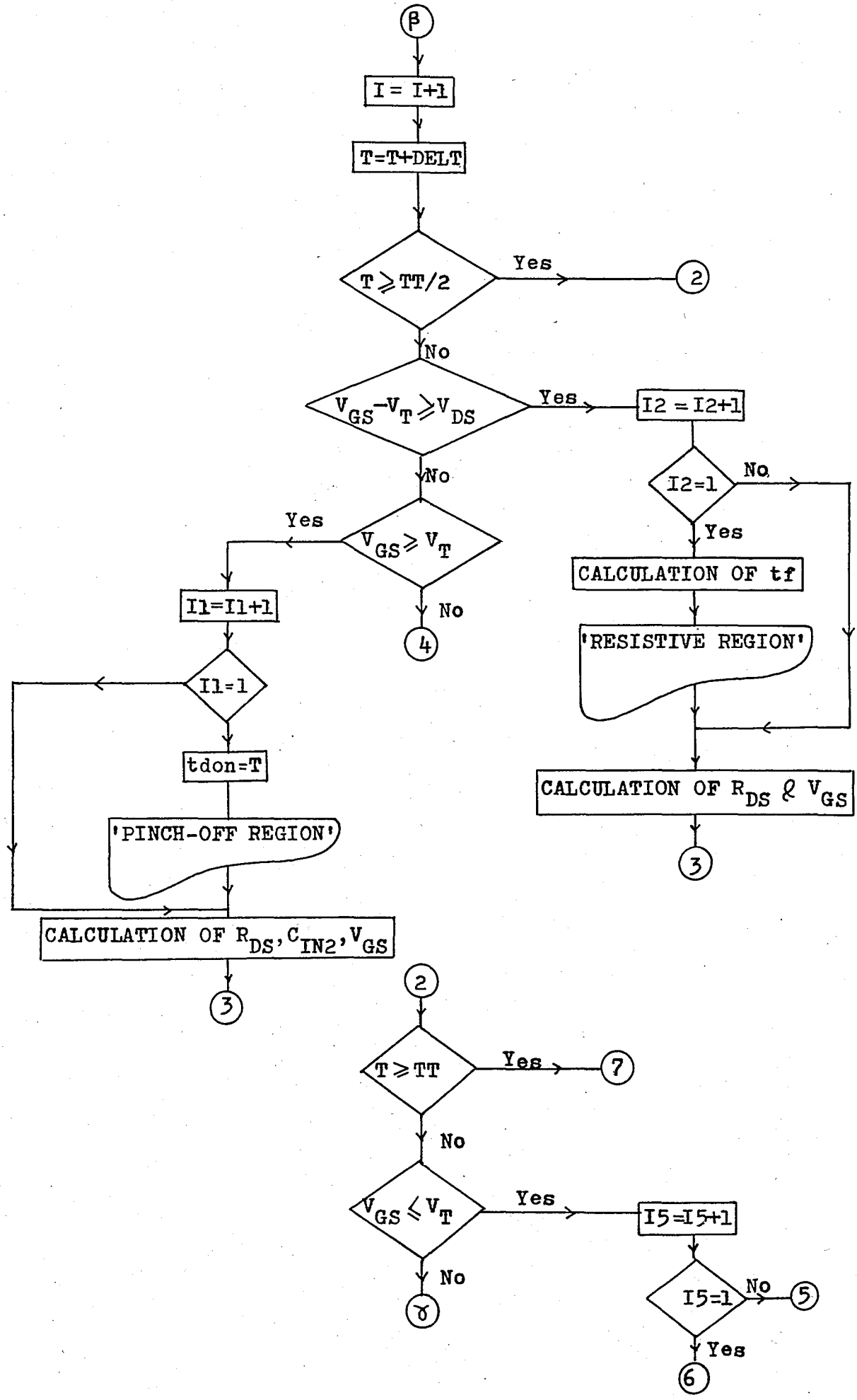

β
CALCULATION OF AI01
CALL BJTRLCA
CALCULATION OF △
△ < 0
Yes
CALL BJTRLCC
CALCULATION OF AIL,VC
No
△ > 0
Yes
CALL BJTRLCD
CALCULATION OF AIL,VC
No
CALL BJTRLCB
CALCULATION OF AIL,VC
1
'T,VC,AIL,R,C,△'
CALCULATION OF V01,V02
I= I+1
T=T+DELT
γ

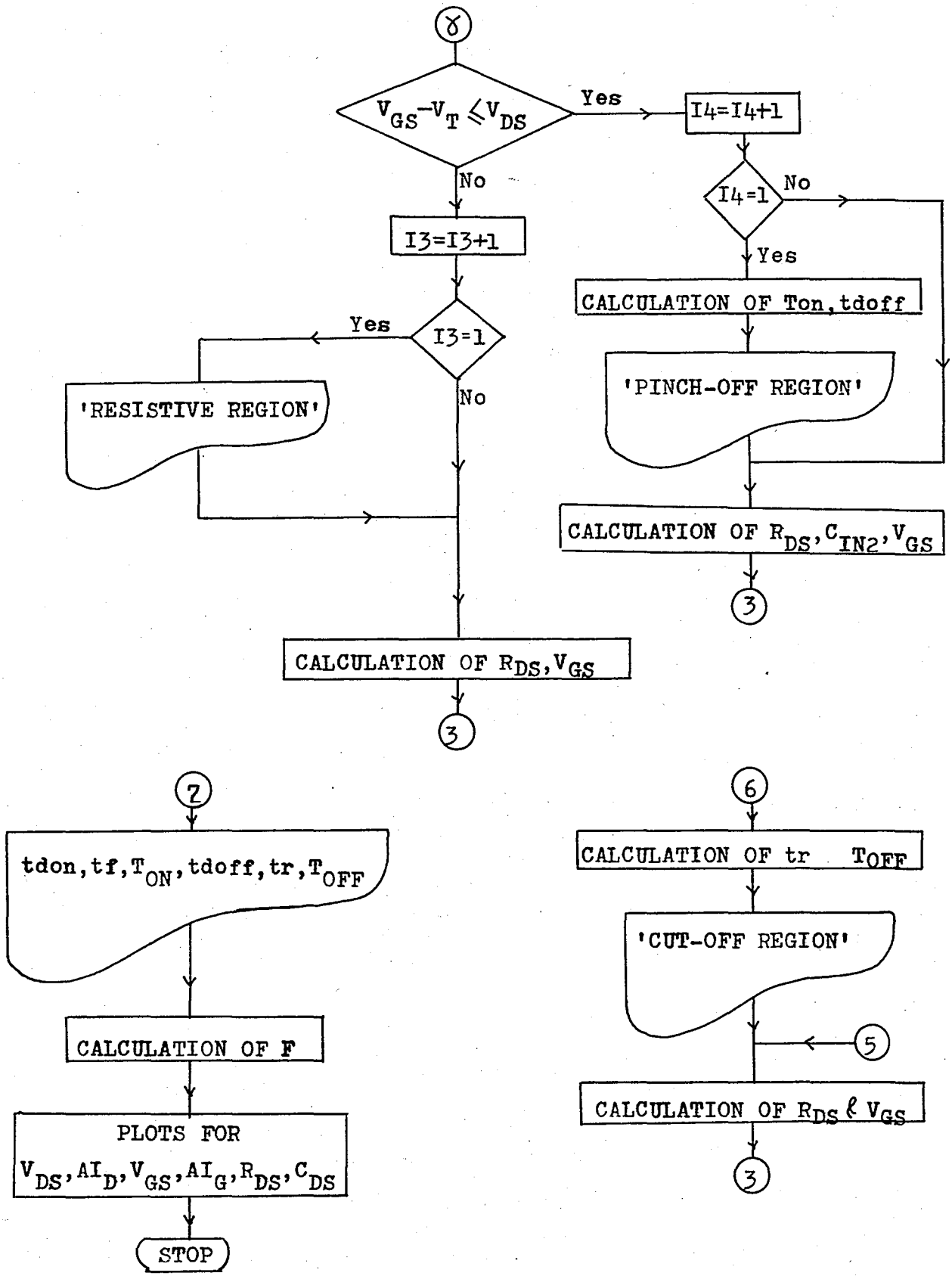

γ
T ⩾ tdon
No
2
Yes
T ⩾ t1
No
I1 = I1+1
Yes
I1=1
Yes
'TURN-ON TRANSIENT REGION'
No
CALCULATION OF R,C
3
T ⩾ t2
No
Yes
I2 = I2+1
No
I2=1
Yes
'SATURATION REGION'
CALCULATION OF R,C
3
T ⩾ t3
No
Yes
I3 = I3+1
I3=1
Yes
'TURN-OFF TRANSIENT REGION'
No
CALCULATION OF R,C
3
T⩾TT
No
Yes
I4 = I4+1
No
I4=1
Yes
'CUT-OFF REGION'
CALCULATION OF R,C
3
'DELT,tdon,t1,t2,t3'
CALCULATION OF F
PLOTS FOR V_c,AI_L,R,C
STOP

3.3.2. Flowchart Related to the Computer Simulation of VVMOS and VDMOS Switching Circuit with RLC Load

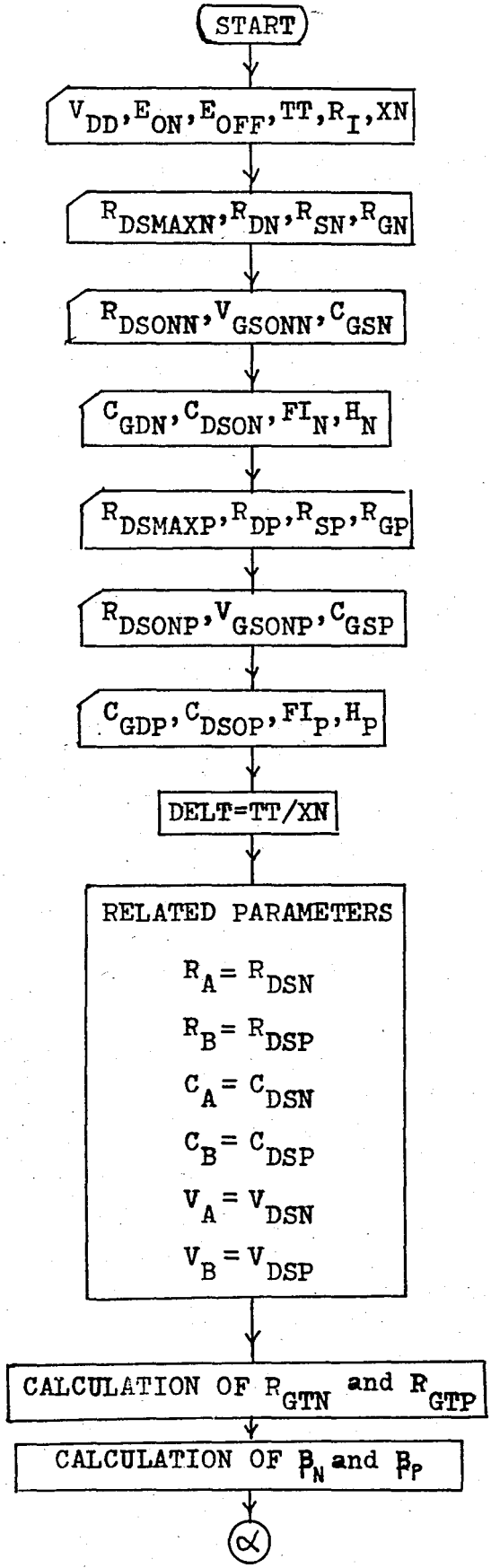


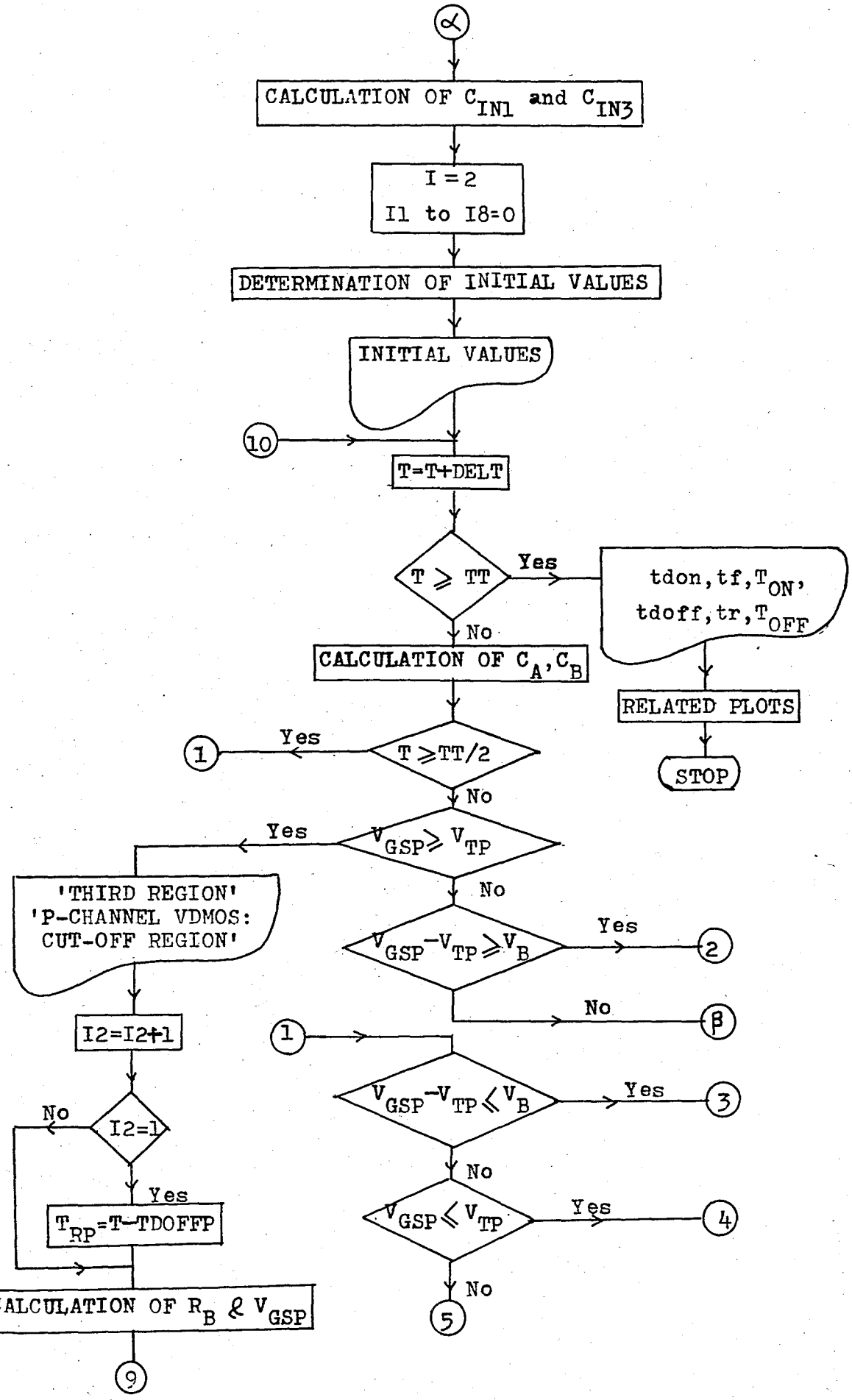

α
CALCULATION OF C_{DS}
ALl = 0
Yes
CALL MOSRC
CALCULATION OF AI_D & V_{DS}
1
No
CALCULATION OF AI_{01}
CALL MOSRLCA
CALCULATION OF Δ
Δ < 0
Yes
CALL MOSRLCC
CALCULATION OF AI_D & V_{DS}
No
Δ > 0
Yes
CALL MOSRLCD
CALCULATION OF AI_D & V_{DS}
No
CALL MOSRLCB
CALCULATION OF AI_D & V_{DS}
1
T, V_{GS}, AI_G, V_{DS}, AI_D, R_{DS}, C_{DS}, Δ
CALCULATION OF V_{01} & V_{02}
β

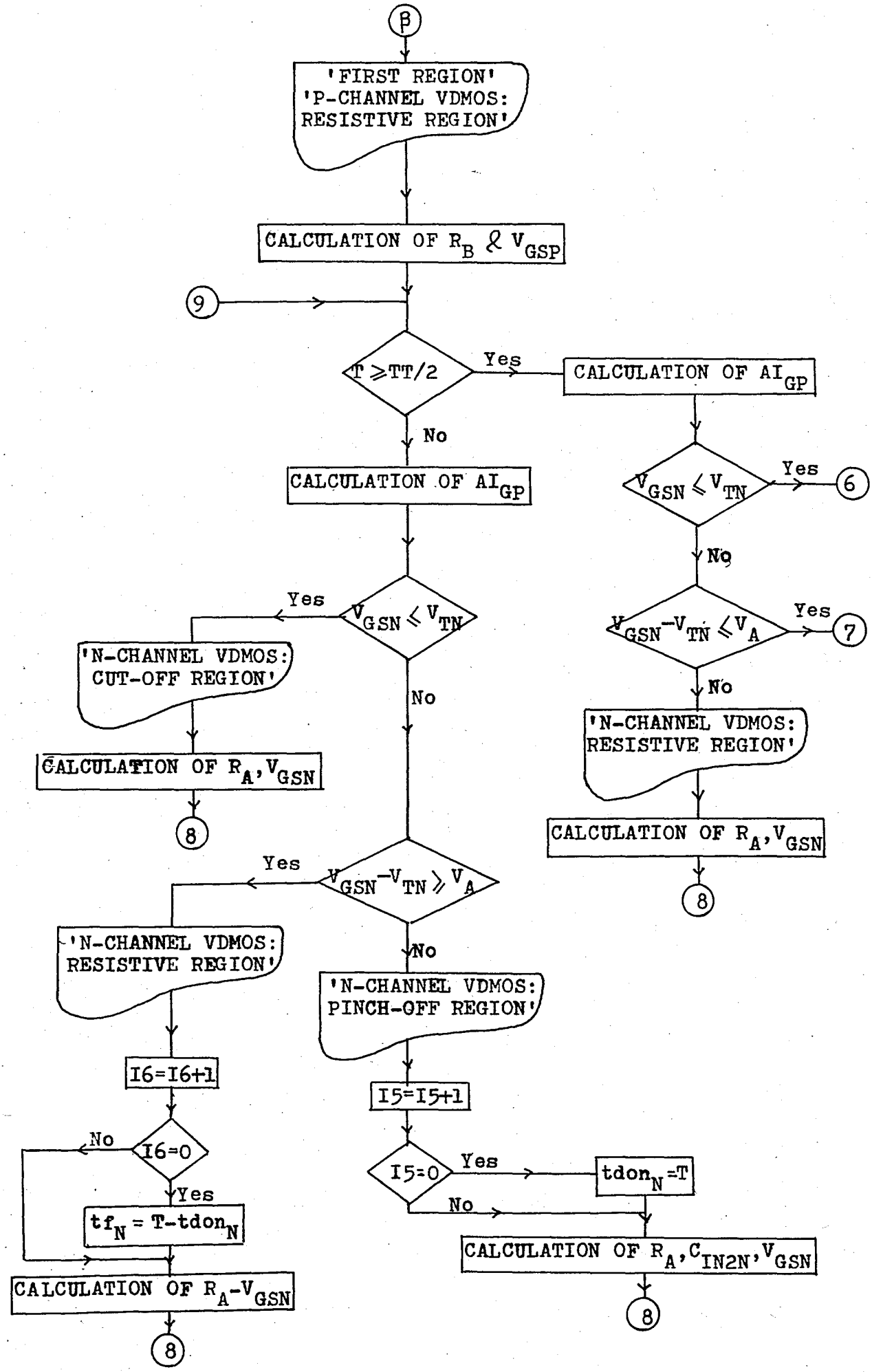

β
I = I+1
T=T+DELT
T ≥ TT/2
Yes
2
No
VGS−VT ≥ VDS
Yes
I2 = I2+1
No
I2=1
No
Yes
CALCULATION OF tf
'RESISTIVE REGION'
CALCULATION OF RDS & VGS
3
VGS ≥ VT
Yes
No
4
I1=I1+1
I1=1
tdon=T
'PINCH-OFF REGION'
CALCULATION OF RDS, CIN2, VGS
3
2
T ≥ TT
Yes
7
No
VGS ≤ VT
Yes
I5=I5+1
No
γ
I5=1
No
5
Yes
6

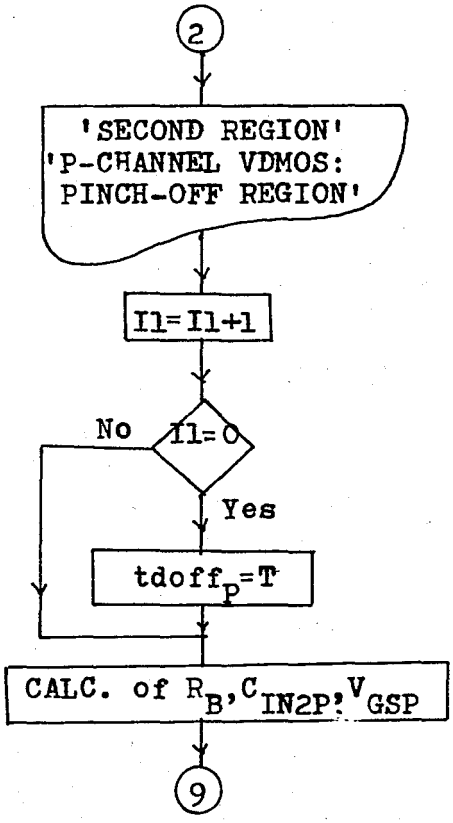

8
$V_{GS}-V_T \leq V_{DS}$
Yes
I4=I4+1
No
I3=I3+1
I4=1
No
Yes
CALCULATION OF Ton, tdoff
Yes
I3=1
'PINCH-OFF REGION'
'RESISTIVE REGION'
No
CALCULATION OF R_{DS}, C_{IN2}, V_{GS}
3
CALCULATION OF R_{DS}, V_{GS}
3
7
tdon, tf, T_{ON}, tdoff, tr, T_{OFF}
6
CALCULATION OF tr T_{OFF}
'CUT-OFF REGION'
5
CALCULATION OF F
CALCULATION OF R_{DS} & V_{GS}
PLOTS FOR
$V_{DS}, AI_D, V_{GS}, AI_G, R_{DS}, C_{DS}$
3
STOP

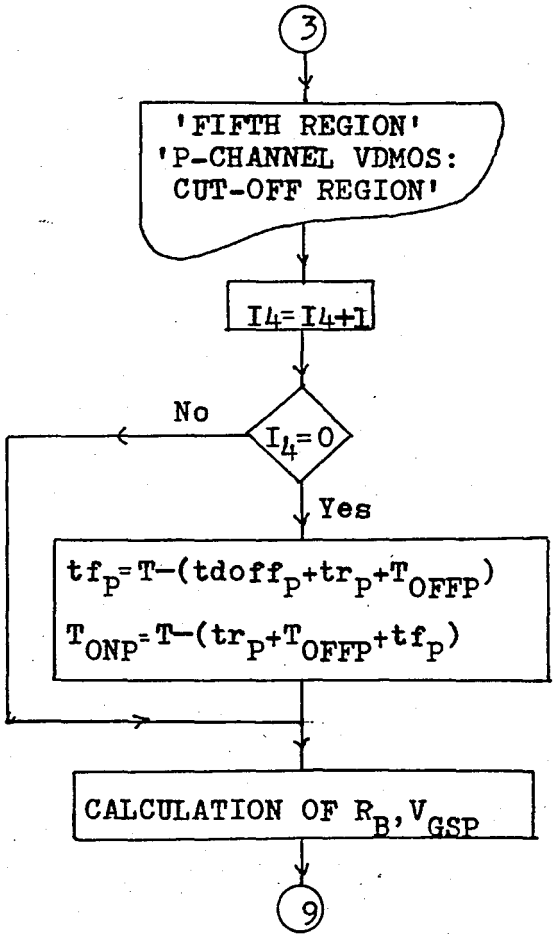
3.3.3. Flowchart Related to the Computer Simulation of CVDMOS Inverter

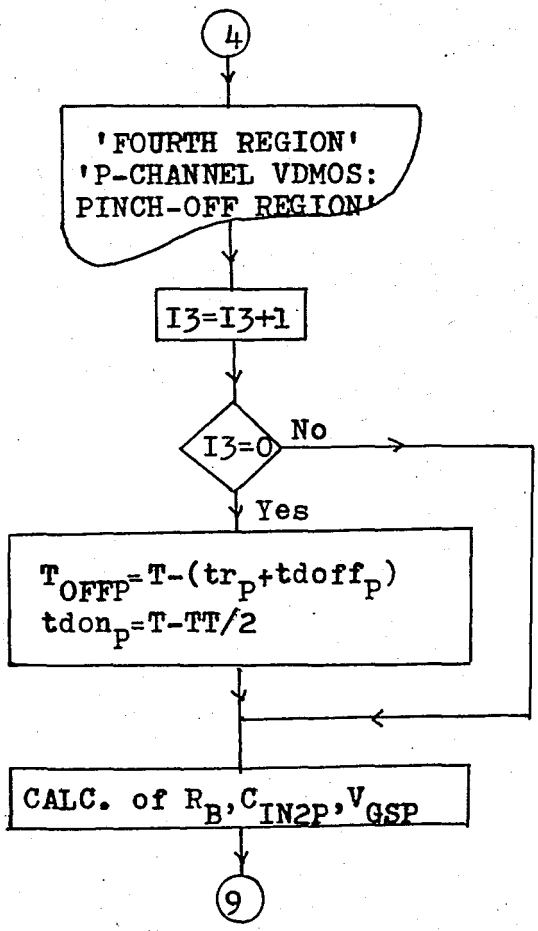


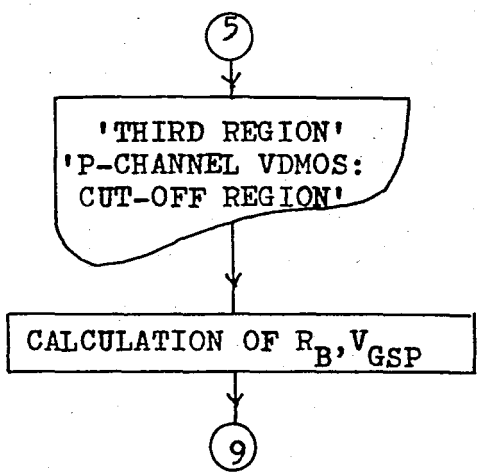

α
CALCULATION OF C_{IN1} and C_{IN3}
I = 2
I1 to I8=0
DETERMINATION OF INITIAL VALUES
INITIAL VALUES
10
T=T+DELT
T ⩾ TT
Yes
tdon, tf, T_{ON}, tdoff, tr, T_{OFF}
RELATED PLOTS
STOP
No
CALCULATION OF C_A, C_B
1
Yes
T ⩾ TT/2
No
Yes
$V_{GSP} \geqslant V_{TP}$
'THIRD REGION'
'P-CHANNEL VDMOS:
CUT-OFF REGION'
No
$V_{GSP} - V_{TP} \geqslant V_B$
Yes
2
No
β
I2=I2+1
1
$V_{GSP} - V_{TP} \leqslant V_B$
Yes
3
No
I2=1
No
$V_{GSP} \leqslant V_{TP}$
Yes
4
Yes
T_{RP}=T−TDOFFP
No
5
CALCULATION OF R_B & V_{GSP}
9

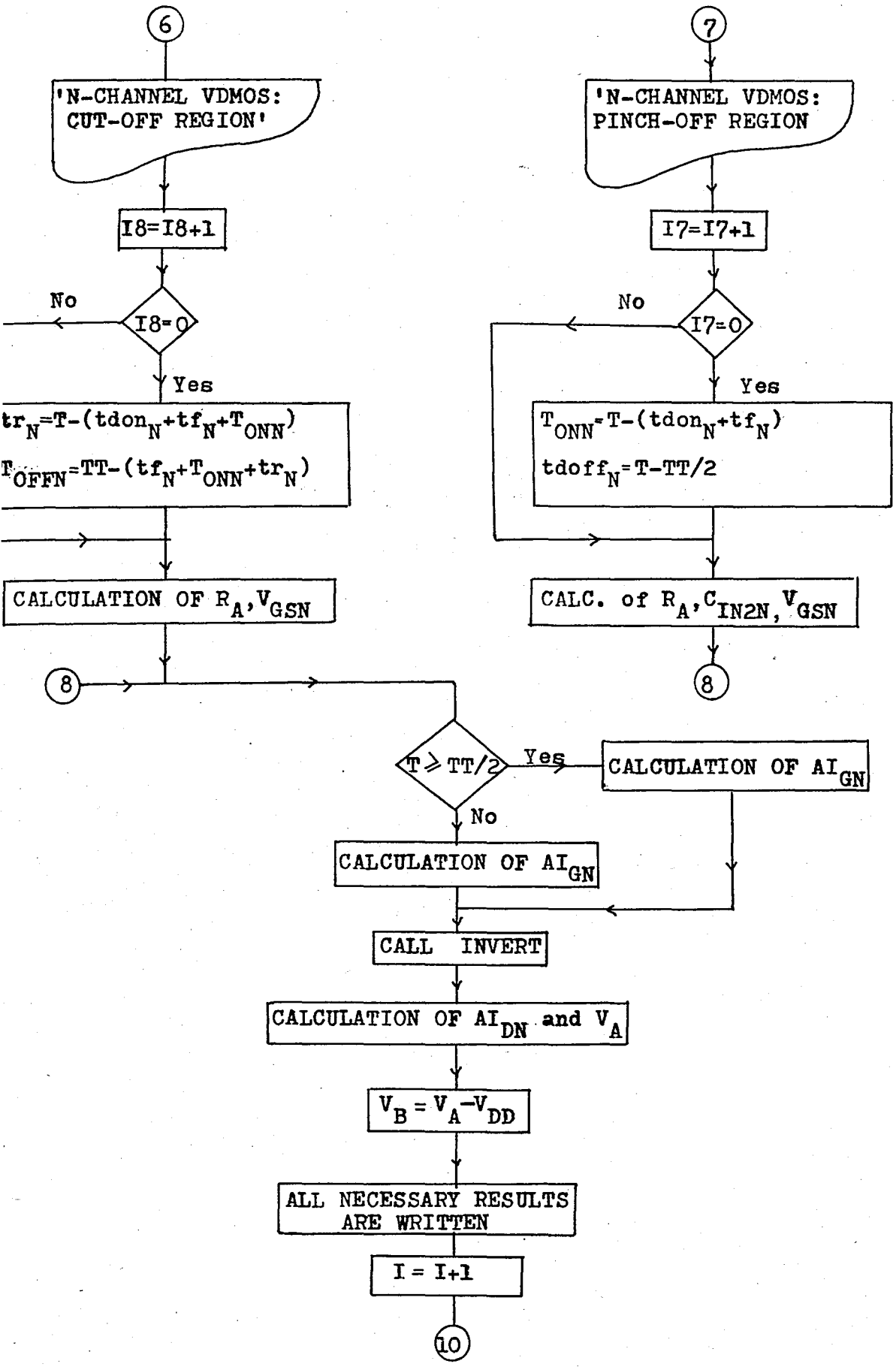

β
'FIRST REGION'
'P-CHANNEL VDMOS: RESISTIVE REGION'
CALCULATION OF R_B & V_{GSP}
9
T ≥ TT/2
Yes
CALCULATION OF AI_{GP}
No
CALCULATION OF AI_{GP}
$V_{GSN} \leq V_{TN}$
Yes
6
No
$V_{GSN} - V_{TN} \leq V_A$
Yes
7
No
'N-CHANNEL VDMOS: RESISTIVE REGION'
CALCULATION OF R_A, V_{GSN}
8
$V_{GSN} \leq V_{TN}$
Yes
'N-CHANNEL VDMOS: CUT-OFF REGION'
CALCULATION OF R_A, V_{GSN}
8
No
$V_{GSN} - V_{TN} \geq V_A$
Yes
'N-CHANNEL VDMOS: RESISTIVE REGION'
I6=I6+1
I6=0
No
Yes
$tf_N = T - tdon_N$
CALCULATION OF R_A-V_{GSN}
8
No
'N-CHANNEL VDMOS: PINCH-OFF REGION'
I5=I5+1
I5=0
Yes
$tdon_N$=T
No
CALCULATION OF R_A, C_{IN2N}, V_{GSN}
8


2
'SECOND REGION'
'P-CHANNEL VDMOS:
PINCH-OFF REGION'
I1=I1+1
No
I1=0
Yes
tdoff$_P$=T
CALC. of R_B,C_{IN2P},V_{GSP}
9


3
'FIFTH REGION'
'P-CHANNEL VDMOS:
CUT-OFF REGION'
I4=I4+1
No
I_4=0
Yes
tf_P=T-(tdoff$_P$+tr_P+T_{OFFP})
T_{ONP}=T-(tr_P+T_{OFFP}+tf_P)
CALCULATION OF R_B,V_{GSP}
9


4
'FOURTH REGION'
'P-CHANNEL VDMOS:
PINCH-OFF REGION'
I3=I3+1
I3=0
No
Yes
T_{OFFP}=T-(tr_P+tdoff$_P$)
tdon$_P$=T-TT/2
CALC. of R_B,C_{IN2P},V_{GSP}
9


5
'THIRD REGION'
'P-CHANNEL VDMOS:
CUT-OFF REGION'
CALCULATION OF R_B,V_{GSP}
9


6
'N-CHANNEL VDMOS: CUT-OFF REGION'
I8=I8+1
No
I8=0
Yes
tr_N=T-(tdon_N+tf_N+T_ONN)
T_OFFN=TT-(tf_N+T_ONN+tr_N)
CALCULATION OF R_A,V_GSN
7
'N-CHANNEL VDMOS: PINCH-OFF REGION
I7=I7+1
No
I7=0
Yes
T_ONN=T-(tdon_N+tf_N)
tdoff_N=T-TT/2
CALC. of R_A,C_IN2N,V_GSN
8
8
T≥TT/2
Yes
CALCULATION OF AI_GN
No
CALCULATION OF AI_GN
CALL INVERT
CALCULATION OF AI_DN and V_A
V_B = V_A-V_DD
ALL NECESSARY RESULTS ARE WRITTEN
I = I+1
10

IV. COMPARISON OF THEORETICAL AND EXPERIMENTAL RESULTS

4.1. Introduction

For controlling the validities of BJT and VVMOS-or VDMOS - transistor models which are developed in the chapter two for practical switching applications,waveform measurements is taken and compared with the computer simulations.For this purpose experimental waveforms of BJT switching circuits are photographed in the laboratory.Some practical measurements related to the VDMOS switching circuit with a resistive load are taken from a research paper,(16).

In all the measurements and computer simulations,the operating frequency is 1 MHz.

To obtain the experimental measurements of the switching circuits a transistor which is adequate to the switching applications is chosen initially.By using the data sheets the values of the circuit elements are determined.Finally,experimental measurements are taken.

The analysis of the BJT,VVMOS and VDMOS switching circuits and CVDMOS inverter were made in the chapter three.To run the computer simulations which are to be compared with measurements the elements and parameters of the transistor model must be determined initially by using the transistor parameters.The expressions which are given in the chapter two is used for this conversion.

In this chapter the measurements and computer simulations of BJT and VDMOS switching circuits are given together.In the BJT switching circuits,the comparisons are made for the resistive, resistive-inductive,resistive-inductive-capacitive loads,separately. But in the VDMOS switching circuit,the comparison is made only for the resistive load.For the VVMOS switching circuits and CVDMOS invert only computer simulations are presented.

4.2. Verification of the Validity of the BJT Modeling Procedure

In order to verify the validity of the BJT model for practical switching applications,waveforms are photographed from a CRT screen. The bipolar switching transistor 2N1711 is chosen.The parameters which is necessary for this transistor are given in Table 4.1,(5). A 12V collector supply voltage is used and a square wave of which ON and OFF voltages are 4V and -2V,recpectively,is applied to the input of the circuits from a HP8007B pulse generator with 50Ω source impedance and pulse transition time of 2 ns.Waveform measurements were taken on a Tektronix oscilloscope with 250 MHz bandwidth.

TABLE 4.1 2N1711 bipolar switching transistor parameters

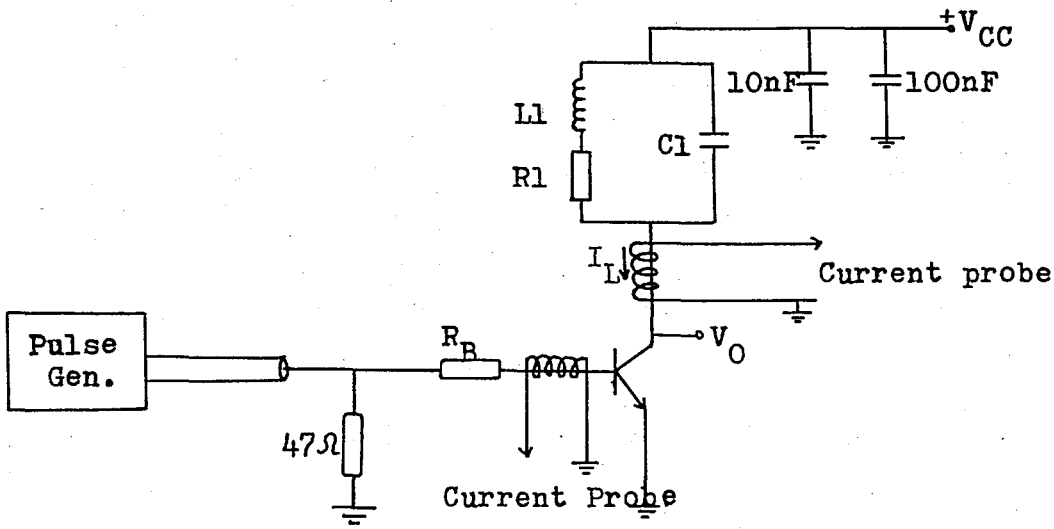
R_{BB}	$1.63 \cdot 10^{-2}$ Ω
R_{EE}	$6.2\ 10^{-2}$ Ω
R_{CC}	$6.2\ 10^{-2}$ Ω
R_E	$2.5\ 10^{4}$ Ω
R_C	$8.15\ 10^{3}$ Ω
I_{ES}	$1.845\ 10^{-12}$A
I_{CS}	$2.8\ 10^{-12}$A
M_E	1.1
M_C	1.1
TEMP	270°K
N_E	0.5
N_C	0.5
B_N	100
B_I	1
V_{ZE}	1.5V
V_{ZC}	1.0V
F_N	70 MHz

F_I	7.5 MHz
C_{JEO}	92 pF
C_{JCO}	83 pF
C_{BE}	80 pF

The switching circuit with RLC load is set up as shown in Figure(4.1).For the resistive load the values of the load inductor and capacitor are taken as zero.In the computer simulation the same method is used.

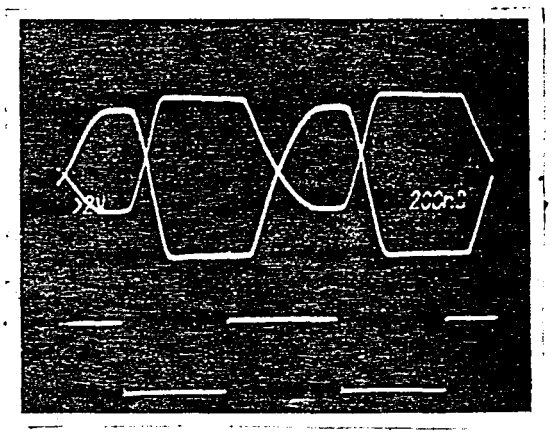
A termination resistor of 47Ωis placed at the end of the coaxial cable.At the input of the switching circuit ON and OFF values of the square wave were E_{ON}=2V and E_{OFF}=-1V,respectively. The values of the circuit elements are chosen as R_B=1K8,Rl= 330Ω, Ll=17.5μH and Cl=10 pF by looking at the safe operating conditions of 2N1711 from the data book.Two capacitors of 10nF and 100nF are used as the bypass capacitors.

The circuit is set up on the printed circuit instead of the breadboard to avoid the stray capacitances of the breadboard at 1 MHz

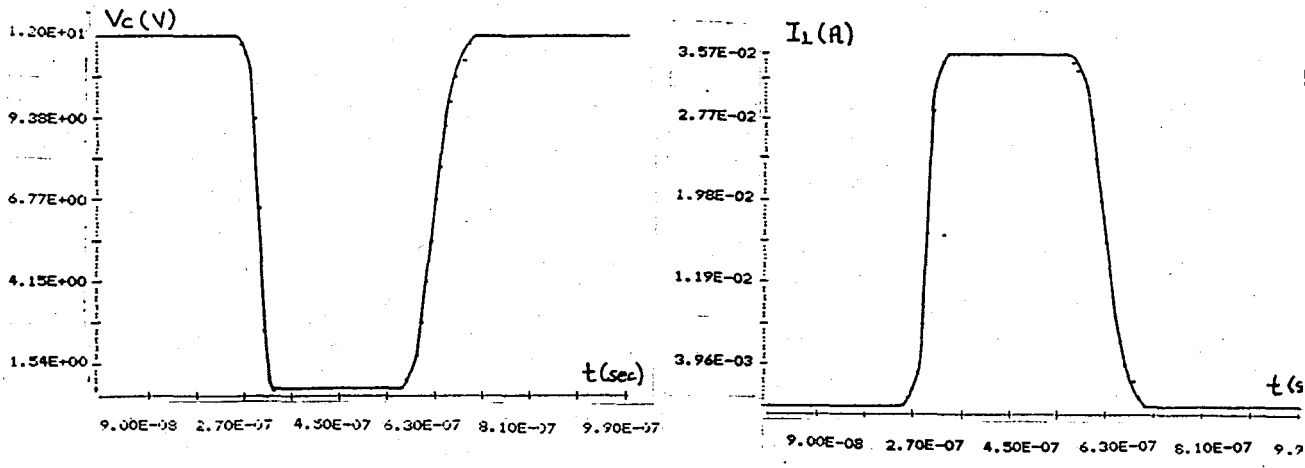


FIGURE(4.1) BJT switching circuit and measurement set-up

The measurable terminal waveforms comprised the collector to emitter voltage V_C and the load current I_L.The load current waveforms are obtained by using a P6042 Tektronix current probe.



FIGURE(4.2) Oscilloscope measurements of the switching waveforms related to the BJT switching circuit with resistive load Vertical scales,V_{IN}:2V/div.,V_C:5V/div.,I_L:10 mA/div.



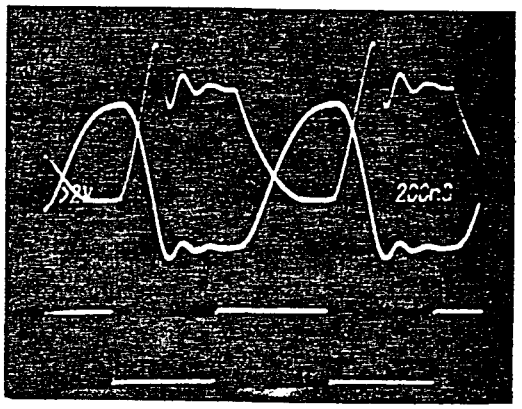
a)Output voltage b)load current

FIGURE(4.3) Simulated switching waveforms of the BJT switching circuit with resistive load

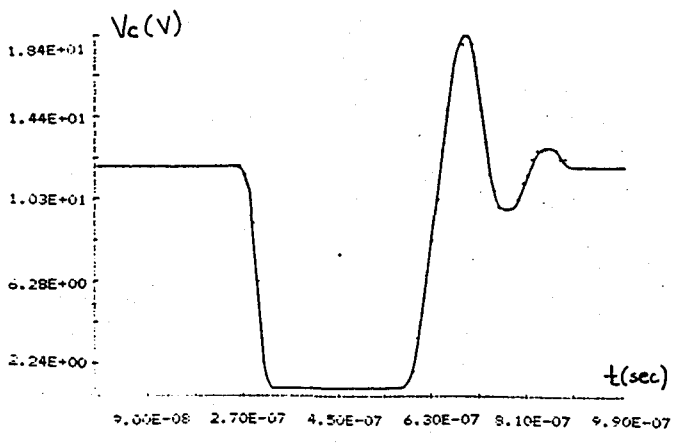
The values of the model parameters,tron,T_S,troff,V_{CES},R_{MIN}, R_{MAX},C_{MIN},and C_{MAX},can be determined by substituting the calculated

base and collector current and voltage values and the transistor parameters which are given in Table(4.1),into Eqs.(2.3.6),(2.3.7), (2.3.8),(2.3.13),(2.3.16),(2.3.17),(2.3.27),and (2.3.28),respectively.

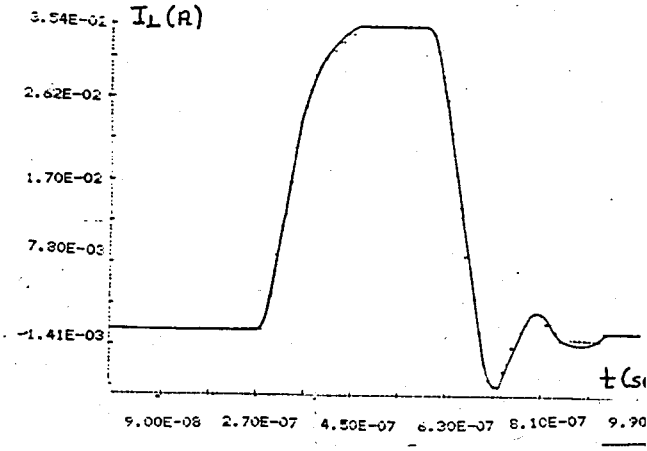
For the computer simulation of the BJT switching circuits the model parameters are taken as tron=0.28 μsec,T_S= 0.06 μsec,V_{CES}= 0.2V, troff=0.14 μsec,R_{MIN}=0.9 Ω,R_{MAX}=4 10^7 Ω ,C_{MIN}=32.6 pF,C_{MAX}= 620 pF, C_{BMIN}=80 pF,and V_G=0.7V.



FIGURE(4.4) Oscilloscope measurements of the switching waveforms related to the BJT switching circuit with resistive-inductive load Vertical scales,V_{IN}:2V/div.,V_C:5V/div.,I_L:10mA/div.



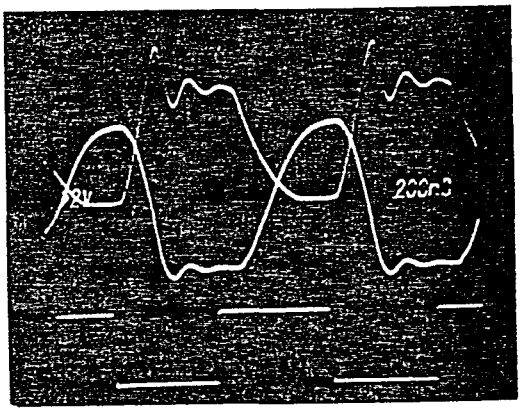
a)Output voltage



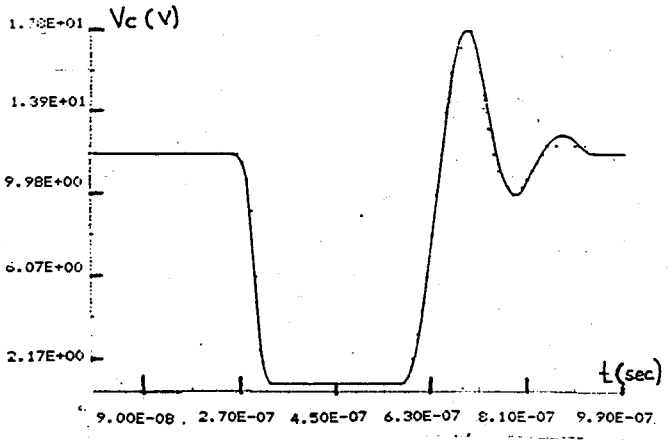
b)Load current

FIGURE(4.5) Simulated switching waveforms of the BJT switching circuit with resistive-inductive load

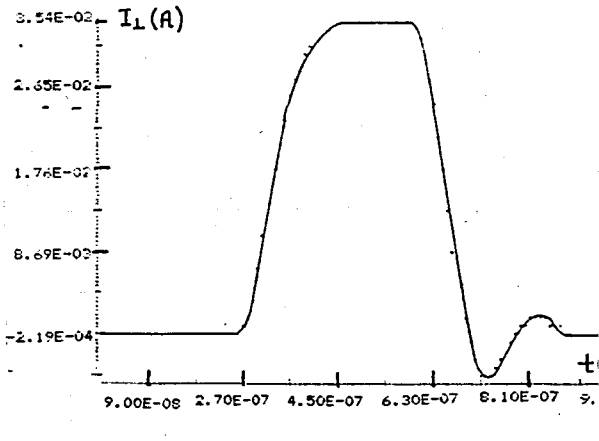
For the BJT switching circuits with resistive,resistive-inductive and resistive-inductive-capacitive loads the output voltage and load current experimental waveforms are shown in Figures (4.2),(4.4), and (4.6),respectively.The related computer simulation results are



FIGURE(4.6) Oscilloscope measurements of the switching waveforms related to the BJT switching circuit with RLC load
Vertical scales,V_{IN}:2V/div.,V_C:5V/div.,I_L:10 mA/div.



a)Output voltage



b)Load current

FIGURE(4.7) Simulated switching waveforms of the BJT switching circuit with RLC load

shown in Figures (4.3),(4.5),and (4.7),respectively,for direct comparison with measurements under the same conditions.A good

agreement is seen between the detailed oscilloscope photographs and the simulations based on the present model.Waveform details,such as the change of slope in V_C and I_L during their transitions,the ringing and smooth V_C and I_L shapes show a good correlation.The simulation results match the experimental results to within 9 per cent.Calculated and measured peak values of the overshoots,V_{CMAX}, are given in Table(4.2).

TABLE 4.2 Comparison of theoretical and measured ringing frequencies and overshoots

Parameters		RL load	RLC load
Calculated	f_D	6.66 MHz	5.83 MHz
Simulated		6.34 MHz	5.42 MHz
Measured		6.9 MHz	6.0 MHz
Simulated	V_{CMAX}	18.4 V	17.8 V
Measured		18.1 V	18.0 V

In this modelling procedure only the output side of the bipolar transistor is modelled.This procedure affects partially the accuracy of the model.In spite of this situation,there is an agreement between the measured and simulated waveforms as shown in Table(4.2).

4.3. Verification of the Validity of the VVMOS and VDMOS Modeling Procedure

In order to verify the validity of the VVMOS-or VDMOS-model for practical switching circuits,VVMOS and VDMOS switching circuits which were given in Figure(3.2) are simulated,separately.For the VVMOS switching circuits only theoretical waveforms are obtained. Simulated waveforms of the VDMOS switching circuit with resistive load are compared with the measured waveforms which are taken from reference paper (16) under the same circuit conditions.In addition, VDMOS model is applied to a complementary VDMOS inverter and the simulated results are also shown at the end of this section.

4.3.1. VVMOS Transistors

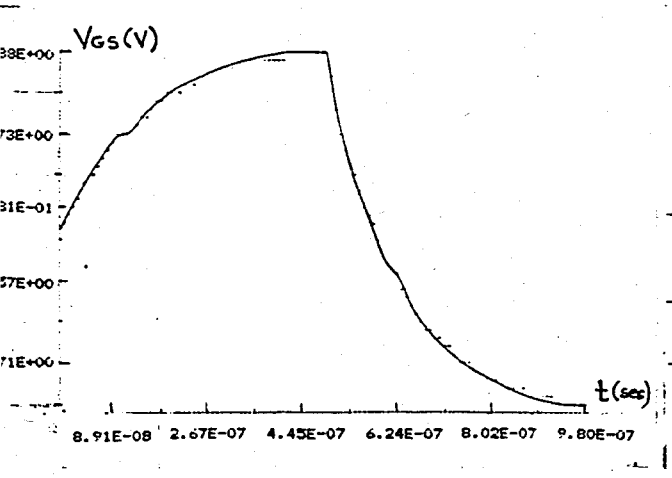
To control the VVMOS modelling procedure the VVMOS transistor whose parameters are given in Table(4.3),is applied to the switching circuit with RLC loads.The element values are R1=820Ω ,L1=47μH, and C1=15 pF.A 12V drain supply voltage is used and a square wave whose ON and OFF voltages are E_{ON}=5V and E_{OFF}=-5V was applied to the gate terminal through a resistance of 2200Ω.

TABLE 4.3 VVMOS transistor parameters (15)

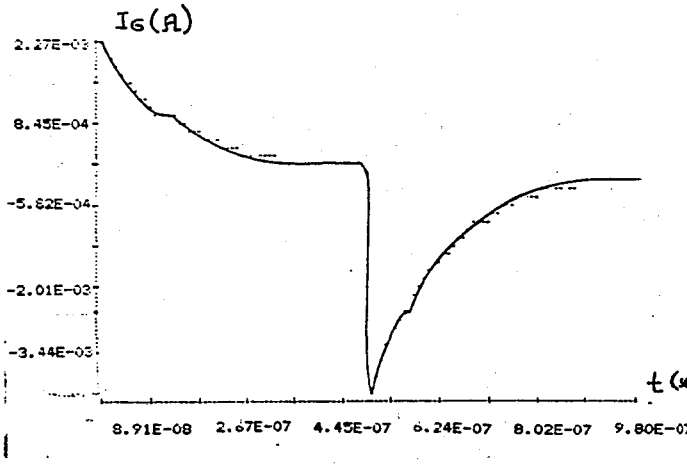
C_O	35 nF/cm^2
C_{on}	12 nF/cm^2
Z	1.85 cm
L	2 μm
X_n	2.2 μm
Y_{ov}	2 μm
Y_G	8 μm
C_{GS}	38 pF
C_{GD}	20 pF

C_{DSO}	$15 \cdot 10^{-9}$ pF.cm^{-2}
ϕ	0.9 V
H	0.5
V_T	2.5 V
R_N	5.7 Ω
μ	190 cm^2/V.s
g_n^-	5 Ω.cm
d/a	7.8
R_{DSON}	5.85 Ω
V_{GSON}	3.5 V
A	$6.75 \cdot 10^{-3}$ cm^2
Za	$1.5 \cdot 10^{-3}$ cm^2

For the VVMOS switching circuits with resistive,resistive-inductive,and resistive-inductive-capacitive loads the simulated terminal waveforms comprised the gate to source voltage V_{GS},the gate current I_G,the drain to source voltage V_{DS},the drain current I_D,and the drain to source capacitance C_{DS}.Waveforms are shown in

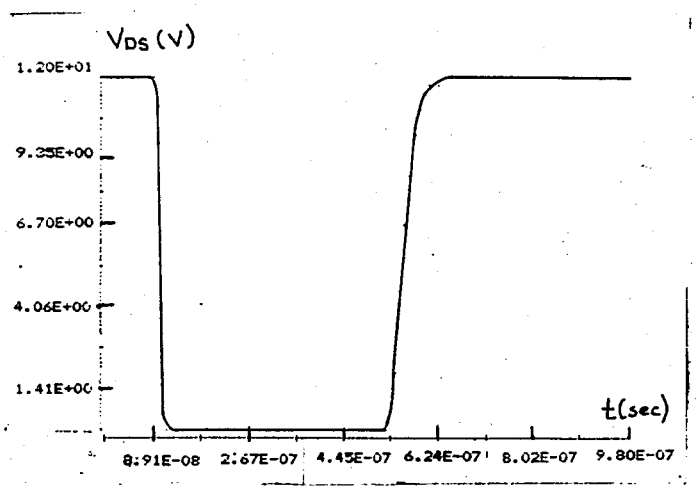


a)Gate to source voltage

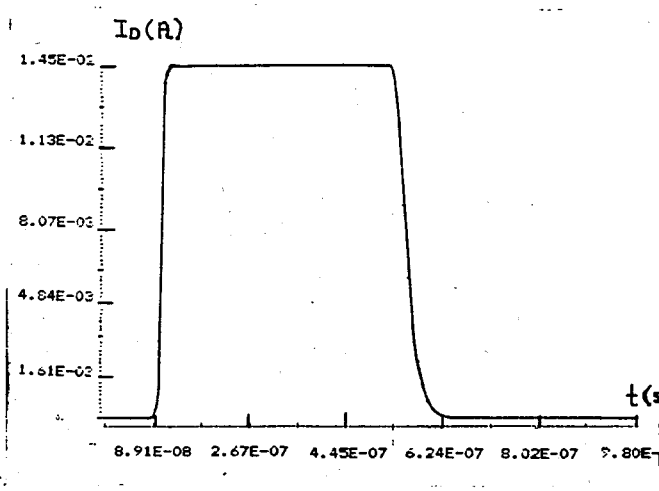


b)Gate current

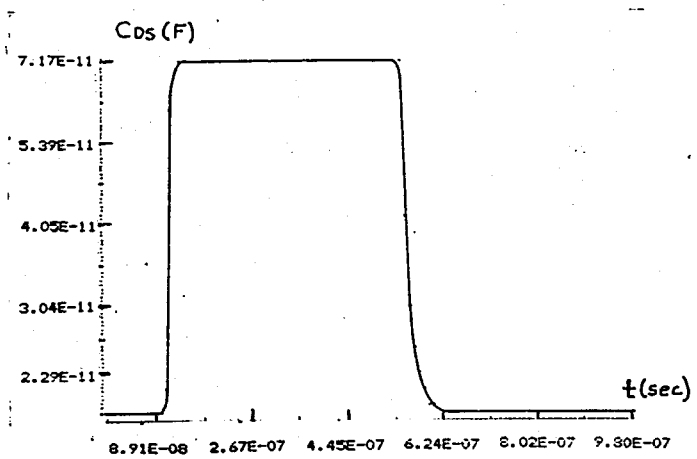
FIGURE(4.8) Simulated switching waveforms related to the input side of the VVMOS switching circuit with resistive load



a)Drain to source voltage



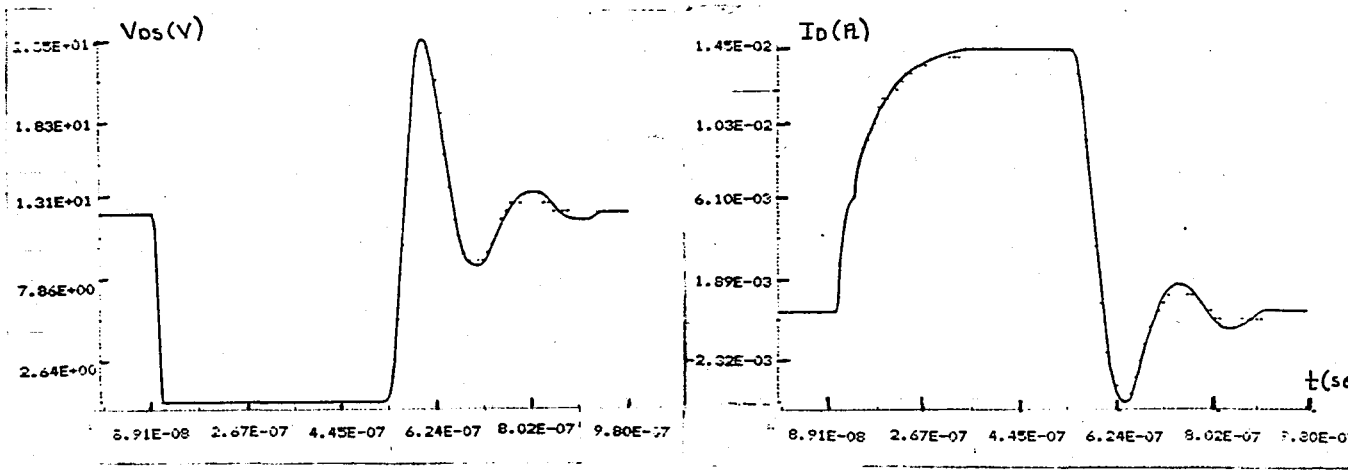
b)Drain current



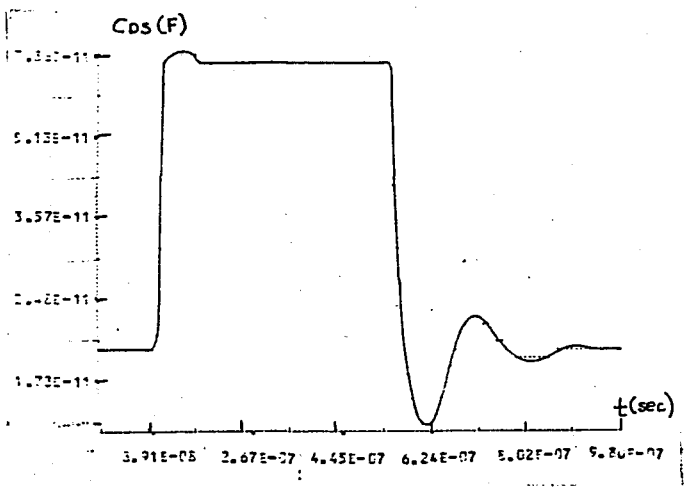
c)Drain to source capacitance

FIGURE(4.9) Simulated switching waveforms related to the output side of the VVMOS switching circuit with resistive load

Figures (4.8),(4.9),(4.10),and (4.11).Figures (4.8) and (4.9) show the gate to source voltage,gate current,the drain to source voltage, drain current,and drain to source capacitance waveforms,respectively, for the resistive load.The turn-on part of the switching cycle begins with a short delay,while V_{GS} rises rapidly to the threshold voltage. This is followed by a plateau phase,where V_{GS} is approximately



a)Drain to source voltage b)Drain current

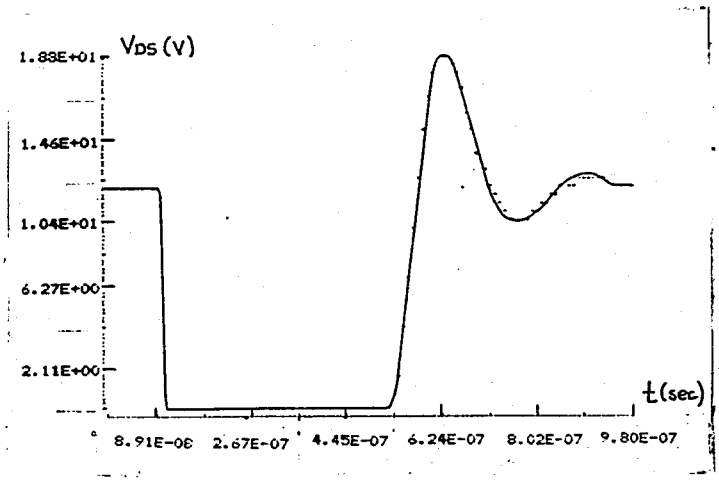


c)Drain to source capacitance

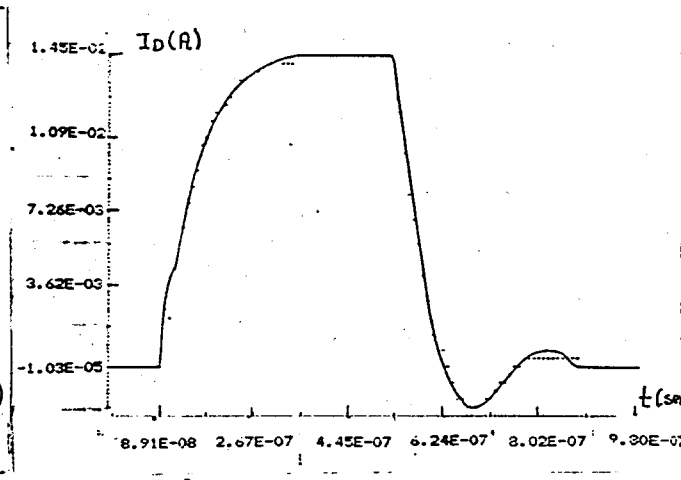
FIGURE(4.10) Simulated switching waveforms related to the output side of the VVMOS switching circuit with resistive-inductive load

constant as the transistor passes through the pinch-off region, with V_{DS} falling and I_D rising. Finally the device enters the resistance region and V_{GS} continues to charge towards the gate drive voltage, while V_{DS} remains small and attains the value corresponding to the ON-resistance, R_{DSON}. A converse behavior results during the turn-off phase as the VVMOS is driven initially from the resistance region

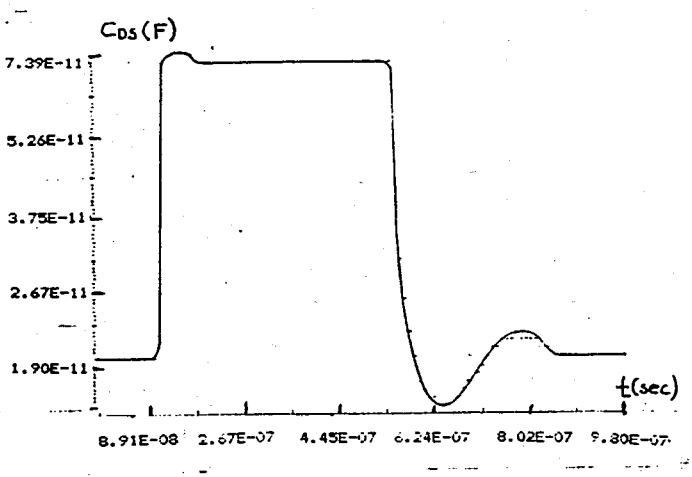
into the cut-off state.The output capacitance is a drain to source voltage dependent junction capacitance as shown in Figure (4.9.c).



a)Drain to source voltage



b)Drain current



c)Drain to source capacitance

FIGURE(4.11) Simulated switching waveforms related to the output side of the VVMOS switching circuit with RLC load

For the RL and RLC loads,the output voltage,load current,and drain to source capacitance waveforms are shown in Figures (4.10) and (4.11),respectively.Waveform details,such as the change of slope in V_{DS} and I_D during their transitions,the ringing and smooth V_{DS}

and I_D shapes,show a good correlation with the desired waveforms. The simulation ringing frequencies and the values of the output voltages and load currents of the switching circuits with RL and RLC loads during ringing correlate to within 4.8 per cent of the theoretical calculations.The overshoots of the drain to source voltages are seen in the drain to source capacitance waveforms because of their V_{DS} dependent junction capacitance characteristics. Calculated and simulated ringing frequencies and switching waveform transition parameters of particular interest,such as 10 per cent to 90 per cent risetime and falltime are given in Table(4.4).

TABLE 4.4 Simulated and calculated VVMOS switching characteristics

Waveform			Resistive load	RL load	RLC load
Turn-on	V_{GS}	tr	270 nsec	270 nsec	270 nsec
	V_{DS}	tf	25 nsec	14 nsec	15 nsec
	I_D	tr	25 nsec	133 nsec	125 nsec
Turn-off	V_{GS}	tf	280 nsec	280 nsec	280 nsec
	V_{DS}	tr	89 nsec	35 nsec	45 nsec
	I_D	tf	90 nsec	40 nsec	71 nsec
Ringing freq.		Simulated	——	4.88 MHz	3.74 MHz
		Calculated	——	5.22 MHz	3.94 MHz

As a result it is seen that the simulated switching waveforms correlate the desired results and this situation verifies the accuracy of the modelling procedure.

4.3.2. VDMOS Transistors

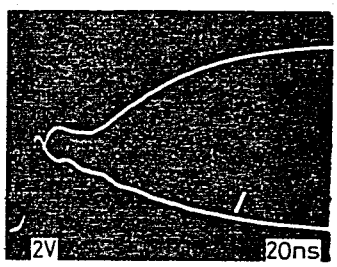
In order to verify the validity of the VDMOS model for practical switching applications,waveform measurements were taken for the transistor switching a resistive load.As the VDMOS switching transistor,IRF139 MOSFET which is an n-channel enhancement transistor is chosen.The parameters of this transistor are given in Table(4.5). A 20V drain supply voltage was used,so the switched current was 4A because of the resistive load of 5Ω,and 12V pulses were applied to the gate terminal from an HP214B pulse generator with 25Ω source impedance and pulse-transition times of 11 nsec.Waveform measurements were taken on a Tektronix oscilloscope with 250 MHz bandwidth.

TABLE 4.5 VDMOS (IRF130) Model Parameters (16)

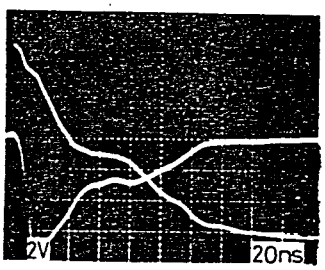
R_S	0.005Ω
R_D	0.07Ω
C_{GD}	600 pF
C_{GS}	550 pF
C_{DSO}	1100 pF
ϕ	0.9 V
H	0.5
V_T	3.4 V
B	1.1687
R_G	4.5Ω
R_{DSON}	0.14Ω
V_{GSON}	10 V
C_P	80 pF

The measurable terminal waveforms comprised the gate to source voltage V_{GS} the gate current I_G,the drain to source voltage V_{DS},

and the drain current I_D.Results are displayed in Figures (4.12) and (4.14).Figures (4.12.a) and (4.14.a) show detailed oscilloscope photographs of the actual waveforms during the turn-on transition of the VDMOS transistor while Figures (4.12.b) and (4.14.b) show corresponding waveforms for the turn-off phase.The variations of the

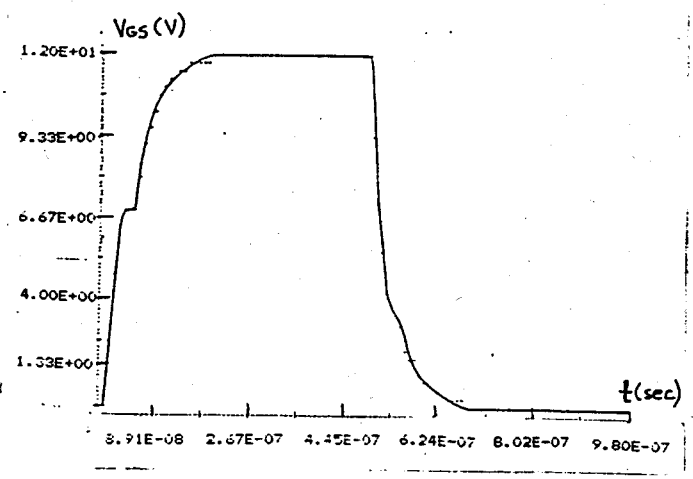


a)Turn-on part

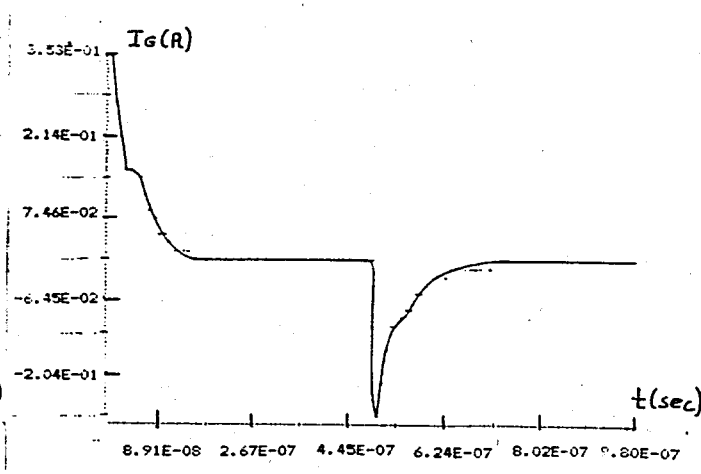


b)Turn-off part

FIGURE(4.12) Oscilloscope measurements of V_{GS} and I_G waveforms related to the VDMOS switching circuit with resistive load Vertical scales,V_{GS}:2V/div.,I_G:0.1A/div.



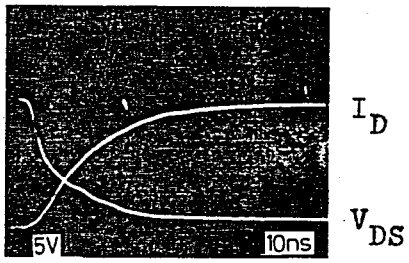
a)Gate to source voltage



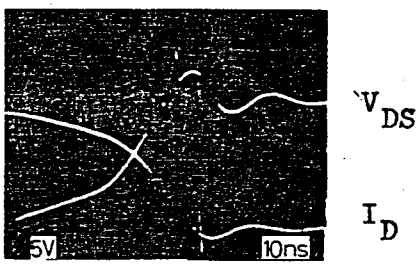
b)Gate current

FIGURE(4.13) Simulated switching waveforms related to the input side of the VDMOS switching circuit with resistive load

switching waveforms are similar to those of VVMOS transistor that's why the explanation given in section(4.2.1) is also valid for the

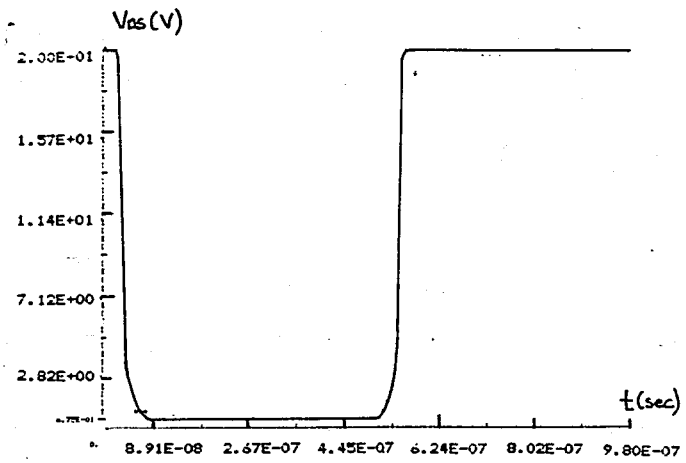


a)Turn-on part

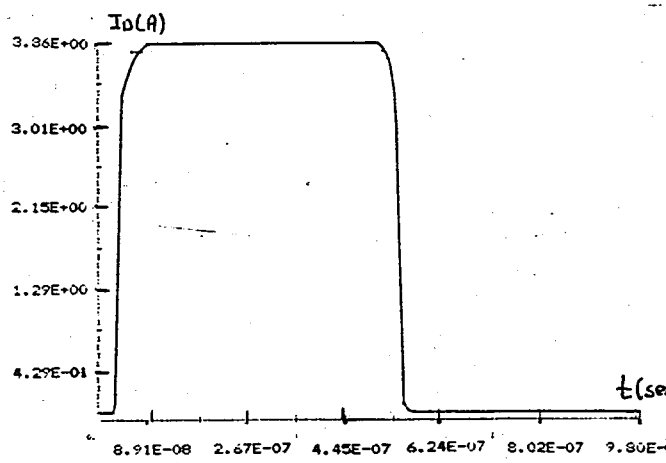


b)Turn-off part

FIGURE(4.14) Oscilloscope measurements of V_{DS} and I_D waveforms related to the VDMOS switching circuit with resistive load Vertical scales,V_{DS}:5V/div.,I_D:1A/div.



a)Drain to source voltage



b)Drain current

FIGURE(4.15) Simulated switching waveforms related to the output side of the VDMOS switching circuit with resistive load

the VDMOS switching waveforms.

Computer simulation results using the VDMOS model with parameter values given in Table(4.5) are shown in Figures (4.13) and (4.15) for direct comparison with measurements under the same circuit conditions.A good agreement is seen between the experimental waveforms and predictions based on the present model.Waveform details,such as the V_{GS} plateau,the change of slope in V_{DS} during its transition,

the smooth I_D shape as well as the timing relations between the various voltages and currents, show very good agreement. The V_{GS} plateau does not seen in the simulated waveform perfectly because oscilloscope measurements are made separately for the turn-on and turn-off transients with 20 nsec/div. However, simulated waveform shows complete waveform within one period of 1 MHz. The ringing in V_{DS} or I_D owing to the presence of the drain inductor under 1 MHz operating frequency is not seen in the simulated results because the model does not include any inductor because of its simple characteristic Switching waveform transition parameters, risetime tr and falltime tf, are compared to measurements in Table(4.6).

TABLE 4.6 Comparison between measured and simulated VDMOS switching characteristics

Waveform		Measured	Simulated
Turn-on	V_{GS}: tr	122 nsec	116 nsec
	V_{DS}: tf	31 nsec	29 nsec
	I_D : tr	36 nsec	33 nsec
	I_G : peak	0.3 A	0.35 A
Turn-off	V_{GS}: tf	108 nsec	107 nsec
	V_{DS}: tr	44 nsec	35 nsec
	I_D : tf	44 nsec	33 nsec
	I_G : peak	-0.35 A	-0.27 A

It is seen that the simulation correlates the experimental data and a good agreement for all the switching waveforms verifies the accuracy of the modelling procedure.

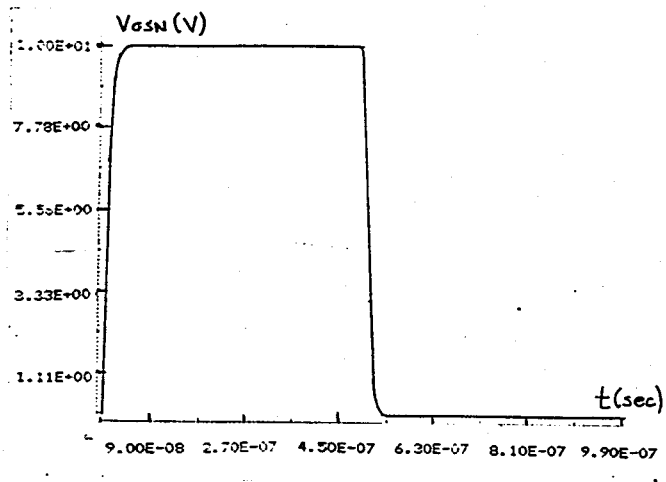
4.3.3. Complementary VDMOS Inverter

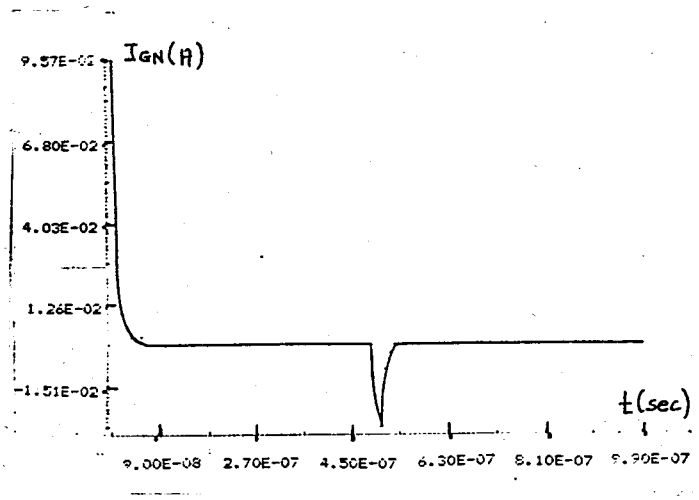
An n-channel enhancement VDMOS transistor,BST78,whose parameters are given in Table(4.7),(24),and a complementary p-channel VDMOS transistor are used for CVDMOS inverter which was shown in Figure (3.6).A 10V supply voltage was applied to the source of p-channel transistor and 10V pulses were applied at the gate terminal from a pulse generator with 100 Ω source impedance.

TABLE 4.7 N-channel VDMOS transistor (BST78) parameters (24)

R_S	0.05 Ω
R_D	0.7 Ω
R_G	4.5 Ω
C_{GS}	75 pF
C_{GD}	5 pF
C_{DSO}	100 pF
ϕ	0.9 V
H	0.5
V_T	3.4 V
R_{DSON}	15 Ω
V_{GSON}	10 V
t_{on}	<10 nsec
t_{off}	<100 nsec

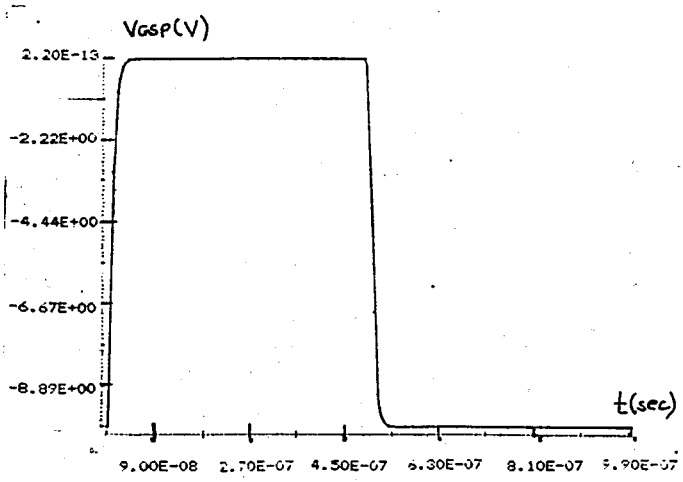
In the CVDMOS inverter the simulated terminal waveforms comprised the n- and p-channel transistor gate to source voltage, gate current waveforms,n-channel transistor drain to source voltage and drain current waveforms.These waveforms are shown in Figures (4.16),(4.17),and (4.18),respectively,for every transistor.Here the n-channel transistor drain to source voltage and drain current are

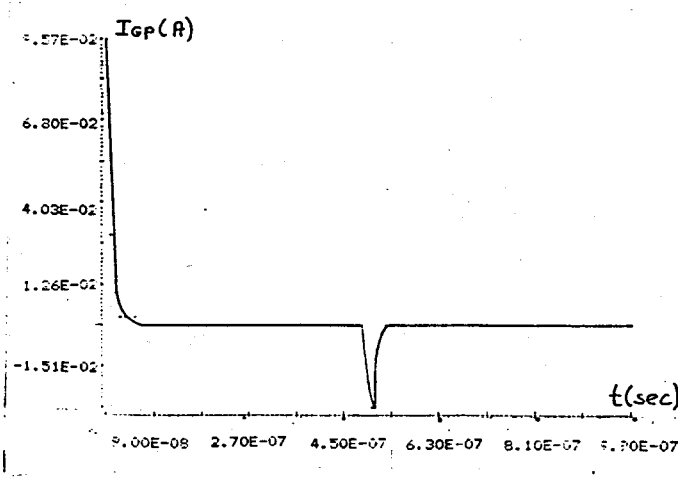




a)Gate to source voltage b)Gate current

FIGURE(4.16) Simulated switching waveforms related to the n-channel transistor in CVDMOS inverter

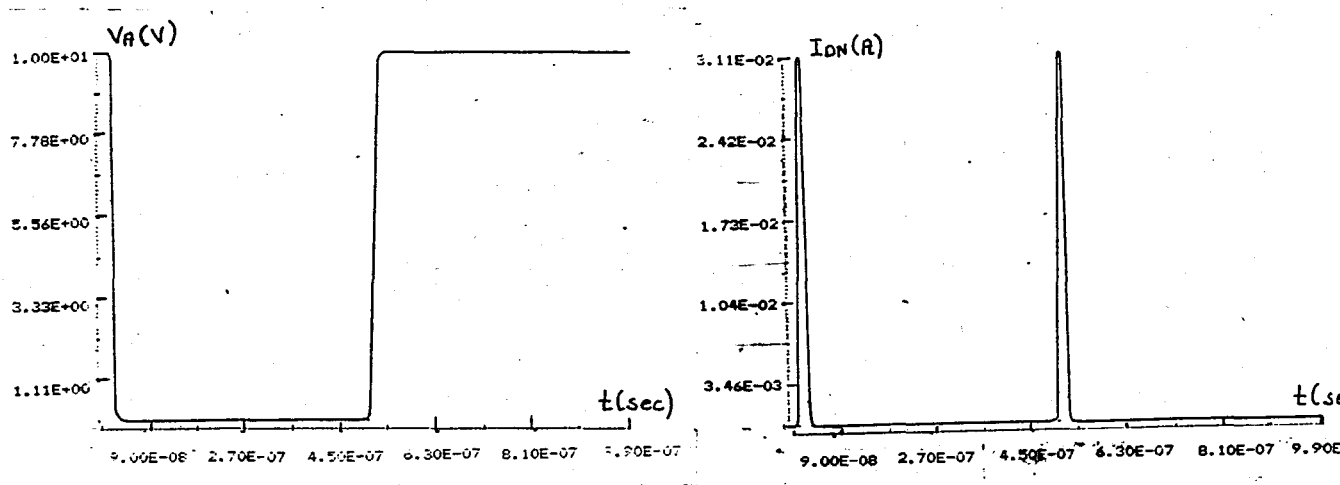




a)Gate to source voltage b)Gate current

FIGURE(4.17) Simulated switching waveforms related to the p-channel transistor in CVDMOS inverter

the output voltage, V_A, and supply current, I_{DN}, of the inverter. The turn-on part of the output voltage or supply current begins with a short delay while V_{GSN} and V_{GSP} rise rapidly to the threshold voltage. As



a) Output voltage b) Supply current

FIGURE(4.18) Simulated switching waveforms related to the CVDMOS inverter

the transistors pass through the pinch-off region V_A falls and I_{DN} rises.Finally n-channel transistor enters the resistance region while p-channel transistor enters the cut-off region and V_{GSN} and V_{GSP} continue to charge towards the ON and OFF gate drive voltages, respectively,while the output voltage remains small and attains the value corresponding to the n-channel transistor ON resistance.In the pinch-off region, supply current attains the maximum value but in the resistive region it has a small value again because of the p-channel MOS OFF resistance.A converse behavior results during the turn-off phase of the inverter

Waveform details,such as the change of slope in V_A during its transition,the spikes in I_{DN}during the pinch-off region and very small values in the other regions,the variations of the gate to source voltage and gate current waveforms,as well as the timing relations between the various voltages and currents show very good correlation.If the switching waveform transition parameters which

TABLE 4.8 Simulated CVDMOS inverter switching characteristics

Waveform		Simulated
Turn-on	V_{GSN}: tr	31 nsec
	V_{GSP}: tf	31 nsec
	V_A : tf	18 nsec
	I_{DN} : tr	9 nsec
Turn-off	V_{GSN}: tf	31 nsec
	V_{GSP}: tr	31 nsec
	V_A : tr	27 nsec
	I_{DN} : tf	9 nsec

are given in Table(4.8) are compared to the transition times which are given in Table(4.7) it can be seen that there is an agreement between the values.As a result,all of these explanations verify the accuracy of the modelling procedure.

V. CONCLUSION

Large-signal models for transistors are necessary tools for device engineer and circuit designer.Over the past few years a number of models have been proposed.At large-signal levels a transistor exhibits significant effects which can not be analyzed by means of the simpler models.These effects are generally caused by harmonic components of the voltages and currents generated by non-linear mechanisms within the transistor.The non-linear model which has received the most attention is the Ebers-Moll model.But high computer costs are seen a disadvantage in the Ebers-Moll model. That's why it is needed to develop a new model to overcome the high computational complexity of the Ebers-Moll model.

In this thesis a newly developed time-variant linear large-signal model (15) is applied to the bipolar and vertical VMOS-or DMOS-transistors in the switching circuits.This model can be considered as the best one which provides an optimum combination of accuracy, ease of parameter acquisition,simplicity,and less computational complexity.

In the time-variant linear large-signal BJT model only the output side of the transistor is modelled assuming that the input is driven by a square wave.In the vertical MOS transistors channel conduction is proportional to the gate voltage.That's why a complete model is developed for the vertical MOS transistors.A rigorous criterion for the accuracies of the models was set by evaluating the closeness of simultaneous matching between measurements and simulations for all the accessible waveforms of the devices.The simulated switching characteristics are obtained by changing the corresponding model elements with a determined time-interval within one period.In this case the previous calculations are taken as the initial conditions

In the new BJT model the output resistance and capacitance which represent the transistor are changed exponentially in the transition regions.This method is very adequate for obtaining the collector voltage and current waveforms which are closer to the real variations.The model parameters have physical origins within the device and they are readily obtained from the data sheets and static curve-tracer measurements.This leads to a particularly fast and simple model definition.The accuracy of the linear large-signal BJT model was verified by detailed comparisons of simulated and measured switching characteristics pertaining to a practical high-speed switching circuits.Such simulations have direct applications to the evaluation of switching performance.The agreement between predicted and experimental waveforms confirms the validity of this modelling procedure.

In the vertical VMOS or DMOS transistor model the transistor is represented by an input capacitance and an output resistance and capacitance.The output resistance is a function of the gate to source voltage beyond the cut-off region.This relation is used for developing a complete model.The output capacitance,however,is a function of the drain to source voltage.This model parameters have also physical origins within the transistor and they are obtained from the data sheets.This model has also fast and simple model definition.The accuracy of the model is verified by the good correlation obtained between detailed simulated and measured switching characteristics on the experimental high-speed switching circuits and complementary VDMOS inverter.

This new time-variant linear model which is developed for the BJT and VVMOS-or VDMOS-switching circuits approaches the ideal model on the basis of physical processes,facility of analysis,ease of

parameter acquisition and offers less computational costs.

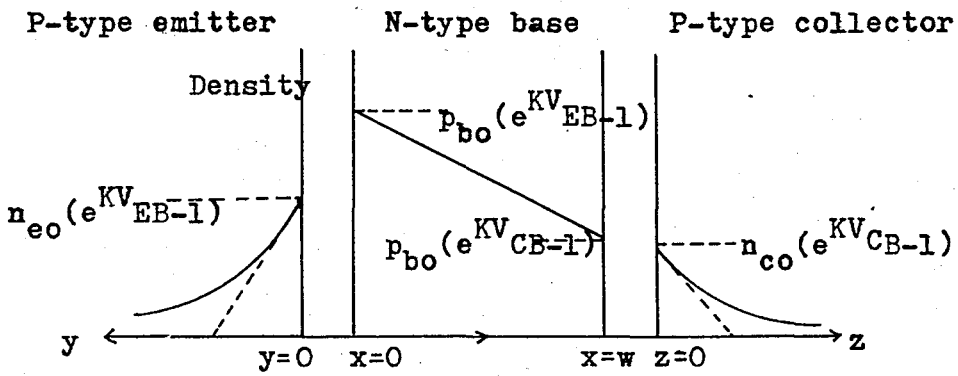
In the BJT modelling procedure,modelling only the output side of the transistor affects partially the accuracy of the model.But as a complete model the VVMOS-or VDMOS-transistor model has a good accuracy.

This proposed model is developed for only the switching circuits. That's why it is very useful for the analysis of high-speed transistor switching circuits and class-E amplifiers in which transistor is used as a switch.But it should not be used for amplification purposes.

APPENDIX-A

EBERS-MOLL MODEL

The voltage applied to the junctions of a transistor establishes given minority-carrier concentrations at the edges of the depletion regions.In the saturated (ON) mode of operation,both the emitter and collector junctions are forward-biased.Figure(A.1) illustrates the excess minority-carrier density distribution for an idealized P-N-P uniform-base transistor operating in this mode.



FIGURE(A.1) Excess minority-carrier distribution

The total hole density at the emitter edge of the base pb(0) can be expressed as follows.

$$pb(0) = pb_0.(\exp(K.V_{EB})) \qquad (A.1.1)$$

where pb_0 is the equilibrium hole density,V_{EB} is the emitter to base voltage,and K = q/k.T.Therefore,the excess minority-carrier density (over the equilibrium density),pb'(0),is given by

$$pb'(0) = pb_0.(\exp(K.V_{EB})-1) \qquad (A.1.2)$$

By a similar reasoning process,the excess minority carrier density at the collector edge of the base,pb'(w),can be defined as follows.

$$pb'(w) = pb_0.(\exp(K.V_{CB})-1) \qquad (A.1.3)$$

The excess minority-carrier concentrations in the p-type collector and emitter regions are given by

$$nc'(0) = nc_0.(\exp(K.V_{CB})-1) \qquad (A.1.4)$$

and

$$ne'(0) = ne_0.(\exp(K.V_{CB})-1) \qquad (A.1.5)$$

Eq.(A.1.1) is accurate provided the majority carrier concentration on the injecting side of the p-n junction is not increased by high level effects.For narrow base transistors,the emitter junction will generally be described by (A.1.2) and (A.1.5).However,in deep saturation,(A.1.3) and (A.1.4) may not be rigorosly true.This has been suggested to be a possible limitation to this model.

The emitter and collector currents can be expressed in terms of the excess minority-carrier density gradients as follows.

$$I_E = A.q\left[-Dp.\frac{dpb'}{dx}\bigg|_{x=0} - Dn.\frac{dne'}{dy}\bigg|_{y=0}\right] \qquad (A.1.6)$$

and

$$I_C = A.q\left[Dp.\frac{dpb'}{dx}\bigg|_{x=w} - Dn.\frac{dnc'}{dz}\bigg|_{z=0}\right] \qquad (A.1.7)$$

where A is the cross-sectional area and Dp and Dn are the hole and electron diffusion constant,respectively.

Assumption of a linear gradient in the base (the key simplification of the Ebers-moll model) leads to the following expressions:

$$\frac{dpb'}{dx}\bigg|_{x=0} = \frac{pb'(0)-pb'(w)}{w} \qquad (A.1.8)$$

$$\left.\frac{dpb'}{dx}\right|_{x=0} = \frac{-pb_0(\exp(KV_{EB})-1)-pb_0(\exp(KV_{CB})-1)}{w} \qquad (A.1.9)$$

and

$$\left.\frac{dpb'}{dx}\right|_{x=w} = \left.\frac{dpb'}{dx}\right|_{x=0} \qquad (A.1.10)$$

In the emitter and collector regions, these expressions become

$$\left.\frac{dne'}{dy}\right|_{y=0} = \frac{-ne'(0)}{Le} = \frac{-ne_0}{Le}.(\exp(KV_{EB})-1) \qquad (A.1.11)$$

and

$$\left.\frac{dnc'}{dz}\right|_{z=0} = \frac{-nc'(0)}{Lc} = \frac{-nc_0}{Lc}.(\exp(KV_{CB})-1) \qquad (A.1.12)$$

When (A.1.9), (A.1.10), (A.1.11), and (A.1.12) are substituted into (A.1.6) and (A.1.7) and the constants are considered, the emitter and collector currents are given by

$$I_E = A_{11}(e^{K.V_{EB}}-1)+A_{12}(e^{K.V_{CB}}-1) \qquad (A.1.13)$$

$$I_C = A_{21}(e^{K.V_{EB}}-1)+A_{22}(e^{K.V_{CB}}-1) \qquad (A.1.14)$$

In their paper, Ebers and Moll defined the constants in these equations in terms of the following measurable parameters.

I_{EO} : the saturation current of the emitter junction with zero collector current.

I_{CO} : the saturation current of the collector junction with zero emitter current.

α_N : the transistor current gain with emitter and collector performing only their prescribed functions.

α_I : the transistor current gain with the emitter and collector performing inverted functions.

When the constants in (A.1.13) and (A.1.14) are expressed in terms of these definitions, the standard Ebers and Moll relationship results, as follows.

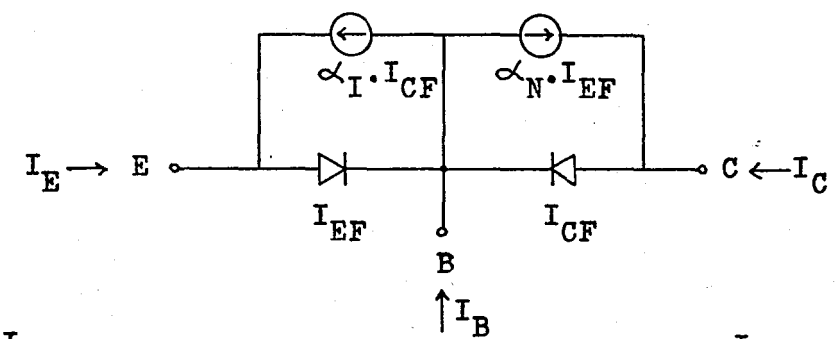
$$I_E = \frac{I_{EO}}{(1-\alpha_N \cdot \alpha_I)} \cdot (e^{K \cdot V_{EB}} - 1) - \frac{\alpha_I \cdot I_{CO}}{(1-\alpha_N \cdot \alpha_I)} \cdot (e^{KV_{CB}} - 1) \qquad (A.1.15)$$

and

$$I_C = \frac{-\alpha_N \cdot I_{EO}}{(1-\alpha_N \cdot \alpha_I)} \cdot (e^{K \cdot V_{EB}} - 1) + \frac{I_{CO}}{(1-\alpha_N \cdot \alpha_I)} \cdot (e^{K \cdot V_{CB}} - 1) \qquad (A.1.16)$$

$$I_E + I_B + I_C = 0 \qquad (A.1.17)$$

These equations can be interpreted by a fairly simple electrical diagram, as illustrated in Figure(A.2).



$$I_{EF} = \frac{I_{EO}}{(1-\alpha_N \cdot \alpha_I)} \cdot (e^{KV_{EB}} - 1) \qquad I_{CF} = \frac{I_{CO}}{(1-\alpha_N \cdot \alpha_I)} \cdot (e^{KV_{CB}} - 1)$$

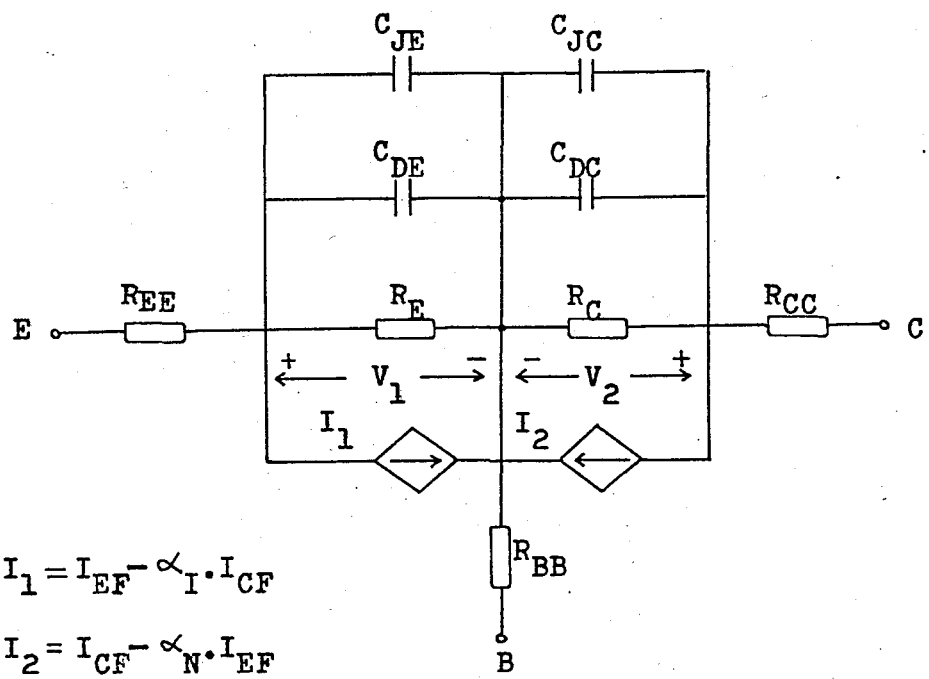
FIGURE(A.2) Circuit representing equations

This equivalent equivalent circuit not only accurately represents the large-signal equations, but also provides a physical description of the action taking place within the device. The emitter current I_E can be conceived of as being composed of two components: a component I_{EF} produced by the minority carriers injected from the emitter into base, and a component $\alpha_I \cdot I_{CF}$ that results from a collected component of the

current injected from the collector into the base.The collector current I_C also consists of emitted and collected components.

It is important to note that,even though these relationships were developed for large-signal operation,they are general and valid for all junction bias conditions.When both junctions are forward-biased,the transistor is in the (ON) saturated mode;when the emitter is forward-biased and the collector reverse-biased,the transistor is in the ACTIVE mode;and when both junctions are reverse-biased,the transistor is in the OFF mode.For reverse collector bias,the Ebers-Moll equations reduce to those normally used to describe operation in small-signal applications.

It is possible to obtain a more complete Ebers-Moll model with the addition of bulk resistances,leakage resistances,and capacitances to include high-frequency effects.This model is shown in Figure(A.3).The characterization of a transistor according to the model shown in Figure(A.3) can be divided into two segments:a D.C. portion and an A.C. portion (1).



FIGURE(A.3) Complete Ebers-Moll model

APPENDIX-B

VVMOS (VERTICAL V-GROOVE MOS) TRANSISTORS

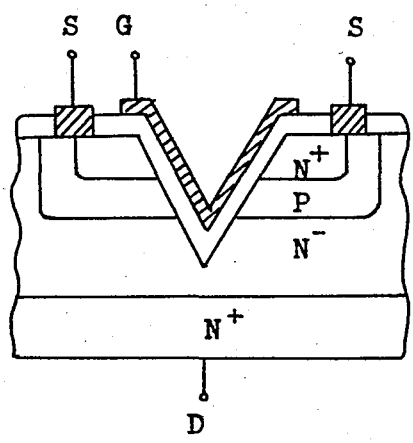
I. INTRODUCTION

Until several years ago,Field Effect Transistors have been useful only at low (<1W) power levels.While possessing many theoretical advantages over their bipolar counterparts,the practical limitations in manufacturing high power devices precluded FET's competing with BJT's and SCR's in power applications.A major limitation was that FET's were strictly horizontal devices,so their current densities were much less than the bipolar's (which utilized vertical current flow).For a given current,then,the FET chip area had to be considerably larger,which meant a lower yield and a resulting higher cost.Medium power FET's were therefore much costlier to fabricate than the bipolar counterparts,and high power FET's were even more impractical.

A new FET technology has recently been developed to increase current density and allow production of high voltage,high current FET's.This technology-VVMOST,or Vertical V-groove Metal Oxide Semiconductor Transistor-exploits a diffused channel and vertical current flow to achieve its high power capabilities.Voltage and current levels compared to those of power bipolar devices are now feasible.

II. GENERAL REVIEW TO VVMOS TRANSISTORS

Figure(A.4) shows a cross section of a VVMOST channel.The substrate, which eventually becomes the drain and provides a low resistance current path,is N^+ material.An N^- epi-layer increases the drain to source breakdown voltage by absorbing the depletion region from the drain-body junction, which is mormally reverse-biased.Also,the epi-layer greatly reduces the feedback capacitance since the gate overlaps N^- rather than N^+ material.



FIGURE(A.4) Cross section of a VVMOST channel

In operation,both the gate and drain are positive with respect to the source (and body).The gate produces an electric field which induces an N-type channel on both surfaces of the body facing the gate,allowing electrons to flow from the source,through the N-type channel,and epi, and into the substrate(drain).Because current flow-in the form of electrons-is entirely through N-type material,the VVMOST is a majority carrier device.A greater gate voltage enhances a deeper channel,so the current path from the drain to source is wider and current flow is increased.

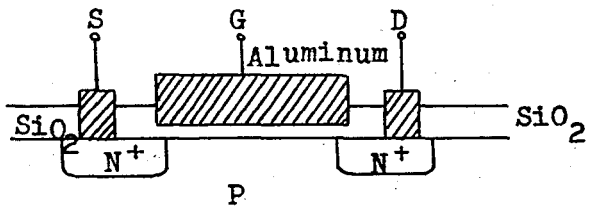
As a result,the structure of the VVMOST has the high density advantage and it offers (23)

1) A high channel width per unit area due to the contribution of both sides of the groove;
2) A constant transconductance above pinch-off due to velocity saturation;and
3) The devices operate in the enhancement mode and have very low on-resistance and are thus suitable for both amplification and switching applications.

Disadvantages of the structure are a fairly complex process involving at least five masking steps and the possibility of saturation current decrease with increasing drain to source voltage.

III. COMPARISON OF VVMOS POWER TRANSISTORS WITH MOSFETS

Figure(A.5) shows a conventional horizontal MOSFET.The N^+source and drain are simultaneously diffused into the p-type substrate,which also serves as the body.Current flows horizontally from source to drain through the channel,which is induced on the top surface of the substrate.



Substrate and Body

FIGURE(A.5) The cross section of a conventional MOSFET

The vertical structure of VMOS gives it several important advantages over conventional MOS (16)

1) The length of the channel is determined by diffusion depths,which are much more controllable than the mask spacings used to define the channel length of conventional MOS,so the width/length ratio of the channel -which determines current density-is greater.

2) Each V-groove creates two channels,so current density is inherently doubled,for each gate stripe.

3) The substrate forms the drain contact,so drain metal is not needed on top of the chip.This further reduces chip area and keeps the saturation resistance low.

4) The high current density of VVMOST results in low chip capacitance, especiallly the feedback capacitance (gate-drain) since the overlap

of the gate and drain are kept to a minimum.Extra gate-drain overlap must be allowed in conventional MOSFET's to guard against mask-misalignment,which increases the source-gate and gate-drain capacitance.

5) The VVMOST epi-layer absorbs the depletion region from the reverse biased body-drain P-N diode,and therefore greatly increases the breakdown voltage while it has only a minimal effect on other device parameters (other than adding a series resistance).To fabricate a high voltage MOSFET the body region must be lightly doped so it can absorb the depletion region.The lightly doped material is very sensitive to oxide contamination and good long term stability is hard to achieve.Also,the gate oxide must be thick enough to withstand the entire gate-drain voltage so a high voltage standard MOSFET lacks transconductance.

The output characteristics of VVMOST are similar to a conventional MOSFET with several exceptions.The output conductance is low because of the buffering effect of the epi-region,and the $g_m$is constant above a definite current.VVMOST has a very short channel where,as the drain-source current flow increases,electron velocity saturation results.The constant g_m is one of the consequences resulting from this velocity saturation.The others can be expressed as:The output characteristics assume a constant current plateau,the forward transconductance saturates, and most important,a linear transfer characteristic results.The g_m of a conventional (long channel) MOSFET is proportional to the gate voltage; drain current is therefore proportional to (V_{GS}^2).

IV. COMPARISON OF VVMOS POWER TRANSISTORS WITH BJTs

VVMOSTs uniquely combine the advantages of the power bipolar transistor with those of the MOSFET.The result is a high-power,high-voltage,high-gain power transistor with no minority-carrier storage time,

no thermal runaway and a greatly inhibited secondary breakdown characteristic,all of which are contributing to the spectacular rise in the popularity of the VVMOS power FET.

During the initial phase of construction VVMOST closely resembles the double-diffused epitaxial power bipolar transistor.Both begin with an N^+substrate and an N^-epitaxial into which is first diffused a P and then an N^+layer forming a four-layer structure.One distinguishing feature of VVMOST,as shown in Figure(A.6),is the anisotropically etched V-groove cut normally to the surface that extends through both the N^+,P and into the N^-epitaxial region.By virtue of this V-groove an oxide-insulated gate overlays the P-channel providing fail-safe control over the current path.This current path is established in an identical fashion to that of any enhancement-mode MOSFET.A positive gate potential inverts the P-channel and the resulting electron-enhanced N-channel,extending from the N^+source to the N^-epi,offers an interrupted,low resistance current path devoid of the thermal problems associated with the typical power bipolar transistors.

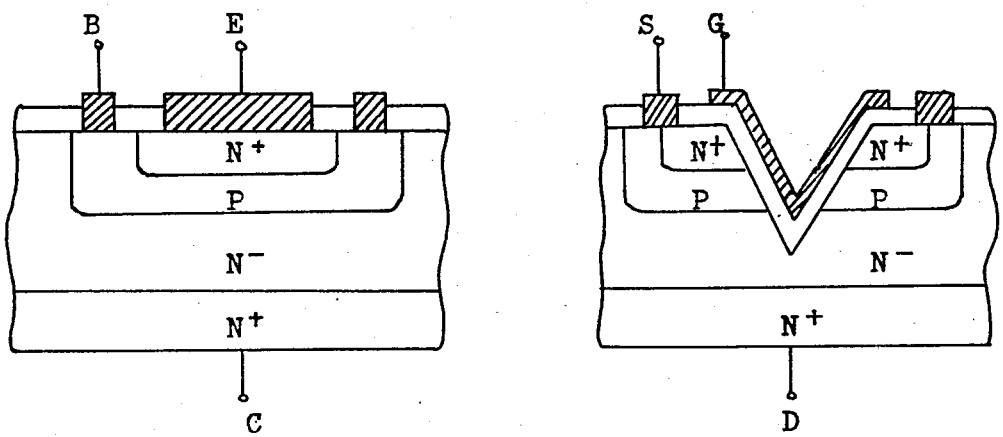
The vertical VMOST structure,like the power bipolar transistor,offers a large surface area for source metal and the entire backside of the chip for the drain.This is of great importance as it allows maximum current carrying capacity unavailable to a non-vertical structure.

Of the advantages that VVMOST has compared to bipolars,many are well known in small signal applications but many others are apparent only at higher power levels.They include:

1) High input impedance-low drive current.The "beta" of a VVMOST device (the output current divided by the input current) is therefore over 10^9.Since the resultant drive power is negligible.
2) No minority carrier storage time.VVMOST is a majority carrier device-its charge carriers are controlled by electric fields,rather than the physical injection and extraction (or recombination) of minority carriers in the active region.The switching delay time is small

and is caused primarily by external parasitic elements.

3) No failure from secondary breakdown or current hogging.Since the temperature coefficient of the VVMOST drain to source ON voltage is positive (a bipolar's is negative),VVMOST draws less current as the device heats up.If the current density were to increase at one particular point of the channel,the temperature rises and the current decreases.The current automatically equalizes throughout the chip, so no hot spots or current crowding-which eventually leads to failure in a bipolar,can develop.Similarly,current is automatically shared between paralleled devices so no ballasting resistors are needed.



FIGURE(A.6) A comparison of a four-layer bipolar transistor with VVMOST

Operationally,VVMOST is unique among power transistors.Channel conduction is proportional to gate voltage,not to any sort of injection current,typical of the bipolar transistor.Whatever input current that does exist beyond that attributed to leakage may be identified as the charging current necessary to overcome the input capacitance in very high-speed switching situations.Because the steady-state gate current is negligible,the familiar parameter,beta,is of little importance. Consequently,VVMOST exhibits a high input resistance that makes it ideal for many logic control applications.

APPENDIX C

COMPUTER PROGRAMS

```
      PROGRAM BJT(BJT,OUTPUT,TAPE5=BJT,TAPE6=OUTPUT)
      DIMENSION T(300),VC(300),AIL(300),R(300),C(300)
C     ***************************************
C     *    ANALYSIS OF BJT SWITCHING CIRCUITS    *
C     *              WITH                        *
C     *  RESISTIVE-INDUCTIVE-CAPACITIVE LOAD     *
C     *              BY USING                    *
C     *      TIME-VARIANT LINEAR BJT MODEL       *
C     ***************************************
C     ********** DATA **********
C     ***************************************
      INTEGER XN
      DATA T1,TRON,TS,TROFF/1.E-6,2.8E-7,6.E-8,1.4E-7/
      DATA EON,VG,RBT,CBMIN/2.,.7,1801.,8.E-11/
      DATA VCC,VCES,RMAX/12.,.2,4.E7/
      DATA RMIN,CMAX,CMIN/.9,6.2E-10,32.6E-12/
      DATA R1,AL1,C1,XN/330.,0.,0.,100/
C     DATA R1,AL1,C1,XN/330.,17.5E-6,0.,100/
C     DATA R1,AL1,C1,XN/330.,17.5E-6,10.E-12,100/
      DELT=TT/XN
C     ********** GENERAL EXPLANATIONS **********
C     ***************************************
C     FUNCTION OF SW:
C     1)IF SW=1.,RELATED VALUES & CURVES ARE TO BE
C       OBTAINED AT THE OUTPUT
C     2)IF SW HAS A DIFFERENT VALUE,ONLY RELATED
C       CURVES ARE TO BE OBTAINED AT THE OUTPUT
      SW=1.
C     ******** CALCULATION OF DELAY TIME **********
C     ***************************************
      I=1
      T(I)=0.
      VBE=0.
    2 VBE=(EON-VBE)*(1.-EXP((-1.*DELT)/(RBT*CBMIN)))
     $+VBE
      IF(VBE.GE.VG) GO TO 1
      I=I+1
      T(I)=T(I-1)+DELT
      GO TO 2
    1 TDON=T(I)
C     ********** PROGRAM **********
C     ***************************************
      I=1
      I1=0
      I2=0
      I3=0
      I4=0
      T(I)=0.
      V01=VCC
      V02=0.
      AI01=0.
      T1=TDON+TRON
      T2=TT/2.+TS
      T3=T2+TROFF
C     ********** TURN-ON DELAY REGION **********
C     ***************************************
      IF(SW.EQ.1.) GO TO 100
      GO TO 200
  100 WRITE(6,3)
      WRITE(6,4)
      WRITE(6,5)
      WRITE(6,6)
  200 CONTINUE
   15 R(I)=RMAX
      C(I)=CMIN
   20 CONTINUE
      IF(AL1.EQ.0.) GO TO 7
      GO TO 8
    7 CONTINUE
      CALL BJTRC(I,VCC,VCES,V01,V02,R,R1,C,C1,A11,
     $A12,A13,A16,AT1,AT2)
      AIL(I)=A12+A13*EXP(-1.*A11*DELT)
      VC(I)=AT1+AT2*EXP(-1.*(1./(R(I)*C(I)))*DELT)+
     $A16*EXP(-1.*A11*DELT)
      GO TO 16
    8 CONTINUE
      IF(R1.EQ.0) GO TO 9
      AI01=(V02/R1)*(1.-EXP(-1.*(R1/AL1)*DELT))+
     $AI01*EXP(-1.*(R1/AL1)*DELT)
      GO TO 10
    9 AI01=(V02/AL1)*DELT+AI01
   10 CONTINUE
      CALL BJTRLCA(I,VCC,VCES,V01,V02,AI01,R,R1,C,
     $C1,AL1,AA1,AA2,AA3,AA4,AB1,AB2)
      DT=AB1**2.-4.*AB2
      IF(DT.LT.0.) GO TO 11
      IF(DT.GT.0.) GO TO 12
      CALL BJTRLCB(I,VCES,V01,R,C,AA1,AA2,AA3,AA4,AB1,
     $B1,B2,B3,BA11,BA33,BB1,BB2)
      AIL(I)=B1+(B2+B3*DELT)*EXP(-1.*(AB1/2.)*DELT)
      VC(I)=BA11+BB1*EXP(-1.*(1./(R(I)*C(I)))*DELT)+
     $(BB2+BA33*DELT)*EXP(-1.*(AB1/2.)*DELT)
   16 CONTINUE
      IF(SW.EQ.1) GO TO 300
      GO TO 400
  300 WRITE(6,13)T(I),VC(I),AIL(I),R(I),C(I),V01,V02,
     $AI01,DT
  400 V01=VC(I)
      V02=VCC-VC(I)
      I=I+1
      T(I)=T(I-1)+DELT
      IF(T(I).GE.TDON) GO TO 14
      GO TO 15
   11 CALL BJTRLCC(I,VCES,V01,R,C,AA1,AA2,AA3,AA4,
     $AB1,AB2,C0,C13,C14,CA1,CB2,CB3,CC)
      AIL(I)=(AA4/AB2)+2.*C13*EXP(-1.*(AB1/2.)*DELT)
     $*COS(C0*DELT)-2.*C14*EXP(-1.*(AB1/2.)*DELT)
     $*SIN(C0*DELT)
      VC(I)=CA1+CC*EXP(-1.*(1./(R(I)*C(I)))*DELT)+CB2*
     $EXP(-1.*(AB1/2.)*DELT)*COS(C0*DELT)-(1./C0)*
     $(((CB2*AB1)/2.)-CB3)*EXP(-1.*(AB1/2.)*DELT)
     $*SIN(C0*DELT)
      GO TO 16
   12 CALL BJTRLCD(I,VCES,V01,R,C,AA1,AA2,AA3,AA4,
     $AB1,AB2,D4,DA1,DB1,DB2,DB3,DC22,DC32,DD1,DD2)
      AIL(I)=DB1+DB2*EXP(D4*DELT)+DB3*EXP(DA1*DELT)
      VC(I)=DD1+DD2*EXP(-1.*(1./(R(I)*C(I)))*DELT)+
     $DC22*EXP(D4*DELT)+DC32*EXP(DA1*DELT)
      GO TO 16
   14 CONTINUE
      IF(T(I).GE.T1) GO TO 17
C     ********** TURN-ON TRANSIENT REGION **********
C     ***************************************
      I1=I1+1
      IF(I1.EQ.1) THEN
      GO TO 500
      ELSE
      GO TO 600
      ENDIF
  500 CONTINUE
      IF(SW.EQ.1.) GO TO 700
      GO TO 600
  700 WRITE(6,18)
      WRITE(6,19)
      WRITE(6,5)
      WRITE(6,6)
  600 R(I)=RMAX*EXP(((T(I)-TDON)/TRON)*ALOG(RMIN/RMAX))
      C(I)=CMIN*EXP(((T(I)-TDON)/TRON)*ALOG(CMAX/CMIN))
      GO TO 20
   17 CONTINUE
      IF(T(I).GE.T2) GO TO 21
C     ********** SATURATION REGION **********
C     ***************************************
      I2=I2+1
      IF(I2.EQ.1) THEN
      GO TO 800
      ELSE
      GO TO 900
      ENDIF
  800 CONTINUE
      IF(SW.EQ.1.) GO TO 1000
      GO TO 900
 1000 WRITE(6,22)
      WRITE(6,23)
      WRITE(6,5)
      WRITE(6,6)
  900 R(I)=RMIN
      C(I)=CMAX
      GO TO 20
   21 CONTINUE
      IF(T(I).GE.T3) GO TO 24
```

```
C     ********** TURN-OFF TRANSIENT REGION **********
C     ***********************************************
      I3=I3+1
      IF(I3.EQ.1) THEN
      GO TO 1100
      ELSE
      GO TO 1200
      ENDIF
 1100 CONTINUE
      IF(SW.EQ.1.) GO TO 1300
      GO TO 1200
 1300 WRITE(6,25)
      WRITE(6,26)
      WRITE(6,5)
      WRITE(6,6)
 1200 R(I)=RMIN*EXP(((T(I)-T2)/TROFF)*ALOG(RMAX/RMIN))
      C(I)=CMAX*EXP(((T(I)-T2)/TROFF)*ALOG(CMIN/CMAX))
      GO TO 20
   24 CONTINUE
      IF(T(I).GE.TT) GO TO 27
C     ********** CUT-OFF REGION **********
C     ************************************
      I4=I4+1
      IF(I4.EQ.1) THEN
      GO TO 1400
      ELSE
      GO TO 1500
      ENDIF
 1400 CONTINUE
      IF(SW.EQ.1.) GO TO 1600
      GO TO 1500
 1600 WRITE(6,28)
      WRITE(6,29)
      WRITE(6,5)
      WRITE(6,6)
 1500 R(I)=RMAX
      C(I)=CMIN
      GO TO 20
   27 CONTINUE
C     ********** TIMING CALCULATION **********
C     ****************************************
      WRITE(6,30)
      WRITE(6,31)
      WRITE(6,32)
      WRITE(6,33)
      WRITE(6,34)DELT,TDON,T1,T2,T3
C     ****** CALCULATION OF DAMPING FREQUENCY *******
C     ************************************************
      PI=3.14
      CT=CMIN+C1
      TD=SQRT(AL1*CT)
      IF(TD.EQ.0.) GO TO 35
      F=(1./(2.*PI*SQRT(AL1*CT)))/1.E6
C     RELATED DAMPING FREQUENCY IS CALCULATED ONLY
C     AT THE CUT-OFF REGION AS MEGAHERTZ
      WRITE(6,36)
      WRITE(6,37)
      WRITE(6,38)F
   35 CONTINUE
C     ********** RELATED CURVES **********
C     ************************************
      WRITE(6,39)
      WRITE(6,40)
      CALL PLOT(111,46,T,VC,XN,0,'*')
      WRITE(6,41)
      WRITE(6,42)
      CALL PLOT(111,46,T,AIL,XN,0,'*')
      WRITE(6,43)
      WRITE(6,44)
      CALL PLOT(111,46,T,R,XN,3,'*')
      WRITE(6,45)
      WRITE(6,46)
      CALL PLOT(111,46,T,C,XN,3,'*')
      WRITE(6,47)
      WRITE(6,48)
C     ********** FORMAT SECTION **********
C     ************************************
    3 FORMAT(/,12X,'THE TURN-ON DELAY REGION:')
    4 FORMAT(12X,'************************')
    5 FORMAT(/,15X,'T(SECOND)',2X,'VC(VOLTS)',2X,
     $'IL(AMPERE)',2X,' R(OHMS) ',2X,' C(FARAD) ',
     $2X,'VO1(VOLTS)',2X,'VO2(VOLTS)',2X,
     $'IO1(AMPERE)',2X,'    DT    ')
    6 FORMAT(15X,'**********',2X,'**********',2X,
     $'**********',2X,'**********',2X,'**********',
     $2X,'**********',2X,'**********',2X,
     $'**********',2X,'**********')
   13 FORMAT(15X,E9.4,2X,E9.4,2X,E10.4,2X,E9.4,2X,
     $E10.4,2X,E10.4,2X,E10.4,2X,E11.4,2X,E10.4)
   18 FORMAT(/,12X,'THE TURN-ON TRANSIENT REGION:')
   19 FORMAT(12X,'**************************')
   22 FORMAT(/,12X,'THE SATURATION REGION:')
   23 FORMAT(12X,'************************')
   25 FORMAT(/,12X,'THE TURN-OFF TRANSIENT REGION:')
   26 FORMAT(12X,'*******************************')
   28 FORMAT(/,12X,'THE CUT-OFF REGION:')
   29 FORMAT(12X,'********************')
   30 FORMAT(/,12X,'THE TIMING CALCULATION:')
   31 FORMAT(12X,'**********************')
   32 FORMAT(/,28X,'DELT=TT/XN',6X,'  TDON  ',5X,
     $'T1=TDON+TRON',4X,'T2=TT/2+TS',4X,'T3=T2+TROFF')
   33 FORMAT(28X,'**********',6X,'**********',5X,
     $'**************',4X,'************',4X,'**************')
   34 FORMAT(28X,E10.4,6X,E8.3,5X,E12.6,4X,E10.4,4X,E11.6)
   36 FORMAT(/,48X,'THE RELATED DAMPING FREQUENCY')
   37 FORMAT(48X,'***************************')
   38 FORMAT(/,39X,'F=1./(2.*PI*SQRT(AL1*(CMIN+C1)))=',
     $E11.5,'MHZ')
   39 FORMAT(/,25X,'RELATED CURVES FOR A BJT SWITCHING ',
     $'CIRCUIT WITH RESISTIVE-INDUCTIVE-CAPACITIVE LOAD')
   40 FORMAT(25X,'*************************************',
     $'*******************************************')
   41 FORMAT(/,60X,'CURVE OF VC(I) VERSUS T(I)')
   42 FORMAT(60X,'*****************************')
   43 FORMAT(/,60X,'CURVE OF AIL(I) VERSUS T(I)')
   44 FORMAT(60X,'******************************')
   45 FORMAT(/,60X,'CURVE OF RLOG(I) VERSUS T(I)')
   46 FORMAT(60X,'*****************************')
   47 FORMAT(/,60X,'CURVE OF CLOG(I) VERSUS T(I)')
   48 FORMAT(60X,'*****************************')
      STOP
      END
```

```
C     ************ SUBROUTINE SECTION ************
C     ********************************************
      SUBROUTINE BJTRC(I,VCC,VCES,V01,V02,R,R1,C,C1,
     $A11,A12,A13,A16,AT1,AT2)
C     THIS SUBROUTINE IS USED FOR THE CASE OF AL1=0.
C     ********************************************
      DIMENSION R(300),C(300)
      A2=R(I)*R1*C(I)*C1*(VCC-V02-V01)
      A3=R(I)*C(I)*(VCC-V01)+R1*C1*(VCC-V02-VCES)
      A4=VCC-VCES
      A6=R(I)*R1*(C(I)+C1)
      A7=R(I)+R1
      A8=A2/A6
      A9=A3/A6
      A10=A4/A6
      A11=A7/A6
      A12=A10/A11
      A13=-1.*((A11**2.)*A8-A11*A9+A10)/A11
      A14=A12*R(I)
      A15=-A14
      A16=A13*R(I)/(1.-A11*R(I)*C(I))
      A17=-A16
      A18=VCES
      A19=-A18
      AT1=A14+A18
      AT2=A15+A17+A19+V01
      RETURN
      END
C     ********************************************
      SUBROUTINE BJTRLCA(I,VCC,VCES,V01,V02,AI01,R,
     $R1,C,C1,AL1,AA1,AA2,AA3,AA4,AB1,AB2)
C     ********************************************
      DIMENSION R(300),C(300)
      A1=R(I)*AL1*C(I)*C1*(VCC-V01-V02)
      A2=R(I)*R1*C(I)*C1*(VCC-V02-V01)+AL1*C1*(VCC
     $-V02-VCES)+AI01*R(I)*AL1*C(I)
      A3=R(I)*C(I)*(VCC-V01)+R1*C1*(VCC-V02-VCES)+
     $AI01*AL1
      A4=VCC-VCES
      A5=R(I)*AL1*(C(I)+C1)
      A6=R(I)*R1*(C(I)+C1)+AL1
      A7=R(I)+R1
      AA1=A1/A5
      AA2=A2/A5
      AA3=A3/A5
      AA4=A4/A5
      AB1=A6/A5
      AB2=A7/A5
      RETURN
      END
C     ********************************************
      SUBROUTINE BJTRLCB(I,VCES,V01,R,C,AA1,AA2,AA3,
     $AA4,AB1,B1,B2,B3,BA11,BA33,BB1,BB2)
C          THIS SUBROUTINE IS USED FOR THE CASE OF
C                    DT=(AB1**2.-4.*AB2)=0.
C     ********************************************
      DIMENSION R(300),C(300)
      B1=(4.*AA4)/(AB1**2.)
      B2=(-1.*(AB1**3.)*AA1+(AB1**2.)*AA2-4.*AA4)/
     $(AB1**2.)
      B3=((AB1**3.)*AA1-2.*(AB1**2.)*AA2+4.*AB1*AA3
     $-8.*AA4)/(4.*AB1)
      BA11=R(I)*B1+VCES
      BA12=-BA11
      BA21=(2.*R(I)*B2)/(AB1*R(I)*C(I)-2.)
      BA22=-BA21
      BA31=-(4.*B3*(R(I)**2.)*C(I))/((AB1*R(I)*C(I)-2.)
     $**2.)
      BA32=-BA31
      BA33=(2.*B3*R(I))/(2.-AB1*R(I)*C(I))
      BB1=BA12+BA21+BA31+V01
      BB2=BA22+BA32
      RETURN
      END
C     ********************************************
      SUBROUTINE BJTRLCC(I,VCES,V01,R,C,AA1,AA2,AA3,
     $AA4,AB1,AB2,C0,C13,C14,CA1,CB2,CB3,CC)
C          THIS SUBROUTINE IS USED FOR THE CASE OF
C                    DT=(AB1**2.-4.*AB2)<0.
C     ********************************************
      DIMENSION R(300),C(300)
      C0=(1./2.)*SQRT(4.*AB2-(AB1**2.))
      C1=(AB1/2.)*(3.*AB2-(AB1**2.))
      C2=C0*(AB1**2.-AB2)
      C3=(AB1**2.)/2.-AB2
      C4=C0*AB1
      C5=-1.*(AB1/2.)
      C6=C0
      C7=((AB1**2.)-4.*AB2)/2.
      C8=C1*AA1+C3*AA2+C5*AA3+AA4
      C9=C2*AA1-C4*AA2+C6*AA3
      C10=C7**2.+C4**2.
      C11=C8*C7-C9*C4
      C12=C9*C7+C8*C4
      C13=C11/C10
      C14=C12/C10
      CA1=(AA4/AB2)*R(I)+VCES
      CA2=-CA1
      CB1=((C13*R(I))*(AB1*R(I)*C(I)-2.)-C14*
     $(R(I)**2.)*C(I)*2.*C0)/(AB2*(R(I)**2.)*
     $(C(I)**2.)-AB1*R(I)*C(I)+1.)
      CB2=-CB1
      CB3=(2.*C0*C14*R(I)*(R(I)*C(I)*AB1-2.)+4.*(R(I)**2.)
     $*C(I)*(C0**2.)*C13+AB1*CB2*(AB2*(R(I)**2.)*(C(I)**2.
     $-AB1*R(I)*C(I)+1.))/(2.*(AB2*R(I)**2.*C(I)**2.-
     $AB1*R(I)*C(I)+1.))
      CC=CA2+CB1+V01
      RETURN
      END
C     ********************************************
      SUBROUTINE BJTRLCD(I,VCES,V01,R,C,AA1,AA2,AA3,
     $AA4,AB1,AB2,D4,DA1,DB1,DB2,DB3,DC22,DC32,DD1,DD2)
C          THIS SUBROUTINE IS USED FOR THE CASE OF
C                    DT=(AB1**2.-4.*AB2)=0.
C     ********************************************
      DIMENSION R(300),C(300)
      D0=(1./2.)*SQRT(AB1**2.-4.*AB2)
      D1=(AB1/2.)*(3.*AB2-AB1**2.)
      D2=(AB1**2.-AB2)*D0
      D3=(AB1**2.)/2.-AB2-AB1*D0
      D4=-1.*(AB1/2.)+D0
      D5=2.*D0
      DA1=-1.*(AB1/2.)-D0
      DA2=(AB1**2.)/2.-AB2+AB1*D0
      DB1=AA4/AB2
      DB2=((D1+D2)*AA1+D3*AA2+D4*AA3+AA4)/(D4*D5)
      DB3=-1.*((D1-D2)*AA1+DA2*AA2+DA1*AA3+AA4)/
     $(DA1*D5)
      DC11=DB1*R(I)
      DC12=-DC11
      DC21=-1.*(DB2*R(I))/(1.+R(I)*C(I)*D4)
      DC22=-DC21
      DC31=-1.*(DB3*R(I))/(1.+DA1*R(I)*C(I))
      DC32=-DC31
      DC41=VCES
      DC42=-DC41
      DD1=DC11+DC41
      DD2=DC12+DC21+DC31+DC42+V01
      RETURN
      END
```

```
C     ****************************************
      SUBROUTINE PLOT(IX,IY,X,Y,N,NL,IPL)
C     IX  : LENGTH OF X AXIS
C     IY  : LENGTH OF Y AXIS
C     X   : X AXIS
C     Y   : Y AXIS
C     N   : NUMBER OF POINTS
C
C        NL             X AXIS          Y AXIS
C        ****           ******          ******
C         0             NORMAL          NORMAL
C         1              LOG             LOG
C         2              LOG            NORMAL
C         3             NORMAL           LOG
C     ****************************************
      DIMENSION X(500),Y(500),U(111),V(56),D(12),E(12)
      CHARACTER *1 A(56,111),F(111)*1,IPL*1
      REAL MIN,MIN1,MAX,MAX1,INCX,INCY
      DO 796 I=1,56
      DO 796 J=1,111
      A(I,J)=' '
  796 CONTINUE
      IF(IX.GT.111.OR.IX.LT.2) IX=111
      IF(IY.GT.56.OR.IY.LT.2) IY=56
      IF(NL.EQ.1.OR.NL.EQ.2) THEN
      DO 87 I=1,N
      X(I)=ALOG10(X(I))
   87 CONTINUE
      END IF
      IF(NL.EQ.1.OR.NL.EQ.3) THEN
      DO 89 I=1,N
      Y(I)=ALOG10(Y(I))
   89 CONTINUE
      END IF
      DO 12 I=1,IX
      F(I)='-'
   12 CONTINUE
      DO 22 I=1,IX,10
      F(I)='+'
   22 CONTINUE
      MIN=X(1)
      MAX=X(1)
      MIN1=Y(1)
      MAX1=Y(1)
      DO 50 I=1,N-1
      IF(X(I+1).GT.MAX) MAX=X(I+1)
      IF(X(I+1).LT.MIN) MIN=X(I+1)
      IF(Y(I+1).GT.MAX1) MAX1=Y(I+1)
      IF(Y(I+1).LT.MIN1) MIN1=Y(I+1)
   50 CONTINUE
      INCX=(MAX-MIN)/(IX-1)
      INCY=(MAX1-MIN1)/(IY-1)
      U(1)=MIN
      V(1)=MIN1
      DO 100 I=1,IX-1
      U(I+1)=U(I)+INCX
  100 CONTINUE
      DO 110 I=1,IY-1
      V(I+1)=V(I)+INCY
  110 CONTINUE
      DO 70 I=1,N
      M=1
      DIFF=ABS(X(I)-U(1))
      DO 80 J=1,IX-1
      IF(ABS(X(I)-U(J+1)).LT.DIFF) THEN
      DIFF=ABS(X(I)-U(J+1))
      M=J+1
      END IF
   80 CONTINUE
      L=1
      DIFF1=ABS(Y(I)-V(1))
      DO 90 J=1,IY-1
      IF(ABS(Y(I)-V(J+1)).LT.DIFF1) THEN
      DIFF1=ABS(Y(I)-V(J+1))
      L=J+1
      END IF
   90 CONTINUE
      A(L,M)=IPL
   70 CONTINUE
      L2=0
      L3=0
      DO 150 I=1,IY,5
      L2=L2+1
      IF(NL.EQ.1.OR.NL.EQ.3) D(L2)=10**V(I)
      IF(NL.NE.1.AND.NL.NE.3) D(L2)=V(I)
  150 CONTINUE
      DO 160 I=1,IX,10
      L3=L3+1
      IF(NL.EQ.1.OR.NL.EQ.2) E(L3)=10**U(I)
      IF(NL.NE.1.AND.NL.NE.2) E(L3)=U(I)
  160 CONTINUE
      IF(NL.EQ.1.OR.NL.EQ.2) THEN
      DO 489 I=1,N
      Y(I)=10**Y(I)
  489 CONTINUE
      END IF
      IF(NL.EQ.1.OR.NL.EQ.3) THEN
      DO 490 I=1,N
      Y(I)=10**Y(I)
  490 CONTINUE
      END IF
      K7=((IY-1)/5)*5+1
      IP=(IX-1)/10+1
      PRINT 300
      DO 120 I=IY,1,-1
      IF(I.EQ.K7) THEN
      K7=K7-5
      L=I/5+1
      PRINT 200, D(L),(A(I,J),J=1,IX)
      GO TO 120
      END IF
      PRINT 300,(A(I,J),J=1,IX)
  120 CONTINUE
      PRINT 400,(F(I),I=1,IX)
      PRINT 450,(E(I),I=1,IP)
      RETURN
  300 FORMAT(1H1,/)
  200 FORMAT(3X,1PE10.2,1X,'+',111A1)
  300 FORMAT(14X,'I',111A1)
  400 FORMAT(15X,111A1,/)
  450 FORMAT(11X,11(1PE9.2,1X),1PE9.2,/)
      END
```

```
      PROGRAM VMOS(VMOS.OUTPUT,TAPE5=VMOS.TAPE6=OUTPUT
      DIMENSION T(300),VGS(300),AIG(300),VDS(300),
     $AID(300),RDS(300),CDS(300)
C     ***********************************************
C     *    ANALYSIS OF VVMOST SWITCHING CIRCUITS    *
C     *                  WITH                       *
C     *     RESISTIVE-INDUCTIVE-CAPACITIVE LOAD     *
C     *                BY USING                     *
C     *     TIME-VARIANT LINEAR  VVMOST MODEL       *
C     ***********************************************
C     ******************* DATA ********************
C     *********************************************
      INTEGER XN
      DATA VDD,EON,EOFF,RG/12.,5.,-5.,2200./
      DATA TT,RDMAX/1.E-6,5.E7/
      DATA CGS,CGD,RDO,VGSO/38.E-12,20.E-12,5.85,3.5/
      DATA FI,H,VT,CDSO/.9,.5,2.5,15.E-9/
      DATA A,ZA,RN/6.5E-3,1.5E-3,5.7/
      DATA R1,AL1,C1,XN/820.,0.,0.,100/
C     DATA R1,AL1,C1,XN/820.,47.E-6,0.,100/
C     DATA R1,AL1,C1,XN/820.,47.E-6,15.E-12,100/
      DELT=TT/XN
C     ************ GENERAL EXPLANATIONS ************
C     **********************************************
C     FUNCTION OF SW:
C     1)IF SW=1.,RELATED VALUES & CURVES ARE TO BE
C       OBTAINED AT THE OUTPUT
C     2)IF SW HAS A DIFFERENT VALUE,ONLY RELATED
C       CURVES ARE TO BE OBTAINED AT THE OUTPUT
      SW=1.
C     ****************** PROGRAM ******************
C     *********************************************
      I=2
      I1=0
      I2=0
      I3=0
      I4=0
      I5=0
      T(I-1)=0.
      T(I)=0.
      TI=0.
      B1=1./((RDO-RN)*(VGSO-VT))
      CIN1=CGS+CGD
      CIN3=CGS+CGD
      VGS(I-1)=0.
      AIG(I-1)=(EON-VGS(I-1))/RG
      VDS(I-1)=VDD
      AID(I-1)=0.
      RDS(I-1)=RDMAX
      CDS(I-1)=(CDSO/((1.+VDS(I-1)/FI)**H))*(A-ZA)
      V01=VDD
      V02=0.
      AI01=0.
C     ************ TURN-ON DELAY REGION ************
C     **********************************************
      IF(SW.EQ.1.) GO TO 100
      GO TO 200
  100 WRITE(6,1)
      WRITE(6,2)
      WRITE(6,3)
      WRITE(6,4)
  200 CONTINUE
   17 RDS(I)=RDMAX
      VGS(I)=(EON-VGS(I-1))*(1.-EXP((-1.*(T(I)-TI))/
     $(RG*CIN1)))+VGS(I-1)
      TI=T(I)
   20 CONTINUE
      IF(T(I).GE.TT/2.) GO TO  5
      AIG(I)=(EON-VGS(I))/RG
      GO TO 6
    5 AIG(I)=(EOFF-VGS(I))/RG
    6 CDS(I)=(CDSO/((1.+VDS(I-1)/FI)**H))*(A-ZA)
      IF(AL1.EQ.0.) GO TO 7
      GO TO 8
    7 CONTINUE
      CALL MOSRC(I,VDD,V01,V02,RDS,R1,CDS,C1,A11,A12,
     $A13,A14,A16,AT)
      AID(I)=A12+A13*EXP(-1.*A11*DELT)
      VD3(I)=A14+AT*EXP(-1.*(1./(RDS(I)*CDS(I)))*
     $DELT)+A16*EXP(-1.*A11*DELT)
      GO TO 500
    8 CONTINUE
      IF(R1.EQ.0.) GO TO 9
      AI01=(V02/R1)*(1.-EXP(-1.*(R1/AL1)*DELT))+
     $AI01*EXP(-1.*(R1/AL1)*DELT)
      GO TO 10
    9 AI01=(V02/AL1)*DELT+AI01
   10 CONTINUE
      CALL MOSRLCA(I,VDD,V01,V02,AI01,RDS,R1,CDS,
     $C1,AL1,AA1,AA2,AA3,AA4,AB1,AB2)
      DT=AB1**2.-4.*AB2
      IF(DT.LT.0.) GO TO 11
      IF(DT.GT.0.) GO TO 12
      CALL MOSRLCB(I,V01,RDS,CDS,AA1,AA2,AA3,AA4,
     $AB1,B1,B2,B3,BA11,BA33,BB1,BB2)
      AID(I)=B1+(B2+B3*DELT)*EXP(-1.*(AB1/2.)*DELT)
      VDS(I)=BA11+BB1*EXP(-1.*(1./(RDS(I)*CDS(I)))*
     $DELT)+(BB2+BA33*DELT)*EXP(-1.*(AB1/2.)*DELT)
  500 CONTINUE
      IF(SW.EQ.1) GO TO 300
      GO TO 400
  300 WRITE(6,13)T(I),VGS(I),AIG(I),VDS(I),AID(I),
     $RDS(I),CDS(I),V01,V02,AI01,DT
  400 V01=VDS(I)
      V02=VDD-VDS(I)
      I=I+1
      T(I)=T(I-1)+DELT
      IF(T(I).GE.TT/2.) GO TO 14
      IF((VGS(I-1)-VT).GE.VDS(I-1)) GO TO 15
      IF(VGS(I-1).GE.VT) GO TO 16
      GO TO 17
   11 CALL MOSRLCC(I,V01,RDS,CDS,AA1,AA2,AA3,AA4,AB1,
     $AB2,C0,C13,C14,CA1,CB2,CB3,CC)
      AID(I)=(AA4/AB2)+2.*C13*EXP(-1.*(AB1/2.)*DELT)
     $*COS(C0*DELT)-2.*C14*EXP(-1.*(AB1/2.)*DELT)
     $*SIN(C0*DELT)
      VDS(I)=CA1+CC*EXP(-1.*(1./(RDS(I)*CDS(I)))*DELT)
     $CB2*EXP(-1.*(AB1/2.)*DELT)*COS(C0*DELT)-(1./C0)*
     $(((CB2*AB1)/2.)-CB3)*EXP(-1.*(AB1/2.)*DELT)
     $*SIN(C0*DELT)
      GO TO 500
   12 CALL MOSRLCD(I,V01,RDS,CDS,AA1,AA2,AA3,AA4,AB1,
     $AB2,D4,DA1,DB1,DB2,DB3,DC11,DC22,DC32,DD)
      AID(I)=DB1+DB2*EXP(D4*DELT)+DB3*EXP(DA1*DELT)
      VDS(I)=DC11+DD*EXP(-1.*(1./(RDS(I)*CDS(I)))*DELT)
     $+DC22*EXP(D4*DELT)+DC32*EXP(DA1*DELT)
      GO TO 500
   16 CONTINUE
C     ************** PINCH-OFF REGION **************
C     **********************************************
      I1=I1+1
      IF(I1.EQ.1) THEN
      GO TO 600
      ELSE
      GO TO 700
      ENDIF
  600 TDON=T(I)
      IF(SW.EQ.1.) GO TO 800
      GO TO 700
  800 WRITE(6,18)
      WRITE(6,19)
      WRITE(6,3)
      WRITE(6,4)
  700 RDS(I)=VDS(I-1)/(BT*((VGS(I-1)-VT)**2.))+RN
      CIN2=CIN1+ABS(((VDS(I-1)-VDS(I-2))/(VGS(I-1)-
     $VGS(I-2)))*CGD)
      VGS(I)=(EON-VGS(I-1))*(1.-EXP((-1.*DELT)/(RG*
     $CIN2)))+VGS(I-1)
      GO TO 20
   15 CONTINUE
C     ************** RESISTIVE REGION **************
C     **********************************************
      I2=I2+1
      IF(I2.EQ.1) THEN
      GO TO 900
      ELSE
      GO TO 1000
      ENDIF
  900 TF=T(I)-TDON
      IF(SW.EQ.1.) GO TO 1100
      GO TO 1000
 1100 WRITE(6,21)
      WRITE(6,22)
      WRITE(6,3)
```

```
      WRITE(6,4)
 1000 RDS(I)=1./(BT*(VGS(I-1)-VT))+RN
      VGS(I)=(EON-VGS(I-1))*(1.-EXP((-1.*DELT)/(RG*
     $CIN3)))+VGS(I-1)
      GO TO 20
   14 CONTINUE
C     ***************** SECOND PART ******************
C     ************************************************
      IF(T(I).GE.TT) GO TO 23
      IF(VGS(I-1).LE.VT) GO TO 24
      IF((VGS(I-1)-VT).LE.VDS(I-1)) GO TO 25
C     ************** RESISTIVE REGION ****************
C     ************************************************
      I3=I3+1
      IF(I3.EQ.1) THEN
      GO TO 1200
      ELSE
      GO TO 1300
      ENDIF
 1200 CONTINUE
      IF(SW.EQ.1.) GO TO  1400
      GO TO 1300
 1400 WRITE(6,21)
      WRITE(6,22)
      WRITE(6,3)
      WRITE(6,4)
 1300 RDS(I)=1./(BT*(VGS(I-1)-VT))+RN
      VGS(I)=(EOFF-VGS(I-1))*(1.-EXP((-1.*DELT)/(RG*
     $CIN3)))+VGS(I-1)
      GO TO 20
   25 CONTINUE
C     *************** PINCH-OFF REGION ***************
C     ************************************************
      I4=I4+1
      IF(I4.EQ.1) THEN
      GO TO 1500
      ELSE
      GO TO 1600
      ENDIF
 1500 TON=T(I)-(TDON+TF)
      TDOFF=T(I)-TT/2.
      IF(SW.EQ.1.) GO TO 1700
      GO TO 1600
 1700 WRITE(6,18)
      WRITE(6,19)
      WRITE(6,3)
      WRITE(6,4)
 1600 RDS(I)=VDS(I-1)/(BT*((VGS(I-1)-VT)**2.))+RN
      CIN2=CIN1+ABS(((VDS(I-1)-VDS(I-2))/(VGS(I-1)-
     $VGS(I-2)))*CGD)
      VGS(I)=(EOFF-VGS(I-1))*(1.-EXP((-1.*DELT)/(RG*
     $CIN2)))+VGS(I-1)
      GO TO 20
   24 CONTINUE
C     ***************** CUT-OFF REGION ***************
C     ************************************************
      I5=I5+1
      IF(I5.EQ.1) THEN
      GO TO 1800
      ELSE
      GO TO 1900
      ENDIF
 1800 TR=T(I)-(TDON+TF+TON)
      TOFF=TT-(TF+TON+TR)
      IF(SW.EQ.1.) GO TO 2000
      GO TO 1900
 2000 WRITE(6,26)
      WRITE(6,27)
      WRITE(6,3)
      WRITE(6,4)
 1900 RDS(I)=RDMAX
      VGS(I)=(EOFF-VGS(I-1))*(1.-EXP((-1.*DELT)/(RG*
     $CIN1)))+VGS(I-1)
      GO TO 20
   23 CONTINUE
C     ************** TIMING CALCULATION *************
C     ************************************************
      WRITE(6,28)
      WRITE(6,29)
      WRITE(6,30)
      WRITE(6,31)
      WRITE(6,32)TDON,TF,TON,TDOFF,TR,TOFF
C     ****** CALCULATION OF DAMPING FREQUENCY *******
C     ************************************************
      PI=3.14
      CT=CDS(I-1)+C1
      TD=SQRT(AL1*CT)
      IF(TD.EQ.0.) GO TO 33
      F=(1./(2.*PI*SQRT(AL1*CT)))/1.E6
C     RELATED DAMPING FREQUENCY IS CALCULATED ONLY
C     AT THE CUT-OFF REGION AS MEGAHERTZ
      WRITE(6,34)
      WRITE(6,35)
      WRITE(6,36)F
   33 CONTINUE
C     ************** RELATED CURVES **************
C     ********************************************
      WRITE(6,37)
      WRITE(6,38)
      CALL PLOT(111,46,T,VDS,XN,0.,'*')
      WRITE(6,39)
      WRITE(6,40)
      CALL PLOT(111,46,T,AID,XN,0.,'*')
      WRITE(6,41)
      WRITE(6,42)
      CALL PLOT(111,46,T,VGS,XN,0.,'*')
      WRITE(6,43)
      WRITE(6,44)
      CALL PLOT(111,46,T,AIG,XN,0,'*')
      WRITE(6,45)
      WRITE(6,46)
      CALL PLOT(111,46,T,RDS,XN,3,'*')
      WRITE(6,47)
      WRITE(6,48)
      CALL PLOT(111,46,T,CDS,XN,3.,'*')
      WRITE(6,49)
      WRITE(6,50)
C     ************** FORMAT SECTION **************
C     ********************************************
    1 FORMAT(/,1X,'THE TURN-ON DELAY REGION:')
    2 FORMAT(1X,'************************')
    3 FORMAT(/,3X,'T(SECOND)',2X,'VGS(VOLTS)',2X,
     $'IG(AMPERE)',2X,'VDS(VOLTS)',2X,'ID(AMPERE)',
     $2X,' RDS(OHMS) ',2X,'CDS(FARAD)',2X,
     $'VO1(VOLTS)',2X,'VO2(VOLTS)',2X,'IO1(AMPERE)',
     $2X,'    DT    ')
    4 FORMAT(3X,'**********',2X,'**********',2X,
     $'**********',2X,'**********',2X,'**********',
     $2X,'***********',2X,'**********',2X,
     $'**********',2X,'**********',2X,'***********',
     $2X,'********')
   13 FORMAT(3X,E9.3,2X,E10.4,2X,E10.4,2X,E10.4,2X,
     $E10.4,2X,E11.4,2X,E10.4,2X,E10.4,2X,E10.4,2X,
     $E11.4,2X,E8.2)
   18 FORMAT(/,1X,'THE PINCH-OFF REGION:')
   19 FORMAT(1X,'**********************')
   21 FORMAT(/,1X,'THE RESISTIVE REGION:')
   22 FORMAT(1X,'**********************')
   26 FORMAT(/,1X,'THE CUT-OFF REGION:')
   27 FORMAT(1X,'******************')
   28 FORMAT(/,1X,'THE TIMING CALCULATION:')
   29 FORMAT(1X,'**********************')
   30 FORMAT(/,25X,'    TDON    ',2X,'     TR     ',2X,
     $'    TON    ',2X,'   TDOFF   ',2X,'     TF     ',
     $2X,'    TOFF    ')
   31 FORMAT(25X,'**********',2X,'**********',2X,
     $'*********',2X,'*********',2X,'**********',
     $2X,'**********')
   32 FORMAT(25X,E10.4,2X,E10.4,2X,E9.3,2X,E9.3,2X,
     $E10.4,2X,E10.4)
   34 FORMAT(/,48X,'THE RELATED DAMPING FREQUENCY')
   35 FORMAT(48X,'***************************')
   36 FORMAT(/,40X,'F=1./(2.*PI*SQRT(AL1*(CDS+C1)))= ',
     $E10.4,'MHZ')
   37 FORMAT(/,20X,'RELATED CURVES FOR A VVMOST SWITCHING
     $' CIRCUIT WITH RESISTIVE-INDUCTIVE-CAPACITIVE LOAD
   38 FORMAT(20X,'**************************************
     $'**********************************')
   39 FORMAT(/,55X,'CURVE OF VDS(I) VERSUS T(I)')
   40 FORMAT(55X,'**************************')
   41 FORMAT(/,55X,'CURVE OF AID(I) VERSUS T(I)')
   42 FORMAT(55X,'**************************')
   43 FORMAT(/,55X,'CURVE OF VGS(I) VERSUS T(I)')
   44 FORMAT(55X,'**************************')
   45 FORMAT(/,55X,'CURVE OF AIG(I) VERSUS T(I)')
   46 FORMAT(55X,'**************************')
   47 FORMAT(/,55X,'CURVE OF RDSLOG(I) VERSUS T(I)')
   48 FORMAT(55X,'**************************')
   49 FORMAT(/,55X,'CURVE OF CDSLOG(I) VERSUS T(I)')
   50 FORMAT(55X,'**************************')
      STOP
      END
```

```
C     ********** SUBROUTINE SECTION **********                    C
C     ***************************************
      SUBROUTINE MOSRC(I,VDD,V01,V02,RDS,R1,CDS,C1,
     $A11,A12,A13,A14,A16,AT)                                     C
C     THIS SUBROUTINE IS USED FOR THE CASE OF AL1=0.C
C     ***************************************                    C
      DIMENSION RDS(300),CDS(300)
      A2=RDS(I)*R1*CDS(I)*C1*(VDD-V01-V02)
      A3=RDS(I)*CDS(I)*(VDD-V01)+R1*C1*(VDD-V02)
      A4=VDD
      A6=RDS(I)*R1*(CDS(I)+C1)
      A7=RDS(I)+R1
      A8=A2/A6
      A9=A3/A6
      A10=A4/A6
      A11=A7/A6
      A12=A10/A11
      A13=-1.*((A11**2.)*A8-A11*A9+A10)/A11
      A14=A12*RDS(I)
      A15=-A14
      A16=(A13*RDS(I))/(1.-A11*RDS(I)*CDS(I))
      A17=-A16
      AT=A15+A17+V01
      RETURN
      END
C     ***************************************
      SUBROUTINE MOSRLCA(I,VDD,V01,V02,AI01,RDS,
     $C1,CDS,C1,AL1,AA1,AA2,AA3,AA4,AB1,AB2)
C     ***************************************
      DIMENSION RDS(300),CDS(300)
      A1=RDS(I)*AL1*CDS(I)*C1*(VDD-V02-V01)
      A2=RDS(I)*R1*CDS(I)*C1*(VDD-V01-V02)+AL1*C1*
     $(VDD-V02)+AI01*RDS(I)*AL1*CDS(I)
      A3=RDS(I)*CDS(I)*(VDD-V01)+R1*C1*(VDD-V02)+
     $AI01*AL1
      A4=VDD
      A5=RDS(I)*AL1*(CDS(I)+C1)                                   C
      A6=RDS(I)*R1*(CDS(I)+C1)+AL1
      A7=RDS(I)+R1
      AA1=A1/A5
      AA2=A2/A5                                                   C
      AA3=A3/A5                                                   C
      AA4=A4/A5                                                   C
      AB1=A6/A5
      AB2=A7/A5
      RETURN
      END
C     ***************************************
      SUBROUTINE MOSRLCB(I,V01,RDS,CDS,AA1,AA2,
     $AA3,AA4,AB1,B1,B2,B3,BA11,BA33,BB1,BB2)
C        THIS SUBROUTINE IS USED FOR THE CASE OF
C              DT=(AB1**2.-4.*AB2)=0.
C     ***************************************
      DIMENSION RDS(300),CDS(300)
      B1=(4.*AA4)/(AB1**2.)
      B2=(-1.*(AB1**3.)*AA1+(AB1**2.)*AA2-AA4)/
     $(AB1**2.)
      B3=((AB1**3.)*AA1-2.*(AB1**2.)*AA2+4.*AB1*
     $AA3-8.*AA4)/(4.*AB1)
      BA11=RDS(I)*B1
      BA12=-BA11
      BA21=(2.*RDS(I)*B2)/(AB1*RDS(I)*CDS(I)-2.)
      BA22=-BA21
      BA31=(4.*B3*(RDS(I)**2.)*CDS(I))/((AB1*RDS(I)
     $*CDS(I)-2.)**2.)
      BA32=-BA31
      BA33=(2.*B3*RDS(I))/(2.-AB1*RDS(I)*CDS(I))
      BB1=BA12+BA21+BA31+V01
      BB2=BA22+BA32
      RETURN
      END

      ***************************************
      SUBROUTINE MOSRLCC(I,V01,RDS,CDS,AA1,AA2,AA3,
     $AA4,AB1,AB2,C0,C13,C14,CA1,CB2,CB3,CC)
        THIS SUBROUTINE IS USED FOR THE CASE OF
          DT=(AB1**2.-4.*AB2)<0.
      ***************************************
      DIMENSION RDS(300),CDS(300)
      C0=(1./2.)*SQRT(4.*AB2-(AB1**2.))
      C1=(AB1/2.)*(3.*AB2-(AB1**2.))
      C2=C0*(AB1**2.-AB2)
      C3=(AB1**2.)/2.-AB2
      C4=C0*AB1
      C5=-1.*(AB1/2.)
      C6=C0
      C7=((AB1**2.)-4.*AB2)/2.
      C8=C1*AA1+C3*AA2+C5*AA3+AA4
      C9=C2*AA1-C4*AA2+C6*AA3
      C10=C7**2.+C4**2.
      C11=C8*C7-C9*C4
      C12=C9*C7+C8*C4
      C13=C11/C10
      C14=C12/C10
      CA1=(AA4/AB2)*RDS(I)
      CA2=-CA1
      CB1=((C13*RDS(I))*(AB1*RDS(I)*CDS(I)-2.)-C14*
     $(RDS(I)**2.)*CDS(I)*2.*C0)/(AB2*(RDS(I)**2.)*
     $(CDS(I)**2.)-AB1*RDS(I)*CDS(I)+1.)
      CB2=-CB1
      CB3=(2.*C0*C14*RDS(I)*(RDS(I)*CDS(I)*AB1-2.)+
     $4.*(RDS(I)**2.)*CDS(I)*(C0**2.)*C13+AB1*CB2
     $*(AB2*(RDS(I)**2.)*(CDS(I)**2.)-AB1*RDS(I)*
     $CDS(I)+1.))/(2.*(AB2*(RDS(I)**2.)*(CDS(I)**2.)
     $-AB1*RDS(I)*CDS(I)+1.))
      CC=CA2+CB1+V01
      RETURN
      END
      ***************************************
      SUBROUTINE MOSRLCD(I,V01,RDS,CDS,AA1,AA2,AA3,
     $AA4,AB1,AB2,D4,DA1,DB1,DB2,DB3,DC11,DC22,DC32,
     $DD)
        THIS SUBROUTINE IS USED FOR THE CASE OF
              DT=(AB1**2.-4.*AB2)=0.
      ***************************************
      DIMENSION RDS(300),CDS(300)
      D0=(1./2.)*SQRT(AB1**2.-4.*AB2)
      D1=(AB1/2.)*(3.*AB2-AB1**2.)
      D2=(AB1**2.-AB2)*D0
      D3=(AB1**2.)/2.-AB2-AB1*D0
      D4=-1.*(AB1/2.)+D0
      D5=2.*D0
      DA1=-1.*(AB1/2.)-D0
      DA2=(AB1**2.)/2.-AB2+AB1*D0
      DB1=AA4/AB2
      DB2=((D1+D2)*AA1+D3*AA2+D4*AA3+AA1)/
     $(D4*D5)
      DB3=-1.*((D1-D2)*AA1+DA2*AA2+DA1*AA3+
     $AA4)/(DA1*D5)
      DC11=DB1*RDS(I)
      DC12=-DC11
      DC21=-1.*(DB2*RDS(I))/(1.+RDS(I)*CDS(I)*D4)
      DC22=-DC21
      DC31=-1.*(DB3*RDS(I))/(1.+DA1*RDS(I)*CDS(I))
      DC32=-DC31
      DD=DC12+DC21+DC31+V01
      RETURN
      END
```

```
      PROGRAM DMOS(DMOS,OUTPUT,TAPE5=DMOS,TAPE6=OUTPUT)
      DIMENSION T(300),VGS(300),AIG(300),VDS(300),
     $AID(300),RDS(300),CDS(300)
C     ****************************************
C     *   ANALYSIS OF VDMOST SWITCHING CIRCUITS    *
C     *                WITH                        *
C     *    RESISTIVE-INDUCTIVE-CAPACITIVE LOAD     *
C     *                BY USING                    *
C     *      TIME-VARIANT LINEAR VDMOST MODEL      *
C     ****************************************
C     ****************** DATA ********************
C     ****************************************
      INTEGER XN
      DATA VDD,EON,EOFF,RI/20.,12.,0.,29.5/
      DATA TT,XN,RDMAX/1.E-6,100,5.E7/
      DATA CDS,CGD,RDO,VGSO/550.E-12,600.E-12..14,10./
      DATA FI,H,VT,CDSO/.9,.5,3.4,11.E-10/
      DATA RG,CP,RD,RS/4.5,30.E-12,.07,.005/
      DATA R1,AL1,C1/5.,0.,0./
      DELT=TT/XN
C     ********** GENERAL EXPLANATIONS **********
C     ****************************************
C     FUNCTION OF SW:
C     1)IF SW=1..RELATED VALUES & CURVES ARE TO BE
C       OBTAINED AT THE OUTPUT
C     2)IF SW HAS A DIFFERENT VALUE,ONLY RELATED
C       CURVES ARE TO BE OBTAINED AT THE OUTPUT
      SW=1.
C     ****************** PROGRAM *******************
C     ****************************************
      I=2
      I1=0
      I2=0
      I3=0
      I4=0
      I5=0
      T(I-1)=0.
      T(I)=0.
      TI=0.
      BT=1./(2.*(RDO-RS-RD)*(VGSO-VT))
      RGT=RG+RI
      CIN1=CGS+CGD
      CIN3=CGS+CGD
      VGS(I-1)=0.
      AIG(I-1)=(EON-VGS(I-1))/RGT
      VDS(I-1)=VDD
      AID(I-1)=0.
      RDS(I-1)=RDMAX
      CDS(I-1)=(CDSO/((1.+VDS(I-1)/FI)**H))+CP
      V01=VDD
      V02=0.
      AI01=0.
C     ********** TURN-ON DELAY REGION **********
C     ****************************************
      IF(SW.EQ.1.) GO TO 100
      GO TO 200
  100 WRITE(6,1)
      WRITE(6,2)
      WRITE(6,3)
      WRITE(6,4)
  200 CONTINUE
   17 RDS(I)=RDMAX
      VGS(I)=(EON-VGS(I-1))*(1.-EXP((-1.*(T(I)-TI))/
     $(RGT*CIN1)))+VGS(I-1)
      TI=T(I)
   20 CONTINUE
      IF(T(I).GE.TT/2.) GO TO  5
      AIG(I)=(EON-VGS(I))/RGT
      GO TO 6
    5 AIG(I)=(EOFF-VGS(I))/RGT
    6 CDS(I)=(CDSO/((1.+VDS(I-1)/FI)**H))+CP
      IF(AL1.EQ.0.) GO TO 7
      GO TO 8
    7 CONTINUE
      CALL MOSRC(I,VDD,V01,V02,RDS,R1,CDS,C1,A11,A12,
     $A13,A14,A16,AT)
      AID(I)=A12+A13*EXP(-1.*A11*DELT)
      VDS(I)=A14+AT*EXP(-1.*(1./(RDS(I)*CDS(I)))*DELT)+
     $A16*EXP(-1.*A11*DELT)
      GO TO 500
    8 CONTINUE
      IF(R1.EQ.0.) GO TO 9
      AI01=(V02/R1)*(1.-EXP(-1.*(R1/AL1)*DELT))+
     $AI01*EXP(-1.*(R1/AL1)*DELT)
      GO TO 10
    9 AI01=(V02/AL1)*DELT+AI01
   10 CONTINUE
      CALL MOSRLCA(I,VDD,V01,V02,AI01,RDS,R1,CDS,
     $C1,AL1,AA1,AA2,AA3,AA4,AB1,AB2)
      DT=AB1**2.-4.*AB2
      IF(DT.LT.0.) GO TO 11
      IF(DT.GT.0.) GO TO 12
      CALL MOSRLCB(I,V01,RDS,CDS,AA1,AA2,AA3,AA4,
     $AB1,B1,B2,B3,BA11,BA33,BB1,BB2)
      AID(I)=B1+(B2+B3*DELT)*EXP(-1.*(AB1/2.)*DELT)
      VDS(I)=BA11+BB1*EXP(-1.*(1./(RDS(I)*CDS(I)))*DELT)+
     $(BB2+BA33*DELT)*EXP(-1.*(AB1/2.)*DELT)
  500 CONTINUE
      IF(SW.EQ.1) GO TO 300
      GO TO 400
  300 WRITE(6,13)T(I),VGS(I),AIG(I),VDS(I),AID(I),RDS(I),
     $CDS(I),V01,V02,AI01,DT
  400 V01=VDS(I)
      V02=VDD-VDS(I)
      I=I+1
      T(I)=T(I-1)+DELT
      IF(T(I).GE.TT/2.) GO TO 14
      IF((VGS(I-1)-VT).GE.VDS(I-1)) GO TO 15
      IF(VGS(I-1).GE.VT) GO TO 16
      GO TO 17
   11 CALL MOSRLCC(I,V01,RDS,CDS,AA1,AA2,AA3,AA4,AB1,
     $AB2,C0,C13,C14,CA1,CB2,CB3,CC)
      AID(I)=(AA4/AB2)+2.*C13*EXP(-1.*(AB1/2.)*DELT)
     $*COS(C0*DELT)-2.*C14*EXP(-1.*(AB1/2.)*DELT)
     $*SIN(C0*DELT)
      VDS(I)=CA1+CC*EXP(-1.*(1./(RDS(I)*CDS(I)))*DELT)+
     $CB2*EXP(-1.*(AB1/2.)*DELT)*COS(C0*DELT)-(1./C0)*
     $(((CB2*AB1)/2.)-CB3)*EXP(-1.*(AB1/2.)*DELT)
     $*SIN(C0*DELT)
      GO TO 500
   12 CALL MOSRLCD(I,V01,RDS,CDS,AA1,AA2,AA3,AA4,AB1,
     $AB2,D4,DA1,DB1,DB2,DB3,DC11,DC22,DC32,DD)
      AID(I)=DB1+DB2*EXP(D4*DELT)+DB3*EXP(DA1*DELT)
      VDS(I)=DC11+DD*EXP(-1.*(1./(RDS(I)*CDS(I)))*DELT)
     $+DC22*EXP(D4*DELT)+DC32*EXP(DA1*DELT)
      GO TO 500
   16 CONTINUE
C     ********** PINCH-OFF REGION **********
C     ****************************************
      I1=I1+1
      IF(I1.EQ.1) THEN
      GO TO 600
      ELSE
      GO TO 700
      ENDIF
  600 TDON=T(I)
      IF(SW.EQ.1.) GO TO 800
      GO TO 700
  800 WRITE(6,18)
      WRITE(6,19)
      WRITE(6,3)
      WRITE(6,4)
  700 RDS(I)=VDS(I-1)/(BT*((VGS(I-1)-VT)**2.))+RS
      CIN2=CIN1+ABS(((VDS(I-1)-VDS(I-2))/(VGS(I-1)-
     $VGS(I-2)))*CGD)
      VGS(I)=(EON-VGS(I-1))*(1.-EXP((-1.*DELT)/(RGT*
     $CIN2)))+VGS(I-1)
      GO TO 20
   15 CONTINUE
C     ********** RESISTIVE REGION **********
C     ****************************************
      I2=I2+1
      IF(I2.EQ.1) THEN
      GO TO 900
      ELSE
      GO TO 1000
      ENDIF
  900 TF=T(I)-TDON
      IF(SW.EQ.1.) GO TO 1100
      GO TO 1000
 1100 WRITE(6,21)
      WRITE(6,22)
      WRITE(6,3)
      WRITE(6,4)
 1000 RDS(I)=1./(BT*(VGS(I-1)-VT))+RS+RD
```

```
      VGS(I)=(EON-VGS(I-1))*(1.-EXP((-1.*DELT)/(RGT*
     $CIN3)))+VGS(I-1)
      GO TO 20
   14 CONTINUE
C     ************** SECOND PART ***************
C     ******************************************
      IF(T(I).GE.TT) GO TO 23
      IF(VGS(I-1).LE.VT) GO TO 24
      IF((VGS(I-1)-VT).LE.VDS(I-1)) GO TO 25
C     ************** RESISTIVE REGION **************
C     ******************************************
      I3=I3+1
      IF(I3.EQ.1) THEN
      GO TO 1200
      ELSE
      GO TO 1300
      ENDIF
 1200 CONTINUE
      IF(SW.EQ.1.) GO TO  1400
      GO TO 1300
 1400 WRITE(6,21)
      WRITE(6,22)
      WRITE(6,3)
      WRITE(6,4)
 1300 RDS(I)=1./(BT*(VGS(I-1)-VT))+RS+RD
      VGS(I)=(EOFF-VGS(I-1))*(1.-EXP((-1.*DELT)/(RGT*
     $CIN3)))+VGS(I-1)
      GO TO 20
   25 CONTINUE
C     ************** PINCH-OFF REGION **************
C     ******************************************
      I4=I4+1
      IF(I4.EQ.1) THEN
      GO TO 1500
      ELSE
      GO TO 1600
      ENDIF
 1500 TON=T(I)-(TDON+TF)
      TDOFF=T(I)-TT/2.
      IF(SW.EQ.1.) GO TO 1700
      GO TO 1600
 1700 WRITE(6,18)
      WRITE(6,19)
      WRITE(6,3)
      WRITE(6,4)
 1600 RDS(I)=VDS(I-1)/(BT*((VGS(I-1)-VT)**2.))+RS
      CIN2=CIN1+ABS(((VDS(I-1)-VDS(I-2))/(VGS(I-1)-
     $VGS(I-2)))*CGD)
      VGS(I)=(EOFF-VGS(I-1))*(1.-EXP((-1.*DELT)/(RGT*
     $CIN2)))+VGS(I-1)
      GO TO 20
   24 CONTINUE
C     ************** CUT-OFF REGION **************
C     ********************************************
      I5=I5+1
      IF(I5.EQ.1) THEN
      GO TO 1800
      ELSE
      GO TO 1900
      ENDIF
 1800 TR=T(I)-(TDON+TF+TON)
      TOFF=TT-(TF+TON+TR)
      IF(SW.EQ.1.) GO TO 2000
      GO TO 1900
 2000 WRITE(6,26)
      WRITE(6,27)
      WRITE(6,3)
      WRITE(6,4)
 1900 RDS(I)=RDMAX
      VGS(I)=(EOFF-VGS(I-1))*(1.-EXP((-1.*DELT)/(RGT*
     $CIN1)))+VGS(I-1)
      GO TO 20
   23 CONTINUE
C     ************** TIMING CALCULATION ************
C     **********************************************
      WRITE(6,28)
      WRITE(6,29)
      WRITE(6,30)
      WRITE(6,31)
      WRITE(6,32)TDON,TF,TON,TDOFF,TR,TOFF
C     ****** CALCULATION OF DAMPING FREQUENCY ******
C     **********************************************
      PI=3.14
      CT=CDS(I-1)+C1
      PD=SQRT(AL1*CT)
      IF(PD.EQ.0.) GO TO 33
      F=(1./(2.*PI*SQRT(AL1*CT)))/1.E6
C     RELATED DAMPING FREQUENCY IS CALCULATED ONLY
C     AT THE CUT-OFF REGION AS MEGAHERTZ
      WRITE(6,34)
      WRITE(6,35)
      WRITE(6,36)F
   33 CONTINUE
C     ************** RELATED CURVES ****************
C     **********************************************
      WRITE(6,37)
      WRITE(6,38)
      CALL PLOT(111,46,T,VDS,XN,0,'*')
      WRITE(6,39)
      WRITE(6,40)
      CALL PLOT(111,46,T,AID,XN,0,'*')
      WRITE(6,41)
      WRITE(6,42)
      CALL PLOT(111,46,T,VGS,XN,0,'*')
      WRITE(6,43)
      WRITE(6,44)
      CALL PLOT(111,46,T,AIG,XN,0,'*')
      WRITE(6,45)
      WRITE(6,46)
      CALL PLOT(111,46,T,RDS,XN,3,'*')
      WRITE(6,47)
      WRITE(6,48)
      CALL PLOT(111,46,T,CDS,XN,3.'*')
      WRITE(6,49)
      WRITE(6,50)
C     ************** FORMAT SECTION ****************
C     **********************************************
    1 FORMAT(/,1X,'THE TURN-ON DELAY REGION:')
    2 FORMAT(1X,'************************')
    3 FORMAT(/,3X,'T(SECOND)',2X,'VGS(VOLTS)',2X,
     $'IG(AMPERE)',2X,'VDS(VOLTS)',2X,'ID(AMPERE)',
     $2X,' RDS(OHMS) ',2X,'CDS(FARAD)',2X,
     $'V01(VOLTS)',2X,'V02(VOLTS)',2X,'I01(AMPERE)
     $2X,'   DT   ')
    4 FORMAT(3X,'**********',2X,'**********',2X,
     $'**********',2X,'**********',2X,'**********',
     $2X,'**********',2X,'**********',2X,
     $'**********',2X,'**********',2X,'**********',
     $2X,'********')
   13 FORMAT(3X,E9.3,2X,E10.4,2X,E10.4,2X,E10.4,2X,
     $E10.4,2X,E11.4,2X,E10.4,2X,E10.4,2X,E10.4,2X,
     $E11.4,2X,E8.2)
   18 FORMAT(/,1X,'THE PINCH-OFF REGION:')
   19 FORMAT(1X,'********************')
   21 FORMAT(/,1X,'THE RESISTIVE REGION:')
   22 FORMAT(1X,'********************')
   26 FORMAT(/,1X,'THE CUT-OFF REGION:')
   27 FORMAT(1X,'*****************')
   28 FORMAT(/,1X,'THE TIMING CALCULATION:')
   29 FORMAT(1X,'**********************')
   30 FORMAT(/,25X,'   TDON   ',2X,'    TR    ',2X,
     $'   TON   ',2X,'  TDOFF  ',2X,'    TF    ',
     $2X,'   TOFF   ')
   31 FORMAT(25X,'**********',2X,'**********',2X,
     $'**********',2X,'**********',2X,'**********',
     $2X,'**********')
   32 FORMAT(25X,E10.4,2X,E10.4,2X,E9.3,2X,E9.3,2X,
     $E10.4,2X,E10.4)
   34 FORMAT(/,48X,'THE RELATED DAMPING FREQUENCY')
   35 FORMAT(48X,'****************************')
   36 FORMAT(/,40X,'F=1./(2.*PI*SQRT(AL1*(CDS+C1)))=
     $E10.4,'MHZ')
   37 FORMAT(/,20X,'RELATED CURVES FOR A VDMOST',
     $' SWITCHING CIRCUIT WITH RESISTIVE-INDUCTIVE
     $'CAPACITIVE LOAD')
   38 FORMAT(20X,'************************',
     $'**************************************
     $'***************')
   39 FORMAT(/,55X,'CURVE OF VDS(I) VERSUS T(I)')
   40 FORMAT(55X,'***************************')
   41 FORMAT(/,55X,'CURVE OF AID(I) VERSUS T(I)')
   42 FORMAT(55X,'***************************')
   43 FORMAT(/,55X,'CURVE OF VGS(I) VERSUS T(I)')
   44 FORMAT(55X,'***************************')
   45 FORMAT(/,55X,'CURVE OF AIG(I) VERSUS T(I)')
   46 FORMAT(55X,'***************************')
   47 FORMAT(/,55X,'CURVE OF RDSLOG(I) VERSUS T(I)')
   48 FORMAT(55X,'*************************** )
   49 FORMAT(/,55X,'CURVE OF CDSLOG(I) VERSUS T(I)
   50 FORMAT(55X,'*************************** ,
      STOP
      END
```

```
      PROGRAM APL(INV.OUTPUT,TAPE5=INV.TAPE6=OUTPUT)
      DIMENSION T(300),RA(300),RB(300),CA(300),
     $CB(300),VA(300),VB(300),VGSN(300),VGSP(300),
     $AIGN(300),AIGP(300),AIDN(300)
C     ***********************************************
C     *                APPLICATION                  *
C     *                   OF                        *
C     *     TIME-VARIANT LINEAR VDMOST MODEL        *
C     *                   TO                        *
C     *           A CVDMOS INVERTER                 *
C     ***********************************************
C     ********** DATA **********
C     ***********************************************
      INTEGER XN
      DATA VDD,RI,EON,EOFF/10.,100.,10.,0./
      DATA TT,XN,RDMAXN,RDMAXP/1.E-6,100,12.E7,12.E7/
      DATA CGSN,CGDN,CPN/75.E-12,5.E-12/
      DATA RDON,VGSON/15.,10./
      DATA FIN,HN,VTN,CDSON/.9,.5,3.4,100.E-12/
      DATA RSN,RDN,RGN/.05,.7,4.5/
      DATA CGSP,CGDP/75.E-12,5.E-12/
      DATA RDOP,VGSOP/15.,-10./
      DATA FIP,HP,VTP,CDSOP/.9,.5,-3.4,100.E-12/
      DATA RSP,RDP,RGP/.05,.7,4.5/
      DELT=TT/XN
C     ********** GENERAL EXPLANATIONS **********
C     ***********************************************
C     FUNCTION OF SW:
C     1)IF SW=1.,RELATED VALUES & CURVES ARE TO BE
C       OBTAINED AT THE OUTPUT
C     2)IF SW HAS A DIFFERENT VALUE,ONLY RELATED
C       CURVES ARE TO BE OBTAINED AT THE OUTPUT
      SW=1.
C     ***********************************************
C     ******* EXPLANATION OF THE PARAMETERS ******
C     RA(I)=RDSN(I)
C     RB(I)=RDSP(I)
C     CA(I)=CDSN(I)
C     CB(I)=CDSP(I)
C     VA(I)=VDSN(I)
C     VB(I)=VDSP(I)
C     ***********************************************
C     ***************** PROGRAM ******************
C     INITIAL CONDITIONS:
C     """""""""""""""""""
      I=2
      I1=0
      I2=0
      I3=0
      I4=0
      I5=0
      I6=0
      I7=0
      I8=0
      BTN=1./(2.*(RDON-RSN-RDN)*(VGSON-VTN))
      BTP=ABS(1./(2.*(RDOP-RSP-RDP)*(VGSOP-VTP)))
      RGTN=RI+RGN
      RGTP=RI+RGP
      CIN1N=CGSN+CGDN
      CIN3N=CGSN+CGDN
      CIN1P=CGSP+CGDP
      CIN3P=CGSP+CGDP
      T(I-1)=0.
      VA(I-1)=VDD
      VB(I-1)=0.
      AIDN(I-1)=0.
      CA(I-1)=(CDSON/((1.+VA(I-1)/FIN)**HN))
      CB(I-1)=(CDSOP/((1.-VB(I-1)/FIP)**HP))
      VGSN(I-1)=0.
      VGSP(I-1)=-VDD
      RA(I-1)=RDMAXN
      RB(I-1)=ABS(1./(BTP*(VGSP(I-1)-VTP)))+RSP+RDP
      AIGN(I-1)=(EON-VGSN(I-1))/RGTN
      AIGP(I-1)=(EON-VDD-VGSP(I-1))/RGTP
      IF(SW.EQ.1.) GO TO 100
      GO TO 200
  100 WRITE(6,1)
      WRITE(6,2)
      WRITE(6,3)T(I-1),VGSN(I-1),AIGN(I-1),VA(I-1),
     $AIDN(I-1),RA(I-1),CA(I-1),VGSP(I-1),AIGP(I-1),
     $VB(I-1),RB(I-1),CB(I-1)
  200 CONTINUE
      GO TO 4
   37 CONTINUE
      IF(T(I).GE.TT/2.) GO TO 5
      AIGN(I)=(EON-VGSN(I))/RGTN
      GO TO 6
    5 AIGN(I)=(EOFF-VGSN(I))/RGTN
    6 CONTINUE
      CALL INVERT(I,VDD,VA,VB,RA,RB,CA,CB,A1,A2,A7,
     $F1,F2,F3,F4,H1,H3,H4,H5,H6)
      AIDN(I)=F1+F2*EXP(-1.*A1*DELT)+F3*EXP(-1.*A2*
     $DELT)+F4*EXP(-1.*A7*DELT)
      VA(I)=H1+H6*EXP(-1.*A1*DELT)+H3*DELT*EXP(-1.*A1*
     $DELT)+H4*EXP(-1.*A2*DELT)+H5*EXP(-1.*A7*DELT)
      VB(I)=VA(I)-VDD
      IF(SW.EQ.1.) GO TO 300
      GO TO 400
  300 WRITE(6,3)T(I),VGSN(I),AIGN(I),VA(I),AIDN(I),
     $RA(I),CA(I),VGSP(I),AIGP(I),VB(I),RB(I),CB(I)
  400 I=I+1
    4 T(I)=T(I-1)+DELT
      IF(T(I).GE.TT) GO TO 7
      CA(I)=(CDSON/((1.+VA(I-1)/FIN)**HN))
      CB(I)=(CDSOP/((1.-VB(I-1)/FIP)**HP))
      IF(T(I).GE.TT/2.) GO TO 8
      IF(VGSP(I-1).GE.VTP) GO TO 9
      IF((VGSP(I-1)-VTP).GE.VB(I-1)) GO TO 10
      GO TO 11
    8 CONTINUE
C     HALF PERIOD
      IF((VGSP(I-1)-VTP).LE.VB(I-1)) GO TO 12
      IF(VGSP(I-1).LE.VTP) GO TO 13
      GO TO 14
   11 CONTINUE
C     THE FIRST REGION:
C     """""""""""""""""
C     P-CHANNEL VDMOST:RESISTIVE REGION
      IF(SW.EQ.1.) GO TO 500
      GO TO 600
  500 WRITE(6,15)
      WRITE(6,16)
      WRITE(6,17)
  600 RB(I)=ABS(1./(BTP*(VGSP(I-1)-VTP)))+RSP+RDP
      VGSP(I)=(EON-VDD-VGSP(I-1))*(1.-EXP((-1.*DELT)/
     $(RGTP*CIN3P)))+VGSP(I-1)
   28 CONTINUE
      IF(T(I).GE.TT/2.) GO TO 18
      AIGP(I)=(EON-VDD-VGSP(I))/RGTP
      IF(VGSN(I-1).LE.VTN) GO TO 19
      IF((VGSN(I-1)-VTN).GE.VA(I-1)) GO TO 20
      GO TO 21
   18 AIGP(I)=(EOFF-VDD-VGSP(I))/RGTP
      IF(VGSN(I-1).LE.VTN) GO TO 22
      IF((VGSN(I-1)-VTN).LE.VA(I-1)) GO TO 23
      GO TO 24
   10 CONTINUE
C     THE SECOND REGION:
C     """""""""""""""""""
C     P-CHANNEL VDMOST:PINCH-OFF REGION
      I1=I1+1
      IF(I1.EQ.1) GO TO 700
      GO TO 800
  700 TDOFFP=T(I)
  800 CONTINUE
      IF(SW.EQ.1.) GO TO 900
      GO TO 1000
  900 WRITE(6,25)
      WRITE(6,26)
      WRITE(6,27)
 1000 RB(I)=ABS(VB(I-1)/(BTP*((VGSP(I-1)-VTP)**2.)))+RSP
      CIN2P=CIN1P+ABS(((VB(I-1)-VB(I-2))/(VGSP(I-1)-
     $VGSP(I-2)))*CGDP)
      VGSP(I)=(EON-VDD-VGSP(I-1))*(1.-EXP((-1.*DELT)/
     $(RGTP*CIN2P)))+VGSP(I-1)
      GO TO 28
    9 CONTINUE
C     THE THIRD REGION:
C     """""""""""""""""
C     P-CHANNEL VDMOST:CUT-OFF REGION
      I2=I2+1
      IF(I2.EQ.1) GO TO 1100
      GO TO 1200
 1100 TRP=T(I)-TDOFFP
```

```
 1200 CONTINUE
      IF(SW.EQ.1.) GO TO 1300
      GO TO 1400
 1300 WRITE(6,29)
      WRITE(6,30)
      WRITE(6,31)
 1400 RB(I)=RDMAXP
      VGSP(I)=(EON-VDD-VGSP(I-1))*(1.-EXP((-1.*DELT)/
     $(RGTP*CIN1P)))+VGSP(I-1)
      GO TO 28
   14 CONTINUE
C     HALF PERIOD
C     P-CHANNEL VDMOST:CUT-OFF REGION
      IF(SW.EQ.1.) GO TO 1500
      GO TO 1600
 1500 WRITE(6,29)
      WRITE(6,30)
      WRITE(6,31)
 1600 RB(I)=RDMAXP
      VGSP(I)=(EOFF-VDD-VGSP(I-1))*(1.-EXP((-1.*DELT)/
     $(RGTP*CIN1P)))+VGSP(I-1)
      GO TO 28
   13 CONTINUE
C     THE FORTH REGION:
C     *****************
C     P-CHANNEL VDMOST:PINCH-OFF REGION
      I3=I3+1
      IF(I3.EQ.1) GO TO 1700
      GO TO 1800
 1700 TOFFP=T(I)-(TDOFFP+TRP)
      TDONP=T(I)-TT/2.
 1800 CONTINUE
      IF(SW.EQ.1.) GO TO 1900
      GO TO 2000
 1900 WRITE(6,32)
      WRITE(6,33)
      WRITE(6,27)
 2000 RB(I)=ABS(VB(I-1)/(BTP*((VGSP(I-1)-VTP)**2.)))+RSP
      CIN2P=CIN1P+ABS(((VB(I-1)-VB(I-2))/(VGSP(I-1)-
     $VGSP(I-2)))*CGDP)
      VGSP(I)=(EOFF-VDD-VGSP(I-1))*(1.-EXP((-1.*DELT)/
     $(RGTP*CIN2P)))+VGSP(I-1)
      GO TO 28
   12 CONTINUE
C     THE FIFTH REGION:
C     *****************
C     P-CHANNEL VDMOST:RESISTIVE REGION
      I4=I4+1
      IF(I4.EQ.1) GO TO 2100
      GO TO 2200
 2100 TFP=T(I)-(TDOFFP+TRP+TOFFP)
      TONP=TT-(TRP+TOFFP+TFP)
 2200 CONTINUE
      IF(SW.EQ.1.) GO TO 2300
      GO TO 2400
 2300 WRITE(6,34)
      WRITE(6,35)
      WRITE(6,17)
 2400 RB(I)=ABS(1./(BTP*(VGSP(I-1)-VTP)))+RSP+RDP
      VGSP(I)=(EOFF-VDD-VGSP(I-1))*(1.-EXP((-1.*DELT)/
     $(RGTP*CIN3P)))+VGSP(I-1)
      GO TO 28
   19 CONTINUE
C     N-CHANNEL VDMOST:CUT-OFF REGION
      IF(SW.EQ.1.) GO TO 2500
      GO TO 2600
 2500 WRITE(6,36)
      WRITE(6,1)
      WRITE(6,2)
 2600 RA(I)=RDMAXN
      VGSN(I)=(EON-VGSN(I-1))*(1.-EXP((-1.*DELT)/(RGTN*
     $CIN1N)))+VGSN(I-1)
      GO TO 37
   21 CONTINUE
C     N-CHANNEL VDMOST:PINCH-OFF REGION
      I5=I5+1
      IF(I5.EQ.1) GO TO 2700
      GO TO 2800
 2700 TDONN=T(I)
 2800 CONTINUE
      IF(SW.EQ.1.) GO TO 2900
      GO TO 3000
 2900 WRITE(6,38)
      WRITE(6,1)
      WRITE(6,2)
 3000 RA(I)=VA(I-1)/(BTN*((VGSN(I-1)-VTN)**2.))+RSN
      CIN2N=CIN1N+ABS(((VA(I-1)-VA(I-2))/(VGSN(I-1)-
     $VGSN(I-2)))*CGDN)
      VGSN(I)=(EON-VGSN(I-1))*(1.-EXP((-1.*DELT)/(RGTN*
     $CIN2N)))+VGSN(I-1)
      GO TO 37
   20 CONTINUE
C     N-CHANNEL VDMOST:RESISTIVE REGION
      I6=I6+1
      IF(I6.EQ.1) GO TO 3100
      GO TO 3200
 3100 TFN=T(I)-TDONN
 3200 CONTINUE
      IF(SW.EQ.1.) GO TO 3300
      GO TO 3400
 3300 WRITE(6,39)
      WRITE(6,1)
      WRITE(6,2)
 3400 RA(I)=1./(BTN*(VGSN(I-1)-VTN))+RSN+RDN
      VGSN(I)=(EON-VGSN(I-1))*(1.-EXP((-1.*DELT)/
     $(RGTN*CIN3N)))+VGSN(I-1)
      GO TO 37
   24 CONTINUE
C     N-CHANNEL VDMOST:RESISTIVE REGION
      IF(SW.EQ.1.) GO TO 3500
      GO TO 3600
 3500 WRITE(6,39)
      WRITE(6,1)
      WRITE(6,2)
 3600 RA(I)=1./(BTN*(VGSN(I-1)-VTN))+RSN+RDN
      VGSN(I)=(EOFF-VGSN(I-1))*(1.-EXP((-1.*DELT)/
     $(RGTN*CIN3N)))+VGSN(I-1)
      GO TO 37
   23 CONTINUE
C     N-CHANNEL VDMOST:PINCH-OFF REGION
      I7=I7+1
      IF(I7.EQ.1) GO TO 3700
      GO TO 3800
 3700 TONN=T(I)-(TDONN+TFN)
      TDOFFN=T(I)-TT/2.
 3800 CONTINUE
      IF(SW.EQ.1.) GO TO 3900
      GO TO 4000
 3900 WRITE(6,38)
      WRITE(6,1)
      WRITE(6,2)
 4000 RA(I)=VA(I-1)/(BTN*((VGSN(I-1)-VTN)**2.))+RSN
      CIN2N=CIN1N+ABS(((VA(I-1)-VA(I-2))/(VGSN(I-1)-
     $VGSN(I-2)))*CGDN)
      VGSN(I)=(EOFF-VGSN(I-1))*(1.-EXP((-1.*DELT)/(RGTN*
     $CIN2N)))+VGSN(I-1)
      GO TO 37
   22 CONTINUE
C     N-CHANNEL VDMOST:CUT-OFF REGION
      I8=I8+1
      IF(I8.EQ.1) GO TO 4100
      GO TO 4200
 4100 TRN=T(I)-(TDONN+TFN+TONN)
      TOFFN=TT-(TFN+TONN+TRN)
 4200 CONTINUE
      IF(SW.EQ.1.) GO TO 4300
      GO TO 4400
 4300 WRITE(6,36)
      WRITE(6,1)
      WRITE(6,2)
 4400 RA(I)=RDMAXN
      VGSN(I)=(EOFF-VGSN(I-1))*(1.-EXP((-1.*DELT)/(RGTN*
     $CIN1N)))+VGSN(I-1)
      GO TO 37
    7 CONTINUE
C     ********** TIMING CALCULATION **********
C     ****************************************
      WRITE(6,40)
      WRITE(6,41)
      WRITE(6,42)
      WRITE(6,43)
      WRITE(6,44)TDONN,TFN,TONN,TDOFFN,TRN,TOFFN
      WRITE(6,45)
      WRITE(6,46)
      WRITE(6,47)
      WRITE(6,48)
      WRITE(6,49)TDOFFP,TRP,TOFFP,TDONP,TFP,TONP
      WRITE(6,50)
C     ********** RELATED CURVES **********
C     ************************************
```

```
      WRITE(6,51)
      WRITE(6,52)
      CALL PLOT(111,46,T,VA,XN,0,'*')
      WRITE(6,53)
      WRITE(6,54)
      CALL PLOT(111,46,T,VB,XN,0,'*')
      WRITE(6,55)
      WRITE(6,56)
      CALL PLOT(111,46,T,AIDN,XN,0,'*')
      WRITE(6,57)
      WRITE(6,58)
      CALL PLOT(111,46,T,VGSN,XN,0,'*')
      WRITE(6,59)
      WRITE(6,60)
      CALL PLOT(111,46,T,AIGN,XN,0,'*')
      WRITE(6,61)
      WRITE(6,62)
      CALL PLOT(111,46,T,VGSP,XN,0,'*')
      WRITE(6,63)
      WRITE(6,64)
      CALL PLOT(111,46,T,AIGP,XN,0,'*')
      WRITE(6,65)
      WRITE(6,66)
      CALL PLOT(111,46,T,RA,XN,3,'*')
      WRITE(6,67)
      WRITE(6,68)
      CALL PLOT(111,46,T,RB,XN,3,'*')
      WRITE(6,69)
      WRITE(6,70)
      CALL PLOT(111,46,T,CA,XN,3,'*')
      WRITE(6,71)
      WRITE(6,72)
      CALL PLOT(111,46,T,CB,XN,3,'*')
      WRITE(6,73)
      WRITE(6,74)
C     ************** FORMAT SECTION **************
C     ********************************************
    1 FORMAT(8X,'   T    ',2X,'  VGSN  ',2X,'   IGN   '
     $,2X,'  VDDT  ',2X,'  AIDN  ',2X,'  RDSN  ',2X,
     $'  CDSN  ',2X,'  VGSP  ',2X,'   IGP   ',2X,
     $'  VDSP  ',2X,'  RDSP  ',2X,'  CDSP  ')
    2 FORMAT(8X,'********',2X,'********',2X,'*********',
     $2X,'********',2X,'********',2X,'********',2X,
     $'********',2X,'********',2X,'********',
     $2X,'********',2X,'********',2X,'********')
    3 FORMAT(8X,E7.2,2X,E8.2,2X,E9.2,2X,E8.2,2X,
     $E8.2,2X,E8.2,2X,E8.2,2X,E8.2,2X,E9.2,2X,E8.2,
     $2X,E8.2,2X,E8.2)
   15 FORMAT(/,2X,'THE FIRST REGION:')
   16 FORMAT(2X,'*****************')
   17 FORMAT(2X,'P-CHANNEL VDMOST:RESISTIVE REGION')
   25 FORMAT(/,2X,'THE SECOND REGION:')
   26 FORMAT(2X,'******************')
   27 FORMAT(2X,'P-CHANNEL VDMOST:PINCH-OFF REGION')
   29 FORMAT(/,2X,'THE THIRD REGION:')
   30 FORMAT(2X,'*****************')
   31 FORMAT(2X,'P-CHANNEL VDMOST:CUT-OFF REGION')
   32 FORMAT(/,2X,'THE FOURTH REGION:')
   33 FORMAT(2X,'******************')
   34 FORMAT(/,2X,'THE FIFTH REGION:')
   35 FORMAT(2X,'*****************')
   36 FORMAT(2X, N-CHANNEL VDMOST:CUT-OFF REGION')
   38 FORMAT(2X,'N-CHANNEL VDMOST:PINCH-OFF REGION')
   39 FORMAT(2X,'N-CHANNEL VDMOST:RESISTIVE REGION')
   40 FORMAT(///,2X,'THE TIMING CALCULATION FOR N-',
     $'CHANNEL VDMOST')
   41 FORMAT(2X,'*****************************',
     $'**************')
   42 FORMAT(28X,'   TDONN   ',2X,'   TFN   ',2X,
     $'   TONN   ',2X,'  TDOFFN  ',2X,'   TRN   ',
     $2X,'   TOFFN  ')
   43 FORMAT(28X,'**********',2X,'*********',2X,
     $'**********',2X,'**********',2X,'*********',
     $2X,'*********')
   44 FORMAT(28X,E11.4,2X,E9.3,2X,E10.4,2X,E10.4,2X,
     $E9.3,2X,E9.3)
   45 FORMAT(/,2X,'THE TIMING CALCULATION FOR P-',
     $'CHANNEL VDMOST')
   46 FORMAT(2X,'*****************************',
     $'**************')
   47 FORMAT(/,28X,'   TDOFFP   ',2X,'   TRP   ',2X,
     $'   TOFFP   ',2X,'   TDONP   ',2X,'   TFP   ',
     $2X,'   TONP   ')
   48 FORMAT(28X,'**********',2X,'*********',2X,
     $'**********',2X,'**********',2X,'*********',
     $2X,'*********')
   49 FORMAT(28X,E12.4,2X,E9.3,2X,E9.3,2X,E11.4,
     $2X,E9.3,2X,E10.4)
   50 FORMAT(1H1)
   51 FORMAT(//,40X,'RELATED CURVES FOR A COMPLEMENTARY
     $'VDMOST INVERTER')
   52 FORMAT(40X,'**********************************',
     $'**********')
   53 FORMAT(/,55X,'CURVE OF VA(I) VERSUS T(I)')
   54 FORMAT(55X,'''''''''''''''''''''''''''''')
   55 FORMAT(/,55X,'CURVE OF VB(I) VERSUS T(I)')
   56 FORMAT(55X,'''''''''''''''''''''''''''''')
   57 FORMAT(/,55X,'CURVE OF AIDN(I) VERSUS T(I)')
   58 FORMAT(55X,'''''''''''''''''''''''''''''')
   59 FORMAT(/,55X,'CURVE OF VGSN(I) VERSUS T(I)')
   60 FORMAT(55X,'''''''''''''''''''''''''''''')
   61 FORMAT(/,55X,'CURVE OF AIGN(I) VERSUS T(I)')
   62 FORMAT(55X,'''''''''''''''''''''''''''''')
   63 FORMAT(/,55X,'CURVE OF VGSP(I) VERSUS T(I)')
   64 FORMAT(55X,'''''''''''''''''''''''''''''')
   65 FORMAT(/,55X,'CURVE OF AIGP(I) VERSUS T(I)')
   66 FORMAT(55X,'''''''''''''''''''''''''''''')
   67 FORMAT(/,55X,'CURVE OF RALOG(I) VERSUS T(I)')
   68 FORMAT(55X,'''''''''''''''''''''''''''''')
   69 FORMAT(/,55X,'CURVE OF RBLOG(I) VERSUS T(I)')
   70 FORMAT(55X,'''''''''''''''''''''''''''''')
   71 FORMAT(/,55X,'CURVE OF CALOG(I) VERSUS T(I)')
   72 FORMAT(55X,'''''''''''''''''''''''''''''')
   73 FORMAT(/,55X,'CURVE OF CBLOG(I) VERSUS T(I)')
   74 FORMAT(55X,'''''''''''''''''''''''''''''')
      STOP
      END
C     ********************************************
C     ************ SUBROUTINE SECTION ************
      SUBROUTINE INVERT(I,VDD,VA,VB,RA,RB,CA,CB,A1,
     $A2,A7,F1,F2,F3,F4,H1,H3,H4,H5,H6)
      DIMENSION RA(300),RB(300),CA(300),CB(300),
     $VA(300),VB(300)
      A1=1./(RA(I)*CA(I))
      A2=1./(RB(I)*CB(I))
      A3=CA(I)*RA(I)*RB(I)+RA(I)*RB(I)*CB(I)
      A4=RA(I)+RB(I)
      A5=RA(I)*CA(I)+RB(I)*CB(I)
      A6=CA(I)*CB(I)*RA(I)*RB(I)
      A7=A4/A3
      B0=VDD*A1*A2
      B1=VDD*(A1+A2+A1*A2*A5)-VA(I-1)*A2+VB(I-1)*A1
      B2=VDD*(1.+A2*A5+A1*A5+A1*A2*A6)-VA(I-1)*(1.+
     $A2*A5)+VB(I-1)*(1.+A1*A5)
      B3=VDD*(A5+A2*A6+A1*A6)-VA(I-1)*(A5+A2*A6)+
     $VB(I-1)*(A5+A1*A6)
      B4=A6*(VDD-VA(I-1)+VB(I-1))
      D0=B0/A3
      D1=B1/A3
      D2=B2/A3
      D3=B3/A3
      D4=B4/A3
      E0=D0/CA(I)
      E1=D1/CA(I)
      E2=D2/CA(I)
      E3=D3/CA(I)
      E4=D4/CA(I)
      F1=D0/(A1*A2*A7)
      F2=(D4*(A1**4.)-D3*(A1**3.)+D2*(A1**2.)-D1*A1
     $+D0)/(A1*(A1-A2)*(A7-A1))
      F3=(D4*(A2**4.)-D3*(A2**3.)+D2*(A2**2.)-D1*A2
     $+D0)/(A2*(A2-A1)*(A7-A2))
      F4=(D4*(A7**4.)-D3*(A7**3.)+D2*(A7**2.)-D1*A7
     $+D0)/(A7*(A7-A1)*(A2-A7))
      H1=E0/((A1**2.)*A2*A7)
      H2=((A2+A7)*(-1.*2.*(A1**5.)*E4+E3*(A1**4.)-E1*
     $(A1**2.)+2.*A1*E0)+A2*A7*(3.*E4*(A1**4.)-2.*
     $E3*(A1**3.)+E2*(A1**2.)-E0)+(A1**6.)*E4-
     $(A1**4.)*E2+(A1**3.)*2.*E1-3.*E0*(A1**2.))/
     $((A1**2.)*((A2-A1)**2.)*((A7-A1)**2.))
      H3=(E4*(A1**4.)-E3*(A1**3.)+E2*(A1**2.)-E1*A1
     $+E0)/(A1*(A1-A2)*(A7-A1))
      H4=(E4*(A2**4.)-E3*(A2**3.)+E2*(A2**2.)-E1*A2
     $+E0)/(A2*((A1-A2)**2.)*(A2-A7))
      H5=(E4*(A7**4.)-E3*(A7**3.)+E2*(A7**2.)-E1*A7
     $+E0)/(A7*((A1-A7)**2.)*(A7-A2))
      H6=H2+VA(I-1)
      RETURN
      END
```

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