140 Mb/s DEQPSK MODEM IF STAGE

by

M. Akif Suyabatmaz

B.S. in EE., Boğaziçi University, 1982

Submitted to Institude for Graduate Studies in Science and Engineering in partial fullfillment of the requirements for the degree of

Master of Science

in

Electrical Engineering

Boğaziçi University

1985

140 Mb/s DEQPSK MODEM

IF STAGE

This Thesis has been approved :

Y. Doç. Dr. Ömer CERİD

(Thesis Supervisior)

Prof. Dr. Ergür TÜTÜNCÜOĞLU

Y. Doç. Dr. Avni MORGÜL

ACKNOWLEDGEMENTS

I wish to acknowledge my indebteness to the project manager, Mr. Ali Beygu, for his drive and enthusiasm, to Y. Doç.Dr. Ömer Cerid, who consulted and helped me during and before the preparation of this thesis.

I must especially thank to Mr. Hüseyin Kalman, for his endless patience, and to all staff of Scientific and Technical Research Council of Turkey who provided me the proper working conditions for the completion of this thesis.

I also wish to express my deep appreciation to my parents for their consent, support and patience not only for the completion of this thesis, but all through my life.

ABSTRACT

Recently, as the digital technology progresses, the exploding capacity of digital information nececities fast digital communication systems. Since the congestion prevailing in many regions of radio frequency spectrum has created the need for improved spectrum utilization techniques, the demand for multilevel (M-ary) digital modulation techniques has also increased.

In this thesis, a differentially encoded and differentially decoded quadrature phase shift keyed modem, employing coherent demodulator, was briefly analyzed. System building blocks were investigated and the one, proper to high data rate application, was chosen for system realization.

A working circuit was build as an intermediate frequency (IF) stage, operating at 140 Mbit per second, and realized.

ÖZETÇE

Günümüzde sayısal bilgi iletim sistemine olan ihtiyaç, sayısal verilerin artımına paralel olarak hızla artmaktadır. Veri kapasitesindeki büyüklük hızlı sayısal iletimi gerektirmekte, hızlı sayısal iletim ise güç tasarrufu yapan sayısal modulasyon biçimleri yerine, band tasarrufu yapan çok seviyeli sayısal modulasyon biçimlerini gerekli kılmaktadır.

Bu tezde farksal kodlayıcı ve farksal kod çözücü birimlerini içeren, eşzamanlı demodulasyon prensibini uygulamaya koyan, dört seviyeli faz kodlamalı (QPSK) modulasyon biçimi kısaca analiz edilmiştir. Sistemi oluşturan birimlerin çeşitli işleme yordamları incelenmiş, hızlı iletim sistemine uygun olanı uygulamaya konalarak 140 Mbit/s veri hızı ile çalışan bir sistem ara-frekans katı olarak gerçekleştirilmiştir.

TABLE OF CONTENTS

4. Modulator and summer

5. IF amplifier

6. Demodulator input stage

7. Symbol timing recovery (STR)

8. Carrier recovery (C.R.)

Chapter 4: Evaluation and Conclusion

References

Appandices : A - 1 : Bandpass signals

A - 2 : Bandpass stationary stochastic process representation

A - 3 : M-ary PSK signal representation interms of equivalent low-pass form.

A - 4 : Spectral characteristics of digitally modulated signals.

B - 1 : PLL, Brief theory

B - 2 : Wide-band phase spilitting networks.

B - 3 : Resistive summer and spilitter networks.

IC specifications :

MHF-3P : Double balanced mixer

PM 101 : Biphase modulator

SP 9685: Fast comparator and latch

U 264 : 1 GHz, divide by 64, prescaler

TABLE OF SYMBOLS

$\{a_n\}$: Random binary sequence, serial input data stream into the modulator.

$\{\hat{a}_n\}$: Reconstructed random binary sequence, serial output of the demodulator.

r_b : Rate of the random binary sequence, $\{a_n\}$ $r_b=1/T_b$ (bit/sec.)

$\hat{r}_b$: Reconstructed rate of the random binary sequence, $\{\hat{a}_n\}$. $\hat{r}_b=1/T_b$ (bit/sec.)

CL_s : Clock signal having rate r_b(or $\hat{r}_b$).

$\{I_n\} \triangleq \{I_{in}I_{on}\}$: 4-level symbol sequence, output of the serial to parallel converte

$\{\hat{I}_n\} \triangleq \{\hat{I}_{in}\hat{I}_{on}\}$: Reconstructed 4-level symbol sequence, parallel data steram into the parallel to serial converter.

r_s : rate of the symbol sequence, $\{I_n\}$. $r_s = 1/T_s$ (dibits/sec.).

$\hat{r}_s$: Reconstructed rate of the symbol sequence, $\{\hat{I}_n\}$. $\hat{r}_s = 1/T_s$(dibits/sec).

CL_p : Clock signal having rate r_s (or r_s).

$\{E_n\} \triangleq \{E_{in}E_{on}\}$: 4-level symbol sequence, output of the gray coded differential encoder circuit.

$\{\tilde{R}_n\} \triangleq \{\tilde{R}_{in}\tilde{R}_{on}\}$: 4 level symbol sequence; clocked symbol sequence, $\{\tilde{R}_n\}$.

$\{P_n\} \triangleq \{R_{n-1}\}$: 4 level symbol sequence; single symbol time (T_s) delayed version of the sequence, $\{R_n\}$.

I. INTRODUCTION

Quadriphase modems, having theoretical 2 bits/sec/Hz spectral efficiency are used in system application were 1 b/s Hz theoretical spectral efficiency of binary phase shift keyed (BPSK) systems are not sufficient, for a given bandwidth. However, the price paid for using such a bandwidth efficient system, is to increase the signal to noise ratio (SNR) for a given probability of error, and increased circuit copmlexity. Figure -1, being the general structure of a quadriphase modem, can be used to obtain the block diagrams of various quadriphase modulation schemes by apropriately deleting some modules. The most known types of quadriphase modems can be listed as:

Quadrature phase shift keyed (QPSK) modem : QPSK modem is the minumum structure quadriphase modem. Its block diagram is obtained by deleting the differential encoder and quadrature (Q) arm delay element in the modulator; and the differential decoder and inphase (I) arm delay element in the modulator, of figure-1. However, this modem suffers from phase ambiguity at the receiver, and, when the modulator output is filtered, the modulated signal has large time domain amplitude fluctuations (theoretically infinite dB) as the phases of the I and Q arms change simultaneously.

Offset keyed QPSK (OKQPSK) modem : Deleting the differential encoder

and decoder pair of figure-1, we obtain the OKQPSK modem block diagram. Offseting one arm with respect to the other by an amount equal to incoming serial bit duration , ,Tb, is used to solve the dramatic envelope variation of the filtered QPSK modulated signal. The phase transitions at the I and Q arms of the filtered OKQPSK modulated signal are not instantaneous as in filtered QPSK modulated signal. However the phase transitions can not occur simultaneously ,so, only one channel envelope amplitude can be momentarily zero at a time, limiting the envelope variation of the filtered QKQPSK modulated signal to atmost 3 dB.

Differential QPSK (DQPSK) and Differentially encoded QPSK (DEQPSK) modems: The DEQPSK is a coherent detection scheme while DQPSK in not. The former is totally a different story and is skipped. |1,2,3|. DEQPSK modem structure is obtained by deleting the offset delay elements only, and differential encoder-decoder pair is left to solve the phase ambiguity problem of the QPSK modem, at the cost of (3dB) error performance.

Differentially encoded, offset keyed QPSK (DEOKQPSK) modem : DEOKQPSK modem has the most complete structure, with the block diagram shown in figure-1, and solves the two problems of the QPSK modem. Infact, the differential encoder-decoder pair happenes to be simpler than DEQPSK's one |2|

We have started the DEQPSK modem realization as a first step ,so, the following chapters will deal with this structure only. However some topics of chapter-2 will deal with QPSK signal, rather than DEQPSK signal, to get some reasonable results concerning the operations of the related blocks. To clarify the reason, suppose that, the sequence of information symbols, $\{I_n\}$, is wide sense stationary (wss) and information symbols are mutually uncorrelated. If this sequence is applied to a differential encoder, the output sequence, $\{E_n\}$,

turns out to be Markov sequence with correlated symbols ; and the over all system has a first order memory. When the above properties of the differential encoder do not let the problem to yield a simple result, the differential encoder-decoder pair is assumed not exit in the overall system.

In chapter-2 we have explained the operations and internal organizations of the blocks appearing in the system structure; and chapter-3, deals with the realizations and respective problems of those blocks. Appendix-A is prepared in order to get familiar with the analytical structure of the DEQPSK modem and band pass signals in additive white Gaussian noise (AWGN), while appendix-B is organized to clarify the operations of basic system elements and to give design hints.

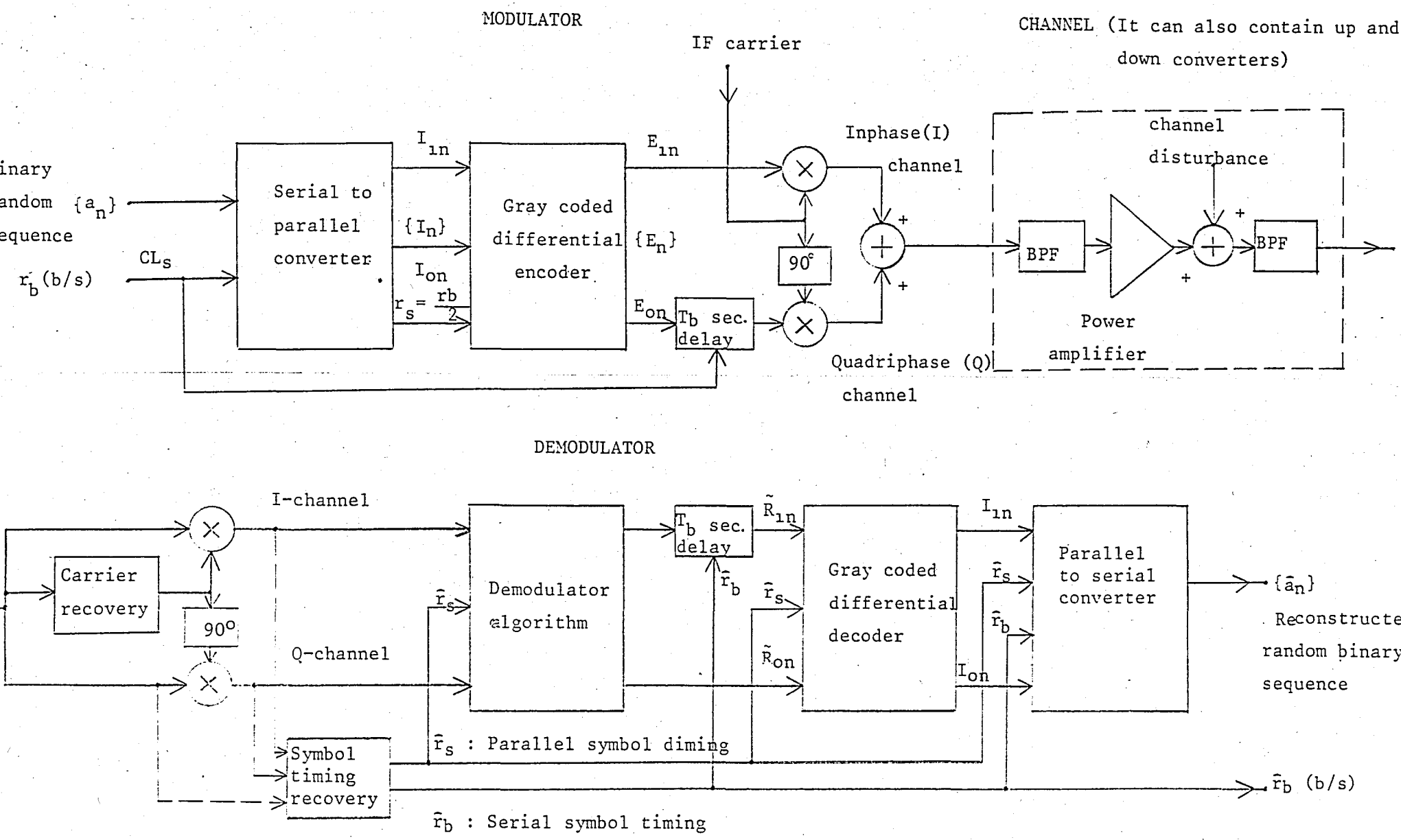
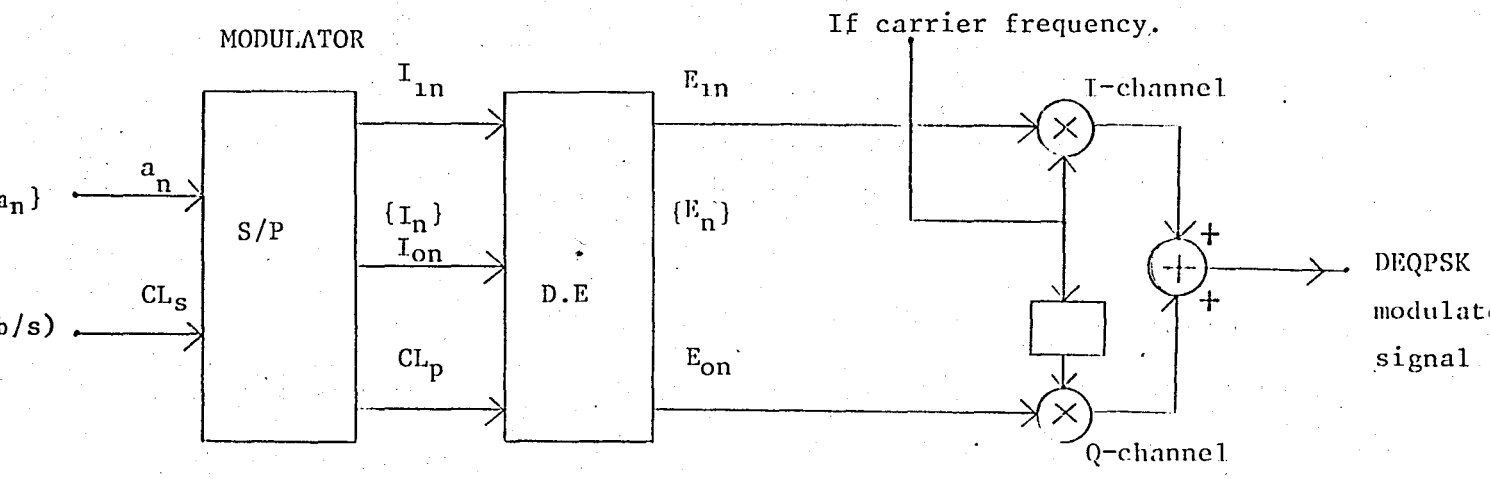


Figure - 1 : General block diagram of a quadriphase modem.

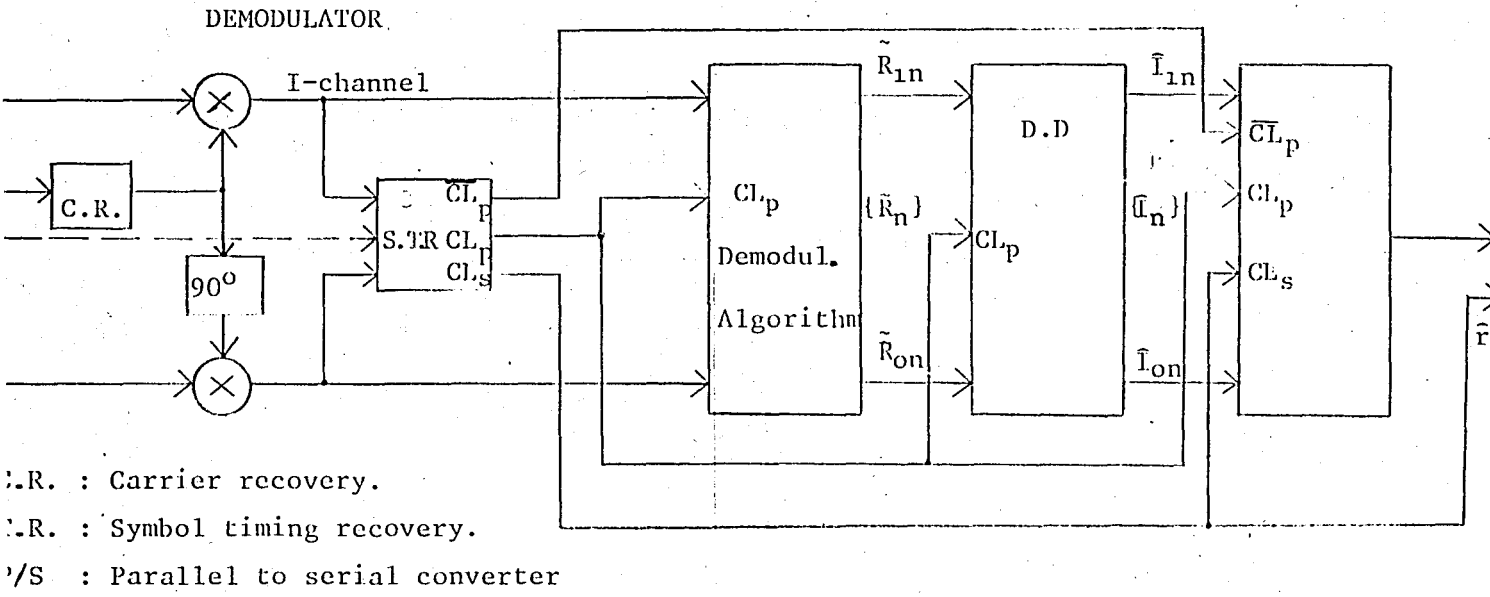
II. DEQPSK THEORY

In this chapter we will review the block of the DEQPSK modem in more detail, then, DEOPSK spectrum and finally its performance.



S/P : Serial to parallel converter

D.E.: Differential encoder



C.R. : Carrier recovery.

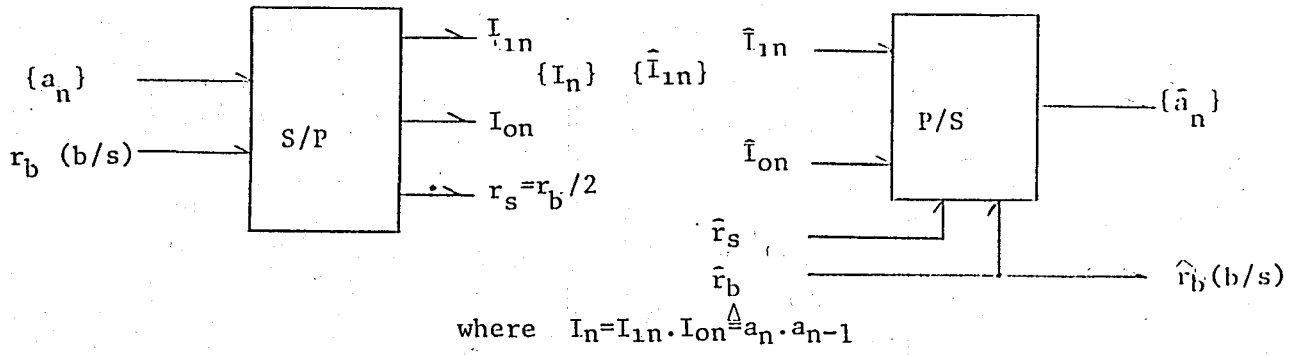
S.R. : Symbol timing recovery.

P/S : Parallel to serial converter

Figure - 2 : DEQPSK modem block diagram.

2-A. STRUCTURE

2-A.1 Serial to parallel converter (s/p) and parallel to serial converter (p/s).

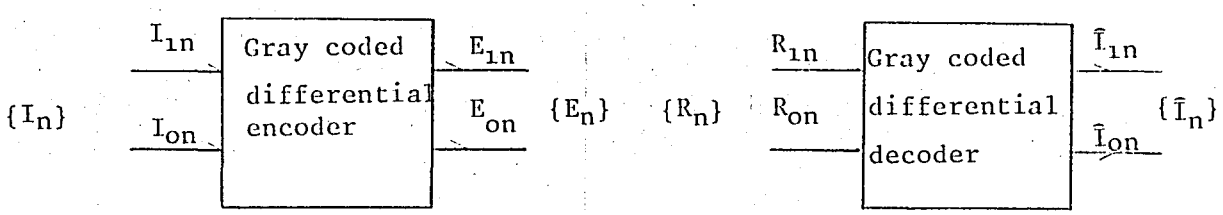


where $I_n = I_{1n} \cdot I_{on} \triangleq a_n \cdot a_{n-1}$

Figure -3 : S/p data flow diagrams.

The binary digits (bits), $\{a_n\}$, from the random binary sequence generator, having the bit rate rb, are mapped uniquely into four dibits (composed of two adjacent pairs of bits) to form information symbols $\{I_n\}$, having symbol rate, $r_s = r_b/2$. The parallel to serial converter is just the reverse of that operation and both circuits have been explained in chapter-3.

2-A.2 Gray Caded differential encoder and decoder.



where $I_n = I_{1n} \cdot I_{on}$

$E_n = E_{1n} \cdot E_{on}$

where $R_n = R_{1n} \cdot R_{on}$

$\hat{I}_n = \hat{I}_{1n} \cdot \hat{I}_{on}$

Figure-4: Gray coded differential encoder and decoder data flow diagrams.

When the absolute phase of the modulator is transmitted as the source information, carrier recovery circuit (such as quadrupter) usually can not extract the correct reference phase, causing phase ambiguity at the demodulator. To overcome this problem differential encoder reassignes the phase transitions as the source information. Denoting four input symbols and four output symbols as

$$I_{no} = \overline{I}_{in} \cdot \overline{I}_{on} = 00 \qquad I_{n2} = I_{in}\,\overline{I}_{on} = 10$$

$$I_{n1} = \overline{I}_{in} I_{on} = 01 \qquad I_{n3} = I_{in}\, I_{on} = 11$$

$$E_{no} = \overline{E}_{in}\,\overline{E}_{on} \qquad E_{n2} = E_{in}\,\overline{E}_{on}$$

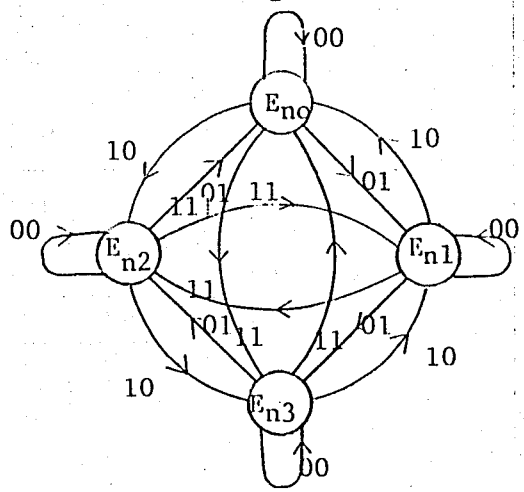
$$E_{n1} = \overline{E}_{in} \cdot E_{on} \qquad E_{n3} = E_{in}\, E_{on}$$

and using the gray coding property (adjacent symbols differ in only one bit) for the output sequence, $\{E_n\}$, we get the assignment rule for the gray coded differential encoder as follows*

- If input symbol is 00, then make no phase jump, transmit the same phase,
- If input symbol is 01, then make a 90^{o} phase jump,
- If input symbol is 11, then make a 180^{o} phase jump,
- If input symbol is 10, then make a 270^{o} phase jump

* *This assignment rule is not unique. Since there are four different input symbols, I_n, there are also $\frac{4\ !}{(4-4)\ !} = 24$ different assignment rules.*

Hence the state diagram and state table is given as



Symbol	Description
0	0 to 1 transition
α	0 to 1 transition
β	1 to 0 transition
1	1 to 1 transition

Input	Present state	Next state	Behavior	Short cut method
$I_{1n}I_{on}$	$E_{1n}E_{on}$	E^{+}_{1n} E^{+}_{on}		
0 0	0 0	0 0	0 0	No change
0 0	0 1	0 1	0 1	
0 0	1 0	1 0	1 0	
0 0	1 1	1 1	1 1	
0 1	0 0	0 1	0 α	Count by 1 in gray sequence
0 1	0 1	1 1	α 1	
0 1	1 0	0 0	β 0	
0 1	1 1	1 0	1 β	
1 0	0 0	1 0	α 0	Count by 3 in gray sequence
1 0	0 1	0 0	0 β	
1 0	1 0	1 1	1 α	
1 0	1 1	0 1	β 1	
1 1	0 0	1 1	α α	Count by 2 in gray sequence
1 1	0 1	1 0	α β	
1 1	1 0	0 1	β α	
1 1	1 1	0 0	β β	

$I_{1n}I_{on}$ \ $E_{1n}E_{on}$	00	01	11	10
00	0	0	1	1
01	0	α	1	β
11	α	α	β	β
10	α	0	β	1

$I_{1n}I_{on}$ \ $E_{1n}E_{on}$	00	01	11	10
00	0	1	1	0
01	α	1	β	0
11	α	β	β	α
10	0	β	1	α

Flip-flop excitation table

Behavior	D	J	K
0	0	0	X
α	1	1	X
β	0	X	1
1	1	X	0
X	X	X	X

The J-K flip-flop realization yields (we drop the subcript 'n' for simplicity)

$$J_{E0} = I_o \cdot \overline{E}_1 + I_1 \qquad J_{E1} = I_1 \cdot \overline{E}_o + I_o.E_o$$

$$K_{E0} = I_1 \cdot \overline{E}_1 + I_oE_1 \qquad K_{E1} = I_1 \cdot E_o + I_o.\overline{E}_o$$

D flip-flop realization yields

$$D_{E0} = I_o.\overline{E}_1.\overline{E}_o + \overline{I}_o.E_1.E_o + I_1.E_1.\overline{E}_o + \overline{I}_1.\overline{E}_1.E_o$$

$$D_{E1} = I_o.\overline{E}_1.E_o + \overline{I}_o.E_1.\overline{E}_o + I_1.\overline{E}_1.\overline{E}_o + \overline{I}_1.E_1.E_o$$

The differential encoder does just the reverse operation. But if we assume that present received information symbol, $R_n = \{R_{1n}.R_{on}\}$, and the previous one, $R_{n-1} = \{R_{1(n-1)}.R_{o(n-1)}\}$, are available at the input of the decoder, it is no more a sequential but a combinational logic. So with the help of gray coded differential encoding rules, we get the gray coded differential decoding rules as follows

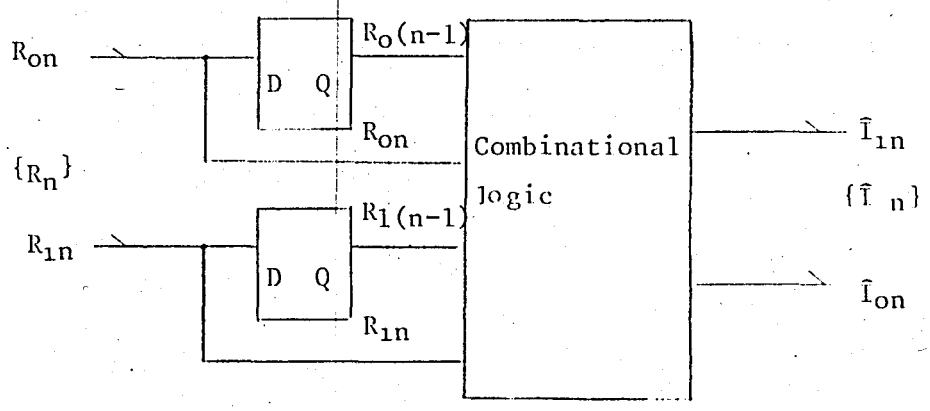
- If the previous symbol and the present symbol are equal, then assign 00 to the output pair,
- If the previous symbol and the present symbol make a gray count by 1, then assign 01 to the oupput pair,
- If the previous symbol and the present symbol make a gray count by 2, then assign 11 to the output pair,
- If the previous symbol and the present symbol make a gray count by 3, then assign 10 to the output pair.

Dropping the subscript n, and defining the previous symbol and received symbol as $R_{n-1} \triangleq P$, $R_n = R$; we get the truth table and output expression given as

$\overline{I}_{on}$ R_1R_o	P_1P_o 00	01	11	10
	0	0	1	1
	1	0	0	1
	1	1	0	0
	0	1	1	0

$\overline{I}_{on}$ R_1R_o	P_1P_o 00	01	11	10
	0	1	1	0
	0	0	1	1
	1	0	0	1
	1	1	0	0

Present symbol		Previous symbol		output symbol	
R_{1n}	R_{on}	$R_{1(n-1)}$	$R_{o(n-1)}$	$\hat{I}_{1n}$	$\hat{I}_{on}$
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	0	0



$$\hat{I}_{on} = R_o\overline{P}_1\overline{P}_o + \overline{R}_oP_1P_o + R_1\overline{P}_1P_o + \overline{R}_1P_1\overline{P}_o$$

$$\hat{I}_{1n} = R_oP_1\overline{P}_o + \overline{R}_o\overline{P}_1P_o + R_1\overline{P}_1\overline{P}_o + \overline{R}_1P_1P_o$$

It is certain that in the case of noise free environment $\{ \hat{I}_n \}$ should equal to $\{ I_n \}$, and this is checked analytically.

2 - A.3. Multiplier, 90° phase shift circuit, IF amplifier, power summer and spilitter networks.

The analog multiplier must have wide bandwidth (ideally, minimum 70 MHz) at the IF frequency (140 MHz) with as little as possible PM-AM conversion. The balanced mixer has extremely wide bandwidth compared with monolithic integrated circuit multipliers, however, due to unbalance, it may have pure isolation amoung its ports. With proper choise of signal levels, the mixer feedthrough and high order intermodulation products are minimized. The biphase modulator used at the modulator side, is nothing but a balanced mixer except for improved amplitude and phase match between the two states. (For technical data refer to I.C. specifications section.)

This modem is designed to be an IF stage, so, in the operating system modulator and demodulator are connected with an IF amplifier only, there is no RF stage in between them. The amplifier is left to Chapter-3, and the rest of this section can be found from the related appendices.

2 - A.4. Carrier Recovery (CR).

It is certain that the heart of the coherent demodulator is the carrier synchronization and this subject has been extensively analyzed in the literature. To proceed with the investigation of various CR schemes, the target value of rms phase jitter (var $\sqrt{\phi}$) or the tolerated circuit complexity has to be known priori. The rms phase jitter depends severely on the bandwidth efficiency of the modulation scheme, and can be found either graphically (P_e versus rms phase jitter), or analytically from the previous works. The types of carrier recovery schemes can be listed as follows.

1. Maximum a posteriori probability (MAP) and maximum likelihood (ML) estimators of carrier phase. |2,17|
2. Costas loop of carrier phase recovery |1,2,15,16|
3. Demod-remod carried phase recovery. |2,18,19|
4. Joint recovery of carrier phase and symbol timing recovery. |2|
5. nth order power law carrier phase recovery |1,2|
6. Decision feedback PLL. |1|.

Maximum likelihood estimator is employed when the estimated parameter (carrier phase) is unknown but not random. However, if estimated parameter is a random variable MAP estimator comes into use, and in this case when the random parameter (carrier phase) has a uniform distribution, ML and MAP estimators are equivalent. |2|. In the MAP estimator strategy the observation of the incoming PSK signal, s(t), corrupted by additive channel noise, n(t) (narrowband bandpass process), on the interval $[0,T_s]$ with the pre-knowledge of signal pulse shape (p(t)), carrier frequency and precise symbol timing, are

used to estimate the carrier phase, $\theta(t)=\theta$ (assumed constant in the interval $[0,T_s]$), which maximizes the conditional probability $p(\theta(t) \mid s(t) + n(t))$. (Figure-5). However it leads to closed loop implementation with active arm filters, mached to the signal pulse shape, p(t), and requires the symbol synchronization pulses to drive the matched filter, all of which make this strategy difficult to implement.

When the active arm filters are replaced by passive low pass filters, accumulator by analog loop filter, bumped phase oscillator by voltage controlled oscillator (VCO) and hyperbolic tangent (tanh) nonlinearity by

$$\tanh X \cong \begin{cases} X & X<<1 \text{ : low SNR approximation} \\ \operatorname{sgn} X & X>>1 \text{ : high SNR approximation} \end{cases}$$

then, one obtains the conventional Costas loop and polarity type Costas loop respectively. |17|. (Figures-7.8) In this case, for a given rate and SNR one can find the optimum filter bandwidth in the sense of minimizing the square rms phase jitter, even, when the symbol synchronization is known, an integrate and dump filter placed on the arms, can still improve the carrier to noise ratio about 4-6 dB depending on data rate. |15| On the otherhand conventional quadriphase Costas loop (Figure -6) and small SNR practical realization of MAP estimator loop (figure -11) are equivalent stochastically. |17| So we conclude that conventional quadriphase Costas loop and its previously shown equivalent |17|, the fourth power loop (figure-9), are low SNR practical realizations of the MAP estimate loop, for QPSK.

The demod-remod tracking loop, joint recovery of carrier phase and

signal timing, and decision feedback PLL are left to references listed previously.

The fourt power loop, when excited by QPSK signal, has the phase error variance (square phase jitter) of [2] :

$$\mathrm{Var}\phi = B.T_s \cdot \left[0.1125 + 1.4625 \frac{1}{\gamma_b} + 24.469 \frac{1}{\gamma_b^2} + 21094 \frac{1}{\gamma_b^3} + 2.531 \frac{1}{\gamma_b^4} \right]$$

B = nosie equivalent bandwidth of the bandpass filter (or PLL) located at 4 time IF carrier frequency (f_{IF}) : (in Hz)

T_s = symbol duration

N_o = double sided noise spectral density at the input of the CR loop.

$\gamma_b = \frac{A^2 T_s}{2N_o}$ = QPSK signal, SNR : (see Chapter -2.B.)

Where it is assumed that Nyquist base band pulse shaping is used, $p(t) = A \operatorname{sinc}(t/T_s)$, and $B \ll \frac{1}{T_s}$. Clearly the steady state rms phase jitter can be made as small as possible, by reducing the loop bandwidth, almost independently from the SNR. However small bandwidth means; inability to track instabilites in the transmitted carrier, prolonged acquisition time for phase recovery, and in the case of passive band pass filter, unsymetry of band pass filter due to mistuning, which degrades the performance of the CR circuit.

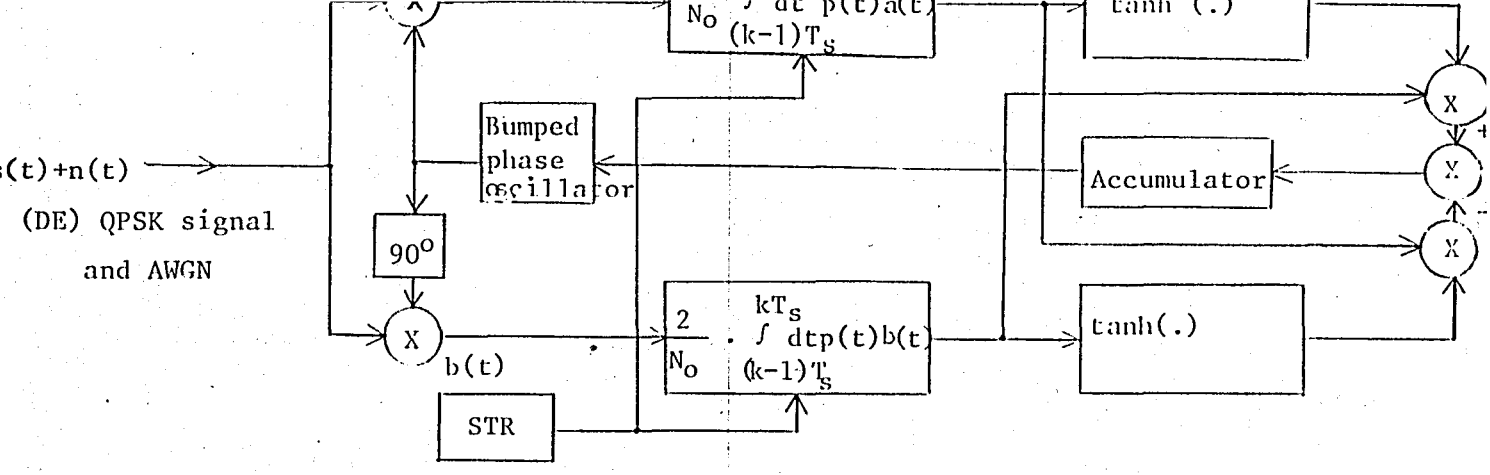


Fig -5 : MAP estimation loop for carrier phase (QPSK)

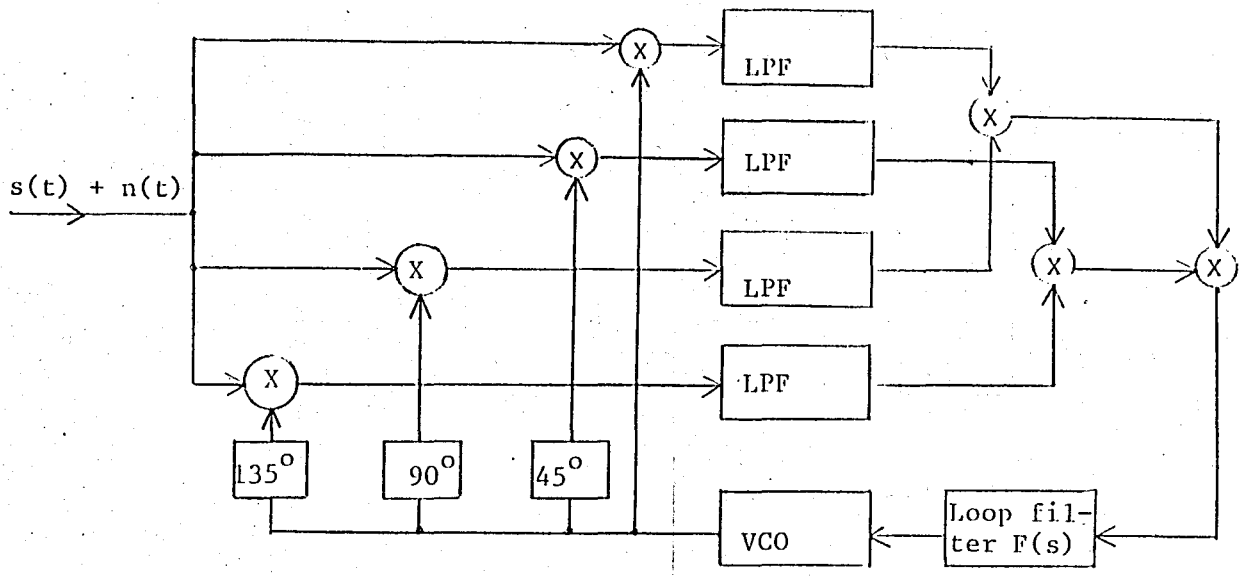


Fig-6 : Conventional quadriphase Costas loop (QPSK)

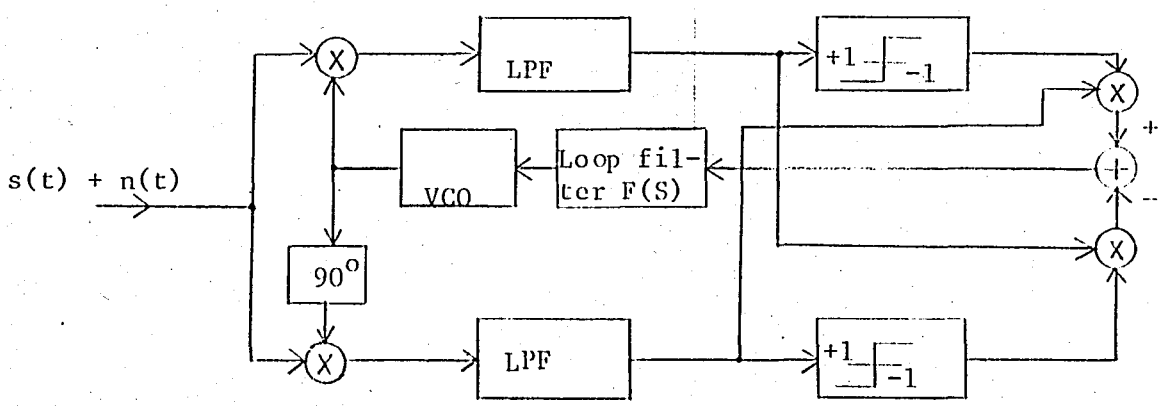


Fig -7 ; Large SNR practical realization of MAP estimator loop with passive arm filters (QPSK)

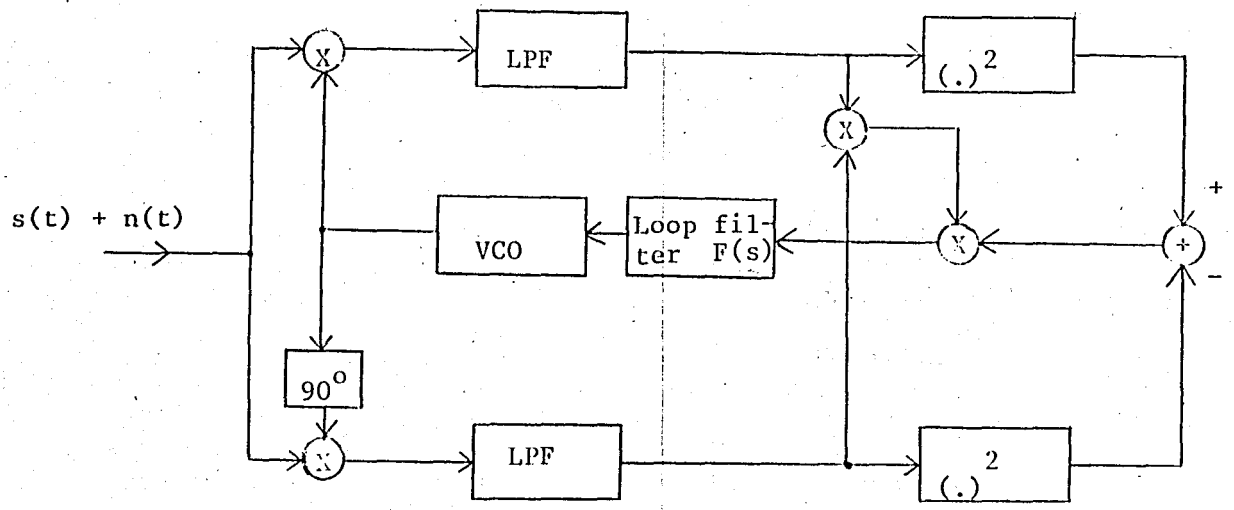


Fig - 8 : Small SNR practical realization of MAP estimator loop with passive arm filters (QPSK)

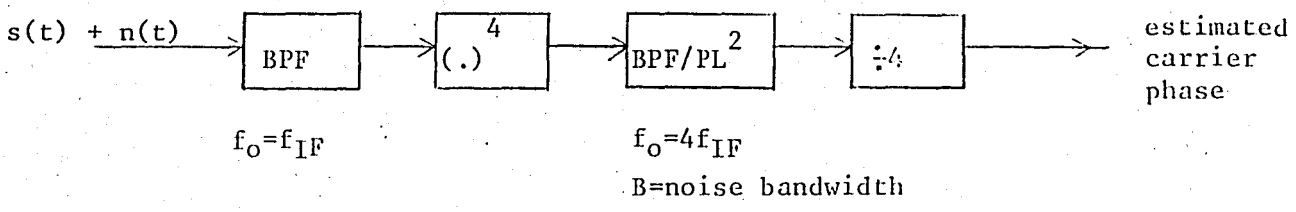


Fig - 9 : Fourth power law carrier phase recovery (QPSK)

2 - A.5 Symbol timing recovery (STR)

The symbol timing extraction, for QPSK signal, can be done basically in two ways, directly on the QPSK modulated signal, parallel symbol timing recovery (PSTR); |13| , or at the baseband, serial symbol timing recovery (SSTR): |14|. But both STR techniques employ nonlinear signal processing elements analog (balanced mixer) or discrete (exclusive-OR gate) type, which generate the discrete prectral components at the multiples of symbol rate, r_s. The nonlinear element may be implemented by a differentiator, a full wave rectifier, a threshold crossing circuit, a half bit delay detector, a squarer, a fourth power circuit, exclusive-OR gate, a delay and multiply circuit. However the last two are superior over the rest, in the performance, complexity and cost |14|.

The delay and multiply PSTR scheme is faster in aquisition and when the delay element is perfectly calibrated, has 3dB higher performance compared to exclusive -OR gate SSTR scheme, however the former is more simpler to implement.

Exclusive -OR gate SSTR

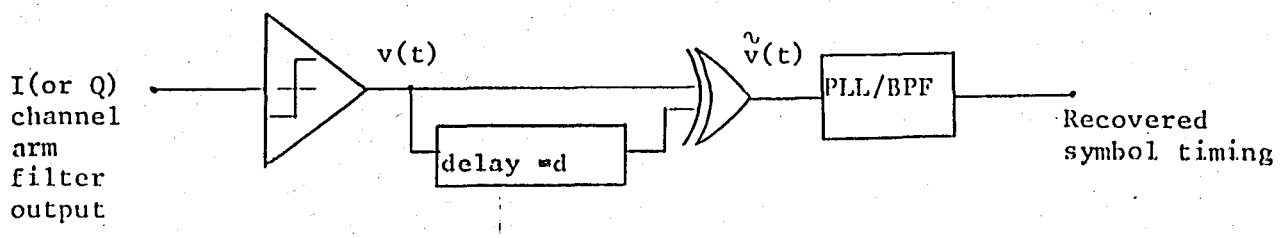


Figure -10 : Exclusive -OR gate SSTR.

The symbol timing clock is recovered from either channel arm filter output* of the demodulator, which contains filtered, non-retun-zero (NRZ) binary random sequence, corrupted by channel noise. We assume that this

equence is WSS, having mutually uncorrelated equiprobable symbols. The output of the hard limiter resembles a return-zero (RZ) random binary sequence, but it contains transition jitter, due to channel noise and intersymbol-interference (ISI), caused by arm filter. However an experimental evidence is given by the author [14] that, the undesired power of $v(t)$, due to transition jitter, is negligible as compared to that of RZ continuous spectral components close to symbol rate frequency. So the jitter free power spectral density of the signal, at the output of hard limiter, having states $(0,A)$ is given from appendix. A-4 as:

$$G_{vv}(f) = \frac{A^2}{4} \cdot T_s \operatorname{sinc}^2 fT_s + \frac{A^2}{4} \cdot u_o(f)$$

Where T_s is the symbol duration, as before, and $u_o(f)$ is the unit impulse function. It is clear that $G_{vv}(f)$ has no spectral components at the symbol rate frequency. The power spectral density at the output of exclusive-OR gate is given as [14].

$$G_{\tilde{v}\tilde{v}}(f) = \frac{2A^2 d^2}{T_s} \operatorname{sinc}^2(f.d) + \frac{A^2.d^2}{T_s^2} \left[u_o(f) + 2 \sum_{1}^{\infty} \operatorname{sinc}^2 \left(\frac{md}{T_s}\right) \cdot u_o\left(f - \frac{m}{T_s}\right) \right]$$

$$= C(f) + D(f)$$

where 'A' is the output high level of the hand limiter, as defined above and

* *It is advisable to employ both arms (I,Q) of the demodulator to extract the symbol timing. This is accomplished simply, by performing the operation of figure -10 (up to the band-pass filter) on both arms, independently and then (wire OR'ing the two paths before they enter to the band pass filter.*

'd' is shown in Figure -10 It is obvious that it does contain line spectra, D(f), at the multiples of symbol rate frequency, $\frac{1}{T_s}$.

The value which determines the best operating point, is the ratio of discrete to residual continuous spectral power (defined as SNR), since it is this ratio which causes clock timing jitter at the output of the bandpass filter. If the bandpass filter is narrow enough ($B \ll 1/T_s$), the continuous spectrum of the signal within that bandwidth can be assumed flat, so the continuous spectral power at the output of the bandpass filter is :

$$C(1/T_s) = B. \frac{2A^2 d^2}{T_s} . \text{sinc}^2 (d/T_s)$$

and the line spectral at the symbol rate frequency is :

$$D(1/T_s) = \frac{2A^2 d^2}{T_s^2} . \text{sinc}^2 (d/T_s)$$

Therefore the signal to noise ratio, as defined previously, is :

$$(SNR) \triangleq \frac{D(1/T_s)}{C(1/T_s)} = \frac{1}{B.T_s} = \frac{f_o}{B} = Q$$

Where Q and f_o are the quality factor and center frequency of the bandpass filter, respectively.

From the last equation, we conclude that, the delay element, having delay d, $0 < d < T_s$, has no effect on the performance, and high Q filter can reduce the clock timing jitter, at the expense of prolanged acquisition

time and inability to track the instabilities of the transmitted clock timing signal.

REMARK :

When bandpass filter is implemented by PLL with phase frequency detector, the phase frequency detector is misdirected by the random signal where some transitions are missing. (see timing diagram of Chapter -3.7.) The LC pre-filter with high Q can introduce many transitions, of almost correct phase, each time it is driven by the data transitions of different phase, hence, improves the operation of phase detector.

2 - A.6 Demodulator

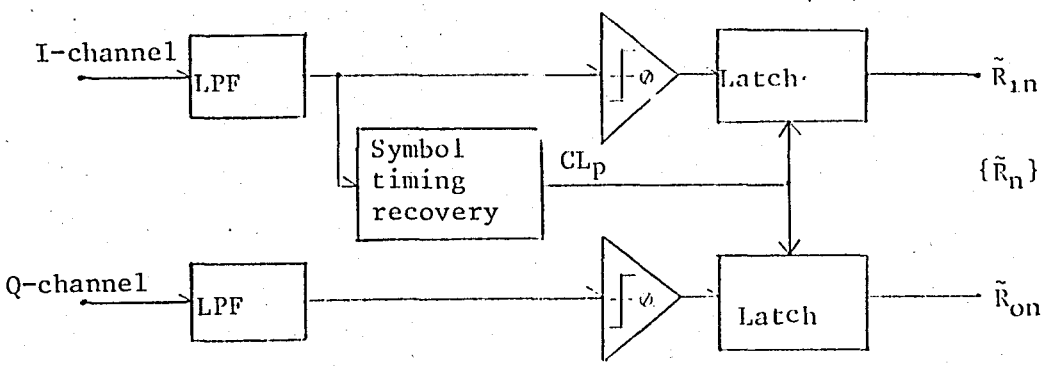


Figure -11 : Demodulator structure.

Demodulation is performed by passive lowpass filters (2 nd order Burtterworth) followed by zero voltage threshold comparators and latches, driven by STR module; due to high data rate and zero mean bipolar input signals. The disadvantage of passive lowpass filter is that, it introduces ISI, if it doesn't have sufficient bandwidth, however large bandwidth means

more noise power injected at the entry of the decision circuit.

The error performance degradation due to the passive filter and filter caused ISI becomes very complex even for the simple RC filter case*, and this subject is not analyzed, but filter bandwidth is chosen equal to symbol data rate. |3|

2 - B. SPECTRUM and SPECTRAL EFFICIENCY

In appendix A.4 the spectral characteristics of digitially modulated signals (when the information source is WSS) are given. If we also assume that, rectangular baseband pulse shaping is employed and complex symbols are mutually uncorrelated having zero mean, $m_I = 0$, and unity variance, $\sigma_I^2 = 1$, we get

$$p(t) = \begin{cases} A & 0 \leq t \leq T_s \\ 0 & \text{else} \end{cases}$$

$$|P(f)|^2 = A^2.T_s^2.\ \text{sinc}^2(f.T_s)$$

So, equivalent lowpass power spectral density of the quadriphase modulated signal is :

$$G_{uu}(f) = \frac{\sigma_I^2}{T_s}\ .\ |P(f)|^2 + \frac{|m_I|^2}{T_s^2}\ |P(0)|^2.\ u_o(f) = A^2.T_s\ \text{sinc}^2(f.T_s)$$

* *H. Stark and F.Z. Tuteur, "Modern Electrical Communications," Prentice-Hall,1979.*

and the modulated power density spectrum :

$$G_{ss}(f) = \frac{1}{2} \left[G_{uu}(f-f_c) + G_{uu}(-f-f_c) \right]$$

On the other hand, the well known ISI free theoretical minumum bandwidth (Nyquist bandwidth) of a baseband information sequence, having a rate, r_s is:

$$B_{min} \geq r_s/2$$

where equality holds with a very special pulse shape, sinc pulse. However when the signal is double sideband modulated, it occupies the twice bandwidth at the RF channel, calling this bandwidth transmission bandwidth, B_T, we get :

$$B_T = 2B_{min} \geq r_s = \frac{r_b}{2}$$

So the bandwidth efficiency, BWEFF, is :

$$BWEFF = \frac{r_b}{B_T} \leq 2 \text{ bits/sec/Hz.}$$

Again equalitity holds only for sinc baseband pulse shaping and it is an upper bound. When α roll of risedcosine pulse shaping is used, we get

$$B_T = (1+\alpha)\ r_s$$

$$BWEFF = \frac{2}{1+\alpha} \text{ b/s/Hz}$$

as a typical achivable efficiency. ($\alpha \neq 0$)

2 - C. ERROR PERFORMANCE

The direct error performance calculation of DEQPSK modem is very complex |1,pp.161,164|, |2,pp.155|, and it is usually given graphically due to non-elementary functions. However binary phase shift keyed (BPSK) modem performance is extensively analyzed and can be adopted to DEQPSK case, giving considerable design insight.

IF the BPSK signal is corrupted by additive white Gaussian noise (AWGN) and demodulated by a matched filter receiver (or its error performance equivalent Nyquist channel receiver), the bit error probability of this system |1,2| becomes

$$P_b = \frac{1}{2} \operatorname{erfc} \sqrt{\gamma_b}$$

where $\gamma_b = \frac{\varepsilon}{N_o}$ = received SNR per bit,

ε = Received energy in a single bit time,

N_o = Double sided noise spectral density,

erfc(X) = complementary error function.

If the BPSK signal has a rectangular baseband pulse shaping, and has a peak amplitude of 'A' at the input of receiver, from appendix-A.1 we have;

$$u(t) = \begin{cases} A & 0 \le t \le Tb \\ 0 & \end{cases}$$

$$\varepsilon = \frac{A^2 \, Tb}{2}$$

When there exists neither crosstalk nor interference between the signals on the I and Q arms of the QPSK demodulator (perfect coherent demodulation), the bit error probability of this modem is identical to bit error probability of BPSK modem [1]

$$P_{b,QPSK} = \frac{1}{2} \operatorname{erfc} \sqrt{\gamma_b}$$

Since the differential decoding is performed after the signal regeneration, error multiplication by a factor of two can occur during decoding. So ideally we have :

$$P_{b,DEQPSK} = \operatorname{erfc} \sqrt{\gamma_b}$$

III. HARDWARE AND HARDWARE DESCRIPTION OF THE SYSTEM

This section includes the circuit realizations and their operational descriptions of the blocks described in chapter -2; and some recommendations concerned with the operations and calibrations of those circuits. However, before proceeding to this chapter, we have some remarks to bear in mind.

First, the analog parts of the system were designed and calibrated (such as 50 Ω matched transistor RF amplifier) with the help HP.'s RF equipment set. So, the RF techniques used, for both analog |4,5| and digital |6| circuits, have not mensioned in this thesis.

Second, the system is realized in a modular way, enabling the operation of each module to be tested independently. However, this modular structure has introduced some redundancy for some digital circuits. So, in this chapter, we introduced and described two networks, (only for those reduntant circuits) one being the implemented circuit, and the other, called basic circuit, being the recommended circuit if modulator and demodulator had been conctructed on single cards, respectively.

3.1- SERIAL TO PARALLEL CONVERTER

Basic circuit : The serial input stream is passed through a two bit shift register, and serial clock is divided by two, to form the parallel clock. However, due to finite delay of this divider, shift register outputs have to be delayed appropriately,* before they are latched by output flip-flops, via parallel clock. Assume that, input data stream has a form

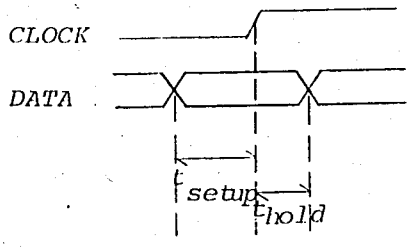
(....., D,C,B,A)

where 'A' is the very first data bit sent, then, the output symbol sequence is formed as

$$\begin{pmatrix} I_1 \\ I_o \end{pmatrix} = \begin{pmatrix} B \\ A \end{pmatrix}, \begin{pmatrix} D \\ C \end{pmatrix} \quad , \ \ldots$$

which will be useful when converting to serial again, at the demodulator.

Implemented circuit : The implemented circuit differs somewhat. First the serial input sequence and the serial clock are buffered; and the shift register pair is clocked with the falling edge of the serial clock. So, Tb/2



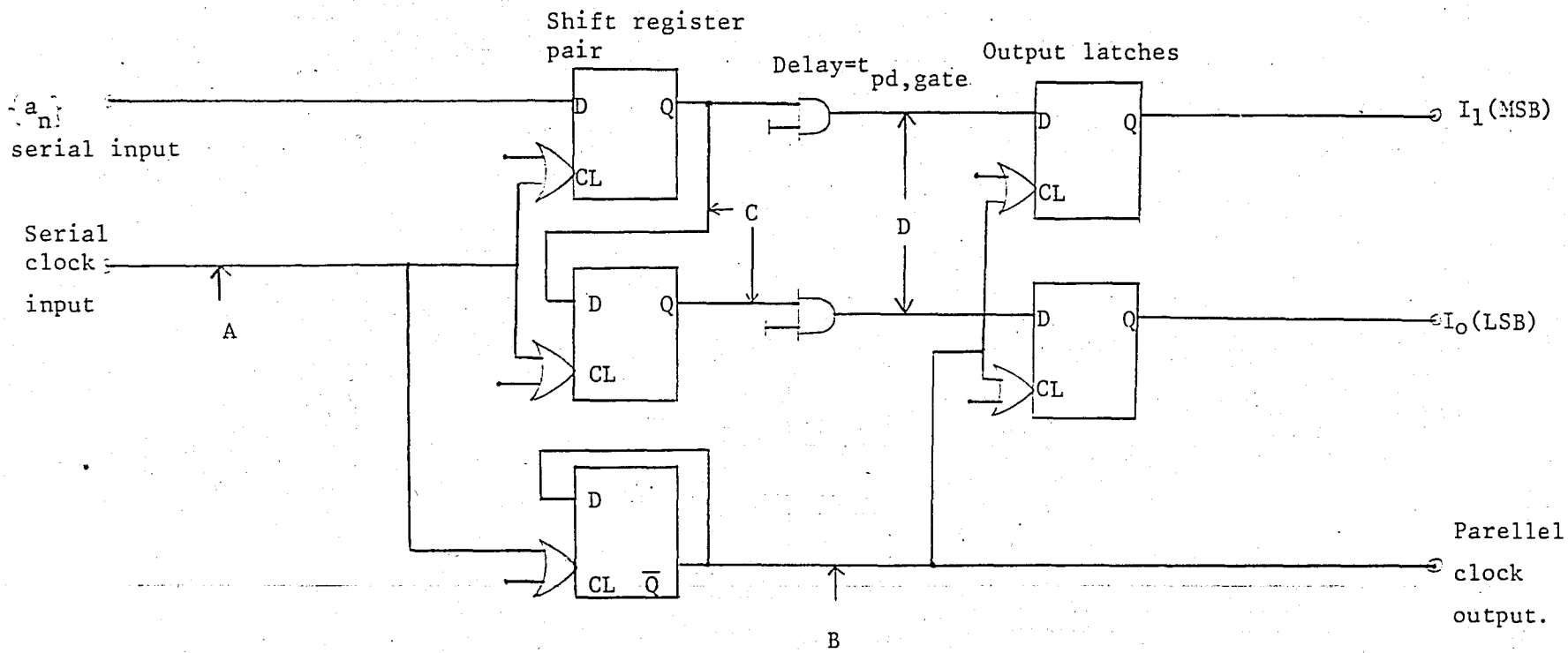
gate delay = t_{pd}

* *10131 ECL D flip-flop requirements :*

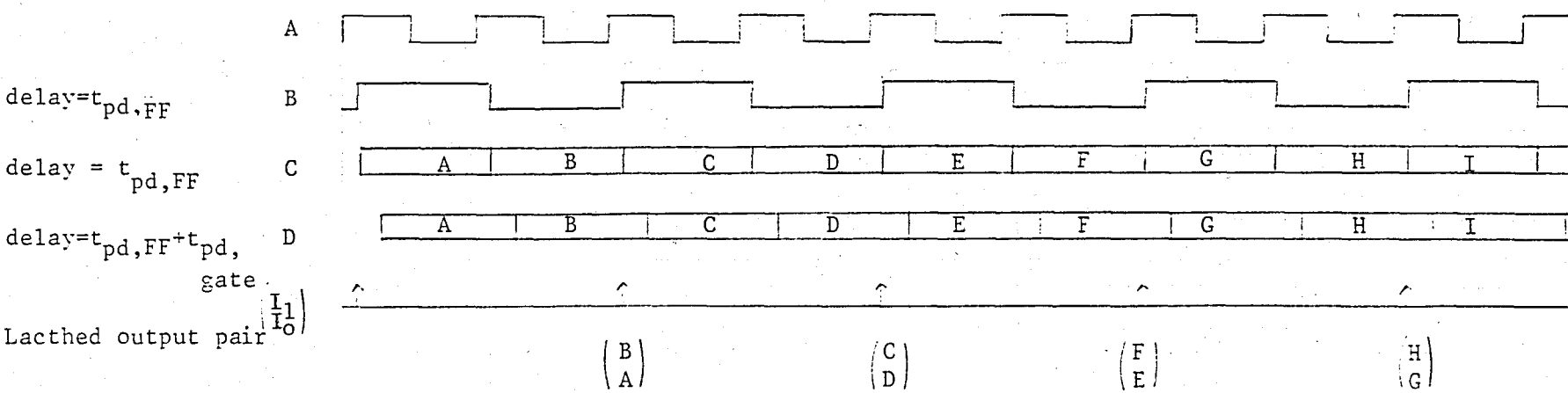
Data should be stable $t_{set,up}$ *(1 ns) seconds before and* t_{hold} *(0.75 ns) seconds after the rising edge of the clock pulse. So, making use of the timing diagram of the basic circuit, we get*

$$t_{pd,gate} > t_{hold,FF}$$

secods delay is generated in between the shift register pair and output lacthes. (See timing diagram.) There is still a third difference, the reset circuit, added for the check of circuit operation during test. The very firsthigh state of data will enable the operation of the serial to parallel converter and acts as a kind of synchronizer. The basic circuit should not include this reset circuit.

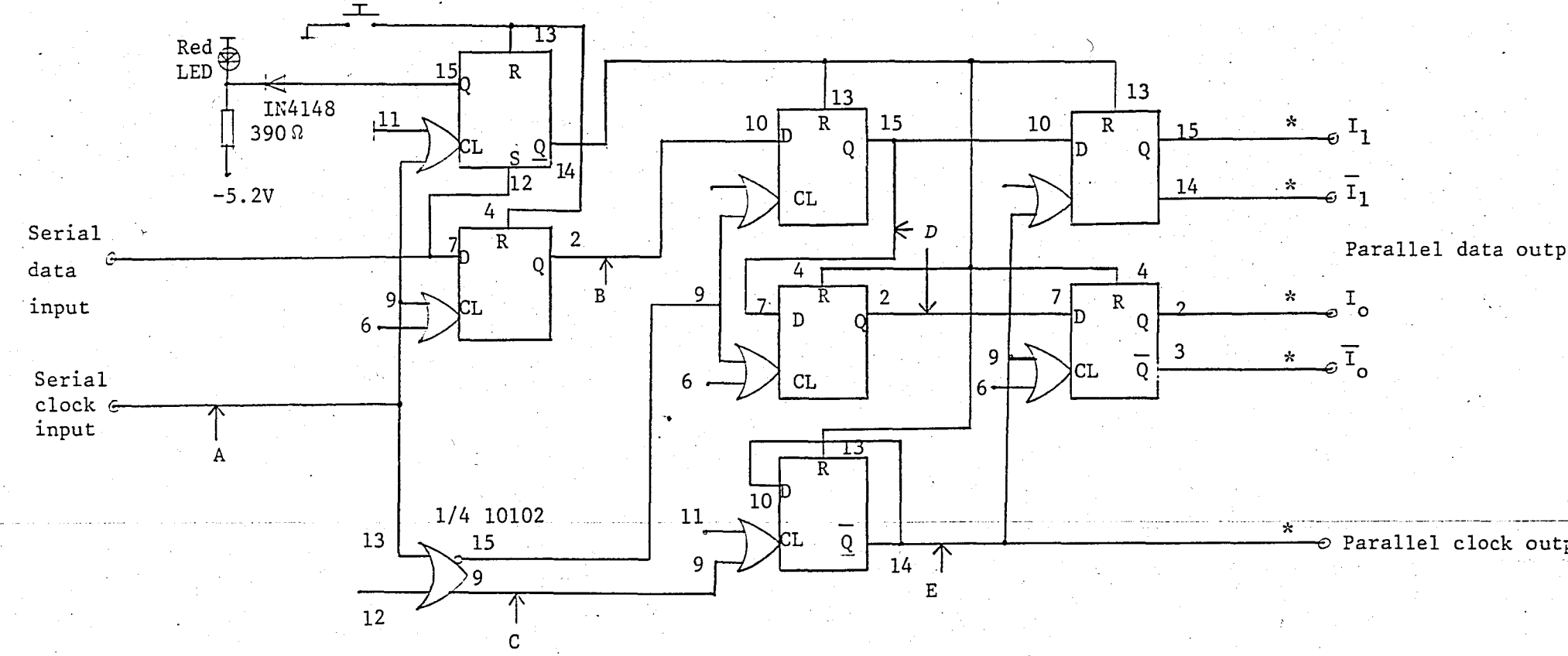


Timing diagram



- SERIAL TO PARALLEL CONVERTER -

(Basic circuit)

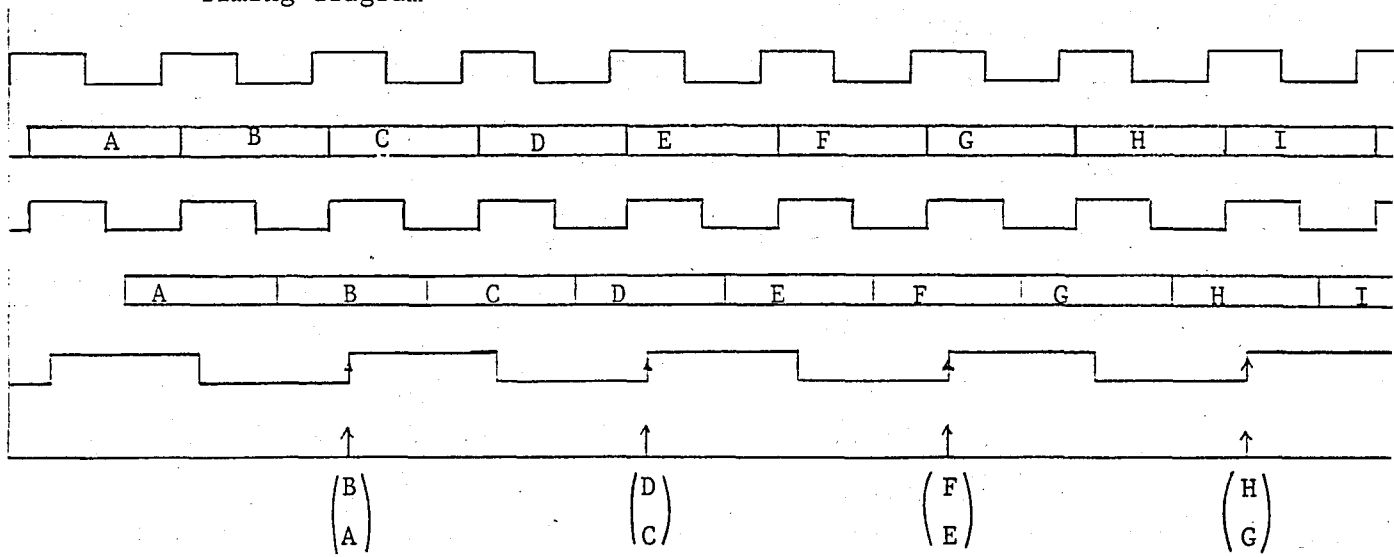


2 D flip-flop=1 10131 ECL IC.

All emitters have 510 ohm bias resistors

* Emitter bias resistors are on the following stage

Timing diagram



- SERIAL TO PARALLEL CONVERTER-
(Implemented circuit.)

3.2 - PARALLEL TO SERIAL CONVERTER.

The basic circuit is very simple in this case. The parallel data outputs ($\bar{I}_1$, $\bar{I}_o$) are sampled and latched by the serial clock, CL_S, twice in a single symbol time, T_S. Each time as the symbol clock (also called parallel clock), CL_S, makes a positive transition, a new symbol appears at the inputs of the parallel to serial converter, and this symbol has a form*

$$\begin{pmatrix} \bar{I}_1 \\ \bar{I}_o \end{pmatrix} = \begin{pmatrix} \bar{B} \\ \bar{A} \end{pmatrix} , \begin{pmatrix} \bar{D} \\ \bar{C} \end{pmatrix} , \ldots$$

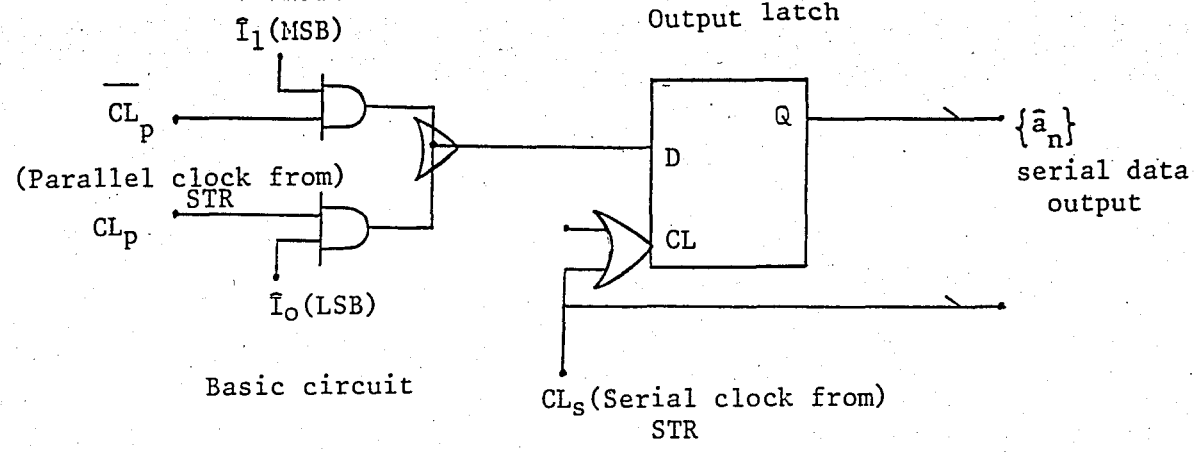
So, at the high state of the parallel clock, least significant bit of the symbol, $\bar{I}_o$, is enabled and latched first, then, at the low state, most significant bit, $\bar{I}_1$, is enabled and latched. Therefore, the output sequence is reconstructed as the original one, as

$$(\ldots . \bar{D},\bar{C},\bar{B},\bar{A})$$

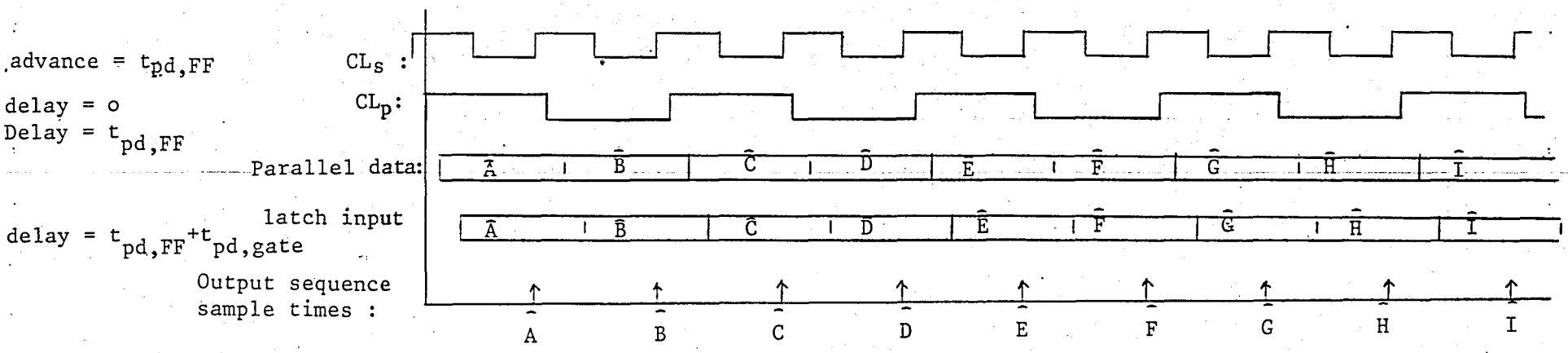
In the implemented circuit, the divide by two flip-flop, just after the VCO of the STR card, is also copied in this card, which is in the same phase as the original one, and rest is totally the same.

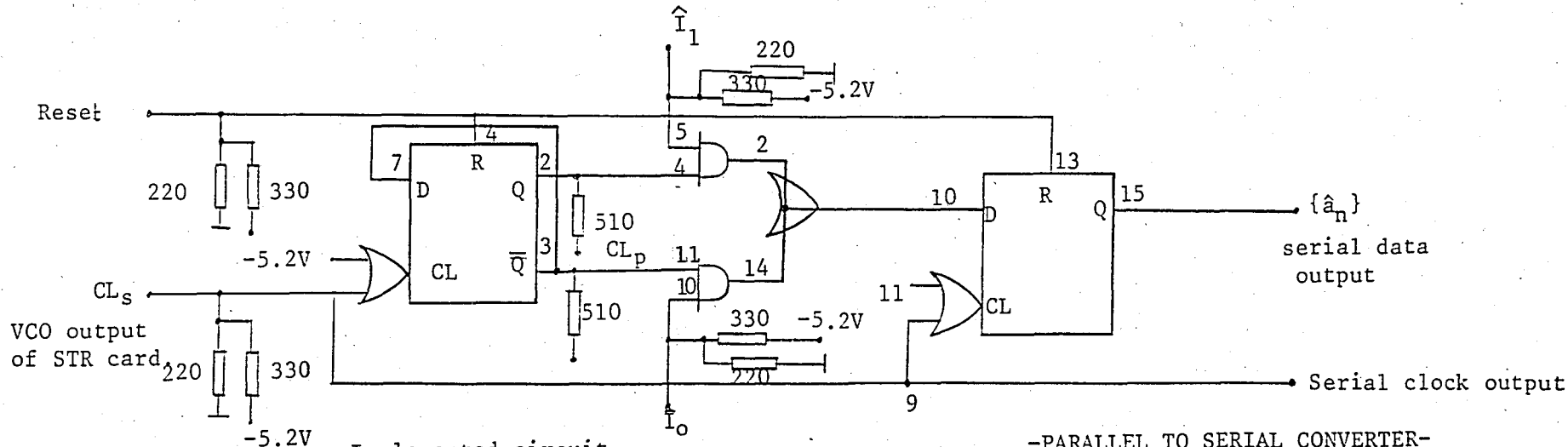
** See serial to parallel converter section (3-1.).*

Not : All resistor values are in ohm, unless otherwise specified.



Timing diagram.





Implemented circuit.

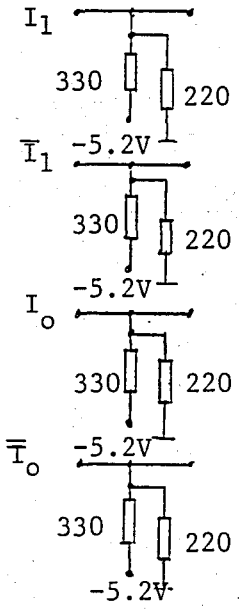
-PARALLEL TO SERIAL CONVERTER-

3.3 - GRAY CODED DIFFERENTIAL ENCODER AND DECODER

Refering to differential decoder circuit, the symbol sequence, $\{\tilde{R}_1\tilde{R}_o\}$, being the outputs of the decision circuits, has not a proper form to operate the differential decoder circuit, since it has state transitions just on the middle of succesive falling edges of the symbol clock, CL_p^*. The first D flip-flops convert this sequence into a proper form, $\{R_1\ R_o\}$, and the second D flip-flops serve as delay elements. The rest of this circuit and the differential encoder circuit perform the respective Boolen function operations, as described in chapter -2.

However, due to simplicity, it is advisable to use J-K flip-flop realization in the encoder circuit.

* *See also chapters 3-6, and 3-7.*

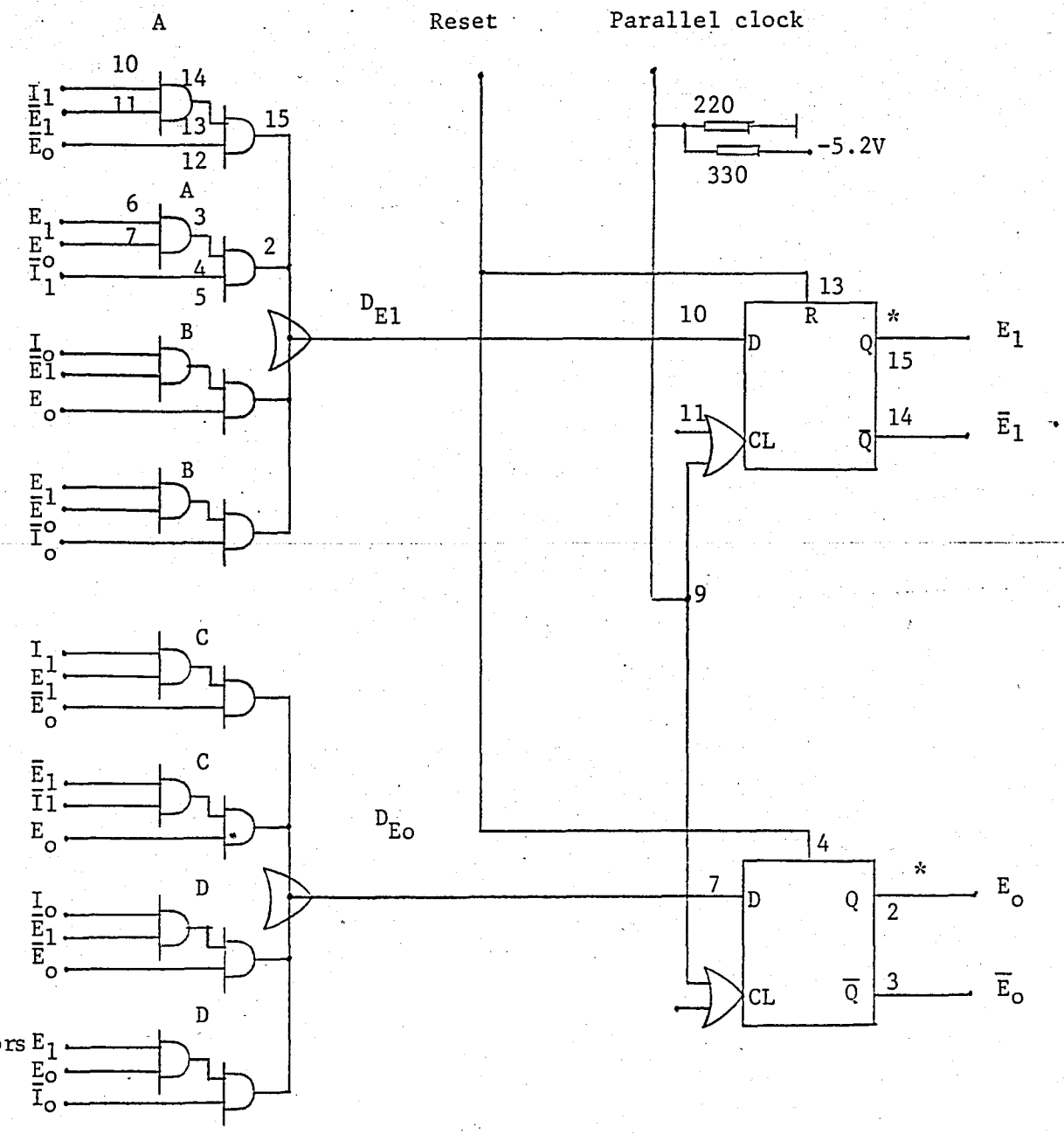


4 AND gate = 1 10104 ECL IC,

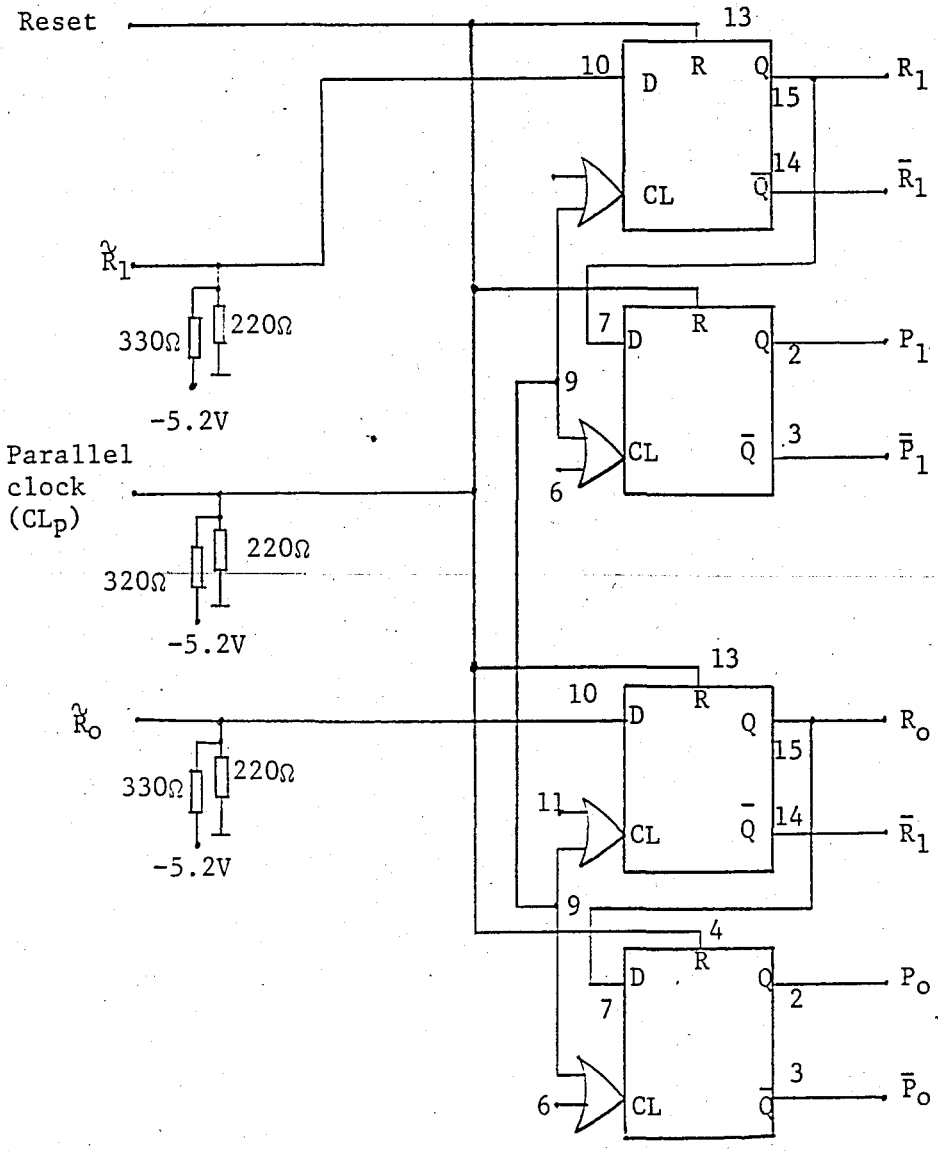
2 D flip-flop = 1 10131 ECL IC.

All emitters have 510 ohm bias resistors

Emitter bias resistors are on the following stage.

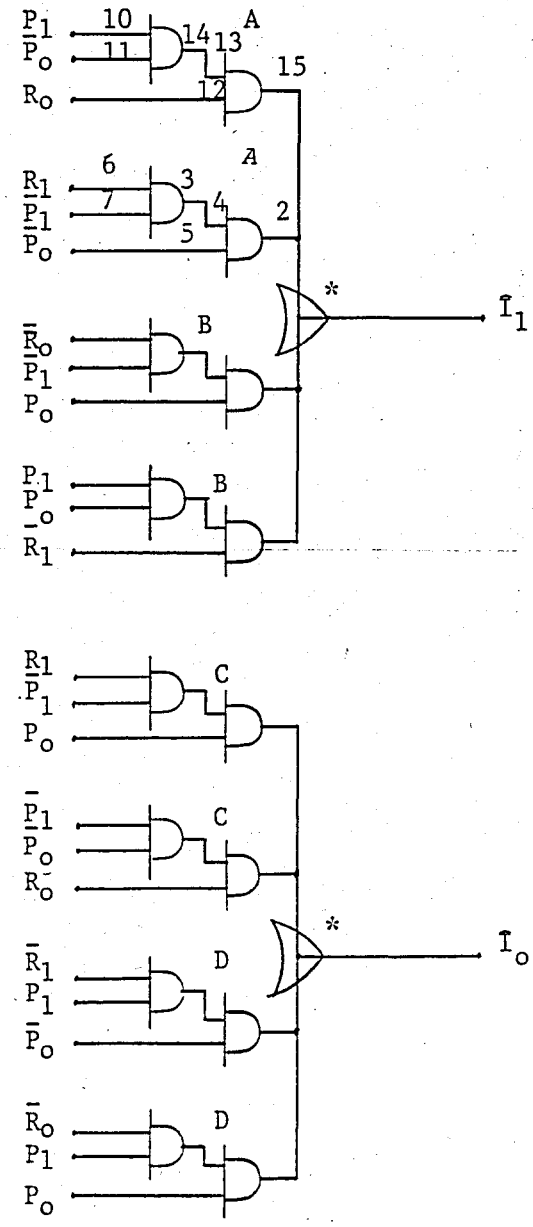


- GRAY CODED DIFFERENTIAL ENCODER-



4 AND gate = 1 10104 ECL IC,
2 D flip-flop=1 10131 ECL IC.
All emitters have 510Ω bias resistors

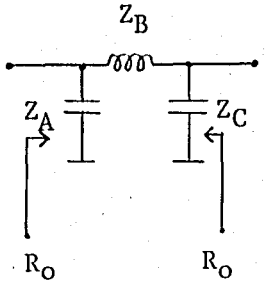
** Emitter bias resistors are on the following stage.*



-GRAY CODED DIFFERENTIAL DECODED-

3.4 - MODULATOR AND POWER SUMMER

The modulator is builded around biphase modulator IC, PM 101, whose electrical characteristics are given in IC specifications section. PM 101 modulators are driven by the line receiver IC, with 10 mA drive current in either state. The IF oscillator (140 MHz external oscillator) is spilled into two, to drive the inphase (I) and quadriphase (Q) channel phase modulators. The Q channel oscillator is 90^{o} phase shifted* prior to the entry into the modulator. The most significant bit of the symbol, I_1, is fed into the I channel and least significant bit, I_o, into the Q channel modulators, respectively, which must be remembered when constructing the demodulator. Finally outputs of I and Q channel modulators are resistively summed, to form the composite DEQPSK modulated IF signal.



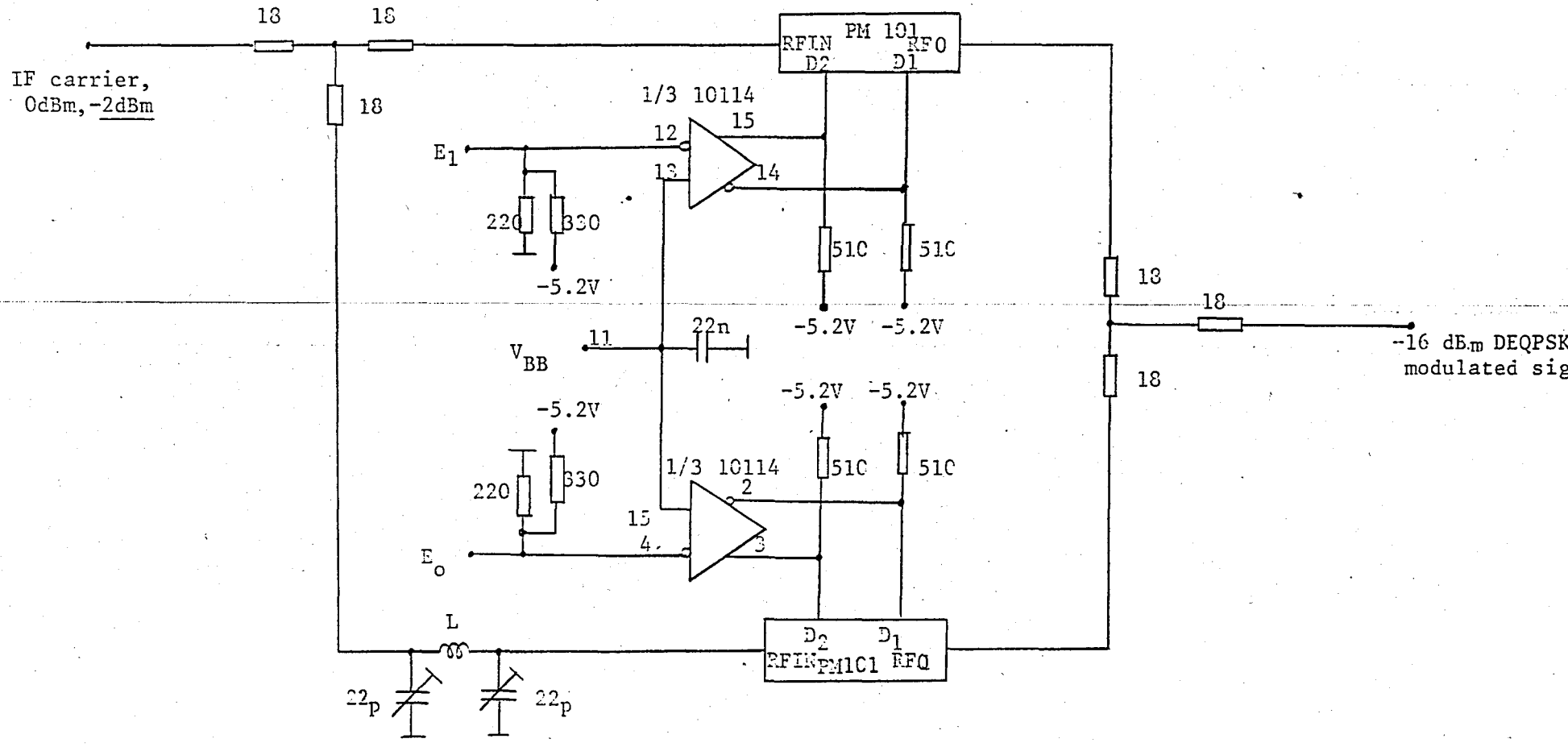
* *The phase shift circuit is a lossless impedance matching network with prescribed phase shift. So it is a minimum 3 element network. The formulas for 'π' network are*

$$Z_A = Z_C = -j\, R_o \left(\frac{\sin\beta}{1-\cos\beta} \right)$$

$$Z_B = j\, R_o \sin\beta$$

If we define $\beta = +\pi/2$ *we obtain one inductor only and we get*

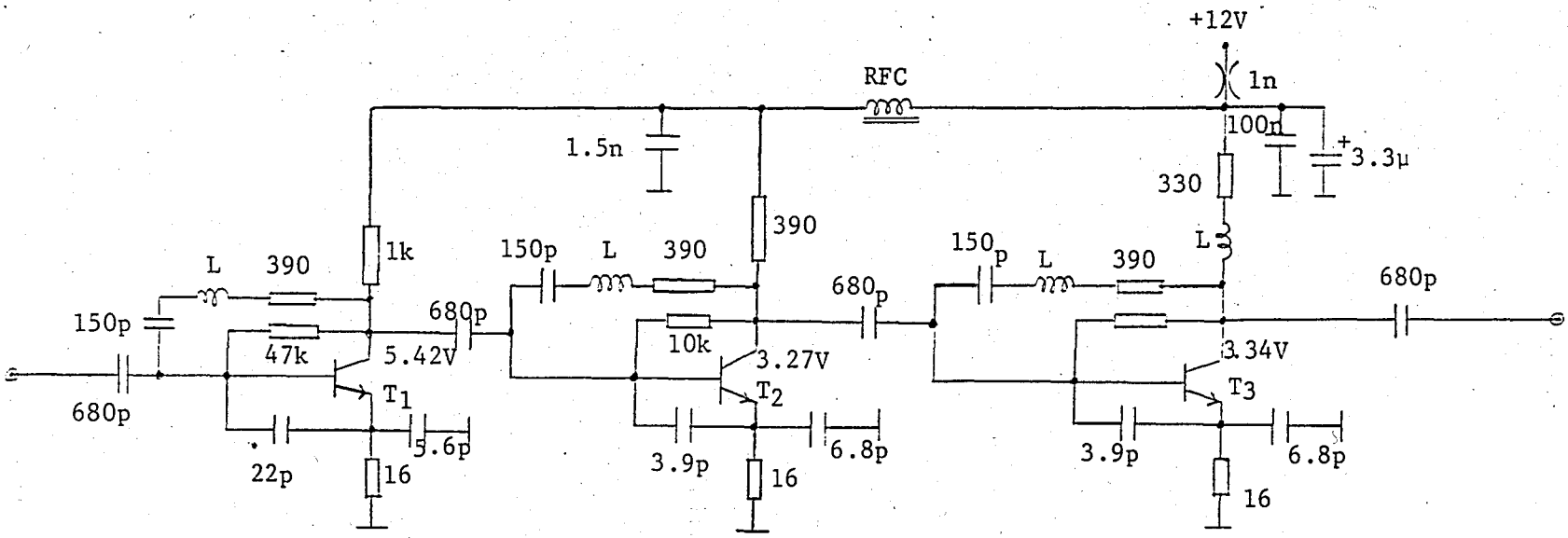
$$X_L = X_C = R_o.$$



L : 4 turns of 0.65 mm wire,
ϕ = 2.2 mm.

-MODULATOR AND SUMMER STAGE-

Not: Resistor values are in ohm,
unless otherwise specified.



L = 5 turns of 65 mm wire, = 3.0 mm

Gain : 27 dB
Freq. - band : 40-860 MHz
Input/output impedance: 75Ω
T_1, T_2 : BFW 92
T_3 : BFW 16 A

Not : Resistor values are in ohm, unless otherwise specified.

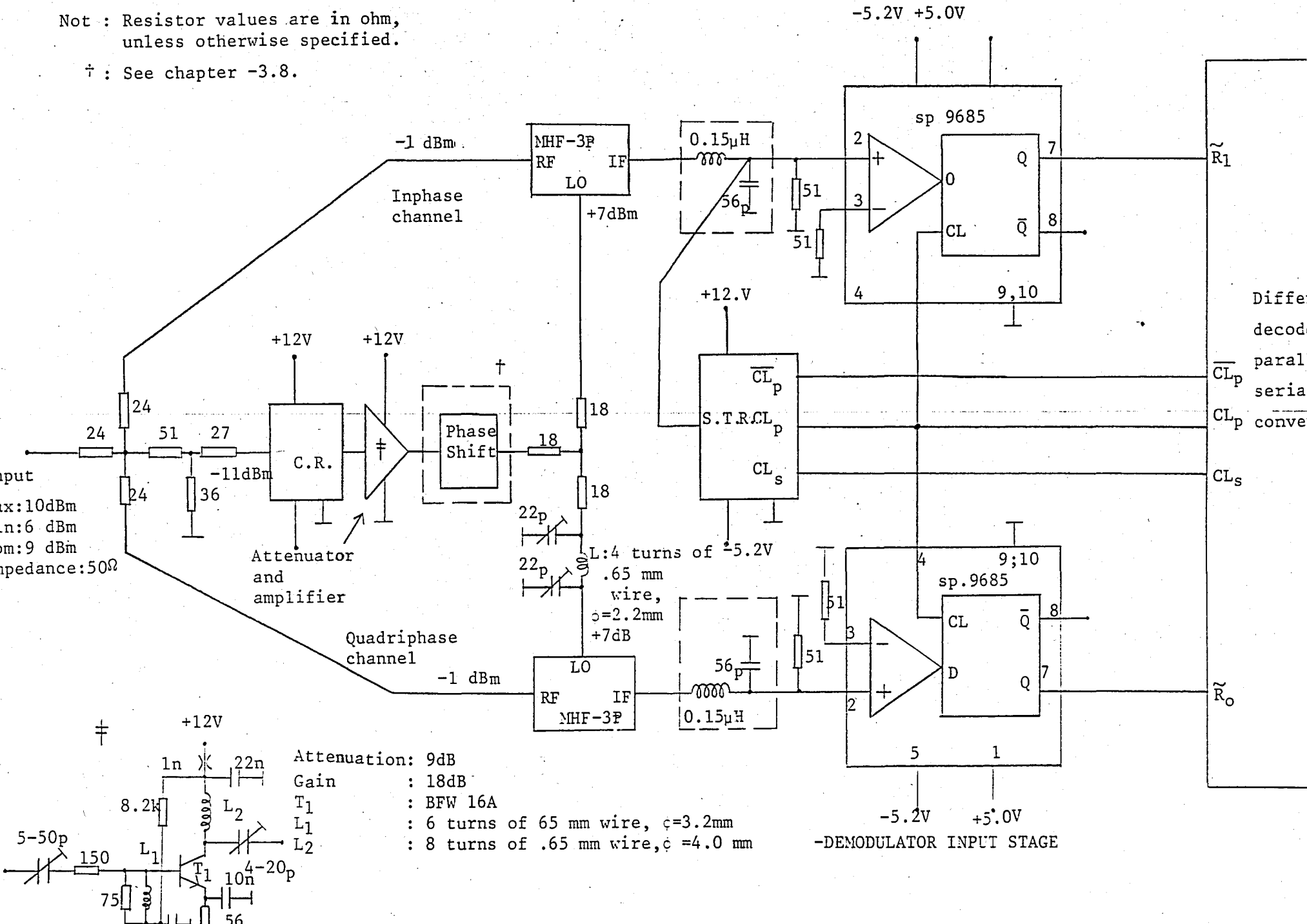
3-5 . IF AMPLIFIER STAGE

This network was already available at the laboratory and duplicated for this modem.

3.6 - DEMODULATOR INPUT STAGE

The received DEQPSK modulated signal is divided into three paths (where power division ratios are shown on the circuit diagram), two into RF channel of the double balanced mixers and one into the carrier recovery (CR) circuit. The output of CR circuit is an ECL gate and is insufficient to drive the two LO inputs of the mixers. So, it is fed to the attenuator followed by single amplifier circuit. The attenuator is a 9.6 dB 'L' section attenuator, having 180 Ω and 50 Ω impedances at the gate and transistor sides respectively, in order to minimize the loading on the gate. The transistor amplifier output is divided into two, one directly driving the LO input of the inphase (I) channel mixer, and the other, driving the LO input of the quadrature (Q) channel mixer, after it is passed through a 90^{o} phase shift network.* Outputs of mixers are lowpass filtered, with second order Butterworth filters (called arm filters), having 70 MHz 3 dB bandwidths. The I channel filter output is applied to the symbol timing recovery (STR) circuit, which extracts the symbol timing signal, CL_p. Arm filter outputs are also applied to the decision comparators, an these comparators are enabled by the STR circuit, with the symbol timing signal, CL_p, to form the digital $I(\tilde{R}_1)$ and Q $(\tilde{R}_o)$ signals.

* *See footnote of chapter 3-4.*


Not : Resistor values are in ohm, unless otherwise specified.
† : See chapter -3.8.
-5.2V +5.0V
sp 9685
-1 dBm
MHF-3P
RF IF
LO
+7dBm
Inphase channel
0.15µH
56p
51
51
+12.V
+12V
+12V
†
24
24
51
27
-11dBm
C.R.
Phase Shift
18
18
18
24
36
22p
22p
L:4 turns of .65 mm wire, ϕ=2.2mm
+7dB
Attenuator and amplifier
Quadriphase channel
-1 dBm
LO
RF IF
MHF-3P
0.15µH
56p
51
51
sp.9685
4 9;10
5 1
-5.2V +5.0V
-DEMODULATOR INPUT STAGE
S.T.R.CLp
CLp
CLs
R̃1
CLp
CLp
CLs
R̃o
Diffe
decod
paral
seria
conve
nput
ax:10dBm
in:6 dBm
om:9 dBm
mpedance:50Ω
+12V
1n
22n
8.2K
L2
5-50p
150
L1
T1
4-20p
10n
75
56
Attenuation: 9dB
Gain : 18dB
T1 : BFW 16A
L1 : 6 turns of 65 mm wire, ϕ=3.2mm
L2 : 8 turns of .65 mm wire, ϕ =4.0 mm

3.7 - SYMBOL TIMING RECOVERY (STR) CIRCUIT*

This circuit extracts the data synchronization signal of the modulator input data stream, and requires fine calibration due to high data rate.

The delay element,'d', is implemented simply by cascaded exclusive -OR ECL gates. The LC prefilter and the following comparator is not included in the circuit card, but, in connection with chapter -2 and the timing diagram below, it is advisable to involve this circuit, in order to improve the operation of the phase detector.

The output of the VCO, being t_{d5} seconds ahead of the parallel clock (CL_p), is tuned to 140 MHz and is used as a serial clock, CL_s, to drive the parallel to serial converter circuit and all the circuits external to the DEQPSK demodulator. The outputs of the divide by two flip-flop, CL_p, and its complement, $\overline{CL}_p$, are the basic reference synchronization signals extracted at the demodulator. Since the CL_p signal enables the decision circuit (see timing diagram), it requires fine calibration, in order for the system performance not to degrade. This is accomplished simply, by inserting a digital delay element, 'D_1', in between the output of divide by two flip-flop and 'V' input of phase detector, which effectively removes the signal path length differences of STR circuit and decision circuits.

* *This circuit is not complete yet, so it is not inserted into the system.*

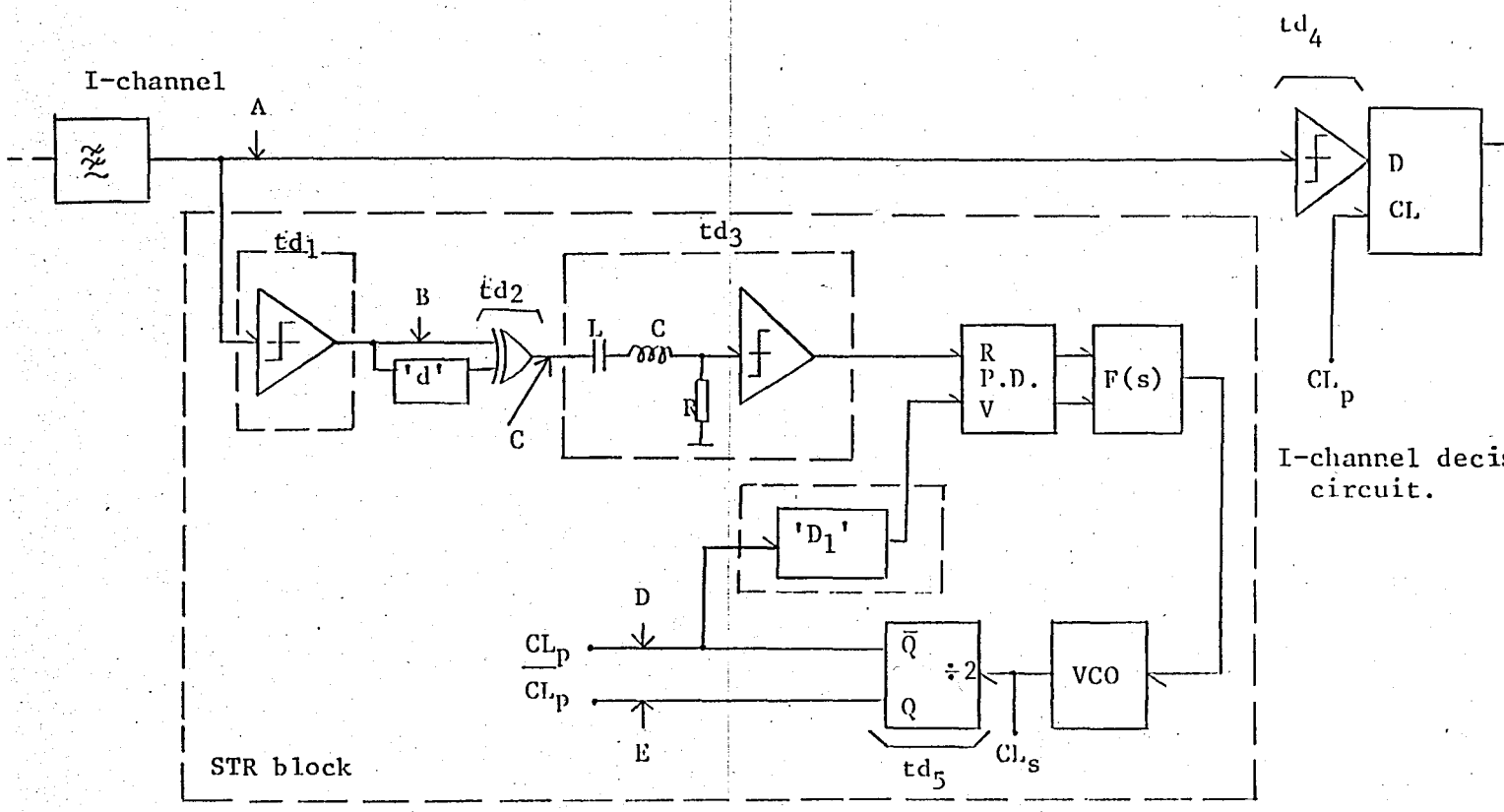
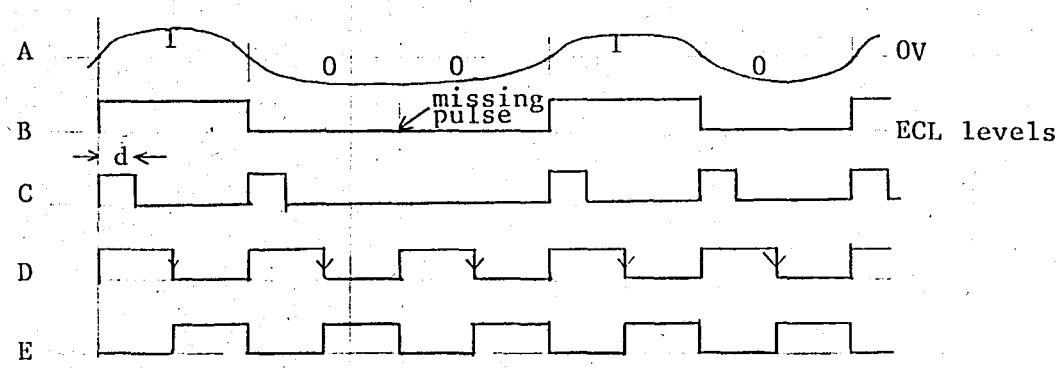


Figure-12 : Serial symbol timing recovery scheme, extended block diagram.

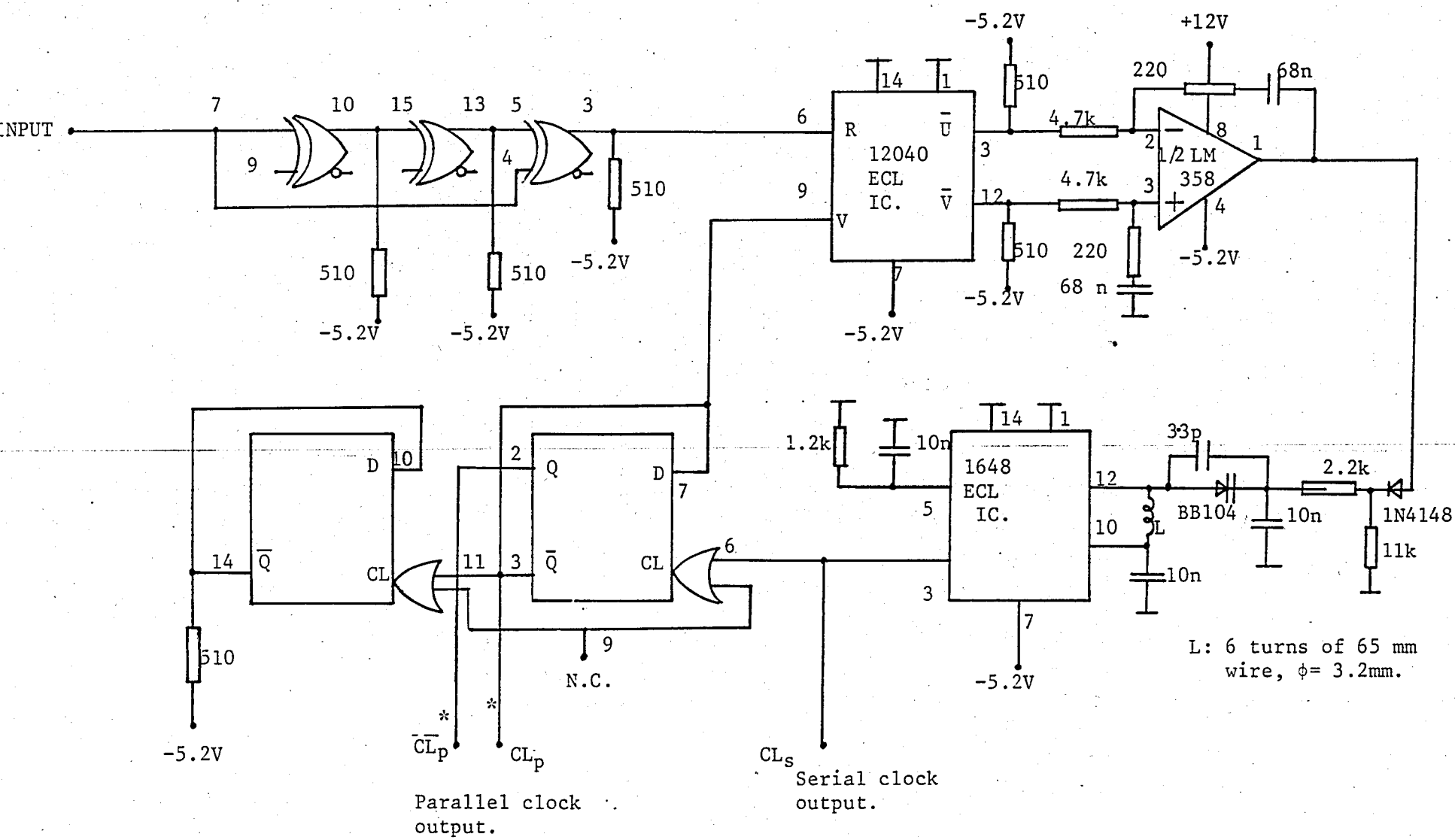
Notes : 1) Framed elements are not included in the implemented circuit (see text).

2) $D_1 \triangleq td_1 + td_2 + td_3 - td_4$



Timing diagram : Ideal elements and jitter free input signal case

Note : the arrow of the 'D' waveform designates the optimum sampl times for decision circuits.



Not : Resistor values are in ohm, unless otherwise specified.

** Emitter bias resistors are on the stages drived by this unit.*
2 D flip-flop = 1 10131 ECL IC.
3 exclusive-OR gate = 3/4 10113 ECL IC.

-SYMBOL TIMING RECOVERY STAGE-

3.8 - CARRIER RECOVERY (CR) CIRCUIT.

This circuit extracts the IF carrier (being DEQPSK modulated) of the modulator and requires fine calibration in order for overall performance not to degrade. (See remark.)

The input preamplifier is used for both isolation and gain purpose before driving the fourth power device. 'L' section impedance matching is performed on both input and output, with HP impedance matching set. The fourth power device is a single transistor biased to the cut off region. The output of this transistor is tuned (parallel tank) to 560 MHz, while input is matched ('π' network) at 140 MHz with large signal parameters. For proper operation in the wide frequency range (110 MHz - 170 MHz) it is also neutralized. Output of this stage feeds a bandpass filter located at 560 MHz. (This filter was already available at the laboratory). Finally, an output amplifier is used to bring the signal to a sufficient level (+10 dBm,+8 dBm) to drive the prescaler. It is again a transistor amplifier and its input and output are matched at 560 MHz, with two 'L' sections. The PLL section (whose card was also available) sees a divide by 64 prescaler, operating on the reference signal path, and divide by 16 circuit, operating at the feedback signal path. Therefore, the VCO output is locked to one fourth of the reference signal, i.e. IF frequency (140 MHz) is extracted at the output of loop VCO. The maximum VCO frequency is set to 145 MHz, since otherwise feedback divide loop does not operate properly, due to speed limitations of those IC's.

Remark : Due to finite delay of the elements in the CR circuit signal

path, the LO inputs of arm mixers do not have 0^{o} phase IF carrier signal. This delay, called D_2, is infact small, but still cause large phase errors due to high IF carrier signal. (Phase error = $2\pi f_{IF} D_2$) So, it is recommended to put a phase shift circuit (see figure -13) in order to compensate this phase error. The calibration operation can be done best experimentally, in a very simple way, as follows. Send IF carrier signal (140 MHz) to the demodulator input. Observe the output of I channel arm mixer and adjust the phase shift, such that the mixer output contains twice of IF carrier frequency and a DC component only.

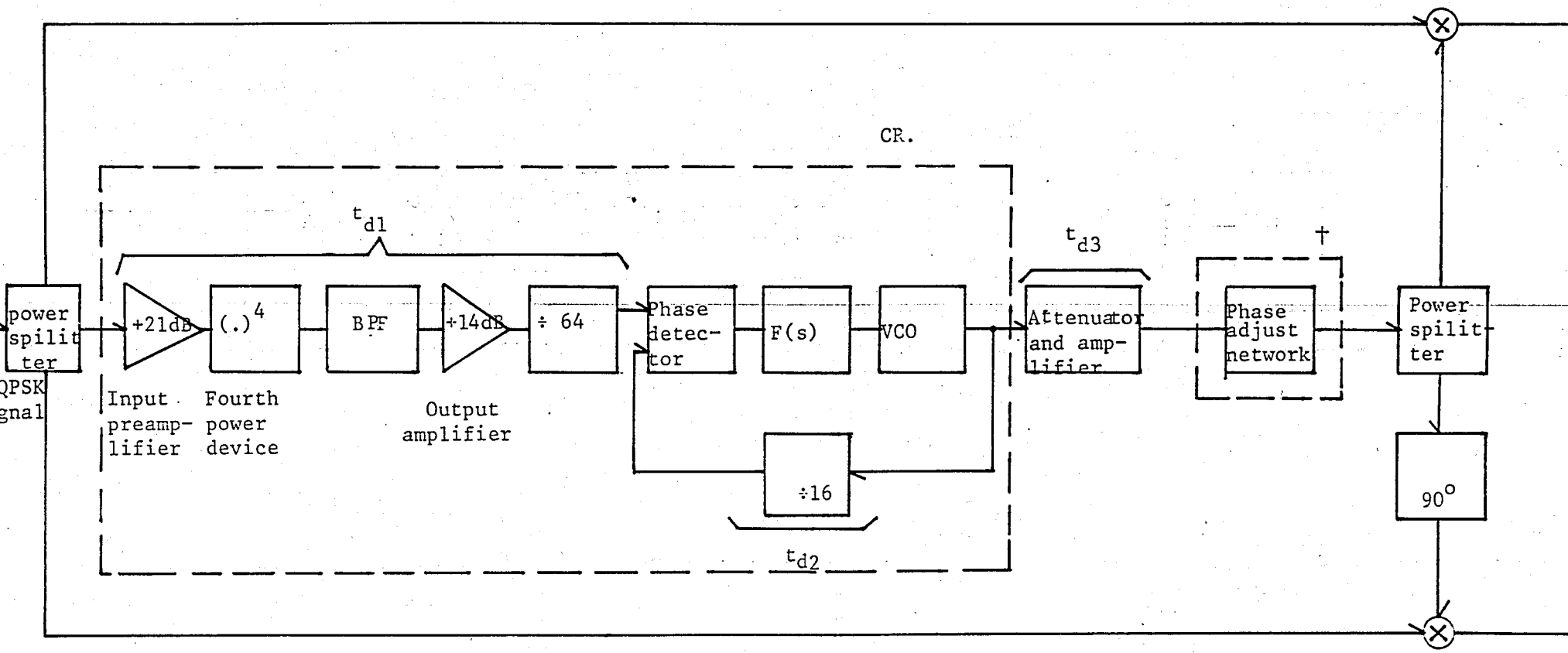
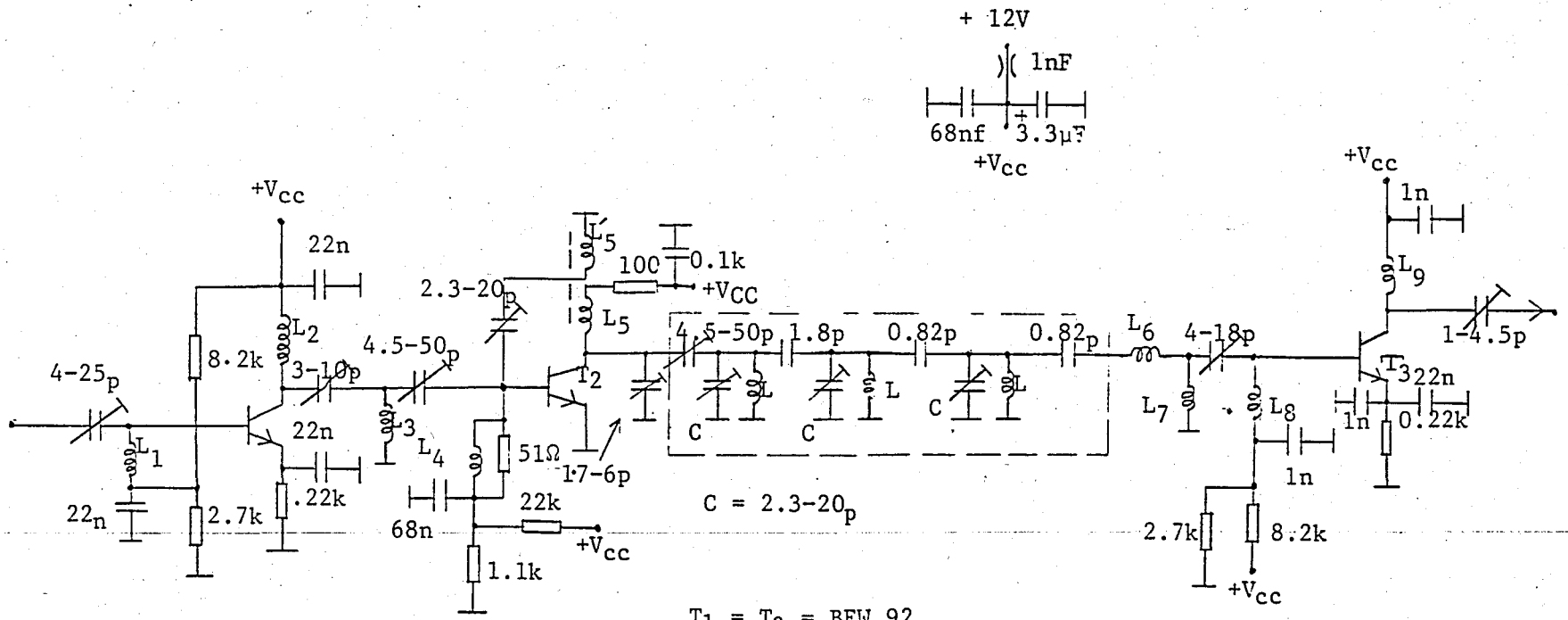


Figure - 13 : CR extended block diagram.

$D_2 = t_{d1} - t_{d2} + t_{d3}$

† : *See text.*



$T_1 = T_3$ = BFW 92

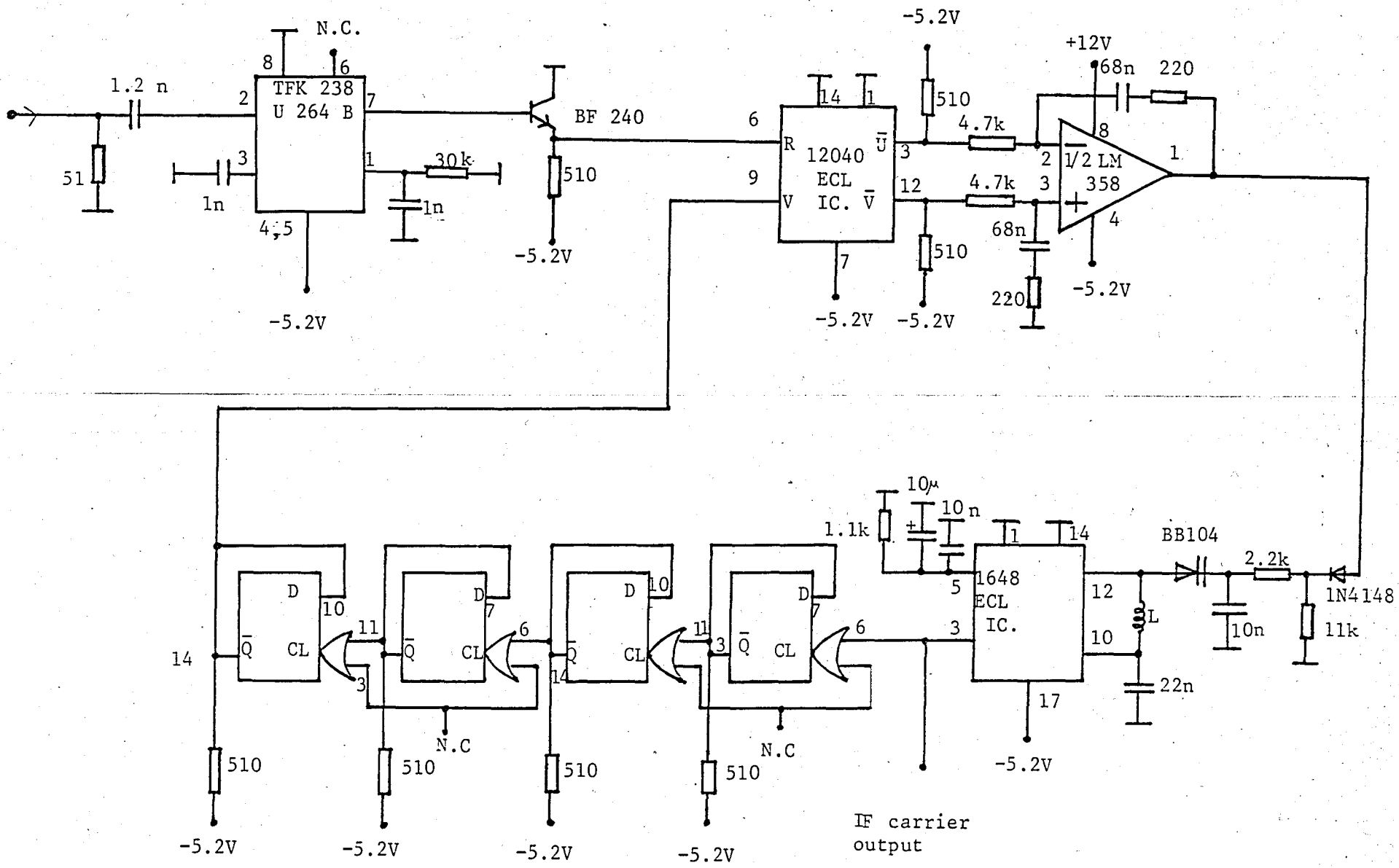
T_2 = BFW 16 A

	diameter (mm)	turns	wire diameter mm
L_1	3.2	6	.65
L_2	4.0	8	.65
L_3	3.3	8	.65
L_4	3.0	4	.65
L_5	2.0	2	.90
L'_5	2.0	2	.90
L_6	2.4	4	.75
L_7	1.4	4	.65
L_8	1.5	3	.65
L_9	1.2	3	.65
L	4.0	1	.65

Input : max : - 6 dBm
min : -12 dBm
Nom : -11 dBm
Impedance : 50Ω
Nominal Input
Frequency : 140 MHz

Output max : 10 dBm
min : 8 dBm
Nom : 9 dBm
Impedance : 50Ω
Nominal output
Frequency : 560 MHz

- CARRIER RECOVERY INPUT STAGE-



Not : Resistor values are in ohm unless otherwise specified.
2 D flip flop = 1 10131 ECL IC.

L = 6 turns of .65 mm wire, ϕ=3.2 mm

-CARRIER RECOVERY PLL STAGE-

IV. EVALUATION AND CONCLUSION

We have taken the very first step in the establishment and improvement of a quadriphase modem. The system structure was selected to be DEQPSK and realized in a modular way. All of the modules, except the STR module, have been tested and put together to form the DEQPSK modem.

The calibration of the modulator has been done, and the whole modulator has been made ready to operate on a single card, with the recommendations of chapter -3. But the 90^{o} phase shift network, on the IF oscillator path, is better to be redesigned with the help of appendix B-2, or, if available, a qudrature (90^{o}) hybid can still improve the operation of the modulator.

The same recommendation, for the 90^{o} phase shift network, also applies to the demodulator's quadrature arm 90^{o} phase shift network. Having supplied the data synchronization signals (CL_p, $\overline{CL_p}$, CL_s) from the modulator card, the whole system had been tested only at 8 Mb/s data rate, due to nonavailability of proper data source, at that time.

The next step to be performed, is to put the STR circuit into operation in conform to the other parts of the demodulator. By this way, once fixing the structure of the demodulator, it is advisable to combine the demodulator,

but mainly the analog portions of it, in a single card, since otherwise neither fine system calibration, nor full data rate of operation is possible to manage. After all, when both modulator and demodulator being implemented on single cards, the system will become to ready undergo performance test and to use.

APPENDICES

A - 1 : BANDPASS SIGNALS

1. A real valued narrow band-pass signal $s(t)$ in the vicinity of a frequency f_c can be expressed as :

$$s(t) = a(t) \cos (2\pi f_c t + \theta(t))$$

$$= x(t)\cos w_c t - y(t) \sin w_c t$$

$$= Re \{ u(t) e^{j 2\pi f_c t} \}$$

where $a(t)$: envelope of $s(t)$

f_c : carrier of $s(t)$

$x(t)$, $y(t)$: quadrature components of $s(t)$

$u(t)$: complex envelope of $s(t)$

$\theta(t)$: phase of $s(t)$

and

$$x(t) = a(t) \cos\theta(t) \qquad y(t) = a(t) \sin\theta(t)$$

$$u(t) = a(t) e^{j\theta(t)} = x(t) + jy(t)$$

These components are called the low-pass signals since the frequency contents of them are concentrated at low frequencies with respect to f_c due

to narrow band nature of $s(t)$. It is simple to show that

$$\text{F.T.}\{ s(t) \} = S(f) = \frac{1}{2}\left[U(f-f_c) + U^*(-f-f_c) \right]$$

$$\{ \text{Energy of the signal} \} = \varepsilon = \langle s^2(t) \rangle = \int_{-\infty}^{+\infty} dt\, s^2(t) = \frac{1}{2}\int_{-\infty}^{+\infty} |u(t)|^2 dt + \frac{1}{2}$$

$$\int_{-\infty}^{+\infty} dt\, |u(t)|^2 \cos(4\pi f_c t + \theta(t))$$

$$\varepsilon \cong \frac{1}{2}\int_{-\infty}^{+\infty} dt\, |u(t)|^2 = \frac{1}{2} \cdot \int_{-\infty}^{+\infty} dt\, a^2(t)$$

2. Real time response band-pass filter $h(t)$ (or $H(f)$) can be expressed interms of equivalent complex low-pass filter component, $c(t)$, (or $C(f)$) as follows;

$H(f) = H^*(-f)$: $h(t)$ is real

defining $C(f-f_c) = H(f)\, u_{-1}(f)$: $u_{-1}(t)$ is a unit step function

so that $C^*(-f-f_c) = H^*(-f)\, u_{-1}^*(-f) = H(f)\, u_{-1}(-f)$

hence $H(f) = C(f-f_c) + C^*(-f-f_c)$

also in time domain $h(t) = c(t)\, e^{j2\pi f_c t} + c^*(t)\, e^{-j2\pi f_c t}$

$h(t) = 2\text{Re}\{ c(t)\, e^{j2\pi f_c t} \}$

where 2 is arbitrary since we could define $C(f-f_c) = \frac{1}{2} H(f)\, u_{-1}(f)$

3. Response of band-pass system to band-pass signal:

Let :

$$s(t) = \text{Re}\{ u(t)\, e^{j2\pi f_c t} \}$$

$$h(t) = 2\text{Re}\{ c(t)\, e^{j2\pi f_c t} \}$$

then $R(f)=S(f).H(f) = \frac{1}{2}\left[U(f-f_c) + U^*(-f-f_c)\right].\left[C(f-f_c) + C^*(-f-f_c)\right]$

$$R(f) = \frac{1}{2}\left[U(f-f_c).\ C(f-f_c) + U^*(-f-f_c)C^*(-f-f_c)\right]$$

since crossterms vanishes due to narrow band nature.

$$R(f) \triangleq \frac{1}{2}.\left[V(f-f_c) + V^*(-f-f_c)\right]$$

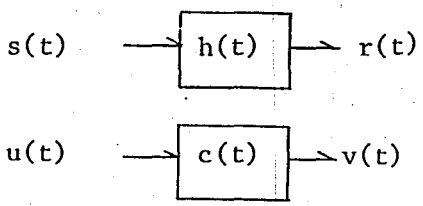
where

$$V(f) = U(f).\ C(f)$$

Rewriting

$$v(t) = u(t)^*\ c(t)\ ;\quad V(f) = U(f)\ .\ C(f) \quad \text{and} \quad r(t) = Re\ \{\ v(t)\ e^{j2\pi f_c t}\ \}$$

Bandpass and Lowpass Representations



So that transformation from band-pass to low-pass (or vice versa) can be done at any point on the block diagram and the rest can be analyzed with that representation.

A - 2 : BANDPASS STATIONARY STOCHASTIC PROCESS REPRESENTATION

Suppose $s(t)$ is a sample function ofaW.S.S. stochastic process with power spectral density (p.s.d) of $G_{ss}(f)$ located in the vinicity of f_c. The stochastic process $s(t)$ is said to be narrow band band-pass process if the width of $G_{ss}(f)$ is much smaller than the carrier f_c. In that case, the sample function $s(t)$ has equivalent low-pass representation given in app. A-1. The autocorrelation (AC) function of $s(t)$ is :

$$R_{ss}(t,\zeta) = E\{ s^*(t)\, s(t+\zeta) \}$$

$$= E\{ [x(t)\cos 2\pi f_c t - y(t)\sin 2\pi f_c t].[x(t+\zeta)\cos 2\pi f_c(t+\zeta) - y(t+\zeta)\sin 2\pi f_c(t+\zeta)] \}$$

expending and remembering that $s(t)$ is W.S.S.

$$R_{ss}(t+\zeta,t) = R_{ss}(\zeta)$$

and setting the time dependent coefficients to zero we get $R_{ss}(\zeta)$ and some relations ;

$$R_{ss}(\zeta) = R_{xx}(\zeta)\cdot\cos 2\pi f_c\zeta - R_{yx}(\zeta)\cdot\sin 2\pi f_c\zeta$$

$$R_{xx}(\zeta) = R_{yy}(\zeta)$$

$$R_{xy}(\zeta) = -R_{yx}(\zeta)$$

indicating that AC functions of quadruture components are interrelated. Now we can define AC function of equivalent low-pass process as follows

$$u(t) = x(t) + jy(t)$$

$$R_{uu}(\zeta) = \frac{1}{2} \cdot E \{ u^*(t)\, u(t+\zeta) \}$$

So that, using above interelation we get :

$$R_{uu}(\zeta) = R_{xx}(\zeta) + j\, R_{yx}(\zeta)$$

hence: $R_{ss}(\zeta) = \mathrm{Re} \{ R_{uu}(\zeta)\, e^{j2\pi f_c \zeta} \}$

informing that the AC function of band-pass stochastic process is completely determined from the AC function of equivalent low-pass process, u(t). Finally taking the Fourier transform and noting that for any stationary complex process, $G_{uu}(f)$ is real function of frequency (since $R_{uu}(\zeta) = R_{uu}(-\zeta)$)

$$G_{ss}(f) = \frac{1}{2} \left[G_{uu}(f-f_c) + G_{uu}(-f-f_c) \right]$$

A - 3 : M-ARY PSK SIGNAL REPRESENTATION IN TERMS OF EQUIVALENT LOW PASS FORM.

Digital phase modulation of a carrier results, when the binary digits from the information sequence, $\{ a_n \}$, are mapped into a set of discrete phases of the carrier. An M-ary PSK signal is generated by mapping blocks of $k=\log_2 M$ binary digits of the sequence $\{a_n\}$, into one of M corresponding phases :

$$\theta_m = 2\pi(m-1)/M \qquad m = 1,M.$$

Resulting equivalent low pass signal :

$$u(t) = \sum_n I_n \, p(t - \frac{n}{r_s})$$

where

r_s = symbol rate = $\frac{1}{T_s}$

$p(t)$ = baseband pulse shape defined in the interval $[0,T_s]$

$I_n = e^{j\theta_n}$

So, QPSK or DEQPSK* modulated signal can be represented in terms of equivalent lowpass from as :

$$u(t) = \sum_n I_n \, p \, (t - \frac{n}{r_s})$$

** The statistics of $\{I_n\}$ are modified by the differential encoder, which inturn, modifies the power spectrum density of the DEQPSK modulated signal.*

and I_n takes one of four possible values, say $\left(\pm \frac{1}{\sqrt{2}} \pm j \frac{1}{\sqrt{2}} \right)$ or $(\pm 1, \pm j)$.

Equivalent low pass form of (DE)QPSK signal, $u(t)$, can also be expressed in a form close to quadrature amplitude modulation (QAM) scheme as follows

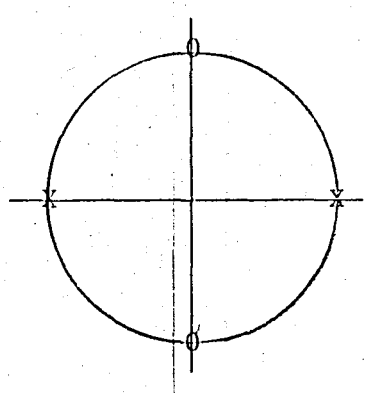
$$u(t) = \sum_n I_n \, p\left(t - \frac{n}{r_s}\right) = \sum_n (I_{nr} + j \, I_{nq}) \, p\left(t - \frac{n}{r_s}\right)$$

$$s(t) = \sum_n I_{nr} \, p(t - n/r_s) \cos 2\pi f_c t - \sum_n I_{nq} \, p(t - n/r_s) \sin 2\pi f_c t$$

where $\{I_{nr}\}$ and $\{I_{nq}\}$ are both complex binary sequences having the property

$$|I_{nr}|^2 = |I_{nq}|^2 .$$

Thus, (DE)QPSK modulated signal can be regarded as two BPSK modulated signals operating in quadrature, if $\{I_{nr}\} = \{\pm 1\}$ is a real and $\{I_{nq}\} = \{\pm j\}$ is an imaginary binary sequences respectively.



I_n domain

X : elements of $\{I_{nr}\}$

0 : elements of $\{I_{nq}\}$

A - 4 : SPECTRAL CHARACTERISTICS OF DIGITALY MODULATED SIGNALS

Remembering appendix A - 2, it is sufficient to the determine the autocorrelation (AC) function and power spectum density (p.s.d.) function of the equivalent low-pass process, u(t), in order to determine the AC function of the sample function, s(t), as defined in app. A-1. Starting with

$$u(t) = \sum_n I_n p(t-nT_s) \; ; \quad T_s = \frac{1}{r_s}$$

I_n ; is the nth real or complex valued information symbol

$p(t)$; is the baseband pulse shape, real or complex valued, defined in the interval $[0,T_s]$.

We assume that the sequence of information symbols $\{I_n\}$ is W.S.S with

$$E\{I_n\} = m_I$$

$$\frac{1}{2} E\{I_n^* I_{n+m}\} = R_{II}(m)$$

so that with the help of app. A.2

$$R_{uu}(t+\zeta,t) = \frac{1}{2} E\{u^*(t)\, u(t+\zeta)\} = \frac{1}{2} \sum_{n,m} E\{I_n^* I_m\} p^*(t-nT_s)p(t-mT_s+\zeta)$$

$$= \sum_{m,n} R_{II}(m-n)\, p^*(t-nT_s)p(t+\zeta-mT_s)$$

$$= \sum_m R_{II}(m) \sum_n p^*(t-nT_s).p(t+\zeta-nT_s-mT_s)$$

The inner summation is periodic in t variable, with period T_s, so is $R_{uu}(t+\zeta, t)$

$$R_{uu}(t+\zeta+T_s\ ;\ t+T_s)\ R_{uu}(t+\zeta, t)$$

Also $E\{u(t)\} = m_I . \Sigma\, p(t-nT_s)$ is too periodic with period T_s. Therefore $u(t)$ is a cyclostationary process. The AC function of a cyclostationary process is found by time averaging $R_{uu}(t+\zeta, t)$ in order to eliminate t variable :

$$R_{uu}(\zeta) = \frac{1}{T_s} \int_{-T_s/2}^{T_s/2} dt\ R_{uu}(t+\zeta, t) = \Sigma\, R_{II}(m) . \frac{1}{T_s} \int_{-T_s/2-nT_s}^{T_s/2-nT_s} dt . p(t)p(t+\zeta-mT_s)$$

$$= \Sigma\, R_{II}(m) \frac{1}{T_s} \int_{-\infty}^{+\infty} dt\ p^*(t) . p(t+\zeta-mT_s)$$

Since $p(t)$ is a deterministic energy signal ($0 < \int_{-\infty}^{\infty} |p(t)|^2 dt < \infty$) its AC function given as :

$$R_{pp}(\zeta) = \langle p(t),\ p(t+\zeta) \rangle = \int_{-\infty}^{+\infty} dt\ p^*(t)p(t+\zeta)$$

Hence $R_{uu}(\zeta) = \frac{1}{T_s} \sum_m R_{II}(m) . R_{pp}(\zeta-mT_s)$

Finally the average p.s.d. function is :

$$G_{uu}(f) = \frac{1}{T_s} \int_{-\infty}^{+\infty} d\zeta \left[\sum_m R_{II}(m)\ R_{pp}(\zeta-mT_s) . e^{-j2\pi f\zeta} \right]$$

$$= \frac{1}{T_s} \sum_m R_{II}(m) \int_{-\infty}^{+\infty} d\zeta\ R_{pp}(\zeta-mT_s) e^{-j2\pi f\zeta}$$

$$= \frac{1}{T_s} \cdot \sum_m R_{II}(m)\ e^{-j2\pi fmT_s} \int_{-\infty}^{\infty} d\zeta\ R_{pp}(\zeta)\ e^{-j2\pi f\zeta}$$

So: $$G_{uu}(f) = \frac{1}{T_s} |P(f)|^2\ G_{II}(f)$$

where $P(f) = \text{F.T.}\ \{\ p(t)\ \}$,

$$G_{II}(f) \triangleq \sum_m R_{II}(m)\ e^{-j2\pi fmT_s} .$$

It is interesting to note that $G_{II}(f)$ is the exponential Fourier (extention) series with the $R_{II}(m)$ as the Fourier coefficients. Hence

$$R_{II}(m) = T_s \int_{-1/2T_s}^{1/2T_s} df\ G_{II}(f)\ e^{j2\pi fmT_s}$$

Let us consider the case, for which the information symbols in the sequence are complex and mutually uncorrelated. Therefore

$$E\ \{I_n\} = m_I \quad ; \quad E\ \{I_n^*\} = m_I^*$$

$$\sigma_I^2 = E\ \{\ |\ I_n - E\{I_n\}|^2\ \} = E\ \{\ |I_n|^2\} - |m_I|^2$$

$$E\ \{I_n^* I_{n+m}\} = \begin{cases} E\ \{\ |I_n|^2\ \} & m = 0 \\ E\ \{I_n^*\}.E\ \{I_{n+m}\} & m \neq 0 \end{cases}$$

$$R_{II}(m) = E\ \{\ I_n^*\ I_{n+m}\} = \begin{cases} \sigma_I^2 + |m_I|^2 & m = 0 \\ |m_I|^2 & m \neq 0 \end{cases}$$

So $$G_{II}(f) = \sigma_I^2 + |m_I|^2 \sum_m e^{-j2\pi f m T_s}$$

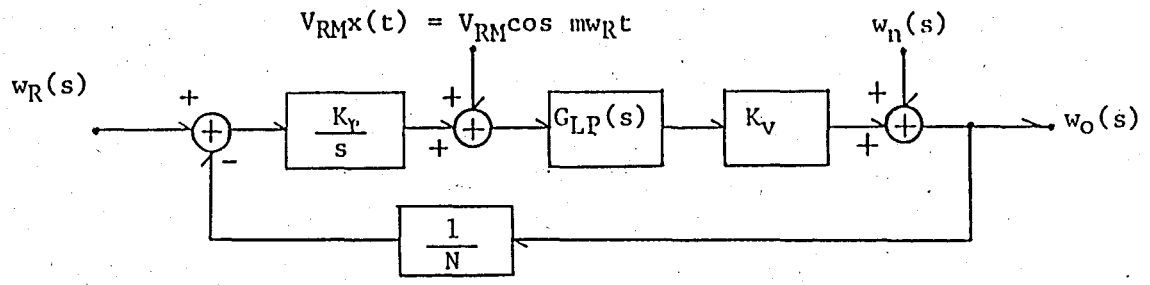
$$= \sigma_I^2 + \frac{|m_I|^2}{T_s} \sum_m u_o\left(f - \frac{m}{T_s}\right) \quad ; u_o(f) \text{ is the unit impulse function .}$$

Finally

$$G_{uu}(f) = \frac{\sigma_I^2}{T_s} \cdot |P(f)|^2 + \frac{|m_I|^2}{T_s^2} \sum_m \left|P\left(\frac{m}{T_s}\right)\right|^2 \cdot u_b\left(f - \frac{m}{T_s}\right)$$

B - I. PLL, BRIEF THEORY.

We shall consider the operation of the PLL in its linear range, so that, signals have small perturbations around the nominal values, loop parameters may be considered constant and simple s-domain (or z-domain) analysis can lead to simple but powerful design equations. Let us start with the block diagram, shown.



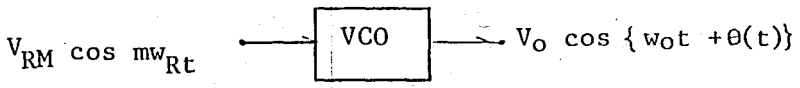
Where, $G_{LP}(s)$ is the loop filter (active or passive), K_v(rad/sec/volts) is the voltage controlled oscillator (VCO) frequency gain, $w_n(s)$ VCO noise in the vicinity of nominal VCO output frequency (f_o), and K_ϕ (volts/radian) is the phase detector gain. Phase detector is modelled as to pass only the low frequency error signal spectrum (spectrum around DC component of the error signal), so, the rest of the error signal spectrum (around all possible harmonics of the reference frequency), which constitute the undesired portion, is included externally as

$$V_{RM}\, x(t) = V_{RM} \cos mw_R t$$

where m is used to designate the dominating harmonic.

The undesired portion of the error signal should be small enough for good spectral purity. Because, they narrow band frequency modulate (NBFM) the nominal output frequency, fo, to produce sidebands at the multiples

of the reference frequency, in the vicinity of f_o. (see figure B-1.1)

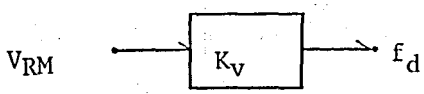


V_o = output peak amplitude of VCO.

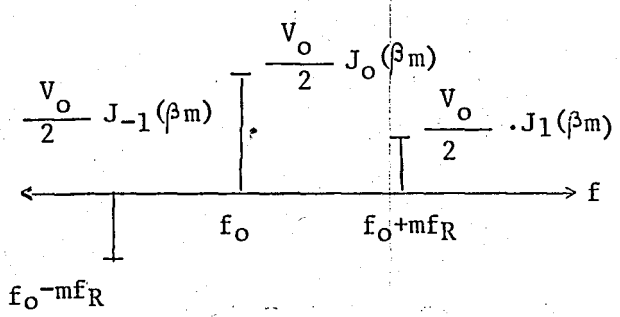
$\theta(t) = \beta_m \sin mw_R t$

$$\beta m = \frac{f_d}{mf_R} \quad ; \quad fd = K_v \cdot V_{RM}$$

a) VCO signal flow



b) VCO model to the reference harmonics



$$J_n(X) \cong \frac{1}{2^n n!} X^n; \quad X << 1$$

c) Single sided frequency spectrum.

Figure B-1.1.

The input voltage, V_{RM}, into the VCO, sets the frequency deviation, f_d, according to the formula

$$f_d = K_v \cdot V_{RM}$$

Considering only the first sideband (NBFM approximation) the sideband amplitude to the center frequency amplitude ratio (in dB usually) is a design parameter given by

$$\frac{m \text{ th reference harmonic first sideband amplitude}}{m \text{ th reference harmonic center frequency amplitude}} = \frac{(V_o/2)\ J_1(\beta m)}{(V_o/2)\ J_o(\beta m)}$$

$$\simeq \frac{1}{2} \cdot \beta m$$

$$= \frac{1}{2} \cdot \frac{f_d}{m f_R}$$

Ideally, for balanced mixer and exclusive -OR gate types of phase detectors, error signal has no component around the first harmonic of the reference frequency. |8,pp.106| The strongest component of the undesired portion of the error signal is concentrated around the second harmonic of the reference frequency. However, for D flip-flop type of phase detectors*, the strongest component is concentrated around the first harmonic, and the maximum amplitude of this component, V_{R1}, is simply the Fourier extension fundamental coefficient

* *Phase frequency detector is also a D flip-flop type phase detector, having fast acquisition aiding logic and larger input phase range (-360° to + 360).* |8|

of a square wave, when its duty cycle is $\tau = T_o/2$, [8, pp. 106].

$$V_{R1} = (V_{DD}-V_{SS}) \left(\frac{2}{\pi}\right) \text{ volts}$$

where $(V_{DD}-V_{SS})$ is the peak to peak output swing of the phase detector.

Now, let's drive the transfer functions with respect to inputs, $w_R(s)$ $V_{RM}.X(s)$ and $w_n(s)$.

$$\text{Loop gain} = GH(s) = \frac{K_\varphi . K_v}{N.s} \cdot G_{LP}(s)$$

$$\text{Closed loop gain} = \frac{\text{forward gain}}{1 + \text{loop gain}} = \frac{1}{\text{feedback gain}} \cdot \frac{\text{loop gain}}{1 + \text{loop gain}} = \frac{1}{H_i(s)} \cdot \frac{GH(s)}{1 + GH(s)}$$

Closed loop gain to the reference frequency input :

$$\frac{w_o(s)}{w_R(s)} = N. \left(\frac{GH(s)}{1 + GH(s)}\right)$$

Closed loop gain to the VCO noise :

$$\frac{w_o(s)}{w_n(s)} = \frac{1}{1 + GH(s)} = 1 - \frac{GH(s)}{1 + GH(s)}$$

Closed loop gain to the undesired portion of the error signal generated by the

phase detector :

$$\frac{w_o(s)}{X(s)} = V_{RM} \cdot K_v \, G_{LP}(s) \cdot \frac{1}{1 + GH(s)} \tilde{=} V_{RM} \cdot K_v \, G_{LP}(s)$$

$$= V_{RM} \cdot \frac{N.s}{K_\varphi} \cdot \left(\frac{GH(s)}{1 + GH(s)}\right)$$

The transfer function, $GH(s)/\ 1 + GH(s)$, is the basic design parameter to be optimized, with respect to wide pull in and hold in range, fast setling time and narrow bandwidth. The second equation, which relates the output frequency to the VCO noise, is made as small as possible with a low noise oscillator and sufficient loop bandwidth, such that, the VCO noise (in the vicinity of f_o) falls into the loop bandwidth. (See the equation above, when $GH(s)/\ [1 + GH(s)] \tilde{=} 1$) The last equation informs us that, spectral purity is achived only with $G_{LP}(s)$, since, at the reference frequency harmonics of the error signal high pass behavior of the $1/\ [1 + GH(s)]$ term does not introduce any attenuation. However, those frequencies fall into the cut off band of the loop filter, $G_{LP}(s)$. Numerically, assuming $[1 + GH(jmw_R)] \tilde{=} 1$, and employing a D flip-flop type of phase detector, we get the expression for the required sideband suppression as follows :

Using phasor representation :

we get $V_{R1}.\cos w_R t \qquad V_{R1} \angle 0^o \ ; \ X(jw_R) = 1 \angle 0^o$

$$\left|w_o(jw_R)\right| \triangleq w_d = V_{R1}.K_v \left|G_{LP}(jw_R)\right| \quad \text{rad/sec}$$

But $$\frac{\text{sideband amplitude}}{\text{center frequency amplitude}} = \frac{\beta_1}{2} = \frac{w_d}{2w_R}$$

is a given quantity. So we get the necessary condition required by the loop filter for a given sideband suppression, $\beta_{1/2}$, as

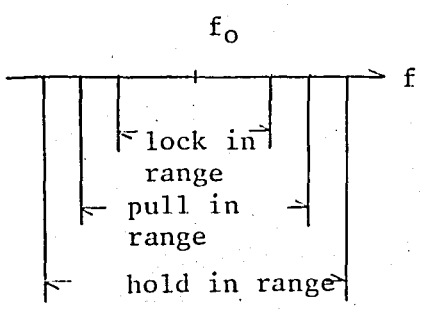
$$|G_{LP}(jw_R)| \leq \frac{w_d}{V_{R1}.K_v} = \frac{2w_R.\ (\beta_{1/2})}{(V_{DD}-V_{SS})(\frac{2}{\pi}).K_v}$$

where $V_{R1} = (V_{DD}-V_{SS})(\frac{2}{\pi})$ and w_d is the frequency deviation of NBFM, as both defined previously. It is clear that required attenuation of the filter increases proportionally to the VCO gain. For instance, voltage controlled crystal oscillator having a very low gain (K_v), has also very pure output at the cost of small tuning range.

The type of the system is defined as the multiplicity of a pole at the origin, namely 'n' in the general expression of the loop gain function, given as

$$GH(s) = G_o.\ \frac{\prod_k (T_k\ s+1)}{s^n \prod_i (T_i\ s+1)}$$

Also, the order of the system is defined as the highest power in the denominator of GH(s). Type-1 systems have been extensively analyzed in the past, and it is shown that |8|, the lock in range, pull in range and hold in range*



* *A locked loop will remain lock over the hold in range. Suppose, the loop VCO is mistuned (for example, in the absence of reference signal) prior to locking operation. The loop may skip many cycles, then ceases cycle skipping and pulls into lock, if the VCO mistuning frequency remains in the pull in (also called the frequency acquisition) range. Otherwise, if the VCO mistuning frequency is beyond the pull in range, the loop may skip cycles indefinitelly. However, if the VCO mistuning frequency remains in the lock in (also called seize frequency) range, the loop pulls into lock exponentially, without any cycle skipping* |8|

In the definitions above, 'may' is used to indicate the worst case conditions of the initial phase.

all depend proportionally on the velocity constant, K_V where

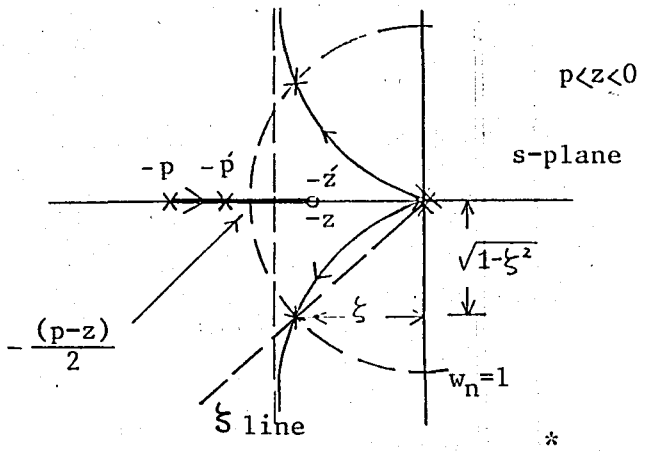
$$K_V = \lim_{s \to 0} s.GH(s)$$

Hence, all these 3 quantities must also be included in the PLL design, since K_V assumes a finite value for type-1 systems. Since for type-2 or higher order system, the velocity constant becomes infinite, these 3 quantities also become infinite (actually they are limited by the unsymmetry of the phase detector, offset voltage of the phase detector and active components in the loop, tuning range of VCO, etc), so, they need not be considered in the PLL design.

The type-2 third order organization is the most used one. However, if the reference frequency is close to the loop bandwidth, then extra atenuation is supplied by another pole, when type-2 fourth order organization is employed. The type-2 second order system however, has no reference filtering at all, but simple and extensively analyzed. Now we will give the normalized* root locus plots and brief analysis of the most commonly used PLL systems; third order and fourth order type-2 systems.

* *The closed loop transfer function involves a second order factor, of the form $w_n^2/(s^2+2\zeta w_n s+w_n^2)$, which, by the design, dominates over the system behavior, hence sets approximately the loop bandwidth, setting time and damping coefficient. So, the transfer functions are normalized with respect to the w_n, to simplify the design*

Third order type-2 system :



Loop gain, GH(s), and $\frac{GH(s)}{1 + GH(s)} = G_f(s)$ are defined as *

$$GH(s) = K \frac{(s + z)}{s^2(s + p)}$$

$$G_f(s) = \frac{GH(s)}{1 + GH(s)} = \acute{K} \frac{s + z'}{(s^2 + 2\zeta s + 1)(s + p')}$$

where primed symbols denote the closed loop parameters. If we choose p' and z' very close to each other, their individual effects, on the closed loop transfer function, $G_f(s)$, cancel out, and closed loop system behaves like a second order system having a transfer function

$$G_f(s) = \frac{\acute{K}}{(s^2 + 2\zeta s + 1)}$$

So, in this case, loop behavior is readly found from the well known theory of the second order systems, and the problem turns out to be the determination of the value of the open loop parameters from a given closed loop transfer function. We can find the values of the open loop parmeters,

* *Since feedback gain involves a frequency independent term ($\frac{1}{N}$) and affect the closed gain as a scale factor, it is discarded in this analysis.*

simply, by the coefficient matching technique and can get one design algorithm as follows

1. Choose $(\acute{p}/\acute{z})$ ratio. By design, closed loop $(\acute{p})$ and zero $(\acute{z})$ are made as close as possible, such as : $(\acute{p}/\acute{z}) = 1.2$

2. Choose any two of undamped natural frequency (w_n), damping factor (ζ) or settling time (t_s).

3. Find the third parameter from the equation :

$$w_n . t_s . \zeta = \begin{cases} 4 & \text{for \% 2 final value error} \\ 3 & \text{for \% 5 final value error} \end{cases}$$

4. Use the equations below, to find the values of the open loop paremeters (p,z,K)

a). $K = K' = (p'/z')$

b). $p' = \dfrac{K'-1}{2\zeta}$

c). $z = z' = (p'/K')$

d). $p = 2\zeta + p'$

5. Denormalize the open loop transfer function with respect to w_n. (This step may be skipped to obtain the normalized system design.)

$$GH(s) = K. \frac{(s/w_n + z)}{(s/w_n)^2 (s/w_n + p)}$$

$$\Longrightarrow \quad K \longrightarrow K. w_n^2$$

$$z \longrightarrow z. w_n$$

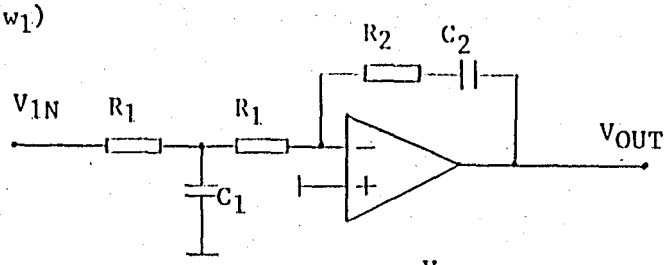
$$p \longrightarrow p. w_n$$

6. Realize the system, where $GH(s) = \frac{K_\varphi . K_v}{N.s} . G_{LP}(s)$ as given previously. A proper loop filter can be given as

$$G_{LP}(s) = -\frac{1}{2R_1C_2} \cdot \frac{(1 + s/w_2)}{s(1 + s/w_1)}$$

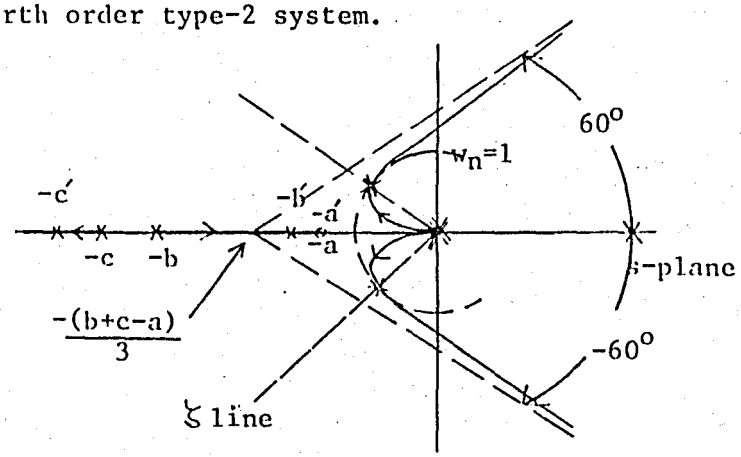
$$w_1 = \frac{2}{R_1C_1}$$

$$w_2 = \frac{1}{R_2C_2}$$



$$G_{LP}(s) = \frac{V_{OUT(s)}}{V_{IN(s)}}$$

Fourth order type-2 system.



$0 < a < b \,||\, c$

$0 < b < c$

Loop gain, GH(s), and $\frac{GH(s)}{1 + GH(s)} = G_f(s)$ are defined as

$$GH(s) = K. \frac{(s + a)}{s^2(s+b)(s+c)}$$

$$G_f(s) = \frac{GH(s)}{1 + GH(s)} = K' \frac{(s+ a')}{(s^2+2\xi s+1)(s+b')(s+c')}$$

where primed symbols denote the closed loop parameters. By choosing the closed loop zero (a') and the closed loop pole (b') (see root locus plot) very close to each other, their individual effects, on the closed loop transfer function, cancel out. So, closed loop system behaves like to third order system, having transfer function :

$$G_f(s) = K' \cdot \frac{1}{(s^2+2\zeta s+1)(s+c')}$$

The operation of this system is usually optimized with respect to the rejection of the reference harmonics, generated by phase the detector, and in this case, one design algorithm is given as follows.

1. Choose w_n, ζ , closed loop pole (c') and (b'/a') ratio.

By design (b'/a') ratio is made as close to unity as possible and c' with can be choosen, such that, the closed loop transfer function, $G_f(s)$, performs a prescribed third order filter function. (Sometimes the value of c' needs to corrected.)

2. Use equations below to find the values of the open loop parameters. (K, a,b,c.)

a). $K = K' = (b'/a') \cdot c'$

b). $b' = \frac{K'-c'}{2\zeta c'+1} = \frac{(b'/a')-1}{2\zeta c' +1} \cdot c'$

c). $a = a' = \frac{b'}{(b'/a')}$

d). $b.c = 1 + b'.c' + 2\xi(b'+c')$

$b+c = 2\xi + b'+c'$

3. Denormalize the open loop transfer function with respect to w_n. (This step may be skipped to obtain the normalized system design).

$$GH(s) = K. \frac{(s/w_n + a)}{(s/w_n)^2 (s/w_n+b)(s/w_n+c)}$$

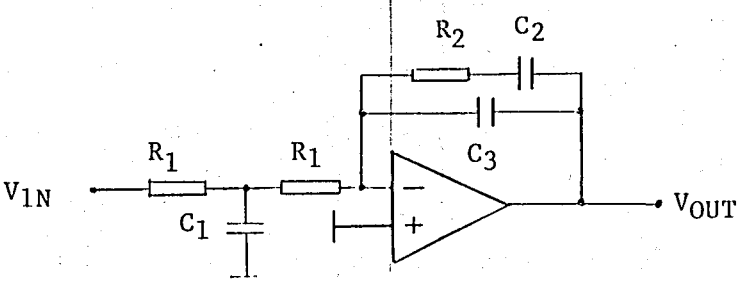
$$\Longrightarrow \quad K \leftarrow K.\ w_n^3$$

$$a \leftarrow a.\ w_n$$

$$b \leftarrow b.\ w_n$$

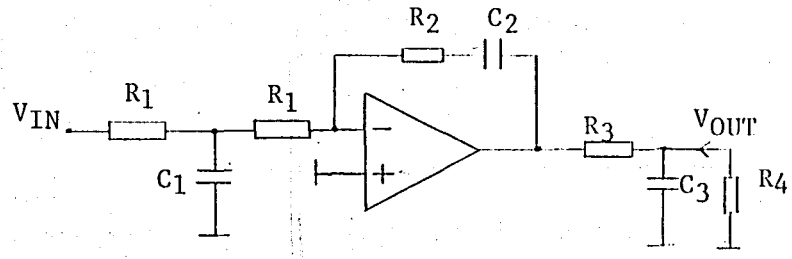
$$c \leftarrow c\ \ w_n$$

4. Realize the system, where $GH(s) = \frac{K_\varphi \cdot K_V}{N.s} G_{LP}(s)$ as given previously. Two proper loop filters are given as:



$$G_{LP}(s) = -\frac{1}{2R_1(C_2+C_3)} \cdot \frac{(1 + s/w_2)}{s(1+s/w_1)(1+s/w_3)}$$

$$w_1 = \frac{2}{R_1 C_1} \qquad w_2 = \frac{1}{R_2 C_2} \qquad w_3 = \frac{1}{(C_2 || C_3) R_2} \qquad C_2 || C_3 = \frac{C_2 . C_3}{C_2+C_3}$$



$$G_{LP}(s) = -\frac{1}{2R_1C_2} \cdot \frac{R_4}{R_3 + R_4} \cdot \frac{(1+s/w_2)}{s(1+s/w_1)(1+s/w_3)}$$

$$w_1 = \frac{2}{R_1C_1} \quad ; \quad w_2 = \frac{1}{R_2C_2} \quad ; \quad w_3 = \frac{1}{(R_3 \| R_4)C_3} \qquad R_3 \| R_4 = \frac{R_3 \cdot R_4}{R_3 + R_4}$$

As a final step, one overall design algorithm can be given as follows

1). Start with closed loop parameters

2). Determine the values of the open loop parameters

3). Find phase and gain margins

4). Find the loop filter transfer function

5.) Check if the sideband to carrier suppression is satisfied.

If any of the above conditions fails, then

1). Change the order of the system

2). Change the type of the system

3). Replace the elements of PLL by others (such as VCO (K_v), phase detector (K_φ), N)

4). Change overall design strategy.

B - 2. WIDE-BAND PHASE SPILITTING NETWORKS

The design of a single, realizable, constant phase shift network over a prescribed frequency band is almost impossible, but two networks can make this problem solved. One way of producing a constant phase difference is possible, if one has phase shift networks, such that their phase shifts (β_1, β_2) varies as the logarithm of frequency, in the prescribed band.* Mathematically

$$\beta_1 = C + \log f \quad \beta_2 = C + \log K_f$$

$$\beta = \beta_2 - \beta_1 = \log K = \text{constant}.$$

However, the networks should also have constant amplitude in that band. This second limitation usually restricts the final networks to the lattice types, since the finite ladder networks, having any phase shift, have also amplitude variations.

Now, let's focus carefully on the difference phase function defined as

$$y(w) = \tan\left[\frac{1}{2}\beta(w)\right] \quad ; \quad \beta(w) = \beta_2(w) - \beta_1(w)$$

Since, the difference phase function is odd (the difference of odd functions is also odd), the approximation problem turns out to be the approximation of a constant via odd rational functions. On the other hand, the difference phase function does not need to satisfy all the properties of Foster's reactance theorem. That is, it should be an odd rational function of frequency, which

* *Such networks are investigated under the heading: 'Logarithmic phase response filters'. J.D. Rhodes,'Theory of electrical filters',John Willey and Sons, 1976.*

is zero or infinite at zero and infinite frequencies, its zeroes and poles need not alternate or occur at real frequencies, and, the degree of denominator and numerator can differ widely. Since, at zero and infinite frequencies, the difference phase function is either zero or infinite, approximation has a band-pass nature and has a form

$$w_L = \sqrt{k}$$

$$w_H = 1/\sqrt{k}$$

in the vicinity of w=1. Also, since the difference phase function is to be constant, no zeroes or poles are allowed in the approximation band. The last statement also implies that, the difference phase function is better not to have any real pole or zero, except at zero and infinite frequencies, since any real pole or zero, not necessarly being in the approximation band, would introduce further deviation from a constant. By the same reasoning, zeroes or poles at zero and infinite frequencies should be of first order, so degree of numerator and denonimator should differ at most by one.

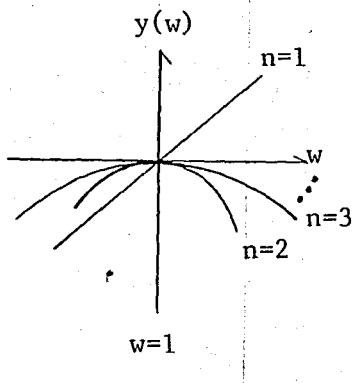
Making use of all the properties above and letting y(w) be a symetric function in the logarithmic frequency scale, in the vicinity of w=1, we get (for any complexity, n) |23|

$$y_1(w) = w \quad y_2(w) = k\,\frac{w}{1+w^2} \quad y_3(w) = w.\,\frac{a + w^2}{1 + aw^2}$$

$$y_4(w) = k\,\frac{w\,(1 + w^2)}{(1 + aw^2)(1 + w^2/a)} \quad y_5(w) = w\,\frac{(a + w^2)(b + w^2)}{(1 + aw^2)(1 + bw^2)} \quad \ldots.$$

leaving the coefficients to be determined.

In the maximally flat approximation case, complete analytical solutions are exist for all orders of n.



N th order maximally flat approximation :

$$y_n(w) = \text{tanhntanh}^{-1}w = \frac{(1+w)^n-(1-w)^n}{(1+w)^n+(1-w)^n}$$

or

$$\frac{1-y_n(w)}{1+y_n(w)} = \left(\frac{1-w}{1+w}\right)^n$$

Expanding some of them,

$$y_1(w) = w \qquad y_2(w) = \frac{2w}{1+w^2} \qquad y_3(w) = \frac{w(3+w^2)}{1+3w^2} \qquad y_4(w) = \frac{4w(1+w^2)}{1+6w^2+w^4}$$

$$y_5(w) = \frac{w(w^4+10w^2+5)}{1+10w^2+5w^4} \qquad y_6(w) = \frac{2w\ (3+10w^2+3w^4)}{1+15w^2+15w^4+w^6}$$

If we define the limits of frequency band as before, phase error around nominal

value, β_o, as δ_m, and setting $\beta_o = 90^o$, we get

$$\beta(w) = \beta_2(w) - \beta_1(w) \quad ; \sqrt{k} \leq w \leq \frac{1}{\sqrt{k}}$$

$$y(w) = \tan\left[\frac{1}{2}\beta(w)\right] \quad ; \quad \beta(w = \sqrt{k}^{\pm 1}) = \beta_o - \delta_m$$

$$y_{min} \triangleq y(w)\Big|_{w=(\sqrt{k})^{\pm 1}} = \tan\frac{1}{2}(\beta_o - \delta_m) = \frac{\tan(\beta_o/2) - \tan(\delta m/2)}{1 + \tan(\beta_o/2).\tan(\delta m/2)}$$

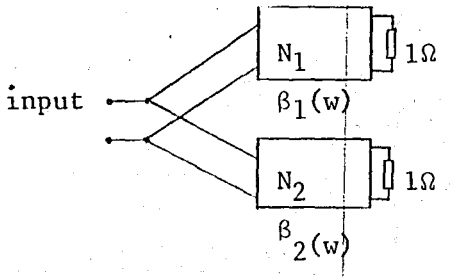
Finally:

$$y_{min} = \frac{1-\tan(\delta m/2)}{1+\tan(\delta m/2)} \quad ; \quad \text{or,} \quad \tan(\delta m/2) = \frac{1 - y_{min}}{1 + y_{min}}$$

Hence, for any given two quantities the third one can be found from.

$$\tanh^{-1} y_{min} = n \tanh^{-1}\sqrt{k}$$

In the equiripple Tchebycheff approximation case, simple algebric solutions are obtained only for nonprime values of n, otherwise algebric theory becomes difficult and in this case, eliptic function theory has to be used. Even, when the algebric theory is simple to apply, tables has to be used and this subject is left to |23|.



Determination of factorized network functions from a given general

phase expression, $y(w) = \tan [\beta(w)/2]$:

Since, $y(w) = \tan (\beta/2)$, is an odd rational function of w, it can be expressed as

$$y(w) = \tan (\beta/2) = \frac{w\, N(-w^2)}{M(-w^2)} \quad *$$

Hence

$$(\beta/2) = \arg \{ M(-w^2) + jw\, N(-w^2) \}$$

For the network shown, the final phase difference function can be expressed in terms of phase functions of network 1 and network 2 as

$$-(\beta_1/2) = \arg [M_1(-w^2) - jw\, N_1(-w^2)]$$

$$(\beta/2) = (\beta_2 - \beta_1)/2 = \arg \{ [M_2(-w^2) + jw\, N_2(-w^2)] . [M_1(-w^2) - jw\, N_1(-w^2)] \}$$

so, we have

$$M(-w^2) + jw\, N(-w^2) \triangleq [M_2(-w^2) + jw\, N_2(-w^2)] . [M_1(-w^2) - jw\, N_1(-w^2)]$$

When $y(w)$ is prescribed, $M(-w^2) + jw\, N(-w^2)$ is readly found. The promlem then, is to factor it into product of two polynomials (last expression), such that corresponding phase characteristics wN_2/M_2, wN_1/m_1 are physical.

* *Recalling the properties of the all-pass filter transfer function, H(s) such a definition is more realistic, since*

$$H(s) = \frac{p(-s)}{p(s)} \quad , \quad p(s) = M(s^2) + s \cdot N(s^2)$$

$$\text{so} \qquad H(jw) = \frac{M(-w^2) - jwN(-w^2)}{M(-w^2) + jwN(-w^2)}$$

A theorem states that [20]; w.N/M is realizeable as the impedance of two terminal network whenever N and M are even polynomials in s with real coefficients, such that $M(s^2) + sN(s^2)$ has no root on the right half s plane.

From the theorem and evenness property of the polynomials (M,N), it follows that $\frac{s\hat{N}(s^2)}{\hat{M}(s^2)}$ is also an impedance function of a physical network, whenever $\hat{M}(s^2)-s\hat{N}(s^2) = \tilde{M}((-s^2))-s\tilde{N}((-s^2))$ has no roots on the left half s plane.

The factorization procedure is then as follows:

1). Replace w by (s/j), in the given phase expression

$$y(w) = \frac{w\,N(-w^2)}{M(-w^2)} \Longrightarrow M(-w^2)+jw\,N(-w^2)\Big|_{w=s/j} = M(s^2)+sN(s^2) \triangleq p(s)$$

where p(s) has real coefficients, since $M(s^2)$ and $N(s^2)$ have.

2). Determine all the roots of p(s). For maximally flat case, roots are simply found from the expression

$$s_k = -\tan\left[\frac{\pi}{n}.\left(\frac{1}{4}+k\right)\right] \quad ; \; k = 0,1, \ldots, n-1$$

n= order of the appraximation.

3). Assign all the positive real part roots to the factor

$$M_1(s^2) - sN_1(s^2)$$

and all the negative real part roots to the factor

$$M_2(s^2) + sN_2(s^2)$$

4). Realize both network independently as tandem connected first order or second order lattice networks.

Notes:1). For the first network, actual roots are found just reversing the sign of the associated roots.

2). For single negative real part root, $-p(p>0)$ we have

$$H(s) = \frac{1-s/p}{1+s/p} \triangleq \frac{1-as}{1+as} \qquad -\tan\beta/2 = \frac{w}{p} \triangleq aw \quad ; \quad a \triangleq \frac{1}{p}$$

For negative real part complex root pair, $-\alpha \pm \beta \quad (\alpha, \beta > 0)$

$$H(s) = \frac{(s-\alpha+j\beta)(s-\alpha-j\beta)}{(s+\alpha-j\beta)(s+\alpha+j\beta)} = \frac{s^2(\frac{1}{\alpha^2+\beta^2})-s(\frac{2\alpha}{\alpha^2+\beta^2})+1}{s^2(\frac{1}{\alpha^2+\beta^2})+s(\frac{2\alpha}{\alpha^2+\beta^2})+1} \triangleq \frac{1-as+bs^2}{1+as+bs^2}$$

$$-\tan\beta/2 = \frac{2\alpha w}{\alpha^2+\beta^2-w^2} = \frac{(\frac{2\alpha}{\alpha^2+\beta^2})\,w}{1-w^2/(\alpha^2+\beta^2)} \triangleq \frac{aw}{1-bw} \quad ; \quad b \triangleq \frac{1}{\alpha^2+\beta^2}, \; a \triangleq 2\alpha.b$$

A given example will clarify the theory and will be used in system. $n \triangleq 2$; This simplest structure has still satisfactory performance, for instance, its 5^o phase error band at f_o=140 MHz is 113 MHz-173 MHz= 60 MHz.

$$\tan(\beta/2) = y_2(w) = \frac{2w}{1+w^2}$$

Design steps are :

1) $N(-w^2) = 2$ $\quad\}\quad p(s) = M(s^2) + sN(s^2) = -(s^2-2s-1)$

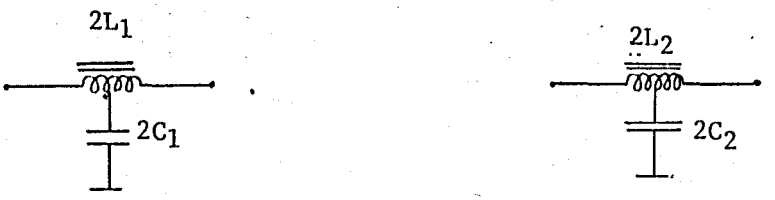
$M(-w^2) = Hw^2$

2) $S_{1,2} = -\tan\left[\frac{\pi}{2}\left(\frac{1}{4}+k\right)\right]$ $\quad k = 0,1 \Longrightarrow S_2 = (\sqrt{2}-1) \triangleq -\frac{1}{a_2}$

$$S_1 = (\sqrt{2}+1) \triangleq \frac{1}{a_1}$$

3,4) $H_1(s) = \frac{1-a_1 s}{1-a_2 s}$ $\qquad H_2 = \frac{1-a_2 s}{1-a_2 s}$

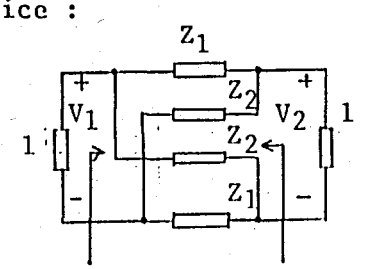
5) Realization :



$L_1 = C_1 = a_1 = \frac{1}{\sqrt{2}+1}$ $\qquad L_2 = C_2 = a_2 = \frac{1}{\sqrt{2}-1}$

QUICK REVIEW OF LATTICE NETWORKS

General, symetric lattice :

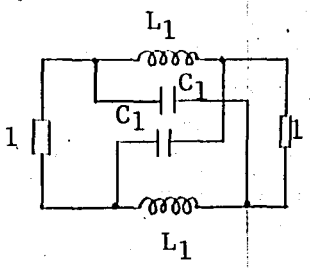


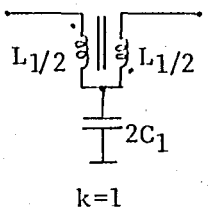
$Z_1 . Z_2 = 1$

$\tan(\gamma/2) = Z_1 = \frac{1}{Z_2}$; $\frac{V_1(s)}{V_2(s)} = e^{\gamma(s)}$; $\gamma(s) = \alpha(s)+j\beta(s) \triangleq j\beta(s)$

$$\tan(\beta/2) = \frac{Z_1}{j} = \frac{1}{jZ_2}$$

First order section :



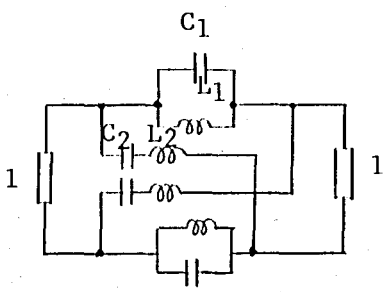


$$H(s) = \frac{1-as}{1+as}$$

$$\tan(\beta/2) = aw = wL_1 = wC_1$$

$$C_1 = L_1 = a$$

Second order section :



$$H(s) = \frac{1 - as + bs^2}{1 + as + bs^2}$$

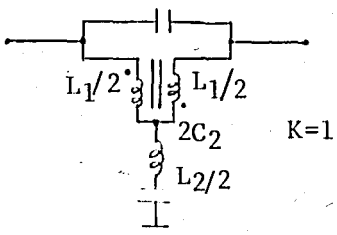
$$\tan(\beta/2) = \frac{aw}{1-bw^2} = \frac{wL_1}{1-w^2L_1C_1} = \frac{w\,C_2}{1-w^2L_2C_2}$$

$$L_1 = C_2 = a$$

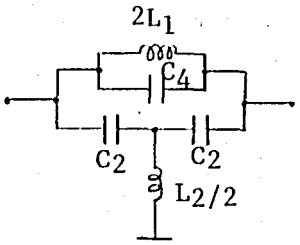
$$L_2 = C_1 = \frac{b}{a}$$

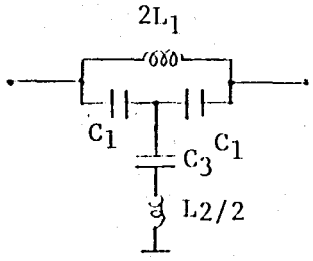
Equivalent circuits of second order section $C_1/2$

$(\frac{a^2}{b}) \geq 1$



$0 < (\frac{a^2}{b}) < 1$





$$C_4 = \frac{1}{2}(C_1 - C_2) = \frac{b}{2a}\left(1 - \frac{a^2}{b}\right) \qquad C_3 = \frac{2C_1 \cdot C_2}{C_1 - C_2} = \frac{2a}{1 - a^2/b}$$

Two first order section to one second order transformation.

$$H_1 = \frac{1 - a_1 s}{1 + a_1 s} \quad ; \quad H_2 = \frac{1 - a_2 s}{1 + a_2 s} \quad ; \quad H(s) = \frac{1 - as + bs^2}{1 - as + bs^2}$$

$$H \triangleq H_1 . H_2$$

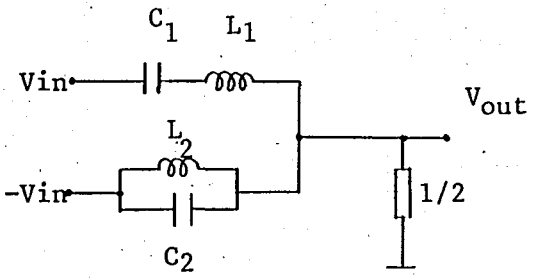
$$H = \frac{1 - (a_1 + a_2)s + a_1 . a_2 s^2}{1 + (a_1 + a_2)s + a_1 . a_2 s^2}$$

$$\Longrightarrow \quad a = a_1 + a_2$$

$$b = a_1 + a_2$$

Useful half lattice networks |22|;

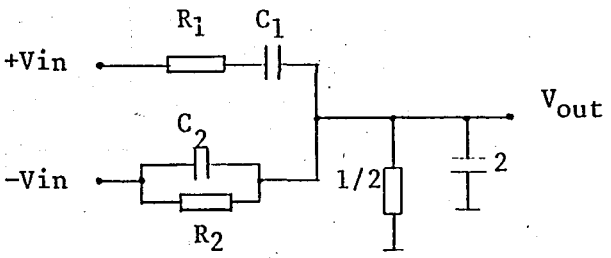
$$H(s) = k.\frac{1 - as + s^2}{1 + as + s^2} = \frac{V_o(s)}{V_{IN}(s)}$$



$$k = \frac{1}{2}$$

$$L_1 = C_2 = \frac{1}{a}$$

$$L_2 = C_1 = a$$



$$a = \left(\frac{R_2}{R_1} - 2\right) = \left(\frac{1}{R_2} + 2\right)$$

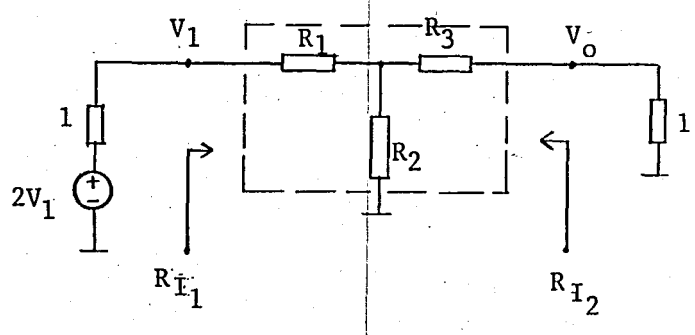
$$R_1C_1 = R_2C_2 = 1$$

$$k = \frac{a-2}{a+2}$$

$$C_1 = a^2 - 4$$

$$C_2 = a - 2$$

B - III. RESISTIVE POWER SUMMERS AND SPILITTERS.



The design formulas for symetric ($R_{I_1} = R_{I_2} = 1$) 'T' network attenuator having attenuation, α

$$\alpha = \ell n \left(\frac{V_1}{V_o}\right) = \ell nn ; \frac{V_1}{V_o} \triangleq n \quad ; \quad n = \text{integer} \geq 2$$

are

$$R_3 = R_1 = \frac{\cosh\alpha - 1}{\sinh\alpha} = \left(\frac{n-1}{n+1}\right)$$

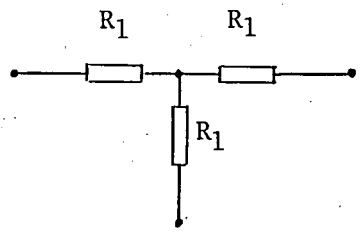
$$R_2 = \frac{1}{\sinh\alpha} = \frac{2n}{(h-1)(n+1)} = \frac{R_1+1}{n-1}$$

So, we see that, R_2 is a (n-1) parallel connected R_1 resistor having termination into 1Ω.

Hence for any two different port* and when N=2, we have

* *Unused port must be terminated into* 1Ω.

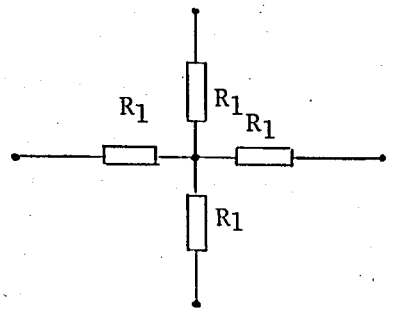
$$\frac{P_{out}}{P_{in}} = \left(\frac{V_{out}}{V_{in}}\right)^2 = \frac{1}{n^2} = \frac{1}{4}$$



$$R_1 = \frac{n-1}{n+1} = \frac{1}{3}$$

For n = 3

$$\frac{P_{out}}{P_{in}} = \frac{1}{n^2} = \frac{1}{9}$$



$$R_1 = \frac{n-1}{n+1} = \frac{1}{2}$$

REFERENCES*

1. J.G. Proakis, "Digital Communications," McGraw - Hill Book Comp., 1983 (BU)†

2. K. Feher, "Digital Communications", Prentice - Hall Inc., Englewood Cliffs, N.J., 1981 (BU)†

3. K.S. Shanmugam, "Digital and analog communication systems", John Willey and sons, 1979 (BU)†

4. G.D. Vendelin, "Design of amplifiers and oscillators by the s-parameter method", John Willey and sons, 1982 (MAE)

5. W.H. Froehner,"Quick amplifier design with scattering parameters", Electronics, pp.100-109; oct., 1967 (BU)

6. William R. Blood Jr, "MECL system design handbook", Motorola Inc., 1971 (MAE Physics department)

7. Clarke and Hess,"Communication circuits : Analysis and Design", Addison-Wesley publishing company, 1978. (BU)

8. W.F. Egan, "Frequency synthesis by phase lock, "John Willey and sons,1981(MAE)

9. "High Power transistor microwave oscillators", R.C.A., RF power transistors application note: AN-6084 (MAE)

** 1st, 2nd, 3rd sources are BU, ITU and MAE libraries respectively.*
† Not in library, course book.

10. "Microwave amplifiers and oscillators using the RCA - 2N 5470 power transistor", R.C.A., RF power transistors application note:AN-3764 (MAE)

11. K. Ogata, "Modern control engineering", Prentice - Hall Inc., Englewood Cliffs, N.J., 1970 (BU)

12. "UHF power generation using RF power transistors", R.C.A., RF power transistors application note : AN-3755 (MAE)

13. K.Feher, "A new symbol timing recovery tehcnique for burst modem applications", IEEE Trans. Communications, vol. com-26, No.1, pp.100-108; Jan., 1978. (BU)

14. K. Feher, "A digital approach to symbol timing recovery systems", IEEE Trans. communications, vol. Com-28, No.12, pp. 1993-1999; Dec., 1980 (BU)

15. M.K. Simon, "Optimum performance of suppressed carrier receivers with Costas loop tracking", IEEE Trans. Communications, vol. com-25 pp. 215-227, No.2, Feb., 1977 (BU)

16. C.R. Cahn, "Improving frequency acquisition of a Costas loop", IEEE Trans. communications, vol-com-25, pp. 1453-1459; Dec., 1977 (BU)

17. M.K. Simon, "Optimum receiver structures for phase-multiplexed modulations", IEEE Trans-communications, vol. com-26, No.6, pp. 865-872, 1978 (BU)

18. C.L. Weber, "Demod-remod coherent tracking receiver for QPSK and SQPSK", IEEE Trans. communications, vol-com-26, No.12,pp 1945-1953; Dec., 1980 (BU)

19. C.L. Weber, "Performance analysis of demod-remod coherent receiver for QPSK and SQPSK input", IEEE Trans. Communications, Vol. com-286, No.12,. pp. 1954-1993; Dec., 1980 (BU)

20. S. Darlington, "Realization of Constant phase difference", Bell Sys. Tech. Jour., vol. XX1X, pp. 94-104; Jan., 1950 (ITU)

21. R.B. Dome, "Wideband phase shift networks", Electronics, Vol. 19, pp. 112-115, Dec., 1946 (ITU)

22. D.G.C. Luck, "Properties of some wideband phase-spilitting networks", PROC. I.R.E., vol. 37, pp. 147-151, Feb., 1949 (BU)

23. W. Saraga, "The design of wideband phase spilitting networks", PROC. I.R.E., vol. 38, pp. 754-770; July, 1950. (BU)

24. D.K. Weaver, "Design of RC wideband 90-degree phase-difference networks", PROC. I.R.E., pp. 671-676; April, 1954 (BU)

25. J.D. Rhodes, "Theory of electrical filters, "John Willey and sons, 1976 (MAE)

26. Lam, Harry Y-F., "Analog and digital filters", Prentice-Hall, Inc., Englewood Cliffs, N.J, 1979 (BU)

PLUG-IN DOUBLE-BALANCED MIXERS

MLLF-3, 20 kHz-65 MHz
MLF-3, 200 kHz-200 MHz
MHF-3, 5 MHz-500 MHz

- 20 kHz to 500 MHz Coverage
- High Isolation

Guaranteed Specifications *

(From -55°C to +85°C)

MLLF-3		
Frequency Range:		
RF, LO Ports		0.02-65 MHz
IF Port		DC-65 MHz
Conversion Loss:		
0.02-65 MHz		6.5 dB Max
Isolation:		
LO to RF	(0.02 - 1 MHz)	45 dB Min
	(1-65 MHz)	40 dB Min
LO to IF	(0.02-1 MHz)	45 dB Min
	(1-65 MHz)	35 dB Min
RF to IF	(0.01-1 MHz)	40 dB Min
	(1-65 MHz)	25 dB Min
MLF-3		
Frequency Range:		
RF, LO Ports		0.2-200 MHz
IF Port		DC-200 MHz
Conversion Loss:		
0.2-50 MHz		6 dB Max
50-200 MHz		7.5 dB Max
Isolation:		
LO to RF	(0.2-50 MHz)	35 dB Min
	(50-200 MHz)	30 dB Min
LO to IF	(0.2-50 MHz)	35 dB Min
	(50-200 MHz)	25 dB Min
RF to IF	(0.2-50 MHz)	25 dB Min
	(50-200 MHz)	20 dB Min
MHF -3		
Frequency Range:		
RF, LO Ports		5-500 MHz
IF Port		DC-500 MHz
Conversion Loss:		
5-150 MHz		7 dB Max
150-500 MHz		9 dB Max
Isolation:		
LO to RF	(5-150 MHz)	40 dB Min
	(150-500 MHz)	35 dB Min
LO to IF	(5-150 MHz)	35 dB Min
	(150-500 MHz)	25 dB Min
RF to IF	(5-150 MHz)	30 dB Min
	(150-500 MHz)	25 dB Min

Operating Characteristics

Impedance:	50 Ohms Nominal
Maximum Input:	
Total Power	400 mW Max @25°C
	Derated to 85°C @3.2 mw/°C
IF Port Current	50 mA Max
DC Polarity:	Positive
DC Offset:	
MLLF-3	2 mV Typical
MLF-3	1 mV Typical
MHF-3	1 mV Typical
RF Input for 1 dB Compression:	+4.5 dBm Typical
MLLF-3 @ RF = 30 MHz	
MLF-3 @ RF = 100 MHz	
MHF-3 @ RF = 200 MHz	
RF Input for 1 dB Desensitization:	+2 dBm Typical
MLLF-3 @ RF = 30 MHz	
MLF-3 @ RF = 100 MHz	
MHF-3 @ RF = 200 MHz	
SSB Noise Figure:	Within 1 dB of Conversion Loss
Typical Two-Tone IM Ratio: (with -10 dBm input, each input, 30 MHz and 35 MHz IF)	
	MLLF-3 @ 50 MHz ≥49 dB
	MLF-3 & MHF-3 @ 200 MHz ≥46 dB

*All specifications apply when operated at +7 dBm available LO power, with 50 ohm source and load impedance.

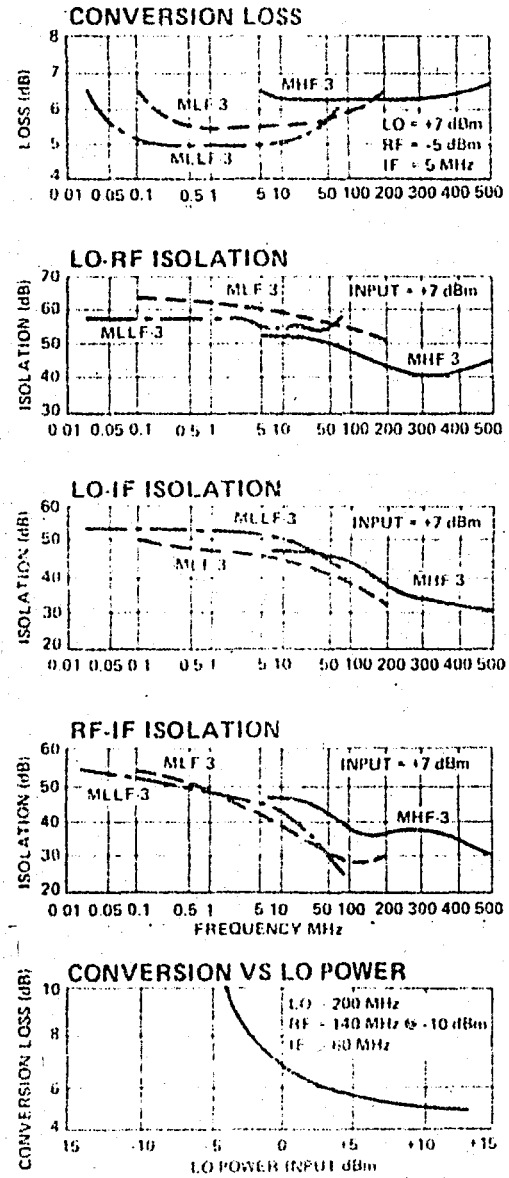
Adams Russell ANZAC . . . the qualitative difference

This unit has been designed to meet or exceed the following environmental criteria:

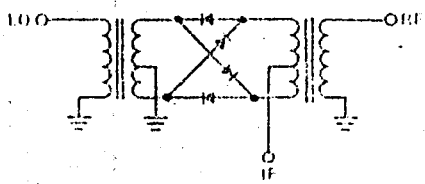
Governing Document: MIL-STD-202E		
Test	Method	Condition
Visual Inspection	Anzac Workmanship Manual	
Mechanical Inspection	Device Outline Dwg.	
Thermal Shock	107	A
Moisture Resistance	106	

Specific device testing to these and other environmental tests is available at additional cost.

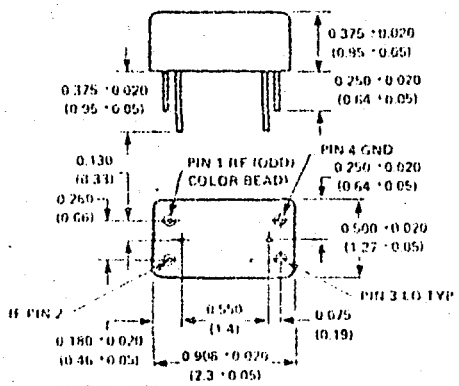
Typical Performance



Schematic



Mechanical Data



UNLESS OTHERWISE NOTED, XXX = ±0.010 ±(.X = ±0.3) PIN DIAMETER = .017 +.003 (.01 +.008)

WEIGHT (APPROX.) 0.23 OUNCES 6.5 GRAMS
*DIMENSIONS IN ( ) ARE IN MM

FINISH: CASE - ELECTROPLATED TIN PER MIL-T-17027
COVER - NICKEL SILVER PER QQ-C-585 1
LEADS: WELDABLE AND SOLDERABLE PER MIL-STD-1276B

Ordering Information

MODEL NO.	PART NO.	UNIT PRICE (1-100 UNITS)
MLLF-3	9529	$55
MLF-3	9289	55
MHF-3	9299	55

Delivery is from stock.

80 Cambridge Street, Burlington, Mass. 01803 (617) 273-3333 TWX 710 • 332 • 0258

BIPHASE MODULATOR

10-750 MHz

- Phase Deviation 1° Typical
- TO-8 Case

Guaranteed Specifications*

(From -55°C to +85°C)

Frequency Range:	10-750 MHz
Insertion Loss:	
10-500 MHz	3.0 dB Max
10-750 MHz	3.5 dB Max
VSWR:	
50-500 MHz	1.3:1 Max
10-750 MHz	1.6:1 Max
Amplitude Balance:	0.2 dB Max
Phase Deviation:	
10-500 MHz	2° Max
10-750MHz	3° Max

Operating Characteristics

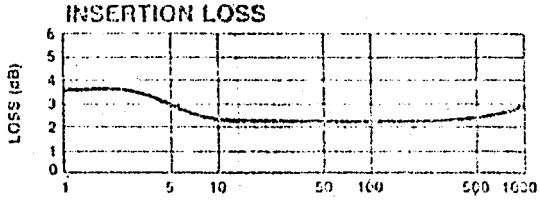
Impedance:	50 Ohms Nominal
RF Input Level:	+ 17 dBm Max
Carrier Suppression: (100 MHz RF, 1 MHz Modulation)	35 dB Typ
Control Input:	
Logic 1	+ 10 mA Drive Current
Logic 0	– 10 mA Drive Current

PHASE STATE	LOGIC STATE	
	D1	D2
0°	1	0
+ 180°	0	1

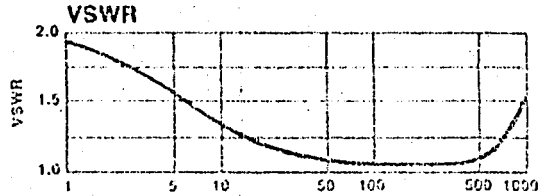
*All specifications apply with 50 ohm source and load impedance and inputs to –3 dBm.

Typical Performance

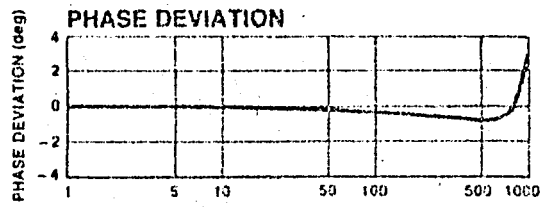
INSERTION LOSS



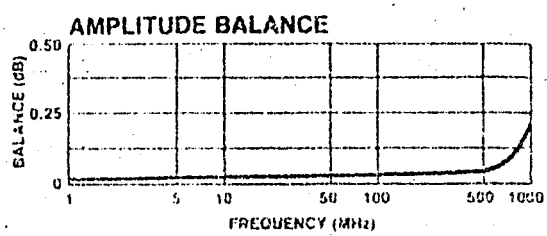
VSWR



PHASE DEVIATION



AMPLITUDE BALANCE



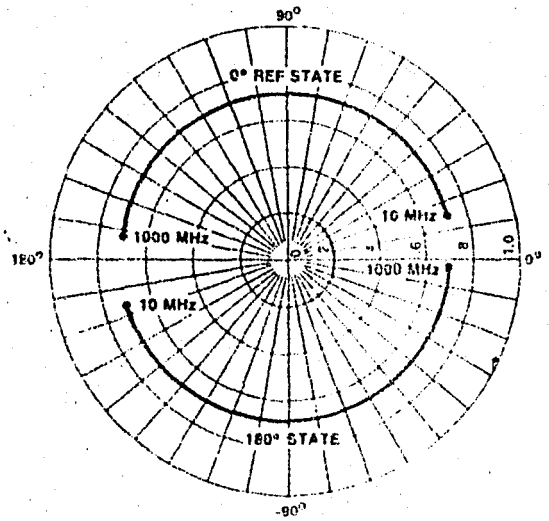
Adams Russell ANZAC . . . the qualitative difference

This unit has been designed to meet or exceed the test requirements of MIL-STD-883B, Method 5008 for hybrid microcircuits modified as follows:

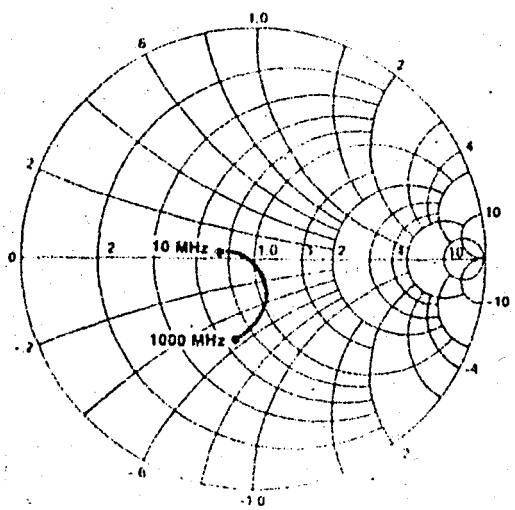
Stabilization Bake	Condition B
Temperature Cycle	Condition B
Burn-in	85 °C
Seal, Fine	5 x 10⁻⁸ atm cc/sec.

Specific device testing to these and other environmental tests is available at additional cost.

Typical Performance

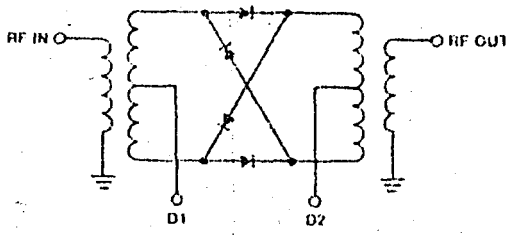


TRANSMISSION LOSS & PHASE

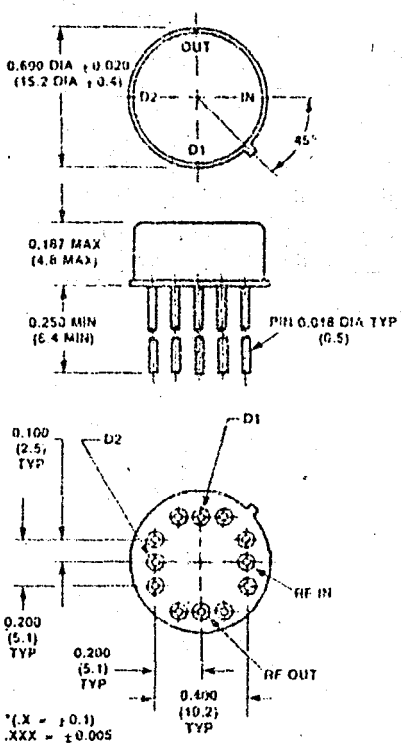


IMPEDANCE BOTH PORTS

Schematic



Mechanical Data



*(.X = ±0.1)
.XXX = ±0.005

*DIMENSIONS IN ( ) ARE IN MM
PINS NOT MARKED ARE GROUND

FINISH: CASE-GOLD ELECTROPLATED PER MIL-G-45204 TYPE 1, CLASS 1
COVER-NICKEL, GRADE A
LEADS: WELDABLE AND SOLDERABLE PER MIL-STD-1276B CLASS 1

Ordering Information

MODEL NO.	PART NO.	UNIT PRICE (1-5 UNITS)
PM-101	9089	$100

Delivery is from stock.

80 Cambridge Street, Burlington, Mass. 01803 (617) 273-3333 TWX 710 • 332 • 0258

U 250 B

			Min.	Typ.	Max.	
Frequenzbereich *Frequency range* ΔU_q = −3 dB, Verstärkerstufe *Amplifier stage*	Fig. 1					
A_1	Pin 6	f_{g1}	17		250	kHz
A_2	Pin 11	f_{g2}	10		250	kHz
Ausgangsstrom *Output current*						
Verstärkerstufe A_1, A_2 *Amplifier stage*	Pin 6, 11	I_Q	210	300	480	µA
Filterstufe a, b, c, d *Filter stage*	Pin 8, 10, 16, 13	I_Q	70,7	1	1,6	mA
Eingangsstrom Filterstufe *Input current filter stage* a, b, c, d	Pin 7, 9, 15, 14	I_I		1,5	2,3	µA
Grenzfrequenzen *Cut-off frequencies* ΔU_q = −3 dB untere/*lower*	Fig. 1	f_{ga}	29	32		kHz
obere/*upper*		f_{gb}		404	43	kHz
Sperrverhalten Fig. 1, Pin 11, f = 10 kHz		$-\Delta U_q$		17		dB
f = 100 kHz		$-\Delta U_q$		35		dB

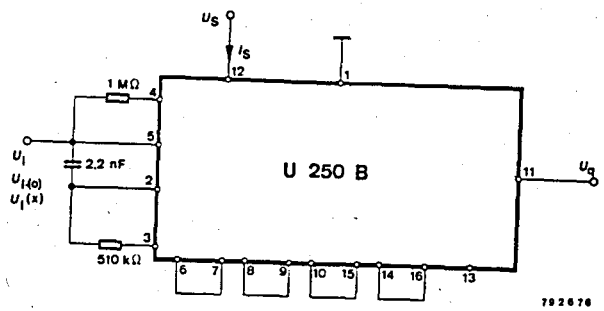


Fig. 2 Meßschaltung
Test circuit

U 264

Monolithisch Integrierte Schaltung
Monolithic Integrated Circuit

Anwendung: 1-GHz-Frequenzteiler für Frequenzsynthese in FS-Tunern
Application: *1 GHz frequency divider for frequency synthesizers in TV-tuners*

Besondere Merkmale:

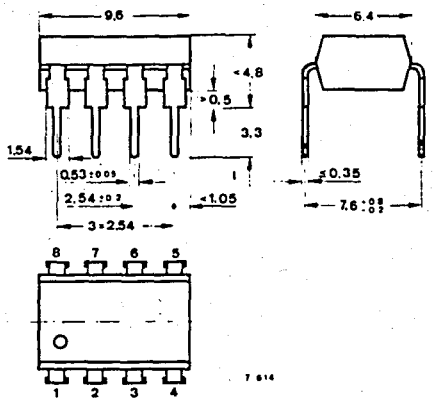
- Hohe Eingangsempfindlichkeit
- Großer nutzbarer Frequenzbereich
- Übersteuerungsfester Eingang
- Hohe dynamische Stabilität
- Geringer Leistungsbedarf
- Großer Versorgungsspannungsbereich
- Geringer Schaltungsaufwand

Features:

- *High input sensitivity*
- *Large operation frequency range*
- *Large signal compatibility*
- *High dynamic stability*
- *Low power dissipation*
- *Wide supply voltage range*
- *Few external components*

Vorläufige technische Daten · *Preliminary specifications*

Abmessungen in mm
Dimensions in mm



Kunststoffgeh
Plastic
20 A 8 DIN 4
DIP 8-
Gewicht · *W*
max.

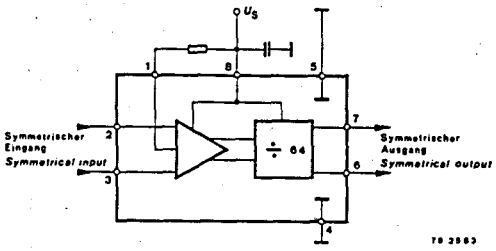


Fig. 1 Blockschaltbild und Anschlußbelegung
Block diagram and pin connections

1 Eingangs-Symmetrie-Einstellung
Input balance adjustment
2+3 Differentialeingänge mit interner Vorspannung
Differential inputs with internal bias voltage
4+5 Masse, Bezugspunkt
Earth, reference point
6+7 Differentialausgänge
Differential outputs
8 U_S

Bemerkungen:

Um Schwingneigungen des Teilers ohne Eingangssignal sicher zu unterdrücken, wird der Breitbandverstärker auf geringfügige Unsymmetrie eingestellt. (Widerstand zwischen Pin 1 und U_S).
Der IC ist für eine Betriebsspannung von U_S = 5 V optimiert, die Empfindlichkeit ändert sich aber im gesamten Betriebsspannungsbereich nur unwesentlich. Es ist jedoch eventuell erforderlich, bei $U_S \leq 4{,}5$ V den Widerstand R_1 zu verkleinern.

Notes:

To avoid oscillation of the frequency divider without input signal, the wide band preamplifier is adjusted to a slight unbalanced bias (resistor between Pin 1 and U_S).

The IC is optimised for supply voltage of U_S = 5 V. The sensitivity changes slightly throughout the supply voltage range.

It may be useful in case of $U_S \leq 4.5$ V to reduce resistor R_1.

Absolute Grenzdaten
Absolute maximum ratings

Bezugspunkt Pin 4+5
Reference point 4+5

Versorgungsspannung *Supply voltage*	Pin 8	U_S	6	V
Eingangsspannungsbereich *Input voltage range*	Pin 2, 3	U_i	0...U_S	V
Verlustleistung *Power dissipation*				
t_{amb} = 55 °C		P_{tot}	600	mW
t_{amb} = 70 °C		P_{tot}	550	mW
t_{amb} = 85 °C		P_{tot}	400	mW

Sperrschichttemperatur *Junction temperature*	t_j	125	
Umgebungstemperaturbereich *Ambient temperature range*	t_{amb}	0...85	
Lagerungstemperaturbereich *Storage temperature range*	t_{stg}	−25...+125	

Wärmewiderstand
Thermal resistance

		Min.	Typ.	Max.
Sperrschicht-Umgebung *Junction ambient*	R_{thJA}			100

Elektrische Kenngrößen
Electrical characteristics

U_S = 5 V, t_{amb} = 25 °C, Bezugspunkt Pin 4+5, Fig. 2
Reference point Pin 4+5

			Min.	Typ.	Max.
Versorgungsspannungsbereich *Supply voltage range*	Pin 8	U_S	4,0	5,0	6,0
Versorgungsstrom *Supply current*	Pin 8				
U_S = 4 V		I_S		50	
U_S = 5 V		I_S		65	
U_S = 6 V		I_S		85	
Eingangsempfindlichkeit *Input sensitivity* R_G = 50 Ω	Pin 2	U_i		5	10
Übersteuerungsfestigkeit *Large signal compatibility* R_G = 50 Ω	Pin 2	U_i	500		
Frequenzbereich *Frequency range*		f_i	10		1000
Differentielle Ausgangsspannung *Differential output voltage*		U_{qd}		1,5	

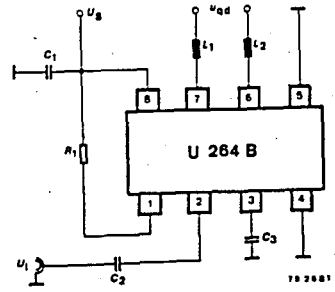
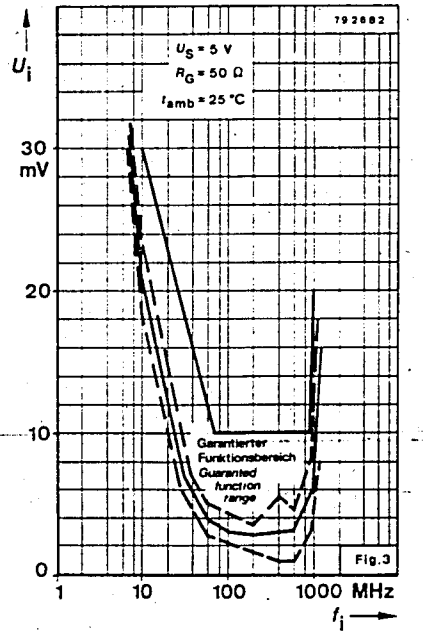
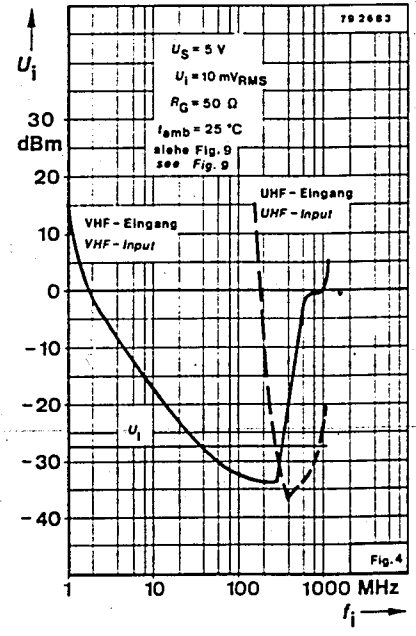
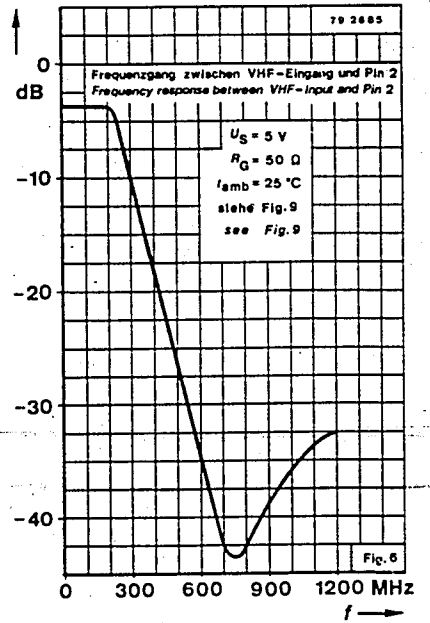


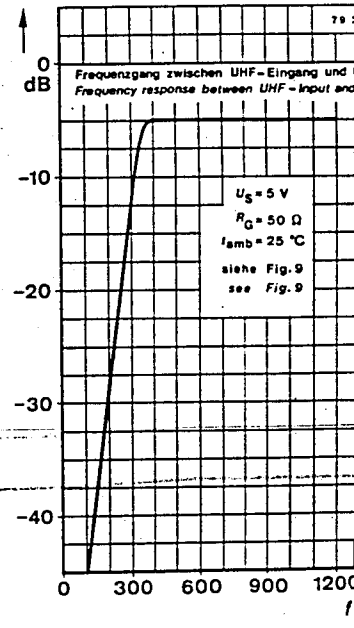
Fig. 2 Meßschaltung

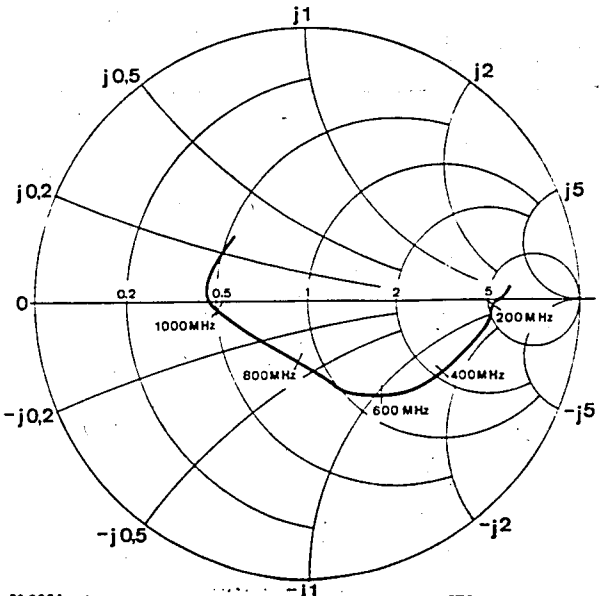
$L_1 = L_2 \approx 150$ nH – 6 Wdg ⌀ 0,45 CuL auf/







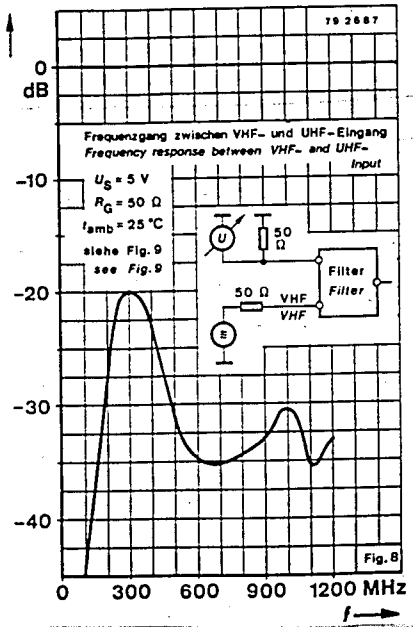




Eingangswiderstand R_i
Input resistance

U_S = 5 V
Z_L = 50 Ω
f = 200...1000 MHz
t_{amb} = 25 °C
siehe Fig. 2
see Fig. 2

Fig. 2



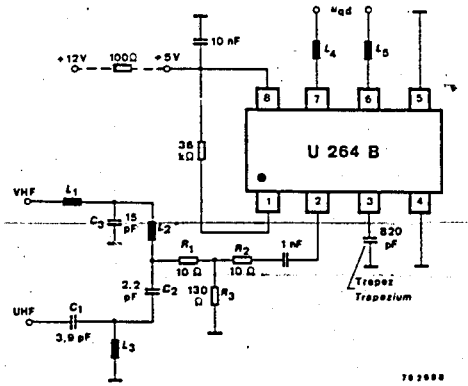
U 264 B

Anwendungsbeispiel:

Vor dem Teiler wird eine Frequenzweiche für VHF/UHF und ein Dämpfungsglied zur resonanzfreien Anpassung geschaltet.
Empfindlichkeit und Filtercharakteristik siehe Fig. 5...8.

Application note:

In front of the divider IC a frequency selecting VHF/UHF filter and an attenuator for non resonant input matching is located.
For sensitivity and filter characteristic, see Fig. 5...8.



$L_1 = L_3$ 20 nH –3 Wdg ø 0,45 CuL auf/*on* ø 2,5
L_2 40 nH –5 Wdg ø 0,45 CuL auf/*on* ø 2,5
$L_4 = L_5$ 150 nH –6 Wdg ø 0,45 CuL auf/*on* ø 4

Fig. 9 Eingangsteiler für Frequenzsynthese in FS-Tunern
Input divider for frequency synthesiser in TV-tuners

U 353

Monolithisch integrierte Schaltung
Monolithic integrated circuit

N-Kanal-Si-Gate-Technologie
N-Channel-Si-Gate-Technology

Anwendung: Niederohmiges Schalterpaar für leistungsloses Umschalten von Signalquelle bis 10 MHz

Application: *Low ohmic pair of powerless controlled switches for signal sources up to 10*

Besondere Merkmale:

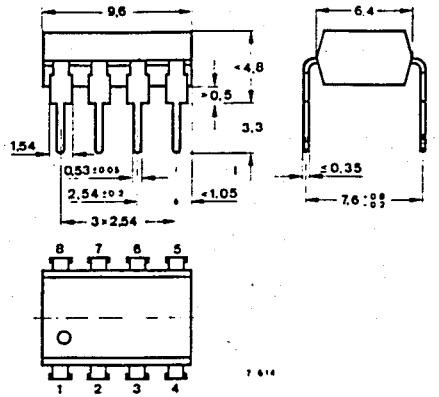
- Widerstand im „Ein"-Zustand ≦ 5 Ω
- Kleine Kapazitäten
- Integrierte Schutzeinrichtung für die Steuerelektroden
- Leistungslose Ansteuerung

Features:

- *On-state resistance ≦ 5 Ω*
- *Low capacitances*
- *Protected gates*
- *Wattless control*

Vorläufige technische Daten · *Preliminary specifications*

Abmessungen
Dimensions



Kunststoffgeh
Plastic
DIP 8-
DIP 8
Gewicht · *W*
ma

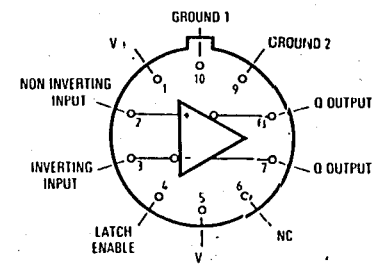
SP9685

ULTRA FAST COMPARATOR

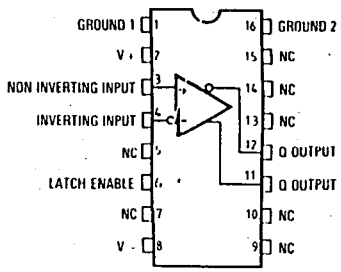
The SP9685 is an ultra-fast comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50 Ω terminated transmission lines. The high resolution available makes the device ideally suited to analogue-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used, the latch enable may be connected to ground.

The device is pin compatible with the AM685 but operates from conventional +5V and −5.2V rails.



CM10



DC16

DG16

On metal package, pin 5 is connected to case. On DIP pin 8 is connected to case

Fig. 1 Pin connections

FEATURES

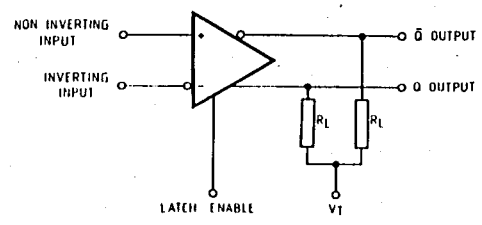
- Propagation Delay 2.2ns typ.
- Latch Set-up Time 1ns max.
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- Pin Compatible with AM685 – But Faster

QUICK REFERENCE DATA

- Supply voltages +5V, −5.2V
- Operating temperature range −30°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	6V
Negative supply voltage	−6V
Output current	30mA
Input voltage	±5V
Differential input voltage	±5V
Power dissipation	300mW
Storage	−55°C to +150°C
Lead temperature (soldering 60 sec)	300°C



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0V or 200–2000Ω connected to −5.2V

Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{AMB} = 25°C$
$V_{CC} = +5.0V \pm .25V$
$V_{EE} = -5.2V \pm .25V$
$R_L = 50\,\Omega$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−5		+5	mV	Rs <100 Ω
Input bias current		10	20	μA	
Input offset current			5	μA	
Supply currents Icc		19	23	mA	
IEE		23	34	mA	
Total power dissipation		210	300	mW	
Min. latch set-up time		0.5	1	ns	
Input to Q output delay		2.2	3	ns	100 mV pulse 10 mV overdrive
Input to $\bar{Q}$ output delay		2.2	3	ns	
Latch to Q delay		2.5	3	ns	
Latch to $\bar{Q}$ delay		2.5	3	ns	
Min. latch pulse width		2	3	ns	
Min. hold time			1	ns	
Common mode range	−2.5		+2.5	V	
Input capacitance		3		pF	
Input resistance	60			kΩ	
Output logic levels					
Output High	− .96		− .81	V	At nominal supply
Output Low	−1.85		−1.65	V	voltages, see Fig. 4
Common mode rejection ratio	80			dB	
Supply voltage rejection ratio	60			dB	

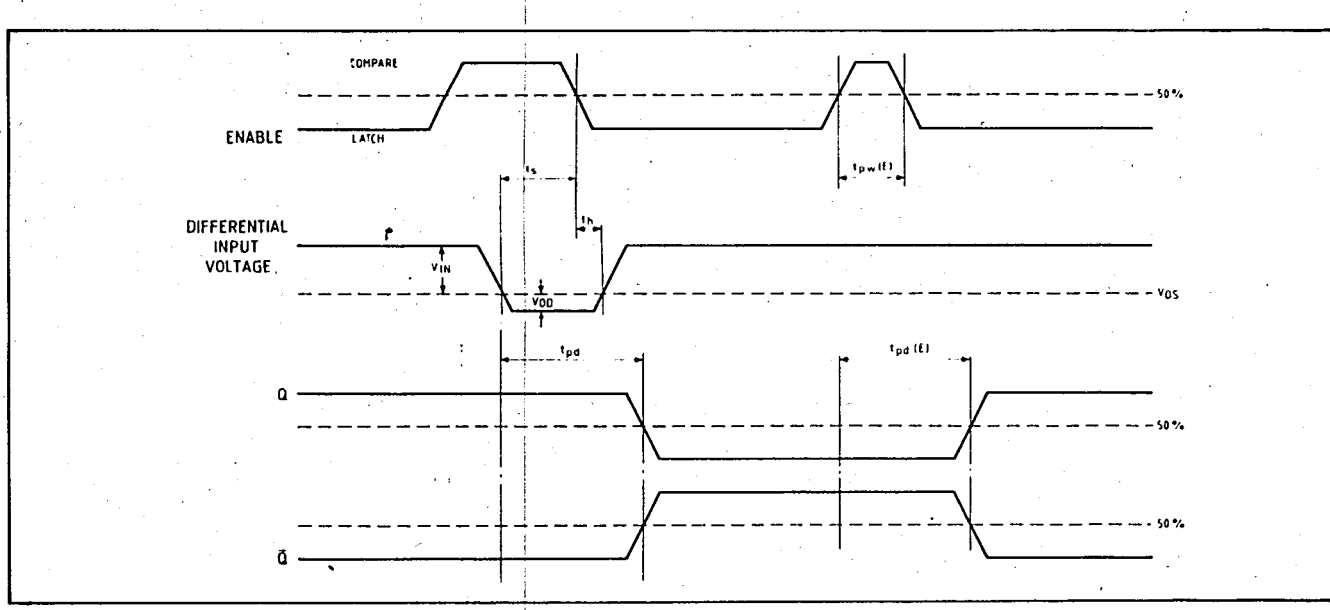


Fig. 3 Timing diagram

OPERATING NOTES

Timing diagram

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time tpd. Output Q and $\bar{Q}$ transitions are essentially similar in timing. The inpu signal must occur at a time t_s before the latch fallin edge, and must be maintained for a time t_h after th latch falling edge, in order to be acquired. After t_h, th output ignores the input status until the latch is aga strobed. A minimum latch pulse with $t_{pw(E)}$ is require for the strobe operation, and the output transition occur after a time $t_{pd(E)}$.

Definition of terms

Vos Input offset voltage – The potential differenc required between the input terminals to obta zero output potential difference.

Ios Input offset current – The difference betwee

the currents into the inputs when there is zero potential difference between the outputs.

Switching terms (refer to Fig. 3)

t_{pd+} Input to output high delay – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} Input to output low delay – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ Latch enable to output high delay – The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ Latch enable to output low delay – The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transistion to the 50% point of an output HIGH to LOW transition.

t_s Minimum set-up time – The minimum time before the negative transition of the latch enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h The minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ Minimum latch enable pulse width – The minimum time that the latch enable signal must be HIGH in order to acquire and hold an input signal change.

V_{CM} Input voltage range – The range of input voltages for which the offset and propagation delay specifications are valid.

CMRR Common mode rejection ratio – The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Latched and unlatched gain

The gain of a high speed, high gain comparator is difficult to measure, because of input noise and the possibility of oscillations when in the linear region. For a full ECL output level swing, the unlatched input shift required is approximately 1mV. In the latched mode, the feedback action in effect enhances the gain and the limitation between the noise/oscillation level; under these conditions the usable resolution is 100µV, although this is only achieved by careful circuit design and layout.

Interconnection techniques

High speed components in general need special precautions in circuit board design to achieve optimum system performance. The SP 9685, with around 50 dB gain at 200MHz, should be provided with a ground plane having a low inductance ground return. All lead lengths should be as short as possible, and RF decoupling capacitors should be mounted close to the supply pins. In most applications, it will be found to be necessary to solder the device directly into the circuit board. The output lines should be designed as microstrip transmission lines backed by the ground plane with a characteristic impedance between 50Ω and 150Ω. Terminations to –2V, or Thevenin equivalents, should be used.

Measurement of propagation and latch delays

A simple test circuit is shown in Figure 4. The operating sequence is:

1. Power up and apply input and latch signals. Input 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.
3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

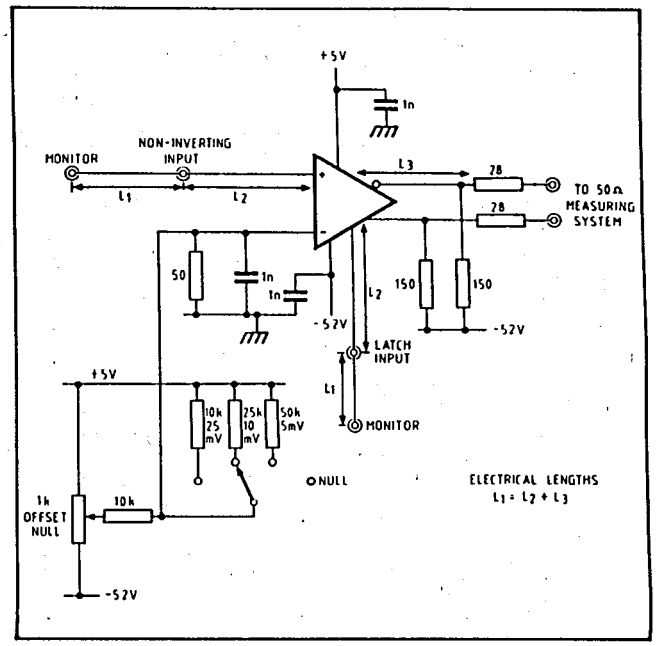


Fig. 4 SP9685 test circuit

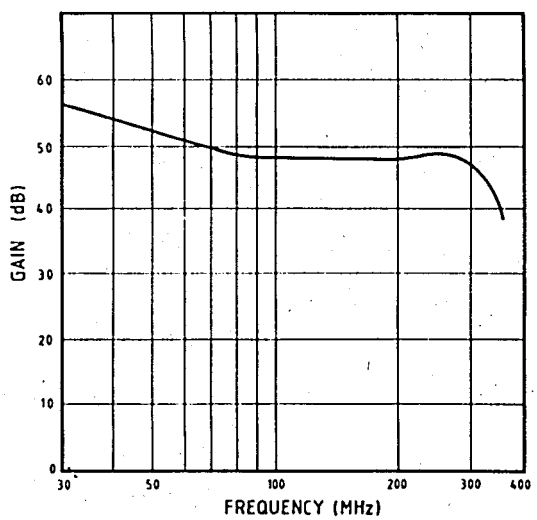


Fig. 5 Open loop gain as a function of frequency

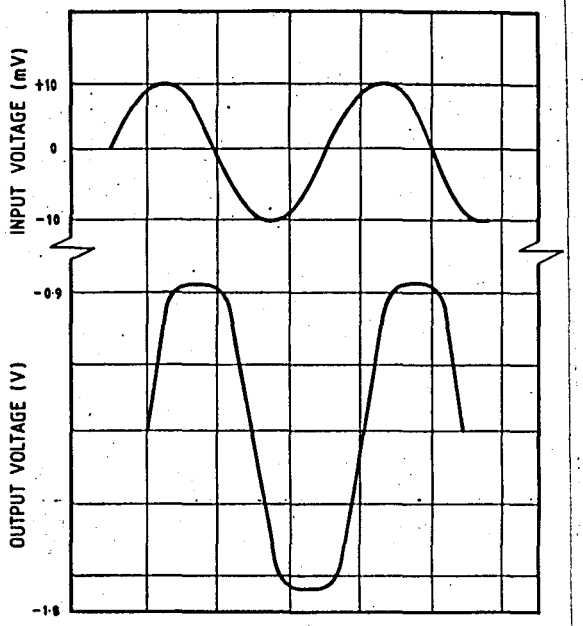


Fig. 6 Response to a 100MHz sine wave

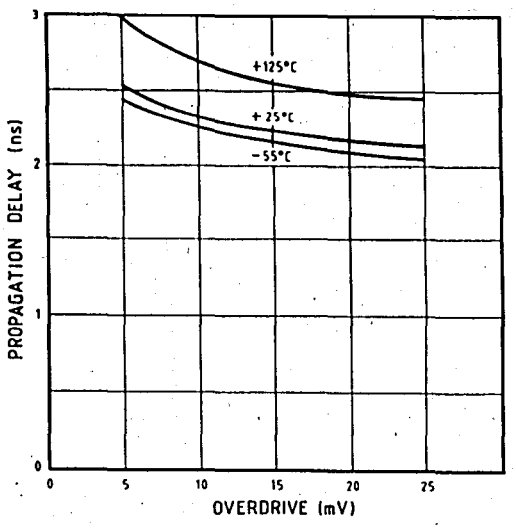


Fig. 7 Propagation delay, latch to output as a function of overdrive

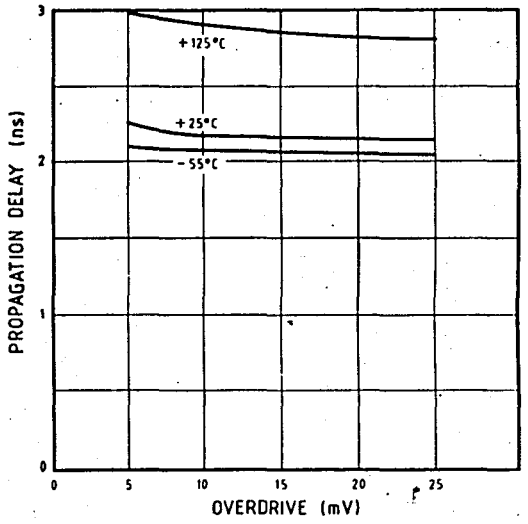


Fig. 8 Propagation delay, input to output as a function overdrive

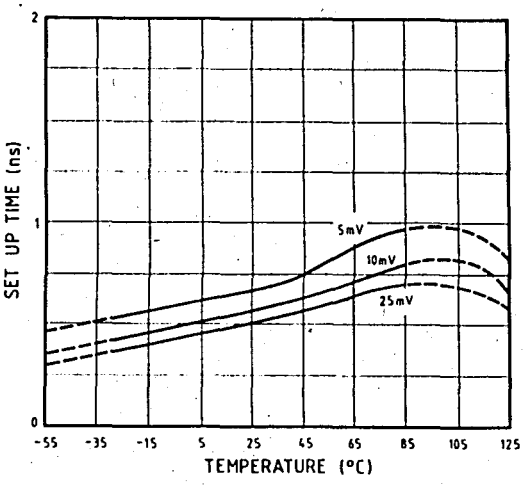


Fig. 9 Set-up time as a function of temperature

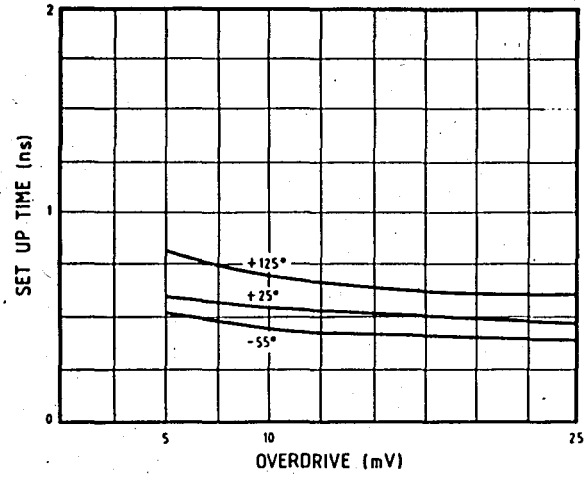


Fig. 10 Set-up time as a function of input overdrive

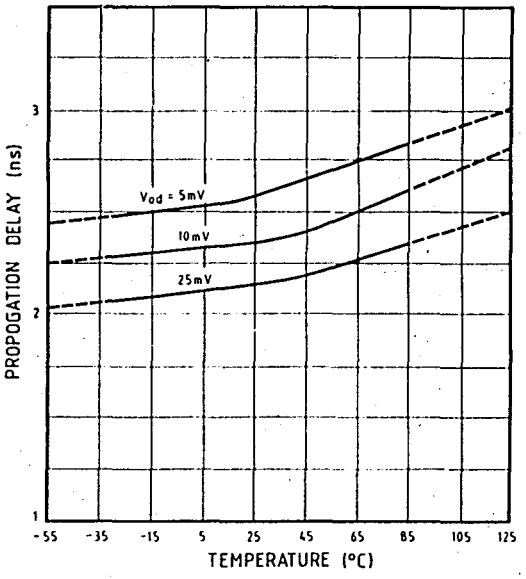


Fig. 11 Propagation delay, input to output as a function of temperature

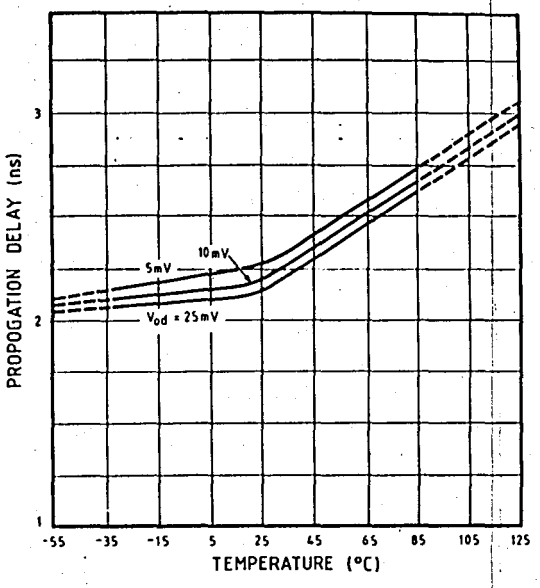


Fig. 12 Propagation delay, latch to output as a function of temperature

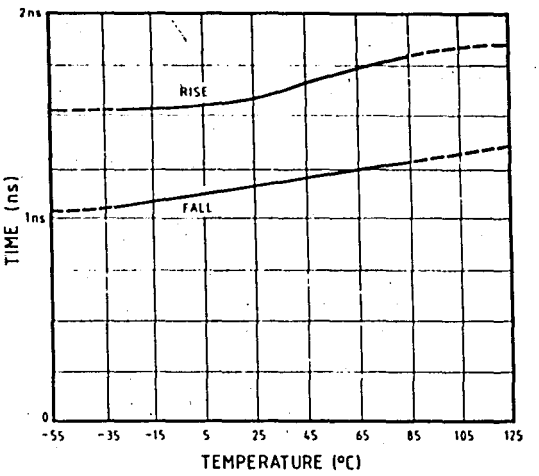


Fig. 13 Output rise and fall times as a function of temperatur

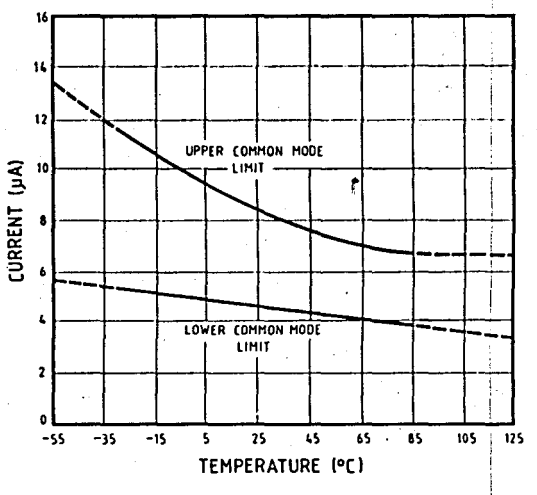


Fig. 14 Input bias currents as a function of temperature

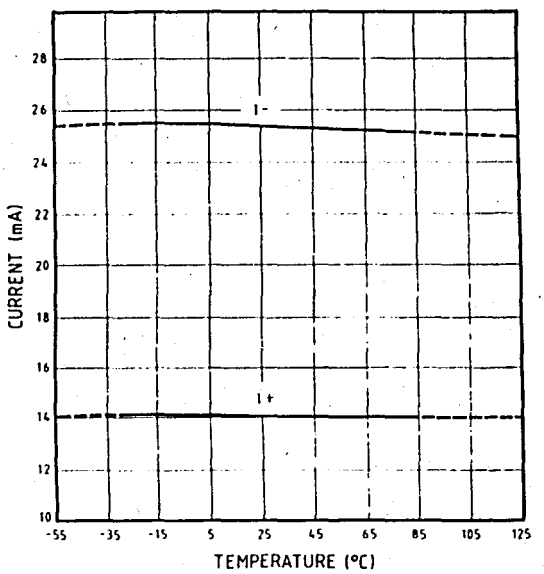


Fig. 15 Supply current as a function of temperature

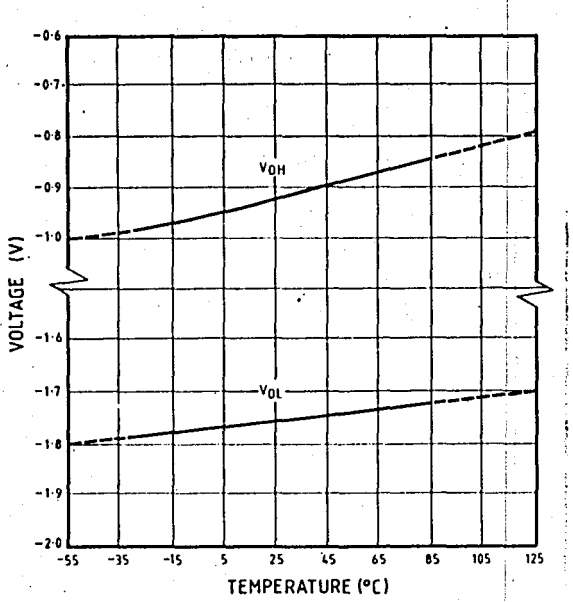


Fig. 16 Output levels as a function of temperature

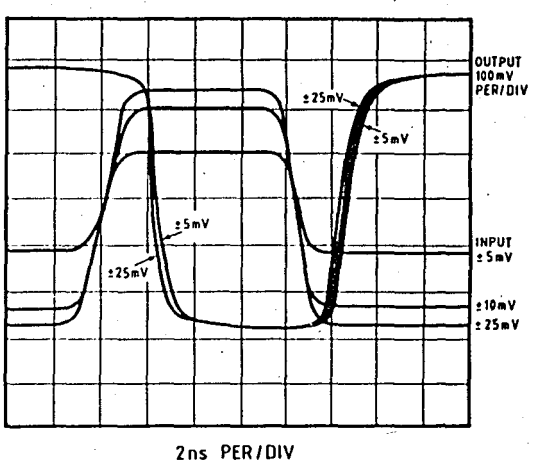


Fig. 17 Response to various input signal levels

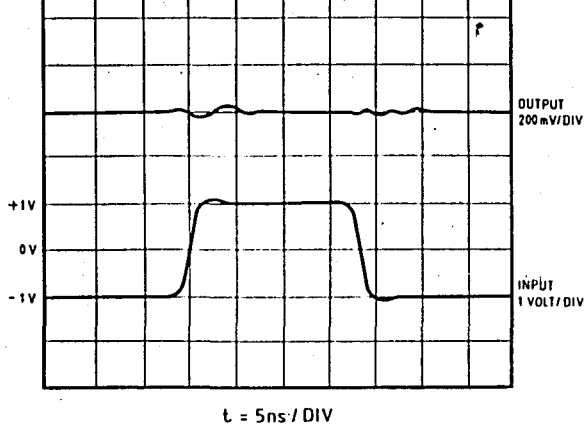
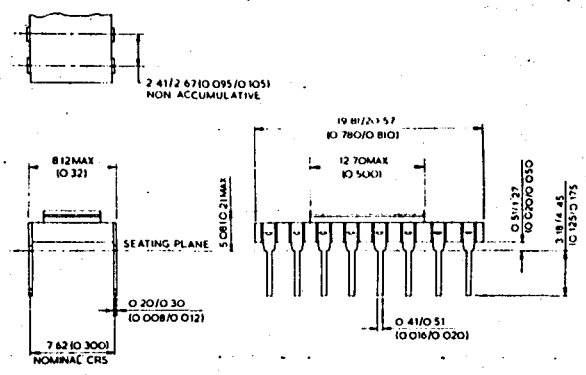


Fig. 18 Common mode pulse response

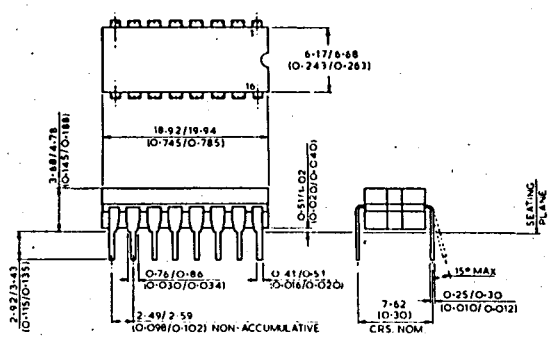
PACKAGE DETAILS

Dimensions are shown thus: mm (in)



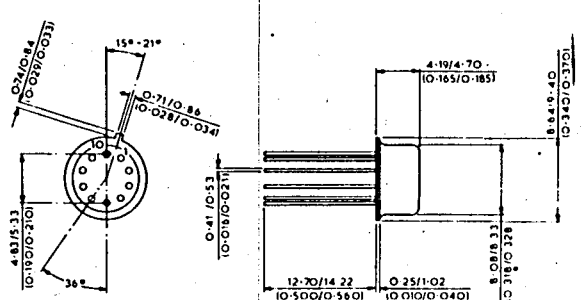
16 LEAD DILMON

DC16



16 LEAD CERAMIC D.I.L.

DG16



10 LEAD TO-5

CM10