PRECISE POWER CONTROL ON TIME AXIS

by

Rıfkı YAPAKÇI

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APPROVED BY

Doç. Dr. Okyay KAYNAK

Doç. Dr. Oğuz TOSUN

Y. Doç. Dr. Ömer CERİD

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ABSTRACT

The object of this thesis is to design and realize a versatile microcomputer system and apply it to the precise control of electrical power.

The specific application of this system as presented in the thesis is to control the temperature of a liquid on time axis by controlling the power of a heater unit according to specific requirements. Other possible applications could be chemical reactions that require precise temperature control or experiments that have to be realized under specific temperature conditions. These requirements can be fulfilled by automatic control means most safely. A microcomputer based system is the optimum way of doing this.

In this thesis, the design and the implementation of a microcomputer based temperature control system is presented. The main blocks of the system are a microcomputer an instrumentation amplifier and a digital firing angle control circuit. The system realised operated satisfactorily enabling the control of temperature on time axis with a 0.25 ^{o}C resolution.

ÖZETÇE

Bu tezin amacı, elastik yapıda bir mikrobilgisayar tasarımlayarak bunu elektrik gücün hassas bir şekilde kontrolüne uygulamaktır.

Tezde sunulan bu sistemin özel uygulama alanı, bir ısıtıcı ünitenin gücünün kontrol edilerek, bir sıvının ısısının özel gereksinimlere göre kontrol edilmesidir. Diğer uygulama alanları, hassas ısı kontrolü gerektiren kimyasal reaksiyonlar veya özel ısı koşulları gerektiren deneyler olabilir. Bu gereksinimler ancak otomatik kontrol vasıtasıyla en emin bir şekilde karşılanabilirler. Bir mikrobilgisayar sistemi bu sorunların çözümünde en uygun araçtır.

Bu tezde, mikrobilgisayar tabanlı bir ısı kontrol sistemi tasarımlanarak gerçekleştirilmiştir. Bir mikrobilgisayar bir araçsal yükseltici ve bir sayısal tetikleme devresi sistemin ana yapı taşlarını oluşturmaktadır. Sistem, zaman ekseninde 0.25 ^{o}C hassasiyetle kontrolü sağlayarak, tatmin edici bir şekilde çalışmıştır.

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CHAPTER I

INTRODUCTION

Control of power is an important area in electronics. Until microprocessors become available, analog and hardwired digital control methods were usually used to control power.

Microprocessors and other micro chips contributed a new dimension to power control units. By using this new technology power can be controlled precisely on time, according to the programme written into the system. Of course this is a very important development because of the fact that it gives very broad elasticity to control power.

Microcomputer systems are very efficient to control industrial processes. It has some advantages over analog control systems and TTL systems : Precise control can be achieved ; real time concept can be included easily; design and equipment cost decrease appreciably. In some industrial processes, it may be necessary to control environmental conditions. One of the important environmental condition is temperature. In this thesis, the design and the implementation of a microprocessor based system to control the temperature of the liquid in a tank is described.

CHAPTER 2

SYSTEM LAYOUT

1.1. Theory

Instantenous power, P, in an a.c. circuit may be expressed as:

$$P=V\cdot I=V_m \sin wt\cdot I_m \sin(wt+\emptyset) \qquad (2.1)$$

where,

V_m=Peak Value of the Voltage.

I_m=Peak Value of the Current.

wt=Angular Frequency.

$\emptyset$=Phase Difference between the Voltage and Current

Average power is given by,

$$Pav=\frac{1}{2} V_m I_m \cos\emptyset=V I \cos\emptyset \qquad (2.2)$$

where,$\cos\emptyset$ is called the power factor, V and I are the RMS values of voltage and the current respectively.

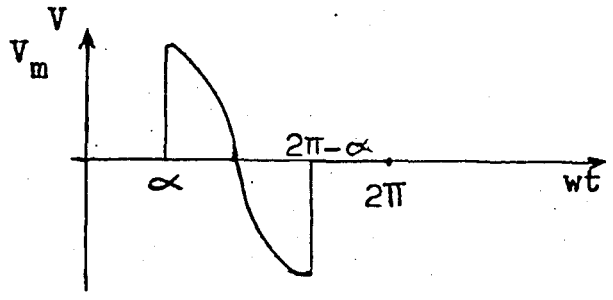


Figure 2.1.1 A Sinusoidal Voltage Waveform with a Delay Angle of

Referring to Figure 2.1.1 , the average power, as a function of delay angle, , can be expressed;

$$P_{av} = \frac{V_m I_m}{2\pi} \int_{\alpha}^{2\pi-\alpha} \sin wt \cdot \sin (wt \, \phi) \, dwt$$

$$= \frac{V_m I_m}{2\pi} \int_{\alpha}^{2\pi-\alpha} \frac{1}{2} (\cos \phi \cdot \cos(2wt+\phi)) \, dwt$$

$$= \frac{V_m I_m}{4\pi} \left(\cos \phi \int_{\alpha}^{2\pi-\alpha} dwt - \frac{1}{2} \sin(2wt+\phi) \Big|_{\alpha}^{2\pi-\alpha} \right)$$

$$= \frac{V_m I_m}{4\pi} \left(2 \cos\phi \, (\pi-\alpha) - \frac{1}{2} (\sin(\phi-2\alpha) \right.$$

$$\left. - \sin (2\alpha+\phi)) \right)$$

$$P_{av} = \frac{V_m I_m}{2} \cos\phi \, (\pi-\alpha) - \frac{1}{4} (\sin(\phi - 2\alpha)$$

$$- \sin(2 \, - \phi)) \qquad (2.3)$$

For a resistive circuit, that is ϕ is zero, average power is;

$$P_{av} = \frac{V_m I_m}{2\pi} \left((\pi - \alpha) - \frac{1}{2} \sin 2\alpha \right) \qquad (2.4)$$

In order to control a.c. power in an electrical circuit two ways can be adopted : Either phase angle of the a.c. waveform is controlled or the cycles of the waveform are controlled.

In this thesis, beeause of the precise power control, phase control for the power control is adopted. The EMI problem is encountered and tried to be suppressed.

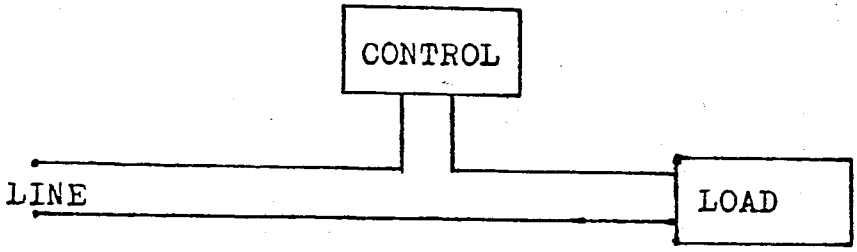
In order to understand the measures for suppression of EMI, characteristics of the interference must be explored first. To have interference at all, we must have a transmitter, a creator of interference and a receiver, a device affected by the interference. Common transmitters are opening and closing switches and relay contacts, all forms of electric and electronic circuits with rapidly changing voltages and currents. Receivers are generally electronic circuits both high and low impedance which are sensitive to pulse or high frequency energy. Often the very circuits generating the interference are sensitive to similar interference from outer circuits nearby or on the same power line.

EMI can generally be seperated into two categories radiated and conducted. Radiated interference travels by way of electromagnetic E and H waves just as desirable RF energy does. Conducted interference travels on power, communications or control wires.

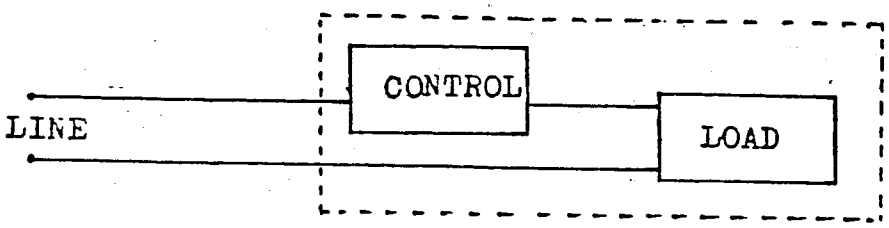
As it is seen the two are not seperate packages independently control is not possible. In any case both interference forms must be considered when interference elimination steps are taken.

Phase control circuits using thyristors and triacs are very offensive in creating EMI. These controls are gen erally connected in one of the two ways shown in Figure 2.1.2 a and b .

The circuits in Figure 2.1.2 may be re-drawn as shown in Figure 2.1.3 illustrating the complete circuit for RF energy.



a. Separately Mounted Control.



b. Control and Load are in the Same Enclosure

Figure 2.1.2 Two Methods in Phase Control Circuits.

The switch in the control box represents the thyristor shown in the blocking state. In phase control operation this switch is open at the beginning of each cycle of the power line alterations. After a delay, determined by the remainder of control circuitry, the switch is closed and remains that way until the instantenous current drops to zero. This switch is the source from which the RF energy flows down the power lines and through the various capacitors to ground.

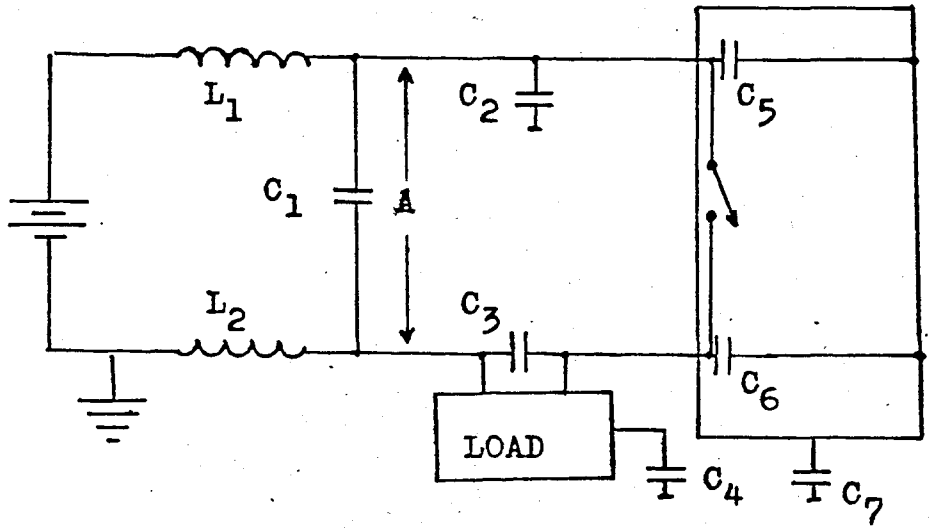


Figure 2.1.3 RF Energy Sources in Separately Mounted control.

If the load is passive such as a lamp or a motor which doesn't generate interference, it may be considered as an impedance by-passed with the wire to wire capacitance of its leads.

If it is another RF energy source, however such as a motor with a commutator, it must be treated separately to reduce interference form that source. The power source can be treated as d.c., as far as the high frequency interference pulses are considered. The inductance, associated with the power source, comes from two separate phenomena. First is the leakage impedance of supply transformer and second is the self inductance of the wires, between the power line transformer and the load.

One of the most difficult parameters to pin down in the system is the effect of grounding. Most industrial and commercial wiring and many homes use a grounded conduit

system which provides excellent shielding of radiated energy emanating from the wiring. However, a large number of homes are being wired by two or three wire insulated cable without conduit. The capacitances C_2, C_4 and C_7 to ground will be affected by the grounding system used.

Before the switch in the control is closed, the system is in steady state condition with the upper line of the power line at the system voltage and the bottom line and the load at the ground potential. When the switch is closed, the upper line potential instantenously falls due to the line and source inductance, then it rises back to its original value as the line inductance is charged.

While the upper line is rising, the line from control to the load also rises in potential. The effect of both of these line increasing in potential together, causes an electrostatic field change which radiates energy. In addition any other loads connected across the power lines, at point A for example, would be affected by a temporary loss of voltage created by the closing of switch and the line and source inductance. This is a form of conducted interference.

A second form of radiated interference is inductive coupling in which the power line and ground form a one turn primary of an air-core transformer. In this mode an unbalanced transient current flows down the power lines with the difference current flowing to the ground through the various capacitive paths available. This type of interference is a problem only when the receiver is within about one wavelength of the transmitter at the offending frequency.

Radiated interference from the control circuit is of little consequence due to several factors. The lead lengths are so short compared to the wavelength in question that they make extremely poor antenna. In addition most of

these control circuits are mounted in metal enclosures which provide shielding for radiated energy generated within the control circuitry.

Both forms of radiated interference which are results of conducted interference on the power lines are caused by rapid rise in current. Thus, if this current rise is slowed all forms of interference will be reduced.

When the switch closes it shows very low impedance. Since this reason, it will show very little benefit to put a parallel capacitance to the switch in slowing down the current. The capacitors will be charged to a voltage determined by the circuit constants and the phase angle of the line voltage just before the switch closes. When the switch closes the capacitor will discharge quickly, its current is limited only by its own resistance and the resistance of the switch. However a series inductor will slow down the current rise in the load and thus reduce voltage transients on all lines.

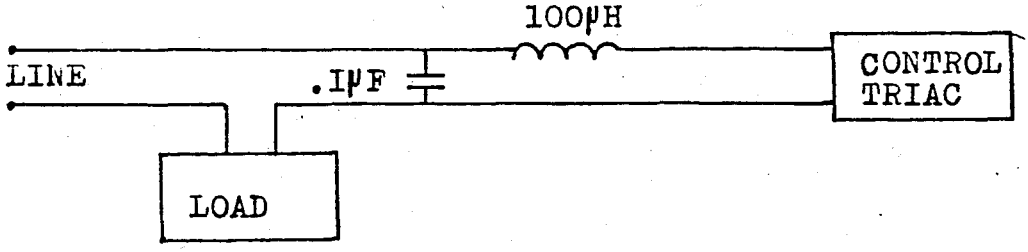


Figure 2.1.4 One Possible EMI Reduction Circuit.

Although the circuit of Figure 2.1.4 will be effective in many cases the filter is unbalanced, providing an RF current path through the capacitances to ground. It has, therefore, been found advantageous to divide the inductor into two parts and to put each half in each line to the control. Figure 2.1.5 illustrates this circuit showing the

polarity marks of the two coils which are wound on the same core.

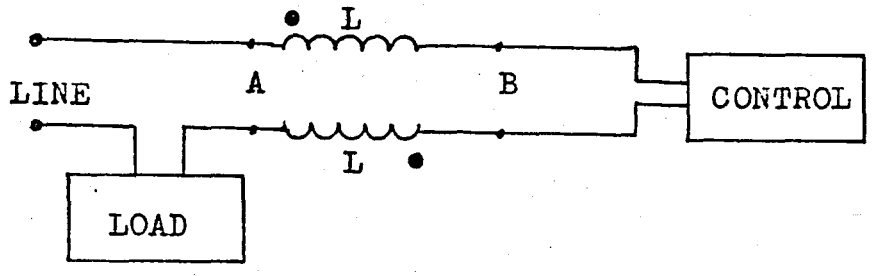


Figure 2.1.5 Split Inductor Circuit.

Where the control circuit is sensitive to fast rising line transients, a capacitor at point B will do much to eliminate this problem. The capacitor must charge through the impedance of the inductor, thus limiting the rate of voltage change (dv/dt) applied to the thyristor while it is in blocking state.

As mentioned above the EMI problem is the main disadvantage as far as the comparison between phase angle control and integral cycle control is made.

Integral cycle control is another a.c power control way. In this approach some cycles are inhibited to pass through the load. Gate triggering of thyristor or a triac occur at the zero crossings of the line waveform. Hence, no EMI problem comes out. But power control by this method is not as precise as phase angle control. The most precise proportion of the power that can be controlled by this method is one percent. Hence, despite the problem of EMI, for precise control ability the former way of control is adopted.

2.2. Operation of the System

This system described in this thesis was designed as versatile as possible. This is why it may be used for controlling other industrial processes. Specific application here is to control temperature inside a water tank.

To use the system, a temperature versus time diagram should be drawn as in Figure 2.2.1.

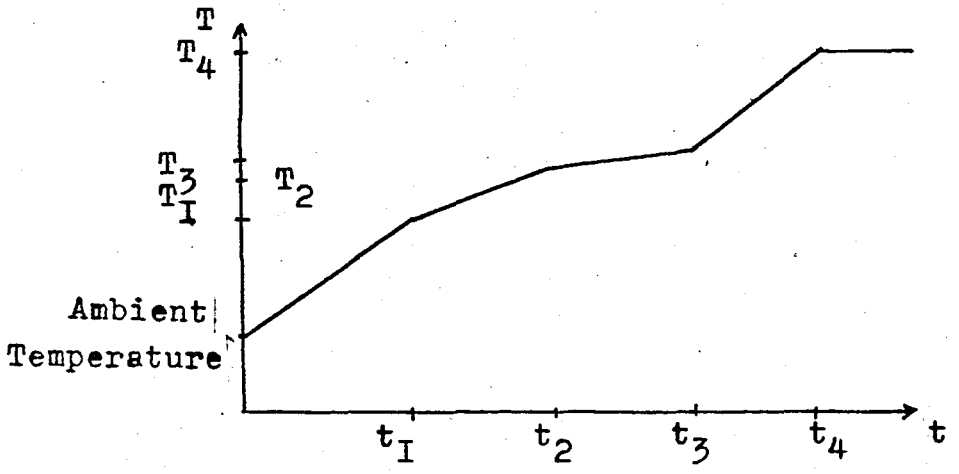


Figure 2.2.1 A Temperature versus Time Diagram.

This diagram is entered to the microcomputer by keyboard. If any of the data is given by mistake, it is possible to clean the wrong one and re-enter the true one. It is also possible to return to the beginning by resetting the system and change any one of temperature and time data pair at any time.

When entrance of data lasts RUN command is given and the time and the real temperature is displayed and the diagram is realized. The microcomputer controls the slope of the diagram. If any time there is a deviation from it the system takes necessary steps by changing firing angle to correct the slope.

The block diagram of the system is shown in Figure 2.2.2. The temperature sensed by PT100 probe is converted to differential signal by a bridge which is adjusted to give 0 V at 25°C. This differential signal is amplified by an instrumentation amplifier, to couple the signal to A/D converter. This amplified d.c signal is converted to digital signal by the A/D converter and becomes ready for being used by microcomputer.

The microcomputer gets this data and compare it with the data that should exist. If there is a deviation from the required value then it checks the required temperature slope. This deviation is compensated by changing the firing angle through the firing angle control circuitry.

Digital firing angle circuitry can control the firing angle with a resolution at 180°/256 0.703°. The input to this circuitry comes from the microcomputer, which produces the 8-bit firing angle data to the input of the Digital Firing Angle Control Circuit, consequently this data is converted to appropriate firing pulses. Firing pulses are generated in synchronization with the line frequency. These firing angle pulses are used to fire triac to control the power.

Display unit displays the data entered at programming stage. It also displays the real time and the real temperature inside the tank when the system runs. It consists of two three-digit sections. Three digits at the right hand si side displays the entered temperature data, and the real temperature when it runs. Three digits at the left hand side displays the entered time data and real time as hours and minutes when it runs.

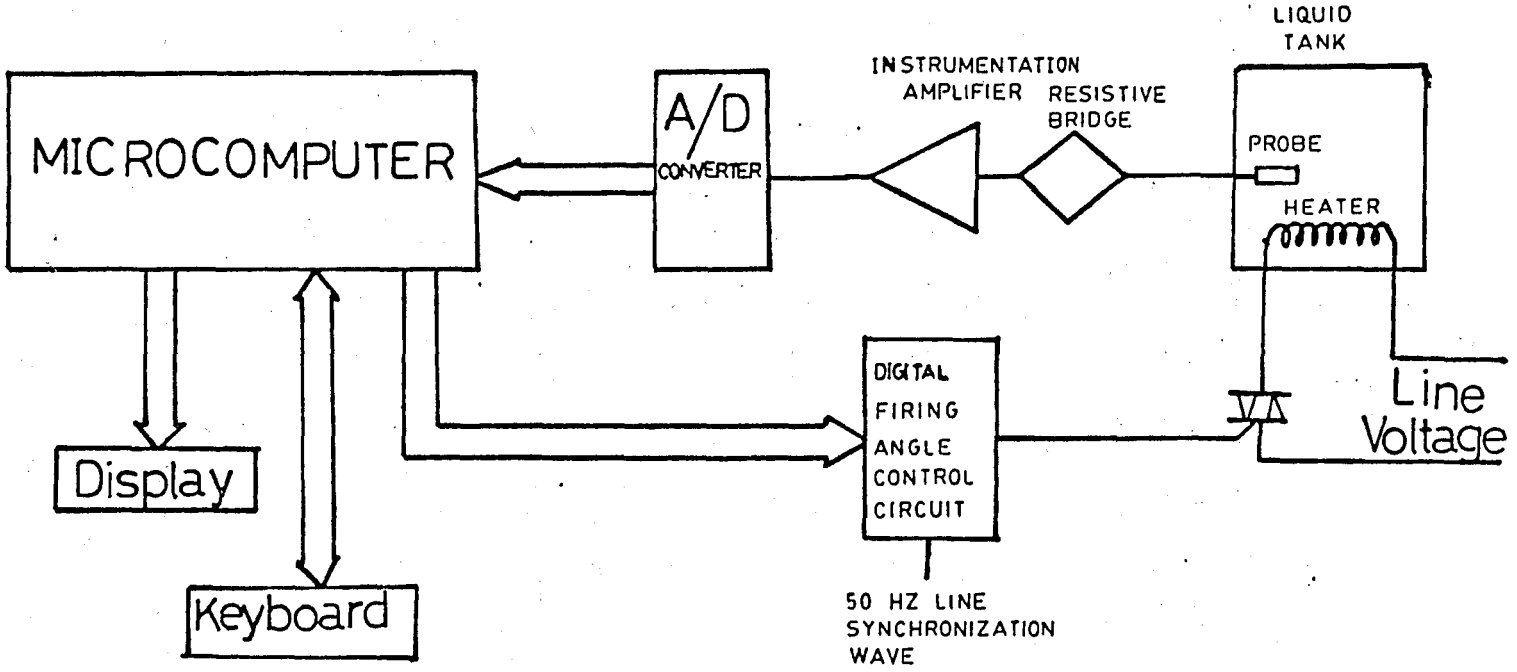


Figure 2.2.2 The Block Diagram of the System

CHAPTER III

MICROCOMPUTER

3.1. Microcomputer Operation

Microcomputer was designed as versatile as possible as shown in Figure 3.1. It can be used for many other purposes due to this property. It has an A/D converter to get and process analog signals. It can communicate with the outer world by using I/O ports of 8255 PPI (Programmable Peripheral Interface) in different modes.

The CPU used in microcomputer board is Zilog Z-80 which is one of the most suitable 8-bit microprocessors for control applications. Many software and hardware properties of Z-80 are used in this thesis. It runs at 1.79 MHz.

The monitor program which operates the system is embedded into 2716 EPROM which is 2Kx8 bit erasable programmable read only memory. The monitor program is given at Appendix B.

All the system variables and program data are stored into 6116 RAM which is 2Kx8 bit static random access memory. For the proper operation of the system some variables should be used. In addition, the data given to the system can be considered as program variables when the system runs. Staticness of the RAM doesn't necessitate any refresh operation.

Two 8255 PPIs, Programmable Peripheral Interface, are used in the microcomputer for interfacing the peripherals to the CPU. Each one of 8255 PPI has three-parallel I/O ports which can be used in three modes of operation.

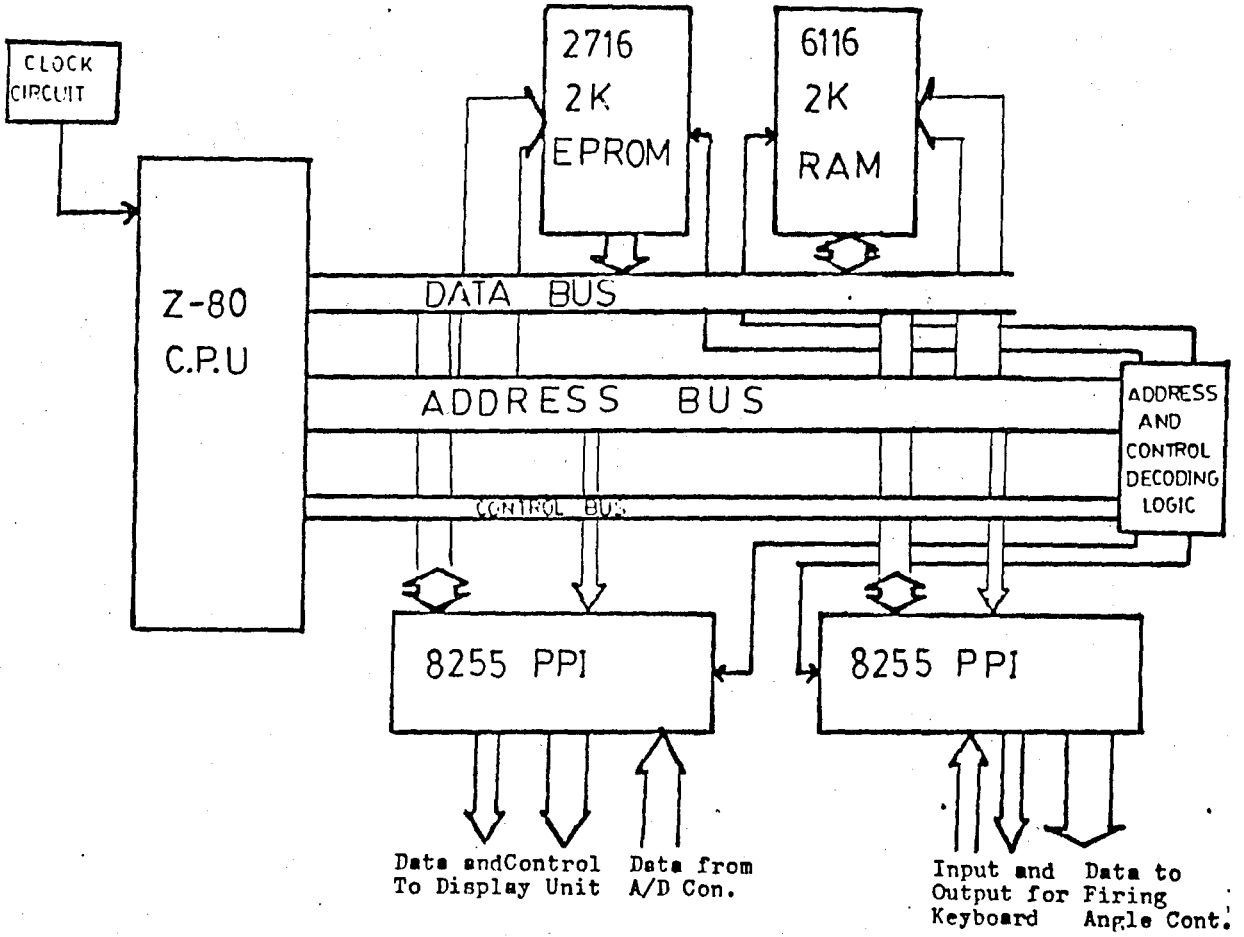


Figure 3.1 The Block Diagram of the Microcomputer

These properties of 8255 will be examined later. One port is used for the digital data from A/D converter. One port as two halves is used to scan the keyboard. Another port gives 8-bit firing delay angle data to the digital firing angle control circuit. One 8-bit port and another half port is used for display unit. Four bit BCD data is strobed into display unit by using one bit for each digit.

Memory Map: The locations of the 2716 and 6116 memories are shown in Figure 3.2.

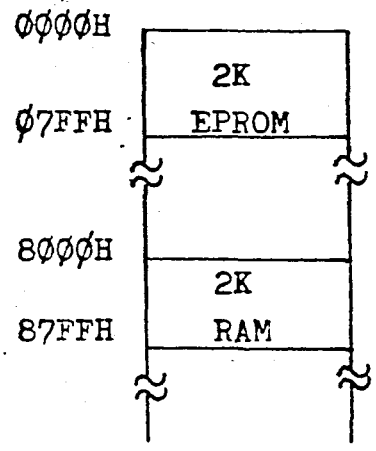


Figure 3.2 The Memory Map of the Microcomputer.

The reason for this memory map is to simplify the decoding. Decoding circuit is shown in Figure 3.3.

I/O Map: Each 8255 PPI consists of four registers, as far as I/O addressing is considered. These are A, B, C and Control registers.

Table 3.1 shows these ports, addresses for each port and functions.

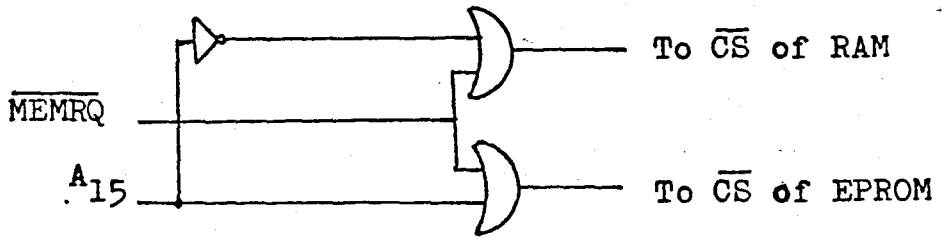


Figure 3.3 Memory Decoding Circuit.

8255 # 1	Port	I/O Add.	Functions of the Ports
	A	Ø4	Input from A/D converter.
	B	Ø5	Control signals to $\overline{LE}$ of BCD to 7-segment display driver.
	C_{lower}	Ø6	BCD data to display.
	C_{upper}	Ø6	PC_4, write signal to A/D converter to start A/D conversion. PC_5 is point signal for showing seconds.
	CONTROL	Ø7	
8255 # 2			
	A	Ø8	8-bit data to digital firing angle control circuit.
	B	Ø9	Unused
	C_{lower}	ØA	Input for keyboard scanning.
	C_{upper}	ØA	Output for keyboard scanning.
	CONTROL	ØB	

Table 3.1 The Addresses and Functions of 8255 PPI Ports.

Address decoding logic for 8255 PPIs is shown in Figure 3.4.

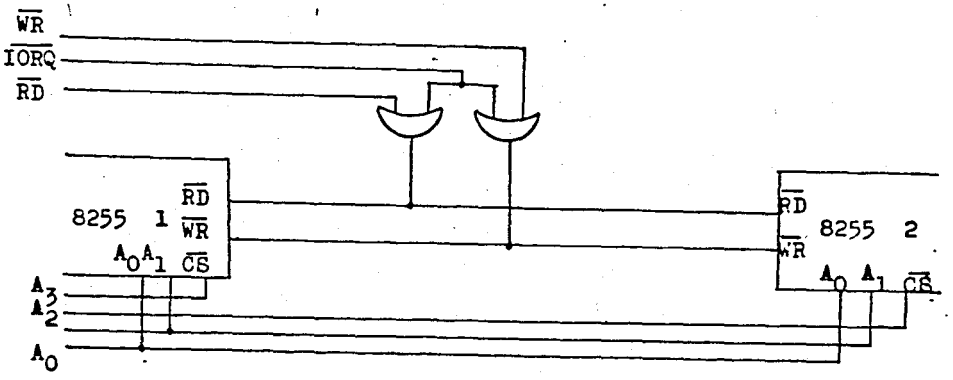


Figure 3.4 Address Decoding Logic for 8255 PPIs.

All the ports except the one connected to A/D converter are brought out on the computer board. So, these ports can be used for other purposes according to the peripheral necessity.

3.2. Microprocessor Unit. Z-80

3.2.1. Z-80 Architecture

The Z-80 microprocessor is an 8-bit device that is the data bus is eight bits wide and is the path for all data transferred between external memory and I/O devices and CPU registers. The architecture of the Z-80 is shown in Figure 3.2.1. The address bus is two bytes wide normally the address bus would specify external memory address of 0 to 65535 (Ø to 64K) since the Z-80 has full complement of I/O instructions, no memory mapped I/O would be required.

In memory mapped I/O, some portion of memory map would be dedicated to address of I/O devices.

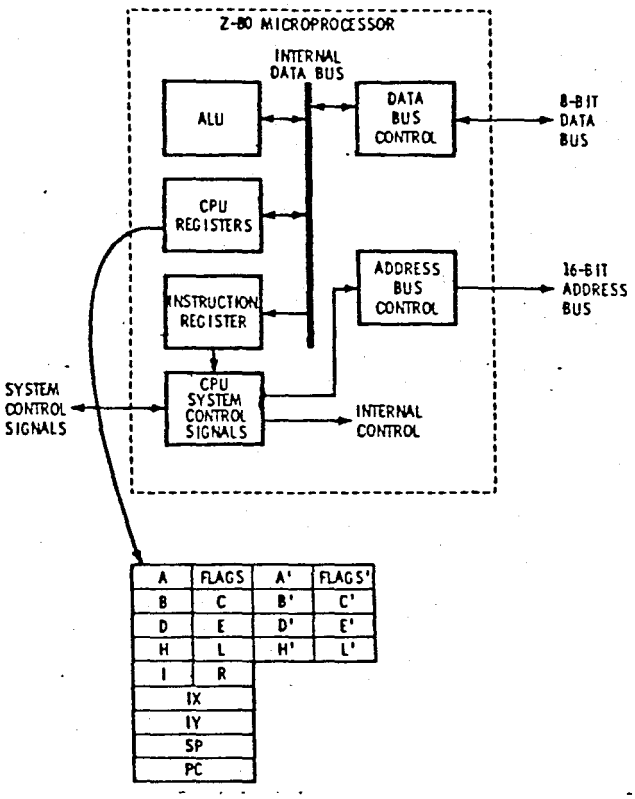


Figure 3.2.1 The Z-80 Microprocessor Architecture

The main path for data within the CPU is an internal data bus which connects the CPU registers , arithmetic and logical unit, data bus, control and instruction registers. The arithmetic and logical unit performs additions subtractions, logical functions of ANDing, ORing and Exclusive OR-ing and shifting operations between two eight bit operands. In addition, BCD operations may be performed under control of a Decimal Adjust Accumulator instruction.

3.2.2. General Purpose Registers

The CPU registers and status flags for the Z-80 may be illustrated in Figure 3.2.2.

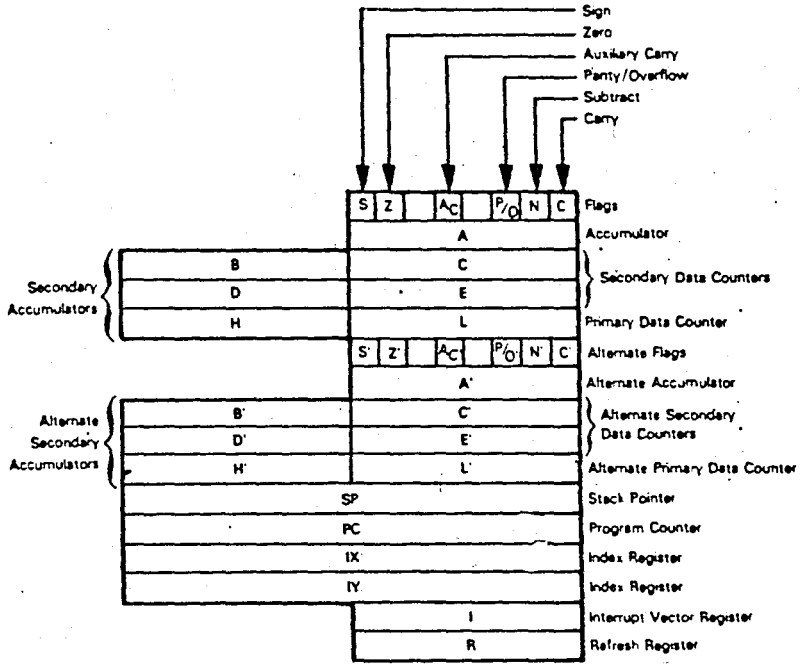


Figure 3.2.2 CPU Registers and Status Flags.

The accumulator is the primary source and destination for one operand and two operand instructions. All 8-bit arithmetic and Boolean instructions take one of the operand from the accumulator and return the result to the accumulator. An instruction must therefore load the accumulator before the Z-80 can perform any 8-bit arithmetic and Boolean operation.

The B, C, D, E, H and L registers are all secondary registers. Data stored in any of these six registers may be accessed with equal ease, such data can be moved to any other register or can be used as the second operand in two operand instructions.

There are however some important differences in the functions of registers B, C, D, E, H and L.

Registers H and L are the primary data pointers for the Z-80. That is to say, these two registers are normally used to hold the 16-bit memory address of data being accessed. Data may be transferred between any register and the memory addressed by H and L. Since HL is the primary data pointer it often takes fewer bytes of object code and less instruction cycles to perform operation with it.

Registers B, C, D and E provide secondary data storage. Frequently the second operand for two operand instructions is stored in one of these four registers.

There are a limited number of instructions that treat registers B and C or D and E as 16-bit data pointers. But these instructions move data between memory and the accumulator only.

Registers IX and IY are the index registers. They provide a limited indexing capability. When an instruction is executed in an indexed addressing mode one of the two index registers is used to calculate the memory address. The memory operand is obtained by adding the contents of the index register and an 8-bit value contained in the displacement of the instruction employing the indexed addressing mode. Indexed operations of this kind are extremely powerful for efficient programming.

The alternate registers F', A', B', C', D', E', H' and L' provide a duplicate set of general purpose registers; one instruction exchanges AF and the alternate BC', DE', HL'. The advantage in two blocks of general purpose registers is that a programmer may rapidly switch from one block to another. In the simplest case, this provides more register storage in the CPU.

There are a number of instructions that handle 16-bit data at a time. These instructions refer to pairs of CPU registers as follows;

High Order Byte		Low Order Byte
F	and	A
B	"	C
D	"	E
H	"	L
F'	and	A'
B'	"	C'
D'	"	E'
H'	"	L'

The combinations of the accumulator and flags treated as a 16-bit unit used only for stack operations and alternate register switches. Arithmetic operations access B and C , D and E, H and L as 16-bit data units.

Second use for these register pairs is double precision arithmetic. This involves adding subtracting incrementing or decrementing a 16-bit value . Most arithmetic and logical operations in the Z-80 are oriented toward 8-bit operations but the Z-80 allows limited operations between the register pairs and the stack pointer and the index registers IX and IY.

Flag Register: The carry status flag holds carries out of the most significant bit in any arithmetic operation. The carry flag is also included in shift instructions; it is reset by Boolean instructions.

The subtract flag is designed for internal use during decimal adjust operations. This flag is set to 1 for all subtract instructions and reset to zero for all add instructions.

The parity/overflow flag is a multiple use flag, depending on the operation being performed. For arithmetic operations, it is an overflow flag. For input, rotate and Boolean operations, it is a parity flag with 1 = even parity, 0 = odd parity. During block transfer and search operations it remains set until the byte counter decrements to zero; then it is reset to zero. It is also set to the current state of the interrupt enable flip-flop (IFF2) when LD A,I or LD A,R instructions are executed.

The zero flag is set to 1 when any arithmetic and Boolean operation generates a zero result. The zero status is set to Ø when such an operation generates a non-zero result.

The sign status flag acquires the value of the most significant bit of the result following the execution of any arithmetic and Boolean instructions.

The auxilary carry status flag holds any carry from bit 3 to 4 resulting from the execution of any arithmetic operation. The purpose of this flag is to simplify Binary Coded Decimal (BCD) operations.

All of the above status flags keep their current value until an instruction that modifies them is executed.

The PC register is a 16-bit register that holds the location of the current instruction being fetched from memory. Instructions in the Z-80 are one, two, three or four bytes long.

The CPU will automatically increment the PC by one, two, three or four depending on the length of the instruction being executed. The PC is available to the programmer only in the sense that it may be loaded or stored. No arithmetic or logical operations on the PC are permitted.

The 16-bit stack pointer allows to implement a stack anywhere in addressable memory. The size of stack is limited only by the amount of addressable memory present. The stack should be used for accessing subroutines and processing interrupts.

The Interrupt Vector Register, I, is used to hold the page address of an interrupt service routine. The last special purpose register is the 7-bit Memory Refresh Register, R. When external memory consist of dynamic memories, the R register allows automatic refreshing of this type of semiconductor memory which periodically needs to have every cell read or refreshed to retain its contents.

3.2.3. Interface Signals and Timing

The pinout of the Z-80 Microprocessor is shown in Figure 3.2.3 with the pins logically grouped according to the function rather than the actual physical representation.

Address and Data Bus : The address bus is represented by the signal A_{15} through $A_{\emptyset}$. Address bus is active high and tri-state. When I/O devices are addressed the lower byte of address bus is used.

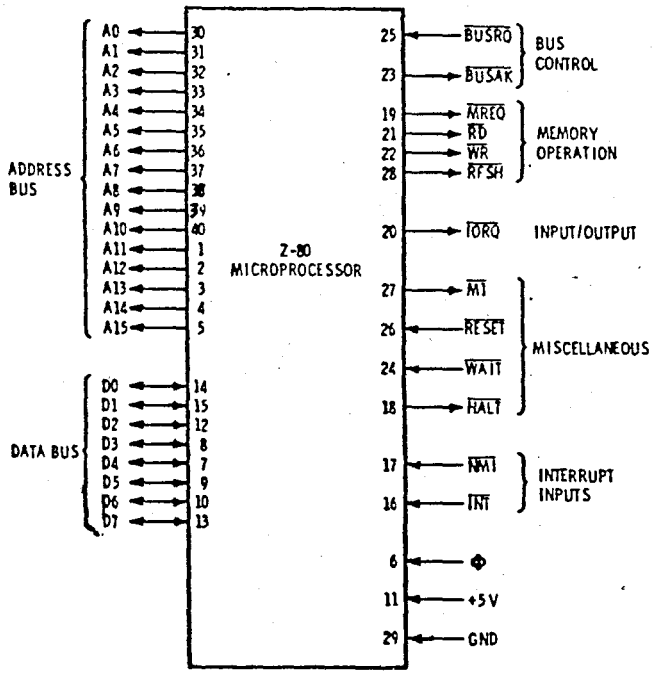


Figure 3.2.3 The Pinouts of Z-80 Microprocessor

The data bus signals D_7-$D_\emptyset$ are also tri-state active high signals. The data bus is bidirectional permitting data to be transferred to CPU registers or from them.

Bus Control Signals : There are two signals related to bus control, one is input, $\overline{BUSRQ}$, and the other is $\overline{BUSAK}$. BUSRQ is an active low signal that is generated by an external device to gain control of the CPU buses. The CPU responds with acknowledge signal $\overline{BUSAK}$.

Memory Signals : There are four signals associated with memory operation : $\overline{MEMRQ}$, $\overline{RD}$, $\overline{WR}$ and $\overline{RFSH}$. The first MEMRQ, Memory Request, is a tri-state active low signal indicating that the address bus holds a valid memory address.

The $\overline{RD}$ and $\overline{WR}$ signals are tri-state active low outputs to external memory indicating whether the memory operation is to be a read or write. The $\overline{RFSH}$ signal is not directly related to normal memory operation. It is used only when dynamic memories are used as external memories.

Input/Output Signals : Signal $\overline{IORQ}$ is a tri-state active low signal which indicates that the least significant eight bits of address bus holds a valid I/O address. Signals $\overline{RD}$ and $\overline{WR}$ must then be used to determine whether the I/O operation is to be an I/O read or I/O write.

Other CPU Signals : The $\overline{M1}$ signal is an active low signal indicating that the CPU is in instruction fetch cycle. The $\overline{RESET}$ signal is an active low input signal that is used as a master CPU reset. This signal would be brought low immediately after power up, or at any time when the microcomputer system is to be reset.

The $\overline{WAIT}$ signal is a signal associated with slow memories or I/O devices. As long as the $\overline{WAIT}$ signal is low the CPU will "mark time", doing nothing while the external memory or I/O device responds to a previous memory or I/O request.

Interrupt Related Signals : The remaining logic signals are related to interrupt control signals. Signal $\overline{NMI}$ is a negative edge triggered input that specifies a non-maskable interrupt is to be performed. The CPU transfers control to the address ØØ66 H.

The main interrupt signal $\overline{INT}$ is an active low input signal that is supplied by external devices to cause an interrupt. The interrupt signal will be recognized by the CPU, if the interrupt flip-flop in CPU is set and if the

$\overline{BUSRQ}$ is not active. If these conditions are met, the CPU accepts the interrupt and acknowledges the interrupt by sending out an $\overline{IORQ}$ during the fetch ($\overline{M1}$) time of the next instruction.

Z-80 Timing : All instructions in the Z-80 may be broken into a set of basic cycles. There are two kinds of cycles the most basic being a clock cycle or T cycle. The T cycles are used to control operations within a longer cycle called the machine cycle or M cycle. Every instruction executed within the Z-80 consists of from one to six machine cycles.

Machine Cycles :

1. Op-code fetch cycle (M1 cycle).
2. Memory data read or write cycle.
3. I/O read and write cycles.
4. Bus request and acknowledge cycle.
5. Interrupt request/acknowledge cycle.
6. Non-maskable Interrupt request/acknowledge cycle.
7. Exit from a HALT instruction.

3.3. Programmable Peripheral Interface (PPI)

The function of 8255 PPI is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures,

Figure 3.3.1 shows data bus buffer and read write control functions of 8255.

Data Bus Buffer : This tri-state bidirectional 8-bit buffer is used to interface the 8255 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU.

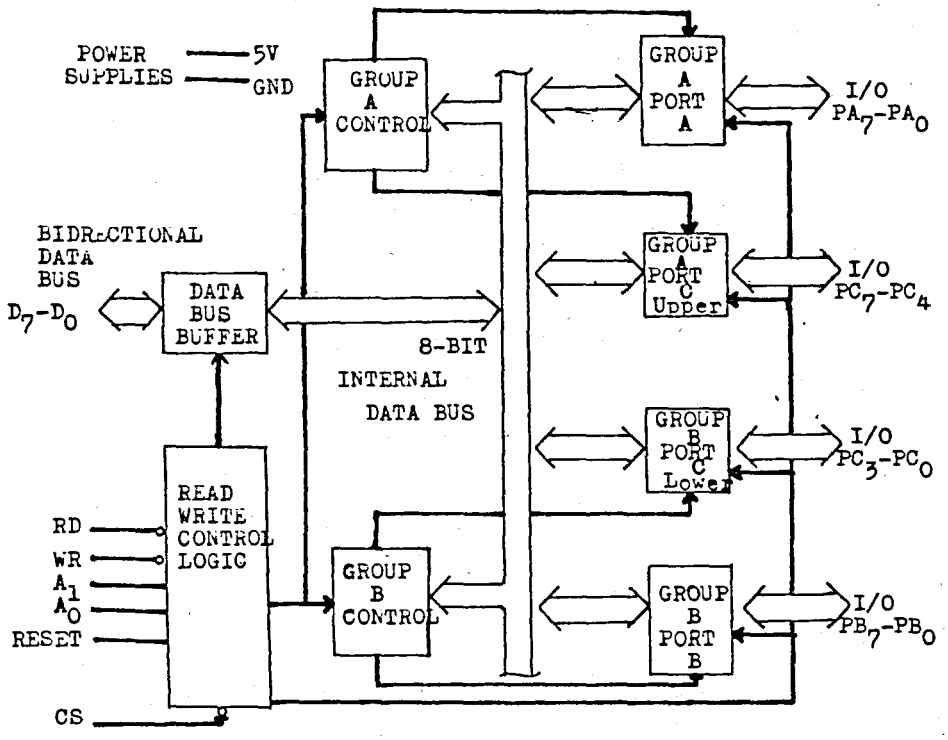


Figure 3.3.1 Read, Write and Control Logic of 8255.

Read, Write and Control Logic : The function of this block is to manage all of the internal and external transfers of both data and control or status word.

Group A and Group B Controls : The functional configuration of each port is programmed by the system software. In essence the CPU outputs a control word to the 8255.

The control word contains information such as "mode", "bit set", etc. that initializes the functional configuration of the 8255.

Each of the control blocks (Group A and Group B) accepts commands from the read write control logic, receives "control words" from the internal data bus, and issues the proper commands to its associated ports. The Control Word Register can only be written into. No read operation of the Control Word Register is allowed.

Ports A,B and C : The 8255 contains three 8-bit ports : A,B and C. All can be configured in a wide variety of functional characteristics by "the system software", but each has its own special features or "personality" to further enhance the power and flexibility of 8255.

PORT A: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

PORT B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

PORT C: One 8-bit data output latch/buffer and one 8-bit data input buffer. This port can be divided into two 4-bit ports under the mode control.

3.3.1. 8255 PPI Operational Description

Mode Selection : There are three basic operation mode that can be selected by the system software:

Mode Ø Basic input/output
Mode 1 Strobed input/output
Mode 2 Bi-directional bus

When 8255 PPI is resetted all ports will be set to the input mode.

After the reset is removed, the 8255 can be remain in this mode with no additional initialization required. During the system program any other modes may be selected using a single output instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for port A and port B can be separately defined, while port C is divided into two portions as required by the port A and port B definitions. Modes may be combined so that their functional definitions can be "tailored" to almost any I/O structure.

3.3.2. Operating Modes

As mentioned above, it has three operation modes. The basic input/output mode (Mode Ø) is used in this thesis so, only this mode will be examined in detail.

Mode Ø : This functional configuration provides simple input and output operations for each of the three ports no "hand shaking" is required, data is simply written to or read from a specified port.

Mode Ø Basic Functional Definitions :

a. Two 8-bit ports and two 4-bit ports.
b. Any port can be input or output.
c. Outputs are latched.
d. Inputs are not latched.
e. 16 different Input/Output configurations are possible in this mode.

Table 3.1 shows mode Ø port definitions.

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

Table 3.1 Mode Ø Port Definitions.

3.4. A/D Conversion

Signals which may assume any value in a continuous range are called analog signals. When analog signals must be processed there is often a great advantage in converting the signal to digital form so that the processing can be done digitally.

At the input of a digital processing system, the overall process of converting an analog signal to a digital form includes a sequence of four individual processes called; sampling, holding, quantizing and encoding. These processes are not necessarily performed as separate operations. Generally sampling and holding are done simultaneously in a type of circuit referred to as a Sample and Hold circuits while quantizing and encoding are done simultaneously in a circuit referred to as an A/D converter.

Interfacing an A/D converter to microcomputer bus is shown in Figure 3.4.1.

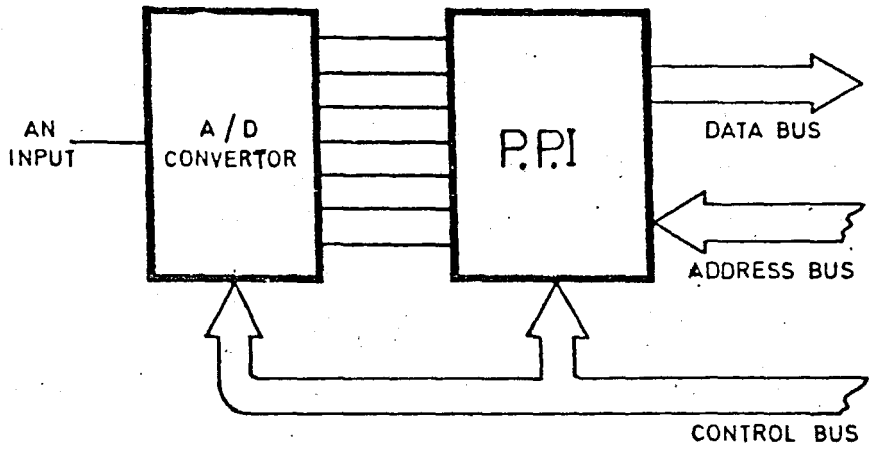


Figure 3.4.1 Interfacing an A/D Converter to Microcomputer Buses.

During a read cycle the address on the address bus is decoded and if the PPI is enabled by the correct address the data from A/D converter is presented to the data bus. During the write cycle the address bus is decoded. If the address is valid than the converter is strobed to initiate conversion.

The time interval between the write and read cycles is a function of conversion time for the particular converter used. If the time period is short, it will probably be acceptable to HALT or INHIBIT further system operations until the conversion is complete. If the conversion time is long it may be preferrable to carry out other operations while conversion is in progress and INTERRUPT when conversion is complete. Most A/D converters have a busy output, sometimes called EOC (End of Conversion) which can be used to generate interrupts.

Another problem that must be considered is the effect of analog signal changes during the conversion cycle which can cause gross errors. This can be solved by using a sample and hold amplifier to hold the signal constant during conversion, necessitating further circutry to produce further pulses for this device.

One solution to the above problem is to use specifically designed analogue input peripherals. This directly interfaces to the microprocessor bus system and contains all components necessary to read analogue changes into a microprocessor based system.

3.4.1. ADC(0801), 8-Bit μP Compatible A/D Converter

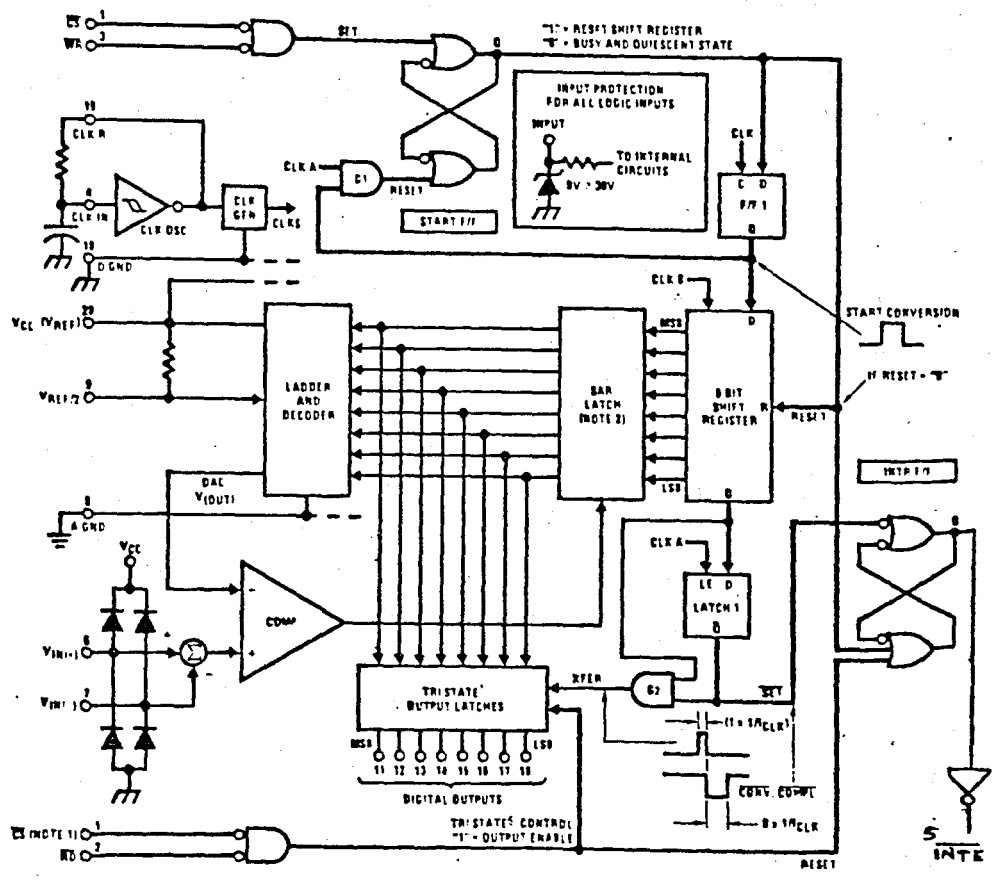
ADC 0801 is a CMOS 8-bit successive approximation A/D converter which use a differential potentiometric ladder similar to the 256 products.

Differential analog voltage input allows increasing the common mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analogue voltage span to the eight bits of resolution.

Specifications :

a. 8-bit resolution
b. Total error - 1/4 LSB
c. Conversion time 100 mSec.
d. Access time 135 nSec.

Functional Description : The ADC 0801 combines a circuit equivalent of the 256 R network. Analog switches are sequenced by successive approximation logic. The block diagram of ADC 0801 is shown in Figure 3.4.2.



Note 1: $\overline{CS}$ shown twice for clarity.
Note 2: SAR = Successive Approximation Register.

Figure 3.4.2 The Block Diagram of ADC 0801

The most significant bit is tested first and after eight comparisons a digital 8-bit binary code is transferred to an output latch and than an interrupt is asserted. A conversion in progress can be interrupted by issuing a second start command. The device may be operated in the free running mode by connecting INTR to the WR input with CS 0. To insure start-up under all possible conditions, an external write pulse is required during the first power up cycle.

On the high to low transition of the WR input the internal SAR latches and the shift register stages are reset. As long as the CS input and WR input remain low the A/D is

resetted. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register; resets the interrupt F/F and inputs a "1" to the D flip-flop.

Internal clock signals then transfer this "1" to the Q output of F/F 1. Then AND gate ,G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide CS and WR signals and the converter will start after at least one of these signals return high and the internal clocks again provide a reset signal for the start F/F.

After the "1" is clocked through the 8-bit shift register, it appears as the input to the D type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate G2, causes the new digital word to transfer to the tri-state output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the interrupt flip-flop to set. An inverting buffer then supplies the INT output signal.

This SET control of the INTR F/F remains low for eight of the external clock periods (as the internal clocks runs at 1/8 of the frequency of the external clock periods). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both

held low), the $\overline{\text{INTR}}$ output will still signal the end of conversion, because the set input can control the Q output of the INTR F/F eventhough the RESET input is constantly at a "1" level in this operating mode. This interrupt output will therefore stay low for the duration of the SET signal, which is eight periods of the external clock frequency (assuming the A/D is not started in this interval).

When operating in the free running or continuous conversion mode, the START F/F is SET by the high-to-low transition of the $\overline{\text{INTR}}$ signal. This resets the SHIFT REGISTER which causes the input to the D type latch, LATCH 1 to go low. As the latch enable input is still present, the Q output will go low which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{\text{INTR}}$ output pulse to only a few propogations delay.

When data is to be read the combination of both CS and RD being low will cause the INTR F/F to be reset and the tri-state output latches will be enabled to provide the 8-bit digital outputs.

3.5. Semiconductor Memories

All digital computer systems require facilities for storing information. The information so stored may consists of the numbers to be used in a computation, intermediate computational results, instructions which will direct a computation or all three. That part of a digital processor which provide this facility is called memory.

Semiconductor memories are used for both program and data storage. Program storage devices hold the instructions, that direct the operation of a microprocessor based system; data storage devices store the actual bits of information to be manipulated. The major distinction between

the types of memory used for these respective purposes is that program storage devices must be non-volatile, that is capable of retaining their contents without a steady power supply, while volatile memories used for data storage lose their contents when power is removed.

Non-volatile program storage is needed in microcomputer systems to make the program firmware. Virtually all microprocessor based products use some type of non-volatile read-only memory to store all basic programs. The different types of read-only-memory devices are ROMs, PROMs, EPROMs and EEPROMs.

The monitor program storage device in this thesis is an EPROM, Erasable Programmable Read Only Memory. EPROMs can be programmed by the designer or user as often as desired. They are programmed electrically and can be erased for reprogramming by exposing the chip to special ultraviolet light through a window in the EPROM package. The electrical programming operation traps electrical charges in the bit storage cells selected by addressing word locations on the chip. Intense ultraviolet light dissipates these charges. Between erasures, the EPROM is non-volatile and can retain data for many years without being powered.

Erasable PROMs or EPROMs add considerable flexibility to the programming stage. The only drawback to EPROM is that they must be removed from the equipment to be reprogrammed. Despite this inconvenience, EPROM s are today the most popular program storage memory devices.

The EPROM used in this thesis is a 2Kx8 bit EPROM which is named 2716. The reset vector of Z-80 microprocessor, that is to say, the address on the address bus when the system is resetted, is ØØØØH. Due to this fact the monitor program has to be exist at the beginning of memory map. The EPROM is located between the addresses ØØØØH to Ø7FFH in

this system.

The 2716 is a word addressable 16384 bit EPROM. It is a silicon gate N-Channel MOS device. Some important features of 2716 can be stated as follows:

a. Single 10 % 5V Power Supply.
b. Automatic Power Down Mode (Standby).
c. Organized as 2048 Bytes of 8 bits.
d. Low power dissipation, 555 mW max. active power.
e. TTL compatible during read and program.
f. Maximum Access Time 450 nS.

Data storage devices on the other hand must be capable of writing data into storage as well as reading it out. This is due to the fact that stored data is constantly being changed. Random access memories, called RAMs, are used for this purfose due to their read/write property. However, semiconductor RAMs are volatile requiring steady power supply for keeping their contents.

RAMs can be classified into two major groups, Dynamic RAMs and Static RAMs. In dynamic RAMs a stored charge switches a transistor either on or off, storing the information. Since the charge eventually leaks off, the cell needs to be refreshed at regular intervals hence, the term dynamic memory comes out, peripheral circuitry senses the data and re-writes it into the cell. The resulting increase in density and reduction in power make dynamic RAMs very popular.

On the other hand Static RAMs require no refreshing for keeping their contents. But static memory cells have two main drawbacks : Relatively large size and high power consumption, both critical parameters for high-density memories. Non-requirement of additional hardware for refreshing and suitable organizations make usable static RAMs for small

microprocessor based systems.

The RAM used in this thesis work is a 2Kx8 bit static RAM which is called 6116.

This is a High Speed CMOS device consisting of 2048x8 bit cells. Important features of 6116-3 RAM are as follows:

a. Single 5V supply.
b. Access time : 150 nS.
c. Standby power dissipation : 100 mW.
   Operation power dissipation : 180 mW (typical).
d. All inputs and outputs are TTL compatible.

CHAPTER IV

INSTRUMENTATION AMPLIFIER

An instrumentation amplifier is a commited "gain block" that measures the difference between the voltages existing at its two input terminals, amplifies it by a precisely set gain and causes the result to appear between a pair of terminals in the output circuit. Referring to Figure 4.1 ,

$V_S - V_R = G(V^+ - V^-)$, in which V_S Sense or output voltage, V_R Reference voltage, G Gain, $(V^+ - V^-)$ is the differential input voltage.

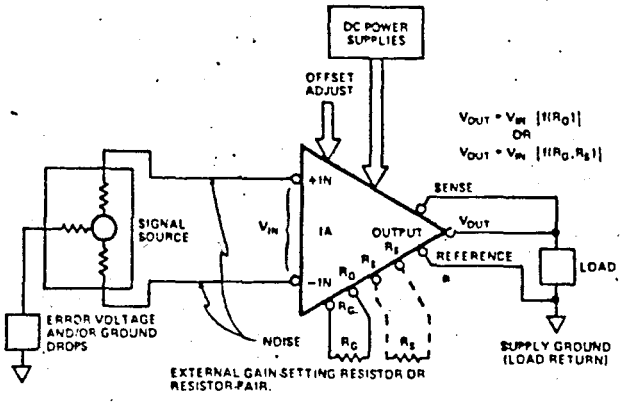


Figure 4.1 Basic Instrumentation Amplifier Functional Diagram.

An ideal instrumentation amplifier responds only to the difference between the input voltages. If the input voltages are equal ($V = V =$ VCM, the common mode voltage),

the output of the ideal instrumentation amplifier will be zero.

An amplifier circuit which is optimized for performance as an instrumentation amplifier gain block has high input impedance, low offset and drift, low non linearity, stable gain, low effective output impedance. It is commonly used for applications which capitalize on these advantages. Examples : Transducer amplification for thermocouples, strain gage bridges, current shunts and biological probes.

4.1. Instrumentation Amplifier Architecture

Classic 3-OpAmp instrumentation amplifier circuit is shown in Figure 4.1.1.

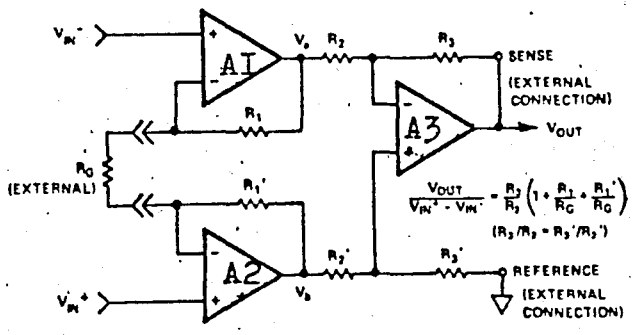


Figure 4.1.1 3-Op Amp Instrumentation Amplifier

The Op Amps are used extremely in instrumentation amplifiers as building blocks. A1 and A2 are input Op Amps, they give high input impedance. RG is used to control the gain. But the gain is adjusted by the ratio of R3/R2 structurally.

Hence,

$$V_{out} = \frac{R_3}{R_2}\left(\frac{2R_1}{R_G} + 1\right)\Delta V \qquad (4.1.1)$$

4.2. Instrumentation Amplifier Specifications

Gain : These specifications refer to the linear transfer function of the device. For example, for the above circuit from equation 4.1.1.

$$A_V = \frac{V_{out}}{\Delta V} = \frac{R_3}{R_2}\left(\frac{2R_1}{R_G} + 1\right) \qquad (4.2.1)$$

is the gain of the circuitry. There are some limitations on the gain of instrumentation amplifier due to noise and drift.

Equation Error : This gives the deviation from the gain equation when the resistors at nominal values. This can be compensated by using trimmers for R_G and R_3. However, systems using microprocessors (or computers) can be made self calibrating to take into account lumped gain errors of all the stages in the analog portion of the system from transducer to A/D converter.

Nonlinearity : Nonlinearity is defined as the deviation from a straight line on the plot of output vs. input. The magnitude of linearity error is the maximum deviation from a "best straight line" with the output, swinging through its full scale range. Nonlinearity is usually specified in percent of full scale output range.

Gain Versus Temperature : These numbers give the deviations from the gain equation as a function of temperature.

Settling Time : It is defined as that legth of time required for the output voltage to approach and remain within a certain (±) tolerance of its final value. It is usually specified for a fast step that will drive the output through its full scale range and it includes slew rate. Factors contributing to the setling time are slew rate limiting, underdamping and thermal gradients.

Offset voltage : Offset voltage and common mode rejection specifications are often considered the key specifications of instrumentation amplifiers. While initial offset can be adjusted to zero, shifts in offset voltage with time and temperature introduce errors. Systems that involves microprocessors can correct for offset errors in the whole measurement chain.

Offset voltage and offset drift are functions of gain. The offset, measured at the output is equal to a constant plus a term proportional to gain.

Input Bias and offset currents : Input bias currents are those currents needed to bias the input transistors of a dc amplifier or to supply the function leakage of FETs. FET input devices have lower input bias currents than those using bipolar transistors but FET leakage currents increase dramatically with temperature approximately doubling every 11°C. Since bias currents can be considered as a source of offset voltage (when multiplied by source resistance); the change in bias currents is of more concern than the magnitude of bias current. Input offset current is the difference between the two bias currents.

Although instrumentation amplifiers have differential inputs there must be a return path for the bias currents. If it is not provided those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying outputs of floating sources, such as transformers and thermocouples as well as ac coupled sources, there must still be a dc return path is impractical an isolator should be used.

Common Mode Rejection (CMR): It is a measure of the change in output voltage when both inputs are changed by equal amounts. CMR is usually specified for a full range common mode voltage change at a given frequency and a specified imbalance of source impedance. CMR is a logarithmic expression of the common mode rejection ratio, (CMRR), CMR 20 log (CMRR). The common mode rejection ratio is defined as the ratio of the difference signal gain to the gain of common mode signal. In most instrumentation amplifiers the CMR increases with gain, because the front-end configuration doesn't amplify common mode signals, and the amount of common mode signal appearing at the output stays relatively constant as the signal gain (G) increases. However, at higher gains amplifier bandwidth decreases. Since defferences in phase shift through the differential input stage will show-up as common mode errors, CMR becomes more frequency dependant at higher gains.

4.3. The Bridge and Instrumentation Amplifier Used in This Thesis

Bridges are the most popular examples of balanced networks. The concept of symmetry is inherently used in bringing a network to a balanced form. To show this idea let's look at the Wheatstone Bridge shown in Figure 4.3.1.

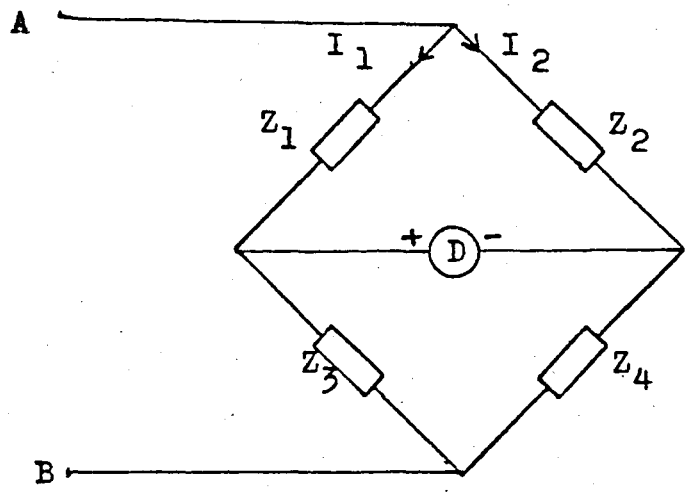


Figure 4.3.1 The Wheatstone Bridge Circuit.

At balance, that is to say when no current flowing through the measuring device:

$$I_1 Z_4 = I_2 Z_3 \qquad (4.3.1)$$

$$I_1 Z_2 = I_2 Z_1 \qquad (4.3.2)$$

By dividing 4.3.1 by 4.3.2,

$$\frac{Z_4}{Z_2} = \frac{Z_3}{Z_1} \quad , \quad Z_1 Z_4 = Z_2 Z_3 \qquad (4.3.3)$$

By taking $Z_2 = Z_4 = Z_3 = R$ and $Z_1 = R_X$

$$V_D = \left(\frac{R}{R_X + R} - \frac{1}{2} \right) V_{AB} \qquad (4.3.4)$$

In this thesis a Wheatstone Bridge is used for generating a difference signal resulting from the temperature change in the liquid tank. The bridge is so designed that it will be in balance at 25°C. The variable resistance is an RTD , PT100 probe. It is of resistance dependant on temperature. Its resistance versus temperature characteris tics is given as a table in Appendix.

In the circuit the temperature dependant resistance prome is connected such that, the connecting wires will contribute nothing. This connection is an industrial standart connection. It provides one connection to one end and two to one other end of the sensor. By this configuration compensation is achieved for lead resistance and temperature change in lead resistance. This is the most commonly used configuration.

The RTD, PT 100 : It is a temperature sensing transducer. It is made up of platinum wire and it operates on the principals of change in electrical resistance of platinum wire as a function of temperature.

Of all usable metals, platinum meets best the requirements of thermometry. It can be highly refined. It resists contamination and it is mechanically and electrically stable. The relation between the temperature and resistance is quite linear. Drift and errors with age and use are negligible. Platinum resistance is used for temperature measurement in the range-220 to 600°C (standard). The maximum temperature is determined by the type of insulation material used to inclose the platinum winding.

The Sensing Element: The heart of the platinum resistance thermometer is the sensing element, made up of high purity platinum wire wound upon a ceramic core. Its resistance is 100.0 at 0°C.

Response times: 50% Response is the time the temperature sensing element needs in order to reach 50% of its steady state value, in a similar manner 90% response time is defined.

Mesurement current and self heating: Temperature measurement is carried out almost exclusively with direct current. The permissible measurement currents are determined by the location of the element and the medium which is to be measured. The self heating error for the PT100 used in this thesis is 0.12 in $^{o}C/mW$ for flowing air, V=1 m/s and 0.20 $^{o}C/mW$ for still air.

The temperature measurement error, T(^{o}C) can be calculated from,

$$T = P \times S \qquad (4.3.5)$$

In which, S is the measurement error for the element in ^{o}C per miliwatt. With a given value of measuring current, I, the power can be calculated from $P = I^2.R$, where, R is the corresponding resistance value.

In this thesis the voltage applied to the bridge is tried to be held as low as possible. It is 1V. Hence, the self heating measurement error at $25^{o}C$;

$$T = P \times S$$

$$P = I^2.R = \left(\frac{1}{2 \times 109.7}\right)^2 \times 109.7 = 2.27 \text{ mW}$$

$$P = 2.27 \text{ mW} \quad \text{at } 25^{o}C$$

At $89^{o}C$ which is the maximum temperature handled by this system,

$$P = \left(\frac{1}{109.7 \quad 134.3}\right)^2 \times 134.3 = 2.24 \text{ mW}$$

S is given $0.12^{\circ}C/mW$

$T = 2.25 \times 0.12 = 0.27^{\circ}C$ which is an acceptable error.

The complete schematic diagram of the bridge and instrumental amplifier is given in Figure 4.3.1.

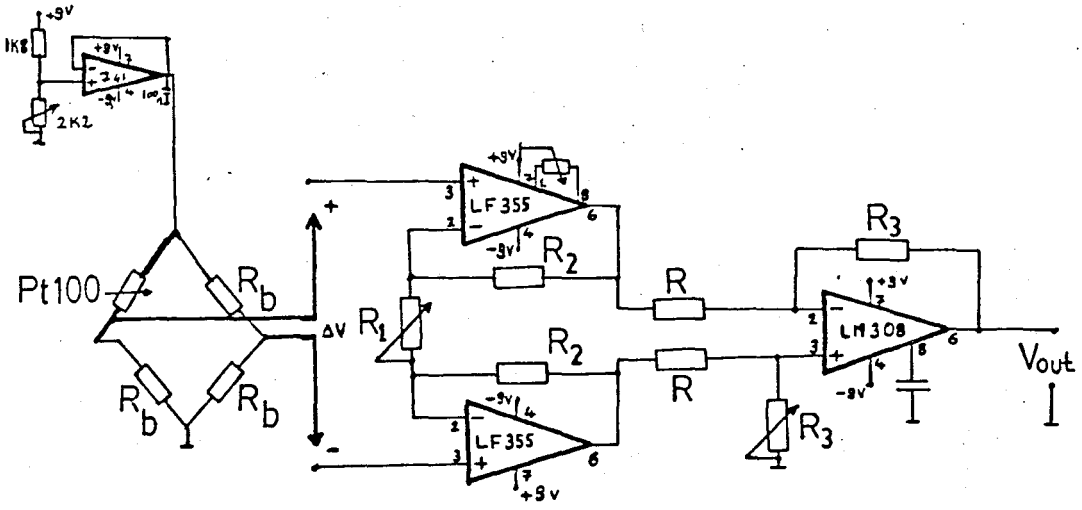


Figure 4.3.1 The Circuit Diagram of the Bridge and Instrumentation Amplifier

The instrumentation amplifier consists of three Op Amps. Two input Op Amps gives high input impedance and high CMRR as FET input Op Amps. System offset voltage is adjusted by R.

Amplifier gain is,

$$A = \frac{R_3}{R}\left(\frac{2R_2}{R_1} + 1\right) \qquad (4.3.6)$$

The maximum difference signal is obtained at 89 °C.

$$V = \left(\frac{1}{2} - \frac{109.7}{134.3 \quad 109.7} \right) x1 = 50.4 \text{ mV}$$

This difference signal should be 5V at the output of instrumentation amplifier for A/D conversion. Hence, the gain ;

$$A = \frac{V_{out}}{V} = \frac{5}{50.4 \times 10^{-3}} = 99.2$$

This value of gain is set by R_1 in the circuit. The instrumentation amplifier output is coupled to the A/D converter resistively by a 1K resistor in computer board. In this circuit ;

$R_b = 109.73$ which equals the resistance of PT100 at 25 °C.

$R = 1.5K$, $R_3 = 4.7K$, $R_2 = 47K$, $R_1 = 10K$

CHAPTER V

DIGITAL FIRING ANGLE CONTROL

5.1. Circuit Operation

This circuit is used for supplying a triac by firing pulses synchronised with the mains. The firing angle is determined by an 8-bit control input.

A phase coherent control waveform is generated internally by a voltage controlled oscillator which is precisely synchronized with a multiple of the line frequency by a phase locked loop. Therefore the operation of the trigger circuit is free from waveform distortion and transients, usually found on industrial supply lines. The phase locked loop can be designed to have a fast response in order to minimize disturbances during supply frequency transients at start up.

5.2. Basic Phase Locked Loop Operation

Figure 5.2.1 shows the basic blocks of a phase locked loop. The input signal e_i is a sinusoidal of arbitrary frequency, while the voltage controlled oscillator signal e_o is an sinusoidal of the same frequency as the input, but of arbitrary phase. If,

$$e_i = \sqrt{2}\, E_i .\ \mathrm{Sin}\left(W_o t + \theta_1(t)\right) \qquad (5.2.1)$$

$$e_o = \sqrt{2}\, E_o .\ \mathrm{Sin}\left(W_o t + \theta_2(t)\right) \qquad (5.2.2)$$

The output of the multiplier (phase detector) is,

$$e_d = e_i . e_o = 2E_i . E_o \ \mathrm{Sin}\left(\theta_1(t) - \theta_2(t)\right) + \mathrm{Sin}\left(2W_o t + \theta_1(t) + \theta_2(t)\right) \qquad (5.2.3)$$

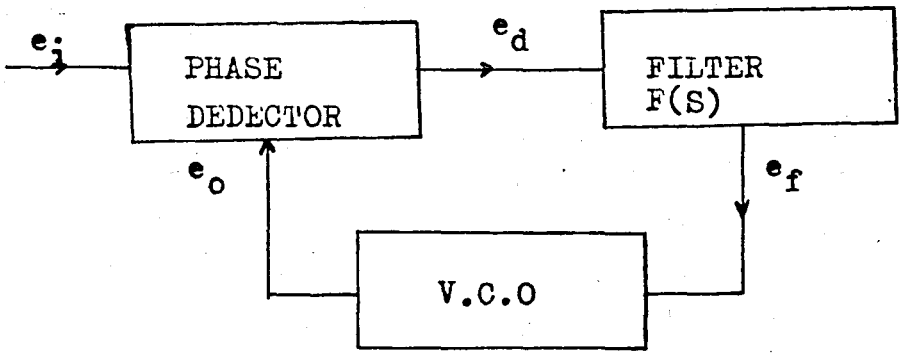


Figure 5.2.1 Basic Blocks of PLL

The amount of phase error resulting from a given fre ency shift can be found by knowing the "dc" loop gain of the system . Considering the phase detector to have a transfer function,

$$E_d = K_d(\theta_1 - \theta_2) \qquad (5.2.4)$$

and the voltage controlled oscillator to have a transfer function,

$$\theta_2 = K_o \cdot e_f \qquad (5.2.5)$$

By taking Laplace transform of 5.2.5.,

$$\theta_2(S) = \frac{K_o \cdot e_f}{S} \qquad (5.2.6)$$

The phase of the V.C.O output will be proportinal to the integral of the control voltage Combining these

equations,

$$\frac{\theta_2(S)}{\theta_1(S)} = \frac{K_o K_D F(S)}{S + K_o K_D F(S)} \qquad (5.2.7)$$

Now lets consider the ac performance which is governed by the components of the loof filter placed between the phase detector and the V.C.O. In fact, it is this loop filter that makes the phase locked loop so powerful. Only a resistor and capacitor are all that is needed to produce an arbitrarily narrow bandwidth at any selected center frequency. One of the simplest filters is an RC network.

$$\frac{e_f}{e_d} = \frac{1}{1 + SR_1C_1} \qquad (5.2.8)$$

$$\frac{\theta_2(S)}{\theta_1(S)} = \frac{K_o \cdot K_D/\tau_1}{S^2 + S/\tau_1 + K_o K_D/\tau_1} \qquad (5.2.9)$$

$$\tau_1 = R_1 C_1$$

in which R_1 and C_1 are the components of the filter.

In terms of servo theory, the damping factor and natural frequencies are;

$$W_n = \sqrt{\frac{K_o K_D}{R_1 C_1}} \qquad (5.2.10)$$

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{R_1 C_1 K_o K_D}} \qquad (5.2.11)$$

The damping factor is ;

$$\zeta = \frac{1}{2}\left(\tau_2 + \frac{1}{K_o \cdot K_D}\right)\sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}} \simeq \frac{W_n \cdot \tau_2}{2} \qquad (5.2.12)$$

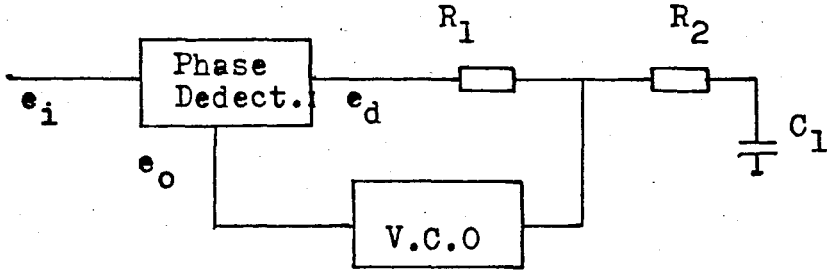


Figure 5.2.2 RC Filter with Damping Resistor.

5.3. Description of the Circuit

The block diagram of the circuit is shown in Figure 5.3.1. The principal waveforms are shown in Figure 5.3.2. A transformer and a comparator are used for shaping the sinusoidal line waveform. The comparator converts the ac input voltage to a square wave which is used to synchronize the phase locked loop frequency synthesizer. This consists of CMOS phase locked loop element 4046 with its own voltage controlled oscillator and a nine bit counter. The loop filter is selected in order to obtain a type 2

PLL which produces a phase coherent output relative to the input. The square wave of the second input of the phase detector has the same frequency as the synchronizing signal at the output of the comparator and the two signals are phase coherent.

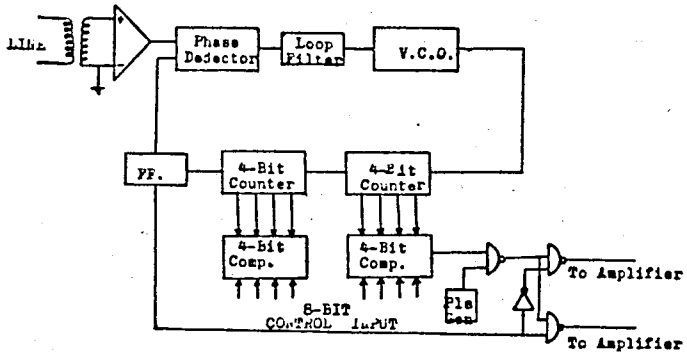


Figure 5.3.2 The Block Diagram of Digital Angle Control System.

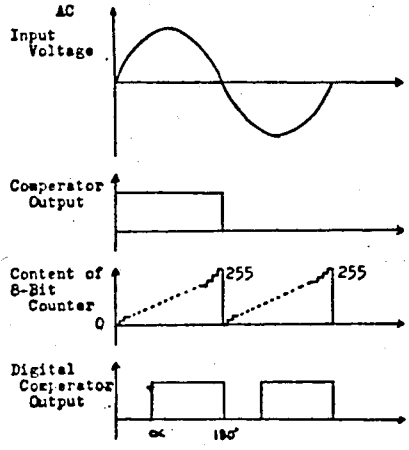


Figure 5.3.3 The Principal Waveforms

The content of the nine-bit counter is effectively a linear digital ramp synchronized in phase and frequency with the ac input voltage. At the beginning of each cycle (0°), the counter content is zero and it is incremented by

the 25.6 kHz. Signal from the V.C.O is divided by 9-bit counter to attain 511 at the end of the cycle (360°).

The desired delay angle is provided by the digital comparator which detects coincedence of the 8-bit counters content with the digital control input. Hence, the delay angle is directly proportional to the control input and can be varied from 0° to 180° by steps of 180°/256 0.7°.

The comparator output is fed to the pulse distributing circuit which transmits triggering pulses from an oscillator to appropriate pulses.

5.4. Trigger Pulse Shaping

So far we have obtained the comparator output ANDed with pulses generated by a pulse generator. A triac has four operation modes :

I^+ ; $A_2(+)$, G(+), positive voltage and positive gate current.

I^- ; $A_2(+)$, G(-), positive voltage and negative gate current.

III^+ ; $A_2(-)$, G(+), negative voltage and positive gate current.

III^- ; $A_2(-)$, G(-), negative voltage and negative gate current.

Present triacs are most sensitive in modes I and III . Slightly less so in mode I , and much less sensitive in mode III . Therefore III mode is not recommended to be used.

Due to this fact, in this circuit, comparator output pulses for negative and positive cycles are taken apart and shaped independently.

Figure 5.3.3 shows the generation sequence of firing pulses to the triac. As it is mentioned above the comparator output is ANDed with a pulse generator which has a higher frequency than the comparator output. The ANDed comparator signal is then ANDed once with a 50 Hz square wave synchronized with the mains and once with inverted 50 Hz. So, the firing pulses for positive and negative half cycles are generated separately.

These firing pulses must be applied to the same point, the gate of the triac. So, they have to be combined before applied to the gate. Before summing these signals, polarity invertion must be done for negative half cycles. This is accomplished by using a 741 Op Amp as an inverter. Another 741 is used as a buffer. Combination of these signals are achieved by a summer circuit. The complete circuit diagram of Digital Firing Angle Control System is in Figure 5.3.4.

Summed firing pulses can be coupled to the gate of the triac by some means, by pulse transformers, by opto-couplers etc. For safety operation high voltage circuit and the main control circuit has to be isolated from each other.

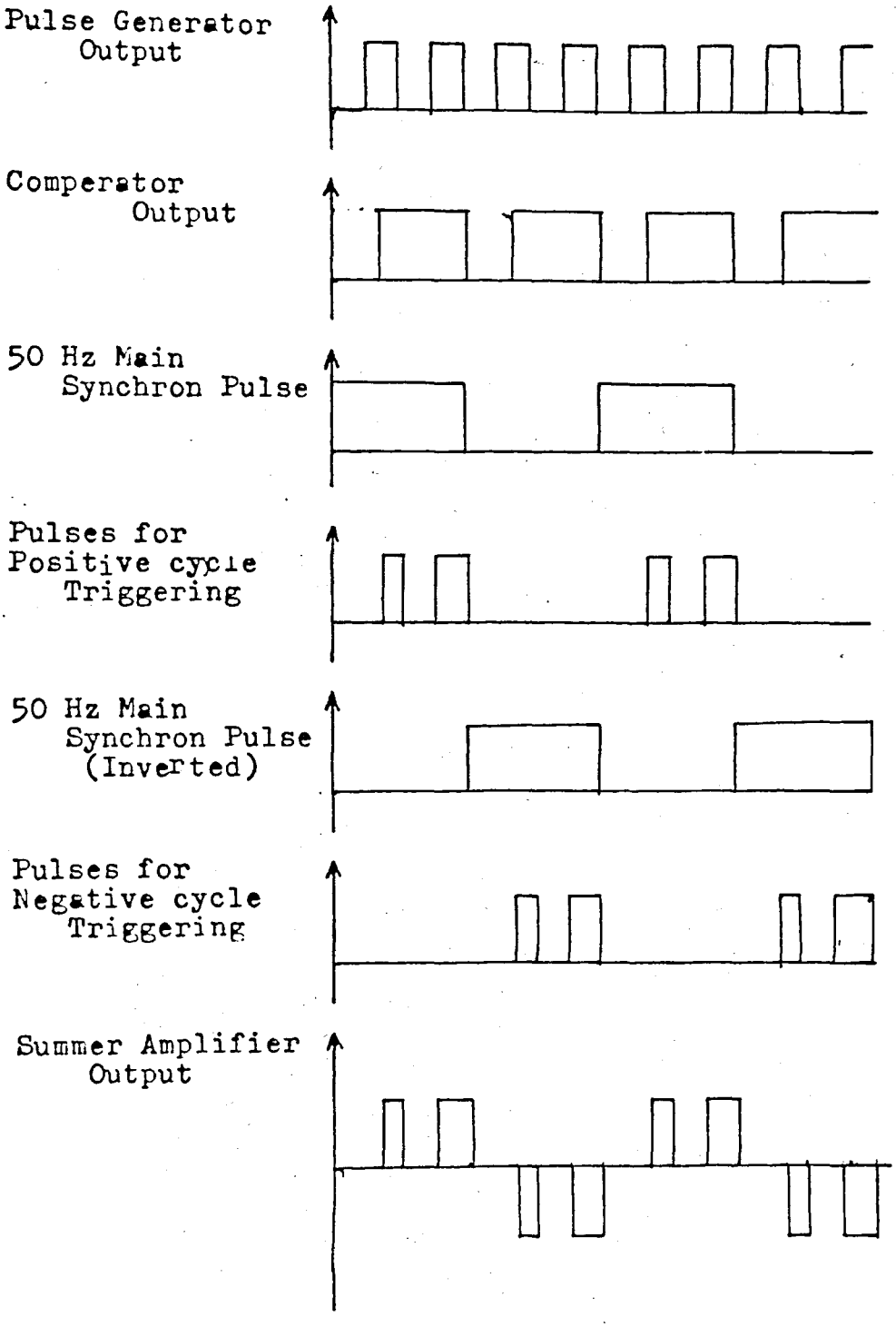


Figure 5.3.3. Genaration Squence of Firing Pulses.

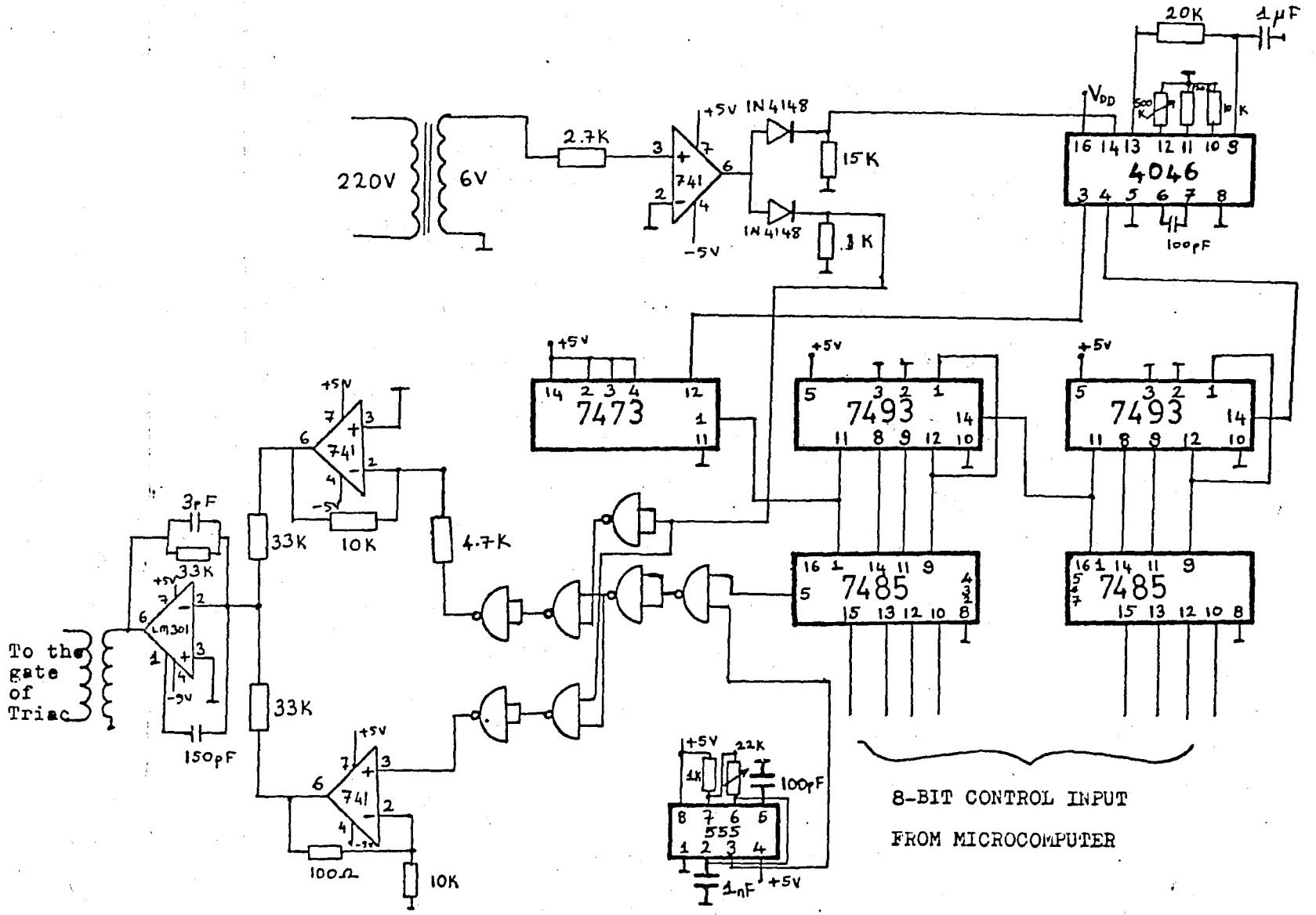


Figure 4.3.4 The Circuit Diagram of the Firing Angle Control System

CHAPTER VI

DISCUSSION

The realised system operated satisfactorily, but some limitations which stemmed from the fact that the system used 8-bit data for all the computations and control from A/D converter to Digital Firing Angle Control. The maximum decimal data that can be represented by a byte is 255. This limits the temperature range and power control. Of course, this range could be widened by extra hardware and software but this was unnecessary for this system.

The temperature control range is from 25°C to 89°C. This limitation comes from the above fact. The difference between limits is 64°C. Hence the temperature is controlled with 0.25°C steps.

The maximum and minimum slopes of temperature versus time diagram are also limited due to 8-bit operation. The lower limit is 5.8×10^{-2} °C/min and the upper limit is 15°C/min.

Of course, these limits also depend on the power of the heater in the tank. In the system realized only one heater of 600 W power was used. If this heater is divided into two 300 W heaters, then power control range would be extended.

Due to the dynamics of water in the tank, the sampling period should be as 200 mS as long. As it decreases the control applied to the system approaches to on-off control.

In this thesis a hardware based display unit is used. This could be a software based one which is scanned at some frequency, but this would be lessen the control capability of the microcomputer. Due to this reason the former way is adopted.

For the microcomputer system a double sided PCB was designed which caused some difficulty in its manufacture at the university workshop. However, the complexity of the circuit necessitate this, a single sided PCB could not be used.

CHAPTER VII

CONCLUSION

The complete hardware and firmware of a microcomputer based system controlling ac power is realised in the work described in this thesis. The microcomputer is designed such that it is very easy to adapt it to any other industrial process control. The instrumentation amplifier and digital phase angle control circuits can also be used freely in other applications.

The question whether the approach used in this thesis is an optimum one or not might be raised. If only a coarse control of power is required, then the system described is too sophisticated and expensive. There are many simpler and less expensive approaches. However, if a precise control is required for delicate processes a system like the one described is necessary. Considering the control accuracy that it provides, its cost (which is not forbiddingly high) is justified.

APPENDIX A.

TEMPERATURE VERSUS RESISTANCE TABLE OF PT 100

°C	Ohm	Diff.	°C	Ohm	Diff.	°C	Ohm	Diff.	°C	Ohm	Diff.	°C	Ohm	Diff.	°C	Ohm	Diff.
20	10.41		−160	35.48	0.42	−100	60.20	0.41	−40	84.21	0.40	± 0	100.00	0.39	+ 60	123.24	0.38
19	10.81	0.40	159	35.90	0.42	99	60.61	0.41	39	84.61	0.40	+ 1	100.39	0.39	61	123.62	0.38
18	11.20	0.39	158	36.31	0.41	98	61.01	0.40	38	85.00	0.39	2	100.78	0.39	62	124.01	0.39
17	11.60	0.40	157	36.73	0.42	97	61.42	0.41	37	85.40	0.40	3	101.17	0.39	63	124.39	0.38
16	11.99	0.39	156	37.15	0.42	96	61.82	0.40	36	85.79	0.39	4	101.56	0.39	64	124.77	0.38
15	12.39	0.40	155	37.57	0.42	95	62.23	0.41	35	86.19	0.40	5	101.95	0.39	65	125.16	0.39
14	12.78	0.39	154	37.98	0.41	94	62.63	0.40	34	86.59	0.40	6	102.34	0.39	66	125.54	0.38
13	13.18	0.40	153	38.40	0.42	93	63.04	0.41	33	86.98	0.39	7	102.73	0.39	67	125.92	0.38
12	13.57	0.39	152	38.82	0.42	92	63.44	0.40	32	87.38	0.40	8	103.12	0.39	68	126.30	0.38
11	13.97	0.40	151	39.23	0.41	91	63.85	0.41	31	87.77	0.39	9	103.51	0.39	69	126.69	0.39
10	14.36	0.39	150	39.65	0.42	90	64.25	0.40	30	88.17	0.40	10	103.90	0.39	70	127.07	0.38
09	14.78	0.42	149	40.07	0.42	89	64.65	0.40	29	88.57	0.40	11	104.29	0.39	71	127.45	0.38
08	15.19	0.41	148	40.48	0.41	88	65.06	0.41	28	88.96	0.39	12	104.68	0.39	72	127.83	0.38
07	15.61	0.42	147	40.90	0.42	87	65.46	0.40	27	89.36	0.40	13	105.07	0.39	73	128.22	0.39
06	16.03	0.42	146	41.31	0.41	86	65.86	0.40	26	89.75	0.39	14	105.46	0.39	74	128.60	0.38
05	16.45	0.42	145	41.73	0.42	85	66.27	0.41	25	90.15	0.40	15	105.85	0.39	75	128.98	0.38
04	16.86	0.41	144	42.14	0.41	84	66.67	0.40	24	90.55	0.40	16	106.23	0.38	76	129.36	0.38
03	17.28	0.42	143	42.56	0.42	83	67.07	0.40	23	90.94	0.39	17	106.62	0.39	77	129.74	0.38
02	17.70	0.42	142	42.97	0.41	82	67.47	0.40	22	91.34	0.40	18	107.01	0.39	78	130.13	0.39
01	18.11	0.41	141	43.39	0.42	81	67.88	0.41	21	91.73	0.39	19	107.40	0.39	79	130.51	0.38
00	18.53	0.42	140	43.80	0.41	80	68.28	0.40	20	92.13	0.40	20	107.79	0.39	80	130.89	0.38
99	18.96	0.43	139	44.21	0.41	79	68.68	0.40	19	92.52	0.39	21	108.18	0.39	81	131.27	0.38
98	19.38	0.42	138	44.63	0.42	78	69.08	0.40	18	92.92	0.40	22	108.57	0.39	82	131.65	0.38
97	19.81	0.43	137	45.04	0.41	77	69.48	0.40	17	93.31	0.39	23	108.95	0.38	83	132.03	0.38
96	20.23	0.42	136	45.45	0.41	76	69.88	0.40	16	93.71	0.40	24	109.34	0.39	84	132.41	0.38
95	20.66	0.43	135	45.87	0.42	75	70.29	0.41	15	94.10	0.39	25	109.73	0.39	85	132.80	0.39
94	21.08	0.42	134	46.28	0.41	74	70.69	0.40	14	94.49	0.39	26	110.12	0.39	86	133.18	0.38
93	21.51	0.43	133	46.69	0.41	73	71.09	0.40	13	94.89	0.40	27	110.51	0.39	87	133.56	0.38
92	21.93	0.42	132	47.10	0.41	72	71.49	0.40	12	95.28	0.39	28	110.89	0.38	88	133.94	0.38
91	22.36	0.43	131	47.52	0.42	71	71.89	0.40	11	95.68	0.40	29	111.28	0.39	89	134.32	0.38
90	22.78	0.42	130	47.93	0.41	70	72.29	0.40	10	96.07	0.39	30	111.67	0.39	90	134.70	0.38
89	23.21	0.43	129	48.34	0.41	69	72.69	0.40	9	96.46	0.39	31	112.06	0.39	91	135.08	0.38
88	23.63	0.42	128	48.75	0.41	68	73.09	0.40	8	96.86	0.40	32	112.44	0.38	92	135.46	0.38
87	24.06	0.43	127	49.16	0.41	67	73.49	0.40	7	97.25	0.39	33	112.83	0.39	93	135.84	0.38
86	24.49	0.43	126	49.57	0.41	66	73.89	0.40	6	97.64	0.39	34	113.22	0.39	94	136.22	0.38
85	24.92	0.43	125	49.99	0.42	65	74.29	0.40	5	98.04	0.40	35	113.61	0.39	95	136.60	0.38
84	25.34	0.42	124	50.40	0.41	64	74.68	0.39	4	98.43	0.39	36	113.99	0.38	96	136.98	0.38
83	25.77	0.43	123	50.81	0.41	63	75.08	0.40	3	98.82	0.39	37	114.38	0.39	97	137.36	0.38
82	26.20	0.43	122	51.22	0.41	62	75.48	0.40	2	99.21	0.39	38	114.77	0.39	98	137.74	0.38
81	26.62	0.42	121	51.63	0.41	61	75.88	0.40	1	99.61	0.40	39	115.15	0.38	99	138.12	0.38
80	27.05	0.43	120	52.04	0.41	60	76.28	0.40				40	115.54	0.39	100	138.50	0.38
79	27.47	0.42	119	52.45	0.41	59	76.68	0.40				41	115.93	0.39	101	138.88	0.38
78	27.90	0.43	118	52.86	0.41	58	77.07	0.39				42	116.31	0.38	102	139.26	0.38
77	28.32	0.42	117	53.27	0.41	57	77.47	0.40				43	116.70	0.39	103	139.63	0.37
76	28.74	0.42	116	53.68	0.41	56	77.87	0.40				44	117.08	0.38	104	140.01	0.38
75	29.17	0.43	115	54.09	0.41	55	78.27	0.40				45	117.47	0.39	105	140.39	0.38
74	29.59	0.42	114	54.49	0.40	54	78.66	0.39				46	117.86	0.39	106	140.77	0.38
73	30.01	0.42	113	54.90	0.41	53	79.06	0.40				47	118.24	0.38	107	141.15	0.38
72	30.43	0.42	112	55.31	0.41	52	79.46	0.40				48	118.63	0.39	108	141.52	0.37
71	30.86	0.43	111	55.72	0.41	51	79.85	0.39				49	119.01	0.38	109	141.90	0.38
70	31.28	0.42	110	56.13	0.41	50	80.25	0.40				50	119.40	0.39	110	142.28	0.38
69	31.70	0.42	109	56.54	0.41	49	80.65	0.40				51	119.78	0.38	111	142.66	.038
68	32.12	0.42	108	56.94	0.40	48	81.04	0.39				52	120.17	0.39	112	143.04	0.38
67	32.54	0.42	107	57.35	0.41	47	81.44	0.40				53	120.55	0.38	113	143.41	0.37
66	32.96	0.42	106	57.76	0.41	46	81.83	0.39				54	120.94	0.39	114	143.79	0.38
65	33.38	0.42	105	58.17	0.41	45	82.23	0.40				55	121.32	0.38	115	144.17	0.38
64	33.80	0.42	104	58.57	0.40	44	82.63	0.40				56	121.70	0.38	116	144.55	0.38
63	34.22	0.42	103	58.98	0.41	43	83.02	0.39				57	122.09	0.39	117	144.93	0.38
62	34.64	0.42	102	59.39	0.41	42	83.42	0.40				58	122.47	0.38	118	145.30	0.37
61	35.06	0.42	101	59.79	0.40	41	83.81	0.39				59	122.86	0.39	119	145.68	0.38

APPENDIX B.
THE MONITOR PROGRAM OF THE SYSTEM.

```
0010        ORG   8000H
0020 ;            "This program is prepare
d as firmware for"
0030 ;            "the thesis named PRECIS
E POWER CONTROL"
0040 ;            "ON TIME AXIS realised b
y RIFKI YAPAKCI"
0050 ;            "Start up routine"
0060 START: IM1
0070 ;            "Interrupt mode is set t
o 1"
0080        DI
0090        LD    SP,87FFH
0100 ;            "Stack pointer is initia
lized"
0110        LD    A,90H
0120        OUT   (7),A
0130 ;            "Configuration of 8255#1
"
0140        LD    A,0FFH
0150        OUT   (5),A
0160        LD    A,81H
0170        OUT   (0BH),A
0180 ;            "Configuration of 8255#2
"
0190        LD    HL,NUMDT
0200        CALL  ZERPO
0210        LD    HL,ZERO
0220        CALL  ZERPO
0230        LD    HL,LTSDT
0240        CALL  ZERPO
0250 ;            "All the system variable
s are initialised"
0260 TIMAD  EQU   8002H
0270 TEMAD  EQU   8004H
0280 NUMDT  EQU   8006H
0290 NUDP   EQU   8007H
0300 FLAGS  EQU   8008H
0310 LTSDT  EQU   8009H
0320 LTSTE  EQU   800CH
0330 LTSTI  EQU   800FH
0340 ZERO   EQU   8012H
0350 SSEND  EQU   8015H
0360 SENDS  EQU   8016H
0370 MINTS  EQU   8017H
0380 HRS    EQU   8018H
0390 MIDGT  EQU   8019H
0400 HRDGT  EQU   801BH
0410 RESEC  EQU   801DH
0420 POINT  EQU   801EH
0430 MUNCD  EQU   801FH
0440 MULER  EQU   8020H
0450 RESUL  EQU   8021H
0460 DIVND  EQU   8023H
0470 DISR   EQU   8025H
0480 QUOT   EQU   8026H
0490 REMA   EQU   8027H
0500 FITE   EQU   8028H
0510 DIF    EQU   8029H
```

```
0520 RETEM EQU  802AH
0530 ANGLE EQU  802BH
0540 RETE  EQU  802CH
0550 RETDG EQU  802DH
0560 ;          "Locations of the system
 variables"
0570       CALL ADCON
0580 ;          "Convertion start pulse
for A/D converter"
0590       LD   HL,8030H
0600       LD   (TIMAD),HL
0610       LD   HL,8130H
0620       LD   (TEMAD),HL
0630 ;          "TEMP & TIME add are set
"
0640       OR   20H
0650       JR   AD1
0660       NOP
0670       JP   TIM
0680 AD1   OUT  (6),A
0690 CAKYS CALL KEYSC
0700       JR   CAKYS
0710 ;          "Subroutine keyscane"
0720 ;          "There is no initial con
dition"
0730 ;          "Final condition: The nu
mber of key is in C"
0740 ;          "Registers used:A,B,C,D,
E,L"
0750 KEYSC LD   C,20
0760       CALL DELAY
0770       SUB  A
0780       OUT  (0AH),A
0790       LD   E,0FH
0800       IN   A,(0AH)
0810       AND  E
0820       CP   E
0830       RET  Z
0840       CALL DEBNC
0850       LD   C,0FFH
0860       LD   L,4
0870       LD   B,4
0880       LD   D,0EFH
0890 GROW  LD   A,D
0900       OUT  (0AH),A
0910       IN   A,(0AH)
0920       AND  E
0930       CP   E
0940       JR   NZ,KEYLC
0950       RLC  D
0960       LD   A,C
0970       ADD  L
0980       LD   C,A
0990       DJNZ GROW
1000 KEYLC INC  C
1010       RRA
1020       JR   C,KEYLC
1030 ;          "Key # is in C"
1040 KCONT IN   A,(0AH)
1050       AND  E
1060       CP   E
1070       JR   NZ,KCONT
1080       CALL DEBNC
1090 ;          "SUBROUTINE SJUMTB"
1100 ;          "This subroutine identif
y the key"
1110 ;          "Input : The # of key is
 in reg C"
```

```
1120 SJUMT LD   A,9
1130       CP   C
1140       JR   NC,NUMKY
1150       LD   HL,JUMTB
1160       LD   A,0FH
1170       SUB  C
1180       ADD  A
1190       LD   E,A
1200       LD   D,0
1210       ADD  HL,DE
1220       LD   E,(HL)
1230       INC  HL
1240       LD   D,(HL)
1250       EX   DE,HL
1260       JP   (HL)
1270 JUMTB DEFW RUN
1280       DEFW CLEAR
1290       DEFW STOP
1300       DEFW DEGIS
1310       DEFW TEMP
1320       DEFW TIME
1330 STOP  JP   START
1340 ;          "Numeric key routine:"
1350 ;          "Initial condition:The n
umber is in reg.C"
1360 ;          "Final condition :number
 is displayed and saved"
1370 ;          "Used registers: All the
 registers"
1380 NUMKY LD   A,3
1390       LD   HL,NUMDT
1400       LD   B,(HL)
1410       INC  B
1420       CP   B
1430       RET  C
1440       LD   (HL),B
1450       LD   A,C
1460       LD   HL,LTSDT+1
1470       LD   E,L
1480       LD   D,H
1490       INC  DE
1500       LD   C,2
1510       LD   B,0
1520       LDDR
1530       LD   (DE),A
1540       LD   HL,FLAGS
1550       BIT  5,(HL)
1560       JR   NZ,ZZZZZ
1570       CALL ZERLE
1580 ZZZZZ CALL LDTRI
1590       RET
1600 ;          "Display routine"
1610 ;          "Initial conditions:"
1620 ;          "The add.of first data t
o be displayed is in HL"
1630 ;          "The first digit locatio
n is in D reg"
1640 SENDT LD   B,3
1650       LD   E,0FFH
1660       LD   C,5
1670       OUT  (C),E
1680 SECON LD   A,(HL)
1690       OR   0F0H
1700       OUT  (5),A
1710       OUT  (C),D
1720       NOP
1730       LD   A,0FFH
```

```
1740        OUT   (C),A
1750        RLC   D
1760        INC   HL
1770        DJNZ SECON
1780        LD    D,0FFH
1790        OUT   (C),D
1800        RET
1810 ;              "Delay routine "
1820 ;              "Initial condition:"
1830 ;              "Amount of delay as mili
seconds is in C reg."
1840 DELAY LD    B,68H
1850 DLYCN NOP
1860        DJNZ DLYCN
1870        DEC   C
1880        JR    NZ,DELAY
1890        RET
1900 DEBNC PUSH BC
1910        LD    C,10
1920        CALL DELAY
1930        POP   BC
1940        RET
1950 ;              "Clear routine"
1960 ;              "It clears the last ente
red data ."
1970 CLEAR LD    HL,LTSDT
1980        CALL ZERPO
1990        CALL ZERRI
2000        SUB   A
2010        LD    (NUMDT),A
2020        RET
2030 ;              " Change routine"
2040 ;              " It changes the desired
 temp. time data pair"
2050 DEGIS CALL BCDBI
2060        AND   A
2070        LD    E,A
2080        LD    D,0
2090        LD    HL,8130H
2100        ADC   HL,DE
2110        LD    (TEMAD),HL
2120        LD    HL,8030H
2130        ADC   HL,DE
2140        LD    (TIMAD),HL
2150        LD    HL,LTSDT
2160        CALL ZERPO
2170        RET
2180 ;              "Temp routine "
2190 ;              "It takes last entered d
ata and save it"
2200 TEMP  LD    HL,FLAGS
2210        BIT   4,(HL)
2220        RET   NZ
2230        CALL BCDBI
2240        LD    HL,(TEMAD)
2250        LD    (HL),A
2260        INC   HL
2270        LD    (TEMAD),HL
2280        SUB   A
2290        LD    (NUMDT),A
2300        LD    HL,NUDP
2310        INC   (HL)
2320        LD    HL,LTSDT
2330        LD    DE,LTSTE
2340        LD    BC,0003H
2350        LDIR
2360        LD    HL,LTSDT
```

```
2370          CALL ZERPO
2380          CALL ZERLE
2390          LD   HL,FLAGS
2400          SET  4,(HL)
2410          BIT  5,(HL)
2420          JR   Z,TEMEN
2430          RES  4,(HL)
2440          RES  5,(HL)
2450          LD   HL,LTSTI
2460          LD   D,0F7H
2470          CALL SENDT
2480 TEMEN    RET
2490 BCDBI    AND  A
2500          LD   DE,NUMDT
2510          LD   A,(DE)
2520          LD   B,A
2530          LD   HL,LTSDT
2540          DEC  A
2550          ADD  L
2560          LD   L,A
2570          LD   A,3
2580          LD   C,0
2590          CP   B
2600          JR   NZ,SMSID
2610          LD   D,6
2620          CALL CALC
2630          LD   D,5
2640          CALL CALC
2650          LD   D,2
2660          CALL CALC
2670          DEC  B
2680          DEC  HL
2690 SMSID    LD   A,2
2700          CP   B
2710          JR   NZ,LSDIG
2720          LD   D,3
2730          CALL CALC
2740          LD   D,1
2750          CALL CALC
2760          DEC  B
2770          DEC  HL
2780 LSDIG    LD   A,(HL)
2790          ADD  C
2800          JR   C,BINUM
2810          RET
2820 CALC     LD   A,(HL)
2830 CONTS    ADD  A
2840          JR   C,BINUM
2850          DEC  D
2860          JR   NZ,CONTS
2870          ADD  C
2880          JR   C,BINUM
2890          LD   C,A
2900          RET
2910 ;             "Time routine"
2920 ;             "It takes last entered d
ata and save it"
2930 TIME     LD   HL,FLAGS
2940          BIT  5,(HL)
2950          RET  NZ
2960          CALL BCDBI
2970          LD   HL,(TIMAD)
2980          LD   (HL),A
2990          INC  HL
3000          LD   (TIMAD),HL
3010          CALL LDTLE
3020          SUB  A
```

```
3030            LD    (NUMDT),A
3040            LD    HL,LTSDT
3050            LD    DE,LTSTI
3060            LD    BC,0003H
3070            LDIR
3080            CALL  ZERRI
3090            LD    HL,LTSDT
3100            CALL  ZERPO
3110            LD    HL,FLAGS
3120            SET   5,(HL)
3130            BIT   4,(HL)
3140            JR    Z,TIMEN
3150            RES   4,(HL)
3160            RES   5,(HL)
3170            LD    HL,LTSTE
3180            LD    D,0FEH
3190            CALL  SENDT
3200 TIMEN      RET
3210 LDTLE      LD    HL,LTSDT
3220 SELE       LD    D,0F7H
3230            CALL  SENDT
3240            RET
3250 LDTRI      LD    HL,LTSDT
3260 SERI       LD    D,0FEH
3270            CALL  SENDT
3280            RET
3290 ZERLE      LD    HL,ZERO
3300            CALL  SELE
3310            RET
3320 ZERRI      LD    HL,ZERO
3330            CALL  SERI
3340            RET
3350 ZERPO      SUB   A
3360            LD    B,3
3370 ZEPOC      LD    (HL),A
3380            INC   HL
3390            DJNZ  ZEPOC
3400            RET
3410 BINUM      CALL  ZERRI
3420            SUB   A
3430            LD    HL,NUMDT
3440            LD    (HL),A
3450            LD    HL,LTSDT
3460            CALL  ZERPO
3470            RET
3480 ;                "Time interrupt routine"
3490 ;                "It shows the real time
after RUN"
3500 TIM        EXX
3510            EX    AF,A'F'
3520            LD    HL,SSEND
3530            INC   (HL)
3540            LD    A,(HL)
3550            CP    60
3560            JR    NZ,TIEND
3570            PUSH  HL
3580            LD    HL,(RESEC)
3590            INC   (HL)
3600            POP   HL
3610            SUB   A
3620            LD    (HL),A
3630            INC   HL
3640            INC   (HL)
3650            PUSH  HL
3660            LD    A,(POINT)
3670            XOR   20H
3680            LD    (POINT),A
```

```
3690        OUT   (6),A
3700        LD    HL,RETE
3710        LD    A,(HL)
3720        INC   HL
3730        PUSH  HL
3740        CALL  BIBCD
3750        INC   HL
3760        LD    (HL),0FFH
3770        POP   HL
3780        LD    D,0FEH
3790        CALL  SENDT
3800 ;            "Real temperature is dis
played"
3810        CALL  KEYSC
3820        POP   HL
3830        LD    A,(HL)
3840        CP    60
3850        JR    NZ,TIEND
3860        SUB   A
3870        LD    (HL),A
3880        INC   HL
3890        INC   (HL)
3900        LD    A,(HL)
3910        PUSH  AF
3920        LD    HL,MIDGT
3930        PUSH  HL
3940        CALL  BIBCD
3950        POP   HL
3960        LD    D,0F7H
3970        CALL  SENDT
3980        POP   AF
3990        CP    60
4000        JR    NZ,TIEND
4010        LD    HL,MINTS
4020        SUB   A
4030        LD    (HL),A
4040        INC   HL
4050        INC   (HL)
4060        LD    DE,HRDGT
4070        LDI
4080        PUSH  HL
4090        CALL  BIBCD
4100        POP   HL
4110        LD    D,0F7H
4120        CALL  SENDT
4130 TIEND  EX    AF,A'F'
4140        EXX
4150        EI
4160        RETI
4170 ;            "Binary to BCD convertio
n routine"
4180 ;            "Initial conditions:"
4190 ;            "Binary data is in Acc.H
L shows LSD"
4200 BIBCD  LD    B,0
4210        CP    10
4220        JR    C,LSID
4230 CONT1  SUB   10
4240        INC   B
4250        CP    10
4260        JR    NC,CONT1
4270 LSID   LD    (HL),A
4280        INC   HL
4290        LD    (HL),B
4300        RET
```

```
4310 ;          "Multiplication routine
 MUNCD*MULER=RESUL"
4320 ;          " Initial conditions:"
4330 ;          "Multiplicand and multip
lier are in related loc."
4340 ;          "Final condition: Result
 is in RESUL variable"
4350 MUTIP LD   HL,MUNCD
4360       LD   E,(HL)
4370       LD   D,0
4380       INC  HL
4390       LD   A,(HL)
4400       LD   HL,0
4410       LD   B,8
4420 MULT  ADD  HL,HL
4430       RLA
4440       JR   NC,CHCNT
4450       ADD  HL,DE
4460 CHCNT DJNZ MULT
4470       LD   (RESUL),HL
4480       RET
4490 ;          "RUN is the main control
routine"
4500 RUN   EI
4510 ;          "Interrupt is enabled"
4520       LD   HL,SSEND
4530       CALL ZERPO
4540       LD   HL,HRS
4550       CALL ZERPO
4560       LD   HL,HRDGT
4570       CALL ZERPO
4580 ;          "All time data is initia
lized"
4590       LD   HL,ANGLE
4600       LD   A,128
4610       LD   (HL),A
4620 ;          "At first ,half of the f
ull angle is set"
4630       CALL ZERLE
4640 ;          "Time display shows 0"
4650 COSTP CALL DITE
4660       CALL TIDIF
4670       LD   DE,(RESUL)
4680       LD   (DIVND),DE
4690       LD   A,(DIF)
4700       LD   (DISR),A
4710       CALL DIV1
4720 ;          "The time difference req
uired for one step inc"
4730       LD   HL,FITE
4740       LD   DE,RETEM
4750       LDI
4760 BBBBB LD   DE,RESEC
4770       LD   A,(DE)
4780       LD   HL,QUOT
4790       CP   (HL)
4800       JR   NZ,CONTR
4810 ;          "Is one step completed"
4820       SUB  A
4830       LD   (DE),A
4840       LD   HL,RETEM
4850       INC  (HL)
4860 ;          "Real temp is incremente
d one step"
4870       DEC  HL
4880       DEC  (HL)
4890 ;          "Step number is decremen
```

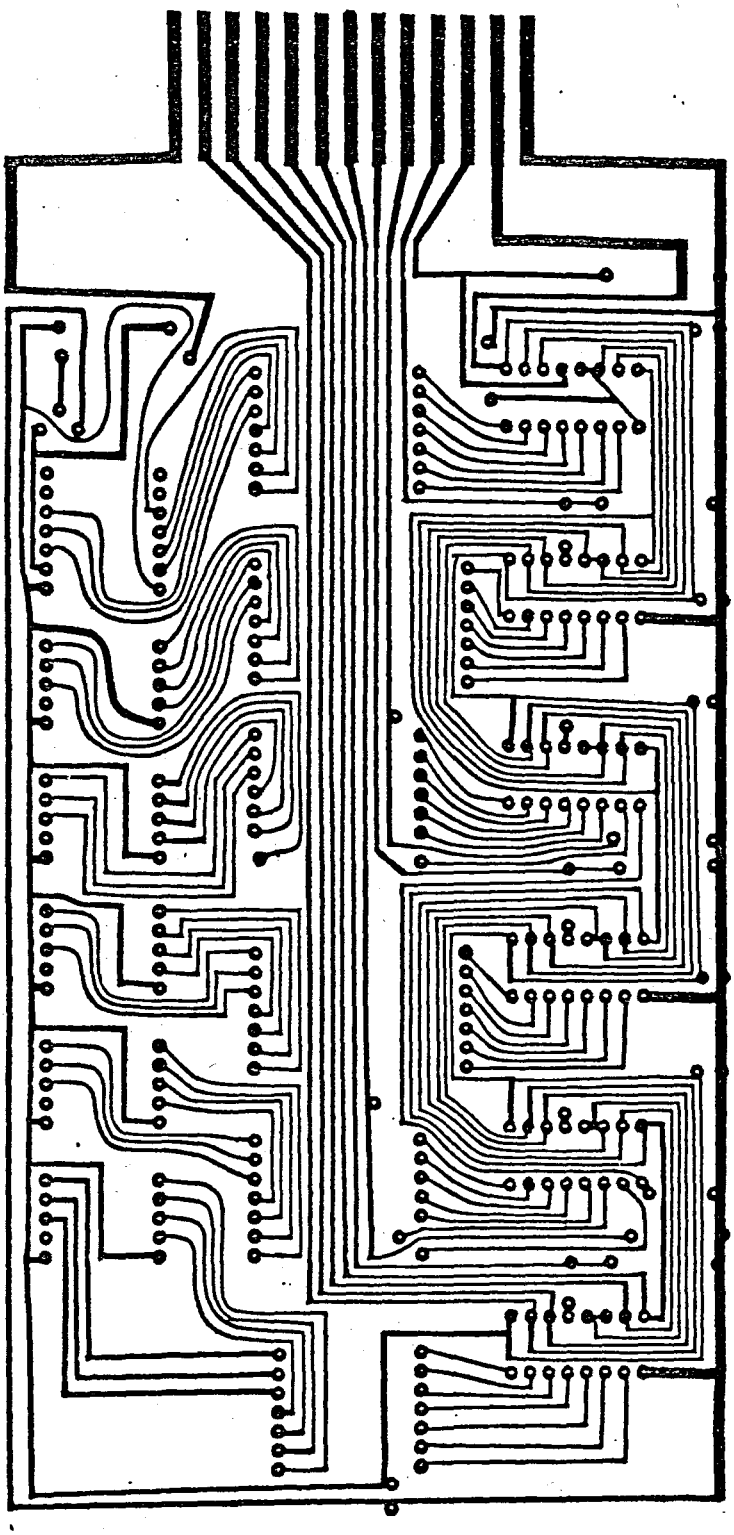
```
ted by one"
4900        SUB  A
4910        CP   (HL)
4920        JR   NZ,BBBBB
4930 ;           "is the sector completed
"
4940        LD   HL,REMA
4950        CP   (HL)
4960        JR   Z,ENDCH
4970        LD   DE,QUOT
4980        LDD
4990        INC  HL
5000        LD   (HL),A
5010        LD   HL,DIF
5020        INC  (HL)
5030        JR   BBBBB
5040 ENDCH  LD   HL,NUDP
5050        SUB  A
5060        CP   (HL)
5070        JR   NZ,COSTP
5080 ;           "Isthe control completed
?"
5090        JP   START
5100 ;           "Control function is com
pleted"
5110 CONTR  CALL COSTR
5120        IN   A,(4)
5130        PUSH AF
5140        LD   BC,(QUOT)
5150        PUSH BC
5160        LD   HL,QUOT
5170        LD   (HL),0
5180        CP   4
5190        JR   C,RRRRR
5200        LD   HL,DIVND
5210        LD   (HL),A
5220        INC  HL
5230        INC  HL
5240        LD   (HL),4
5250        CALL DIV1
5260 RRRRR  LD   A,(QUOT)
5270        ADD  25
5280        LD   HL,RETE
5290        LD   (HL),A
5300 ;           "Real temperature is sav
ed"
5310        POP  BC
5320        LD   (QUOT),BC
5330        POP  AF
5340        LD   HL,RETEM
5350        CP   (HL)
5360        PUSH AF
5370        LD   HL,ANGLE
5380        JR   Z,OTANG
5390        SUB  A
5400        CP   (HL)
5410        JR   Z,MING
5420 ;           "Is the angle minumum"
5430        DEC  (HL)
5440 MING   POP  AF
5450        JR   C,OTANG
5460        LD   A,254
5470        CP   (HL)
5480        JR   Z,MANG
5490 ;           "Is the angle maximum"
5500        INC  (HL)
```

```
5510 MANG  INC  (HL)
5520 OTANG LD   A,(HL)
5530       OUT  (8),A
5540       JP   BBBBB
5550 ;          "Calculation of the diff
erence of temp datum"
5560 DITE  CALL COSTR
5570       IN   A,(4)
5580       LD   (FITE),A
5590       LD   D,0
5600       LD   HL,NUDP
5610       LD   E,(HL)
5620       LD   HL,(TEMAD)
5630       SUB  A
5640       SBC  HL,DE
5650 ;          "First temperature data
address is calculated"
5660       LD   A,(HL)
5670       SUB  25
5680       LD   HL,MUNCD
5690       LD   (HL),A
5700       INC  HL
5710       LD   (HL),4
5720       CALL MUTIP
5730       LD   A,(RESUL)
5740       LD   HL,FITE
5750       SUB  (HL)
5760       LD   (DIF),A
5770       RET
5780 TIDIF LD   HL,NUDP
5790       LD   E,(HL)
5800       LD   D,0
5810       SUB  A
5820       LD   HL,(TIMAD)
5830       SBC  HL,DE
5840       LD   A,(HL)
5850       LD   (MUNCD),A
5860       LD   A,60
5870       LD   (MULER),A
5880       CALL MUTIP
5890       LD   HL,NUDP
5900       DEC  (HL)
5910       RET
5920 ;          "Division routine DIVND/
DISR=QUOT"
5930 ;          "Initial conditions:"
5940 ;          "Dividend and divisor ar
e in related variables"
5950 ;          "Final condition:Result
is in QUOT variable"
5960 ;          "Remainder is in REMA va
riable"
5970 DIV1  SUB  A
5980       LD   C,A
5990       LD   DE,(DISR)
6000       LD   D,A
6010       LD   HL,(DIVND)
6020 DIVCO LD   A,H
6030       AND  A
6040       JR   NZ,CCOMP
6050       LD   A,L
6060       SUB  E
6070       JR   C,RMAIN
6080 CCOMP AND  A
6090       SBC  HL,DE
6100       INC  C
```

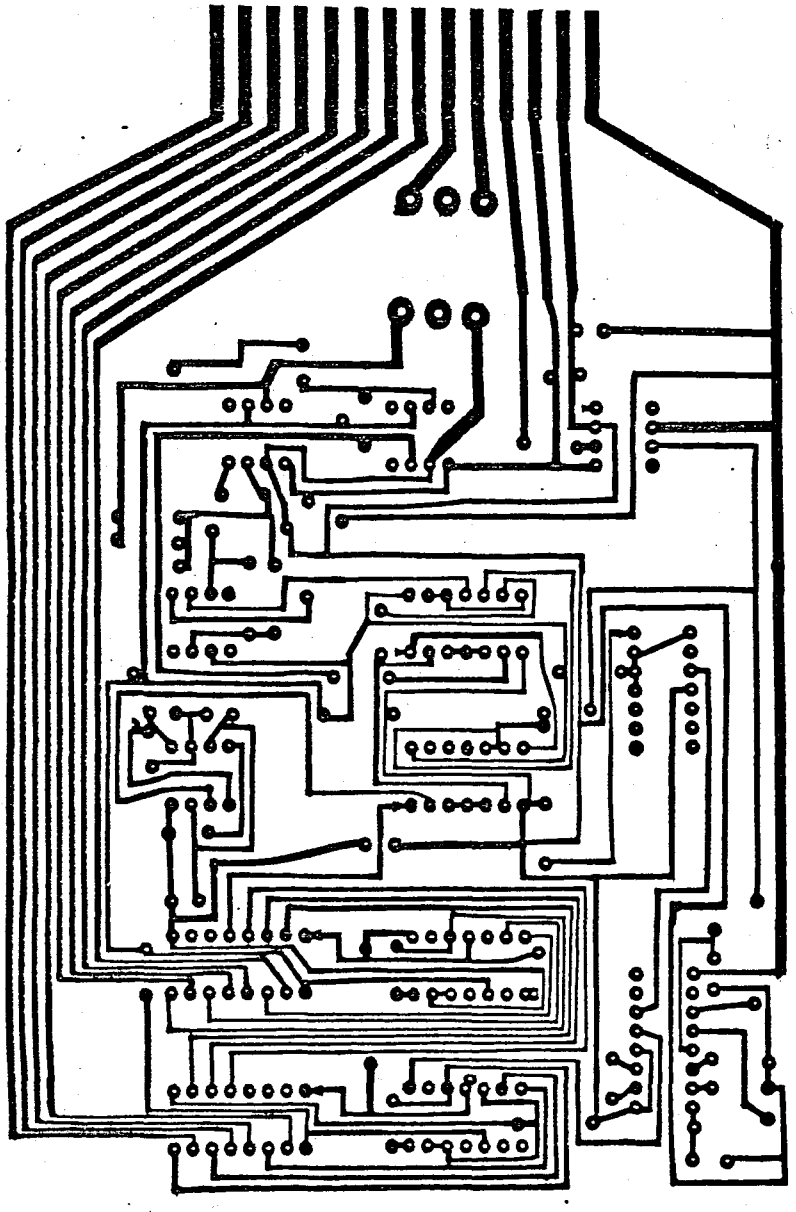
```
6110            JR    DIVCO
6120 RMAIN      LD    DE,QUOT
6130            LD    A,C
6140            LD    (DE),A
6150            INC   E
6160            LD    A,L
6170            LD    (DE),A
6180            RET
6190 ;                "This routine sends conv
. start pulse to A/D con"
6200 ADCON      LD    A,(POINT)
6210            AND   0EFH
6220            OUT   (6),A
6230            PUSH  AF
6240            LD    C,2
6250            CALL  DELAY
6260            POP   AF
6270 ADC1       OR    10H
6280            OUT   (6),A
6290            RET
6300 CONSTR     CALL  ADCON
6310            LD    C,1
6320            CALL  DELAY
6330            RET
6340            END
```

APPENDIX C.

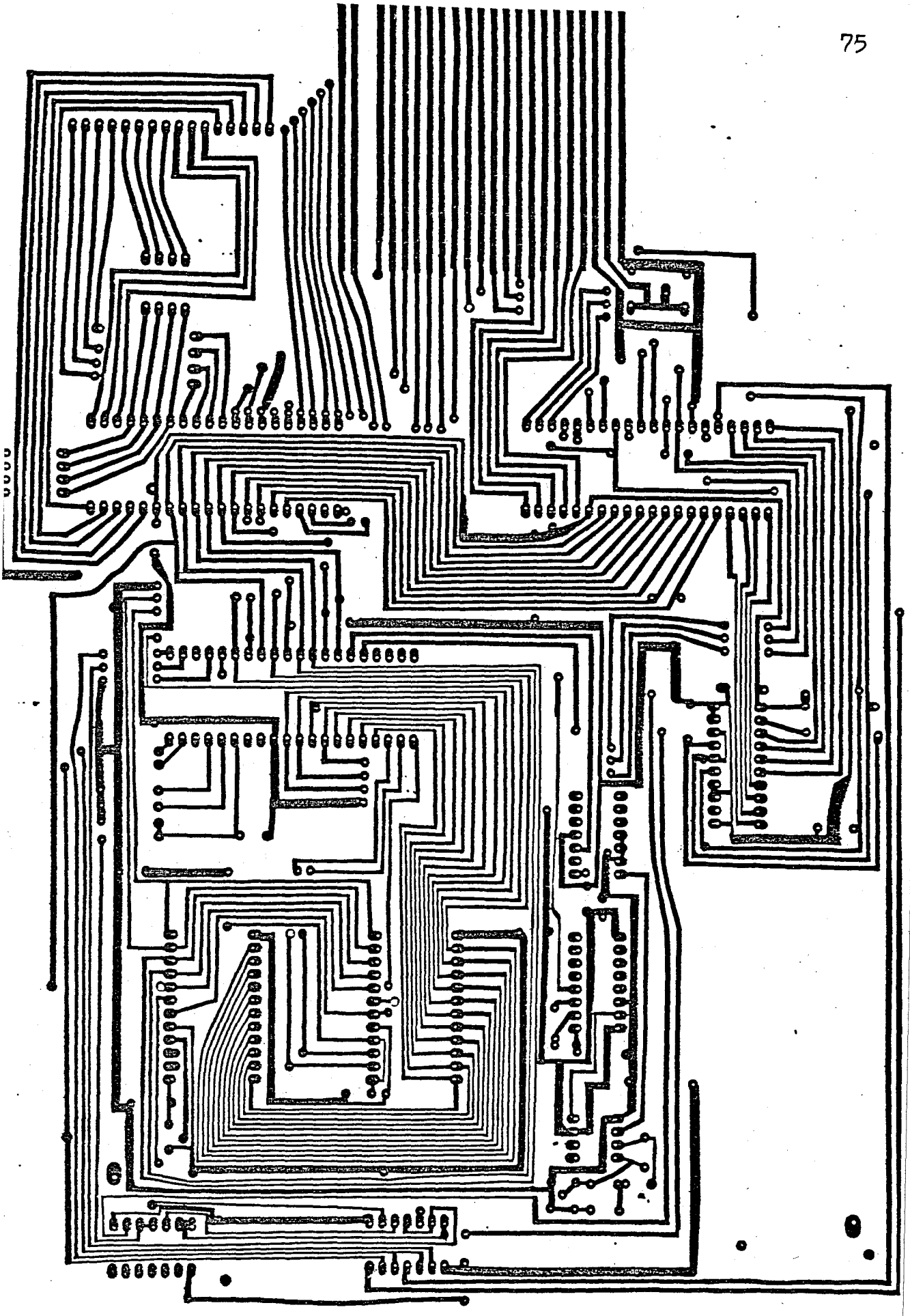
THE PCB LAYOUTS OF SYSTEM UNITS.



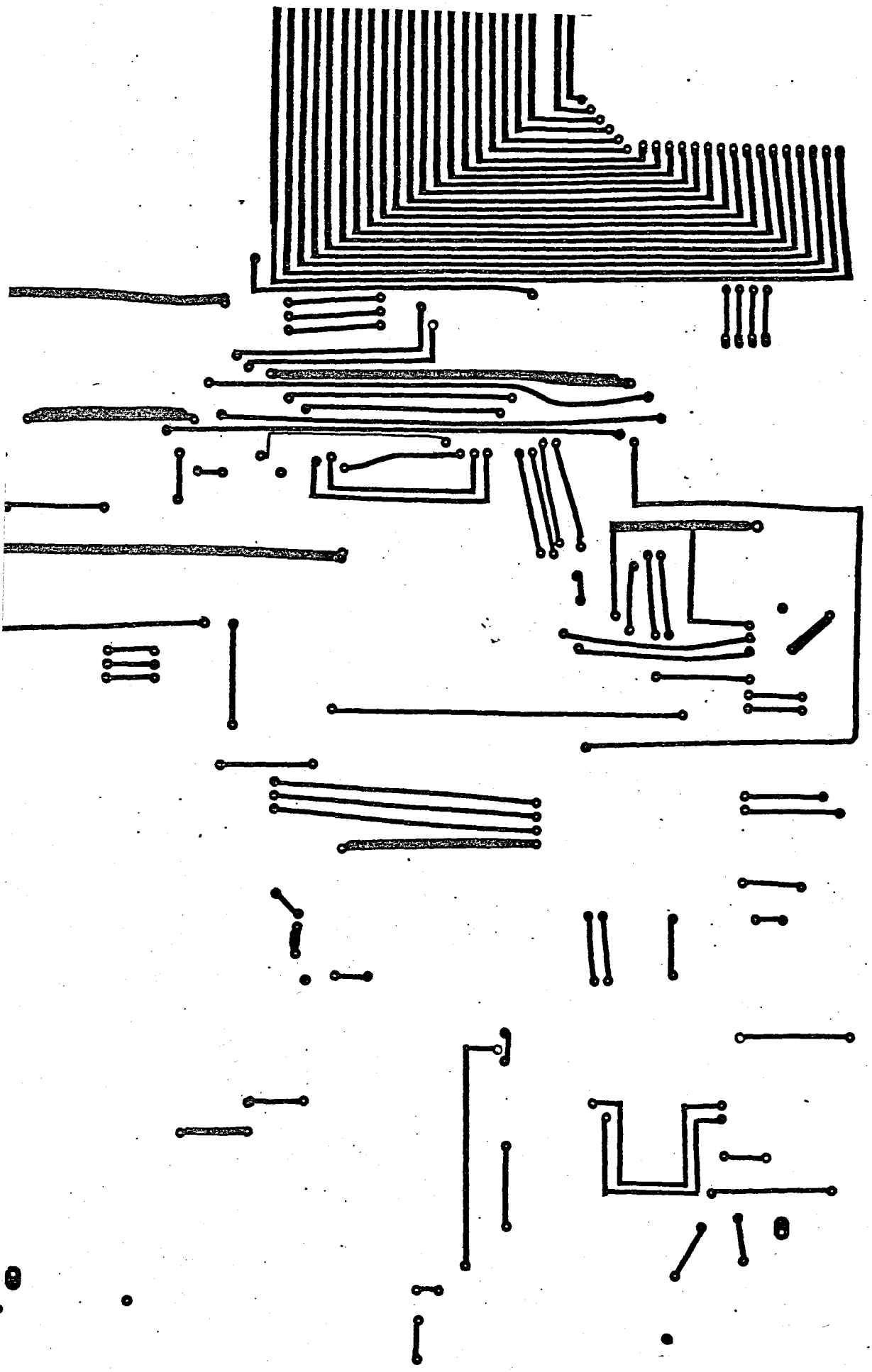
The PCB Layout of Display Unit.



The PCB Layout of Digital Firing Angle Control Circuit.



The PCB Layout of the Microcomputer (Underside)



The PCB Layout of the Microcomputer (Comppnent side)

APPENDIX D

OPERATING INSTRUCTIONS

TIME: The time data is entered by this instruction. It is given as minutes. This data is given relatively to the end of preceding sector. That is, the beginning of the given data is the end of the former sector. The maximum time data can be entered is 255 minutes.

TEMP: The temperature data is given by this instruction. It is given in ^{o}C . The maximum time data can be entered is 88 ^{o}C.

CLEAR: It is used for clearing the wrong data before being entered.

CHANGE: It is used for changing the data pair before RUNning the system. The data pair number which will be changed is entered first, then the CHANGE key is pressed. The data pair given this time will be changed by the old one.

RUN: This instruction is used for running the system.

STOP: This is used to stop the running system.

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