ÇANKAYA UNIVERSITY
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
ELECTRONIC AND COMMUNICATION ENGINEERING

MASTER THESIS

DESIGN AND IMPLEMENTATION OF A 1kW SINGLE PHASE GRID TIE INVERTER

OĞUZ ŞİMŞEK

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Title of the Thesis: **Design and Implementation of a 1kW Single Phase Grid Tie Inverter**

Submitted by **Oğuz ŞİMŞEK**

Approval of the Graduate School of Natural and Applied Sciences, Çankaya University

Prof. Dr. Taner ALTUNOK
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science

Prof. Dr. Celal Zaim ÇİL
Head of Department

This is to certify that I have read this thesis and that in my opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

Assoc. Prof. Dr. M. Timur AYDEMİR
Co-Supervisor

Assoc. Prof. Dr. Klaus Werner SCHMIDT
Supervisor

Examination Date: 19.09.2013

Examining Committee Members

Assistant Prof. Dr. Ulaş BELDEK (Çankaya Univ.)

Assoc. Prof. Dr. Klaus Werner SCHMIDT (Çankaya Univ.)

Assoc. Prof. Dr. M. Timur AYDEMİR (Gazi Univ.)

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Name, Last Name : Oğuz Şimşek

Signature :

Date : 19.9.2013

ABSTRACT

DESIGN AND IMPLEMENTATION OF A 1kW SINGLE PHASE GRID TIE INVERTER

ŞİMŞEK, Oğuz

M.Sc., Department of Electronics and Communication Engineering

Supervisor: Assoc. Prof. Dr. Klaus Werner SCHMIDT

Co-Supervisor: Assoc. Prof. Dr. M. Timur AYDEMİR

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Renewable energy sources and their power processing equipment are gaining increasing importance in the market. Excess of energy harvested from a renewable source is either stored for future use or sold to other users that are in need of electrical energy at the time of harvesting. Since storage of excess energy is an inefficient and costly process, a better way of dealing with excess energy is to transfer the energy to the interconnected power grid by means of appropriate power processing. In this thesis work, design and implementation of a high efficiency power processing equipment known as Grid Tie Inverter (GTI) to achieve energy transfer to the grid is studied.

The target of this study is to convert low voltage direct current (DC) electrical energy harvested from the photo voltaic (PV) panels to high voltage alternating current (AC). The magnitude and phase of the processed alternating current is then controlled in a way such that the power flows towards the grid with a low DC and low reactive component. To achieve this goal, the voltage of the PV panels is stepped up to an appropriate DC link voltage by using a boost type converter known as the Z-Source. The required DC analysis and transfer functions

of the Z-Source converter are obtained by the circuit averaging technique and a proportional-integral (PI) regulator is designed and implemented to stabilize the DC link voltage. The stabilized DC link voltage is then converted to alternating current using a full bridge inverter. The required grid voltage and phase information is obtained by digital implementation of a single phase time-delay based synchronous reference frame phase locked loop circuit (TDB-SRF PLL). The control of the current flowing into the grid is carried out by using the D-Q synchronous reference frame approach. Hereby, the direct (D) and quadrature (Q) components of the grid current are calculated using Park's transformation. The magnitudes of the D and Q components are stabilized by separate digital PI controllers. The outputs of the PI controllers are then converted back to the rotating reference frame using the inverse Park's transformation. The output of the transformation is used as a control signal to drive the full bridge inverter. The scope of the thesis comprises both the modeling and simulation of the GTI components and the design and implementation of a prototype GTI. A thorough experimental evaluation confirms the practicability of the proposed design.

Keywords: Photo-voltaic panels, grid tie inverter, Z-source inverter, D-Q control, synchronous reference frame, phase locked loop

ÖZ

1 kW TEK FAZLI ŞEBEKE BAĞLANTILI EVİRİCİ TASARIMI VE UYGULAMASI

ŞİMŞEK, Oğuz

Yüksek Lisans, Elektronik ve Haberleşme Mühendisliği

Tez Yöneticisi: Assoc. Prof. Dr. Klaus Werner SCHMIDT

Ortak Tez Yöneticisi: Assoc. Prof. Dr. M. Timur AYDEMİR

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Günümüz şartlarında yenilenebilir enerji kaynakları ve bu kaynakların kullanımını mümkün kılan güç kaynaklarının pazardaki önemi giderek artmaktadır. Yenilenebilir kaynaklar kullanılarak üretilen enerjinin üretim anında ihtiyaç fazlası olan kısmı, daha sonra kullanılmak üzere depolanmakta ya da üretim anında enerji ihtiyacı olan kullanıcılara satılmaktadır. Enerji depolamanın pahalı ve düşük verimli bir işlem olması sebebi ile, üretim anında ihtiyaç fazlası olan enerjinin uygun güç çevrim yöntemleri kullanılarak enterkonnekte şebekeye aktarılması daha verimli bir yöntem olarak görülmektedir. Bu tez çalışmasında şebekeye enerji aktarılmasında kullanılan ve Şebeke Bağlantılı Evirici olarak bilinen yüksek verimli bir güç kaynağının tasarımı ve uygulaması yapılmıştır. Bu çalışmanın amacı fotovoltaik panellerden elde edilen düşük gerilimli doğru akım elektrik enerjisini yüksek voltajlı alternatif akıma dönüştürmek, üretilen alternatif akımın genliği ve fazını şebekeye aktarılan güç, düşük doğru akım ve tepkisel güç ihtiva edecek şekilde kontrol etmektir. Bu amaca ulaşmak için fotovoltaik panellerden sağlanan düşük voltajlı doğru akım, Z-Kaynak olarak bilinen yükselten çevirici

ile uygun doğru akım bara gerilimine yükseltilmektedir. Doğru akım bara gerilimininin kontrolü için gerekli doğru akım analizi ve gerekli transfer fonksiyonları Ortalama Eşdeğer Devre yöntemine göre bulunmuş ve doğru akım bara gerilimi Alan-Oransal kontrol yöntemi ile belirlenen değerde dengelenmiştir. Dengelenmiş doğru akım bara gerilimi Tam Köprü Evirici vasıtası ile alternatif akıma dönüştürülmüştür. Şebeke akımının kontrolü için gerekli şebeke voltajı genlik ve faz bilgileri geciktirme tabanlı, örnek eşzamanlı eksen takımı yöntemine göre çalışan faz kilitlemeli çevrim devresinin mikrodenetleyicide sayısal olarak uygulanması ile elde edilmiştir. Şebeke akımı, örnek eşzamanlı eksen takımı (D-Q) yöntemi ile kontrol edilmiştir. Şebeke akımının D ve Q eksenleri Park dönüşümü kullanılarak hesaplanmış ve bu eksenlerin genlikleri her biri için birer Alan-Oransal denetleyici kullanılarak dengelenmiştir. Denetleyici çıkışları ters Park dönüşümü kullanılarak Döner Eksen bileşenlerine dönüştürülmüş ve Tam köprü evirici devresinin kontrol sinyali elde edilmiştir. Tez çalışması kapsamında Şebeke Bağlantılı Evirici bölümlerinin benzetim, simülasyon ve uygulama örneğinin tasarım ve uygulaması bulunmaktadır. Önerilen tasarımın uygulanabilir olduğu deneysel çalışma sonuçları ile doğrulanmıştır.

Anahtar Kelimeler: Foto voltaik panel, Şebeke bağlantılı evirici, Z- Kaynak , D-Q kontrol, Örnek eş zamanlı eksen takımı, Faz kilitlemeli çevrim.

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To my dear wife
Müzeyyen ŞİMŞEK
and daughters
Gizem ŞİMŞEK
Zeynep Naz ŞİMŞEK

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LIST OF ABBREVIATIONS

CCM	Continuous Conduction Mode
CMRR	Common Mode Rejection Ratio
DAC	Digital to Analog Converter
DCM	Discontinuous Conduction Mode
D-Q	Direct-Quadrature
DSP	Digital Signal Processor
FB	Full Bridge
GTI	Grid Tie Inverter
IGBT	Insulated Gate Bipolar Transistor
MIPS	Mega Instructions Per Second
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
Msps	Mega Samples Per Second
OSC	Oscilloscope
PI	Proportional Integral
PID	Proportional Integral Derivative
PLL	Phase Locked Loop
PV	Photovoltaic
PWM	Pulse Width Modulation
SG	Signal Generator
SRF	Synchronous Reference Frame
TDB	Time Delay Based
VCO	Voltage Controlled Oscillator
VSI	Voltage Source Inverter
ZSC	Z Source Converter
ZSI	Z Source Inverter

CHAPTER I

LITERATURE REVIEW AND THE GTI

1.1 INTRODUCTION

Grid tie inverters are one of the most important part of photovoltaic (PV) power generation systems. Low voltage electrical energy harvested from the photovoltaic panels is converted to the usable high voltage alternating current (AC) and sent to the interconnected grid by using grid tie inverters. Sending the generated energy into the grid mitigates the problem of storing excess energy available at the time of production. Grid connection can be regarded as some kind of energy storage because the energy sent to the grid can be used anytime. Grid connection also provides a power balancing feature. As an example, a washing machine requires as much as 2kW of power for half an hour to heat up the water, A PV installation with a peak power of 1kW cannot provide the required power although it can furnish the heat up energy within one hour. The power balancing feature becomes a big advantage for small power PV generation installations because the maximum power capability of the inverters can be sized according to the available power rating of the PV panels.

1.2 BASIC STRUCTURE OF THE PV SYSTEMS

The basic structure of a PV System is shown in fig. 1.1. The system consists of two components; PV panels for harvesting the energy and the grid tie inverter (GTI) for processing and sending the energy to the grid. There are two mandatory tasks in grid connected PV systems: Extraction of the maximum available power from the PV panels and injecting DC free active power into the grid. The injected current should be in phase with the grid voltage and should have a pure sinusoidal wave shape.[3] As will be introduced in this chapter, PV panels behave as a current source with a magnitude of current that depends on the irradiation. The output

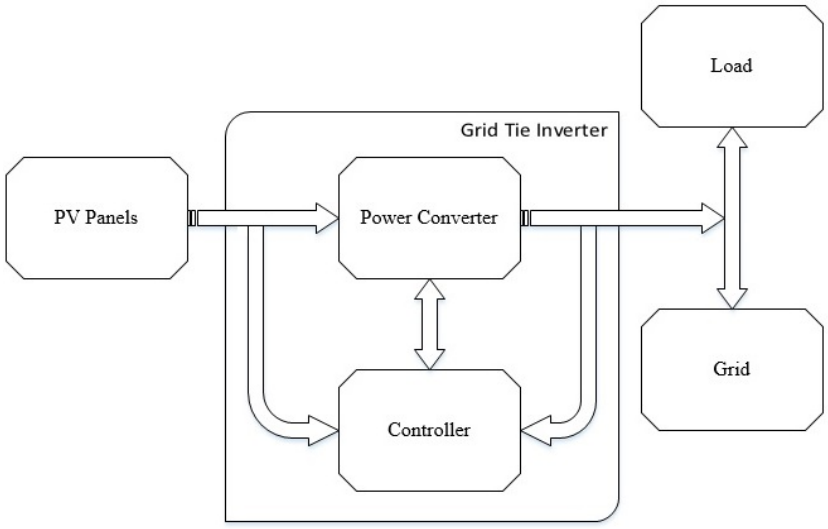

Figure 1.1 Basic Structure of a PV System.

voltage and thus the output power of the PV panels will greatly vary depending on the load impedance. The output current and the corresponding output voltage of the PV panels should be kept at a point such that the maximum available power can be extracted. This process is called maximum power point tracking (MPPT). The general idea of implementing MPPT is to observe the output power and track the maximum power point of the PV panels by applying a small change in the input impedance of the power converter.

Injecting active power into the grid may be achieved by a single or multistage power processing. Depending on the operating voltage of the PV panels, it may be required to boost the voltage of the panels to an appropriate DC link voltage. Having an appropriate DC link voltage, it is required to produce an output current which should be sinusoidal and in phase with the grid voltage. Boosting the voltage of the PV panels and injecting sinusoidal active power into the grid requires a control strategy. The control strategy for the grid tie inverter mainly consists of two cascaded voltage and current loops [4] for controlling the power and a phase locked loop (PLL) to obtain grid voltage vector amplitude and phase informations of the grid. Usually there is a fast internal current loop which regulates the grid current and hence determines the quality of the injected power. A slower external loop is used to regulate the DC link voltage.

1.3 PV MODEL

The basic model of a PV cell is shown in fig. 1.2. A PV panel is made up of this cell by connecting many cells in series as shown in fig. 1.5. The cell produces a current with a magnitude that depends on the irradiation. The output current and voltage of a PV cell is also influenced by the cell temperature. Increase in the cell temperature greatly reduces the output voltage and hence the output power. Fig. 1.3 and fig. 1.4 shows the irradiation and temperature dependence of a PV panel [9].

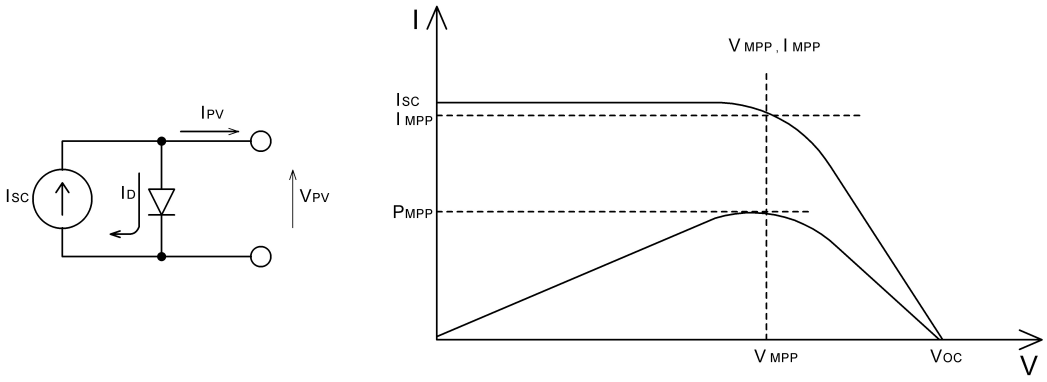

Figure 1.2 PV Cell Model and Output Characteristics.

When no current is drawn from the cell, the open circuit voltage V_{OC} is present at the output of the PV cell. The maximum current supplied from the cells for a specific irradiation is the short circuit current I_{SC}. As can be seen from fig. 1.2, the output power considerably varies with the change of the output voltage. There is a point in the power curve at which the output power is maximum for given athmospheric and irradiation conditions. This point is called the maximum power point P_{MPP}. To utilize the maximum available energy, the operating point P_{MPP} should be tracked. The process of tracking this point is named as maximum power point tracking (MPPT). There are many methods and papers describing different MPPT algorithms. Among all the methods, the "perturb and observe" method is the most popular approach. The references [10, 11, 12, 13, 14] give detailed information of the most popular methods for tracking the maximum power point.

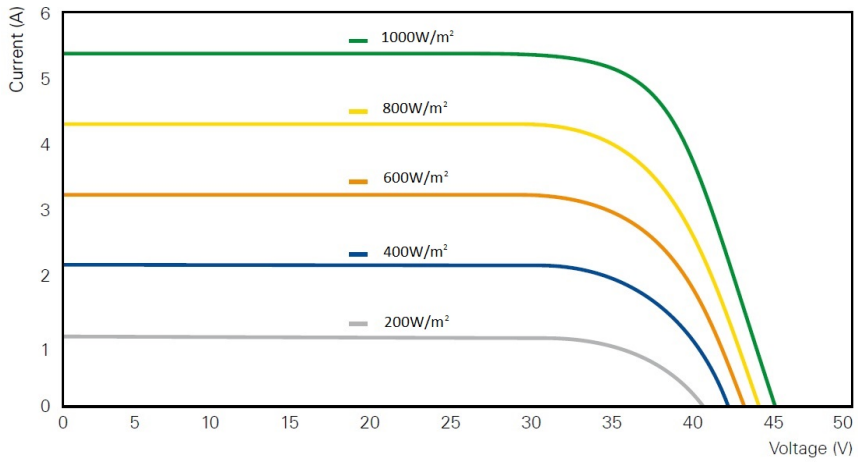

Figure 1.3 The Irradiance Dependence of a PV Panel [9].

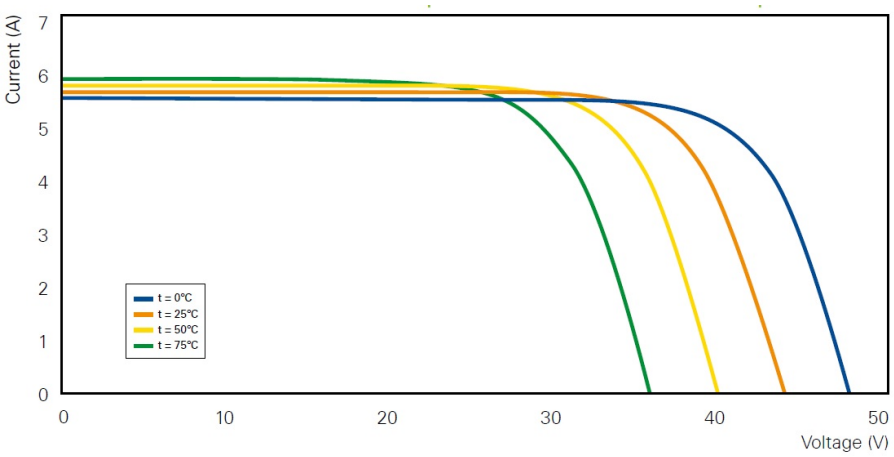

Figure 1.4 The Temperature Dependence of a PV Panel [9].

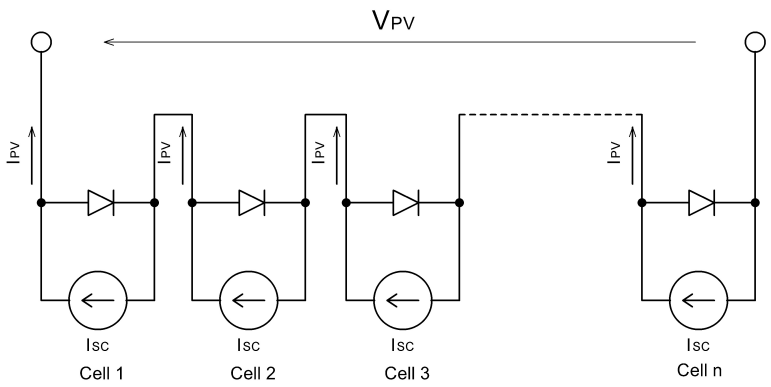

Figure 1.5 Multiple Cell Structure of a PV Panel.

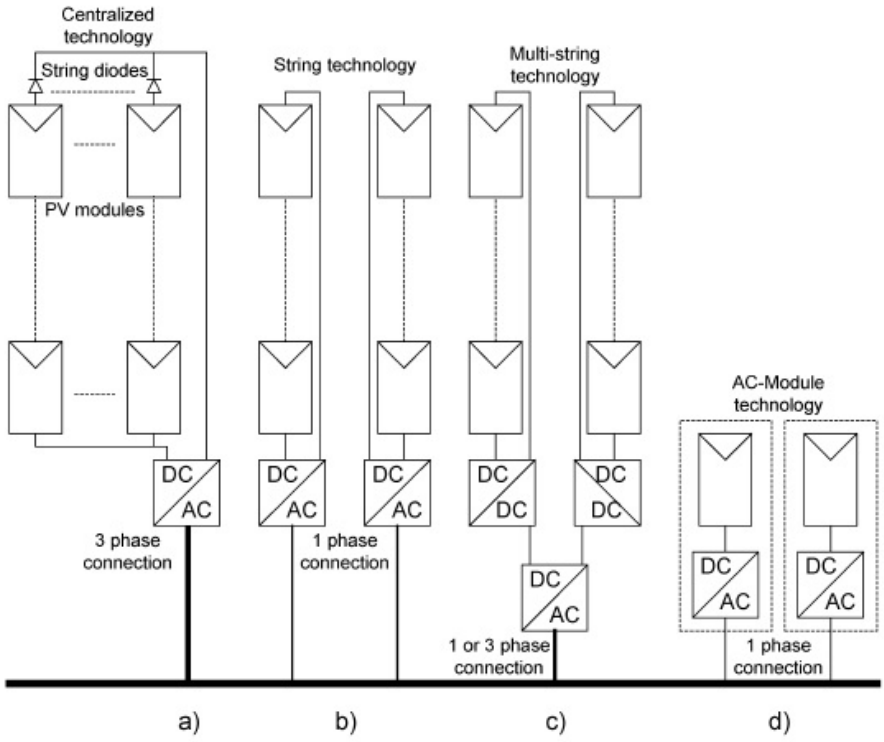

Figure 1.6 Overview of PV Technologies. (a) Centralized Technology. (b) String Technology. (c) Multistring Technology. (d) AC Module Technology.

1.4 PAST AND PRESENT PV SYSTEMS

The technologies used in PV systems are illustrated in fig. 1.6 [5]. The past technology (a) was based on centralized inverters that interface a large number of PV modules with the grid. PV modules are divided into series connections which are called "Strings". Using the String structure, a DC-DC boost stage as is needed for low voltage PV modules is avoided. In order to reach higher power levels the strings are connected in parallel through the string diodes. It has to be noted that the centralized technology suffers from several drawbacks such as: High voltage DC cables between the PV panels, losses in the string diodes, inefficiencies caused by the centralized MPPT and degraded design flexibility because of a large number of PV module connections.

The present technology is shown in fig. 1.6(b,c). The system consists of string inverters and an AC module. The string inverter (b) is a reduced version of the centralized inverter. In the string inverter, a single string of PV modules is connected to the inverter. The input voltage may be high enough to avoid voltage boosting to match the required DC link voltage [5]. To avoid the voltage boosting

stage, roughly 16 PV modules in series are required for European systems. The total open-circuit voltage for 16 PV modules may reach as high as 720 V. In this case, 1000-V rated MOSFET/IGBT transistor components are required in order to allow for a 75% voltage derating of the semiconductors. High open circuit voltage may become a problem for the switching components since high voltage withstanding capability of MOSFET/IGBT increases switching and conduction losses. The advantage of this system over the centralized inverter is that there are no losses associated with string diodes and separate MPPTs can be applied to each string. This increases the overall efficiency and reduces the cost. The AC module depicted in fig. 1.6(d) is the integration of the inverter into the PV module, forming a single electrical device. The inverter can be designed according to the very specific PV module since there is no need of connecting another PV module to the inverter. The modular structure allows easy expandability of the system and system setup does not require skilled technical personal. This allows mass production and distribution of the system at lower manufacturing costs. The study presented in this thesis can be applied to both string and AC module technology whereas the focus is given to the string technology.

1.5 STRUCTURE OF THE GRID TIE INVERTER

There are two main topology groups for grid tie inverters: The inverters with and without galvanic isolation. Galvanic isolation can be on the DC side with high frequency transformers or on the AC side with bulky grid frequency transformers [8]. DC and AC side galvanic isolation is shown in fig. 1.7 and fig. 1.8, respectively. Galvanic isolation provides safety but reduces the overall efficiency. Higher efficiency, smaller size and lower costs are possible if the transformers providing galvanic isolation are left out [7]. Without galvanic isolation, safety issues arise because of the PV panels parasitic capacitance. This parasitic capacitance leads to the flow of leakage currents between the PV panel and the ground. According to the standards, there are certain limitations for the average leakage currents. [7] depicts the limits for leakage currents according to the German standard VDE 0126-1-1. Elimination of the isolation transformers may also lead to DC current injection to the grid. This DC current may saturate the power transformers and most standards limit the maximum DC current injection to 0.5 to 1 percent of the rated output current.

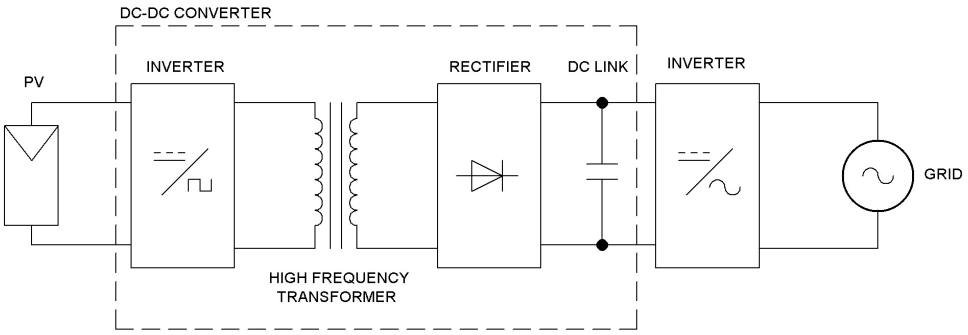

Figure 1.7 Grid Tie Inverter With DC Side Galvanic Isolation.

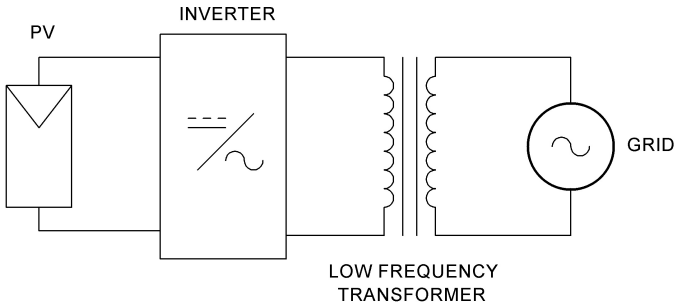

Figure 1.8 Grid Tie Inverter With AC Side Galvanic Isolation.

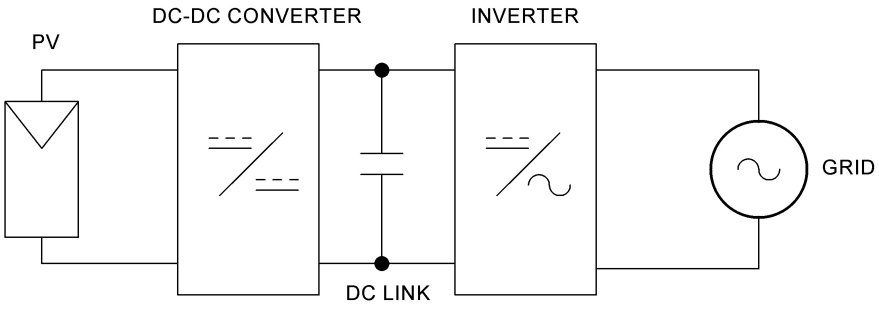

Figure 1.9 Grid Tie Inverter Without Galvanic Isolation.

The transformer-less grid tie inverter which is the focus of this thesis is shown in fig. 1.9.

1.6 CONTROL OF THE GRID TIE INVERTER

The DC to AC section of the grid tie inverter is expected to deliver only active power to the grid. Reactive power that circulates between the grid and the inverter degrades the system efficiency and many international standards limit the maximum allowable reactive power flow to some small value. In order to achieve active power flow the steady state error between the desired and actual grid current should be kept zero at grid frequency and the current should be in phase with the grid voltage. Since the signals to be controlled are at the grid frequency, simple proportional-integral (PI) controllers cannot be used because of the finite gains of PI controllers at frequencies other than zero [15]. There are many control techniques in the literature to ensure infinite control loop gain at grid frequency to enable exact tracking of reference signals. D-Q control [16, 17, 18, 19, 20] is one of the techniques that provide stationary exact tracking of the grid current which will be applied in this thesis. The main advantage of the D-Q control is the transformation of the time varying signals into DC signals which provide simple PI controllers to be used to track the sinusoidal reference current.

1.7 MOTIVATION, OBJECTIVES AND THE SCOPE

It is evident that the interest in the renewable energy sources increase everyday. Out of these renewable sources, PV systems are one of the most important source of energy. The production processes and the efficiency of the PV panels have reached a point where the cost per kWh is attractive and usage of PV systems is increasing all over the world. The grid tie inverters are the integral part of the system and the demand for this inverter is in parallel to the PV panels. Development of a prototype of the GTI is very important from the industrial aspect since there is an increasing demand in the market. The trend in the market is towards the scalable, efficient, light and reliable PV systems. The efficiency, cost and the reliability of the GTI can be improved by minimizing the active stages and using transformer-less topologies (see fig. 1.9). The active stages can be minimized using the Z-Source Inverter (ZSI) [1] topology. In this topology, the DC-DC voltage boost and DC-AC inverter stages can be combined into a single stage without increasing the number of active components. The ZSI also improves the reliability by removing the shoot-through phenomena which is one of the major issues for full bridge voltage source inverters (FBVSI) used in the

DC-AC stages. In this thesis, a prototype of a high efficiency single stage, single phase ZSI-Grid tie inverter is developed. The first contribution of this thesis is a detailed design procedure of the GTI based on parameters such as minimum and maximum output power, minimum and maximum grid voltage and minimum PV voltage. The second contribution of the thesis is the creation of detailed simulation models and control algorithms for all GTI components. In particular, the simulation models support the choice of the design parameters and enable the verification of system parameters and control algorithms. The third contribution is the verification of the designed circuit by real implementation results. Finally, the fourth contribution is the detailed implementation of the control algorithms of the GTI in a microcontroller and the validation of the overall design by hardware experiments. In summary, the objective of this study is to produce a prorotype of a Grid tie inverter that can serve as a platform for further improvements toward design of an industrial product. Hereby, the main focus of the thesis work is on boosting the low voltage PV panel output to 450V DC link voltage and sending power to the grid. Hence, the scope of this study is the design of a Z-Source grid tie inverter which is powered by a DC current limited voltage source.

1.8 OUTLINE OF THE THESIS

The remainder of this thesis is organized as follows: In Chapter 2, mathematical modeling of the Z-Source converter, D-Q control and PLL circuit is described. Chapter 3 elaborates on the design of the Grid tie inverter and related simulations. Chapter 4 presents the results obtained from the implementation and in Chapter 5, conclusions of the thesis as well as future research objectives are presented.

CHAPTER II

MODELING THE GTI

2.1 INTRODUCTION

The grid tie inverter (GTI) is a power processing equipment which converts a low voltage DC power into an AC power and pushes this power into the grid. Achieving this goal requires in general incorporating at least two stages; power and control blocks. Control block design can be carried out if the model of the power stage is known or identifiable. Mathematical modeling is one of the methods to determine the behavior of a system in terms of mathematical equations. In this thesis the behavior of the system is analyzed and linear models of the GTI components in the form of transfer functions for control design are derived. The block diagram of the grid tie inverter studied in this thesis is shown in fig. 2.1.

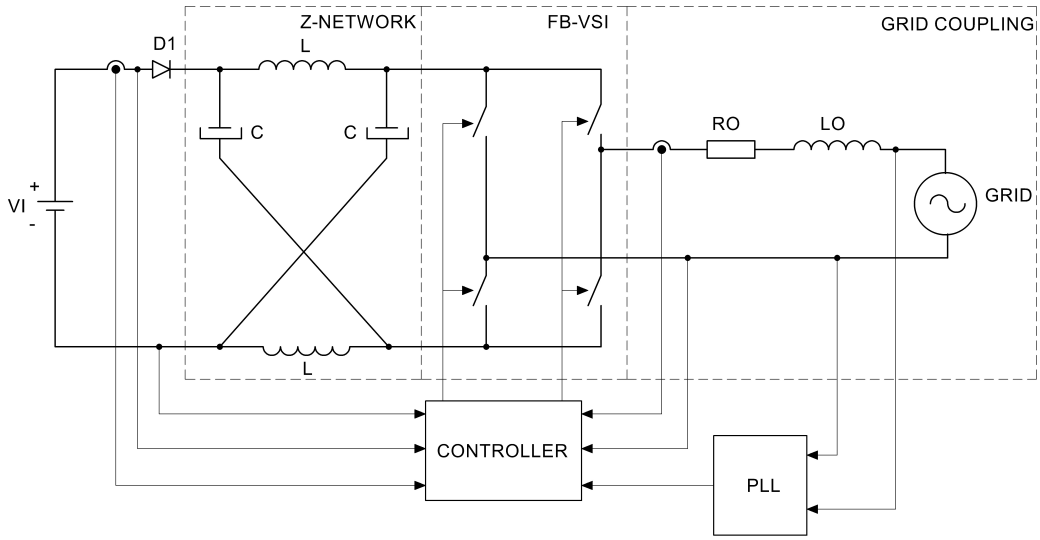

Figure 2.1 Simplified Block Diagram of the GTI.

The power stage of the GTI is subdivided into the sections Z-Source, full bridge voltage source inverter (FB-VSI) and grid coupling. Combining the FB-VSI with the Z-Source network reveals some unique features such as buck-boost functionability with the same number of switches that are present in a full bridge. The

resulting structure is called the Z-source inverter (ZSI) [1]. The Z-source inverter can be modeled by using the reduced single switch equivalent of a full bridge. The grid coupling side is modeled together with the full bridge and all the relevant transfer functions are derived. The simple model of a PLL circuit is also provided at the end of this section which is needed to extract grid related information from measurements.

2.2 DC AND STEADY STATE ANALYSIS OF THE Z-SOURCE CONVERTER

The Z-Source converter is shown in fig. 2.2. The Z-Network becomes symmetric by setting L_1, L_2 and C_1, C_2 to the same inductance L and capacitance C values, respectively. For steady state analysis, we make the following assumptions: The switching elements $S1$ and $D1$ are lossless, the input voltage source V_i is ideal and R_o is small enough to ensure continuous inductor currents. Continuous inductor current for the Z-Source converter is a condition which sould be ensured by design for the proper operation of the GTI. This subject of continuous inductor current is evaluated in more detail in the subsequent chapters. The ideal circuit component approach is realistic up to an extent since the expected efficiency of a practical GTI is over 95% which requires too little losses to be present.

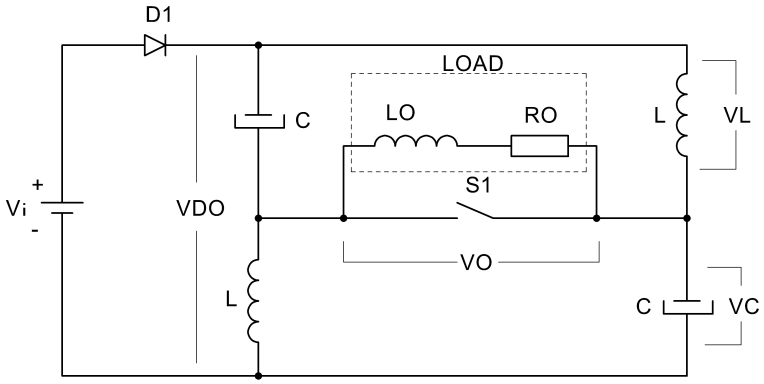

Figure 2.2 The Z-Source Converter.

The Z-Source Converter has two modes of operation namely *shoot-through state* examined as *Mode 1* and *non shoot-through* state examined as *Mode 2*. In the *shoot-through* state, the voltage across the load becomes zero and the load current circulates through the switch $S1$. In the *non shoot-through* state, the energy transfer occurs when the switch $S1$ is open.

Mode 1; Mode 1 starts when the switch $S1$ is turned on at $t = 0$. $S1$ conducts for a time defined by the duty cycle D. The duration of the on time is given by;

$$t_{on} = DT_S, \tag{2.1}$$

where T_S is the switching period. In mode 1, the voltage across the load is zero, the two Z-source capacitors are connected in series over $S1$, resulting in $2V_C$ to appear at V_{DO}, $D1$ turns off and no energy is transferred from V_i to the Z-source. The voltage across L is equal to V_c and the current through L starts increasing linearly. Mode 1 ends when $t = D.T_S$. The equivalent circuit for Mode 1 is shown below in fig. 2.3.

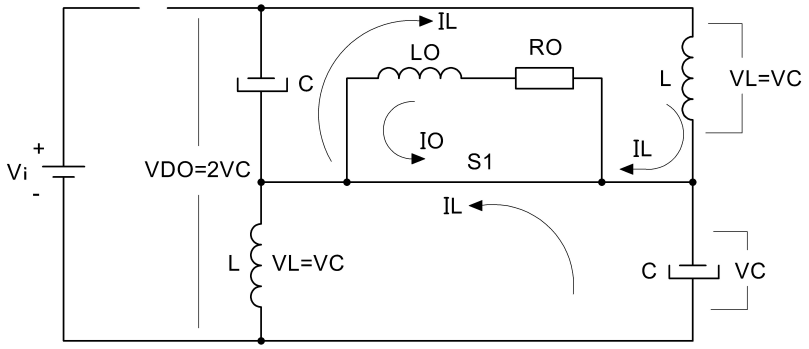

Figure 2.3 Equivalent Circuit for Mode 1.

Mode 2; Mode 2 continues for the remaining time of the period which is denoted as D'. During Mode 2 the switch $S1$ is off and the off time is given by;

$$t_{off} = D'T_S, \tag{2.2}$$

where, $D' = 1 - D$.

In Mode 2, the current through the inductors forces $D1$ to turn on, causing energy transfer from V_i to the Z-source. The voltage across the load is $2V_c - V_i$ and the current through the Z-source inductors starts decreasing linearly. The equivalent circuit for Mode 2 is shown in fig. 2.4 and related current waveforms in fig. 2.5 respectively.

2.2.1 Inductor Ripple Current and Capacitor Ripple Voltage

In the steady state, the average inductor current over one switching period is constant. In Mode 1, the inductor voltage is equal to the capacitor voltage. Thus,

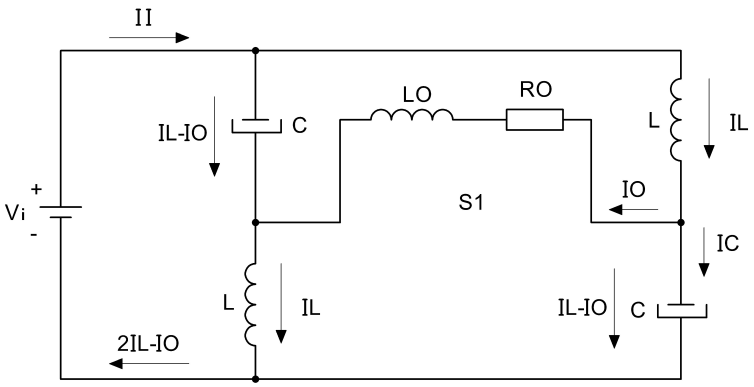

Figure 2.4 Equivalent Circuit for Mode 2.

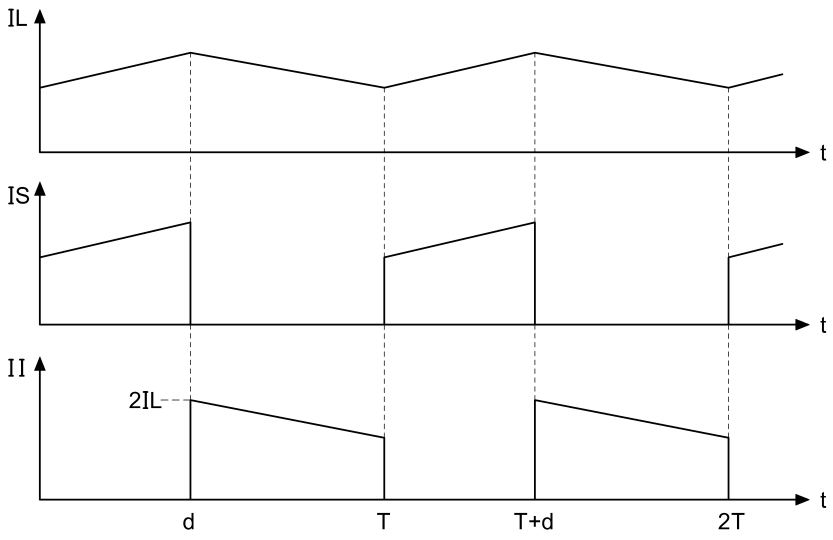

Figure 2.5 Input(I_I), Switch (I_S) and Inductor(I_L) Current Waveforms.

the amount of current rise is a function of the capacitor voltage V_c, switch on time and the inductance value L. Assuming that the capacitor ripple voltage is negligible and it is constant during Mode 1, the inductor ripple current can be determined by using Faraday's law of induction;

$$v = L\frac{di}{dt} \tag{2.3}$$

Then the amount of current rise during Mode 1 is;

$$\Delta I_L = \frac{V_C D T_S}{L} \tag{2.4}$$

The capacitor ripple voltage and parasitic resistances serve to reduce the maximum ripple current of I_L. Since the current rise in the inductor is a function of the time integral of the voltage across it, any reduction in the voltage such as capacitor voltage decay causes less ripple current through the inductor. Thus, the maximum ripple current of I_L occurs for $\Delta V_C = 0$. An important point for ΔI_L shows itself in 2.4, where the ripple current does not depend on the load current. Assuming that the inductance value, the capacitor voltage and the switching period are constant (which is generally the case), ΔI_L is only a function of the duty cycle D.

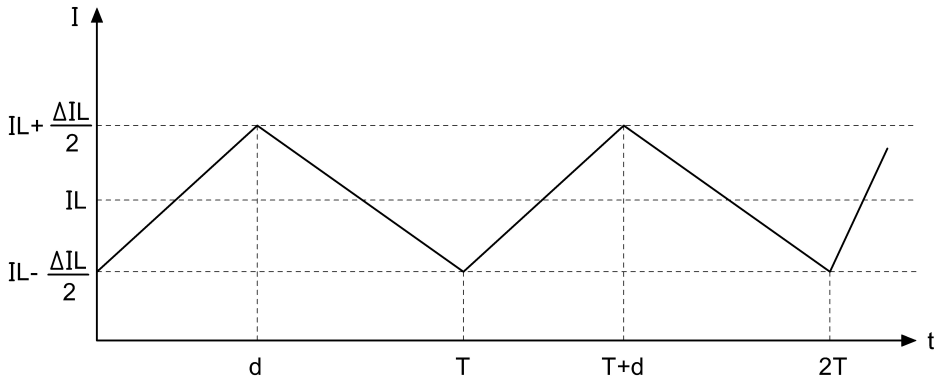

Figure 2.6 Inductor Ripple Current Waveform.

Once I_L, C and t_{on} are known, the amount of charge that flows out from the capacitor during t_{on} can be calculated using the definition of current;

$$I = \frac{Q}{t} \tag{2.5}$$

The total charge out of the Z-source capacitor during t_{on} is;

$$Q = I_L t_{on} \tag{2.6}$$

Then, the capacitor ripple voltage ΔV_C can be calculated using the definition of the capacitance;

$$Q = CV \tag{2.7}$$

The Z-source capacitor ripple voltage ΔV_C is;

$$\Delta V_C = \frac{I_L D T_S}{C} \tag{2.8}$$

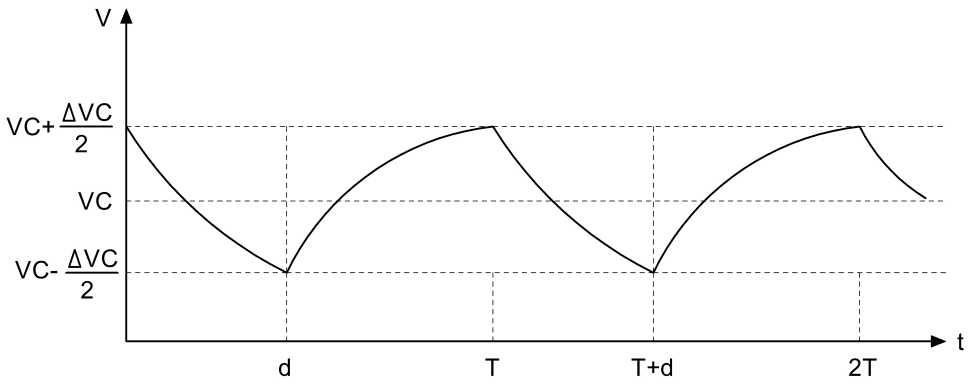

Figure 2.7 Capacitor Ripple Voltage Waveform.

As can be seen from the fig. 2.6, the average inductor current $I_{L(avg)ton}$ during Mode 1 is equal to the average inductor current $I_{L(avg)}$. In the steady state, the average capacitor voltage is constant over one switching period (see fig. 2.7) . Hence, the amount of charge that flows out of the capacitor during Mode 1 should be returned to the capacitor in Mode 2. That is, in the steady state, the following capacitor charge balance equation should always be satisfied;

$$I_{C(avg)} = \frac{1}{T_S} \int_0^{T_S} i_c(t) dt = 0 \tag{2.9}$$

Using the capacitor charge balance, the average value of the current returned to the capacitor during t_{off} can be calculated;

$$D I_L = D' I_{C(toff)} \tag{2.10}$$

and

$$I_{C(toff)} = \frac{D}{D'} I_L \tag{2.11}$$

2.2.2 DC input to Capacitor and Output Voltage Conversion Ratio

The voltage applied to the Z-source inductor L during turn on is V_C and during turn off the input voltage source V_I is connected in series with V_C. Because the polarity of the Z-Source capacitor is reversed with respect to the input voltage source, the resulting voltage over inductor L during turn off is found to be $V_I - V_C$.

According to the volt-second balance equation, the average voltage over an inductor in the periodic steady state should be equal to zero.

$$V_{L(avg)} = \frac{1}{T_S}\int_0^{T_S} V_L(t)dt = 0. \tag{2.12}$$

Using the volt-second balance equation,

$$V_{L(avg)} = DV_C + D'(V_I - V_C) = 0. \tag{2.13}$$

Then, arranging and simplifying 2.13 yields;

$$\frac{V_C}{V_I} = \frac{1-D}{1-2D} \tag{2.14}$$

In Mode 1, the output voltage V_O is zero, In Mode 2 the output voltage is found to be $2V_C - V_I$. Arranging the equation and solving for V_O produces

$$V_O = D \cdot 0 + D'(2V_C - V_I). \tag{2.15}$$

Substituting 2.14 into 2.15 yields

$$V_O = D'(\frac{2(1-D)V_I}{1-2D} - V_I), \tag{2.16}$$

and arranging and simplifying 2.16 yields

$$\frac{V_O}{V_I} = \frac{1-D}{1-2D}. \tag{2.17}$$

2.17 shows that the average output voltage V_O is equal to the capacitor voltage V_C. The relation in Mode 2 can be used to obtain the peak output voltage V_{Opeak} as

$$V_{Opeak} = 2V_C - V_I. \tag{2.18}$$

Substituting 2.14 into 2.18 and arranging the equation yields

$$\frac{V_{Opeak}}{V_I} = \frac{1}{1-2D}. \tag{2.19}$$

It is evident from 2.19 that theoretically the duty cycle is limited to a maximum value of 0.5 and the Boost ratio is 1 for $D = 0$, infinity for $D = 0.5$. This result is shown below in fig. 2.8

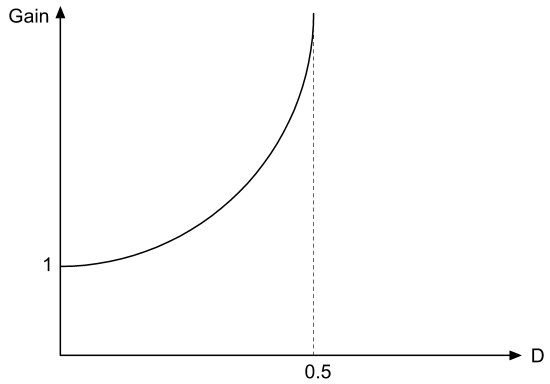

Figure 2.8 Gain vs. Duty Cycle.

2.2.3 Steady State Averaged Values of Switch and Input Current

Referring to fig. 2.3 in Mode 1, the switch S carries a current from the lower and upper halves of Z-source network, the amount of current from each half is equal to I_L. The switch also carries a freewheeling load current in the opposing direction which is equal to the output current I_O. Then the average switch current can be expressed as;

$$I_S = D(2I_L - I_O) \tag{2.20}$$

Referring to fig. 2.4, Input current is non-zero in Mode 2. During the time the switch S is off, both inductors force current through input voltage source and the output inductor L_O forces current over the Z-Source capacitors in the reverse direction. The average input current from the input voltage source can be expressed as;

$$I_I = D'(2I_L - I_O) \tag{2.21}$$

Referring to fig. 2.4 again in Mode 2, the inductor current relationship is;

$$I_L = I_O + I_{Ctoff} \tag{2.22}$$

inserting 2.10 into 2.22 and rearranging yields;

$$I_L = \frac{1-D}{1-2D} I_O \tag{2.23}$$

plugging 2.23 into 2.21 yields the Output to Input current relationship as;

$$I_I = \frac{1-D}{1-2D} I_O \tag{2.24}$$

2.2.4 Boundary Condition for Discontinuous Conduction Mode

The entire analysis is based on the assumption that the inductor currents are continuous, that is, the circuit operates in the continuous conduction mode (CCM). It is crucial to determine the conditions which keep the circuit in the CCM. The continuous inductor current in the Z-source converter needs a clarification because the inductor current I_L never becomes zero regardless of the operating mode.

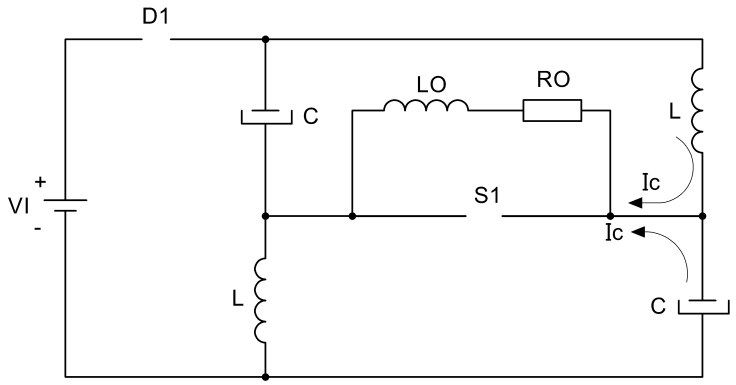

Figure 2.9 Equivalent Circuit for the Discontinous Mode of Operation.

The equivalent circuit for the discontinuous mode is shown in fig. 2.9. When the charge in the Z-source inductors L exhausts, $D1$ turns off. The capacitors cause a current of $2I_c$ to flow over the series connected L_O and R_O through the inductors L. Each inductor carry a current of I_c. The boundary between CCM and DCM thus can be better defined as the condition where the input current falls to zero just at the beginning of Mode 1. The circuit will then be called to be in CCM if the input current does not prematurely fall to zero during Mode 2. The output inductor L_O has an important impact on the boundary condition since the average output current during Mode 2 depends on the time constant $\frac{L_O}{R_O}$. The output inductor L_O will be treated as zero at the beginning so that the calculations are extensively simplified.

Using the definition above, the minimum inductor current I_{Lmin} at the end of Mode 2 where the input current falls to zero can be calculated using the input current relationship

$$I_I(t) = 2I_L(t) - I_O(t) \ , \ \{DT_S < t \leq T_S\}. \tag{2.25}$$

Setting the input current $I_I(t) = 0$ at time $t = T_S$, $I_{L_{min}}$ at the end of Mode 2 is

found as

$$I_{L_{min}} = \frac{I_O}{2}. \tag{2.26}$$

Using 2.18, the minimum inductor current $I_{L_{min}}$ at the boundary can be written as

$$I_{L_{min}} = \frac{2V_C - V_I}{2R_O}. \tag{2.27}$$

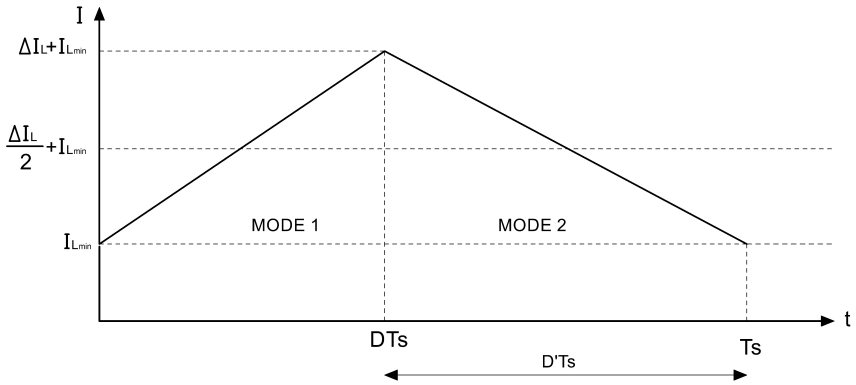

Figure 2.10 Inductor Current Waveform at The (CCM)-(DCM) Boundary.

The inductor current I_L at the boundary is shown in fig. 2.10. The average voltage of the Z-source capacitor V_C during the steady state in CCM is constant. This is because the amount of charge that flows out of the capacitor during Mode 1 is returned back to the capacitor in Mode 2. Referring to fig. 2.10, it can be seen that the area under the inductor current is larger in Mode 2 since D' is always larger than D. The charge difference between Mode 2 and Mode 1 should flow through R_O during Mode 2 so that the capacitor charge is balanced. The boundary condition for CCM can then be written as

$$\frac{D' - D}{D'}(\frac{\Delta I_L}{2} + I_{L_{min}}) \leq \frac{2V_C - V_I}{R_O}. \tag{2.28}$$

Rearranging 2.28, the resistance R_O that keeps the system in CCM can be obtained as

$$R_O \leq \frac{L}{(1-D)(1-2D)DT_S}. \tag{2.29}$$

The inductor current I_L will be continuous and the input current I_I will not fall to zero during Mode 2 if 2.29 is satisfied. The average output current is $\frac{V_C}{R_O}$ but current flows only in Mode 2 because there is no filter inductance L_O to make the output current continuous. When there is a large enough inductance L_O

which makes the output current continuous, the required current during Mode 2 to keep the Z-source in CCM can not flow. The worst case condition happens for $\frac{L_O}{R_O} >> T_S$. In that case, the output current becomes constant over the switching period. The average output current should be increased by a factor such that it is the same as the current during Mode 2 in the case without L_O. That is,

$$\frac{V_C}{kR_O} = \frac{2V_C - V_I}{R_O}. \tag{2.30}$$

k can be found by evaluating 2.30 as

$$k = D'. \tag{2.31}$$

For the case where $\frac{L_O}{R_O} >> T_S$, the output resistance value R_O should be scaled by D'. Therefore, an optimistic value for R_O which keeps the Z-source in CCM can be written as;

$$R_O \leq \frac{L}{(1-2D)DT_S}. \tag{2.32}$$

2.3 SMALL SIGNAL MODELING OF THE ZSC

The power stage of the Z-source converter requires a control circuit to regulate the desired output parameter against several disturbances such as output power and input voltage deviations. The Z-source converter includes highly nonlinear elements such as diode and switch. In order to apply well established linear control theory, the system should be averaged and linearized. In this context, state-space averaging and circuit averaging methods are two popular methods. The state-space averaging technique involves the averaging of the state equations, whereas, in the circuit averaging technique, the averaging is performed on the switching component waveforms. This technique is preferred by many authors because it provides good intuitive insight into converter behavior. In our modeling of the Z-source converter, the circuit averaging technique is used. The small signal modeling presented in this thesis is based on the model developed in [2].

Fig. 2.11 shows two input-to-output nonlinear switching network. The principle of the circuit averaging technique is to replace these nonlinear elements with their average models. Average model can be determined by choosing one of the terminal voltages and one of the terminal currents as the independent input. The remaining terminal voltage and current are expressed as a function of the independent terminal voltage and current, respectively. In this model $i_1(t)$, $v_2(t)$ are

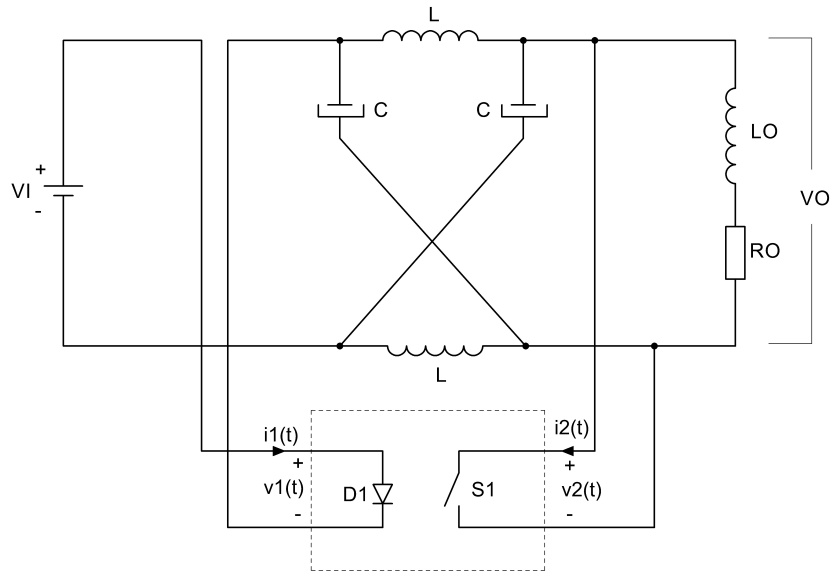

Figure 2.11 Z-Source Converter With Separated Nonlinear Elements.

selected as independent inputs and $i_2(t)$, $v_1(t)$ are selected as dependent outputs of the nonlinear switching network. The dependent output $i_2(t)$ corresponds to the switch current i_S and $v_1(t)$ corresponds to the diode voltage v_D. The average values for these dependent outputs should be written in terms of the independent inputs which correspond to i_I and v_O, respectively.

Combining 2.20, 2.21 and solving for I_S yields the switch current in terms of the input current I_I as

$$I_S = \frac{D}{D'} I_I. \tag{2.33}$$

During Mode 1, the voltage across the diode is $2V_c - V_i$ and during Mode 2 the diode voltage is zero because it is forward biased and assumed to be lossless. Thus the average voltage across the diode is

$$V_D = D(2V_C - V_I). \tag{2.34}$$

Combining 2.15, 2.34 and solving for V_D yields the average diode voltage V_D in terms of the output voltage V_O as

$$V_D = \frac{D}{D'} V_O. \tag{2.35}$$

Equations 2.33 and 2.35 can be used to obtain the average DC model of the Z-source converter in continuous conduction mode. 2.33 can be realized by using a current-controlled current source since the independent input and dependent output is a current signal. Because of the same relationship between the independent

and dependent ports, 2.35 can be realized by using a voltage-controlled voltage source. The obtained model is shown below in fig. 2.12.

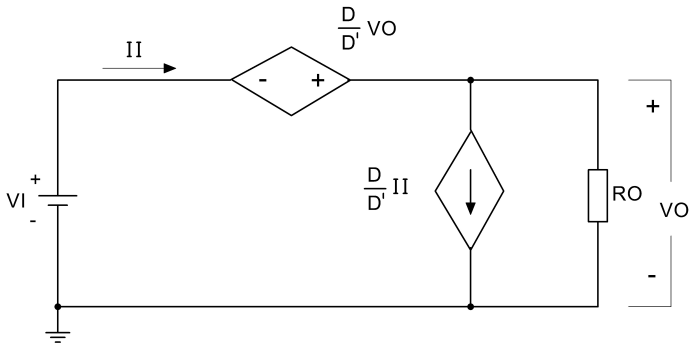

Figure 2.12 DC Model of the Z-Source Converter for CCM.

The large signal averaged model is obtained by approximating the averaged DC quantities by low frequency large signal time-dependent quantities. The approximations are $i_S \approx I_S$, $i_I \approx I_I$, $v_D \approx V_D$, $v_O \approx V_O$, $d_T \approx D$.

The relationships among the large signal quantities are approximated using the same relationships between the DC quantities as

$$i_S \approx \frac{d_T}{d'_T} i_I \tag{2.36}$$

and

$$v_D \approx \frac{d_T}{d'_T} v_O, \tag{2.37}$$

where

Duty cycle $d_T = D + \hat{d}$,

Switch current $i_S = I_S + \hat{I}_S$,

Diode voltage $v_D = V_D + \hat{v}_D$,

Input current $i_I = I_I + \hat{i}_I$,

Output voltage $v_O = V_O + \hat{v}_O$.

The quantities $\hat{d}$, $\hat{i}_S$, $\hat{v}_D$, $\hat{i}_I$ and $\hat{v}_O$ are small signal AC components. Therefore 2.36 and 2.37 can be written as

$$i_S = I_S + \hat{i}_S = \frac{D + \hat{d}}{D'} - \hat{d}(I_I + \hat{i}_I), \tag{2.38}$$

$$i_S = \frac{D+\hat{d}}{D'}\frac{1}{1-\frac{\hat{d}}{D'}}(I_I+\hat{i}_I), \tag{2.39}$$

and

$$v_D = V_D + \hat{v}_D = \frac{D+\hat{d}}{D'} - \hat{d}(V_O+\hat{v}_O), \tag{2.40}$$

$$v_D = \frac{D+\hat{d}}{D'}\frac{1}{1-\frac{\hat{d}}{D'}}(V_O+\hat{v}_O). \tag{2.41}$$

The expression $\frac{1}{1-\frac{\hat{d}}{D'}}$ in 2.39 and 2.41 can be simplified by the Maclaurin series expansion. Using the expansion rule

$$\frac{1}{1-x} = 1 + x + x^2 + ... + x^n, \tag{2.42}$$

and noting that $\hat{d}$ is a small signal perturbation whose quantity is much smaller than D' such that $|\frac{\hat{d}}{D'}| \ll 1$, the first order approximation of the Maclaurin series expansion can be used. This results in the simplification

$$\frac{1}{1-\frac{\hat{d}}{D'}} = 1 + \frac{\hat{d}}{D'}. \tag{2.43}$$

Substituting 2.43 into 2.39 and 2.41 yields

$$i_S = I_S + \hat{i}_S = \frac{D+\hat{d}}{D'}(1+\frac{\hat{d}}{D'})(I_I+\hat{i}_I) \tag{2.44}$$

and

$$v_D = V_D + \hat{v}_D = \frac{D+\hat{d}}{D'}(1+\frac{\hat{d}}{D'})(V_O+\hat{v}_O). \tag{2.45}$$

The nonlinear model of the Z-source converter can be obtained by expanding 2.44 and 2.45 using the equality $D + D' = 1$. This results in the following equations

$$i_S = \frac{D}{D'}I_I + \frac{D}{D'}\hat{i}_I + \frac{I_I}{D'^2}\hat{d} + \frac{I_I}{D'^2}\hat{d}^2 + \frac{\hat{d}I_I}{D'^2} + \frac{\hat{d}^2 I_I}{D'^2}, \tag{2.46}$$

$$v_D = \frac{D}{D'}V_O + \frac{D}{D'}\hat{v}_O + \frac{V_O}{D'^2}\hat{d} + \frac{V_O}{D'^2}\hat{d}^2 + \frac{\hat{d}\hat{v}_O}{D'^2} + \frac{\hat{d}^2\hat{v}_O}{D'^2}. \tag{2.47}$$

The nonlinear terms appear either as power of or multiplication of small signal quantities. Because the small signal quantities are small by definition, their powers and multiplications are much smaller and can hence be neglected. The equations 2.46 and 2.47 reduce to

$$i_S = I_S + \hat{i}_S = \frac{D}{D'}I_I + \frac{D}{D'}\hat{i}_I + \frac{I_I}{D'^2}\hat{d}, \tag{2.48}$$

$$v_D = V_D + \hat{v}_D = \frac{D}{D'}V_O + \frac{D}{D'}\hat{v}_O + \frac{V_O}{D'^2}\hat{d}. \tag{2.49}$$

Equations 2.48 and 2.49 represent the DC and linear small signal model of the Z-source converter operating in continuous conduction mode. They can be realized by current controlled current source and voltage controlled voltage source respectively as shown below in fig. 2.13

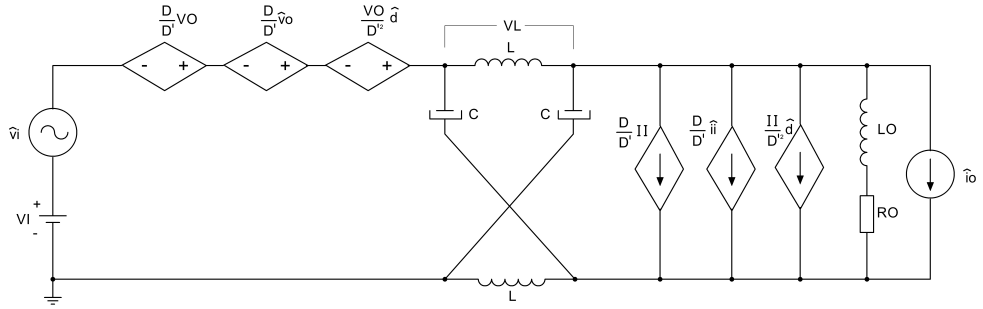

Figure 2.13 DC and Averaged Small Signal Linear Model of the ZSC.

According to the superposition property of linear systems, the AC small signal model can be stripped out from 2.48 and 2.49 as shown below in fig. 2.14

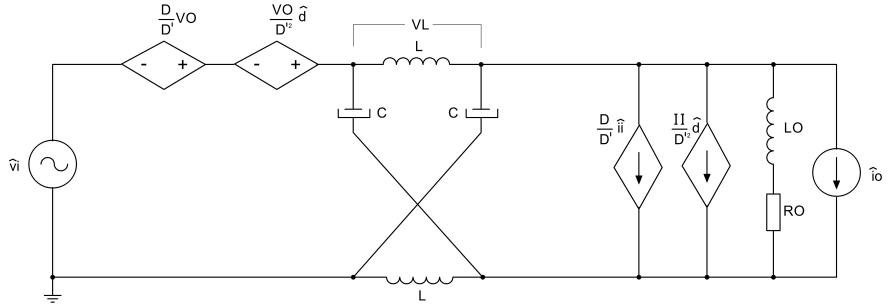

Figure 2.14 Small Signal Linear Model of the Z-Source Converter.

2.4 DERIVING TRANSFER FUNCTIONS FOR CLOSED LOOP VOLTAGE CONTROL

Designing a voltage control loop for the Z-source converter requires two transfer functions; Input to capacitor voltage transfer function T_{ci} and Control to capacitor voltage transfer function T_{cc}

2.4.1 Input to Capacitor Voltage Transfer Function T_{ci}

The small signal model to derive the input to capacitor voltage transfer function can be obtained by setting $\hat{d} = 0$ and $\hat{i}_O = 0$ in the small signal model shown in fig. 2.14. The resulting model is shown below in fig. 2.15.

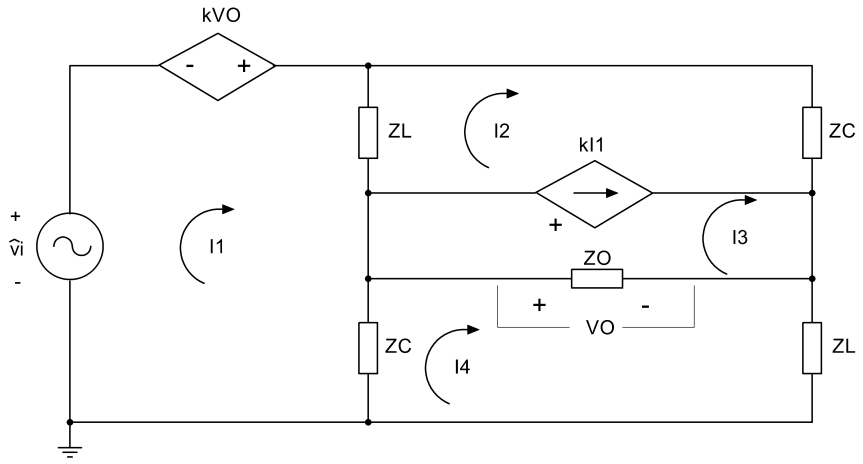

Figure 2.15 Small Signal Model to Derive the Input to Capacitor Voltage Transfer Function.

Fig. 2.15 is organized in a way that the mesh analysis can be applied easily. The linear components are shown in the impedance form. Calculations are carried out using this notation so that the parasitic components of the capacitors and the inductors can be taken into account without complicating the calculations.

As is shown in fig. 2.15, there are four meshes in the circuit. The system of linear equations can be written to determine the currents in the meshes using Kirchhoff's voltage law,

Mesh 1: $\hat{v}_i + k\hat{v}_O - I_1(z_L + z_C) + I_2 z_L + I_4 z_C = 0$,

Mesh 2 and 3: $I_1 z_L - I_2 z_L - I_2 z_C - I_3 z_O + I_4 z_O = 0$,

$kI_1 = I_3 - I_2$ and thus $I_1 = \frac{I_3 - I_2}{k}$,

Mesh 4: $I_1 z_C - I_4 z_C - I_4 z_O + I_3 z_O - I_4 z_L = 0$,

where $k = \frac{D}{D'}$. The equations above can be written in matrix form by combining the mesh currents and substituting $\frac{I_3 - I_2}{k}$ for I_1,

$$\underbrace{\begin{bmatrix} z_L + \frac{z_C+z_L}{k} & -kz_O - \frac{z_L-z_C}{k} & kz_O + z_C \\ -z_L - z_C - \frac{z_L}{k} & \frac{z_L}{k} - z_O & z_O \\ -\frac{z_C}{k} & \frac{z_C}{k} + z_O & -z_C - z_O - z_L \end{bmatrix}}_{Z} \cdot \underbrace{\begin{bmatrix} I_2 \\ I_3 \\ I_4 \end{bmatrix}}_{I} = \underbrace{\begin{bmatrix} -\hat{v}_i \\ 0 \\ 0 \end{bmatrix}}_{V} \tag{2.50}$$

The unknown matrix I can be found by the matrix operation

$$I = Z^{-1}V. \tag{2.51}$$

Using the Matlab symbolic toolbox, the matrix I is found as;

$$I = \begin{bmatrix} \frac{\hat{v}_i(z_O+z_L-kz_O)}{z_Oz_C+z_Oz_L+2z_Cz_L+k^2z_Oz_C+k^2z_Oz_L-2kz_Oz_C+2kz_Oz_L} \\ \frac{\hat{v}_i(z_O+z_L+k(z_O+z_L+z_C))}{z_Oz_C+z_Oz_L+2z_Cz_L+k^2z_Oz_C+k^2z_Oz_L-2kz_Oz_C+2kz_Oz_L} \\ \frac{\hat{v}_i(z_O+z_C+kz_O)}{z_Oz_C+z_Oz_L+2z_Cz_L+k^2z_Oz_C+k^2z_Oz_L-2kz_Oz_C+2kz_Oz_L} \end{bmatrix}, \tag{2.52}$$

where $k = \frac{D}{D'}$.

Using Ohm's law, the voltage over the capacitor is

$$\hat{v}_C = I_2 z_C. \tag{2.53}$$

Expanding and arranging 2.53 produces the input to capacitor voltage relationship as

$$\frac{\hat{v}_C}{\hat{v}_i} = \frac{D'^2 z_O z_C - DD' z_C z_O + D'^2 z_L z_C}{z_L z_O + (D'-D)^2 z_C z_O + 2D' z_C z_L}. \tag{2.54}$$

To find the Input to capacitor voltage transfer function, Laplace equivalents of the impedances are substituted in 2.54 which are

$$z_L = sL, \tag{2.55}$$

$$z_C = \frac{1}{sC}, \tag{2.56}$$

$$z_O = R + sL_O. \tag{2.57}$$

Then the transfer function T_{ci} is obtained as

$$T_{ci} = \frac{\hat{v}_C}{\hat{v}_i} = \frac{s(D'L_O(D'-D) + D'^2L) + (D'^2 - DD')R}{s^3L_OLC + s^2RLC + s(2D'^2L + L_O(D'-D^2)) + (D'-D)^2R}. \tag{2.58}$$

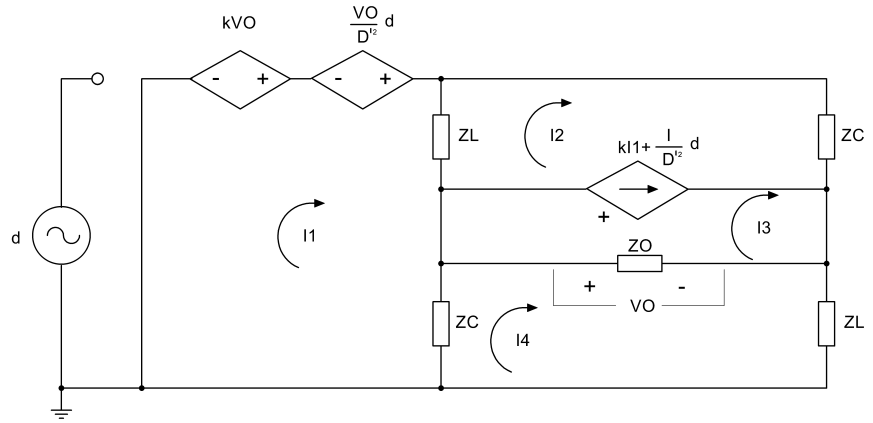

Figure 2.16 Small Signal Model to Derive the Control to Capacitor Voltage Transfer Function.

2.4.2 Control to Capacitor Voltage Transfer Function T_{cc}

The control to capacitor voltage transfer function T_{cc} can be derived by setting $\hat{v}_i = 0$ and $\hat{i}_O = 0$ in the small signal model shown in fig. 2.14. The small signal model shown below in fig. 2.16 is reorganized to simplify the calculations.

The structure of meshes is the same as in fig. 2.15 except for the dependent sources. Writing the system of linear equations for the meshes produce the following equations:

Mesh 1: $-I_1(z_L + z_C) + I_2 z_L + I_4 z_C + k(I_4 - I_3)z_O = \frac{-\hat{d}}{D'^2} V_O$,

Mesh 2 and 3: $I_1 z_L - I_2 z_L - I_2 z_C - I_3 z_O + I_4 z_O = 0$,

$kI_1 = I_3 - I_2 - \frac{I}{D'^2}\hat{d}$ and $I_1 = \frac{I_3 - I_2}{k} - \frac{I}{kD'^2}\hat{d}$.

Thus $I_1 = \frac{D'^2(I_3 - I_2) - I\hat{d}}{DD'}$,

Mesh 4: $I_1 z_C - I_4 z_C - I_4 z_O + I_3 z_O - I_4 z_L = 0$.

where $k = \frac{D}{D'}$ and I is the average input current to the Z-source. The equations above can be written in matrix form as shown below after necessary arrangements and substitutions;

$$\underbrace{\begin{bmatrix} \frac{z_C D' + z_L}{D} & \frac{(-z_L - z_C)D'}{D} - \frac{D}{D'} z_O & \frac{D}{D'} z_O + z_C \\ -z_C - \frac{z_L}{D} & \frac{D'}{D} z_L - z_O & z_O \\ -\frac{D'}{D} z_C & \frac{D'}{D} z_C + z_O & -z_C - z_O - z_L \end{bmatrix}}_{Z} \cdot \underbrace{\begin{bmatrix} I_2 \\ I_3 \\ I_4 \end{bmatrix}}_{I} = \underbrace{\begin{bmatrix} (-V_O D - I D'(z_L + z_C))\hat{d} \\ \frac{I z_L \hat{d}}{DD'} \\ \frac{I z_C \hat{d}}{DD'} \end{bmatrix}}_{V} \tag{2.59}$$

The unknown matrix I is found by the matrix operation

$$I = Z^{-1}V. \tag{2.60}$$

Using the Matlab symbolic toolbox, the matrix I is found as;

$$I = \begin{bmatrix} \frac{-(D^2\hat{d}(V_O z_O + I z_L z_O)(z_L + z_C) - DD'\hat{d}(z_L + z_C)(V_O z_L + V_O z_O - I z_L z_O))}{den} \\ \frac{A}{den} \\ \frac{B}{den} \end{bmatrix} \tag{2.61}$$

Hereby, the unspecified parameters are given as

$A = (D'(D\hat{d}(2Iz_C^2 z_L + Iz_O z_C^2 + Iz_C z_L^2 + 2Iz_O z_C z_L + V_O z_O z_C) + I\hat{d}z_C z_L^2) + D\hat{d}(V_O z_L^2 + V_O z_C z_L + V_O z_L z_O - Iz_C z_L z_O) + D^2\hat{d}(V_O z_C^2 + V_O z_C z_L + V_O z_C z_O - Iz_C^2 z_O) - D'^2 I\hat{d}z_C z_L^2),$

$B = (\hat{d}(V_O z_C z_O - Iz_C^2 z_O)D^2 + (z_L(\hat{d}(V_O z_O - Iz_C z_O) + 2D'I * \hat{d}z_C z_O) + D'\hat{d}(V_O z_C^2 + V_O z_C z_O + Iz_C^2 z_O))D - z_L(D'^2 V_O \hat{d}z_C - D'V_O \hat{d}z_C)),$

den=$(D'(z_O D^3 z_C^2 + z_O D^3 z_C z_L - 2z_O D^2 D' z_C^2 + z_O D^2 z_C z_L + z_O D^2 z_L^2 + 2DD'^2 z_C^2 z_L + z_O DD'^2 z_C^2 + DD'^2 z_C z_L^2 + 3z_O DD'^2 z_C z_L - z_O DD' z_C z_L + z_O DD' z_L^2 - D'^3 z_C z_L^2 + D'^2 z_C z_L^2)).$

The voltage over the capacitor $\hat{v}_c$ is

$$\hat{v}_c = I_2 Z_C. \tag{2.62}$$

Expanding and arranging 2.62 yields

$$T_{cc} = \frac{\hat{v}_c}{\hat{d}} = \frac{-(Dz_C(z_C + z_L)(DV_O z_O - D'V_O(z_L + z_O) + Iz_L z_O))}{den}. \tag{2.63}$$

2.4.3 D-Q Model

In the D-Q control technique, the feedback signals are transformed into the synchronous reference frame by applying Park's transformation. After this transformation, the AC time varying signals become DC signals which allow standard PI controllers to be used without the drawbacks present for the stationary reference frame application of PI controllers. The outputs from the controllers are then transformed back into the stationary reference frame by applying the inverse Park's transformation. The transformation and inverse transformation matrices for Park's transform are given below in 2.64 and 2.65 respectively

$$T = \begin{bmatrix} sin(wt) & -cos(wt) \\ cos(wt) & sin(wt) \end{bmatrix}, \tag{2.64}$$

$$T^{-1} = \begin{bmatrix} sin(wt) & cos(wt) \\ -cos(wt) & sin(wt) \end{bmatrix}. \tag{2.65}$$

Before developing the D-Q model, the approximate model for the power stage will be developed and the D-Q transform will be applied to the overall grid connected system.

2.4.4 Full Bridge Voltage Source Inverter (FB-VSI)

The full bridge inverter is the only active power section of the whole system by which the output current, phase and frequency can be controlled. In the GTI, the full bridge VSI is combined with the Z-source converter to utilize the advantages of the Z-network. This brings the necessity for a modification of the standard FB-VSI gating signals since the controllable elements are still the same four switches. The modifications to the gatings of the FB-VSI will not be discussed here because the switching scheme for the Z-source inverter (ZSI) uses only the zero states of the standard FB-VSI switching scheme which does not affect the modeling of the FB-VSI. The full bridge voltage source inverter with four ideal switches and $R-L$ load is shown below in fig. 2.17.

The AC voltage source G at the output of the full bridge represents the grid which is an output disturbance from the control perspective and can be considered as if

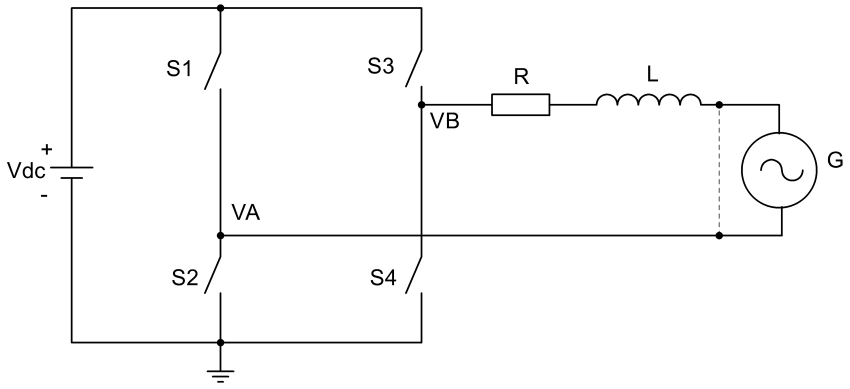

Figure 2.17 The Full Bridge VSI.

it is shorted to simplify the modeling. The basic switching scheme of the FB-VSI to produce an AC output voltage is shown in fig. 2.18.

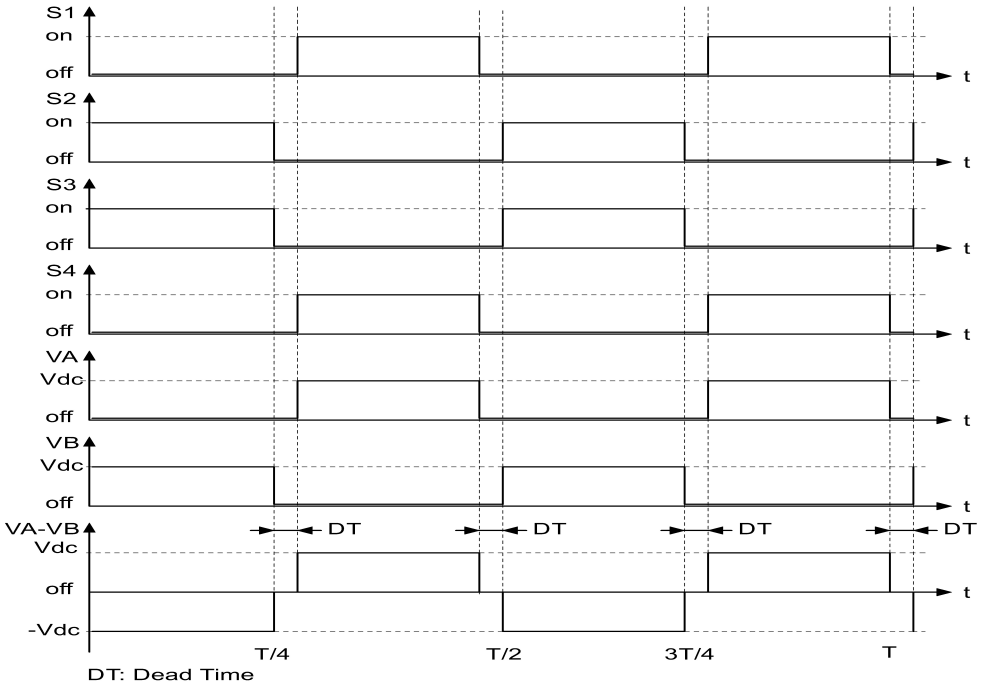

Figure 2.18 Basic Switching Scheme of the FB-VSI.

The gating signals for $S2$ and $S4$ are the inverse of the gating signals of $S1$ and $S3$, respectively. The switch $S4$ is kept on to produce the positive half cycle and similarly $S2$ is kept on to produce the negative half cycle. The output ripple current of the inverter can be made smaller or the filter size can be reduced and higher control capability can be gained by using multiple pulses per half cycle to produce the same output waveform. Using multiple pulses per half cycle also improves the wave shaping capability which is the major advantage since the expected output waveform of a grid tie inverter is a sinusoidal shaped signal.

This point will be addressed in the subsequent sections of the text and multiple pulses per half cycle to produce a quasi-square wave will be used for modeling purpose without degrading the accuracy of the model for the sinusoidal output waveform case. The gating signals of the switches can be modified to produce multiple pulses per half cycle as shown below in fig. 2.19.

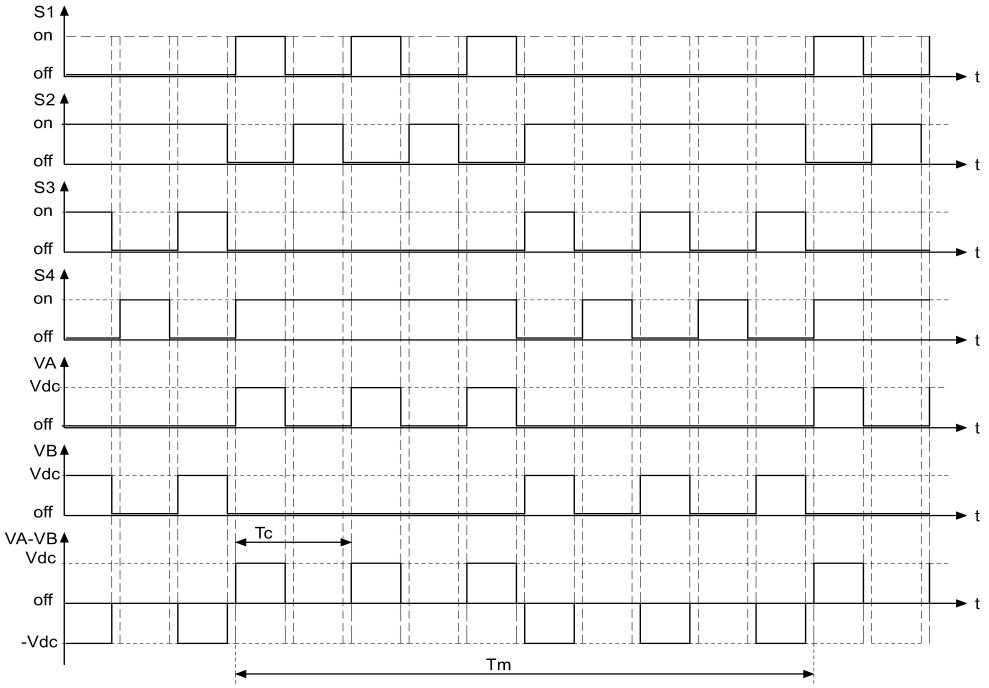

Figure 2.19 Multiple Pulses Per Half Cycle Switching Waveforms.

The period of the pulses in one half cycle is called T_C and the corresponding frequency is called the carrier frequency. T_M is the period of the modulated signal and this signal will be present at the output of the FB-VSI after filtering. Assuming that the carrier frequency is much larger than the modulated signal frequency ($T_M >> T_C$), the full bridge VSI can be regarded as two Buck converters each operating in one half cycle. Since half cycles are symmetric and inversion of the output voltage polarity is done by the switches $S4$ and $S2$ which are always on during positive and negative cycles respectively, the model can be reduced to a single buck converter as shown below in fig. 2.20.

As can be seen from the switching waveforms, the average output voltage V_{a-b} depends solely on the switching actions of $S1$ and $S2$ independent of the output current and the conduction mode in which the circuit operates. This is because the load voltage is defined as V_{a-b}, not the voltage across the resistor R as in the case for the buck converter. The average model of the switching network shown in fig. 2.20 can be calculated using the average values of the current and voltage

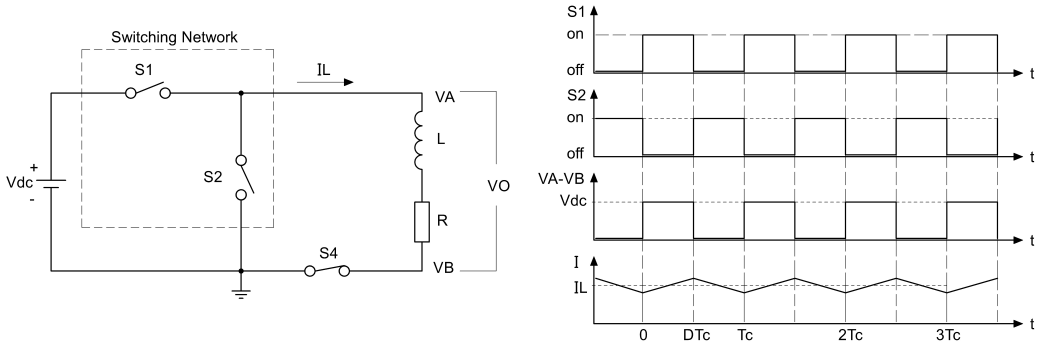

Figure 2.20 Reduced Model and Steady State Waveforms for Positive Half Cycle.

of $S1$ and $S2$ respectively. The current through $S1$ during on period is I_L and the average value over one switching cycle is

$$I_{S1} = \frac{1}{T_C}\int_0^{T_C} i_{S1}dt = \frac{1}{T_C}\int_0^{DT_C} I_L dt = DI_L. \tag{2.66}$$

The voltage across the switch $S2$ during on period is V_{DC} and the average voltage across the switch $S2$ can be calculated as

$$V_{S2} = \frac{1}{T_C}\int_0^{T_C} v_{S2}dt = \frac{1}{T_C}\int_0^{DT_C} V_{DC}dt = DV_{DC}. \tag{2.67}$$

Using the average values in 2.66 and 2.67, the average model of the switching network in fig. 2.20 can be represented by the dependent sources as shown in fig. 2.21a. According to the current splitting theorem, the dependent current source can be split into two parts as shown in fig. 2.21b, considering that the parallel combination of a current source and a voltage source is equal to the voltage source. Using the equalities stated above, the model can be simplified as shown in fig. 2.21c.

Assuming that the frequency of the carrier wave is much larger than the modulated signal, the small signal dynamics at low frequencies can be neglected and the average model can be used as an approximate model. Since the input-output relationship is linear in the approximate model and the voltage polarity is inverted using the switches $S2$ and $S4$ in the FB-VSI, the FB-VSI in grid tie configuration can be modeled as a controllable voltage source as shown in fig. 2.22.

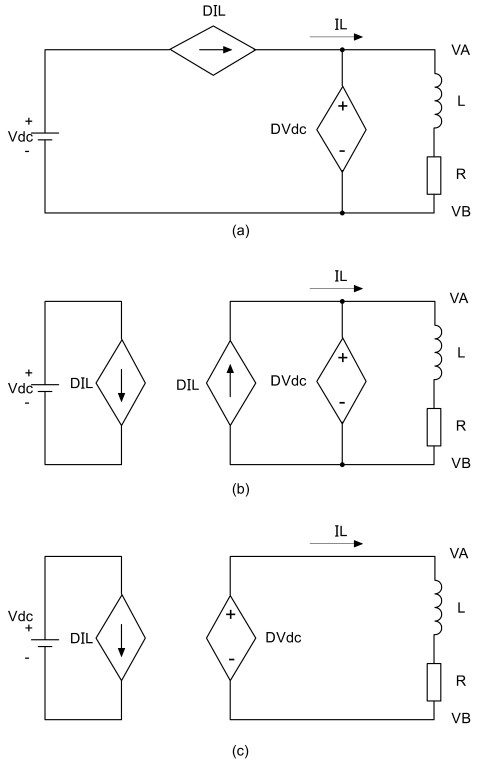

Figure 2.21 Average Model of the Buck Switching Network.(a) Dependent Sources in Original Branches.(b) Model With Dependent Current Sources Split Into Two Sources.(c) Simplified Model.

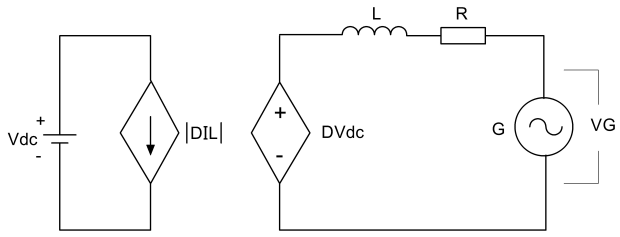

Figure 2.22 FB-VSI Approximate Model in Grid Connected Configuration.

2.4.5 Inductor Ripple Current in Grid Connected Configuration

The output waveform of the full bridge in grid connected configuration is a quasi-square wave with varying duty cycle to form a sinusoidal output current. Since the frequency of the modulated sinusoidal signal is much smaller than the switching frequency, we can simplify our analysis by assuming that the grid voltage is constant over a switching period.

Keeping in mind the assumption stated above, referring to fig. 2.17 and using 2.3, the absolute value of the output inductor current ΔI_{L_O} can be expressed at any instant of time as

$$|\Delta I_{L_O}| = \frac{(V_{dc} - |V_G(t)|)d(t)T_S}{L_O}, \tag{2.68}$$

where $d(t)$ is the duty cycle of the corresponding switch ($S1$ or $S3$) at the time (t) and $V_G(t)$ is the grid voltage at the time (t) which is assumed to be constant during the time $(t + T_S)$. Since the grid voltage is symmetric, we can omit the absolute value operators in 2.68 by constraining our attention to the positive half cycle. 2.68 becomes;

$$\Delta I_{L_O} = \frac{(V_{dc} - V_G(t))d(t)T_S}{L_O}. \tag{2.69}$$

2.69 can be further simplified by noting that the average value of the bridge output voltage during the switching period is very close to the grid voltage,

$$\int_t^{t+T_S} (V_B - V_A)d(t)dt \approx V_G(t). \tag{2.70}$$

Using the approximation 2.70, 2.69 can be rewritten as

$$\Delta I_{L_O} = \frac{V_{dc}d(t)(1 - d(t))T_S}{L_O}. \tag{2.71}$$

The DC link voltage V_{dc}, switching period T_S and output inductance L_O are constant. Only the duty cycle $d(t)$ contributes to the change in ΔI_{L_O}. By inspection, it can be deduced that $d(t)(1-d(t))$ takes its maximum value of 0.25 for $d(t) = 0.5$. The maximum ripple current then can be expressed as

$$\Delta I_{L_O} = \frac{V_{dc}T_S}{4L_O}. \tag{2.72}$$

Now the D-Q model can be developed using fig. 2.22. The model can be described by

$$DV_{DC} - I_L R - L\frac{dI_L}{dt} - V_G = 0, \tag{2.73}$$

$$L\frac{dI_L}{dt} = DV_{DC} - I_L R - V_G. \tag{2.74}$$

The D-Q model can be obtained by applying Park's transformation to 2.74. By applying the transformation, the time varying AC signals become DC signals and standard PI controllers can be used to control the system. Park's transformation requires two orthogonal axes for transformation which makes Park's transformation unusable for single phase systems. There are several proposed techniques in the literature to produce the normal component that is needed for single phase Park's transformation. In this thesis, the phase delay technique is chosen for its simplicity in implementation. In the phase delay technique, the second component which is normal to the first component is produced by delaying the first component by 90 degrees of the phase angle.

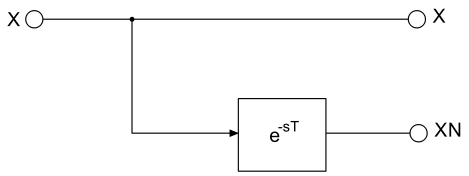

Figure 2.23 Obtaining the Orthogonal Component by Time Delay Technique.

The delay time in fig. 2.23 is chosen such that T corresponds to $\frac{1}{4}$ of the signal period time and X_N denotes the normal component that is produced by the delaying process.

D and Q components of a signal X are given by the Park's transformation as;

$$\begin{bmatrix} X_D \\ X_Q \end{bmatrix} = \underbrace{\begin{bmatrix} sin(wt) & -cos(wt) \\ cos(wt) & sin(wt) \end{bmatrix}}_{T} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{2.75}$$

and the inverse transformation as;

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \underbrace{\begin{bmatrix} sin(wt) & cos(wt) \\ -cos(wt) & sin(wt) \end{bmatrix}}_{T^{-1}} \begin{bmatrix} X_D \\ X_Q \end{bmatrix} \tag{2.76}$$

Substituting $X_{\alpha,\beta} = T^{-1}X_{D,Q}$ in 2.74 and using the chain rule for the derivative term yields

$$(\frac{d}{dt}T^{-1}I_{L(D,Q)} + T^{-1}\frac{d}{dt}I_{L(D,Q)}) = \frac{1}{L}T^{-1}(DV_{DC(D,Q)} - RI_{L(D,Q)} - V_{G(D,Q)}), \tag{2.77}$$

$$T^{-1}\frac{d}{dt}I_{L(D,Q)} = \frac{1}{L}T^{-1}(DV_{DC(D,Q)} - RI_{L(D,Q)} - V_{G(D,Q)}) - \frac{d}{dt}T^{-1}I_{L(D,Q)}, \tag{2.78}$$

$$TT^{-1}\frac{d}{dt}I_{L(D,Q)} = T\frac{1}{L}T^{-1}(DV_{DC(D,Q)} - RI_{L(D,Q)} - V_{G(D,Q)}) - T\frac{d}{dt}T^{-1}I_{L(D,Q)}, \tag{2.79}$$

$$\frac{d}{dt}I_{L(D,Q)} = \frac{(DV_{DC(D,Q)} - V_{G(D,Q)})}{L} - \frac{R}{L}\begin{bmatrix} I_D \\ I_Q \end{bmatrix} - \begin{bmatrix} 0 & -w \\ w & 0 \end{bmatrix}\begin{bmatrix} I_D \\ I_Q \end{bmatrix}, \tag{2.80}$$

where

$$T\frac{d}{dt}T^{-1} = \begin{bmatrix} 0 & w \\ w & 0 \end{bmatrix}, \tag{2.81}$$

$$\begin{bmatrix} \dot{I_D} \\ \dot{I_Q} \end{bmatrix} = \frac{1}{L}\left(\begin{bmatrix} DV_{DC(D)} \\ DV_{DC(Q)} \end{bmatrix} - \begin{bmatrix} V_{G(D)} \\ V_{G(Q)} \end{bmatrix}\right) + \left(\begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} - \begin{bmatrix} 0 & -w \\ w & 0 \end{bmatrix}\right)\begin{bmatrix} I_D \\ I_Q \end{bmatrix}. \tag{2.82}$$

The reference signal for Parks transformation $sin(wt)$ is obtained from the grid G and the normal component $V_{G(Q)}$ is the 90 degrees delayed version of $V_{G(D)}$. Then,

$$V_{G(\alpha)} = Asin(wt) \tag{2.83}$$

and

$$V_{G(\beta)} = Asin(wt - \frac{\pi}{2}) = -Acos(wt). \tag{2.84}$$

Using Park's transformation to find the D and Q components of the grid yields

$$V_{G(D)} = V_{G(\alpha)}sin(wt) - V_{G(\beta)}cos(wt), \tag{2.85}$$

$$V_{G(D)} = Asin(wt)sin(wt) + Acos(wt)cos(wt) = A, \tag{2.86}$$

$$V_{G(Q)} = V_{G(\alpha)}cos(wt) + V_{G(\beta)}sin(wt), \tag{2.87}$$

$$V_{G(Q)} = Asin(wt)cos(wt) - Acos(wt)sin(wt) = 0. \tag{2.88}$$

Hereby, A is the peak value of the grid voltage. As can be seen from 2.88, the Q component of the grid voltage is zero and 2.82 becomes;

$$\begin{bmatrix} \dot{I_D} \\ \dot{I_Q} \end{bmatrix} = \frac{1}{L}\left(\begin{bmatrix} DV_{DC(D)} \\ DV_{DC(Q)} \end{bmatrix} - \begin{bmatrix} V_{G(D)} \\ 0 \end{bmatrix}\right) + \left(\begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} - \begin{bmatrix} 0 & -w \\ w & 0 \end{bmatrix}\right)\begin{bmatrix} I_D \\ I_Q \end{bmatrix}.$$

(2.89)

Using 2.89, we can write the describing equations explicitly and draw the $D-Q$ model of the system.

$$L\frac{d}{dt}I_D = DV_{DC(D)} - V_{G(D)} - RI_D + I_Q wL, \tag{2.90}$$

$$L\frac{d}{dt}I_Q = DV_{DC(Q)} - RI_Q - I_D wL. \tag{2.91}$$

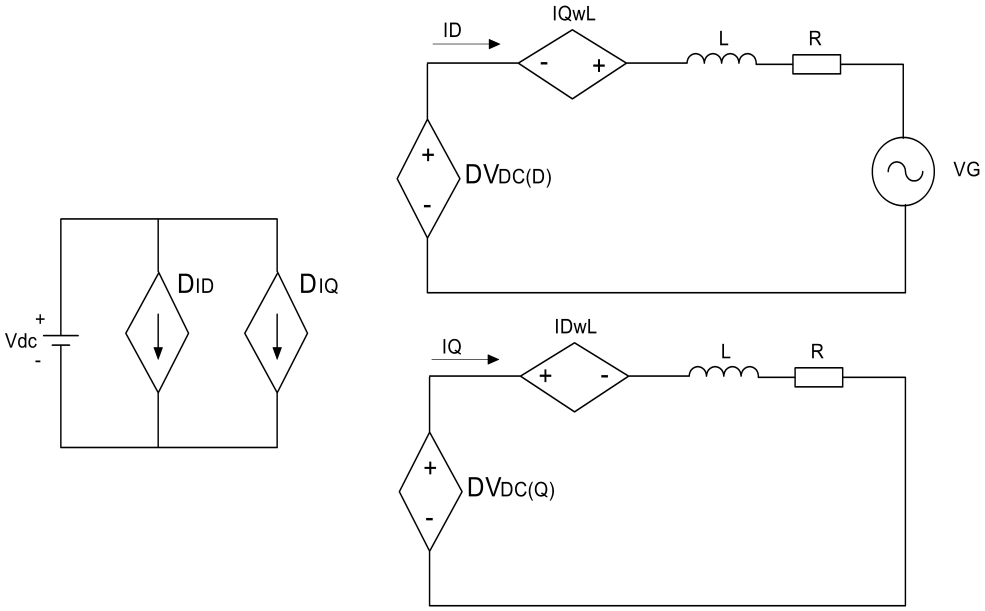

Figure 2.24 D-Q Model of the GTI.

From the control perspective, the D component of the grid voltage $V_{G(D)}$ and the cross coupling terms $I_Q wL$, $I_D wL$ are measurable output disturbances which can be canceled out in the control loop. Redrawing the model by removing the canceled output disturbances results in two identical system models for each component as shown below in fig. 2.25.

The identical transfer functions of the system can be simply written as

$$\frac{I_d(s)}{DV_{DC(D)}(s)} = \frac{1}{R+sL}, \tag{2.92}$$

$$\frac{I_q(s)}{DV_{DC(Q)}(s)} = \frac{1}{R+sL}. \tag{2.93}$$

It is important to note that the time delay in fig. 2.23 to produce the orthogonal component of the grid current is omitted in the model. The effect of the time delay will show itself as the decreased bandwidth of the feedback loop. The analytical solution of the D-Q model with a time delay is highly complicated and it was chosen to verify and adjust the bandwidth of the system by simulation.

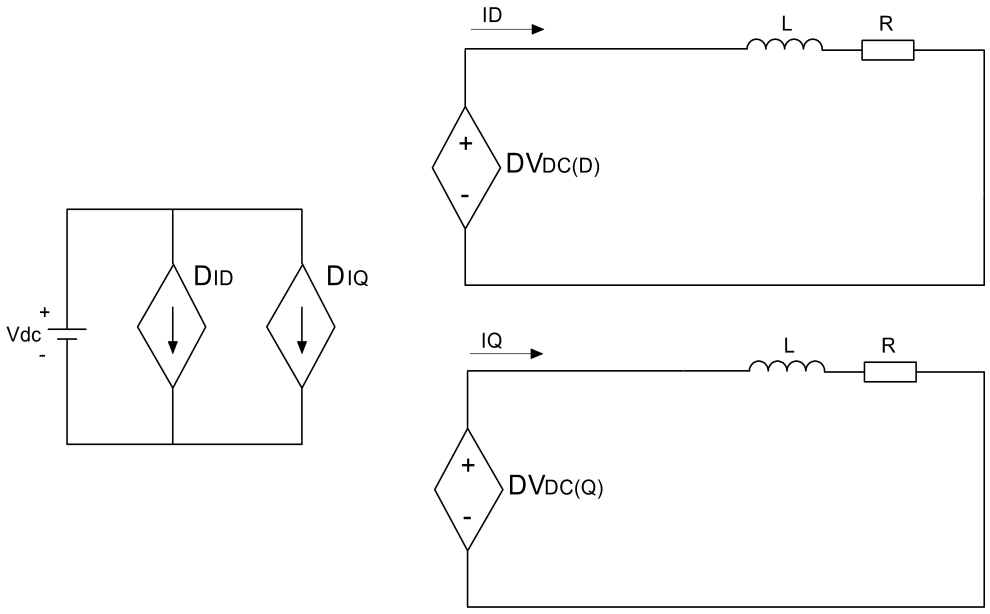

Figure 2.25 D-Q Model of the GTI Without Output Disturbances.

2.4.6 Phase Locked Loop (PLL)

The phase angle, frequency and magnitude of the grid voltage vector are the required information for the control of the grid connected systems. The required information can be obtained by using a PLL system.

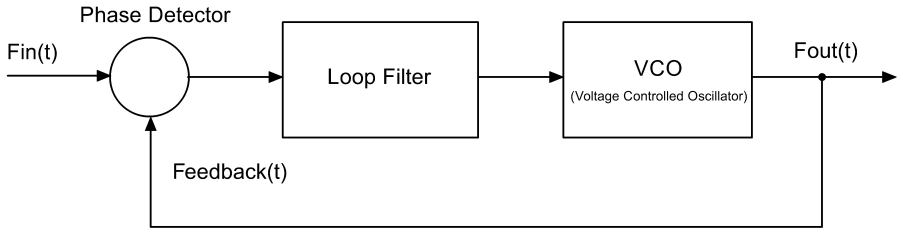

Figure 2.26 Basic Model of the PLL.

Fig. 2.26 shows the basic model of the PLL circuit. The phase detector determines the phase difference between the input signal and the feedback signal. VCO is the oscillator whose output frequency is a function of its input voltage and the Loop filter is a filter with low pass characteristic. The phase difference and the voltage vector magnitude can be obtained by using the synchronous reference frame (SRF) approach as explained in [21, 22]. Fig. 2.27 shows a transport delay based SRF PLL.

In SRF PLL, a synchronous reference frame is created by using Park's transformation. Then, the D and Q outputs of Park's transformation provide angle

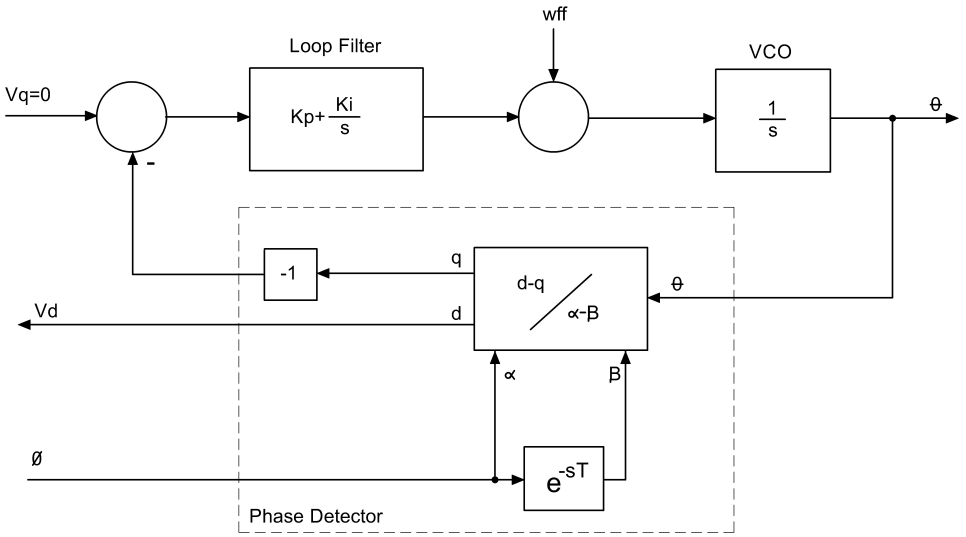

Figure 2.27 Transport Delay Based SRF PLL.

displacement information of the reference frame with respect to the grid voltage vector. When the rotational speed of the reference frame is the same as that of the grid voltage vector, the outputs D and Q become DC and their magnitude corresponds to the projection of the grid voltage vector over the D and Q axes. The D axis can be fully aligned with the grid voltage vector by setting the projection over the Q axis to zero. Once aligned, the magnitude of the D axis is the same as the magnitude of the grid voltage vector which is one of the required parameters for the control of the GTI power stage. The phase angle or the phase difference information which is used to adjust the frequency of the VCO can be obtained from the Q axis. The working principle can be explained on a Phasor diagram as shown below in fig. 2.28.

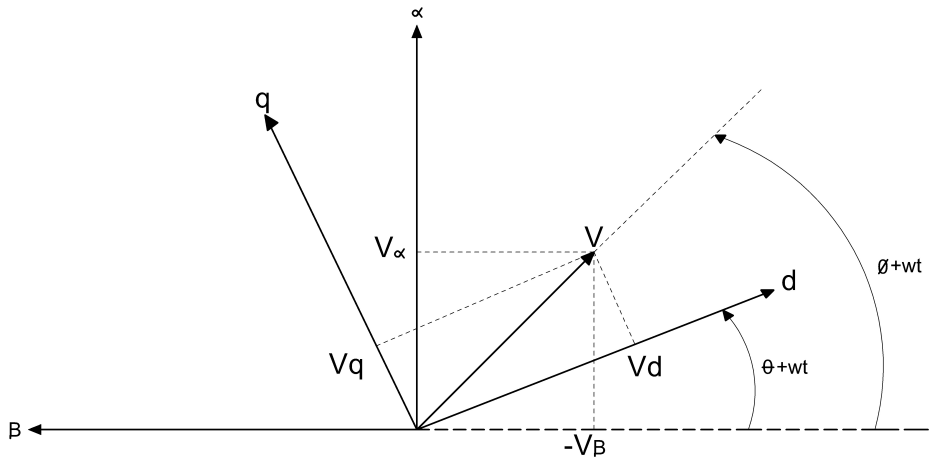

Figure 2.28 Phasor Representation of the Grid Voltage Vector, $\alpha - \beta$ and $d - q$ Axes.

In fig. 2.28, $\alpha - \beta$ are the stationary frame axes with which the vector V is referenced, $d - q$ are the frame axes which rotate synchronously to the vector V and wt is the angular speed. The magnitudes of the axes d and q can be determined by calculating the projection of the vector V over the $d - q$ axes as

$$V_d = Vcos(\phi - \theta), \tag{2.94}$$

$$V_q = Vsin(\phi - \theta). \tag{2.95}$$

Using 2.95, the model of the PLL as in fig. 2.27 can be simplified as shown in fig. 2.29.

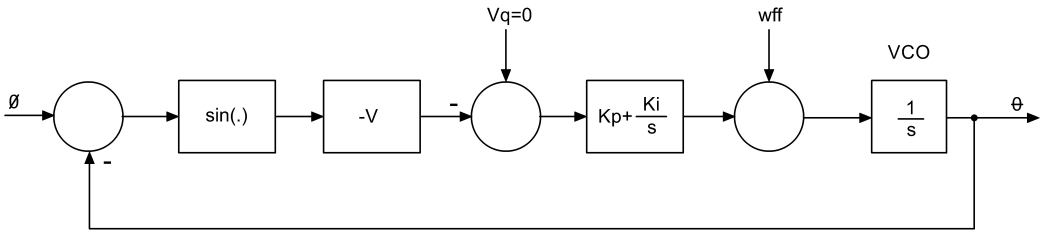

Figure 2.29 Simplified Model of the Transport Delay Based SRF PLL.

The Q output of the $d - q$ block provides information about the phase difference of the incoming signal ϕ and the output phase of the VCO θ. The simplified model is nonlinear due to the trigonometric function $sin(.)$. The main task of the PLL is to track the phase of the input signal, thus in the steady state the output phase of the VCO equals the phase of the input signal, resulting in very small variations of the phase error around zero. Defining the operating point around zero, the nonlinear model can be linearized using the Taylor series expansion of the sine function

$$sin(x) = x - \frac{x^3}{3!} + \frac{x^5}{5!} - \frac{x^7}{7!} + \frac{x^9}{9!} - ... \tag{2.96}$$

For small values of x, the values for the terms higher than the first order become much smaller and can be ignored, which results in the following approximation;

$$sin(x) = x \tag{2.97}$$

The linear model of the SRF PLL can be redrawn as shown in fig. 2.30 using 2.97.

The linear model can be used to obtain the transfer function from the input ϕ to the output θ which can be written as

$$\theta(s) = \phi(s)\frac{V(K_p s + K_i)}{s^2} - \theta(s)\frac{V(K_p s + K_i)}{s^2}. \tag{2.98}$$

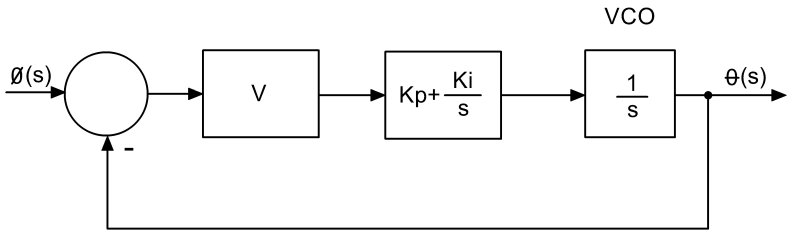

Figure 2.30 Linear Model of the SRF PLL.

Arranging 2.98 yields a typical second order transfer function with

$$\frac{\theta(s)}{\phi(s)} = \frac{V(K_p s + K_i)}{s^2 + V(K_p s + K_i)}. \tag{2.99}$$

2.5 CHAPTER SUMMARY

In this chapter the small signal model of the Z-source inverter is developed and the transfer functions needed to control the ZSI are derived. The D-Q model of the GTI and the synchronous reference frame PLL circuit are studied, whereby the derivation of the relevant transfer functions is performed. Based on the transfer functions derived in this section, the control design will be studied in the subsequent chapters.

CHAPTER III

DESIGN AND SIMULATION OF THE GTI

3.1 INTRODUCTION

In this chapter, the design and verification of the design parameters for the grid tie inverter by simulation is presented. In the first section, design parameters are defined. According to the design parameters, component values are calculated using the derivations presented in the previous chapter. The circuit with the calculated components is simulated in Simulink to verify the accuracy of the derivations. In the second section, feedback controllers for the PLL, DC link voltage and the line input current are designed. Simulations for the designed closed loop systems are presented.

3.2 THE Z-SOURCE CONVERTER

The parameters defined for the design of the Z-Source Converter are listed in table 3.1. The maximum output power $P_{O_{max}}$ is set as the design target. The switching frequency F_S is one of the key parameters in the design and its selection is a compromise between many factors. Considering the switching speeds of the available IGBTs, instruction execution speed of the affordable microcontrollers and size of the inductances it is decided to set the switching frequency to 40kHz. The minimum output power $P_{O_{min}}$ has a direct relationship to F_S and the value listed in the table is found reasonable to keep the size of the system small. The Z-source components L, C, L_O and shoot-through duty cycle d_s are calculated according to the design parameters and simulated to verify the accuracy of the derivations.

To determine the gain of the Z-source converter, it is first required to find the peak value of the maximum grid voltage. Since the power flow should be from the

Parameter	Symbol	Value	Unit
Max. Output Power	$P_{O_{max}}$	1000	W
Min. Output Power	$P_{O_{min}}$	110	W
Max. Grid Voltage	$V_{g_{max}}$	235	V_{RMS}
Min. Grid Voltage	$V_{g_{min}}$	190	V_{RMS}
Min. Input Voltage	$V_{i_{min}}$	245	V_{DC}
Operating Frequency	F_S	40	kHz
Z-Source Capacitor Ripple Voltage	ΔV_C	75	mV
Output Inductor Ripple Current	ΔI_{L_O}	30	% of I_O at $P_{O_{max}}$

Table 3.1 Z-Source Design Parameters.

GTI to the grid, the DC link voltage V_{DC} should be greater than the maximum value of the grid voltage. Taking into account the switch and the conduction losses of the wiring and the output filter (V_{loss}), the required output voltage V_O of the GTI will be set (V_{loss}) volts higher than the determined V_O. The average output voltage over a switching period of the Full bridge using (2.67) is

$$V_O = V_{S2} = DV_{DC} \tag{3.1}$$

and the required DC link voltage is

$$V_{DC} = \frac{V_O + V_{loss}}{D}. \tag{3.2}$$

The peak value of the maximum grid voltage is

$$V_{g_{peak}} = V_{g_{max}} \cdot \sqrt{2} \qquad V_{g_{peak}} = 235 \cdot \sqrt{2} = 332.3V. \tag{3.3}$$

The maximum duty cycle D for the grid current control can occupy the interval of the period that remains from the maximum shoot-through duty cycle d_s, That is,

$$D = 1 - d_s. \tag{3.4}$$

Equating the Z-source input to output voltage relation (2.19) to (3.2) and solving for d_s yields the shoot-through duty cycle d_s and the DC link voltage V_{DC} as

$$\frac{V_{i_{min}}}{1 - 2d_s} = \frac{V_O + V_{loss}}{1 - d_s} \qquad , \qquad d_s = \frac{V_O + V_{loss} - V_i}{2(V_O + V_{loss}) - V_i}. \tag{3.5}$$

By setting $V_{loss} = 10$ Volts, d_s is found as

$$d_s = \frac{332.3 + 10 - 245}{2 \cdot (332.3 + 10) - 245} = 0.2213. \tag{3.6}$$

Using (3.2) and (3.4),

$$V_{DC} = \frac{V_O + V_{loss}}{D} \ , \ V_{DC} = 439.6V. \tag{3.7}$$

The maximum output current of the Z-source is found to be

$$I_O = \frac{P_{O_{max}}}{V_O} \ , \ I_O = \frac{1000}{342.3} = 2.92A \tag{3.8}$$

and the current I_L through the Z-source inductor L and the input current I_I to the Z-source using (2.23) and (2.24) are

$$I_L = I_I = \frac{1 - d_s}{1 - 2d_s} I_O \ , \ I_L = I_I = \frac{1 - 0.2213}{1 - 2 \cdot 0.2213} \cdot 2.92 = 4.08A. \tag{3.9}$$

Using (2.20), the average switch current I_S can be found as

$$I_S = d_s(2I_L - I_O) \ , \ I_S = 0.2213 \cdot (2 \cdot 4.08 - 2.92) = 1.16A. \tag{3.10}$$

Using (2.14) the Z-source capacitor voltage V_C is found as

$$\frac{V_C}{V_i} = \frac{1 - d_s}{1 - 2d_s} \ , \ V_C = \frac{1 - 0.2213}{1 - 2 \cdot 0.2213} \cdot 245 = 342.3V. \tag{3.11}$$

Having found V_C, we can determine the required load resistance $R_{O_{max}}$ for the minimum output power $P_{O_{min}}$ as

$$R_{O_{max}} = \frac{(V_C)^2}{P_{O_{min}}} \ , \ R_{O_{max}} = \frac{342.3^2}{110} = 1065\Omega \tag{3.12}$$

and $R_{O_{min}}$ for the maximum output power $P_{O_{max}}$ as

$$R_{O_{min}} = \frac{(V_C)^2}{P_{O_{max}}} \ , \ R_{O_{min}} = \frac{342.3^2}{1000} = 117.2\Omega. \tag{3.13}$$

3.2.1 Determination of the Z-Source Capacitor Value

Using the design parameters in table 3.1 and (2.8), the value of the capacitor is found as

$$\Delta V_C = \frac{I_L d_s T_S}{C} \ , \ C = \frac{4.08 \cdot 0.2213 \cdot 25 \cdot 10^{-6}}{0.075} = 301\mu F. \tag{3.14}$$

The standard value of $330\mu F$ will be used for the value of C. Then the ripple voltage ΔV_C becomes

$$\Delta V_C = \frac{I_L d_s T_S}{C} \ , \ \Delta V_C = \frac{4.08 \cdot 0.2213 \cdot 25 \cdot 10^{-6}}{330 \cdot 10^{-6}} = 68.4mV. \tag{3.15}$$

3.2.2 Determination of the Z-Source Inductor Value

The output current I_O at minimum output power defined in table 3.1 is

$$I_O = \frac{P_{O_{min}}}{V_O} \ , \ I_O = \frac{110}{342.3} = 321mA. \tag{3.16}$$

Using (2.32), the condition for the continuous conduction mode can be written as

$$R_O \leq \frac{L}{(1-2d_s)d_sT_S} \text{ and thus } L \geq (1-2d_s)d_sT_SR_O. \tag{3.17}$$

The inductance value L that keeps the Z-source in continuous conduction mode with the minimum output power is

$$L \geq (1 - 2 \cdot 0.2213) \cdot 0.2213 \cdot 25 \cdot 10^{-6} \cdot 1065 = 3.28mH. \tag{3.18}$$

3.5mH Inductors will be used for the Z-source. The Inductor ripple current ΔI_L using (2.4) is

$$\Delta I_L = \frac{V_C d_s T_S}{L} \ , \ \Delta I_L = \frac{342.3 \cdot 0.2213 \cdot 25 \cdot 10^{-6}}{3.5 \cdot 10^{-3}} = 541mA. \tag{3.19}$$

3.2.3 Determination of the Output Inductor value

The requirement for the output ripple current ΔI_{LO} in table 3.1 is

$$\Delta I_{LO} = 0.3 \cdot I_{O_{(Pmax)}} \ , \ \Delta I_{LO} = 0.3 \cdot 2.92 = 0.88A. \tag{3.20}$$

Using (2.72), we obtain

$$L_O = \frac{V_{DC}T_S}{4\Delta I_{L_O}} \ , \ L_O = \frac{445.6 \cdot 25 \cdot 10^{-6}}{4 \cdot 0.88} = 3.2mH. \tag{3.21}$$

The output inductor L_O will be set to 3.5 mH. The designed circuit parameters for simulation are shown in table 3.2.

The circuit with the designed component values is simulated in MATLAB. The switched model of the Z-source converter is connected to a PWM generator with fixed duty cycle and the simulation is run for at least 1 second for the system to settle down to the steady state. The average and instantaneous values are recorded in the workspace. The results of the simulation are compared to the derived values to verify the accuracy of the derivations. In the derivations, the

Parameter	Symbol	Value	Unit
Capacitor Value	C	330	μF
Inductor Value	L	3.5	mH
Output Inductor Value	L_O	3.5	mH
Max. Output Resistance Value	$R_{O_{max}}$	1065	Ω
Min. Output Resistance Value	$R_{O_{min}}$	117.2	Ω

Table 3.2 Designed Circuit Parameters for the Z-Source.

components are considered to be ideal (lossless) to simplify the calculations. In the simulation, the components are also given very low parasitic characteristics to comply with the derivation conditions. The results of the simulation will reflect the condition where the efficiency η is close to unity. The simulation setup is shown in fig. 3.1.

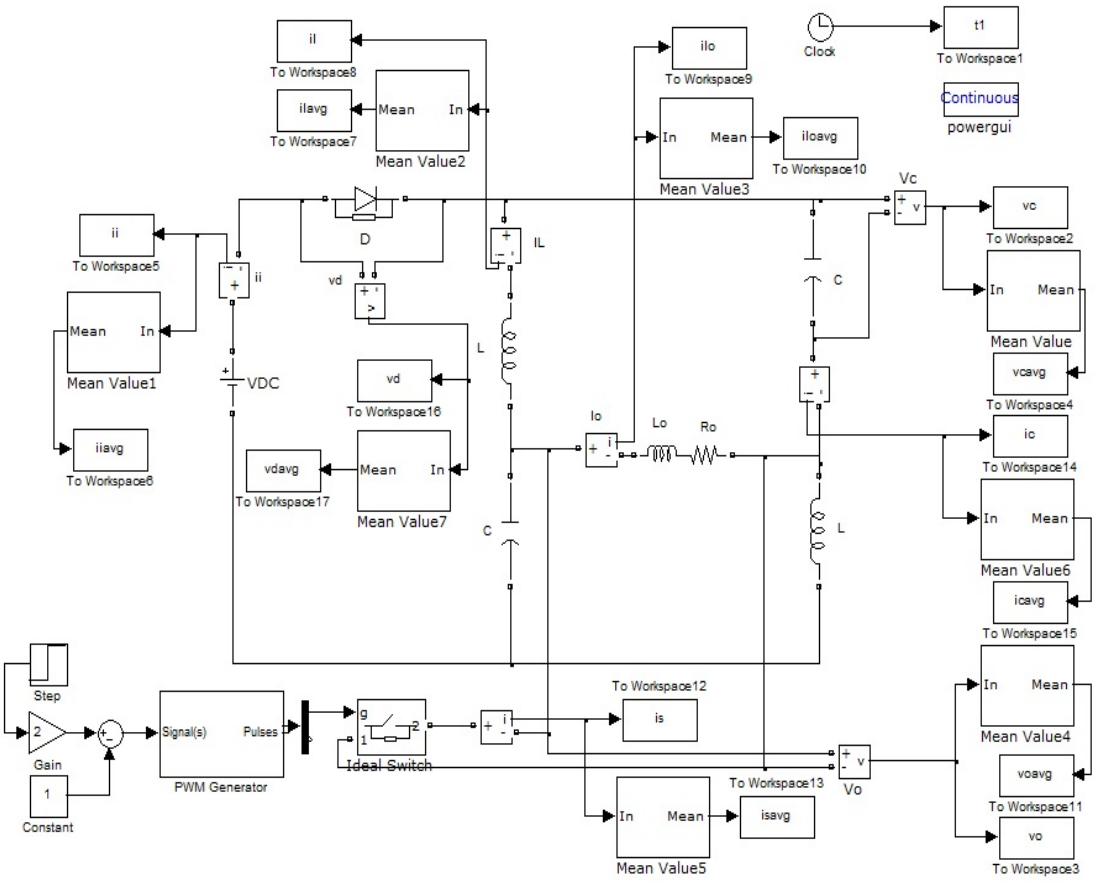

Figure 3.1 Simulation Setup for the Z-Source Converter.

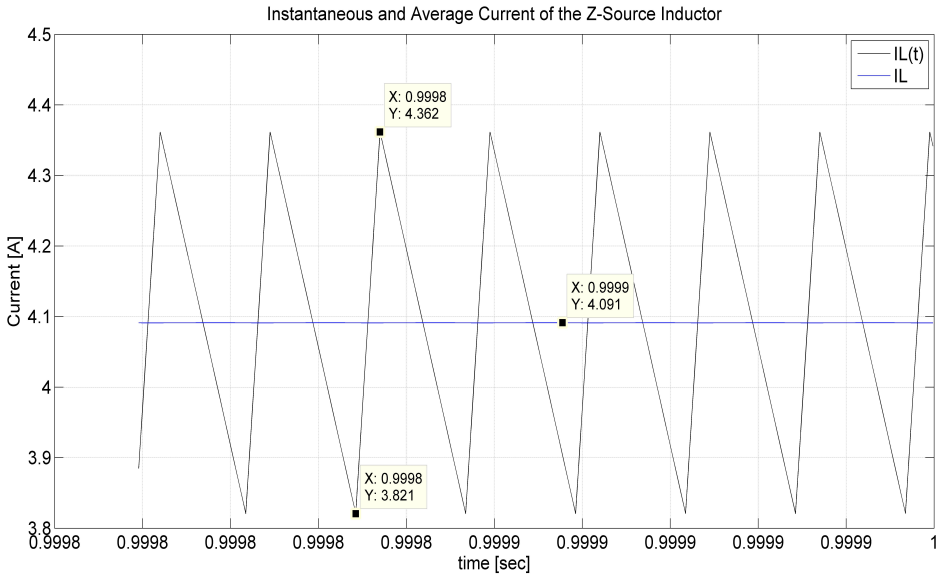

Figure 3.2 Instantaneous and Average Current I_L of ZSC at $P_{O_{max}}$.

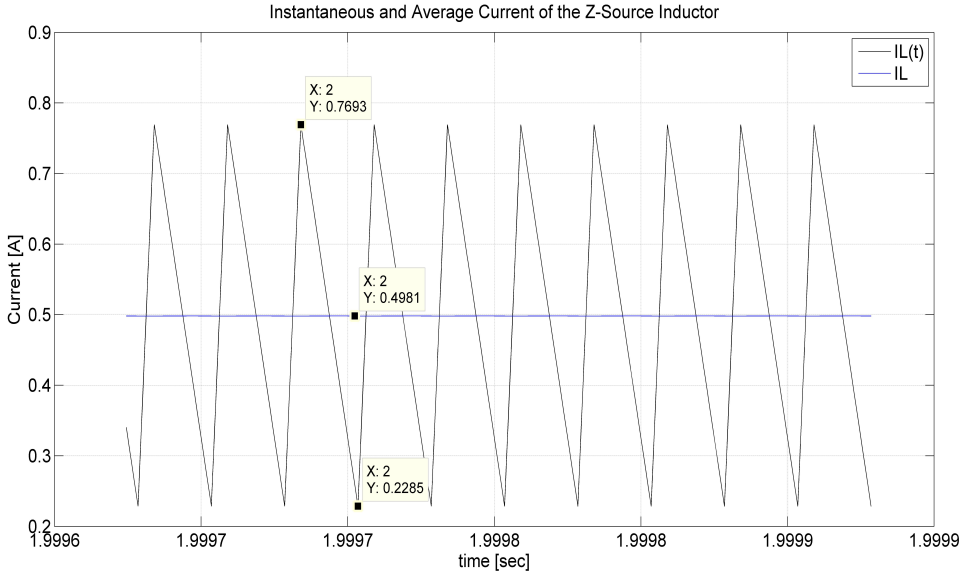

Figure 3.3 Instantaneous and Average Current I_L of ZSC at $P_{O_{min}}$.

The simulation results for the Z-Source inductor current for maximum and minimum output load are shown in fig. 3.2 and fig. 3.3, respectively. The calculated inductor ripple current ΔI_L in (3.19) and average inductor current I_L in (3.9) are in agreement with the simulation results.

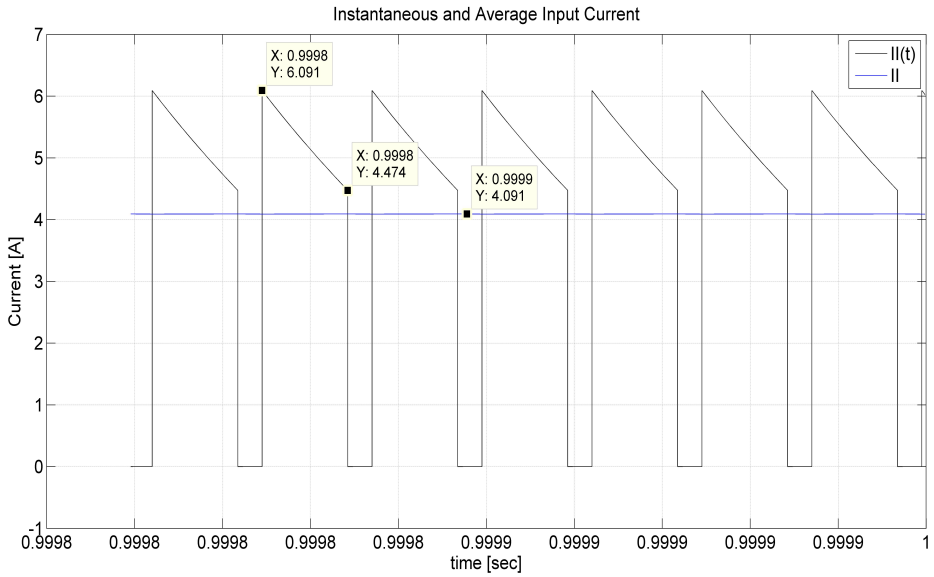

Figure 3.4 Instantaneous and Average Input Current I_I of ZSC at $P_{O_{max}}$.

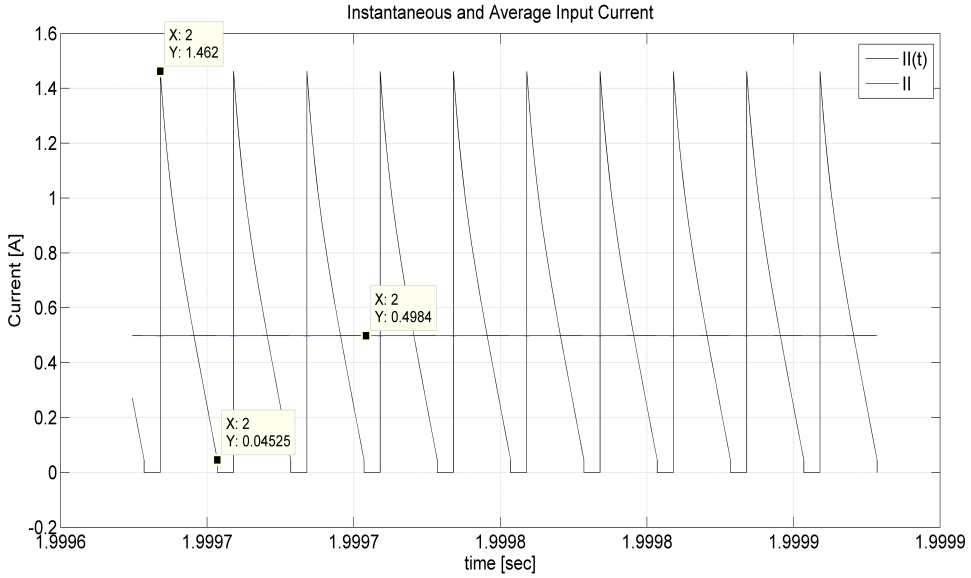

Figure 3.5 Instantaneous and Average Input Current I_I of ZSC at $P_{O_{min}}$.

The simulation result in fig. 3.5 show that the input current I_I is continuous during the switch off time, thus it is also verified by simulation that the circuit is in CCM for the minimum output power $P_{O_{min}}$. Fig. 3.4 shows the input current I_I for the maximum output power $P_{O_{max}}$.

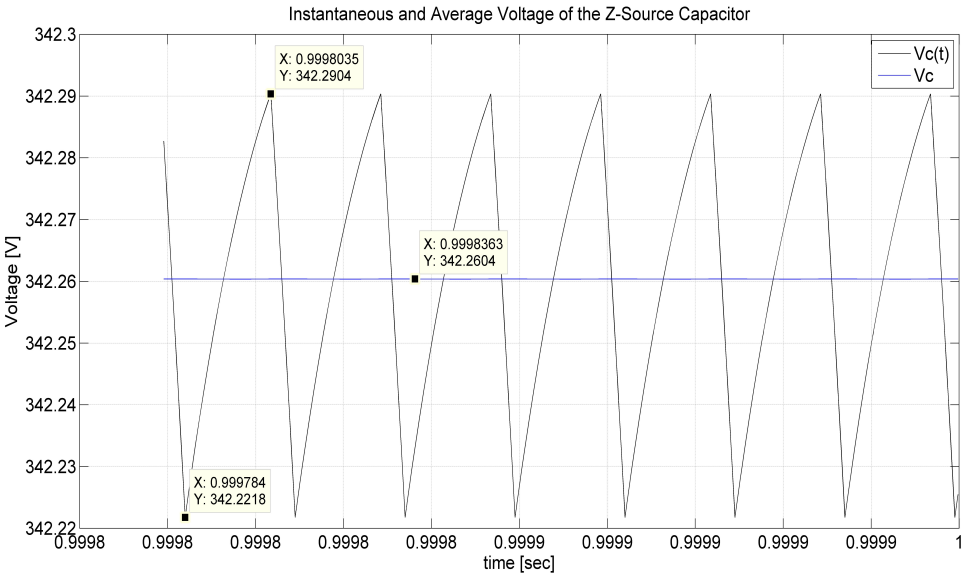

Figure 3.6 Instantaneous and Average Voltage of V_C of ZSC at $P_{O_{max}}$.

Fig. 3.6 shows the instantaneous and average voltage of the capacitor C. The calculated values for ΔV_C in (3.15) and V_C in (3.11) are in agreement with the simulation results.

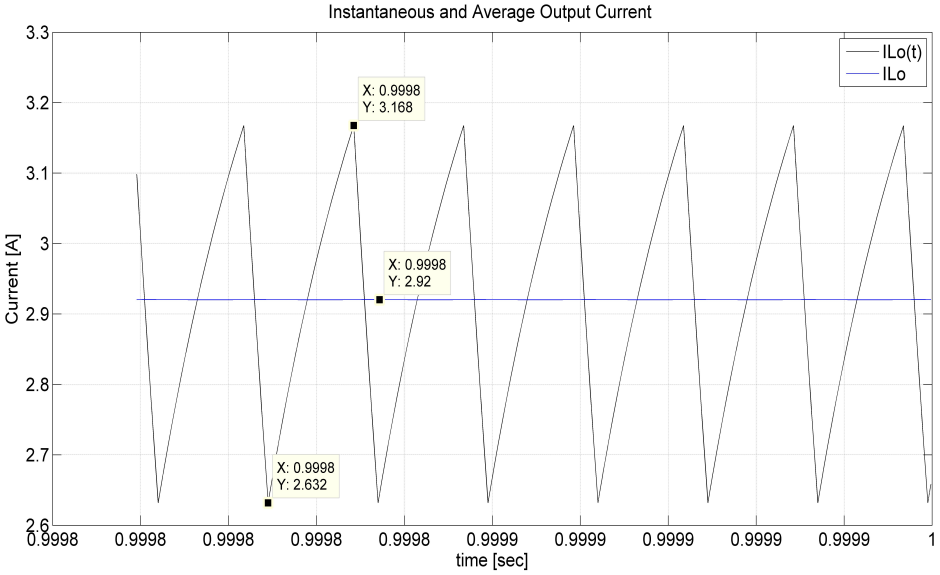

Figure 3.7 Instantaneous and Average Current of I_{LO} of ZSC at $P_{O_{max}}$.

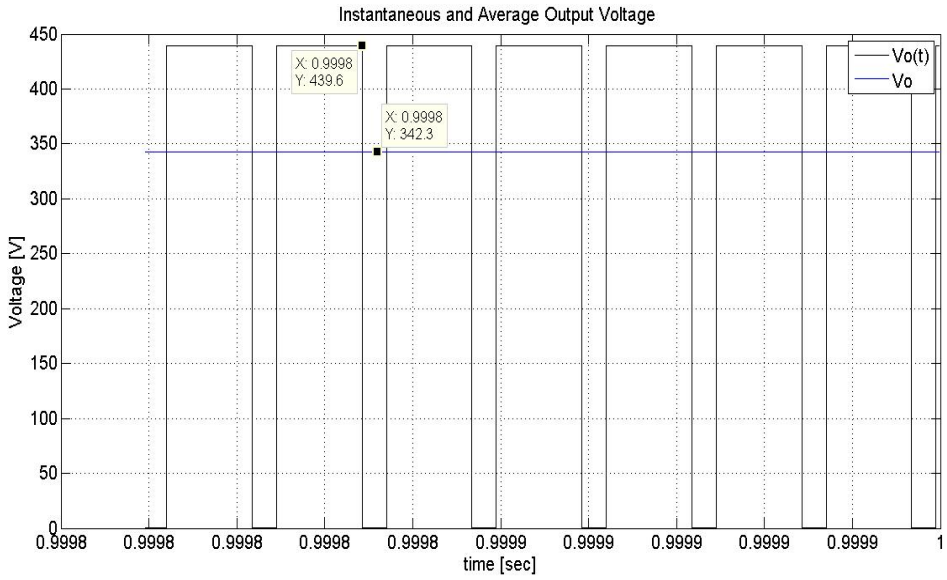

Figure 3.8 Instantaneous and Average Value of V_O of ZSC at $P_{O_{max}}$.

The simulation results for the output current I_{LO} and the output voltage V_O are shown in fig. 3.7 and fig. 3.8 respectively. They are both consistent with the calculations in (3.8) and (3.11).

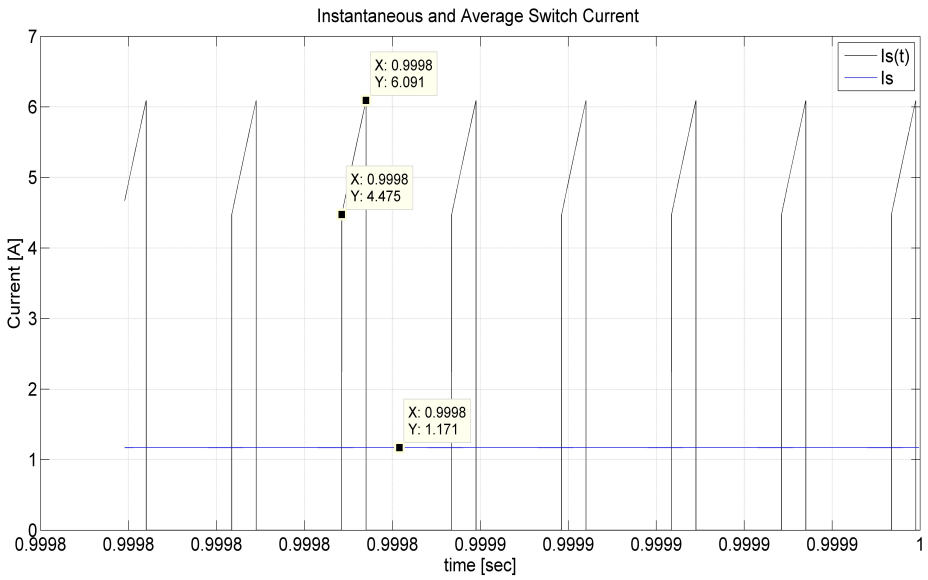

Figure 3.9 Instantaneous and Average Value of Switch Current I_S of ZSC at $P_{O_{max}}$.

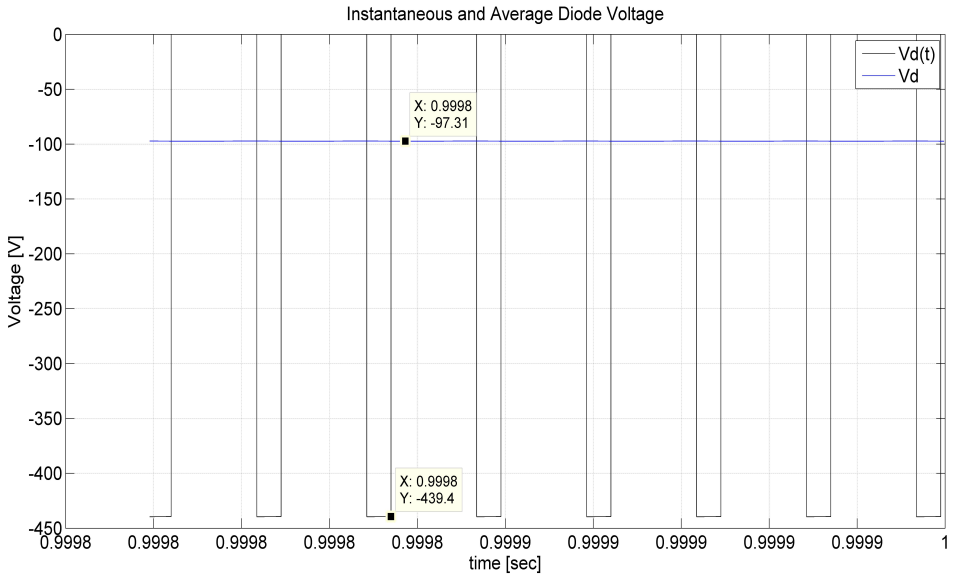

Figure 3.10 Instantaneous and Average Value of the Diode Voltage V_D of ZSC at $P_{O_{max}}$.

The simulation results for the instantaneous and average values of switch current I_S and diode voltage V_D are shown in figures 3.9 and 3.10 respectively.

3.2.4 Controller Design for Stabilisation of the Z-Source Capacitor Voltage V_C

The transfer function T_{cc} of the Z-source converter from the control input d_s to capacitor voltage V_C with the designed circuit parameters can be calculated using (2.63). The transfer function T_{cc} is used to stabilize the DC-Link voltage which is achieved by estimation rather than direct measurement. The floating nature of the DC-Link in the Z-source converter makes it difficult to measure the DC-Link directly, an easier way to stabilise the DC-Link is to measure and use the input and one of the capacitor voltages of the Z-Source to estimate the DC-Link voltage [23]. The transfer function is calculated using MATLAB by substituting the impedances and operating point and evaluating (2.63) with the substitutions as follows.

$$z_L = sL \tag{3.22}$$

$$z_C = \frac{1}{sC} \tag{3.23}$$

$$z_O = R_O + sL_O \tag{3.24}$$

$$D' = 1 - d_s \tag{3.25}$$

$$V_C = \frac{1 - d_s}{1 - 2d_s} V_I \tag{3.26}$$

$$V_O = (1 - d_s)(2V_C - V_I) \tag{3.27}$$

$$I = \frac{1 - d_s}{1 - 2d_s} \frac{V_C}{R_O}. \tag{3.28}$$

Using the operating point and the substitutions above, the transfer function T_{cc} is calculated as

$$T_{cc} = \frac{-1.588 \cdot 10^4 s^2 - 2.328 \cdot 10^7 s + 7.103 \cdot 10^{12}}{s^3 + 3.349 \cdot 10^4 s^2 + 1.319 \cdot 10^6 s + 9.005 \cdot 10^9}. \tag{3.29}$$

The Bode diagram of the transfer function T_{cc} is shown in fig. 3.11.

The locations of the poles and zeros of the T_{cc} are $P_1 = -33454$ rad/sec, $P_{2,3} = -15.68 \mp 518j$ rad/sec, $Z_1 = -21894$ rad/sec, $Z_2 = 20428$ rad/sec. The pole locations show that the T_{cc} is stable but there is a right half plane zero (RHP) at 20428 rad/sec. The system is non-minimum-phase which means thats the output will fall before rising (undershoot) when a step increase in d_s occurs. A PID controller with zero derivative coefficient obtained by simulation is found

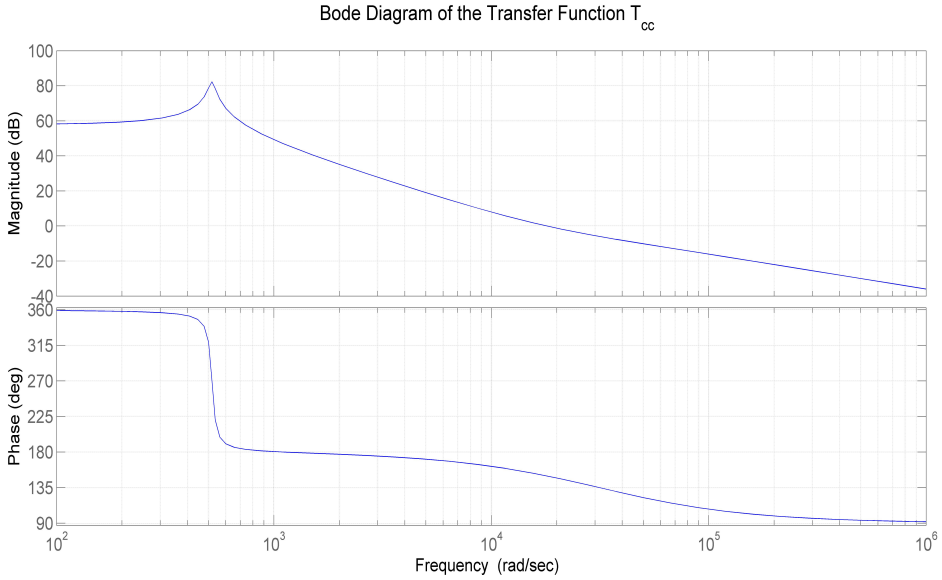

Figure 3.11 Bode Diagram of the Transfer Function T_{cc}.

satisfactory for the closed loop performance. A low pass filter $H(s)$ in the feedback path with a cut off frequency of 3000 rad/sec is also included to account for the delays and filtering requirements. The parameters for the controller $C_z(s)$ are $K_p = 0.048$, $K_i = 5.4$ and $K_d = 0$. The continuous time transfer function of the controller is

$$C_z(s) = \frac{0.048s + 5.4}{s(s + 90)}. \tag{3.30}$$

The bode plot of the compensated system is shown in fig. 3.12. The phase and gain margins are 66.3 deg at 43 rad/sec and 15.1 dB at 495 rad/sec. respectively. The step response of the closed loop feedback system is shown in fig. 3.13.

Since the controller will be implemented digitally, the transfer function $C_z(s)$ should be discretized. Using MATLAB, the discrete time transfer function $C_z(z)$ is calculated as

$$C_z(z) = \frac{\overbrace{1.216 \cdot 10^{-7}}^{a} z - \overbrace{1.182 \cdot 10^{-7}}^{b}}{z^2 - \underbrace{1.998}_{c} + \underbrace{0.9978}_{d}} \tag{3.31}$$

The sampling time T_s is $25 \cdot 10^{-6}$, which is the switching period of the Z-source converter. The control algorithm is then calculated as

$$\frac{Y(z)}{E(z)} = \frac{az - b}{z^2 - cz + d} \tag{3.32}$$

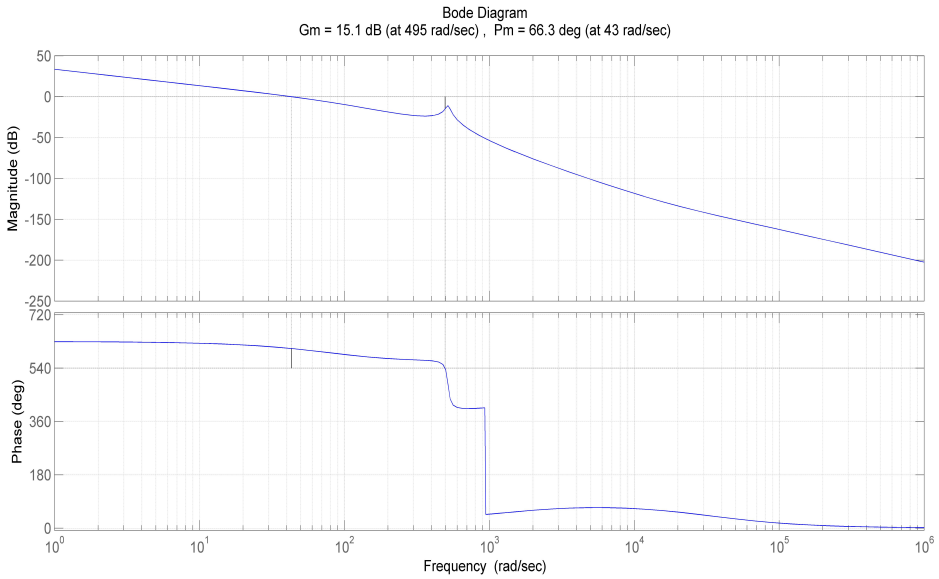

Figure 3.12 Bode Diagram of the Compensated System.

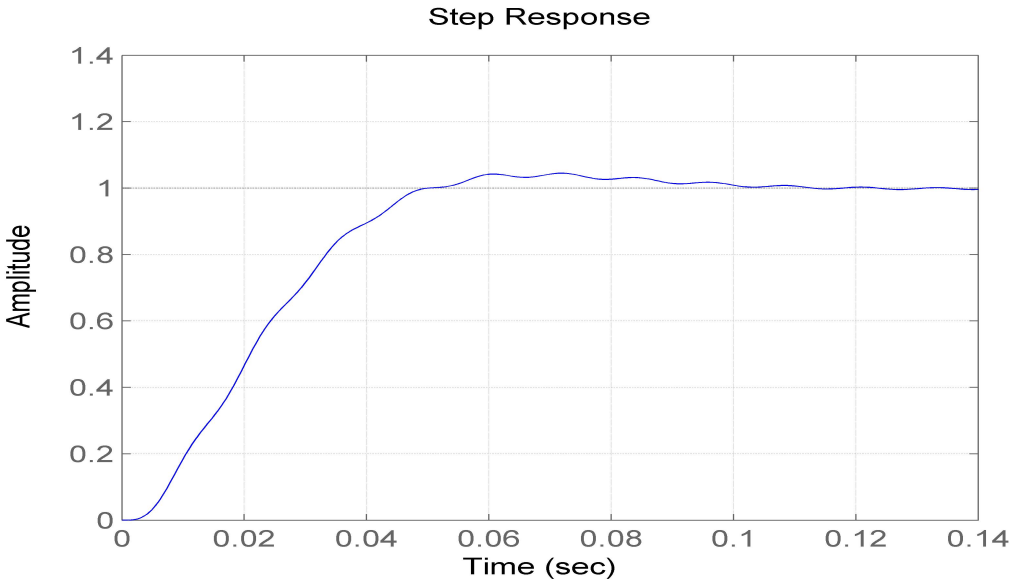

Figure 3.13 Step Response of the Closed Loop System.

$$Y(z)(z^2 - cz + d) = (az - b)E(z) \tag{3.33}$$

$$Y(z)(1 - cz^{-1} + dz^{-2}) = (az^{-1} - bz^{-2})E(z) \tag{3.34}$$

$$Y_k = cY_{k-1} - dY_{k-2} + aE_{k-1} - bE_{k-2}. \tag{3.35}$$

The Z-source switching circuit is simulated in MATLAB using the difference equation 3.35 as the controller. The simulation setup and the simulation result are shown in fig. 3.14 and fig. 3.15 respectively .

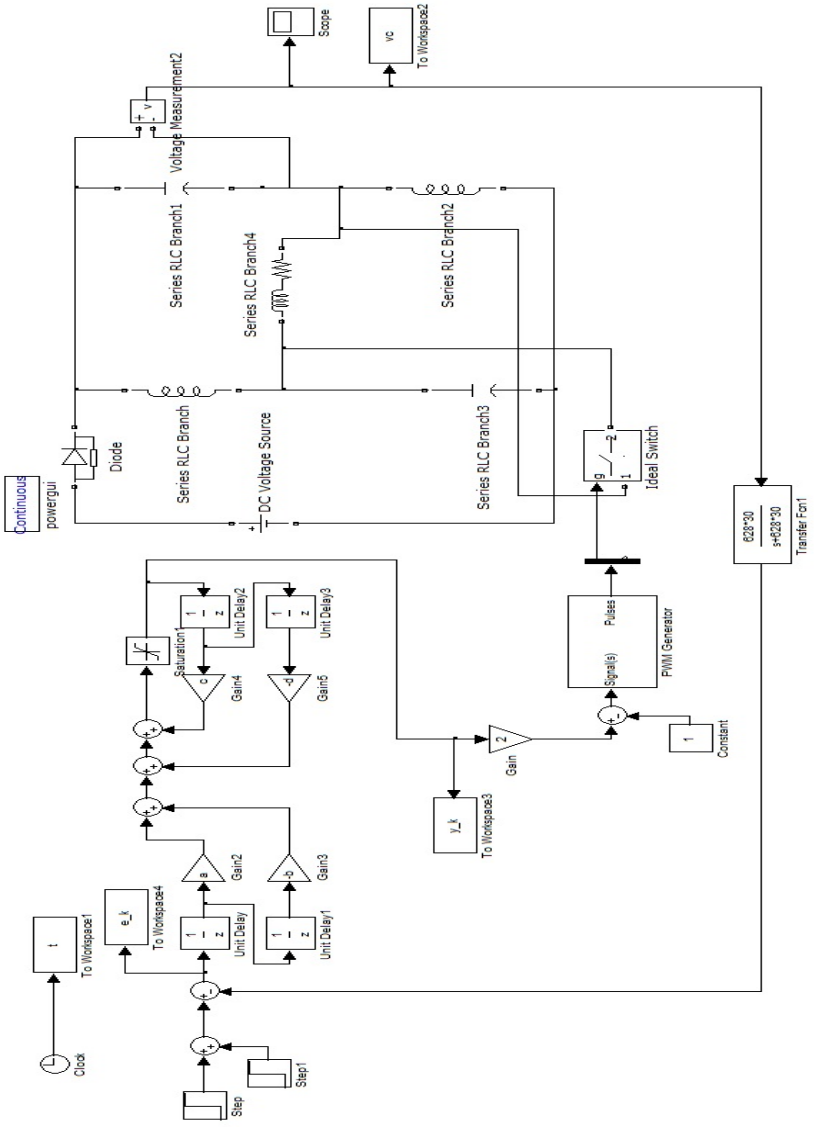

Figure 3.14 Simulation Setup for Z-Source Closed Loop Feedback Control With Digital Controller.

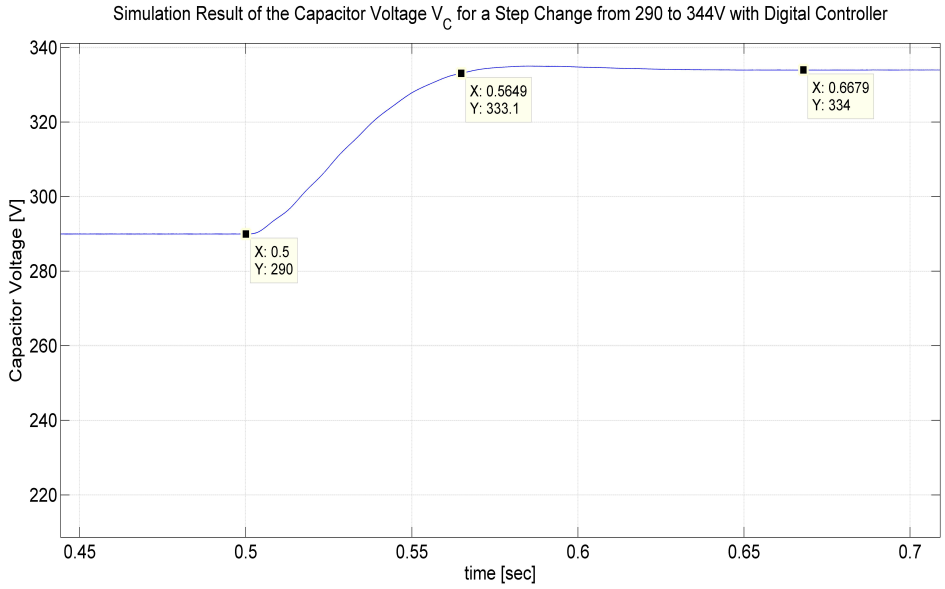

Figure 3.15 Simulation Result of a Step Change in the Capacitor Voltage V_C From 290 to 344 V With Digital Controller.

3.3 DESIGN OF THE CONTROLLER FOR THE PHASE LOCKED LOOP "*PLL*"

The transfer function in (2.99) is a second order transfer function. The controller can be designed using different methods such as using well known properties of the second order systems or the parameters of the controller can be manually adjusted by looking at the step response of the closed feedback loop. The expected performance criteria from the PLL is to have a stable VCO output even under distorted grid condition. High bandwidth may increase the sensitivity to disturbances and low bandwidth may degrade the system performance. Although it can be improved further, the parameters K_p and K_i obtained by manual tuning are found to be satisfactory for the PLL system. The parameters obtained are $K_p = 0.1$ and $K_i = 5$. The nominal grid voltage is taken to be $220V_{rms}$ and the magnitude of the grid voltage vector V at nominal grid voltage is $V = 220 \cdot \sqrt{2} = 311$.

Evaluating (2.99) with the defined parameters K_p , K_i and V, the closed loop transfer function T_{pll} of the PLL is found as

$$T_{pll} = \frac{31.1s + 1555}{s^2 + 31.1s + 1555}. \tag{3.36}$$

The PI controller $C(s)$ with the defined parameters K_p and K_i is

$$C(s) = \frac{0.1s + 5}{s}. \tag{3.37}$$

The step response of the closed loop system is shown in fig. 3.16.

The controller $C(s)$ is discretized in MATLAB, the corresponding discrete time controller $C_z(z)$ with sampling time $T_s = 25 \cdot 10^{-6}$ is

$$C_z(z) = \frac{\overbrace{0.1}^{a} z - \overbrace{0.09988}^{b}}{z - 1}. \tag{3.38}$$

The control algorithm is calculated using 3.38 as

$$\frac{Y(z)}{E(z)} = \frac{az - b}{z - 1} \tag{3.39}$$

$$Y(z)(z - 1) = (az - b)E(z) \tag{3.40}$$

$$Y(z)(1 - z^{-1}) = (a - bz^{-1})E(z) \tag{3.41}$$

$$Y_k = aE_k - bE_{k-1} + Y_{k-1}. \tag{3.42}$$

The digital controller in (3.42) is simulated in SIMULINK with a phase jump of -90 degrees in the grid voltage.

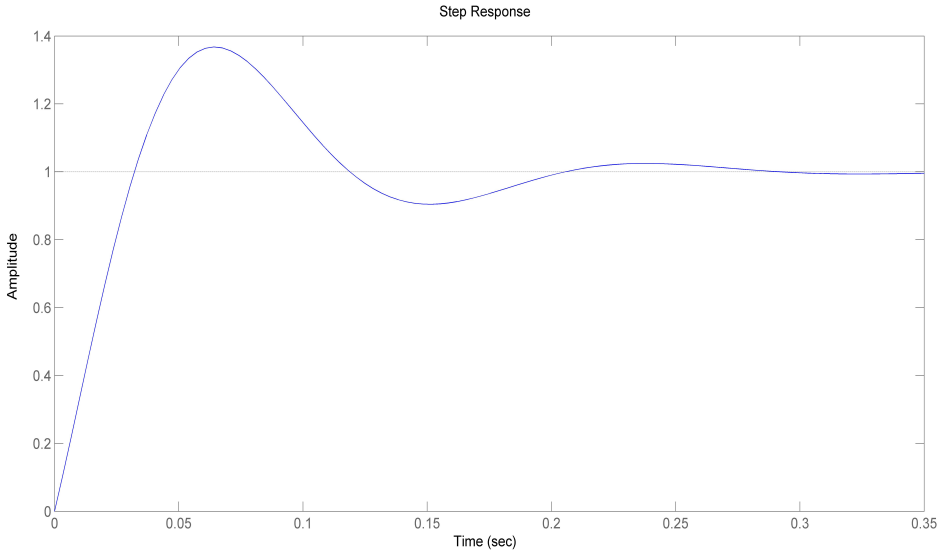

Figure 3.16 Step Response of the Closed Loop System T_{pll}.

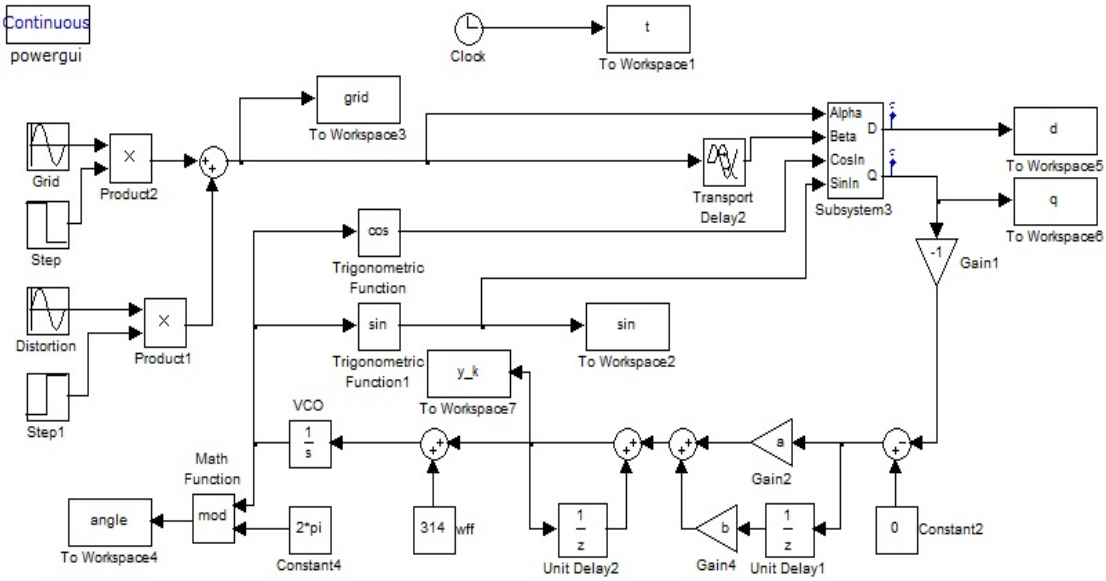

Figure 3.17 Simulation Setup for the PLL Circuit.

Fig. 3.17 shows the simulation setup for the PLL circuit in fig. 2.27.

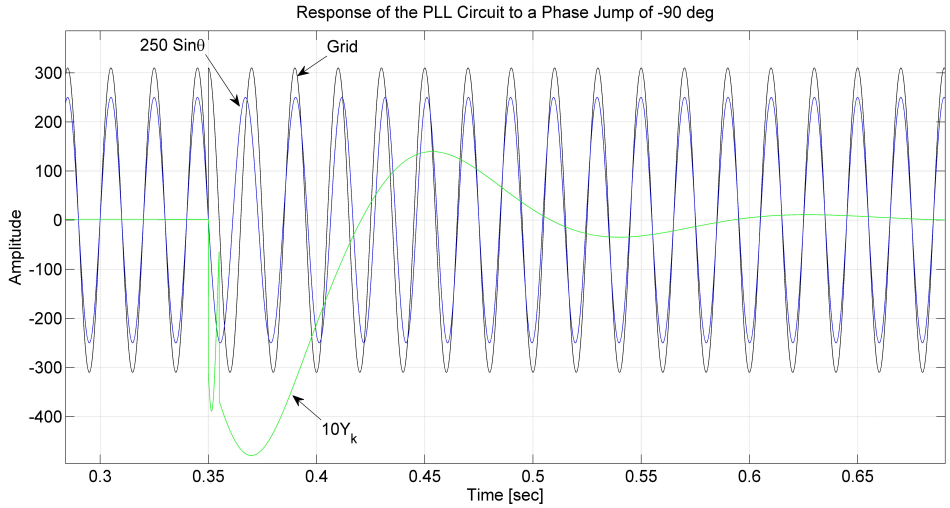

Figure 3.18 Response of the PLL Circuit to a -90 deg. Phase Jump. (Grid, Sinθ and Controller Output)

Fig. 3.18 shows the response of the PLL to a -90 degree phase jump at $t = 0.35sec$. Please note that $sin\theta$ and the controller output Y_k are scaled for the sake of clarity.

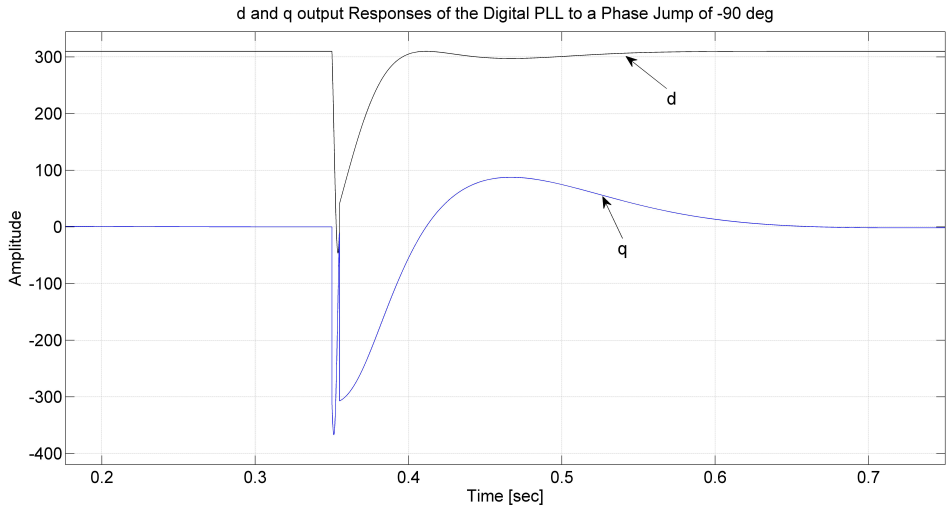

Figure 3.19 Response of the PLL Circuit to a -90 deg. Phase Jump. (d and q Outputs)

Fig. 3.19 shows the response of the D and Q outputs of the PLL to a -90 degree phase jump at $t = 0.35sec$. Many simulations were carried out including distorted grid conditions and it was found that the designed controller stabilizes the system and the performance of the PLL is satisfactory.

3.4 DESIGN OF THE CONTROLLER FOR THE GRID CURRENT CONTROL (D-Q CONTROL)

D-Q control is intended to stabilize the supplied grid current. The controllers should be designed such that the current sent to the grid has low harmonic content and is in phase with the grid voltage. There are two identical first order plant models in (2.92) and (2.93) which will result in two identical PI controllers for the D and Q components of the grid current. The value of the output inductor L_o which is denoted as L in (2.92) and (2.93) is determined in (3.21) and listed in table 3.2. The resistance value R represents the parasitic resistances. The estimated parasitic resistance of the output inductance is 0.1Ω. Considering the additional wiring resistances, the value of R is set to 0.3Ω. The plant model $G_{DQ}(s)$ is then calculated as

$$G_{DQ}(s) = \frac{1}{0.0035s + 0.3}. \tag{3.43}$$

The parameters of the stabilizing PI controller are determined as $K_p = 2.4$ and $K_i = 607.5$ by manual tuning. The transfer function of the controller $C(s)$ is

$$C(s) = \frac{2.4s + 607.5}{s}. \tag{3.44}$$

The Bode plot of the feedback system is shown in fig. 3.20.

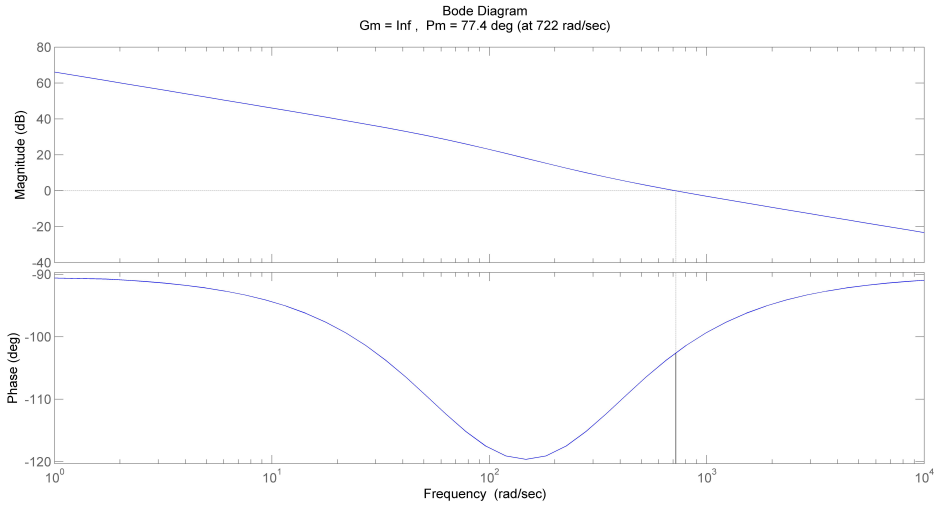

Figure 3.20 Bode Plot of the Compensated Feedback System for D-Q Control.

Although it can be deduced from the bode plot that the bandwidth of the system can be increased because of the high phase and infinite gain margins, simulations

show that some oscillatory behaviour in the waveforms starts when increasing the controller gain by 20. This is because the transport delay used to produce the orthogonal component is not included in the D-Q modeling for simplification. It was decided to a use low bandwidth feedback system for the implementation at the beginning to stay away from the instability, then the feedback system can be improved according to the real implementation results. The step response of

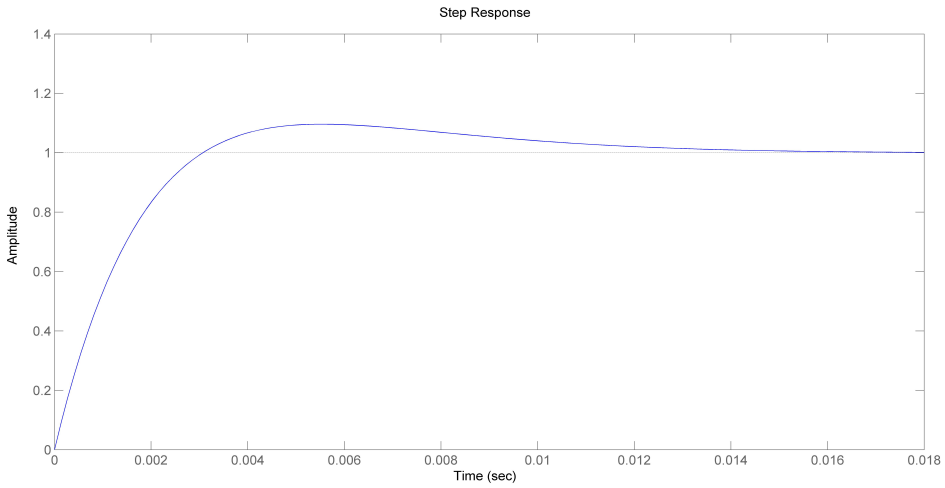

Figure 3.21 Step Response of the D-Q Closed Loop System.

the feedback system with the designed controller $C(s)$ is shown in fig. 3.21. A simulation of the D-Q control block in SIMULINK is carried out with the setup as shown in fig. 3.22. The D-Q control block consists of two PI controllers $D-PI$ and $Q-PI$ each controlling the corresponding component of the grid current. The set-point for $Q-PI$ is set to zero so that the current flowing into the grid is fully aligned with the grid voltage vector. Thus, the grid current becomes in phase with the grid voltage. $DF1$, $DF2$, $DF3$ are the disturbance feedforward paths which cancel the measurable output disturbances shown on the D-Q model (see fig. 2.24) $I_Q wL$, $I_D wL$ and $Grid$ respectively. The grid current components I_Q and I_D are produced by applying the D-Q transformation to the measured grid current. The magnitude of the disturbance feedforward DF3 is equal to the grid voltage vector magnitude which is supplied by the PLL.

A step in the grid current set-point from 1A to 2A is applied at $t = 0.785$. The result of the simulation is shown in fig. 3.23. Here, we note that the "'Grid Current"' and "'D Component of the Grid Current"' is scaled by 50 for the sake of clarity.

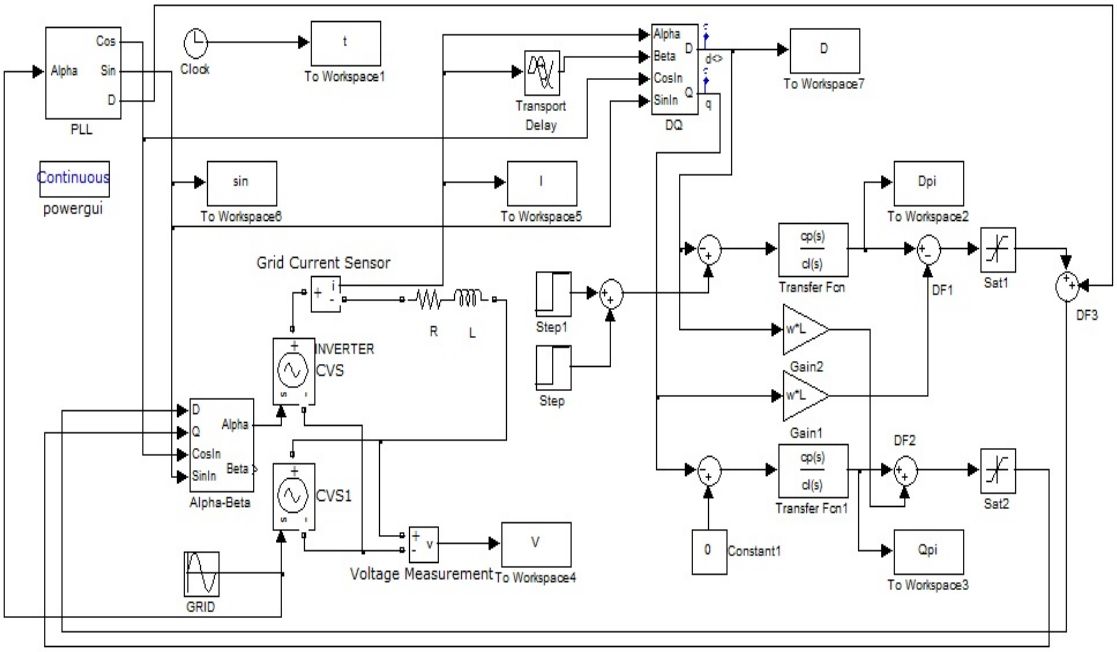

Figure 3.22 Simulation Setup for the D-Q Control Block.

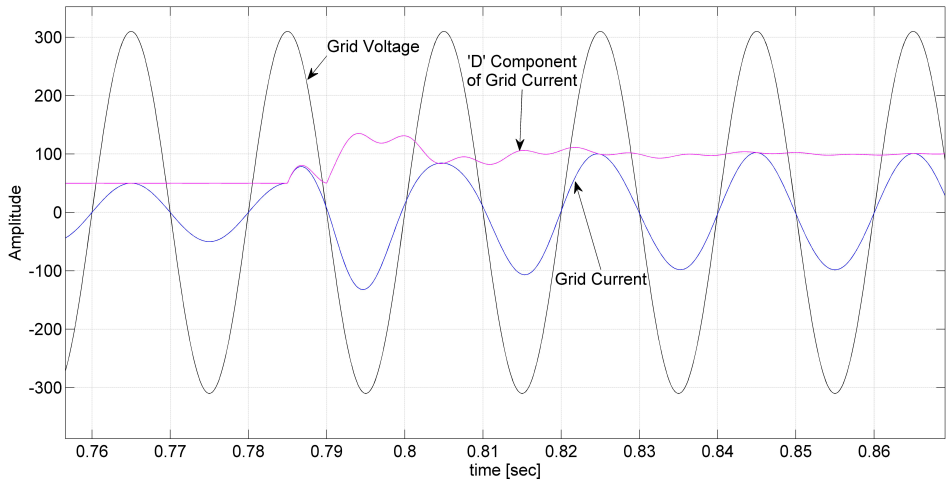

Figure 3.23 Response of the D-Q Control Block to a Step Change in the Current Setpoint.

The simulation results show that the D-Q control block with the designed controllers can stabilize the grid current. It can also be observed in fig. 3.23 that the grid current is in phase with the grid voltage as required.

The designed controller in 3.44 is discretized in MATLAB for digital implementation. The obtained discrete time controller $C_z(z)$ is

$$C_z(z) = \frac{\overbrace{2.4}^{a} z - \overbrace{2.385}^{b}}{z-1}\ ,\ T_s = 25 \cdot 10^{-6} \tag{3.45}$$

The control algorithm for $C_z(z)$ using 3.45 is;

$$\frac{Y(z)}{E(z)} = \frac{az-b}{z-1} \tag{3.46}$$

$$Y(z)(z-1) = (az-b)E(z) \tag{3.47}$$

$$Y(z)(1-z^{-1}) = (a-bz^{-1})E(z) \tag{3.48}$$

$$Y_k = aE_k - bE_{k-1} + Y_{k-1}. \tag{3.49}$$

The control algorithm in (3.49) will be used for both D-PI and Q-PI controllers in implementation.

3.5 HARDWARE DESIGN

The hardware design is divided into two distinct parts; Power section and control section. The power section consists of all the power related components such as the power switching circuit, Z-Network and the system power supply. The control section consists of the sensor buffers, PWM-Gate drivers and auxiliary circuits for debugging purposes. The following subsections present the explanations of the power and control sections with related schematics. A full schematic and the printed circuit board (PCB) layout of the system can be found in the appendix.

3.5.1 Power Section

The power section is further divided into three parts for clarity; PV input filtering and the Z-Network, the power switching circuit and the system power supply. Each part is presented in the following subsections.

PV Input Filtering and the Z-Network

PV input filtering consists of the optional filter inductor which is connected to the circuit through $CN4$ and the capacitors $C6$, $C7$, $C8$ as shown in fig. 3.24. Since the input current of the Z-Source is discontinuous, it may be required to have continuous input current to the system for maximum power exploration purpose. The capacitors $C6$, $C7$, $C8$ also provide energy storage with low impedance characteristics which is important for high frequency switching. Without using filter capacitors at the input, inductances of the input cables may cause too much voltage drop at the input of the system. An optional filter inductor is not used in this study because the discontinuous input current is not an issue for the power source from which the system is energized.

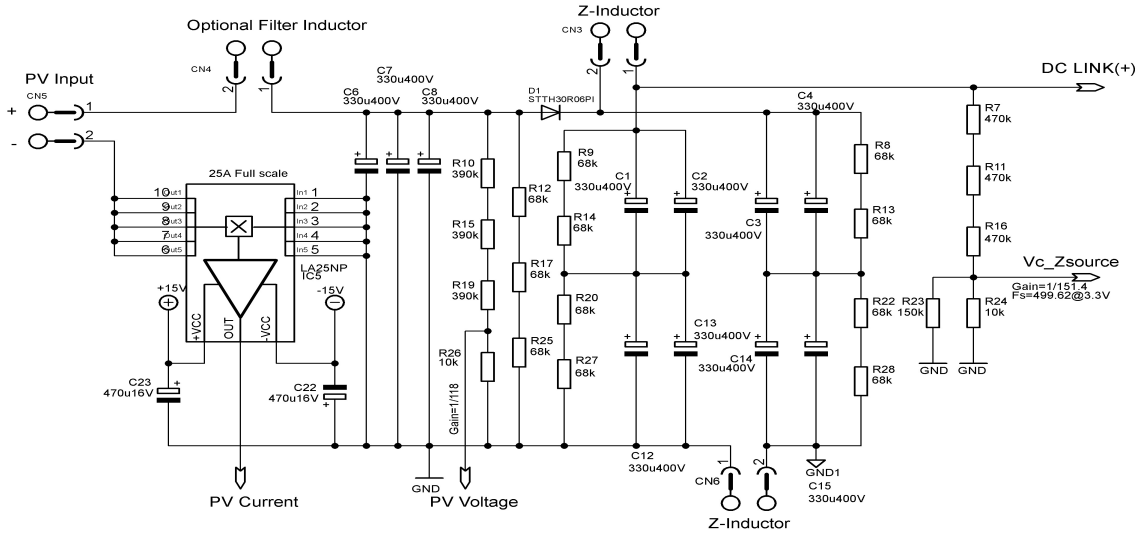

Figure 3.24 DC Input Filter and the Z-Network.

The Z-Network consists of $C1, C2, C3, C4, C12, C13, C14, C15$, $D1$ and $CN3, CN6$ for inductor connections. Non of the inductors are the integral part of the PCB, they are connected to the PCB using screw type connectors. Four capacitors are connected in series-parallel connection to form the calculated 330νF value for the Z-source. The purpose of this connection is to increase the voltage withstanding capability of the capacitors. Each capacitor is connected in parallel with resistors for proper voltage sharing. D1 is selected to withstand the required blocking voltage, allow average input current flow with low loss and provide fast switching characteristics. The selected diode also provides an insulated base for heat sink mounting. PV voltage is measured using a voltage divider formed by $R10, R15, R19, R26$. The gain of the divider is set to $\frac{1}{118}$ which allows a full scale

range of 389.4V to be measured by the controller with $3.3V$ analog to digital (A/D) reference voltage. Z-source capacitor voltage is measured in a similar way. $R7, R11, R16, R23, R24$ form the voltage divider. The gain of the divider for the Z-source capacitor voltage measurement is set to $\frac{1}{151.4}$ which provides 499.62V full scale measurement range.

The Power Switching Circuit

The power switching circuit consists of four Insulated Gate Bipolar Transistors (IGBT) connected in full-bridge configuration. Each IGBT is equipped with a turn-off snubber to mitigate the turn-off losses. The selected IGBTs feature high switching speed, low saturation voltage and 600V collector to emitter break down voltage. The grid current is measured using a closed loop hall effect current sensor $IC1$. The sensor provides galvanic isolation between inputs and outputs and features a high bandwidth from DC to 150kHz. The output of the sensor is a bidirectional current signal which is proportional to the measured current. The sensor can measure up to $\mp 12A$ with the connection configuration shown in fig. 3.25.

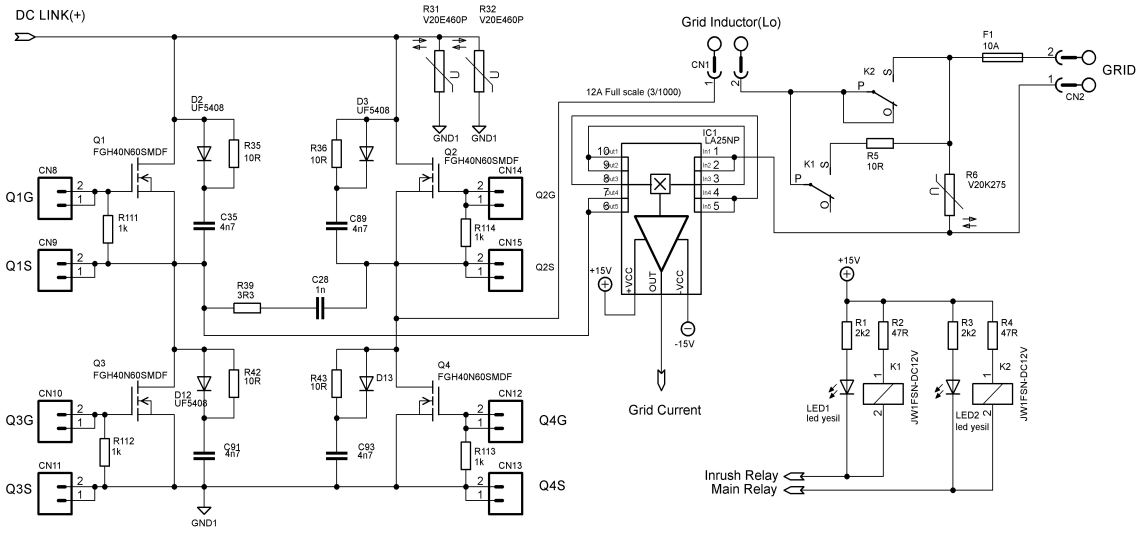

Figure 3.25 The Power Circuit.

Relays $K1, K2$ and resistor $R5$ are used to control the connection of the power module to the grid. The varistors $R6, R31, R32$ provide over-voltage protection for the grid connection and DC link respectively.

System Power Supply

The required power for all the control tasks of the system is supplied by the circuit in fig. 3.26. The circuit consists of a line frequency step down transformer and linear regulators to supply the required voltages. The power supply provides $\pm 15V$ for analog circuits and $5V$ for digital circuits.

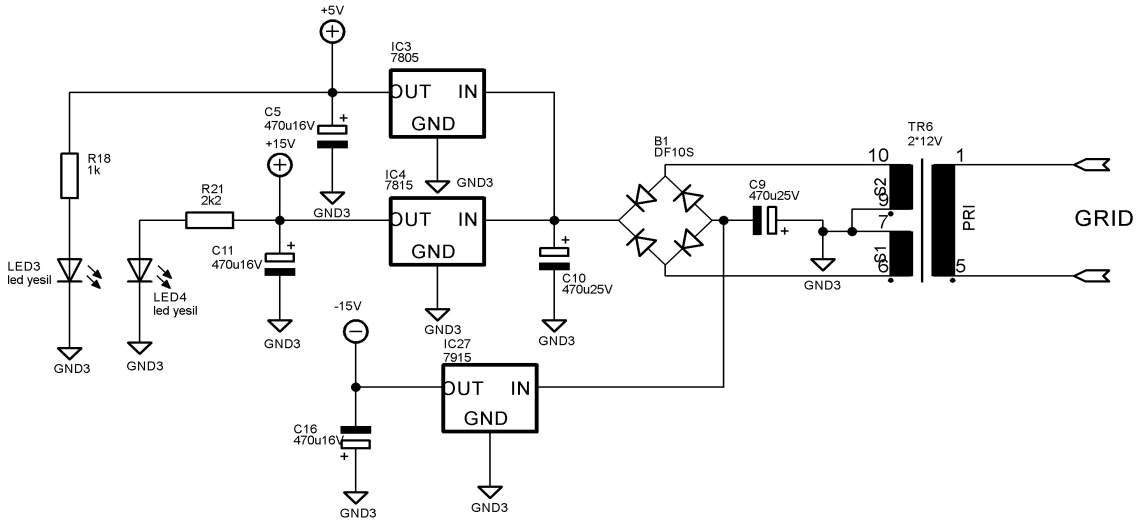

Figure 3.26 System Power Supply.

3.5.2 Control Section

The control section of the system is composed of the gate drivers, grid voltage sensor, buffers and the control circuitry. Each part is presented in the following subsections.

Gate Drivers

Because of the floating nature of the DC link and the selected reference ground of the control circuit, driving the gates of the IGBTs becomes an issue. Fig. 3.27 shows the driver circuitry for one leg. The circuit for the other leg is a similar circuit with the same function. The main issue with the connection to the IGBT's is the problem of different reference points. The control circuitry is referenced to the PV input ground connection and the reference points for the IGBT's are their emitters. At least one power source isolated from the control reference point is needed to supply the driving circuits. In this study, a separate power supply

for each driver is provided. Each leg of the full bridge has a high frequency transformer with two secondaries to supply the driving circuits.

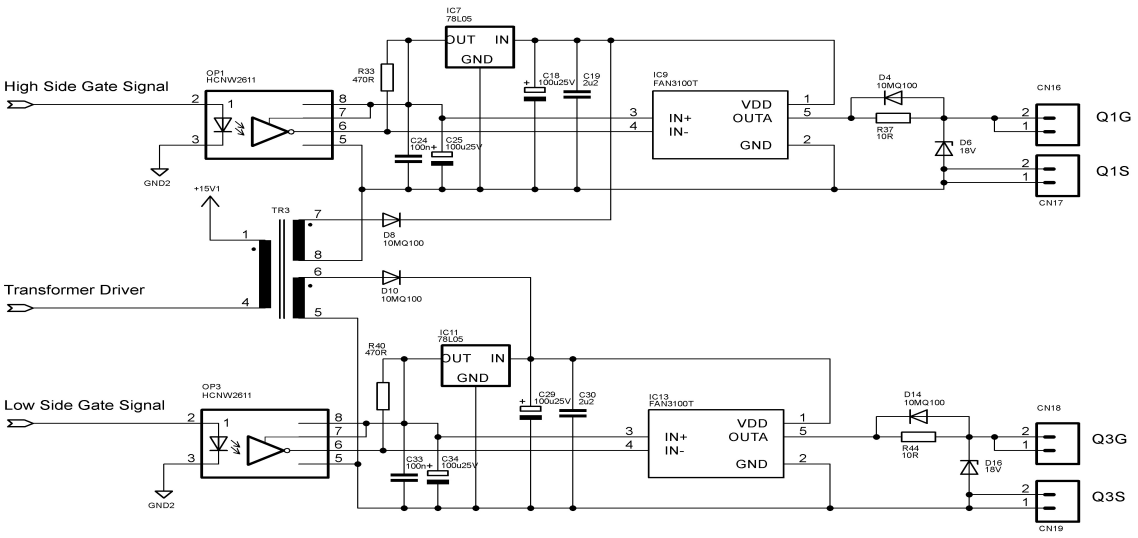

Figure 3.27 The Gate Drivers.

The switching frequency of the gate driver supply transformer is 40kHz. The transformers are driven by a fixed duty cycle of %45 and provide power to the gate drivers continuously. The required PWM signals for the gate drivers are isolated using opto couplers $OP1, OP2, OP3, OP4$. The selected opto coupler features low pulse width distortion and high common mode rejection ratio (CMRR).

Grid Voltage Sensor

The grid voltage sensor shown in fig. 3.28 is one of the most important parts of the system. The instantaneous value and the phase of the grid voltage are measured using this circuitry. The main requirements for this sensor are very low phase shift, low offset voltage and galvanic isolation from the grid. Galvanic isolation is provided by a low distortion line frequency step down voltage reference transformer.

The output of the transformer is scaled by $R110$ and shifted up by $1.65V$ by the opamp circuits to provide a single ended (0-3.3V) signal to the A/D inputs of the controller. The opamp's in the circuit feature very low offset voltage, low input bias current and high speed operation. The output of the sensor circuit is low impedance to allow proper operation of the A/D converter.

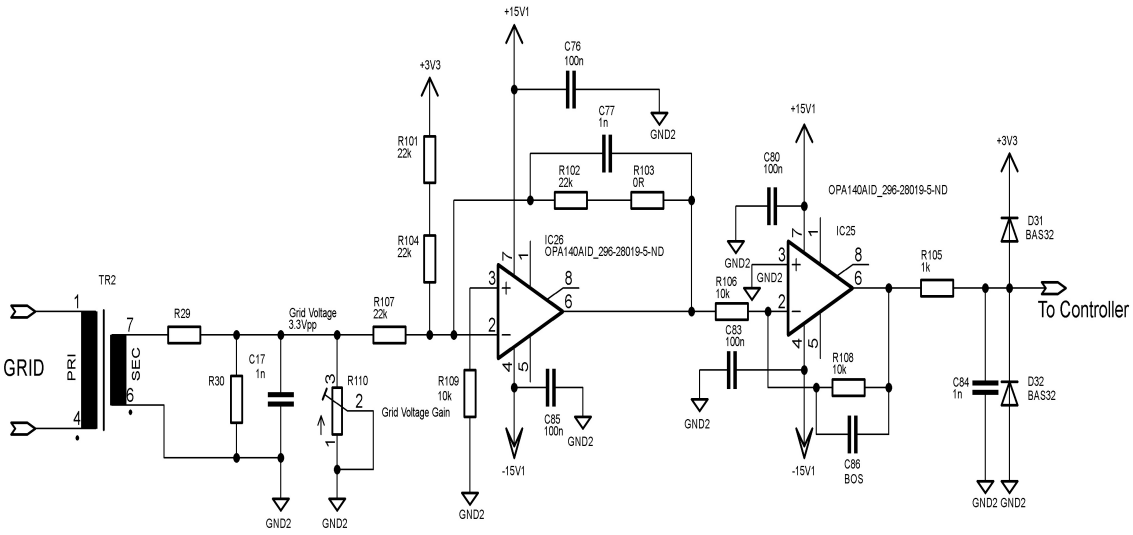

Figure 3.28 Grid Voltage Sensor.

Grid Current Buffer

The grid current buffer shown in fig. 3.29 is a similar circuit to the grid voltage sensor. The only difference is that the input of the buffer is connected to the current sensor.

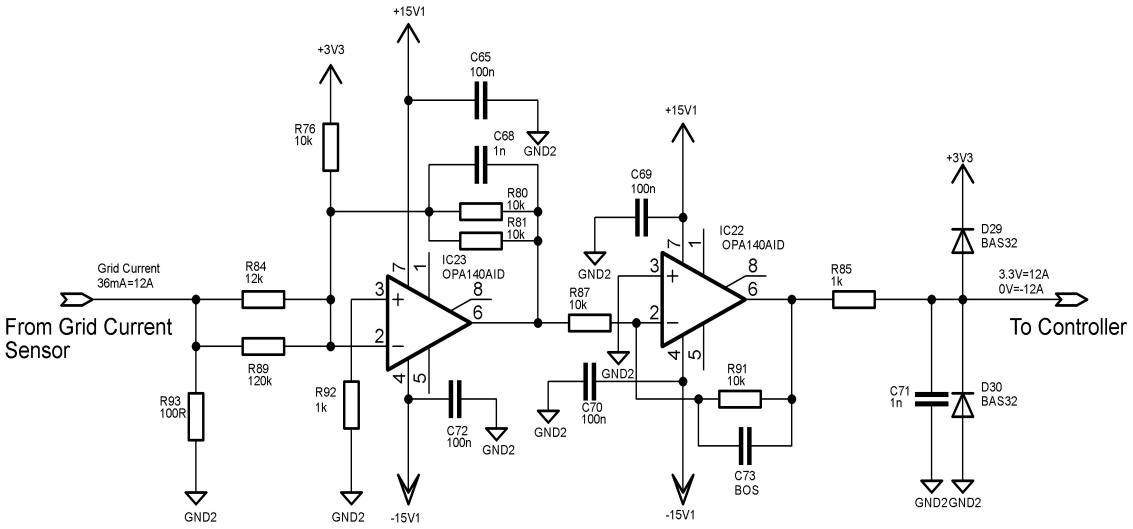

Figure 3.29 Grid Current Buffer.

The current produced by the current sensor is converted to a voltage over $R93$, scaled and shifted up to produce an output voltage of 0-3.3V which represents -12A for 0V and 12A for 3.3V.

Z-Source Capacitor and PV Voltage Buffers

The buffers for Z-source capacitor and PV voltage are non-inverting unity gain amplifiers which provide impedance adjustment for the proper operation of the A/D converter of the control circuitry. One of the buffers used for Z-source capacitor voltage measurement is shown in fig. 3.30.

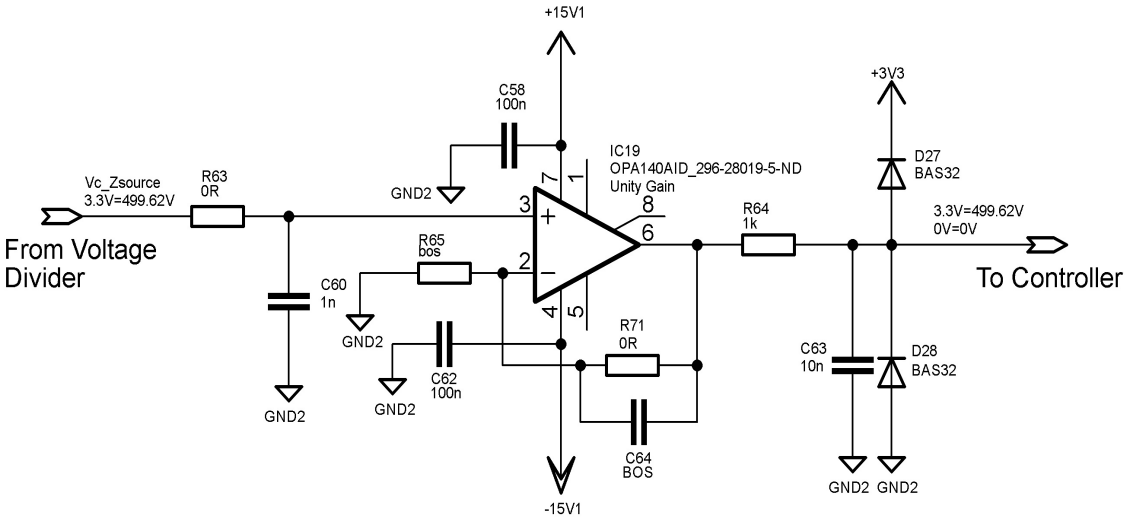

Figure 3.30 Z-Source Capacitor Voltage Buffer.

Control Circuit

The core of the control circuit is the 16 bit microcontroller $IC21$ which is specifically designed for power conversion applications. The microcontroller is selected for the control of the grid tie inverter for its following features;

- 50 Mega Instructions Per Second (MIPS) execution speed
- High speed PWM Module, 1.04ns PWM resolution
- 2 Msps 10 bit A/D Converter
- 40bits Accumulators and DSP instructions (MAC/MPY)
- Single cycle mixed sign Multiplication
- 32bit/16bit Hardware Divide
- 5V Tolerant I/O's

$IC21$ operates from 3.3V supply which is provided by the low dropout linear regulator $IC16$. The interface between the PWM outputs of the microcontroller and the gate drive opto couplers is provided by the non-inverting open drain buffer IC $IC20$. The digital to analog converter (DAC) IC $IC24$ is used to view the data inside the microcontroller for debugging purpose and it has no control function in the operation of the circuit.

The combination of the full bridge and the Z-source control signals (see section 2.4.4) is performed in the "OR" circuit formed by $D33, D34, D35, D36$. The microcontroller produces PWM signals for each leg of the full bridge and Z-source separately. PWM3H and PWM3L outputs of $IC21$ are used to control the High and Low side switches of the bridge leg "'B"' and similarly PWM2H and PWM2L outputs control the bridge leg "'A"'. The inverted PWM control signal for the Z-source is activated on PWM1H or PWM1L outputs depending on the grid alternance and then logically "OR"'ed to the high side control signals. Using "OR" structure, high speed and high precision control signals are obtained without the software overhead. The combination of the PWM signals and the designed control circuit are shown in fig. 3.31 and fig. 3.32 respectively.

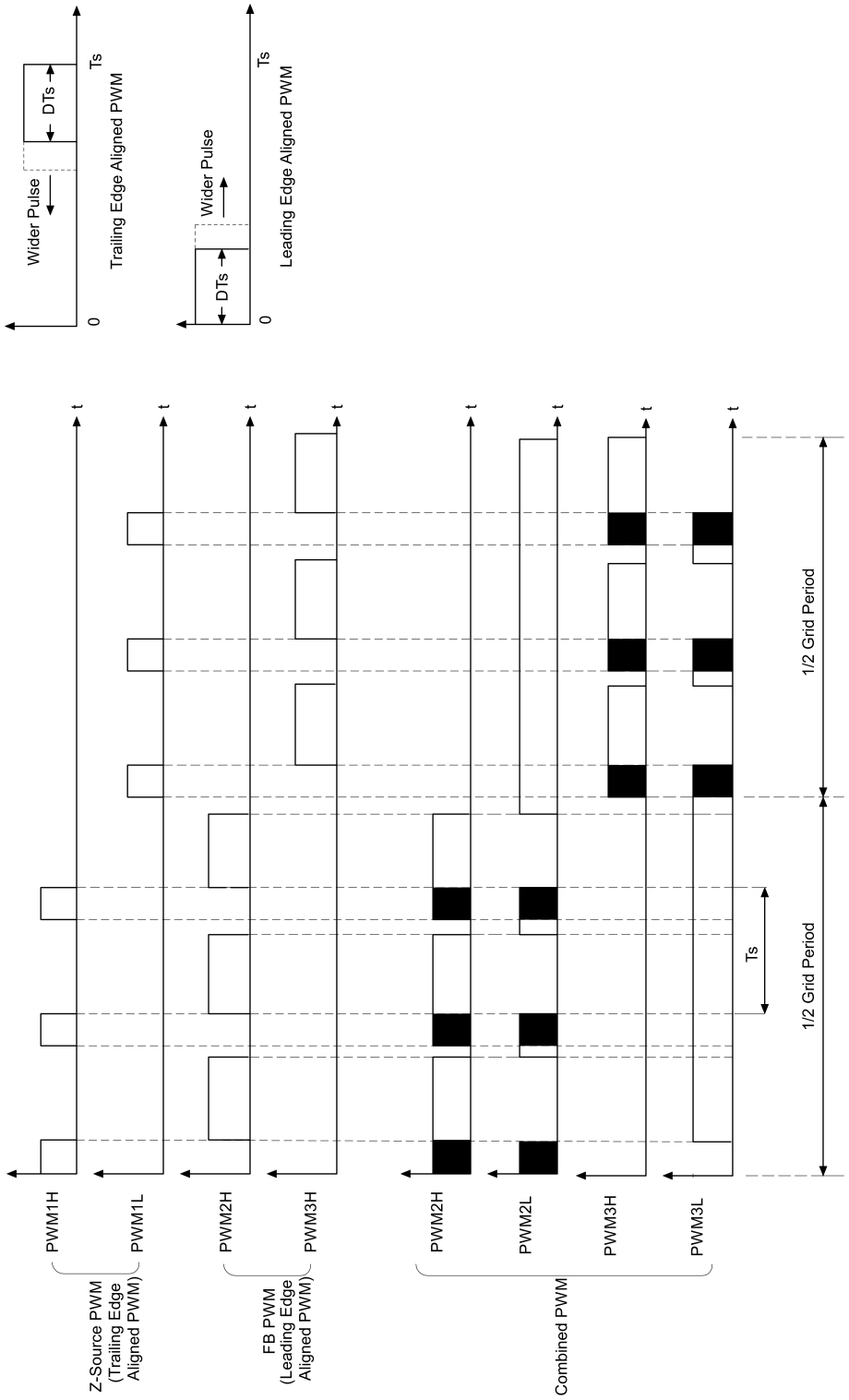

Figure 3.31 Combination of the PWM Signals for Full Bridge and the Z-Source.

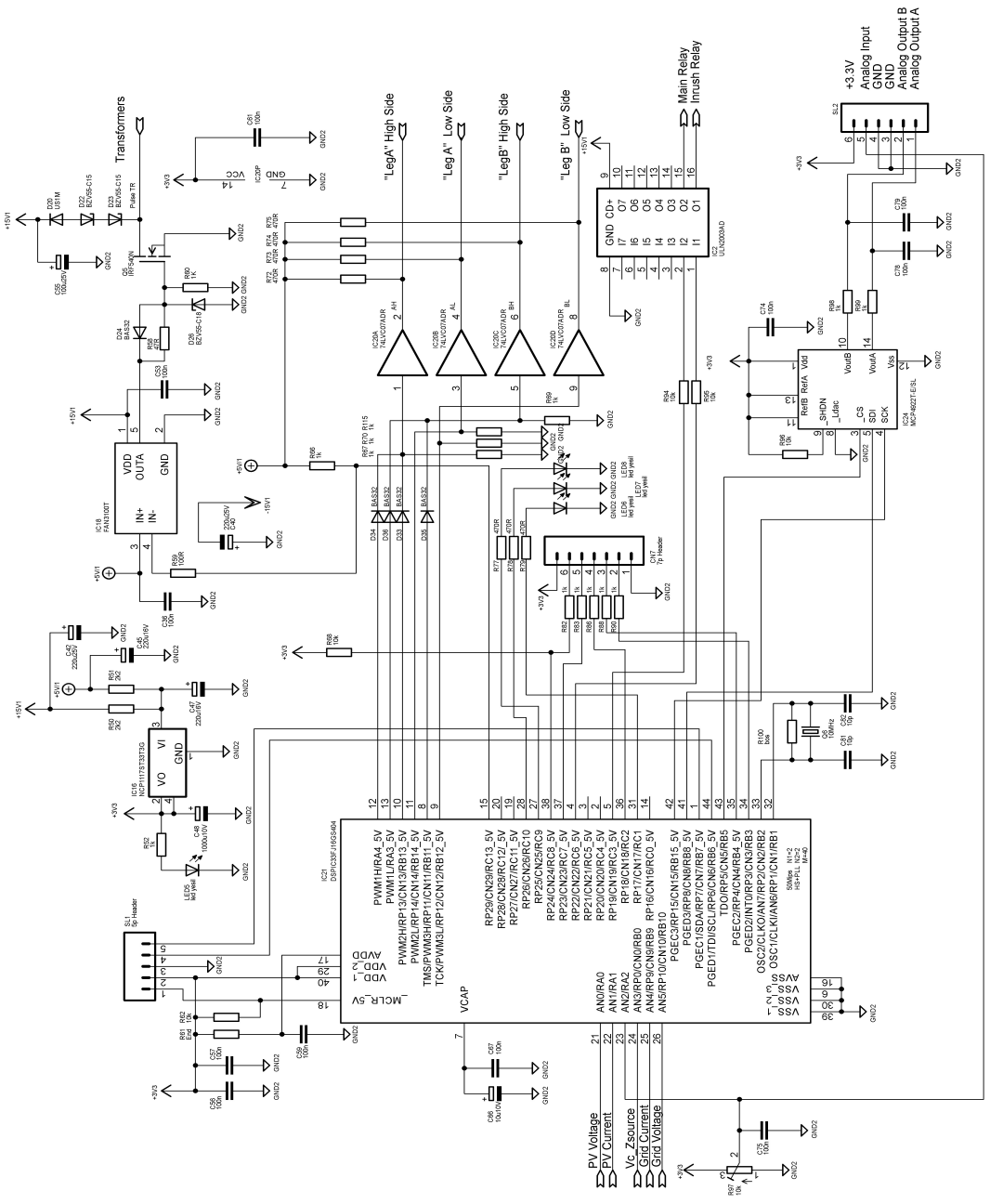

Figure 3.32 Control Circuit and PWM Drivers.

3.6 SOFTWARE DESIGN

The control software of the GTI is based on an interrupt driven execution of a series of instructions. All the control software is embedded into an interrupt service routine that runs once every $25\mu s$. The interrupt that starts the code execution is generated by the time base of the PWM module. The sampling instances of the A/D converter are also synchronised to the PWM module. The timing of the system is summarized in fig. 3.33.

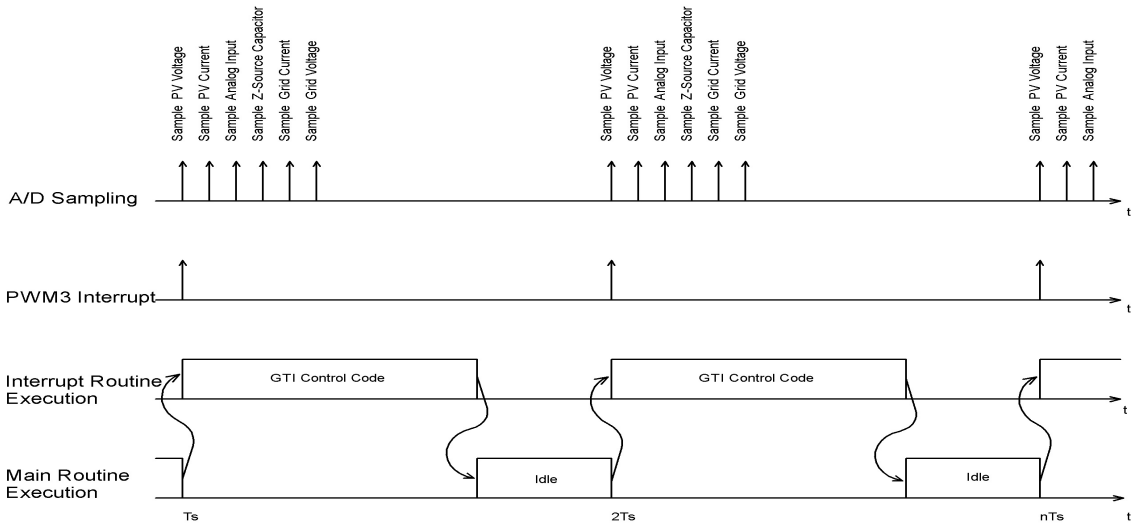

Figure 3.33 Timing of the System.

The A/D conversion process automatically advances once triggered. The A/D module samples and converts the analog inputs sequentially and places the results into the dedicated buffers. A PWM3 interrupt triggers the A/D module and at the same time the program execution branches to the interrupt service routine. The main routine does not include any control related software except for the initialization code that runs only once at start up. The program flow is shown in fig. 3.34.

The software of the GTI is coded in assembler to optimize the execution time. The measured run time of the PWM3 interrupt routine in simulator is $13.1\mu s$ which means that the microcontroller code execution load is roughly at the half and remaining time can be used to improve the system.

Figure 3.34 Software Algorithm.

3.7 CHAPTER SUMMARY

In this chapter, the complete design procedure of the GTI is presented. The critical component values are determined according to the design specifications and the required voltage-current relationships are calculated using the derivations in the previous chapter. The required transfer functions are calculated using the designed component values and controllers are designed. The designed circuit is then simulated in MATLAB to verify the component waveforms, voltage-current relationships and closed-loop responses. The consistency between the simulations and derivations is shown. The hardware and software designs are also presented. The blocks of the hardware are explained using the schematic diagrams of each relevant block in detail.

CHAPTER IV

EXPERIMENTAL RESULTS

4.1 INTRODUCTION

In this chapter, the results of the experiments with the designed prototype are presented. The experiments are grouped into three sections as the PLL, the Z-source converter and lastly all the sections of the GTI are tested as a whole. The measurements are recorded using a digital oscilloscope and the screen-shots are downloaded to the computer as pictures. The oscilloscope is galvanically isolated from the grid to prevent ground fault currents and direct measurements are carried out using high voltage, differential voltage and DC current probes where possible. A small software is added to the control code of the GTI to output software produced signals at the analog output ports of the prototype. The scaling factors for these signals are depicted at the explanation parts of each test. A schematic representation of the prepared hardware setup for the tests are also provided in each subsection . The digital to analog (D/A) converter used in the control board is a $12bits$ unipolar output two channels device which can not output bipolar signals. For unipolar signals, the digital data produced in the software is sent to the D/A converter after proper scaling to fit into 12bits. In the bipolar signal case, the digital data is shifted up by half the full range (added 2048) after proper scaling so that 1.65V is output for the representation of zero. By this way, it becomes possible to observe the digital data with negative sign. The channel of the oscilloscope (OSC) is given 1.65 offset so that the OSC channel marker is aligned with zero when the digital data is zero.

4.2 EXPERIMENTAL RESULTS FOR THE PHASE LOCKED LOOP

A test setup is prepared and the prototype of the GTI is connected to a signal generator (SG) and oscilloscope (OSC) as shown in fig. 4.1. The resistor $R29$ on the control board is removed to disable the voltage reference transformer $TR2$ and the SG is connected across $R110$ (see fig. 3.28). The amplitude of the SG at the connection point is adjusted to 2 Vpp at 50Hz. which is equal to the voltage level of the voltage reference transformer when the grid voltage is 220Vp.

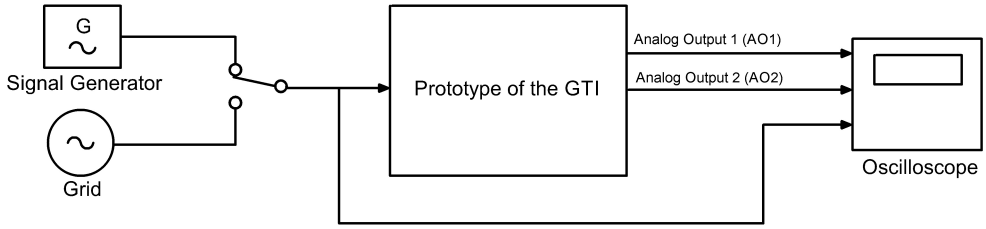

Figure 4.1 Test Setup for the PLL.

The Channel 1 (CH1)(Blue) of the OSC is connected to the analog output A (AOA) of the control board at which the $Sin\theta$ produced by the PLL is streamed out and CH2 (Red) of the OSC is connected to the SG output. The captured waveform is shown in fig. 4.2.

The waveform captured with the test setup is exactly the expected signal. The PLL locks to the input signal with very low phase shift and it is stable throughout the observations. To test the consistency between the real implementation and the simulation of the PI controller, a disturbance of -90 deg phase shift is applied to the input signal. The control software is modified so that the output of the PI controller Y_k is present at the AOA. The digital data for Y_k is scaled by 8 and shifted up by half the output range for better view before sending to the D/A converter as explained in Section 4.1. The channel gain of the OSC becomes $31 rad/div$ for $200 mV/div$ original setting.

Fig. 4.3 shows the PI output response to a jump of $-90 deg$ phase shift. A comparison with the simulation result in fig. 3.18 shows that the simulated and experimented results are in very good agreement. This verifies the correctness of the implementation. Fig. 4.4 shows a more detailed view of the response.

The output of the VCO is a continuously increasing signal since it is the inte-

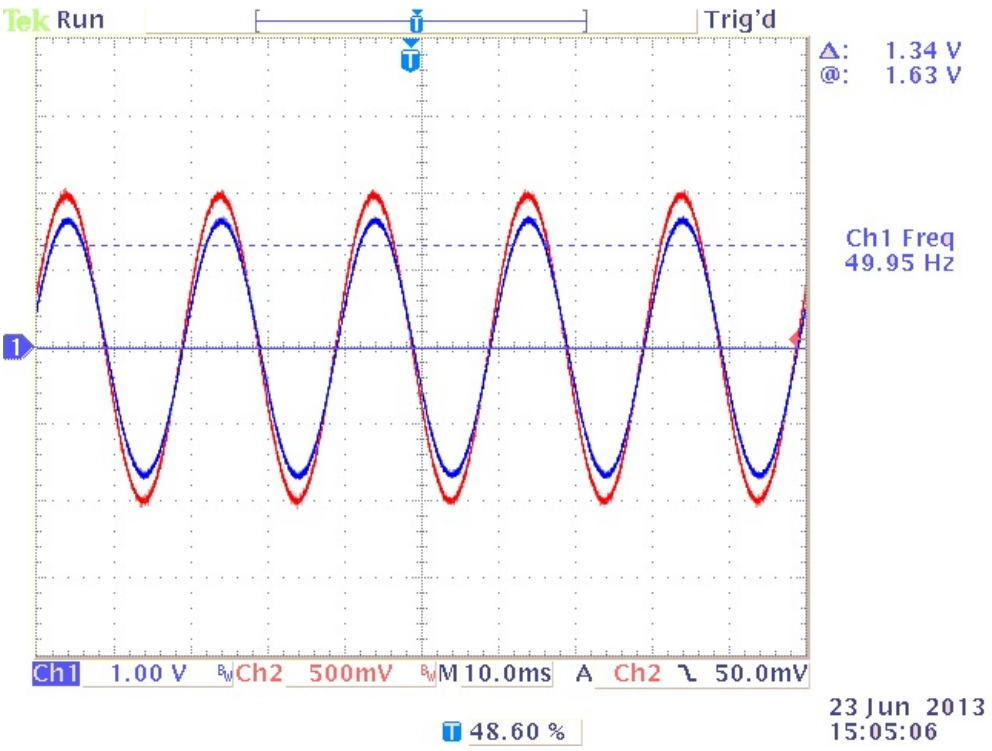

Figure 4.2 PLL Locked Steady State Waveform.

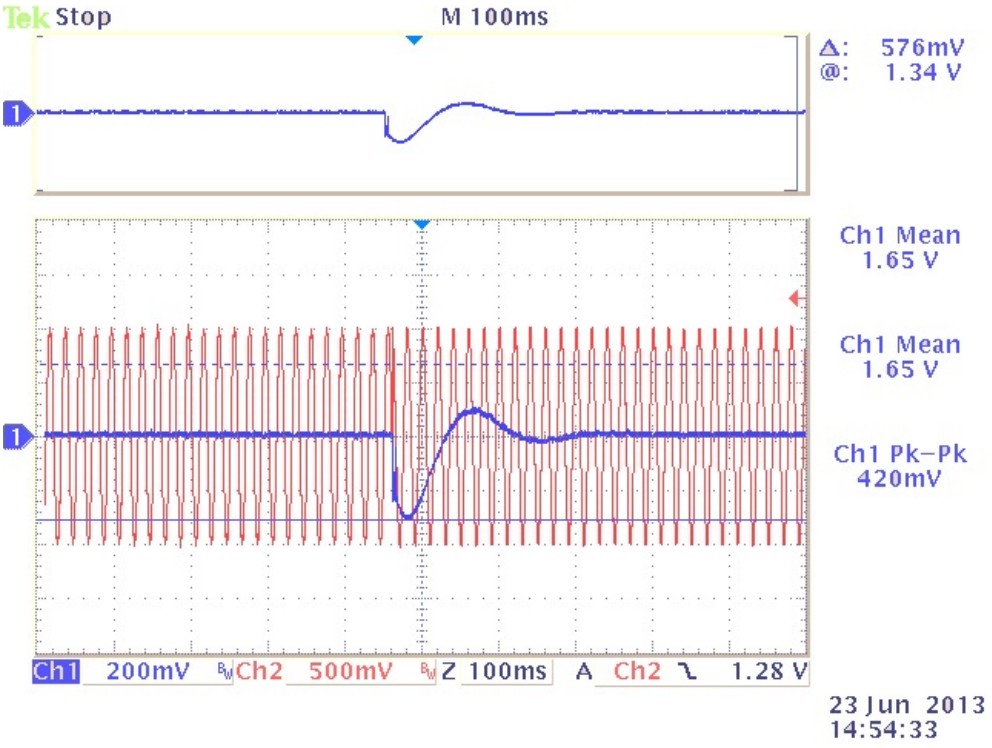

Figure 4.3 PLL-PI Controller Response to a -90 deg Phase Jump.

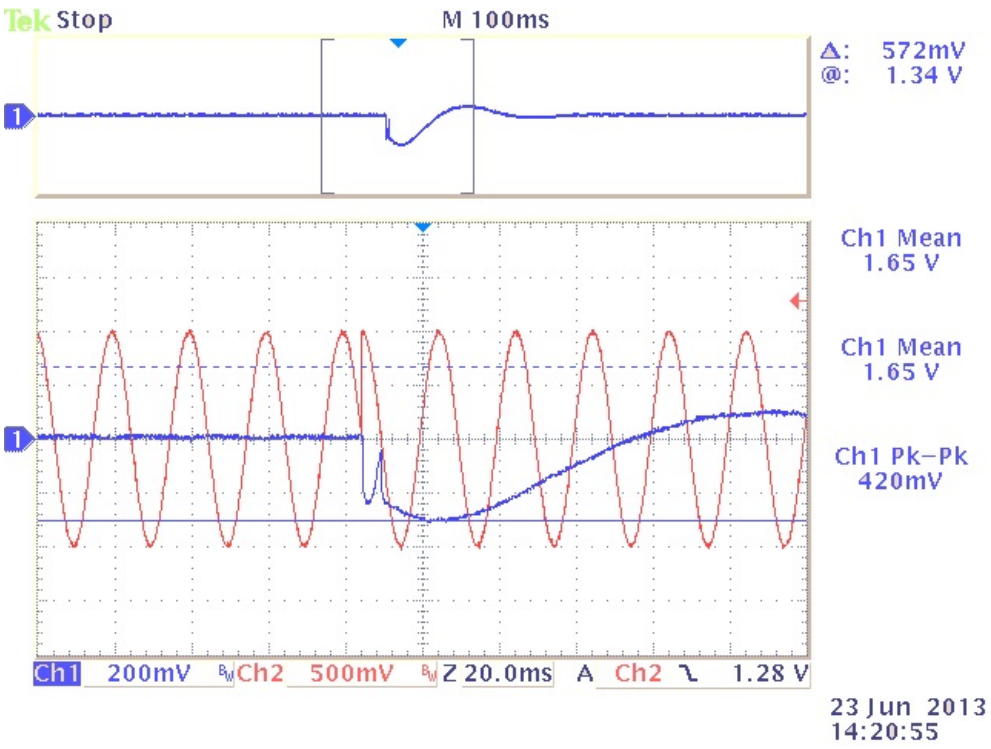

Figure 4.4 PLL-PI Controller Response to a −90 deg Phase Jump (Detailed View).

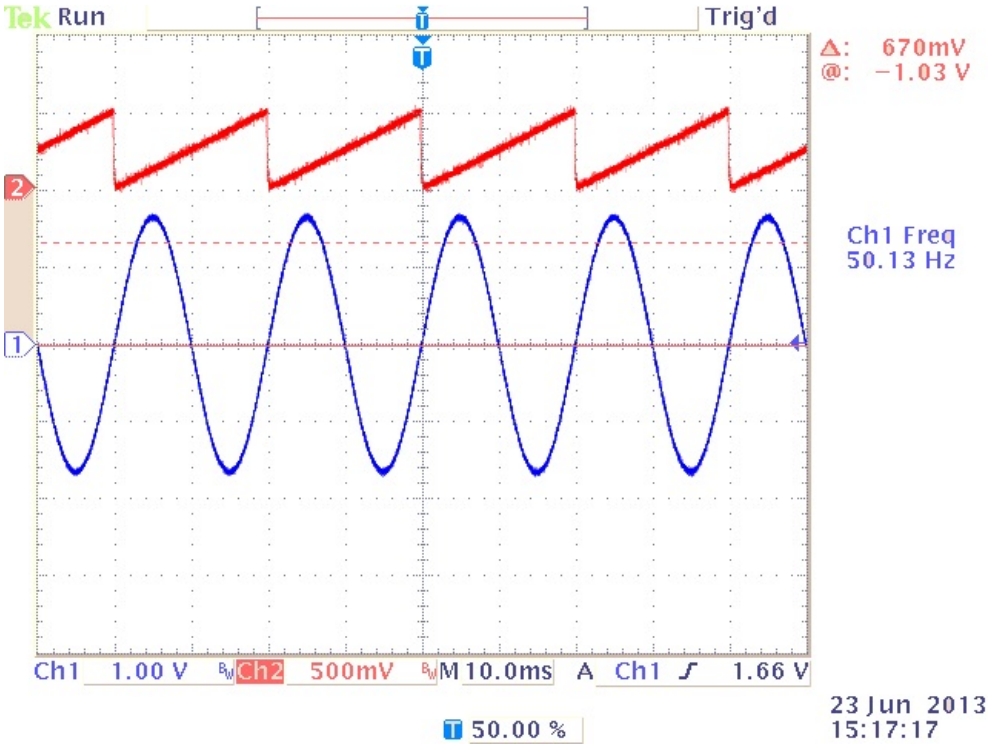

Figure 4.5 PLL VCO Output and Corresponding Sine Wave.

grated value of the controller output plus the feedforward term. The signal to be produced using the VCO output is periodic and its range is $\{0 : 2\pi\}$. Therefore a modulo operation is performed on the output of the VCO in the software. The VCO output and the corresponding sine wave produced using the VCO output is shown in fig. 4.5.

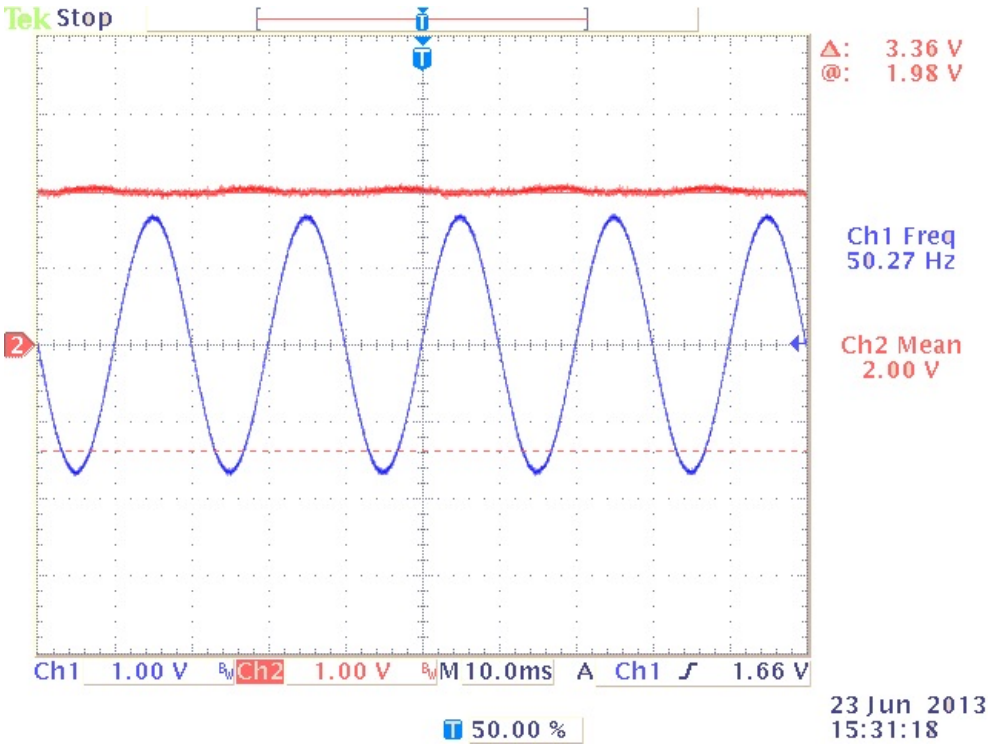

Figure 4.6 PLL D Output vs. Input Signal.

One of the outputs from the PLL which is required for the proper operation of the D-Q block is the magnitude of the grid voltage vector. This signal is used as a feedforward term and is very important for the closed-loop performance of the D-Q block. The grid voltage vector magnitude signal produced by the PLL is shown in fig. 4.6. CH1 (Blue) shows the sine wave of the VCO and CH2 (Red) shows the D output of the PLL in response to an input signal of 2Vpp 50Hz. The gain of CH2 corresponds to 155V/div. with the scaling used for the analog output.

Fig. 4.7 shows the sine wave output of the VCO (CH2 "Red") for the real grid condition. In this case the grid is highly distorted but the operation of the PLL is still satisfactory.

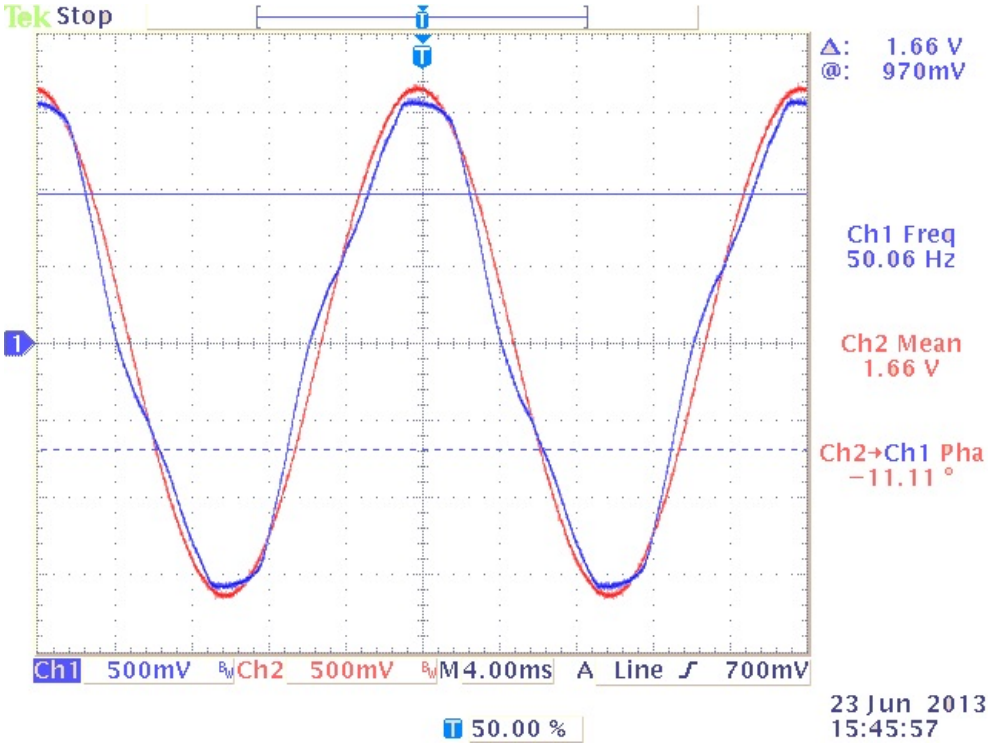

Figure 4.7 PLL Sinewave Output vs. Distorted Grid.

4.3 EXPERIMENTAL RESULTS FOR THE Z-SOURCE CONVERTER

The Z-Source converter with the designed component values is tested to verify the derivations and the simulations. The setup and the measurements points are shown in fig. 4.8. An output resistance R_O close to the designed value of 117.2Ω for maximum output power $P_{o_{max}}$ is connected and the set-point of the Z-source capacitor voltage is set to a value so that the output power is very close to $P_{o_{max}}$ (1kW.)

The captured waveform of the inductor current I_L, capacitor voltage V_C and the DC-Link voltage (V_O) is shown in fig. 4.9 and output current I_O, voltage across the output resistor V_{RO} in fig. 4.10. The results of the simulations and experiments are listed in table 4.1 for the ease of comparison.

Param.	**Value (Sim.)**	**Ref.**	**Value(Exp.)**	**Ref.**
V_I	$245V$	Set as	$245V$	Measured
d_s	22.13%	Set as	21.44%	fig. 4.9
I_L	$4.091A$	fig. 3.2	$4.33A$	fig. 4.9
ΔI_L	$0.541A$	fig. 3.2	$0.56A$	fig. 4.9
I_I	$4.091A$	fig. 3.4	$4.33A$	Measured
V_C	$342.26V$	fig. 3.6	$335V$	fig. 4.9
ΔV_C	$68.2mV$	fig. 3.6	[1]	—
I_{LO}	$2.92A$	fig. 3.7	$2.928A$	fig. 4.10
ΔI_{LO}	$0.536A$	fig. 3.7	$0.47A$	fig. 4.10
V_O	$342.3V$	fig. 3.8	$335V$	fig. 4.10
$V_{O_{peak}}$	$439.6V$	fig. 3.8	$426V$	fig. 4.10
P_{in}	$1002.3W$	Calculation	$1060.85W$	Calculation
P_{Out}	$999.5W$	Calculation	980.88	Calculation
η	99.72%	Calculation	92.46%	Calculation

Table 4.1 Comparison of the Simulated and Measured Values of the Z-Source.

As can be noticed in table 4.1, there are slight deviations between the simulated and the measured values. The main reason is the omitted efficiency η in the simulation. The calculated efficiency for the simulation is very close to unity because all the components in the simulation are lossless except the small parasitic resistance of $D1$. As the second reason, the duty cycle d_s has some small contribution

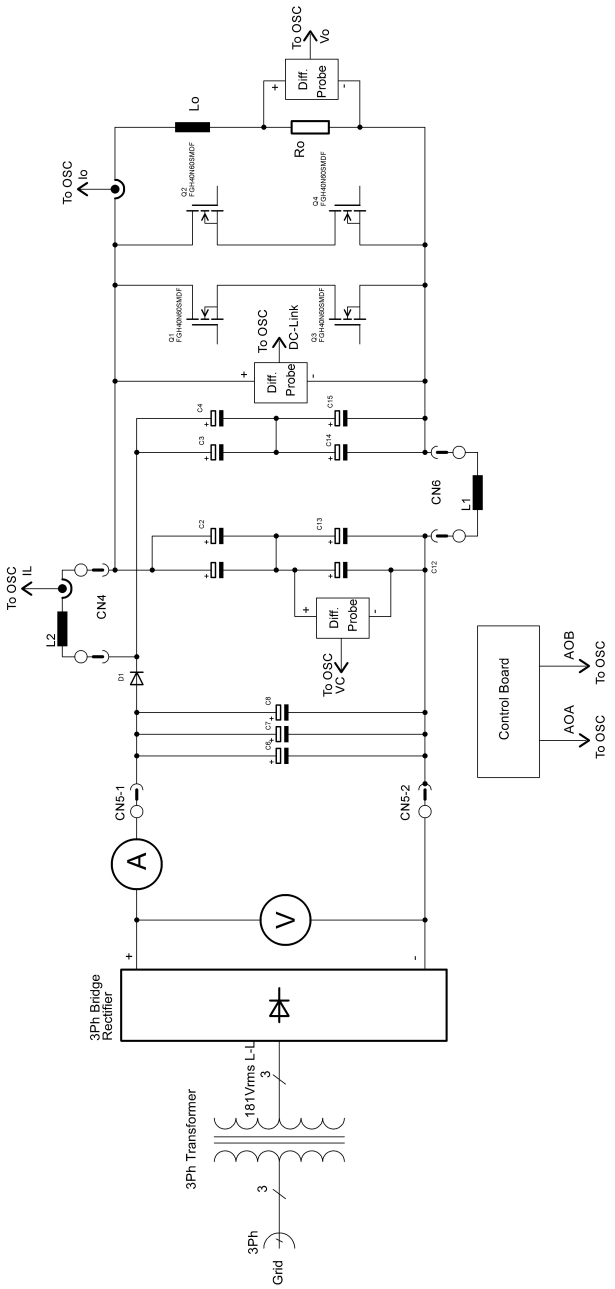

Figure 4.8 Prepared Test Setup and the Measurement Points of Z-Source Converter.

to the deviation since the output power is fine-tuned to approximately 1kW by changing the capacitor voltage V_C set-point. The experimental results and simulations agree up to a high extent and can be expected to agree better if the results are normalized by the efficiencies.

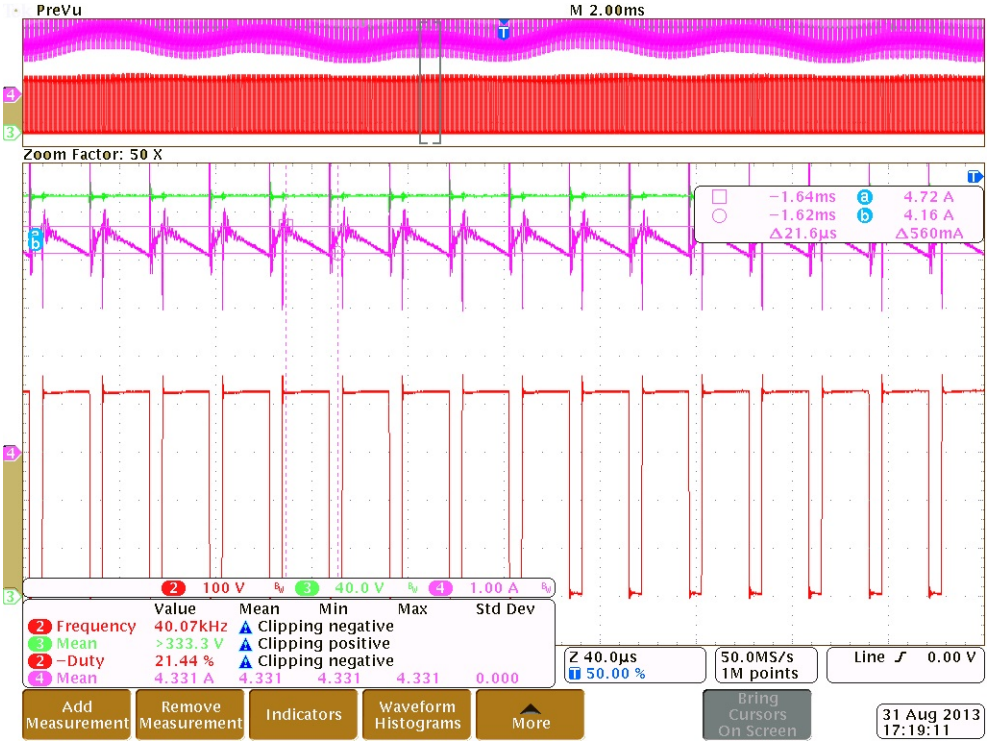

Figure 4.9 Experimental Waveforms of the ZSC. $(I_L, V_C, DC - Link)$

The traces shown in fig. 4.9 are; CH2 (Red): DC-Link Voltage V_O, CH3 (Green): Capacitor voltage V_C, CH4 (Purple): Inductance current I_L.

The traces shown in fig. 4.10 are; CH2 (Red): Voltage across the output resistance V_{RO}, CH3 (Green): Capacitor voltage V_C, CH4 (Purple): Output current I_{LO}.

To test the expected performance of the designed digital PI controller and compare the experimental results with the simulations, a step change in the set-point of V_C from 290V to 334V is applied. The result is shown in fig. 4.11. The traces in the figure are: CH1 (Blue): Digital PI controller output Y_k, CH2 (Red): Output voltage V_O, CH3 (Green): Capacitor voltage V_C and CH4 (Purple): Inductor current I_L. The comparison of the captured response with the simulation shown in fig. 3.15 clearly indicates that the settling times are very close to each other and the performance of the controller is as expected. This verifies the accuracy of the implementation.

Figure 4.10 Experimental Waveforms of the ZSC. (I_O, V_{RO}, V_C)

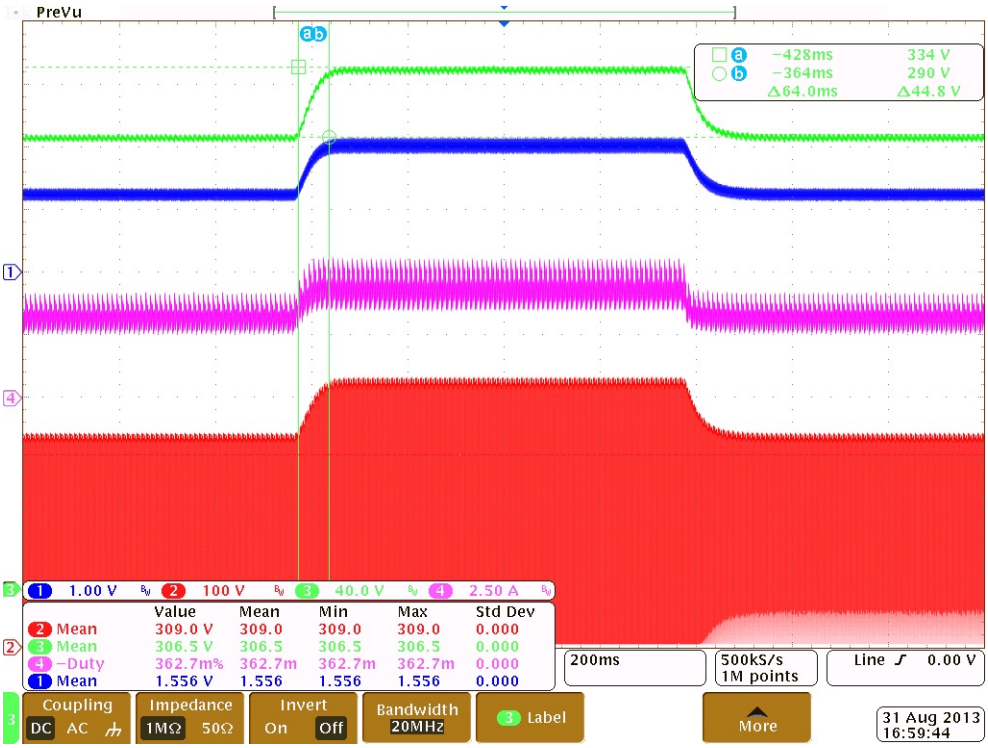

Figure 4.11 Experimental Waveforms of the ZSC. (Step Response)

Figure 4.12 Experimental Waveforms of the ZSC. (DCM Operation)

Fig. 4.12 shows the waveforms of the Z-source converter in discontinuous conduction mode (DCM) of operation. The inductors L and the output resistance R_O is modified on purpose to operate the converter in DCM. The trace CH2 (Red) shows the voltage drop at V_O when the inductor current (CH4, Purple trace) falls close to zero. This voltage drop causes a large amount of distortion in the output current of the GTI since it can not be tolerated within a switching cycle. The calculation of the duty cycle for the output grid current control is based on the voltage present at V_O. Whether it is directly measured or estimated, the voltage drop at V_O caused by DCM operation leads to the incorrect calculation of the duty cycle. Therefore the converter should never be operated in the DCM for the D-Q block to operate correctly.

4.4 EXPERIMENTAL RESULTS FOR THE GRID CONNECTION

The test setup shown in fig. 4.13 is prepared and the prototype of the GTI is connected as shown. The control software of the GTI is designed such that the grid connection sequence is as follows.

- Start Sequence: Ramp the set-point of the capacitor voltage V_C to the required voltage
- Inrush Sequence: Start the D-Q control with the grid current set-point of 0.6A, connect to the grid over 10R resistor at the zero crossing of the grid voltage and wait 0.5sec.
- Connection Sequence: Connect to the grid directly and ramp up the grid current to the required set-point.

The software of the GTI is modified to output the calculated value of the grid current D component at the analog output AOA. This signal is shown on the figures with blue color (CH1). Other traces are connected to the measurement points as: CH2 (Red): Grid voltage, CH3 (Green): Z-source capacitor voltage V_C and CH4 (Purple) Grid current.

Fig. 4.14 shows the complete sequence. The capacitor voltage V_C is ramped up to 330VDC (Start sequence) and the GTI is connected to the grid over the 10R resistor (Inrush sequence). 0.5sec later, the direct connection to the grid is performed and the grid current is ramped up to the set-point within 2.5sec. The detailed view of the inrush sequence is shown in fig. 4.15.

It can be noticed from the fig. 4.15 that the grid current at the instance of connection is higher and it slowly decreases to the set-point. This shows that the bandwidth of the PI controller designed for the D-Q controller is indeed too low. It is expected that this controller reacts to the errors in the grid current very fast. Low bandwidth of the controllers also result in the distorted grid current. The grid current distortion shows itself much more for lower output currents and is also influenced by the nonlinearities in the power and control sections.

The same characteristic of the grid current also shows itself in fig. 4.16. A small increase in the output current occurs at the instance of direct connection to the

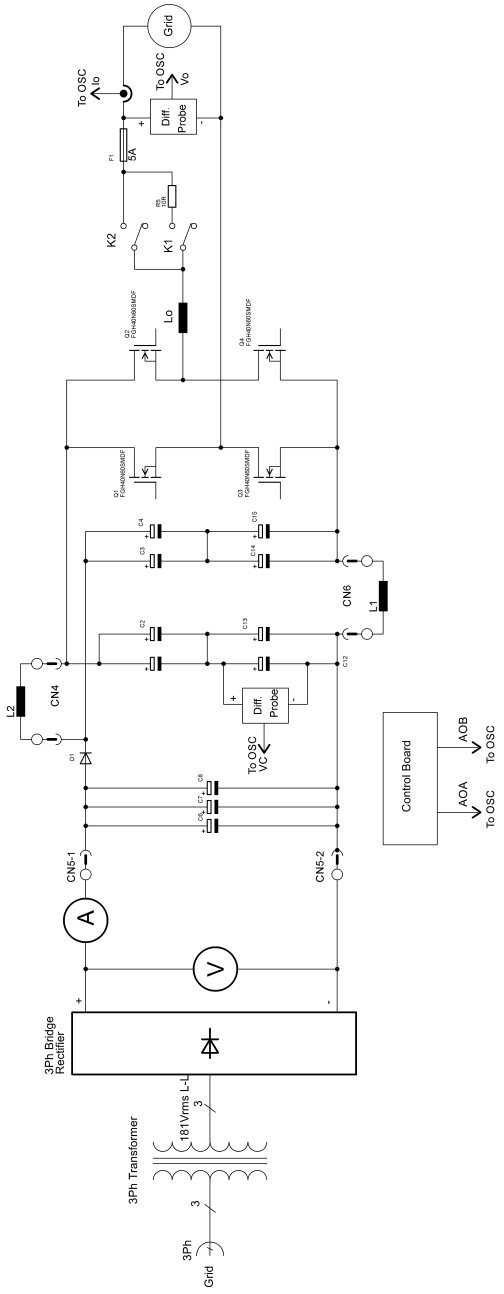

Figure 4.13 Prepared Test Setup and the Measurement Points of the GTI.

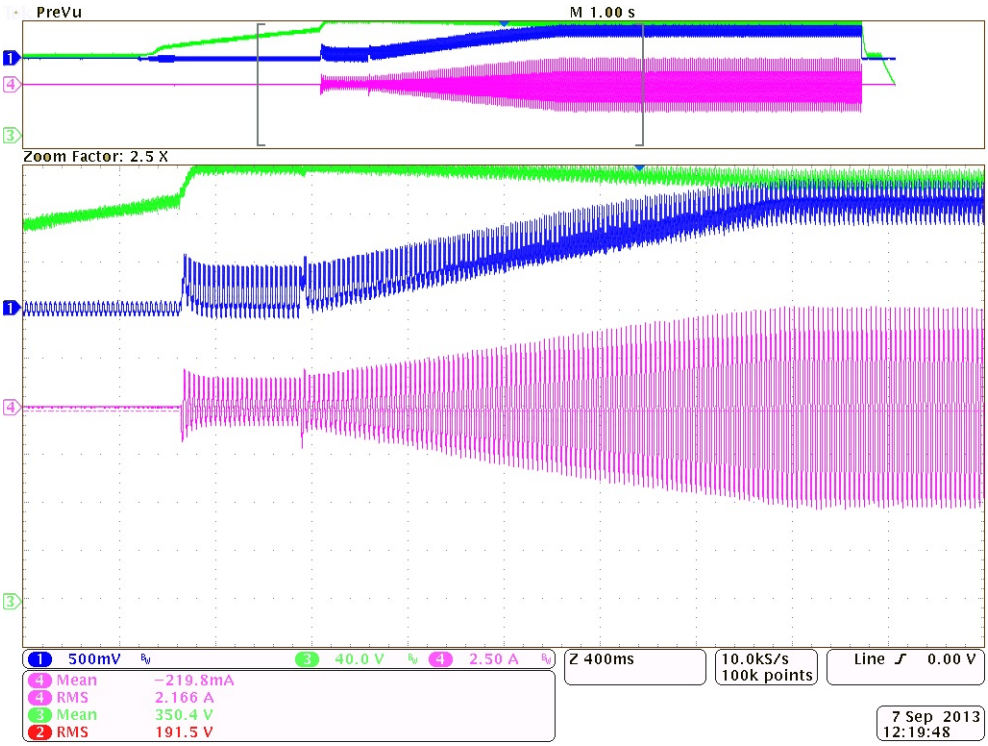

Figure 4.14 Experimental Waveforms of the GTI. (Complete Sequence)

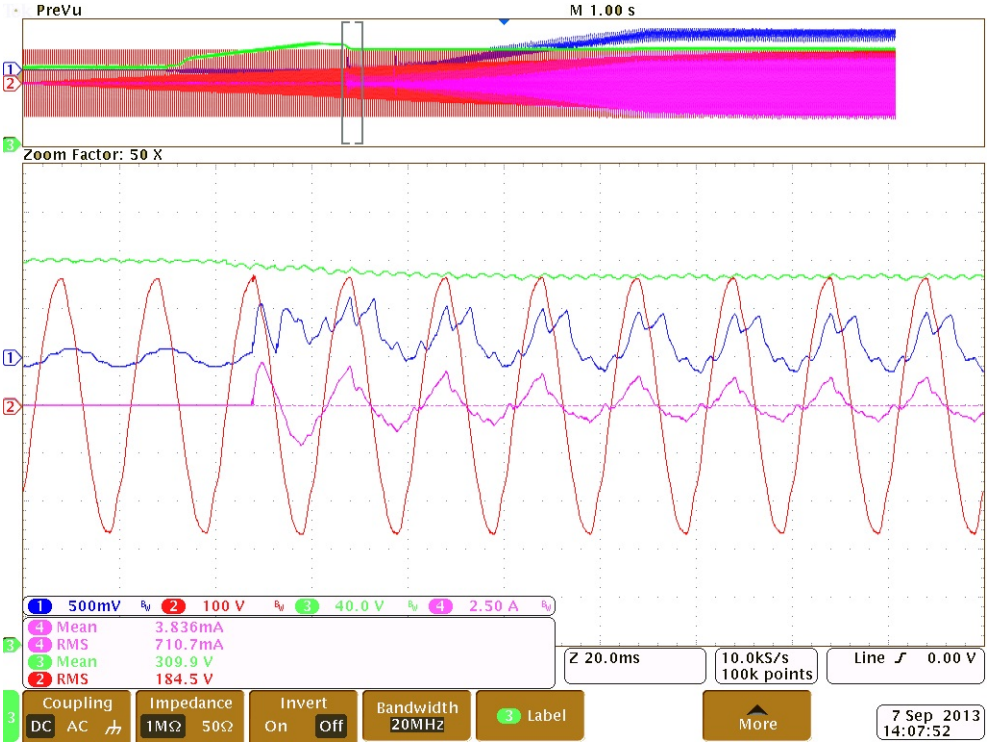

Figure 4.15 Experimental Waveforms of the GTI. (Inrush Sequence)

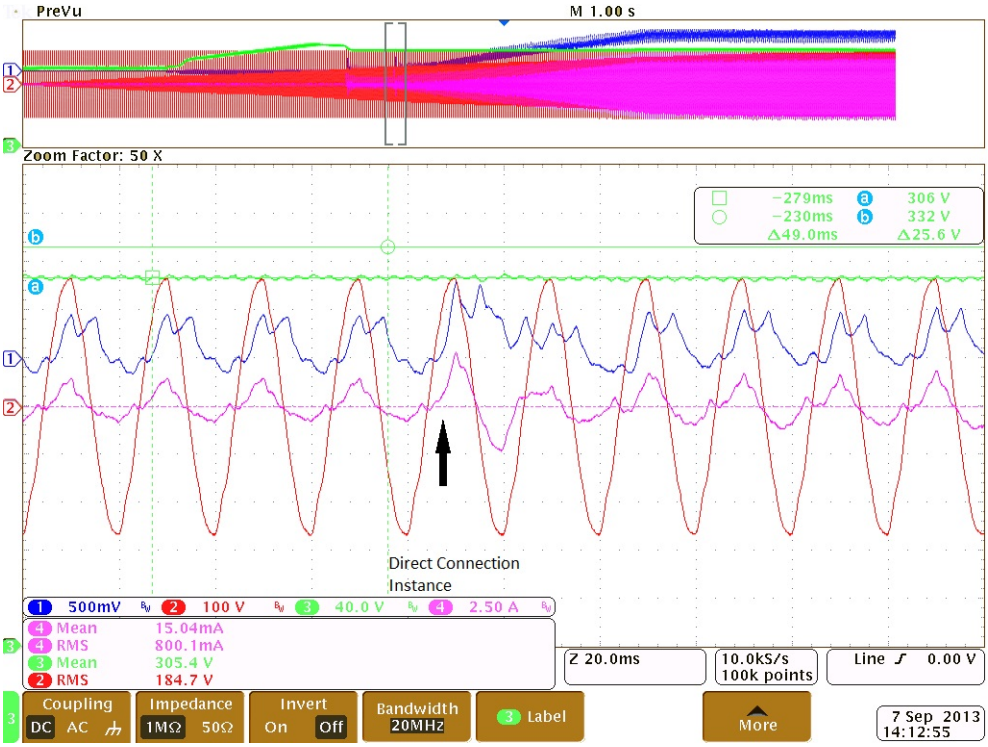

Figure 4.16 Experimental Waveforms of the GTI. (Direct Grid Connection Instance)

grid (Connection sequence) and then the output current is stabilized at the set-point. The ramp up sequence starts resulting in the output current increase.

Fig. 4.17 shows the steady state grid current. The set-point of the grid current is set to 4.1 Arms. The grid current is in phase with the grid voltage which results in active power flow to the grid. The capacitor voltage V_C of the Z-source is also stable.

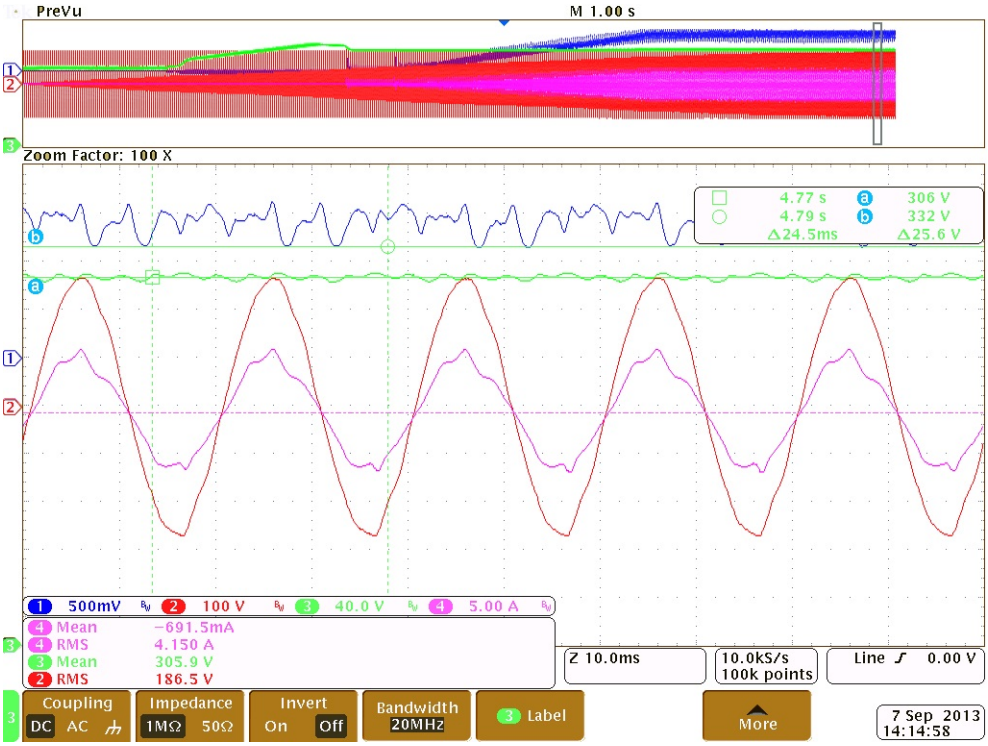

Figure 4.17 Experimental Waveforms of the GTI. (Steady State)

4.5 CHAPTER SUMMARY

The experimental studies on the designed and simulated circuit are presented in this chapter. Each experiment and its test setup are explained in detail. The measurement points are shown and the measurement records are presented. In the first section, The PLL circuit is evaluated, the captured data from the oscilloscope for a specific disturbance is compared to the results of the simulation with the same disturbance. It is shown that the implemented PLL has the same characteristics as the simulated one. In the second section the component waveforms and the controller response for the Z-source converter are verified. It is shown that the simulated and experimented data are in close agreement. In the last section the waveforms of the grid connection are presented. It is shown that the GTI can send power to the grid and the current is in phase with the grid voltage as required.

CHAPTER V

CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

Phase synchronization, voltage boost and inverter sections are the most important parts of a grid tie inverter (GTI). The number of stages in an inverter for voltage boost and DC/AC conversion affects the efficiency and cost. In this study, the Z-source inverter which makes it possible to construct a single stage grid tie inverter is studied. The DC analysis and the small signal models of the power stages are derived by mathematical modeling and are verified by extensive circuit simulations. Linear controllers are designed based on the derived models and these controllers are implemented and tested using the GTI prototype developed in this thesis study. It is shown that the simulation and real implementation results are in close agreement.

It has to be emphasized that the Z-source inverter (ZSI) is a new topology with numerous research results in the literature. The application of this new topology to PV systems brings many advantages as well as some disadvantages. One of the issues that should be dealt with in PV systems is the discontinuous input current of the ZSI. Discontinuous input current may degrade the PV efficiency and it may require larger filtering components than the other topologies such as the boost converter. Controlling the DC link and the full bridge using the same four switches increases the complexity of the PWM scheme and brings some limitations. Using the same switching period for the DC link and output current control poses some issues with the DC link voltage. The shoot-through duty cycle for the Z-network limits the maximum available duty cycle for the output control. For that reason, high boost gains also increase the voltage stress of the switching elements. Another difficulty with this topology is the measurement of the DC link voltage. Direct measurement of the DC link voltage requires complex measurement techniques because of the floating nature of the DC link. Multiple

inductors and capacitors are one of the issues related to the Z-source which may tend to increase the volume and the cost of the system.

5.2 FUTURE WORK

The study presented in this thesis is intended to construct a basis for the design of an industrial product. The concept of the GTI comprises many different topics such that some of the parts of the required sections of the GTI are not fully covered in this study. The MPPT is one of the inevitable parts of a GTI. A MPPT algorithm should be developed and integrated into the software and tested accordingly. The efficiency of the GTI is one of the key points since one of the requirements is to provide the maximum available power to the grid. The power section can be improved to increase the efficiency and reduce the heat-sinking thus cooling requirements. The controllers presented in this study can be further improved which will result in less distorted grid current and thus less harmonic content. The DC component of the grid current observed in this study needs further attention. The offset errors of the sensors and the nonlinearities in the power section may need further attention. It should also be noted that the common mode noise produced by the setup is considerable and needs mitigation.

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APPENDIX A

Matlab Codes

Matlab Code for T_{cc} (2.63)

```
%% vc/d GTI
clc;clear
format long
syms zl zo zc D Dh d vc vi I1 I2 I3 Ro Lo L s C IL Io vo VO I VC VI

Z=[(zl+zc*Dh)/D (-zl-zc)*Dh/D-D*zo/Dh (Dh*zc+D*zo)/Dh
    (-zl-zc*D)/D (Dh*zl-D*zo)/D zo
    -zc*Dh/D zc*Dh/D+zo -zl-zo-zc]; %matrix of mesh currents
Q=[((-VO*D-I*Dh*(zl+zc))*d/(D*Dh^2))' (I*zl*d/(D*Dh))' (I*zc*d/(D*Dh))']';
Zm=simple(Z^-1); %inverse of the mesh current matrix
I1=simple(Zm*Q) % I1 is the matrix of calculated currents in all meshes
vc_d_imp=simple(I1(1,1)*zc/d)
% this is the tr function of interest in impedance form
```

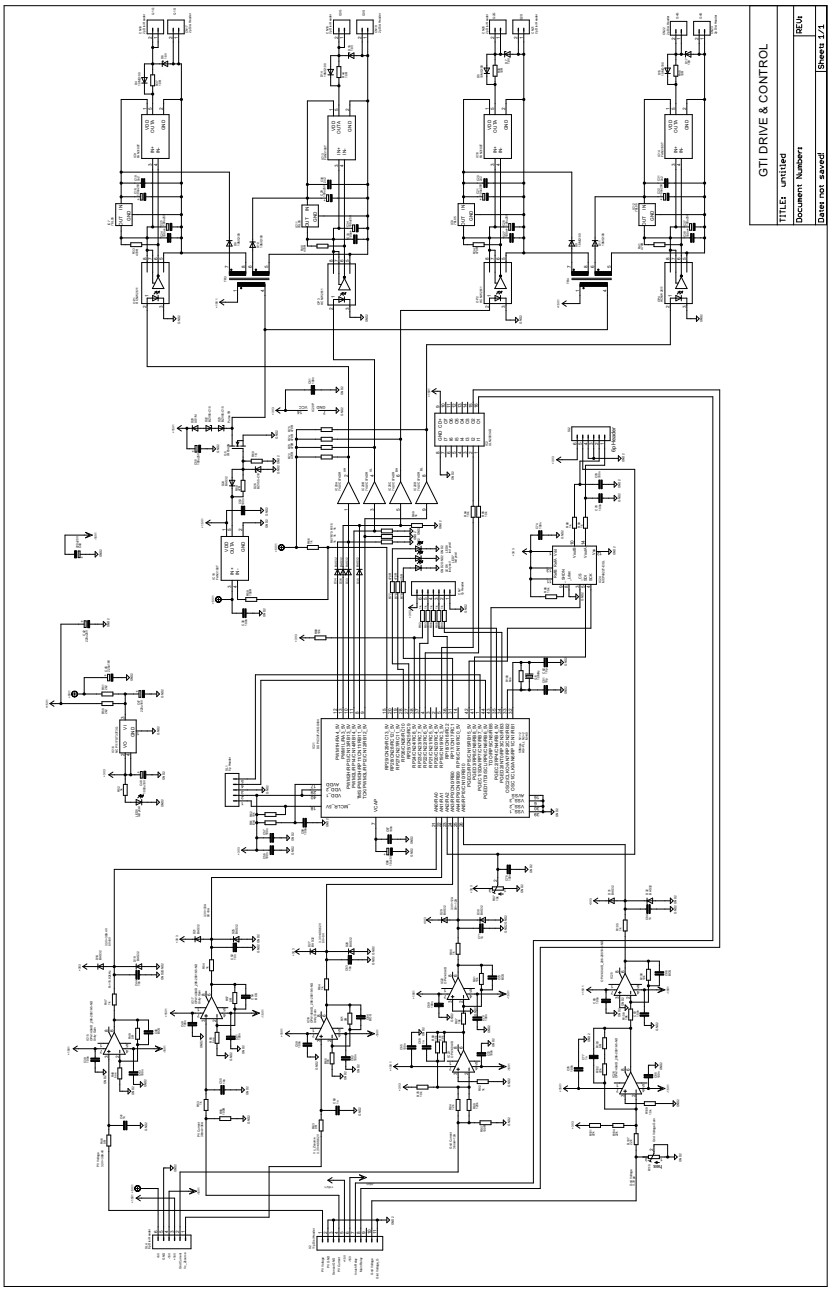
Matlab Code for T_{ci} (2.58)

```
%%  z_source vc_vi transfer function
clc;clear;clear all
syms zl zc z0 k vi I1 I2 I4 I C d D

A=[(zl+zc)/k+zl -k*z0-zl/k-zc/k zc+k*z0
    -zl/k-zl-zc zl/k-z0 z0
    -zc/k z0+zc/k -zc-z0-zl];
B=simple(A^-1);
C=[-vi 0 0 ]';
I=simple(B*C);
I2=I(1,1);
I3=I(2,1);
I4=I(3,1);
k=d/D;
vc=simple(eval(I2*zc/vi'))
  %vc/vi tr function in impedance form
```

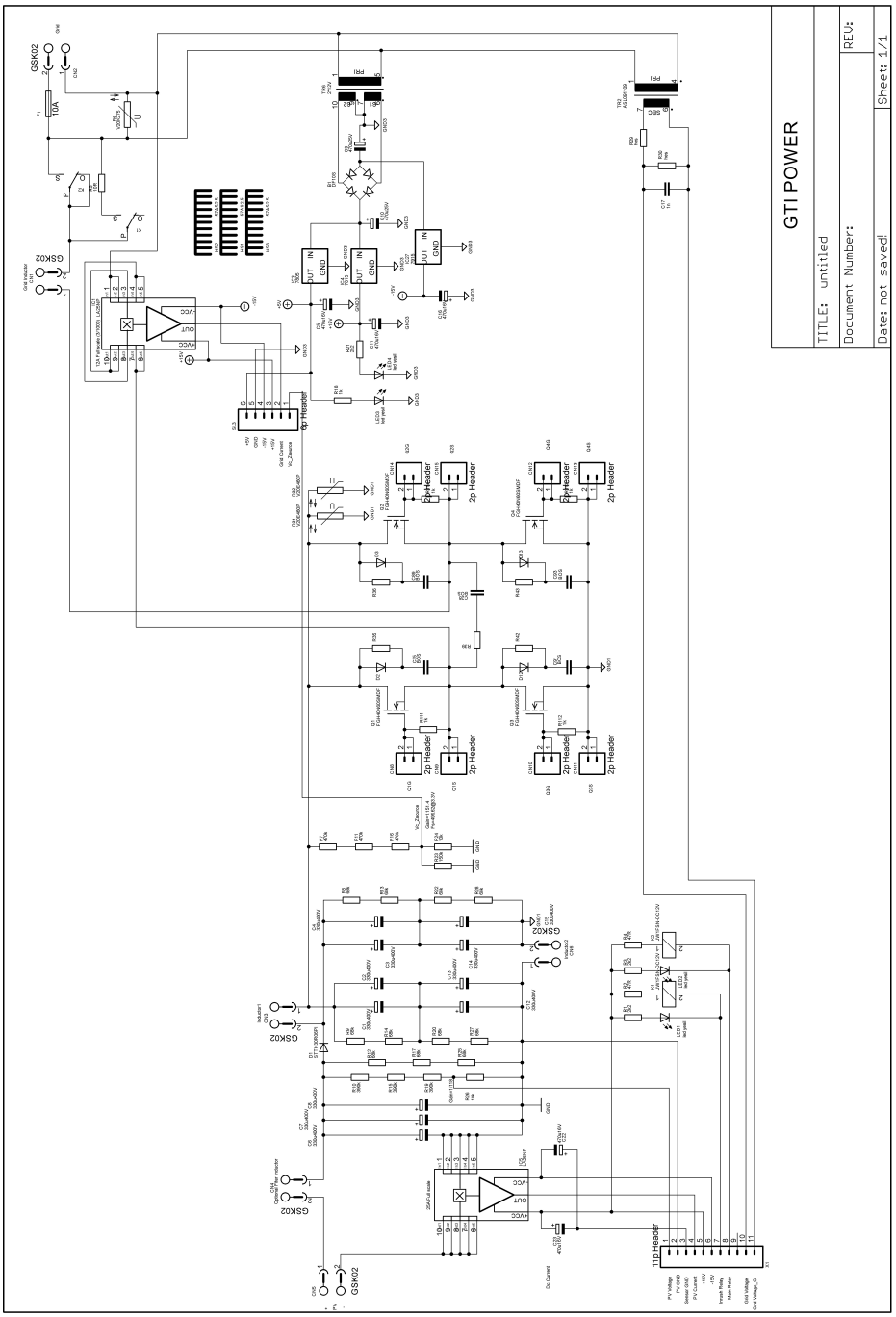
APPENDIX B

Schematic Diagram of the Control Board



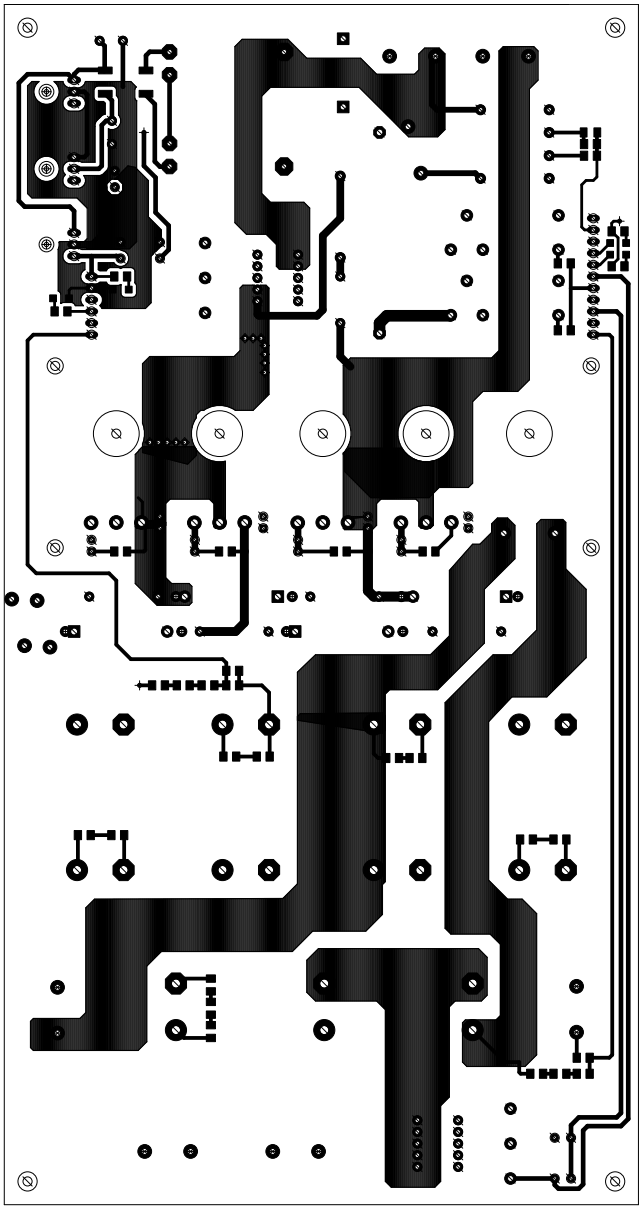
APPENDIX C

Schematic Diagram of the Power Board



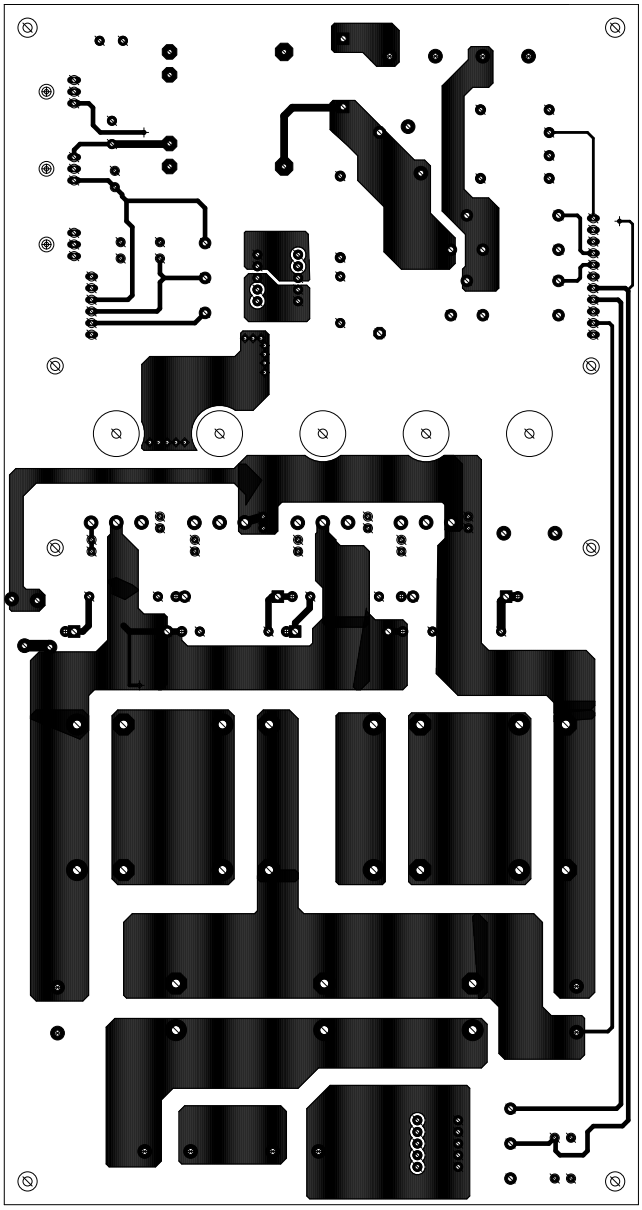
APPENDIX D

PCB Layout of the Power Board (Top Layer)



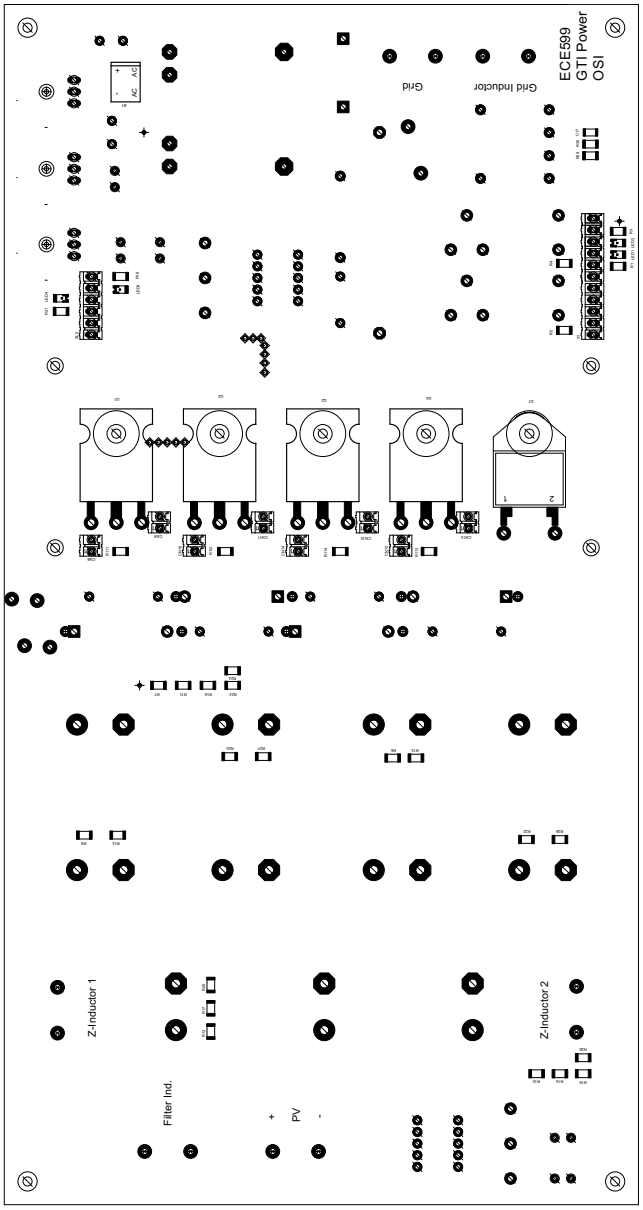
APPENDIX E

PCB Layout of the Power Board (Bottom Layer)



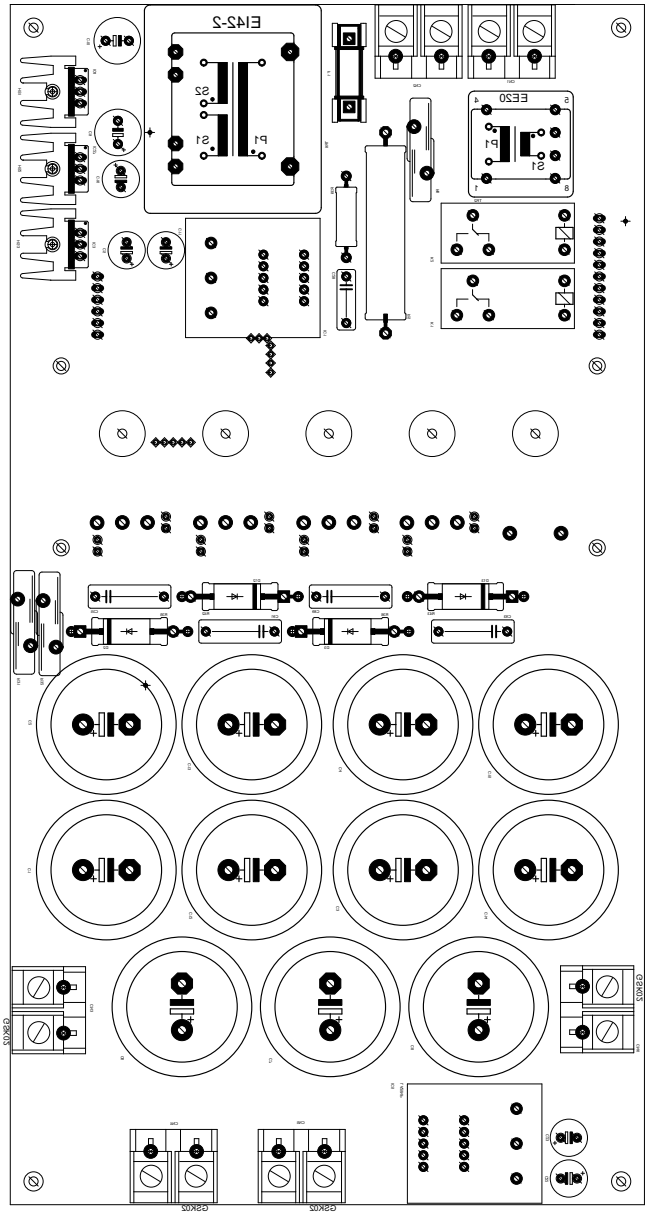
APPENDIX F

PCB Layout of the Power Board (Top Placement)



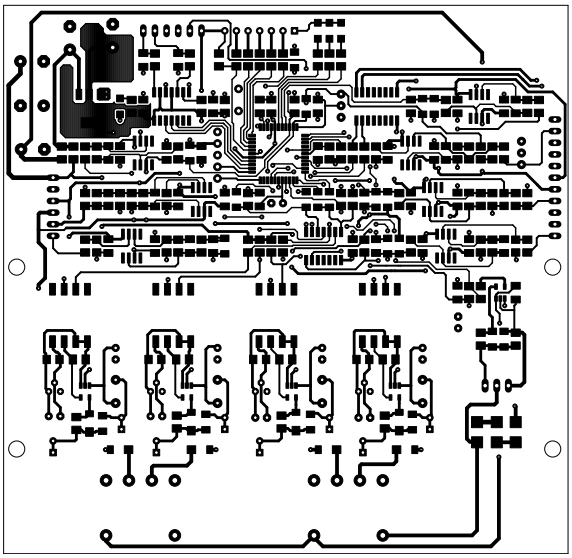
APPENDIX G

PCB Layout of the Power Board (Bottom Placement)



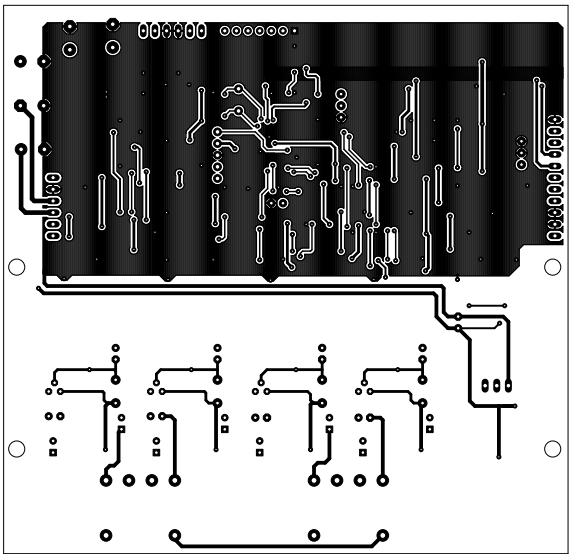
APPENDIX H

PCB Layout of the Control Board (Top Layer)



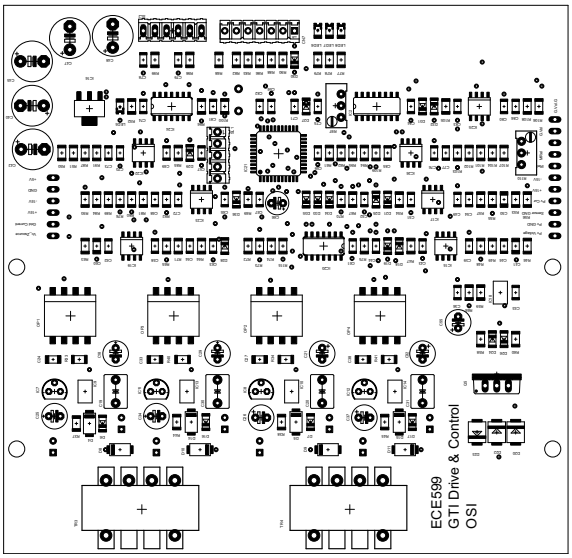
APPENDIX I

PCB Layout of the Control Board (Bottom Layer)



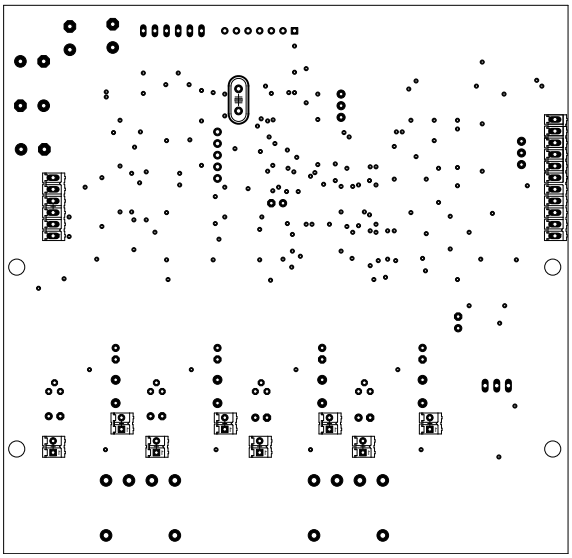
APPENDIX J

PCB Layout of the Control Board (Top Placement)



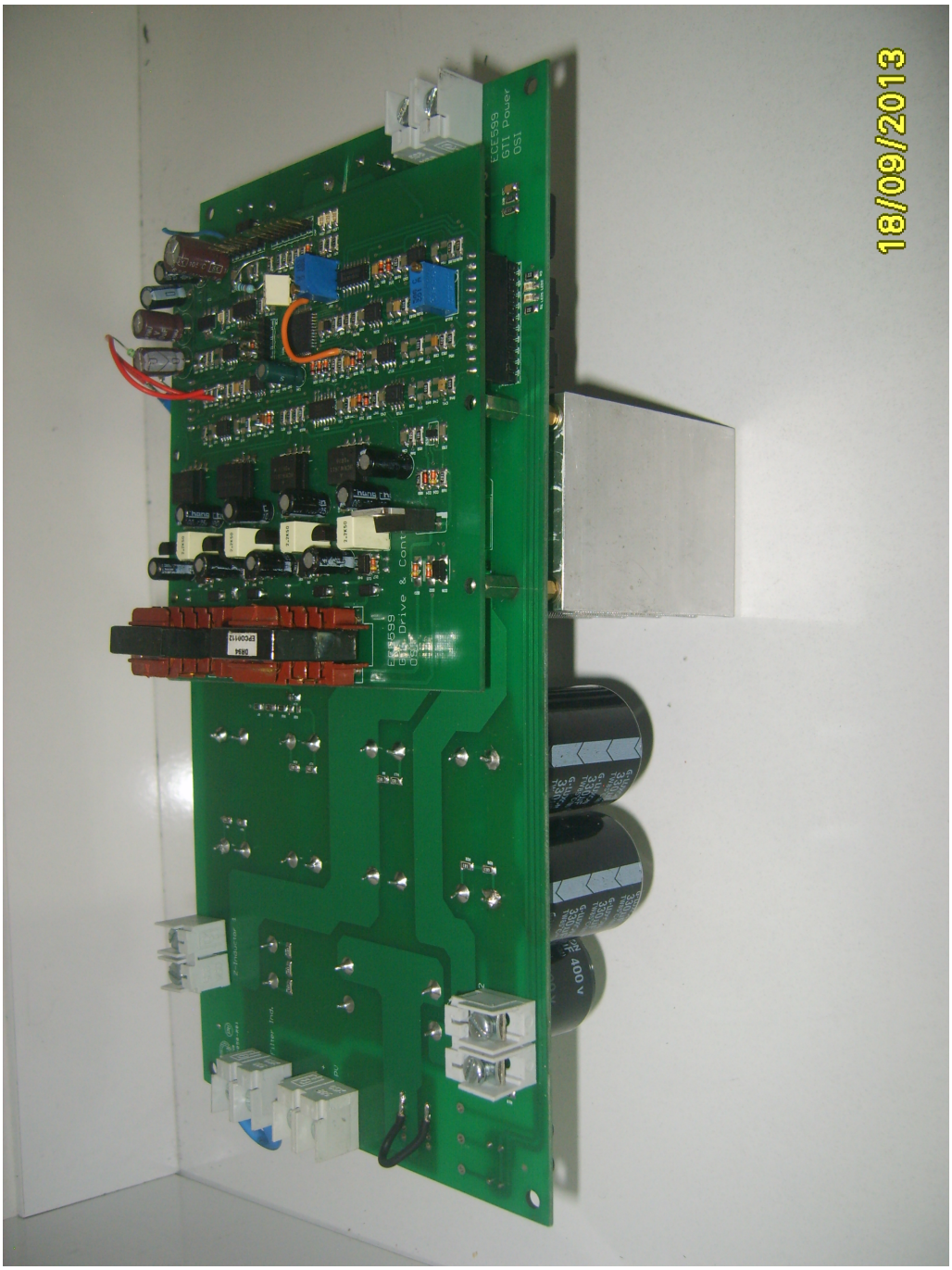
APPENDIX K

PCB Layout of the Control Board (Bottom Placement)



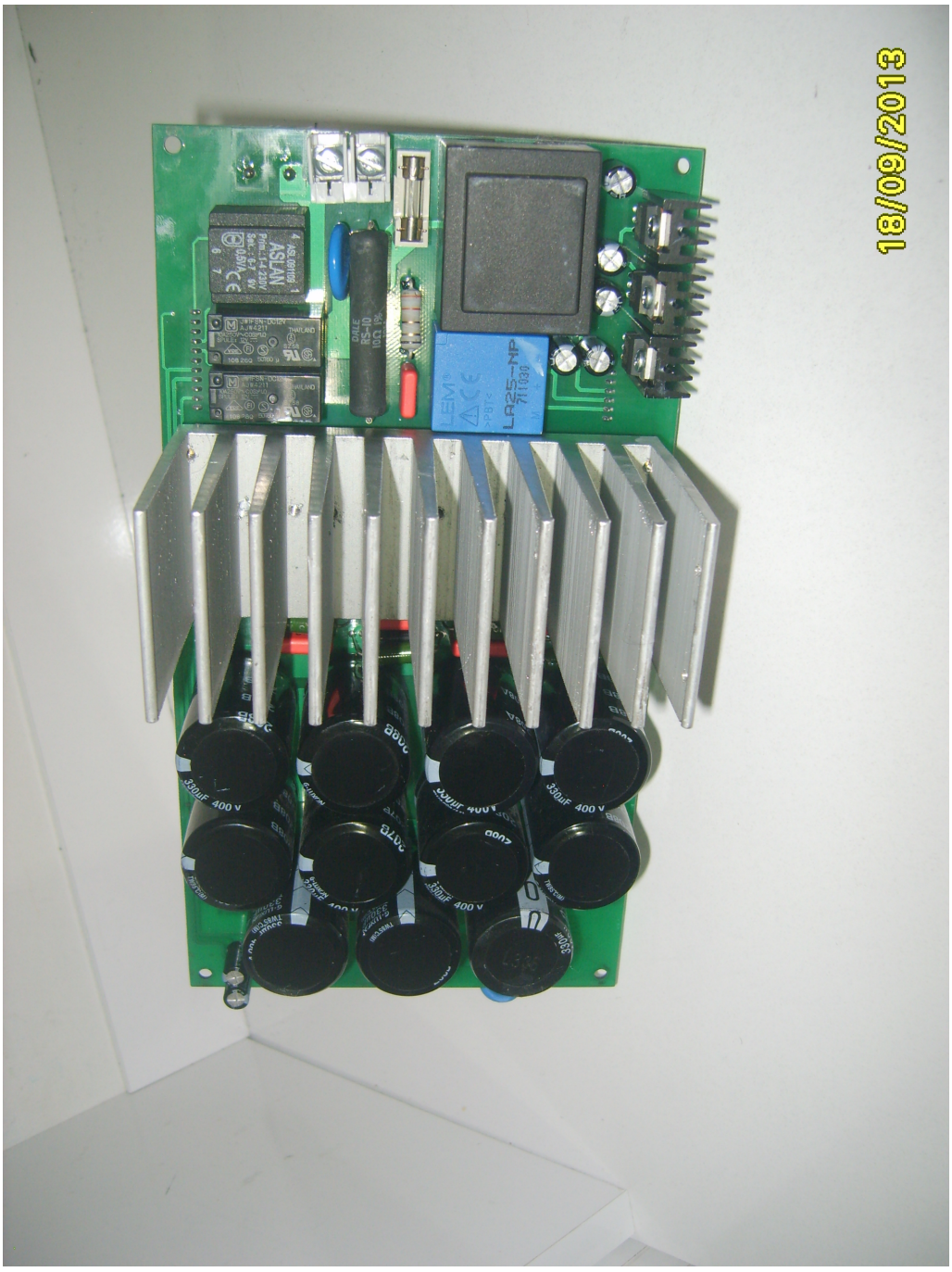
APPENDIX L

Photo of the Prototype GTI (Top View)



APPENDIX M

Photo of the Prototype GTI (Bottom View)



CURRICULUM VITAE

PERSONAL INFORMATION

Surname, Name: ŞİMŞEK, Oğuz
Nationality: Turkish (TC)
Date and Place of Birth: 01 April 1973, İstanbul
Marital Status: Married
Phone: +90 312 267 08 18
e-mail: oguzgz@yahoo.com

EDUCATION

Degree	Institution	Year of Graduation
BS	Anadolu University Business Administration Eskişehir	1996
High School	Yenimahalle E.M.L., Ankara	1990

FOREIGN LANGUAGES

English.

HOBBIES

Music, Movies, Reading technical books.