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OFDM TRANSMITTER AND RECEIVER IMPLEMENTATION ON FPGA

SAMET TİLKİOĞLU

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MASTER THESIS

OFDM Transmitter and Receiver Implementation on FPGA

BY

SAMET TİLKİOĞLU

JUNE 2018

Title of the Thesis: **OFDM Transmitter and Receiver Implementation on FPGA.**

Submitted by **Samet TİLKİOĞLU**

Approval of the Graduate School of Natural and Applied Sciences, Çankaya University.

Prof. Dr. Can ÇOĞUN
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This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

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ABSTRACT

OFDM Transmitter and Receiver Implementation FPGA

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M.Sc. Department of Electronic and Communication Engineering

Supervisor: Prof. Dr. Halil Tanyer EYYUBOGLU

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In this thesis, digital modulations which are 4QAM and QPSK are designed and implemented using FPGA hardware using OFDM communication technique. The Genesys Virtex-5 development card produced by Digilent is used as hardware. The development of the relevant card software was developed with the System Generator Blocks and native Simulink blocks in Simulink (MATLAB 2012a) and transferred to the corresponding card. In the steps of developing algorithms, digital modulation techniques are used.

Keywords: OFDM (Orthogonal Frequency-Division Multiplexing), Transmitter, Receiver, Wireless Communication, FPGA (Field Programmable Gate Array), MATLAB, Simulink, System Generator, FFT, IFFT

ÖZ

FPGA üzerinde OFDM Alıcı ve Verici Uygulaması

TİLKİOĞLU, Samet

Yüksek Lisans, Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Tez Yöneticisi: Prof. Dr. Halil Tanyer EYYUBOGLU

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Bu tezde, OFDM haberleşme tekniği kullanılarak dijital modülasyonlardan olan 4QAM ve QPSK modülasyon çeşitleri, FPGA donanımı kullanılarak tasarlanmış ve gerçekleştirilmiştir. Donanım olarak Digilent firması tarafından üretilen Genesys Virtex-5 geliştirme kartı kullanılmıştır. İlgili kartın yazılımının geliştirilmesi, Simulink (MATLAB 2012a) üzerinde System Generator Blokları ve Simulink Blokları kullanılarak geliştirilmiş ve ilgili karta aktarılmıştır. Algoritma geliştirme safhalarında, dijital modülasyon teknikleri kullanılmıştır.

Anahtar Kelimeler: OFDM (Ortogonal Frekans Bölmeli Çoğullama), Verici, Alıcı, Kablosuz Haberleşme, FPGA(Alanda Programlanabilir Kapı Dizileri), MATLAB, Simulink, Xilinx ISE, System Generator, FFT, IFFT

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LIST OF ABBREVIATION

Abbreviation	Definition
3G	Third Generations
3GPP	Third Generation Partnership Project
4G	Fourth Generations
ADSL	Asymmetric Digital Subscriber Line
ASIC	Application Specific Integrated Circuit
ASK	Amplitude Shift Keying
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
CP	Cyclic Prefix
CPLD	Complex Programmable Logic Device
dB	Decibel
DFT	Discrete Fourier Transform
DSL	Digital Subscriber Lines
FDM	Frequency Division Multiplexing
FDMA	Frequency Division Multiplexing Access
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IC	Integrated Circuits
IDFT	Inverse Discrete Fourier Transform
IEEE	Institute of Electrical and Electronics Engineers
IFFT	Inverse Fourier Transform
ISI	Intersymbol
LAN	Local Area Network
LOS	Line-of-Sight
LTE	Long Term Evolution

M-FSK	M-ary frequency-shift keying
M-PSK	M-ary phase-shift keying
M-QAM	M-ary quadrature amplitude modulation
MIMO	Multiple-Input and Multiple-Output
OFDM	Orthogonal Frequency Division Multiplexing
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SNR	Signal-Noise Ratio
TTL	Transistor Transistor Logic
USB	Universal Serial Bus
VDSL	Very High Bit Rate Digital Subscriber Line
Wi-Fi	Wireless Fidelity
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	Wireless LAN

LIST OF SYMBOLS

Symbol	Definition
B_W	Bandwidth
P_b	Probability of Error
c	Speed of Light
T_s	Symbol Duration
E_s	Energy per symbol (Joule)
E_b	Energy per bit (Joule)
f_c	Carrier Frequency
f_s	Sampling Frequency
F_s	Symbol rate (1/sec
λ	Wavelength
σ_w^2	Gaussian noise variance
N_o	Noise Power Spectral Density
N_b	Bit per symbol
P_b	Probability of Error

CHAPTER 1. INTRODUCTION

1.1. Background

The word communication arises from the Latin word **‘commūnicāre’**, which means “to share”. Communication can be basically defined step for exchange of information. In other words, communication can be defined as information transfer between different points in space or time, where the term information is loosely employed to cover standard formats that we are all familiar with, such as voice, audio, video, data files, web pages, etc. [1]

In the fastest growing of the communication industry, wireless communication technology has rapidly developed. With this development, necessities of requirement for higher data rates and so enlarging demand on band are arisen. Due to capacity requirements, different type of techniques are tried and applied. OFDM (Orthogonal Frequency Domaain Multiplexing) resolves these needs in communication technologies.

1.1.1. Orthogonal Frequency Division Multiplexing (OFDM) Basics

OFDM which is an air-interface technique has become the popular modulation technique for wireless communication systems. Its concept is based on parallel transmission of data over dispersive channels. When the literature is examined, OFDM has been firstly mentioned in 1957. Year-to-year development can be seen from the list which is given below.

Year

- 1957 The concept of parallel data transmission - **Doelz *et al.***[2]
- 1966 First OFDM scheme proposed - **Chang** [3]

- 1967 **Saltzberg** studied a multi-carrier system employing Orthogonal QAM of the carriers[4]
- 1970 U.S. Patent on OFDM issued [3]
- 1971 **Weinstein** & **Ebert** applied DFT to OFDM modems[5]
- 1980 **Hirosaki** designed a subchannel-based equalizer for an orthogonally multiplexed QAM system [6]

  Keasler *et al.* described an OFDM modem for telephone networks [7]
- 1985 **Cimini** investigated the feasibility of OFDM in mobile communications [8]
- 1987 **Alard** and **Lasalle** employed OFDM for digital broadcasting [9]
- 1991 ANSI ADSL standard [10]
- 1994 ANSI HDSL standard [11]
- 1995 ETSI DAB standard: the first OFDM-based standard for digital broadcasting systems [12]
- 1996 ETSI WLAN standard [13]
- 1997 ETSI DVB-T standard [14]
- 1998 ANSI VDSL and ETSI VDSL standards [15], [16]

  ETSI BRAN standard [17]
- 1999 IEEE 802.11a WLAN standard [17]
- 2002 IEEE 802.11g WLAN standard [18]
- 2003 Commercial deployment of FLASH-OFDM commenced [19], [20]

- 2004 ETSI DVB-H standard [21]

  IEEE 802.16-2004 WMAN standard [22]

  IEEE 802.11n draft standard for next generation WLAN [23]

- 2005 Mobile cellular standard 3GPP Long-Term Evolution (LTE) downlink [24]

- 2007 Multi-user MIMO-OFDM for next-generation wireless [25]

As you seen from the list, even though OFDM's story rely on the old, we can find it in many daily applications such as Wi-Fi, MIMO technique, WiMAX, LTE, DVB standard, DAB broadcast standard and etc.

1.1.2. Field Programmable Gate Array (FPGA) Basics

Field programmable gate arrays (FPGAs) are digital integrated circuits (ICs) that contain configurable (programmable) blocks of logic along with configurable interconnects between these blocks[26]. In other words, they have huge array of gates which can be reprogrammed and reconfigured. They are made from silicon, and we can use them to solve any computable problems. The origins of FPGAs are based on transistor technology. Timeline bar approximately indicates related developments from first mentioned to up to date of FPGA technology.

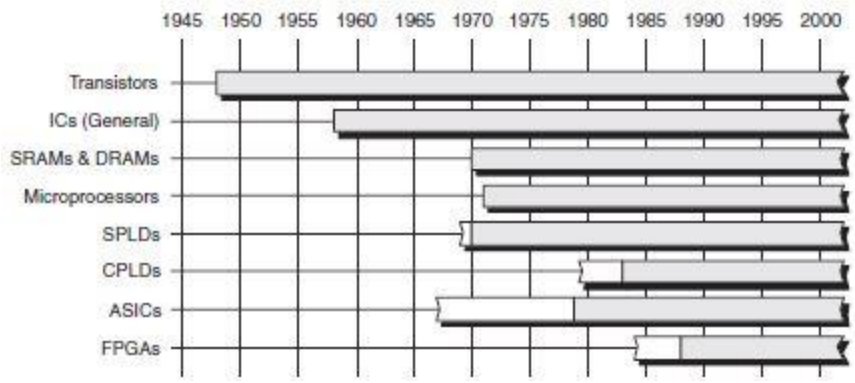


Figure 1: Transistor-Based Technology Timeline [26]

On December 23, 1947, physicists William Shockley, Walter Brattain, and John Bardeen, working at Bell Laboratories in the United States, succeeded in creating the first transistor: a point-contact device formed from germanium. In the following years, BJTs, TTLs, ECLs, and FETs have been pronounced. FETs are often used as abbreviated form of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistor) which are one of the most basic elements of FPGAs. And in the world of FPGAs, MOSFETs are referred to as gates.

Field programmable gate arrays (FPGAs) can now consist of a million equivalent logic gates and tens of thousands of flip-flops. This means that it is not possible to use traditional methods of logic design involving the drawing of logic diagrams when the digital circuit may contain thousands of gates.[27] FPGAs have traditionally found use in high-speed custom digital applications where designs tend to be more constrained by performance rather than cost.[28]

Today digital designers use HDLs (hardware description languages). The most commonly used HDLs are VHDL, Verilog and System Verilog. All of these hardware description languages allow the user to design digital systems by writing a program. The program describes the behavior of the digital circuit. This program can be used to both *simulate* the operation of the circuit and *synthesize* an actual implementation of the circuit in a CPLD, an FPGA, or an application specific integrated circuit (ASIC).[27]

CPLDs and FPGAs are commonly used today, and they have same design flow which consists of the steps below. If we compare them, we can say that FPGAs have more complexity than CPLDs.

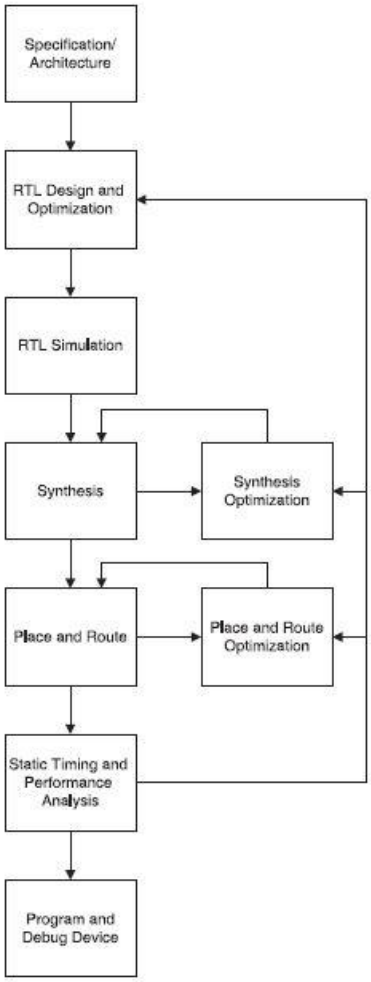


Figure 2: FPGA Design Flow [29]

1.2. Thesis Overview

The main goal of this thesis is OFDM transmitter and receiver implementation. We used Digilent's Genesys FPGA development board as a hardware. It has Xilinx Virtex-5 FPGA. For develop FPGA, model-based design was chosen. For a model-based design environment, Xilinx System Generator (Xilinx ISE 14.2) installed MATLAB/Simulink (R2012a) was used. During the model-based design, both native Simulink blocks and Xilinx System Generator blocks was used. The OFDM technique

of communication systems evaluated using formula-based calculations, waveform-level simulation on Simulink and hardware prototyping via FPGA development board.

First of all, in Chapter 2, wireless communication and digital modulation techniques were mentioned briefly. Then, in Chapter 3, OFDM technique was described with its details. In following chapter, in chapter 4, FPGAs and model-based FPGA design via MATLAB Simulink with Xilinx ISE Design Suite were tried to explain step-by-step. Finally, in Chapter 5, designing OFDM transmitter and receiver design with native Simulink blocks and Xilinx specific blocks in MATLAB Simulink was demonstrated. And FPGA implementation of OFDM from Simulink model using System Generator was constructed and results are given.

CHAPTER 2. WIRELESS COMMUNICATION AND DIGITAL MODULATION TYPES

2.1. An Overview of Wireless Communications

Wireless communications is one of the communication type that is performed and delivered wirelessly. There are different types of wireless communication applications. We can give satellite communication, mobile communication, wireless network communication, infrared communication, and bluetooth communication types as an example for wireless communication.

The first wireless networks were developed in the Pre-industrial age. These systems transmitted information over line-of-sight distances (later extended by telescopes) using smoke signals, torch signaling, flashing mirrors, signal flares, or semaphore flags [30]. The ongoing needs for communication since Pre-industrial age, it has improved day-by-day. After telegraph network which was invented by Samuel Morse in 1838 telephone was invented. Following these events, Italian physicist Guglielmo Marconi who was born in 1874 in Bologna succeeds sending first radio transmission. This event is referred to as a pioneer of wireless communication.

Digital communication systems are becoming increasingly attractive because of the ever-growing demand for data communication and because digital transmission offers data processing options and flexibilities not available with analog transmissions [31]. In other way, digital communication offers the less complexity of communication of during signal processing.

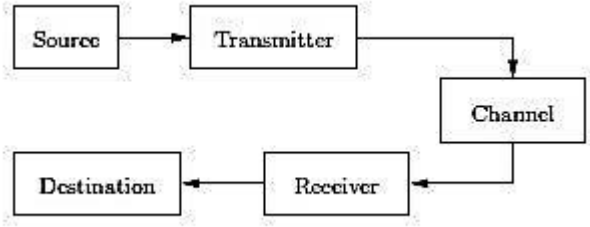


Figure 3: Basic Digital Communication Model

Digital modulation is the process of representing binary information using segments of different sinusoidal waveforms. The parameters that can be adjusted in a sinusoidal wave are its amplitude, frequency and phase [32].

2.2. Digital Modulation Types

The basic purpose of communication is to exchange information as a general. Digital communication systems are communication systems that use digital sequences as an interface between the source and the channel input [33]. This situation is also similar on the receiver side, and we can think of reversing the order of transmitter side.

In digital communication, modulation is a term that is used very frequently. We can define modulation in a general as representation of digital information in terms of analog waveforms. In this form, information can be transferred over the physical channels. In digital communication, the digital data are used, and the data are in the form of a stream of binary data which are 0's and 1's.

A number of other advantages over the analog modulation are offered by digital modulation. It's including powerful error correction techniques, higher data rates, resistance to channel impairments, more efficient multiple access strategies, and better security and privacy. Digital modulations allow us to transfer a bit stream data through the analog channels. Especially, high level modulation techniques such as MQAM allow much higher data rates in digital modulation as compared to analog modulation with the same signal bandwidth. [30]

The most fundamental digital modulation techniques are based on keying, and they are named according to the techniques. These are ASK FSK, PSK and QAM modulation types which are explained below:

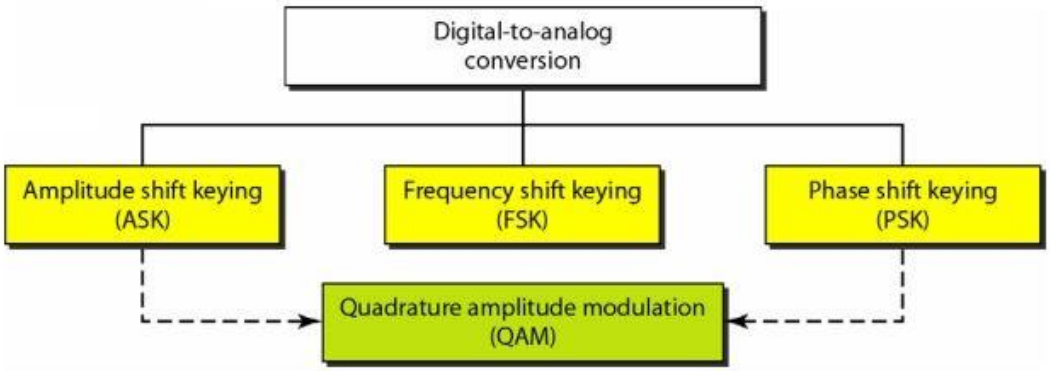


Figure 4: Digital Modulation Types

2.2.1. ASK (Amplitude Shift Keying)

In Amplitude Shift Keying (ASK), the two binary values are represented by two distictive amplitudes of the carrier frequency. This modulation type can be easily understood with the figure which is given below. Mathematically;

$$s(t) = \begin{cases} A\cos(2\pi f_c t) & 1\ (binary) \\ 0 & 0\ (binary) \end{cases}$$

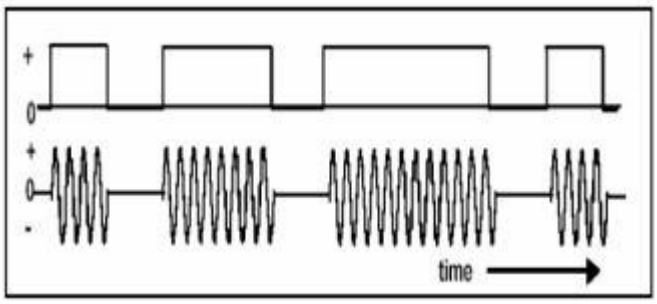


Figure 5: ASK modulation for Digital Data

2.2.2. FSK (Frequency Shift Keying)

The most common form of FSK is binary FSK (BFSK), in which the two binary values are represented by two distinctive frequencies close the carrier frequency. The resulting transmitted signal for one bit time is mathematically explained below.

$$s(t) = \begin{cases} A\cos(2\pi f_1 t) & 1\ (binary) \\ A\cos(2\pi f_2 t) & 0\ (binary) \end{cases}$$

2.2.3. PSK (Phase Shift Keying)

In Phase Shift Keying (PSK) or Digital Phase Modulation, the phases of the carrier signals are shifted to represent data. Mathematically;

$$s(t) = \begin{cases} A\cos(2\pi f_c t) & 1\ (binary) \\ A\cos(2\pi f_c t\ +\ \pi) & 0\ (binary) \end{cases} = \begin{cases} A\cos(2\pi f_c t) & 1\ (binary) \\ -A\cos(2\pi f_c t) & 0\ (binary) \end{cases}$$

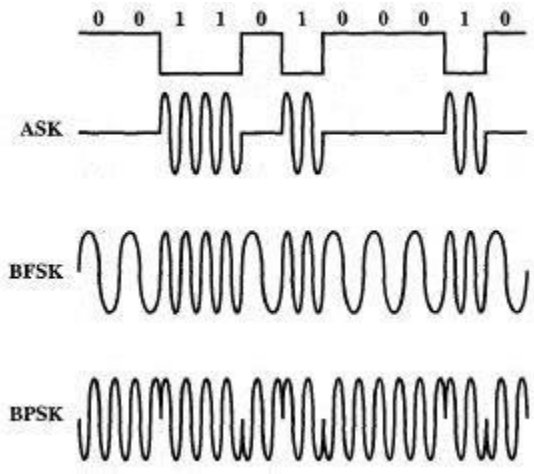


Figure 6: ASK, BFSK and BPSK Modulation Types[34]

In Quadrature phase shift keying (QPSK), the carrier varies in terms of phase the carrier undergoes four changes in phase (four symbols) and can thus represent 2 binary bits of data per symbol. There are four possible phase shifts.

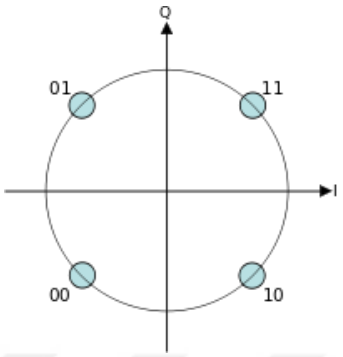


Figure 7: QPSK

2.2.4. QAM (Quadrature Amplitude Modulation)

Quadrature Amplitude Modulation (QAM) is a well-kown analog signaling technique that's used in wireless standards. In QAM, carrier wave is modulated by changing both amplitude and phase. For QAM modulation, we can say that it is a combination of Amplitude Shift Keying (ASK) and Phase Shift Keying (PSK). With QAM modulation, higher data rates can be carried than ASK and FSK.

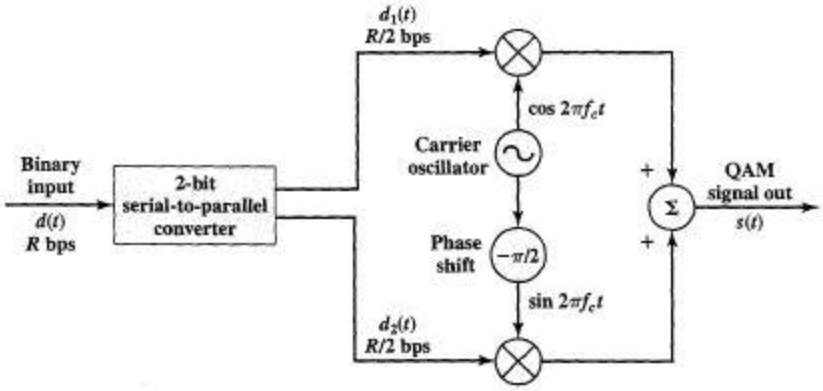


Figure 8: QAM Modulator [34]

QAM can be expressed as:

$$s(t) = A_I \cos(2\pi f_c t) + A_Q \sin(2\pi f_c t)$$

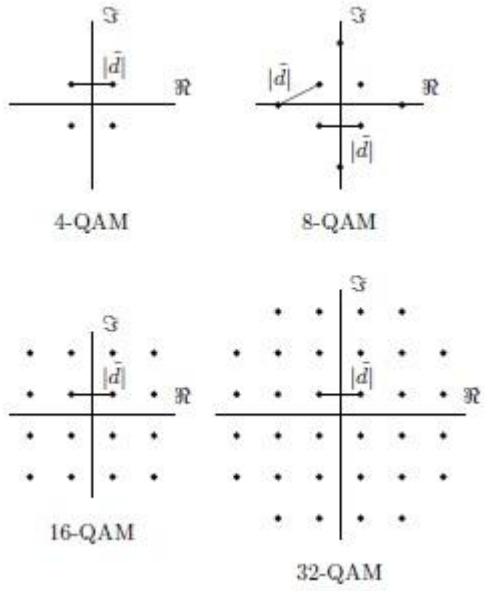


Figure 9: Commonly used QAM (Quadrature Amplitude Modulation) Constellations [35]

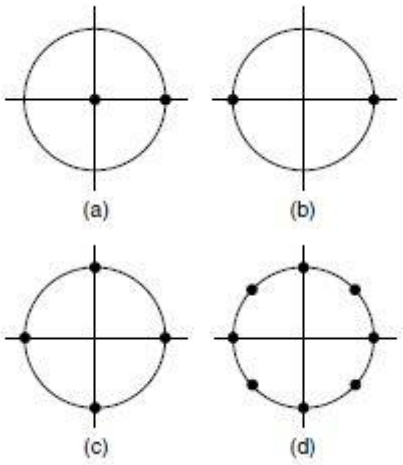


Figure 10: Signal Constellations of Some Basic Single-Carrier Digital Modulation Techniques a) Binary-ASK b) Binary-PSK c) QPSK d) 8PSK

CHAPTER 3. ORTHOGONAL FREQUENCY DOMAIN MULTIPLEXING (OFDM)

3.1. Expression of OFDM

In wireless communication systems technology, OFDM (orthogonal frequency-division multiplexing) has become the popular modulation type. It can be seen as either a modulation technique or a multiplexing technique in literature. This technology has been developed for wideband digital communication, and used for encoding of digital signal of multiple carrier frequencies. In this technique, data is carried with orthogonal sub-carrier signals with different frequencies. Audio broadcasting, DSL Internet Access, Wireless Networks, and in 4G mobile communication systems are using OFDM method.

Frequency division multiplexing (FDM) extends the concept of single carrier modulation by using multiple subcarriers within the same single channel. The evolution of OFDM can be defined as a combination of Frequency Domain Multiplexing (FDM) and Multi-Carrier Modulation/Communication (MCM).

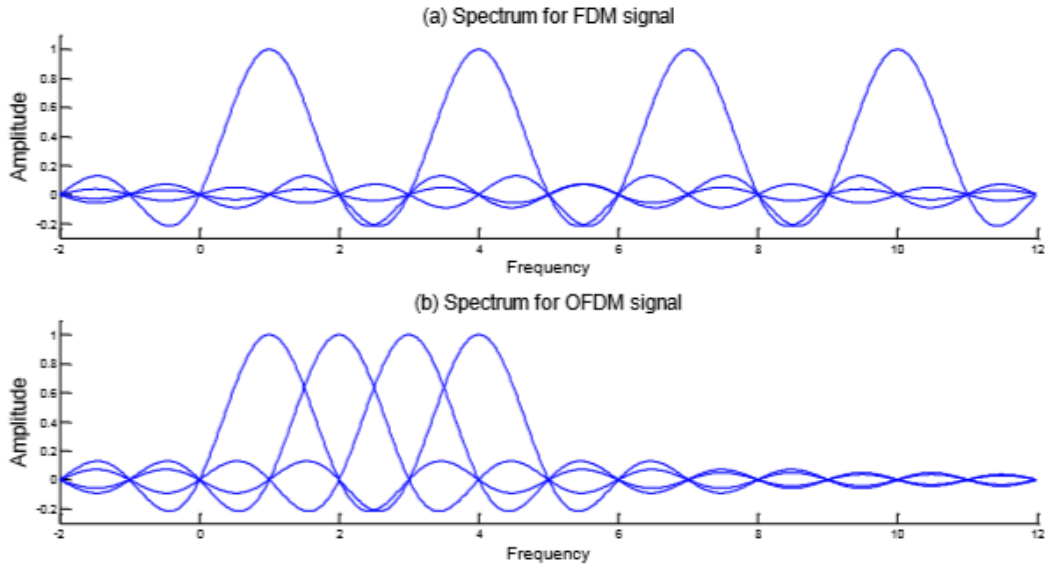


Figure 11: FDM and OFDM Signals

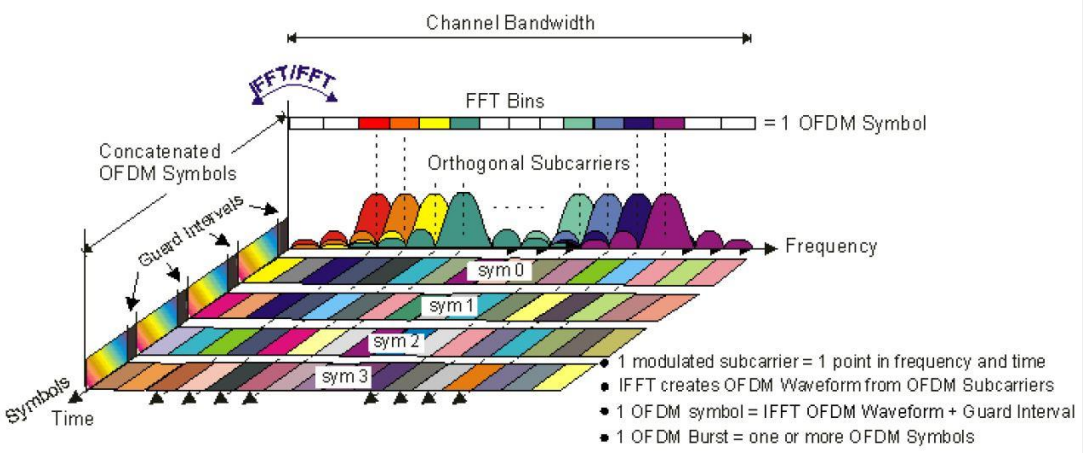


Figure 12: Frequency-Time Representative of an OFDM Signal [36]

Only one sinusoidal wave at all times is used by single-carrier modulation techniques. In the multi-carrier modulation techniques, several sinusoidal waves are transmitted simultaneously. Only one of the three parameters–amplitude, frequency and phase–of the sinusoidal wave are modified by basic single-carrier modulation techniques according to the binary information to be transmitted [32].

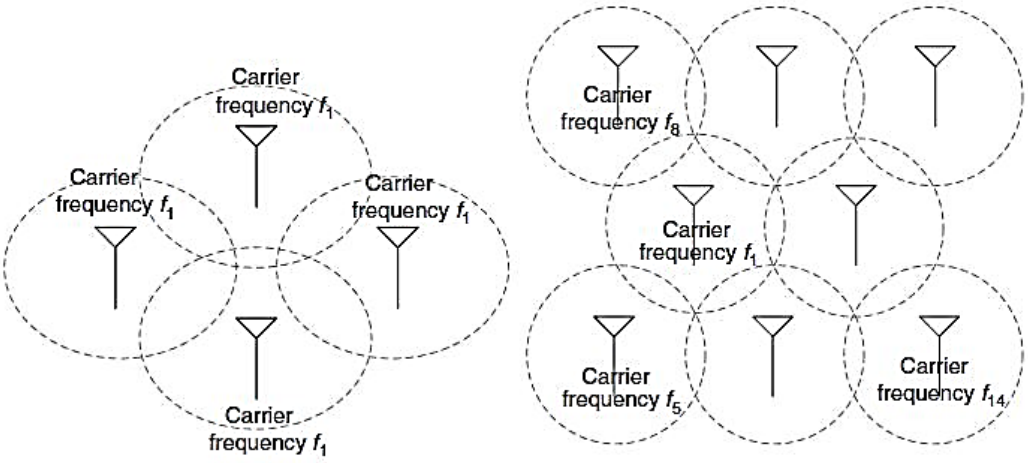


Figure 13: Single-Frequency and Multi-Frequency Network [32]

In a classical parallel-data system, the total signal frequency band is divided into N non-overlapping frequency subchannels. Each subchannel is modulated with a separate symbol, and then the N subchannels are frequency multiplexed. It seems good to avoid spectral overlap of channels to eliminate interchannel interference. However, this leads to inefficient use of the available spectrum [37]. With OFDM technique, use of band becomes efficient.

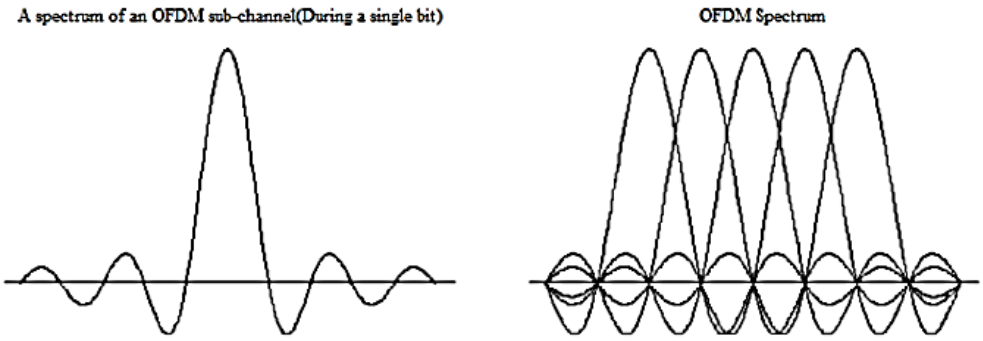


Figure 14: OFDM Spectrum [38]

	DAB				DVB-T		802.11a/g	802.16e-OFDM	3GPP-LTE EUTRA					
Carrier Frequency (GHz)	≤0.375	≤1.5	≤1.5	≤3	0.4 ~ 0.8		2.5, 5.8	2-11	2					
Sample Frequency (MHz)	2				6.8, 8, 9.14		20	8/7*B, 7/6*B	1.92	3.84	7.68	15.36	23.04	30.72
Bandwidth (MHz)	1.5				6, 7, 8		20	1.5~28	1.25	2.5	5	10	15	20
FFT Size	2048	1024	512	256	8192	2048	64	256	128	256	512	1024	1536	2048
Used Subcarriers	1536	768	384	192	6817	1705	52	200	76	151	301	601	901	1201
Guardband Ratio	0.25				0.1678	0.1675	0.1875	0.2185	0.41					
Subcarrier Spacing (KHz)	1	2	4	8	1.116[1]	4.464[1]	312.5	125[2]	15					
FFT Period (μs)	1000	500	250	125	896[1]	224[1]	3.2	8[2]	66.7					
Guard Interval (μs)	246	123	62	31	224, 112, 56, 28[1]	56, 28, 14, 7[1]	0.8	2, 1, 0.5, 0.25[2]	4.67, 16.67					
Guard Interval Ratio	1/4				1/4, 1/8, 1/16, 1/32		1/4	1/4, 1/8, 1/16, 1/32	9/128, 1/4					
Constellation	DQPSK				QPSK, 16-QAM, 64-QAM		BPSK, QPSK, 16-QAM, 64-QAM	BPSK, QPSK, 16-QAM, 64-QAM	QPSK, 16-QAM, 64-QAM					
Maximum Data Rate (bps)	1.8M				31.67M[1]		54M	104.7M[2]	> 100M[3]					

[1]: For a 8-MHz channel [2]: For a 28-MHz channel [3]: For a 20-MHz channel

Figure 15: System Parameters of Several Wireless Communication Standards using the OFDM Technology

The OFDM transmission has the following **advantages**:

• OFDM is an efficient way to deal with multipath; for a given delay spread, the usage complexity is essentially lower than that of a single-carrier system with an equalizer,

• In relatively slow time-varying channels, it is possible to enhance capacity significantly by adapting the data rate per SC according to the signal-to-noise ratio (SNR) of that particular SC,

• OFDM is robust against narrowband interference because such interference affects only a small percentage of the SCs,

• OFDM makes single-frequency networks possible, which is especially attractive for broadcasting applications [37].

On the other hand, OFDM also has some **drawbacks** compared with single carrier modulation:

• OFDM is more sensitive to frequency offset and phase noise,

• OFDM has a relatively large peak-to-average-power ratio, which tends to diminish the power efficiency of the radio frequency RF amplifier [37].

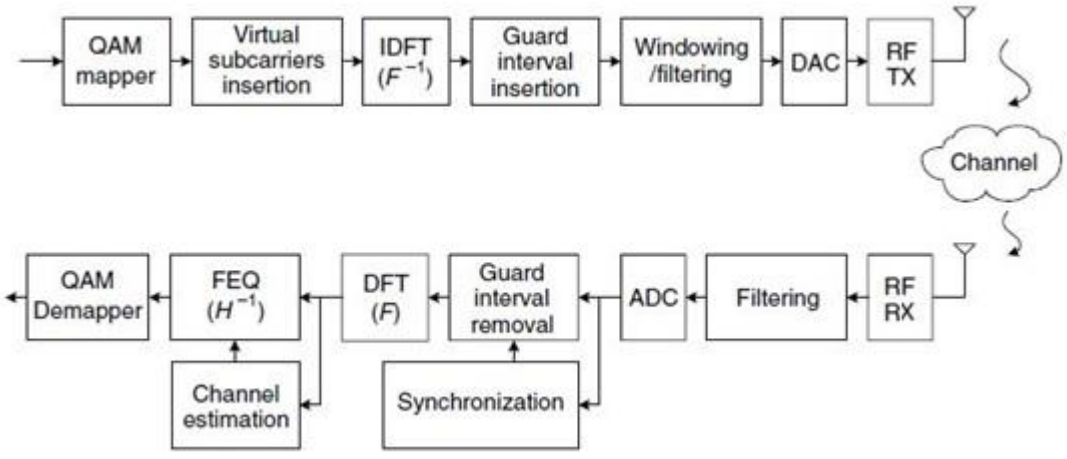


Figure 16: OFDM Transceiver Architecture for QAM [32]

In Figure, on transmitter side, the message bits into a sequence of PSK or QAM symbols are mapped by OFDM transmitter. They will be subsequently converted into N parallel streams. Each of N symbols are carried out by the different subcarrier. This situation is also similar on the receiver side, and we can only think of reverse.

There are a lot of parameter to develop OFDM system, and these parameters are detailed below step-by-step.

3.2. Orthogonality

In OFDM, all of subscribers are chosen orthogonal each other. Orthogonal is another word for perpendicular. It means that subcarriers are perpendicular in a mathematical sense, allowing the spectrum of each sub-channel to overlap another without interfering with it. The subcarriers are closely spaced and are modulated with low data rates. With orthogonal procedure, sub-channels can be prevented from undesired effects of channels as a crosstalk. Moreover, we can say that the orthogonality technique simplifies the design both the transmitter and receiver sides.

Time-limited complex exponential signals:

$$\{e^{j2\pi f_k}\}_{k=0}^{N-1}$$

Different subcarriers frequencies:

$$f_{k=\frac{k}{T_{sym}}}$$

To make a decision of orthogonality, the integral of their products should equal to zero:

$$\frac{1}{T_{sym}}\int_0^{T_{sym}} e^{j2\pi f_k t}\, e^{-j2\pi f_i t}\, dt = \frac{1}{T_{sym}}\int_0^{T_{sym}} e^{j2\pi\frac{k}{T_{sym}}t}\, e^{-j2\pi\frac{k}{T_{sym}}t}\, dt$$

$$= \frac{1}{T_{sym}}\int_0^{T_{sym}} e^{j2\pi\frac{(k-i)}{T_{sym}}t}\, dt$$

$$= \begin{cases} 1, & k=i \\ 0, & otherwise \end{cases}$$

For discrete systems, equation becomes;

$$t = nT_s = nT_{sym} = \frac{nT_{sym}}{N}, \qquad n = 0,1,2, \dots \ , N-1.$$

Now, equation can be written in the discrete time domain:

$$\frac{1}{N}\sum_{n=0}^{N-1} e^{j2\pi\frac{k}{T_{sym}}.nT_s} \; e^{-j2\pi\frac{k}{T_{sym}}.nT_s} = \frac{1}{N}\sum_{n=0}^{N-1} e^{j2\pi\frac{k}{T_{sym}}.\frac{nT_{sym}}{N}} \; e^{-j2\pi\frac{k}{T_{sym}}.\frac{nT_{sym}}{N}}$$

$$= \frac{1}{N}\sum_{n=0}^{N-1} e^{j2\pi\frac{(k-i)}{N}.n}$$

$$= \begin{cases} 1, & k = i \\ 0, & otherwise \end{cases}$$

3.3. Concept of FFT and IFFT

Many practical problems in signal analysis involve either infinitely long or very long signals where the Fourier series is not appropriate. For these cases, the Fourier transform (FT) and its inverse (IFT) has been developed. This transform has been used with great success in virtually all quantitative areas of science and technology where the concept of frequency is important. [39]

The Fast Fourier Transform (FFT) and its inverse (IFFT) are very important algorithms in signal processing, software-defined radio, and the most promising modulation technique; Orthogonal Frequency Division Multiplexing (OFDM). The **F**ast **F**ourier **T**ransform (FFT) algorithm has a long history. Its modern discovery is attributed to Cooley and Tukey in 1965. Details can be available from the publication which is 'An Algorithm for the Machine Calculation of Complex Fourier Series (1992)'.

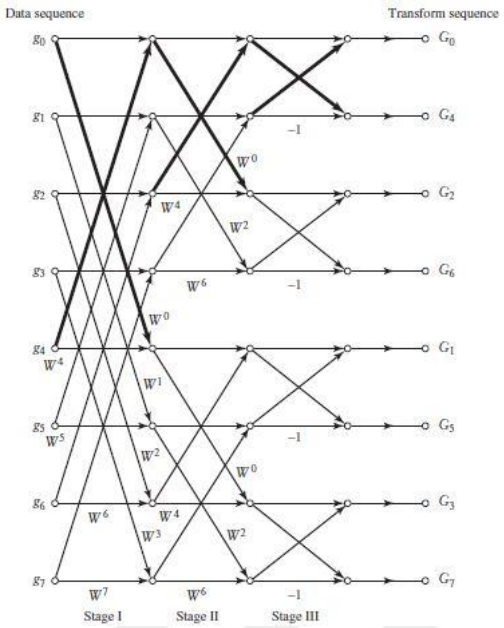


Figure 17: FFT Algorithm for Parallel Data

3.3.1. Discrete Fourier Transform (DFT)

The Discrete Fourier Transform (DFT) is a specific kind of Fourier transform. A French physicist and mathematician, Joseph Fourier, formalized the notion of the spectrum in the early nineteenth century. The Fourier transform of a real-valued or complex function of the real-variable t is defined by

$$\boldsymbol{x(t)} \quad \overset{\boldsymbol{FT}}{\leftrightarrow} \quad \boldsymbol{X(\omega)}$$

$$\boldsymbol{X(\omega) = \int_{-\infty}^{\infty} x(t) e^{-j\omega t}\, dt}$$

In OFDM, Discrete Fourier Transform (DFT) is used for modulating each subchannel onto the appropriate carrier on transceiver side. Before FFT processing modulated digital signals are mapped to particular sub-carrier (serial-to-parallel conversion).

$$\boldsymbol{x_n} \quad \overset{\boldsymbol{DFT}}{\longleftrightarrow} \quad \boldsymbol{X_k}$$

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{-kn}$$

$$= \sum_{n=0}^{N-1} x_n e^{-jk\frac{2\pi}{N}n} \qquad k = 0, \dots, N-1.$$

In the Discrete Fourier transform (DFT), both the input and the output consist of sequences of numbers defined at uniformly spaced points in time and frequency, respectively. [40]

In Simulink, the FFT block computes the fast Fourier transform (FFT) across the first dimension of an N-D input array.

Figure 18: Simulink FFT Block

3.3.2. Inverse Discrete Fourier Transform (IDFT)

In OFDM, before IFFT processing modulated digital signals are mapped to particular sub-carrier (serial-to-parallel conversion). Then, inverse Discrete Fourier Transform (iDFT) are applied;

$$X_k \overset{DTFT}{\longleftrightarrow} x_n$$

$$x_n = \frac{1}{N} \sum_{n=0}^{N-1} X_k W_N^{-kn}$$

In Simulink, The IFFT block computes the inverse fast Fourier transform (IFFT) across the first dimension of an N-D input array.

Figure 19: Simulink IFFT Block

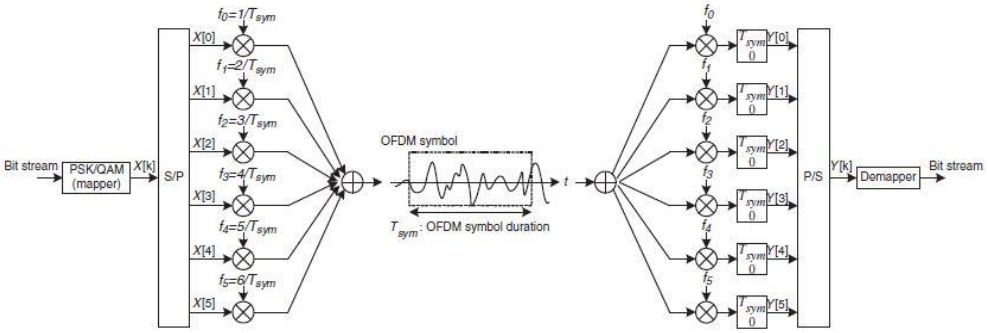


Figure 20: IFFT in Transmitter Side and FFT in Receiver Side

3.4. Serial to Parallel Conversion

The Serial to Parallel step takes a series of inputs of any size and creates a single output of a specified multiple of that size. The input series can be ordered either with the most significant word first or the least significant word first.

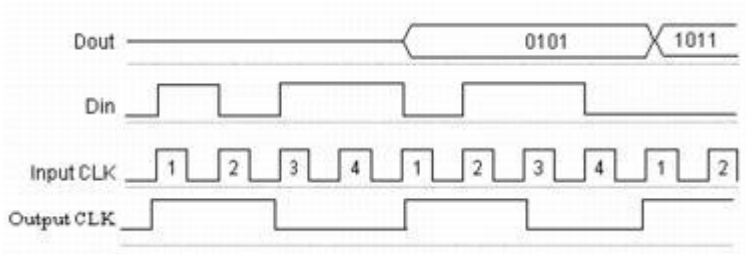


Figure 21: Serial to Parallel Conversion

3.5. Parallel to Serial Conversion

In OFDM, parallel to serial conversion is used for summing all subcarriers and combining them into one signal. Input word is split into N time-multiplexed output words where N is the ratio of number of input bits to output bits. The order of the output can be either least significant bit first or most significant bit first (depends on application).

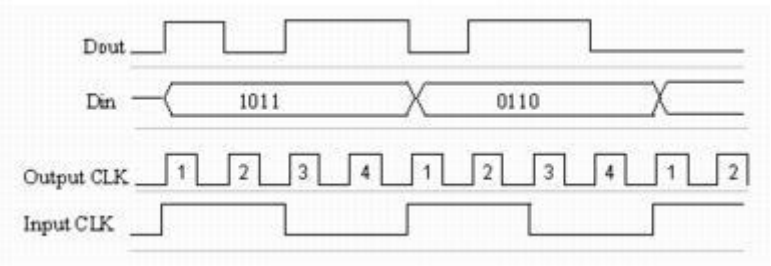


Figure 22: Parallel to Serial Conversion

3.6. Guard Interval / Cyclic Prefix

Usually adding cyclic prefix (CP) has two purposes that are eliminate the inter-symbol interference (lSI) and inter-channel interference (ICI) [41]. The Cyclic Prefix or Guard Interval is a periodic extension of the last part of an OFDM symbol that is added to the front of the symbol in the transmitter, and is removed firstly at the receiver side before demodulation [38].

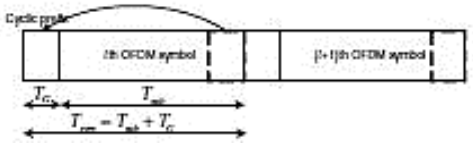


Figure 23: OFDM Symbol with Cyclic Prefix

To preserve the orthogonality of the subcarriers and the independence of subsequent OFDM symbols, Guard Interval (GI) was introduced. The guard interval, a cyclic prefix, is a copy of the last part of the OFDM symbol, which is transmitted before the so-called effective part of the symbol [37]. If cyclic prefix is not inserted in the guard interval, received symbol represents linear convolution and intercarrier interference (ICI) is seen after FFT operation by the receiver [42]. Because of that, after IFFT operation, Cyclic Prefix added.

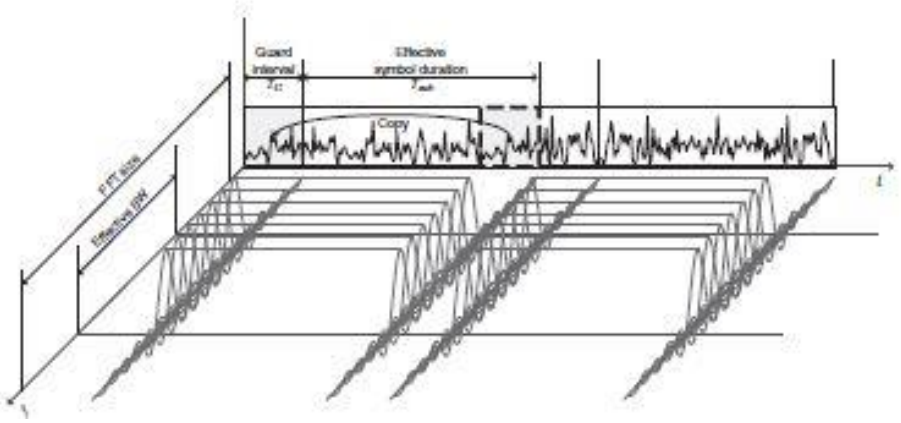


Figure 24: Time / Frequency Domain Description of OFDM Symbols with Cyclic Prefix

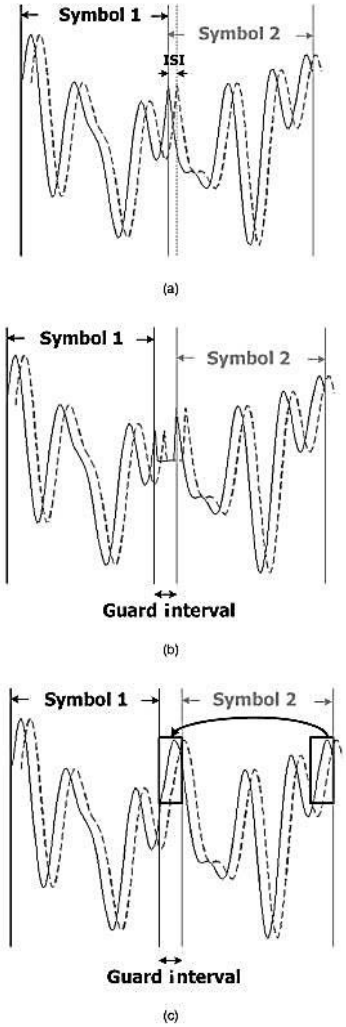


Figure 25: (a) Illustration of ISI due to multipath delay; (b) zero-padding guard interval to avoid ISI; (c) guard interval with cyclic prefix to eliminate ISI and ICI [32]

3.7. Cyclic Suffix

Cyclic suffix (CS) is a cyclic extension of the OFDM system. It is diverse from CP. CS is the copy of the head part of an effective OFDM symbol, and it is inserted at the end of the symbol [43]. With both CP and CS, we can suppress the ISI effect of the multipath channel.

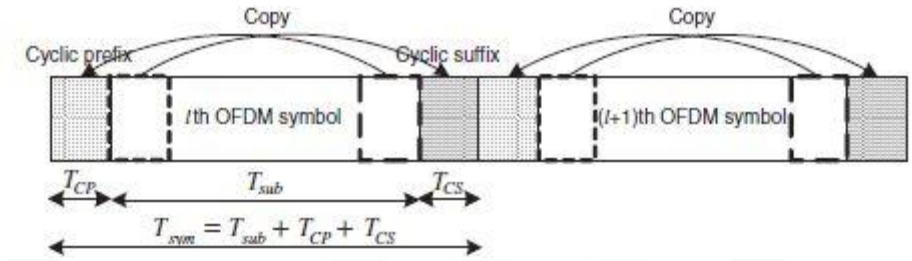


Figure 26: OFDM symbol with both Cyclic Prefix (CP) and Cyclic Suffix (CS) [43]

3.8. Windowing

Due to the side lobes of its FT (Fourier Transform) being a sinc function, a rectangular pulse has a very large bandwidth. For reducing the level of these side lobes windowing is a well-known technique. Also, it reduces the signal power transmitted out of band. During its effective period, signal must not be influced by the applied in an OFDM system.

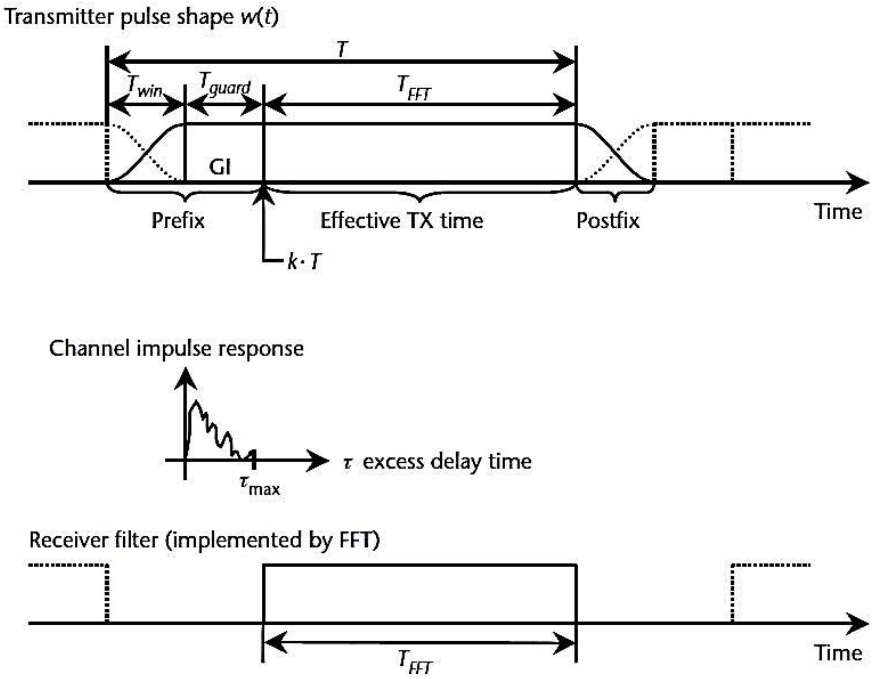


Figure 27: Cyclic Extension and Windowing of the OFDM Symbol

3.9. Channel Models

Between transmitter and receiver, environement can be defined as channel. On channel transmission system are influenced by reflection, refraction and scatter. In theoretical model, there are some methods. In the thesis, AWGN, Rayleigh Fading and Rician Fading were used to model the communication channel.

3.9.1. Additive White Gaussian Noise (AWGN)

Additive White Gaussian Noise is the channel which is one of the simplest mathematical models for various physical communication channels, including wirelines and some radio channels. It is a noise that affects the transmitted signal when it passes through the channel.

3.9.2. Multipath Fading

The term fading, means rapid fluctuations of the amplitudes, phases, or multipath delays of a radio signal. In ideal channel, the transmitted signal passes via the channel and go to the receiver side. In receiver side, the signal is demodulated with a specific algorithm to get representation of the message signal which is transmitted.

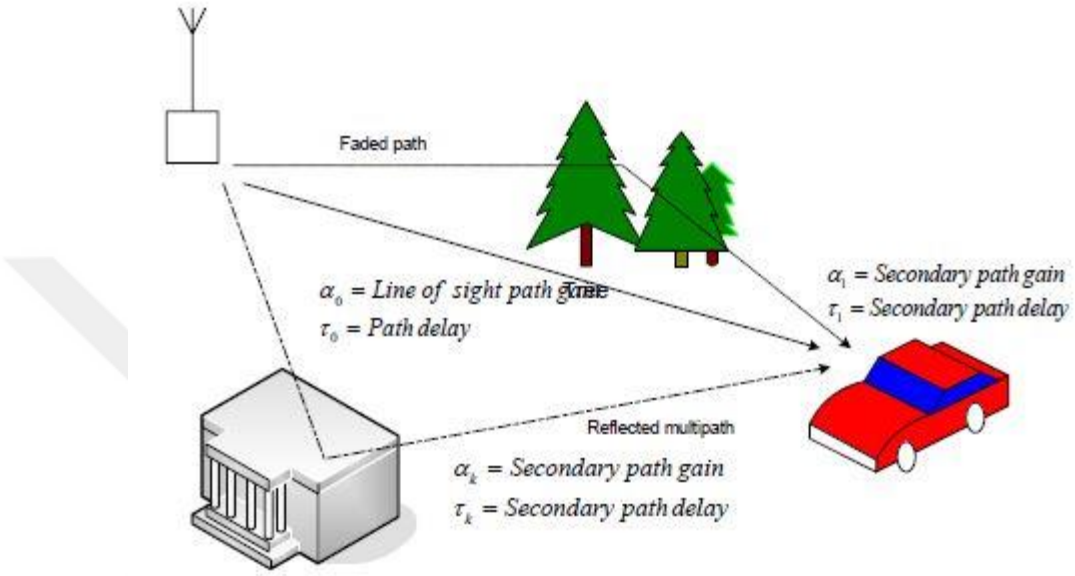


Figure 28: Multipath Fading 1

In practice, this scenario cannot be fully observed especially receiver side. The receiver side, our signal includes of a mixture of reflected, attenuated, diffracted and refracted signals. In OFDM, ISI and multipath fading effects have been minimized by sending data in parallel subcarriers and at a low data rate [44].

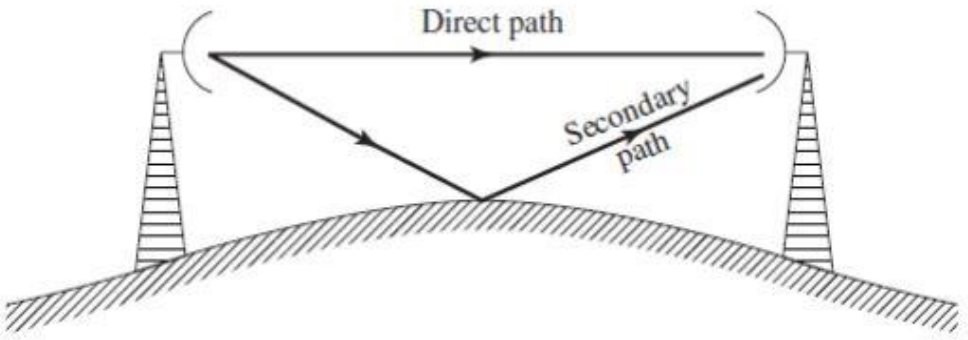


Figure 29: Multipath Fading 2

In wireless telecommunications, multipath is the propagation that results in radio signals reaching the receiving antenna by two or more paths. These paths may be the result of reflections from buildings, mountains or other reflective surfaces including water, etc. that may be adjacent to the main path.

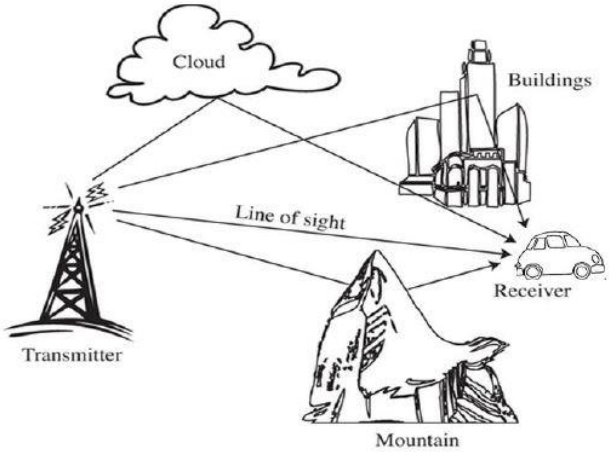


Figure 30: Multipath Propagation Effects

Propagation in a mobile radio channel is determined mainly by its multiple natures. The path from the transmitter side to the receiver side either has also reflections and some of obstructions. Because of the signal reaches the receiver from many different routes, each of these signals has a slightly different delay and gain. The time delays result in phase shifts which added to main signal.

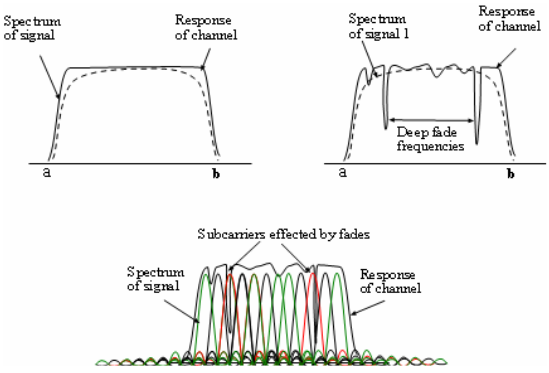


Figure 31: Fading Effect

3.9.2.1.Rayleigh Fading

Rayleigh fading is observed when no LOS, path exists in between transmitter and receiver, but only have indirect path than the resultant signal received at the receiver will be the sum of all the reflected and scattered waves. In other words, where the magnitudes of the signals arriving by the various paths have a distribution known as the Rayleigh distribution, this is known as Rayleigh fading.

3.9.2.2.Rician Fading

Rician Fading occurs when there is a LOS (Line-of-Sight) as well as the non-LOS path in between the transmitter and receiver, i.e. the received signal comprises on both the direct and scattered multipath waves [45].

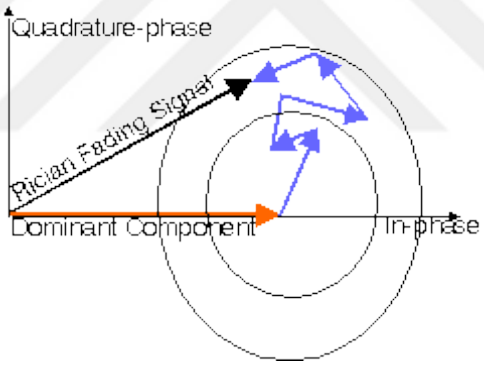


Figure 32: Phasor Diagram of Rician Fading

3.10. Performance of OFDM System

OFDM performance evaluated with those channels in terms of bit-error rates (BERs) and signal-to-noise ratios (SNRs) calculation over AWGN and multipath fading channels.

3.10.1. Bit Error Rate (BER) Measurement

The performance analysis is enable for modern digital communications systems. With the end-to-end performance measurements, our system can become more stable. The measure of that performance is usually Bit Error Rate (BER), which quantifies the reliability of the entire system from "bits in" to "bits out", including the electronics, antennas and signal path in between [46]. In our Simulink model which includes Xilinx blocks and Simulink blocks, BER calculated with native Simulink block which is shoven below.

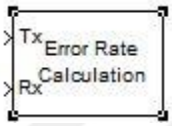


Figure 33: Simulink Error Rate Calculation Block

It compares input data from a transmitter with input data from a receiver, and is calculating the BER.

$$\mathbf{BER} = \frac{\textbf{Bits in Error}}{\textbf{Total bits received}}$$

BER can also be defined in terms of the probability of error (POE or P_e) [30] and expressed generally as

$$\boldsymbol{P_e} = \frac{\mathbf{1}}{\mathbf{2}}(\mathbf{1} - \boldsymbol{erf})\sqrt{\frac{\boldsymbol{E_b}}{\boldsymbol{N_0}}}$$

For M-ary QAM, Bit Error Probability (Probability of Bit Error) becomes:

$$\boldsymbol{P_e} = \frac{\sqrt{\boldsymbol{M}} - \mathbf{1}}{\sqrt{\boldsymbol{M}}\,\mathbf{log_2}\,\sqrt{\boldsymbol{M}}}\;\boldsymbol{erfc}\left(\sqrt{\frac{\mathbf{3}\;\mathbf{log_2}\,\boldsymbol{M}\;\boldsymbol{E_b}}{\mathbf{2}(\boldsymbol{M}-\mathbf{1})\;\boldsymbol{N_0}}}\right)$$

For M=4, equation reduces to the Bit Error Probability of QPSK (for single-carrier):

$$P_e = \frac{1}{2} erfc\left(\sqrt{\frac{E_b}{N_0}}\right)$$

For M-ary QAM with N subchannels, P_e becomes:

$$P_e = \frac{\sqrt{M}-1}{\sqrt{M}\,\log_2\sqrt{M}}\; erfc\left(\sqrt{\frac{\left(2^{\sqrt{N}}-1\right)}{2^{\sqrt{N}-1}}\,\frac{3\,\log_2 M\;E_b}{2\,(M-1)\,N_0}}\right)$$

For M=4 (QPSK), equation becomes, P_e becomes:

$$P_e = \frac{1}{2}\; erfc\left(\sqrt{\frac{\left(2^{\sqrt{N}}-1\right)}{2^{\sqrt{N}-1}}\,\frac{E_b}{N_0}}\right)$$

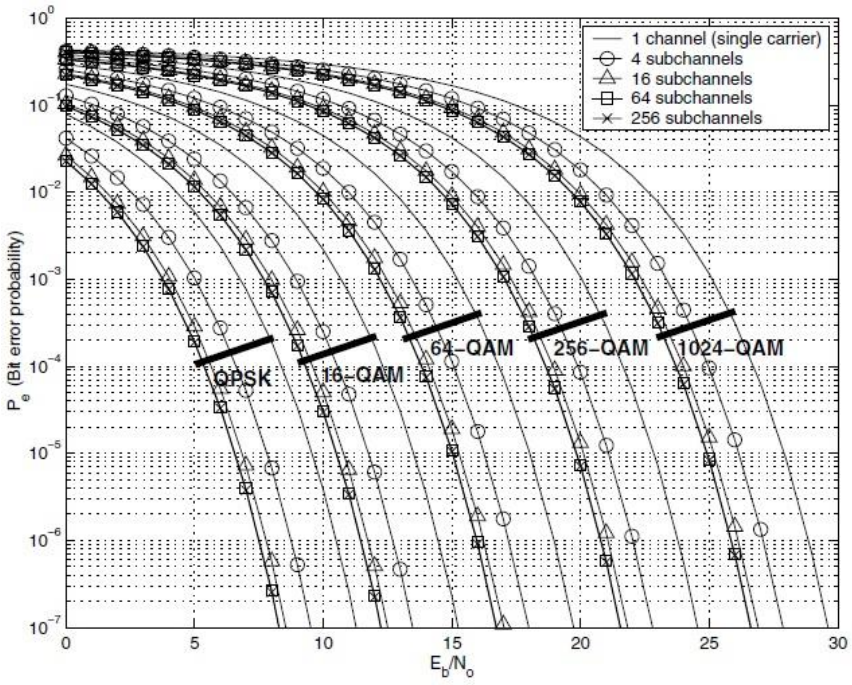


Figure 34: Theoretical Bit Error Probability vs. E_b/N_0 for M-QAM-N

3.10.2. Signal to Noise Ratio (SNR)

SNR is the ratio of the received signal to the noise in the frequency range. SNR is inversely related to BER, that is high BER causes low SNR.

$$\boldsymbol{SNR = \frac{Signal\ Power}{Noise\ Power} = \left(\frac{F_s}{B}\right)\left(\frac{E_s}{N_0}\right) = N_b\left(\frac{F_s}{B}\right)\left(\frac{E_b}{N_0}\right)}$$

F_s: Symbol rate (1/sec)

B: Bandwidth (Hz = 1/sec) ≥ F_s

N_0: Noise power spectral density

E_s: Energy per symbol (Joule)

E_b: Energy per bit (Joule)

N_b: Bit per symbol

CHAPTER 4. FPGAs & DIGILIENT'S GENESYS VIRTEX-5 DEVELOPLMENT BOARD

Todays, field programmable gate arrays (FPGAs) are using many areas which ares Aerospace, Medical, Automotive, Broadcast, Consumer Electronics, Industrial, Digital Signal Processing, Communication. Although there are many produces of FPGAs, two companies which are Xilinx and Intel (Altera) taking on this role more. They are two major manufacturers which are Xilinx and Intel (Altera).

In communication systems, DSPs and FPGAs are using generally. Reasons of for preference ofFPGAs are their high performance data processing ability. DSP performance is derived from the FPGA's ability to construct highly parallel architectures for processing data. In contrast with a microprocessor or DSP processor, where performance is tied to the clock rate at which the processor can run, FPGA performance is tied to the amount of parallelism that can be brought to bear in the algorithms that make up a signal processing system.[47]

In our thesis, developed model was impelemented on Digilent's Genesys Virtex-5 (Xilinx) FPGA board.

4.1. Digilent Genesys™ Virtex-5 FPGA Development Board

The Genesys circuit board is a complete, ready-to-use digital circuit development platform based on a Xilinx Virtex-5 LX50T. The large on-board collection of high-end peripherals, including Gbit Ethernet, HDMI Video, 64-bit DDR2 memory array, and audio and USB ports make the Genesys board an ideal host for complete digital systems, including embedded processor designs based on Xilinx's MicroBlaze. [48]

Figure 35: Digilent's Genesys Virtex-5 FPGA Development Board

4.2. Digilent Genesys™ Virtex-5 FPGA Development Board Feature

- Xilinx Virtex 5 LX50T FPGA, 1136-pin BGA package,
- 256Mbyte DDR2 SODIMM with 64-bit wide data,
- 10/100/1000 Ethernet PHY and RS-232 serial port,
- Multiple USB2 ports for programming, data, and hosting,
- HDMI video up to 1600x1200 and 24-bit color,
- AC-97 Codec with line-in, line-out, mic, and headphone,
- Real-time power monitors on all power rails,
- 16Mbyte StrataFlash™ for configuration and data storage,
- Programmable clocks up to 400MHz,
- 112 I/O's routed to expansion connectors,
- GPIO includes eight LEDs, two buttons, two-axis navigation switch, eight slide switches and a 16x2 character LCD.

4.3. Board Configuration

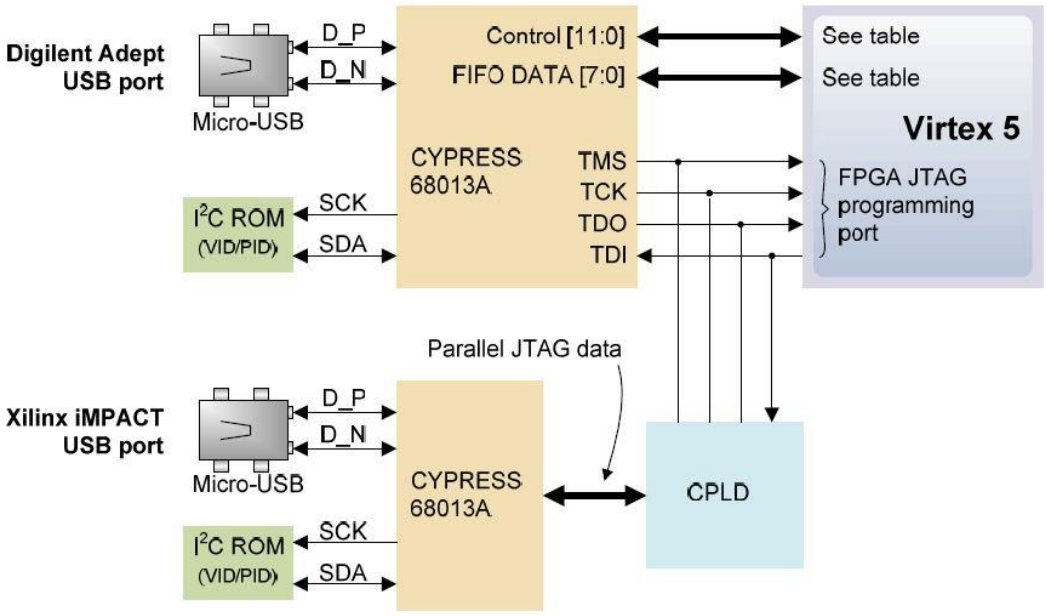


Figure 36: Board Programming Configuration

4.4. Adept System

The Digilent Adept System is a collection of application programs, runtime libraries and drivers that allow users to interact programmatically with various Digilent products. The Digilent Adept Runtime contains the shared libraries and drivers that support the applications programs, and the Digilent Adept SDK provides the link libraries and documentation needed to write applications programs to work with the Adept System [49].

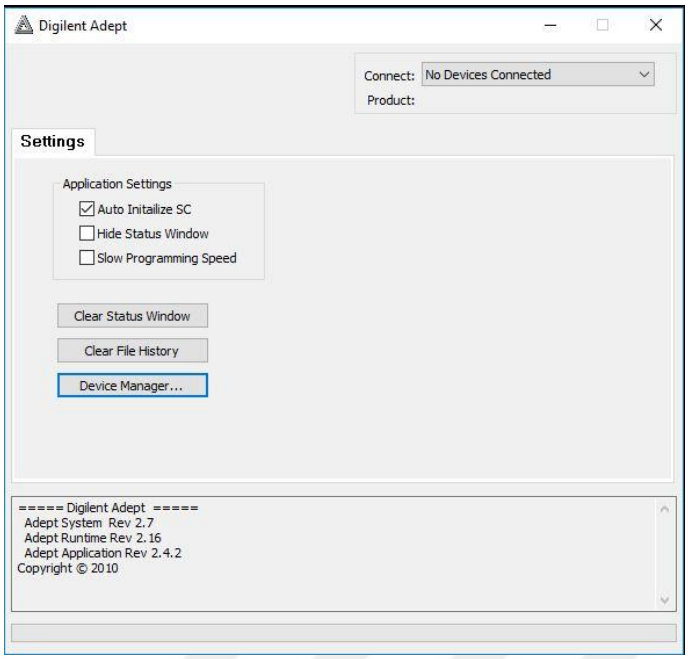


Figure 37: Adept Screen before Connection is Established

The Genesys board includes two USB peripheral ports – one for Adept software and another for Xilinx's iMPACT software. Either port can program the FPGA and StrataFlash, but Adept offers a simplified user interface and many additional features such as automated board test and user-data transfers. The Adept port is also compatible with iMPACT, if the Digilent Plug-In for Xilinx Tools is installed on the host PC (download it free from the Digilent website). [48]

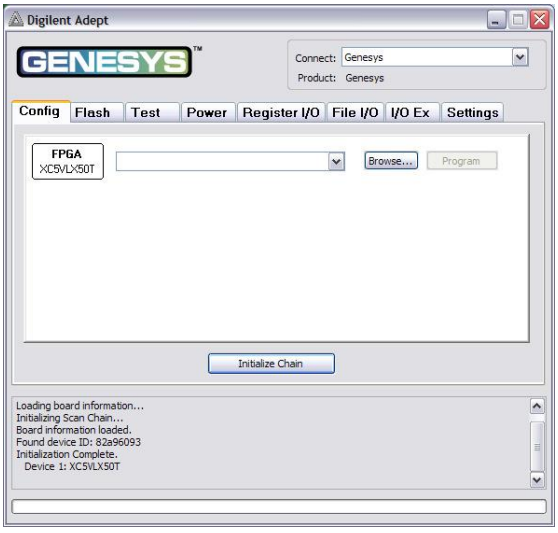


Figure 38: Adept Screen after Connection is Established

Adept's can be used fort o run automated board tests for our board. From Digilent USB2 interface, connection is possible between PC and the device. Adept automatically recognizes the Genesys board and presents a graphical interface with tabs for each of these applications [48].

With this interface, we can verify that our board works. After connection with cable via USB port, we can check on board 256Mbyte DDR2 RAM, flash memories, short circuits, 16 slide switches and 16 push buttons.

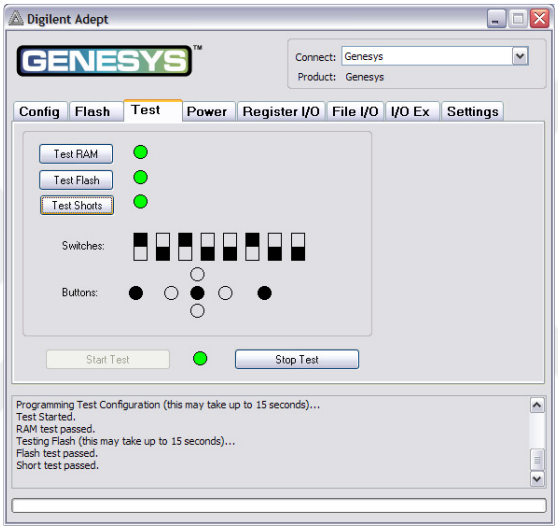


Figure 39: Adept Test Window

CHAPTER 5. MATHWORKS' MATLAB/SIMULINK AND XILINX'S SYSTEM GENERATOR FOR DSP

Large-scale systems are all around and exist in diverse fields such as complex chemical processes, biomedical systems, social economic systems, transportation systems, ecological systems, electrical systems, mechanical systems, and aeronautical and astronautics systems[50]. With conventional techniques, all these large and complex systems are difficult to model. Hence, these systems can be decoupled or partitioned into suitable numbers of interconnected subsystems to reduce their complexity for modeling purposes [50]. Similar to mentioned purposes above, MATLAB (R2012a) environment was selected to develop all of models in thesis.

5.1. MathWorks' MATLAB/Simulink

MATLAB which developed by MathWorks is the software. Users can analyze data, can develop algorithms and can create mathematical models. It offers a wide range of usage areas. For analyze digital signals, MATLAB is a most handy tool.

Simulink also developed by MathWorks and integrated with MATLAB. It is graphical programming software which offers system-level design, simulation, automatic code generation, and continuous test and verification of embedded systems. It also supports model-based hardware design using system generator (Xilinx). In thesis, it used for model-based FPGA design.

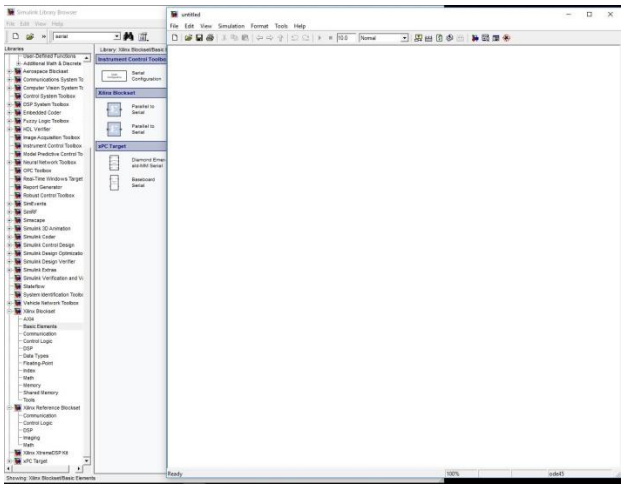


Figure 40: MATLAB - Simulink and Its Blockset Screen

5.2. Xilinx ISE Design Suite and System Generator

Xilinx is one of Technology Company which is an American origin. This company has Xilinx ISE Design Suite is Xilinx's software development environment. It offers a comprehensive set of familiar and powerful tools, libraries and methodologies. To design model-based FPGA, Xilinx ISE Design Suite should be installed to user PC. During installation of Xilinx ISE Design Suite, there are options which depend on what you want from software. To install System Generator, Vivado System Edition option should be chosen during installation of Xilinx ISE Design Suite. To design model-based FPGA from MATLAB/Simulink, development environment which can be Linux or Windows should include System Generator. System generator is a DSP design tool from Xilinx that enables the use of Mathworks Model-Based Simulink for FPGA design.

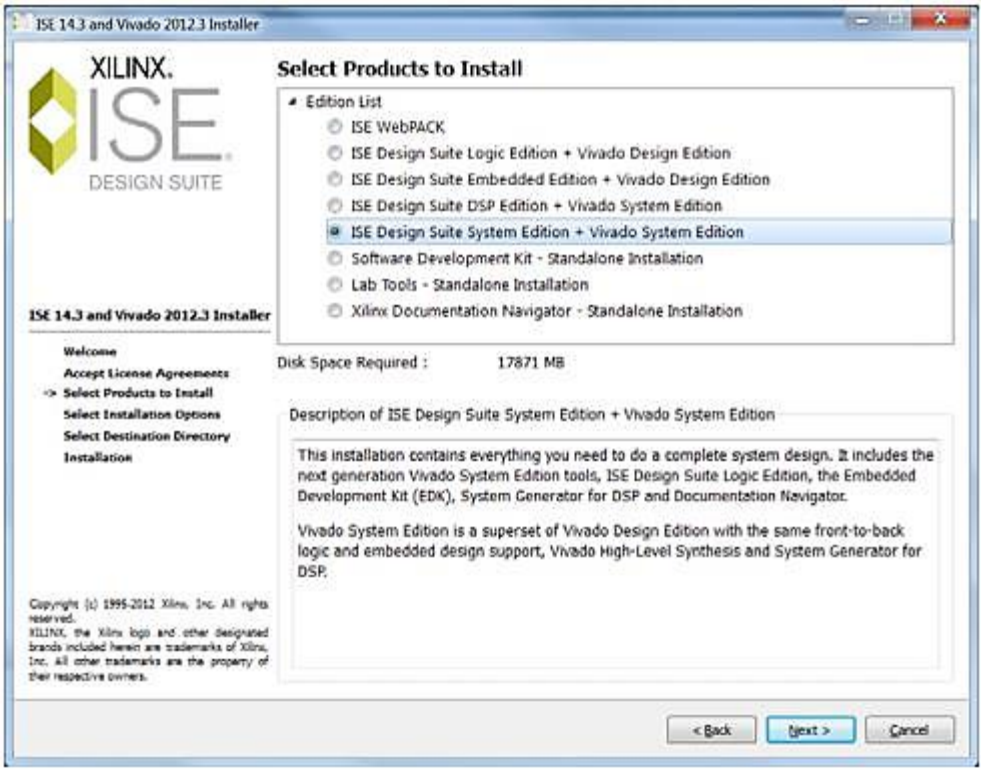


Figure 41: Xilinx ISE Design Suite Installation Screen

Xilinx System Generator that facilitates FPGA hardware design pioneered the idea of compiling an FPGA program from MATLAB and Simulink model. It provides system modeling and automatic code generation from MATLAB and Simulink. During the design of Simulink model, system generator blocksets can be used like other Simulink blocksets. Moreover, designer can also use both Simulink native blocks and Xilinx System Generator blocks at the same time. The blocks provide abstractions of mathematical, logic, memory, and DSP functions that can be used to build sophisticated signal processing systems [47]. User can design hardware using these System Generator Blocks.

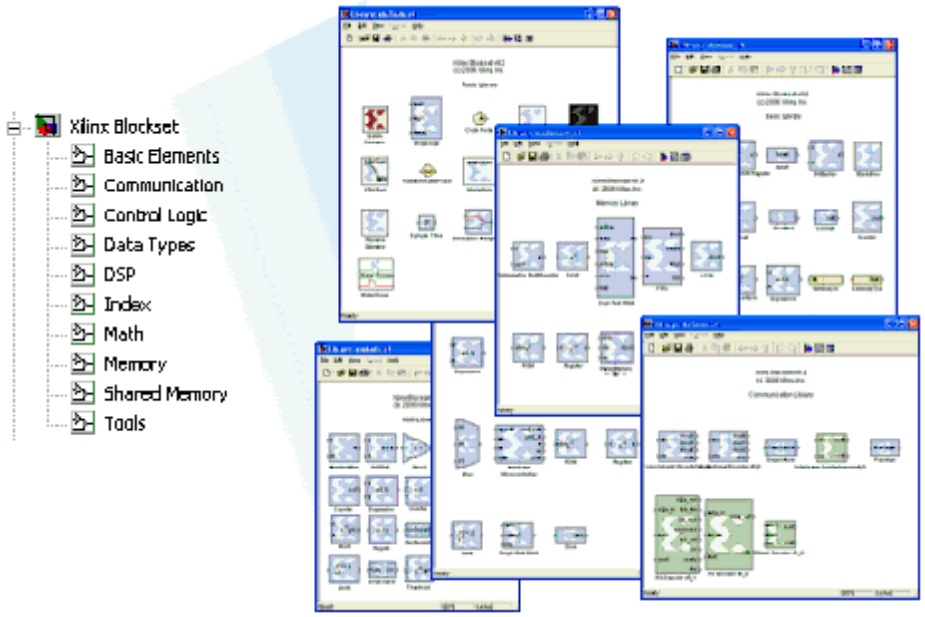


Figure 42: Simulink System Generator Blocksets [47]

Xilinx FPGAs or RTL design methodologies are not required when using System Generator. Designs are captured in the Simulink modeling environment using a Xilinx-specific block set. All of the downstream FPGA implementation steps including RTL synthesis and Place and Route are automatically performed to produce an FPGA programming bitstream. [51]

5.3. MATLAB/Simulink & System Generator Configuration

In this thesis, Xilinx's FPGA which is Virtex-5 were used as said before. To design model-based FPGA, Mathworks' Simulink environment was used with System Generator blocks. Used software to design hardware should be selected with suitable versions. Installing exact versions of software is one the most important step of taking a short lead. With the wrong versions of Xilinx ISE Design Suite and MATLAB, designing can be incomprehensible. They must also be compatible with the hardware to be used. As mentioned, Genesys Virtex-5 development board was used as hardware; for software Xilinx ISE Design Suite 14.2 and MATLAB 2012a were used. To configure Xilinx ISE Design Suite and Matlab softwares, MATLAB should be

installed first, and then Xilinx ISE Design Suite should be installed. During installing Xilinx ISE Design Suite, from configuration window which is 'Select a MATLAB installation for System Generator', actual MATLAB version must be selected, and then configuration can be completed.

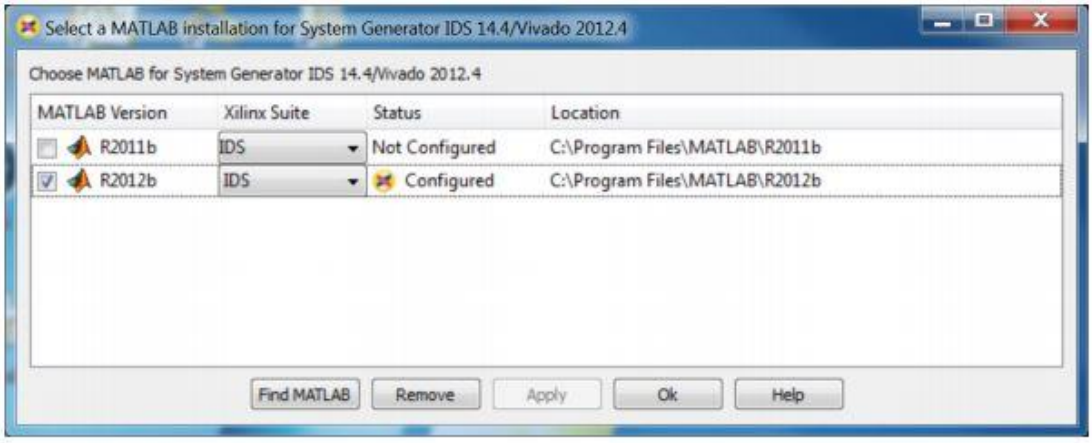


Figure 43: MATLAB Configuration Window of System Generator

5.4. Xilinx Blocksets

5.4.1. Organization of Blockset Libraries

There are 12 different types of libraries.

Library	Description
Index	Every block includes index in the Xilinx Blockset.
AXI4 Blocks	This library Includes every block the supports tjhe AXI4 Interface.
Basic Element Blocks	This library includes standard building blocks for digital logic.

Communication Blocks	This library commonly used in digital communications systems. Communication Blocks library includes forward error correction and modulator blocks.
Control Logic Blocks	This library includes blocks for control circuitry and state machines.
Data Type Blocks	This library includes blocks that convert data types (includes gateways).
DSP Blocks	This library includes Digital Signal Processing (DSP) blocks.
Floating-Point Blocks	This library includes blocks that support the Floating-Point data type as well as other data types. Only a single data type is supported at a time. For example, a floating-point input produces a floating-point output; a fixed-point input produces a fixed-point output.
Index Blocks	This library includes All System Generator blocks.
Math Blocks	This library includes blocks that implement mathematical functions.
Memory Blocks	This library includes blocks that implement and access memories.
Shared Memory Blocks	This library includes blocks that implement and access Xilinx shared memories.
Tool Blocks	This library includes “Utility” blocks.

Table 1: Organization of Blockset Libraries of Xilinx [52]

5.4.2. Used Xilinx System Generator Blocks

- Constant

The Xilinx Constant block generates a constant values. These values can be a fixed-point value, a boolean value, or a DSP48 instruction. If we compare with Simulink constant block, it is similar to the this block, but can be used to directly drive the inputs [52].

Figure 44: Xilinx System Generator - Constant Block Symbol

- Convert

With the Xilinx convert block, each input sample can be convertable to a number of a desired arithmetic type [52].

Figure 45: Xilinx System Generator - Convert Block Symbol

- Counter

The Xilinx Counter block implements a free running or count-limited type of an up, down, or up/down counter. [52].

Figure 46: Xilinx System Generator - Counter Block Symbol

- Delay

Wtih the Xilinx Delay block, developer can implements a fixed delay [52].

Figure 47: Xilinx System Generator - Delay Block Symbol

- Down Sample

With the Xilinx Down Sample block, designer can reduces the sample rate of design. [52].

Figure 48: Xilinx System Generator - Down Sample Block Symbol

- Gateway In

With the Xilinx Gateway In blocks, data which produced by System Generator blocks can be input for your Simulink design. [52].

Figure 49: Xilinx System Generator - Gateway In Block Symbol

- Gateway Out

Xilinx Gateway Out blocks are the outputs from the Xilinx portion of your Simulink design. This block converts the System Generator fixed-point or floating-point data type into a Simulink integer, single, double or fixed-point data type [52].

Figure 50: Xilinx System Generator - Gateway Out Block Symbol

- LFSR

Linear Feedback Shift Register (LFSR) block supports both the Galois and Fibonacci structures. LFSR blocks are using either the XOR or XNOR gates [52].

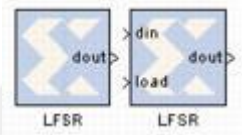


Figure 51: Xilinx System Generator - LFSR Block Symbol

- Serial to Parallel

Serial to Parallel block can take a series of inputs of any size. This block can create multiple outputs from the single input. [52].

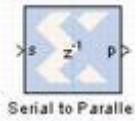


Figure 52: Xilinx System Generator - Serial to Parallel Block Symbol

- Parallel to Serial

The Parallel to Serial block can the parallel input words. With this block, input can split into N time-multiplexed outputs. N is the ratio of number of input bits to output bits [52].

Figure 53: Xilinx System Generator - Parallel to Serial Block Symbol

- Register

The Xilinx Register block models a D flip-flop-based register, having latency of one sample period [52].

Figure 54: Xilinx System Generator – Register Block Symbol

- System Generator

The System Generator token serves as a control panel for controling system and simulation parameters. It's also used for code generation. Every Simulink model which is containing Xilinx Blockset must contain System Generator block. [52].

Figure 55: Xilinx System Generator Block Symbol

- Time Division Demultiplexer

The Xilinx Time Division Demultiplexer block's input should be serial. This block can convert input to multiple outputs at a slower rate [52].

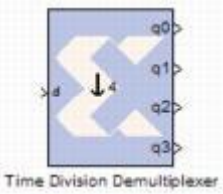


Figure 56: Xilinx System Generator - Time Division Demultiplexer Block Symbol

- Time Division Multiplexer

The Xilinx Time Division Multiplexer block can multiplex the inputs' values into a single faster rate output stream [52].

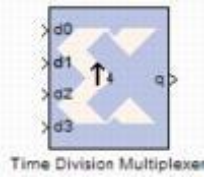


Figure 57: Xilinx System Generator - Time Division Multiplexer Block Symbol

- Up Sample

To increase the sample rate, the Xilinx Up Sample block can be usable.. The output period becomes (input period/n) [52].

Figure 58: Xilinx System Generator - Up Sample Block Symbol

- MCode

To use user-supplied MATLAB function within the model, the Xilinx MCode block can be usable. A parameter of the block name should be same with the M-function name. During a Simulink simulation, this block can executes the user-defined M-code to calculate its outputs. Moreover, user-defined code can be translated into VHDL or Vegilog codes when hardware is generated [52].

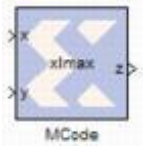


Figure 59: Xilinx System Generator - Mcode Block Symbol

- ROM

Read-only memory (ROM) is Xilinx ROM block which is a single port [52].

Figure 60: Xilinx System Generator - ROM Block Symbol

- Fast Fourier Transform 7.1

The Xilinx Fast Fourier Transform 7.1 block can be used for Discrete Fourier Transform (DFT) or Inverse Discrete Fourier Transform. Moreover, this block has option to add Cyclic Prefix to transformed data [52].

Figure 61: Xilinx System Generator - Fast Fourier Transform 7.1 Block Symbol

- AddSub

The Xilinx AddSub block can be used as an adder or a subtractor. The operation should be Addition or Subtraction [52].

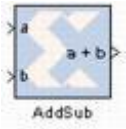


Figure 62: Xilinx System Generator - AddSub Block Symbol

- CMult

The Xilinx CMult block implements a gain operator.With this block, input gained by a constant value [52].

Figure 63: Xilinx System Generator - Cmult Block Symbol

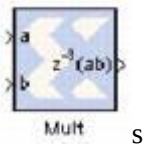
- Delay

With the Xilinx Delay block, designer can implement a fixed delay of specific cycles [52].

Figure 64: Xilinx System Generator - Delay Block Symbol

- Mult

The Xilinx Mult block computes the product of the data on its two input ports [52].



s

Figure 65: Xilinx System Generator - Mult Block Symbol

- WaveScope

Wtih the System Generator WaveScope block, designer can see a powerful and easy-to-use waveforms. Moreover, designer can make debug processes with this block[52].

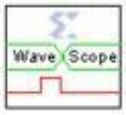


Figure 66: Xilinx System Generator - WaveScope Block Symbol

5.4.3. Used Simulink Blocks

- Terminator

This block terminates unconnected output port.

Figure 67: Simulink - Terminator Block Symbol

- Inport

This block creates input port for subsystem or external input.

Figure 68: Simulink - Inport Block Symbol

- Outport

This block creates output port for subsystem or external output.

Figure 69: Simulink - Outport Block Symbol

- Scope and Floating Scope

This block displays signals generated during simulation.

Figure 70: Simulink - Scope and Floating Scope Block Symbol

- Real-Imag to Complex

This block converts real and/or imaginary inputs to complex signal.

Figure 71: Simulink - Real-Imag to Complex Block Symbol

- To Workspace

This block Writes data to MATLAB workspace.

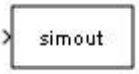


Figure 72: Simulink - To Workspace Block Symbol

- Discrete Time Scatter Plot Scope

This block displays in-phase and quadrature components of modulated signal constellation.

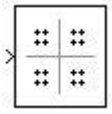


Figure 73: Simulink - Discrete Time Scatter Plot Scope Block Symbol

- Error Rate Calculation

This block computes bit error rate or symbol error rate of input data.

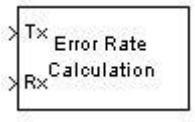


Figure 74: Simulink - Error Rate Calculation Block Symbol

- Display

This block shows value of input.

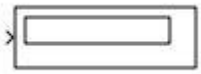


Figure 75: Simulink - Display Block Symbol

5.4.4. Conversion of Simulink Model for Target Board

After a model prepared with Xilinx blocks is seen to work without errors, conversion can be performed. At this stage, 'System Generator' icon is selected.

System Generator icon is shown below.

Figure 76: System Generator Icon

The pop-up screen is shown below. The 'Compilation' tab is selected from the screen that opens after pressing the system generator icon.

Figure 77: System Generator Configuration Window

Then select 'Hardware Co-Simulation' from Compilation option, after, 'New Compilation Target' is selected. The pop-up screen is shown below. From the displayed screen below, select the FPGA model.

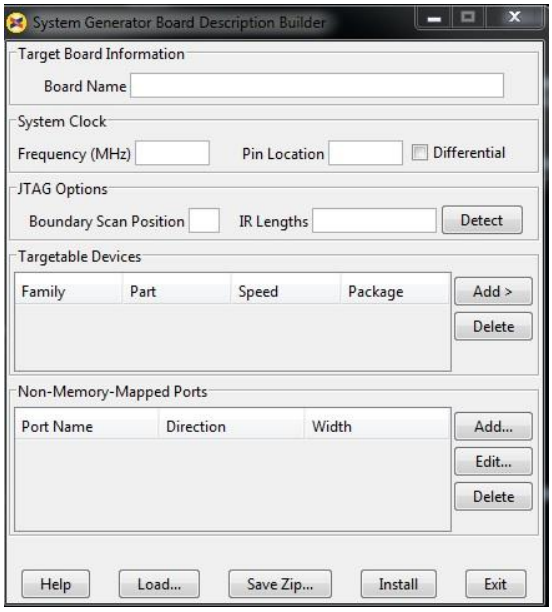


Figure 78: System Generator Board Description Builder Window

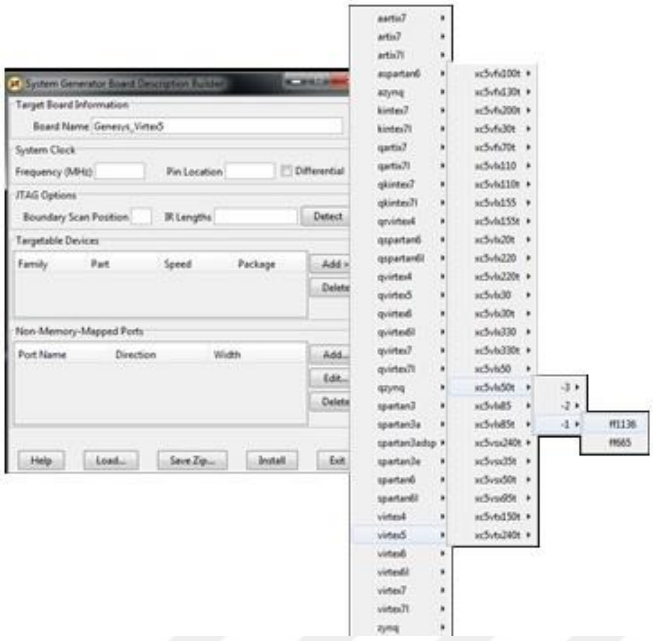


Figure 79: Adding Target FPGA Window

After selecting FPGA model (Virtex-5 > xc5vlx50t > -1 > ff1136), 'Frequency' and 'Pin Location' values should ve entered. The **Frequency** value was set at '100 MHz', and **Pin Location** value was set 'AG18' for Genesys development card which is containing Virtex-5, Then, press the 'Install' button and 'Save Zip…' button.

After the configuration, model file can be converted into FPGA language with the help of system generator. When the run button is pressed, conversion is done automatically.

CHAPTER 6. DESIGN and IMPLEMENTATION of OFDM RECEIVER AND TRANSMITTER ON GENESYS VIRTEX-5 FPGA DEVELOPMENT BOARD

There are two similar modulation schemes which are Quadrature Phase Shift Keying (QPSK) and 4-Quadrature Amplitude Modulation (4QAM). Both are similar in number of information bit transmittable per symbol; meaning these modulation schemes are both capable of conveying 2 bits information per symbol [53]. In OFDM, baseband data on each sub-carrier being independently modulated commonly using some type of Quadrature Amplitude Modulation (QAM) and Quadrature Phase-Shift Keying (QPSK). When the number of M-ary is 4, QAM and QPSK have similar processes. In this thesis, M-ary number accepted as a 4, and QAM & QPSK modulated OFDM is shown with the same model (final model).

The digital modulations which are QPSK and 4QAM are implemented on Simulink with Xilinx ISE 14.2 Design Suite - System Generator. As mentioned previous chapters, the System Generator blocks provide control of system and simulation parameters, and code generation processes. The experimental results were performed using Digilent's Genesys Virtex-5 Development Board and the obtained waveforms is viewed on Simulink.

System Generator blocks and Simulink blocks were used on all of models. First of all, QAM/PSK digital modulation sheme developed on Simulink. Initially, transmitter and receiver sides are developed. After verification for 4QAM and QPSK modulations, OFDM system was designed. For OFDM system, 4QAM modulation was implemented. All of models (systems) and their subsystems are shown with figures below.

6.1. QPSK / 4QAM Modulation Simulink Model

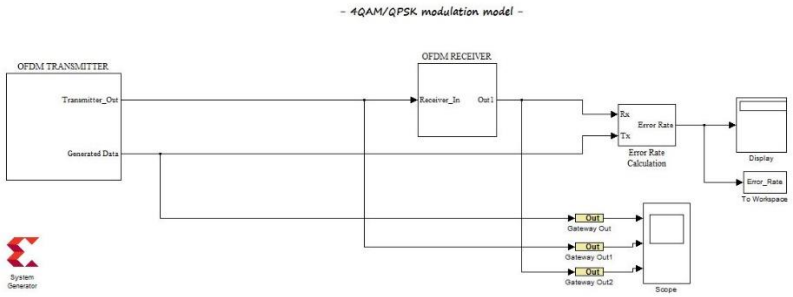


Figure 80: 4QAM & QPSK Modulation Simulink Model without Channel

This model as seen in Figure 80, includes Tranmitter, Receiver and Error Calculation Subsystem. To see the operability of the transmitter and receiver sides, channel did not been added firstly.

6.1.1. QPSK / 4QAM Modulation Simulink Model – Transmitter Side

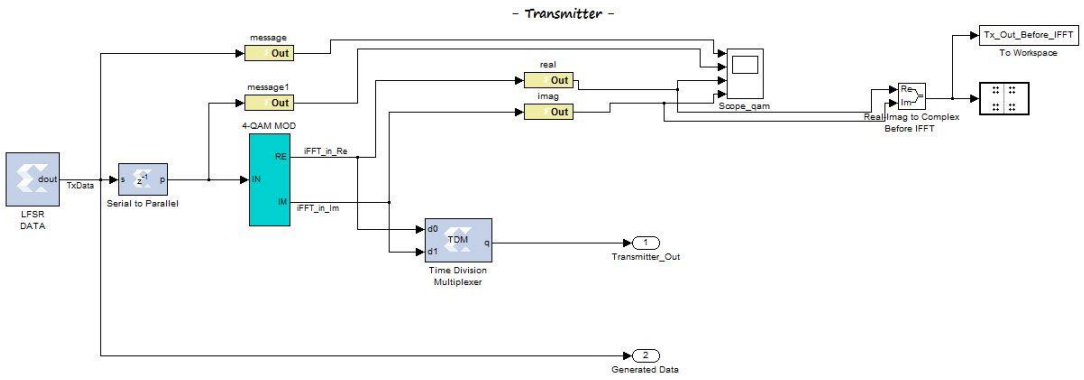


Figure 81: 4QAM & QPSK Modulation Simulink Model – Transmitter Subsystem

Tranmitter subsystem was detailed in Figure 81. On transmitter side, generated data from Xilinx LFSR block paralleled with the Xilinx Serial to Parallel Converter.

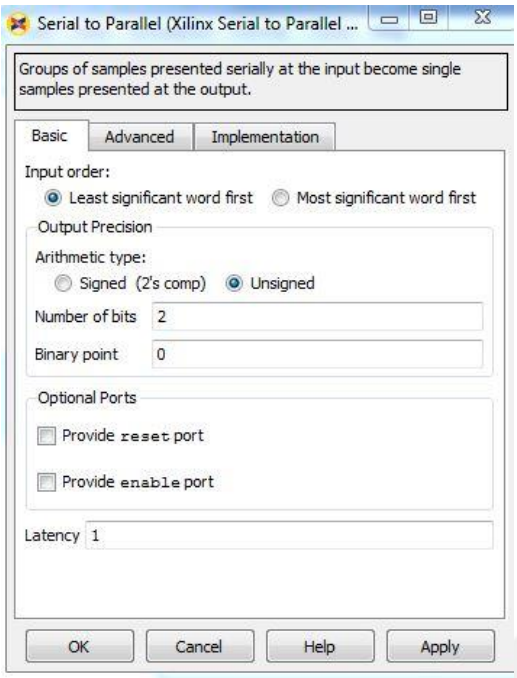


Figure 82: Setting Window Xilinx Serial to Parallel Block

In the Xilinx Serial to Parallel block, The 'Number of Bits' value is selected according to the modulation M-ary number. The 'Number of Bits' can be calculated with $\mathbf{log_2}(\boldsymbol{M-ary\ value})$.

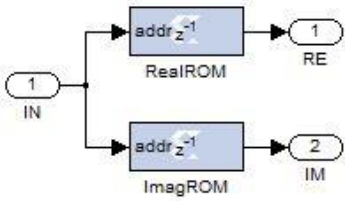


Figure 83: 4-QAM Mapping Subsystem

With 4-QAM MOD Subsystem, paralleled data mapped with the Xilinx ROM block. After mapping process, datas which are I and Q multiplexed with Xilinx Time Division Multiplexer block. The purpose of using TDM is to combine the I and Q data into a single signal. When using QAM modulation, the values in the ROM should be as a Table 2:

Depth	4
Initial Value Vector (Real Part)	$[-1 -1 +1 +1]/\sqrt{2}$
Initial Value Vector (Imaginary Part)	$[+1 -1 +1 -1]/\sqrt{2}$

Table 2: ROM Block Settings for QAM

If the model shown in Figure 81 is to be used for QPSK modulation, the ROM settings in the 4-QAM MOD must be edited.When using QPSK modulation, the values in the ROM should be as a Table 3:

Depth	4
Initial Value Vector (Real Part)	$[+1, 0, -1, 0]$
Initial Value Vector (Imaginary Part)	$[0, +1, 0, -1]$

Table 3: ROM Block Settings for QPSK

After mapping process, generated symbols converted to complex value with the Simulink Real-Imag to Complex block. To display complex values (symbols), Simulink 'Discrete-Time Scatter Plot Scope' was used. In transmitter side, diplayed symbols for 4QAM can be seen in Figure 84.

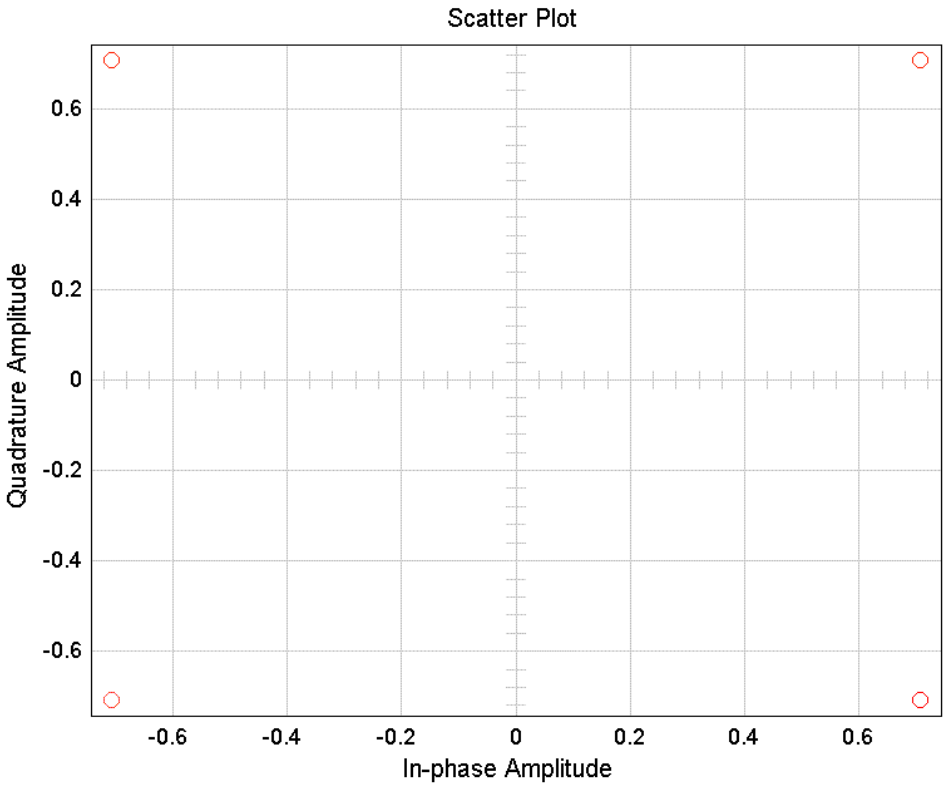


Figure 84: 4QAM Transmitted Symbols

6.1.2. QPSK / 4QAM Modulation Simulink Model – Receiver Side

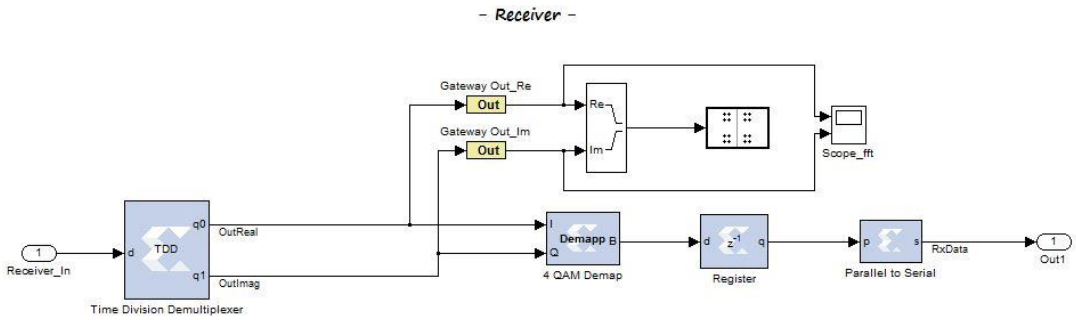


Figure 85: 4QAM & QPSK Modulation Simulink Model – Receiver Subsystem

On receiver side, received data demultiplexed with Xilinx Time Division Demultiplexer block. In the other words, data divided into two data which can called as I and Q signals. After getting I and Q datas, symbols converted to complex value with the Simulink Real-Imag to Complex block. Before converting complex value,

Xilinx Gateway out Block was used to use Xilinx blocks output values which are I and Q with Simulink blocks.To display complex values (symbols), Simulink 'Discrete-Time Scatter Plot Scope' was used. Diplayed symbols in receiver side can be seen in Figure 86.

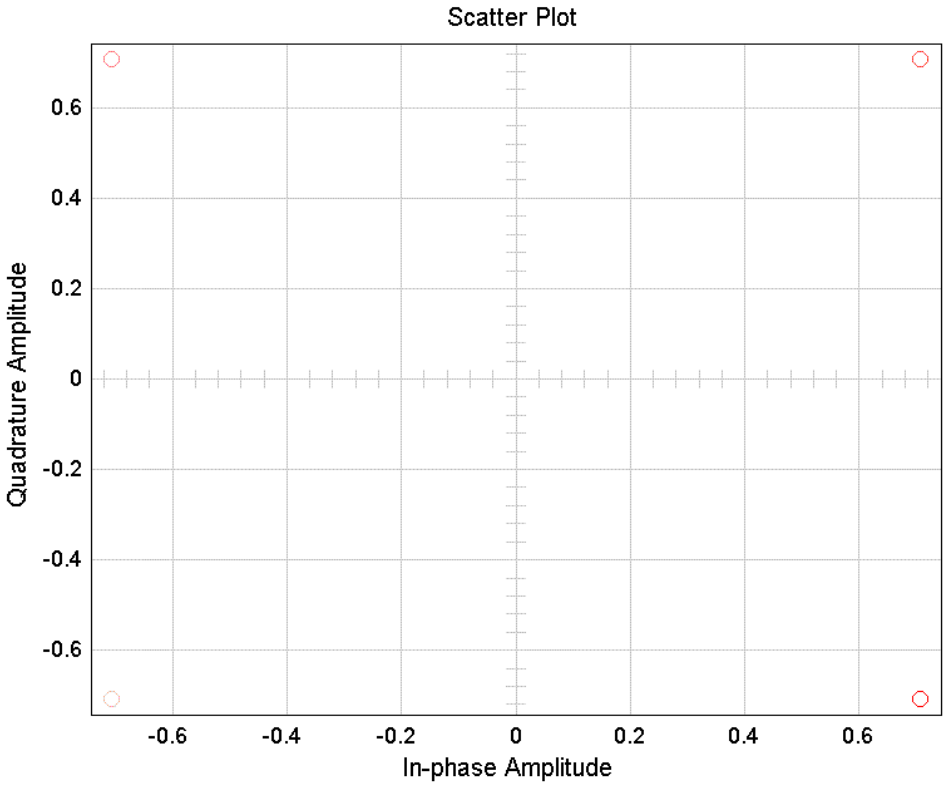


Figure 86: 4QAM Received Symbols

MCode block applied after Time Division Demultiplexer block to I and Q signals. MCode's code is shown in Table 4:

```
%% 4QAM % QPSK Demapper
function B = Demapp(I, Q)
if (I > 0)
    if (Q > 0)
        B = xfix({xlUnsigned,2,0},2);
    else
        B = xfix({xlUnsigned,2,0},3);
    end;
else
    if (Q > 0)
        B = xfix({xlUnsigned,2,0},0);
    else
        B = xfix({xlUnsigned,2,0},1);
    end;
end;
```

Table 4: Mcode Block's Code for QAM Demapper

The MCode block receives 2 inputs and outputs a single output. As seen in Table 4, conditional statements was used. The function name is Demapp, and inputs named with I and Q. Function gives different outputs for different decisions.

After Mcode block, Register and Parallel to Serial blocks were applied. Then, initially generated data and received data compared with Simulink native Error Rate Calculation block. Moreover, to display generated and received data, Simulink Scope and Floating Scope block was used. Displayed generated and received datas can be seen in Figure 87.

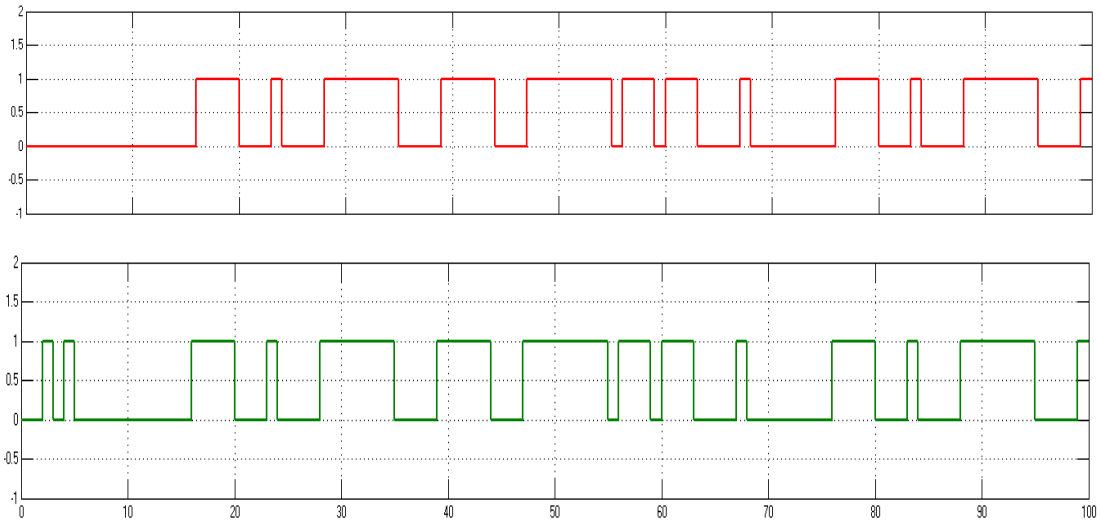


Figure 87: Generated & Received Datas of Model for 4-QAM Modulation (from Scope and Floating Scope block)

6.1.3. QPSK / 4QAM Modulation Simulink Model – Channel

As you seen from Figure 87, developed model which is for 4 QAM works smoothly. Up to this point, the operability of the transmitter and receiver sides has been seen. After completing this step, channel was added to our model. Channel added model and channel internal structure (subsystems) are shown in Figure 88, Figure 90, Figure 91, Figure 92.

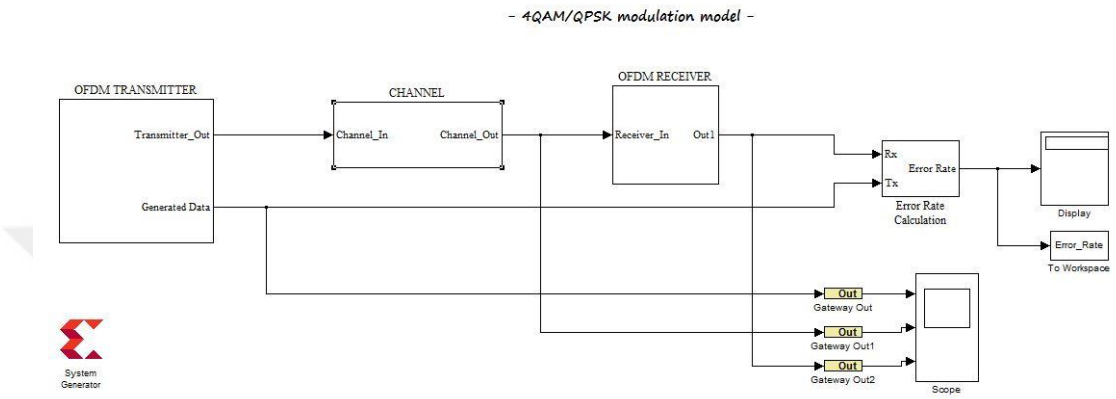


Figure 88: 4QAM & QPSK Modulation Simulink Model with Channel

Model which can be seen in Figure 88, includes Tranmitter, Channel, Receiver and Error Calculation Subsystem respectively.

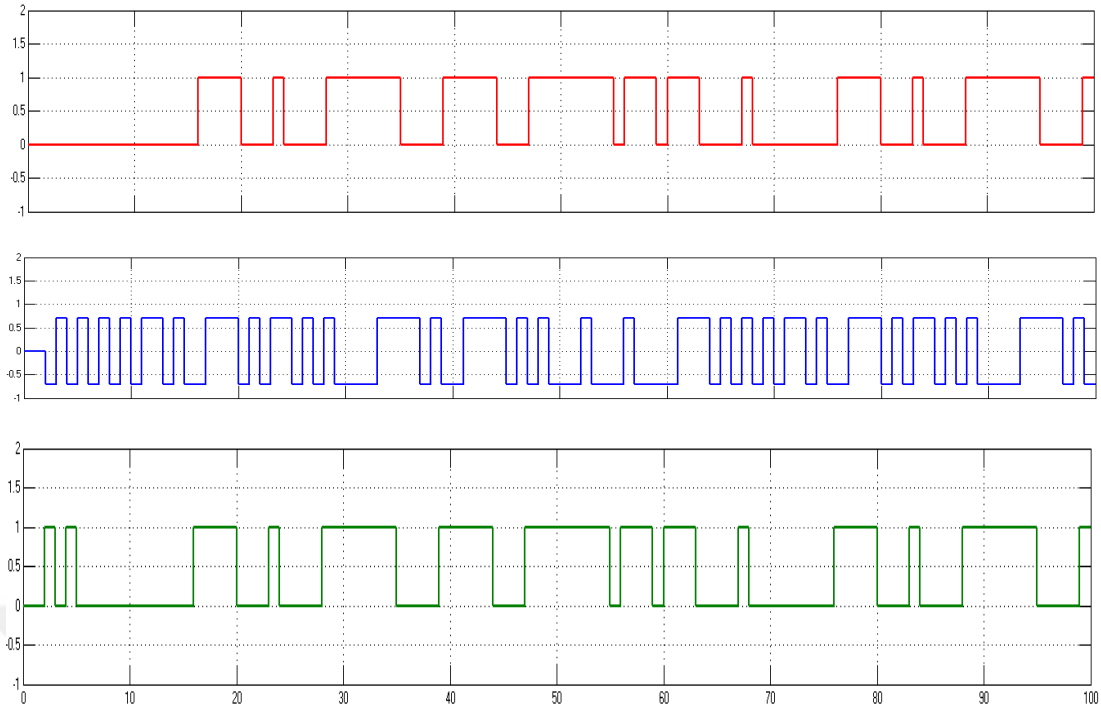


Figure 89: Generated, Transmitted and Received Datas (Respectively)

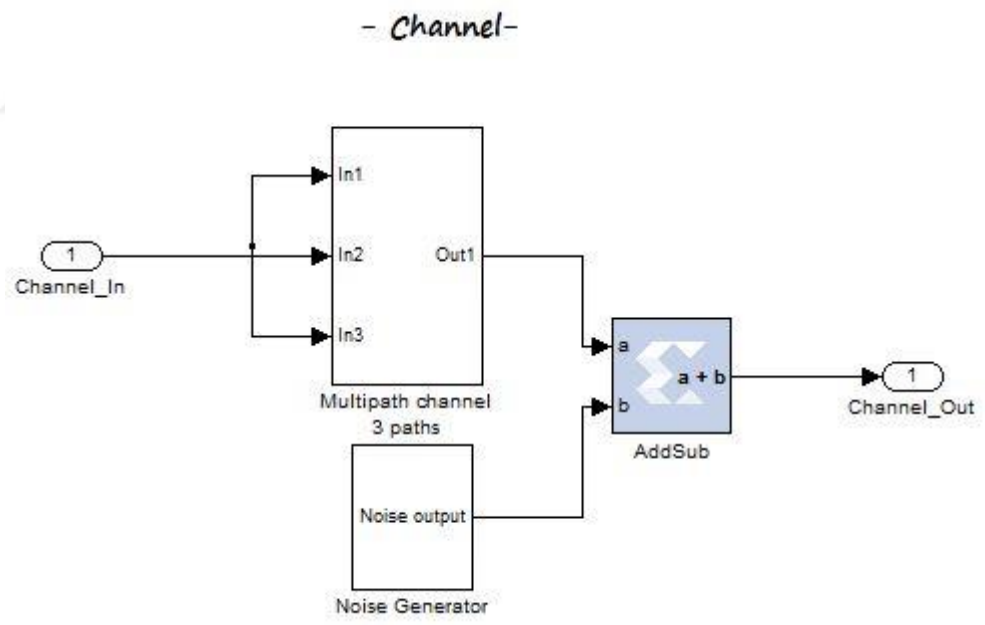


Figure 90: Channel Subsystem

Channel subsystem as seen in Figure 90, includes Noise Generator Subsystem and Multipath Channel Subsystem. Noise Generator subsystem as seen in Figure 92, was added for to see effects of AWGN (Additive White Gaussian Noise) Channels.

Multipath Channel as seen in Figure 91, was added for to see effects of Rician and Rayleigh Fading Channels.

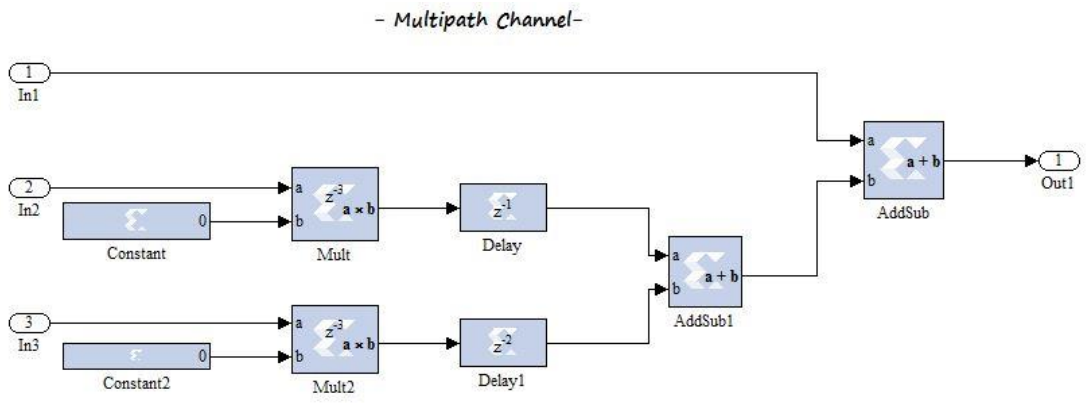


Figure 91: Multipath Fading Subsystem

Multipath Fading Subsystem consist only of Xilinx Blocks which are Constant, Mult, Delay, AddSub. The signals were taken over 3 different paths and tried to model the effects that could be encountered in practical applications.

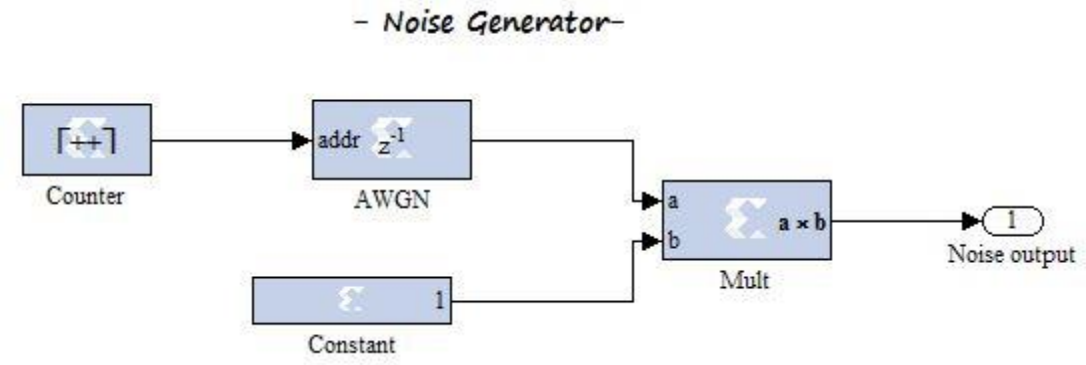


Figure 92: Additive White Gaussian Noise Generator Subsystem

Noise Generator Subsystem consist only of Xilinx Blocks which are Constant, Counter, ROM , Mult. Noise was created with these Xilinx blocks, the generated noise was added with the signal coming from the transmitter side, and then it was forwarded to the receiver side.

With Channel Subsystem, AWGN channel and multipath channel was modelled. Although AWGN effects can be seen, multipath fading effect can not be seen in Simulink design. In the literature researches and our experiments, feasibility

of this situation (multipath fading effects) has been tried many times. Finally, we can say that like it is not possible to see multipath fading effects with available blocks.

6.1.4. QPSK / 4QAM Modulation Simulink Model – Error Rate Calculation

QPSK and 4 QAM Simulink design error rate calculated by model which is shown Figure 93. Initially, generated data and received data compared with Simulink native Error Rate Calculation block. Before this block, Xilinx Gateway out Block was used to use Xilinx blocks output value with Simulink blocks (Error Rate Calculation & Scope and Floating Scope).

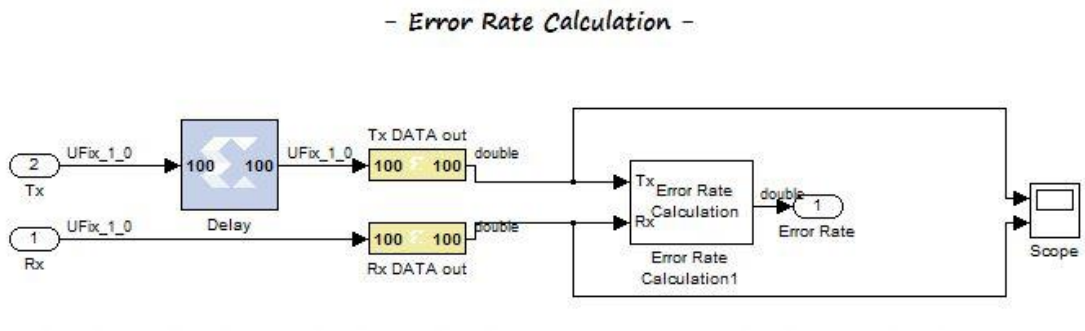


Figure 93: Error Rate Calculation Subsystem of Model

After error calculation, generated data and received data was also shown with scope block. Displayed datas were displayed in Figure 94.

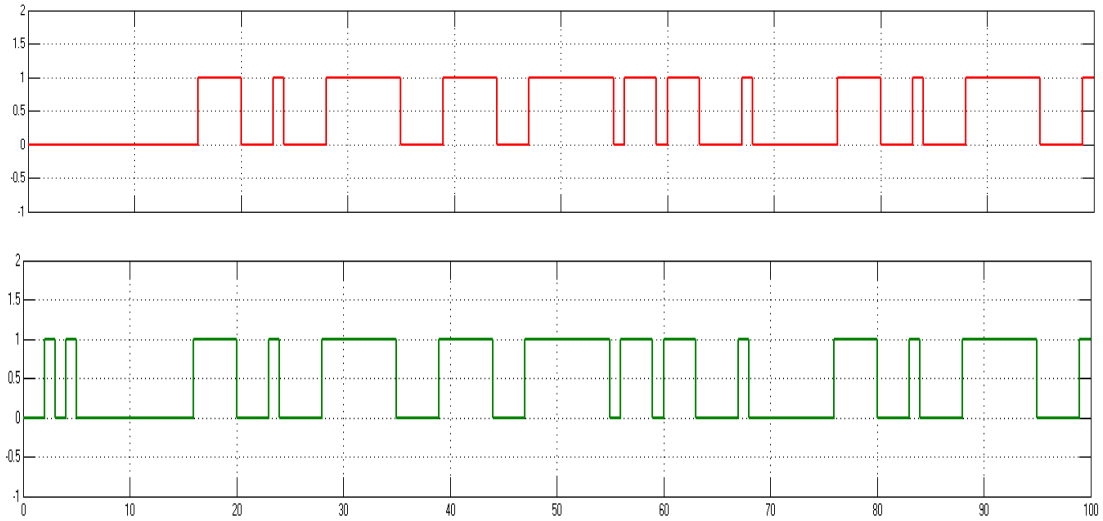


Figure 94: Generated & Received Datas of Model for 4-QAM Modulation (from Scope and Floating Scope block)

6.2. OFDM System using 4QAM Modulation Simulink Model

As mentioned, when the number of M-ary is 4, QAM and QPSK have similar processes. In thesis, M-ary number accepted as a 4, and QAM modulation used for implementation of OFDM. For implementation, the ROM settings were used in Table 2. As mentioned, ROM settings should be changed as in Table 3, if you want to model OFDM with QPSK modulation.

OFDM model with 4QAM was showen in Figure 95, and subsystems were detailed step-by-step in the following figures.

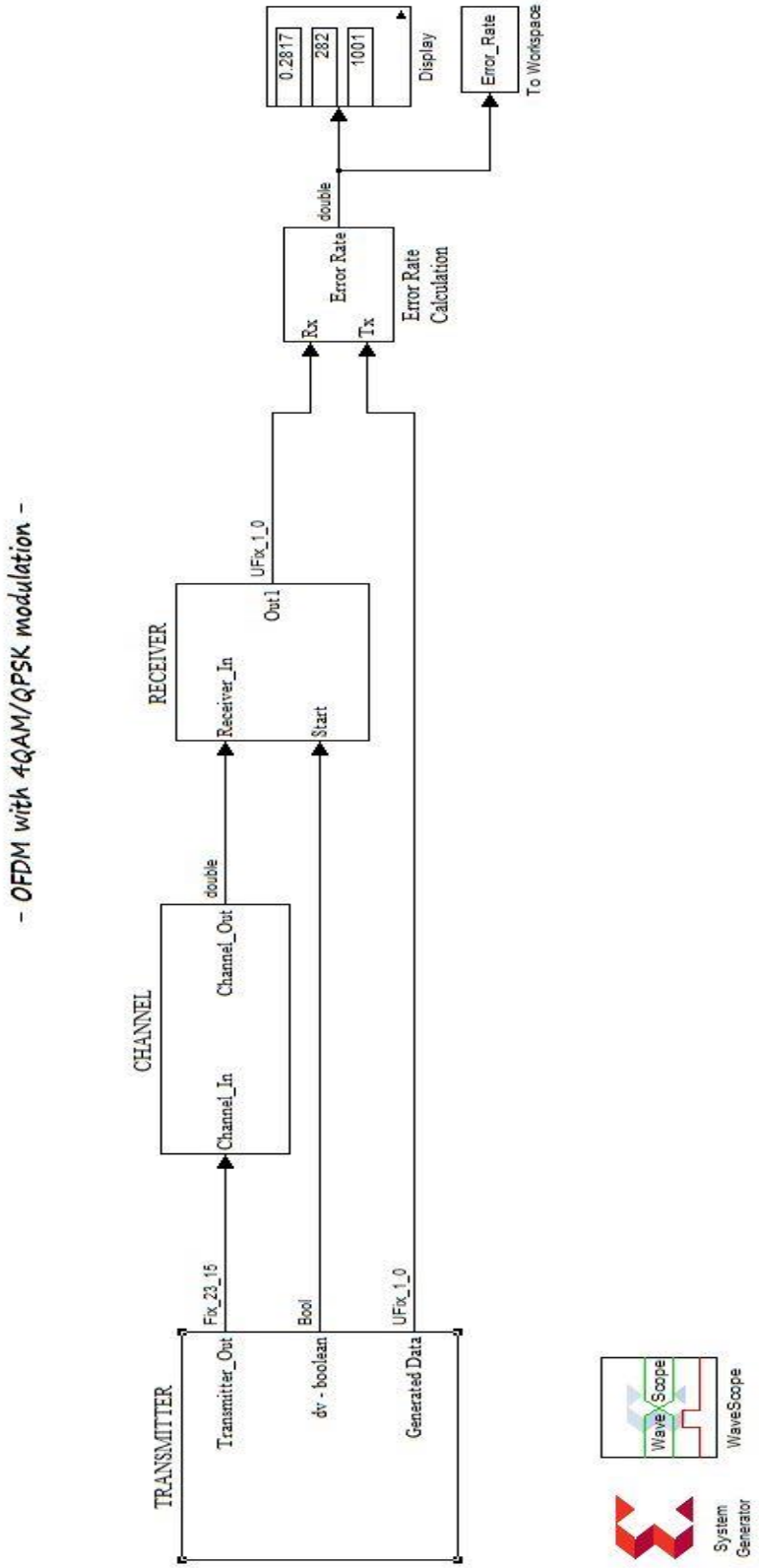


Figure 95: Simulink Model of Implementation

As seen in Figure 95, implementation model Tranmitter, Channel, Receiver and Error Calculation Subsystem respectively.

6.2.1. OFDM System using 4QAM Modulation Simulink Model – Transmitter Side

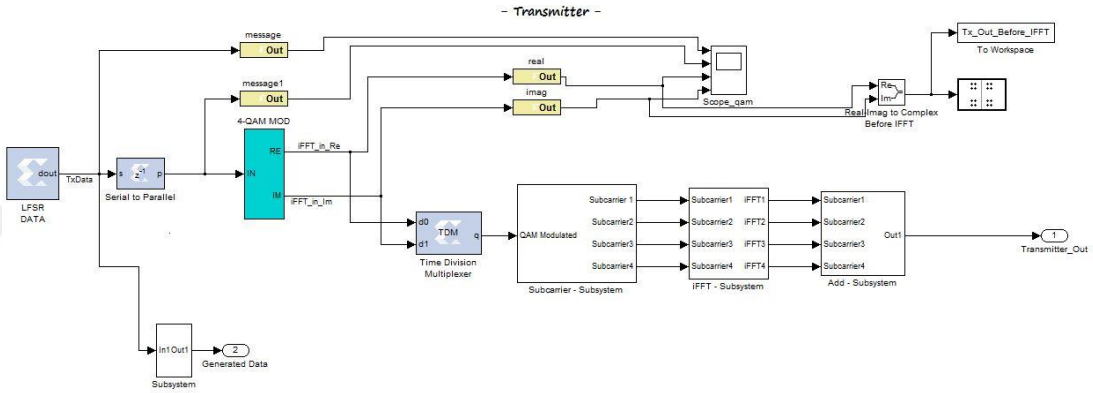


Figure 96: OFDM System - Transmitter Subsystem of Model

Transmitter Subsystem consist of Xilinx System Generator and Simulink Native Blocks. Similar operations which for 4-QAM Modulation Model until the Xilinx Time Division Multiplexer Block were repeated. Then, our signal divided into subcarriers firstly with the Xilinx blocks shown in the Figure 97. Then, subcarriers displayed with Simulink Scope and Floating Scope Block.

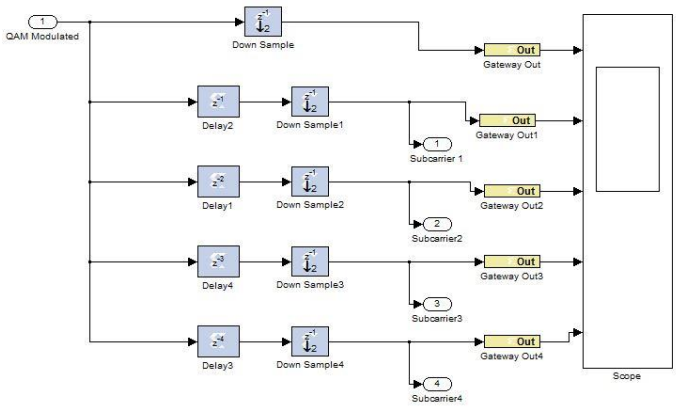


Figure 97: : OFDM System - Transmitter Side - Dividing into Subcarriers Subsystem

Displayed subcarriers can be seen in Figure 98.

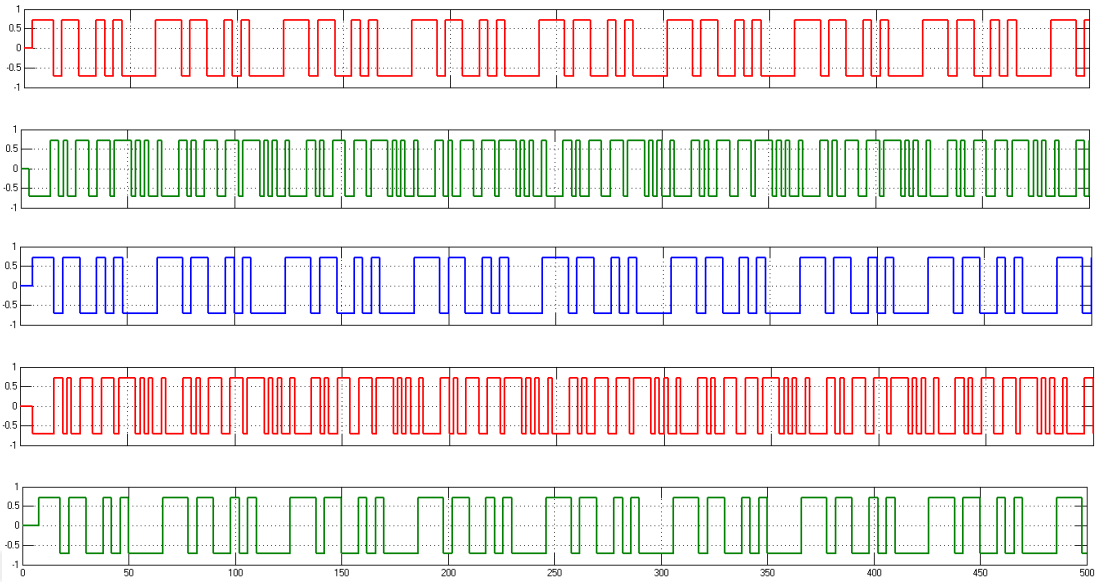


Figure 98: Generated Data & Subcarriers (respectively)

This subsystem consist of Xilinx System Generator Blocks and Simulink native Blocks. Time Division Multiplexer, Time Division Demultiplexer and Gateway Out are from Xilinx, and Scope and Floating Scope is from Simulink. Morever, this subsystem also includes IFFT subsystems which includes Xilinx Fast Fourier Transform 7.1 Blocks.

In Applying IFFT to all Subscarrier Subsystem, data was divided into real and imaginary parts. Then, IFFT subsystem was applied. After IFFT subsystem step, IFFT outputs which are real and imaginary was multiplexed with Xilinx Time Division Multiplexer Block.

After getting subcarriers, IFFT was applied each subcarriers with the Xilinx blocks shown in the Figure 99.

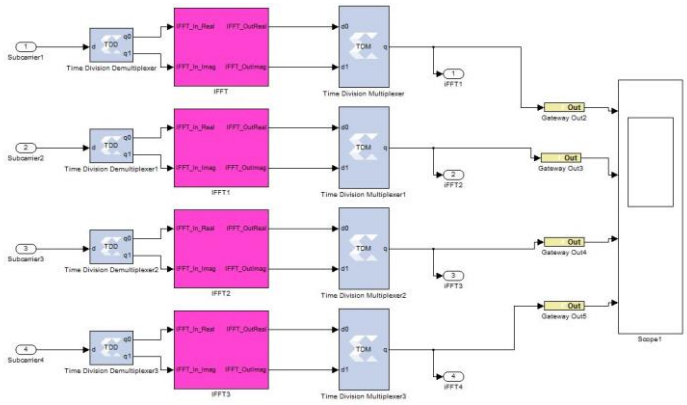


Figure 99: OFDM System – Tranmitter Side – Applying IFFT to all of Subcarriers Subsystem

As seen in the results in Figure 100 , the delay was observed on this step.

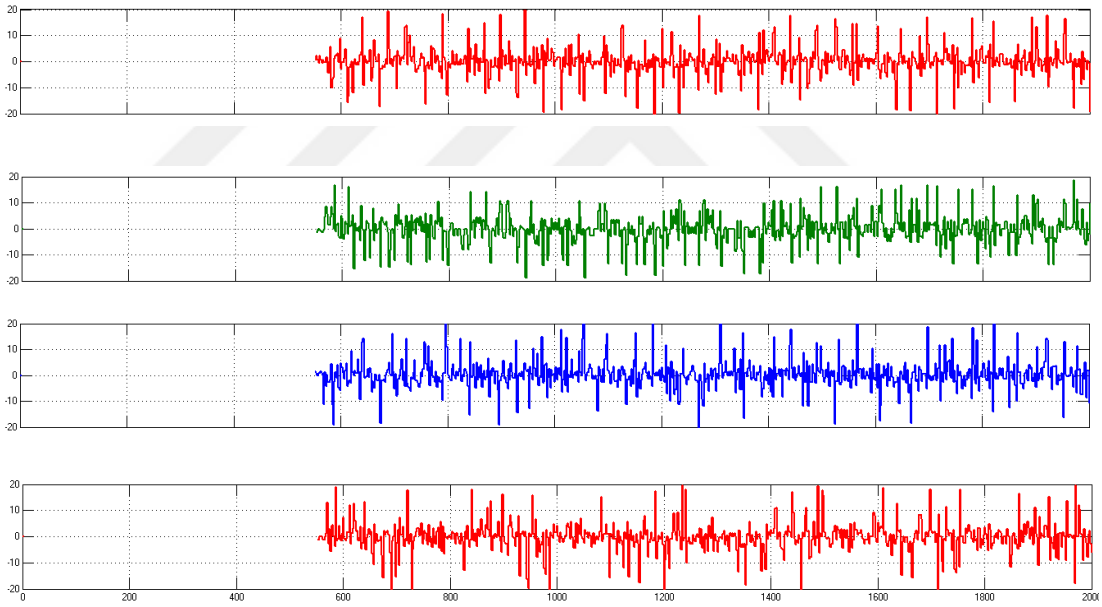


Figure 100: Results of Applying IFFT to all of Subcarriers (after Time Division Multiplexer Block)

As seen in Figure 101, IFFT Subsystem consist of Xilinx System Generator and Simulink native Blocks. Fast Fourier Transform 7.1, Constant, Convert, Register, Gateway In and Gateway Out Blocks are from Xilinx. To Workspace, Terminator and Pulse Generator Blocks are from Simulink.

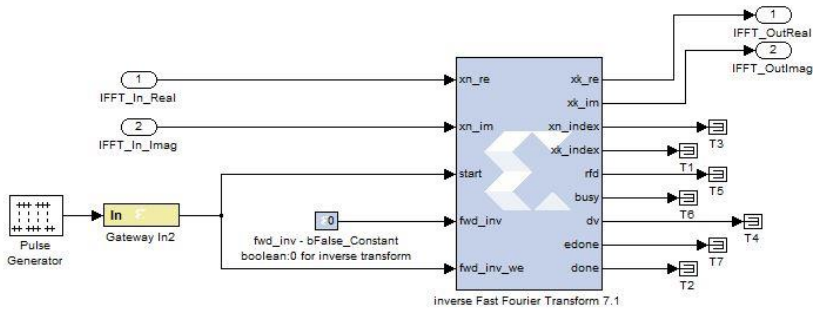


Figure 101: OFDM System – Transmitter Side – IFFT Subsystem

IFFT Subsystem is shown in Figure 101. It can be said that the performance of the IFFT (Fast Fourier Transform 7.1) block is not at the desired level if we compare Simulink native IFFT block.

6.2.2. OFDM System using 4QAM Modulation Simulink Model – Receiver Side

The generated signal passes through the channel after the transmitter and arrives at the receiver.

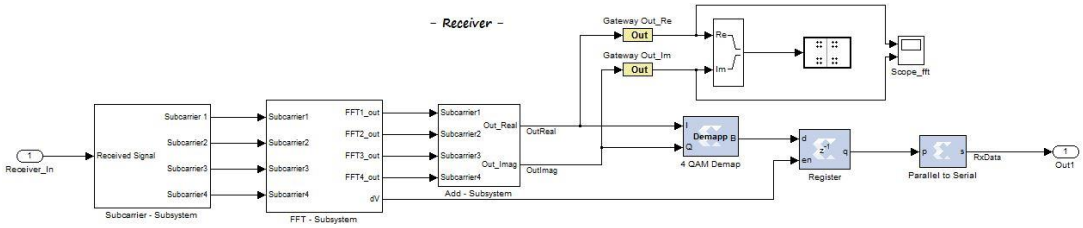


Figure 102: OFDM System – Receiver Subsystem

On receiver side, our signal divided into subcarriers firstly with the Subcarrier – Subsystem. This subsystem's internal structure can be seen in the Figure 103.

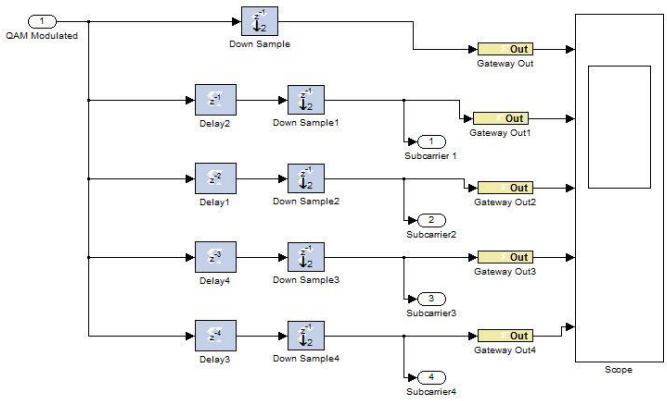


Figure 103: OFDM System – Receiver Side – Dividing into Subcarriers Subsystem

As seen in Figure 103, Dividing into Subcarriers Subsystem consist of Xilinx System Generator and Simulink native Blocks. Delay, Down Sample and Gateway Out from Xilinx, and Scope and Floating Scope from Simulink.

Dividing into Subcarriers results are shown in Figure 104.

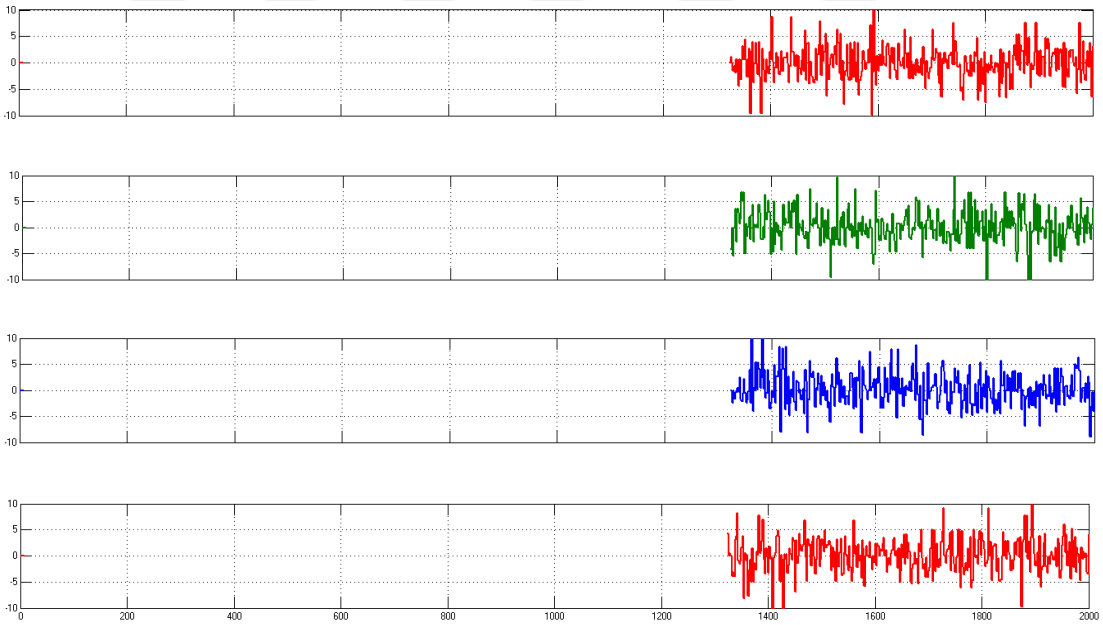


Figure 104: Results of Dividing into Subcarriers

After getting subcarriers, FFT was applied each subcarriers with the Xilinx blocks shown in the Figure 105.

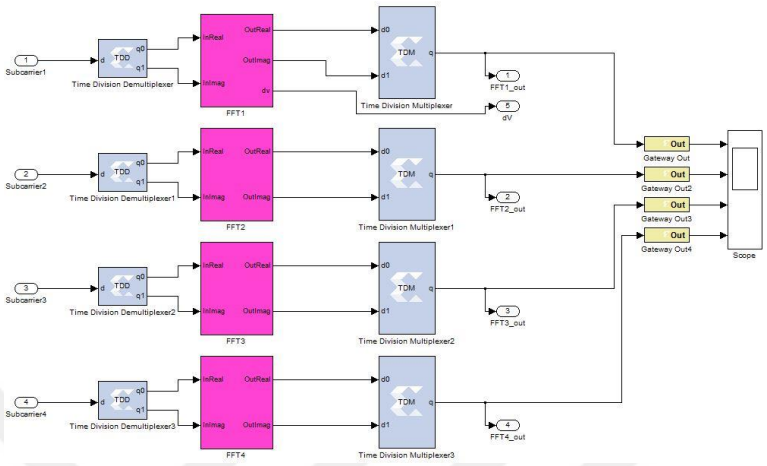


Figure 105: OFDM System – Receiver Side – Applying FFT to all of Subcarriers Subsystem

In Applying FFT to all Subscarrier Subsystem, received data was divided into real and imaginary parts. Then, FFT subsystem was applied. After FFT subsystem step, FFT outputs which are real and imaginary was multiplexed with Xilinx Time Division Multiplexer Block. Multiplexed results are shown in

As seen in Figure 105, Applying FFT to all of Subcarriers Subsystem consist of Xilinx System Generator and Simulink native Blocks. Time Division Multiplexer, Time Division Demultiplexer and Gateway Out are from Xilinx, and Down Sample and Gateway Out from Xilinx, and Scope and Floating Scope from Simulink. Moreover, it also consist of FFT Subsystem. FFT Subsystem is shown in Figure 107.

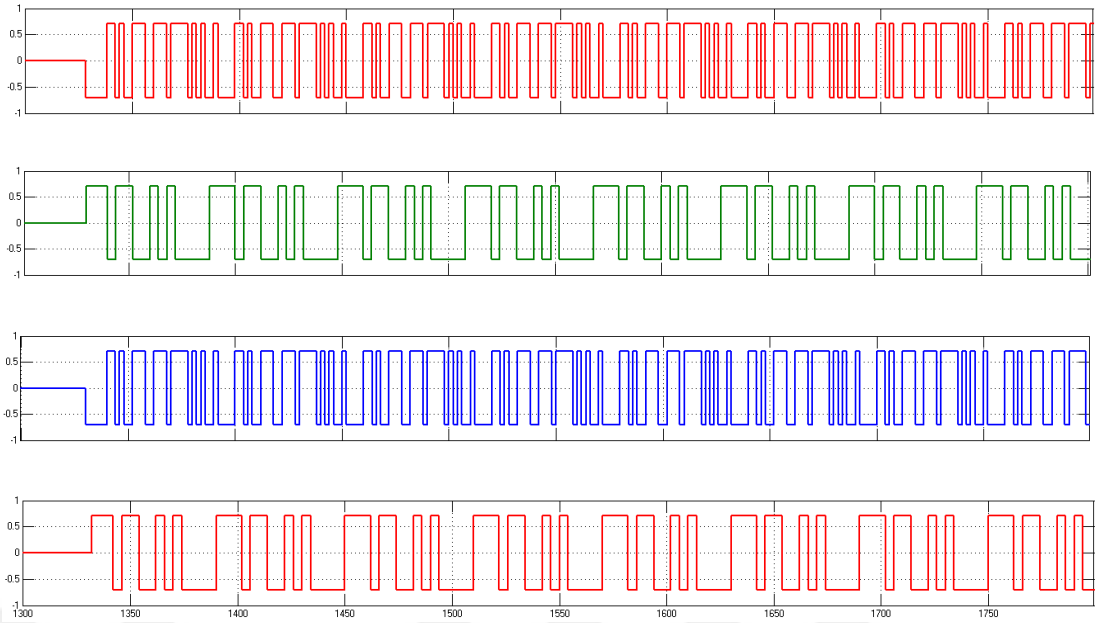


Figure 106: Results of Multiplexed FFT Results

As you seen from the figure, because of FFT 7.1 block latency, delay was observed.

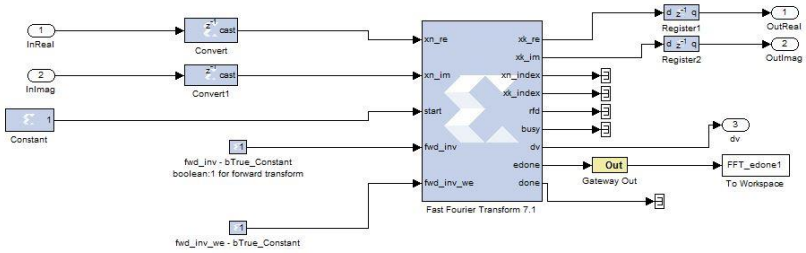


Figure 107: OFDM System – Receiver Side – FFT Subsystem

FFT Subsystem consist of Xilinx System Generator and Simulink native Blocks. Fast Fourier Transform 7.1, Constant, Convert, Register, Gateway Out Blocks are from Xilinx. To Workspace and Terminator Blocks are from Simulink.

It can be said that the performance of the FFT (Fast Fourier Transform 7.1) block is not at the desired level if we compare Simulink native FFT block.

6.2.3. OFDM System using 4QAM Modulation Simulink Model – Channel

Same blocks which are used for 4QAM & QPSK was used to design OFDM channel. These can be seen from figures which are Figure 90, Figure 91 and Figure 92.

6.2.4. OFDM System using 4QAM Modulation Simulink Model – Error Rate Calculation

Same block which is used for 4QAM & QPSK was used to calculate OFDM performance. This can be seen from figure which is Figure 93. As said, although AWGN effects can be seen, multipath fading effect can not be seen in Simulink design. Moreover, if we compare with 4QAM modulation systems and 4QAM modulation systems with OFDM technique, we can not see the superiority of the structure that is designed using OFDM. This is because the of the channel structure. Our channel is flat channel and it is not enough to see the OFDM dominance. If you want to see superiority of the OFDM technique in the channel, filter must be designed on the channel. The available blocks for the filter design that can provide this indication are not sufficient.

CHAPTER 7. CONCLUSION

In this thesis, I focused on OFDM communication technology which is used in new generation communication infrastructures and which is expected to be used frequently in the future, which is one of the wireless communication technologies. OFDM technique was implemented with 4QAM modulation type. We also comment on OFDM technique implemented QPSK modulation with the OFDM technique implemented 4QAM results. Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier transmission. This technique transform a frequency selective channel into a group of flat narrowband channels that it is immunity against large delay spreads of the wireless channel by preserving orthogonality in the time and frequency domain.

The aim of the thesis is to show the OFDM receiver and transmitter, as understood from the thesis topic. In order to achieve the final aim, the QAM and QPSK modulation types which are frequently used in the OFDM technique have been preferred. Moreover, because of its features that can be re-edited in the design stages and is often preferred in today's communications technology infrastructures, FPGA hardware is preferred to perform the our related system. For development environment, Xilinx System Generator installed Simulink (MATLAB R2012a) was chosen.

In the thesis; Introduction, Wireless Communication and Digital Modulation Types, OFDM (Orthogonal Frequency Division Multiplexing), FPGAs & Digilent's Genesys Virtex-5 Development Board, MathWorks' Matlab/Simulink and Xilinx's System Generator for DSP, and finally, Design and Implementation of OFDM Receiver and Transmitter on Genesys Virtex-5 FPGA Development Board chapters were included. Firstly, the literature of OFDM technology and FPGA technology were mentioned. Developments in these technologies were given from its first use to this time. Secondly, digital communication technique is detailed and theoretical information about ASK, FSK, PSK and QAM which are digital communication modulation types are given. Thirdly, OFDM is explained In detail. Various techniques, methods, and terms used in the OFDM technique have been attempted to be conveyed

in detail. Methods used to measure OFDM performance and communication channel models are also included. Fourthly, detailed information about the FPGAs and the Digilent's Genesys Virtex-5 development card with OFDM are shown with all the details. Fifthly, the introduction of the Xilinx System Generator on Simulink, the introduction of System Generator blocks that enable model-based design in the Simulink environment, the development of models with Xilinx blocks, and the evolution of the model for the Virtex-5 FPGA card were described. Finally, QAM and QPSK modulation types were developed using the OFDM technique. In these models, the relevant modulation types are modeled with the parameters required for constructing the OFDM receiver and transmitter. In addition, channel modeling (additive white noise channel and multipath channel) has been carried out in order to give results that are close to practical results. The corresponding model has been provided to work on the FPGA card, and the OFDM technique has been demonstrated.

For the future work, the model in the Simulink environment will be converted to both VHDL and Verilog languages. The implementation in the model will also be shown with Verilog and VHDL codes on Digilent's Genesys Virtex-5 Development Board. Conversion to both VHDL and Verilog languages will be done with the steps which were mentioned in section 5.4.4.

REFERENCES

[1] U. Madhow, *Fundamentals of Digital Communication*.

[2] M. L. Doelz, E. T. Heald, and D. L. Martin, "Binary Data Transmission Techniques for Linear Systems," *Proc. IRE*, vol. 45, no. 5, pp. 656–661, 1957.

[3] R. W. Chang, "Orthogonal Frequency Division Multiplexing," *US Pat. No. 3,488,445 Orthogonal Freq. Div. Mult.*, 1966.

[4] B. R. Saltzberg, "Performance of an efficient parallel data transmission system," *Perform. an Effic. parallel data Transm. Syst. IEEE Trans. Commun.*, vol. 15, pp. 805–811, 1967.

[5] A. Peled,A & Ruiz, "Data transmission by frequency-division multiplexing using the discrete Fourier transform," *IEEE Trans. Commun.*, vol. 19, no. 628–634, 1971.

[6] B. Hirosaki, "An analysis of automatic equalizers for orthogonally multiplexed QAM systems," *IEEE Trans. Commun.*, vol. 28, pp. 73–83, 1980.

[7] and P. T. T. W. E. Keasler, D. L. Bitzer, "US Patent No. 4,206,320: High-speed Modem Suitable for Operating with a Switched Network," 1978.

[8] L. J. Cimini, Jr., "Analysis and Simulation of a Digital Mobile Channel Using Orthogonal Frequency Division Multiplexing," *IEEE Trans. Commun.*, vol. 33, no. 7, pp. 665–675, 1985.

[9] M. A. and R. Lassalle, "Principles of modulation and channel coding for digital broadcasting for mobile receivers," *EBU Tech. Rev.*, pp. 168–190, 1987.

[10] J. M. Cioffi, "A Multicarrier Primer," *ANSI T1E1.4/91-157*, 1991.

[11] A. C. T1-Telecommunications, “A Technical Report on High-Bit-Rate Digital Subscriber Lines (HDSL),” vol. Technical, 1994.

[12] E. T. S. Institute, “Digital Audio Broadcasting (DAB); DAB to mobile, portable and fixed Receivers,” vol. ETSI ETS 3, 1995.

[13] E. T. S. Institute, “Radio Equipment and Systems (RES); High PErformance Radio Local Area Network (HIPERLAN) Type 1; Functional specification,” vol. ETSI ETS 3, 1996.

[14] E. T. S. Institute, “Digital Video Broadcasting (DVB); Framing structure, channel coding and modulation for digital terrestrial television (DVB-T),” vol. ETSI ETS 3, 1997.

[15] “Very-high-speed Digital Subscriber Lines: System Requirements,” vol. ANSI T1E1., 1998.

[16] E. T. S. Institute, “Transmission and Multiplexing (TM); Access transmission systems on metallic access cables; Very high speed Digital Subscriber Line (VDSL); Part 1: Functional requirements,” vol. ETSI TS 10, 1998.

[17] E. T. S. Institute, “Broadband Radio Access Networks (BRAN); Inventory of broadband radio technologies and techniques,” vol. ETSI TR 10, 1998.

[18] IEEE, “IEEE Standard 802.11g: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications,” 2003.

[19] “Ofdm for Mobile Data Communications,” vol. White Pape, pp. 1–8, 2003.

[20] “FLASH-OFDM for 450 MHz – Advanced Mobile Broadband Solution for 450 MHz Operators,” vol. White Pape, 2004.

[21] European Telecommunications Standards Institute, “Digital Video Broadcasting (DVB); Transmission system for handheld terminals (DVB-H),” vol. ETSI EN 30, 2004.

[22] R. B. Marks and R. Marks, “IEEE Standard for Local and Metropolitan Area Networks Part 16: Air Interface for Fixed Broadband Wireless Access

Systems," *IEEE Std 802162004*, vol. 070, no. February, pp. 1–857, 2004.

[23] Institute of Electrical and Electronics Engineers, "Draft IEEE Standard for Information Technology – Telecommunications and Information Exchange Between Systems – Local andMetropolitan Area Networks – Specific Requirements – Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifi," vol. IEEE P802., 2008.

[24] Ericsson, "Long Term Evolution (LTE): an introduction," 2007.

[25] M. Jiang and L. Hanzo, "Multi-user MIMO-OFDM for next-generation wireless," vol. 95, p, 2007.

[26] C. Maxfield, *The Design Warrior ' s Guide to FPGAs*. 2004.

[27] R. E. Haskell and D. M. Hanna, *Introduction to Digital Design Using Digilent FPGA Boards*. 2009.

[28] Altium, "FPGA Design Basics," 2008.

[29] S. Kilts, *Advanced FPGA Design Architecture, Implementation, and Optimization*. 2007.

[30] Andrea Goldsmith, "Wireless Communication," 2004.

[31] B. Sklar, "Digital Communications Fundamentals and Applications (2nd Edition)," 2011.

[32] T.-D. Chiueh and P.-Y. Tsai, *OFDM Baseband Receiver Design for Wireless Communications*. John Wiley & Sons, 2008.

[33] R. G. Gallager, "Principles of Digital Communication - MIT Course Material," 2004.

[34] W. Stallings, *Wireless communications and networks (2nd edition)*. Pearson Prentice Hall.

[35] K. Vasudevan, "Digital Communications and Signal Processing," 2008.

[36] "Concepts of Orthogonal Frequency Division Multiplexing (OFDM) and 802

. 11 WLAN," pp. 1–4, 2014.

[37] R. Prasad, *OFDM for Wireless Communications Systems*. 2004.

[38] P. C. S. Bhavsar, H. Pandey, "Design and Implementation of OFDM Trans-Receiver using IEEE 802.11 (WLAN)," *IJMER*, vol. 4, no. 1, pp. 55–67, 2014.

[39] T. Do-Hong, "Principles of Digital Communications and Coding."

[40] S. Haykin and M. Moher, "Introduction to Analog and Digital Comunications," 2007.

[41] J. Zhang and Z. Zhang, "Simulation and analysis of OFDM system based on simulink," *2010 Int. Conf. Commun. Circuits Syst. ICCCAS 2010*, 2010.

[42] N. Khambekar, D. Liang, and V. Chaudhary, "Utilizing OFDM guard interval for spectrum sensing," *IEEE Wirel. Commun. Netw. Conf. WCNC*, no. 0, pp. 38–42, 2007.

[43] Y. S. Cho, J. Kim, W. Y. Yang, and C. G. Kang, *MIMO-OFDM Wireless Communications with MATLAB®*. 2010.

[44] K. S. R. K.Mahender, T.A.Kumar, "Performance Study of OFDM over Multipath Fading Channels for Wireless Communications," vol. 12, 2017.

[45] U. S. R. Akbar, S.A.Raza, "Performance Evaluation of WiMAX," 2009.

[46] Gary Breed, "Fundamental Concept and Measurement Issues," *High Freq. Electron.*, pp. 46–47, 2003.

[47] Xilinx, "Xilinx System Generator for DSP User Guide," vol. UG640, 2012.

[48] D. Inc., "Genesys ™ Board Reference Manual," 2013.

[49] Digilent Inc., "Digilent Adept System Programmer's Reference Manual," 2010.

[50] D. K. Chaturvedi, *Modeling and Simulation of System Using Matlab and Simulink*. 2010.

[51] M. D. S. P. Design, "Vivado Design Suite Tutorial: Implementation," vol. 986,

pp. 1–100, 2014.

[52] Xilinx, “Vivado Design Suite Reference Guide - Model-Based DSP Design Using System Generator,” 2016.

[53] B. O. Omijeh, “A Computer-Based Comparative Performance Analysis of QPSK and 4-QAM Schemes in Fading Channels,” *Int. J. Sci. Eng. Res.*, vol. 6, no. 11, 2015.

APPENDIX

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