ELECTRONIC TUNABILITY IN ANALOG FILTERS

by

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ABSTRACT

ELECTRONIC TUNABILITY IN ANALOG FILTERS

In the beginning years of the analog design, discrete components were being used in the analog design procedures. After manufacturing, trimmer capacitors and potentiometers were used for electronic tunability to compensate for the electronic component non-idealities and tolerances. After 1970s, analog circuits have been implemented as integrated circuits, where element tolerances are unacceptably high. Non-idealities and parasitics due to IC implementation are serious problems for the circuits after manufacturing. Therefore, electronic tuning of some parameters after production has been a very important feature in IC design. In the thesis following major tunability methods are examined: Electronic tunability with MOSFET-C technique, with mixed translinear loops, with operational transconductance amplifiers and with adjusting current-gain.

During electronic tuning of the desired parameters, some other parameters of the circuit such as linearity, stability, gain and high frequency performance, may be affected in an undesired way. Therefore, trade-offs between tunability and other parameters of the circuits are illustrated to find effective tunability ranges. Moreover, in the thesis new tunable filter circuits are suggested for each of these methods as examples and detailed non-ideality and parasitic component analyses of these circuits are given.

ÖZET

ANALOG SÜZGEÇLERDE ELEKTRONİK AYARLANABİLİRLİK

Analog devre tasarımının ilk yıllarında ayrık devre elemanları kullanılmaktaydı. Üretimden sonra ayarlı dirençler ya da kondansatörler vasıtasıyla devre elemanlarının tolerans ve ideal olmayan davranışlarından kaynaklanan sapmalar düzeltilirdi. 1970'lerden sonra analog devreler tümleşik devre olarak tasarlanmaya başlanmıştır. Tümleşik devrelerde özellikle pasif devre elemanlarının toleransları oldukça yüksektir. Ayrıca tümleşik devre tasarımının kendisinden kaynaklanan parazitik elemanlar ve idealden sapmalar ciddi birer sorun teşkil eder. Bu sebeplerden dolayı, tümleşik devrelerin üretiminden sonra bazı devre parametrelerinin ayarlanabilir olması çok önemli bir özelliktir. Tezde tümleşik devre analog süzgeçlerin elektronik ayarlanmasında kullanılan dört ana yaklaşım karşılaştırmalı olarak incelenmiştir: MOSFET-C tekniği ile elektronik ayarlanabilirlik, "Mixed translinear loops" kullanarak elektronik ayarlanabilirlik, OTA kullanarak elektronik ayarlanabilirlik, akım kazancı kontrolü ile elektronik ayarlanabilirlik.

Süzgeç devrelerinde bazı parametreler elektronik olarak ayarlarken, devrenin diğer parametrelerinde (Doğrusallık, kararlılık, yüksek frekanslarda çalışabilme, kazanç vb.) bozulmalar meydana gelebilir. Bu sebepten dolayı efektif ayarlanabilirlik aralıklarının tespiti için elektronik ayarlanabilirlik ile diğer devre parametrelerinin ilişkileri de gösterilmiştir. Bu amaçla, tezde her bir metot için yeni ayarlanabilir süzgeç devreleri önerilmiş ve bu devrelerin idealden sapma ve parazitik elemanlardan etkilenmeleri detaylı şekilde incelenmiştir.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS/ABBREVIATIONS

C_{OX}	The gate oxide capacitance of a MOSFET transistor per unit area
I_C	Control current for the OTA and controlled conveyor
I_A	Control current for the current adjusting in E-DDCC
I_D	Drain current of a MOSFET transistor
L	Length of a MOSFET transistor
N_A	The doping concentration of the substrate
q	The electron charge
Q	Quality factor of a biquad filter
V_B	Bulk (substrate) potential
V_C	Control voltage
W	Width of a MOSFET transistor
V_{Th}	The threshold voltage of the MOSFET corresponding to a V_B bulk potential
V_T	Thermal voltage
V_{AN}	Early voltages of the NPN transistors
V_{AP}	Early voltages of the PNP transistors

α	Current gain between the X and Z ports of the current conveyors
α'	Electronically tunable current gain
β	Voltage gain in current conveyors between X and Y ports
β_F	Current gain of the BJT transistor
C_π	Parasitic capacitances C_{be} for BJT and C_{gs} for CMOS
C_μ	Parasitic capacitances C_{bc} for BJT and C_{gd} for CMOS
γ	Current gain between the X and Y ports of the current conveyors
γ'	The fabrication process parameter of CMOS
μ	Carrier mobility in the channel of the MOSFET transistor
ε_S	The silicon dielectric constant
ω_0	Angular pole frequency of a filter
ω_p	Angular corner frequency of an active element's gain

CCI	First generation current conveyor
CCII	Second generation current conveyor
CCIII	Third generation current conveyor
CCCI	Current controlled first generation current conveyor
CCCII	Current controlled second generation current conveyor
CCCIII	Current controlled third generation current conveyor
CDBA	Current difference buffered amplifier
C-CDBA	Current controlled current difference buffered amplifier
CFOA	Current feed-back operational amplifier
CMRR	Common mode rejection ratio
COA	Current operational amplifier
DDCC	Differential difference current conveyor
DVCC	Differential voltage current conveyor
E-CCII	Electronically tunable second generation current conveyor
E-DDCC	Electronically tunable differential difference current conveyor
E-DTA	Electronically tunable differential transconductance amplifier
FET	Field effect transistor
FDNR	Frequency dependent negative resistor
IC	Integrated circuit
IVB	Inverting voltage buffer
MRC	MOS resistive cell
NMOS	N type metal oxide semiconductor
PMOS	P type metal oxide semiconductor
Op-amp	Operational amplifier
OTA	Operational transconductance amplifier
OTRA	Operational transresistance amplifier
THD	Total harmonic distortion
VLSI	Very large scale integration
VM	Voltage mode

1. INTRODUCTION

1.1. Historical Review

An analog filter is an electronic circuit that alters the amplitude and/or phase characteristics of an electrical signal with respect to frequency. The filters are basically frequency selective networks designed to remove unwanted signal components and/or enhance wanted ones. Traditionally, passive analog filters were used as resistively terminated lossless LC filters; they achieve complex poles and the desired sharp transition regions between pass-bands and stop-bands (Valkenburg, 1995). The design of active filters has effectively started with the use of operational amplifiers (op-amp) as active element or building block. In the early 1940's, George Philbrick and his fellow workers developed the differential amplifiers using vacuum tubes (Gewartowski and Watson, 1965). These were used in various analog applications such as filtering in radar systems and in some control applications (Spangenberg, 1948; Gewartowaski and Watson, 1965; Oman, 1974).

In 1947, John Ragazzini used the name operational amplifier for the first time to represent the assembly of vacuum tubes in the form of differential amplifiers, used for a variety of applications including filters and oscillators. These tubes were bulky, consumed large power and dissipated a lot of heat besides being expensive (Van Valkenburg, 1995). In 1948, the transistor was introduced and the circuits designed with tubes were converted into comparatively much smaller units. In 1955, the work on filters using op-amps was accelerated and the well-known Sallen-Key active RC circuit was reported (Sallen and Key, 1955). The advent of operational amplifier in integrated circuit (IC) form made the active-RC filters a practical reality.

Between 1960 and 1970, a great deal of work was done on active-R type filters and active-RC type filters (Soderstrand, 1976; Kumar and Shukla, 1990). First commercially available monolithic op-amp (Fairchield's μa709) was produced in 1965 (Toumazou *et al*., 1998). In this period, a typical state-of-art active filter involved a PCB mounted circuit comprising discrete passive components together with IC op-amps. Another significant

milestone of this era was the development of special-purpose discrete components and op-amp ICs interconnected on a ceramic or glass substrate. However, it was recognized that there were considerable benefits to be gained from producing an all-IC active filter.

As the concept of microminiaturization was introduced, inductors were found to be too large. Therefore, the designers started replacing RLC circuits with active-RC circuits in which gains were obtained using op-amps together with resistors and capacitors in the feed-back loop. Also in 1969, it was realized that it is possible to replace passive inductors in passive ladder prototype filters with active RC counterparts such that the ladder is transformed to an active RC filter (Antonio, 1969). Bruton presented an idea to resolve this problem, which has been named after him as Bruton transformation. This introduced the concept of frequency dependent negative resistor (FDNR) (Valkenburg, 1995).

Between 1968 and 1970, the concept of current conveyor was introduced (Sedra and Smith, 1970). In the early 1970s operational transconductance amplifier (OTRA) also known as Norton amplifier (National Semiconductor's LM3900) was produced commercially, (Toumazou *et al*., 1998). In 1976, a novel active device was introduced by RCA Solid State, which was given the name operational transconductance amplifier (OTA), and it provides electronic tunability (Franco, 1976) in contrast to the op-amp. After 1980s, MOSFET-C filters where the passive resistors are replaced by MOS transistors in some special topologies using op-amps became popular and used for electronic tunability (Banu and Tsividis, 1983).

1.2. Classification of the Analog Filters

The analog filter is a system that can be employed to filter continuous-time signals. It can be realized with passive elements such as resistors and capacitors with/without a gain element such as op-amp, operational transconductance amplifiers or current conveyors. When selecting components for the design of an analog filter, one should consider the following factors: The technology desired for the system implementation, availability of DC power supplies for the active devices, power consumption, cost, the frequency range of operation, the sensitivity to parameter changes and stability, weight and size of the implemented circuit, and noise and dynamic range of the realized filter.

The analog filters are further classified considering types of the elements used:

(i) **Passive Filter:** Passive filters are built with resistors, capacitors and inductors. They have no power gain because passive filters have no amplifying device. In particular the physical size and weight of the inductor is prohibitive in addition to their large dissipation factors complicating synthesis, their unsuitability for integrated circuit realization and their non-linear core saturation characteristics. On the other hand, passive RC filters have natural frequencies restricted to the negative real axis and have poor performance on the basis of quality factor.

(ii) **Active Filters:** Active filters also use resistors and capacitors. Inductors are replaced and simulated by circuits using active devices capable of producing gain. These devices can range from single transistors to integrated circuit such as the op-amp and OTA. An active filter offers the following advantages over a passive filter such as gain and frequency adjustment flexibility, low cost, occupying less space due to integrability property.

1.3. Applications of the Active Filters

Throughout the communication and measurement industries, electrical filters in all technologies are being used in huge numbers (Bowron and Stephenson, 1979). Indeed it becomes difficult to name any electrical system that does not contain some kind of signal filter. There can be little doubt that rapid growth in large-scale telecommunication systems provides a major market impetus in active filters. One very important use is in conjunction with PCM-CODEC (pulse code modulation coder/decoder) chips for the digitization of telephones. Other applications include de-emphasis and pre-emphasis, aliasing, equalization, and active impedance matching networks for repeaters, and low-pass filters to suppress harmonics. An interesting example of communication application is in dual tone multi-frequency (DTMF) signaling for use in touch-tone dialing in the telephone market. It is also used in associated systems such as the radiotelephone link.

Other major applications of active filters lies in instrumentation, examples are noise rejection in digital voltmeters, harmonic filtering in transformers, vibration and shock studies. They also play major role in the field of medical electronics where they have a distinct advantage over passive filters in low and sub audio range. Many physiological signals fall within three-decade band below 20Hz, such as heart-monitoring by electrocardiograph (ECG) and brain wave recording by electroencephalograph (EEG).

1.4. High Order Active Filters

The order of a filter is important for several reasons. It is directly related to the number of components in the filter and therefore to its cost, physical size and the complexity of the design task. Therefore, higher order filters are more expensive, take up more space and are more difficult to design. The primary advantage of a higher order filter is that it will have a steeper roll-off slope than a similar lower-order filter. The order of an active-RC filter is related to the number of capacitors it contains.

The oldest and probably the best-known method of active filter design starts by factoring a high order transfer function $H(s)$ into a product $H(s)=\Pi H_i(s)$, where the factors $H_i(s)$ are second order sections or biquads for even order filters and an addition a first order or third order section for odd order filters. This is a modular approach and is convenient for designers to realize higher order filters. The reason of using biquad blocks is to obtain complex poles easily.

The first and second order standard transfer functions realizable with an active filter are given in Table 1.1, where a_0, a_1, a_2, b_0, b_1, b_2 are constants.

1.5. Active Elements Used in Analog Filter Design

Active elements that have received considerable attention in the literature can be listed as follows: Operational amplifier, operational transconductance amplifier, and current conveyors. The versatility and low cost of IC op-amps have made them one of the most popular building blocks in the active filter realization.

Table 1.1. The first and second order standard transfer functions

Type	Transfer Function	Pass Band	Stop Band
First Order Low-pass Filter	$H(s)=\frac{a_0}{b_0+b_1 s}$	$0<\omega<\omega_C$	$\omega>\omega_C$
First Order High-pass Filter	$H(s)=\frac{a_1 s}{b_0+b_1 s}$	$\omega>\omega_C$	$0<\omega<\omega_C$
First Order All-pass Filter	$H(s)=\frac{b_0-b_1 s}{b_0+b_1 s}$	$0<\omega<\infty$	–
Second Order Low-pass Filter	$H(s)=\frac{a_0}{b_0+b_1 s+b_2 s^2}$	$0<\omega<\omega_C$	$\omega>\omega_C$
Second Order High-pass Filter	$H(s)=\frac{a_2 s^2}{b_0+b_1 s+b_2 s^2}$	$\omega>\omega_C$	$0<\omega<\omega_C$
Second Order Band-pass Filter	$H(s)=\frac{a_1 s}{b_0+b_1 s+b_2 s^2}$	$\omega_L<\omega<\omega_H$	$0<\omega<\omega_L$, $\omega>\omega_H$
Second Order Notch (Band Reject) Filter	$H(s)=\frac{b_0+b_2 s^2}{b_0+b_1 s+b_2 s^2}$	$0<\omega<\omega_L$, $\omega>\omega_H$	$\omega_L<\omega<\omega_H$
Second All-pass Filter	$H(s)=\frac{a_0-a_1 s+a_2 s^2}{a_0+a_1 s+a_2 s^2}$	$0<\omega<\infty$	–

The OTA has performance features and versatility similar to that of an op-amp and in addition, it provides electronic tunability of its transconductance gain. The op-amp concept has been in use since the late 1940s, its limitations have been also well-known beside its advantages. For example, voltage mode (VM) op-amp circuits have limited bandwidth at high closed loop gains due to constant gain bandwidth product. Furthermore, the limited slew rate of the operational amplifier affects the large signal and high frequency operation. To overcome these drawbacks, Sedra and Smith (1968) introduced new active building block known as first generation current conveyor (CCI) and further developed a second generation current conveyor (CCII) in 1970 (Sedra and Smith, 1970). The current conveyor is a general-purpose building block as the operational amplifier is. Current conveyor is an active three-port device with terminals X, Y, and Z. The current conveyor exhibits high linearity, wide dynamic range, and better high frequency performance compared to the op-amp (Roberts and Sedra, 1989; Sedra, 1989; Wilson, 1990). After Fabre introduced the controlled current conveyor (Fabre *et al.*, 1995a), current conveyors became very popular in the tunable circuit design.

1.6. Objective of the Thesis

In the beginning years of the analog design, discrete components were being used in the analog design procedures. After completing the design, trimmer capacitors and potentiometers were used for electronic tunability to compensate for the electronic component non-idealities and tolerances. After 1970s, analog circuits have been implemented as integrated circuits. In IC design, especially passive element tolerances are very high. Non-idealities and parasitics due to IC implementation is a serious problem for the circuits. Therefore, tuning some parameters of the circuits after production electronically has been very important feature for IC design.

1.7. The Previous Work

In this thesis, electronic tunability of the analog filters are examined and described with the novel example circuits such as first and second order all-pass filters, notch filters and a FDNR simulator. Although there are several examples of this type of circuits in the literature, most of them are not electronically tunable. The electronic tunable ones are explained below.

First and high-order all-pass filters are widely used in analogue signal processing in order to shift the phase of an electrical signal while keeping the amplitude constant. Op-amp based circuits (Ponsonby, 1966) use large number of passive elements and they suffer from the limited bandwidth performance of the op-amp. Also, several voltage and current-mode first order all-pass sections (APSs) using second-generation current conveyors have been reported (Salawu, 1980; Fabre *et al.,* 1989; Higashimura and Fukui*,* 1990; Soliman, 1997; Cicekoglu *et al.,* 1999; Khan and Maheshwari, 2000a; Toker *et al.,* 2001). However, some of these circuits employ four or more passive components (Salawu, 1980; Higashimura and Fukui, 1990; Soliman, 1997). Considering the versatility and easy implementation of CCII+, many first order all-pass networks employing a single CCII+ were also tabulated (Cicekoglu *et al.,* 1999; Toker *et al.*, 2001). Some of these all-pass networks employ only three passive elements, namely two resistors and one grounded capacitor. In general the most widely used type of current conveyor in active network

applications is CCII+, because its construction is traditionally accepted to be simpler compared to CCII–. Thus many of the CCII based all-pass filters are presented using this component where the negative type remained less popular. In last years the negative type conveyor deserves also attention due to the high performance CCII– realizations (Awad and Soliman, 1999; Seguin and Fabre, 2001b). For example, two all-pass filters employing two resistors, a capacitor and a single CCII– have been reported (Khan and Maheshwari, 2000a; Metin *et al*., 2003). These filters can also be implemented using a current controlled current conveyor (CCCII) (Fabre *et al.,* 1995a) and in this case the number of the resistors reduces by one. The capacitor in (Metin *et al*., 2003) is grounded. It is well known that floating capacitors can be realized if the IC process offers two poly layers. Some of the IC processes exhibit double-poly layers, but they are expensive. Furthermore, it should be noted that, grounded IC capacitors have less parasitics compared to floating counterparts, which is important from the performance point of view.

Some of these current conveyor based all-pass filters can be made tunable employing controlled conveyor such as (Khan and Maheshwari, 2000b; Soliman, 1997). The circuit presented by (Minaei and Cicekoglu, 2006) includes a controlled conveyor, an op-amp, and two capacitors. It is tunable but it is not canonical due to its two capacitors. Some recent papers by Horng (Horng, 2005; Horng *et al.*, 2006a; Horng *et al.*, 2006b) emphasize the importance of the design with only grounded passive elements. The grounded resistors can be replaced by MOSFET based electronic resistors and electronic tunability is obtained. However, these circuits are not canonical due to their two capacitors and resistors and they have element matching restriction. A tunable all-pass filter suitable for low voltage operation is presented by (Toker and Ozoguz, 2003). This circuit uses only one active element and a single capacitor. However, this circuit has the drawback of requiring expensive twin-well process for proper operation.

Also in the literature, some OTA based first order all-pass filters were presented (Shah and Ahmad, 1990; Al-Hashimi *et al.,* 2000). The circuit in (Shah and Ahmad, 1990) employs a grounded capacitor and four resistors. The circuit in (Geiger and Sánchez-Sinencio, 1985) includes two OTAs, one resistor and one capacitor. These are voltage-mode filters. The current-mode OTA based circuit in (Al-Hashimi *et al.,* 2000) uses a capacitor and two OTAs, one dual output OTA and one triple output OTA.

The OTA is as well widely used in the design of electronically tunable second order filters (Franco, 1976; Sun, 2002; Urbas and Osiowski, 1982; Malvar, 1982; Deliyannis *et al*., 1999). This active element provides advantages of design simplicity and electronic tunability compared to classical op-amps. Also, the OTA-C circuits have been shown to be potentially advantageous for the design of high-frequency analog filters (Sun, 2002). In 1976, Franco proposed first example of electronically tunable filter circuit with OTA (Franco, 1976). The circuit proposed in (Urbas and Osiowski, 1982) uses two OTAs to realize a biquad filter. Also the filter circuit reported in (Malvar, 1982) employs three OTAs. Moreover, in (Deliyannis, 1999) many OTA based filter circuits are described briefly. In the classical continuous-time filter approach, operational transconductor amplifiers and capacitors are used together because an OTA and a capacitor can easily implement an integrator that is a basic building block of many filter structures.

In the MOSFET-C technique the resistors are replaced by MOSFETs in special topologies whose non-linearities are canceled. In the classical approach, op-amp based active RC circuits are converted to balanced form and MOS transistors replace passive resistors with an advantage of improved common mode rejection ratio (CMRR) and noise rejection. The price paid for balanced design is doubling of the number of capacitors and resistors hence doubling of the chip area. In (Czarnul, 1986), a MOS resistive integrator circuit is presented that do not need balanced structure. Furthermore many active RC prototypes in the literature are suitable to be converted to MOSFET-C implementation (Czarnul and Tsividis, 1988). Moreover, an excellent collection of papers on continuous-time filters, mainly MOSFET-C and OTA/g_m -C filters, has been published in a single volume (Tsividis and Voorman, 1993).

In the literature, some second order all-pass filters using current conveyors in voltage mode were proposed (Pal, 1991; Pal and Singh, 1982; Soliman, 1999; Higashimura and Fukui, 1988). One of them employs two capacitors, four resistors and three current conveyors (Pal and Singh, 1982). The circuits in (Soliman, 1999; Higashimura and Fukui, 1988) use two capacitors, four resistors and a single second generation current conveyor.

Notch filters are needed to filter out the unwanted frequencies of an electrical signal. In the literature, some second order VM notch filters using current conveyor were proposed (Pal and Singh, 1982; Higashimura and Fukui, 1988; Soliman, 1999). One of

them employs two capacitors, four resistors and three current conveyors (Pal and Singh, 1982). The circuits in (Higashimura and Fukui, 1988; Soliman, 1999) use two capacitors, four resistors and a single current conveyor. In a recently published paper, an OTRA with two capacitors and four resistors are employed for realizing second order notch active filter (Cakir *et al*., 2005). The first generation current conveyor (Smith and Sedra, 1968) is also used in the implementation of second order all-pass/notch filter employing four resistors and two capacitors (Aronhime *et al.,* 1990).

These presented circuits in the literature use active and/or passive components more than necessary. Another contribution of this thesis is that several new filter circuits are presented to explain some important concepts in electronically tunable circuits. These circuits have reduced number of active and passive components and they are more suitable for IC realizations.

1.8. Thesis Plan

The thesis focuses on providing electronic tunability for the analog filters and finding new opportunities with respect to electronic tunable filters. The thesis consists of six chapters as shown in the flow chart in Fig. 1.1.

The first chapter of the thesis provides a background for the filters such as, historical review, classification and applications and components of the filters. Secondly, Chapter 2 introduces MOSFET-C technique, which is based on the following principle: MOSFETs replace passive resistors in special topologies such that their non-linearities are canceled and they provide electronic tunability. Chapter 3 reports the benefits of the mixed translinear loop based controlled conveyors and illustrates possible advantages of the first generation current conveyor over the second generation using new all-pass filters, a notch filter and a FDNR simulator circuits as examples. Also a relatively new active element found in 2004 based on the mixed translinear loop is examined in this chapter: The controlled CDBA (C-CDBA). A CMOS C-CDBA implementation is given and used in a new all-pass filter implementation. Chapter 4 introduces comparatively review on tunable all-pass filters using the OTA considering some trade-offs in analog design. Also two OTA-C and OTA-RC biquad filter examples are compared considering the linearity and

the tunability restrictions due to the frequency limitation of the g_m. Next, Chapter 5 reports the work on realization of electronic tunability with the current gain adjustment introducing a new active element denoted as electronically tunable DDCC (E-DDCC). In Chapters 2 and 3, passive resistors are replaced with controllable active components due to MOSFET based resistor or controlled conveyor, but in Chapter 5 the current-gain of the active element is used for tunability. Furthermore, it is shown that tunability range may be limited by stability constraints for an analog filter. A stability procedure is given and some MATLAB codes are developed to determine the tunability range restricted by stability conditions. The procedure given in this chapter can be used to evaluate the tunability range of a specific filter considering the limitations put by stability conditions. Chapter 6 provides a conclusion of the work done in the thesis and a comparison of the electronic tunability techniques. The chapters of the thesis have been titled as follows:

- Introduction
- Electronic tunability with MOSFET-C technique
- Electronic tunability with mixed translinear loops
- Electronic tunability with operational transconductance amplifiers
- Electronic tunability with adjusting current-gain
- Conclusions and scope of further research

A more detailed description of each chapter is given as follows:

Chapter 1 provides an introduction to the electrical filters such as, historical review, classification and applications and components used in the filters.

Chapter 2 examines the MOSFET-C technique. In this chapter, two MOSFET-C techniques are examined that do not need an active element consisting of many transistors. In the first technique, a special MOS resistive cell (MRC) is examined including a MOSFET and an inverting voltage amplifier (Acar and Ghausi, 1987). As a contribution of the thesis, we realized this MRC with three transistors for low-voltage and high frequency of operation. The advantages and detailed analysis of the new derived 3-transistor MRC are shown with a new electronically tunable all-pass filter example. The second technique

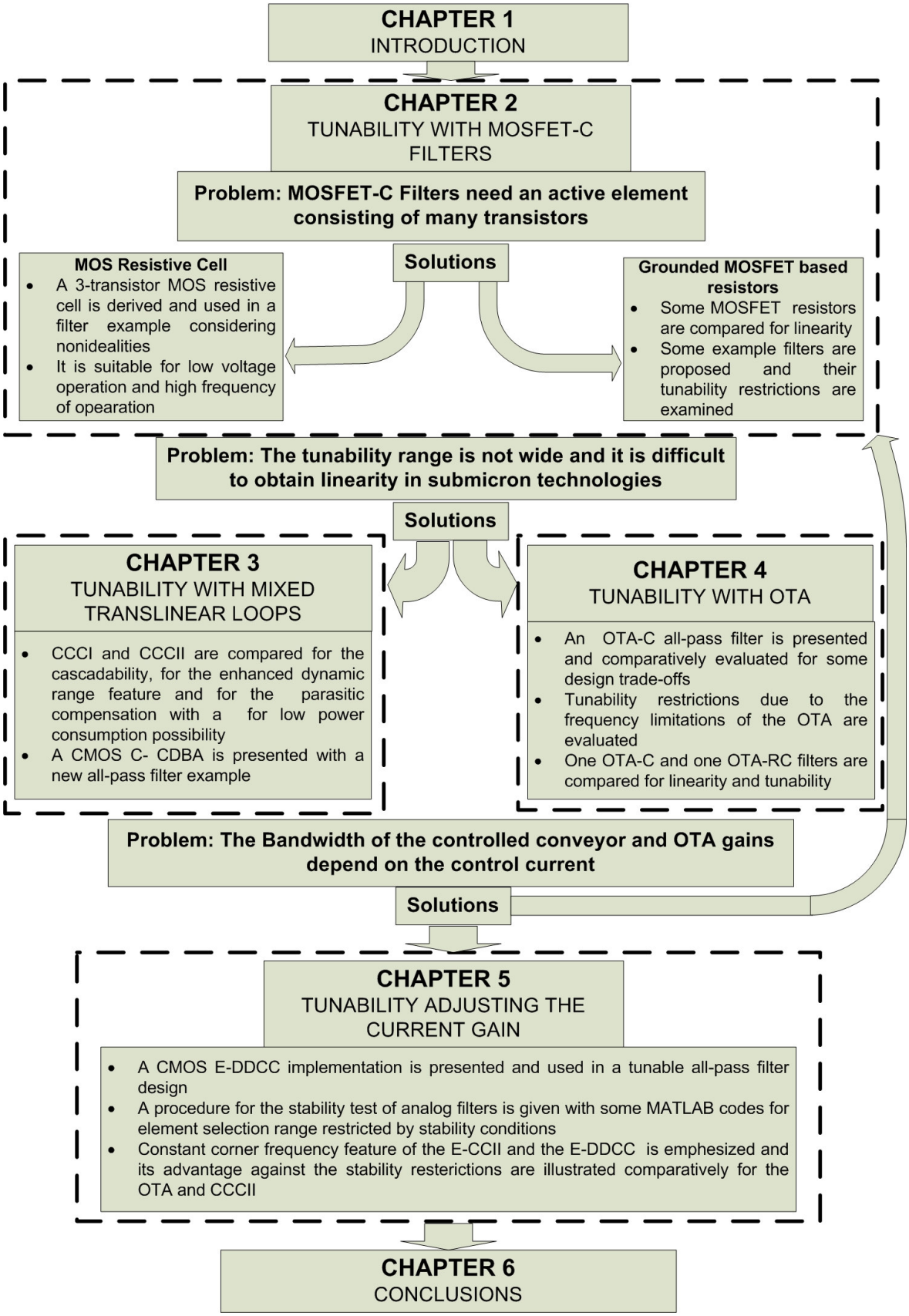


Figure 1.1. Flow-chart of the thesis

consists of replacing grounded resistors with MOS based electronic resistors. Some grounded MOSFET based resistors are compared for linearity and this approach is explained with new all-pass filter circuits, which are CCII based and DDCC based, with reduced active and passive elements. Moreover, the tunability restrictions of MOSFET-C filters are explained.

Chapter 3 focuses on mixed translinear loop based active elements such as controlled current conveyors. The current conveyor based circuits containing resistors in series to the X terminals can benefit the advantages of removing the resistors and switching the CCII to the CCCII, such as compensating active element non-idealities and electronic tunability. In Section 3.1, the principle of obtaining current controlled resistor using mixed translinear loop is described.

In Section 3.2, the advantage of controlled conveyor for tuning element-matching condition is presented with a new all-pass filter example (Metin *et al*., 2003). The matching conditions usually depend on the current and/or voltage gain of the current conveyors. It is very difficult to realize the actual matching conditions after manufacturing, because during IC implementation large deviations in gain parameters occur. Using tuning, deviations in the transfer function due to the non-idealities in the gain of the current conveyor can be compensated.

Then in Sections 3.3, 3.4 and 3.5, we focused on advantages of the first generation current conveyor over the second generation while examining electronic tunability with controlled conveyors. Having a high impedance Y terminal seems the evident advantage of the CCII over the CCI, because the CCII can be used in the design of cascadable VM filter easily. Nevertheless, in Section 3.3, it is shown that also the first generation current conveyor is able to provide high input impedance in some situations that the second generation cannot. In Section 3.4, a drawback of the cascadability using the Y terminal of the CCII with respect to dynamic range is emphasized and a second order tunable notch/all-pass filter is presented for enhanced dynamic range being compared with cascadable circuits from the literature. Therefore, in Sections 3.3 and 3.4, it is shown that the second generation current conveyor does not have a serious advantage over the first generation.

Section 3.5 illustrates a possible advantage of using the first generation current conveyor for reduced power consumption compared to the second generation. The controlled current conveyors are useful to provide electronic tunability for the circuits including a series resistor connected to the terminal X as described before. However, except this case, the parasitic resistance at the X terminal is desired to be ideally zero. In the controlled current conveyor, the simplest way to decrease the undesired parasitic resistor of the X terminal is to use sufficiently high biasing current, but this will increase the power consumption. On the other hand, there are some special current conveyor structures having very low parasitic resistance at the X terminal such as the circuit in (Awad and Soliman, 1999), but these are not current controlled type. The use of only one type of current conveyor simplifies the configuration (Higashimura and Fukui, 1996; Horng *et al.*, 1997). Therefore, if one of the conveyors is controlled current conveyor then for the others practically controlled conveyors with sufficiently high biasing currents are employed instead of standard conveyors. In fact, the CCI provides an easy method for compensating parasitic resistor in the X terminal derived from its terminal relationship. Furthermore, different from the CCII, the CCI does not need high biasing current to avoid undesired parasitic resistance at the X terminal, which is an important parameter for power consumption. Thus, in this section, an electronically tunable FDNR simulator example using controlled CCIs is presented to illustrate the parasitic compensation feature reducing power consumption.

In Section 3.6, beside popular active elements such as the controlled conveyor, another mixed-translinear cell based active element is examined. Maheshwari and Khan adapted mixed translinear loop in the CCCII to the CDBA with a BJT based implementation to obtain a controlled CDBA (Maheshwari and Khan, 2004). In the C-CDBA, the resistors in series with both input terminals N and P are electronically controllable similar to CCCII. In this part of the thesis, a CMOS implementation of the C-CDBA is presented. Moreover, the tunability and cascadability advantages of the C-CDBA are emphasized with a novel first order all-pass circuit.

In Chapter 4, the OTA is examined for electronic tunability. In Section 4.1, an OTA-C first-order all-pass filter is proposed and compared with other OTA-C first-order all-pass filters from the literature. During the comparison some trade-offs in analog design are

discussed. In Section 4.2, OTA-C and OTA-RC filters are comparatively examined for the tunability restrictions due to the frequency limitation of the g_m and for the linearity. The traditional philosophy in active filter design is to use op-amps with RC elements or to use OTAs with capacitors. However the advantages of using additional passive resistors and the reduction of the number of OTAs have not been examined in detail. Obvious advantages may be reduction in power consumption and noise but somewhat less obvious benefit may be linearity enhancement and increase in the tunability range.

Chapter 5 emphasizes another approach to the electronic tunability: Adjusting the current gain. In the controlled current conveyor and OTA based filters, the corner frequencies of the active element gains depend on the control currents. This variation in the corner frequency limits element selection range for the high frequency of operation and stability. In the literature there is an active element called electronically tunable current conveyor (E-CCII) where its current gain can be controlled externally with a constant corner frequency. We adapted the controlled current gain principle of the E-CCII to the DDCC, because the E-DDCC is a more general type active element and it can replace the current conveyor. The E-DDCC with a grounded resistor at its X terminal can even replace OTA because of differential voltage input terminals. Firstly we presented a CMOS E-DDCC internal structure, and used it in an all-pass filter application for electronic tunability.

Furthermore, Chapter 5 focuses on advantage of the constant corner frequency property in the evaluation of the filter stability, which limits the tunability range of the analog filters. A stability test procedure is given to determine element selection ranges of the elements restricted by stability problems. Also, some MATLAB codes are given to show element selection ranges in an easy interpretable graphical format. The procedure includes effects of biasing currents on the parasitic elements and the corner frequency of the gains of the OTA and CCCII.

Chapter 6 makes a conclusion and comparison of the work done in the previous chapters. Also presents some ideas for future research work.

2. ELECTRONIC TUNABILITY WITH MOSFET-C TECHNIQUE

In the CMOS technology, passive resistors occupy large areas on the integrated circuits. Also, they have limited values and high tolerances due to process variations in addition to large temperature coefficients. In these respects, it could be attractive to implement the resistors using MOS transistors. MOSFET-C filters consist of MOS transistors, capacitors, and active elements that are usually operational amplifiers. The MOSFETs are operated in the so-called triode region, where they can act as linear resistors. The MOS transistors serve the function of voltage-controlled resistors. Attractive features of MOSFET-C filters are their electronic tunability and their amenability to standard cell design (Tsividis *et al*., 1986). The electronic tunability is an important feature from IC realization point of view for fine adjustment against large manufacturing tolerances.

Different topologies and techniques are used in order to cancel out the effects of MOS transistor non-linearities in MOSFET-C filters. Some cancel the non-linearities in the current of the device; others cancel non-linearities in the sum or difference of the currents in two or more devices. In the classical approach as briefly explained in Section 2.1, the circuits are converted to balanced form to obtain symmetrical voltages on the resistors, with an advantage of improved common mode rejection ratio (CMRR) and noise rejection. However, this approach results in increase in the number of capacitors that cause excessive chip area. Hence, an integrator circuit is presented in (Czarnul, 1986) that does not need balanced form.

Theoretically, there is no restriction of MOSFET-C filters for high frequency of operation. However, well-known limitations of the op-amps cause difficulties in the operation of these filters. Therefore, in the thesis, we focused on techniques that do not need an active element consisting of many transistors. Also, illustrated approaches in the thesis do not require the circuits being converted to balanced forms:

(i) In the first technique, a special MOS resistive cell (MRC) is used consisting of a MOSFET operating in triode region and an inverting voltage amplifier. This MRC is implemented with three transistors in the thesis.

(ii) In the second approach, grounded resistors are replaced with MOSFET based resistors, where MOSFETs operate in saturation region.

In Section 2.2, we proposed a simple implementation of MRC block in (Acar and Ghausi, 1987) with only three transistors for low-voltage and high frequency of operation. The advantages and detailed analysis of the derived MRC are shown with a new electronically tunable first order all-pass filter example. Also, we proposed solutions to the non-idealities due to this replacement.

In Section 2.3, it is shown that how grounded resistors are replaced with MOSFET based resistors for electronic tunability is with three new all-pass filter examples. However, these resistance values may be restricted by the topology of the circuits. For example, in the filter of Section 2.3.1, the parasitic Z terminal resistance of the current conveyor limits the maximum value of the MOSFET based resistor in parallel. Then, in Section 2.3.2, two other filters are presented that do not have such a restriction.

2.1. Classical Approach: Linearized Integrator Blocks

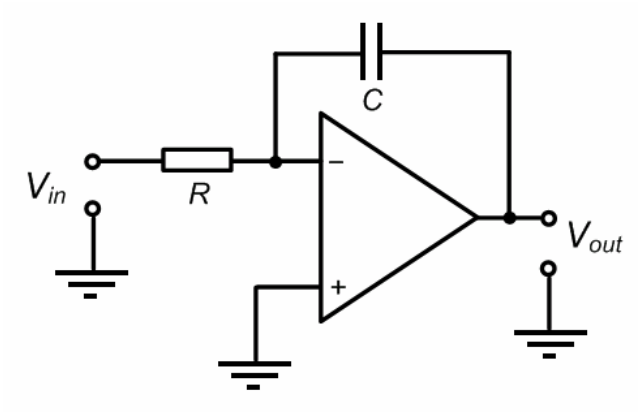
In this method linearized integrator blocks are used. If the integrator of Fig. 2.1(a) is converted to balanced form and the resistors are replaced by MOSFETs, the MOSFET-C integrator in Fig. 2.1(b) is obtained.

Banu and Tsividis (1983) explain how non-linearities of the MOSFETs are cancelled out. The drain current of an NMOS transistor in nonsaturation is

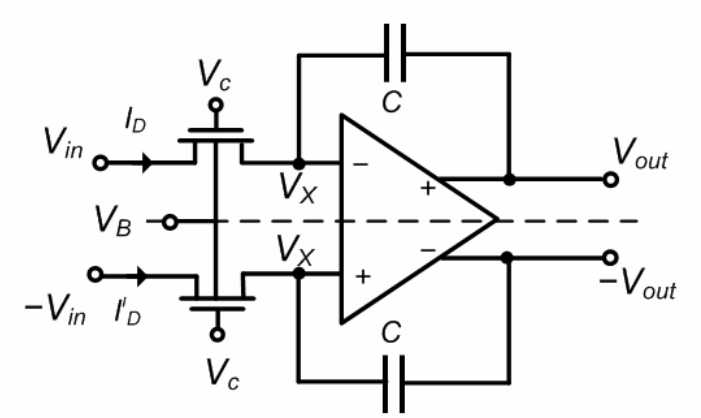
$$I_D = 2K_P \left\{ \begin{array}{l} (V_C - V_B - V_{FB} - \phi_B)(V_1 - V_2) - \frac{1}{2}\left[(V_1 - V_B)^2 - (V_2 - V_B)^2\right] - \\ \frac{2}{3}\gamma\left[(V_1 - V_B + \phi_B)^{3/2} - (V_2 - V_B + \phi_B)^{3/2}\right] \end{array} \right\} \qquad (2.1a)$$

$$\gamma = \frac{1}{C_{OX}}\sqrt{2qN_A\varepsilon_S} \tag{2.1b}$$

$$K_P = \frac{1}{2}\mu\, C_{OX}\frac{W}{L} \tag{2.1c}$$



(a)



(b)

Figure 2.1. (a) An active-RC integrator (b) The MOSFET-C integrator

where I_D is the drain current in the triode region, V_C, V_B, V_1, V_2 are the gate, substrate, drain, and source potentials with respect to ground, W and L are the channel width and length, μ is the carrier effective mobility in the channel, V_{FB} is the flat-band voltage, C_{OX} is the gate oxide capacitance per unit area, ε_S is the silicon dielectric constant (1.04 pF/cm), q is the electron charge and Φ_B is the approximate surface potential in strong inversion for zero backgate bias (classically, this potential has been taken to be $2\Phi_F$, with Φ_F being the Fermi potential (Banu and Tsividis, 1983). N_A is the doping concentration of the p-type

substrate. The fabrication process parameter γ' has the dimension of $\gamma'^{1/2}$ and is typically $0.5V^{1/2}$ (Sedra and Smith, 1998). The 3/2 power terms in (2.1a) can be expanded in Taylor series with respect to V_1 and V_2, which keeps the device in triode region. Then (2.1a) can be written in the general form as,

$$I_D = K_P\left[a_1(V_1 - V_2) + a_2(V_1^2 - V_2^2) + a_3(V_1^3 - V_2^3) + a_4(V_1^4 - V_2^4) + ...\right] \tag{2.2}$$

where the coefficients a_is (i=1, 2, 3…) are independent of V_1, V_2 and these coefficients are the functions of the gate and substrate potentials (V_C and V_B) and the process and physical parameters of the transistor.

The inverse of ($K_P a_1$) is the small-signal resistance R of the transistor; it can be shown that

$$R = \frac{1}{K_P a_1} = \left[\mu C_{OX}\frac{W}{L}(V_C - V_{Th})\right]^{-1} \tag{2.3}$$

where V_{Th} is the threshold voltage corresponding to $-V_B$ bulk bias. The value of R may be varied with V_C (henceforth called the control voltage); therefore, for small signals, the MOSFET can be used as a voltage-controlled resistor.

Firstly, consider replacing the resistor in Fig. 2.1(a) with a MOSFET whose small-signal channel resistance is R. Using the relation (2.2) with $K_P a_1 = 1/R$ we have

$$V_{out}(t) = -\frac{1}{RC}\int_{-\infty}^{t} V_{in}dt - \frac{K_P}{C}\int_{-\infty}^{t}(a_2 V_{in}^2 + a_3 V_{in}^3 + \ldots)dt \tag{2.4}$$

The first term in (2.4) represents the ideal response of the active RC integrator and the second one represents the error due to MOSFET non-linearities. For large signals, this error term in the output becomes significant and produces excessive second order harmonic distortion, which limits the dynamic range (Banu and Tsividis, 1983).

Secondly, the fully balanced integrator in Fig. 2.1(b) will be analyzed. The cancellation of second order term in (2.4) can be accomplished by a fully balanced integrator in Fig. 2.1(b). Assuming infinite op-amp gain and zero offset voltage, the two input terminals of the op-amp are at the same potential, V_X. Writing the KVL equations for the two output terminals, we have,

$$V_{out}(t) = -\frac{1}{C}\int_{-\infty}^{t} I_D dt + V_X \tag{2.5a}$$

$$-V_{out}(t) = -\frac{1}{C}\int_{-\infty}^{t} I'_D dt + V_X \tag{2.5b}$$

The solution for V_{out} is obtained by subtracting (2.5b) from (2.5a):

$$V_{out}(t) = -\frac{1}{2C}\int_{-\infty}^{t} (I_D - I'_D) dt \tag{2.6}$$

The values of the currents I_D and I'_D are given according to (2.2):

$$I_D = K_P\left[a_1(V_{in} - V_X) + a_2(V_{in}^2 - V_X^2) + a_3(V_{in}^3 - V_X^3) + ...\right] \tag{2.7a}$$

$$I'_D = K_P\left[a_1((-V_{in}) - V_X) + a_2((-V_{in})^2 - V_X^2) + a_3((-V_{in})^3 - V_X^3) + ...\right] \tag{2.7b}$$

When (2.7b) is subtracted from (2.7a), all the even order terms in V_X and all the terms in V_{in} are canceled out:

$$I_D - I'_D = 2K_P\left[a_1 V_{in} + a_3 V_{in}^3 + a_5 V_{in}^5 + ...\right] \tag{2.8}$$

Since the high-order non-linear terms such as a_3 and a_5 are much smaller than the linear term a_1, the right-hand side of (2.8) is practically linear in V_{in}. Using (2.8) in (2.6), we obtain

$$V_{out}(t) \cong -\frac{1}{RC}\int_{-\infty}^{t} V_{in}\,dt \tag{2.9}$$

Consequently, in this technique, each integrator block is individually linearized.

2.2. Acar-Ghausi Technique

In the previous section, it is shown that the resistors are replaced with MOSFETs in some special topologies such that non-linearities due to MOSFETs are canceled. In this classical MOSFET-C approach, the filters are composed of balanced integrator blocks where each of them is individually linearized. This approach however results circuits with large component count. Moreover, these special topologies require active elements, such as op-amps consisting of many transistors. However, in this section, we presented a three-transistor MOS resistive cell (MRC) derived from (Acar and Ghausi, 1987).

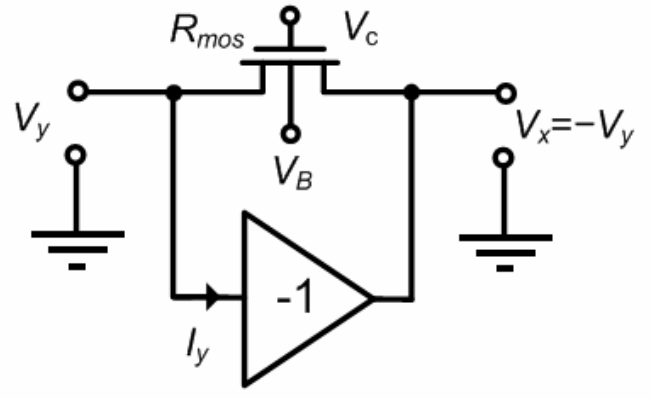


Figure 2.2. The MOS resistive cell (MRC) for canceling even order non-linearities of the MOS transistor

As an alternative approach to the balanced design, Acar and Ghausi presented a simple technique for cancellation of non-linearities. In this technique a unity gain inverting voltage buffer (IVB) cancels out even order non-linearities of a MOS transistor that is in parallel to itself (Acar and Ghausi, 1987). The MOS resistive cell is shown in Fig. 2.2. Here, the IVB is characterized with the following equations:

$$V_x = -V_y \qquad I_y = 0 \tag{2.10}$$

The IVB provides opposite signals at the drain and source of the MOSFET, so even order terms in its drain current are cancelled out in nonsaturation as given by (2.2). Therefore, a voltage controlled linear MOS resistor is obtained. If the resistance of the MOSFET based electronic resistor is represented by R_{mos}, the drain current will be equal to $I_D = 2V_1/R_{mos}$. Then the R_{mos} value can be given as follows,

$$R_{mos} = \frac{1}{K_P a_1} = \frac{L}{\mu C_{OX} W (V_C - V_{Th})} \tag{2.11}$$

2.2.1. A Tunable MOSFET-C All-pass Filter for Low Voltage Operation

In this section, we propose a new all-pass filter using only three MOS transistors two resistors and one capacitor, providing electronic tunability. The circuit is also very suitable for low voltage operation, since it uses only two MOS transistors between its rails. Also the presented circuit is expected to consume less power compared to current conveyor based all-pass circuits employing larger number of transistors. The functionality of the proposed circuit is verified with experiments and SPICE simulations.

The presented circuit is given in the Fig. 2.3(a). The MOS transistors M_1 and M_2 in Fig. 2.3(b) implement the IVB of the MRC. The routine analysis of the proposed circuit in Fig. 2.3(a) gives the voltage transfer function as,

$$\frac{V_o}{V_i} = \frac{-sCR_1R_{mos} + R_2(2 + sCR_{mos})}{(R_1 + R_2)(2 + sCR_{mos})} \tag{2.12}$$

It is possible to match resistors with much better precision than 0.1 per cent in the IC technology (Gray and Meyer, 1993). For the element matching condition of $R_1 = 2R_2$, a first order all-pass transfer function is obtained,

$$\frac{V_o}{V_i} = \frac{1}{3}\ \frac{1 - sCR_{mos}/2}{1 + sCR_{mos}/2} \tag{2.13}$$

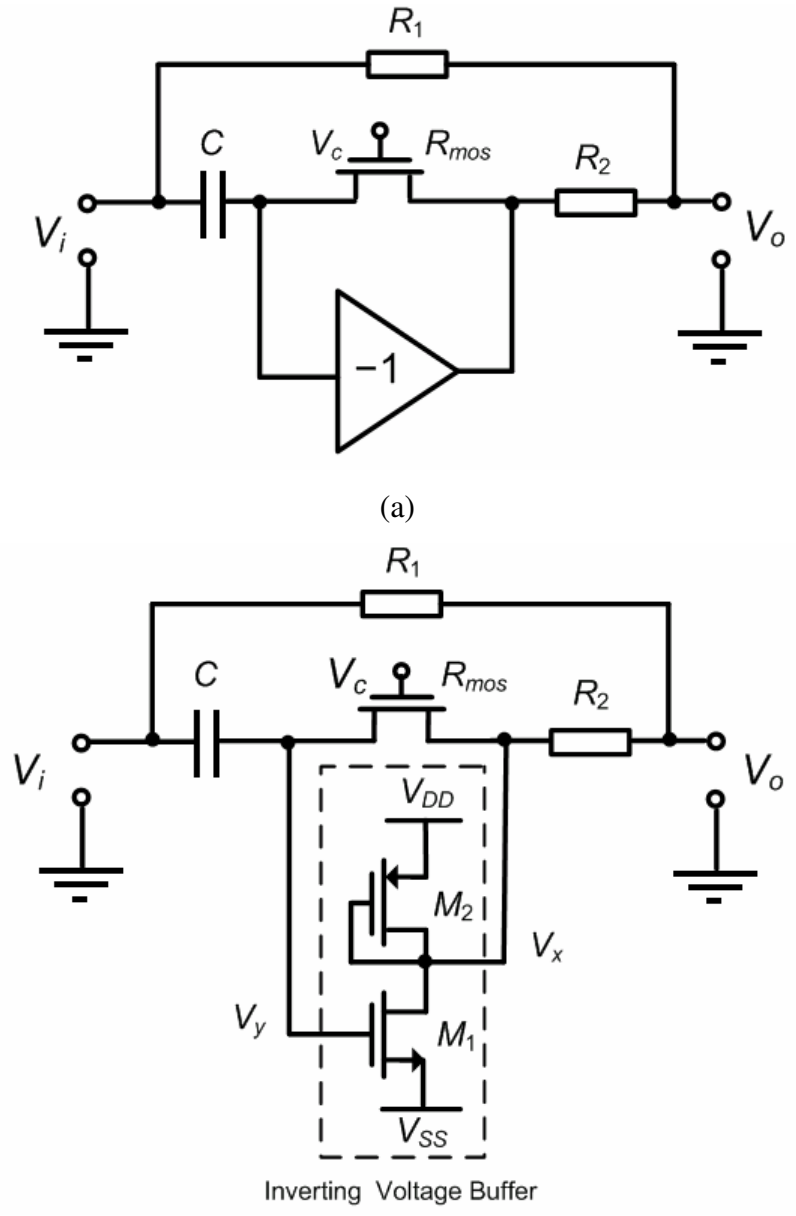


Figure 2.3. (a) The presented MOSFET-C all-pass filter (b) A possible CMOS implementation

2.2.2. Compensating the Effect of the Output Impedance

The presented three-transistor MRC implementation adapts MOSFET-C technique to low-power technology. However, this simple MRC has an important non-ideality affecting the characteristics of the circuits: Non-zero output resistance of the IVB. To compensate

the effect of this parasitic output resistance, we proposed to change two parameters of the circuit such as the gain of the IVB and resistor matching ratios.

2.2.2.1. Compensation with the Gain of the Inverting Voltage Buffer. Firstly, the gain parameter of the IVB is used to compensate for the unwanted effects of the parasitic output resistance. Denoting the parasitic output resistance of the active element in Fig. 2.4 as R_O, the transfer function can be given for the case $R_1 = 2R_2$,

$$\frac{V_o}{V_i} = \frac{R_O(1+sCR_{mos}) + R_2(1+k+sCR_{mos}(1-2k)+3sCR_O)}{R_O(1+sCR_{mos}) + 3R_2(1+k+sC(R_{mos}+R_O))} \tag{2.14}$$

here, k is the gain of the IVB. For a nonzero R_O, a k value can be calculated to achieve an all-pass filter response as follows,

$$k = \frac{R_O}{R_{mos}} + \frac{R_O}{6R_2} + \frac{\sqrt{13R_O^2R_{mos}^2 + 48R_OR_2R_{mos}(R_O+R_{mos}) + 36R_2^2(R_O+R_{mos})^2}}{6R_2R_{mos}} \tag{2.15}$$

The graphical representation of k can be given in Fig. 2.5 for various R_{mos} and R_O values for R_2=10kΩ and R_2=1kΩ. Figure 2.5 shows that choosing a k value appropriately can compensate for the unwanted effects of the R_O.

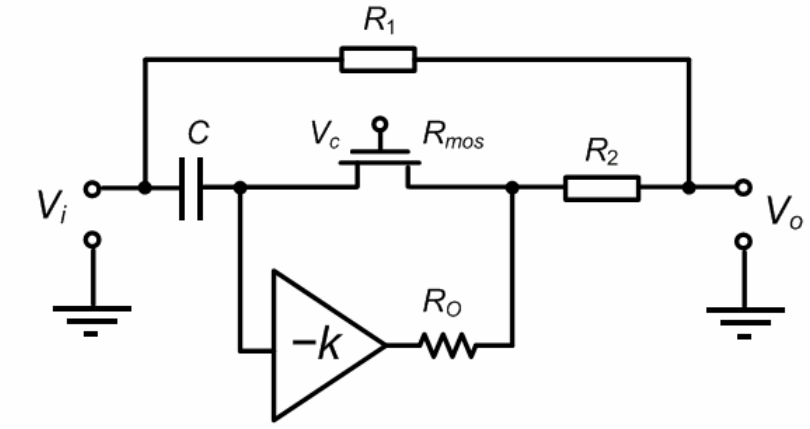


Figure 2.4. The compensation for the unwanted effect of the R_O by choosing a proper gain value k

2.2.2.2. Compensation with the Resistor Matching Ratio. Secondly, a resistor-matching ratio is used to compensate for undesired effects of the nonzero R_O to achieve an all-pass response. The new transfer function of the circuit in Fig. 2.6 for the element matching condition of $R_1 = mR_2$ can be calculated considering R_O in Fig. 2.6 as,

$$\frac{V_o}{V_i} = \frac{R_O + R_2(2 + sC(1+m)R_O) + sCR_{mos}(R_2 - mR_2 + R_O)}{R_O + R_2(1+m)(2 + sCR_O) + sCR_{mos}(R_2 + mR_2 + R_O)} \tag{2.16}$$

The resistor matching ratio m that results an all-pass response is given below,

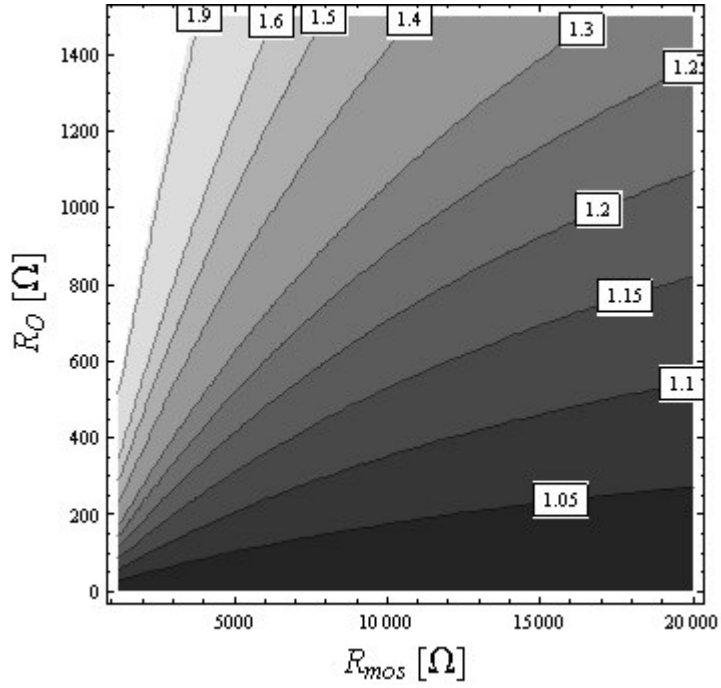
$$m = \frac{3R_2R_O + R_O^2 + (R_2 + R_O)R_{mos} + \sqrt{R_O^2(R_2 + R_O)^2 + R_{mos}(6R_2^2R_O - 2R_O^3 + (R_2 + R_O)(9R_2 + 5R_O)R_{mos})}}{2R_2(R_{mos} - R_O)} \tag{2.17}$$

For various R_{mos} and R_O values, the graphical representation of m can be given in Fig. 2.7 for R_2=10kΩ and R_2=1kΩ. Figure 2.7 illustrates how to select an m value for a proper design compensate for the effect of the R_O.

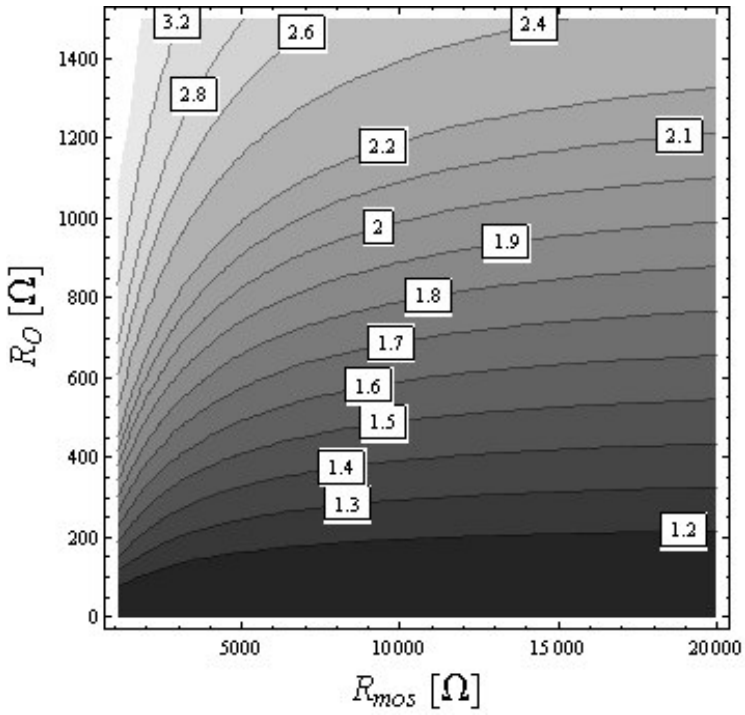
As a summary, both methods can be used to compensate the unwanted effect of the output resistance of the active device. The technique in Section 2.2.2.1 is more convenient than the one in this section, because changing the gain of the IVB is easier than the resistor matching operation. Therefore, the first method is used in the simulations and the experiment.

2.2.3. Limitations of the Input Signal and the Control Voltage

To employ the MOSFET in MRC as a linear resistor, the terminal and control voltages of the MOSFET must keep it in non-saturation region. Thus, the terminal voltages of the MRC V_y, V_x must satisfy the following conditions in Fig. 2.2,



(a)



(b)

Figure 2.5. Optimum gain value k (constant k-value curves) for the circuit in Fig. 2.4 (to preserve the all-pass response) versus R_{mos} and R_O (a) For R_2=10kΩ (b) For R_2=1kΩ

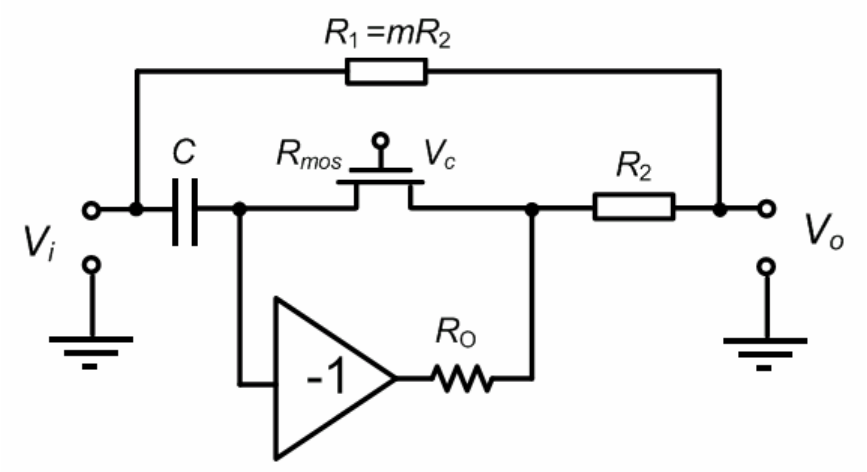


Figure 2.6. The compensation for the unwanted effect of R_O with a proper resistor-matching ratio m

$$V_x = -V_y \tag{2.18a}$$

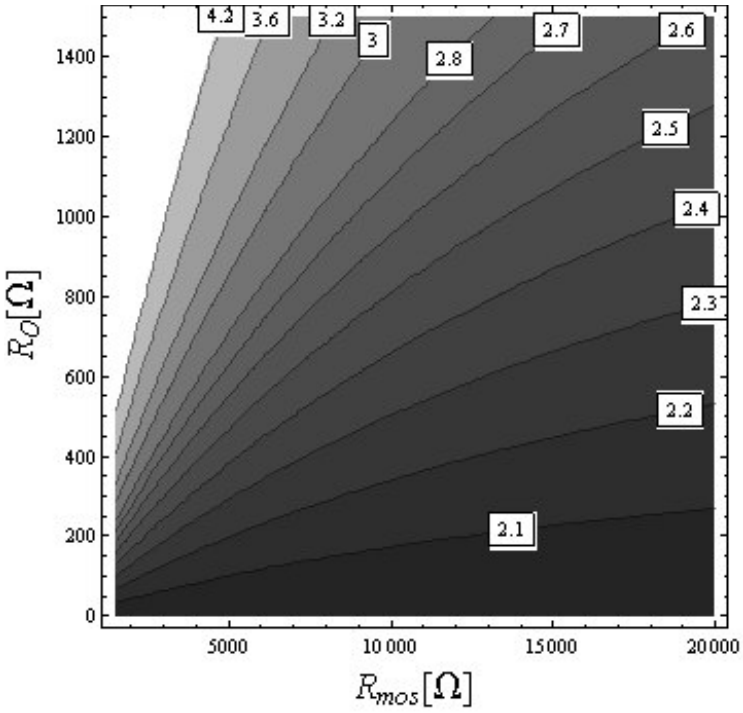
$$V_B \le V_y \tag{2.18b}$$

$$V_y \le V_C - V_{Th} \tag{2.18c}$$

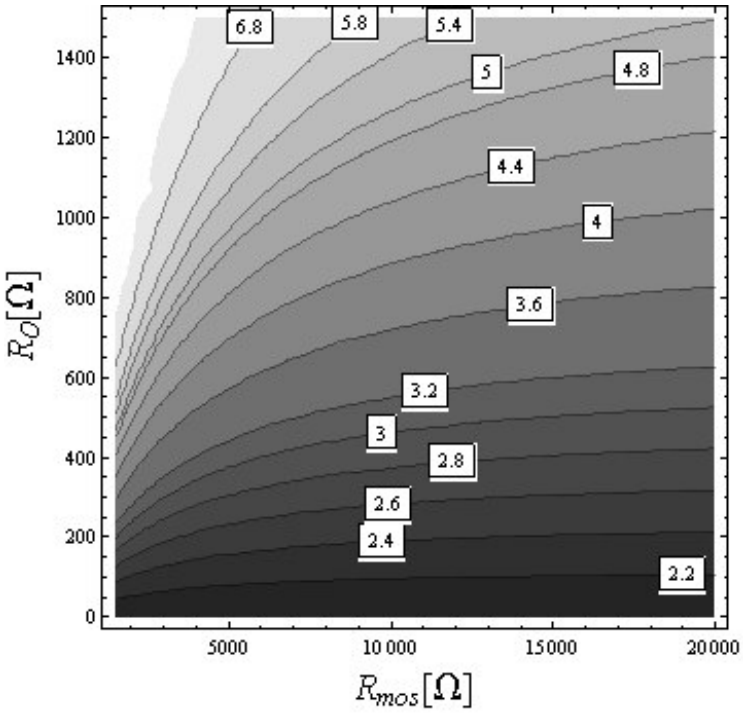
$$V_{Th} = V_{Th0} + \gamma'(\sqrt{2\Phi_f + V_B} - \sqrt{2\Phi_f}) \tag{2.18d}$$

where V_{Th0} is the threshold voltage for V_B = 0; Φ_f is a physical parameter with ($2\Phi_f$) typically 0.6V; γ' is a fabrication-process parameter given in (2.1b). (Sedra and Smith, 1998).

It is clear that the conditions in (2.18) will impose a limitation on the filter's input signal amplitude V_i, such as $\left|V_y(j\omega)\right| \le V_m$, where $V_m = \min\{|V_C - V_{Th}|, |V_B|\}$ and magnitude of the voltage at the terminal of the MRC is $|V_y(j\omega)| = (R_{mos}^2 C^2 \omega^2 / 4 + R_{mos}^2 C^2 \omega^2) V_i$. Thus, (2.18) yields the condition of considering V_y in Fig. 2.2.



(a)



(b)

Figure 2.7. Optimum resistor-matching value m (constant m-value curves) for the circuit in Fig. 2.6 (to preserve all-pass response) versus R_{mos} and R_O (a) For R_2=10kΩ (b) For R_2=1kΩ

$$V_i \le V_m \frac{4 + R_{mos}^2 C^2 \omega^2}{R_{mos}^2 C^2 \omega^2} \tag{2.19}$$

Equation (2.19) shows that the input signal limitation is $V_i \le V_m$ at the sufficiently high frequency region.

2.2.4. Simulation and Experimental Results

To verify the theoretical analyses, the proposed circuit in Fig. 2.3(b) is simulated using the SPICE circuit simulation program. The M_1 and M_2 transistors in Fig. 2.3(b) are used to implement the IVB in Fig. 2.3(a). The supply voltages are V_{DD}=1.5V and V_{SS} = −1.25V. For the simulations, 0.35µm CMOS real process (level 49) parameters from TSMC in Table 2.1 are used. The dimensions of the M_1 and M_2 are chosen respectively as (W_1=30µm, L_1=0.5µm) and (W_2=60µm, L_2=0.5µm) to obtain an IVB with an appropriate voltage gain compensating the effect of the R_O. The passive element values are C=5pF, R_1=20kΩ, and R_2=10kΩ. The NMOS based resistor, R_{mos}, (W=2µm, L=2µm) is biased with the control voltages of V_C=1.25V, V_C=1.75V, V_C=3.25V to produce R_{mos}=15.6kΩ, R_{mos}=7.7kΩ, and R_{mos}=3.8kΩ resistance values respectively. Theoretical and simulated gain and phase responses and electronic tunability of the circuit with V_C are shown in Fig. 2.8. The pole frequency of the presented circuit is changed between 4MHz and 16.8MHz successfully. Furthermore to show non-linearity cancellation, total harmonic distortion values are found for the sinusoidal input signal amplitudes with peak value of 0.5V, 1V and 1.5V at 150kHz, 300kHz, 450kHz and 600kHz as shown in Fig. 2.9. Simulation results agree quite well with the theoretical analysis.

We have also tested the performance of the proposed circuit in Fig. 2.3(b) experimentally. For the purpose, the circuit is realized using 4007 MOS transistor arrays. To obtain a gain value of $k \cong +1.4$ compensating for the effect of the R_O, the M_2 is realized with a series of two PMOS transistors due to the fixed transistor sizes of the 4007. For this reason, the supply voltages V_{DD} and V_{SS} are respectively selected as 5.15V and −4.30V to avoid offset at the output of the IVB. The capacitor and resistor values are chosen as C=10nF, R_1=200kΩ, and R_2=100kΩ.

Table 2.1. TSMC 0.35μm MOSFET BSIM3v2 SPICE Parameters

TSMC 0.35μm MOSFET BSIM3v2 (Level 49) model from MOSIS
.MODEL CMOSN NMOS (LEVEL = 49 +VERSION = 3.1 TNOM = 27 TOX = 7.7E-9 XJ = 1E-7 NCH = 2.3579E17 +K1 = +0.5542796 +K2 = 0.0155863 K3 = 2.3475646 VTH0 = 0.5048265 +K3B = -3.3142916 W0 = 4.145888E-5 NLX = 1.430868E-7 DVT0W = 0 DVT1W = 0 + DVT2W = 0 DVT0 = -0.0150839 DVT1 = 1.51022E-3 DVT2 = 0.170688 +U0 = 415.8570638 UA = 5.057324E-11 UB = 1.496793E-18 UC = 2.986268E-11 +VSAT = 1.237033E5 A0 = 0.9098788 AGS = 0.2120181 B0 = 1.683612E-6 B1 = 5E-6 +KETA = -4.011887E-4 A1 = 0 A2 = 1 RDSW = 1.156967E3 PRWG = -8.468558E-3 +PRWB = -7.678669E-3 WR = 1 WINT = 5.621821E-8 LINT = 1.606205E-8 +XL = -2E-8 XW = 0 DWG = -6.450939E-9 DWB = 6.530228E-9 VOFF = -0.1259348 +NFACTOR = 0.3344887 CIT = 0 CDSC = 1.527511E-3 CDSCD = 0 +CDSCB = 0 ETA0 = 1.21138E-3 ETAB = -1.520242E-4 DSUB = 0.1259886 +PCLM = 0.8254768 PDIBLC1 = 0.4211084 PDIBLC2 = 6.081164E-3 PDIBLCB =-5.865856E-6 +DROUT = 0.7022263 PSCBE1 = 7.238634E9 PSCBE2 = 5E-10 PVAG = 0.6261655 +DELTA = 0.01 MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 +KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 +WLN = 1 WW = -1.22182E-15 WWN = 1.137 WWL = 0 LL = 0 LLN = 1 +LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.4 CGDO = 3.5E-10 +CGSO = 3.5E-10 CGBO = 0 CJ = 8.829973E-4 PB = 0.7946332 MJ = 0.3539285 + CJSW = 2.992362E-10 PBSW = 0.9890846 MJSW = 0.1871372 PVTH0 = -0.0148617 +PRDSW = -114.7860236 PK2 = -5.151187E-3 WKETA = 5.687313E-3 +LKETA = -0.018518)
.MODEL CMOSP PMOS (LEVEL = 49 +VERSION = 3.1 TNOM = 27 TOX = 7.7E-9 XJ = 1E-7 NCH = 8.52E16 VTH0 = -0.6897992 +K1 = 0.4134289 K2 = -5.342989E-3 K3 = 24.8361788 K3B = -1.4390847 W0 = 2.467689E-6 +NLX = 3.096223E-7 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.3209807 +DVT1 = 0.4695965 DVT2 = -8.790762E-4 U0 = 150.6275733 UA = 2.016943E-10 +UB = 1.714919E-18 UC = -1.36948E-11 VSAT = 9.559222E4 A0 = 0.9871247 +AGS = 0.3541967 B0 = 3.188091E-6 B1 = 5E-6 KETA = -0.0169877 A1 = 0 A2 = 1 +RDSW = 2.443009E3 PRWG = 0.0260616 PRWB = 0.141561 WR = 1 WINT = 5.038936E-8 +LINT = 1.650588E-9 XL = -2E-8 XW = 0 DWG = -1.535456E-8 DWB = 1.256904E-8 +VOFF = -0.15 NFACTOR = 1.5460516 CIT = 0 CDSC = 1.413317E-4 CDSCD = 0 +CDSCB = 0 ETA0 = 0.3751392 ETAB = 2.343374E-3 DSUB = 0.8877574 PCLM = 5.8638076 +PDIBLC1 = 1.05224E-3 PDIBLC2 = 3.481753E-5 PDIBLCB = 2.37525E-3 + DROUT= 0.0277454 +PSCBE1 = 3.013379E10 PSCBE2 = 3.608179E-8 PVAG = 3.9564294 DELTA = 0.01 +MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 +UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = -5.22182E-16 +WWN = 1.125 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 +XPART = 0.4 CGDO = 3.02E-10 CGSO = 3.02E-10 CGBO = 0 CJ = 1.397645E-3 +PB = 0.99 MJ = 0.5574537 CJSW = 3.665392E-10 PBSW = 0.99 MJSW = 0.3399328 +PVTH0 = 0.0114364 PRDSW = 52.7951169 PK2 = 9.714153E-4 WKETA = 0.0109418 +LKETA = 7.702974E-3)

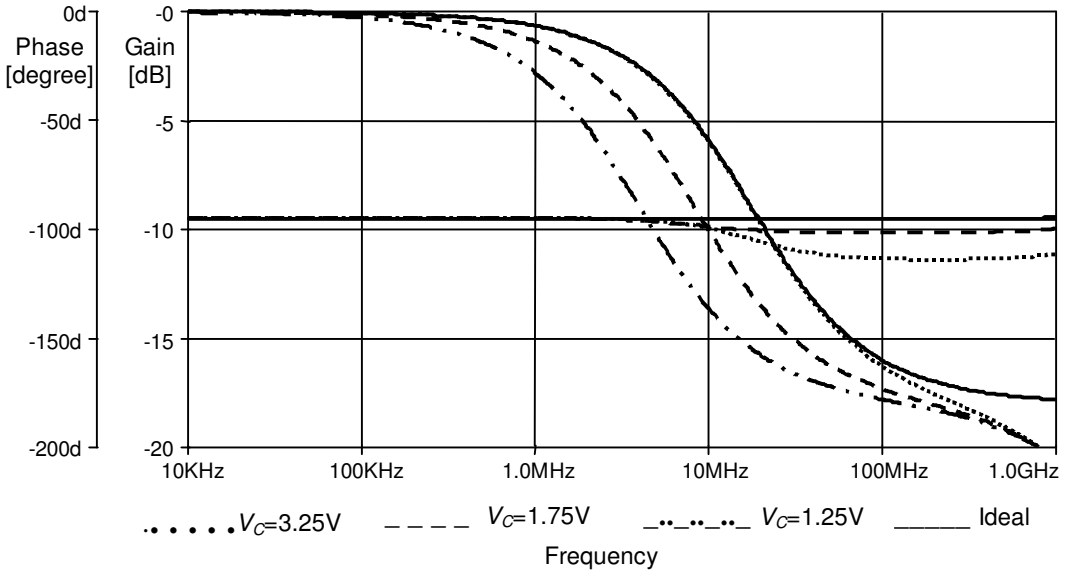


Figure 2.8. Simulation results to illustrate the tunability of the pole frequency with control voltage V_C

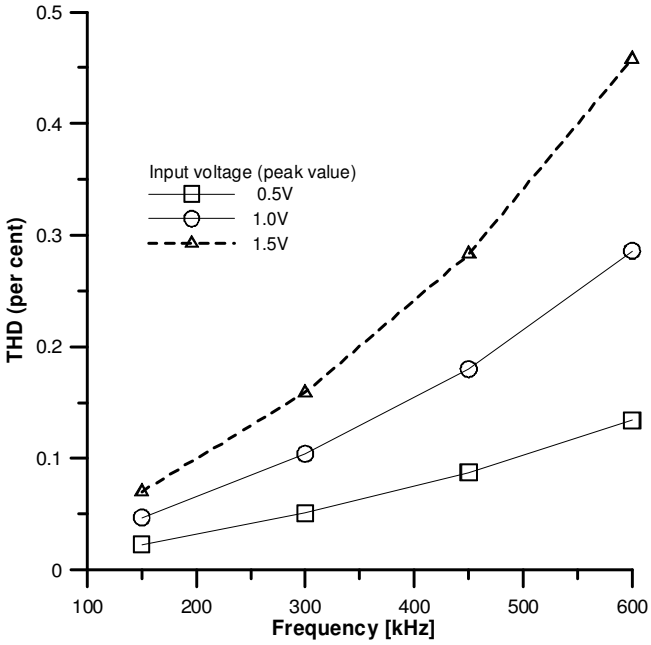


Figure 2.9. THD values for various input signal amplitudes between 150kHz and 600kHz

The bulk of the R_{mos} NMOS transistor is connected to V_{SS}. The measured gain and phase responses are depicted in Fig. 2.10. The phase responses are depicted for three

different control voltages, V_C =4.66V, V_C =5V and V_C =5.66V and the gain response is depicted for V_C =5.66V.

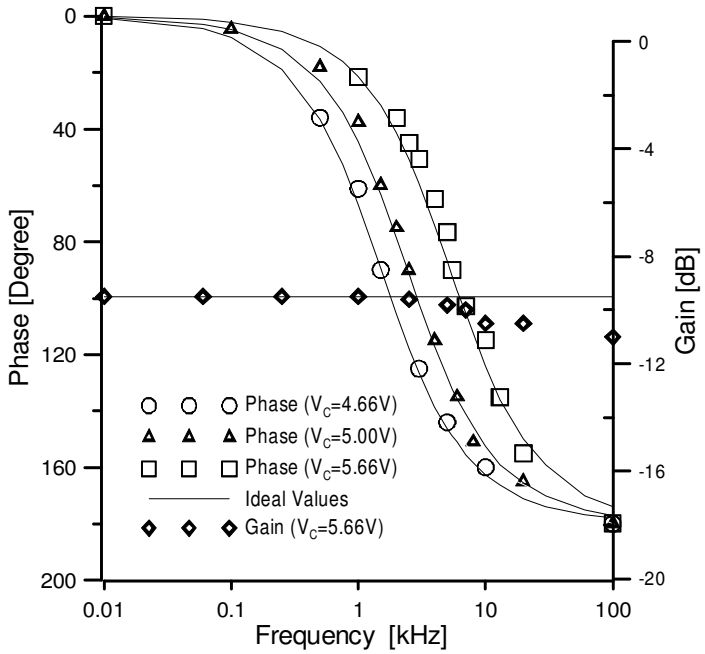


Figure 2.10. The experimental phase and gain responses to illustrate electronic tunability

2.3. Replacing Grounded Resistors with MOSFET Based Electronic Resistors

In this section, a well-known method for replacement of grounded resistors by MOSFET based resistors is examined with some new all-pass filter examples. Firstly, some MOSFET based resistors realizations are compared in terms of linearity and the most suitable one is chosen. Exploiting the advantage of the electronic resistors is possible with large resistor values. However, these resistance values may be limited by parasitic terminal resistances of the active elements. In Section 2.3.1, two all-pass filters are presented describing this topic. Then, in Section 2.3.2, two other filters are presented that do not have such a restriction.

Bilotti (1966) firstly showed use of a MOS transistor as a grounded non-linear resistor. Then, some MOSFET based resistor circuits were presented such as (Babanezhad and Temes, 1984; Han and Park, 1984; Wilson and Chan, 1989; Wang, 1990a; Wang, 1990b; Al-Ruwaihi and Noras, 1994). The MOSFET based resistors in (Babanezhad and Temes, 1984; Han and Park, 1984) have the inconvenience of using MOS depletion

transistors. The MOSFET based resistor circuits in (Wilson and Chan, 1989; Wang, 1990a; Wang, 1990b; Al-Ruwaihi and Noras, 1994) are compared for linearity in this section. In the simulations, the (W/L) ratios are chosen from original works and they are modified for the 0.35μm technology from TSMC to obtain resistor value of 3.65kΩ with suitable control voltages. Level 49 SPICE parameters are used in the simulations. In Fig. 2.11(a) (Wilson and Chan, 1989), the transistor aspect ratios are $(W/L)_{N1}=(W/L)_{N2}=0.7\mu m/5\mu m$, $(W/L)_{N3}=1.3\mu m/5\mu m$, $(W/L)_{N4}=1.3\mu m/5\mu m$, $(W/L)_{N5}=(W/L)_{N6}=7\mu m/1\mu m$, $(W/L)_{N7}=11\mu m/5\mu m$, $(W/L)_{P1}=(W/L)_{P2}=8\mu m/1\mu m$. V_B, V_{SS} and V_{DD} are respectively –1.8V, –2.5V and 2.5V. The control voltage V_C is chosen as 2V. For the circuit in Fig. 2.11(b) (Wang, 1990b), the transistor aspect ratios are $(W/L)_{N1}=(W/L)_{N2}=1.7\mu m/2.1\mu m$. The control voltage V_C is 2.45V. For the circuit in Fig. 2.11(c) (Wang, 1990a), the transistor aspect ratios are $(W/L)_{N1}=1\mu m/2.1\mu m$, $(W/L)_{N2}=(W/L)_{N3}=2\mu m/2.1\mu m$ and $(W/L)_{P1}=(W/L)_{P2}=6.1\mu m/2.1\mu m$. The V_C is 2.31V for the circuit in Fig. 2.11(d) (Al-Ruwaihi and Noras, 1994), the transistor sizes are W=1.65μm and L=2.1μm. The control voltage V_C is chosen as 12V. The linearity comparison of the MOSFET based resistors in Fig. 2.11 is given in Fig. 2.12. Sinusoidal signals with various amplitudes at 1kHz are applied to the electronic resistors. THD values of the current flowing on them are calculated using HSPICE simulations. The simulation results show that the resistor implementation in Fig. 2.11(b) (Wang, 1990b) has better linearity compared to others. The circuit in Fig. 2.11(b) consists of less number of transistors compared to others in Fig. 2.11(a), 2.11(c) and 2.11(d). “There is neither an offset nor a non-linearity component at all in the output of this circuit” (Wang, 1990b). The circuits in (Wilson and Chan, 1989; Wang, 1990a; Al-Ruwaihi and Noras, 1994) are based on the principle of minimizing non-linearity component or offset at the output. Therefore, the circuit in (Wang, 1990b) is chosen and used in circuits of the following sections due to its simplicity and better linearity.

In the MOSFET based resistor circuit in Fig. 2.11(b) (Wang, 1990b), the two MOS transistors are operating in saturation region. The matched transistors M_1 and M_2 are diode connected. A voltage V_{in} is applied to the central node of the circuit, developing a current I_{in} into the node. Using the square law characteristic, the drain currents in M_1 and M_2 can be expressed as,

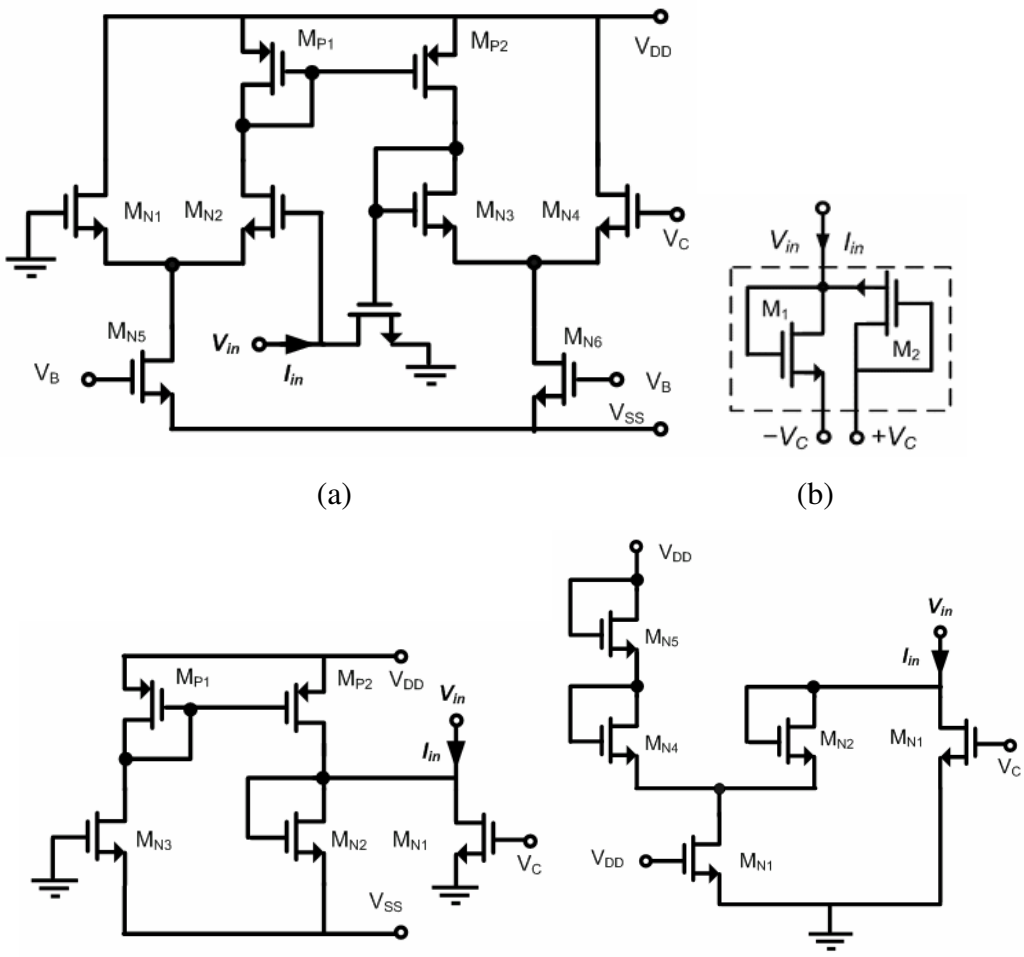


Figure 2.11. Various MOSFET based electronic resistor implementations (a) Wilson and Chan, 1989 (b) Wang, 1990b (c) Wang, 1990a (d) Al-Ruwaihi and Noras, 1994

$$I_{D1} = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_{in} - (-V_C) - V_{Th})^2 \tag{2.20a}$$

$$I_{D2} = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_C - V_{in} - V_{Th})^2 \tag{2.20b}$$

where μ is carrier mobility, C_{OX} is the gate capacitance per unit area, V_{Th} is the threshold voltage and W and L are the channel length and width, respectively. Using Kirchhoff's current law (KCL) and (2.20a) and (2.20b), the equivalent resistance, R_{mos} can be described as,

$$R_{mos} = \frac{V_{in}}{I_{in}} = \frac{L}{2\mu C_{OX} W (V_C - V_{Th})} \tag{2.21}$$

Equation (2.21) is applicable when both MOS transistors remain in the saturation region, which is true if $|V_{in}| < (V_C - V_{Th})$ (Wang, 1990b). Also, "The magnitude of V_{in} is allowed to vary within the free range of supply voltages without significant percentage changes in linearity, thus reaching the maximum available range for the input, $-V_C < V_{in} < V_C$" (Wang, 1990b).

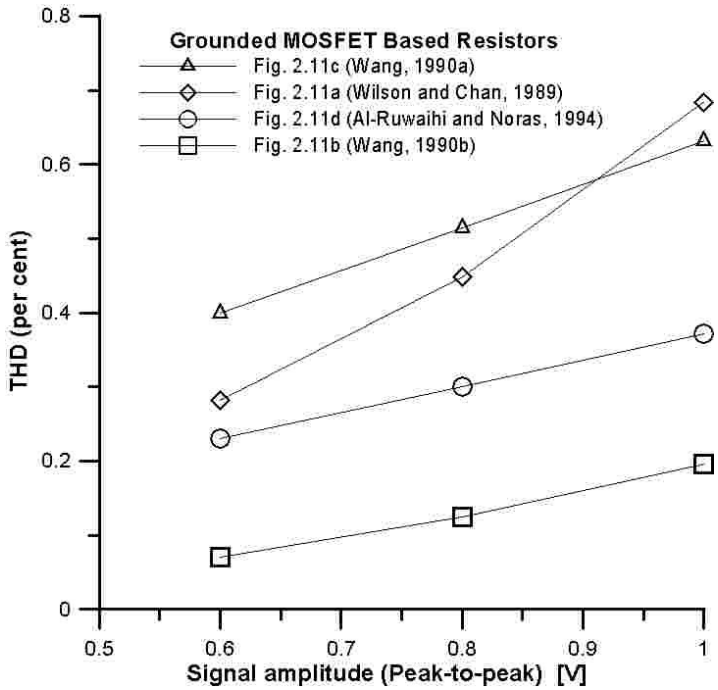


Figure 2.12. THD values of the MOS resistors for various input signal amplitudes at 1kHz

2.3.1. New Tunable All-Pass Filters and Compensation of the Current Conveyor Non-idealities

In this section, the effects of the parasitic resistances and non-ideal gains of the active elements on MOSFET-C filters are examined with two new all-pass filters examples. Parasitic terminal resistances of the current conveyor may limit the maximum and minimum values of the MOSFET based resistors. For example, the Z terminal resistance of the current conveyor limits the maximum value of the parallel connected

MOSFET based resistor. On the other hand, the series parasitic resistance R_X of the X terminal of the current conveyor should be taken into account for the minimum value of the MOSFET based resistor that is series with the X terminal. These unwanted effects are especially critical for the circuits including element-matching conditions as in the example circuits of this section shown in Fig. 2.13.

The proposed two novel all-pass filters with grounded components include one capacitor instead of two as reported recently (Horng, 2005; Horng *et al.*, 2006a; Horng *et al.*, 2006b). The circuits use two dual output current conveyors (DO-CCII). Also, the presented circuits have both low input and high output impedances providing rich cascadability options compared to (Horng, 2005; Horng *et al.*, 2006a; Horng *et al.*, 2006b). This feature is very important for current-mode all-pass filters since they are used as an intermediate stage in the signal-processing path for compensating phase shifts. Thus, additional current conveyors are not needed for cascading. Simulations are performed to verify the theoretical results.

2.3.1.1. The Proposed Tunable First-order All-pass Filters. As mentioned in Chapter 1, the CCII is one of the most popular and versatile active elements in the last three decades. Adding a second Z terminal to the CCII can widen its application area. Considering non-idealities arising from the physical implementation, terminal relationship of dual output CCII can be given as,

$$V_X = \beta V_Y \qquad I_Y = 0 \qquad I_{Z+} = +\alpha_{11} I_X \qquad I_{Z-} = -\alpha_{12} I_X \tag{2.22}$$

where β, α_{11}, α_{12} are respectively voltage and current gains and they are equal to unity for an ideal dual output CCII. The current convention is such that all current directions are into the device.

The proposed first-order all-pass filters are shown in Fig. 2.13(a) and 2.13(b). Their ideal current transfer functions can be respectively expressed as follows,

$$\frac{I_o}{I_i} = K\frac{R_1 - R_2 - sCR_1R_2}{R_2 + sCR_1R_2} \tag{2.23}$$

and using element matching conditions for the case $R=R_1=2R_2$,

$$\frac{I_o}{I_i} = K\frac{1-sCR}{1+sCR} \tag{2.24}$$

where K is equal to 1 for the circuit in Fig. 2.13(a) and K is equal to –1 for the circuit in Fig. 2.13(b).

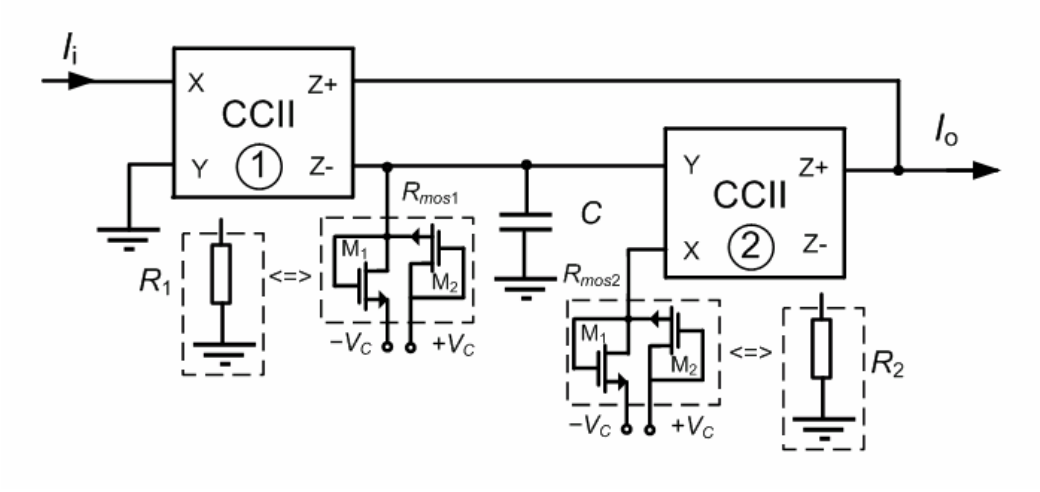
In Fig. 2.13(b), the parasitic Z+ terminal resistance R_{Z1} of the CCII-1 and the parasitic X terminal resistance R_{X2} of the CCII-2 affect respectively maximum value of the R_1 and minimum value of the R_2. Also they disturb the resistor matching conditions. The parasitic capacitance at the Z+ terminal of the CCII-1 C_{Z1} can be ignored since it is parallel to the C and is usually much smaller. Considering R_{Z1}, R_{X2} and the non-ideal gains in (2.22), the modified transfer function of the proposed filter in Fig. 2.13(b) can be given as follows for the case $R=R_1=(1/m)R_2$,

$$\frac{I_o}{I_i} = \frac{R_{X2}R_{Z1}\alpha_{12} + mR_1^2(1+sCR_{Z1})\alpha_{12} + R_1((R_{X2} + (m+sCR_{X2})R_{Z1})\alpha_{12} - R_{Z1}\beta_2\alpha_2\alpha_{11})}{(R_{X2} + mR_1)(R_{Z1} + R_1(1+sCR_{Z1}))} \tag{2.25}$$

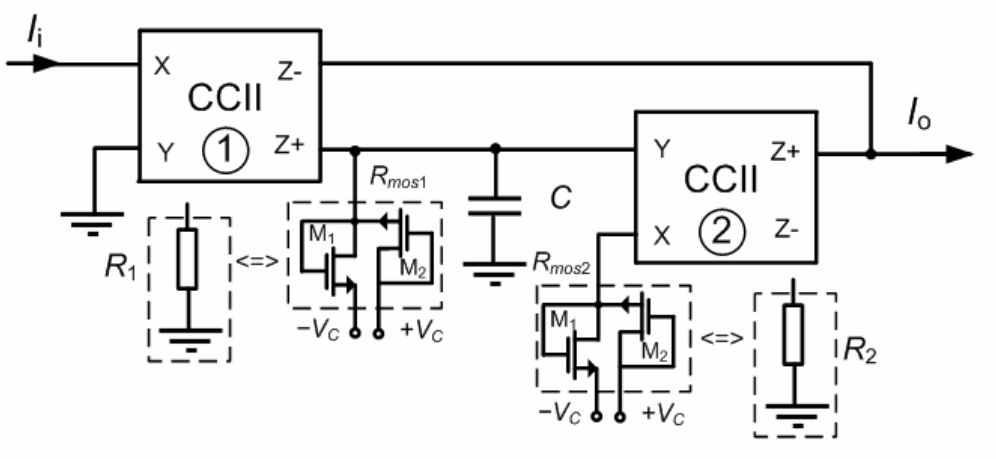
here, α_{11} and α_2 are the current gains of the Z+ terminal of the CCII-1 and CCII-2 respectively. Moreover α_{12} is the current gain of the Z– terminal of the CCII-1 and β_2 is the voltage gain of the CCII-2.

A resistor matching ratio m can be found that achieves all-pass response is given below,

$$m = \frac{\beta_2\alpha_2\alpha_{11}}{2\alpha_{12}}\frac{R_{Z1}}{R_{Z1} + R_1} - \frac{R_{X2}}{R_1} \tag{2.26}$$



(a)



(b)

Figure 2.13. The proposed all-pass filters with grounded resistors suitable for MOSFET based resistor replacement (a) All-pass filter with positive gain (b) All-pass filter with negative gain

Thanks to the electronic tunability, this matching ratio can be easily realized. Therefore, the effects of the non-ideal gains and parasitics of the current conveyor can be fully compensated.

In (2.25), only R_{Z1} and R_{X2} affecting MOSFET based resistors are taken into account. For simplification ignoring R_{X2} and parasitics at Z+ of the CCII-1 and assuming all other parasitic resistances at Z terminals are equal to each other as R_Z, and all parasitic capacitances at Z terminals are also equal to each other as C_Z, and connecting a load

resistor to the output as R_L, the following equation is obtained for the circuit in Fig. 2.13(b):

$$\frac{I_o}{I_i} = -\frac{R_Z(-1+sCR)}{(1+sCR)(R_Z+2R_L(1+sC_ZR_Z))} \tag{2.27}$$

Equation (2.27) shows that the parasitic resistances of the output terminal cause a small decrease in the magnitude of the gain at the low frequencies, which is equal to $R_Z/(R_Z+2R_L)$ at ω=0.

The limited bandwidth of the current and voltage gain of the current conveyor may affect and modify the transfer functions of the circuit. We assume that the current gains and the voltage gain have only a single corner frequency, which are denoted as ω_α and ω_β, respectively. This one-pole model can give only a rough idea about non-ideal frequency response, since the active components have other poles at higher frequencies that may affect the circuit behavior. The current gain and voltage gains are modeled using single-pole model as,

$$\beta(s) = \frac{\beta_0}{1+\frac{s}{\omega_\beta}} \qquad \alpha_{11}(s) = \frac{\alpha_{110}}{1+\frac{s}{\omega_{\alpha 11}}} \qquad \alpha_{12}(s) = -\frac{\alpha_{120}}{1+\frac{s}{\omega_{\alpha 12}}} \tag{2.28}$$

where β_0, α_{110}, and α_{120} are voltage and current gains at low frequencies. Frequency dependent non-ideal transfer functions can be calculated using (2.28) for the circuit in Fig. 2.13(b) for the case R=R_1=2R_2 as follows,

$$\frac{I_o}{I_i} = \frac{-2\alpha_{20}\alpha_{110}\beta_{20}\omega_{\alpha 11}\omega_{\alpha 2}\omega_{\beta 2}(s+\omega_{\alpha 12})+\omega_{\alpha 12}\alpha_{120}(1+sCR)(s+\omega_{\alpha 11})(s+\omega_{\alpha 2})(s+\omega_{\beta 2})}{(1+sCR)(s+\omega_{\alpha 11})(s+\omega_{\alpha 12})(s+\omega_{\alpha 2})(s+\omega_{\beta 2})} \tag{2.29}$$

here the β_{20} is the voltage gain of the CCII-2. The α_{110} and α_{120} are current gains of CCII-1 at low frequencies. The α_{20} is current gain of CCII-2 at low frequencies. The $\omega_{\beta 2}$ and $\omega_{\alpha 2}$

are the parasitic pole frequency of the voltage and current gains of CCII-2 respectively. The $\omega_{\alpha 11}$ and $\omega_{\alpha 12}$ are the parasitic pole frequency of the current gains of CCII-1.

Equation (2.29) shows that four parasitic poles at angular frequency of $\omega_{\beta 2}$, $\omega_{\alpha 11}$, $\omega_{\alpha 12}$, $\omega_{\alpha 2}$ appear due to one-pole model. If the frequencies of these additional poles are sufficiently higher than the pole frequency of the presented all-pass filter such as $\min\{\omega_{\beta 2}, \omega_{\alpha 11}, \omega_{\alpha 12}, \omega_{\alpha 2}\} >> 1/RC$ the effect of them can be ignored.

2.3.1.2. Simulation and Experimental Results. To verify the theoretical analyses, we simulated the circuit proposed in Fig. 2.13(b) using the SPICE circuit simulation program. The presented circuit is simulated employing the internal structure in Fig. 2.14 (Altuntas and Toker, 2002). Transistor sizes are tabulated in Table 2.2. The supply voltages are V_{DD} = 2.5V and V_{SS} = –2.5V. The circuit is biased by I_0=0.3mA. For the simulations, 0.35μm level 49 process parameters from TSMC are used as given by Table 2.1.

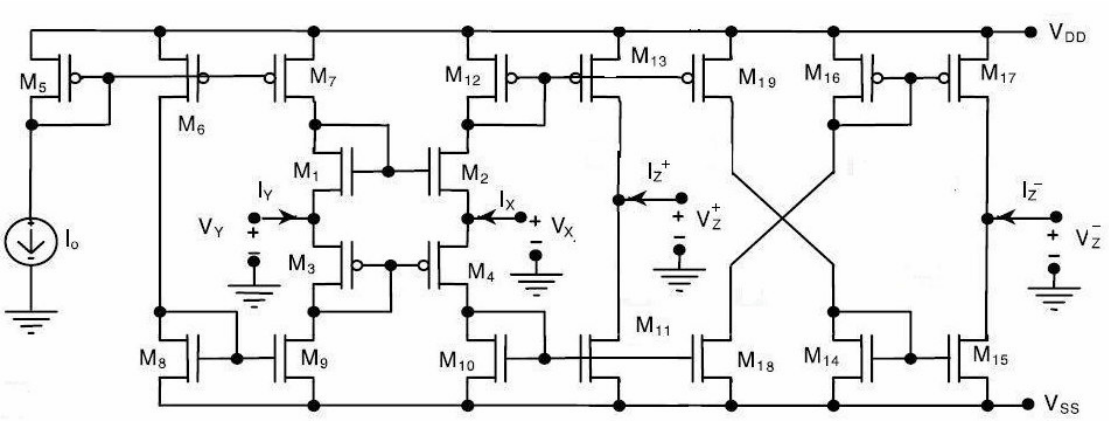


Figure 2.14. A CMOS dual output controlled conveyor implementation

The capacitor value of C=50pF is employed in the simulations. The SPICE simulation results of the gain and phase responses are depicted in Fig. 2.15. When R_1 and R_2 replaced by electronic resistors, the electronic tunability is obtained. The aspect ratio of the MOSFET resistor R_1 is W=2.1μm and L=4.2μm. Two parallel MOSFET resistors are used for R_2. The electronic resistors are biased as R_1=2kΩ and R_2=1kΩ to obtain the pole frequency of 1.59MHz with V_C=5V in uncompensated case. In compensated case, considering parasitics, R_{mos1} is biased by V_C=3V to obtain a matching value as given by (2.26) for compensation. Figure 2.16 shows the tunability of the presented circuit. The pole

frequency of the proposed filter is varied between f_0≅68kHz and f_0≅235kHz for V_C =1.0V, V_C =2.0V and V_C =5V respectively.

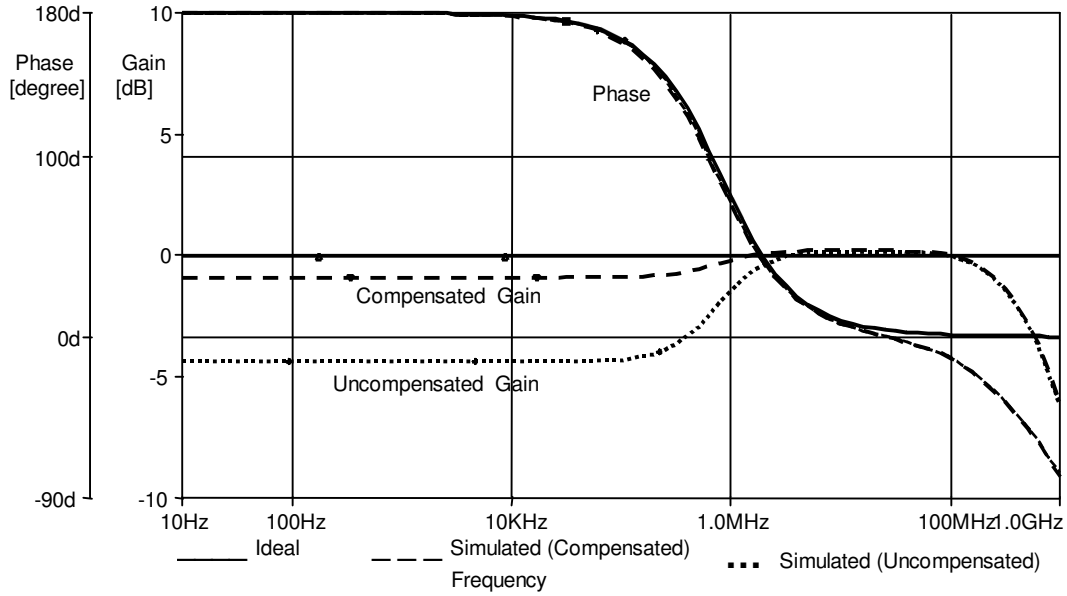


Figure 2.15. The theoretical and simulated phase and gain responses

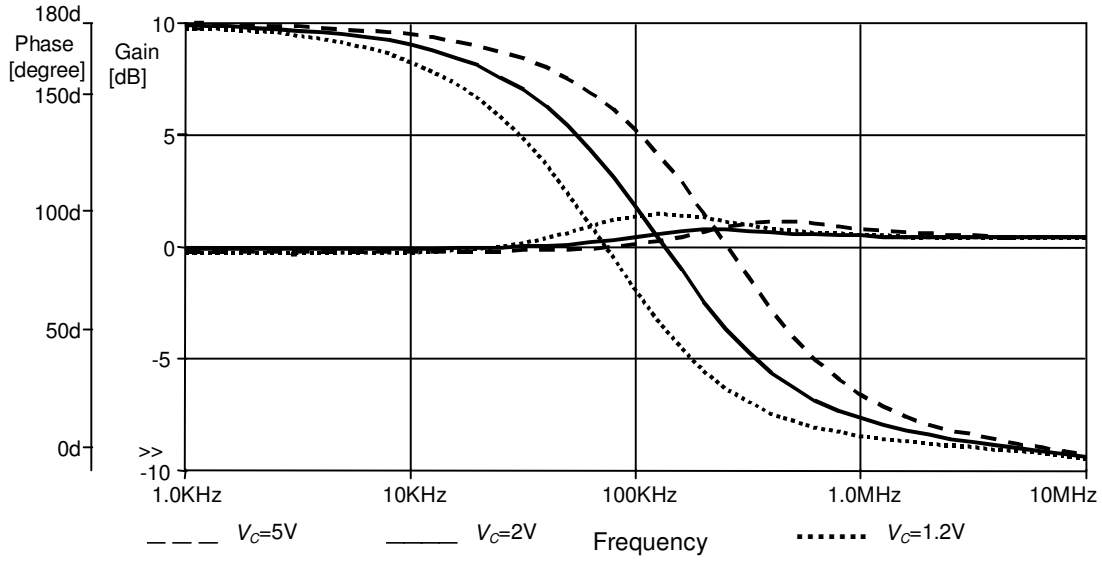


Figure 2.16. Simulated gain and phase responses of the proposed circuit (The pole frequency can be tuned between 68kHz and 235kHz)

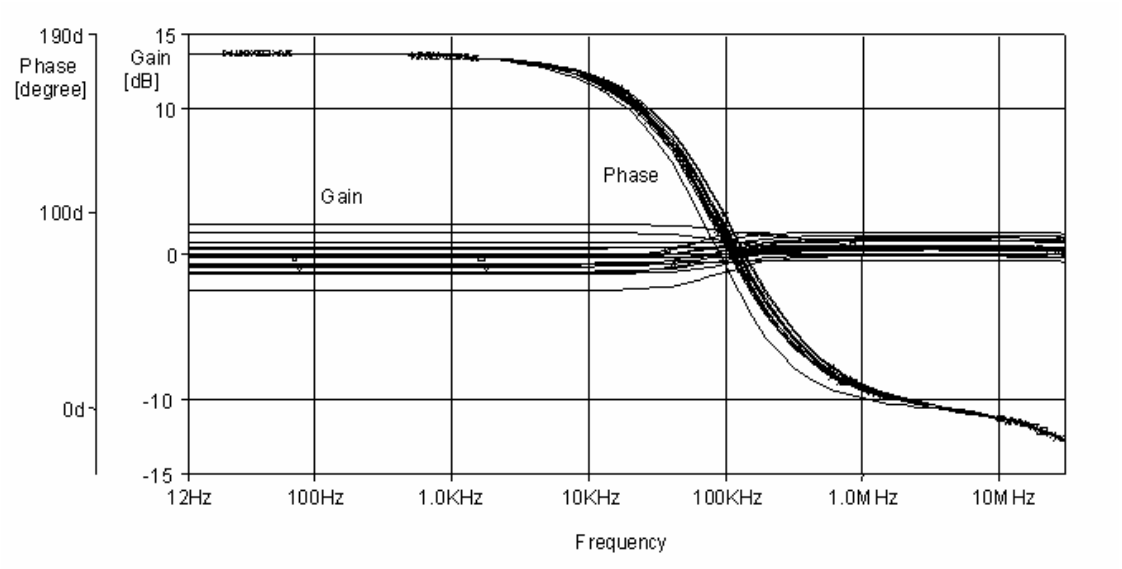
Table 2.2. The dimensions of the transistors used in the current conveyor implementation in Fig. 2.14

TRANSISTOR	W[μm]	L[μm]
M1, M2	19.95	0.35
M3, M4	60.2	0.35
M5, M6, M7	30.1	2
M8, M9	9.8	2
M10, M11, M14, M15, M18	9.8	1.05
M12, M13, M16, M17, M19	30.1	1.05

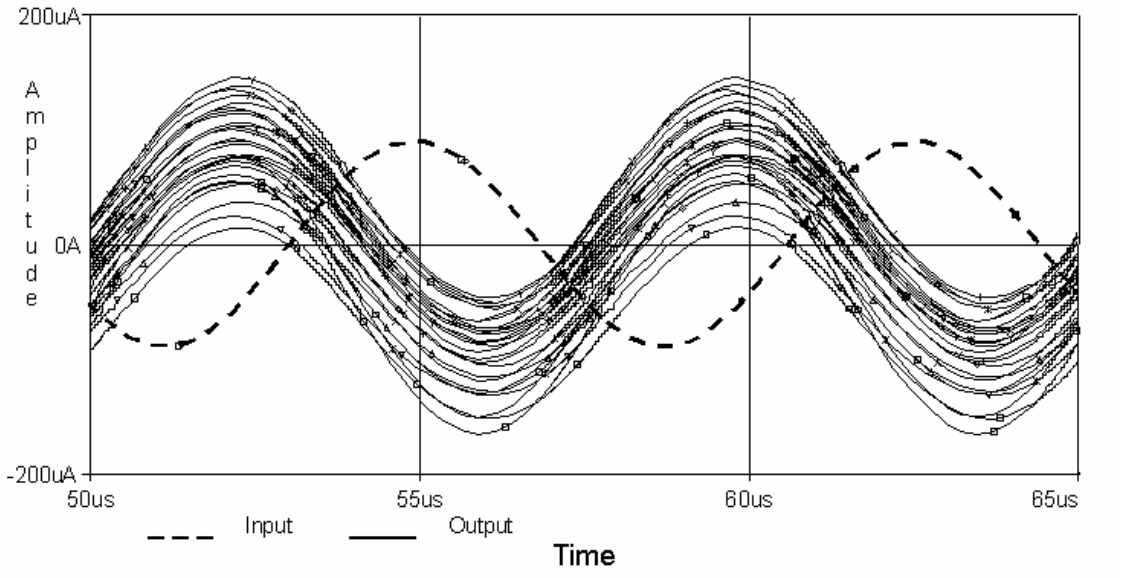
It is very important to perform Monte-Carlo simulations to examine the effects of deviations in transistor sizes on the performance of the integrated circuits. In the Monte-Carlo analysis, tolerances of the MOSFETs changed in a high range on the order of 5 per cent, but the mismatch ranges of the matched IC transistors can be made on the order of one per cent practically. Simulation result of Monte-Carlo analysis in frequency domain and time domain is given in Fig. 2.17(a) and 2.17(b) respectively. They show that the proposed filter works in acceptable ranges against transistor mismatches.

In addition to the simulations, the theoretical predictions presented in this work are verified by experiments. The proposed circuit in Fig. 2.13(a) is designed with the passive element values R_1=200kΩ, R_2=100kΩ, C=100pF to obtain a first-order all-pass filter with a pole frequency of $f_0 \cong$7.95kHz. Realization with the commercially available CFOA AD844s is shown in Fig. 2.18(a). The power supply voltages are +12V and –12V. Theoretical results and measurement data of the phase and gain responses are depicted in Fig. 2.18(b). The photograph of the experiment at the pole frequency is given in Fig. 2.19. In the experiment, a sinusoidal signal with a peak value of 30μA is used as an input signal. At the output a 10kΩ resistor is used as a load and its voltage is measured. The discrepancies may be due to the tolerances of the passive elements, non-idealities of the AD844s and the stray capacitances of the breadboard implementation.

Simulation and experimental results agree quite well with the theoretical analysis. Note that the deviations in gain and phase characteristics at high frequencies are also affected from the poles of voltage and current gains as well as from the terminal parasitics of the active elements, which is examined in the previous section.

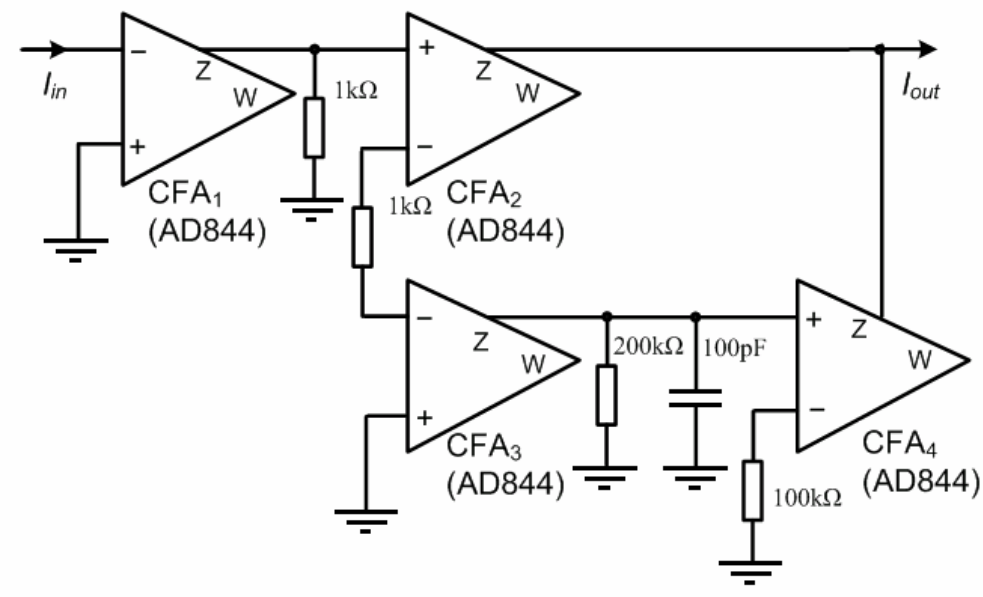


(a)

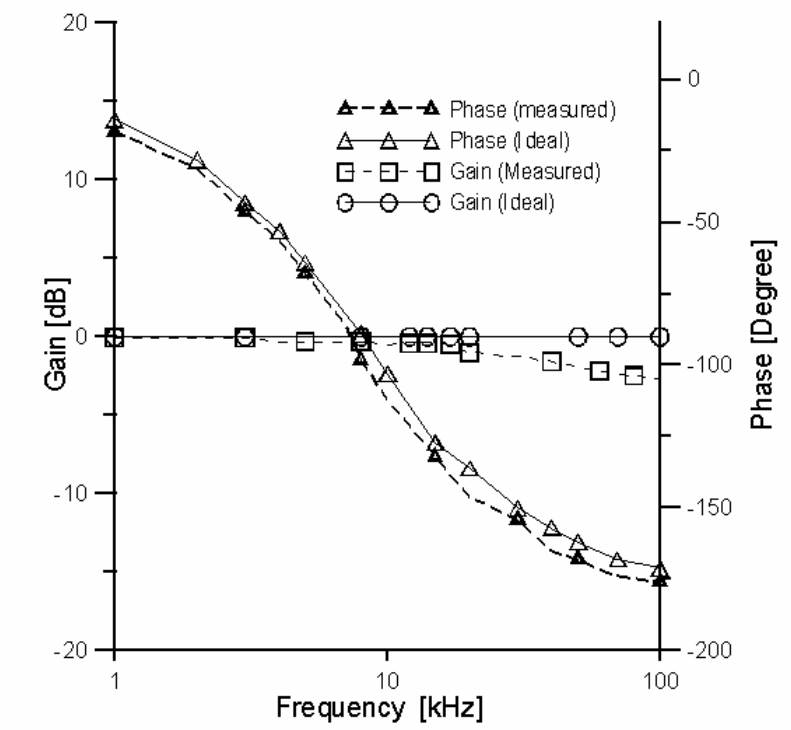


(b)

Figure 2.17. (a) Monte-Carlo analysis for the phase and gain response for V_C=1V and 5 per cent uniform change in the transistor sizes (b) Monte Carlo analysis in time domain 5 per cent uniform change in the transistor sizes



(a)



(b)

Figure 2.18. (a) Realization of the presented circuit in Fig. 2.13(a) with commercially available CFOA AD844s (b) The calculated and experimental all-pass gain and phase responses ($f_0 \cong 7.95$kHz)

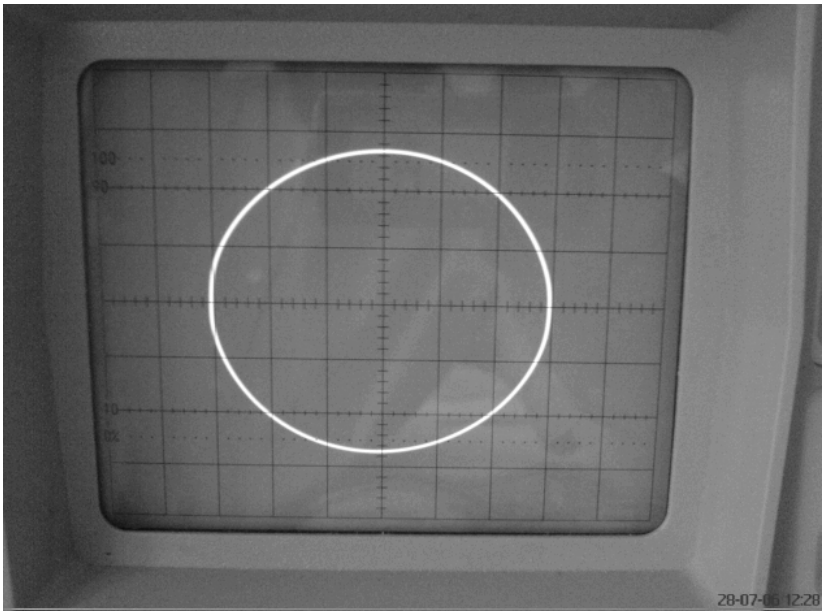


Figure 2.19. The photograph of the experimental result for Lissajou ellipse at the pole frequency (Vertical scale and horizontal scales correspond to 10μA/division)

2.3.2. Electronically Tunable All-pass Filters with DDCC for High Frequency of Operation and Easy IC Realization

In this section we presented two novel all-pass filter circuits using DDCC, a capacitor and a resistor without element-matching restriction. The matching conditions usually depend on the current and/or voltage gain of the current conveyors. Since during IC implementation large deviations in gain parameters occur, it is very difficult to be sure about the matching conditions after manufacturing. Also, different from previous subsection, the maximum values of the electronic resistors in the presented circuits are not limited by the parallel connected parasitic Z-terminal resistance of the active element.

The first presented circuit is very suitable for high frequency applications, because there is a feed forward capacitor in the circuit. The second proposed circuit is suitable for integrated circuit implementation, since it employs a grounded resistor and a grounded capacitor. Moreover it has high input impedance for easy cascadability. Furthermore, both circuits can be made electronically tunable due to the grounded resistors that can be realized with voltage controlled linearized MOS transistors. The theoretical results are verified with SPICE simulations.

2.3.2.1. The Differential Difference Current Conveyor and the Description of the Circuits.
The DDCC (Chiu *et al*., 1996) used in this study is a five-port building block and the electrical symbol of the DDCC is shown in Fig. 2.20. Considering the non-idealities arising from the physical implementation of the DDCC, its terminal relationship can be characterized with the following equations:

$$I_{Y1}=0 \quad I_{Y2}=0 \quad I_{Y3}=0 \quad I_Z=\alpha I_X \quad V_X=\beta_1 V_{Y1}-\beta_2 V_{Y2}+\beta_3 V_{Y3} \tag{2.30}$$

where ideally $\beta_1=\beta_2=\beta_3=1$ and $\alpha=\pm 1$ that represent the voltage and current transfer ratios of the DDCC respectively. There are two types of DDCCs depending on the sign of α, namely positive type (DDCC+) or negative type (DDCC–).

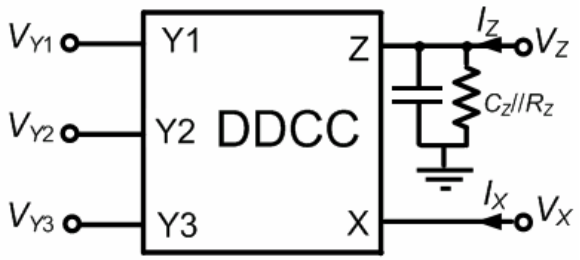
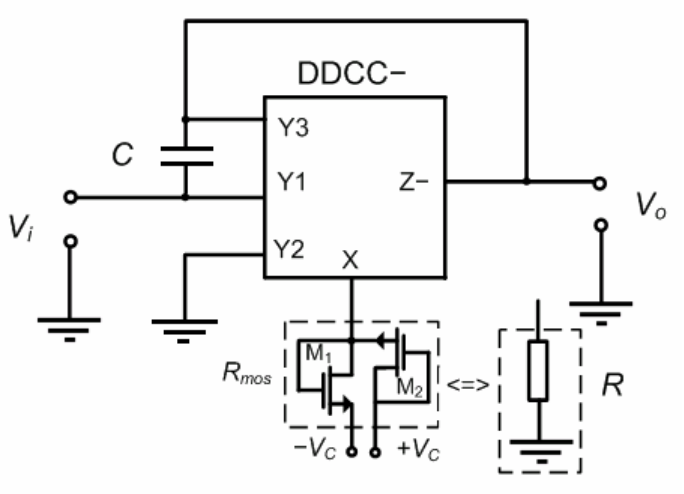


Figure 2.20. Circuit symbol of the DDCC including parasitics (For an ideal DDCC parasitics R_Z and C_Z are omitted)

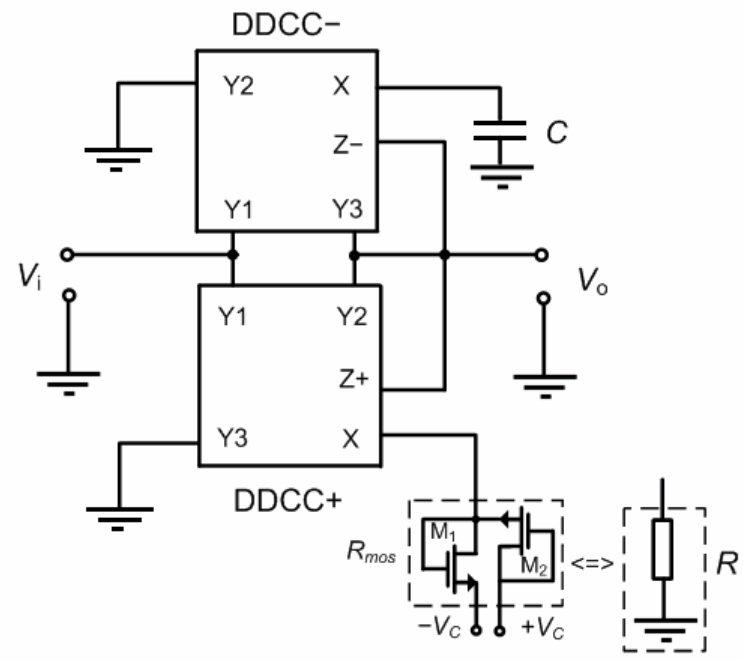
The proposed circuits are shown in Fig. 2.21 and their transfer functions are given for the ideal case ($\beta_1=\beta_2=\beta_3=1$ and $\alpha=1$)

$$\frac{V_o}{V_i}=K\frac{1-sCR}{1+sCR} \tag{2.31}$$

where the $K=-1$ for Fig. 2.21(a) and $K=+1$ for Fig. 2.21(b). Considering the active element non-idealities as given in (2.30), the transfer function in (2.31) can be given for the circuits in Fig. 2.21(a) and Fig. 2.21(b) respectively as follows,



(a)



(b)

Figure 2.21. The proposed all-pass filters suitable for MOSFET based electronic resistors (a) The tunable all-pass filter for high-frequency operation (b) The tunable and cascadable all-pass filter for IC implementation

$$\frac{V_o}{V_i} = -\frac{\alpha\beta_1 - sCR}{\alpha\beta_3 + sCR} \tag{2.32a}$$

$$\frac{V_o}{V_i} = \frac{\alpha_2\beta_{21} - sCR\alpha_1\beta_{11}}{\alpha_2\beta_{22} + sCR\alpha_1\beta_{13}} \tag{2.32b}$$

In (2.32b), α_1 and α_2 represent current gains of the DDCC– and DDCC+ respectively in Fig. 2.21(b). The β_{11} and β_{13} are the voltage gains at the Y1 and Y3 terminals of the DDCC–; β_{21} and β_{22} are the voltage gains at the Y1 and Y2 terminals of the DDCC+ in Fig. 2.21(b). Equations (2.32a) and (2.32b) show another opportunity for electronic tunability. The current gains α in (2.32a) and α_1, α_2 in (2.32b) can be used for tuning the pole frequencies of the filters. This topic will be examined later in Chapter 5.

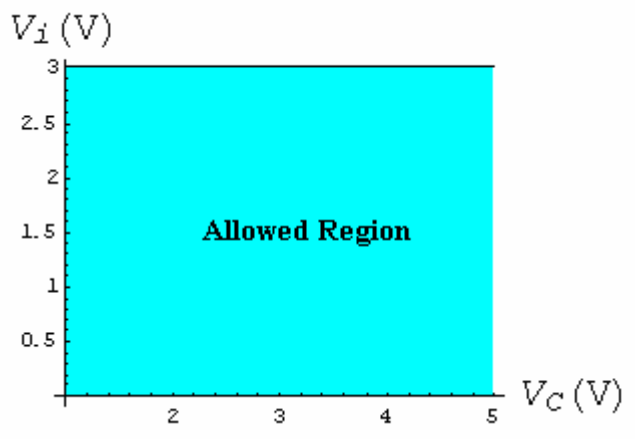
2.3.2.2. Limitations of the Input Signal and the Control Voltage. As stated in the beginning of this Section 2.3, both MOS transistors of the electronic resistor in Fig. 2.11(b) should remain in the saturation region, which is true if $|V_{in}|<(V_C - V_{Th})$, where $|V_{in}|$ is the magnitude of the voltage on the resistor. Also, Wang (1990) notes that "The magnitude of V_{in} is allowed to vary within the free range of supply voltages without significant percentage changes in linearity, thus reaching the maximum available range for the input, $-V_C < V_{in} < V_C$".

The magnitude of the voltage on the electronic resistor in Fig. 2.21(a) is equal to $|V_{in}(j\omega)| = V_i(2C^2R_{mos}^2\omega^2 / (1+C^2R_{mos}^2\omega^2))$, where V_i is the filter input signal amplitude. Here, considering the resistor value of the R_{mos} given in (2.21) and the magnitude of the voltage on the R_{mos}, the following condition can be found between the filter input signal amplitude V_i and the control voltage V_C for the all-pass filter in Fig. 2.21(a),

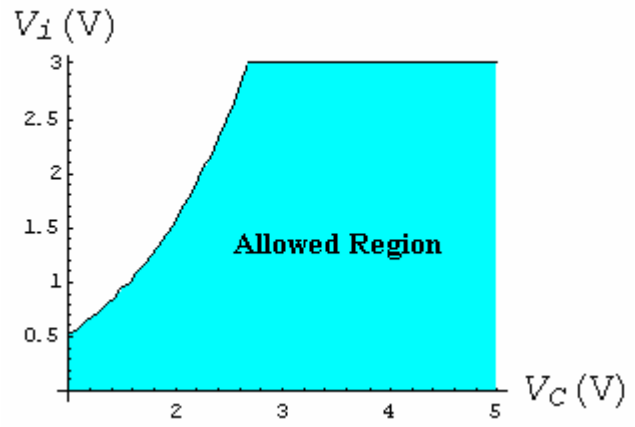
$$V_i < V_C \frac{4\mu_n^2 C_{OX}^2 (W/L)^2 (V_C - V_{Th})^2 + C^2\omega^2}{2C^2\omega^2} \tag{2.33}$$

where, $\omega = 2\pi f_o$ is the operating frequency of the filter. For various V_i and V_C values, the graphical representation of (2.33) is given in Fig. 2.22 for V_{Th}=0.55V, $\mu_n C_{OX}$ = 0.05mA/V^2, (W/L)=1/4 and C=100pF.

Figure 2.22 shows that there is an input signal limitation at high frequencies for the circuit in Fig. 2.21(a), which is suitable for high frequency of operation due to its feed-forward capacitor. For example, Figure 2.22(b) shows that for an input 0.75V (peak value) V_C should be greater than 1.3V for the linear operation of the MOSFET based resistor.



(a)



(b)

Figure 2.22. The relation between input signal limitation and control voltage (a) f_o=100kHz (b) f_o=3MHz

2.3.2.3. Simulation Results and Discussions. To verify the theoretical analyses, we simulated the proposed circuits using DDCC implementation shown in Fig. 2.23, using the SPICE circuit simulation program. For the simulations, 0.35μm TSMC level 49 process parameters in Table 2.1 are used. The supply voltages are V_{DD}=1.5V and V_{SS}= –1.5V. The biasing voltage is chosen

as V_{BB}= –1.0V. (Ibrahim, 2004) The aspect ratios of the transistors are given in Table 2.3.

The proposed circuit in Fig. 2.21(a) is designed with the passive element values R_{mos}=100kΩ (W=1µm, L=40µm and V_C=2V), C=5pF to obtain a first-order all-pass filter with a pole frequency of f_0≈318.5kHz. Figure 2.24 shows the tunability of the circuit in Fig. 2.21(a). The pole frequency of the proposed filter varied between f_0≅198.5kHz (for V_C=1.2V) and f_0≅477kHz (for V_C=5V). AC response at high frequencies is close to ideal response due to the feed-forward capacitor in Fig. 2.21(a). In Fig. 2.25, theoretical and simulation results of AC analysis are shown for the circuit in Fig. 2.21(b). The passive element values are chosen as R_{mos}=50kΩ (W=2µm, L=40µm and V_C=2V) and C=10pF for a pole frequency of f_0≈318.5kHz.

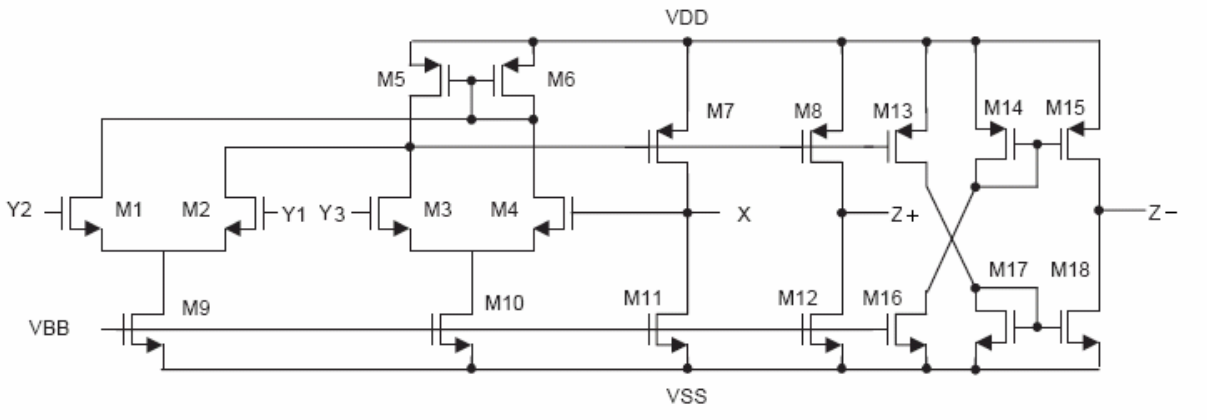


Figure 2.23. A CMOS realization of the DDCC

Table 2.3. Transistor aspect ratios of the DDCC implementation given in Fig. 2.23

TRANSISTORS	W (µm)	L (µm)
M1-M4	1.2	0.7
M5-M6	20.45	0.7
M7-M8-M13-M14-M15	21	0.7
M9-M10	14.4	0.5
M11-M12-M16-M17-M18	87	0.7

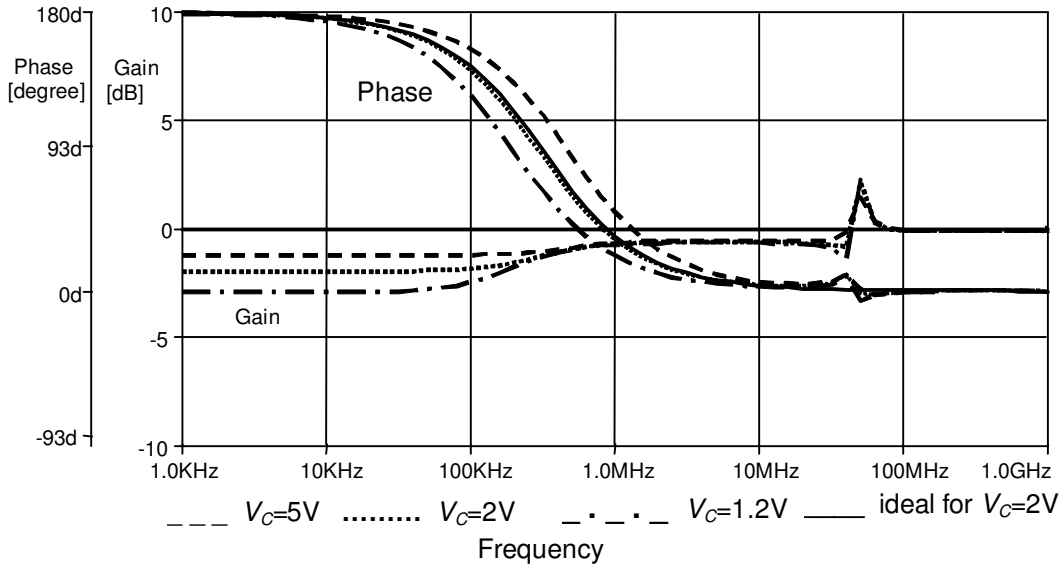


Figure 2.24. Illustrating the tunability of the presented circuit in Fig. 2.21(a) by changing the pole frequency between 111kHz and 317kHz with the electronic resistor

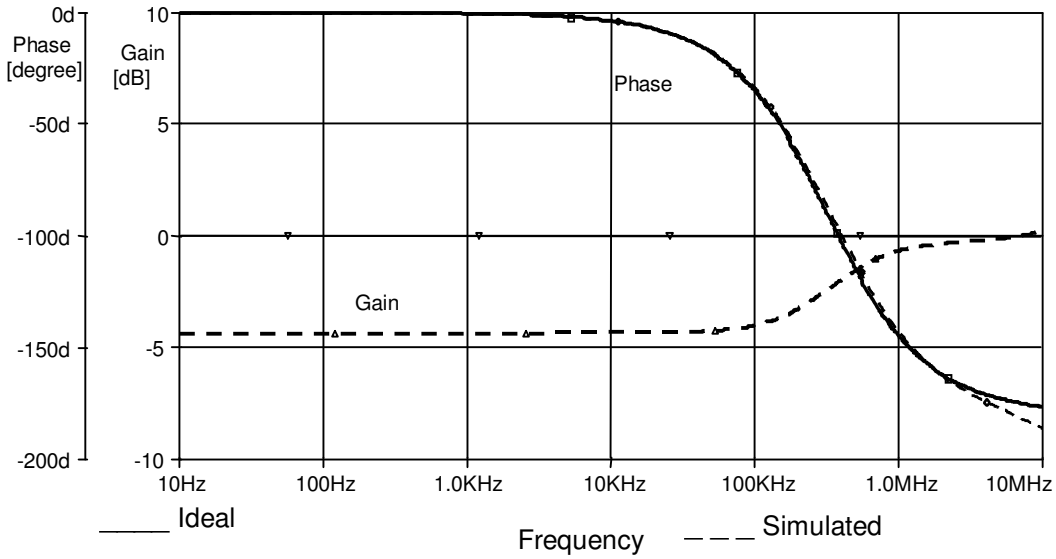


Figure 2.25. The ideal and simulated phase and gain responses of the presented circuit in Fig. 2.21(b) for R_{mos}=50kΩ and C=10pF

In Fig.s 2.24 and 2.25, the magnitude of the voltage gains at ω=0 are less than unity. The reason for this deviation is the parasitics at the Z terminal of the DDCC. Considering parasitic resistance R_Z and the parasitic capacitance C_Z at the Z terminal that are shown in Fig. 2.20, the following transfer functions are obtained respectively.

$$\frac{V_o}{V_i} = -\frac{R_Z(\alpha\beta_1 - sCR\ )}{R + \alpha\beta_3 R_Z + sR(C + C_Z)R_Z} \tag{2.34a}$$

$$\frac{V_o}{V_i} = \frac{R_Z(\alpha_2\beta_{21} - sCR\alpha_1\beta_{11})}{2R + R_Z\alpha_2\beta_{22} + sR(C\alpha_1\beta_{13} + C_Z)R_Z} \tag{2.34b}$$

Equations (2.34a) and (2.34b) show that the voltage gains at ω=0 are approximately equal to $R_Z/(R+R_Z)$ and $R_Z/(2R+R_Z)$ respectively resulting slightly reduced gain and this can be observed in Fig.s 2.24 and 2.25. The parasitic resistance R_Z can be easily increased employing cascoded-output stage for the Z terminal to avoid reduced voltage gain. Furthermore, (2.34) shows that the inclusion of parasitic capacitances at the Z terminal C_Z, and the finite output resistance of the Z terminal R_Z, does not result an increase in the order of the transfer function.

A sinusoidal input with frequency value of f=132kHz and peak-to-peak value of V_{pp}=1V was applied to the filters constructed with above mentioned passive element values. There is a 40mV DC shift at all the outputs. Total harmonic distortion was found less than 1 per cent, and given detailed in Fig. 2.26 for both passive and electronic resistors comparatively.

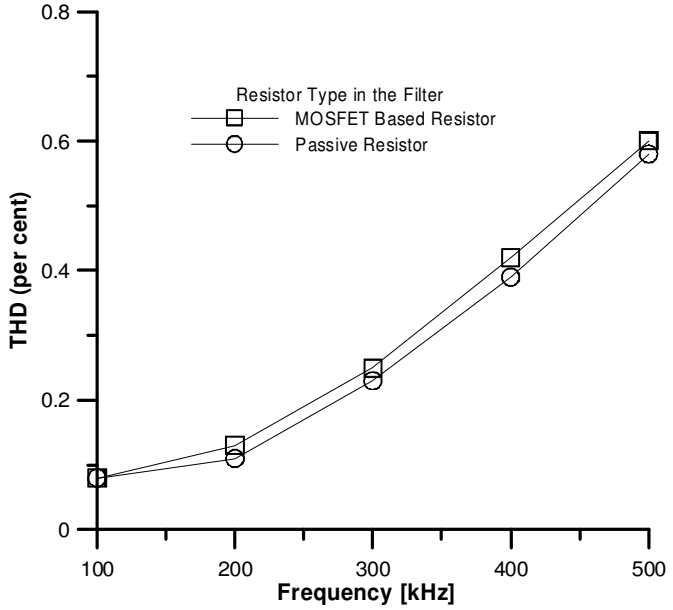


Figure 2.26. The THD comparison of the passive resistor and electronic resistor in the proposed all-pass filter in 2.21(a) using peak-to-peak 1V sinusoidal input

Consequently, the simulation results show that the proposed all-pass circuits work well. In the circuits, the effect of the parasitics of the DDCC at the Z terminal should be taken into consideration. The cascode output stages in the DDCC can be used to increase the R_Z to avoid reduced voltage gain problem.

2.4. Summary

In Section 2.2, we implement Acar-Ghausi MRC with only three transistors adapting MOSFET-C filters to low-voltage/low-power design trend. Non-idealities of this new MRC circuit examined and some solutions are proposed. Exploiting the advantage of a MOSFET based resistor is possible with high resistor values. However, parasitic resistances of the active elements restrict the maximum value of the MOSFET based resistors in parallel. Hence, in Section 2.3.1, this situation is shown with filter examples. Later in Section 2.3.2, some other filter examples are given not limited by this problem.

The MOSFET-C filters have a restriction with respect to tunability range. MOSFET based resistors are tuned by voltage. The trend of low-voltage IC design not only reduces power supply voltages but also limits the range of control voltages. Also, as examined in this chapter, operation conditions of the MOSFETs and relation of these conditions with input signal amplitude are expected to keep the control voltages in a narrow range.

On the other hand, the current and voltage relations of the MOSFETs given in this chapter are valid only for transistor sizes greater than approximately 2μm due to some undesired effects such as channel length modulation and mobility reduction. These prevent the length of the MOSFET-based resistors being reduced. It is possible to mention about a scalability problem adapting MOSFET-C filters to the submicron IC technologies. Conversely, the active elements such as controlled conveyor and OTA that can be successfully scaled for new submicron technologies have been widely used in the design of electronically tunable circuits for the last decade.

Therefore, in the next two chapters, electronic tunability with controlled conveyor and OTA will be examined respectively for their larger tunability range.

3. ELECTRONIC TUNABILITY WITH MIXED TRANSLINEAR LOOP

In this chapter of the thesis, we will focus on electronically tunable circuits using mixed translinear loops such as controlled current-conveyors (Fabre *et al.*, 1995a). Controlled current conveyors allow current conveyor applications to be extended to the domain of electronically programmable functions. A controlled conveyor provides electronic tunability of the parasitic resistance at port X with its bias current. Moreover, all the CCII-based circuits employing one external resistance connected to the port X can be replaced by controlled conveyor based circuits by exploiting the parasitic resistance at port X. Provided that all-passive resistors in a circuit are replaced by these parasitic resistors, this type of circuits are called as translinear-C circuits.

The advantages of the using controlled current conveyors can be listed as follows;

(i) The matching conditions usually depend on the current and/or voltage gain of the current conveyors. During IC implementation large deviations in gain parameters may occur, so it is very difficult to be sure about the actual matching conditions after manufacturing. However, it is possible to compensate for the effect of non-ideal voltage and current gains with proper matching condition due to the parasitic X terminal resistance of the controlled conveyor.
(ii) The parasitic X terminal resistance of the controlled conveyor can directly tune various parameters of the filter circuit, such as center frequency and quality factor.
(iii) In the circuit using minimum number of resistors, the resistors are replaced by parasitic X resistance of controlled current conveyors under a suitable connection. In this way, an electronically tunable circuit is obtained.

In Section 3.1, the principle of controlled conveyor is given. In Section 3.2, one of the benefits of the controlled current conveyors is examined: Tuning the element matching conditions to compensate for deviations because of the non-ideal gains of the current conveyor. Opportunities of using different types of current-conveyors in the design of electronically tunable circuits have not been appreciated enough, since the second

generation current-conveyor is the most commonly used component in the related research area. The possibilities of these less commonly used active elements are also examined in the scope of this thesis. For example, in Section 3.3, we show that first generation current conveyor is able to provide high input impedance for cascadability where second generation cannot. In Section 3.4, the relation of cascadability and enhanced dynamic range is illustrated with a tunable notch/all-pass filter example, comparing it with other notch filters from the literature. In Section 3.5, an opportunity of first generation current conveyor compared to second generation is shown for reduced power consumption possibility with a tunable FDNR example. In Section 3.6, a relatively new active element using mixed translinear loops is illustrated: The controlled CDBA. A CMOS implementation of the controlled CDBA is given and the benefit of this element is shown with a novel tunable all-pass filter example.

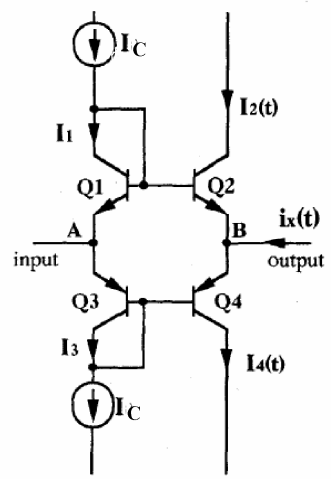


Figure 3.1. Schematic form of the translinear loop from (Fabre *et al.*, 1996)

3.1. Current Controlled Resistors Using Mixed Translinear Loops

The input cell is implemented from a mixed translinear loop composed of complementary bipolar transistors, so the conveyor is characterized by an excellent frequency response for voltage transfer from the port Y to the port X. By this configuration less number of active and passive elements and less silicon area is required. However there is an undesired parasitic resistance at the X port. This parasitic resistance leads to conversion errors when a load resistance is connected at the port X or to incorrect transfer

functions when this load is a capacitor (Fabre *et al.*, 1995b). It is possible to take advantage of this parasitic resistance because its value depends on biasing current of the conveyor.

3.1.1. Theoretical Approach

The mixed translinear loop, shown in Fig. 3.1 contains two PNP and two NPN transistors. It is characterized by the translinear relationship between collector currents of these transistors (Fabre *et al*., 1996).

$$I_1 I_3 = I_2 I_4 \tag{3.1}$$

This circuit is biased by two identical currents ($I_1 = I_3 \approx I_C$, by assuming current gains β_F of the transistors much greater than unity). Thus, it represents a high impedance input port (point A) and a low impedance output port (point B). This circuit is a voltage follower. The voltage difference between the points A and B depends on the value of the current $i_x(t)$; its expression is given by

$$V_{BA}(t) = -V_T \log \frac{I_2(t)}{I_C} \tag{3.2}$$

where $V_T \approx 26$ mV at 27 °C is the thermal voltage. The relationship allows, in the particular case of the loop shown in Fig. 3.1 (i.e., for $I_1 = I_3 \approx I_C$), to calculate the expressions for the currents $I_2(t)$ and $I_4(t)$ (Fabre *et al*., 1996). They are given by

$$I_2(t) = \frac{1}{2}\left[\sqrt{i_x^2(t) + 4I_C^2} - i_x(t)\right] \tag{3.3}$$

$$I_4(t) = \frac{1}{2}\left[\sqrt{i_x^2(t) + 4I_C^2} + i_x(t)\right] \tag{3.4}$$

Now, assuming that the magnitude of the current $i_x(t)$ is much smaller than $2I_C$, (3.2) and (3.3) lead to

$$R_X = \frac{V_{BA}(t)}{i_x(t)} = \frac{V_T}{2I_C} \tag{3.5}$$

This relationship shows that the small signal resistance of the X terminal of the controlled conveyor is equal to $R_X = V_T/2I_C$. Therefore, it can be controlled by biasing current I_C of the loop.

3.2. Advantage of the Controlled Conveyor for Non-ideality Compensation

Some circuits require resistor-matching conditions to realize a filter function. These matching conditions usually depend on the current and/or voltage gain of the current conveyors. Since large deviations in the gain parameters might occur during IC implementation, it is very difficult to be sure about the matching conditions after manufacturing. For a number of cases however, it is possible to compensate for the non-idealities of the voltage and current gains by tuning the resistor matching conditions with the controlled conveyor. Therefore, the effect of the deviations of the active element can be fully compensated for by tuning the resistor matching conditions due to controlled conveyor. In this section, this advantage of the controlled conveyor is shown with an all-pass filter example (Metin *et al.*, 2003), which includes a grounded capacitor, a resistor and a controlled conveyor.

3.2.1. The Proposed First-order All-pass Filter for Non-ideal Gain Compensation

Considering the non-idealities arising from the physical implementation, the terminal relationship of the CCCII can be given as (Fabre *et al.*, 1996),

$$V_X = \beta V_Y + R_X I_X \qquad I_Y = 0 \qquad I_Z = \pm\alpha I_X \tag{3.6}$$

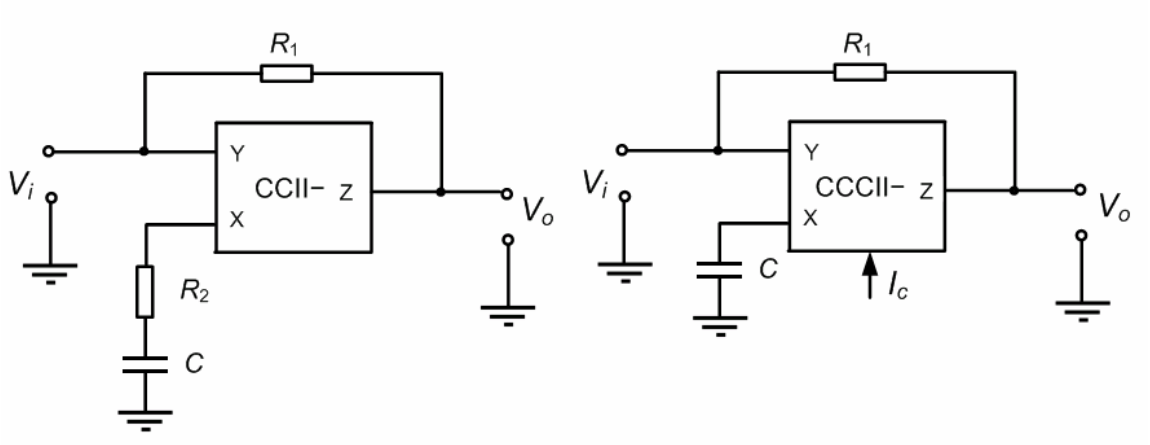
where ideally β=1 and α=±1, they represent respectively non-ideal voltage and current gains. Here, if the sign of α is equal to +1, this corresponds to a positive type CCCII (CCCII+). If it is equal to –1, this corresponds to a negative type CCCII (CCCII–). The current convention is such that all currents flow into the device. Equation (3.6) resembles

(2.22) for R_X=0. The proposed first-order all-pass filter using a single CCII– is shown in Fig. 3.2(a). Its voltage transfer function can be expressed as,

$$\frac{V_o}{V_i} = \frac{1 + sCR_2 - sCR_1}{1 + sCR_2} \tag{3.7}$$

With R= R_1/2= R_2, (3.7) reduces to

$$\frac{V_o}{V_i} = \frac{1 - sCR}{1 + sCR} \tag{3.8}$$



(a) (b)

Figure 3.2. (a) All-pass filter with a single CCII– (b) All-pass filter with a single CCCII–

The CCCII– based all-pass filter is given in Fig. 3.2(b). Its voltage transfer function is the same as given in equation (3.8) with R_X=R_2=R, where R_X is the X-terminal parasitic resistance of the CCCII–, which can be expressed as in (3.5). The non-ideal transfer function of the CCCII– based all-pass filter can be given as,

$$\frac{V_o}{V_i} = \frac{1 + sC(R_2 - \alpha\beta R_1)}{1 + sCR_2} \tag{3.9}$$

Therefore, all the non-ideal effects could be fully compensated for proper matching condition (R_X = R_2 = $\alpha\beta R_1$/2) due to the CCCII–.

3.2.2. Experimental and Simulation Results

In order to verify the above given theoretical analysis, the proposed all-pass filter with a pole frequency of $f_0 \cong 33.86$kHz is designed with passive element values of R_1=2kΩ, R_2=1kΩ, and C=4.7nF. The passive element tolerances are 2 per cent and 5 per cent. The active elements used in these designs are the commercially available CFOA AD844 of Analog Devices with supply voltages of V_{DD} = 12V and V_{SS} = –12V. Two AD844s were used to implement the CCII–. Theoretical results and measurement data of the gain and phase responses are depicted in Fig. 3.3.

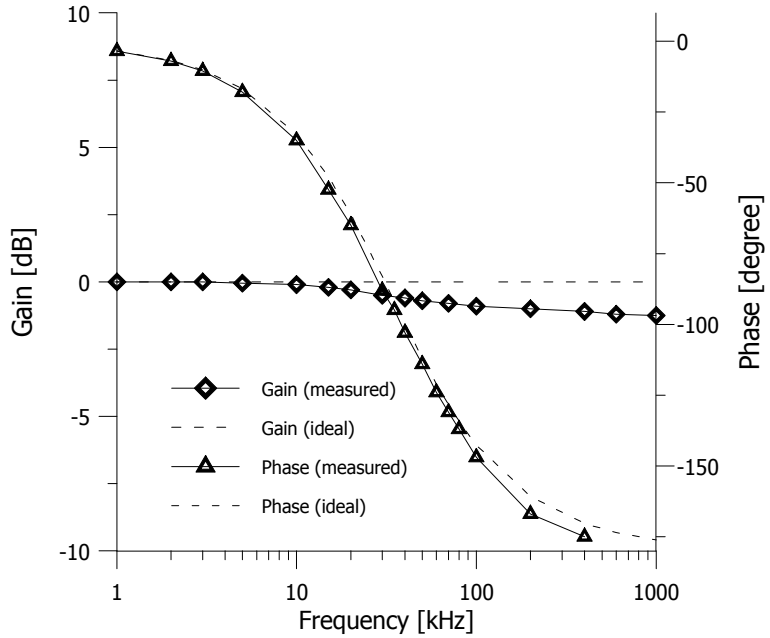


Figure 3.3. The theoretical and measured gain and phase responses of the proposed all-pass filter implemented with two AD844s

In addition to the experiments, a high performance low-voltage BiCMOS CCCII– is designed. The designed CCCII– is a modified version of that given in (Seguin and Fabre, 2001a). It operates in class-A and is illustrated in Fig. 3.4. For the simulations, 0.35μm BiCMOS real process parameters from AMS were used. This technology incorporates vertical NPN transistors with transition frequencies (f_T) up to 20GHz. For all the NMOS transistors the sizes were W=10μm and L=1μm. For the PMOS transistors the sizes were W=10μm, L=0.7μm for M_5, M_6, M_9 and W=15μm, L=0.35μm for M_7, M_8. For the class-A

conveyor employing high performance NPN bipolar junction transistors (BJTs), (3.5) should be modified as (Seguin and Fabre, 2001a):

$$R_X = V_T / I_C \tag{3.10}$$

The passive element values are R_1=1kΩ, I_B=52μA (corresponds to R_X=R_2=500Ω), C=20pF to achieve a pole frequency f_{0ideal}=15.9MHz. The supply voltages are V_{DD} = 1.65V and V_{SS} = –1.65V. Theoretical and simulation results of the gain and phase responses are depicted in Fig. 3.5.

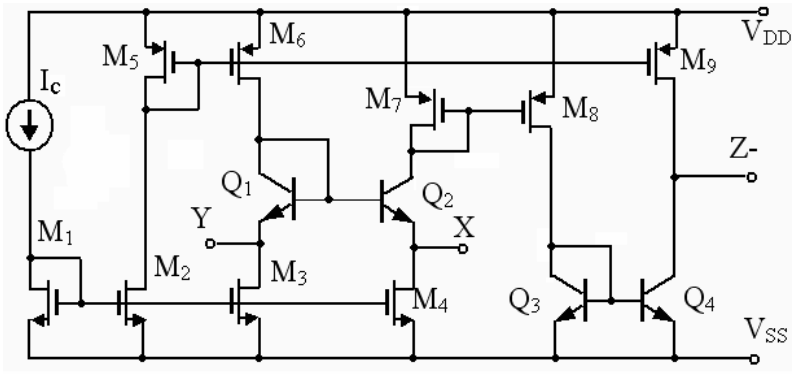


Figure 3.4. Class-A CCCII– implementation using BiCMOS technology

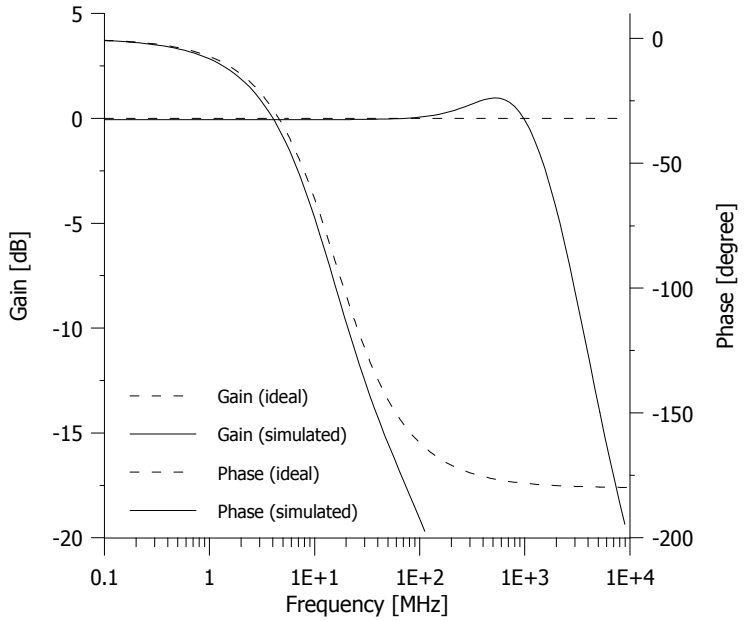


Figure 3.5. Theoretical and simulated gain and phase responses of the first order all-pass filter implemented with the BiCMOS CCCII– in Fig. 3.4

Simulation and experimental results agree quite well with the theoretical analysis. Note that the discrepancies in gain and phase characteristics at high frequencies are also affected from the poles of voltage and current gains as well as from the terminal parasitics of the active elements.

3.3. Obtaining High Input Impedance VM Filter Using First Generation Current Conveyor

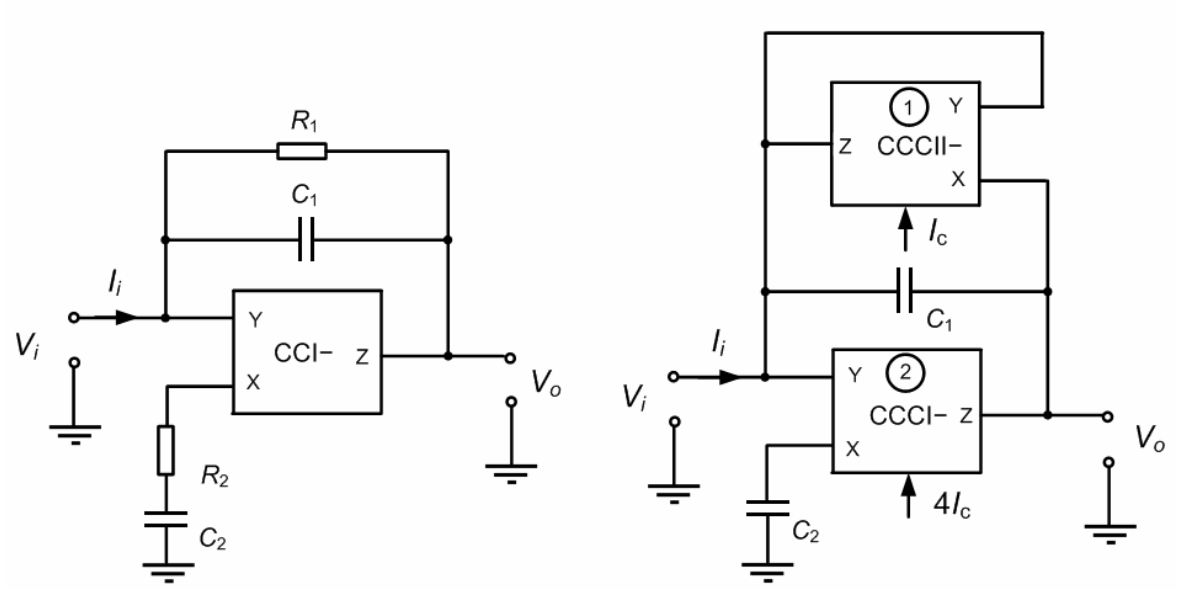
The supposed advantage of the second generation current conveyor over first generation one is its high input impedance Y terminal. Thus, second generation current conveyor can be used in the design of cascadable VM filters. Nevertheless, the first generation current conveyor can also provide high input impedance in some situations that the second generation cannot. In this section, a VM second order all-pass filter is proposed with high input impedance feature. Also, a current controlled CCI (CCCI) is shown being derived from (Fabre *et al.*, 1996) so that the proposed filter can provide electronic tunability. Simulations are performed to verify the theoretical results.

3.3.1. Tunable All-pass Filter Using First Generation Current Conveyor

This section presents a case that the CCI is able to provide cascadability for a VM filter, where CCII is not. A tunable and resistorless VM all-pass filter is presented with additional high input impedance feature. The presented circuit shown in Fig. 3.6(a) includes only two capacitors having two less resistors than (Soliman, 1999; Higashimura and Fukui, 1988). Also, only two controlled conveyors are sufficient for a tunable and resistorless design as shown in Fig. 3.6(b). Furthermore, the presented filter offers simpler element matching conditions compared to its counterparts.

The proposed filter is very suitable for high frequency applications, since a capacitor between the input and the output of the filter introduces a feed-forward path at high frequencies. Thus, non-idealities of the active component are ineffective at high frequencies. Note that in this case all signal power is provided by the driving signal source.

In the presented example filter, the quality factor value Q is 0.5 like (Soliman, 1999). Fortunately, the benefit of the all-pass filters whose Q values between 0.3 and 0.558 are remarked in (Schaumann and Valkenburg, 2001). They can provide very flat delay equalization. For Q=0.558 maximally flat delay equalization is obtained (Schaumann and Valkenburg, 2001) and the proposed circuit's Q value is very close to that value. Consequently, due to advantages mentioned above, such as high input impedance, reduced number of components and feed forward capacitor, the proposed circuit will be very useful for the delay equalization of the second order filters.



(a) (b)

Figure 3.6. (a) The proposed cascadable all-pass filter implemented with a CCI– (b) Electronically tunable version of (a)

3.3.2. Presented Tunable All-pass Filter Circuit

The terminal relationships of the negative type CCCI (CCCI–) can be characterized with the following equations,

$$V_X = \beta\, V_Y + R_X I_X, \qquad I_Y = \gamma I_X, \qquad I_Z = -\alpha I_X \tag{3.11}$$

here β, γ and α are the voltage and current gains of the CCCI–. Also, for R_X =0, this is called CCI–. The current convention is such that all currents directions are into the device.

A controlled conveyor implementation is given in Fig. 3.7 and a CCCI– is obtained when S1 is closed and a CCCII– is obtained when S1 is open. The transfer function of the presented circuit in Fig. 3.6(a) is given for the ideal case (β = 1, γ = 1, and α = –1) as follows,

$$\frac{V_o}{V_i} = \frac{1+(C_2R_2+C_1R_1-C_2R_1)s+C_1C_2R_1R_2s^2}{1+(C_1R_1+C_2R_2)s+C_1R_1C_2R_2s^2} \tag{3.12}$$

This transfer function yields the following all-pass response when the component matching conditions, R_1=4R_2 and C_2=4C_1 are fulfilled,

$$\frac{V_o}{V_i} = \frac{1-2C_1R_1s+C_1^2R_1^2s^2}{1+2C_1R_1s+C_1^2R_1^2s^2} \tag{3.13}$$

The pole frequency of the all-pass filter can be given as follows,

$$f = f_0 = \frac{1}{2\pi C_1R_1} \tag{3.14}$$

Passive sensitivities of the pole frequency of the presented circuits are no more than unity, such as, $\left|S_{R_1}^{f}\right| = \left|S_{C_1}^{f}\right| = 1$. Considering the active element non-idealities, the transfer function of the proposed circuit can be given as follows,

$$\frac{V_o}{V_i} = \frac{1+(C_1R_1+C_2R_2-\alpha\beta\ C_2R_1)s+C_1C_2R_1R_2s^2}{1+(C_1R_1+C_2R_2)s+C_1C_2R_1R_2s^2} \tag{3.15}$$

Equation (3.15) is independent of the current gain γ. This means that both CCI– or CCII– in the circuit in Fig. 3.6(a) would provide the same transfer function. On the other hand, the input impedance functions differ in each case as shown below in (3.16) and (3.17). Since the current gain γ is ideally equal to unity in the CCCI–, (3.16) gives high input impedance.

$$\frac{V_i}{I_i} = \frac{1+4sC_1R_2}{4sC_1\beta(\alpha-\gamma)} \tag{3.16}$$

$$\frac{V_i}{I_i} = \frac{1+4sC_1R_2}{4sC_1\beta\alpha} \tag{3.17}$$

A comparison of equation (3.16) with (3.17) clearly shows that the CCI– based version has higher input impedance over CCII– based realization thus avoiding the need of a high input impedance buffer.

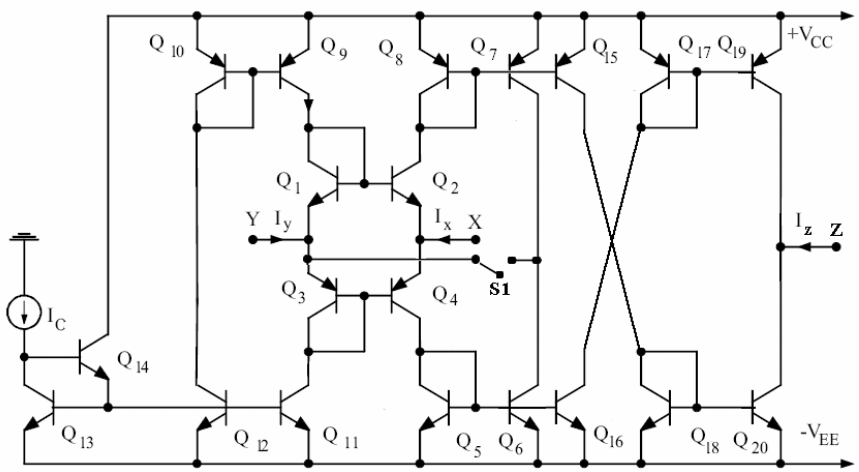


Figure 3.7. A controlled current conveyor implementation (a) When S1 is open, CCCII– is obtained (b) When S1 is closed, CCCI– is obtained

3.3.3. Experimental and Simulation Results

The operation of the proposed filter is verified by an experiment. The proposed circuit in Fig. 3.6(a) is designed with the passive element values R_1=2kΩ, R_2=500Ω, C_1=0.5nF, and C_2=2nF to obtain a second-order all-pass filter with a pole frequency of f_0≅159.2kHz. The CCII– is used in the experiments, because both CCII– and CCI– realize the same all-pass transfer function for the circuit in Fig. 3.6(a). The CCII– is implemented with two commercially available CFOA AD844s. The power supply voltages are +12V and –12V. Theoretical results and measurement data of the phase and gain responses are

depicted in Fig. 3.8. The deviation from the ideal pole frequency is around 3 per cent for the all-pass response.

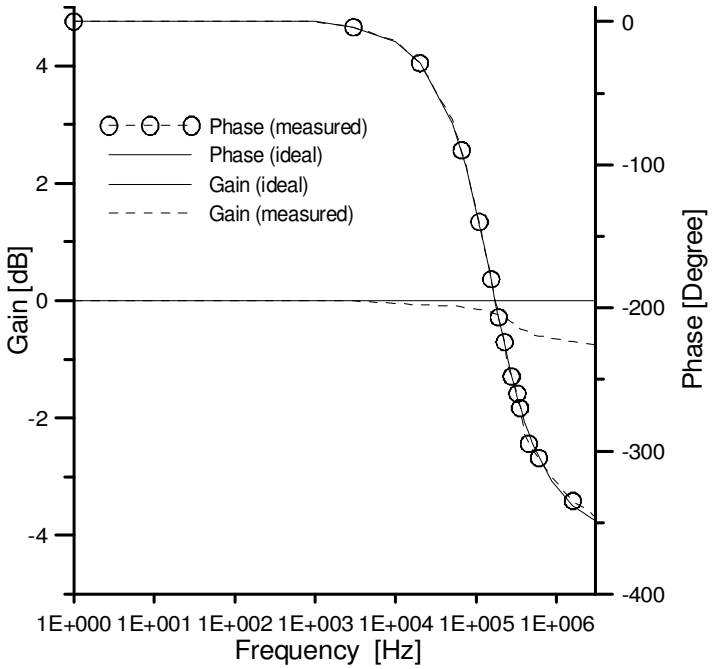


Figure 3.8. The theoretical and measured gain and phase response ($f_0 \cong 159.2$kHz)

In addition to the experiments, a high performance CCCI– is derived from (Fabre *et al.*, 1996) in order to illustrate the performance of the proposed circuit at high frequencies. For the simulations, ALA400 bipolar real process parameters from AT&T are used as shown in Table 3.1. For the employed current conveyor, the parasitic R_X resistance is given as in (3.5).

Table 3.1. ALA400 bipolar real process parameters from AT&T

.MODEL PR100N PNP (IS=73.5E-018 BF=110 VAF=51.8 IKF=2.359E-3 ISE=25.1E-16 NE=1.650 BR=0.4745 VAR=9.96 IKR=6.478E-3 RE=3 RB=327 RBM=24.55 RC=50 CJE=0.180E-12 VJE=0.5 MJE=0.28 CJC=0.164E-12 VJC=0.8 MJC=0.4 XCJC=0.037 CJS=1.03E-12 VJS=0.55 MJS=0.35 FC=0.5 TF=0.610E-9 TR=0.610E-8 EG=1.206 XTB=1.866 XTI=1.7)
.MODEL NR100N NPN (IS=121E-018 BF=137.5 VAF=159.4 IKF=6.974E-3 ISE=36E-16 NE=1.713 BR=0.7258 VAR=10.73 IKR=2.198E-3 RE=1 RB=524.6 RBM=25 RC=50 CJE=0.214E-12 VJE=0.5 MJE=0.28 CJC=0.983E-13 VJC=0.5 MJC=0.3 XCJC=0.034 CJS=0.913E-12 VJS=0.64 MJS=0.4 FC=0.5 TF=0.425E-9 TR=0.425E-8 EG=1.206 XTB=1.538 XTI=2)

Figure 3.9 shows the tunability of the pole frequency with control current. The capacitor values are C_1=50pF, C_2=200pF. The supply voltages are V_{DD}=2.5V and V_{SS}= –2.5V. The pole frequency of the filter is changed between 210kHz and 2.1MHz with the control current I_C (1µA for R_1=R_{X1}=13kΩ, R_2=R_{X2}=3.25kΩ and 10µA for R_1=R_{X1}=1.3kΩ, R_2=R_{X2}=325Ω). The deviation from ideal in the phase response of the circuit is due to parasitic inductive element of the X terminal of the CCCI− that is effective at high frequencies. This is verified by using a modified ideal CCCI− with an additional series inductance to the X terminal in the simulations.

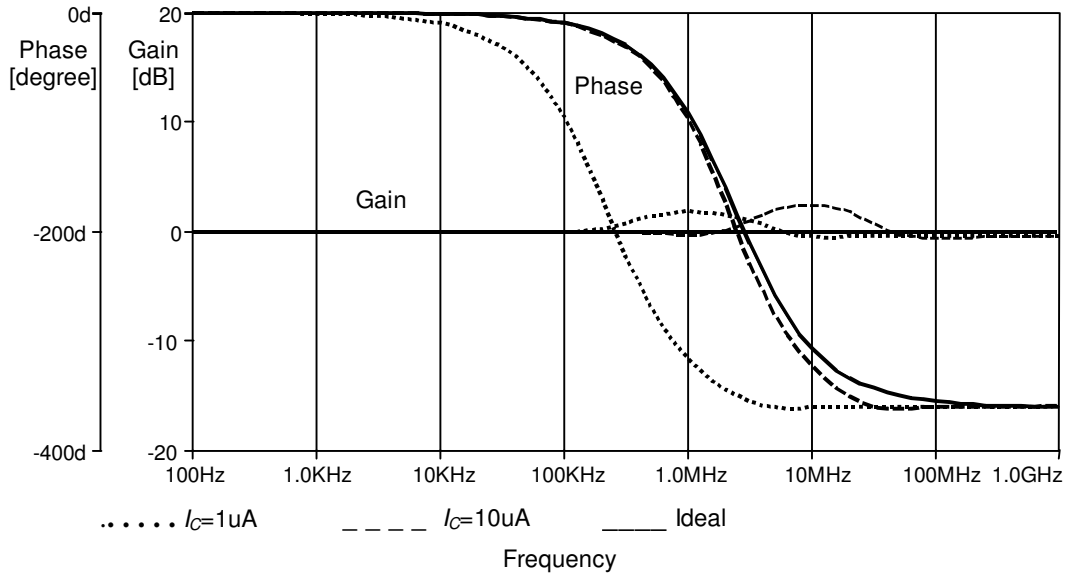
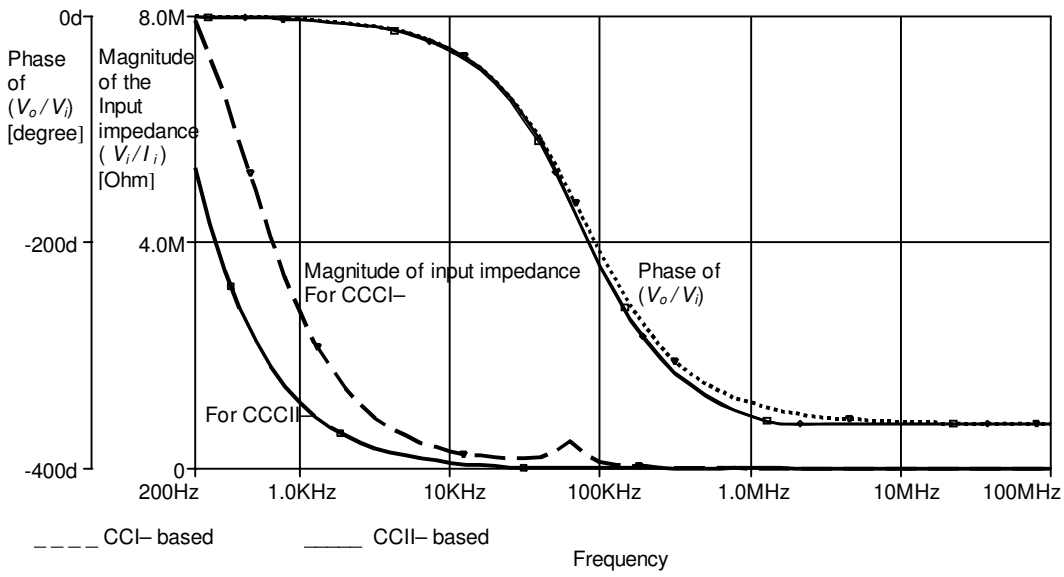
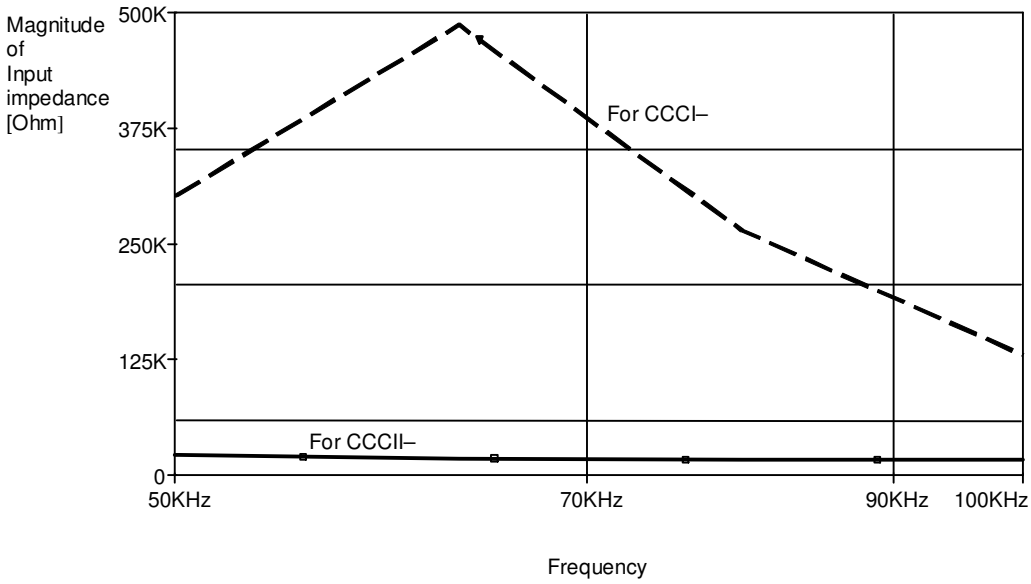


Figure 3.9. Illustrating electronic tunability of the proposed circuit

The magnitude of the input impedance of presented all-pass filter in Fig. 3.6(b) is shown in Fig. 3.10(a). We have replaced the second current conveyor in Fig. 3.6(b) with a CCCII– and magnitude of the input impedance for this case is also illustrated in the same figure. Moreover, the phase responses of the voltage transfer functions for both cases are also shown in Fig. 3.10(a). The passive element values are C_1=50pF, C_2=200pF, R_{X2}=R_2=40kΩ (corresponds to I_{C2}=0.325µA), R_{X2}=R_2=10kΩ (corresponds to I_{C1}=1.3µA) giving a pole frequency of $f_{0ideal} \cong$ 78kHz. Figure 3.10(b) compares the magnitudes of the input impedances for the both cases around the pole frequency, because an all-pass filter is usually operated around the pole frequency. The magnitudes of the input impedance of the CCCI– and CCCII– based circuits are respectively 280kΩ and 16kΩ.



(a)



(b)

Figure 3.10. Illustrating high input impedance property of CCI– based circuit (a) Input impedances comparison for CCI– and CCII– (b) The input impedances comparison around the pole frequency

Simulation and experimental results agree very well with the theoretical analysis. The high input impedance feature of the presented circuit for CCCI– based implementation is verified with simulations. Finally considering (3.16), note that $\alpha < \gamma$ may result unstability, therefore special care is needed.

3.4. Tunable Enhanced Dynamic Range Filters

The apparent advantage of the second generation current conveyor over first generation is supposed to be its high input impedance terminal. In this section, we show that this supposed advantage of CCII has also an inconvenience for the enhanced dynamic range in filter design.

The signal handling capability of the filters is called dynamic range. In this section, a topological form for the synthesis of filters with high dynamic range is proposed. A biquad notch/all-pass filter is shown in conformity with the given topological form. The presented circuit is compared with other notch filters in the literature. It has less number of components, better high-frequency response and dynamic range compared to others. Since the circuit includes a minimum number of resistors, it can easily provide electronically tunable circuits through resistor/controlled current conveyor replacement. It is shown that there is a trade-off between dynamic range and high input impedance property for an analog filter. Simulations are performed to verify the theoretical results.

3.4.1. Enhanced Dynamic Range Notch/All-pass Filter Circuit

Recently there is a growing interest towards low voltage low power analog filters. Reduced supply voltages however limit the voltage swings of the input/output terminals of the active building blocks. This in turn reduces the dynamic range of the filter. Thus the signal processing quality is deteriorated with associated signal to noise ratio reduction. In this section, a topological form for the synthesis of filters with high dynamic range is proposed. A simple way to provide high input impedance, which is important for cascading in VM circuits, is to apply the input signal source to the high input impedance terminal(s) of the active component(s) without any other connection to this terminal. For example the Y terminal of the CCII can be used for this purpose.

In this section, we present a VM biquad notch/all-pass filter that fits a certain topological form. It employs a single CCI, two resistors and two capacitors and has an enhanced dynamic range (Metin *et al.*, 2007). Since the number of the resistors can be reduced by one employing a controlled conveyor, we used a current controlled CCI for

realizations. The first beneficial property of the presented circuits is the use of the minimum number of resistors, in other words three fewer resistors than the circuits in (Pal and Singh, 1982; Higashimura and Fukui, 1988; Soliman, 1999; Cakir *et al*., 2005) are used. The resistors can be replaced by controlled current conveyors, as active resistors and an electronically tunable circuit is obtained without a significant increase in chip area since the number of resistors is minimal. The second advantage of the proposed circuits is electronic configurability which means that the element matching condition can be controlled electronically with the resistor in series to the X terminal to change the filtering function as notch or all-pass operation, but the circuits reported in (Higashimura and Fukui, 1988; Soliman, 1999; Cakir *et al*., 2005) would need an additional active element to be used as a resistor for changing element-matching conditions for both notch and all-pass functions. The third advantage of the proposed circuit is that it is suitable for high frequency of operation since it uses a feed-forward capacitor between its input and output. This capacitor short-circuits the input to the output at high frequencies. This property is important for notch and all-pass filters since in contrast to a low-pass or a band-pass function, both require a flat frequency response at the high frequency region. The fourth advantage of the circuit is reduced total harmonic distortion as a result of enhanced dynamic range. Moreover there is another mechanism that is effective at high frequencies. Due to the feed-forward capacitor the active element is bypassed and very low THD is obtained. In this case however one should ensure that the input signal source is capable to drive the load at the output since the active filter is bypassed and the load is driven directly by the input signal source. SPICE simulations and Routh-Hurwitz stability analysis are performed to illustrate the functionality of the circuit. Furthermore the presented circuit is compared with other VM notch/all-pass filter circuits (Higashimura and Fukui, 1988; Soliman, 1999) in terms of frequency response and THD.

3.4.2. Dynamic Range Considerations of Current Conveyor Based Filters

The THD performance of an analog filter is related to the magnitude of the voltage swings at the terminals of the active component. The allowed maximum voltage swings are related to the magnitude of the supply voltages and to the non-linearity of the active device. For analog voltage-mode filters where high input impedance is desired the input port is selected to be the Y terminal of the current conveyor. This in turn fixes the voltage

swings at the Y terminal and at the X terminal independent of the voltage gain of the overall circuit. For maximum performance, the output node of the filter should be selected such that it has the maximum voltage swing. For the CCCII (Fabre *et al.*, 1996) given in Fig. 3.11 as an example, the Y terminal voltage swing is equal to $-V_{EE}+ V_{EB}+V_{CESAT}<V_Y<V_{CC}-V_{BE}-V_{ECSAT}$, that is around ±1.6V for ±2.5V power supply. One can derive advantages about the dynamic range if the input signal source is applied to a passive network rather than directly to a terminal of the active element. In this case the input signal may be voltage divided by the passive RC network and then applied to the input terminals of the active block as shown in Fig. 3.12. This property is strongly topology dependent, thus the input range enhancement can be different for each topology.

The output however is to be taken directly from a terminal that has the largest signal swing. For example for the current conveyor in Fig. 3.11, maximum possible voltage swing at the Z terminal is slightly higher than the Y terminal. In fact, $-V_{EE}+V_{CESAT} < V_Z <V_{CC}-V_{ECSAT}$ which is around ±2.3V for the ±2.5V power supply. In some cascadable topologies (Higashimura and Fukui, 1988; Soliman, 1999) the input signal is applied directly to the high input impedance terminal of the active component, therefore a trade-off exists between the dynamic range and the high input impedance property for the analog filter.

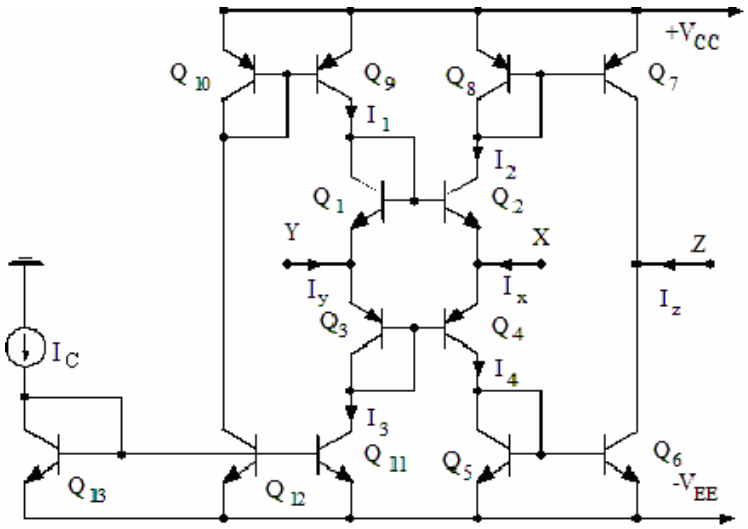


Figure 3.11. The current controlled current conveyor (CCCII)

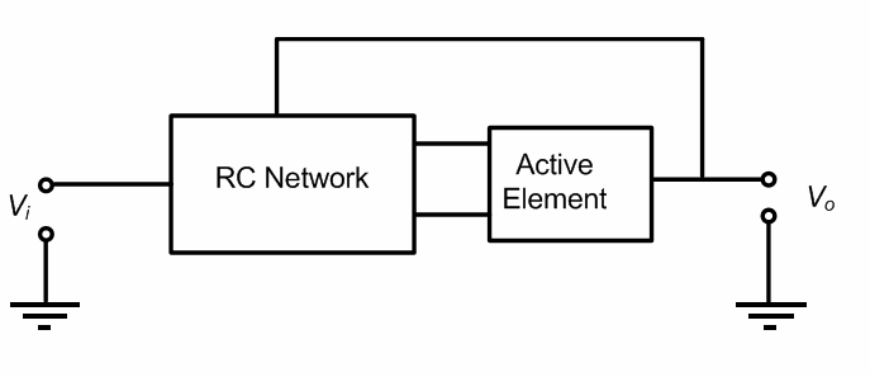
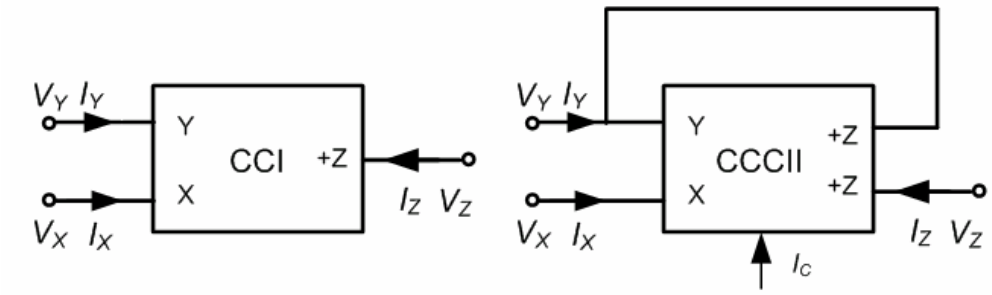


Figure 3.12. The general topology for enhanced dynamic range

For an analog filter the resistor replacement by a CCCII– enables tunability, in this case the X terminal behaves as one of the ports and the Y terminal connected to Z behave as the other port of the realized resistor. However one should note that unlike a passive resistor the CCCII– based active resistor cannot be considered as a bilateral two-port element. Rather it behaves as a resistor with different voltage swing restrictions on both ends. From this view as a resistor connection, the X terminal of the CCCII– should be connected to the higher voltage swing node compared to its Y-Z terminal connected node in the circuit. In case of Fig. 3.11 the voltage at the X terminal will be $V_X = \beta V_Y + R_X I_X$ under the condition of $I_X << 2I_C$. Here, β is the voltage transfer ratio and R_X is the parasitic resistor at the X terminal. As long as the condition of $I_X << 2I_C$ is satisfied, R_X active resistor value should be selected to reduce the voltage swing effects on the X terminal for the enhanced dynamic range.

3.4.3. The Description of the Presented Notch/All-pass Filter Circuit

The CCI as an active element can be useful in realizing single CCI-based high-output impedance CM filters since the output current can be fed back without altering the high impedance of the output port (Aronhime *et al.*, 1990). However, in this section we show the usability of the CCI in VM filters. The electrical symbol of the first-generation current conveyor (Smith and Sedra, 1968) is shown in Fig. 3.13(a). A current controlled CCI (CCCI) can be obtained from the Fabre's CCCII (Fabre *et al.*, 1996) as shown in Fig. 3.13(b).



(a) (b)

Figure 3.13. (a) Circuit symbol of the CCI (b) Obtaining current CCCI from the dual output CCCII

The terminal relationship of the CCCI that is repeated here for convenience can be characterized with the following equations,

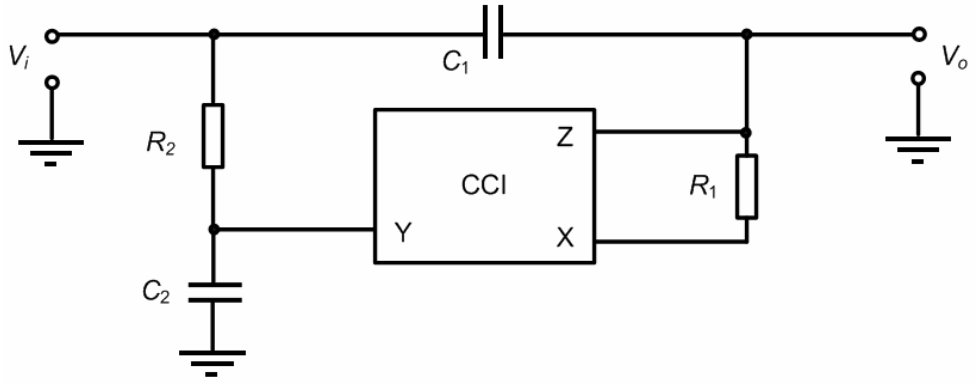
$$V_X = \beta\, V_Y + R_X I_X, \qquad I_Y = \gamma I_X, \qquad I_Z = \alpha\, I_X \tag{3.21}$$

where ideally $\beta = 1$, $\alpha = 1$, $\gamma = 1$ and they represent the voltage or current transfer ratios of the current conveyor. Also, R_X is the parasitic resistance at the X terminal of the conveyor (Fabre, *et al*., 1996).

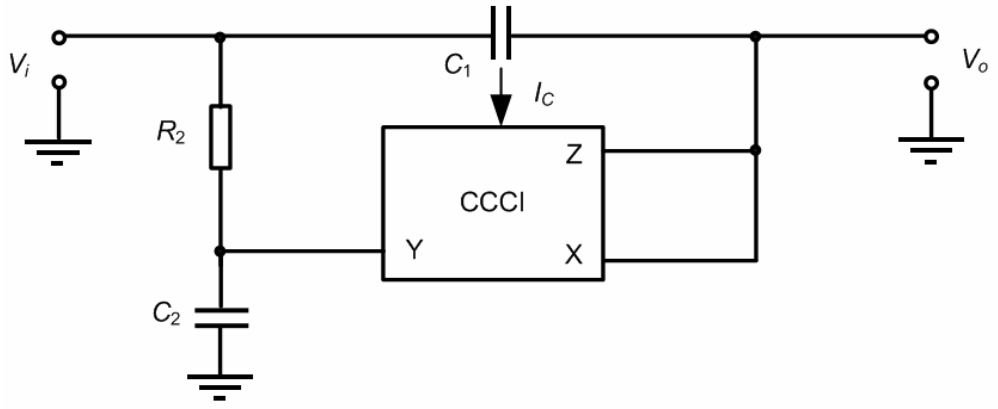
The proposed circuit is shown in Fig. 3.14(a). The number of the resistors can be reduced by one by using CCCI instead of CCI as shown in Fig. 3.14(b). In this case R_1 is replaced with the R_X of the CCCI. Since the number of resistors is minimal, replacing the R_2 with a CCCII– provides an electronically tunable filter as shown in Fig. 3.14(c). The transfer functions are given for the ideal case (α=1, β=1 and γ=1) as follows,

$$\frac{V_o}{V_i} = \frac{2 + sC_1(R_1 - R_2) + s^2 C_1 C_2 R_1 R_2}{2 + 2sC_2 R_2 + sC_1(R_1 - R_2) + s^2 C_1 C_2 R_1 R_2} \tag{3.22}$$

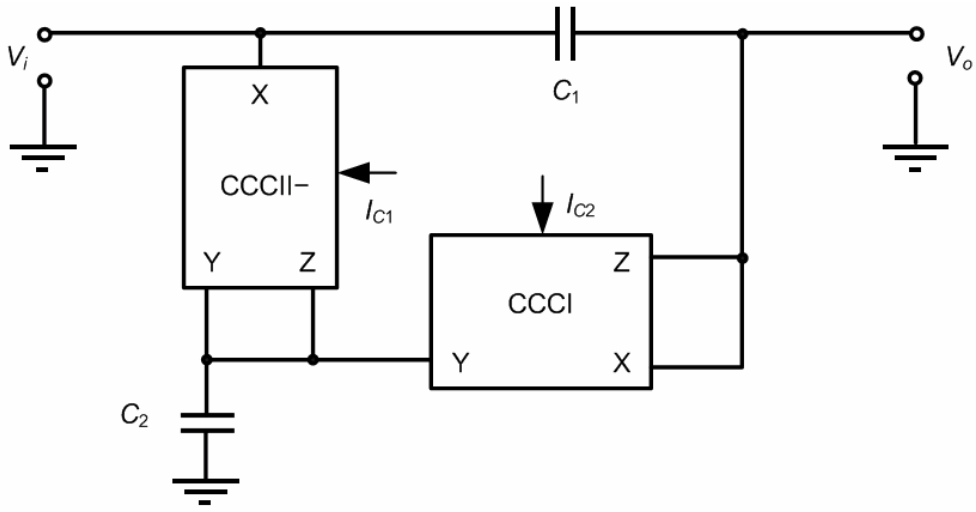
The quality factor and the angular pole frequency (ω_0) for the filter can be given as follows: $Q = \sqrt{2R_1R_2C_1C_2}\,/(2R_2C_2 + (R_1 - R_2)C_1)$, $\omega_0 = \sqrt{2/(R_1R_2C_1C_2)}$. Sensitivities of ω_0 with respect to the capacitors and resistors are one half in magnitude. Sensitivities of the Q to the capacitors and resistors are shown in Table 3.2.



(a)



(b)



(c)

Figure 3.14. (a) The proposed circuit with CCI for enhanced dynamic range (b) The proposed circuit with current controlled CCI for enhanced dynamic range (c) The proposed circuit with current controlled conveyors for electronic tunability

Table 3.2. Sensitivities of Q to passive components

$S_{R_1}^{Q} = -S_{R_2}^{Q}$	$\frac{1}{2} - \frac{C_1 R_1}{2C_2 R_2 + C_1(R_1 - R_2)}$
$S_{C_1}^{Q}$	$-\frac{1}{2} + \frac{2C_2 R_2}{2C_2 R_2 + C_1(R_1 - R_2)}$
$S_{C_2}^{Q}$	$-\frac{1}{2} + \frac{C_1(R_1 - R_2)}{2C_2 R_2 + C_1(R_1 - R_2)}$

Equation (3.22) yields the following notch response when the element matching condition of R_1=R_2=R is fulfilled,

$$\frac{V_o}{V_i} = \frac{2 + s^2 C_1 C_2 R^2}{2 + 2sC_2 R + s^2 C_1 C_2 R^2} \tag{3.23}$$

Considering the active element non-idealities as given in (3.21), the transfer function in (3.23) becomes:

$$\frac{V_o}{V_i} = \frac{\beta(1+\alpha) + sC_1 R(1-\beta\gamma) + s^2 C_1 C_2 R^2}{(1+\alpha) + sR(C_1(1-\beta\gamma) + C_2(1+\alpha)) + s^2 C_1 C_2 R^2} \tag{3.24}$$

Equation (3.24) shows that angular pole frequency and the Q of the transfer function are $\omega_0 = \frac{1}{R}\sqrt{\frac{\alpha+1}{C_1 C_2}}$ and $Q = \frac{\sqrt{C_1 C_2(\alpha+1)}}{C_1(1-\beta\gamma) + C_2(\alpha+1)}$.

Equation (3.22) can be converted to an all-pass response if the element matching condition R_2= $C_1R_1/(C_1-C_2)$ is fulfilled.

$$\frac{V_o}{V_i} = \frac{2(C_1 - C_2) - sC_1 C_2 R_1 + s^2 C_1^2 C_2 R_1^2}{2(C_1 - C_2) + sC_1 C_2 R_1 + s^2 C_1^2 C_2 R_1^2} \tag{3.25}$$

Considering the active element non-idealities as shown in (3.21), the transfer function in (3.25) can be given as follows,

$$\frac{V_o}{V_i}=\frac{\beta(\alpha+1)(C_1-C_2)-sC_1R_1(C_2-C_1+C_1\beta\gamma)+s^2C_1^2C_2R_1^2}{(\alpha+1)(C_1-C_2)+sC_1R_1(C_2\alpha+C_1-C_1\beta\gamma)+s^2C_1^2C_2R_1^2} \tag{3.26}$$

Equation (3.26) shows that angular pole frequency and the quality factor of the transfer function are $\omega_0=\frac{1}{R_1}\sqrt{\frac{(C_1-C_2)\ (\alpha+1)}{C_1^2C_2}}$ and $Q=\frac{\sqrt{(C_1-C_2)C_2(\alpha+1)}}{C_1(1-\beta\gamma)+C_2\alpha}$. Note that the angular pole frequencies of the filters are independent of the voltage gain β and the current gain $\gamma$of the CCI.

3.4.4. The Effects of the Frequency Limitations of the Current Conveyor Gains

Since the X and the Y terminals of the CCI behave as a negative impedance converter (NIC), the stability of the CCI based circuits should be taken into consideration more carefully. Thus, we apply Routh-Hurwitz stability criteria to examine the effects of the frequency dependent non-ideal voltage gain, $\beta(s)$ and the current gains; $\gamma(s)$ and $\alpha(s)$. We assume that the current gains and the voltage gain have only single corner angular frequencies which are denoted as ω_α, ω_γ and ω_β respectively. Therefore, these gains can be modeled as,

$$\beta(s)=\frac{\beta_0}{1+\frac{s}{\omega_\beta}} \qquad \gamma(s)=\frac{\gamma_0}{1+\frac{s}{\omega_\gamma}} \qquad \alpha(s)=\frac{\alpha_0}{1+\frac{s}{\omega_\alpha}} \tag{3.27}$$

where α_0, γ_0 are the value of current gains and β_0 is the value of voltage gain at low frequencies. This one-pole model can give only a rough idea about stability of the circuit, since the active components have other poles and possibly zeroes at higher frequencies that may affect the stability. For simplification, we assume that the pole frequency of the voltage gain is the k times of the pole frequencies of the current gains, i.e. $\omega_\beta\approx k\omega_\alpha\approx k\omega_\gamma\approx k\omega_p$, where ω_p is the corner angular frequency of current gains. For example, the pole frequency f_β of the voltage gain, and the pole frequency f_α of the current gain are respectively 3MHz and 2.5MHz for 2μA, 10MHz and 6MHz for 4μA, and 53MHz and 23MHz for 25μA control currents (here, the pole frequency f_γ of the current gain is close to

the f_α due to duplicated current mirrors in the CCCI implementation as shown in Fig. 3.13(b), although not the same because of different loading effects, we assumed them to be equal for simplicity). Frequency dependent non-ideal transfer functions are obtained by substituting (3.27) into (3.24) for the notch filter as,

$$TF_N = \frac{V_o}{V_i} = \frac{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4}{b_0 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4} \tag{3.28}$$

where $a_0 = (1+\alpha_0)\beta_0\omega_P^2 k$, $a_1 = \omega_P k(\beta_0 + C_1 R\omega_P(1-\beta_0\gamma_0))$, $a_2 = C_1 R\omega_P(1+k+kC_2 R\omega_P)$,

$a_3 = C_1 R(1+C_2 R\omega_P(1+k))$, $a_4 = C_1 C_2 R^2$, $b_0 = \omega_P^2 k(1+\alpha_0)$,

$b_1 = \omega_P(1+k+\alpha_0 + R\omega_P k(C_2(1+\alpha_0) + C_1(1-\beta_0\gamma_0)))$,

$b_2 = 1 + R\omega_P(C_2(1+k+\alpha_0) + C_1(1+k+RC_2\omega_P k))$, $b_3 = R(C_2 + C_1(1+C_2 R\omega_P(1+k)))$,

$b_4 = C_1 C_2 R^2$

and similarly substituting (3.27) into (3.26) for the all-pass filter as,

$$TF_{AP} = \frac{V_o}{V_i} = \frac{c_0 + c_1 s + c_2 s^2 + c_3 s^3 + c_4 s^4}{d_0 + d_1 s + d_2 s^2 + d_3 s^3 + d_4 s^4} \tag{3.29}$$

where $c_0 = (C_1 - C_2)(1+\alpha_0)\beta_0\omega_P^2 k$, $c_1 = k\omega_P((C_1 - C_2)\beta_0 - C_1 R_1\omega_P(C_2 - C_1(1-\beta_0\gamma_0)))$,

$c_2 = C_1 R_1\omega_P((C_1 - C_2)(1+k) + kC_1 C_2 R_1\omega_P)$, $c_3 = C_1 R_1(C_1 - C_2 + C_1 C_2 R_1\omega_P(1+k))$,

$c_4 = C_1^2 C_2 R_1^2$, $d_0 = (C_1 - C_2)(1+\alpha_0)\omega_P^2 k$,

$d_1 = \omega_P((C_1 - C_2)k + (C_1 - C_2)(1+\alpha_0) + C_1 R_1\omega_P k(C_2\alpha_0 + C_1(1-\beta_0\gamma_0)))$,

$d_2 = C_1 - C_2 + C_1 R_1\omega_P(C_1(1+k) + C_2\alpha_0) + C_1^2 C_2 R_1^2\omega_P^2 k$, $d_3 = C_1^2 R_1(1+C_2 R_1\omega_P(1+k))$,

$d_4 = C_1^2 C_2 R_1^2$.

The Routh-Hurwitz criterion is applied on (3.28) and (3.29) to investigate the stability of the circuit. Also, the nominal values of voltage and current gains at low frequencies are assumed to be approximately equal to unity for simplification ($\alpha_0 \approx \beta_0 \approx \gamma_0 \approx 1$).

For the notch realization:

$$R^2C_1C_2>0,\qquad R(C_1(1+(1+k)RC_2\omega_p+C_2)>0,\qquad 2k\omega_p^2>0 \tag{3.30a}$$

$$\frac{C_2+(2+k)RC_2^2\omega_p+RC_1^2\omega_p(1+k+kRC_2\omega_p)(1+(1+k)RC_2\omega_p)+C_1(1+RC_2\omega_p(2(1+k)+(2+k(2+k))RC_2\omega_p))}{C_2+C_1(1+(1+k)RC_2\omega_p)}>0 \tag{3.30b}$$

$$\frac{(\omega_p((2+k)C_2(1+2RC_2\omega_p)(1+kRC_2\omega_p)+RC_1^2\omega_p(1+(1+k)RC_2\omega_p)(2+k+k^2+kRC_2\omega_p(2+k+2kRC_2\omega_p))+C_1(2+k+(2+k(2+k))RC_2\omega_p(2+RC_2\omega_p(2+k+2kRC_2\omega_p)))))}{(C_2+(2+k)RC_2^2\omega_p+RC_1^2\omega_p(1+k+kRC_2\omega_p)(1+(1+k)RC_2\omega_p)+C_1(1+RC_2\omega_p(2(1+k)+(2+k(2+k))RC_2\omega_p)))}>0 \tag{3.30c}$$

and for the all-pass realization:

$$C_1^2C_2R_1^2>0,\qquad C_1^2R_1(1+C_2R_1\omega_p(k+1))>0,\ 2k(C_1-C_2)\omega_p^2>0 \tag{3.31a}$$

$$\frac{C_1-C_2+R_1\omega_p(C_2^2+C_1^2(1+k)+C_1C_2R_1\omega_p(C_2+C_1(1+k(3+k))+C_1C_2R_1\omega_pk(1+k)))}{1+C_2R_1\omega_p(1+k)}>0 \tag{3.31b}$$

$$\frac{(\omega_p((C_1-C_2)^2(2+k)+R_1\omega_p((C_1-C_2)(C_1C_2k+C_2^2(2+k)+C_1^2(2+k+k^2))+C_1C_2R_1\omega_p(-2C_2^2-C_1C_2k(2+k+k^2)+C_1^2(2+k(4+k(2+k)))+C_1C_2R_1\omega_pk(C_1+2C_1k+C_2+C_2k(1+k)+C_1C_2R_1\omega_pk(1+k))))))}{(C_1-C_2+R_1\omega_p(C_2^2+C_1^2(1+k)+C_1C_2R_1\omega_p(C_2+C_1(1+k(3+k))+C_1C_2R_1\omega_pk(1+k))))}>0 \tag{3.31c}$$

Since all terms in (3.30) are positive and all terms in (3.31) are positive for $C_1>C_2$, the filters can be assumed stable. Note that the above calculations are first order approaches to the stability problem and do not guarantee stability. However they give an idea to the designer.

3.4.5. Electronic Configurability and Tunability

Electronic configurability permits changing the filter function simply by an external current. This is achieved by changing the element matching condition by an electronically tunable resistor. As an example consider the following case. Assume $C_1=2C_2=C$ and $2R_1=R_2=2R$ is applied to (3.22) to obtain an all-pass response whereas again $C_1=2C_2=C$ and with $R_1=R_2=R$, one obtains a notch response with the following transfer function,

$$\frac{V_o}{V_i} = \frac{4 + s^2C^2R^2}{4 + 2sCR + s^2C^2R^2} \tag{3.32}$$

Therefore, with $C_1=2C_2=C$, the resistor R_1 in Fig. 3.14(a) can be adjusted to obtain an all-pass response or a notch response. Note that if R_1 is realized with the CCCI as in Fig. 3.14(b), it is possible to configure the filtering function of the circuit electronically through the control current of the current conveyor.

Since the number of resistors is only two, controlled conveyors can be used to replace them without a significant increase in chip area as shown in Fig. 3.14(c). For example the number of resistors in circuits proposed in (Higashimura and Fukui, 1988; Soliman, 1999) is four that makes such a replacement difficult and costly.

3.4.6. Simulation Results

In this subsection tunability feature of the presented circuit in Fig. 3.14 is verified with SPICE simulations. Also, the enhanced dynamic range feature is compared with other notch filters in the literature.

3.4.6.1. Simulation Results of the Presented Circuit. To verify the theoretical analyses, we simulated the circuits proposed in Fig. 3.14 using the SPICE circuit simulation program employing the CCCI implementation based on the modification of the circuit in Fig. 3.11 according to the block diagram shown in Fig. 3.13. The CCCI was implemented by using AT&T ALA400 BJT transistors (Frey, 1993). SPICE parameters of the transistors are tabulated in Table 3.1. DC supply voltages of ±2.5V are used.

The presented circuit in Fig. 3.14(b) is designed with the passive element values R_1=4kΩ (I_C=3.25μA), R_2=4kΩ, C_1=400pF, and C_2=200pF to obtain notch filter with a center frequency of f_0≈199kHz. For realizing all-pass filtering function, the circuit in Fig. 3.14(b) is simulated using passive element values R_1=2kΩ (I_C=6.5μA), R_2=4kΩ, C_1=400pF, C_2=200pF resulting in a center frequency of f_0≈281kHz. Theoretical and simulation results of the AC analysis are depicted in Fig.s 3.15 and 3.16 for the notch and for the all-pass cases, respectively. The frequency response at high frequencies is close to ideal response due to the feed-forward capacitor C_1. To show electronic tunability of the presented circuit, the circuit in Fig. 3.14(c) as a notch filter is tested with the capacitor values of C_1=400pF, C_2=200pF. The resistor values are changed between R_1=R_2=13kΩ (I_{C1}=I_{C2}=1μA) and R_1=R_2=1.3kΩ (I_{C1}=I_{C2}=10μA) as shown in Fig. 3.17. Simulations show that the center frequency is electronically tunable between 57.5kHz and 575kHz.

3.4.6.2. Comparison with Other Notch Filter Circuits in the Literature. In order to emphasize advantage of the proposed circuit, we compared it with other notch/all-pass filter circuits shown in Fig.s 3.18 and 3.19 (Soliman, 1999; Higashimura and Fukui, 1988). For a fair comparison we obtain the CCII– used in (Soliman, 1999; Higashimura and Fukui, 1988) from the current conveyor in Fig. 3.11. The center frequency of the filter is chosen as f_0≈281kHz. The Soliman's circuit (Soliman, 1999) in Fig. 3.18 is designed with the passive element values R_a=R_b=2kΩ, C_1=C_2=400pF, R_1=1kΩ, R_2=2kΩ. The Higashimura's circuit (Higashimura and Fukui, 1988) in Fig. 3.19 is designed with the passive element values R_1=2.857kΩ, R_2=3.265kΩ, C_1=490pF, C_2=70pF, R_a=2kΩ, R_b=2kΩ (the pass-band gain cannot be made equal to unity). In the proposed circuit of Fig. 3.14(c) the passive elements are selected as C_1= 100pF, C_2=400pF, and the bias currents are I_{C1}=I_{C2}=3.25μA result in R_1=R_2=4kΩ. Frequency responses of the circuits are shown in Fig. 3.20. Due to active component non-idealities, some deviations from the theoretical value of the center frequency occur, which is around 6 per cent. Thanks to the tunability of the presented circuit in Fig. 3.14(c), we correct the deviation at the center frequency by applying I_{C1}=I_{C2}=3.35μA. The circuit proposed in (Higashimura and Fukui, 1988) has a low voltage gain for the selected element values as in the original work of Higashimura and Fukui (1988). In the circuit proposed by Soliman (Soliman, 1999), the gain decreases at 3MHz and 30MHz around 1.5dB and 3dB, respectively.

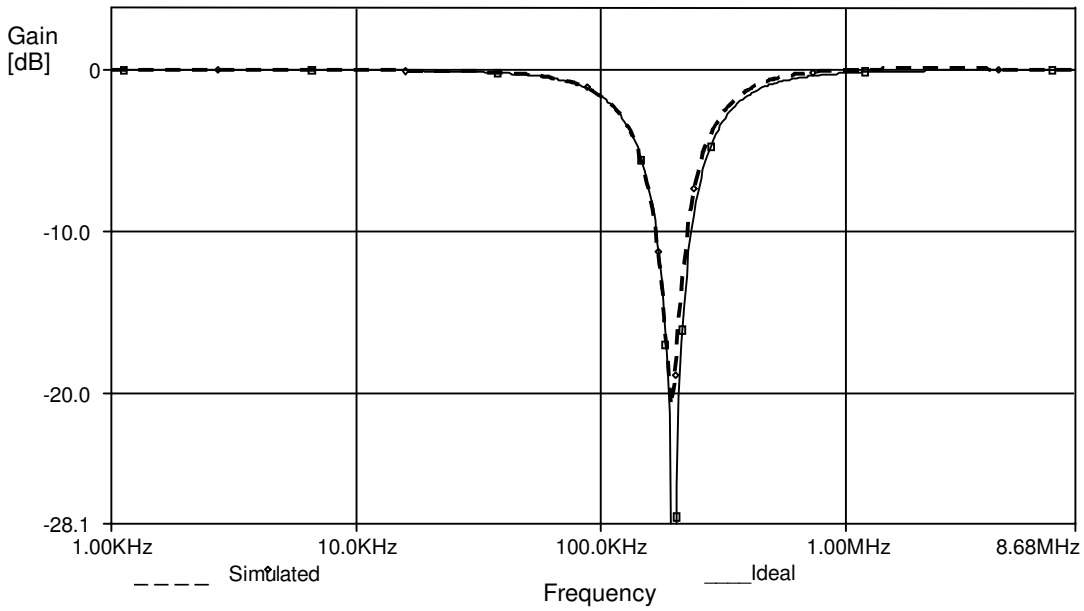


Figure 3.15. Ideal and simulated frequency responses for notch filter configuration

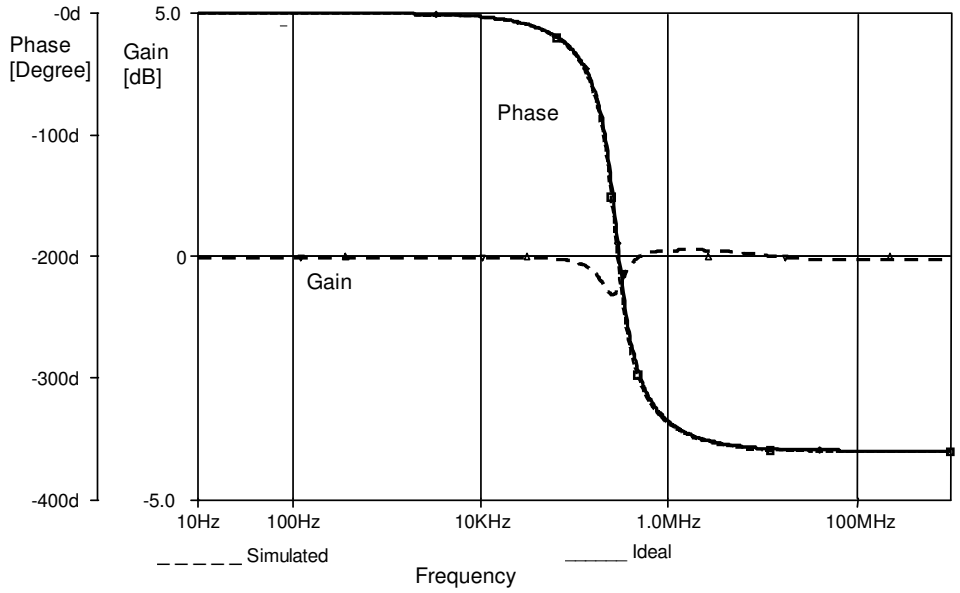


Figure 3.16. Ideal and simulated frequency responses for all-pass filter configuration

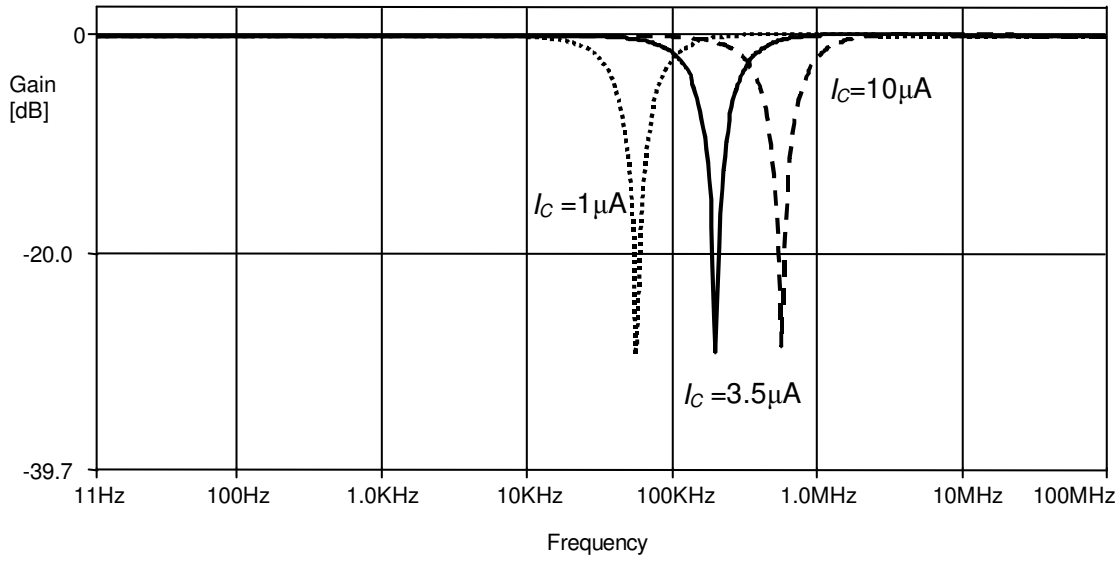


Figure 3.17. Illustrating electronic tunability of the proposed circuit (The center frequency of the filter is tuned between 57.5kHz and 575kHz through various control currents $I_{C1}=I_{C2}=I_C$)

At frequencies beyond 200MHz, the magnitude of the gains of the filters of (Higashimura and Fukui, 1988; Soliman, 1999) start to decrease rapidly. We can say that the presented circuit is better than other circuits in (Higashimura and Fukui, 1988; Soliman, 1999) from frequency response point of view.

In order to compare time domain performances of the circuits, we show total THD values using SPICE simulations in Fig. 3.21. Since the gain of the circuit in (Higashimura and Fukui, 1988) is lower than unity as in the original work of Higashimura and Fukui for the selected component values a fair THD comparison may not be possible. Instead we compared THD performances of the presented circuit with the Soliman's notch filter since in this case both circuits have approximately equal magnitude outputs. We applied 1kHz sinusoidal input signal with various amplitudes to the input of the circuit. We tested both of the circuits of Fig. 3.14(b) and 3.14(c) in terms of THD. Although the presented circuit has a slightly larger gain (0dB), its THD values are lower than the circuit in Fig. 3.18.

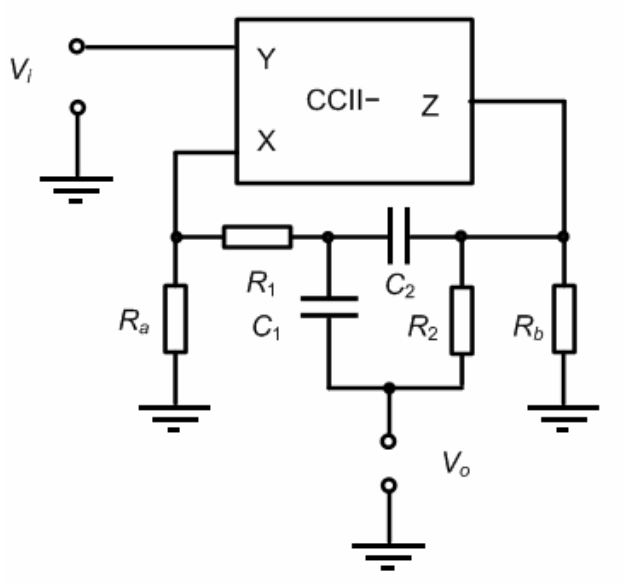


Figure 3.18. Notch/all-pass filter example in (Soliman, 1999)

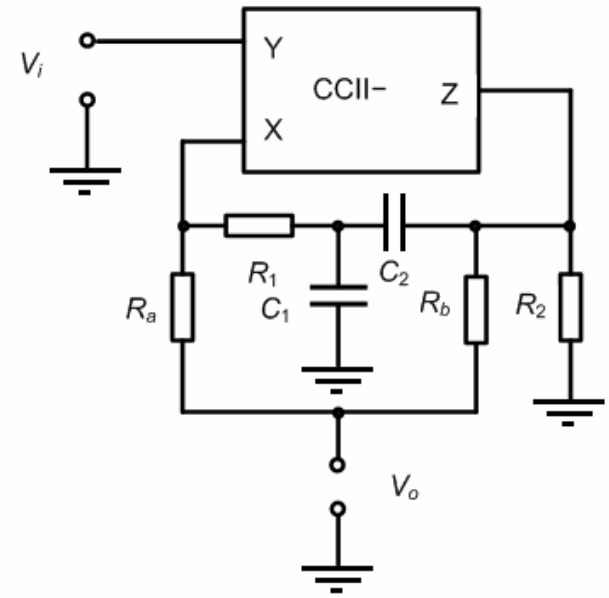


Figure 3.19. Notch/all-pass filter example in (Higashimura and Fukui, 1988)

3.5. The Advantage of CCCI over CCCII for Reduced Power Consumption

As stated before, in the literature, the studies have focused on the CCII and the CCCII. In the previous section, it is shown that the supposed advantage of the CCII, which is allowing the cascadability due to high impedance Y terminal, may be in contradiction with another important feature: Enhanced input dynamic range. In this section, a possible

advantage of the CCCI over CCCII for reduced power consumption is shown with a tunable resistorless floating FDNR simulator example.

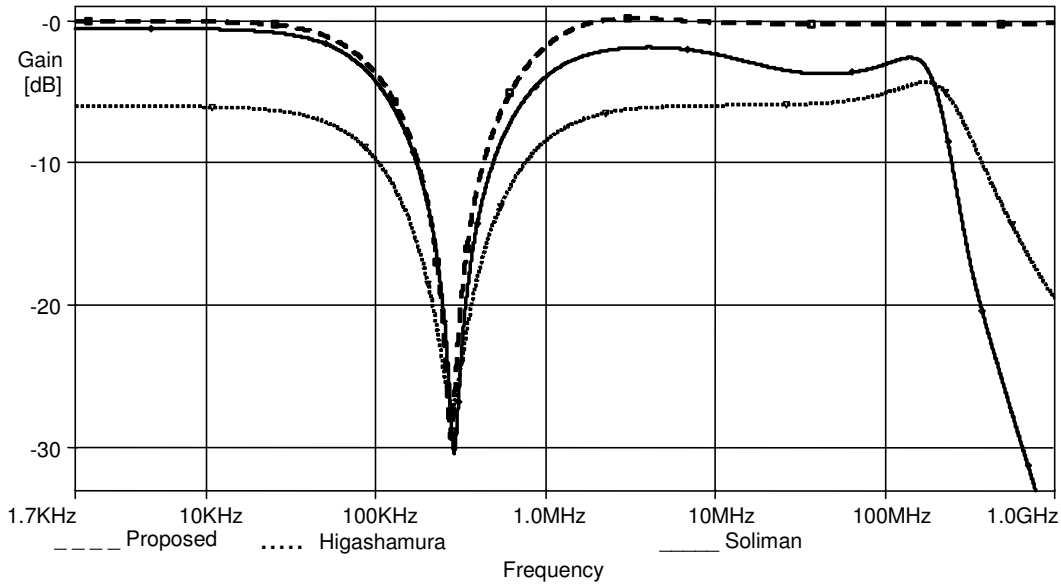


Figure 3.20. The comparison of the roll-off frequencies at high frequency region of the proposed filter with other notch/all-pass filters in the literature for $f_0 \approx 281$kHz

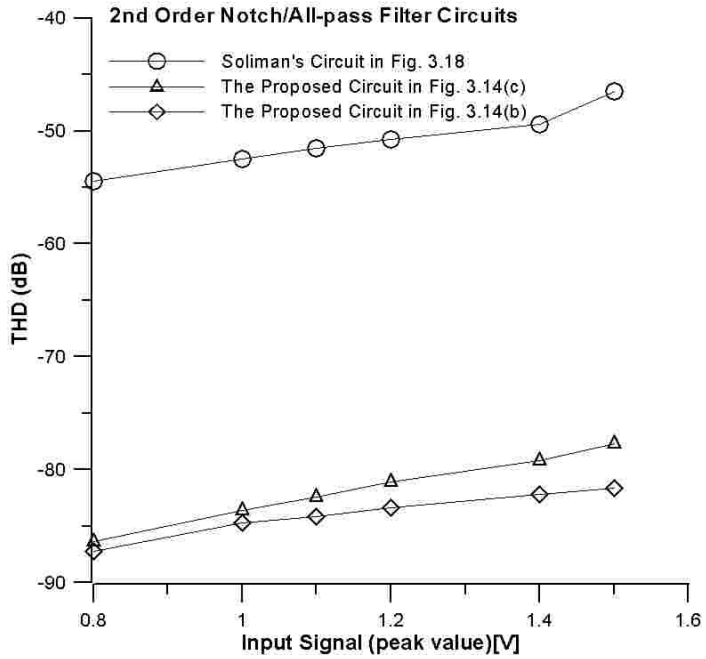


Figure 3.21. The comparison of THD values of the proposed filter with another notch/all-pass filter in (Soliman, 1999) for 1kHz sinusoidal input signal

In controlled current conveyor based circuits, topologies including resistors connected in series to the X terminal are desired. However, except this case, the parasitic resistance at the X terminal is undesired and should be ideally zero. In the controlled current conveyor structure (Fabre *et al.*, 1996), the simplest way to decrease the undesired parasitic resistor of the X terminal is to use sufficiently high biasing current, but this will increase the power consumption. On the other hand, there are some special current conveyor structures having very low parasitic resistance at the X terminal such as the circuit in (Awad and Soliman, 1999; Seguin and Fabre, 2001b), but these are not current controlled type. In analog circuit design engineering, the use of only one type of current conveyor simplifies the configuration. (Higashimura and Fukui, 1996; Horng *et al.*, 1997), so practically controlled and uncontrolled conveyors are not used together.

Due to the difficulties in the implementation of inductors in integrated circuits, inductance or FDNR simulators using active elements are widely used in the design of the LC ladder filters. Fortunately, first generation current conveyor provides better solution for FDNR circuits due to compensation feature. In fact, the CCI provides an easy method for compensating parasitic resistor in the X terminal derived from its terminal relationship.

In this section, the parasitic element compensation feature of the CCI is shown with a floating FDNR simulator example. The proposed FDNR simulator uses the same type of CCIs without element matching restriction. Furthermore, different from the CCCII, the CCCI does not need high biasing current to reduce undesired parasitic resistance at the X terminal, which is an important parameter for power consumption. The simulations are performed using SPICE program to verify the theory.

3.5.1. The Compensation of the Undesired Parasitic Resistor at the X Terminal

A CCCI can be obtained from CCCII as shown in Fig. 3.13. Also, the terminal relationship of the CCCI is given in (3.21). The compensation of the parasitic resistance at the X terminal of the CCI is done by adding a resistor in series of the Y terminal as shown in Fig. 3.22. This can be briefly explained as follows. If a compensation resistance R_C is added in series to the Y terminal of the CCCI, the following terminal relationship can be written

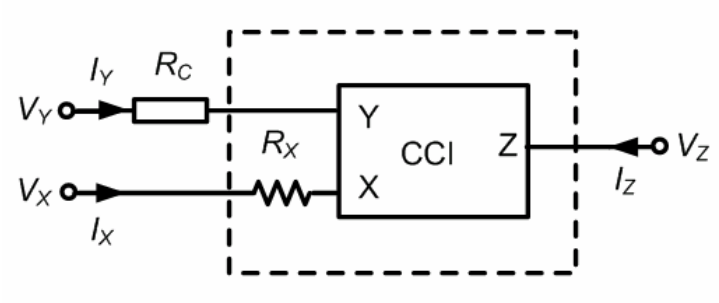


Figure 3.22. The compensation of the parasitic resistance at the terminal X of the CCI by adding an external resistor series to the terminal Y

$$V_X - I_X R_X = V_Y - I_Y R_C \tag{3.33}$$

Therefore, adding a small R_C resistor, the effect of the R_X can be compensated between the X and Y terminal voltages.

3.5.2. Description of the Circuit and the Effect of the Parasitic Resistor at the X Terminal

The proposed FDNR circuit is shown in Fig. 3.23. Employing a CCCI instead of the CCI and removing R as shown in Fig. 3.24 lead to a resistorless and electronically tunable design. The open circuit impedance matrix is given for the ideal case (β=1, γ=1, and α=1) as follows,

$$[Z] = \frac{1}{s^2 C_1 C_2 R}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{3.34}$$

Therefore the value of the FDNR is found as $D_{eq} = C_1 C_2 R = C_1 C_2 (V_T / 2I_C)$.

As explained above the parasitic resistances at the terminal X of the first and third CCIs, such as R_{X1} and R_{X3}, are undesired and they will alter the ideal FDNR behavior. Provided equal corresponding biasing currents are chosen, R_{X1} and R_{X3} will be equal to each other. For R_{X1}=R_{X3} =R_{X13}, (3.34) converts to a modified FDNR open circuit impedance matrix given for R=R_{X2} as follows,

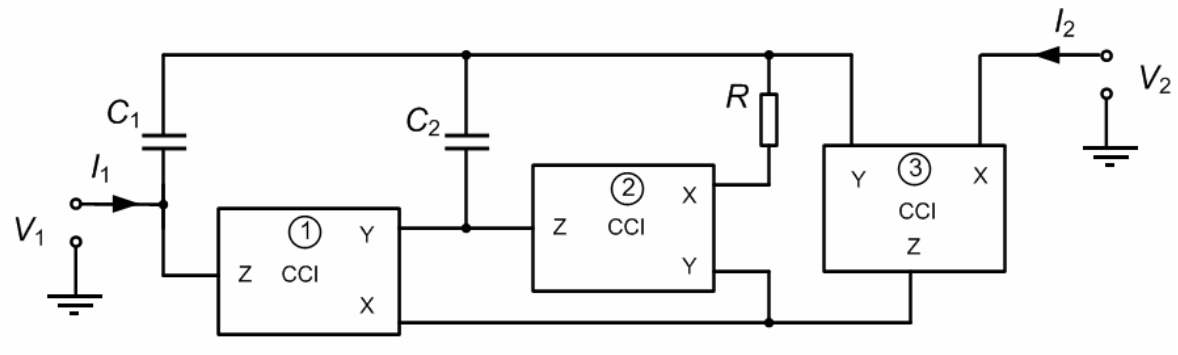


Figure 3.23. The proposed floating FDNR simulator

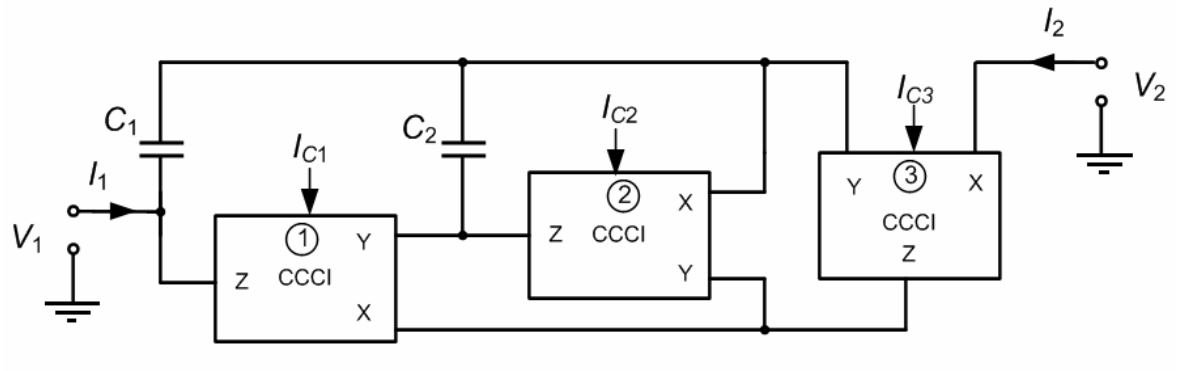
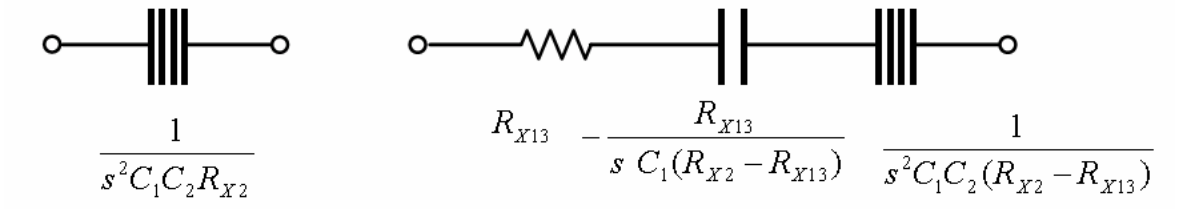


Figure 3.24. The proposed tunable floating FDNR simulator using controlled CCCIs

$$[Z]=(R_{X13}-\frac{R_{X13}}{s\ C_1(R_{X2}-R_{X13})}+\frac{1}{s^2C_1C_2(R_{X2}-R_{X13})})\begin{bmatrix}1 & -1\\ -1 & 1\end{bmatrix} \tag{3.35}$$

The parasitic elements result an equivalent resistor and a negative capacitor in series with the FDNR. The equivalent model of the modified FDNR is given in Fig. 3.25b.



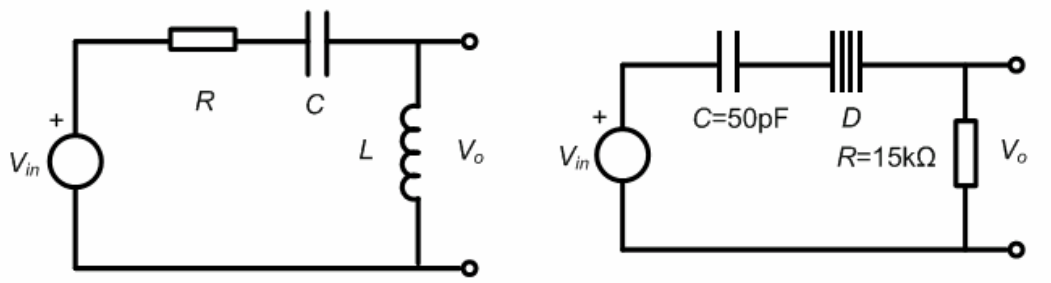
(a) (b)

Figure 3.25. (a) The ideal FDNR (b) Equivalent FDNR model with the effects of the parasitic resistor at the terminal X

3.5.3. Simulations

In the presented FDNR circuit, we obtained a CCCI modifying internal structure in Fig. 3.11 according to block diagram shown in Fig. 3.13. In the simulations, AT&T ALA400 BJT transistors parameters in Table 3.1 are used. The DC supply voltages are ±2.5V. The desired parasitic resistor at the X terminal of the second CCI is changed with external biasing current I_C for tunability. To test the tunability of the presented FDNR simulator, the RLC high-pass filter in Fig. 3.26(a) is converted to a filter circuit as shown in Fig. 3.26(b) by performing Bruton transformation. In the SPICE simulation, the capacitor values are chosen as 50pF for the filter circuit in Fig 3.26(b). The biasing currents are constant as 1mA for the first and third CCIs to minimize parasitic resistances at the X terminals (around 13Ω). The I_C biasing current of the second CCI is varied between 26μA and 130μA to change cut-off frequency of the filter in Fig. 3.26(b), so the electronic tunability of the introduced FDNR simulator is shown in Fig. 3.27. The cut-off frequency of the high-pass filter is changed approximately between 371kHz and 1.5MHz.

The high-pass filter example in Fig. 3.26(b) is given only to test the tunability of the proposed FDNR. The compensation feature of the CCI and the functionality of the proposed floating FDNR simulator are also tested on a third-order LC passive ladder prototype shown in Fig. 3.28(a). Using Bruton transformation, the circuit in Fig. 3.28(b) that can be implemented by FDNR is obtained. It is a high-pass filter that was simulated using the presented FDNR simulator in Fig. 3.24.



(a) (b)

Figure 3.26. (a) Simple high-pass resonance filter (b) Simple high-pass resonance filter obtained by Bruton transform of Fig. 3.26(a) to test tunability of the FDNR

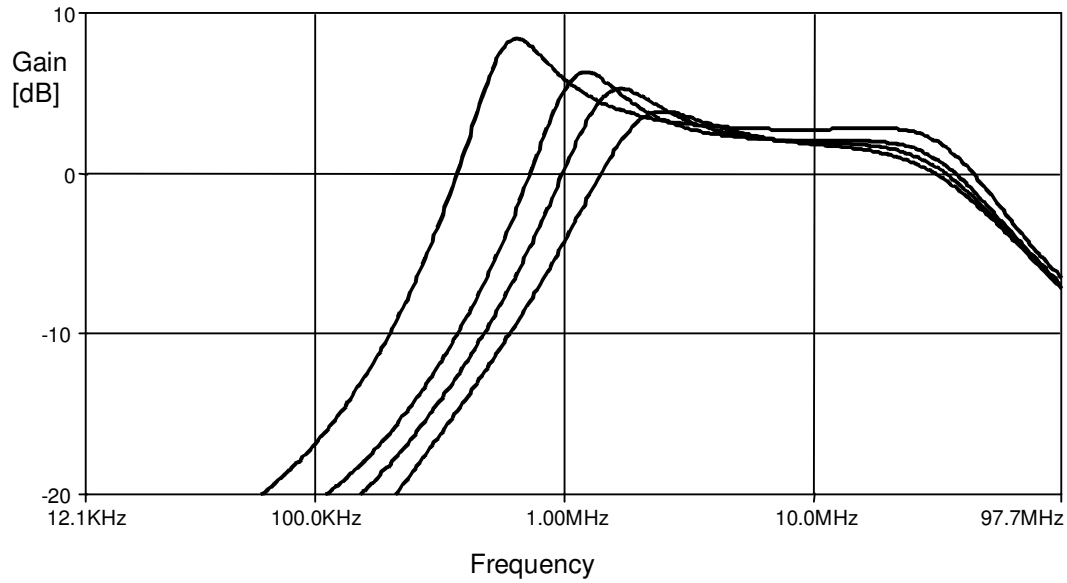
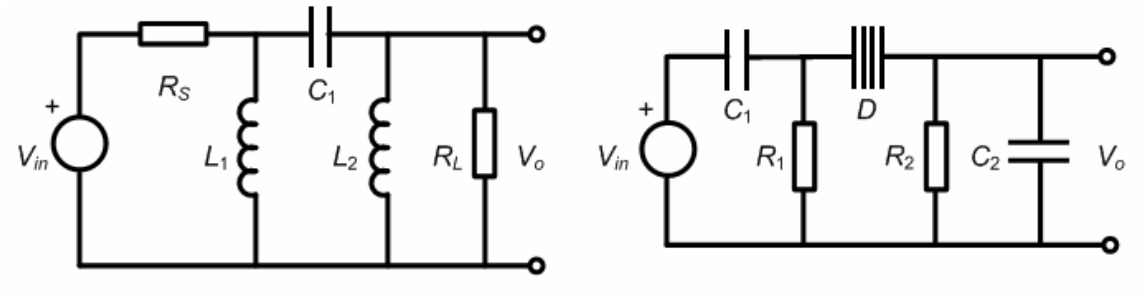


Figure 3.27. Illustration of the electronic tunability of the presented FDNR simulator



(a) (b)

Figure 3.28. (a) Example high-pass ladder prototype circuit (b) Derived circuit with Bruton transformation of the circuit in Fig. 3.28(a)

The passive element values of C_1=C_2=1nF, and R_1=R_2=1kΩ are chosen for the prototype in Fig. 3.28(b). Also C_1=C_2=1nF, and R_{X2}=0.5kΩ (I_{C2} =26μA in second CCCI) are selected for the proposed FDNR simulator in Fig. 3.24. Therefore, a third order high-pass Butterworth filter whose cut-off frequency is 159kHz is obtained. In this simulation the biasing currents are equal to 0.2mA for the first and third CCIs. In the simulation of the compensated case, R_C=35Ω resistors series to the Y terminal of the first and third were sufficient to achieve the cancellation of the effects of the R_{X13}. For the higher R_C values, parasitic inductance at the X terminal becomes dominant and a peaking occurs around 10MHz. R_C is chosen for an acceptable flat response. The theoretical, compensated and uncompensated frequency responses are depicted in Fig. 3.29. In the uncompensated case,

the roll-off starts at 4MHz due to the parasitics. However, in the compensated case, the roll-off starts at 15MHz.

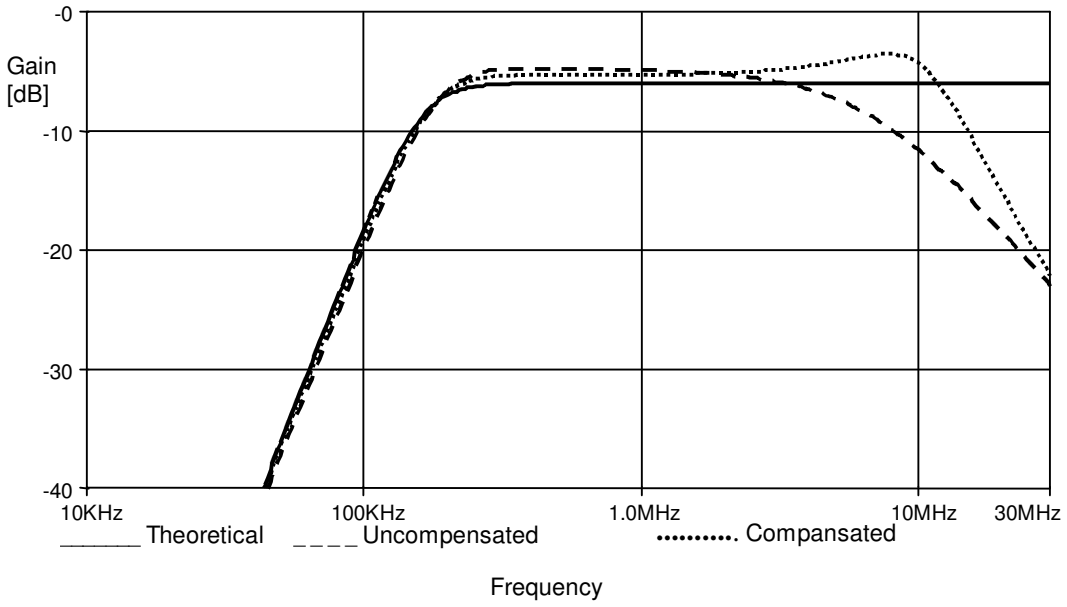


Figure 3.29. Theoretical and simulated frequency responses of the example ladder prototype with the compensated and uncompensated FDNR simulator

3.6. New Opportunities Using the Mixed Translinear Loops: Current Controlled Current Differencing Buffered Amplifier

In this section, a CMOS current controlled current differencing buffered amplifier (C-CDBA) implementation is given. Also, a novel first-order all-pass filter is proposed to show its advantages. Furthermore, an inverting buffer is used in the implementation of the C-CDBA to enrich the new circuit producing capability of the CDBA. The circuit has low output impedance for easy cascadability. Lastly, an electronically tunable band-pass filter is given as an application example using the presented all-pass filter. The theoretical results are verified with SPICE simulations.

3.6.1. The Controlled CDBA

The current conveyor and the current feed back op-amp, which is simply a buffer added to a current conveyor, are the most popular active elements in the last two-decades.

Also, an active element closely resembling them denoted as current differencing buffered amplifier (Acar and Ozoguz, 1999) has become very popular because of the following advantages: The first advantage of the CDBA is its capability of producing new circuits due to its different port relations. It can easily be designed by making a slight modification to the CFOA with the addition of only a few transistors to obtain a second input for current differencing. The second advantage of the ideal CDBA is insensitivity to parasitic input capacitances and input resistances due to the internally grounded input terminals.

After the controlled current conveyor (Fabre, *et al*., 1996) is introduced in the literature, a new period has been opened with respect to electronic tunability in the analog design. The parasitic X-input resistance of the CCCII is controlled with an external current. In this way not only electronic tunability but also reduction in the number of resistors can be achieved. Also, Maheshwari and Khan adapted the controllability of parasitic resistance to the CDBA with a BJT based implementation (C-CDBA) (Maheshwari and Khan, 2004). The resistors in series with the N and P terminals can be replaced by tunable parasitic resistances of the C-CDBA.

In this section, a CMOS implementation of C-CDBA is presented based on BJT implementation of the (Maheshwari and Khan, 2004). Also, the tunability and cascadability advantages of the C-CDBA are emphasized with a novel first order all-pass circuit.

In the literature, some tunable first-order VM all-pass filters were proposed (Toker and Ozoguz, 2003; Horng, 2006a; Minaei and Cicekoglu, 2006). The circuit in (Toker and Ozoguz, 2003) provides tunability with a single active element, but this circuit is not cascadable since it does not have a high input impedance or low output impedance and hence is not suitable for cascading to realize higher order filters. Also, as stated in (Toker and Ozoguz, 2003), this circuit has the drawback of requiring expensive twin-well process for proper operation. The circuits in (Horng, 2006a; Minaei and Cicekoglu, 2006) include two active elements and two capacitors, so they are not canonical. The presented all-pass construction in this work produces for the first time a VM tunable C-CDBA based all-pass filter, canonical in design. The presented circuit here can be made electronically tunable due to the current controlled parasitic resistance property of the C-CDBA.

3.6.2. The Proposed CMOS Realization and the Controlled CDBA

Current Differencing Buffered Amplifier is a four-terminal active element (Acar and Ozoguz, 1999), where P and N are the input terminals and W and Z are the output terminals. Its symbol is given in Fig. 3.30. The current through the Z terminal follows the difference of the currents through the P terminal and the N terminal, and hence it is named as current output. The P terminal is known as positive (non-inverting) input and the N terminal as negative (inverting) input. Moreover, the voltage of the W terminal follows the voltage of the Z terminal. Hence, the W terminal is called voltage output terminal. The terminal relationships of the CDBA can be characterized with the following equations considering non-idealities of the active element,

$$V_P=0 \qquad V_N=0 \qquad I_Z=\alpha_P I_P-\alpha_N I_N \qquad V_W=\pm\beta V_Z \qquad (3.36)$$

where the current gains α_N, α_P and the voltage gain β are ideally equal to one. Here the sign of β defines the type (ICDBA/CDBA). The current convention is such that all currents flow into the device. If the sign of β is equal to 1, this corresponds to classical CDBA. If sign of β is equal to –1, this kind of CDBA is defined as inverting CDBA (ICDBA).

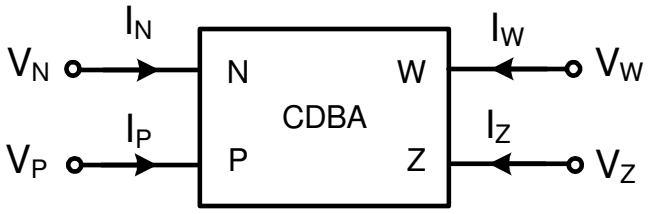


Figure 3.30. The symbol of the CDBA

In Fig. 3.31, a CMOS implementation of the controlled ICDBA/CDBA is presented. The C-CDBA implemented with CMOS technology shown in Fig. 3.31 has exactly the same circuit topology as the BJT implementation in (Maheswari and Khan, 2004). The C-CDBA is based on mixed translinear cells in CMOS CCCII in (Altunbas and Toker, 2002) with the same transistor aspect ratios given in Table 2.2. This active element consists of a differential current controlled current source (DCCCS) followed by an inverting amplifier and a voltage buffer. M_{29} and M_{30} are required to obtain ICDBA. They can be

removed if the classical CDBA is required. Here, M_1-M_4, and M_{18} and M_{19} realize a mixed translinear loop by fixing for both of the N and P terminals at the ground potential. M_5-M_{10} and M_{12} provide biasing for the mixed translinear loops. The M_{11}, M_{13}-M_{19} and M_{20}-M_{21} form a current differencing circuit at the Z terminal for the currents flowing into the N and the P terminals. The transistors M_{24}-M_{28} provide a voltage buffer between Z and W terminals. The transistor aspect ratios of the buffer are $(W/L)_{22\text{-}25}$=0.8μm/0.5μm for M_{22} and M_{25}, $(W/L)_{23\text{-}24}$=4μm/0.5μm for M_{23} and M_{24}, $(W/L)_{26\text{-}27\text{-}28}$=10μm/0.5μm for M_{26}, M_{27} and M_{28} (Ibrahim, 2004).

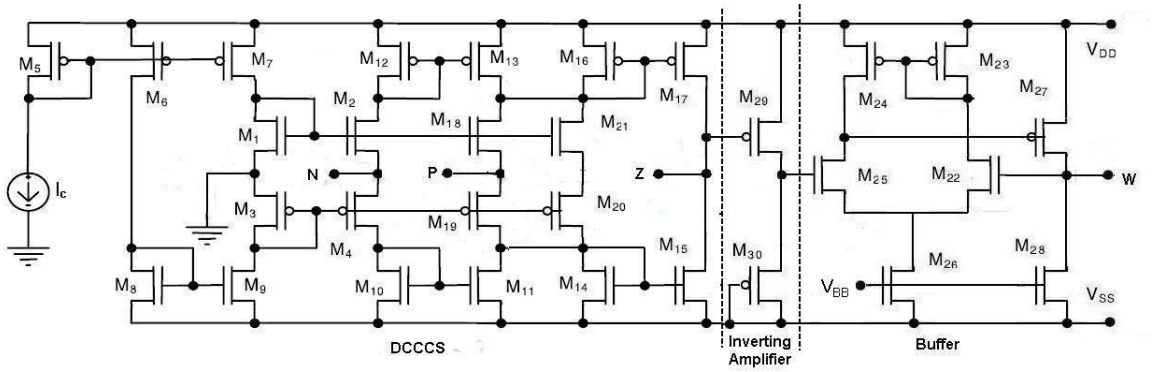


Figure 3.31. The CMOS C-ICDBA implementation (If M_{29} and M_{30} are removed and the Z terminal is connected to the gate of M_{25}, a C-CDBA is obtained)

The calculation of the controlled resistor is described in (Altunbas and Toker, 2002) as follows. The MOS transistors operate in weak inversion (subthreshold region) with the small control currents and for this case the model equations of the MOS transistors are exponential. The current equation can be given as follows,

$$I_D = \frac{W}{L} I_{D0} e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right) \tag{3.37}$$

where n is typically between 1.2 ~ 1.5 and I_{D0} is the drain current at V_{DS} = 0 for W/L = 1. Neglecting the exponential term with V_{DS} in (3.37), the parasitic resistances R_N and R_P can be calculated as follows

$$R_N = R_P = \frac{V_T}{2I_C} \tag{3.38}$$

where $V_T \approx 26\text{mV}$ at 27^{o}C is the thermal voltage. For sufficiently high current values of the I_C (i.e. in strong inversion), and if the MOS transistors operate in saturation region, R_N and R_P resistors in series of the N and P terminals can be calculated as follows,

$$R_N = \frac{1}{g_{m2} + g_{m4}},\ R_P = \frac{1}{g_{m18} + g_{m19}} \tag{3.39}$$

where g_{m2}, g_{m4}, g_{m18} and g_{m19} are the transconductances of M_2, M_4, M_{18}, and M_{19} respectively. They are calculated as follows, $g_{mi} = \sqrt{2\mu_i C_{OX} (W/L)_i I_C}$ $(i = 2,\ 4,\ 18,\ 19)$.

3.6.3. A Tunable All-pass Filter Realization Using C-ICDBA

The proposed circuit is shown in Fig. 3.32. The R_N and R_P and inverting buffer in the circuit of Fig. 3.32(a) can be implemented with current controlled ICDBA (C-ICDBA) and the circuit now becomes as shown in Fig. 3.32(b). Assuming R_N=R_P=R, the transfer function of the all-pass filters can be ideally expressed as follows,

$$\frac{V_0(s)}{V_i(s)} = K\frac{1 - sCR}{1 + sCR} \tag{3.40}$$

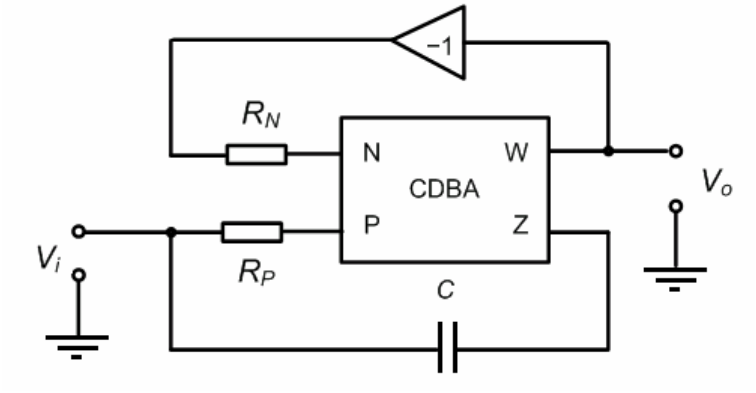
For the circuit in Fig. 3.32(a), K is equal to minus one, i.e. K= –1, and K is equal to one, i.e. K= +1 for the Fig. 3.32(b). Considering non-ideal gains in (3.36) and parasitic resistance R_Z and capacitance C_Z at the Z terminal the ideal transfer function in (3.40) converts to the equation below as follows,

$$\frac{V_0(s)}{V_i(s)} = K\beta\frac{R_Z(\alpha_P - sCR)}{R + R_Z(\alpha_N\beta + sR(C + C_Z))} \tag{3.41}$$

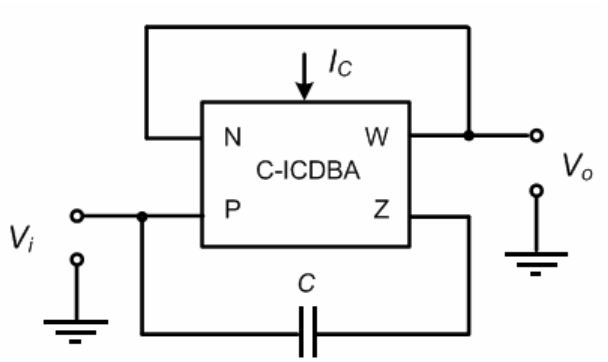
The non-idealities can be fully compensated adjusting the gain β of the inverting buffer stage. The β value can be calculated to achieve an all-pass filter response as follows,

$$\beta = \frac{\alpha_P}{\alpha_N} + \frac{C_Z \alpha_P}{C \alpha_N} - \frac{R}{R_Z \alpha_N} \tag{3.42}$$

The all-pass filter with C-ICDBA has the advantage of using only single passive element and it is a capacitor. Additionally it provides the phase shift tuning through single element as both the R_P and the R_N can be controlled through a single bias current, as they are equal.



(a)



(b)

Figure 3.32. (a) The presented all-pass filter with CDBA (b) The inverting buffer, R_N, and R_P are included in the C-ICDBA for a simpler circuit that provides minimal realization

The parasitic capacitances in the implementation of the current conveyors limit the high frequency of operation. Therefore, the $\beta(s)$ and the $\alpha_N(s)$, $\alpha_P(s)$ are respectively the voltage and current transfer ratios of the C-CDBA that will generally be described by the following first-order functions,

$$\beta(s) = \frac{\beta_0}{1 + s\tau_\beta} \qquad \alpha_N(s) = \frac{\alpha_{N0}}{1 + s\tau_N} \qquad \alpha_P(s) = \frac{\alpha_{P0}}{1 + s\tau_P} \tag{3.43}$$

where the α_{N0}, α_{P0} and β_0 are the value of the current and the voltage transfer ratios at low frequencies and the $\omega_N=1/\tau_N$, the $\omega_P=1/\tau_P$ and the $\omega_\beta=1/\tau_\beta$ represent their corresponding parasitic poles. Combining (3.41) and (3.43) and $R_Z \to \infty$, we obtain,

$$\frac{V_0(s)}{V_i(s)} = K\beta_0 \frac{(1+s\tau_N)(\alpha_{P0} - sCR(1+s\tau_P))}{(\alpha_{N0}\beta_0 + sCR(1+s\tau_N)(1+s\tau_\beta))(1+s\tau_P)} \tag{3.44}$$

Equation (3.43) shows that the effects of these parasitic poles can be ignored in the frequency region of $\omega << \min\{1/\tau_N, 1/\tau_P, 1/\tau_\beta\}$

3.6.4. Simulation and Experimental Results

To verify the theoretical analyses, we simulated the proposed circuit using the presented CMOS C-CDBA in Fig. 3.31, using the SPICE circuit simulation program. The 0.35µ TSMC SPICE parameters are used in the simulations given in Table 2.1. The DC supply voltages are ±2.5V and biasing voltage V_{BB} is –1.7V. In Fig. 3.33, the variation of the R_P and the R_N of the presented C-CDBA with control current is shown. For example, R_P and R_N values of 2.5kΩ, 1.25kΩ, 590Ω and 420Ω are obtained for the control current values of 10µA, 30µA, 100µA and 300µA respectively. In Fig. 3.34, the electronic tunability of the presented all-pass filter in Fig. 3.32(b) is shown for C=100pF. In Fig. 3.35, THD values for various output signal amplitudes at 10kHz are given using C=100pF and R_P=R_N=1.25kΩ (I_C=30µA).

For the experiment, the circuit in Fig. 3.32(a) is realized and the AD844 based model of the CDBA has been adapted as shown in 3.36(a). The circuit in Fig. 3.32(a) is designed with the passive element values R_P=R_N=R=10kΩ and C=100pF to obtain a first-order all-pass filter with a pole frequency of f_0≈159.1kHz. Theoretical and experimental results are depicted in Fig. 3.36(b). Simulation and experimental results agree quite well with the theoretical analysis. Note that the deviations in gain and phase characteristics at high frequencies are also affected from the poles of voltage and current gains as well as from the external terminal parasitics of the active elements. Also, the photograph of the experimental result for Lissajou ellipse at the pole frequency is given in Fig. 3.37.

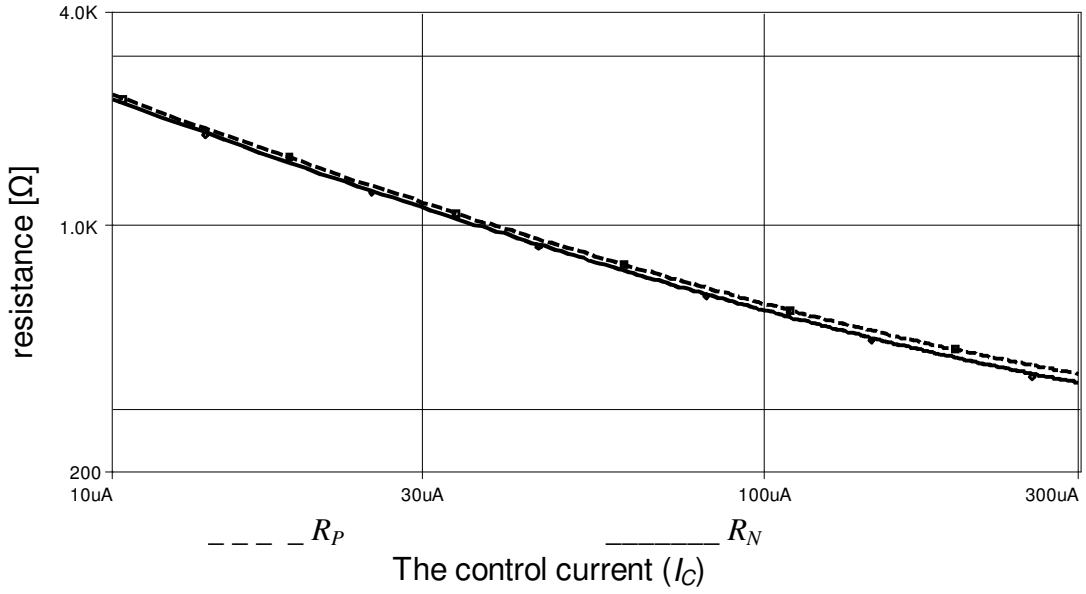


Figure 3.33. The variation of controlled resistor R_P and R_N with bias current

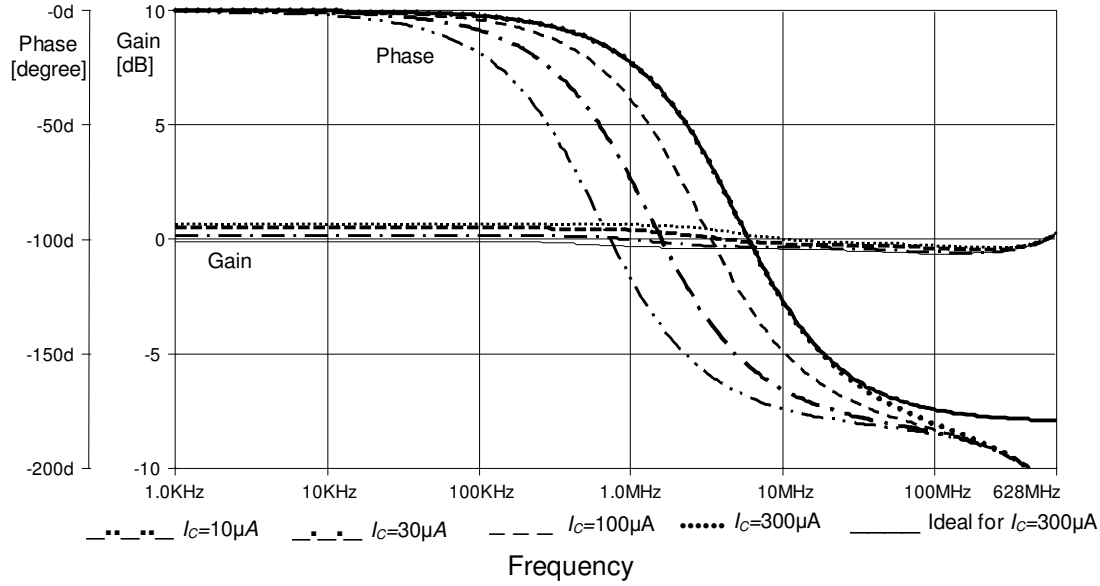


Figure 3.34. Tunability of the presented circuit for various control currents

The presented all-pass filter is used to implement an electronically tunable band-pass filter application as shown in Fig. 3.38. The quality factor of the band-pass filter is determined by R_1 and R_2 that is approximately equal to $Q=R_1/R_2$ (Comer, 1986). In Fig. 3.38, the capacitor and resistor values are chosen as $C_1=C_2=C=100$pF, $R_1=6$kΩ, and $R_2=300$Ω. The buffer in Fig. 3.38 is designed as last two stages of ICDBA implementation in Fig. 3.31. The simulation result is given in Fig. 3.39. The center frequency of the band-pass filter is tuned as 81kHz, 259kHz and 855kHz for the control currents values of 1μA,

3μA, and 7μA respectively. The center frequency of the band-pass filter can be changed in a wide range.

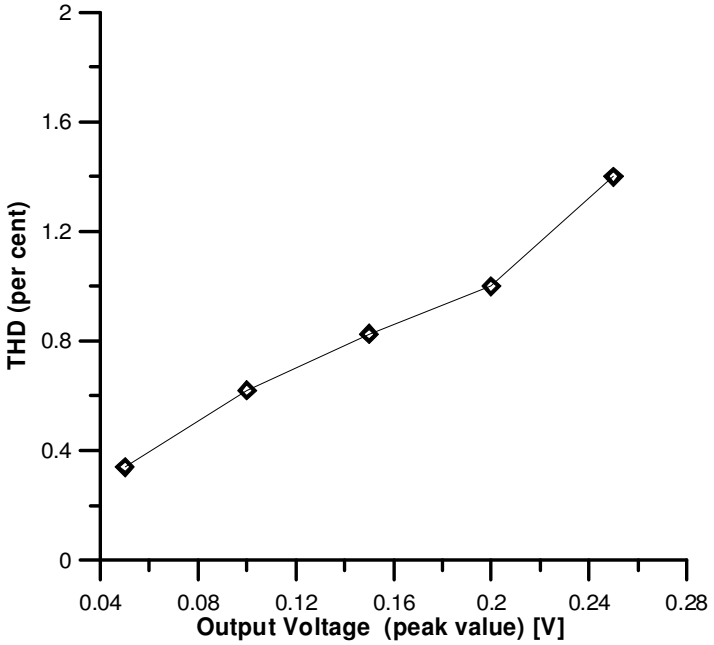
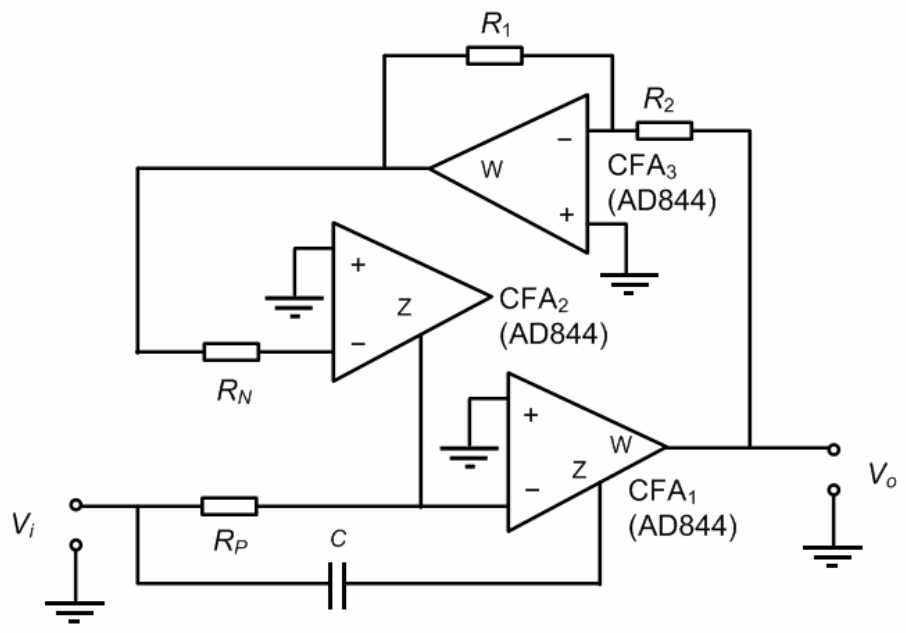


Figure 3.35. THD values for various input signal amplitudes at 10kHz

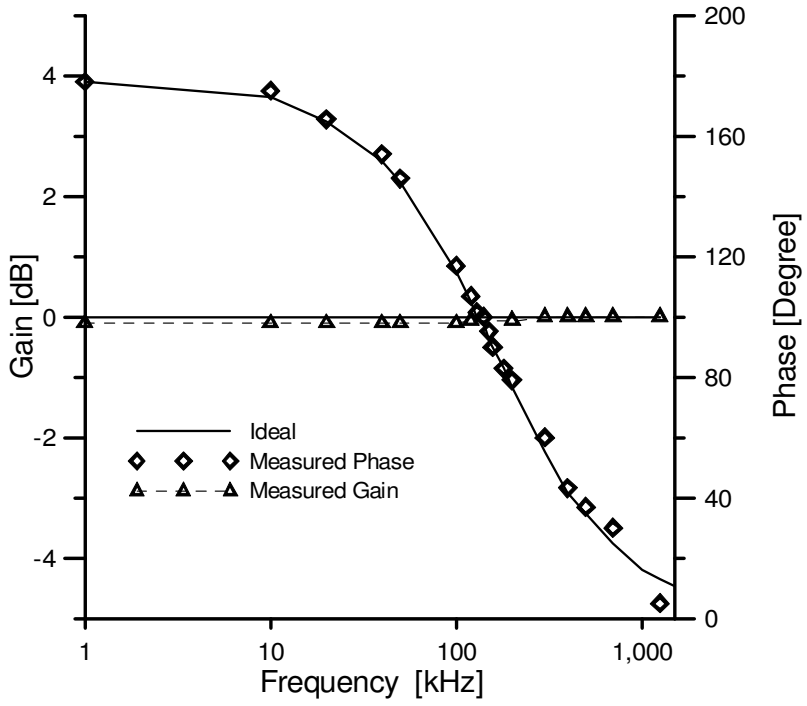
In this section, a novel voltage-mode all-pass filter is also proposed as an application example, which is suitable for high performance analog signal processing. Note that the proposed filter uses a minimum number of passive elements in C-ICDBA based design. Moreover the C-ICDBA based design provides single element tunability. The experimental and simulation results are given to verify the theory.

3.7. Summary

As a summary, in Chapter 3, the mixed translinear loop based tunable active elements such as controlled conveyors and controlled CDBA are examined. Previous studies on the electronically tunable circuits are focused on the current controlled CCII. Possibilities of using other types of current-conveyors have not been examined well. In contrast to trends in the literature, firstly, tunable circuit designs with first generation current-conveyors are examined and compared to the second generation current conveyor based designs, considering high input impedance property, enhanced dynamic range and power consumption due to parasitic compensation.



(a)



(b)

Figure 3.36. (a) Realization of the circuit in Fig. 3.32(a) using current feedback amplifiers (AD844) (b) Experimental and ideal phase and gain responses for the proposed first-order all-pass filter for peak-to-peak 1V sinusoidal input voltage

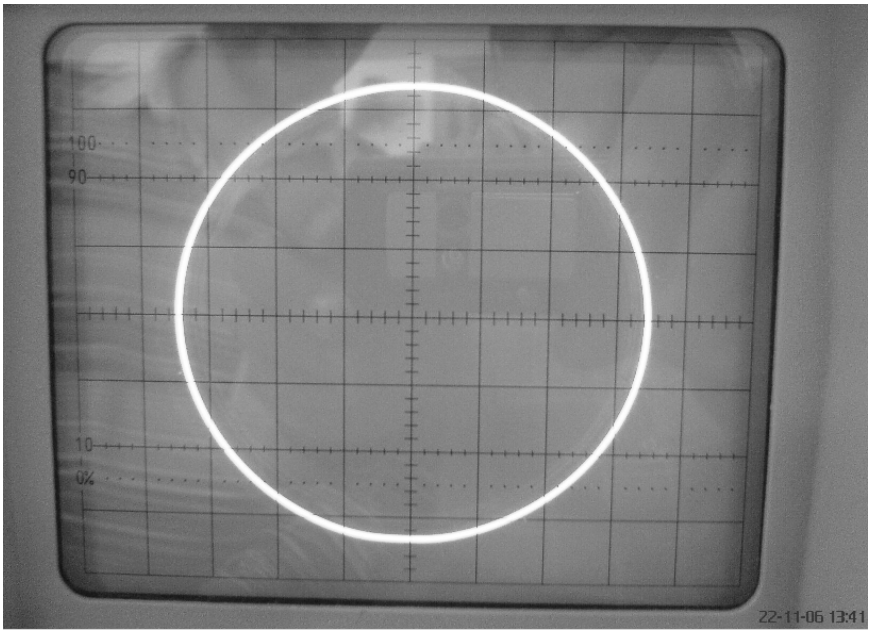


Figure 3.37. The photograph of the experimental result for Lissajou ellipse at the pole frequency (Horizontal and vertical scales are 0.2V/division)

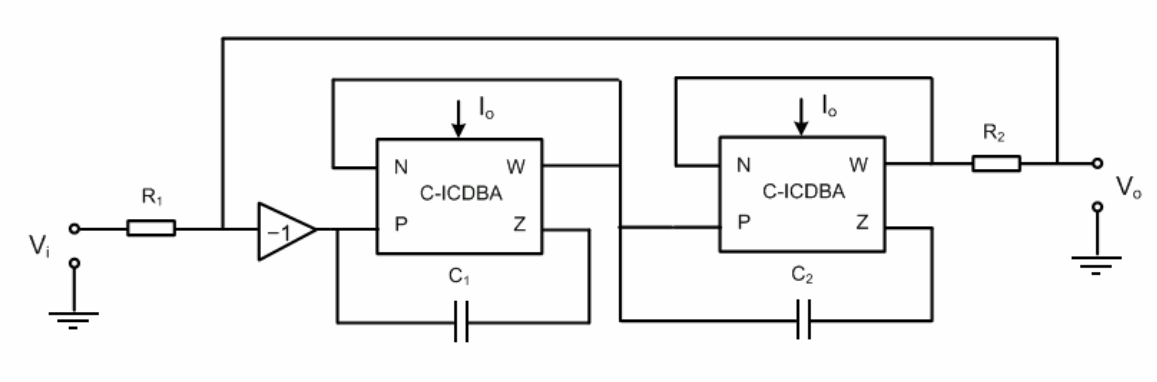


Figure 3.38. Application example: Electronically tunable band-pass filter

Secondly, a relatively new active element based on current conveyor principle, the controlled CDBA is examined. A CMOS C-CDBA implementation is presented. The benefit of the C-CDBA is shown with a novel voltage-mode all-pass filter circuit.

Consequently in this chapter, new opportunities beyond the second generation current conveyors are shown. In the next chapter, the OTA that is another popular active element for the tunability is examined.

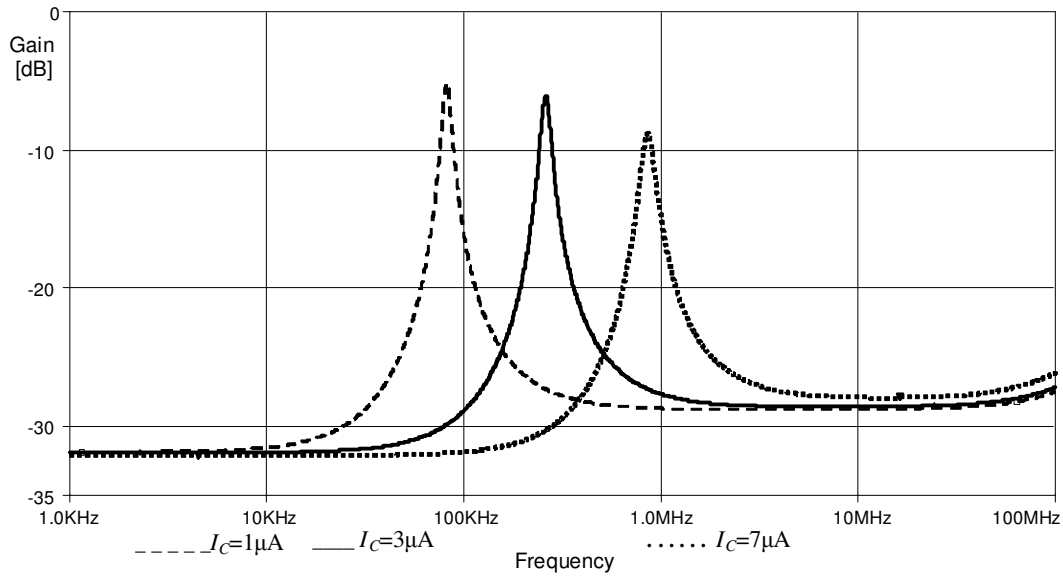


Figure 3.39. Illustrating the tunability of the band-pass filter

4. ELECTRONIC TUNABILITY WITH OTA

The circuits based on the OTA are most suitable from electronic tunability point of view as its transconductance gain can be varied for several decades through its bias current. The OTA is a commercially available and more popular active component than the current conveyor and it has been used widely in many applications. Furthermore, the OTA (or dual output OTA) with a grounded input terminal can replace the CCCII with a grounded X terminal or Y terminal.

The resistor in analog circuit design is not an unavoidable element as the capacitor is. The OTA defines a relation between the voltage and the current; therefore it can easily replace the resistor while simultaneously permitting gain in the circuit. Using transconductance of OTAs instead of fixed value passive IC resistors permits tunability for certain circuit parameters in an IC filter, an unavoidable property due to the high manufacturing tolerances. The well-known high frequency performance advantages of the OTA resulted in a large accumulation of analog filters and they are easily accessible in books.

Basically an OTA is a differential voltage controlled current source (DVCCS) with a tunable transconductance gain. The OTA has performance features and versatility similar to that of an op-amp and in addition, it provides electronic tunability of its transconductance gain. The OTA in general is a more widely used active element to design a high frequency filter compared to op-amp. The terminal relations of an OTA can be given as

$$I_{out} = g_m (V_P - V_N) \tag{4.1}$$

Here I_{out} is the output current defined as flowing out from the OTA. V_P and V_N are inputs and g_m is the tunable transconductance gain.

It is well known that the g_m of the OTA is a frequency-dependent parameter and can be expressed with one-pole model as shown below (Peterson *et al.,* 1987);

$$g_m(s) = \frac{g_{m0}}{1 + \frac{s}{\omega_p}} \tag{4.2}$$

where g_{m0} is the zero-frequency transconductance gain and ω_p is the parasitic pole frequency.

In the first section of this chapter, the OTA is discussed for its electronic tunability by giving a new current-mode first order all-pass filter. Then, it is compared with other OTA based all-pass filters. In the literature OTA based lossy and lossles integrator blocks and filters design using these blocks have emphasized well. However, beside phase equalization, first order filters can be used in the design of quadrature oscillator (Ahmet *et al*., 1997; Horng, 2005; Horng *et al*., 2006) and biquad filter design (Comer and McDermid, 1968; Tarmy and Ghausi, 1970; Moschytz, 1970; Comer, 1986; Metin and Cicekoglu, 2003). In the second part of this chapter, OTA-C and OTA-RC biquad filters are comparatively examined. Effects of g_m of the OTA to the tunability and operation of the filter are examined.

4.1. Discussing Some Trade-offs in Analog Filter Design with a New Tunable All-pass Filter Example

In this section, some trade-offs are examined in analog filter design and an OTA-C first-order all-pass section is proposed and compared with some other all-pass filters (Al-Hashimi *et al*., 2000; Khan and Maheshwari, 2000b; Liu *et al.*, 1995). The following trade-offs are discussed:

(i) Grounded or floating capacitor trade-off: A trade-off exists between convenience for IC implementation and high-frequency operation. In contrast to grounded capacitor, the floating capacitors require an IC process with two poly layers. Also a grounded capacitor has less parasitic elements compared to the floating one in the IC implementation. On the other hand, a floating capacitor between the input and the output of the filter or that by-passes a section of the electronic circuit introduces a

feed-forward path, cancels the effect of non-idealities caused by the active element, and therefore prevents roll-off at high frequencies.

(ii) The tunability range and non-idealities trade-off: The electronically tunable circuits attracted increasing attention in the design of analog integrated circuits, because the absolute tolerances of the electronic components can exceed 20 per cent and thus fine-tuning is a must. On the other hand, due to the parasitic capacitances of the active element parasitic poles are created and this modifies the ideal transfer function. Therefore, the non-idealities may decrease the tunability range of the circuit.

(iii) The cascadability and power consumption/chip area trade-off: The easiest approach to decrease power consumption of the analog filters is to reduce the number of active elements. On the other hand, extra active elements can be required for cascading the analog circuit, which increase power consumption and chip area.

4.1.1. The Presented OTA-C First Order All-pass Filter

The proposed circuit is shown in Fig. 4.1. Routine analysis of the proposed circuit gives the current transfer function as,

$$\frac{I_o}{I_i} = \frac{sC - g_m}{sC + g_m} \tag{4.3}$$

Using (4.2) the reanalysis of the circuit yields,

$$\frac{I_o}{I_i} = \frac{s^2C + (sC - g_{m0})\omega_p}{s^2C + (sC + g_{m0})\omega_p} \tag{4.4}$$

From (4.4) it can be seen that due to the limited bandwidth of the g_m of the OTA, a second order filter response is obtained. In order to operate the circuit as a first-order filter the following condition should be satisfied,

$$\omega^2 << \frac{g_{m0}\omega_p}{C} \tag{4.5}$$

The magnitude of the output impedance function depends on parasitic impedance at the output of the OTA. If the parasitic impedances of the two identical output terminals OTA is represented by R_O, the output impedance function of the filter can be calculated as,

$$Z_O \cong \frac{g_m R_O^2 + R_O + sCR_O^2}{1 + 2sCR_O} \tag{4.6}$$

The circuit has an equivalent output resistance of $g_m R_O^2 + R_O$ at low frequencies and an equivalent output resistance of $R_O/2$ at high frequencies if parasitic capacitors are ignored.

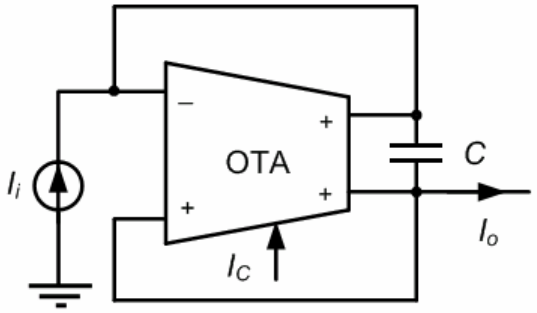


Figure 4.1. The proposed OTA based resistorless all-pass filter

4.1.2. Comparison with Other OTA Based Filters from the Literature

In this section, the circuits in (Al-Hashimi *et al.,* 2000; Khan and Maheshwari, 2000b; Liu *et al.*, 1995) that are interesting examples from the literature performing similar task are reconsidered. They are simulated comparatively in the next section using SPICE. For example, the finite terminal resistances of the active elements directly modify the transfer functions. Moreover, the parasitic capacitances affecting the gain and phase responses at high frequencies, where a single-pole model has been taken for simplicity,

increase the order of the overall transfer function. These non-ideality effects may result unstability for certain passive element values thus limit the tunability range of the circuits. (Stability problems are examined in detail in Chapter 5). These issues are considered and compared with results of the presented circuit in (Al-Hashimi *et al.,* 2000; Khan and Maheshwari, 2000b; Liu *et al.*, 1995). In the comparisons, the OTA internal structures are based on the realization in Fig. 4.2.

4.1.2.1. The OTA Based First-order All-pass Filter in the Literature. The transfer function of the first order all-pass circuit in Fig. 4.3 (Al-Hashimi *et al.,* 2000) can be given as follows,

$$\frac{I_o}{I_i} = -\frac{sC - g_{m2}}{sC + g_{m2}} \tag{4.7}$$

Employing (4.2) in (4.7) with appropriate subscripts, the following transfer function is obtained,

$$\frac{I_o}{I_i} = \frac{s^2C + (sC - g_{m20})\omega_p}{s^2C + (sC + g_{m20})\omega_p} \tag{4.8}$$

where g_{m20} is the zero-frequency transconductance gain of the OTA_2. In order to operate the circuit as a first-order filter the following conditions should be satisfied

$$\omega^2 << \frac{g_{m20}\omega_p}{C} \tag{4.9}$$

Considering the parasitic resistance of the output terminals of the OTAs shown in Fig. 4.3, the output impedance function of the circuit can be calculated as, $Z_O = R_O /2$. When this value is compared to the Z_O of the proposed circuit given by (4.6), it is seen that the proposed circuit provides much higher output impedance at sufficiently low frequencies.

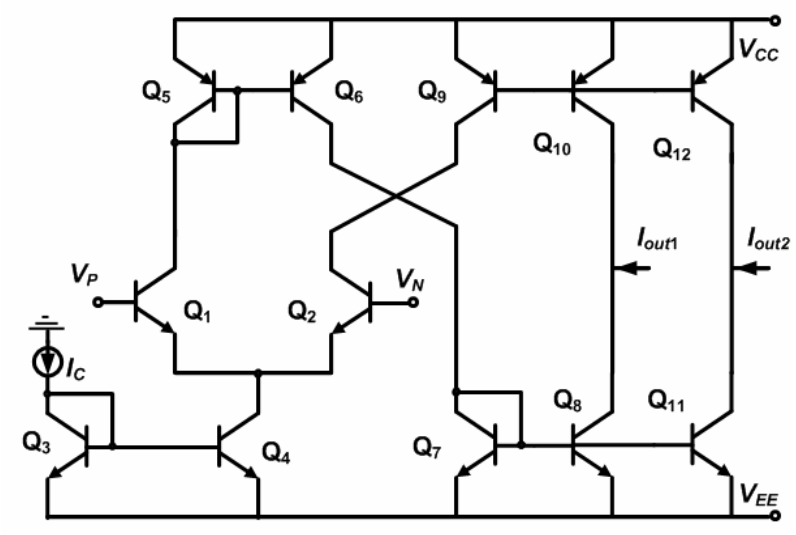


Figure 4.2. A simple bipolar dual output OTA derived from OTA design in (Fabre *et al.*, 1996)

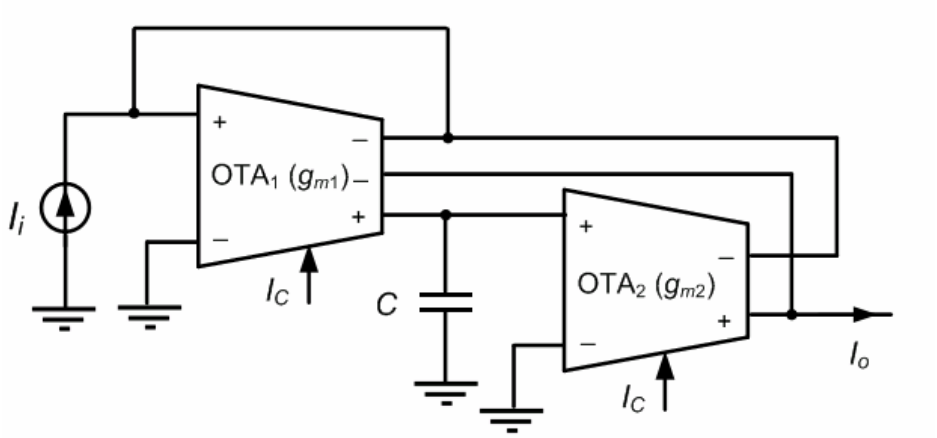


Figure 4.3. OTA based all-pass filter proposed by (Al-Hashimi *et al.*, 2000)

4.1.2.2. The Derived OTA Based All-pass Filter from the Current Conveyor Based Circuits. The OTA can replace current conveyor in some all-pass filter topologies (Khan and Maheshwari, 2000b; Liu *et al.*, 1995). Khan and Maheshwari presented a first order all-pass filter with negative type third generation current conveyor (CCIII–) (Fabre, 1995c) that is suitable for OTA based design (Khan and Maheshwari, 2000b). The CCIII– used in (Khan and Maheshwari, 2000b) can be defined as $V_X = \beta V_Y$, $I_Y = -\gamma I_X$, $I_Z = -\alpha I_X$, where ideally the non-ideal voltage gain β and the non-ideal current gains γ, α are equal to one. The current convention is such that all currents flow into the device. The transfer function of the all-

pass filter in Fig. 4.4 (Khan and Maheshwari, 2000b) can be found as for the ideal case,

$$\frac{I_o}{I_i} = \frac{sCR - 1}{sCR + 1} \tag{4.10}$$

Considering the non-idealities of the active element, the transfer function of the circuit can be found as follows,

$$\frac{I_o}{I_i} = \frac{sCR\ \beta - \alpha}{sCR\ \beta + \gamma} \tag{4.11}$$

In (Liu *et al.*, 1995), an all-pass filter is proposed with a current follower as shown in Fig. 4.5. The current follower is equivalent to a current conveyor with a grounded Y terminal. The terminal relationship of the current follower can be given as $V_X = 0$, $I_Z = \alpha I_X$ considering active element non-idealities. The current convention is such that the currents flow into the device. The transfer function of this circuit is given for the ideal case (α=1) as follows,

$$\frac{I_o}{I_i} = -\frac{sCR\ - 1}{sCR\ + 1} \tag{4.12}$$

The non-ideal transfer function can be given as follows.

$$\frac{I_o}{I_i} = -\frac{sCR\ - \alpha}{sCR\ + 1} \tag{4.13}$$

The OTA based equivalent of all-pass filters in (Khan and Maheshwari, 2000b) and (Liu *et al.*, 1995) is given in Fig. 4.6. The transfer functions of these circuits can be given as follows,

$$\frac{I_o}{I_i} = \frac{sC - g_m}{sC + g_m} \tag{4.14}$$

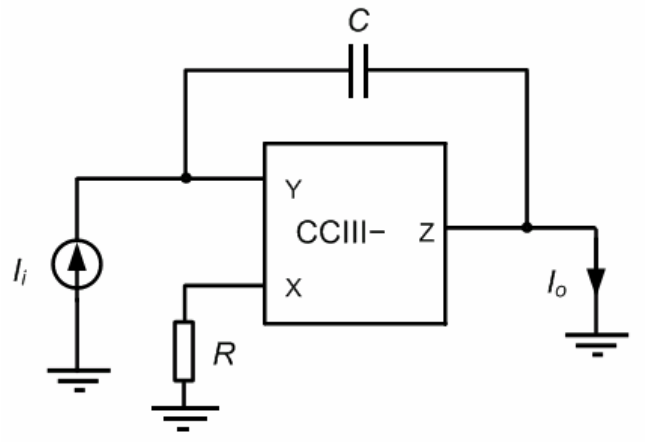


Figure 4.4. All-pass filter circuit in (Khan and Maheshwari, 2000b)

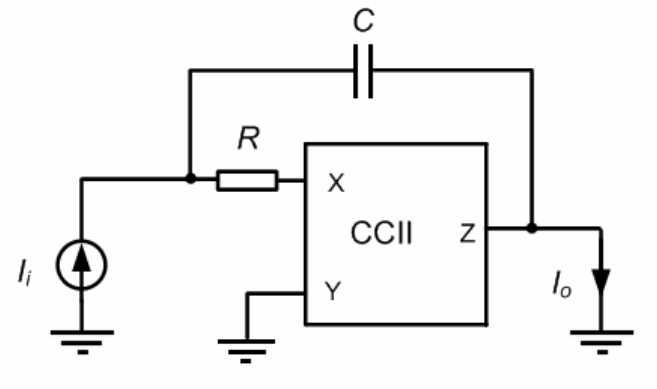


Figure 4.5. All-pass filter circuit in (Liu *et al*., 1995)

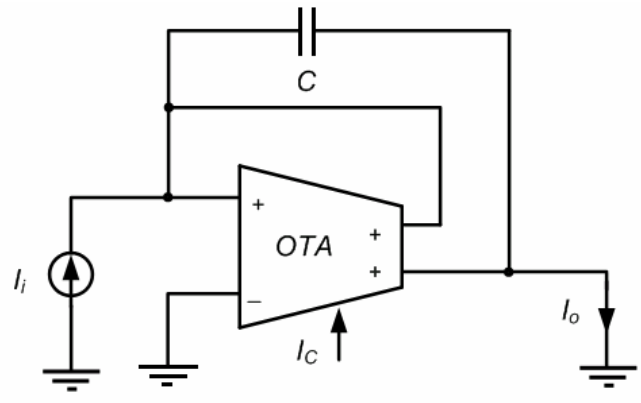


Figure 4.6. OTA based all-pass filter circuit that is equivalent to the current conveyor based designs in (Khan and Maheshwari, 2000b) and (Liu *et al.*, 1995)

4.1.3. Frequency Domain Comparisons

To verify the theoretical analyses, the circuit proposed in Fig. 4.1 is simulated using the SPICE circuit simulation program. The OTAs are simulated using the internal structure shown in Fig. 4.2 (Fabre *et al*., 1996) with supply voltages V_{CC} =2.5V and V_{EE} = −2.5V. The g_m of this OTA is equal to $g_m = I_C/2V_T$, where $V_T \approx$26mV at 27°C is the thermal voltage. The OTA is implemented by using AT&T ALA400 BJT transistors (Frey, 1993). SPICE parameters of the transistors are tabulated in Table 3.1. The capacitor value of C=60pF is employed in the simulations. In order to show the tunability of the presented circuit, the pole frequency of the proposed filter varied between $f_0 \cong$1.3kHz and $f_0 \cong$5MHz for I_C =26μA and I_C =104μA. The SPICE simulation results of the gain and phase responses are depicted in Fig. 4.7.

4.1.3.1. The Frequency Domain Comparison with the Al-Hashimi's OTA based All-pass Filter Circuit. The presented OTA based circuit in Fig. 4.1 is compared with OTA based circuit in Fig. 4.3. In the simulations, dual and triple output OTAs are obtained based on the OTA structure in Fig. 4.2 for the Al-Hashimi's circuit in Fig. 4.3. The phase and the gain responses are depicted in Fig. 4.8 for g_m=0.5mS (I_C=26μA) and C=60pF for a pole frequency of f=1.32MHz. The phase response of the Al-Hashimi's circuit is shifted 180° for a fair comparison with the proposed one. After 10MHz, the magnitude of the gain of the Al-Hashimi's circuit starts rolling off while the proposed circuit provides quite flat phase and gain responses even after hundreds MHz frequency ranges, because the floating capacitor in the presented circuit by-passes a section of the circuit.

4.1.3.2. The Frequency Domain Comparison with Derived OTA All-pass filter from Current Conveyor Based Circuits. The proposed circuit in Fig 4.1 is compared with OTA based implementation of (Khan and Maheshwari, 2000b) and (Liu *et al*., 1995) in Fig. 4.6. In Fig. 4.9, frequency responses are compared for C=60pF and g_m=0.5mS (I_C=26μA) for a pole frequency of f_0=1.32MHz.

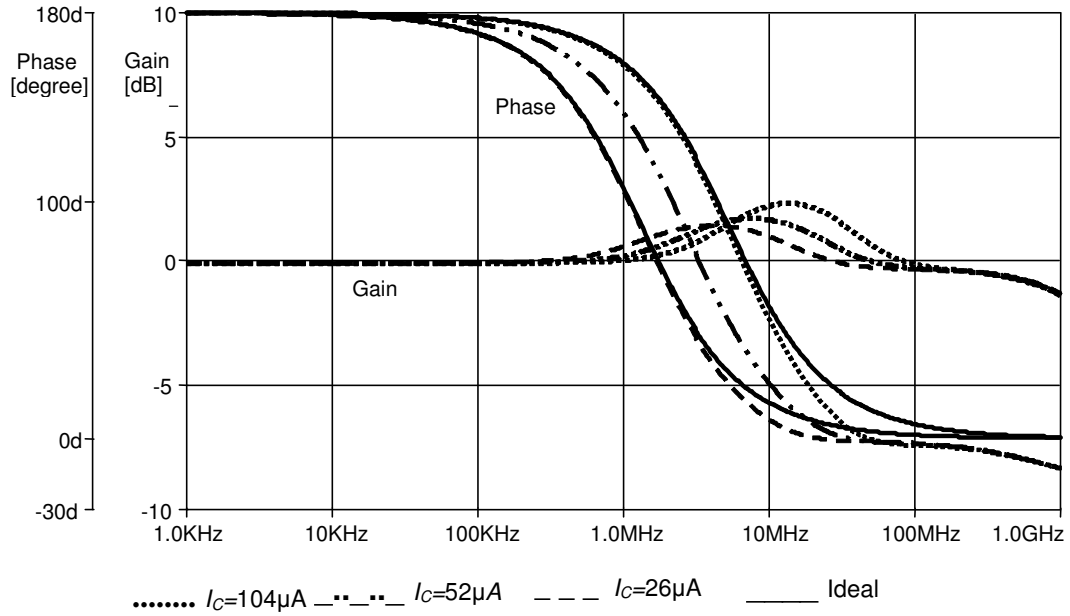


Figure 4.7. Illustrating tunability of the proposed circuit varying its pole frequency between f_0≅195kHz and f_0≅1.5MHz with control current

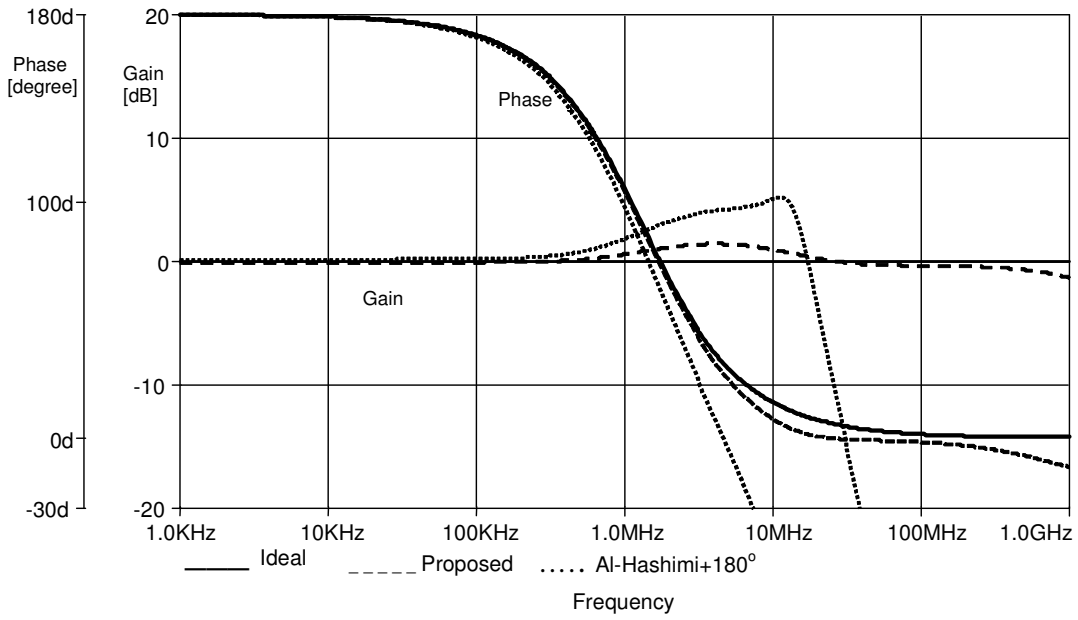


Figure 4.8. The phase and gain response comparison with the Al-Hashimi's circuit (The phase response of Al-Hashimi's circuit is shifted by 180^o for comparison with the proposed circuit)

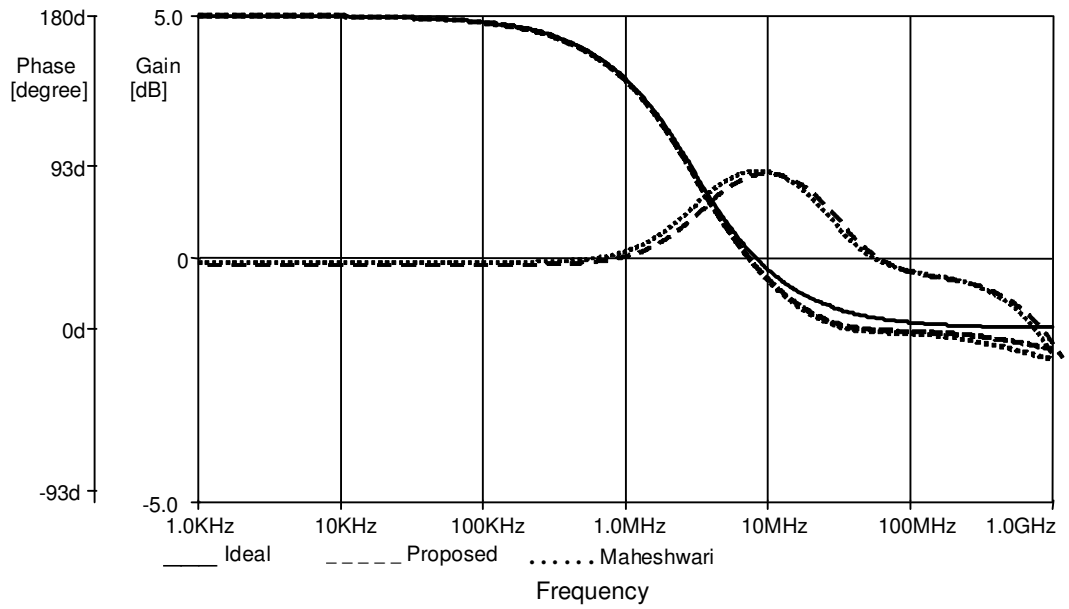


Figure 4.9. The phase and gain response comparisons with the circuit derived from (Khan and Maheshwari, 2000b) and (Liu *et al*., 1995)

4.1.4. Linearity Comparisons

To illustrate the time domain performance, THD analyses are performed using SPICE for low and high frequencies. The filters are constructed with capacitor value of 60pF and control current of 52μA. The THD values for linearity comparison for various input amplitudes at 20kHz are given in Fig. 4.10. Figure 4.10 shows that the input signal amplitude of the examined circuits should be chosen sufficiently lower than the control current to obtain better linearity.

4.1.5. The Experimental Verification of the Proposed Circuit

In the experiment, LM13700 from National Semiconductor that includes two OTAs is used to obtain a dual output OTA. The power supply voltages are chosen as ±12V. The transconductance gain of the LM13700 is calculated as g_m=19.2I_C at 27°C. The two OTAs in LM13700 are biased for a transconductance value of 2mS with I_C=105μA. Figure 4.11 shows the experimental results of the phase and the gain responses with C=0.9nF. A sinusoidal input signal peak to peak 100μA is applied to the filter and at the output a 100kΩ resistor is used as a load. Experimental results are close to ideal values.

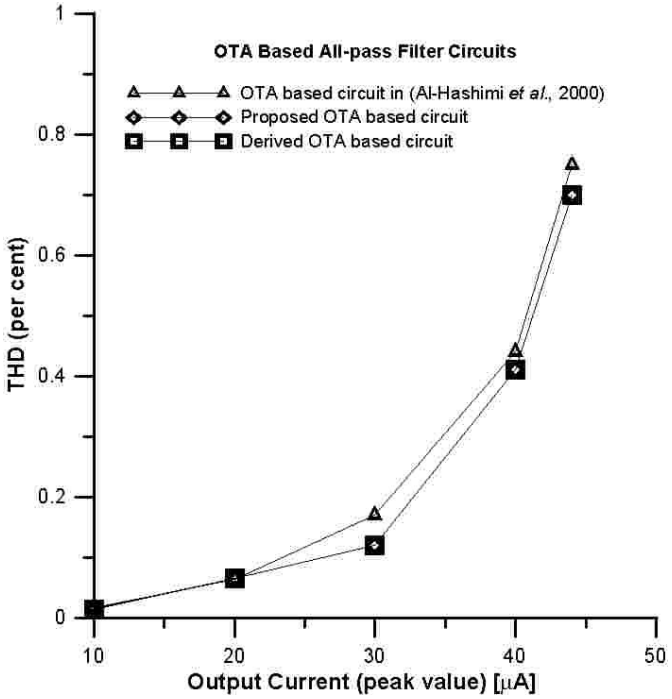


Figure 4.10. THD comparison of output currents with 20kHz sinusoidal input signal when C=60pF and I_C=52μA

4.1.6. Discussions

It seems that the presented circuit can be a good solution for the trade-offs mentioned in the beginning of this section. In contrast to grounded capacitor advantage of (Al-Hashimi *et al*., 2000), the floating capacitor of the presented circuit, which by-passes a section of the circuit and prevents roll-off at high frequencies brings another advantage. The proposed filter is more suitable for high frequency applications than (Al-Hashimi *et al.*, 2000). This floating capacitor can easily be realized with an IC processes that offers two poly layers. The circuit in (Al-Hashimi *et al*., 2000) is cascadable, but it requires two OTAs. Also, the circuits in (Khan and Maheshwari, 2000b; Liu *et al*., 1995), which OTA based equivalents are examined in this thesis, require an extra active element to pickup its output current. In this case, these circuits are expected to require larger chip area and higher power consumption.

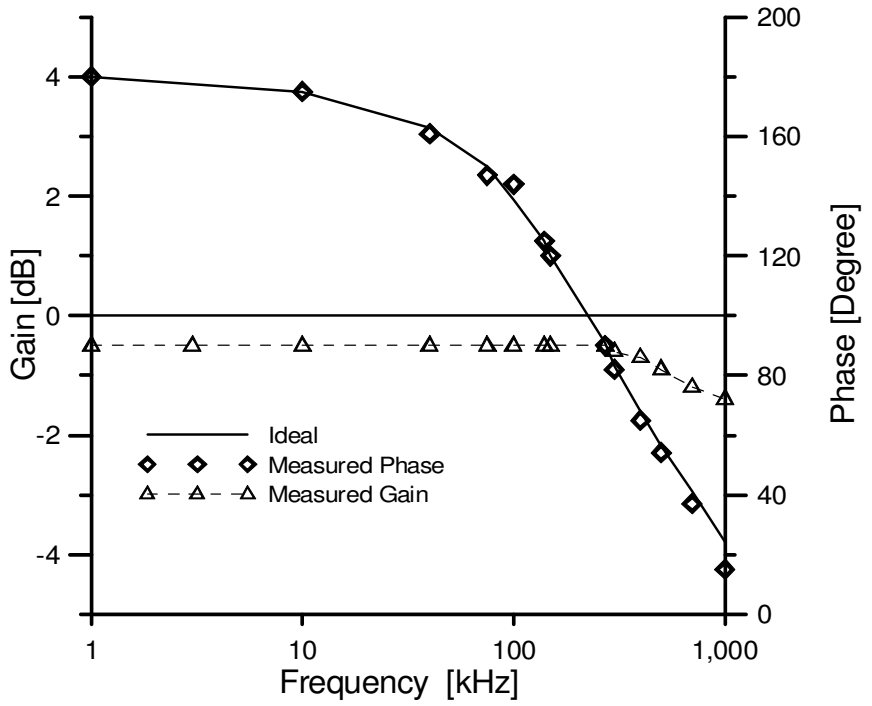


Figure 4.11. Experimental and ideal gain and phase responses of the proposed circuit

As a summary, at high frequencies, the presented circuit has better phase and gain responses compared to Al-Hashimi's OTA based circuit that is an attractive circuit due to grounded capacitor design.

4.2. The Comparison of the OTA-C and OTA-RC Filters for Frequency Limitation and Linearity

In this section, we comparatively examined one OTA-C and one OTA-RC filters with respect to the linearity and the tunability restrictions due to the frequency limitation of the g_m. The frequency limitations of the transconductance of the OTA limits the electronic tunability ranges of the OTA based filters. Furthermore, mixed-mode signal processing capability of the given OTA-RC filter is illustrated. Simulations are performed for both of the OTA-C and OTA-RC based filters to verify the theoretical results.

Mixed-mode or dual-mode circuits have the advantage of working in both voltage-mode and current-mode (Soliman, 1996; Abuelma'atti *et al*., 2004; Abuelma'atti and Bentricia, 2005) and find applications in analog signal processing circuits. A careful

inspection shows that the filter in (Soliman, 1996) is only a current-driven mixed-mode filter. Also, the filters in (Abuelma'atti *et al*., 2004; Abuelma'atti and Bentricia, 2005) can be driven by voltage or current signal, but they use excessive number of passive and active elements.

In this section a modified version of the OTA-RC circuit in (Deliyannis *et al*., 1999) is investigated in detail and it is compared with an OTA-C based filter reported in (Urbas and Osiowski, 1982). It is shown that the OTA-RC circuit in (Deliyannis *et al*., 1999) can also work as a mixed mode filter. SPICE simulations are performed for the circuits in (Urbas and Osiowski, 1982) and (Deliyannis *et al*., 1999).

4.2.1. Effects of Frequency Limitation of the g_m on Tunability

The mixed-mode version of the OTA-RC circuit in (Deliyannis *et al*., 1999) is shown in Fig. 4.12. Routine analysis of the circuit gives the output current and voltage as,

$$V_o = \frac{g_m V_i + I_i}{D(s)} \tag{4.15}$$

$$I_o = g_m \frac{-I_i + s(C_1 + C_2)V_i + s^2 C_1 C_2 R_1 V_i}{D(s)} \tag{4.16}$$

where,

$$D(s) = g_m + s(C_1 + C_2) + s^2 C_1 C_2 R_1 \tag{4.17}$$

Specialization of the numerator in (4.15) and (4.16) gives the following various filter functions:

(i) Selecting I_i=0 results in the following voltage-mode low-pass filter response

$$\frac{V_o}{V_i} = \frac{g_m}{g_m + s(C_1 + C_2) + s^2 C_1 C_2 R_1} \tag{4.18}$$

(ii) Selecting V_i=0 results in the following trans-impedance-mode and current-mode low-pass filter responses,

$$\frac{V_o}{I_i} = \frac{1}{g_m + s(C_1 + C_2) + s^2 C_1 C_2 R_1} \tag{4.19}$$

$$\frac{I_o}{I_i} = \frac{-g_m}{g_m + s(C_1 + C_2) + s^2 C_1 C_2 R_1} \tag{4.20}$$

From (4.17) the angular pole frequency and quality factor of the filter can be found as respectively,

$$\omega_0 = \sqrt{\frac{g_m}{C_1 C_2 R_1}} \tag{4.21}$$

and

$$Q = \frac{\sqrt{g_m C_1 C_2 R_1}}{C_1 + C_2} \tag{4.22}$$

It is seen that pole frequency of the filter circuit can be tuned by changing the g_m.

Considering the frequency-dependent OTA model in (4.2), reanalysis of the OTA-RC circuit in Fig. 4.12 yields,

$$V_o = \frac{g_{m0} V_i + I_i (1 + \frac{s}{\omega_p})}{\hat{D}(s)} \tag{4.23}$$

$$I_o = g_{m0} \frac{-I_i + s(C_1 + C_2) V_i + s^2 C_1 C_2 R_1 V_i}{\hat{D}(s)} \tag{4.24}$$

where,

$$\hat{D}(s) = g_{m0} + s(C_1 + C_2) + s^2(R_1C_1C_2 + \frac{C_1 + C_2}{\omega_p}) + s^3\frac{R_1C_1C_2}{\omega_p} \tag{4.25}$$

From (4.25) it can be seen that due to the limited bandwidth of the transconductance gain of the OTA, a third order filter response is obtained with undesirable terms in their transfer functions. In order to operate the circuit as a second-order filter the following conditions should be satisfied,

$$\omega^2 << \frac{\omega_p(C_1 + C_2)}{R_1C_1C_2} \tag{4.26a}$$

$$R_1 >> \frac{C_1 + C_2}{C_1C_2\omega_p} \tag{4.26b}$$

The OTA-C low-pass filter is shown in Fig. 4.13. The transfer function of this filter can be given as follows,

$$\frac{V_o}{V_i} = \frac{g_{m1}g_{m2}}{g_{m1}g_{m2} + sC_1g_{m2} + s^2C_1C_2} \tag{4.27}$$

In this way, we can compare tunability range of the OTA-RC circuit in Fig. 4.12 with the OTA-C low-pass filter circuit that is shown in Fig. 4.13. Considering frequency-dependent OTA model in (4.2), the transfer function in (4.27) yields,

$$\frac{V_o}{V_i} = \frac{g_{m10}g_{m20}}{g_{m10}g_{m20} + sC_1g_{m20} + s^2(\frac{C_1g_{m20}}{\omega_{p1}} + C_1C_2) + s^3\frac{C_1C_2(\omega_{p1} + \omega_{p2})}{\omega_{p1}\omega_{p2}} + s^4\frac{C_1C_2}{\omega_{p1}\omega_{p2}}} \tag{4.28}$$

In (4.28), ignoring the fourth-order terms, the circuit can operate as ideal case by satisfying the following conditions,

$$g_{m20} << C_2\omega_{p1} \tag{4.29a}$$

$$\omega^2 << \frac{g_{m20}\omega_{p1}\omega_{p2}}{C_2(\omega_{p1}+\omega_{p2})} \tag{4.29b}$$

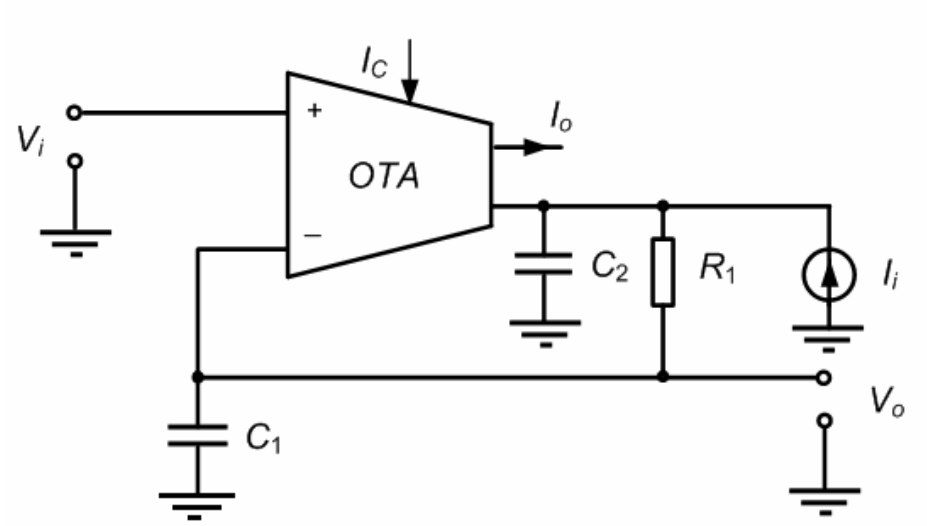


Figure 4.12. The mixed mode OTA-RC low-pass filter based on the filter in (Deliyannis *et al.*, 1999)

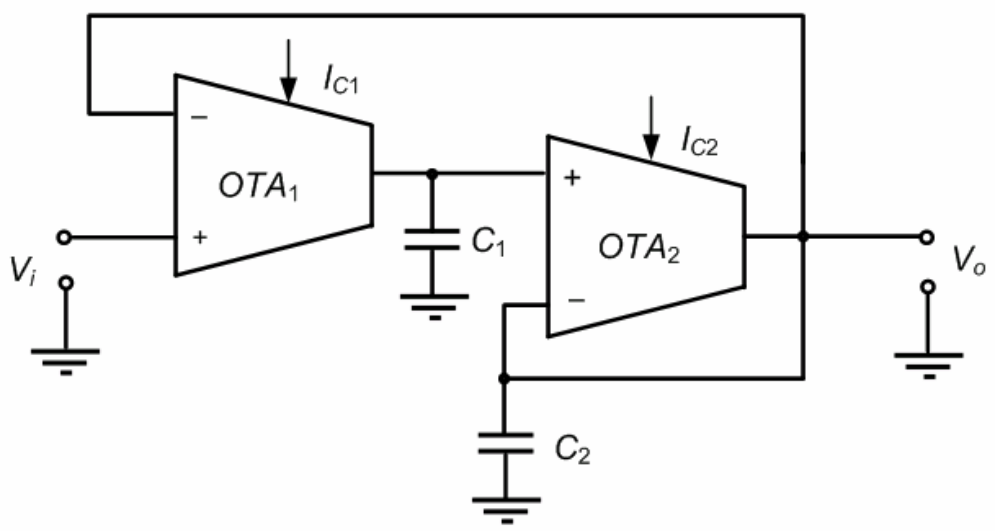


Figure 4.13. The OTA-C low-pass filter (Urbas and Osiowski, 1982)

From (4.26) and (4.29) it can be seen that, while the OTA-RC filter in Fig. 4.12 does not impose any constraint on the transconductance gain of the OTA, the workability of the OTA-C filter in Fig. 4.13 depends on the value of the transconductance gain of the second OTA (g_{m20}). Therefore, in the latter g_{m20} may not be used freely as a tool for tuning the pole frequency or the quality factor of the filter.

4.2.2. Simulation Results

The linearity of the both OTA-RC and OTA-C circuits are examined using the SPICE simulations. The internal structure of the OTA is shown in Fig. 4.14 with supply voltages V_{DD} = 2.5V and V_{SS} = –2.5V. For the simulations, 0.35µm CMOS level 49 real process parameters from TSMC are used. The dimensions of the transistors are $(W/L)_{M1\text{-}M2}$=10.5µm/1.05µm, $(W/L)_{M3\text{-}M4\text{-}M5\text{-}M6}$=4.2µm/1.05µm and others $(W/L)_{M7\text{-}M8\text{-}M9\text{-}M10}$ =12.6µm/1.05µm.

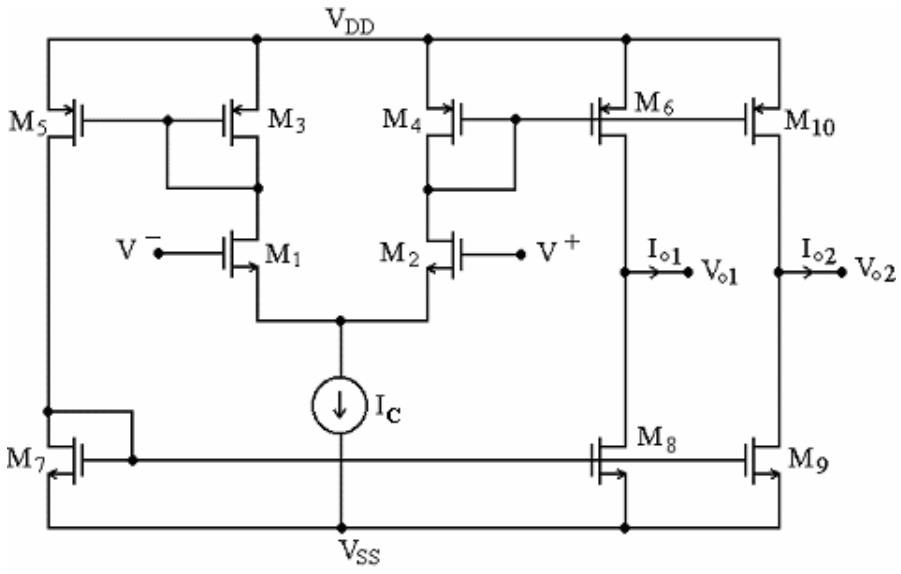


Figure 4.14. A CMOS OTA design

A transient analysis is performed in the SPICE simulation program to evaluate the dynamic range and linearity advantages of the OTA-RC filter over OTA-C filter. For a fair comparison, component values providing the same cut-off frequency and quality factor values for both circuits are chosen. In this way, for the OTA-RC circuit in Fig. 4.12, the component values as selected as R_1=2.5kΩ, C_1=C_2=50pF, I_C =250µA. For OTA-C circuit in Fig. 4.13, the element values are C_1=C_2=105pF, I_{C1}=I_{C2}=250µA to obtain quality factor value of 1 and cut-off frequency value of 3MHz. Sine waveforms with frequencies from f=10kHz to f=450kHz and amplitudes with a peak values of V_p=1.5V are applied to both filters. Total harmonic distortion values are calculated through SPICE simulation program for both of the OTA-RC circuit and the OTA-C circuit as shown in Fig. 4.15. It is observed

that the OTA-RC circuit, which uses a linear resistor instead of active component OTA, has better linearity.

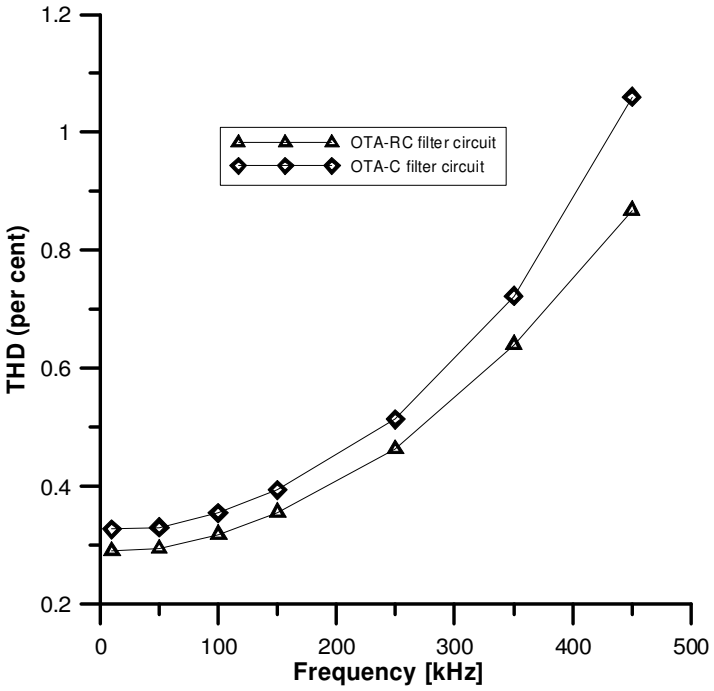


Figure 4.15. Total harmonic distortion of the OTA-C and OTA-RC filter circuits

4.3. Summary

In Section 4.1, a new OTA-C first order all-pass filter is presented. Also, it is compared with some other OTA based filters. Some design trade offs are discussed. In Section 4.2, one OTA-C and one OTA-RC filters are examined with respect to g_m frequency dependency limitations and linearity.

In the preceding three chapters, the control current is used for changing either the parasitic resistance of the translinear loop in Chapter 3 or the g_m of the OTA in Chapter 4. The disadvantage of these methods is to change all biasing conditions of the active device for tuning the control parameter such as R_X or g_m. In the controlled current conveyor and OTA, the corner frequency of the current and transconductance gains at high frequencies naturally depend on biasing currents determining R_X or g_m. Low biasing currents are

required to obtain high R_X value or low g_m value and these decrease the corner frequencies of the gains.

Above mentioned facts cause a difficulty in selecting control currents for high frequency of operation, because the corner frequency of the current and transconductance gains also depend on the control currents. This situation limits the element selection range and may decrease performance in the high frequency of operation.

On the other hand, to overcome these difficulties, the current conveyor can be biased with a constant current providing constant corner frequency for the gains of the current conveyor and its current gain can be adjusted with a small signal current amplifier for electronic tunability. In Chapter 5, electronic tunability with adjusting current gain is examined. The advantages of constant corner frequency feature are especially emphasized for filter stability.

5. ELECTRONIC TUNABILITY ADJUSTING THE CURRENT GAIN

In Chapters 3 and 4, the control current is used for changing either the parasitic resistance or the transconductance gain for electronic tunability. The side-effect in these methods is to change all DC biasing conditions of the OTA and the current conveyor to obtain electronic tunability, since the control current and the biasing currents are the same. Furthermore, the corner frequencies of the active element gains depend on the biasing currents. For example, if the control current is decreased to increase the R_X of the controlled conveyor, bandwidth of the current gain will also be decreased. This may lead to difficulties in selecting control currents for desired operating frequency and in determining element selection range of the filters for stability. On the other hand, to overcome these problems, the current conveyor should be biased with constant currents and its current gain is tuned either using a small signal current amplifier (Surakanpontorn and Kumwachara, 1988; Surakanpontorn and Kumwachara, 1992; Minaei *et al*., 2006) or with current mirror with an adjustable gain (Fabre and Mimeche, 1994; Guvenc, 2006). Therefore "constant bandwidth property" (Carlosena and Moschytz, 1994) is obtained. In this section, it is shown that if the small signal current gain is the major controlling parameter, then better solutions can be offered. In the literature there is an active element called electronically tunable current conveyor (E-CCII) (Surakanpontorn and Kumwachara, 1988; Fabre and Mimeche, 1994), where its current gain can be controlled externally without changing the corner frequency.

In Section 5.1, it is illustrated with simulations how the corner frequency of the gains of both OTA and current conveyor depend on control (biasing) currents. The control currents used for electronic tunability change also the corner frequency of the active element gains. In Section 5.2, the methods of adjusting current gain for electronic tunability are explained. Here, there are two main approaches: current mirror with an adjustable gain or small signal current amplifier. In Section 5.3, using small signal amplifier approach (Surakanpontorn and Kumwachara, 1988; Surakanpontorn and Kumwachara, 1992), a CMOS E-DDCC implementation is given, because DDCC is a more flexible and versatile building block that can replace current conveyor. The DDCC with a grounded resistor at the X terminal, which is denoted as electronically tunable

differential transconductance amplifier (E-DTA) in this thesis, can replace even the OTA due to its differential voltage input. Moreover, the presented E-DDCC is used in an all-pass filter application example. In Section 5.4, equivalent circuits for E-CCII are given using standard current conveyors and electronic resistors. It could be a good idea to implement current adjusting using more than one active element, since E-CCII implementations need more than ten transistors for current adjusting,

In Section 5.5, the advantages of the constant corner frequency property in the evaluation of filter stability are illustrated. Furthermore, a stability test procedure is given that is suitable to determine the stability restrictions of analog filters. In this section firstly, new macro models are proposed for more realistic stability comparison where parasitic components and bandwidth of the OTA and the CCCII depend on the control current. These macro models are considered in the stability tests using Routh-Hurwitz test. Then, the results of these analyses in rough form are reprocessed for their easy interpretation. Therefore, some MATLAB codes are developed so that these complicated stability restrictions can be shown in an interpretable graphical format to guide the application engineer for the optimum or near optimum selection of the filter and element values. These codes help us to find the most suitable biquadratic filters from the still increasing literature for a specific application.

5.1. The Variable Corner Frequency of the Gains of the OTA and the Current Conveyor

In the controlled current conveyor and OTA, the corner frequency of the current and transconductance gains naturally depend on biasing currents determining R_X or g_m. For example, Fig 5.1(a) shows the corner frequency of the g_ms of the OTA in Fig. 4.14 such as 6.6MHz and 333MHz for respectively 2.5μA and 250μA control currents (the dimensions of the transistors are $(W/L)_{M1\text{-}M2}$=6μm/0.5μm, $(W/L)_{M3\text{-}M4\text{-}M5\text{-}M6}$=2.8μm/0.7μm and others $(W/L)_{M7\text{-}M8\text{-}M9\text{-}M10}$ =8.4μm/0.7μm). Also, Fig. 5.1(b) illustrates the corner frequencies of the current gains of the CCCII in Fig. 2.14, such as 43MHz and 315MHz for 2.5μA and 250μA control currents respectively. Low biasing currents are required to obtain high R_X value or low g_m value and they decrease the corner frequencies of the gains.

5.2. Methods of Adjusting the Current Gain

The current conveyor should be biased with constant currents and its current gain is adjusted for electronic tunability either with a small signal current amplifier (Surakanpontorn and Kumwachara, 1988; Surakanpontorn and Kumwachara, 1992) or with current mirror with variable current-gain (Fabre and Mimeche, 1994). As stated before, while biasing current is constant, the input signal is amplified from port X to the port Z. Both approaches are widely used in the literature. For example, in a recent paper a high performance E-CCII is proposed by (Minaei *et al*., 2006). Also, in (Guvenc, 2006) tunable current mirrors are examined detailed.

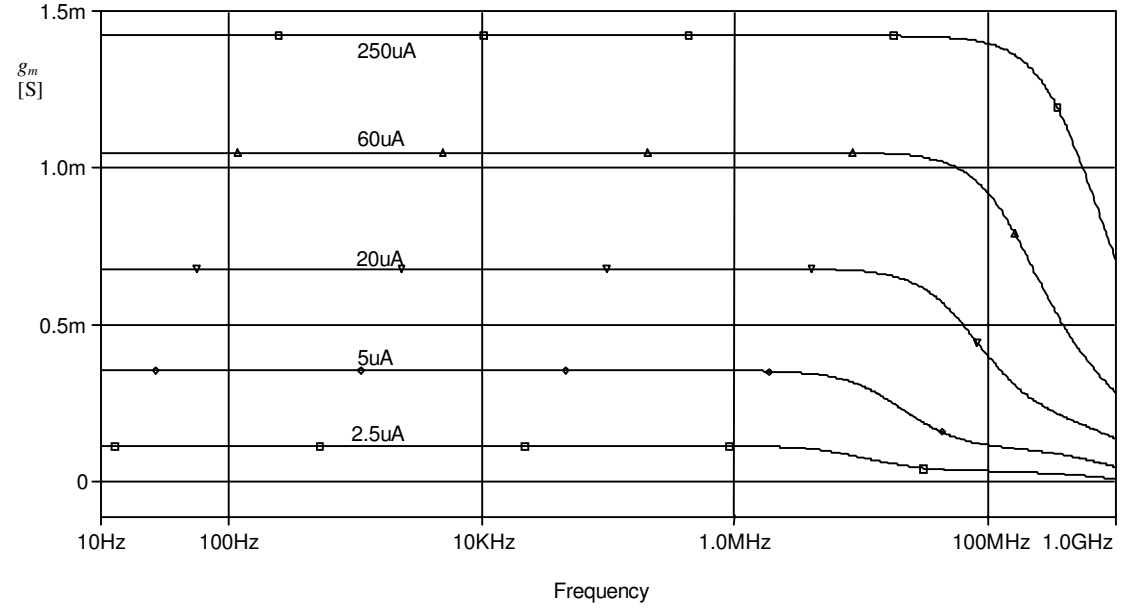
The price is paid for current adjusting is the increase in the number of transistors. Current adjusting requires at least ten additional transistors for the current conveyor.

5.2.1. Current Adjusting with Current Mirror with Variable Gain

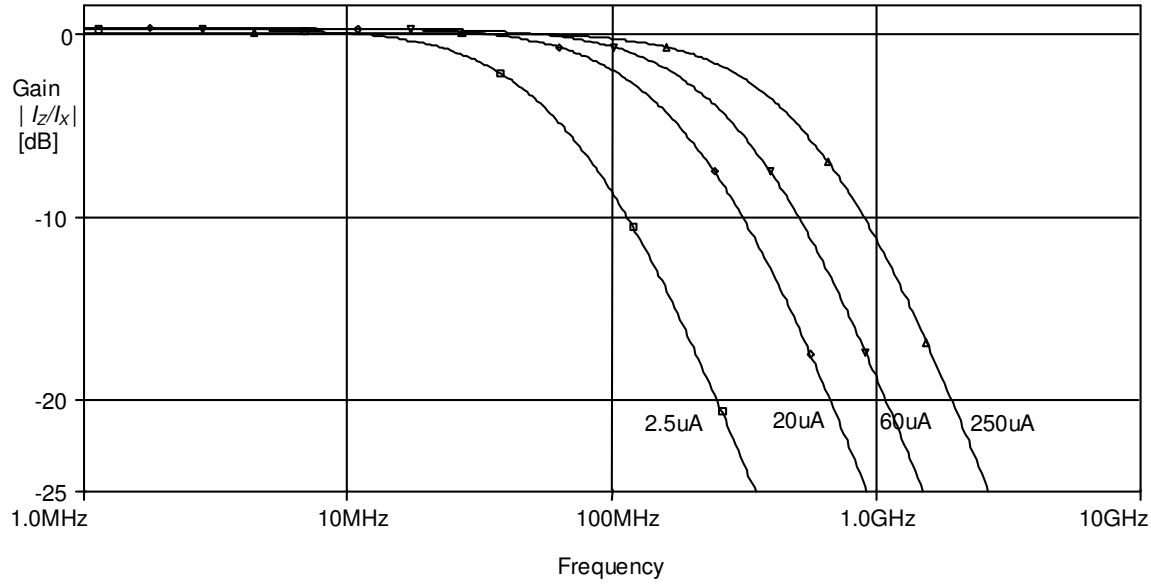
Fabre and Mimeche (1994) presented a BJT based E-CCII implementation using a current mirror with a variable gain. “It uses a mixed translinear loop in input and two complementary current mirrors with adjustable gains to constitute output Z. It works in class A/AB and consequently does not have the above limitations.” (Fabre and Mimeche, 1994). Also, they point out an important advantage of their E-CCII implementation: “The −3dB bandwidth of the current transfer with output short-circuited is 175MHz, for the current gain value of 1. Also note that when the current gain value varies from 0.5 to 5, this bandwidth exhibits low variations. In that case, it always remains higher than 146MHz”.

The E-CCII presented in (Fabre and Mimeche, 1994) employs 12 additional transistors for current mirror with adjustable current gain. Also, Guvenc recently presented four tunable current mirrors suitable for E-CCII design. These designs also require more than ten transistors. However, two of the tunable current mirrors in (Guvenc, 2006) use the linear transition characteristics of the BJT differential pair. Then, these circuits are expected to operate linearly in a wide gain range. Guvenc wrote “According to the simulation results, a gain tuning range of 5 decades for two decades of input range is

achieved with THD below 0.5 per cent". However, this range decreases slightly if a constant corner frequency feature is desired (Guvenc, 2006).



(a)



(b)

Figure 5.1. The relation of the corner frequencies of the transconductance and current gains with the control currents (a) For the OTA (b) For the controlled conveyor

5.2.2. Current Adjusting with a Small Signal Current Amplifier

Surakanpontorn and Kumwachara presented BJT based E-CCII implementation with application examples (Surakanpontorn and Kumwachara, 1988). They observed a constant bandwidth of 30MHz for the current gain values of 1, 3 and 5. Also they presented another E-CCII implementation using CMOS technology (Surakanpontorn and Kumwachara 1992). In the thesis, this CMOS small signal current amplifier is used in the simulations.

5.2.2.1. Description of the Small Signal Current Amplifier. A tunable CMOS small signal current amplifier circuit is shown in Fig. 5.2 presented by (Surakanpontorn and Kumwachara, 1992). Groups of transistors (M_1, M_2, and M_3) and (M'_1, M'_2 and M'_3) function as current squaring circuits, where ports A and B are the input ports. Transistors M_7, M_8, and the current source I_A, form a current-controlled bias circuit, which supplies the bias voltage V_{REF}, to M_3 and M'_3. Let us assume that all the transistors in the circuit are operating in the saturation region characterized by the square-law model of the MOSFET. All the transistors, except M_5, and M'_5 have the same aspect ratio W/L. There are differential input currents, (I_B+i) and (I_B–i), where i is the small signal current, flowing into ports A and B, respectively. Currents I_1 and I_2, can be expressed as (Surakanpontorn and Kumwachara, 1992);

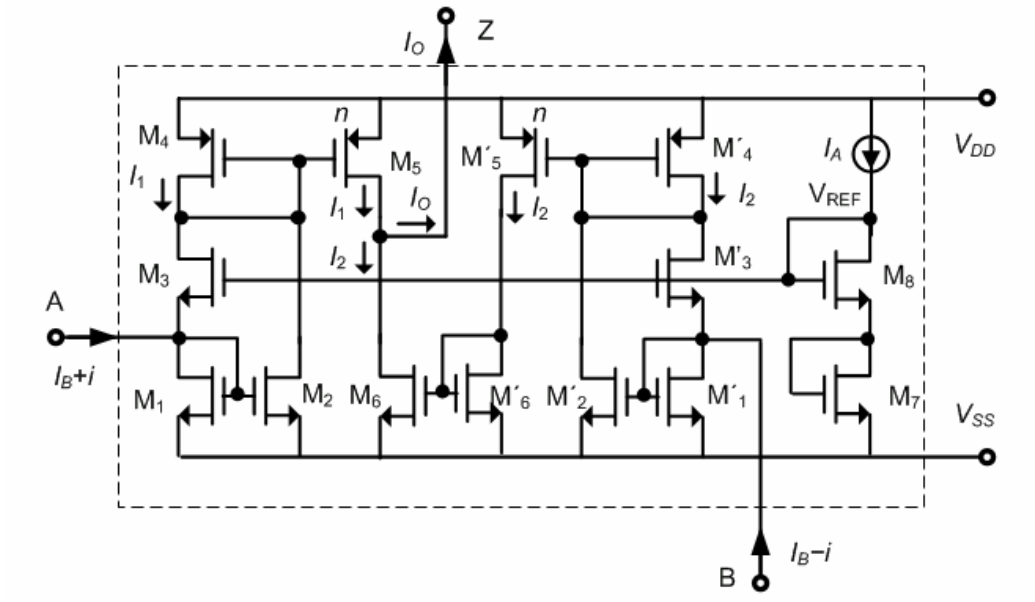


Figure 5.2. Small signal current amplifier (Surakanpontorn and Kumwachara, 1992)

$$I_1 = 2I_A + \frac{(I_B + i)^2}{8I_A} \tag{5.1}$$

$$I_2 = 2I_A + \frac{(I_B - i)^2}{8I_A} \tag{5.2}$$

where, to keep all devices in the on state, the following condition is to be satisfied $|I_B| + |i| < 4I_A$. These currents are multiplied n times by the current mirrors formed by (M_4 and M_5) and (M'_4 and M'_5), where $[(W/L)_{M5} / (W/L)_{M4}] = [(W/L)_{M'5} / (W/L)_{M'4}] = n$. Because M_6 and M'_6 function as a unity gain current mirror, from (5.1) and (5.2), the output current can be written as

$$I_O = n(I_1 - I_2) = \alpha' i = (nI_B/2I_A)i \tag{5.3}$$

We can see that the small signal current is amplified by the factor α' and this factor can be varied electronically. It should be noted that parameter n in (5.3) is introduced to increase the dynamic range of the gain α', because for $n = 1$ the maximum value of the α' is limited at $\alpha'_{max} < 2$, so in this case $\alpha'_{max} \leq 2n$.

5.3. Electronically Tunable DDCC with the Small Signal Current Amplifier

We adapted the controlled current gain principle of the E-CCII to the DDCC, because DDCC is a more general active element that can replace the current conveyor. Furthermore, connecting a grounded resistor in series to the X terminal using its differential Y1 and Y2 ports as the inputs and its Z port as the output, a differential voltage controlled current source is obtained that is equivalent to the OTA as shown in Fig. 5.3. The equivalent E-DDCC circuit for the OTA is denoted as E-DTA in this thesis. Different from the OTA, for the E-DTA, the bandwidth of the g_m does not change with the control current.

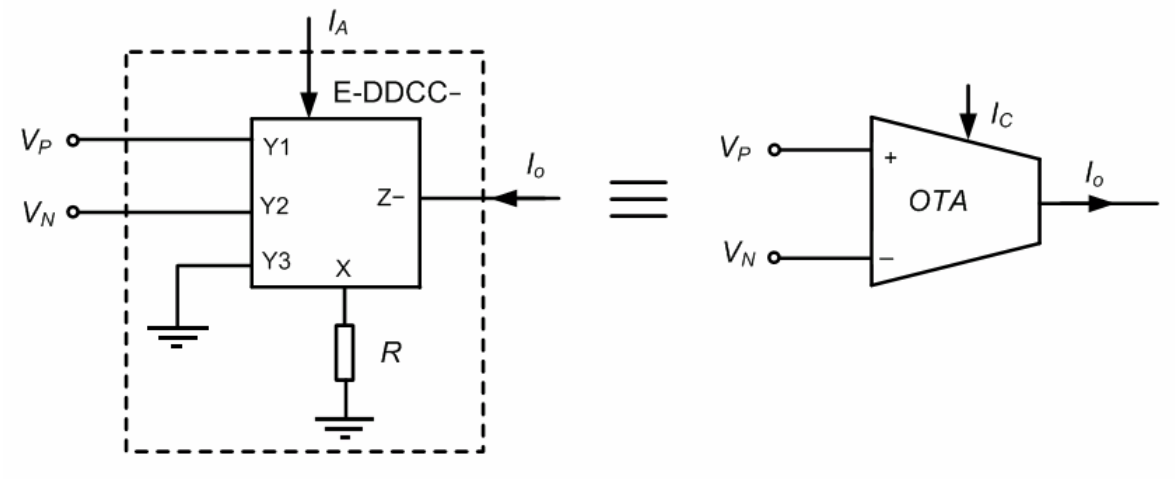


Figure 5.3. The equivalent E-DDCC based circuit for the OTA (E-DTA)

5.3.1. The Presented CMOS Implementation of E-DDCC

The terminal relationship of the E-DDCC can be characterized with the following equations,

$$I_{Y1}=0 \quad I_{Y2}=0 \quad I_{Y3}=0 \quad I_Z=\alpha' I_X \qquad V_X=\beta_1 V_{Y1}-\beta_2 V_{Y2}+\beta_3 V_{Y3} \tag{5.4}$$

where ideally $\beta_1=\beta_2=\beta_3=1$. They represent the voltage transfer ratios of the DDCC. Here, current gain α' is used for electronic tunability.

Figure 5.4 illustrates the complete circuit diagram of the E-DDCC–. Transistor M_5 functions as a current follower stage. If there is a small signal current i flowing out of port X, the current follower will force the drain current of M_5 to be $(I_B + i)$. In the meantime, M_6 will copy the current of M_5, $(I_B + i)$, into node B of the current amplifier, and at the same time, M_{14} will reflect the same current to node C to be input current of the current mirror formed by M_{15}-M_{18}. Owing to drain currents of M_{12} and M_{13}, the drain currents of the transistors M_{15}-M_{16} will be approximately equal to $(I_B + i)$. The usual current mirror M_{15}-M_{18} will reflect the current $(I_B - i)$ to the input port A of the current amplifier. Therefore from (5.4), the output current is equal to $I_Z=\alpha' i$. Because I_Z is in the reverse direction as current I_X then the circuit in Fig. 5.4 realizes E-DDCC–. If the source of the

M_{18} is connected to node B and the source of the M_6 is connected to node A, then an E-DDCC+ can be obtained.

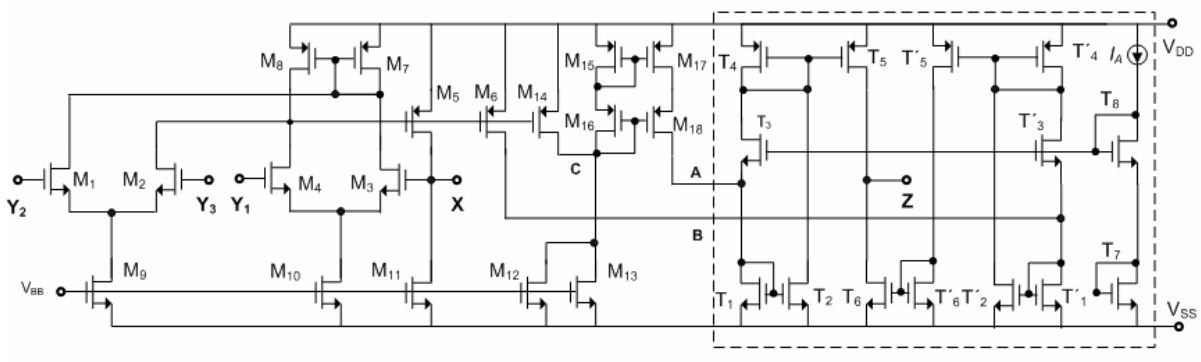


Figure 5.4. The presented CMOS implementation of E-DDCC

5.3.2. The Characteristics of the E-DDCC

To verify the theoretical analyses, the presented E-DDCC in Fig. 5.4 is simulated using the SPICE circuit simulation program. For the simulations, 0.35μm real process parameters from TSMC are used given by Table 2.1. The supply voltages are $V_{DD} = 2.5$V and $V_{SS} = -2.5$V. The biasing voltage is chosen as $V_{BB} = -1.8$V. The aspect ratios of the transistors are given in Table 5.1.

Table 5.1. Transistor aspect ratios of the E-DDCC implementation given in Fig. 5.4

TRANSISTOR	W (μm)	L (μm)	TRANSISTOR	W (μm)	L (μm)
M_1-M_4	1.2	0.7	M_{12}-M_{13}	94.85	0.7
M_5-M_6	21	0.7	M_{14}	84	2.8
M_7-M_8	5.6	0.7	M_{15}-M_{18}	21	0.7
M_9-M_{10}	20.45	0.7	$T´_1$-$T´_4$, T_1-T_4, T_6, $T´_6$	8.4	0.7
M_{11}	86.8	0.7	T_5, $T´_5$	4.2	0.7

In Fig. 5.5, the frequency responses of the current gain (I_Z/I_X) of the E-DDCC are illustrated for different control currents such as I_A=25μA, I_A=75μA, I_A=100μA. In Fig. 5.6, the frequency responses of voltage gain of the E-DDCC such as V_{Y3}/V_X, where Y1 and Y2 terminals are grounded are shown for control currents listed above.

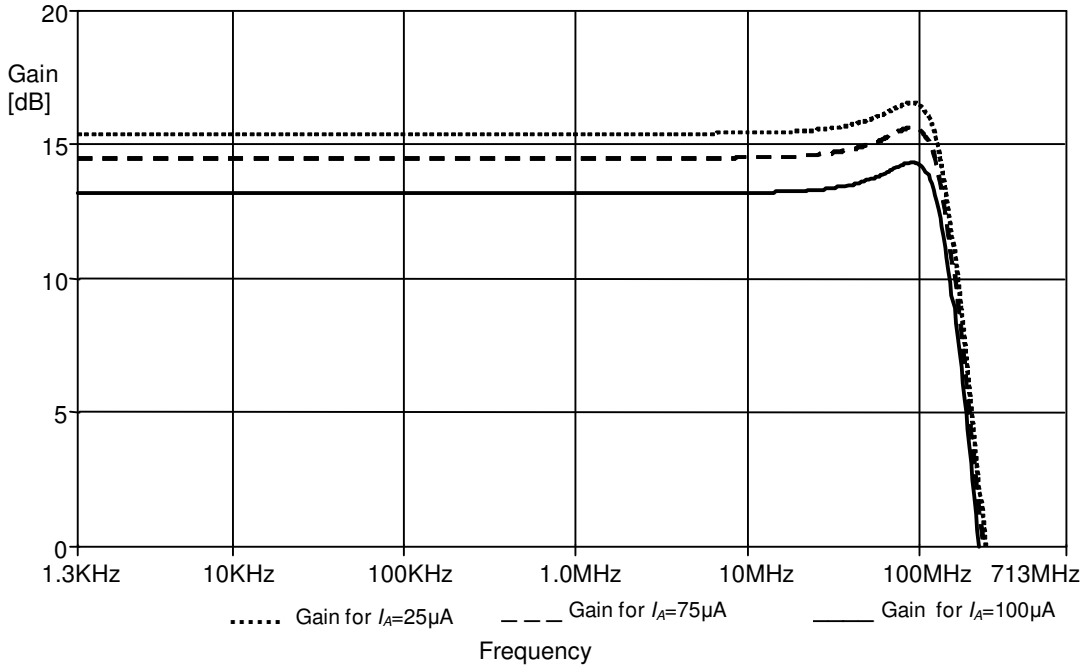


Figure 5.5. The frequency response of the current-gain α'

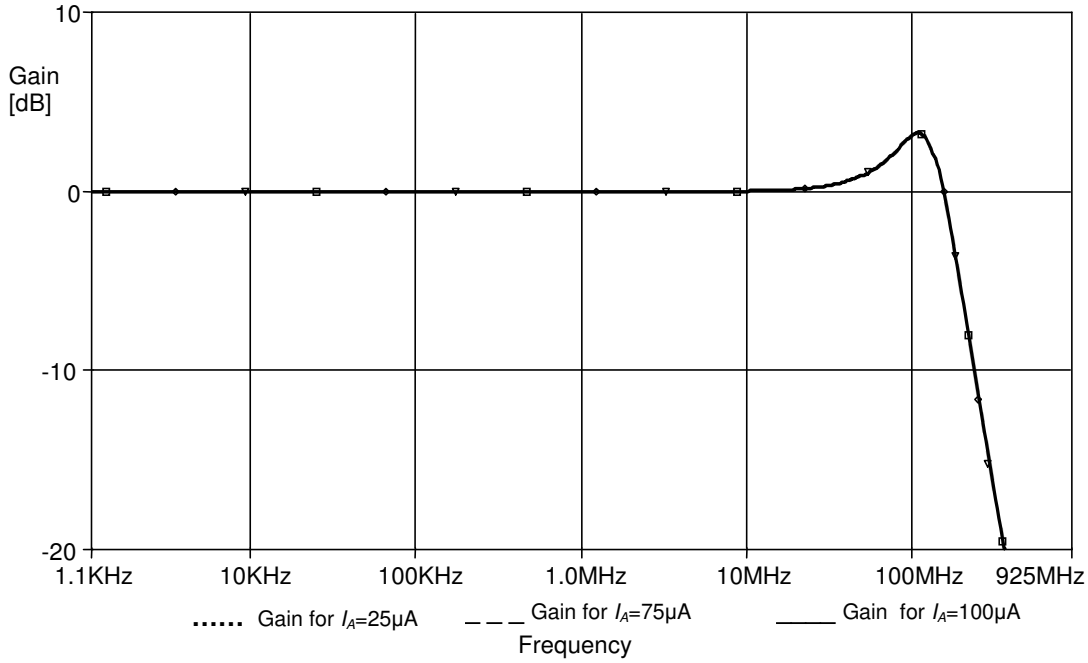


Figure 5.6. The frequency response of the voltage-gain between X and Y3 terminals, where Y1 and Y2 terminals are grounded

These results should be compared with frequency responses in Fig. 5.1. The corner frequency of the current gain is constant for the E-DDCC as shown in Fig. 5.5. However, it

is not constant in Fig. 5.1 and it depends on control current in the OTA and controlled conveyor. These simulation results are consistent with the results in (Surakanpontorn and Kumwachara, 1988; Minaei *et al*., 2006; Fabre and Mimeche, 1994; Guvenc, 2006). Furthermore, Fig. 5.7 shows that electronic tunability of the current gain of the E-DDCC in time domain.

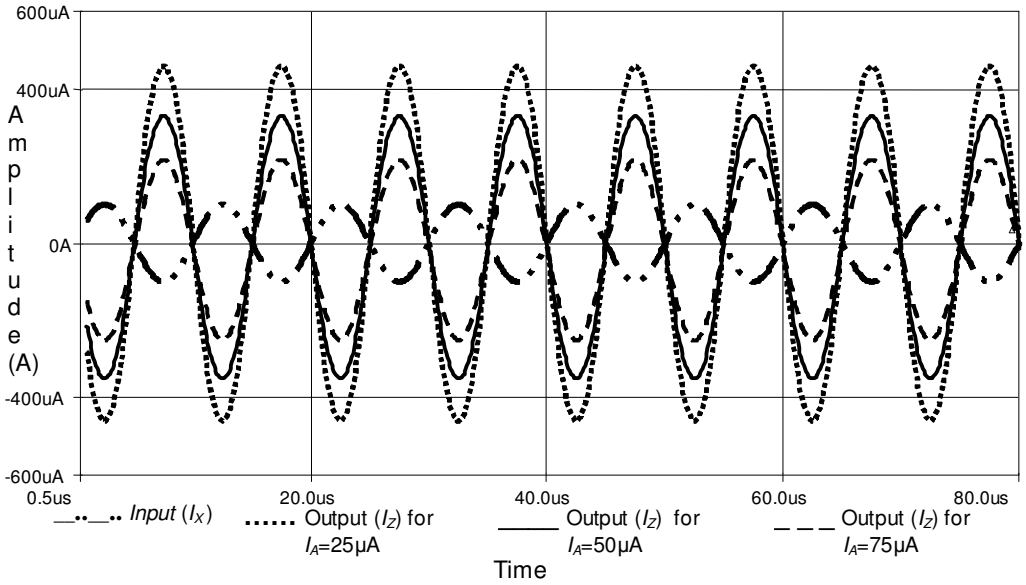


Figure 5.7. The time-domain responses of the current at the terminal Z and X for various control currents

5.3.3. The Tunable All-pass Filter with E-DDCC

In Section 2.3.2, we presented a voltage mode all-pass filter using DDCC. Equation 2.32(a) shows that the current gain α of the DDCC can be used for tuning the pole frequency of the filter. The proposed circuit in Fig. 2.21(a) is adapted to E-DDCC and shown again in Fig. 5.8 for convenience.

SPICE simulations are performed to verify the operation of the filter. The CMOS implementation in Fig. 5.4 is used in the simulations. The passive element values are R=10kΩ and C=50pF. Figure 5.9(a) shows the tunability of the presented circuit in Fig. 5.8 for different control currents.

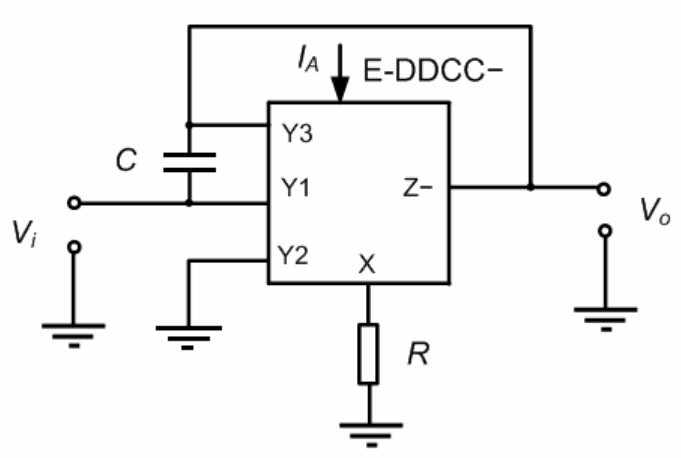
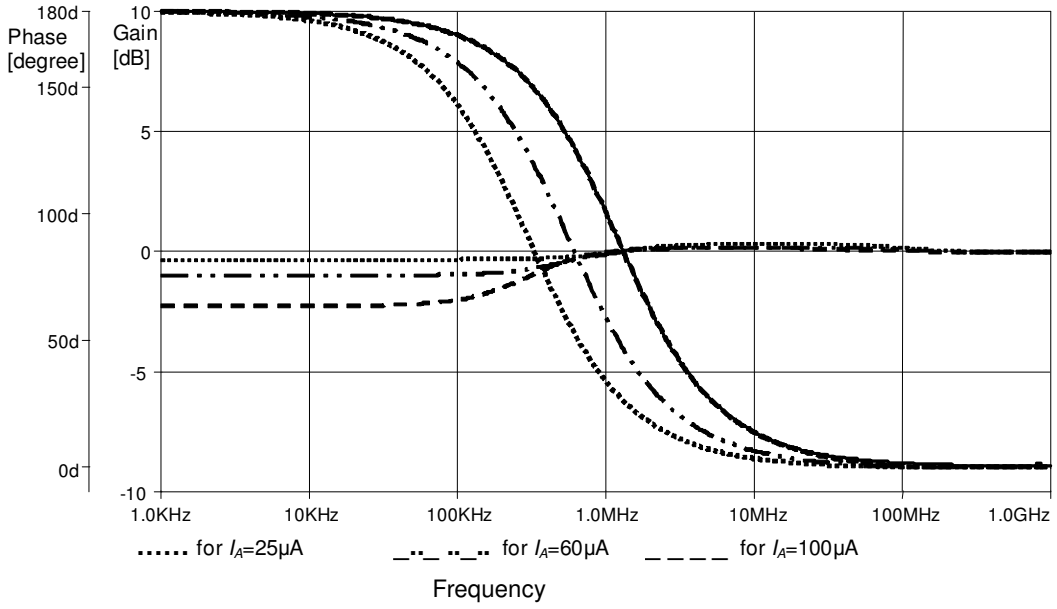


Figure 5.8. The all-pass filter circuit in Fig. 2.21(a) is adapted to the E-DDCC

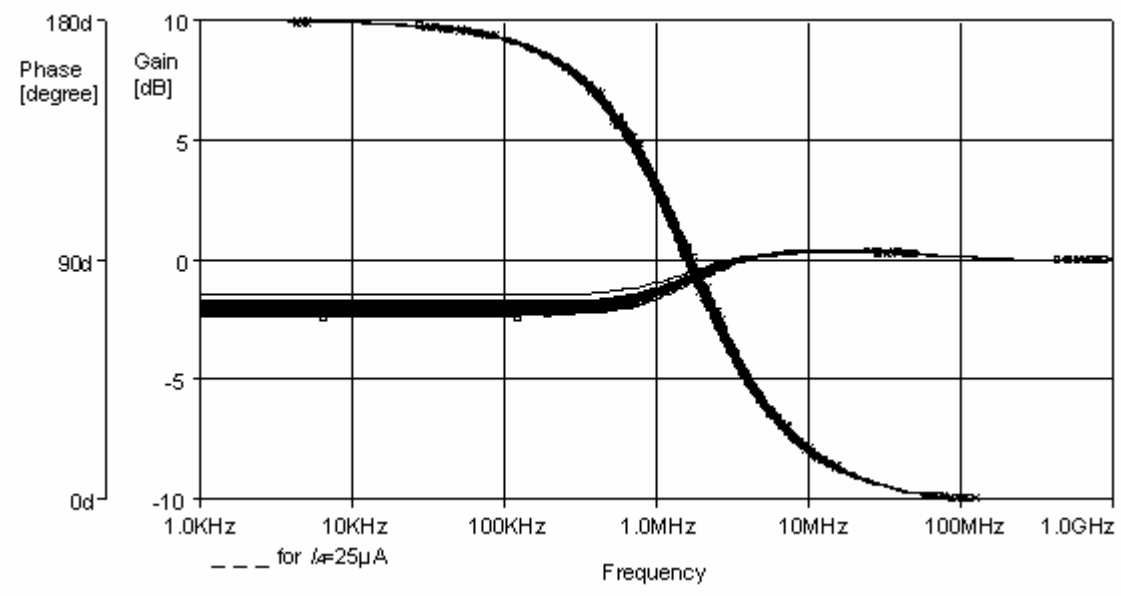
The pole frequency of the proposed all-pass filter is varied between $f_0 \cong 430$kHz and $f_0 \cong 1.5$MHz for $I_A = 25\mu$A, $I_A = 60\mu$A and $I_A = 100\mu$A respectively adjusting the current gain. AC response at high frequencies is close to ideal response due to the feed-forward capacitor in Fig. 5.8. The reason of the decrease in the magnitude of the gain at low frequencies is the finite output resistance of the E-DDCC, which is already examined in Section 2.3.2. Also, Monte-Carlo analyses for the phase and gain responses for 5 per cent uniform change in the transistor sizes are given in Fig. 5.9(b).

5.4. Obtaining E-CCII Using Standard Active Elements

In the literature some examples are given to obtain an E-CCII using classical components. Senani (1980) presents an E-CCII implementation using an op-amp and an OTA as shown in Fig. 5.10(a) but this example does not reflect the philosophy of the current gain adjustment, because of variable corner frequency of g_m of the OTA. Carlosena and Moschytz (1994) presented several possible implementations of variable-gain current conveyors. They can be designed with two op-amps and current mirrors and exhibit constant bandwidth property (Carlosena and Moschytz, 1994). However, using the example equivalent circuits in Fig. 5.10(b) and 5.10(c), it is possible to obtain E-CCII and E-CCII– respectively replacing the grounded resistors with MOSFET based electronic resistors.



(a)

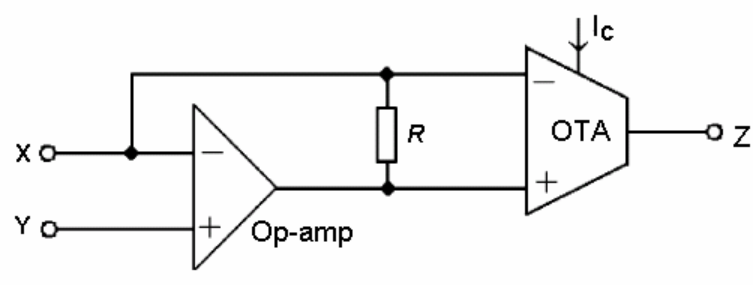


(b)

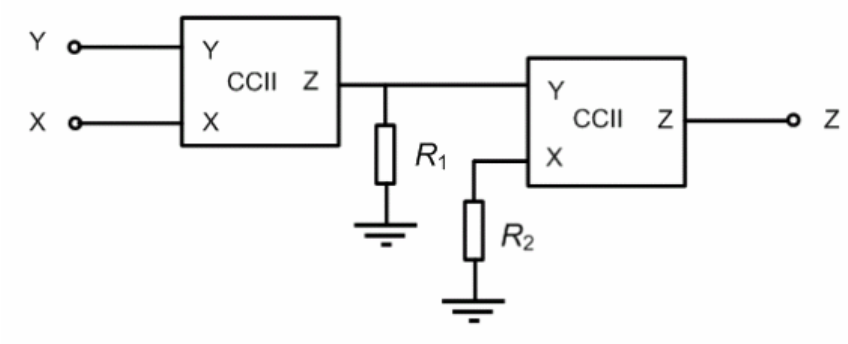
Figure 5.9. (a) Illustrating electronic tunability of the presented all-pass filter circuit (b) Monte-Carlo analysis for the phase and gain responses for 5 per cent uniform change in the transistor sizes

This approach can be acceptable if the number of transistors is taken in to account. The small signal amplifier shown in Fig. 5.2 has 14 transistors that is a sufficient number of transistors to implement a CCII or DDCC. Moreover, if the tunability range of the

current gain is taken into consideration, it is expected to obtain better results tuning MOSFET based resistors.



(a)



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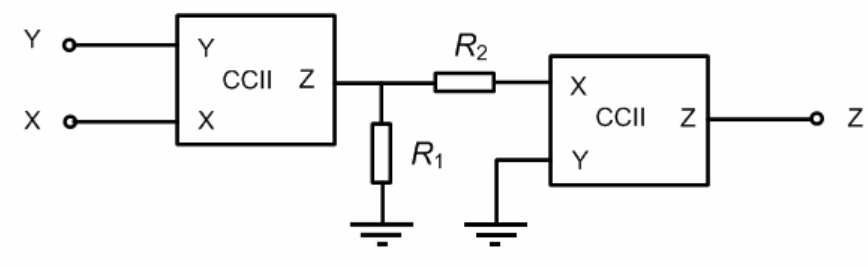


(c)

Figure 5.10. (a) Implementation of E-CCII using the op-amp and OTA by (Senani, 1980) (b) Implementation of E-CCII+ using two CCIIs (c) Implementation of E-CCII– using two CCIIs

5.5. Stability Problems of the Analog Filters

Analog filters can encounter with stability problems. Limited bandwidth of the current and voltage gains affect the stability of the circuits. It should be noted that the corner frequencies of the current and voltage gains of the current conveyor depend on the design and transistor technology used in the realization of the current conveyor. Moreover for the current controlled conveyor and the OTA the corner frequency is not constant and

depends on the control current. However, in E-DDCC the corner frequency is constant. In this section, the advantages of the constant corner frequency property in evaluation of filter stability are illustrated. Furthermore, using the given approach it can be convenient to determine the stability restrictions of analog filters. For example, the parasitic capacitors reduce the magnitude of the gains of the active element at high frequencies. Also, employing a large number of active components in a circuit increases the number of feedback loops and may deteriorate the circuit stability. Consequently, the circuit can be stable for a narrow range of passive elements limiting the tuning range. However, very few works appear in the literature to evaluate the performance degradation due to this stability problem (Aronhime and Dinwiddie, 1991; Cabeza and Carlosena, 1998; Yuce, 2006). Aronhime and Dinwiddie firstly used root-locus analysis to test the stability of an analog filter (Aronhime and Dinwiddie, 1991). Cabeza and Carlosena tested the stability of a very simple CFOA based amplifier considering effects of the parasitic poles (Cabeza and Carlosena, 1998). Yuce shows the relation of stability and filter parameters such as pole frequency and quality factor using one-pole model (Yuce, 2006). The main aim of this section is to point out the effect of variable corner frequency to the stability of the filters and limitations due to stability considerations.

In the section, stability of the OTA, controlled conveyor and E-DDCC based filters are compared. The E-DTA that is an OTA equivalent circuit shown in Fig. 5.3 is compared with the classical OTA and controlled conveyor for an example biquad filter. The tunability limitations due to stability problems are illustrated.

To find stability limitations of the filters root-locus analysis and Routh-Hurwitz criterion are used in the thesis:

- Root-locus analysis is a widely used method to test the stability of the closed loop systems from open loop transfer functions in control engineering. The root-locus method, is one in which the roots of the characteristic equation are plotted for all values of a system parameter. The parameter is usually the gain in a control system (Ogata, 1990). By using root-locus method the designer can predict the effects on the location of the closed loop poles when varying a system parameter.

- The Routh-Hurwitz stability criterion is also used to find necessary (and frequently sufficient) conditions for the stability of a linear time invariant system. Routh-Hurwitz stability criterion tells us whether or not positive roots in a polynomial equation (the denominator for the filters) without actually solving for them (Ogata, 1990). More generally, given a polynomial, some calculations using only the coefficients of that polynomial can lead us to the conditions that it is not stable.

These two methods are widely used and are sufficient in control engineering where usually only the gain is a parameter in a control system. However, for the analog filters, if parasitic and frequency dependent gain parameters of the OTA and CCCII are considered, it is a very difficult task to determine stability limitations of the circuits. Therefore, some software tools are needed to reprocess the results of these stability methods.

In this section firstly, new macro models are proposed for more realistic stability comparison where parasitic components and one-pole models of the OTA and the CCCII depend on the control current. These macro models are used in Routh-Hurwitz stability tests. The conditions obtained by Routh-Hurwitz criterion are firstly given to show their difficulties in determining the stability of analog filters. Then, the results of these analyses in rough form are reprocessed for their easy interpretation. Therefore, some MATLAB codes are developed so that these complicated stability restrictions can be shown in an interpretable graphical format to guide the application engineer for the optimum or near optimum selection of the filter and element values. These codes help us to find the most suitable biquadratic filters from the still increasing literature for a specific application.

5.5.1. The OTA and Current Conveyor Macro Models for Stability Analysis

The OTA and the current conveyor are two widely used active elements used in electronic tunability. In the last decade, the current conveyor has been a more popular active element than the OTA, because it can produce very rich variety of circuit topologies. Also, the controlled current conveyor includes a parasitic inductance in series to the terminal X, which creates extra parasitic pole compared to the OTA.

As shown in Fig. 5.1, the corner frequencies of the voltage and current gains of the controlled current conveyor and the corner frequencies of the transconductance gain of the OTA depend on biasing current I_C. Also, some of the parasitic components of the OTA and CCCII, which are shown in Fig. 5.11, are a function of the I_C such as, the R_Z of the OTA and the R_Z, R_X and L_X of the CCCII in Fig. 5.11. Here, the parasitic terminal resistances R_Zs can be made sufficiently high using cascode-output stage so that their effects can be ignored for simplicity. For the CCCII in Fig. 3.11 and for the OTA in Fig. 4.2 the parasitic output impedances can be calculated as follows,

$$R_Z = \frac{V_{AN}}{I_C} // \frac{V_{AP}}{I_C} \tag{5.5}$$

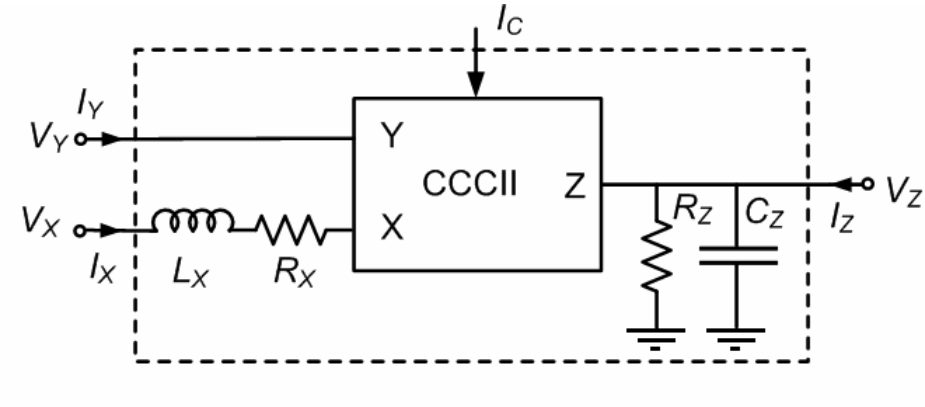
Here, V_{AN} and V_{AP} are the Early voltages of the transistors of the Z terminal of the CCCII and output terminal of the OTA.

As shown in Fig. 5.11(a), also the parasitic elements in series to the terminal X of the CCCII are a function of the control current. The R_X is a function of the control current I_C as given by (3.5) for a BJT based CCCII. The parasitic inductance series to the port X of the CCCII (L_X) is also is a function of the I_C (Bruun, 1995; Fabre and Alami, 1997),

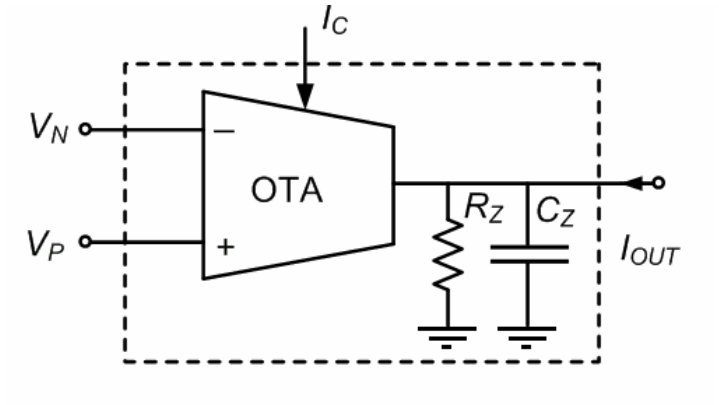
$$L_X = \frac{C_{\pi N} + C_{\pi p}}{g_m^2} = (C_{\pi N} + C_{\pi P}) R_X^2 = (C_{\pi N} + C_{\pi P}) \frac{V_T^2}{I_C^2} \tag{5.6}$$

where, the $C_{\pi N}$ and $C_{\pi P}$ represent the base emitter junction capacitance of respectively the NPN and PNP transistors (Seguin and Fabre, 2001b; Fabre and Alami, 1997).

The values of the current and voltage gains in the terminal relationships of the current conveyors are not constant and serious reductions at high frequencies are observed due to active component non-idealities. In order to model these deviations the one-pole model is in general used.



(a)



(b)

Figure 5.11. The macro models for stability analysis (a) For the CCCII (b) For the OTA

In this model, simple terminal equations are valid up to a cut-off frequency. The one-pole models of the current conveyor and OTA are given in (3.27) and (4.2) respectively. In the macro models in Fig. 5.11, the corner frequency of the OTA and controlled conveyor gains are in form of $\omega_p = g_m / C_{eq}$, where it is given as $\omega_p = g_m / C_Z$ for OTA in (Schaumann *et al.*, 1990) and $\omega_p = g_m / C_\pi$ for a current conveyor in (Ismail and Soliman, 2000), where C_π represents some equivalent parasitic capacitance in the current conveyor as defined in (Ismail and Soliman, 2000). To increase the accuracy of the stability analysis, better models should be used. Including two or more poles in the model increases accuracy of the analyses, but this may not be suitable with respect to computational complexity. The one-pole model can give an idea about stability of the circuits assuming the second parasitic pole is at sufficiently high frequency. For the accuracy, in the thesis ω_p values as a function of I_C are calculated empirically for a given set of I_C and ω_p values obtained by SPICE simulations.

5.5.2. The Example OTA and CCCII Based Filters for Stability Analysis

A current conveyor based new circuit is derived from the OTA based filter in (Chang and Pai, 2000) to explain stability issues well for the OTA and CCCII. The ideal transfer functions of these filters are similar. When active component non-idealities are taken into account, different transfer functions are obtained and their stability conditions will become different.

The example OTA based biquad (Chang and Pai, 2000) is shown in Fig. 5.12. The circuit comprises only two OTAs and only two grounded capacitors. The transconductance gains g_{m1} and g_{m2} are used for tuning the circuit. The derived CCCII based biquad filter is shown in Fig. 5.13. The proposed circuit comprises only two CCCIIs and only two grounded capacitors. In Fig. 5.13, the R_X resistors are employed for tuning the circuit.

For a band-pass filter configuration, the transfer functions of the OTA based and the CCCII based circuits in Figures 5.12 and 5.13 can be given respectively as follows,

$$TF_{OTA}=\frac{I_{o3}}{I_{i2}}=\frac{sg_{m1}g_{m2}}{g_{m1}g_{m2}+sC_1g_{m2}+s^2C_1C_2} \tag{5.7a}$$

$$TF_{CCCII}=\frac{I_o}{I_{i2}}=\frac{sC_1R_2s}{1+sC_1R_2s+s^2C_1C_2R_{X1}R_{X2}} \tag{5.7b}$$

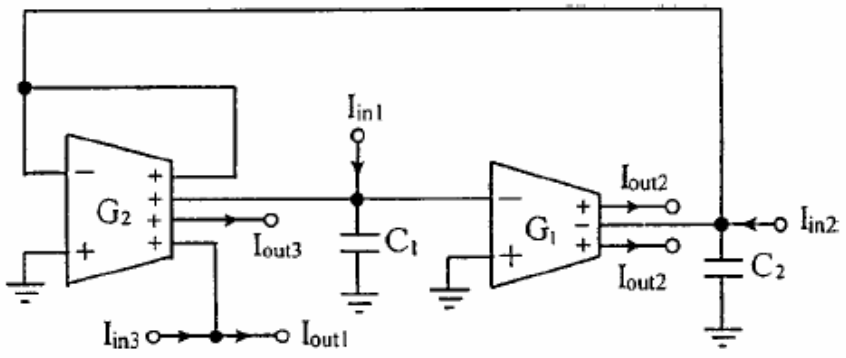


Figure 5.12. Current-mode OTA-C biquad (Chang and Pai, 2000)

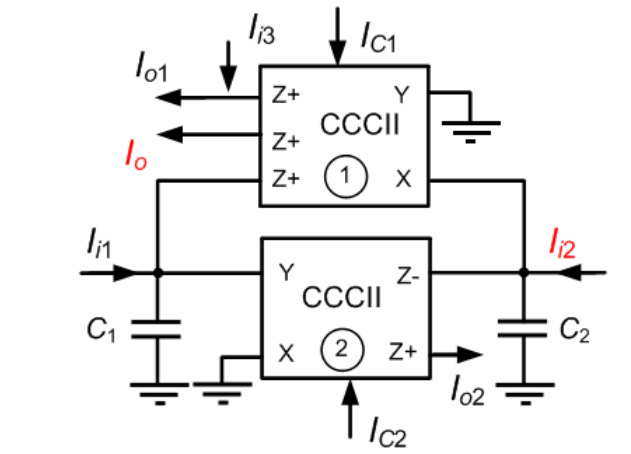


Figure 5.13. The derived current-mode CCCII biquad

5.5.3. A Procedure for Determination the Stability Restriction and Tunability Range

A stability test procedure can be given as follows:

Step 1: The transfer function of the filter is recalculated considering one-pole models given by (4.2) for the OTA and (3.27) for the controlled conveyor.

Step 2: The Routh-Hurwitz stability criterion is applied to the denominator of this non-ideal transfer function. The conditions can be determined analytically by constructing Routh array. Alternatively, the same set of conditions can be obtained as symbolic expressions using symbolic toolboxes of Mathematica or MATLAB. (In the appendix, a code is given for Routh-Hurwitz stability test). These conditions are reprocessed numerically in the next step to determine the parameter ranges with a MATLAB code.

Step 3: In Fig. 5.14, the flow-chart of the MATLAB code is shown. Moreover the MATLAB code is given in the Appendix. The obtained conditions in the previous step can be used to find the tunability range as follows: Some of the circuit parameters can be selected as desired and the others are swept in a desired range. For example, the range of g_m values of OTAs (parasitic R_X resistors for controlled conveyor case) are found for stability corresponding to fixed capacitor values. From the graphs obtained in this way one can easily observe the stable and unstable regions. The code can be explained as,

a) Capacitors and uncontrolled resistors and other constants such as gains are defined in the first part of the code. Here, three kinds of constraints can be taken into account: physical, operational and frequency limitation. Physical constraints determine maximum or minimum element values. For example, maximum value of capacitor can be determined with chip area restrictions. Also, the minimum value of a capacitor should be sufficiently higher than the parasitics of the active element. Secondly, the desired quality factor and the pole frequency of the filter determine the operational constrains. Lastly, the frequency limitations of the active element gains, which are represented by one-pole model in the thesis, increase the order of the filters and some undesired terms appears in the transfer function. As given in (4.26) and (4.29) in Section 4.2, to operate the filter as a biquad, some additional conditions should be taken into account.

b) Two of the tunability parameters such as the g_ms of the OTAs or R_Xs of the controlled conveyors are used as parameters in "FOR loops" of the MATLAB code.

c) Some parasitics such L_X that is given by (5.6) or output impedances that are given by (5.5) depends on control current can be put in this loop. Also corner frequencies of the active elements as illustrated in Section 5.5.1 depend on control current for the OTA and controlled conveyor. These are also defined in this loop as a function of I_C in terms of g_m or R_X for easy calculation.

Step 4: The corner frequency will be assumed as a constant value for the E-CCII and E-DDCC. For the controlled conveyor and the OTA, it depends on control current and it can be found empirically for a given set of control currents and the corresponding ω_p values. For this purpose MATLAB can be used as follows:

a) The control currents, such as 1µA, 3µA, 5µA, 10µA, 30µA, 50µA, 100µA, 300µA and 500µA are given in a vector x=[1 3 5 10 30 50 100 300 500]*1*power(10,-6).

b) The corresponding ω_p values for the control currents are determined with SPICE simulations such as 1.43MHz, 3.93MHz, 6.3MHz, 12.3MHz,

29MHz, 38.8MHz, 52MHz, 70MHz, and 75MHz respectively. They are written as a vector such as y=[1.43 3.93 6.3 12.3 29 38.8 52 70 75]*1*power(10,6) for the controlled conveyor in Fig. 3.11.

c) Using MATLAB command "polyfit(x, y, 4)", the analytical value of ω_p as a function I_C can be found in terms of the I_C for the CCCII in Fig. 3.11 such as $\omega_p(I_C)=6.28\text{x}10^{22}(-2.99(I_C)^4+0.003(I_C)^3)$.

In summary, with this procedure, for some constant parameters, other parameter ranges are graphically determined. The results obtained with the application of the above procedure are given in Sections 5.5.4 and 5.5.5 in Fig. 5.15, Fig. 5.16, Fig. 5.17 and Fig. 5.18. In the next section, this stability procedure is explained with examples.

5.5.4. Stability Comparison of the E-DTA and the Classical OTA

The band-pass current transfer function of the OTA based circuit shown in Fig. 5.12 is given in (5.7a). Considering frequency dependency of g_m given by (4.2), transfer function of the OTA based circuit for the band-pass case, can be given as follows,

$$TF_{OTA}=\frac{sC_1g_{m10}+s^2\dfrac{C_1g_{m10}}{\omega_{p2}}}{g_{m10}g_{m20}+sC_1g_{m10}+s^2C_1\left(\dfrac{g_{m10}}{\omega_{p2}}+C_2\right)+s^3\dfrac{C_1C_2(\omega_{p1}+\omega_{p2})}{\omega_{p1}\omega_{p2}}+s^4\dfrac{C_1C_2}{\omega_{p1}\omega_{p2}}} \tag{5.8}$$

where ω_{p1} and ω_{p2} are corner frequency of the transconductance gains of the OTA_1 and OTA_2 respectively. In (5.8), the effects of the parasitic resistances at the OTA output terminals are ignored for simplicity. Using cascoded output stages, high output resistances are obtained and effect of them can be ignored practically.

From (5.8) it can be seen that due to the limited bandwidth of the transconductance gain of the OTA, a fourth order filter response is obtained with undesirable terms in the transfer function. Ignoring the fourth-order terms, the circuit can operate as a second-order filter by satisfying the following conditions,

$$C_2 >> g_{m10} / \omega_{p2} \tag{5.9a}$$

$$\omega^2 << \frac{g_{m10}}{C_2} \frac{\omega_{p1}\omega_{p2}}{\omega_{p1} + \omega_{p2}} \tag{5.9b}$$

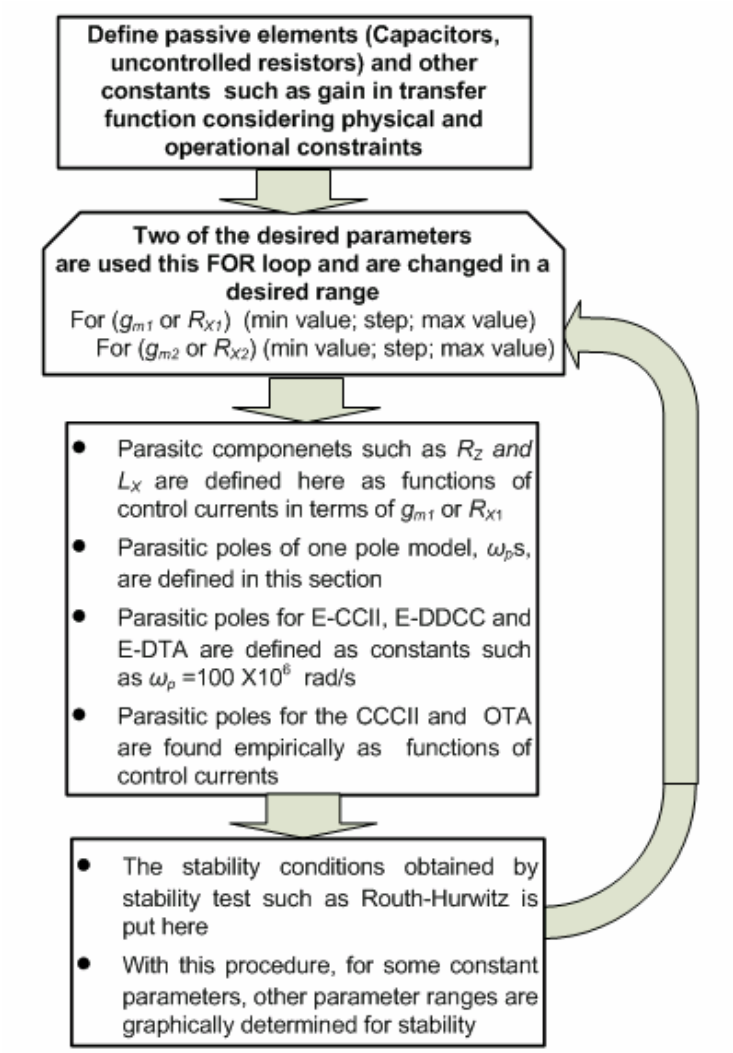


Figure 5.14. Flow chart of the MATLAB code in the stability test procedure

From (5.9) it can be seen that the workability of the OTA-C filter in Fig. 5.12 depends on the value of the transconductance gain of the first OTA (g_{m10}). Therefore, g_{m10} may not be used freely as a tool for tuning the pole frequency or the quality factor of the filter.

5.5.4.1. Stability Analysis of the E-DTA Based Biquad. As explained before, the corner frequencies of the gains of the OTA and current conveyor depend on the control current. The stability advantage of having a constant corner frequency is presented in this chapter. The OTA-C filter in Fig. 5.12 is implemented by E-DTA in Fig. 5.3. To find the stability conditions of the g_{m1} and g_{m2} values making the system unstable, Routh-Hurwitz criterion is applied to (5.8). The conditions obtained by Routh criterion can be given as follows,

$$C_1C_2>0 \tag{5.10a}$$

$$C_1C_2(\omega_{p1}+\omega_{p2})>0 \tag{5.10b}$$

$$C_1\omega_{p1}(C_2\omega_{p2}+\frac{g_{m10}\omega_{p1}}{\omega_{p1}+\omega_{p2}})>0 \tag{5.10c}$$

$$\frac{C_1\omega_{p1}(g_{m10}\omega_{p1}+C_2\omega_{p2}(\omega_{p1}+\omega_{p2}))-C_2g_{m20}\omega_{p1}(\omega_{p1}+\omega_{p2})^2}{g_{m10}\omega_{p1}+C_2\omega_{p2}(\omega_{p1}+\omega_{p2})})>0 \tag{5.10d}$$

$$g_{m10}g_{m20}\omega_{p1}\omega_{p2}>0 \tag{5.10e}$$

Stability test procedure given in the previous section can be applied to this example circuit as follows;

Step 1: As explained in the stability test procedure above firstly non-ideal transfer functions are calculated as given by (5.8).

Step 2: Stability conditions are calculated with Routh-Hurwitz criterion using the Mathematica program at the appendix. The result is given (5.10). As can be seen from the inequalities in (5.10), only (5.10d) could be less than zero, since it includes negative terms.

Step 3: The MATLAB code in appendix whose flow-chart is given in Fig. 5.14 is used in the procedure. Considering desired quality factor and pole frequency of the filter in Fig. 5.12, such as $Q=\sqrt{g_{m1}C_2/g_{m2}C_1}$ and

$\omega_0 = (C_1 C_2 / g_{m2} g_{m1})^{-0.5}$, passive element values are determined. For example, considering the constraints in previous section, arbitrary but reasonable capacitor values are chosen, such as C_1= C_2=5pF. Also, the conditions in (5.9) can be taken into account to minimize frequency limitation effects.

Step 4: The parasitic poles are assumed as ω_{p1}=ω_{p2}=100Mrad/s. The condition in (5.10d) is used for stability test. The g_{m1} and g_{m2}, which are put in the "FOR loop" in the MATLAB code, take different values in the interval of 1μS and 500μS. The MATLAB code is given in Appendix A2.

Figure 5.15 is the graphical representation of the stability test results. It shows the g_{m1} and g_{m2} values restricted by stability conditions. To avoid stability problems, the g_{m1} values can be chosen from the stable area of Fig. 5.15. Also, g_{m1} can be tuned freely without stability problem when g_{m2} value is lower than 260μS for ω_{p1}=ω_{p2}=100Mrad/s. In Fig. 5.16, the analysis is repeated for ω_{p1}=ω_{p2}=150Mrad/s. In this case, the critical value of g_{m2} is increased to 390μS for ω_{p1}=ω_{p2}=150Mrad/s.

5.5.4.2. Stability Analysis of the Classical OTA Based Biquad. In the stability test of the OTA-C filter in Fig. 5.12 using classical OTA, only Step 4 of the stability procedure will be different compared to previous section. Therefore, the MATLAB code that is given in Appendix A3 is used in the Step 4 of this subsection. As explained below, the corner frequencies of the classical OTA depend on biasing currents. As described in Section 5.5.2, the corner frequency of the OTA and current conveyor gains can be practically given in the form of

$$\omega_p = \frac{g_m}{C_{eq}} \tag{5.11}$$

For more accurate results, relation between control current and the corner frequencies can be found empirically as explained in the stability test procedure in the previous subsection.

SPICE simulations show that for the OTA implementation in Fig. 4.14 has the following corner frequencies for the control currents of 3μA, 5μA, 10μA, 30μA, 50μA, 100μA, 300μA and 500μA respectively: 3.5MHz, 4.9MHz, 8MHz, 17.5MHz, 24.77MHz, 41MHz, 106MHz, and 210MHz. From these values, the ω_{p1} and ω_{p2} can be represented with an empirical formula, as a function of control current as follows,

$$\omega_{pn}(I_C)=6.28\text{x}10^{21}(-8.144(I_C)^4+0.0087(I_C)^3) \quad (\text{n}=1, 2) \tag{5.12}$$

The result is given in Fig. 5.17. The pole frequencies ω_{p1} and ω_{p2} of the classical OTA depend on biasing current different from the E-DTA that is a E-DDCC based OTA where the pole frequencies are constant. Figure 5.17 shows that in this case the stable area consisting of g_{m1}-gm_2 pairs is much smaller compared to the cases shown in Fig. 5.15 and Fig. 5.16. Consequently, the E-DTA is expected to relax stability restrictions of OTA-C filters compared to the classical OTA.

5.5.5. Stability Analysis of the CCCII Based Biquad

The derived CCCII based circuit comprises only two CCCIIs and only two grounded capacitors. The use of grounded capacitors is particularly attractive for integrated circuit implementation. Considering one-pole model in (3.27) for $\gamma(s)=0$, the band-pass transfer function given by (5.7b) converts to (5.13). Here, the pole frequency of the $\beta(s)$ ω_β is assumed m times greater than the pole frequency of the $\alpha(s)$ ω_α. The nominal values of current and voltage gains are equal to unity such as, $\alpha_1\approx\alpha_2\approx\beta_1=1$. We assumed $m=2$ for the simplicity. Considering the parasitic inductances at the X terminal the transfer function will become,

$$TF_{CCCII}=\frac{I_o}{I_{i2}}=\frac{sC_1(R_2+L_{x2}s)\omega_{p1}(s+2\omega_{p1})(s+\omega_{p2})}{2\omega_{p1}^2\omega_{p2}+sC_1(R_2+L_{x2}s)(1+sC_2(R_1+L_{x1}s))(s+\omega_{p1})(s+2\omega_{p1})(s+\omega_{p2})} \tag{5.13}$$

As stated before, the corner frequencies of the gains of the CCCII depend on biasing currents. Therefore ω_{p1} and ω_{p2} in (5.13) can be calculated as explained in the procedure.

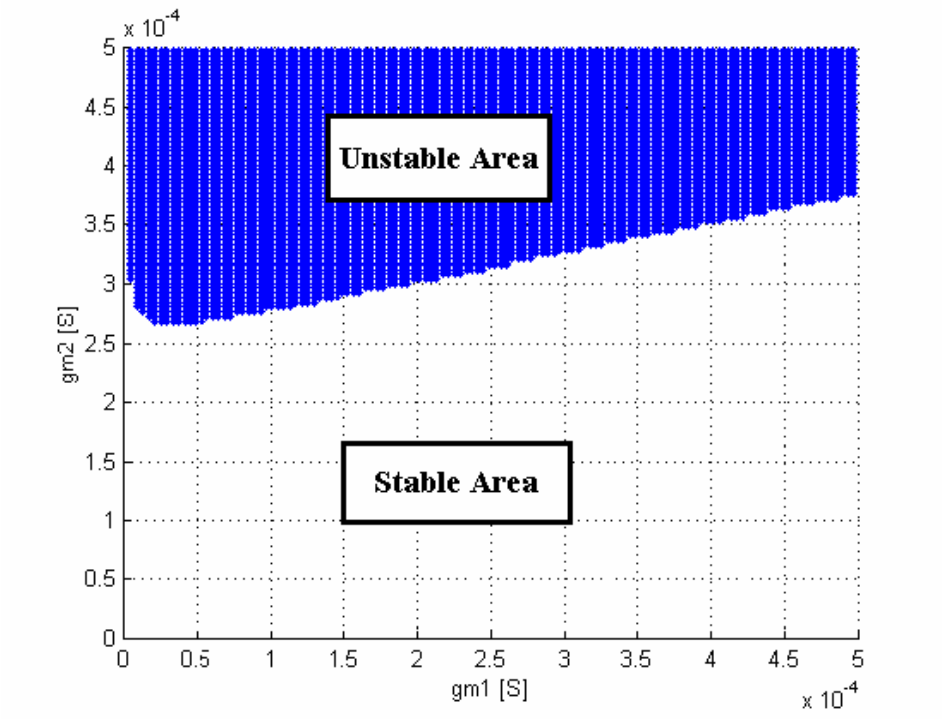


Figure 5.15. The g_m values restricted by stability conditions for the E-DTA with (ω_{p1}=ω_{p2}=100Mrad/s)

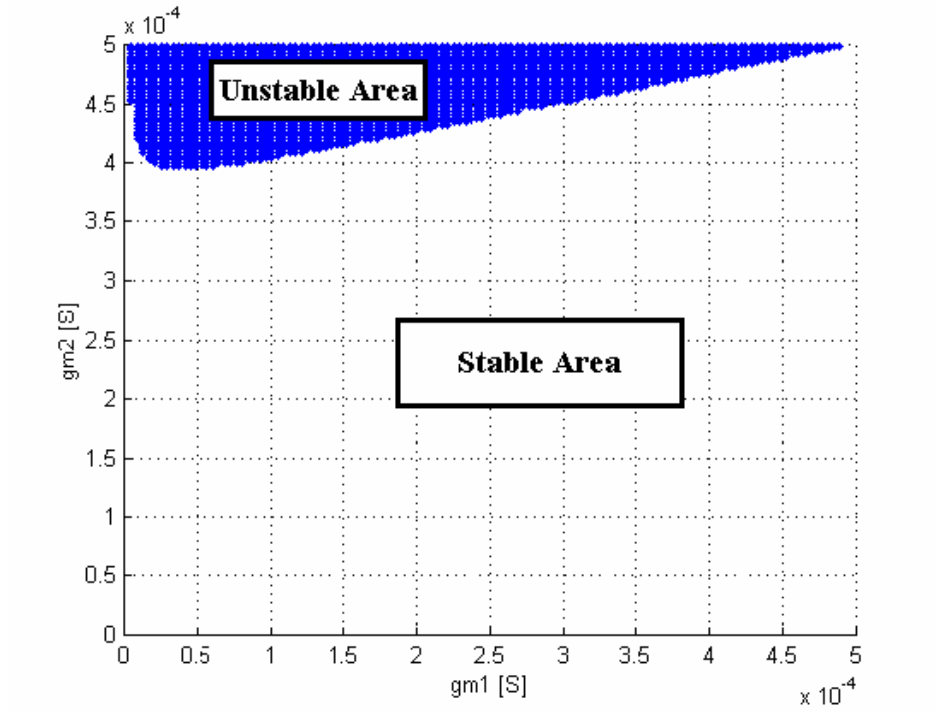


Figure 5.16. The g_m values restricted by stability conditions for the E-DTA with (ω_{p1}=ω_{p2}=150Mrad/s)

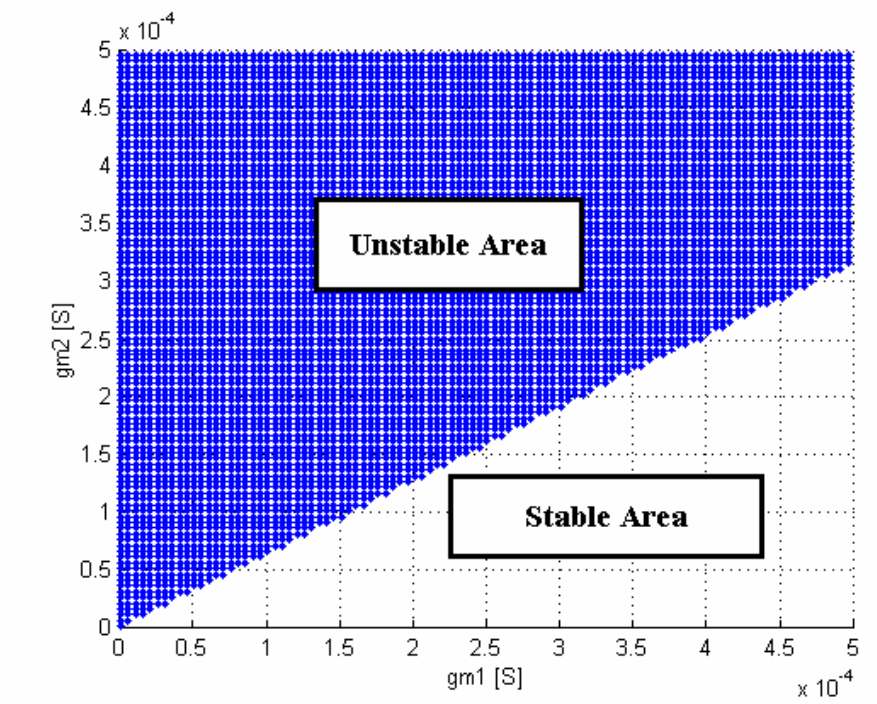


Figure 5.17. The g_m values restricted by stability conditions for the classical OTA where the ω_{p1} and ω_{p2} are dependent on control current

For example, the analytical expression for ω_p as a function I_C for the CCCII in Fig. 3.11 are equal to $\omega_p(I_C)=6.28\text{x}10^{22}(-2.99(I_C)^4 +0.003(I_C)^3)$. Also the L_{X1} and L_{X2} that are parasitic inductances in series to the X terminal of the CCCII depend on biasing current as given by (5.6).

In Fig. 5.18, the result of the procedure is given where ω_ps and L_Xs are functions of I_C. Considering the constraints mentioned in the procedure, arbitrary but reasonable capacitor values are chosen, such as $C_1= C_2$=5pF. R_1, R_2 take different values in the interval of 500Ω and 25kΩ. Figure 5.18 shows the R_1 and R_2 pairs restricted by stability conditions.

5.6. Summary

Firstly, in this chapter, we point out that the corner frequency of the OTA and controlled conveyor gains change with control current. This situation may affect the stability of the filters in an undesired way. It is concluded that tunability and stability are

not completely independent issues. For an electronic filter tunability range may be limited by stability constraints. Therefore, constant bandwidth feature of current adjusting technique is expected to be good solution to the stability problem. In this chapter, a CMOS implementation of the E-DDCC is given. E-DDCC can also be used instead of current conveyor or can replace the OTA as explained in this chapter. Thus, current adjusting technique can be adapted to OTA based filters.

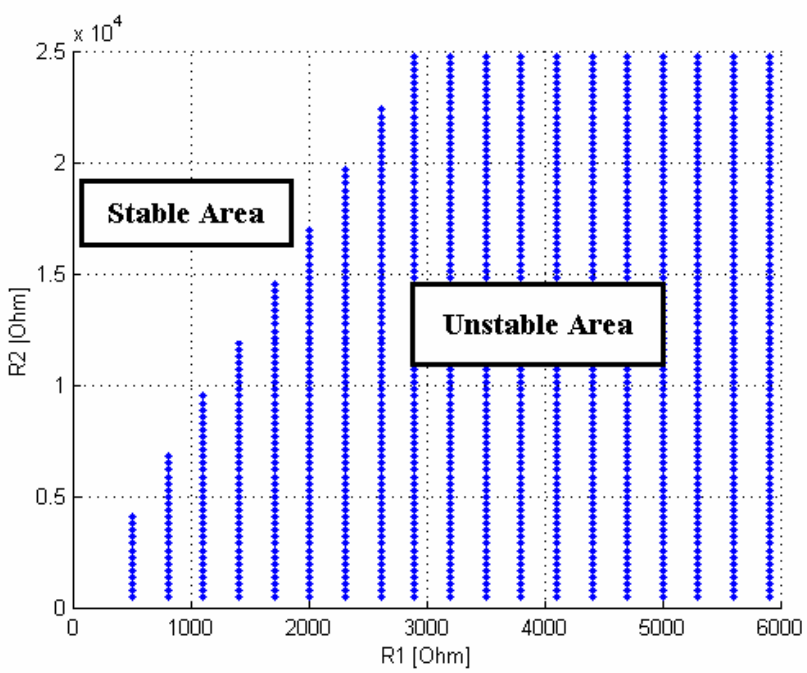


Figure 5.18. Tunability restricted by stability ω_ps and L_Xs are functions of the I_C for the CCCIIs

Also, current adjusting techniques require more than 10 transistors and their tunability ranges are not as wide as the OTA and the controlled conveyor. Hence, it may be a good idea to use two current conveyors and MOSFET based electronic resistors together to obtain E-CCII equivalent circuits. In this way, it is expected to obtain a wide current adjusting range that is proportional to the ratio of the resistors. Moreover in the literature, Carlosena and Moschytz supported this idea by presenting op-amp and CCII based E-CCII equivalent circuits (Carlosena and Moschytz 1994).

The approach given in this chapter can easily be used to evaluate the tunability range of a specific filter considering the limitations put by stability conditions. When stability is more important than other properties of a filter, current adjusting technique should be preffered compared to the methods in Chapters 3 and 4.

6. CONCLUSION

In integrated circuits element tolerances are unacceptably high. Non-idealities and parasitics due to IC implementation are serious problems for the circuits after manufacturing. Therefore, electronic tuning of some parameters after production has been a very important feature in IC design. In the thesis major tunability methods are examined with new example circuits and detailed non-ideality and parasitic component analyses of these circuits are given. Tunability methods are compared and trade-offs between tunability and other parameters of the circuits are illustrated.

6.1. Evaluations of Tunability Methods and Contributions

In this section, a general evaluation of the tunability techniques is given. The contributions of the thesis to the subject are summarized.

- In the thesis we examined two MOSFET-C techniques not requiring an op-amp but reduced number of transistors. Firstly Acar-Ghausi technique is re-visited. The MOS resistive cell in the Acar-Ghausi technique is implemented using only three transistors.
- We presented a new all-pass filter using this 3-transistor MRC adapting MOSFET-C filters to low-voltage/low-power design trend. There are only two transistors between the rails. Also it is very suitable for high frequency of operation due to its simplicity. We found that this simple MRC has an important non-ideality: Non-zero output impedance.
- Two solutions are proposed for the non-zero output impedance problem and these solutions are applied to the presented all-pass filter. One solution is changing the gain k of the inverting voltage buffer and the other solution is changing the matching ratio m of the resistors. Graphical representations for the optimum k and m values are given. Moreover, the functionality of the presented example filter is verified with experiments.
- Another technique not requiring an op-amp is the replacement of the grounded resistor with a simple electronic resistor. Some grounded electronic resistor

implementations in the literature are compared in terms of linearity. The most suitable one is chosen for the simulations. Also several new filter examples are presented with grounded resistors suitable for electronic tunability.

- MOSFET based resistors are tuned by voltage. The trend of low-voltage IC design not only reduces power supply voltages but also limits the range of control voltages. Operation conditions of the MOSFETs and the relation of these conditions to input signal amplitude are expected to keep the control voltages in a narrow range.
- On the other hand, the current and voltage relations of the MOSFET are valid only for transistor sizes greater than approximately 2μm due to some practically undesired effects such as channel length modulation and mobility reduction. This prevents the reduction of the lengths of the MOS transistors, which are used as resistors. Therefore it is possible to mention about a scalability problem adapting MOSFET-C filters to the submicron IC technologies to keep acceptable linearity.
- Conversely, active elements such as the controlled conveyor and the OTA that can be successfully scaled to submicron levels have been widely used in the design of electronically tunable circuits in the last decade. Thus, electronic tunability with controlled conveyor and OTA is also examined due to their larger tunability ranges.
- The advantage of controlled conveyor for tuning element-matching condition is presented with an all-pass filter example published as (Metin *et al.*, 2003)
- The possibilities of less commonly used controlled conveyors such as the first generation current conveyor are also examined. We focused on new opportunities of the CCI compared to the CCII while explaining electronic tunability with controlled conveyors.
- Having a high impedance Y terminal seems the evident advantage of the CCII over CCI, so that it can be used in the design of cascadable voltage mode filter circuits. Nevertheless, it is shown that also the first generation current conveyor is able to provide high input impedance in some filters where the second generation cannot.
- Analog filters with enhanced dynamic range are examined and relation of cascadability using the Y terminal of the CCII with respect to enhanced dynamic range is emphasized. A second order tunable notch/all-pass filter is presented for enhanced dynamic range being compared with cascadable circuits from the literature.

- We illustrate a possible advantage of using first generation current conveyor for reduced power consumption compared to second generation. We presented a simple method for compensating parasitic resistor in the X terminal derived from its terminal relationship of the CCI. Due to this method, the CCI does not need high biasing current to avoid undesired parasitic resistance at the X terminal, which is an important parameter for power consumption. A tunable FDNR simulator example using controlled CCIs is presented to show the parasitic compensation feature reducing power consumption.
- A CMOS implementation of a relatively new active element, which is based on the controlled conveyor principle, is also given and examined: The controlled CDBA. In the controlled CDBA, the resistors in series to both input terminals N and P are electronically controllable similar to CCCII. Furthermore a CMOS implementation of the controlled CDBA is presented. Moreover, the tunability and cascadability advantages of the C-CDBA are emphasized with a novel first order all-pass circuit.
- An OTA-C all-pass filter is proposed with reduced active element and compared with other OTA-C and current conveyor based resistorless filters from the literature. During the comparison some trade-offs in analog design are discussed.
- Also, one OTA-C and one OTA-RC filters are comparatively examined in the related chapter. The advantages of using additional passive resistors and the reduction of the number of OTAs have not been sufficiently examined in the literature. Therefore the effects of frequency limitations of the transconductance gain of the OTA are examined further.
- In the controlled current conveyor and OTA based filters, there is a difficulty in selecting control currents for desired operating frequency, because the corner frequency of the current and transconductance gains also depend on the control currents. This situation limits element selection range with respect to the high frequency of operation and the stability. For these reasons, we emphasize another approach to the electronic tunability: Adjusting the current gain.
- We adapted the controlled current gain principle of the electronically tunable current conveyor (E-CCII) to the DDCC because E-DDCC is a more general type active element that can be used instead of the current conveyor. Moreover, the E-DDCC with a grounded resistor at its X terminal can replace the OTA because of differential

voltage inputs. This E-DDCC based OTA is denoted as E-DTA in the thesis. Firstly we presented a CMOS E-DDCC internal structure, and used it in an all-pass filter application for electronic tunability.

- In the thesis we also focused on stability problem limiting the tunability range of the analog filters. More realistic macro models are recommended for better stability comparison where parasitic components and bandwidth of the OTA and the CCCII depend on the control current. A stability test procedure with MATLAB codes is presented such that the results are shown in an interpretable graphical format to guide the application engineer for the optimum or near optimum selection of the filter and element values.

6.2. Comparisons

In this section, the major techniques of electronic tunability discussed in the thesis are compared. However before starting with comparisons, we should briefly mention the difficulties on this issue. The first difficulty in the comparisons is related with the technology that the performance of the circuits strictly depends on. A limitation that is effective in a CMOS based circuit may not be noticeable in a bipolar transistor based circuit. (Ananda Mohan, 2003). Secondly, there are a lot of OTA and current conveyor implementations in the literature. They have some advantages and disadvantages due to their topological differences compared to each other. Therefore, the comparison given in this chapter can provide only a general idea for tunability methods. However, making a final decision is very difficult in this technologically rapidly developing area, it is easy to find some counter examples about the comments below.

- For some cases MOSFET-C filters can be preferred over OTA-C and translinear-C filters. In conjunction with high tolerances and large chip area requirement of passive IC resistors, replacing them with electronic resistors make MOSFET-C filters attractive. Therefore, MOSFET-C technique can be preferred over the OTA and the controlled conveyor when both high frequency of operation and high resistance values are required. Low control currents are required in the OTA and controlled conveyor to obtain high resistance values. This decreases the bandwidths of them. In a MOSFET-C filter, both high biasing currents can be used for high frequency of

operation and high resistance values with MOSFET resistors can be obtained. On the other hand, in the classical op-amp based MOSFET-C filters, well-known limitations of the op-amps restrict the high frequency performance.

- In the thesis, we proposed an approach adapting MOSFET-C technique to the low voltage/low-power design. Also it is suitable for high frequency of operation due to its simplicity.
- In bipolar OTA and controlled conveyor, the I_C / V_T ratio determines the tunability range. However in the MOSFET-C technique the ratio of $1/(V_C–V_T)$ determines this range. Therefore, with respect to tunability range, the OTA and controlled conveyor could be preferred.
- Both OTA and controlled conveyor can be implemented by comparable number of transistors. However, the current adjusting technique requires large number of transistors. As a result, the current adjusting technique will not be good choice if number of transistors is considered.
- The tunability methods where active elements are biased with constant currents such as the MOSFET-C and the current adjusting technique are expected to provide better stability compared to the OTA and the controlled conveyor. In the thesis, it is shown that the variable corner frequencies of the gains in the OTA and controlled conveyor decrease element selection range in conjunction with stability problems. For the applications where both the tunability and stability are very important such as high Q filters, these techniques should be preferred.

In Table 6.1, the electronic tunability methods are summarized. The comparison considering various criteria in Table 6.1 is a result of several years of work on the subject and reflects our experience. They should not be considered as strong universal claims; it may easily be possible to find counter examples in the literature. Moreover, due to rapid technological development substantial changes in the Table may be expected.

6.3. Ideas for Future Work

- The one-pole model can give an idea about stability of the circuits assuming the second parasitic pole is at sufficiently high frequency. As a future work, more precise models can be developed depending on particular active element including two or more poles and zeros to increase the accuracy of the stability analyses.

- The MRC of Acar and Ghausi can be used in the design of basic building blocks such as integrators, to design analog filters, where low voltage and high frequency of operation is important.

- The E-CCII implementations in the literature employ larger number of transistors compared to standard current conveyors. Also, extending the tunability range of this active element would be very important. Therefore, new techniques and internal structures can be developed for simplicity and wide tuning range especially for CMOS.

Table 6.1. The comparisons of the tunability methods

	CRITERIA	MOSFET-C	Controlled Conveyor	OTA	E-DDCC
1	High frequency performance	Moderate	High	High	High
2	Low-voltage operation and number of transistors between rails	Yes, (2 in the thesis)	Yes, 3	Yes, 3	Yes, 3
3	Tunability range	Narrow	Wide	Wide	Moderate
4	Simple realization	Yes	Yes	Yes	No
5	Stability due to bandwidth variation	Good	Bad	Bad	Good

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APPENDIX A: EXAMPLE CODES FOR STABILITY TESTS

A1: A Mathematica Code for Routh-Hurwitz Stability Tests

```
(* p is the characteristic equation *)
p=(a_n S^n +...+ a_3 S^3 + a_2 S^2 + a_1 S+ a_0);
d=Exponent[p,S];
Array[a,11,11]; Do[Do[a[i][j]=0,{i,1,11,1}],{j,1,11,1}];
Array[b,11];
Do[b[m]=0,{m,1,11,1}];
p=p S;
n=d+1;
Do[b[n+1-m]=Coefficient[p,S^m],{m,1,11,1}];
Module[{j=1},Do[a[1][j]=b[i]; j++;,{i,1,11,2}];];
Module[{j=1},Do[a[2][j]=b[i]; j++;,{i,2,10,2}];];
For[i=3,i<13,i++,  For[j=1,j<(((12-i)/2)+1),j++,  a[i][j]=((a[i-2][j+1]  a[i-1][1])-(a[i-1][j+1]
a[i-2][1]))/a[i-1][1]; If[a[i][1]Š0,a[i][1]=e]]];
Do[Print[FullSimplify[a[i][1]]>0],{i,1,n,1}]
```

A2: MATLAB Code for Stability Test in Section 5.5.4.1

```
clear all
i=1;
% Defining component values
wp1=100*power(10,6);
wp2=100*power(10,6);
C1=5*power(10,-12);
C2=5*power(10,-12);

for gm1=1*power(10,-6):10*power(10,-6):500*power(10,-6);
   for gm2=1*power(10,-6):10*power(10,-6):500*power(10,-6);

% Stability condition

z=gm1.*wp2.*((-1).*C2.*gm2.*(wp1+wp2).^2+C1.*wp1.*(gm1.*wp1+C2.* ...
  wp2.*(wp1+wp2)));

      Z(i,:)=z;
      hold on
      if z<0
            GRID
         plot(gm1,gm2,'.')
         xlabel('gm1 [S]')
         ylabel('gm2 [S]')
      end;
      i=i+1;
   end;
end;
GRID
```

A3: MATLAB Code for Stability Test in Section 5.5.4.2

```
clear all
i=1;
% Defining component values
C1=5*power(10,-12);
C2=5*power(10,-12);

for gm1=1*power(10,-6):10*power(10,-6):500*power(10,-6);
   for gm2=1*power(10,-6):10*power(10,-6):500*power(10,-6);
  %     Corner frequencies depend on the control currents

wp1=6.28.*power(10,21)*(-8.1445*(gm1*0.052)^4 +0.0087*(gm1*0.052)^3 );
wp2=6.28.*power(10,21)*(-8.1445*(gm2*0.052)^4 +0.0087*(gm2*0.052)^3 );

% Stability condition
z=gm1.*wp2.*((-1).*C2.*gm2.*(wp1+wp2).^2+C1.*wp1.*(gm1.*wp1+C2.* ...
 wp2.*(wp1+wp2)));
      Z(i,:)=z;
      hold on
      if z<0
           GRID
        plot(gm1,gm2,'.')
        xlabel('gm1 [S]')
        ylabel('gm2 [S]')
      end;
      i=i+1;
   end;
end;
GRID
```