THE DESIGN ASPECTS OF AN OPTICALLY POWERED CMOS RECEIVER FRONT-END FOR ELECTRICALLY ISOLATED APPLICATIONS

by

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ABSTRACT

THE DESIGN ASPECTS OF AN OPTICALLY POWERED CMOS RECEIVER FRONT-END FOR ELECTRICALLY ISOLATED APPLICATIONS

The receiver circuitry in a wireless communication system is a key component in determining the overall system performance. The power of the receiver circuitry is usually provided from a battery or through copper wires. However, there are a number of application areas including wireless communication, aerospace, defense, and medical, which subject sensors, transducers, and other communication devices to high radio frequency (RF), electromagnetic interference (EMI), or magnetic fields. It is more appropriate to provide power of these systems via optical rather than electrical means. This thesis presents the design and implementation of an optically powered receiver front-end for electrically-isolated micro-scale applications. The presented work first deals with the realization of a miniaturized optical power supply unit. The monolithic integration of complementary metal oxide semiconductor (CMOS) photodiodes together with the active circuitry on the same substrate has been considered in detail. A novel architecture consisting of an integrated photodiode connected to a direct current to direct current (DC/DC) converter has been presented and designed in a low-cost 0.18 μm CMOS process. The DC/DC converter utilized in the presented architecture has a maximum efficiency of 56% and is able to increase the photodiode voltage of 0.5 V and 0.6 V to 1.2 V and 1.5 V, respectively. In the second part of this thesis, the design of a low-power integrated receiver front-end that consists of a low noise amplifier (LNA), voltage gain amplifier, a mixer and a low-pass filter has been presented. A different design technique so-called noise matching has been introduced for the design of the LNA. The differential LNA consumes 1.4 mA from a 1.2V supply voltage and has a measured S_{21} of 30 dB. The noise figure of the LNA has been measured as 7.3 dB with respect to 50 Ω. This translates into a projected noise figure of 0.35 dB when the LNA is used with an example solenoid coil given in this thesis. Finally, the receiver front-end has been powered optically and tested with a light-emitting diode (LED) driver circuitry.

ÖZET

ELEKTRİKSEL YALITILMIŞ UYGULAMALAR İÇİN OPTİK OLARAK GÜÇLENDİRİLEN BİR CMOS ALICI ÖN-UCUNUN TASARIM YÖNLERİ

Telsiz iletişim sisteminde yer alan alıcı devresi, sistemin tüm performansını belirleyen anahtar bir bileşendir. Alıcı devresinin gücü genellikle bir pilden veya bakır kablolar üzerinden sağlanır. Ancak, algılayıcılar, dönüştürücüler ve diğer iletişim aygıtlarını yüksek radyo frekans (RF), elektromanyetik girişim (EMI) veya manyetik alanlara maruz bırakan telsiz iletişim, hava-uzay, savunma ve sağlık gibi birkaç uygulama alanı bulunmaktadır. Bu tür sistemlerin gücünü elektriksel yöntemler yerine optik olarak iletmek daha uygundur. Bu tez, elektriksel yalıtılmış uygulamalar için optik olarak güçlendirilen bir alıcı ön-ucunun tasarımı ve gerçekleştirilmesini sunmaktadır. Sunulan çalışma, öncelikle minyatür bir optik güç sağlama ünitesinin gerçekleştirilmesini ele almaktadır. Tamamlayıcı Metal Oksit Yarıiletken (CMOS) fotodiyotlar ile aktif devrenin aynı taban üzerinde monolitik bütünleştirilmesi detaylı bir şekilde değerlendirilmiştir. Tümleşik bir fotodiyota bağlanmış bir doğru akım/doğru akım (DC/DC) çeviricisini içeren yeni bir mimari sunulmuş ve düşük maliyetli bir 0.18 μm CMOS sürecinde tasarlanmıştır. Sunulan mimaride kullanılan DC/DC çevirici maksimum %56 verimliliğe sahip olup, 0.5 V ve 0.6 V fotodiyot voltajlarini sırasıyla 1.2 V ve 1.5 V'a yükseltebilmektedir. Tezin ikinci bölümünde, düşük gürültülü yükselteç (LNA), gerilim kazançlı yükselteç, karıştırıcı ve alçak geçiren süzgeçten oluşan düşük güç tüketimli bir tümleşik alıcı ön ucunun tasarımı verilmiştir. Tasarlanan farksal LNA devresi, 1.2 V besleme geriliminden 1.4 mA akım tüketmekte olup S_{21} parametresinin değeri 30 dB olarak ölçülmüştür. LNA devresinin gürültü sayısı 50 Ω giriş empedansı için 7.3 dB olarak ölçülmüştür. LNA devresinin tezde verilen örnek bir solenoid bobinle birlikte kullanılması durumunda gürültü sayısının 0.35 dB olacağı öngörülmüştür. Son olarak, alıcı ön ucu optik olarak güçlendirilmiş ve ışık yayan diyot (LED) sürücü devresi ile test edilmiştir.

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LIST OF SYMBOLS/ABBREVIATIONS

A_v	Voltage gain
C_{bot}	Bottom plate parasitic capacitance
C_{gs}	Gate-to-source capacitance
CLK	Clock signal
$\overline{\text{CLK}}$	Inverted clock signal
C_{ox}	Gate oxide capacitance
C_{par}	The sum of parasitic capacitances per stage for DC/DC converter
C_{st}	The stage capacitance for DC/DC converter
C_{top}	Top plate parasitic capacitance
d	Diameter
E_g	The band gap energy of the semiconductor material
E_{ph}	The energy level of incident photons
f	Frequency
g_m	The device transconductance
h	Planck constant
I_D	Drain bias current
I_{DD}	Supply current
$\overline{i_d^2}$	The noise drain current
I_G	The gate leakage current
$\overline{i_g^2}$	The noise gate current
I_{In}	The input current of the converter circuit
I_L	Output current loading
I_0	The intensity of light at the surface of the silicon
I_{Ph}	Photodiode current
I-V	Current-voltage
k	The Boltzman constant
K	Device specific constant for flicker noise term
l	Length
L	Inductance

N	Number of voltage doubler stages
NF	The noise figure
P	Optical power level
P_0	The incident optical power
P_{dyn}	Dynamic power losses
P_{in}	The power drawn from the supply V_{DD}
P_{loss}	The overall power losses in the converter
P_{noise}	The noise power
P_{out}	The power delivered to the load
P_{res}	Resistive power losses
P_{signal}	The signal power
q	The electronic charge
r_g	The gate resistance
$R_{out,id}$	The ideal series output resistance of DC/DC converter
R_P	Parallel resistance
R_S	Source resistance
R_{st}	The resistance for a straight wire
T	The absolute temperature
V_{DD}	Supply voltage
$\overline{v_n^2}$	The thermal voltage noise
V_{out}	Output voltage
V_{Ph}	Photodiode voltage
V_{rms}	Rms value of voltage signal
W	Width of transistor
ω_{op}	The operating frequency
Z_{in}	The input impedance
α	The voltage gain of passive network
α_B	The coefficent for bottom plate parasitic capacitance
α_T	The coefficent for top plate parasitic capacitance
α_{max}	The maximum value for α
$\alpha_{optical}$	The optical absorption coefficient

δ	The skin depth
η	The power efficiency
$\eta_{quantum}$	The quantum efficiency
λ	The optical wavelength
μ_0	The permeability in vacuum
μ_r	The relative permeability of the conductor
ν	The optical frequency
ξ	The enhancement factor resulting from the proximity effect
ρ	The Electrical resistivity
Ω	Ohm

ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
DC/DC	Direct current to direct current
EHPs	Electron and hole pairs
EMI	Electromagnetic interference
FETs	Field-effect transistors
FF	Fill factor
IC	Integrated circuit
IF	Intermediate frequency
LC	Resonance circuit consisting of an inductor and a capacitor
LED	Light-emitting diode
LNA	Low noise amplifier
LO	Local oscillator
MIM	Metal-insulator-metal
MOS	Metal oxide semiconductor
MR	Magnetic resonance
MRI	Magnetic resonance imaging
nMOS	n-type metal oxide semiconductor
PCB	Printed circuit board
pMOS	p-type metal oxide semiconductor
RC	Resistor-capacitor

RF	Radio frequency
RLC	Resistor-inductor-capacitor
RMS	Root-mean square
SMU	Source-measure units
SNR	Signal-to-noise ratio
SOI	Silicon on insulator
UMC	United Microelectronics Corporation

1. INTRODUCTION

The rapid development in wireless communication technology has introduced many types of mobile communication devices, such as cellular phones, global positioning systems, and wireless broadband internet into our daily life. From the system perspective, it is desirable to develop low-power integrated circuits that perform various functions on a single chip. Currently, the complementary metal oxide semiconductor (CMOS) process technology allows a high level of integration and lowers the production costs.

The radio frequency (RF) front-end circuitry is arguably the most important part of a receiver system. Basically, the front-end circuitry consists of the components that downconvert the original incoming RF signal into a lower intermediate frequency (IF). Without a high performance front-end, all other higher layers of signal processing and data handling in a wireless network are irrelevant. The power of the receiver front-end systems is usually provided through copper wiring. However, there are application areas where it is more appropriate to deliver the power of the receiver systems via optical, rather than electrical means. These applications include sensors, low-power communication devices and numerous other electronic devices operating inside high RF [1], EMI [2], or other harsh environments [3]. Delivering power to these systems over fiber optic cable instead of copper wiring or using batteries introduces the following advantages:

- Immunity to surrounding RF fields, magnetic fields, and high voltage effects
- No interfering radiation from the power source
- Operation over longer distances than copper
- No need to change batteries periodically

The work presented in this thesis is concerned with the realization of an optically powered CMOS receiver front-end design for electrically isolated applications. The presented system can target a variety of applications including aerospace, defense, industrial sensors, wireless communications and biomedical. However, in order to demonstrate the practicality of the presented system for a specific application, the

specifications of a biomedical application, namely Magnetic Resonance Imaging (MRI) have been selected.

MRI is a safe and reliable imaging technique that provides good soft tissue contrast while avoiding harmful ionization [4]. It is highly desired to use the MRI technology for minimally invasive procedures that increase the correct diagnosis chance and reduce the probability of surgical operations thereby minimizing the health costs and offering advantages for both the patient and the medical staff. In many of the minimally invasive procedures, a catheter is used to treat vascular diseases like heart coronary disease. Currently, surgeries are performed with X-ray fluoroscopy which exposes the patient and the medical staff to ionizing radiation [5]. Therefore, investigations were made to show that MRI might provide an alternative to X-ray imaging in interventional therapy [6-13]. However, tracking of the catheter tip is needed for real-time MRI, unlike X-ray fluoroscopy [1]. This is due to the fact that real-time MRI is based on updating one or more slices frequently.

Nevertheless, there are obvious obstacles to in-vivo catheter usage in MRI system in its present form. Since MRI operation is based on high magnetic fields, magnetic material usage is prohibited. One other disadvantage is that conductive heating [14,15], due to electric field present in the MRI system, introduces tissue damage, putting an obstacle to signal/power transmission through conductors. In its present form, magnetic resonance (MR) compatible catheters are passive and they do not offer high contrast ratio, resulting in barely noticeable catheter tips, which can easily disappear from the imaging slice [16,17,18]. Therefore, a microsystem, that is compact, miniature, active, and MR compatible is necessary for the localization of catheters, providing a real-time monitoring. The work presented in this thesis is specifically designed as the analog front-end part of an integrated miniature active tracking microsystem placed at the tip of a catheter. However, the presented design is not limited to tracking systems in MRI and can be applied to a variety of applications where miniaturization and optical powering have utmost importance.

The localization technique utilized in the presented design is based on detecting the frequency difference between the applied RF signal and the spin echo signal coming from

the tissue. Basically, a spatial distance of 20 cm that is between -10 cm and +10 cm (relative to the center of the MR plane) translates into a calculated frequency interval of 100 kHz [19]. Figure 1.1 shows the frequency band versus spatial distance for an example gradient field in a 3 Tesla (3T) MRI system. Since the center frequency is 123 MHz for the magnetic field of 3T, the spatial distance covered by this example can be shown with a frequency band between 122.9 MHz and 123.1 MHz.

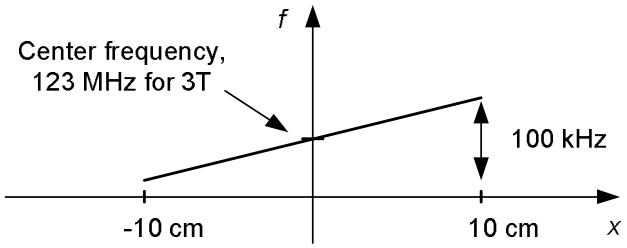

Figure 1.1. The frequency band versus spatial distance for an example gradient in a 3T MRI system

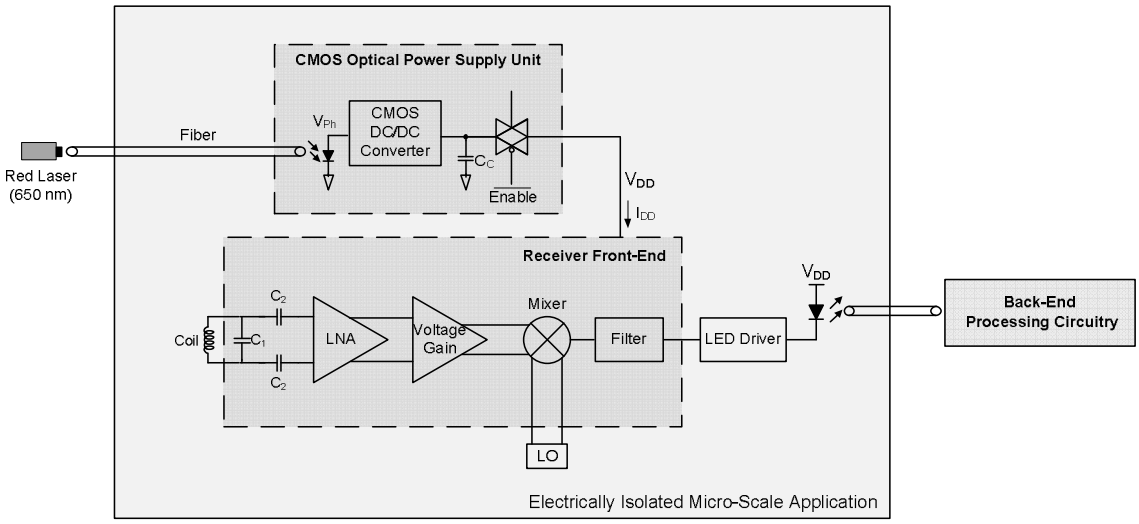

Figure 1.2. The basic block diagram of the optical power supply unit together with the receiver front-end [20]

Motivated by the need for RF safety in MRI systems, a compact CMOS optical power supply unit has been developed in this thesis. The developed module uses a single integrated photodiode in a standard unmodified sub-micron CMOS process as the optical-to-electrical converter. Since a compact optical power supply unit must be able to supply voltage levels higher than the open-circuit voltage of a single silicon photodiode (i.e. 0.6

V) for operation of today's CMOS electronic circuits, a low-voltage DC/DC converter has been designed in order to increase the DC voltage of the photodiode to the desired voltage supply levels. The module can be integrated into a miniaturized system where a micromachined silicon fiber platform carries optical power to be converted into the electrical one. The overall optoelectronic system can be safely used to supply power to the electronic systems which operate in harsh environments. Figure 1.2 shows the basic block diagram of the electrical part of the optical power supply unit together with the receiver front-end presented in this thesis [20].

The receiver front-end, which has been designed specifically for the operating frequency of 123 MHz, consists of a LNA, a voltage gain amplifier, a mixer, and a low-pass filter. The design strategy utilized for the LNA is unique in the sense that it enables an ultra low noise performance (noise figures below 1 dB) and a fully integrated solution. Generally, the method of impedance matching is used in order to maximize power transfer from the coil to the LNA. However, this degrades the noise performance of the LNA and requires the design to include an off-chip inductor for the selected operating frequency of 123 MHz. The technique that will be presented in this thesis for the LNA design utilizes the inductance already in the coil in order to minimize the noise figure.

Much of the work in this thesis is focused on the design, analysis and implementation of the devices and circuits for the optically powered receiver front-end in a low cost CMOS 0.18 µm process as a part of TÜBİTAK 1001 project (108E119). The main contributions of this thesis can be summarized as follows:

- A micro optical power supply unit compatible with standard CMOS foundry processes has been developed. The presented unit accomplishes the integration of a monolithic photodiode together with a low-voltage DC/DC converter that has been especially designed to be able to boost input voltage levels as low as 0.5 V. The existence of a feedback mechanism between the photodiode and the DC/DC converter that acts as an intrinsic voltage regulator for the overall design has been shown and analyzed in detail.
- An ultra-low noise and high gain receiver front-end that consists of a low-noise amplifier has been developed to be integrated with a mixer circuit. The utilized

design strategy, which does not involve impedance matching method, enables an LNA design without an off-chip inductor at the operating frequency of 123 MHz.

- The design, analysis and implementation of the devices and circuits for the optically powered receiver front-end in a low cost CMOS 0.18 µm process have been studied in detail. The overall design can be integrated with any active CMOS circuitry such as sensors, receivers and transducers for applications where electrically isolated power delivery is necessary.

The rest of this thesis is structured as follows: Chapter 2 presents the design, analysis, implementation and characterization of the optoelectronic CMOS power supply unit. In addition, it discusses the possible photodiode configurations in a standard triple-well CMOS process and gives the feedback mechanism between the integrated photodiode and the DC/DC converter in the designed system. Chapter 3 presents the integrated low-power receiver front-end together with the utilized design approach for minimum noise configuration and high gain. Further, the chip implementation and measurement results have been given both for the LNA, and the overall integrated receiver front-end. Finally, the conclusions are given in Chapter 4.

2. INTEGRATED OPTOELECTRONIC CMOS POWER SUPPLY UNIT

There are a number of application areas including wireless communication and medical imaging which subject electrical systems to high RF fields, magnetic fields [1], EMI [2] or high-temperature media [3] where it is more appropriate to provide the power of these systems via optical, rather than electrical means. The main objective of using optical powering is to reduce the number of conductor lines feeding the system of interest, which at the same time helps to eliminate the ohmic losses and the heating effects, for instance in the presence of strong RF fields. Optical powering systems usually consist of an optical power source, a transmission medium, where light is guided, and an optical-to-electrical converter. Although photovoltaic solar cells have been frequently used as optical-to-electrical converters for macro-scale applications [21-24] they are not convenient for emerging micro-scale electronic systems such as biomedical implants [1,25,26,27] and sensors [28,29] which demand compact, miniaturized optical-to-electrical converters. CMOS compatibility of the optoelectronic device becomes an important issue when there is a need for high-level integration of various functionalities in a small area using a single substrate [30-33]. Such a capability greatly reduces the packaging costs as well as resulting in a better noise immunity.

In order to realize a compact optical powering system, a photodiode can be used as the optical-to-electrical converter due to its much smaller size at the expense of reduced efficiency. Photodiodes can be used in photovoltaic (solar cell) mode in contrast to their general usage in reversed biased region as sensors in optical communications [34] and photo sensing applications [35]. In photovoltaic mode, the photodiode, which is basically a semiconductor p-n junction, becomes forward biased and converts optical power into electrical power by supplying photocurrent to any electronic circuit.

A compact optical powering system must typically be able to supply voltage levels higher than the open-circuit voltage of a single silicon photodiode (i.e. 0.6 V) for operation of today's CMOS electronic circuits. Hybrid integration of a discrete photodiode with a

small footprint to power a simple LC resonance circuit has been realized [3]. However, this increases the complexity of packaging especially with the wirebonds going from the photodiode die to the electronic unit. Coupling of the fiber optic cable to the photodiode becomes harder with the wirebonds at its center. Furthermore, this unit cannot support more complex electronic circuits which demand power supplies exceeding the photodiode's open circuit voltage. An energy efficient solution to this problem is to connect as many photodiodes as required in series to reach the desired voltage supply level. A hybrid integration example following this approach has been implemented by using a small photovoltaic power cell, which contains three photodiodes in series [1] fabricated in a special technology. Similarly, using a silicon on insulator (SOI) process, as many photovoltaic cells as desired can be connected in series. In this way, a 50 V supply is generated by the series connection of 90 cells [23]. Although, the wirebonds are carried to the edge allowing room for the fiber optic cable placement with this special photovoltaic cell die, the cost of the system is increased and some additional constraints are put on the optical system. Focusing and aligning a laser beam uniformly over an area occupied by three or more photodiodes becomes critical since the current generated by the photovoltaic cell is limited by the smallest current on any one of the photodiodes in series.

A solution to this challenge is to use CMOS photodiodes as solar cells and hence realize a monolithic integration of solar cells and electronic circuits. Unfortunately, CMOS photodiodes cannot be connected in series on the same die [21] except for a special series connection of n-well/p-substrate photodiode and triple-well photodiode in triple-well CMOS processes [2]. However, it is not possible to connect more than two photodiodes in series to generate a higher supply voltage in this case. A novel solution to this problem is to use a single CMOS photodiode connected to a DC/DC voltage converter circuit. A voltage converter circuit can be designed to increase the DC voltage of a single photodiode to the desired voltage supply levels by inserting as many voltage doublers as required. There are no photodiodes connected in series in this solution. A single photodiode formed from diffusion and n-well layers in CMOS has been shown to generate desired voltage levels by using a monolithic DC/DC converter circuit [36]. However, photodiodes formed from the diffusion layers have less efficiency than other possible photodiode configurations in CMOS. Ideally, a photodiode should be able to absorb all the incoming photons in its depletion region. Depths of these regions must be comparable to the

penetration depth of photons in the semiconductor material that the photodiode is made of. Penetration depth is an important parameter in photodiodes indicating the depth below the surface of the semiconductor material, where photon flux is dropped to 37% (1/e) of the surface incident flux. This depth changes with the wavelength of the photons. Penetration depth is around 3 μm for a light source with 650 nm wavelength in silicon [37]. Therefore, a practical junction depth of around 3 μm is desirable in silicon photodiodes to capture photons of 650 nm wavelength efficiently. As a result, in CMOS technology, deeper junctions such as n-well and triple-well are more efficient in collecting photons of visible range wavelength than the shallow n-diffusion or p-diffusion junctions used for Drain/Source implants. Since single n-well/p-substrate photodiode cannot be connected to an electronic circuit on the same die because of the electrical short of the bulk connection, a triple-well photodiode in a triple-well CMOS process connected to a DC/DC converter circuit stands out as a better solution.

The work presented in this chapter is concerned with the realization of a CMOS power supply unit which is composed of integrated silicon photodiodes and a low-voltage DC/DC converter. Novelty of this work can be summarized as the integration of a monolithic photodiode together with a DC/DC converter to generate a micro optical power supply unit by using a standard CMOS foundry process. The proposed design can be integrated with any active CMOS circuitry such as sensors, receivers and transducers for applications where electrically isolated power delivery is necessary. In addition, for routing the optical power to the optoelectronic converter, a micro-machined silicon platform containing an inclined mirror can be implemented, which drastically reduces the problem of coupling the fiber cable to the photodiode.

This chapter is organized in four sections. Section 2.1 describes the system architecture and the operation principle of the system where the relevance of the integration of electronics with a micro-machined platform is discussed. Section 2.2 presents the theory, operation, and performance characterization of sub blocks. System level experimental verification is supplied in Section 2.3 together with the analysis of the feedback mechanism between the integrated photodiode and the DC/DC converter.

2.1 System Architecture

Physical realization of the presented optical power supply system is shown in Figure 2.1 [38]. There are two main blocks for this system, namely CMOS Application Specific Integrated Circuit (ASIC) chip where optical power is translated into its electrical counterpart and a micromachined silicon based platform which serves both as a path for the fiber line and a mirror that reflects the light coming out of the fiber to the photodiodes on the CMOS chip. The work in this thesis is concerned with the design, analysis and implementation of the CMOS chip for converting optical power into electrical power.

In the micromachined silicon platform, which is the work of an M.Sc thesis [39], the front side of the CMOS chip is facing the mirror of the fiber-platform for optimum coupling of the light to the CMOS photodiode. The platform consists of a V-shaped groove for placement of the fiber cable and a mirror with an angle of 54.7 degrees specified by the micromachining process. Integration of the CMOS chip and the fiber-platform is accomplished by injection of epoxy material between the mirror opening and the CMOS chip.

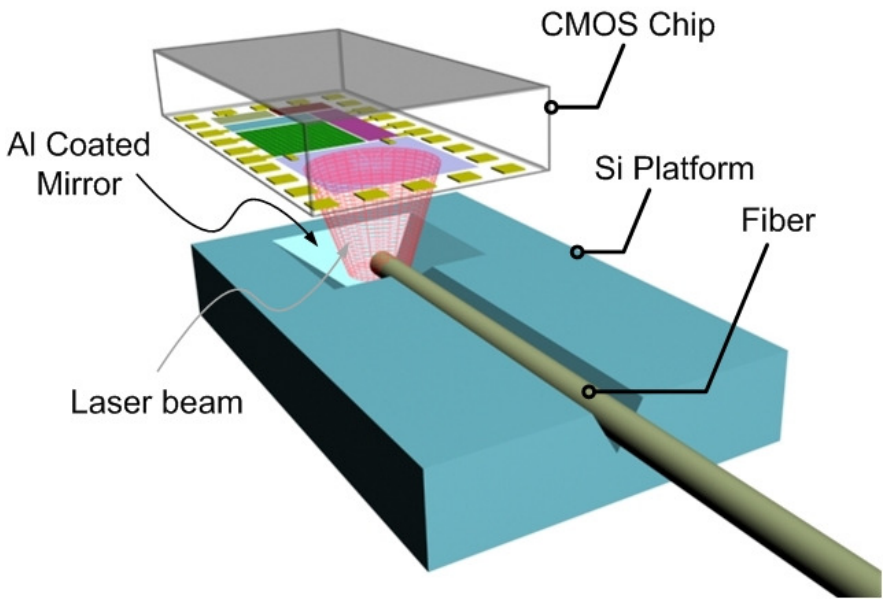

Figure 2.1. Physical realization of the presented optical power supply [38]

Figure 2.2 shows the architecture of the proposed CMOS power supply unit utilized in an electrically isolated micro-scale application. The working principle of the proposed unit can be described as follows; the very low voltage on the photodiode (V_{Ph}) generated by the light from an external laser source serves as the input voltage for the DC/DC voltage converter, where two cascaded stages of voltage doublers driven by two clock signals step up the input voltage to a higher level (V_C) and accumulate the charge on a storage capacitor (C_C). This capacitor is connected to the optical supply unit by using wire bonding, but no interference is induced on operation since fiber cables are safely away from the bond pad of the DC/DC converter output. The accumulated charge can be transferred directly to any electronic system in order for the capacitor to function as a power supply. Besides, transferring the charge through a transmission gate activated by an appropriate control signal (*Enable*) enables supplying more current (I_{DD}) at a voltage level (V_{DD}) for applications powered intermittently [36].

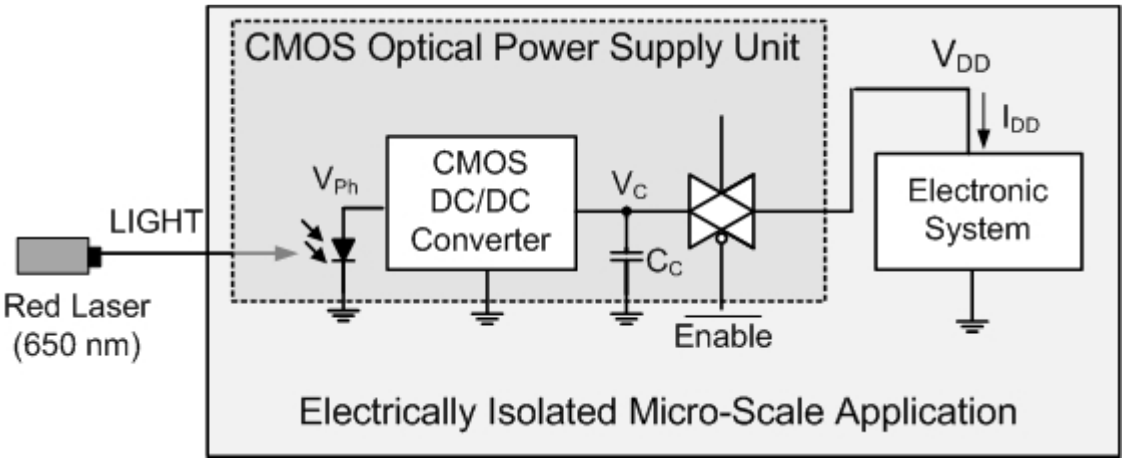

Figure 2.2. The architecture of the proposed CMOS power supply unit

2.2 System Design

2.2.1 Photodiode

Photodiode is a semiconductor device in which a simple p-n junction diode is formed. Basically, a p-n junction converts the photon energy of light into an electrical signal. In fact, a photodiode acts like an ordinary diode but introduces an additive

internally generated current within the junction due to illumination. Photodiodes with increased spectral response and efficiency are designed by specializing basic p-n diodes. For instance, the p-i-n photodiode is a junction diode in which an intrinsic region is inserted between p and n regions to expand the response range. Another type of photodiode, namely avalanche photodiode, increases efficiency by providing a built-in current gain through avalanche multiplication. In each case, the magnitude of the generated current is directly related to the illumination level. Therefore, photodiodes are commonly used for measuring illumination levels or for converting time-varying optical signals into electrical signals. However, this thesis concentrates on extracting electrical power from integrated CMOS photodiodes under illumination. The following subsections discuss the theory of absorption of light in silicon, the operation of semiconductor junction photodiodes, integrated CMOS photodiode implementation issues and experimental verification of the implemented CMOS photodiodes, respectively.

2.2.1.1. Absorption of light in Silicon. When a semiconductor material is exposed to light, the incident photons with energy (E_{ph}) greater than or equal to the band gap energy (E_g) of the semiconductor excite electrons from the valence band to the conduction band, thereby creating free electron and hole pairs (EHPs). The physical basis for this is shown in Figure 2.3. Basically, a photodiode collects a portion of the carrier pairs generated in the material and convert them into an electrical signal so-called photogenerated current.

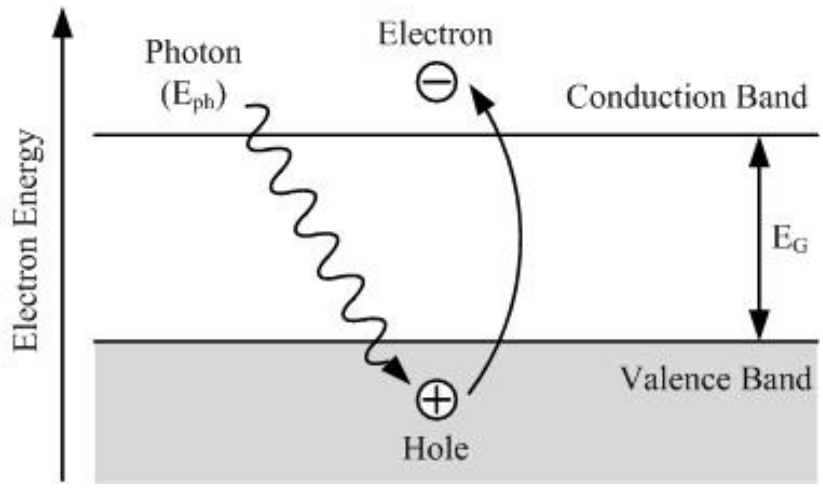

Figure 2.3. The physical basis for the creation of a free electron and a free hole in an intrinsic semiconductor

The band gap energy for silicon is 1.12 eV at room temperature. Since, the energy of photons is inversely proportional to the wavelength; photons with wavelengths above 1100 nm do not have the sufficient energy of 1.12 eV to create EHPs in silicon [40]. Therefore, no electrical signal can be detected in this case. On the other hand, wavelengths below 400 nm generate excess EHPs very close to the surface of the silicon. This is due to the fact that the penetration depth of photons in a material decreases as the wavelength decreases. Therefore, most of the carriers generated by wavelengths below 400 nm do not contribute to the photocurrent due to increased recombination rate at the surface. As a result, a typical silicon photodiode is sensitive to optical wavelengths ranging from 400 nm to 1100 nm.

Light is absorbed exponentially versus depth inside the silicon [41]. The light intensity I in silicon can be given as

$$I = I_0 e^{-\alpha_{optical} x} \tag{2.1}$$

where I_0 is the intensity of light at the surface of the silicon, $\alpha_{optical}$ is the wavelength dependent absorption coefficient, and x is the depth in silicon. Most of the absorption (63%) occurs over a distance of $1/\alpha_{optical}$ which is also called the penetration depth. The absorption coefficient can be approximated for silicon as [42]:

$$\alpha_{\text{optical}} = 10^{13.2-36.7\lambda+48.1\lambda^2-22.5\lambda^3}\ 1/[\text{cm}] \tag{2.2}$$

where the wavelength λ of the light is expressed in μm. Figure 2.4 depicts both the absorption coefficient for silicon and other materials [43]. It is apparent that light signals with shorter wavelength are absorbed close to the surface of the silicon while the ones with longer wavelength penetrate deeper in the substrate. To achieve a photodiode with high speed and good responsivity, the photodiode should be such that most of the photons are absorbed in the depletion region of the photodiode. Hence, an important portion of the generated carriers can be collected to take part in the photocurrent before they recombine with excess carriers in the material. In ideal case, photons should not be absorbed until they have penetrated up to the depletion region and should be absorbed before they penetrate beyond it.

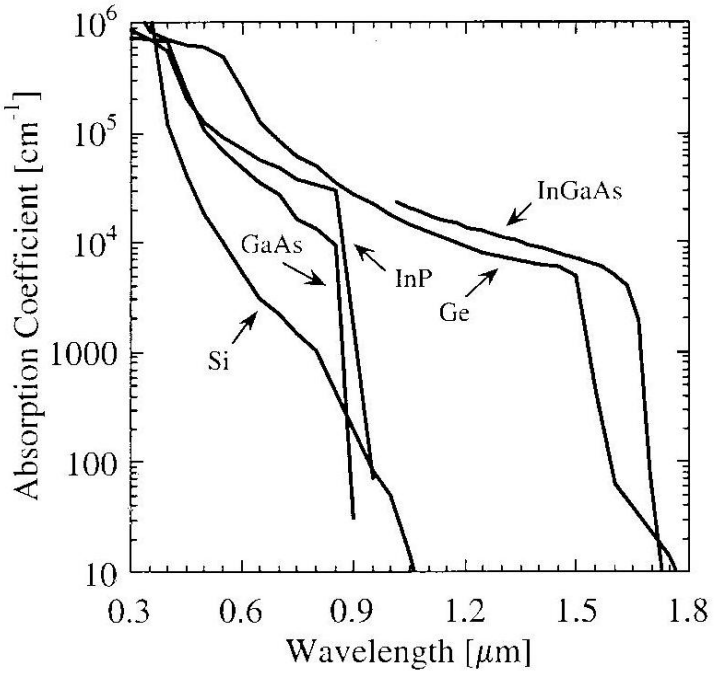

Figure 2.4. Optical absorption coefficient versus wavelength for Si and other materials [43]

2.2.1.2. Operation of Photodiode. The basic principle of operation of a photodiode is as follows. Upon illumination of a p-n junction, incident photons with sufficient energy level ($E_{ph} \geq E_g$) generate electron-hole pairs both in the depletion and neutral regions. Since, the depletion region contains ionized or depleted atoms that create a built-in voltage difference (an internal energy barrier) across the junction, the intrinsic electric field causes the electrons and holes to separate and drifts them in opposite directions, thereby giving rise to a photocurrent in the external circuit. The carriers generated in the neutral regions, but within one diffusion length of either side of the depletion region, diffuse into the depletion region and also get collected across the junction. However, due to the slow diffusion process in the neutral regions, these carriers add a tail to the time response of photodiode. Figure 2.5 illustrates the photocurrent flow consisting of diffusion and drift currents in a p-n junction photodiode [41].

A photodiode can be operated in two modes depending on the application specific requirements. They are referred to as photoconductive mode and photovoltaic mode. Generally, the photoconductive mode is used for photo sensing applications. In this mode, the photodiode is reverse biased such that a positive voltage is applied to the n-side of the p-n junction relative to the p-side. Therefore, the width of the depletion region increases to

encompass more of the semiconductor bulk material within the electric field. This reduces the carrier transit time due to an increased electric field at the junction. Further, the junction capacitance is reduced as it is inversely proportional to the width of the depletion region. This improves the speed of response and linearity of the devices at the expense of increased noise current level. The details of the characteristics will not be discussed in this thesis but readers are referred to [41] and [44].

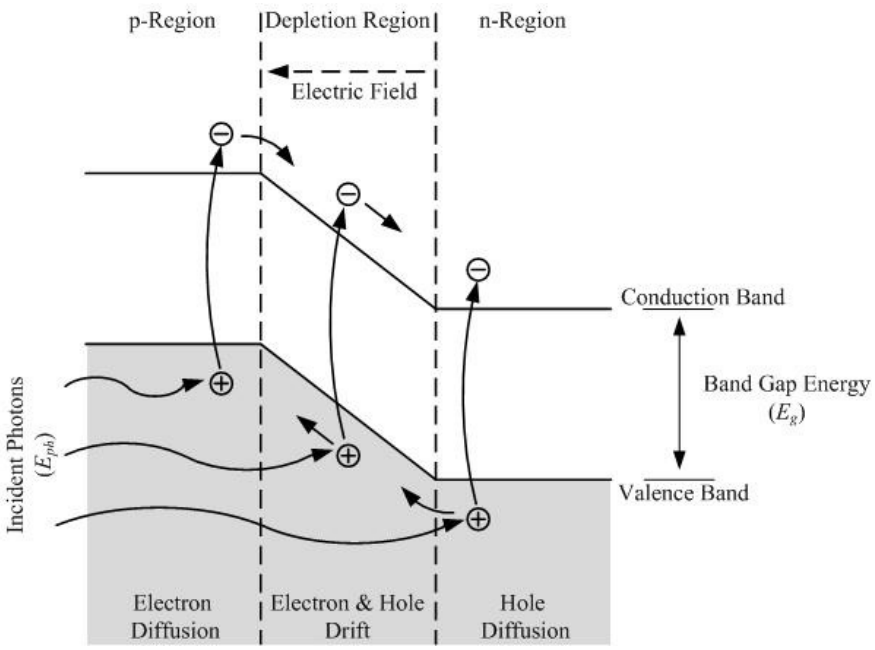

Figure 2.5. The photocurrent flow in a p-n junction photodiode [41]

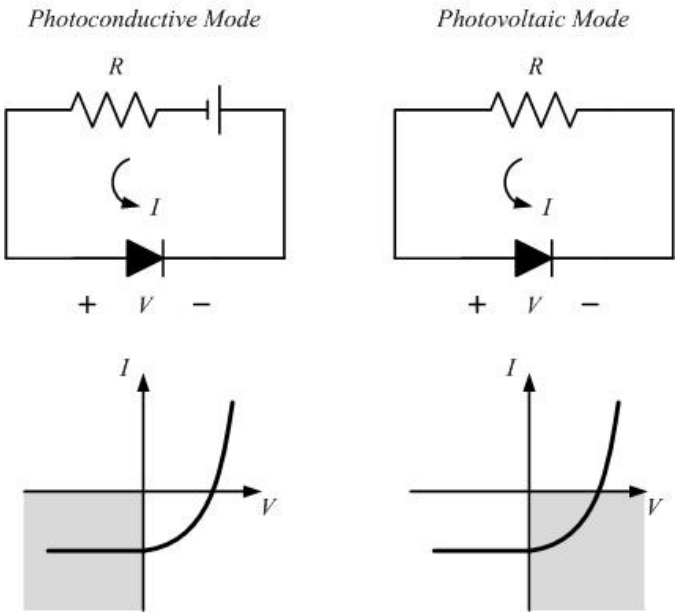

Figure 2.6. The operation modes of an illuminated photodiode

This thesis mainly focuses on operating photodiodes in photovoltaic mode for converting optical power into electrical power. In photovoltaic mode, the photodiode is connected without a bias voltage to a load resistance for supplying photocurrent. Figure 2.6 illustrates both modes of operation together with the *I-V* characteristics of the photodiode. In photoconductive mode, the photodiode is operated in the third quadrant of its *I-V* characteristic where it responds much more linearly to changes in light intensity. Since, the current and junction voltage are both negative in this quadrant, the power is delivered to the device from the external circuit. To deliver power from the photodiode to the external circuit, the photodiode is operated in the fourth quadrant of its *I-V* characteristic, where the current is negative and junction voltage is positive.

The generated photocurrent in a photodiode for a given optical power is related to the quantum efficiency, $\eta_{quantum}$, which is defined as the average number of carrier pairs generated and collected per incident photon. Even when all the incident photons are absorbed without reflection from the surface of the device, the quantum efficiency is always less than unity due to the fact that not all of the generated carrier pairs can be collected within the depletion region. Actually, the quantum efficiency depends on the absorption coefficient, $\alpha_{optical}$ of the semiconductor at the wavelength of interest and on the structure of the photodiode device, mainly the depth and the width of the depletion region. Quantum efficiency can be increased by reducing reflections at the photodiode surface, increasing the absorption within depletion region, and preventing recombination of carrier pairs before they are collected. The quantum efficiency for a photodiode can also be defined as

$$\eta_{quantum} = \frac{I_{ph}/q}{P_0/h\nu} \tag{2.3}$$

where I_{ph} is the measured photocurrent, q is the electronic charge, P_0 is the incident optical power, and $h\nu$ is the energy of a single photon. Another related performance characteristic of a photodiode is the responsivity, which is defined as the photocurrent generated (I_{ph}) per incident optical power (P_0).

$$Responsivity = \frac{I_{ph}}{P_0} \tag{2.4}$$

According to the definition of quantum efficiency in equation (2.3), the responsivity, R_λ can also be expressed as

$$R_\lambda = \frac{\eta_{quantum} q}{h\nu} = \frac{\eta_{quantum} \lambda}{1.24} \; [A/W] \tag{2.5}$$

where the optical wavelength λ is expressed in μm. Therefore, the responsivity clearly depends on the wavelength. Ideally, with a quantum efficiency of 100% (η=1), the responsivity should increase linearly with the wavelength, λ. In practice, however, η is less than unity and limits the responsivity to lie below its ideal characteristic (η=1) with upper and lower wavelength values. Figure 2.7 depicts the responsivity of a typical silicon photodiode together with its ideal characteristic (η=1) as a function of the wavelength [40]. It is important to note that the responsivity decreases more rapidly in the short wavelength region (λ<500nm). This is due to the shallow penetration depth of photons, which lead to a higher surface recombination rate. For large wavelengths (λ>850 nm), the responsivity also decreases; the photons penetrate deep into the substrate and the generated carrier pairs recombine with majority carriers. As seen in Figure 2.7, the responsivity of a silicon photodiode is highest for wavelengths ranging from 600 to 800 nm due to the fact that the carrier pairs are generated near the depletion region of the photodiode junction.

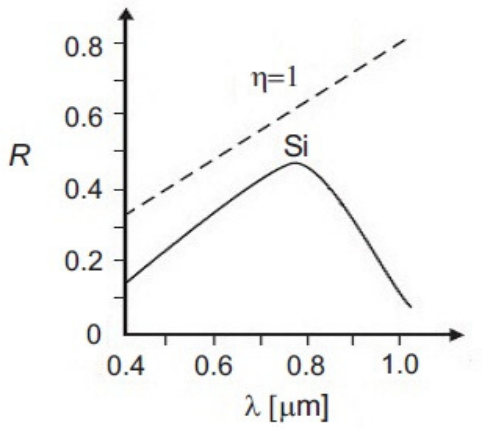

Figure 2.7. The responsivity of a typical silicon photodiode together with its ideal characteristic (η=1) [40]

2.2.1.3. Integrated CMOS Photodiodes. Today, silicon CMOS is an inexpensive and mature fabrication process that is widely used for the realization of high-density and low-power microelectronic circuits. Incorporating an optical functionality into CMOS chips through integration of photodiodes with active circuitry on the same substrate introduces important benefits for optoelectronic systems such as reduced packaging costs, better noise immunity and higher integration capability. To date, III-V semiconductor compounds have been the mostly preferred materials for fabricating photodiodes due to their lower band gap energy and higher mobility, thus leading to higher responsivity and higher bandwidth photodiodes. However, these photodiode technologies are costly and non-standard processing steps are necessary to provide a solution containing both the photodiode of III-V semiconductor compound and active CMOS circuitry on the same substrate [31,45,46].

Instead, a standard CMOS technology can be exploited for obtaining integrated photodiodes. The major disadvantage of these photodiodes in standard CMOS is that this technology is not optimized for optical devices. Basically, the relatively small depletion widths of integrated photodiodes result in a lower efficiency than those of commercial photodiodes. The efficiency is even lower in the newer sub-micron CMOS technologies due to further reduced depletion widths. In a typical 0.18 µm CMOS process, the depth of n-well or p-well is only about 1.2 µm while the penetration depth of photons with wavelength of 650 nm in silicon is around 3 µm. Although, this might be compensated by modifying the technology, the resulting increase in cost may be unacceptable for large scale systems.

The proposed work in this thesis aims to use integrated photodiodes in a standard unmodified sub-micron CMOS process as optical-to-electrical converters. The limited efficiency of these photodiodes is compensated by an important advantage. The integration of a photodiode on the same substrate with active CMOS circuitry results in a low-cost system with an enhanced yield. Further, utilization of a sub-micron CMOS process introduces the capability for the integrated system to be used in increasingly miniaturized electronic devices [25-29].

Any standard CMOS technology can be exploited for obtaining integrated optoelectronic converter for low power applications [47]. As an example let us consider a

triple-well CMOS process, where both twin-well and triple-well field-effect transistors (FETs) are implemented on the same p-type substrate as shown in Figure 2.8 [38]. There are essentially two types of FETs offered in such a technology: (1) low-threshold voltage transistors, marked as twin-well nMOS and twin-well pMOS in Figure 2.8 and (2) standard MOS transistors exemplified as triple-well nMOS transistor in Figure 2.8. It is obvious that low-voltage applications require low-threshold transistors to allow sufficient headroom for electrical signals. Therefore, the DC/DC converter is implemented by using low-threshold voltage (twin-well) MOS transistors. Drain/Source diffusions of MOS transistors are known to be photo sensors with low efficiency and they can be used as CMOS imagers. Because of their relatively low efficiency, they do not represent a suitable way of obtaining power for electronic circuits [48].

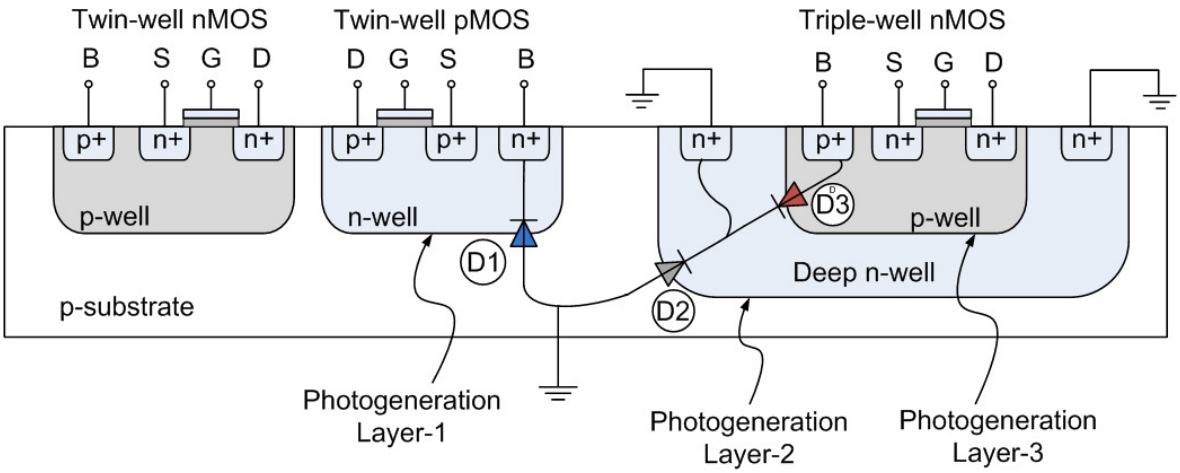

Figure 2.8. Cross section of the triple-well CMOS process [38]

Inspection of Figure 2.8 reveals three types of p-n junctions that can be used as effective photogenerated current sources. The first p-n junction marked as D1 forms a photogeneration layer between the n-well diffusion and the p-type substrate. This type of diode is referred to as n-well photodiode in this thesis. The second type of photodiode, marked as D2 in Figure 2.8, is between the deep n-well and the p-type substrate having a common anode port with D1. D2 is referred to as a parasitic photodiode for the reasons that will be explained shortly. Finally, the third photodiode, shown as D3, is the junction between the p-well and the deep n-well which is isolated from the p-type substrate. This type of diode is referred to as triple-well photodiode in this thesis. As n-well photodiodes

have a common anode connection through p-type substrate, it is not possible to tie them in series to increase the overall voltage.

As can be seen in Figure 2.8, low-threshold voltage transistors share the same substrate which serves as the anode of the n-well photodiode (D1). When this diode is used in photovoltaic mode to induce a positive voltage drop between the anode and the cathode terminal, the input of the DC/DC converter circuitry is effectively grounded. Therefore, it is not possible to boost the voltage of the photovoltage with the combination of an n-well photodiode and a DC/DC converter, if implemented by using twin-well transistors.

Triple-well photodiode (D3) and deep n-well photodiode (D2) have common cathode connection. During the normal operation of D3, the junction between the deep n-well and p-well diffusion of the triple-well transistor is illuminated, which means that the junction between the deep n-well and the substrate receives light as well. As a result, whenever D3 is optically turned on, D2 turns on too, acting as a parasitic photodiode, which steals the useful photo induced current of D3. As a solution, p-type substrate and the n+ contact diffusion of the deep n-well are shorted at the ground potential, which avoids current to be stolen from D3. Because of the necessity to tie the cathode of D3 to ground level, it is not possible to have a series connection of triple-well photodiodes. Although it is allowed to tie n-well (D1) and triple-well (D3) photodiodes in series, this connection puts a severe restriction to the usage of triple-well nMOS transistors [2].

2.2.1.4. CMOS Implementation & Measurement Results. To confirm the preceding considerations in practice and evaluate the feasibility of integrated photodiodes in a sub-micron CMOS process, a number of n-well and triple-well photodiodes have been implemented on a test chip fabricated using UMC 0.18 µm CMOS technology with no process modification. Figure 2.9 shows a micrograph of the test chip. The integrated photodiodes are all squares with a photosensitive area of approximately 300×300 μm^2.

The width of the depletion region for an integrated photodiode decreases with the minimum feature size in sub-micron CMOS technologies. Therefore, the percentage of the photons that are absorbed in the depletion region of the photodiode is reduced together with the device's dimensions and a large number of carrier pairs are generated outside the

depletion region. An alternative solution to this problem is to use the side-walls of deeper junctions such as n-well or triple-well. Actually, the depletion region is still thin but the depth of these wells perpendicular to the surface is larger. Since, the largest dimension of the well is parallel with the incoming light, a larger fraction of the photons are absorbed in the depletion region.

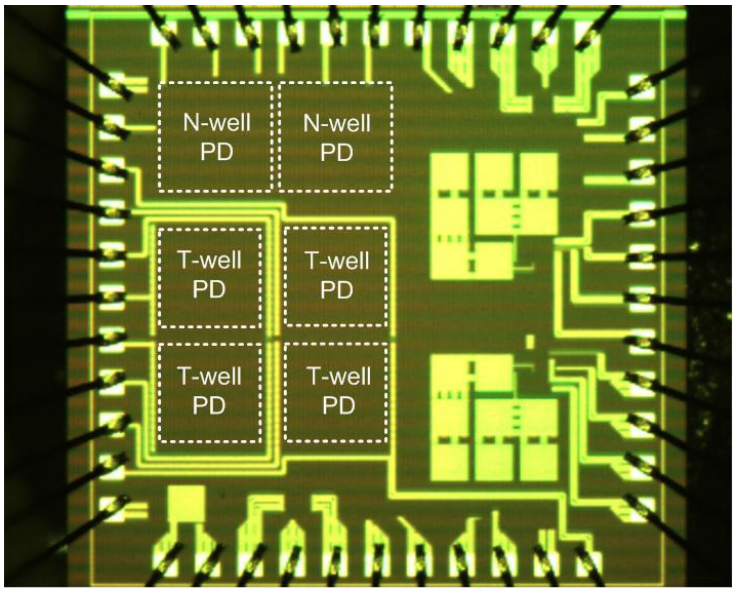

Figure 2.9. A micrograph of the CMOS integrated photodiode chip

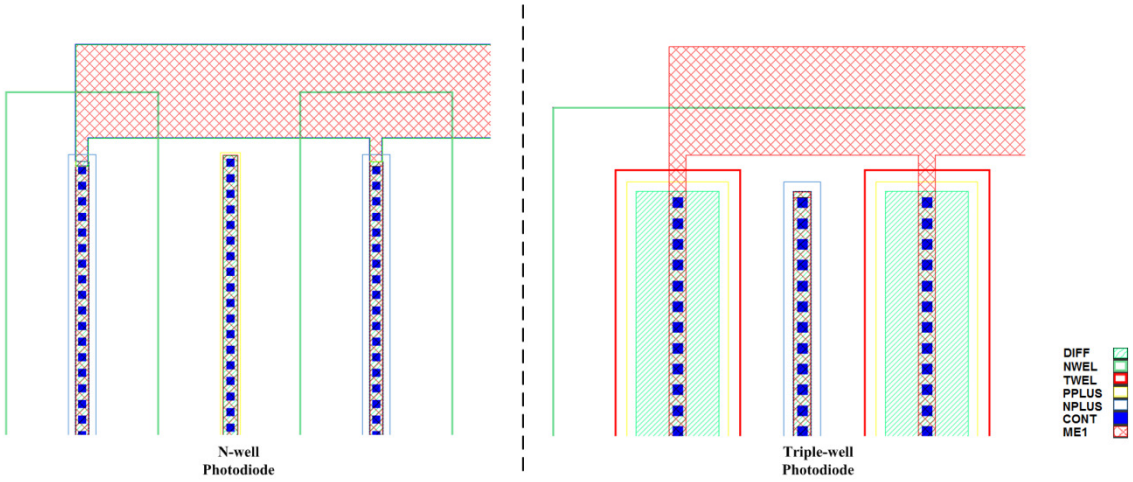

Figure 2.10. A part of the layouts for the integrated photodiodes

A part of the layouts for the implemented n-well and triple-well photodiodes is shown in Figure 2.10. In the n-well photodiode, a sequence of parallel n-well strips and p^+-substrate strips covers the complete area, whereas the triple-well photodiode consists of a

sequence of parallel p-well strips and n^+-contact strips inside a rectangular deep n-well diffusion. All of the strips in the photodiodes are connected to overlying metal paths over their complete length. Relatively small widths have been used for both n-well and p-well strips in the layout to increase the amount of side-wall junctions in the photodiodes.

Using the fabricated integrated circuit (IC) die, n-well and triple-well photodiodes have been characterized. The measurements are meant to demonstrate the practical usability of the devices rather than to provide their extensive physical characterization. The current-voltage characteristics of n-well and triple-well photodiodes have been measured with a semiconductor parameter analyzer (Keithley SCS4200) using the optical set-up shown in Figure 2.11 (built in Bogazici University Micro Nano Characterization Laboratory). Basically, a laser beam at a wavelength of 650 nm is focused on photodiodes using a convex lens (Edmund Optics, f=75 mm, diameter 25 mm) at different power levels such that the spot sizes are smaller than their areas. Each optical power level (P) applied to photodiodes after focusing is measured with an optical power meter (Thor Labs PM100A with sensor S12C).

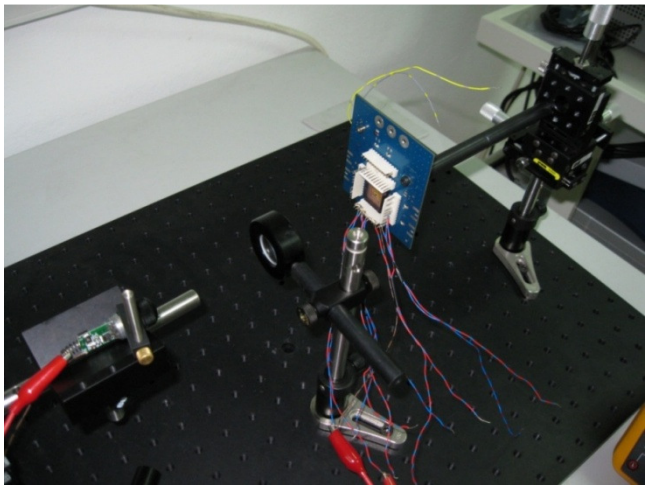

Figure 2.11. Optical set-up for focusing the laser beam onto the CMOS integrated photodiode chip

The current-voltage characteristics of the n-well photodiode at different optical power levels define the efficiency of the photodiode to convert optical power into electrical power. Even though n-well photodiode has an area of 300 µm × 300 µm, because of the dummy metal patterns with gaps automatically placed on the photodiodes for the

uniformity of the metallization process at the foundry, the effective area of the photodiode is reduced. Initial tests have been done on n-well photodiodes covered with metal patterns. These characteristics are shown in Figure 2.12(a). A short-circuit current of around 0.93 mA is achieved from an optical power of 80 mW. The fill factors (FF) related to this characterization varies between 0.769 and 0.664 as the optical power is swept between 40 mW and 160 mW. The reason for the fill factor variation with respect to the power of the illumination is the reduction of the equivalent shunt resistance and the increase in the equivalent series resistance of the photodiode with increasing optical power level.

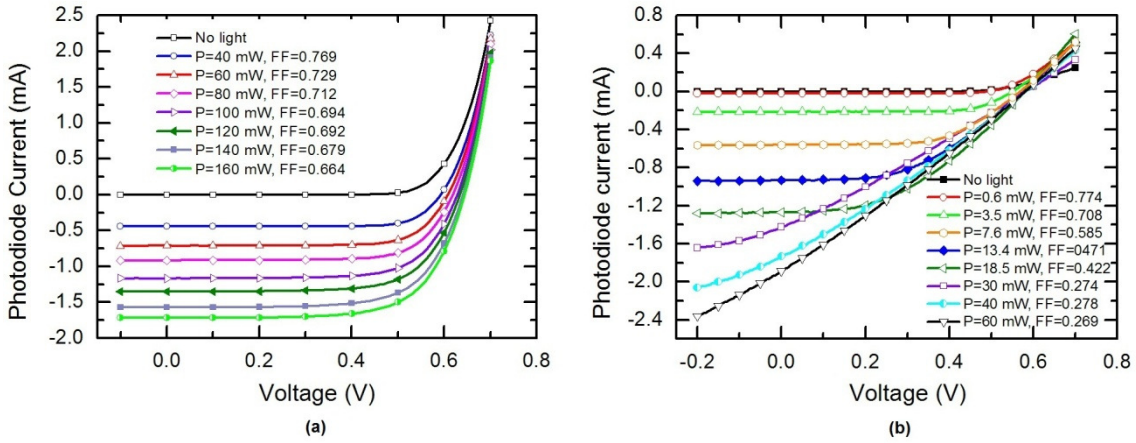

Figure 2.12. Current-Voltage characteristics and fill factor (FF) values of (a) metal covered (b) uncovered n-well photodiode illuminated with a laser by varying the optical power (P)

However, these results do not represent the full capacity of the n-well photodiode since they are mostly covered with metal patterns. These patterns are formed by the topmost four aluminum layers (Metal-3,4,5 and 6) of the UMC 0.18 µm CMOS process. Basically, the incident beam must pass from the air through these metal layers before it reaches the photodiode. Due to the reflection losses, the optical efficiency of the device, which can be defined as the percentage of incident photons onto the chip's surface reaching the photodiode, is reduced. A previous work utilizing a photodiode covered with a periodic metal grating structure measured a maximum optical efficiency of 53% [49]. However, the calculation of optical efficiency for a photodiode covered with a metal structure on top is quite challenging and involves solving coupled-wave equations [21].

In order to measure the maximum capacity of this photodiode, metal layers over the n-well photodiode were removed by in-house wet chemical etching. Figure 2.12(b) shows the current versus the voltage between the terminals of the n-well photodiode after the dummy metal patterns are removed. In these results, the photodiode goes into light saturation at tested optical power levels greater than 30 mW, and the current-voltage characteristics above this power level show an irregular behavior. Above the light saturation level, the current is no longer proportional to the received optical power and the series resistance of the photodiode starts to be dominant. As a result of the voltage drop over this series resistance component, a more linear characteristic between the applied voltage and resulting diode current is observed. The current of the photodiode does not increase much as the optical power is increased beyond this level. The fill factor of this device is extracted to be between 0.774 and 0.269, for the optical power levels between 0.6 mW and 60 mW, due to severe changes in the shunt and series resistances. A short-circuit current of 0.91 mA is achieved from an optical power of 13.4 mW indicating a responsivity of 0.068 A/W. Thus, removing the metal patterns over the n-well photodiode increases its capacity by a factor of 6 meaning that metal patterns over the photodiode reduces its area to $1/6^{th}$ (122 μm × 122 μm). That is why the metal covered n-well results in Figure 2.12(a) do not show any saturation even at measured optical power of 160 mW.

Measuring this factor experimentally is important because the triple-well photodiode is also covered with metal patterns. The reduction in triple-well photodiode current due to metal layers puts an important constraint on DC/DC converter operation and the electronic units supplied by it. Future implementations would require more electrical power. In that case, triple-well photodiodes without any metal coverings must be used and electronic circuits powered by these photodiodes must be optimized based on the current-voltage characteristics of these photodiodes at specific optical powers.

The triple-well photodiode on the chip is one of the most important elements of the system, since it allows integration of other circuitry (DC/DC converter in this case) on the same die. Even though the triple-well photodiode used to power the DC/DC converter circuit consumes an area of 300 μm × 300 μm, it can be deduced from the experimental results of n-well photodiodes that the effective area is reduced to 122 μm × 122 μm due to the dummy metal patterns put on top of them at the foundry.

While determining the current through the triple-well photodiode, the cathode of the photodiode, deep n-well and the p-substrate are shorted to eliminate the effects of the parasitic current due to deep n-well/substrate junction (D2) in Figure 2.8. During the measurements, optical power of the laser is varied from 40 mW to 200 mW with a step value of 40 mW. Results of the measurements are shown in Figure 2.13, where both parasitic current (I_{PAR}) due to D2 and the useful photodiode current (I_{PD}) of D3 are plotted. Generated photodiode current increases linearly with the optical power level of the illumination. These current levels permit the DC/DC converter to function properly with an efficiency around 50 %. At 200 mW of incident light power, 0.85 mA of photodiode current is measured, indicating a responsivity of 0.0043 A/W. From the results of the n-well photodiode covered with metal patterns, it is extrapolated that the same photo current can be generated at an optical power of around 33 mW, indicating a responsivity of 0.026 A/W. This implies that n-well photodiodes are roughly 2.5 times (at high optical power levels) to 3.8 times (at low optical power levels) more efficient than the triple-well photodiodes. The triple-well photodiode current is lower than the n-well photodiode current measured at the same optical power levels, mainly due to the regions where photo-generation occurs. This is expected since the junction depth of the n-well photodiode is deeper than the junction depth of the triple-well diode. The reason for the variation of the efficiency difference between these two photodiodes is that the n-well photodiode enters into saturation regime more rapidly than the triple-well diode.

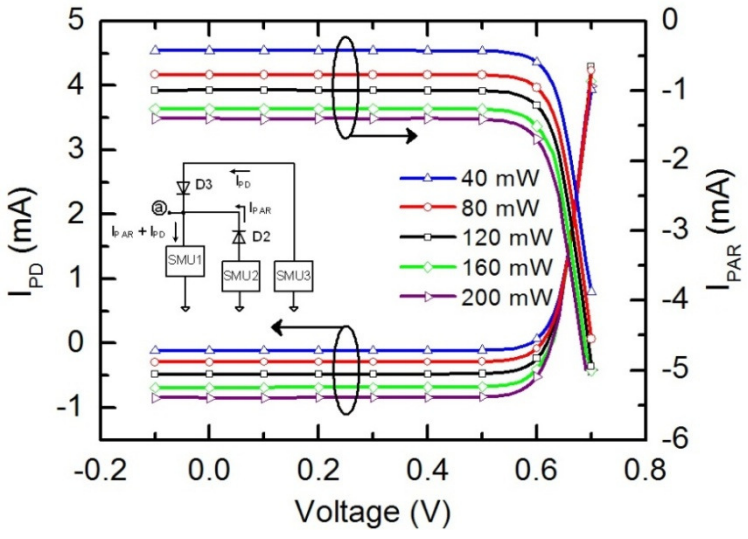

Figure 2.13. Current-voltage characteristics of the parasitic photodiode (D2) and the metal covered triple-well photodiode (D3) at different optical power levels of illumination.

2.2.2 DC/DC Converter Circuit

The challenges mentioned in Section 2.2.1.3 leave only one option to implement an integrated optoelectronic power unit, usage of triple-well photodiode together with a DC/DC converter, realized by low threshold voltage transistors. Integrated DC/DC voltage converters are used to provide a voltage that is higher than the available power supply voltage. Since, the input voltage of the DC/DC converter is provided from a triple-well photodiode, designing a DC/DC converter capable of operating at low voltage levels between 0.5 V-0.65 V is essential for the proposed power supply unit.

Basically, there are two main topologies for DC/DC converters, namely the Dickson charge pump [50] and voltage doubler circuits [51-54]. Due to the body effect, the gain of the Dickson charge pump circuit reduces greatly for low input voltages. Hence, it is not appropriate to use this topology in the proposed design.

The voltage doubler structure [51] has an important advantage over the Dickson charge pump for boosting low-voltages. The fact that the voltage drop across any device never gets larger than the supply voltage enables using low threshold voltage MOS transistors which is very essential for low voltage applications. Further, the usage of low voltage devices allows the circuit to be operated at higher frequencies due to their relatively smaller parasitic capacitances, leading to a smaller silicon area occupation with better power efficiency [55].

2.2.2.1. Operation Principle. Figure 2.14 shows the architecture of the DC/DC converter used in the proposed module. The converter has two main parts; The first part consists of two cascaded stages of voltage doublers, while the second part is the clock generator circuit which is a simple ring oscillator followed by two buffer circuits to drive the high capacitive load of MOS transistors in the voltage doubler circuitry. The input voltage to the DC/DC converter (i.e, the voltage of the photodiode, V_{Ph}) serves as the power supply voltage (V_{DD}) for both the voltage doubler and the clock generator circuits.

As can be seen in Figure 2.14, a single stage of a voltage doubler consists of a pair of storage capacitors, C_1 and C_2, a pair of cross-connected nMOS transistors, M_1 and M_2,

used as switches to charge the storage capacitors, and a pair of pMOS transistors, M_3 and M_4, used as transfer elements. The operation of the circuit for the first stage under no-load conditions can be explained as follows. After the initial transient; when clock signal CLK is high and $\overline{CLK}$ is low, M_1 and M_4 are turned on and M_2 and M_3 are turned off. In ideal case, C_2 is charged to V_{DD} through M_1 and the output of the first stage is charged to $2V_{DD}$ through M_4. When clock signal CLK is low and $\overline{CLK}$ is high, M_2 and M_3 are turned on and M_1 and M_4 are turned off. Hence, C_1 is charged to V_{DD} through M_2 and the output node is again charged to $2V_{DD}$ through M_3.

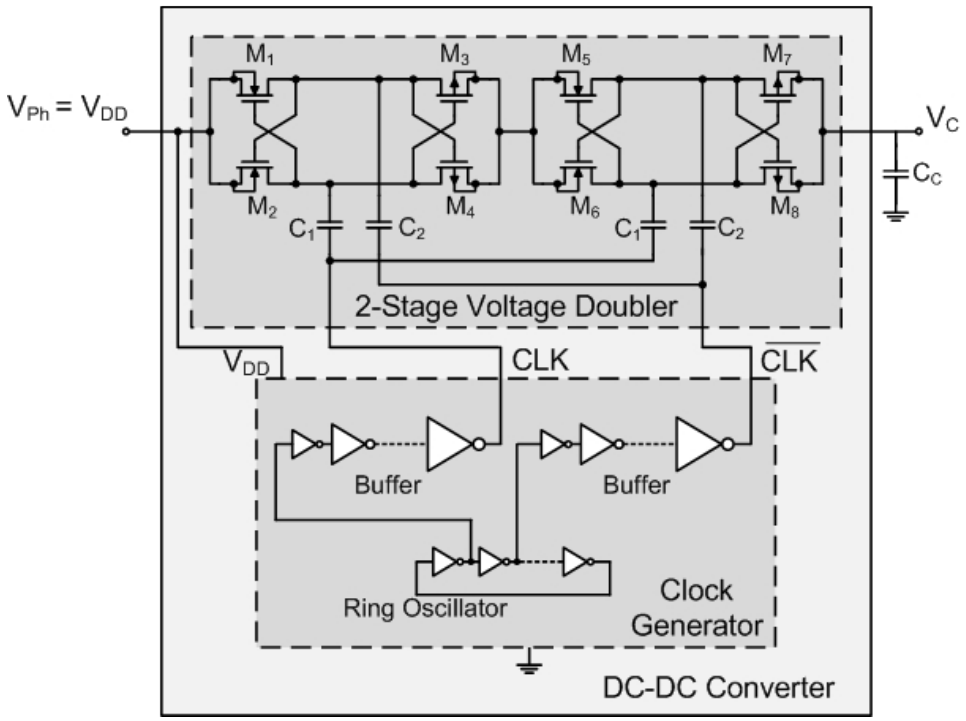

Figure 2.14. The architecture of the CMOS DC/DC Converter

As a result, the voltage at the output node of the first stage is $2V_{DD}$ for the entire period of the clock. In ideal case, a single stage provides a voltage increase of V_{DD} which is actually equal to the voltage of the photodiode, V_{Ph} in the proposed system. Hence, a sufficient number N of voltage doubler stages can be cascaded in order to obtain the required voltage which is ideally equal to $(N+1)V_{Ph}$.

2.2.2.2. Power Efficiency Analysis & Optimization. One of the most important figures of merit for DC/DC converters is the power efficiency [55]. The power efficiency, η of a

DC/DC converter is defined as the ratio between the power P_{out} delivered to the load and the power P_{in} drawn from the supply V_{DD}. The input power P_{in} is equal to the sum of output power, P_{out} and the overall power losses P_{loss} in the converter. Therefore, the power efficiency, η can be expressed as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{2.6}$$

The overall power loss, P_{loss} in the DC/DC converter topologies is composed of two main parts; namely, resistive power losses P_{res} and dynamic power losses P_{dyn}. The resistive power loss is basically due to the finite value of the output resistance of the converter, whereas the dynamic power loss is due to the switching frequency and the overall parasitic capacitance of the converter. In order to maximize the converter's efficiency for a desired current capability, the switching frequency which is controlled by the clock frequency must be selected carefully. Actually, an optimal value exists for the clock frequency so that the power loss is minimized. A higher switching frequency than an optimal value decreases the efficiency of the converter due to increased dynamic power losses. The value of stage capacitors and the number of stages necessary to generate the required voltage play an important role in determining the overall area of the DC/DC converter. As a result, the overall area of the converter which is mainly dictated by the value of stage capacitors can be decreased by increasing the clock frequency. However, increasing the clock frequency further beyond the optimal value decreases the power efficiency [56,67].

An *N*-stage voltage doubler can be modeled as a voltage source with an open-circuit output voltage ideally equal to $(N+1)V_{DD}$ and a series output resistance of $R_{out,id} = N/fC_{st}$ where f is the clock frequency and, C_{st} is the stage capacitance. C_{st} is equal to 2C in the case C_1=C_2=C. With these assumptions, the resistive power losses, P_{res} can be given by $R_{out,id}{I_{out}}^2$ while the dynamic power losses, P_{dyn} are considered to be equal to $k_{sw}NfC_{par}{V_{DD}}^2$, where C_{par} is the sum of parasitic capacitances in one stage, and k_{sw} is a coefficient which is simplified as the ratio between the voltage swing across any parasitic capacitance and the supply voltage, V_{DD}. Using the relations given above, the power efficiency can be expressed as,

$$\eta = \frac{P_{out}}{P_{out} + P_{res} + P_{dyn}} = \frac{V_{out}I_{out}}{V_{out}I_{out} + R_{out,id}{I_{out}}^2 + k_{sw}Nf C_{par}{V_{DD}}^2} \tag{2.7}$$

where $V_{out}$and I_{out} are the mean values of the output voltage and the output current over a clock period. The product $V_{out}I_{out}$ is the mean power delivered to the load by the voltage doubler circuit.

The overall parasitic capacitance C_{par} per each stage consists of two contributions; C_{top}, associated to the top plate of the stage capacitance, and C_{bot} associated to the bottom plate of the same capacitance. Actually, C_{top} and C_{bot} include all the parasitic contributions in each stage and they can be seen as a fraction of the stage capacitance, C_{st}; $C_{top} = \alpha_T C_{st}$ and $C_{bot} = \alpha_B C_{st}$. The values of α_T and α_B depend on the stray capacitances of the storage capacitors, the parasitic capacitance of MOS transistors in the voltage doubler circuit, and the output parasitic capacitance of the clock generator circuit.

In ideal case, the output voltage of a voltage doubler can be expressed as

$$V_{out} = V_{DD} + NV_{DD} - R_{out,id}I_{out} \tag{2.8}$$

From equation (2.8), it is obvious that the voltage gain can be given by *N+1* when there is no current loading ($I_{out} = 0$) at the output of the circuit. However, the voltage gain per stage, and consequently the overall voltage gain decrease when parasitic effects are taken into account. To be more specific, top plate parasitic capacitance C_{top} associated to each stage leads to a division of the voltage applied from the buffer circuit to the bottom plate of storage capacitors. Hence, the voltage increment per stage, ΔV_{st} can be given as,

$$\Delta V_{st} = \left(\frac{C_{st}}{C_{st} + C_{top}}\right) V_{DD} = \frac{1}{1 + \alpha_T} V_{DD} \tag{2.9}$$

The value of the effective output resistance is also affected by the top plate parasitic capacitance and can be expressed as,

$$R_{out} = \frac{N}{f\left(C_{st} + C_{top}\right)} = \frac{1}{(1 + \alpha_T)} \cdot R_{out,id} \tag{2.10}$$

Therefore, the output voltage of a voltage doubler with the effects of parasitic capacitance can be given as [58]

$$V_{out} = V_{DD} + N\Delta V_{st} - R_{out}I_{out} = V_{DD} + \frac{1}{1 + \alpha_T}\left[NV_{DD} - R_{out,id}I_{out}\right] \tag{2.11}$$

Since, the DC/DC converter is supplied from an illuminated photodiode in the presented system shown in Figure 2.14; the supply voltage V_{DD} and the output voltage V_{out} in (2.11) is actually equal to the voltage of the photodiode, V_{Ph} and, the voltage of the output capacitor, V_C respectively. The DC/DC converter is designed to supply an output voltage, V_{C} of 1.2 V with a current capability, I_{out} of 0.3 mA. In order to guarantee these specifications, a worst case photodiode voltage, V_{Ph} of 0.5 V has been taken as the input voltage parameter for the design of the converter. In order to obtain both a small die area and high power efficiency, a relatively high clock frequency of 50 MHz and a total of two stages have been selected for the proposed design. The required stage capacitor, C_{st} has been calculated from equation (2.11) as 40 pF with a reasonable assumption that its value is considerably large compared to the top plate parasitic capacitance, C_{top} ($\alpha_T \ll 1$) for the cascaded voltage doublers.

By using the relations in (2.10) and (2.11), the power efficiency of the DC/DC converter may also be expressed as,

$$\eta = \frac{V_{DD}I_{out}\,(N + 1 + \alpha_T)/(1 + \alpha_T) - R_{out,id}{I_{out}}^2/(1 + \alpha_T)}{V_{DD}I_{out}\,(N + 1 + \alpha_T)/(1 + \alpha_T) + (\alpha_T + \alpha_B)k_{sw}Nf{C_{st}}{V_{DD}}^2} \tag{2.12}$$

The analytical calculations from (2.12) show that the power efficiency increases until the clock frequency reaches about 50 MHz for the presented design. When the clock frequency is increased further, the power efficiency decreases. Figure 2.15 illustrates the optimization plot of DC/DC converter efficiency versus clock frequency based on equation (2.12) when coefficients α_T and α_B are taken into account. The power efficiency at the

clock frequency of 50 MHz has been calculated as 63.7% for a typical photodiode voltage ($V_{Ph} = V_{DD} = 0.6\,V$).

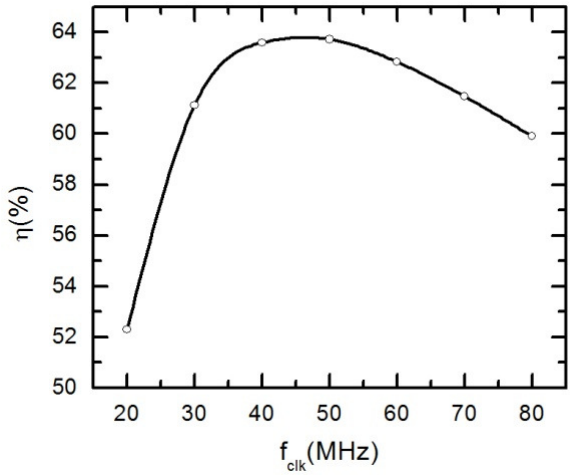

Figure 2.15. The optimization plot of the DC/DC converter efficiency versus clock frequency

In addition, the power efficiency characteristic for the designed DC/DC converter, which consists of two cascaded stages of voltage doublers with a storage capacitance per stage equal to 40 pF ($V_{DD} = 0.6\,V,\ f = 50\,MHz$) has been analyzed for different output current loadings. Figure 2.16 illustrates the calculated power efficiency characteristic of the DC/DC converter versus the output current. The calculations show that the efficiency peaks at an output current around 0.3 mA.

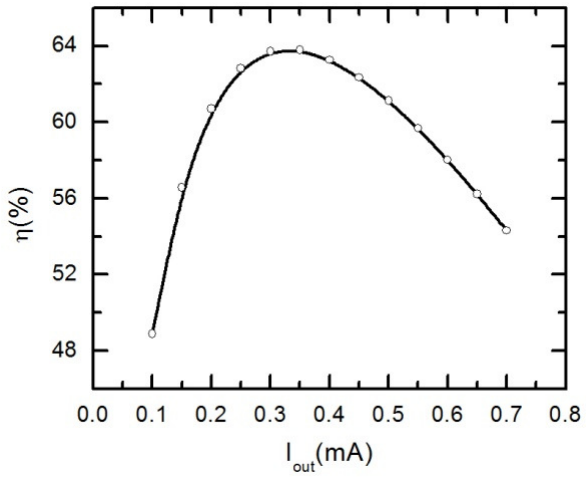

Figure 2.16. The efficiency of the DC/DC converter versus output current

2.2.2.3. Simulation Results. To illustrate the previous considerations, two basic simulations have been performed for the designed circuit with Eldo using the electrical parameters of UMC 0.18 µm CMOS process. Figure 2.17 shows the power efficiency characteristic simulated with Eldo and the theoretical relation given by using (2.12).

It is important to note that the theoretical model gives quite good agreement with the simulated characteristic for output currents up to 0.3 mA, although the quantitative agreement is not particularly good which is due to the fact that the resistances of the MOS switches have not been taken into account in the model. However, the MOS transistors leave their triode operating region, and start to work in saturation for output currents higher than 0.3 mA, thereby increasing their on-resistances. As a result, the simulated efficiency decreases and the theoretical model does not follow the simulated characteristic for high output currents. In order to confirm this, the output characteristic of the circuit simulated with Eldo and the voltage-current characteristic calculated by using (2.11) is also given in Figure 2.18. It is obvious that the slope of the characteristic significantly increases for output currents higher than 0.3 mA. In addition, the characteristic is not linear in this region and the reduced overdrive voltages of the transistors diminish the circuit's driving capability.

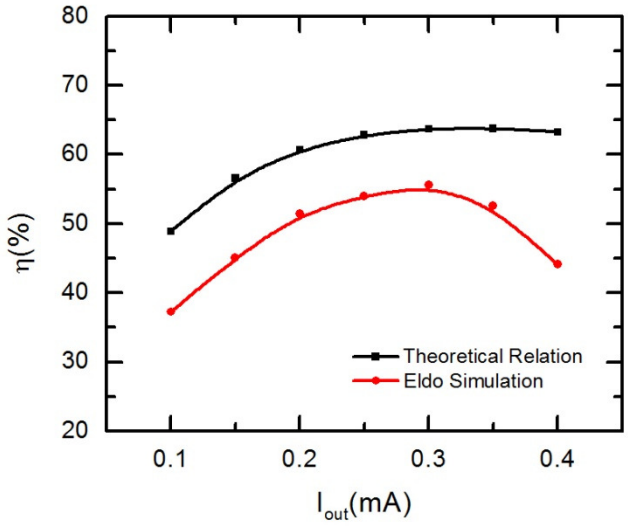

Figure 2.17. The simulated and theoretical power efficiency for the DC/DC converter

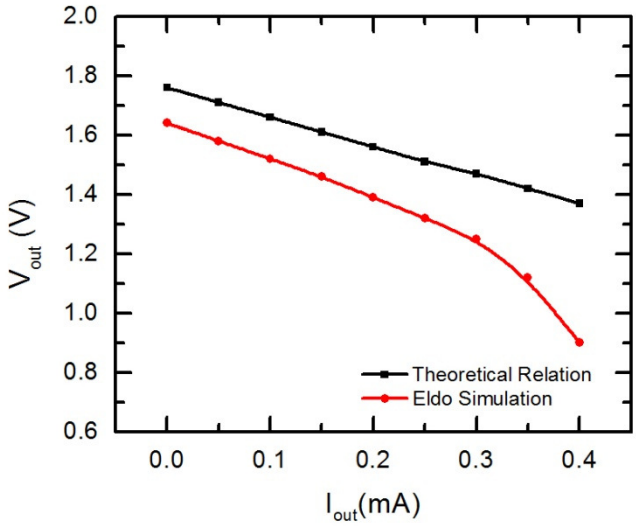

Figure 2.18. The simulated and theoretical current-voltage characteristic for the DC/DC converter

2.2.2.4. Implementation & Measurement Results. To validate the results of the previous analysis, a DC/DC converter utilizing 2-stage voltage doubler circuit topology was designed and fabricated in UMC 0.18 µm CMOS technology. The clock frequency was set to 50 MHz with a ring oscillator circuitry and the total storage capacitance per stage was 40 pF (C_1=C_2=20 pF). Figure 2.19 shows the micrograph of the DC/DC converter. The designed circuitry consumes a total area of 340µm×340µm of which 87.5% is dominated by metal-insulator-metal (MIM) stage capacitors.

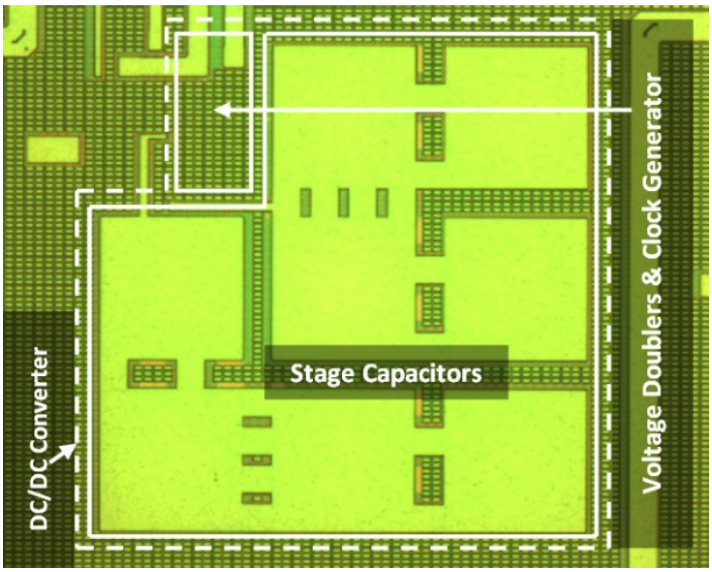

Figure 2.19. The micrograph of the DC/DC Converter

The DC/DC converter circuit is tested for four different input voltage levels; 0.45, 0.5, 0.55 and 0.6 V. These voltage levels are possible open-circuit voltage levels of a silicon photodiode under various light intensities. At these input voltages, source-measure units (SMU) of the semiconductor parameter analyzer sweeps the applied input current in a range that a typical silicon photodiode can supply and measures the current and the voltage seen at the output of the DC/DC converter. All measurements are taken with an output capacitor of 1 μF. Extracted efficiency and current-voltage characteristics are shown in Figure 2.20. The circuit can convert 0.5 V at the input to 1.2 V whereas 0.45 V input voltage is not enough for operation. Measurements reveal 56 % of maximum efficiency for an input voltage of 0.55 V and an input current of 0.54 mA, generating an output voltage of 1.19 V and an output current of 0.14 mA.

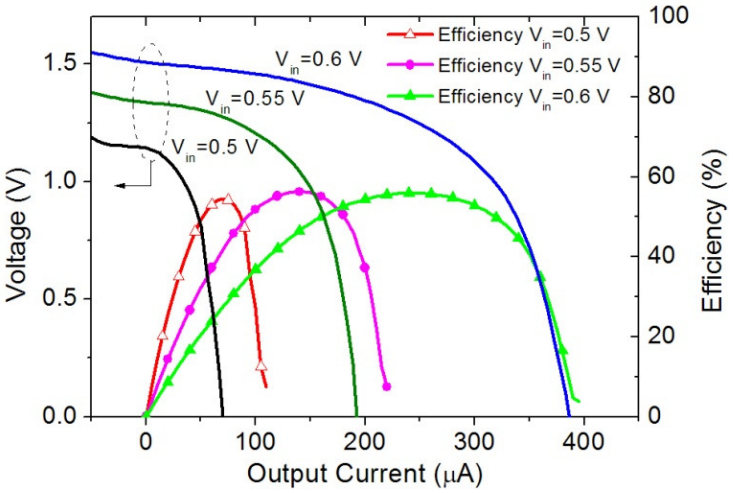

Figure 2.20. The output voltage and the efficiency of the DC/DC converter as a function of the current drawn from the output of the circuitry for different values of the input voltage to be boosted.

2.2.3 Voltage Increase with Charge Accumulation

Although, the combination of a photodiode, a DC/DC converter and a storage capacitor can be used as the basic optical power supply unit, a higher level of current capability is achievable by incorporating a transmission gate between the storage capacitor and the load for intermittently powered applications. The transmission gate functions as a switch, enabling the flow of accumulated charge on the storage capacitor to the load at

definite time instances. The transistors comprising the transmission gate in the design can be sized such that the voltage drop across them is confined to a minimum value.

The value of the storage capacitor C_C can be determined by the discharge time relationship for the storage capacitor as

$$C_C = I_{DD} \frac{\Delta t_{DD}}{\Delta V_{DD}} \tag{2.13}$$

where I_{DD} is the supply current for the circuit being powered by the unit, ΔV_{DD} is the permissible voltage drop on the supply voltage and Δt_{DD} is the on-time interval of the intermittently powered application.

2.3 System Level Integration & Measurement Results

The presented integrated system contains monolithic triple-well photodiode next to the DC/DC converter circuit. Since, the presented system contains both optical and electrical parts, the integration issue plays an important role in the performance of the designed system. In order to evaluate the performance of the integrated overall optoelectronic system; first, the DC/DC converter has been characterized using the triple-well photodiode on the same die with an optical set-up similar to the one previously shown in Figure 2.11. Then, the feedback mechanism between the photodiode and the DC/DC converter that acts an intrinsic voltage regulator has been studied in detail. The resulting system has been characterized in order to give the overall performance metrics. The following subsections discuss the obtained measurement results, in detail.

2.3.1 DC/DC Converter Characterization Using the On-chip Triple-well Photodiode

The DC/DC converter should be able to double the voltage level from the triple-well photodiode on the same die when light is shined on the photodiode surface. In this context, the DC/DC converter circuit is characterized with a laser source at a wavelength of 650 nm without fiber coupling but with a convex lens focusing the incident laser light on it. In

these experiments, the spot size of the laser is smaller than the area of the photodiode. Output voltage versus current of the DC/DC converter circuit is shown in Figure 2.21 for varying optical power levels. An incident optical power level of 40 mW, which corresponds to an optical power density of 44.4 W/cm^2 for an implemented triple-well photodiode with a photosensitive area of 300×300 μm^2, is enough to make the DC/DC converter work and double the voltage to 1.2 V.

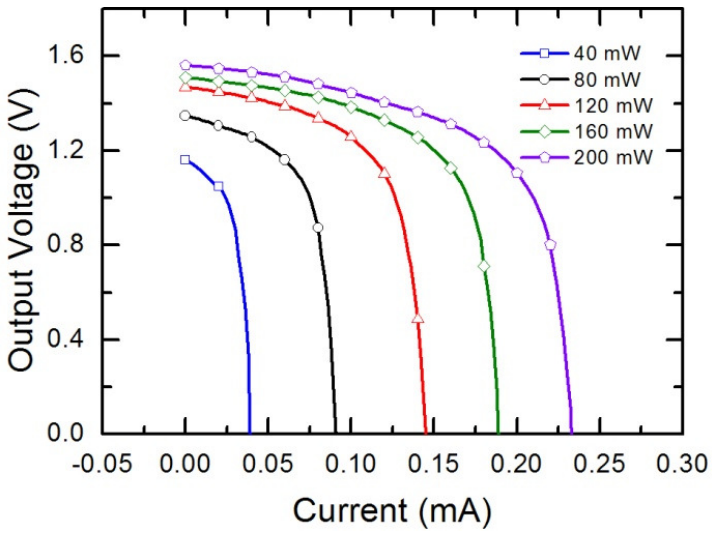

Figure 2.21. The output voltage of the DC/DC converter connected to a triple-well photodiode on the same die versus the current drawn for different power levels of optical illumination

2.3.2 The Feedback Mechanism between the DC/DC Converter and Triple-well Photodiode

The combination of the triple-well photodiode together with the DC/DC converter circuit forms an intrinsic feedback in the presented system, shown in Figure 2.22. The feedback mechanism can be explained as follows. The photovoltaic voltage of the photodiode, V_{ph} serves as the supply voltage, V_{DD}, for the clock generator circuit, and determines the clock frequency for the voltage doubler circuit. For a given output current loading, I_L, the input current of the converter circuit, I_{In}, is directly related with the clock frequency, f_{CLK}. Since the input current of the converter is supplied from the photodiode ($I_{In} = -I_{Ph}$), the current from the photodiode translates into a supply voltage again for the

converter circuit through the current-voltage relation of the photodiode. In this way, a feedback mechanism is created in the closed path that acts to keep the voltage of the photodiode within an input voltage range for the converter circuit.

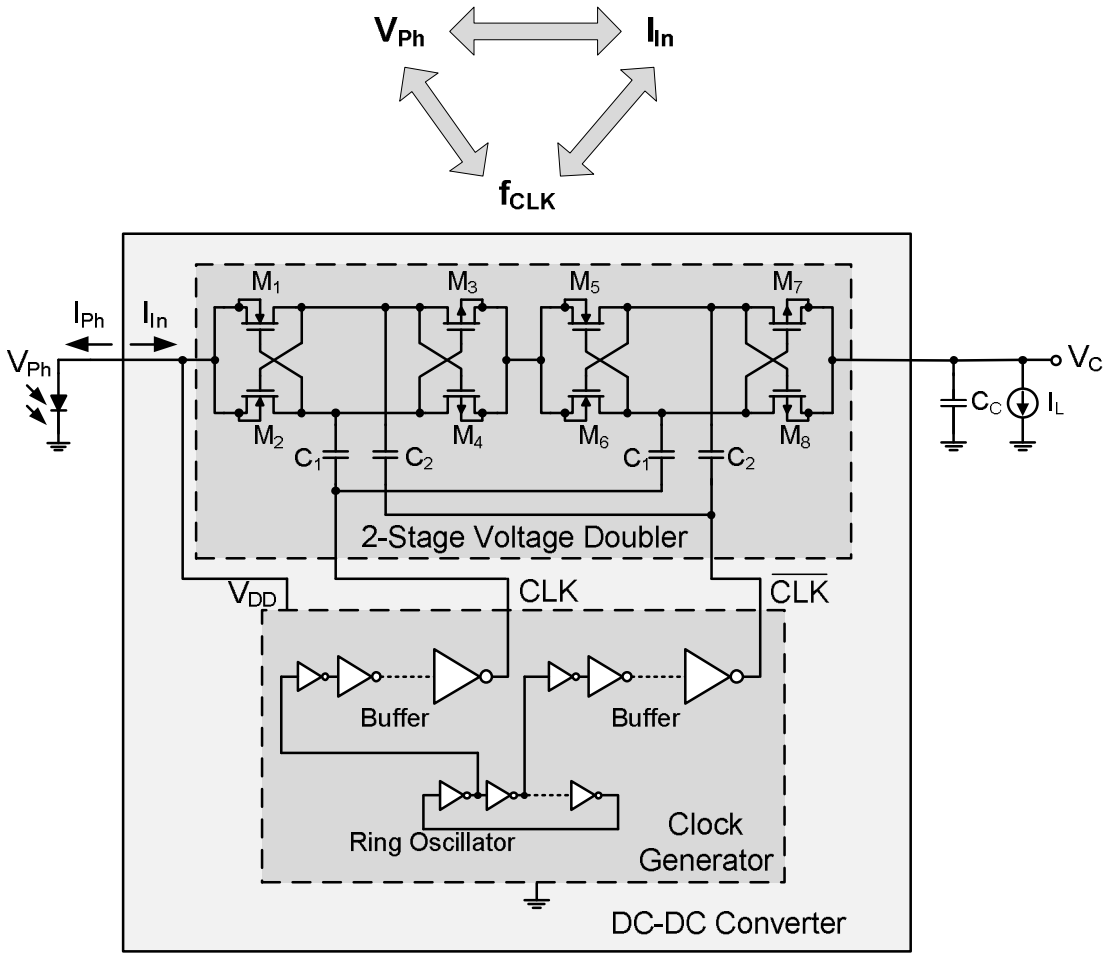

Figure 2.22. The intrinsic feedback between the photodiode and DC/DC converter circuit

In order to illustrate this feedback mechanism, the clock generator circuit has been investigated first as a separate block for different supply voltages ranging from 0.5 V to 0.65 V. Figure 2.23 shows the simulated clock frequency versus supply voltage for the clock generator circuit. Then, the input current characteristic of solely the DC/DC converter circuit has been investigated as a function of the clock frequency. Figure 2.24 shows the simulated input current of the DC/DC converter circuit versus clock frequency for an output current loading of 0.05 mA.

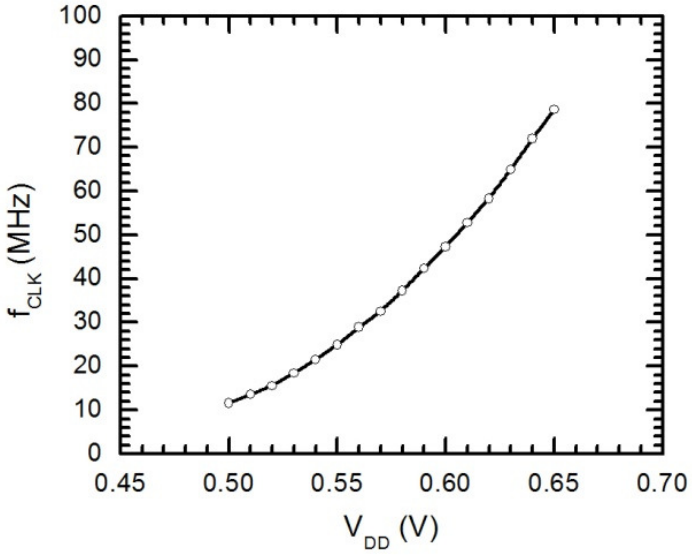

Figure 2.23. The simulated clock frequency of the clock generator circuit versus supply voltage

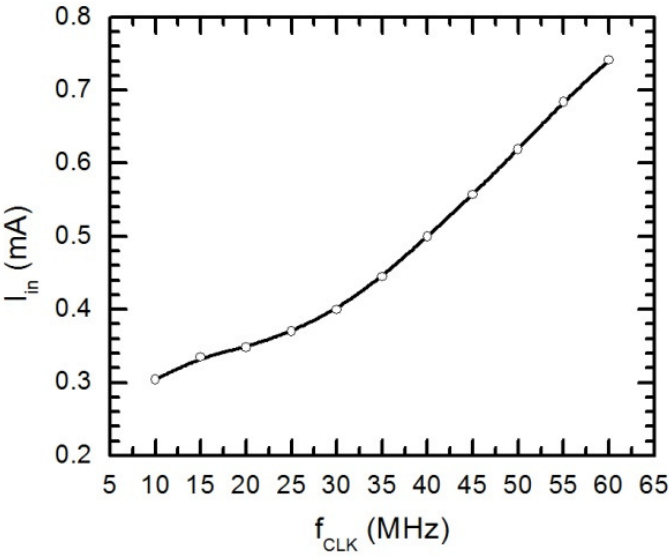

Figure 2.24. The simulated input current characteristic of the converter circuit versus clock frequency for an output current loading of 0.05 mA

The simulated characteristics in Figure 2.23 and 2.24 are related to each other through the current-voltage characteristic of the triple-well photodiode utilized in the presented system. The measured current-voltage characteristics of the triple-well photodiode at different optical power levels of illumination were previously shown in Figure 2.13. In order to illustrate the relation, the current-voltage characteristic at only 200 mW of incident optical power has been reproduced in Figure 2.25 for convenience.

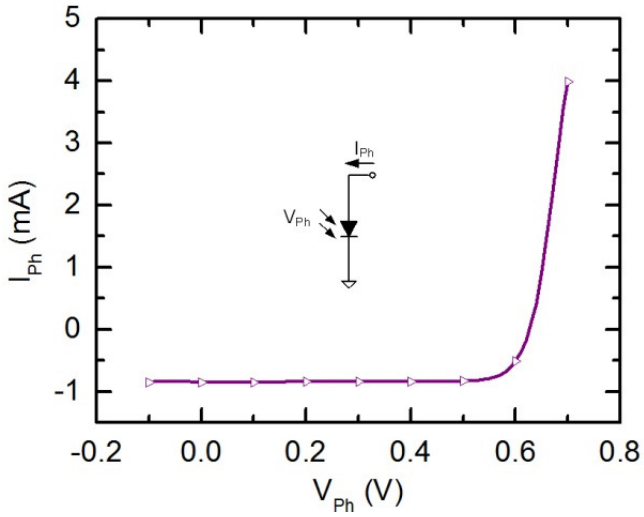

Figure 2.25. The current-voltage characteristic of the triple-well photodiode at 200 mW optical power

It is important to note that the voltage of the photodiode in the system after initial transient can be determined from the characteristics given above. Let us make an initial assumption that V_{Ph} = 0.5 V. From Figure 2.23, the simulated clock frequency for V_{Ph} = V_{DD} = 0.5 V turns out to be approximately 12 MHz. Hence, this leads to an input current of approximately 0.32 mA for the converter circuit, as can be seen from Figure 2.24. According to the current-voltage characteristic of the photodiode given in Figure 2.25, a current of I_{Ph} = − 0.32 mA translates into a photodiode voltage, V_{Ph} of 0.608 V. To further resolve this value, a second iteration can be performed through the simulated characteristics. A V_{Ph} of 0.608 V leads to a clock frequency of 52 MHz which in turn leads to an input current of 0.64 mA for the converter circuit. As a result, the specified current translates into a voltage, V_{Ph} of 0.585 V. In the third iteration, a V_{Ph} of 0.585 V leads to a clock frequency of approximately 40 MHz which in turn leads to an input current of 0.5 mA for the converter circuit. Finally, the specified current translates into a voltage, V_{Ph} of 0.595 V.

In order to verify these considerations, the measured current-voltage characteristics for the optical power level of 200 mW have been modeled and co-simulated with the DC/DC converter circuit. The simulation results showed that the mean value of the photodiode voltage, V_{Ph} is nearly equal to 0.59 V, which is in good agreement with the projected value of 0.595 V. In addition, it is important to note that this intrinsic feedback

mechanism in the presented system acts as a voltage regulator and stabilizes the input voltage of the photodiode, and consequently the output voltage of the converter against variations in the output current loading level.

3. INTEGRATED LOW-POWER RECEIVER FRONT-END

The main aim of this thesis is to develop an optically powered integrated CMOS receiver front-end for electrically isolated micro-scale applications. Since, the previous chapter concentrated on designing an optoelectronic power supply unit for the overall system, this chapter gives the design aspects of an integrated low-power CMOS receiver front-end consisting of an LNA, a voltage gain amplifier and a mixer. However, some general issues will be discussed first, focusing on front-end performance considerations and common receiver topologies.

3.1 Receiver Topologies

There are two main receiver topologies; namely, the homodyne (also called zero Intermediate Frequency (IF) or direct conversion) topology and the heterodyne (also called IF) topology. The difference between these topologies is in whether or not an intermediate frequency is used in the demodulation process. Figure 3.1 shows a simple direct conversion architecture where the incoming signal is converted directly to baseband without the use of an intermediate frequency [59].

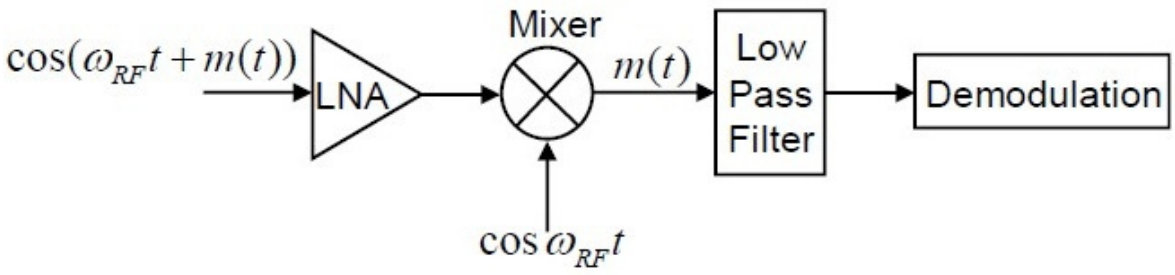

Figure 3.1. A simple direct conversion receiver [59]

The direct conversion architecture has some important advantages over the heterodyne (IF) architecture. Specifically, the direct conversion architecture does not suffer from the image problem while the heterodyne architecture (IF) does due to the usage of an

intermediate frequency [59]. Basically, the image problem is known as the existence of an interfering signal, called as image, at a frequency on the other side of the local oscillator frequency from the desired RF signal (i.e. 2IF away from RF). The most common approach to suppress the image is to use an image reject filter before the mixer in a heterodyne (IF) architecture. This filter is difficult to implement since it has to work at the RF frequencies resulting in an increase in the power consumption of the receiver and integration problems, thus increasing cost. Figure 3.2 shows the architecture of a simple heterodyne (IF) receiver [59].

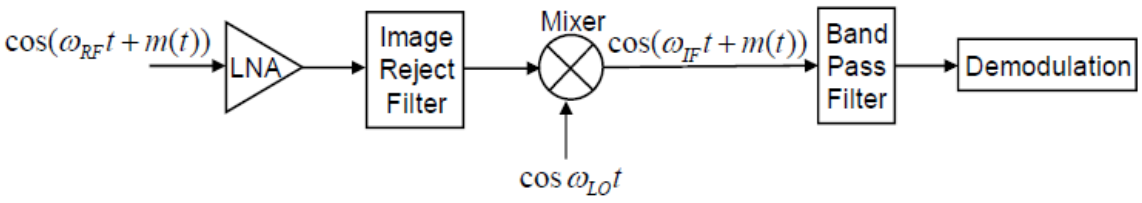

Figure 3.2. A heterodyne (IF) receiver [59]

The direct conversion receiver topology has been selected as the receiver architecture utilized in this thesis due to the fact that this topology introduces the capability of full integration of the front-end. However, the direction conversion receiver topology has a major disadvantage known as the DC offset problem which may be avoided by using offset cancellation techniques [59].

The main contribution of this thesis is not the utilized receiver architecture but the integrated overall optoelectronic solution. Actually, the LNA and mixer circuits have been designed to be functional even for supply voltages as low as 1.2 V within any receiver topology. Therefore, they may be transferred to any other topology specific to application.

3.2 Low Noise Amplifier Design

The Low Noise Amplifier (LNA) is the most critical building block in a receiver system. In the receiver architecture utilized in this thesis, shown Figure 3.3, the antenna receives the signals in electromagnetic domain from free space and converts them to electrical signals. These incoming signals, which contain the desired signals as well as the

unwanted interferers, are then fed to the first stage of the receiver system, the LNA. In general, the desired signals are weaker than the unwanted interferers. Therefore, the LNA has to be able to provide sufficient gain to the desired signals with minimal degradation to their signal-to-noise ratio (SNR).

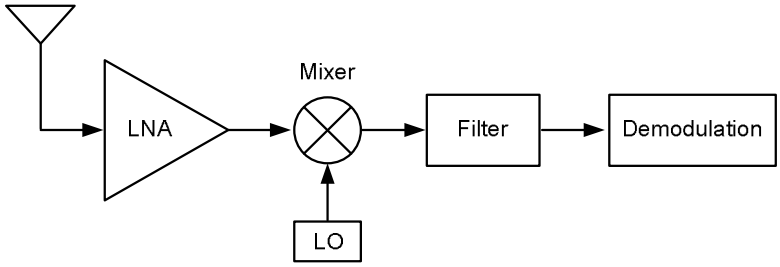

Figure 3.3. The utilized receiver architecture

The signal-to-noise ratio is a measure to quantify how much a signal is degraded by noise. More technically, it is defined as the ratio between the signal power and the noise power. This can be expressed mathematically as

$$SNR = \frac{P_{signal}}{P_{noise}} \; or \; in \; dB \; SNR_{dB} = 10 \, log_{10} \frac{P_{signal}}{P_{noise}} \tag{3.1}$$

where $P_{signal}$is the power of the signal, and P_{noise} is the noise power. As the expression implies, it is desirable to have as high signal-to-noise ratio as possible. However, additional noise is introduced to the signal while the signal passes through any system or device in practice. Therefore, the signal-to-noise ratio at the input of a system or device is always larger than the signal-to-noise ratio at the output. The noise figure (NF) is a measure of the degradation of the SNR and can be defined as the difference in decibels between the input SNR and the output SNR, as given by

$$NF_{dB} = 10 \log_{10} \frac{SNR_{input}}{SNR_{output}} = SNR_{dB_{input}} - SNR_{dB_{output}} \tag{3.2}$$

It is obvious that the noise figure is always larger than 0 dB for a physical system. In addition, a greater value of noise figure means that a higher level of noise is introduced to the signal through that system or device.

When several stages are cascaded in a system as shown in Figure 3.4, the overall noise figure (NF_{tot}) based on the Friis equation can be given as [59],

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_1} + \frac{NF_3 - 1}{A_1 A_2} + \cdots + \frac{NF_n - 1}{A_1 \ldots A_{n-1}} \tag{3.3}$$

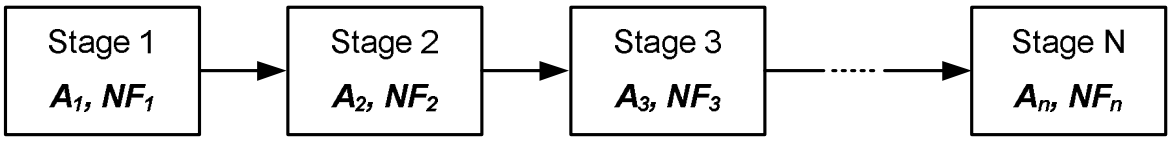

Figure 3.4. The schematic of a cascaded system

In Equation 3.3, A_n is the gain, and NF_n is the noise figure of the nth stage in Figure 3.4. Equation 3.3 indicates that the later the block in the system, the lower its impact on the overall noise figure. This is due to the fact that the noise contribution of each stage is divided by the product of the gains of previous stages. Therefore, it is important to note that the overall noise performance of the receiver is dominated by the noise performance of the first block, which is the LNA. Actually, this is why the amplifier at the front of the receiver path needs to be a low noise amplifier.

By examining equation 3.3, it is noticed that the gain of the first stage appears in the denominator of every term. This means the higher the gain of the first stage, the lower the noise figure contribution from every subsequent stage in the receiver path. Although, it is desired to have large gain for the LNA to decrease the overall noise figure, there is a limit on how large the gain is allowed to be. A very large gain may overload the mixer and compromise dynamic range. Therefore, since the sensitivity of the receiver is defined by the lowest signal level it can detect with certain error limits, and given that the noise performance of the receiver determines the smallest signal it can handle, and that the LNA has a dominant effect on the noise performance of the receiver, it can be concluded that the LNA has a huge impact on the overall sensitivity of the receiver system. The following section describes the noise sources in a MOS transistor since the LNA that will be presented in this thesis is implemented with MOS technology.

3.2.1 Sources of Noise in a MOS Transistor

Since a MOS transistor is essentially a voltage controlled resistor, it exhibits thermal noise [60]. This noise source can be represented by a noise-current generator $\overline{i_d^2}$ from drain to source in the small signal equivalent model given in Figure 3.5 [61].

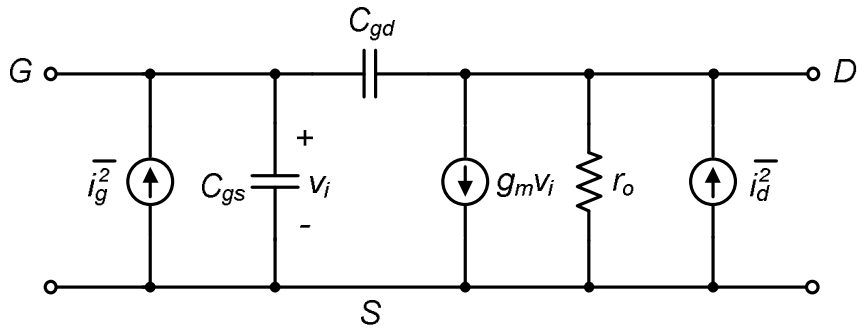

Figure 3.5. MOS small-signal equivalent model with noise sources [61]

Another noise of source in MOS transistor is flicker noise (also called 1/*f* noise), which can be explained by invoking several charge trapping phenomena. Basically, MOS transistors conduct current near the surface of the silicon where some types of defects and certain impurities can randomly trap and release charge. As a result, the distribution of trapping times leads to 1/*f* noise spectrum in MOS transistors. The flicker noise is found experimentally to be represented by a drain-source current generator, and the flicker and thermal noises can be combined in a single noise-current generator $\overline{i_d^2}$ shown in Figure 3.5 with the following equation [61]:

$$\overline{i_d^2}=4kT\left(\frac{2}{3}g_m\right)\Delta f+K\frac{I_D^a}{f}\Delta f \tag{3.4}$$

where the first term belongs to thermal noise, and the second term defines the flicker noise. The variables in equation 3.4 can be explained as follows: k is the Boltzman constant, T is the absolute temperature, g_m is the device transconductance at the operating point, Δf is the noise bandwidth, K is a device specific constant, I_D is the drain bias current, and a is a constant between 0.5 and 2. Actually, the equation is only valid for long channel devices. For short channel devices below 1 µm, thermal noise values considerably larger than the

first term in (3.4) have been measured [62]. This large noise is attributed to carrier heating due to the large electric fields in short channel devices.

Another source of noise in the MOS transistor is described as the shot noise generated by the gate leakage current. This noise has been represented by $\overline{i_g^2}$ in Figure 3.5, and can be given as

$$\overline{i_g^2} = 2qI_G\Delta f \tag{3.5}$$

where q is the electronic charge, I_G is the gate leakage current and Δf is the bandwidth in hertz. Since, the leakage current is usually smaller than 10^{-15} A, the shot noise can be considered to have negligible effect on the overall noise performance of the device. In addition, the noise current sources in (3.4) and (3.5) are independent of each other.

There is another component of gate-current noise which arises from fluctuations in the gate-to-channel potential. Basically, these fluctuations capacitively couple into the gate terminal, and generate a noisy ac gate current. Although, this gate current is negligible at low frequencies, it can become significant at very high radio frequencies. The mean-squared value of this gate current for a long-channel device can be given as [61]

$$\overline{i_g^2} = \frac{16}{15} kT\omega^2 C_{gs}^2 \Delta f \tag{3.6}$$

where $C_{gs} = (2/3)C_{ox}WL$. Since, the gate-current noise in (3.6) and the thermal noise term in (3.4) both originate from thermal fluctuations in the channel, they are correlated. The value of the correlation between these currents is given as 0.39 [63]. For short channel devices below 1 µm, this component of the gate-current noise may be larger than the current given in (3.6) due to increased thermal activity caused by large electric fields [64]. The total gate-current noise, $\overline{i_g^2}$ in Figure 3.5 is the sum of noise current terms in (3.5) and (3.6).

3.2.2 Common Source Low-Noise Amplifier Design via 50 Ω Impedance Matching

The design strategy utilized for the LNA in this thesis is to select a suitable technique that will enable an ultra low noise performance (noise figures below 1 dB) and a fully integrated solution. This section provides a targeted review of common-source LNA architecture and LNA design approaches to give clear insight into the issues involved in such an approach.

The interface between the LNA and the antenna involves an interesting issue which can be interpreted differently by analog designers and microwave engineers. From the noise point of view, a transformation network preceding the LNA may be necessary in order to obtain minimum NF. However, from signal power point of view, a conjugate impedance matching is utilized to deliver maximum power to the LNA. Although, both methods have their own advantages and drawbacks, the latter one is the most widely practiced method in today's receiver systems, i.e., the LNA is designed such that its input impedance is resistive 50 Ω. This is mainly due to the fact that the bandpass filter following the antenna is usually designed to be used in various receiver systems, and should operate with a standard termination impedance, 50 Ω. In the case that the source and load impedances of the filter deviate from 50 Ω significantly, the characteristic of the filter may exhibit loss and ripples in the passband and stopband.

There are three basic single-transistor amplifier stages; namely, the common-drain, the common-gate, and the common-source amplifiers that constitute the basis of existing LNA topologies. However, only the common-source LNA design will be given here, and the readers are referred to [65] for details of the other existing topologies and their variations.

A typical common-source amplifier is shown in Figure 3.6 in which a 50-Ω termination resistor is placed in parallel with the input. Unfortunately, the termination resistor adds thermal noise of its own and attenuates the signal ahead of the transistor. The combination of these two effects leads to unacceptably high noise figure values. In fact, the noise figure of a stage consisting of a parallel resistor, R_P with respect to a source resistance R_S can be given as

$$NF = 1 + \frac{R_S}{R_P} \tag{3.7}$$

Therefore, the noise figure of the LNA exceeds 3 dB for $R_P = R_S$. In addition, it is important to note that the circuit should exhibit an input impedance of 50 Ω without the thermal noise of 50 Ω resistor.

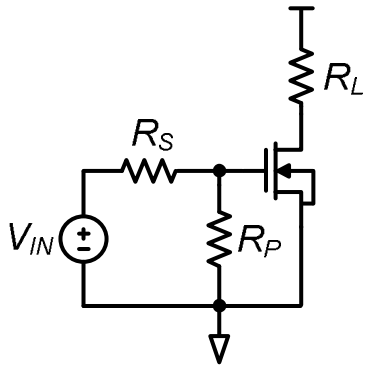

Figure 3.6. A common-source amplifier with resistive termination

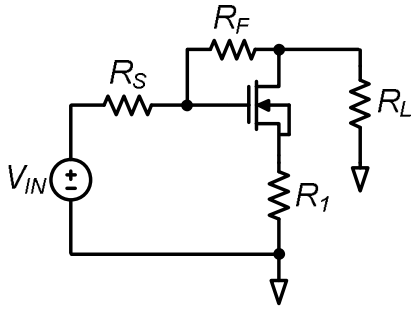

Figure 3.7. A shunt-series amplifier [64]

Another circuit for a common-source amplifier, which provides a broadband real input impedance is shown in Figure 3.7 [64]. Since, this circuit does not attenuate the input signal before amplification; it does have a considerably better noise performance than that of the circuit of Figure 3.6. However, the noise figure of the circuit generally exceeds the minimum noise figure attainable from the device. From the comparison in [64], it is shown that these circuits are usually employed as broadband amplifiers and their power consumption is much higher than other amplifiers with similar performance.

The presented topologies up to this point suffer from noise figure degradation due to the presence of noisy resistances in their signal path. Instead of resistances, the method of inductive source degeneration may be used in order to control the value of the real part of the input impedance through choice of inductance. Figure 3.8 shows an inductively degenerated common-source amplifier circuit.

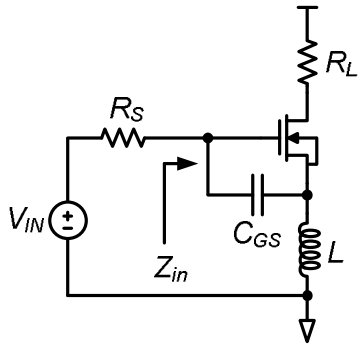

Figure 3.8. An inductively degenerated common-source amplifier

The input impedance of the circuit can be given as [59]

$$Z_{in} = j\omega L + \frac{1}{j\omega C_{GS}} + g_m \frac{L}{C_{GS}} \tag{3.8}$$

where L is the inductance in the source terminal and C_{GS} is the input capacitance of the MOS transistor. Hence, the input impedance is that of a series resistor-inductor-capacitor RLC network, with a resistive term that is directly proportional to the inductance value. It is important to note that the value of the inductor may be selected such that the effect of the input capacitance is tuned out at the operating frequency, ω_{in} as indicated by the following equation:

$$L = \frac{1}{C_{GS}{\omega_{in}}^2} \tag{3.9}$$

Therefore, the imaginary part of the input impedance in (3.8) is terminated at ω_{in}, and the real part, which is equal to $g_m(L/C_{GS})$, can be used to tune the input resistance to the

source resistance (50 Ω) without the need for any real resistance, hence avoiding any deterioration in the amplifier noise figure.

Generally, the inductive degeneration method works very well for high frequency (gigahertz range) narrowband LNAs. For an operating frequency of 1.5 GHz, the value of the required inductance with a C_{GS} of 1 pF turns out to be nearly 11.3 nH, according to the equation in (3.9). Thus, this inductance value can be realized with an on-chip spiral inductor although its quality factor, Q is low due to technology limitations. However, the integration of inductance is not possible for an LNA operating at several tens of MHz with the method of inductive degeneration. The LNA that will be presented in this thesis is designed for an operating frequency of 123 MHz. Since, the required inductance value with an input capacitance of 1 pF can be calculated as 1.67 μH, according to (3.9); the design will require an off-chip inductor which is not acceptable for emerging micro-scale electronic systems such as biomedical implants and sensors. Although increasing the gate-source capacitance may seem as an option to lower the value of the inductance, a practical on-chip inductance value of 15 nH will require a C_{GS} of more than 100 pF which is not practical for virtually any application. Therefore, a design strategy different than the generally practiced impedance matching method is essential for a fully integrated low-power LNA operating at the frequency of 123 MHz. Before discussing the details of the design technique so called noise matching, the following section presents the coil that has been used in the receiver instead of a radio antenna. Nevertheless, the matching of the receiver to the coil plays a vital role just like in radio systems and it is necessary to design the LNA according to the characteristics of the coil.

3.2.3 The Coil

Generally, the degree of required uniformity in the RF field for a specific application determines the type and the dimensions of a coil. Since, any RF heterogeneity in the receiver coil degrades the uniformity of the response, the simplest approach to improving RF uniformity is to merely increase the size of a coil. However, determining minimum coil dimensions necessary for sufficient RF homogeneity relevant to a specific application is beyond the scope of this thesis.

The receiver front-end in this thesis can be used for a range of low-frequency applications in which ultra-low noise performance, low power consumption, and integration capability have utmost importance. In order to illustrate the performance of the receiver front-end, a solenoidal coil has been used as the antenna to pick up signals. As compared to planar coils, the solenoid coil has the advantage that its geometry allows the induction of higher voltage signal amplitudes for the receiver input.

The solenoid coil can be modeled as an inductor, L, in series with a parasitic resistance, R, and its quality factor is given as $Q = \omega L/R$. Figure 3.9 shows the basic equivalent circuit model for the receiver coil.

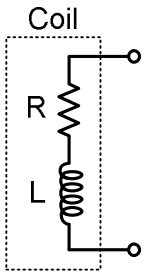

Figure 3.9. The equivalent circuit model for the receiver coil

The value of inductor for the solenoid wound with a single layer of round wire consisting of n-turns can be calculated as [66,67]

$$L = \frac{9850 d_{coil} n^2}{4.5 + 10(l_{coil}/d_{coil})} \text{ [nH]} \tag{3.10}$$

where d_{coil} is the average diameter, and l_{coil} is the average length of the coil expressed in meters. Before considering the coil's parasitic resistance, R, it is important to examine the resistance for an equivalent straight wire of equal length, l:

$$l = n\pi d_{coil} + l_{coil} \tag{3.11}$$

At high frequencies, the current is only carried effectively near the outer perimeter of the wire in a region characterized by the conductor's skin depth (δ). This is known as the

skin effect phenomena. If the wire's electrical resistivity (ρ) is known, the value of the skin depth can be calculated as [68]

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{3.12}$$

Here, f represents the frequency, and $\mu = \mu_0 \mu_r$, where $\mu_0 = 4\pi \times 10^{-7}$ T · m/A is the permeability in vacuum, and μ_r is the relative permeability of the conductor. For annealed copper wire, $\mu_r \cong 1$, $\rho = 1.72 \times 10^{-8}$ Ω · m at 20℃. With these values, (3.12) estimates a skin depth of about 6 μm at 123 MHz. If this value is very small compared to the wire diameter, d, the effective cross-sectional area in which the current flows can be approximated by $\pi \delta d$. In the so-called high frequency limit, the resistance for a straight wire of length of l can be given by

$$R_{st} = \frac{l}{d} \sqrt{\frac{\mu \rho f}{\pi}} \tag{3.13}$$

However, when a straight wire is coiled to form a solenoid, the resistance becomes greater than the value of R_{st} given in (3.13). This is due to the additional eddy currents induced in each turn by the changing magnetic fields of the neighbor turns. These currents dissipate power and contribute to each turn's resistance. This is known as the proximity effect [69]. Therefore, the resistance of a solenoid, R can be expressed as

$$R = R_{st} \xi \tag{3.14}$$

where R_{st} represents the high frequency resistance of an equivalent straight wire, and ξ is an enhancement factor resulting from the proximity effect. Since, the magnetic configuration around each turn is influenced by the winding parameters such as the diameter of the coil wire and the spacing between turns, ξ strongly varies with the winding geometry.

For test purposes of the receiver, a copper wire of 250 µm thickness was used to wind a coil with 3 turns. The coil had an average diameter (d_{coil}) of 3 mm, and an average length (l_{coil}) of 1mm. The impedance measurement of the coil was performed using a vector network analyzer (Rohde & Schwarz ZVB4). The measured values of the model parameters in Figure 3.9 for the coil agree with the analytical results, and can be given as follows; $L = 32.5$ nH and $R = 0.158\ \Omega$ at 123 MHz, resulting in a quality factor of about 160.

3.2.4 Noise Matching via Passive Amplification

In the widely practiced discrete design of RF receivers, an off-the-shelf discrete LNA with an input impedance of 50 Ω is connected to the coil through an impedance matching network. One example of the network consists of capacitors C_1 and C_2, as shown in Figure 3.10 [70]. V_{rms} in the coil's model is the root-mean square (rms) value of the voltage signal, $V(t)$ induced across the coil, and $\overline{v_n^2}/\Delta f$ is the thermal noise due to the parasitic resistance, R. By selecting suitable values for the capacitors, the real part of Z_1 becomes 50 Ω, and the inductive reactance of Z_1 resonates with C_2, leading to Z_2=R_{LNA}=50 Ω.

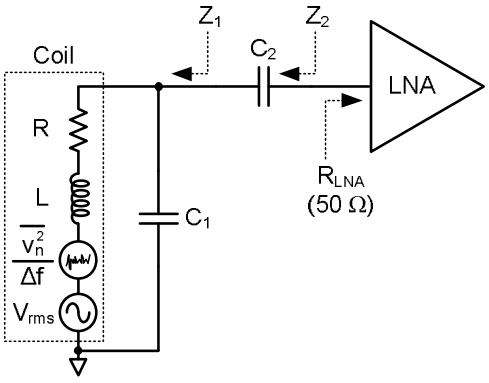

Figure 3.10. 50 Ω Impedance matching between LNA and coil. (After [70])

This method of impedance matching dominantly used to maximize power transfer from the coil to the LNA works satisfactorily as long as the noise figure of the LNA is small at the source impedance of 50 Ω. However, the derivations in Section 3.2.2 show that the input impedance of a MOS transistor is inherently capacitive, and providing a match to

a 50 Ω source degrades the noise performance of the LNA and requires the design to include an off-chip inductor for the operating frequency of 123 MHz.

To minimize the noise figure, a different LNA-coil connection can be utilized without either demanding the 50 Ω input impedance for the LNA or the impedance matching condition [70]. Figure 3.11 shows a general passive network between a coil and an LNA.

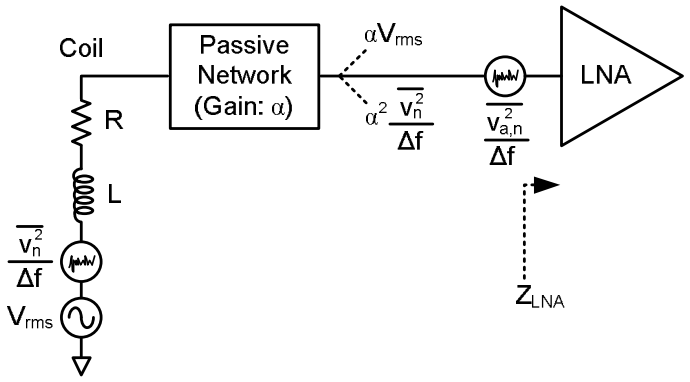

Figure 3.11. A general passive network between a coil and an LNA (After [70])

The passive network has a voltage transfer function of $H(\omega)$ that includes the effect of the LNA's input impedance, Z_{LNA}. The voltage gain of the passive network for the operating frequency of ω_{op} can be defined as $\alpha = |H(\omega)|_{\omega=\omega_{op}}$. If the noise contribution of the passive network is negligible, the passive network will amplify both the voltage signal and the thermal noise of the coil by the same factor, α, thereby maintaining the SNR. The voltage at the output of the network will be αV_{rms}, and the noise power spectral density will be $\alpha^2 \overline{v_n^2}/\Delta f$.

The value of the voltage gain of the passive network plays an important role in the noise performance of the receiver. Figure 3.12 illustrates the passively amplified voltage signal, the coil noise, and the LNA's input referred noise for a large and small α. If α is large enough to make $\alpha^2 \overline{v_n^2}/\Delta f$ much higher than the LNA's input referred noise, $\overline{v_{a,n}^2}/\Delta f$, as shown in the left side of the Figure 3.12, the SNR is not degraded by the LNA. Therefore, the noise figure is small. However, if α is not large enough, and $\alpha^2 \overline{v_n^2}/\Delta f$ is comparable to, or smaller than $\overline{v_{a,n}^2}/\Delta f$, as shown in the right side of the Figure 3.12 [70],

the SNR is degraded greatly by the LNA, resulting in a high noise figure. Therefore, it is necessary to maximize α and minimize the LNA's input referred noise, $\overline{v_{a,n}^2}/\Delta f$ in order to minimize the noise figure. This section discusses how to maximize α and the latter one is given in Section 3.3.

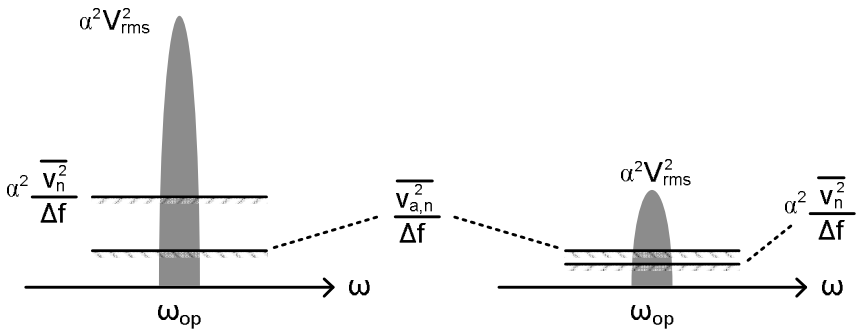

Figure 3.12. The passively amplified voltage signal, the coil noise, and the LNA's input referred noise for a large (left) and small (right) α [70]

For $Z_{LNA} = \infty$, a passive network that will maximize the value of α will be designed. Although various topologies can be used for the passive network, the $C_1 - C_2$ network has been used as the topology here. The aim of the design is to determine the values of C_1 and C_2 in Figure 3.13.

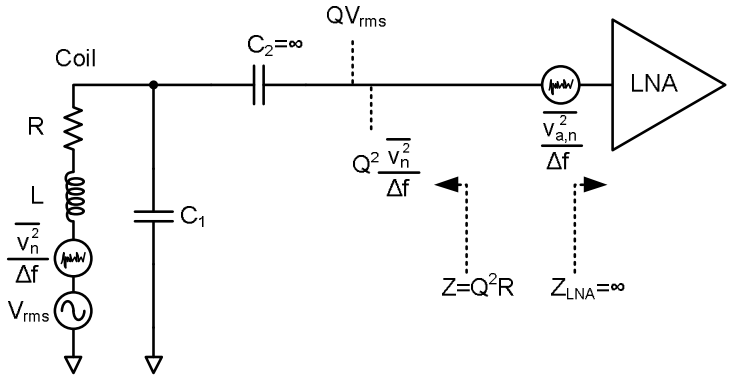

Figure 3.13. Maximum passive amplification (After [70])

Firstly, C_2 should be infinite (short circuit) since any finite value will lower the voltage at the output of the passive network. With $C_2 = \infty$, The α as a function of C_1 can be given as:

$$\alpha(C_1) = \frac{1}{\sqrt{\left(1 - \omega_{op} R C_1 Q\right)^2 + \left(\omega_{op} R C_1\right)^2}} \tag{3.15}$$

The value of α becomes maximum

$$\alpha_{max} = \sqrt{Q^2 + 1} \approx Q \tag{3.16}$$

when C_1 equals

$$C_1 = \frac{1}{\omega_{op} R} \cdot \frac{Q}{Q^2 + 1} \approx \frac{1}{\omega_{op} R Q} = \frac{1}{\omega_{op}^2 L} \tag{3.17}$$

It is important to note that α is maximum when C_1 resonates with L at the operating frequency of ω_{op}.

According to the derivations given above for a fixed LNA input referred noise, a shunt capacitor C_1 that resonates with the coil's inductance L amplifies both the voltage signal and the coil noise by the same factor Q, thereby minimizing the noise figure [71]. It has been assumed that there is no noise in the capacitor. This assumption is quite reasonable since the quality factor of the capacitor is much higher than the coil's Q factor. In this connection, the LC resonator circuit in the minimum noise figure configuration can be seen as a passive preamplifier with a gain of Q but with almost zero noise figure which is unachievable with active amplifiers. In addition, this connection exploits the intrinsic inductance already available in the coil.

For the coil ($L = 32.5$ nH, $R = 0.158\ \Omega$) given in the previous section, the value of C_1 can be calculated as 51.5 pF at 123 MHz by using (3.17). In addition, the value of C_2 can be selected as 1μF in order to confine its impedance to a minimal value at 123 MHz. However, the gain of the designed passive network is smaller than the quality factor of the coil ($Q = 160$). This is mainly due to the fact that the LNA's input impedance, Z_{LNA} cannot be considered as infinite at a relatively high operating frequency of 123 MHz.

However, it will be shown in the following sections that the gain of the designed passive network is more than sufficient to decrease the noise figure to values below 1dB.

As a result, the presented minimum noise figure configuration so called noise matching does not involve impedance matching. This is an important advantage of noise matching technique for the design of the LNA since there is need to use an off-chip inductance to match the input impedance of the LNA to 50 Ω.

3.3 Ultra Low-Noise Amplifier Circuit Design

It is important to remind that noise figure minimization requires two tasks; maximization of α, and minimization of LNA's input referred noise, $\overline{v_{a,n}^2}/\Delta f$. As the Section 3.2.4 discussed the former task, this section focuses on the design of the LNA to perform the latter one. Since, high Z_{LNA} is a requirement for the maximization of α, the common-source topology is selected for the LNA. This topology has a capacitive input impedance that may be considered as relatively high for low frequencies.

The next design decision for the LNA lies in whether to have a single ended or differential architecture. The single-ended LNA architectures have the advantage of high gain and low power consumption. However, they are susceptible to supply noise and their performance can be adversely affected by substrate crosstalk noise when integrated with digital circuitry such as voltage doublers. Actually, it is possible to alleviate the supply noise by layout techniques such as keeping the LNA away from the noisy digital part, or blocking the noise transmission from digital circuitry. However, differential LNAs are inevitable for the design of noise immune receiver systems. They introduce two important advantages. Firstly, the differential amplification of input signal ensures the attenuation of common-mode noise signal. This improves the noise immunity of the receiver. Secondly, the differential LNA eliminates the use of a balun circuit when compared with the case for a single-ended LNA. This is because the Gilbert mixer requires differential input which is already available from the output of a differential LNA.

In this work, the NF requirement for receiver front-end is less than 1 dB since the voltage on the coil antenna is on the order of few micro-volts. In addition, a total voltage gain of at least 60 dB is essential due to the fact that the mixer requires input voltages on the order of few milli-volts. To realize such large gain, a multi stage amplifier topology is used in this work.

Since, single-ended and differential LNAs have their own advantages and disadvantages, both LNA architectures have been designed in this work. The following sub-sections discuss these designs, in detail.

3.3.1 Ultra Low-Noise Single-Ended Amplifier

Figure 3.14 shows the schematic of the designed three-stage single-ended amplifier. The first stage is the ultra low-noise amplifier (LNA) while the second stage is the voltage gain amplifier. The last stage is the source follower in order to drive the low output impedance. A large decoupling capacitor is connected between the gate of transistor M_2 and the ground such that the noise from the biasing voltage can be eliminated.

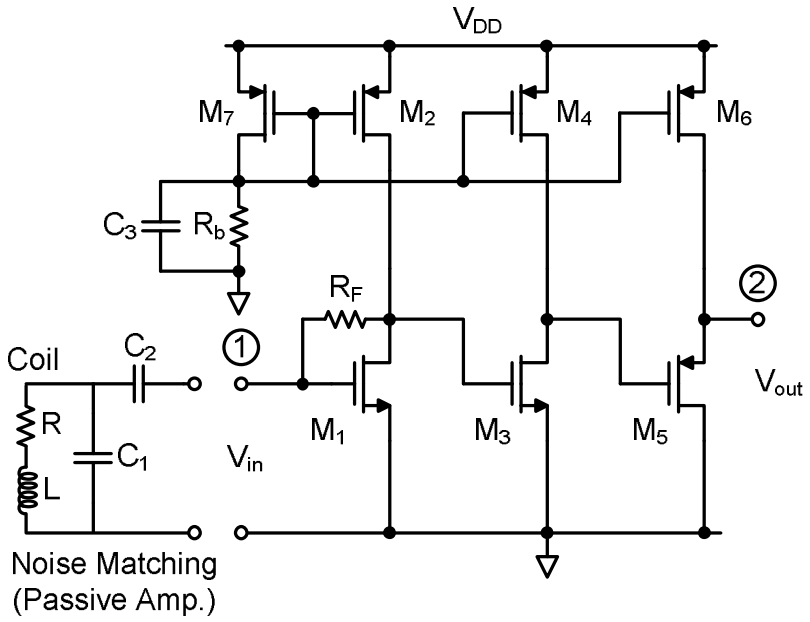

Figure 3.14. The schematic of the designed three-stage single-ended amplifier

The total noise of the LNA is dominated by the channel thermal noise of the transistors, M_1 and M_2, and the thermal noise of the feedback resistance, R_F. More formally, the input referred noise of the LNA calculated through standard small-signal analysis can be expressed as

$$\overline{v_{a,n}^2} \approx 4kT\left(\frac{1}{g_{m1}^2 R_F} + \frac{\gamma}{g_{m1}} + \frac{\gamma g_{m2}}{g_{m1}^2}\right)\Delta f \tag{3.18}$$

where $g_{m1}$and g_{m2} are the transconductances of transistors M_1 and M_2, R_F is the feedback resistance, and γ is a parameter which is equal to 2/3 for long channel devices. In deep sub-micron devices, γ exceeds the value of 2/3 and is about 50% larger for 0.18 µm CMOS [72]. It is important to note that the LNA's input referred noise can be reduced by increasing current and/or R_F. Increasing current is not feasible for low-power applications, whereas large R_F translates to large area. The noise figure of the three-stage amplifier with the coil can be expressed as

$$NF \cong 10\log\left(1 + \frac{\overline{v_{a,n}^2}}{\alpha^2 \overline{v_n^2}}\right) = 10\log\left(1 + \frac{1}{\alpha^2 R}\left(\frac{1}{g_{m1}^2 R_F} + \frac{\gamma}{g_{m1}} + \frac{\gamma g_{m2}}{g_{m1}^2}\right)\right) \tag{3.19}$$

where α is the voltage gain of the passive network and $\overline{v_n^2}$ is the thermal noise of the parasitic resistance, R of the coil. This analysis neglects the contribution of subsequent stages to the amplifier noise figure. This simplification is justifiable provided that the first stage provides sufficient gain. The gain of the LNA stage can be given as

$$A_v = \frac{(1 - g_{m1}R_F)R_L}{R_F + R_L} \tag{3.20}$$

where R_L is the load impedance of LNA. For sufficiently large R_L, A_v can be expressed as

$$A_v = (1 - g_{m1}R_F) \tag{3.21}$$

which simplifies to $-g_{m1}R_F$ when $g_{m1}R_F \gg 1$.

From (3.19) and (3.21), it is obvious that low noise figure and high gain can be achieved simultaneously when g_{m1} and R_F is large enough. However, the LNA is designed for very low power applications. Therefore, the transconductance value has been selected by considering the trade-off between the gain, noise figure and the power consumption.

For a specified target noise figure, the transconductance value of g_{m1} can be calculated by using equation (3.19). A moderately high feedback resistance of $R_F = 100\,K\Omega$ has been selected for achieving high gain and high input impedance. With a current consumption budget of 1.2 mA for the LNA, a transconductance of $g_{m1} = 24\,mS$ is the upper limit for transistors M_1 and M_2. Figure 3.15 shows the noise figure of the single-ended LNA versus the voltage gain of the passive network, α for the selected g_{m1} of $20\,mS$. This relationship has been evaluated by using equation (3.19). The parasitic resistance, R is 0.158 Ω for the coil given in Section 3.2.3, and γ has been selected as 1 since a 0.18 µm CMOS technology is used in the design.

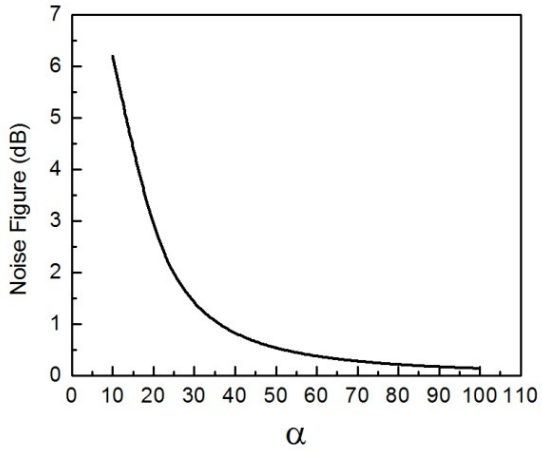

Figure 3.15. The noise figure of the single-ended LNA versus the voltage gain of the passive network, α

The value of α is approximately equal to 56 for the designed LNA. Actually, this is smaller than the quality factor of the coil (Q=160). The main reason for this can be explained as follows: The LNA's input impedance cannot be considered infinitely high for the operating frequency of 123 MHz. Therefore, the finite value for Z_{LNA} lowers the value of the voltage at the output of the passive network. As a result, the obtained value of α is

smaller than Q. Nevertheless, α is still large enough to make $\alpha^2\overline{v_n^2}$ much higher the LNA's input referred noise $\overline{v_{a,n}^2}$, resulting in a calculated noise figure of 0.42 dB.

The calculation of the value for α depends on modelling the input impedance of the LNA. In most of the common CMOS models, a quasistatic model is assumed [73]. This model assumes no resistance at the gate of the MOS. However, there is an intrinsic resistance seen at the gate due to the finite charging time of the carriers at high frequencies. The existence of the gate resistance, r_g has been verified through simulation by using the non-quasistatic model. Figure 3.16 shows the gate circuit model of the LNA together with the passive network and the coil.

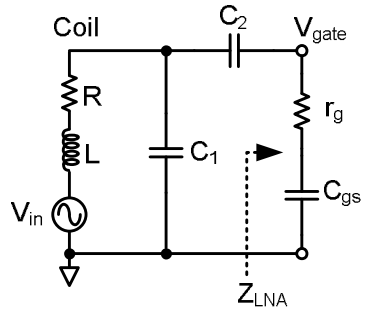

Figure 3.16. The gate circuit model of the LNA together with the passive network and the coil.

The voltage gain at the gate of the transistor can be expressed as:

$$\alpha = A_v = \left|\frac{V_{gate}}{V_{in}}\right| = \left|\frac{\dfrac{1}{\dfrac{1}{Z_{LNA}} + j\omega C_1}}{R + j\omega L + \dfrac{1}{\dfrac{1}{Z_{LNA}} + j\omega C_1}}\right| \tag{3.22}$$

where $Z_{LNA} = r_g + 1/j\omega C_{gs}$. It is important to note that C_2 in Figure 3.16 is selected large enough such that it is a short-circuit element at the operating frequency of 123 MHz. According to the simulations carried out by using the non-quasistatic model, the designed LNA has an input impedance $Z_{LNA} = 442 - j884\,\Omega$ at 123 MHz. For the coil parasitic

resistance of $R = 0.158\ \Omega$ given in Section 3.2.3, the value of α is calculated as 56.5 with the capacitance value C_1 of 51.5 pF.

3.3.1.1. Simulation Results. To validate the equations obtained previously for the performance parameters of the LNA, a comparison has been made with simulation results. Figure 3.17 shows the simulated voltage gain, α at the gate of the transistor M_1 versus frequency for the single-ended LNA. The simulated voltage gain of the passive network has a maximum value of 56.5 at 123 MHz.

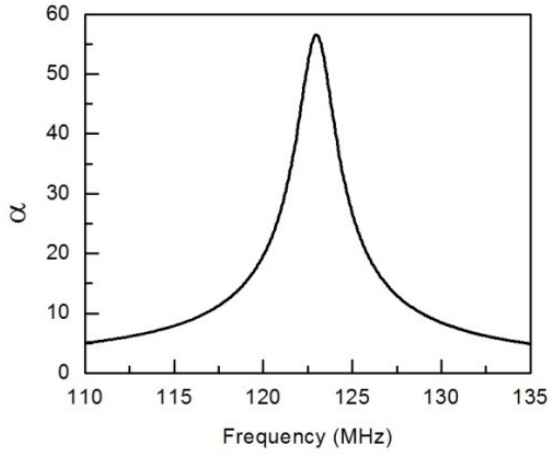

Figure 3.17. The simulated voltage gain, α versus frequency for the single-ended LNA

The noise figure simulation for the designed three-stage single-ended amplifier is shown in Figure 3.18. The simulated noise figure has a minimum value of 0.56 dB at 123 MHz. This is due to the fact that the voltage gain of the passive network has been maximized at this frequency by utilizing the noise matching method, as described previously. In addition, it is important to note that the calculated noise figure of 0.42 dB was solely for the first stage which is the LNA. Therefore, the difference between the simulated and calculated values comes from the noise contribution of the subsequent stages.

Figure 3.19 shows the overall gain of the designed three-stage amplifier with standard termination impedance, 50 Ω. The overall gain has a maximum value of approximately 60 dB at 123 MHz.

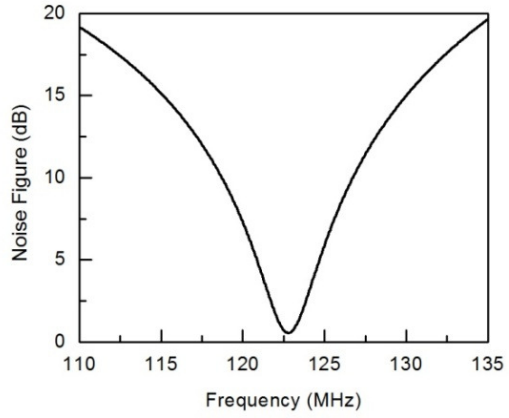

Figure 3.18. The noise figure simulation for the three-stage single-ended amplifier

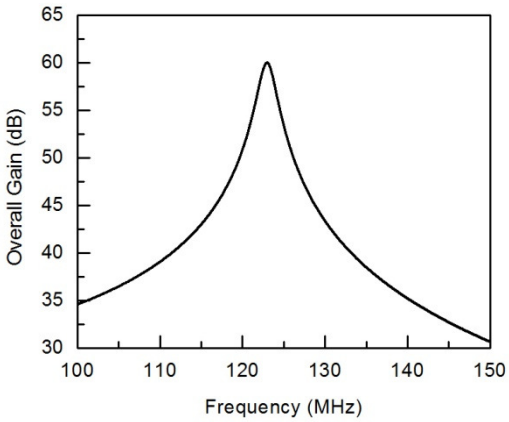

Figure 3.19. The overall gain of the designed three-stage amplifier with 50 Ω termination impedance

3.3.1.2. 1st Generation Chip Implementation & Measurement Results. The single-ended LNA is implemented in UMC 0.18 µm CMOS technology. Figure 3.20 shows the micrograph of the designed LNA and the test printed circuit board (PCB). The core of the LNA, which is about 500µm×230µm, draws 1.6 mA from a 1.4 V power supply.

In order to test the designed LNA, an RF signal at 123 MHz from a signal generator has been fed to the input of the LNA (node 1 in Figure 3.14), and the output at node 2 has been measured using a spectrum analyzer. Figure 3.21 shows the measured output signal when the input signal power is -78 dBm. From this, the voltage gain has been extracted to be approximately 25 dB which is in good agreement with the voltage gain of the LNA without the coil.

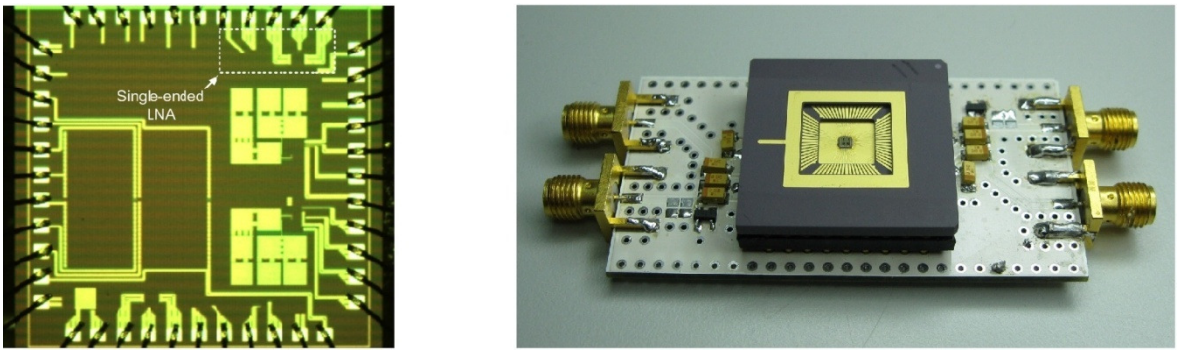

Figure 3.20. The micrograph of the single-ended LNA (1st Generation Chip) and test PCB

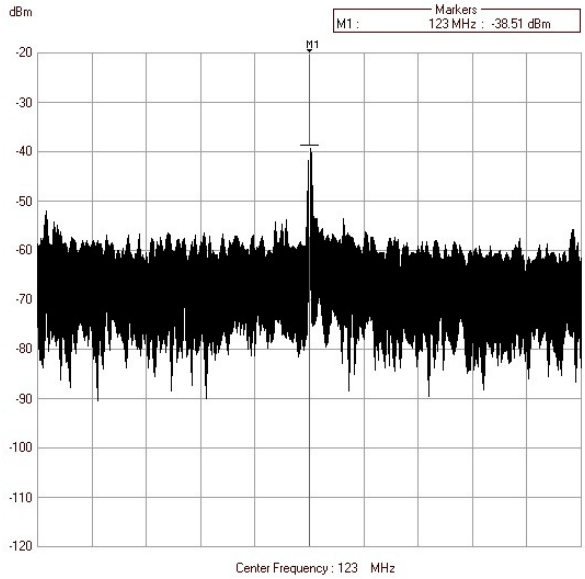

Figure 3.21. The measured output signal of the designed three stage single-ended amplifier

3.3.2 Ultra Low-Noise Differential Amplifier

Since the supply voltage of the receiver is provided from the integrated optoelectronic power supply unit containing a triple-well photodiode and DC/DC converter, as described in Chapter 2, it is essential to design a differential LNA which is more immune to supply noise arising from the digital part of the circuit, namely, the DC/DC converter.

Figure 3.22 shows the schematic of the designed two-stage fully-differential amplifier. The first stage is the ultra low-noise amplifier while the second stage is the voltage gain amplifier which drives the following analog circuitry in the receiver system,

namely, the Gilbert mixer. As seen from Figure 3.22, the ultra low-noise amplifier uses two equal resistors R_{cf} to cancel out the differential signals. In this way, a common-mode biasing voltage is generated for the gates of transistors M_3 and M_4. It is important to note that the upper part of this circuit belongs to both the common-mode and differential amplifier. Basically, M_3 and M_4 are DC current sources for the differential signals, but amplifiers for the common mode signals.

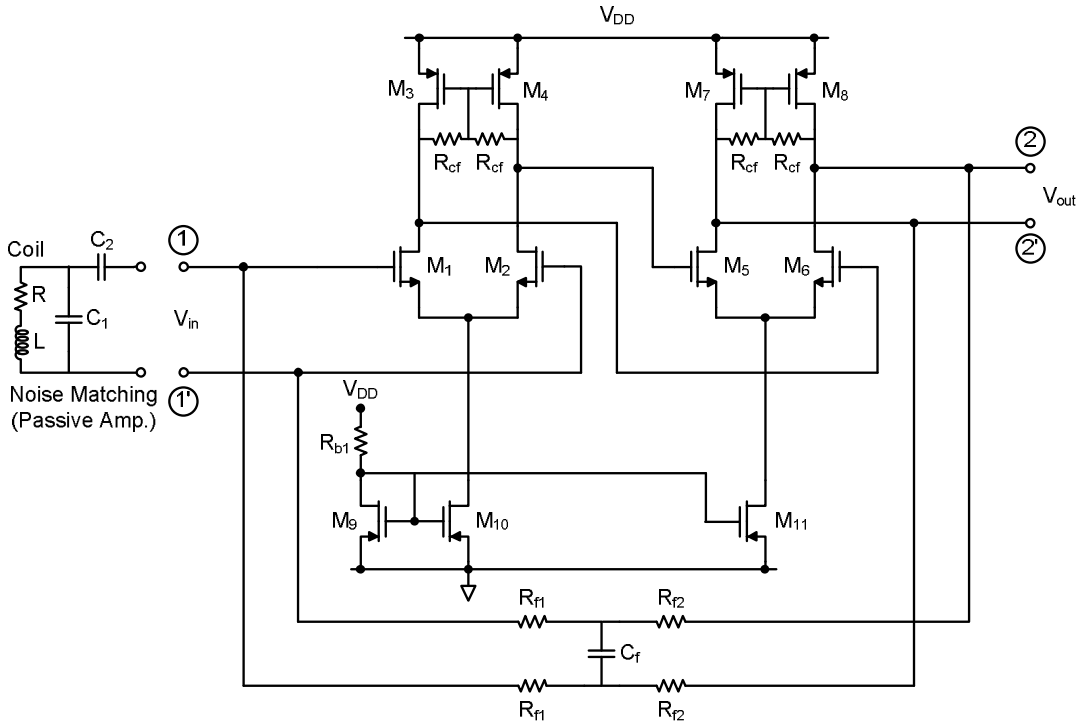

Figure 3.22. The schematic of the designed two-stage fully-differential amplifier

Since, the LNA stage consists of two equal halves that exhibit the same amount of noise, the input noise power for one half of the circuit has been calculated and simply multiplied by two in order to find the total noise of the LNA. The input referred total noise of the LNA can be expressed as

$$\overline{v_{a,n}^2} \approx 4kT\left[2\left(\frac{1}{g_{m1}^2 R_{cf}} + \frac{\gamma}{g_{m1}} + \frac{\gamma g_{m3}}{g_{m1}^2}\right)\right]\Delta f \tag{3.23}$$

where $g_{m1}$and g_{m3} are the transconductances of transistors M_1 and M_3, and R_{cf} is the common mode feedback resistance. As a result, the noise figure of the differential LNA

with the coil can be given as

$$NF \cong 10\log\left(1+\frac{\overline{v_{a,n}^2}}{\alpha^2\overline{v_n^2}}\right) = 10\log\left(1+\frac{2}{\alpha^2 R}\left(\frac{1}{g_{m1}^2 R_{cf}}+\frac{\gamma}{g_{M1}}+\frac{\gamma g_{m3}}{g_{m1}^2}\right)\right) \tag{3.24}$$

where α is the voltage gain of the passive network, and $\overline{v_n^2}$ is the thermal noise of the parasitic resistance, R of the coil. On the other hand, the gain of the LNA can be expressed as

$$A_v = g_{m1}(R_{cf} \,//\, r_{o1} \,//\, r_{o3}) \tag{3.25}$$

where $r_{o1}$and r_{o3} are the output resistances of transistors M_1 and M_3. From (3.24) and (3.25), it is obvious that low noise figure and high gain can be obtained when g_{m1} and R_{cf} are large enough. However, the current consumption budget of the differential LNA is restricted to a maximum value of 1 mA for the presented design. With the selected transconductance value of $g_{m1} = 6.3\,mS$ and $R_{cf} = 10\,K\Omega$, the noise figure of the LNA can be calculated by using equation (3.24). Figure 3.23 shows the noise figure of the differential LNA versus the voltage gain of the passive network, α for the coil parasitic resistance of $R = 0.158\,\Omega$.

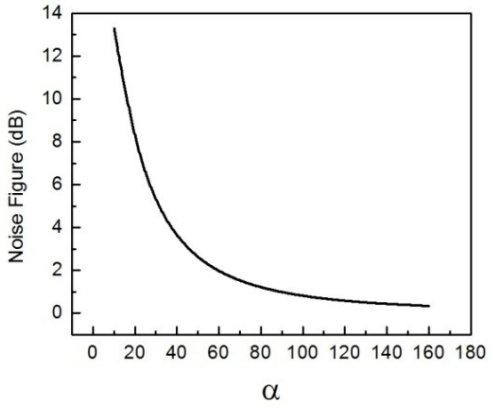

Figure 3.23. The noise figure of the differential LNA vs. the voltage gain of the passive network, α

It is important to remind that the value of α plays an important role in determining the noise figure of the LNA with the coil, as previously described in Section 3.2.4. The simulated value of α is approximately equal to 128.5 for the designed LNA which is smaller than the quality factor of the coil (Q=160). This is due to the fact that the designed LNA's input impedance, Z_{LNA} has a finite value of $1345 - j4445\ \Omega$ at the operating frequency of 123 MHz. Nevertheless, α is still large enough resulting in a calculated noise figure of 0.51 dB for the differential LNA with the coil when $\gamma = 1$. Since, the voltage gain of the presented LNA is approximately 16.5 for $g_{m1} = 6.3\,mS$, $R_{cf} = 10\,K\Omega$, and $r_{o1}\,//\,r_{o3} \cong\ 3.5\,K\Omega$, the noise contribution of subsequent stages can be considered to have negligible effect in the noise performance of the designed two-stage differential amplifier.

Finally, the voltage gain amplifier following the LNA stage in Figure 3.22 has been designed for an additional voltage gain of approximately 6. This stage consumes a current of approximately 0.2 mA, and the total current consumption of the designed two-stage amplifier is about 1.2 mA.

3.3.2.1. Simulation Results. Figure 3.24 shows the simulated voltage gain of the passive network, α versus frequency for the differential LNA. The value of α reaches its maximum value of 128 at the operating frequency of 123 MHz while the gain of the LNA is almost flat over the frequency spectrum and equal to 14.5.

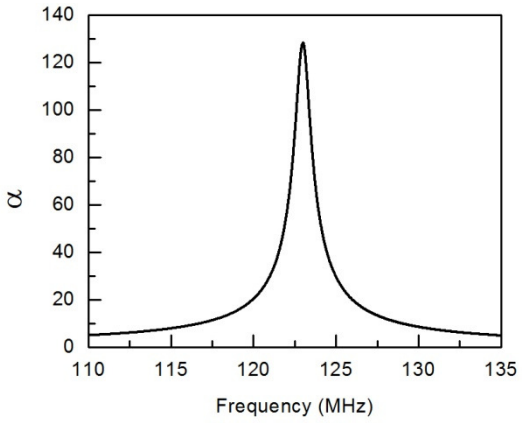

Figure 3.24. The simulated voltage gain of the passive network, α versus frequency for the differential LNA

The noise figure simulation for the designed three-stage differential amplifier is shown in Figure 3.25. The simulated noise figure has a minimum value of 0.67 dB at 123 MHz. This is due to the fact that the voltage gain of the passive network has been maximized at this frequency by utilizing noise matching method, as described previously.

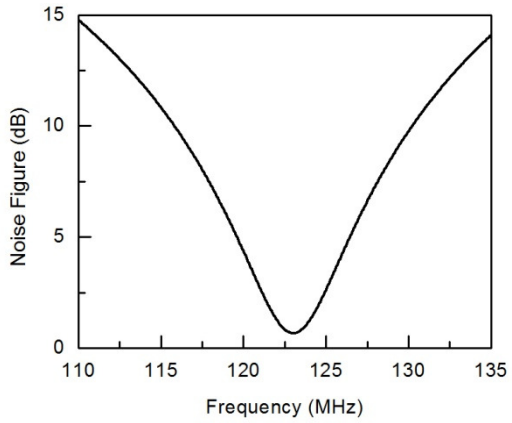

Figure 3.25. The noise figure simulation for the three-stage differential amplifier

3.3.2.2. 2nd Generation Chip Implementation & Measurement Results. The two-stage fully-differential amplifier is implemented in UMC 0.18 µm CMOS technology. Figure 3.26 shows the micrograph of the 2nd generation chip consisting of the designed two-stage differential amplifier. The core of the two-stage amplifier, which is about 105µm×215µm, draws 1.4 mA from a 1.2 V power supply.

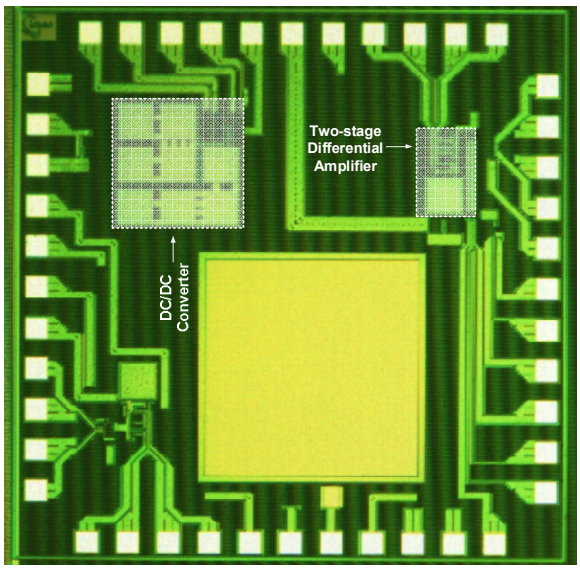

Figure 3.26. The micrograph of the 2nd generation chip

In order to test the amplifier individually, a buffer circuit as shown in Figure 3.27 has been added in order to be able to drive 50-Ω impedance. Therefore, all of the measurements that will be presented in this section include the effect of the buffer as well.

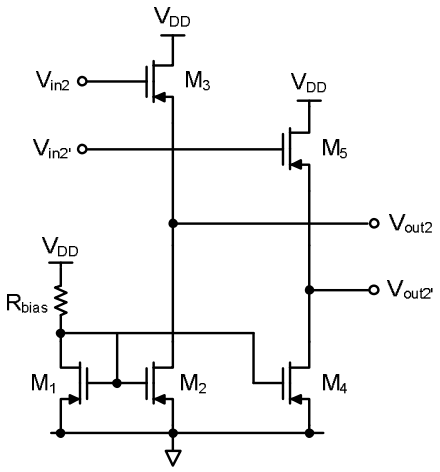

Figure 3.27. The buffer circuit

Figure 3.28 shows the block diagram of the PCB that has been used to test the designed amplifier. Basically, the PCB consists of balun circuits and the 2nd generation chip. Basically, an RF signal at 123 MHz from the signal generator (Rohde & Schwarz SMB100A) has been fed to the input of the amplifier (IN), and the output (OUT) has been measured using the spectrum analyzer (Rohde & Schwarz FSH6).

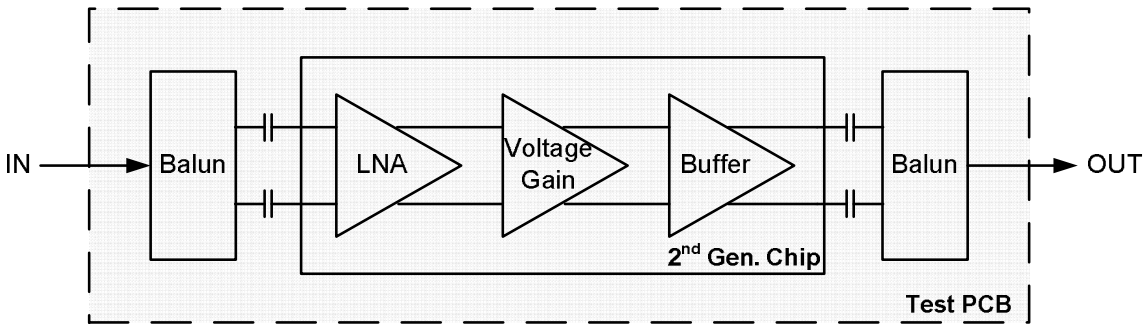

Figure 3.28. The block diagram of the PCB for testing

Figure 3.29 shows the measured output signal which is -49.68 dB when the input signal power is -80 dBm. Therefore, S_{21} is about 30 dB which is in good agreement with the simulated value of 34.8 dB. The difference between these values is due to the insertion loss of the balun circuits and the parasitics of the PCB.

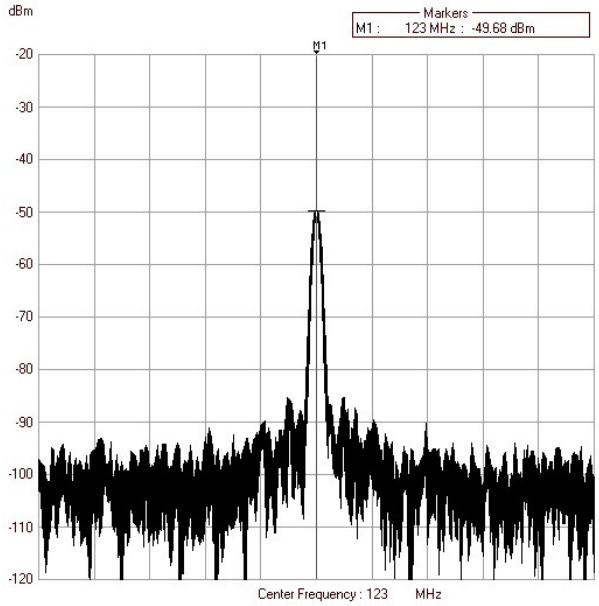

Figure 3.29. The measured output signal of the differential LNA

In order to verify the measurement result given above, the S_{21} parameter of the amplifier has also been measured with the vector network analyzer (Rohde & Schwarz ZVB4). Figure 3.30 shows the measured S_{21} parameter. In the frequency range of 150 kHz–400 MHz, S_{21} decreases from 31 dB to 16 dB. At 123 MHz, S_{21} is about 29.2 dB.

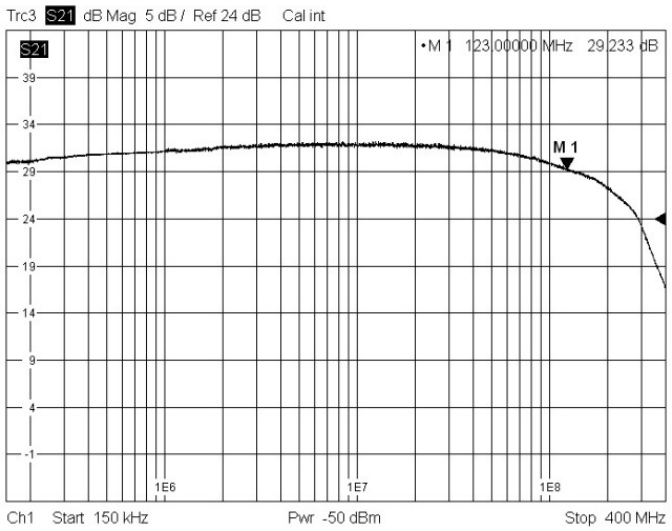

Figure 3.30. The measured S_{21} parameter

Finally, the input referred 1-dB compression point which is measured as -38 dBm is shown in Figure 3.31.

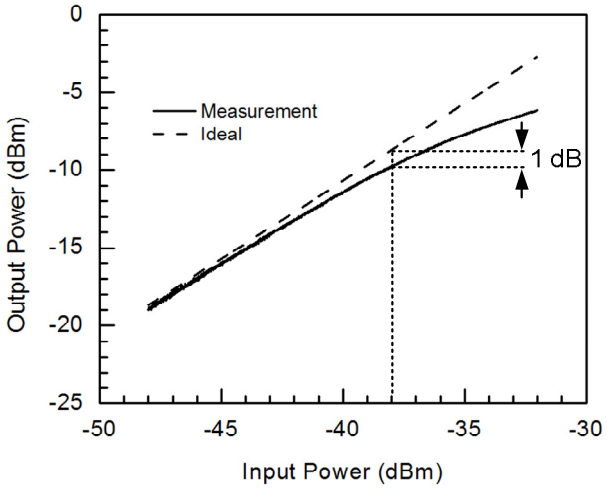

Figure 3.31. The input-referred 1-dB compression point

Since, the RF measurement devices are designed for 50 Ω input impedance systems, it is not easy to measure the noise figure of the presented amplifier with the coil antenna. Therefore, a technique combining both measurement and analytical calculation has been used in here to project the noise figure. Basically, the noise figure of the amplifier has been measured using an HP 8970B noise figure meter as 7.3 dB with respect to 50 Ω at 123 MHz. This measured noise figure has been used to extract the input referred noise of the amplifier, $\overline{v_{a,n}^2}/\Delta f$ according to the following equation:

$$NF = 10\log\left(1 + \frac{\overline{v_{a,n}^2}/\Delta f}{\overline{v_{n,ref}^2}/\Delta f}\right) \tag{3.26}$$

where $\overline{v_{n,ref}^2}/\Delta f$ is the thermal noise of the input impedance, 50 Ω. The extracted value of $\overline{v_{a,n}^2}/\Delta f = \left(1.9\, nV/\sqrt{Hz}\right)^2$ for the measured noise figure of 7.3 dB can be used to calculate the noise figure of the LNA with the coil. Since, the simulated value of α is 128, and the parasitic resistance of the coil, R is 0.158 Ω, the noise figure expression in (3.26) can be evaluated by using the thermal noise of the coil's translated impedance, $\overline{v_{n,ref}^2}/\Delta f = 4kT\alpha^2 R$. The calculated noise figure is 0.35 dB for the overall amplifier. However, this value cannot be considered completely reliable since the exact value of α is not available through measurement.

3.4 Mixer Circuit

Mixers are essential components that perform frequency translation in RF transceiver systems. A downconversion mixer utilized in a receiver path has two different input ports, namely, the RF port and the local oscillator (LO) port. The RF port senses the signal to be downconverted and the LO port senses the periodic waveform generated by a local oscillator. Ideally, the downconversion mixer multiplies these input signals to produce the frequency translated output signal at the IF port.

There are many different mixer circuit topologies and implementations that are suitable for use in receiver systems. However, the Gilbert mixer is the most widely used double-balanced mixer topology in RF applications because of its compact layout and moderately high performance [65]. More specifically, this mixer topology provides reasonable conversion gain (IF power output with respect to the RF power input) and good rejection at the RF and LO ports. [74,75]

Figure 3.32 shows the active-loaded configuration of the Gilbert mixer [74] utilized in the receiver presented in this thesis. Basically, the circuit consists of three parts; a transconductance stage, an LO switch stage, and an active load stage. The RF input signal is amplified in the transconductance stage, downconverted to an IF current signal in the LO switch stage, and then converted to a voltage signal by the active load stage.

In the presented receiver system in this work, the output (nodes 2-2') of the two-stage amplifier, previously shown in Figure 3.22, is directly connected to the RF port of the mixer while the external LO signal is capacitively coupled to the mixer. The output of the mixer is connected to a resistor-capacitor (RC) low-pass filter in order to eliminate the high frequency output component.

The mixer circuitry is designed to have a voltage conversion gain of at least 20 dB with a current consumption budget of 0.25 mA [76]. The voltage conversion gain can be expressed as

$$A_v = g_m R_L \tag{3.27}$$

where $g_m$is the transconductance of M_1 and M_2 , and R_L is the effective load resistance of the mixer. In fact, R_L is determined by the input impedance of the RC filter. In order to satisfy the voltage conversion gain requirement for the mixer, a transconductance of 1mS has been selected for a defined R_L of 16 $K\Omega$. A gate voltage of 0.8 V has been selected for the transistors in the LO switch stage in order to guarantee the saturated operation of transistors (M_1 and M_2) in the transconductance stage for a supply voltage V_{DD} of 1.2 V.

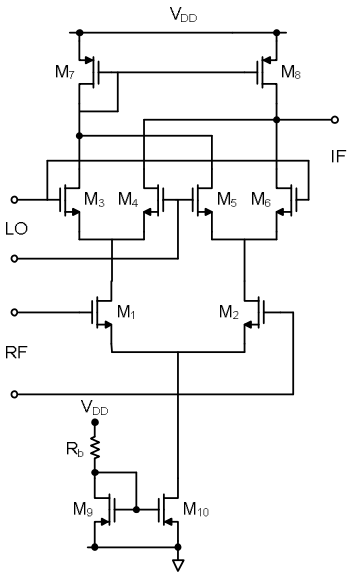

Figure 3.32. Active-loaded Gilbert mixer configuration [74]

The voltage gain (without the coil) of the previous stage which consists of the LNA and the voltage gain amplifier is about 37.5 dB. When the coil is used, the gain of the passive network adds to the specified gain, resulting in an overall voltage gain of 79.6 dB. An input RF signal of 1 μV amplitude on the coil is amplified to a voltage of 9.55 mV at the input of the mixer. Figure 3.33 shows the simulated single sideband noise figure of the mixer at the operating frequency of 123 MHz versus LO power. The power of LO signal has been selected as 0 dBm in order to minimize the noise figure of the mixer. The simulated noise figure is 5.5 dB at the LO power of 0 dBm. Actually, the effect of the noise figure of the mixer on the entire receiver noise performance is quite negligible due to the fact that the overall gain of the preceding stages is 37.5 dB.

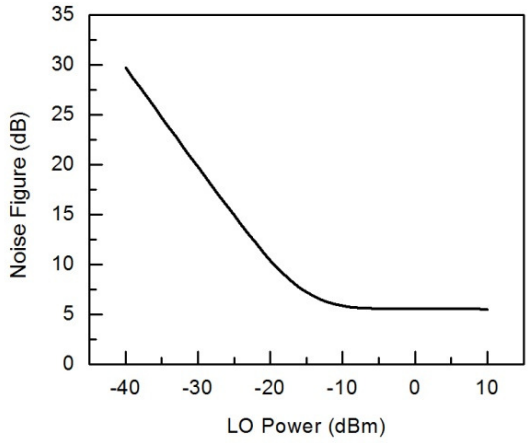

Figure 3.33. The single sideband noise figure of the mixer at 123 MHz vs. LO power

Figure 3.34 shows the simulated downconversion gain versus LO power. The downconversion gain is about 18.1 dB for the selected LO power of 0 dBm. In addition, the designed circuit has a simulated voltage conversion gain of 22.8 dB at the output of the RC filter. The mixer circuitry is implemented in UMC 0.18 µm CMOS technology, and its core size is about 200µm×130µm.

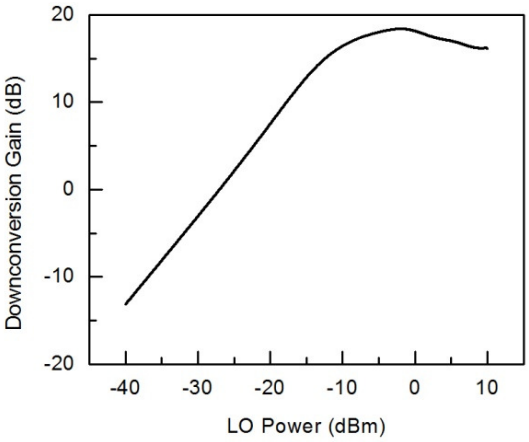

Figure 3.34. The simulated downconversion gain vs. LO power

Figure 3.35 shows the simulated IF signal power versus RF signal power. For the simulation, the RF power has been applied with a power source that has the output impedance of the preceding stage, namely the voltage gain amplifier. The input referred 1-dB compression point is -48 dBm for the designed mixer circuit.

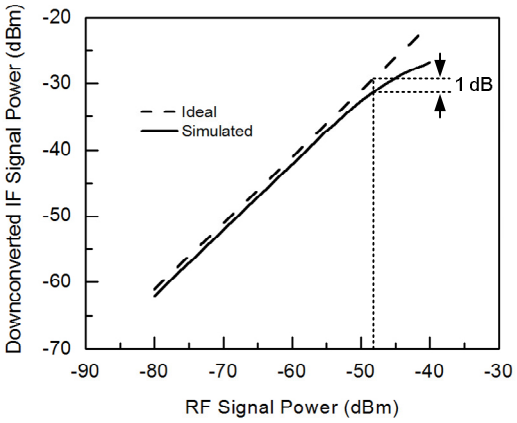

Figure 3.35. The simulated IF signal power vs. RF power

3.5 The Receiver Front-End Performance

Figure 3.36 shows the receiver front-end presented in this thesis that consists of a coil antenna, a differential LNA, a voltage gain amplifier, an active loaded mixer, and a low-pass filter. This thesis has aimed to design the most important parts of the receiver front-end system namely, the LNA and the voltage gain stages. The overall front-end circuit consumes a total current of 1.65 mA from a 1.2 V supply voltage.

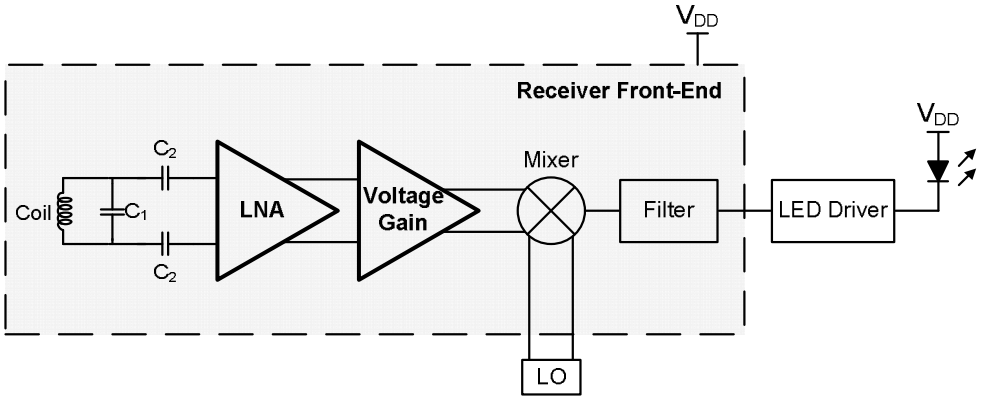

Figure 3.36. The receiver front-end

The performance of the receiver front-end has been tested without the coil. Figure 3.37 shows the block diagram of the test PCB for the receiver front-end. Basically, an RF signal with a power level of −80 dBm has been applied to the RF input of the receiver front-end, and the frequency of the signal has been swept continuously between 122.8

MHz and 123.2 MHz. In addition, an LO signal with a power level of 0 dBm at 121.8 MHz has been applied to the LO input of the designed front-end. For the test purpose, a practical load impedance, R_{LED} of 100 Ω has been used. The output of the circuit, which has been measured as −40 dBm with the spectrum analyzer, is shown in Figure 3.38.

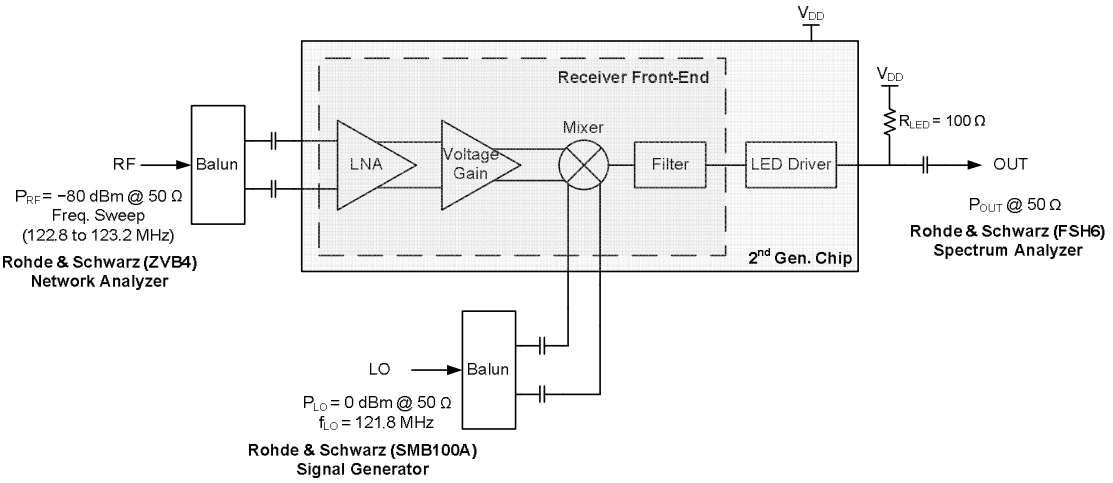

Figure 3.37. The block diagram of the test PCB for the receiver front-end

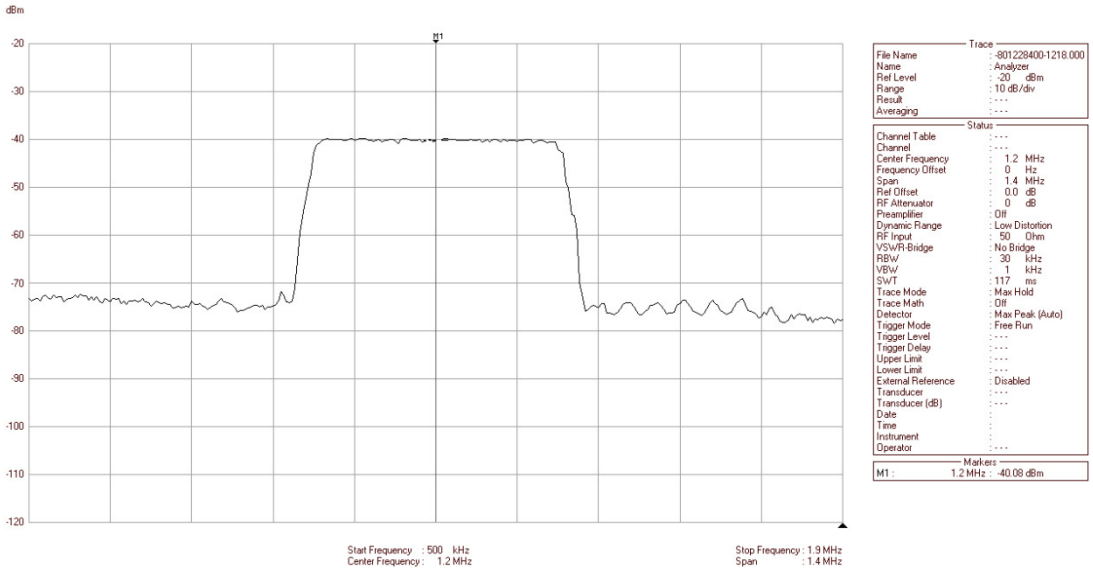

Figure 3.38. The output of the 2nd generation chip (P_{out}) measured with spectrum analyzer

The gain of the overall circuit is quite flat and equal to 40 dB for the selected bandwidth. This result is in good agreement with the simulations of the receiver front-end together with the LED driver circuitry that has been used in the tests. More importantly, the designed front-end circuit performs frequency translation operation correctly. As seen

from Figure 3.38, the frequency of the output signal changes from 1 MHz (f_{RF} = 122.8 MHz, f_{LO} = 121.8 MHz) to 1.4 MHz (f_{RF} = 123.2MHz, f_{LO} = 121.8 MHz).

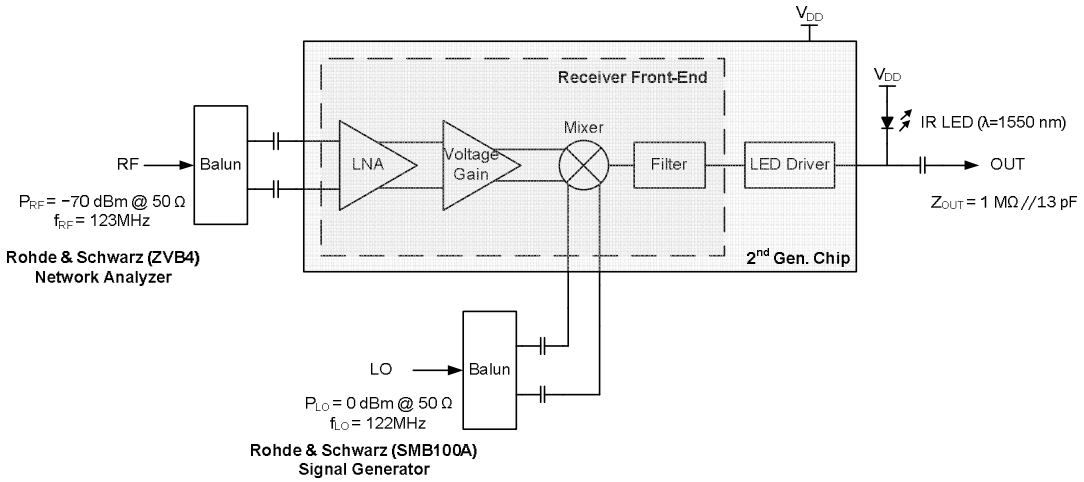

Figure 3.39. The measurement set-up for the receiver front-end with an IR LED Die

In addition, the designed receiver front-end circuit has been tested with an IR LED die from Roithner Lasertechnik (C155-30). Figure 3.39 shows the measurement set-up and the applied inputs to the receiver front-end circuit. The output of the overall circuit, which has been measured with the oscilloscope, is shown in Figure 3.40. The output has a DC voltage of 510 mV and a peak-to-peak AC voltage of 45.6 mV. In addition, the frequency of the output signal is 1 MHz (f_{RF} = 123MHz, f_{LO} = 122 MHz) as expected.

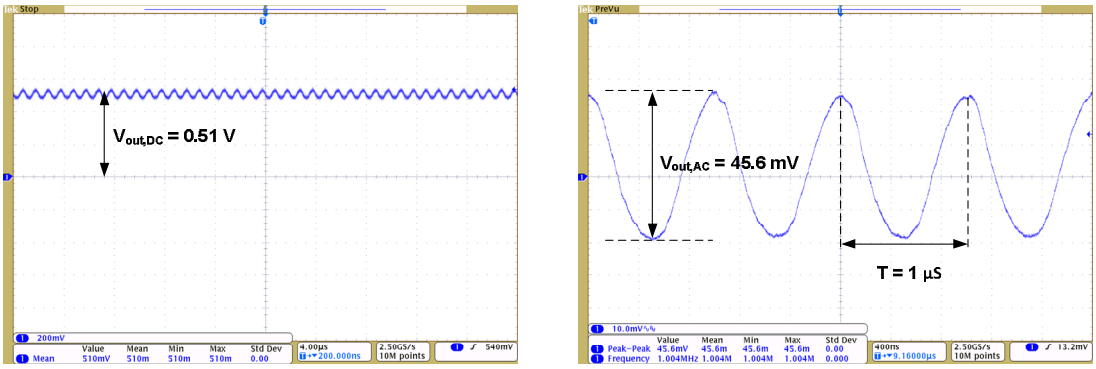

Figure 3.40. The output of the 2nd generation chip measured with oscilloscope

Since, the supply voltage of the overall circuit is 1.2 V, the DC voltage on the LED die is equal to 0.69 V. Figure 3.41 shows the measured I-V characteristic of the LED die

utilized in the measurements. Basically, a peak-to-peak AC voltage of 45.6 mV translates into a peak-to-peak AC current of approximately 1 mA.

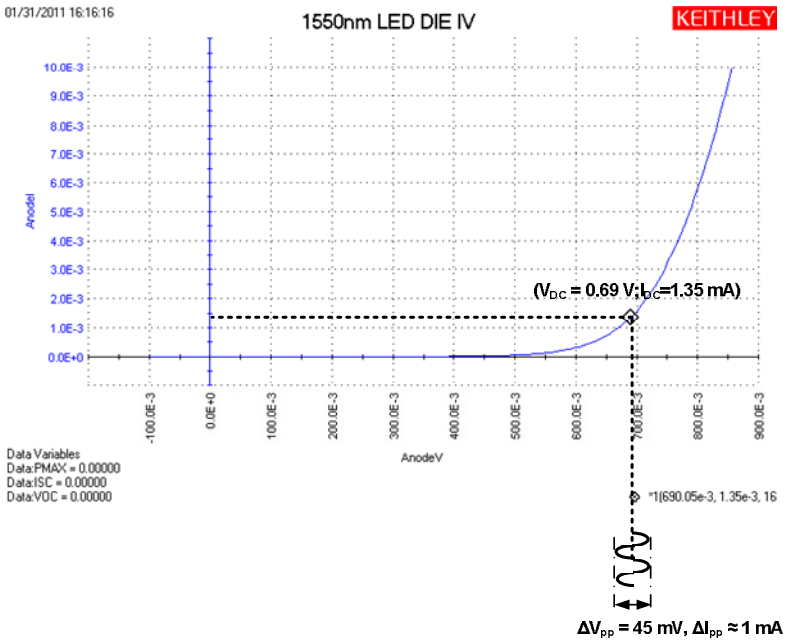

Figure 3.41. The measured I-V characteristic of the LED die

Finally, the measurement set-up, which is shown in Figure 3.42, has been constructed by Baykal Sarioglu and Umut Cindemir. Basically, a laser beam at a wavelength of 650 nm is focused onto the triple-well photodiode using a convex lens. In order to be able to supply the high current level that is required by the receiver front-end, the transmission gate in the power supply unit has been fed with an appropriate control signal having a duty cycle of 10 %. Therefore, it is important to note that the receiver front-end circuit is powered intermittently. In addition, RF and LO inputs of the receiver front-end are fed with signals of -70 dBm and 0 dBm power levels, respectively.

Figure 3.43 shows both the measured output voltage (V_{OUT}) of the LED driver circuitry and the supply voltage, V_{DD} of the overall optically powered receiver front-end circuit. During the operation of the receiver front-end, the supply voltage, V_{DD} decreases from 1.35 V to 1.15 V. This translates into a measured value for the output voltage of the LED die that decreases from 0.65 V to 0.45 V. Since, the average value for V_{DD} is approximately 1.2 V for the duration the overall system is powered on, the receiver front-end circuit performs as expected. In addition, the average value for the output voltage is

0.55 V and is in good agreement with the measurements conducted with the emulated LED load resistance of 100 Ω. However, it is important to note that only the envelope of the amplified RF signal is visible in the circle shown in Figure 3.43. Therefore, Figure 3.44 shows V_{OUT} in a larger scale for the duration previously shown in the circle. The output voltage has a peak-to-peak AC voltage of 50 mV. Moreover, the frequency of the output signal is 1 MHz (f_{RF} = 123MHz, f_{LO} = 122 MHz) as expected.

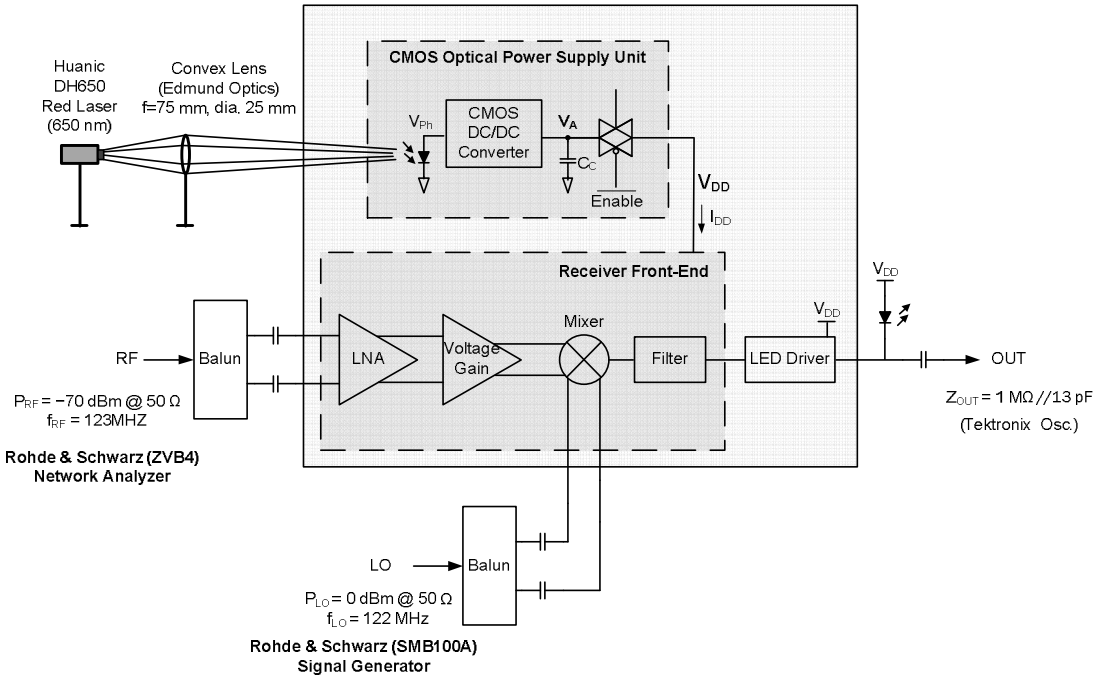

Figure 3.42. The measurement set-up for the optically powered receiver front-end

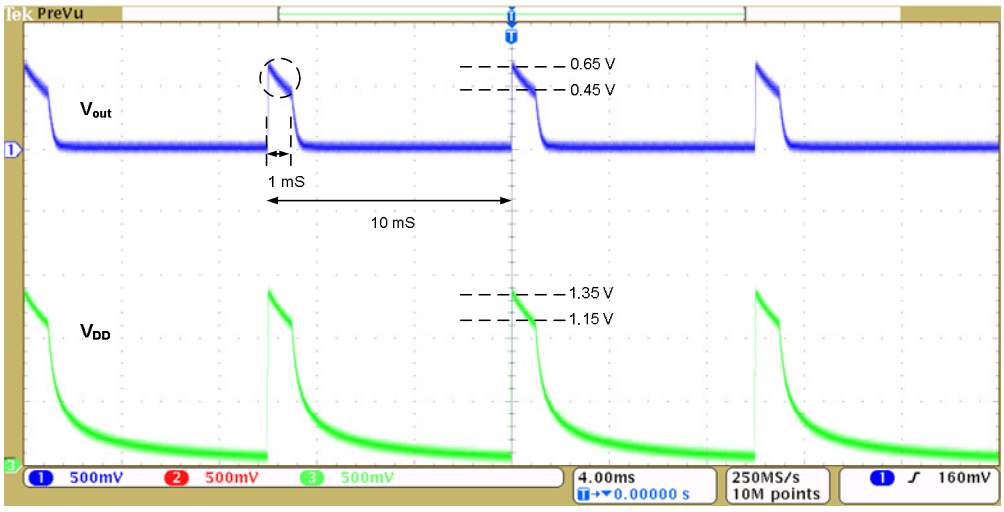

Figure 3.43. The measured output voltage (V_{OUT}) of the LED driver circuitry and the supply voltage, V_{DD} of the overall optically powered receiver front-end circuit

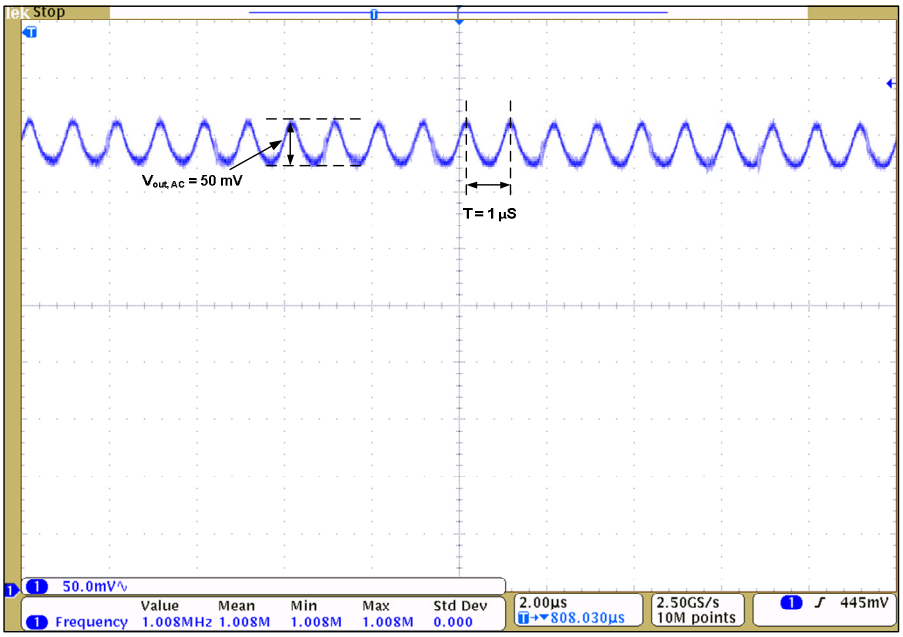

Figure 3.44. The measured output voltage, V_{OUT} of the LED driver circuitry shown in a larger scale for the overall optically powered receiver front-end circuit

4. CONCLUSIONS

In this thesis, the design approaches and methodologies have been presented to realize an optically powered CMOS receiver front-end for electrically isolated applications. The research is firstly concentrated on developing a miniaturized optical power supply unit for the operation of the overall system. In this context, utilizing integrated photodiodes in a standard unmodified sub-micron CMOS process as the optical-to-electrical converters has been explored. Due to the technical issues hindering the series connection of CMOS photodiodes on the same die, an architecture which consists of a single triple-well CMOS photodiode connected to a DC/DC voltage converter circuit has been presented. Based on this architecture, a novel optical power supply unit compatible with standard CMOS foundry processes has been developed. The measurements revealed that on-chip triple-well photodiode offers a projected responsivity of 0.026 A/W. In addition, the designed CMOS DC/DC converter has a maximum efficiency of 56% and is able to increase the photodiode voltage of 0.5 V and 0.6 V to 1.2 V and 1.5 V, respectively. The integrated circuit, which contains monolithic triple-well photodiode next to the DC/DC converter circuit, can be integrated into a miniaturized system where a micromachined silicon fiber platform carries optical power to be converted into the electrical one. Since overall size of the system is small, it can be safely used to supply power to the electronic systems which operate in harsh environments.

The presented integrated system is able to deliver 200 µA of bias current with a 1.2 V of supply voltage to an electronic system continuously, when an external optical power of 200 mW is given as the input. Improvement of the overall power efficiency can be achieved by decreasing the optical wavelength. Since, the depth of n-well or p-well is only about 1.2 µm while the penetration depth of photons with wavelength of 650 nm in silicon is around 3 µm, a fraction of photons are absorbed outside the depletion region of a photodiode. However, decreasing the wavelength leads to a shallower penetration depth, and the portion of the photons absorbed inside the depletion region may be increased which results in a higher efficiency photodiode. According to the obtained measurement results, it is projected that the same electrical power from an optical power of 200 mW can

be achieved with an optical power of 33.5 mW, if dummy metal pattern over the photodiode is removed.

In the second part of this thesis, a receiver front-end that consists of an LNA, voltage gain amplifier, a mixer and a low-pass filter has been presented. However, this thesis aimed to design the most important parts of the receiver front-end namely the LNA and the voltage gain amplifier. The design strategy for the LNA is different from the widely practiced method of impedance matching. The utilized technique so-called noise-matching enables a fully-integrated receiver solution with an ultra low-noise performance. The differential LNA consumes 1.4 mA from a 1.2V supply voltage and has a measured S_{21} of 30 dB. In addition, the noise figure of the LNA has been measured as 7.3 dB with respect to 50 Ω. This translates into a projected noise figure of 0.35 dB when the LNA is used with an example solenoid coil given in this thesis.

The overall receiver front-end has been tested electrically with a LED driver circuitry. The measurement results showed that the receiver front-end performs frequency translation operation correctly for the bandwidth of interest. Finally, the receiver front-end has been powered optically and tested again with the LED driver circuitry connected to a commercially available IR LED die. The measurement results showed that the utilized LED die can be modulated with a peak-to-peak voltage of 50 mV when the RF input power level is as low as -70 dBm.

The work presented in this thesis has concerned the realization of an optically powered receiver front-end. To design the presented system, the specifications of an application, namely active catheter localization in MRI systems have been chosen. The future work includes the exploration of the back-end design in order to demonstrate the presented system for the specific application.

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