ASYNCHRONOUS SIGMA-DELTA ANALOG TO DIGITAL CONVERTERS

by

Balkır Kayaaltı

B.S, Microelectronics, Electrical and Electronics Engineering Department, 2000

M.S, Microelectronics, Electrical and Electronics Engineering Department, 2003

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APPROVED BY:

Prof. Ömer Cerid (Thesis Supervisor)	.....
Prof. Günhan Dündar	.....
Prof. Uğur Çilingiroğlu	.....
Prof. Oğuzhan Çiçekoğlu	.....
Assoc. Prof. Johannes Hegt	.....

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ABSTRACT

ASYNCHRONOUS SIGMA-DELTA ANALOG TO DIGITAL CONVERTERS

Analog to digital conversion is the process of translating analog real world signals to their corresponding binary encoded form which digital devices need. Among the examples for analog signal sources storage devices like harddisks and sensor devices can be given. Analog to digital converters are key components that make this translation. There are different types of analog to digital converter circuits. A specific topology can be selected according to its achievable number of bits, speed, power and according to its area of usage. Sigma-delta analog to digital conversion is a popular type which can be used in applications where high resolution with moderate bandwidth is desired. High resolutions are achieved due to the consequence of the inherent noise suppression by the loop filter. Oversampling, which corresponds to the sampling of the input signal with a higher rate than that of the regular Nyquist rate is their other advantage. This process pushes the quantization noise away from the baseband, and thereby higher signal to noise ratios are achieved. There are mainly two sub-types of sigma delta converters. The first, is the discrete time version which uses discrete time signals and components. The second is the continuous time version which uses entire continuous time signals and components except the quantizer and the Digital to analog converter (DAC) in the feedback. These two types are both clocked with an external clock signal, so the output is synchronous i.e. synchronized with a clock. Designing a new type of the circuit which does not use an external clock; but instead using the self oscillation created in the converter loop can be a an alternative third type. This type of the converter will not use sampling process inside the loop, so clock jitter due to the sampling can be eliminated in the sigma-delta loop, where usually a high frequency signal is sampled. If the sampling is done with a lower frequency compared to the one in the loop, effect of the clock jitter can be reduced. Asynchronous sigma-delta

converters contain some nonlinear control theory concepts such as limit cycle periodic modes of the loop and the presence of the quantizer nonlinearity on the spectrum and performance. This thesis is about the theory of such converters and their design procedure with a real circuit implementation.

ÖZET

ASENKRON SİGMA-DELTA ANALOG DİJİTAL ÇEVİRİCİLER

Analog dijital çeviriciler gerçek kaynaklı analog sinyalleri dijital kodlanmış hallerine çeviren araçlardr. Bu dijital sinyaller, ardından gelen dijital sinyal işleme devrelerinde kullanılır. Analog sinyal kaynaklarına harddisk gibi kayıt cihazları ve optik sensörler örnek olarak gösterilebilir. Analog dijital çeviricilerin bir çok çeşidi vardır. Barındırdıkları avantaj ve dezavantajlara gõre istenilen bir topoloji seçilebilir. Delta-sigma analog dijital çeviriciler sağladıkları yüksek çözünürlük sayesinde günümüzde oldukça yaygın ve popülerdirler. Yüksek çöznürlük devredeki filtrenin içsel gürültü bastırmasından kaynaklanır. 'Yüksek örnekleme' yani işaretin standart 'Nyquist örnekleme' frekansından daha yüksek bir frekansla örneklenmesi ile basamaklama gürültüsü sinyal bandından uzağa doğru itilir. Böylelikle daha yüksek işaret gürültü oranı elde edilir. Sigma-delta analog dijital çeviriciler iki çeşittir. Birincisi örneklenmiş işaretler ve örnekleyici devre elemanları ile çalşan örneklenmiş zaman sigma delta çeviricilerdir. İkinci çeşit ise, sürekli zaman işaret ile çalışan ve basamaklayacı hariç sürekli zaman devre elemanları kullanan sürekli zaman delta sigma çeviricilerdir. Bu iki devre de senkron devrelerdir; yani dşarıdan verilen bir saat sinyaline senkronizedir. Dışardan bir saat işareti verilmeksizin kendi salınımlarını üretip kullanan yeni bir çevirici mevcut ikisine yeni bir alternatif olacaktır. Bu devre dışarıdan bir saat işareti almayacağı için, saat seğirmesi engellenecektir. Bu tip çeviricilerde daha önce karşılaşılmayan limit döngü ve doğrusal olmayan basmaklayıcının yarattğı distorsiyon etkileri vardır. Bu tez bu tip çeviricilerin matematiksel analizi ve devre gerçeklemesi ile ilgilidir.

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LIST OF SYMBOLS/ABBREVIATIONS

A_{CM}	Differential gain
A_{DC}	Zero frequency gain
A_{dif}	Common mode gain
C_{gd}	Gate to drain capacitance
C_I	Integration capacitance
g_{ds}	Drain to source transconductance
g_m	Gate transconductance
Λ	Tsypkin fuction
$\Sigma - \Delta$	Sigma-Delta
ω_u	Unity gain frequency
ADC	Analog to Digital Converter
AMS	Austrian Micro Systems
ASDM	Asynchronous Sigma-Delta Modulator
CIC	Cacaded Integrator Comb
DAC	Digital to Analog Converter
DF	Sinusoidal Describing Function
FFT	Fast fourier transform
FOM	Figure of Merit
FIR	Finite Impulse Response
HDTV	High definition television
IIR	Infinite Impulse Response
IM3	Third Harmonic Intermodulation
kHz	Kilo Hertz
LSB	Least significant bit
MHz	Mega Hertz
MOS	Metal Oxide Semiconductor
Msps	Megasamples per second

NTF	Noise Transfer Function
PCM	Pulse Code Modulation
PWM	Pulse Width Modulation
OSR	Over Sampling Ratio
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SINAD	Signal to Noise and Distortion
SNR	Signal to Noise Ratio
VDD	Drain to Drain Voltage
Vgs	Gate to Source Voltage
VSS	Source to Source Voltage
xDSL	Digital subscriber lines

1. INTRODUCTION

1.1. Motivation for Asynchronous Sigma-Delta Analog to Digital Conversion

Signal processing is the art of shaping an electrical signal, by means of linear and nonlinear circuit elements which transform an input signal to a desired output signal. In the years till 70's, signal processing was done in purely analog domain. With the advances in electronic fabrication techniques; it was possible to integrate many digital devices in a small area and digital signal processing became more popular. Despite numerous advantages of the digital domain, some of the signal path is still analog, thus some signal processing still has to be done in the analog domain. Mixed signal circuits where analog and digital signals are translated to each other, are receiving much attention due to their impact on the performance of the whole signal processing circuit. Analog to digital conversion is the process to convert the analog signal to digital codes. Different types of analog to digital converters (ADC) offer different performance parameters such as: conversion rate, resolution, power consumption and dynamic range. Some ADC types can be given as: successive approximation, integrating, flash, pipe-line and sigma delta. The most popular ones are flash, pipe-line and sigma delta.

Integrating ADC's are used in very slow applications such as instrumentation and have limited usage.

Successive approximation register (SAR) ADC's are mainly used for speeds up to 5 megasamples per second (Msps). They achieve resolutions from 8 to 16 bits with low power consumption. Therefore they are used widely in portable battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition. Their main disadvantage is the high performance requirement of the DAC and comparator inside the ADC structure used internal. Because of its internal search algorithm, the comparator works at higher speed than the ADC. The used comparator should be very

fast and low input referred noise. Therefore, offset cancellation techniques are widely used. The DAC should also be accurate and needs to be calibrated.

Flash analog-to-digital conversion is the fastest way to convert an analog signal to a digital signal. A typical flash ADC diagram is given in Fig. 1.1. A N-bit Flash ADC is composed of 2^{N-1} comparators. A resistive-divider with 2N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator below it. Each comparator produces a high output when its analog input voltage is higher than the reference voltage applied to it. This type of converter is also known as parallel ADC. They are mainly used where large bandwidths are required. Typical used areas include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives. They consume considerable power. The resolution is limited usually to 8-bits, due to component matching limits. Also, every additional bit causes doubling the die area. Achievable Signal to Noise Ratio (SNR) is highly degraded when clock jitter is present, especially at high input frequencies.

The pipelined analog-to-digital converter (ADC) architecture have received interest due to their wide range of sampling rates from a few megasamples per second (MSPS) up to hundreds Msps. Typical pipelined ADC is given in Fig. 1.2. Resolutions range from 8 bit at high sample rates to 16 bit at low rates. This performance metrics makes it suitable to be used in applications including CCD imaging, ultrasonic medical imaging, digital receivers, base stations, digital video (for example, HDTV), xDSL, cable modems, and fast ethernet. The resolution limitation is due to the capacitor and resistor mismatches of the components used inside.

Among the other analog to digital converters, Sigma-Delta ($\Sigma - \Delta$) analog to digital Pulse Code Modulation (PCM) converters are currently popular in the fields covering wireless communication due to their high resolutions for medium bandwidth, ease of design, and low power consumption. High resolution is the consequence of the inherent quantization noise suppression by the loop filter. With higher order loop filters, even better signal to noise ratios (SNR) can be achieved. Oversampling is the

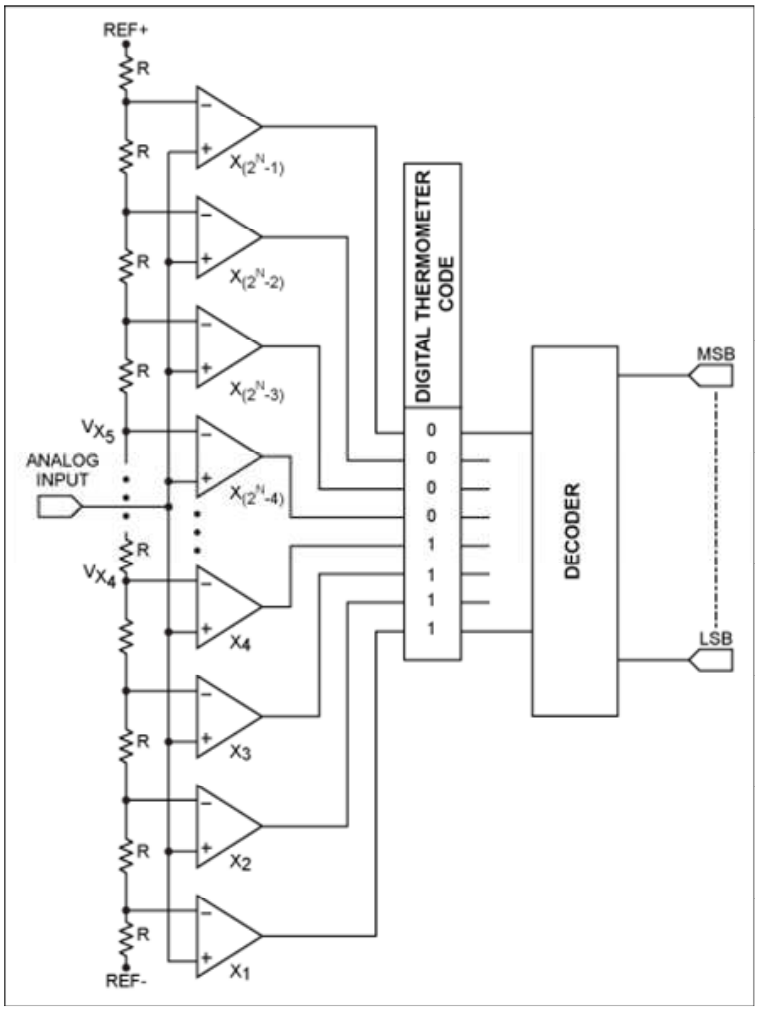


Figure 1.1. Diagram of the flash ADC

process of sampling the signal at the output of the quantizer with a higher sampling rate than that of the conventional 'Nyquist rate'. This pushes the quantization noise outside the signal band and enables to achieve dramatic signal to noise ratios. Resolutions up to 20 bits are achievable at low frequency (several hundered kilo hertz (kHZ)) input signals. Inputs of frequencies above one megahertz (MHz) requires filter orders of four and more. The achievable resolutions at that frequency range 12 to 14 bits. The building blocks of $\Sigma - \Delta$ ADC's are relatively easy to design and do not require high performance and precise circuits. A decimation filter is used after the $\Sigma - \Delta$ converter to filter the high frequency noise and also slow down the rate of conversion. This requires some additional die area.

Sigma-delta converters mainly have two types. The first is the discrete time ver-

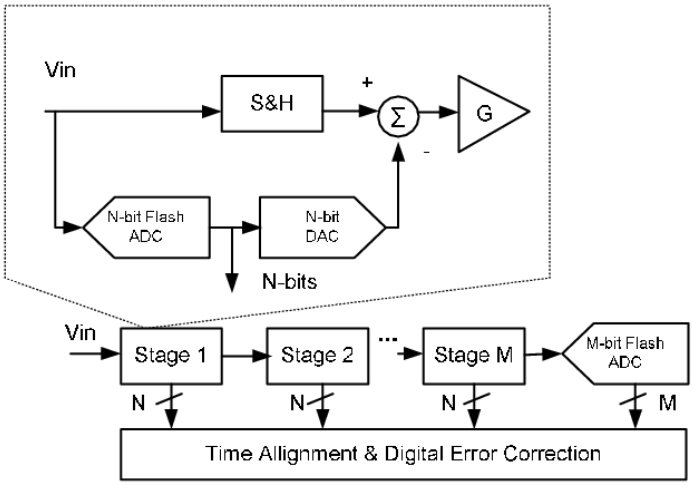


Figure 1.2. Diagram of the pipeline ADC

sion, which is currently the most popular type. It uses discrete time input signals and also discrete time electronic components. The power consumption which is caused from switching actions in discrete data is its biggest disadvantage. Another disadvantage is the requirement of relatively high bandwidth circuit blocks to work with the sampled input signal.
Continuous versions are better in terms of power consumption than the discrete time working ones. However, this type of converter suffers from performance degradation caused by the clock jitter noise injected at the quantizer. This noise can not be eliminated by the loop filter and deteriorates the SNR by a significant amount.

Besides the conventional synchronous circuit approach, converters can be built to not generate digital words but a periodic train of pulses modulated according to the input signal level. Such an operation can be better studied with the help of Table 1.1.

All signals can be classified as a member of four domains. Time sampled signals belong to 'domain 2 and 4'. 'Domain 4', is the digital signal domain where amplitude is discretized and binary coded at fixed time instants. 'Domain 2' is the discrete time signals domain, where amplitude value is sampled at certain time samples. 'Domain 3' is the asynchronous signal domain where signals are discretized only according to their amplitude value. Working in asynchronous signal domain may bring the opportunity to reduce power consumption for slow activity signals. While the technology advances,

Table 1.1. Different domains in signal processing depending on the sampling at either time or amplitude

Amplitude	Time	
	Continuous	**Sampled**
Continuous	**Domain 1 Analog domain**	**Domain 2 Discrete time domain**
Sampled	**Domain 3 Asynchronous**	**Domain 4 Digital domain**

supply voltages tend to decrease and circuit sizes tend shrink further. Reduction in the supply voltage threatens the dynamic range of the analog to digital converters. If the required bandwidth with improved technologies is considered, one can observe that the signal bandwidth is increasing continuously. Nowadays, wireless standards using increasing bandwidths such as WiFi and WiMax are in demand. Increasing the loop filter degree and oversampling can be utilized to attain higher bandwidths as stated earlier. However, they come at a cost. High order loop filters bring problems of stability, namely a phenomenon called limit cycle where the modulator oscillates at a low frequency. Increasing the oversampling ratio to high levels is dependent on technology. The other problem for continuous time converters is excess loop delay, which causes stability problems. In this thesis, asynchronous sigma delta converters will be investigated. Their potential according to their advantages and disadvantages will be outlined.

1.2. Objective of the Thesis

The main objective of the thesis is to investigate the performance of asynchronous sigma delta ADC's and explore the feasibility to their usage. To additional objectives are construction of an adjustable frequency ASDM and to construct a decimation filter for asynchronous PWM output. The available number of bits and the parameters that influence it is to be investigated.

There are two main objectives of the thesis. The first is to build a current-mode

asynchronous $\Sigma - \Delta$ modulator with adjustable loop delay. The loop delay will be realized with the quantizer delay. Through adjusting this delay ASDM working in a desired limit cycle frequency can be realized. The second objective is to build an asynchronous decimation filter which will process the PWM data generated by the ASDM and outputs digital converted data.

1.3. Key features and Contributions

The asynchronous ADC represented in this dissertation has the following key features and contributions

- The control theory analysis of loop delay based ASDM's is done. The previous implementations of the asynchronous $\Sigma - \Delta$ modulators are using quantizers with hysteresis. The analysis of the ASDM's with quantizer delay has been given.
- Stability and limit cycle operating region of ASDM's is given analytically. ASDM's have also stability concern; i.e, the limit cycle oscillation can change frequency and even can break with time. Stability analysis to ensure a working design is also given.
- Current mode comparator with adjustable delay is given. Previous ASDM implementations are using comparators with hysteresis. Since the implementation in this dissertation is based on a loop delay asynchronous modulator, an adjustable delay current comparator is given.
- Current mode implementation of a first and second order ASDM is given. Their advantages and disadvantages compared to implementation are outlined.
- A Feedforward second order ASDM design is given. Previous second order ASDM's are of feedback type.
- A decimation filter to process the ASDM's PWM output is given. The filter is based on Cascaded Integration Comb (CIC) architecture and the integration parts are using delay lines. The data is sampled after it is integrated with a slow clock signal.
- Reduced clock jitter affect for the overall ADC is shown. Since the sampling operation is not done in the $\Sigma - \Delta$ loop, the output is less sensitive to the

sampling clock jitter.

1.4. Thesis Organization

The organization of the thesis is as follows:
Chapter 2 presents background of sigma delta ADC's and summarizes the previous studies related to the thesis. Chapter 3 gives the control theory methods for analyzing limit cycle behavior as, stability analysis. Also, a subchapter to derive the output spectrum of the ASDM is given. Chapter 4 provides the decimation filter background for the proposed filtering scheme in this dissertation. Chapter 5 is dedicated to the circuit implementation of the asynchronous modulator.Circuit schematics and associated layouts for selected and newly proposed circuit blocks are given as schematics and associated layout. Chapter 6 gives the integrated circuit (IC) implementation of the ASDM modulators and the decimation filter. Chapter 7 details the results of the implemented ADC. Chapter 8 concludes the thesis.

2. SIGMA DELTA ADC BACKGROUND

Analog to digital converters are electronic devices that translate an analog domain signal (Table 1.1 upper-left) to a digital signal (Table 1.1 down-right). They implement nonlinear and linear operations to sample the signal information carried on amplitude and time axes and produce a digital code as output. The translation function '$\mathfrak{F}$' in Figure 2.1 can be further divided into some sub-functions which translate the signals to other domains. However, the parent function '$\mathfrak{F}$' as a whole should carry the operation to go from the analog domain to the digital.

Different techniques for building ADC's are present among which are flash, pipeline and sigma-delta architectures. Depending on the performance requirements and the topology's advantages and disadvantages of the topology, a particular topology can be selected. In the general case, a specific ADC type exhibits an optimum performance for a specific bandwidth and resolution requirement. Sigma delta ADC's are applicable for medium bandwidth and high resolution[1]. High resolutions in this topology are

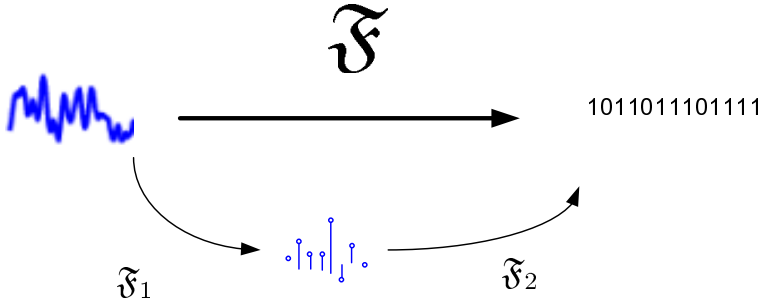


Figure 2.1. ADC operations depicted as a function across the signal domains

achievable due to oversampling and noise shaping through loop filtering. A detailed explanation of $\Sigma - \Delta$ ADC's is given in the next section.

2.1. Overview and Background of Sigma-Delta ADC's

The block diagram of a typical sigma delta ADC is given in Fig. 2.2. The ADC is composed of two succeeding stages: The first is the delta sigma modulator which

converts the analog input signal to a pulse code modulated train of pulses. The second stage is the digital low pass filter and the decimator. The operation of this stage will be explained later. If the modulator given in Fig. 2.3 is examined in detail, it can be

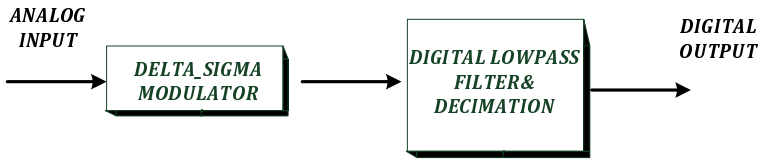


Figure 2.2. Delta sigma ADC block diagram

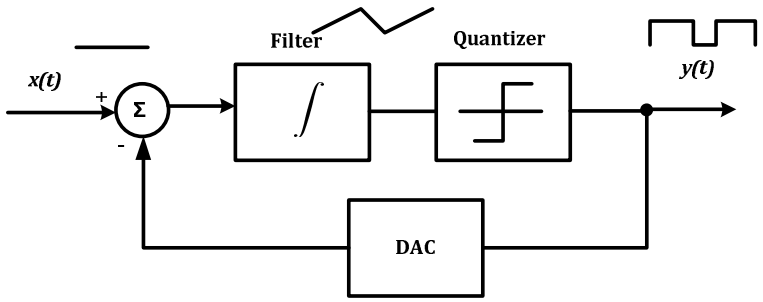


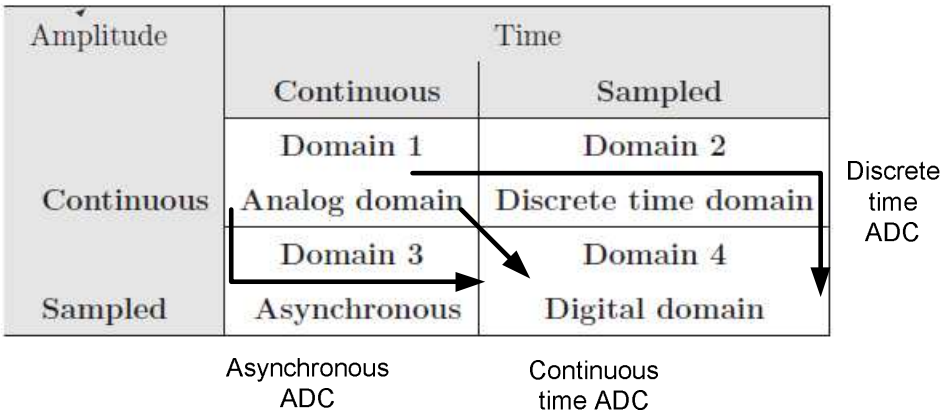
Figure 2.3. Sigma-delta modulator

seen that the modulator in its simplest form consists of a negative feedback loop with a filter and a comparator in the feed-forward path. In first order implementations, the filter is an integrator. The output of the comparator is fed back to the input to generate an error signal. If a two value output quantizer is used the error signal cannot reach to zero value and always makes the comparator generate an alternating output PCM pulse.

2.1.1. Types of Sigma-Delta Modulation

Depending of the domain of operation, sigma-delta modulators can be constructed in two types: Discrete-time sigma delta and continuous time sigma-delta ADC's . Both ADC's are synchronous since domain 3 in Table 2.1 is not visited in any part of their operation.

Table 2.1. ADC operations depicted as a function across the signal domains.Arrows showing possible domain transitions for ADC's. A discrete-time $\Sigma - \Delta$ ADC between domain 1 ,2 and 4. Continuous time $\Sigma - \Delta$ ADC between in domains 1 and 4.



These ADC's use synchronous circuit elements. In Fig. 2.4 a discrete time ADC is shown. The signal is sampled first and then passed through an anti-aliasing filter. The resulting sampled signal passes through a discrete time modulator. The integrator here is implemented as its discrete-time counterpart which is an accumulator. At every clock period, the state of the output changes. Although it is still the most popular $\Sigma-\Delta$ architecture, it suffers from two big problems. The first is the power consumption generated by switching all the discrete time components in succeeding clock cycles. The other problem is the bandwidth requirement of the analog blocks such as the filter to handle sampled and held version of the input signal which are composed of multiple harmonics of the sampling clock frequencies. Despite its disadvantages, this type was very popular and still is the dominant architecture in usage, due to the relative simplicity of design. Continuous time versions of $\Sigma - \Delta$ ADC's use continuous time components except the quantizer and the DAC in the feedback, which are clocked elements to realize the time sampling of the signal. A typical continuous time $\Sigma - \Delta$ ADC is given in Fig. 2.5. This architecture solves some problems of its discrete time counterpart like excess power consumption and high bandwidth requirements for the components. Unfortunately, it introduces a new problem: clock jitter. Since all the components in the loop work in the analog domain, a shift in the frequency of the sampling clock is directly reflected to the whole signal path. This is a severe

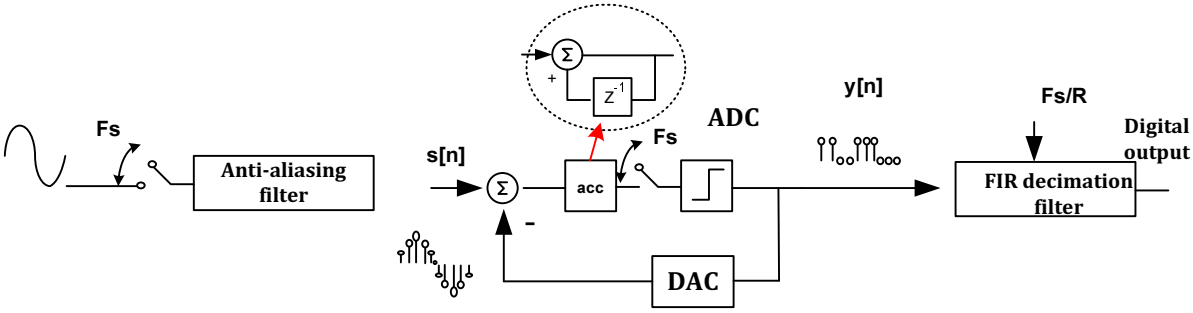


Figure 2.4. Block diagram of a discrete time $\Sigma - \Delta$ ADC

problem which deteriorates the performance and limits the usage of continuous time $\Sigma - \Delta$ converters [5], [6].

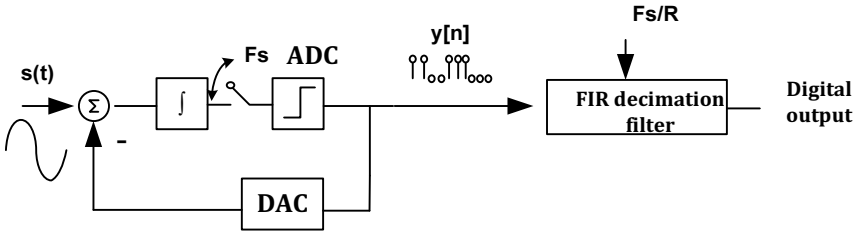


Figure 2.5. Block diagram of a continuous time $\Sigma - \Delta$ ADC

In all of the topologies, comparator is the building block of a quantizer. Quantization refers to discretization of the amplitude of the coming signal at certain time instants. A typical voltage transfer curve of a multi-bit quantizer is shown in Fig. 2.6. Quantization noise is the main noise source in the $\Sigma - \Delta$ ADC's. The spectrum of the quantized signal was of interest and investigated in [7], [8]. It is worth to remind that in ADC's quantization, generally refers to discretization of the amplitude at certain time instants. Hence, it contains time sampling operation, too. Under these conditions assuming that quantization error and input signal is uncorrelated, this noise can be treated as having a white spectrum. In fact these signals have a correlation to some extend and this is more obvious when input signal is an exact multiple of the sampling frequency. But for calculations, white noise assumption is accurate enough to make coarse performance calculations of the modulator. Therefore, the quantizer can be replaced by a noise source with flat spectrum which is added to the signal in the loop. It has been shown that the circuit can be separated to two circuits for noise signal and input signal [9]. The resulting circuits are shown in Fig. 2.7. In this work, after

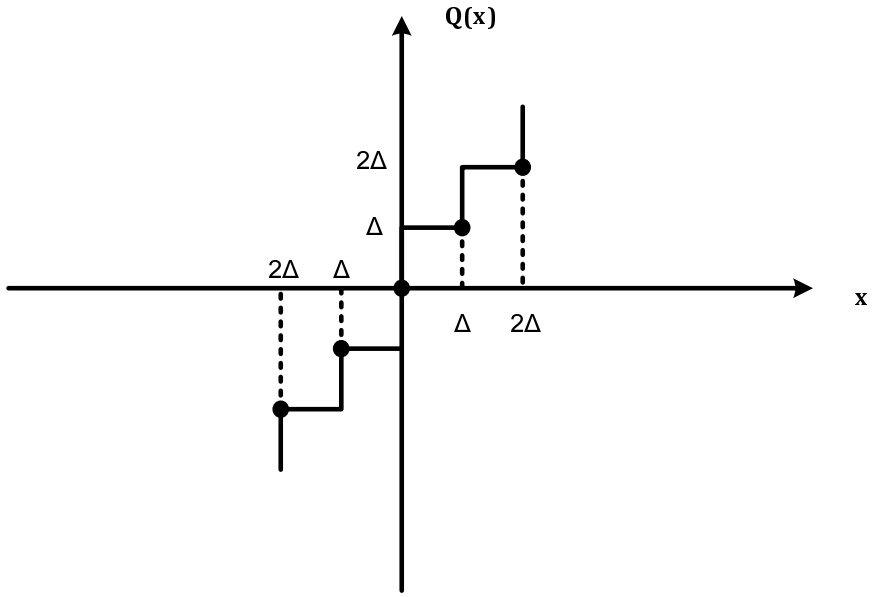


Figure 2.6. Multistep quantizer transfer characteristics $\Sigma - \Delta$ ADC

some cumbersome calculations, the expression for SNR and NTF were given, which relate the performance to filter order and oversampling ratio . A typical second order

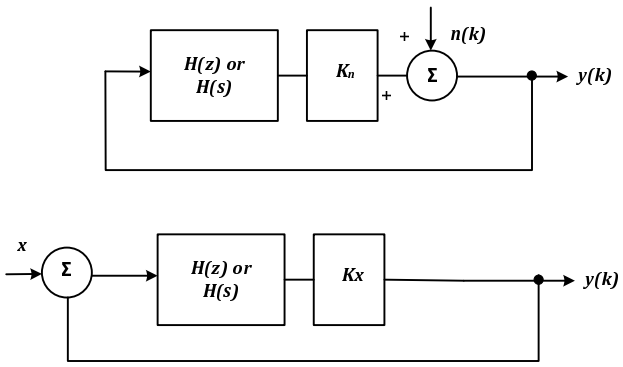


Figure 2.7. Separated circuits for noise and signal as given in [9].

synchronous sigma-delta modulator output spectrum is given in Fig 2.8. The signal is at 1 MHz and the sampling rate F_s is 100 MHz. The noise is shaped according to the NTF, hence the loop filter. The action of oversampling is seen as pushing the quantization noise away from the in-band.

A third possibility to build $\Sigma - \Delta$ ADC's is the asynchronous $\Sigma - \Delta$. A coarse block diagram is given in Fig. 2.9. The output of the ASDM unlike the other two topologies is a PWM signal, and is not time sampled; i.e., not synchronized. This type

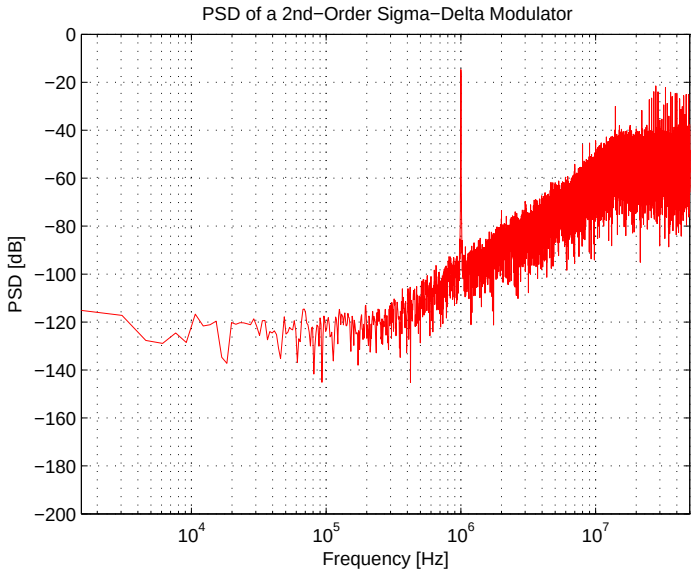


Figure 2.8. Typical spectrum of a second order synchronous modulator

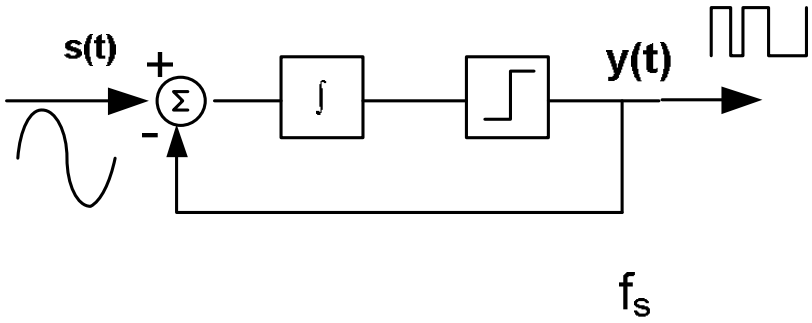


Figure 2.9. The asynchronous $\Sigma - \Delta$ modulator (ASDM)

of modulators is not new indeed. Nonlinear control applications such as heaters use this structure. The first studies were about the control aspects of these systems [10], [11]. The first possible use of ASDM in communication devices was given in [12], [13]. However, these devices have not received any attention until near time to be used in communication systems. The next work was on the use of ASDM's in electric inverter circuits as a Pulse Width Modulation (PWM) generator where an analytical treatment for ASDM's was also given in [14]. The possibility of applying ASDM to ADC is further investigated by design equations and performance metrics in [15]. Also, the causes that limit the performance were treated analytically. The first disadvantage is the lack of quantization noise suppression in the loop, since sampling is done after the ASDM. The second disadvantage is that the spectrum of an ASDM is much more noisy (contains

signal harmonics) and distorted compared to ordinary SDM's. However, there are some advantages such as the possibility of operations at very high speeds without the need of an external clock signal. Moreover the inherent variation of the limit cycle frequency due to jitter does not corrupt input signal, because the Bessel components are sufficiently suppressed in the in-band. Working at high speeds help to separate the noise harmonics from the baseband sufficiently. An implementation of a monolithic ASDM is given in [16].

If ASDM is aimed to be used in an ADC application, it has to be followed by a sampler and filter to get a final digital signal. Possible structures are depicted in Fig. 2.10. Type (a) is the option where an ordinary sampler at a rate equal to a high sampling frequency (F_s) is used. The sampled signal should be fed to an ordinary FIR filter or a Cascaded Integration Comb (CIC) filter [26]. Type (b) is an analog implementation of a FIR filter with delay lines called Time to Digital converter (TDC). When using this option, a lower sampling rate can be used.

The last configuration (c) which is the contribution of this dissertation to directly use an semi-analog version of the CIC filter. The detailed operation of this filter is given in Section four. To get rid of sampling at high frequencies, the integrator parts of the filter which are basically digital accumulators are build with a full adder and an analog delay. The incoming pulses from the ASDM are counted in terms of this delay. In integration parts, the signal will be slowed. Then a sampler samples the signal and finally the digital signal passes through a digital comb filter.

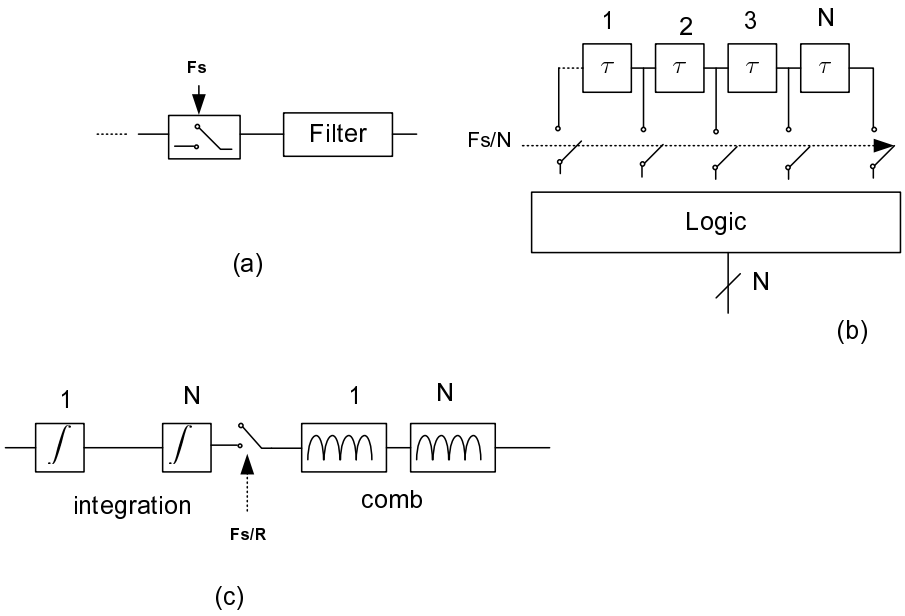


Figure 2.10. Possible sampling and filtering combinations of ASDM signals to get a digital ADC output

3. MATHEMATICAL ANALYSIS OF ASDM's

The aim of this chapter is to provide readers with the following:

- To give different control theory approaches to study the behavior of nonlinear ASDM systems in a unified manner
- To give period and frequency expressions of the delay and hysteresis quantizer based ADSM.
- To give the possible use of a quantizer with time delay as a building block of an ASDM.

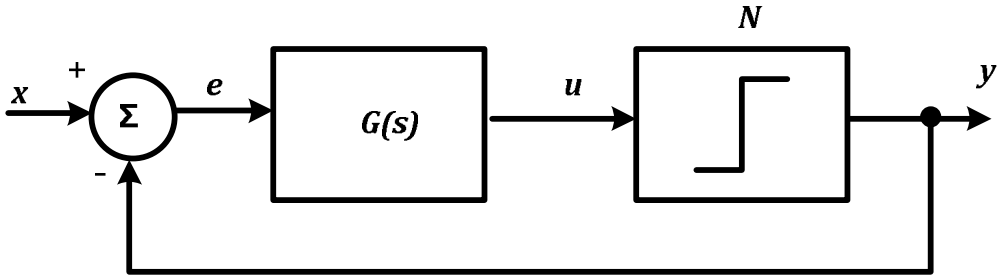


Figure 3.1. A first order ASDM block diagram

A typical first order ASDM is given in Fig. 3.1. The nonlinear function of the quantizer is depicted as 'N(u)'. To write a differential equation of the output and input, a mathematical function is needed for presenting the nonlinearity 'N'. The function $\tanh(n.u)$ can serve this purpose, because of its saturation characteristics.

$$N(u) = \tanh(n.u) \tag{3.1}$$

$$e(t) = x(t) - y(t) \tag{3.2}$$

$$e(t) = \dot{u(t)} = x(t) - y(t) = \frac{d\left[\tanh^{-1} y(t)\right]}{d(t)} = \frac{n}{1 - n^2 y^2}(dy/dt) \tag{3.3}$$

Finally a differential equation is obtained as below:

$$\frac{dy}{dt}n - n^2y^3 + n^2xy^2 + y - x = 0 \tag{3.4}$$

(3.4) is of Abel type and has no known closed type solution [25]. For '$x = 0$' a transient exponential decay is observed. As another alternative, control theory techniques should be used. Let's consider a nonlinear system based on hard limiter called relay systems in control theory. The block diagram of such a system is given in Fig. 3.2. Most of the

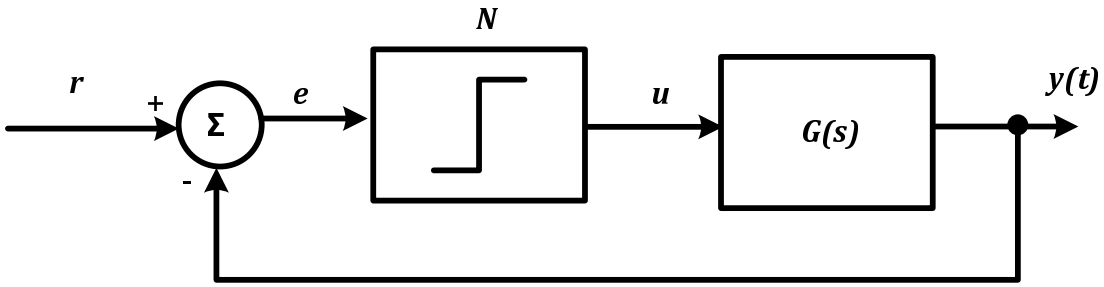


Figure 3.2. A relay system

time, it is of interest to have dead-zones in the relay characteristics. The characteristics of the hard limiter are given in Fig. 3.3 and the analytical expression in (3.5).

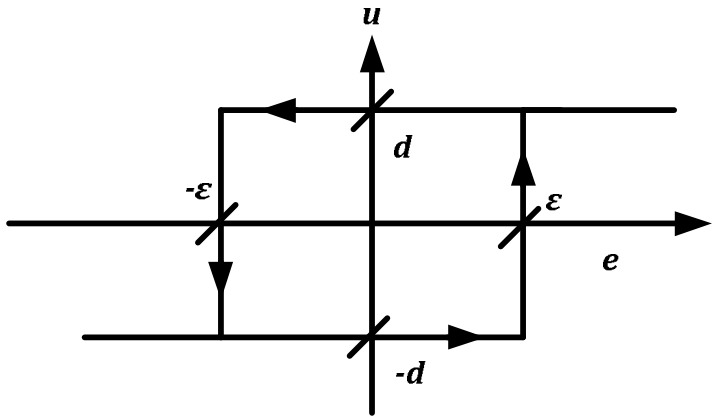


Figure 3.3. Hardlimiter with hysterisis characteristics

$$u(t) = \left\{ \begin{array}{llll} e > \ \varepsilon & or & (e > -\varepsilon & and\ u(t-) = \ d)\ then\ u(t) = \ d \\ e < -\varepsilon & or & (e < \ \varepsilon & and\ u(t-) = -d)\ then\ u(t) = -d \end{array} \right\} \tag{3.5}$$

3.1. Describing Function Approach

One way to deal with the nonlinearity in the loop is linearizing it. A process called 'quasi-linearization' allows one to represent a nonlinear function as a variable gain linear function [17], [18]. The idea can be better understood by the use of Fig. 3.4. The variable gain should be defined only for a specific signal; e.g, sinusoidal signal with a specific frequency. 'The sinusoidal describing function (DF)' is given as the following

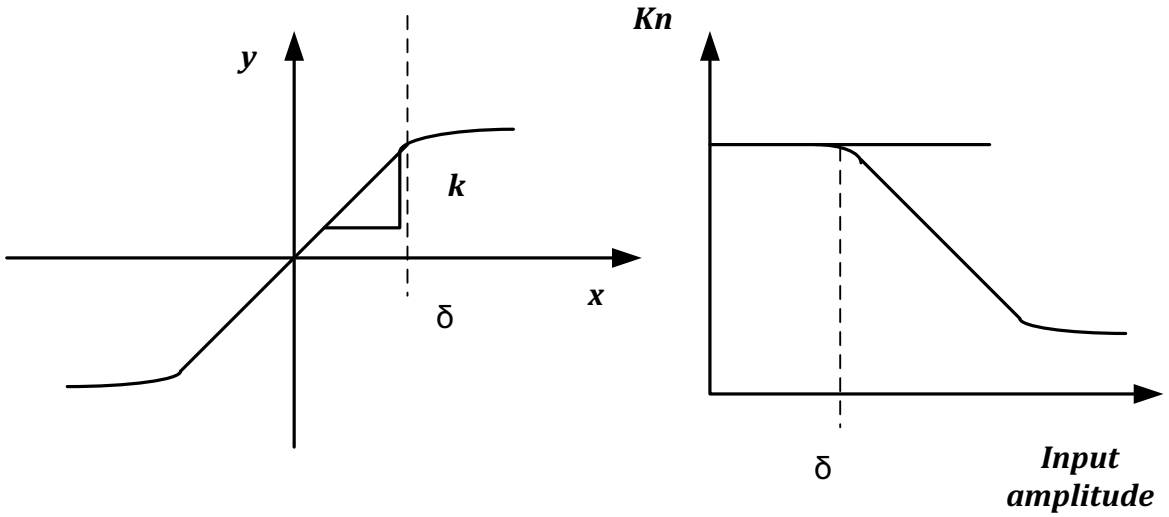


Figure 3.4. Hardlimiter characteristics (left), DF gain according to amplitude (right)

relation:

$$N(a,\omega) = \frac{phasor\ representation\ of\ the\ output\ component\ at\ frequency\ \omega}{phasor\ representation\ of\ the\ input\ component\ at\ frequency\ \omega} = \frac{A_1(a,\omega)}{A} e^{j\phi_1(A,\omega)} \tag{3.6}$$

'DF' is the complex first harmonic gain of a nonlinearity driving a sinusoidal signal. It should be noted that there exist also exponential and gaussian describing functions [17], [18]. But in $\Sigma - \Delta$ applications, use of the sinusoidal function is sufficient when limit cycle properties are studied. However, noise added by amplitude discretization can be studied using the other DF's. From now on, the term DF is used only for sinusoidal signals. For the ideal relay type characteristics the DF is given as [17]:

$$N(A) = \frac{4}{\pi}\frac{D}{A} \tag{3.7}$$

where A denotes the amplitude of the input signal and D is the saturation output. For the relay with hysteresis, the DF equation is [17]:

$$N(a,\phi) = \frac{4D}{\pi A}\sqrt{1-(h/A)^2} - j\frac{4h}{\pi A^2} = \frac{4D}{\pi A}e^{-j(sin^{-1}h/A)} \tag{3.8}$$

To find the point of oscillation, hence the limit cycle frequency, 'Harmonic Balance equation' which is analogous to 'Barkhausen criterion' in oscillators is used. The oscillation occurs when the following condition is satisfied [18].

$$1 + N(A)G(i\omega) = 0 \tag{3.9}$$

If $G(s) = 1/i\omega$ an integrator, Eq. 3.9 gives

$$\frac{1}{\omega i}\left(\frac{4D}{\pi A}\sqrt{1-(h/A)^2} - i\frac{4h}{\pi A^2}\right) = -1 \tag{3.10}$$

$$\omega = \frac{4h}{\pi\epsilon} \tag{3.11}$$

This expression is valid for G(s)=$\frac{1}{s}$; for different filter functions, a direct expression may not necessarily be found.

3.2. Time Domain Approach

Time domain approach has been utilized mostly in early papers [20],[19]. Especially, the work in [19] is concerned with state space analysis of nonlinear systems.

A system like that in Fig. 3.2, may sustain periodic oscillations called 'limit cycle oscillation' when no input is applied. If the input to the circuit is zero, $e = -y$. The ASDM circuit is the same as the system in Fig. 3.2 with zero input condition. It should be noted that if no input is applied, the position of the relay is not important for the limit cycle behavior. For the linear part of the circuit, state space representation is as

follows.

$$\begin{aligned} \frac{dx}{dt} &= Ax + Bu \\ y &= Cx \end{aligned} \tag{3.12}$$

The state space equation can be integrated to obtain the transfer function related to the time as:

$$f(t) = C(I + e^{At})^{-1} \int_0^t (e^{A\tau} B d\tau) \tag{3.13}$$

The initial state x(0), state x(t) and output y(t) can be calculated accordingly with the formulas below:

$$a = x(0) = (I + e^{Ah})^{-1} \int_0^h (e^{A\tau} B d\tau) d \tag{3.14}$$

$$x(t) = e^{At} x(0) + \int_0^t e^{A(t-\tau)} B u(\tau) d\tau \tag{3.15}$$

$$y(t) = C \left(e^{At} x(0) + \int_0^t e^{A(t-\tau)} B u(\tau) d\tau \right) + Du(t) > -\epsilon \tag{3.16}$$

Defining some symbols as the following will put the above equations in a more convenient form.

$$\begin{aligned} \phi = e^{At} \qquad \Gamma &= \int_0^t e^{As} ds B \\ x(h) &= \phi a - \Gamma d \end{aligned} \tag{3.17}$$

It will be clearer if the waveforms in the circuit are examined through Fig. 3.5. In the analysis, it is first assumed that periodic oscillation with period T=2h exists. Then, necessary conditions for these oscillations are investigated. It is clear that the quantizer switches at time instants of multiple of 'h'. At the instant of switching (t=h) the gain

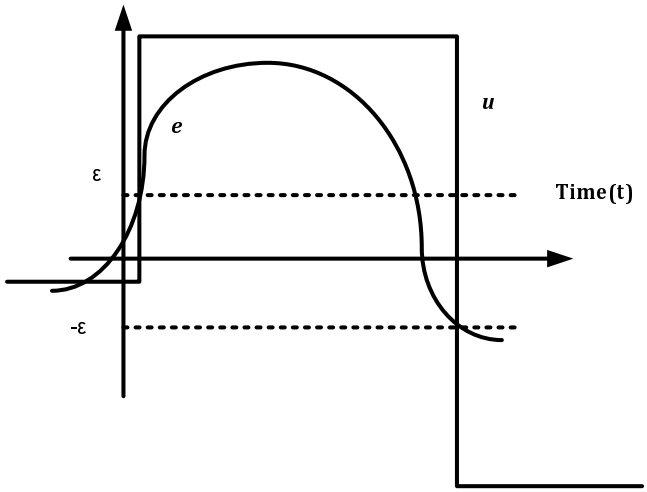


Figure 3.5. Waveforms in the hardlimiter circuit. 'e' is signal before the nonlinearity and u is the output of the nonlinearity. Dashed lines correspond to hysteresis levels of the nonlinearity.

of the nonlinearity should be exactly '$\frac{\epsilon}{d}$' [21]

$$f(h) = C(I + e^{Ah})^{-1} \int_0^h (e^{A\tau} B d\tau) = \frac{\epsilon}{d} \tag{3.18}$$

Eq. 3.18, refers to the gain of the nonlinearity block at switching instants. If this function intersects the necessary gain at the frequency where the intersection is, an oscillation should exist. A second condition for oscillation is that y(t) should not switch to the other threshold. That is,

$$y(t) > -\epsilon \quad for \;\; 0 < t < h. \tag{3.19}$$

A third necessary condition for limit cycle oscillation is that the signal ' $d(e(t))/dt$' should be positive or in other words '$d(y(t))/dt$' should be negative at time=h. That is the same to say it is negative at t=0. To put in formal form it should be ensured that:

$$\frac{dy(0)}{dt} = \frac{dx(0)}{dt} C > 0 \tag{3.20}$$

This is called the velocity condition and used to check for local stability. However, it should be also checked if the oscillation will change frequency or it is asymptotically stable.

3.3. Tsypkin's Frequency Domain Approach

There is some frequency domain related work done in this field [23],[24].The main idea is that: A pulse response of a linear system can be found exactly by sampling the response with zero order hold with period 'h', where '2h' denotes the limit cycle period. Considering zero order sampled version of G(s) as H(z) the following equations are obtained.

$$H(z) = C((zI - \phi)^{-1})\Gamma \tag{3.21}$$

The value $H(-1)$ gives the gain of G(s) at the switching instants so [22]:

$$H(-1) = \frac{-\epsilon}{d} \tag{3.22}$$

An alternative representation of the H(z) is given as,

$$H(z) = \sum_{n=-\infty}^{\infty} \frac{1 - z^{-1}}{logz + 2\pi in}\ G(\frac{1}{h}logz + \frac{2\pi in}{h}) \tag{3.23}$$

The velocity function which is '$H_v(-1) = sG(s)$', can be calculated as

$$H_v(-1) = \frac{4\omega}{\pi} \sum_{n=0}^{\infty} Re\ \ G(i\omega(1 + 2n)) \tag{3.24}$$

The Tsypkin function is defined as the sum of H(z) and K(z) as:

$$\Lambda(i\omega) = \frac{4\omega}{\pi} \sum_{n=0}^{\infty} Re\ \ G(i\omega(1 + 2n)) + i\frac{4}{\pi} \sum_{n=0}^{\infty} \frac{Im\ \ G(i\omega(1 + 2n))}{2n + 1} \tag{3.25}$$

The Tsypkin function is the complex function of the pulse response of G(s) and velocity of 'G(s)s'. The polar plot of '$\Lambda(i\omega)$' is called 'Typskin plot' or 'hadograph'. In order to obtain the point of the limit cycle, this curve should be intersected with $y = \frac{-\epsilon}{d}$. The real part of the intersection should be negative to ensure velocity considerations. Normally, this is done by plots but numeric calculations are also possible. Especially when '$G(i\omega)$ ' decreases rapidly, as in the case of SDM's which have integrators, approximations are also possible. In the case of a first order ASDM, since $G(i\omega) = \frac{1}{s}$,

$$H(-1) = \frac{4}{\pi}\sum_{n=0}^{\infty}\frac{ImG(i\omega(1+2n))}{1+2n} \approx \frac{4}{\pi}ImG(i\omega) \tag{3.26}$$

and

$$H_v(-1) = \frac{4\omega}{\pi}\sum_{n=0}^{\infty}ReG(i\omega(1+2n)) \approx \frac{4\omega}{\pi}ReG(i\omega) \tag{3.27}$$

Thus the point of intersection gives:

$$\omega_c \approx \frac{4}{\pi}\frac{d}{\epsilon} \tag{3.28}$$

If the terms in the series is also taken into account:

$$\omega = \frac{4}{\pi}\frac{d}{\epsilon}\left(1+\frac{1}{9}+\frac{1}{25}\right) \tag{3.29}$$

So the actual frequency is about 15.1% off. This deviation is also present with the describing function method which is based on the principle of the gain for the first harmonic of the pulse. The amount of error caused by DF approximation is small where the order of G(s) is high, however large deviations are present when the order is small. Stability of the limit cycle can be checked with the Jacobian of the Poincaré map as below:

$$W = (I - \frac{vC}{Cv})\Phi \tag{3.30}$$

According to its accurate solutions, Typskin method is better for our analysis. Since a first order system is already investigated in the above sections, it is better to look for a second order system. This time $G(s) = \frac{1}{s^2}$.

$$\begin{aligned}\Phi = e^{Ah} &= 1 + Ah + A^2h^2/2 + \cdots \\ &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + \begin{bmatrix} 0 & h \\ 0 & 0 \end{bmatrix} = \begin{bmatrix} 1 & h \\ 0 & 1 \end{bmatrix}\end{aligned} \tag{3.31}$$

$$\Gamma = \int_0^h e^{As} B ds = \int_0^h \begin{bmatrix} 1 & s \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \end{bmatrix} ds = \int_0^h \begin{bmatrix} s \\ 1 \end{bmatrix} ds = \begin{bmatrix} h^2/2 \\ h \end{bmatrix} \tag{3.32}$$

$$H(z) = C(zI - \phi)^{-1}\Gamma = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} z-1 & -h \\ 0 & z-1 \end{bmatrix}^{-1} \begin{bmatrix} h^2/2 \\ h \end{bmatrix} = \frac{h^2(z+1)}{2(z-1)^2} \tag{3.33}$$

Clearly, $H(-1) = 0$ so limit cycles exist when there is no hysteresis i.e. when $\epsilon = 0$, but with arbitrary period (depending on the initial condition of x). Any value of 'h' will give H(-1)=0. The stability of the limit cycle should also be checked. To find $a = x(0)$, applying $a = \Phi a - \Gamma d$ and taking d=1 and solving the equation below gives the 'a' value as,

$$a = \begin{bmatrix} 1 & h \\ 0 & 1 \end{bmatrix} a - \begin{bmatrix} h^2/2 \\ h \end{bmatrix} \; and \; a = \begin{bmatrix} 0 \\ h/2 \end{bmatrix} \tag{3.34}$$

$$v = Aa + Bd = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} 0 \\ h/2 \end{bmatrix} = \begin{bmatrix} h/2 \\ 0 \end{bmatrix} \tag{3.35}$$

$$W = (I - \frac{vC}{Cv})\Phi = \begin{bmatrix} 0 & 0 \\ -2/h & -1 \end{bmatrix} \tag{3.36}$$

$$det(SI - W) = \begin{bmatrix} z & 0 \\ 0 & z \end{bmatrix} - \begin{bmatrix} 0 & 0 \\ -2/h & -1 \end{bmatrix} = \begin{bmatrix} z & 0 \\ 2/h & z+1 \end{bmatrix} \tag{3.37}$$

The roots are inside the limit circle so the oscillations are locally stable but not asymptotically stable. It is worth to note that when hysteresis exists, no oscillations will be present.

Time delay circuit components might be also interesting, since all quantizers in ADC's have some delay. So when the loop filter G(s) has a finite delay, the state space equations become:

$$\begin{aligned} \tfrac{dx(t)}{dt} &= Ax(t) + Bu(t-\tau) \\ y(t) &= Cx(t) \end{aligned} \tag{3.38}$$

In order to hold the zero order sampling conditions assuming that the delay time is $0 < \tau < h$, where h is the first switching time, the following formula holds for the state vector 'x':

$$x(kh+h) - \Phi x(kh) = \int_{kh}^{kh+h} e^{A(kh+h-s')} Bu(s'-\tau)ds' \tag{3.39}$$

Defining functions Γ_0 *and* Γ_1

$$x(kh+h) - \Phi x(kh) = \underbrace{\int_{kh}^{kh+\tau} e^{A(kh+h-s')}ds'B}_{\Gamma 0} \; u(kh-h) + \underbrace{\int_{kh+\tau}^{kh+h} e^{A(kh+h-s')}ds'}_{\Gamma 1} \; u(kh) \tag{3.40}$$

$$x(kh+h) = \Phi x(kh) + \Gamma_1 u(kh-h) + \Gamma_0 u(kh) \tag{3.41}$$

The transfer function at time h and the equivalent value is:

$$f(h) = C(I + \Phi(h))^{-1}(\Gamma_0(h) - \Gamma 1(h)) = \epsilon/d \tag{3.42}$$

It is worth to investigate any possibility of first or second order systems for our ASDM converter which is either a delayed integrator or an delayed low-pass filter. In the general case, when the state space equation is as follows

$$\frac{dx(t)}{dt} = \alpha x(t) + \beta u(t - \tau) \tag{3.43}$$

$$\Gamma_0 = \int_0^{\tau} e^{As} ds B = \int_0^{\tau} e^{\alpha s} ds \beta = \beta \frac{e^{\alpha(h-\tau)} - 1}{\alpha} \tag{3.44}$$

$$\Gamma_1 = \int_{\tau}^{h-\tau} e^{As} ds B = \int_{\tau}^{h-\tau} e^{\alpha s} ds = \beta \frac{e^{\alpha(h)} - e^{\alpha(h-\tau)}}{\alpha} \tag{3.45}$$

The gain at the switching instants is

$$f(h) = C(I + \Phi(h))^{-1}(\Gamma_0(h) - \Gamma 1(h))(-1)^m = \epsilon/d = \beta \frac{2e^{\alpha(h-\tau)} - e^{\alpha h} - 1}{\alpha(1 + e^{\alpha h})} \tag{3.46}$$

If the delay is adjusted, it is wiser to not allow any hysteresis (hardlimiter), not to increase the dimension of the equation. If that is the case,

$$h = \frac{1}{\alpha} ln \frac{1}{2e^{\alpha\tau} - 1} \tag{3.47}$$

The integrator with delay is when $\alpha = 0$

$$h = \tau/2 \tag{3.48}$$

So $T = 4\tau$. If $\alpha = 1$ which corresponds to the system with a delayed lowpass filter.

$$h = ln\frac{1}{2e^{\tau} - 1} \tag{3.49}$$

Exploring a second order integrator as a loop filter, which is $G(s) = \frac{e^{-s\tau}}{s^2}$, the following relations are obtained.

$$\Phi = \begin{bmatrix} 1 & h \\ 0 & 1 \end{bmatrix} \tag{3.50}$$

$$\Gamma_0 = \int_0^{h-\tau} e^{As} ds B = \left\{ \int_0^{h-\tau} \begin{bmatrix} 1 & s \\ 0 & 1 \end{bmatrix} ds \right\} \begin{bmatrix} 0 \\ 1 \end{bmatrix} = \begin{bmatrix} (h-\tau)^2/2 \\ h-\tau \end{bmatrix} \tag{3.51}$$

$$\Gamma_1 = \int_{h-\tau}^{h} e^{As} ds B = \left\{ \int_{h-\tau}^{h} \begin{bmatrix} 1 & s \\ 0 & 1 \end{bmatrix} ds \right\} \begin{bmatrix} 0 \\ 1 \end{bmatrix} = \begin{bmatrix} h\tau - \tau^2/2 \\ \tau \end{bmatrix} \tag{3.52}$$

$$\Gamma_0 - \Gamma_1 = \begin{bmatrix} h^2/2 + \tau^2 - 3h\tau \\ h - 2\tau \end{bmatrix} \tag{3.53}$$

$$f(h) = C(I + \Phi)^{-1}(\Gamma_0 - \Gamma_1) = \tag{3.54}$$

$$\begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} 2 & -h \\ 0 & 2 \end{bmatrix} \begin{bmatrix} h^2/2 + \tau^2 - 3h\tau \\ h - 2\tau \end{bmatrix} = \tag{3.55}$$

$$\tau^2/2 - h\tau \tag{3.56}$$

For no hysteresis, period of the oscillations is found as $T = 2h = 2\tau$. It is seen that increasing the integration order halved the period of oscillations. The oscillations however are not stable. A basic idea for this is that the double integrator gives a 180

degrees phase shift and the delay an additional amount. Since the total phase is above 180 degrees and the NL(Non-linear) block will also provide a delay, the oscillations will grow over time.

3.4. Spectral Analysis of ASDM's

The first order ASDM in the input signal modulates the duty cycle of the square wave output. But this type of modulation is a little different from original PWM signals; since the frequency of the signal changes also with the amplitude of the input as in Fig. 3.6.

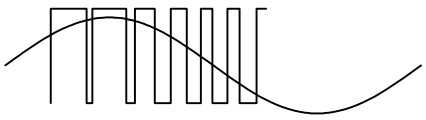


Figure 3.6. Sinusoidal signal modulated PWM

Analyzing the circuit given in Fig. 3.1. If the hysteresis levels are at $\pm\epsilon$, the integrator output signal which will be a ramp function, changes direction when reaching one of the thresholds. The total period $T = T_1 + T_2$ is the sum of up and down ramps. Time spent in these regions are related by the integrator input as follows:

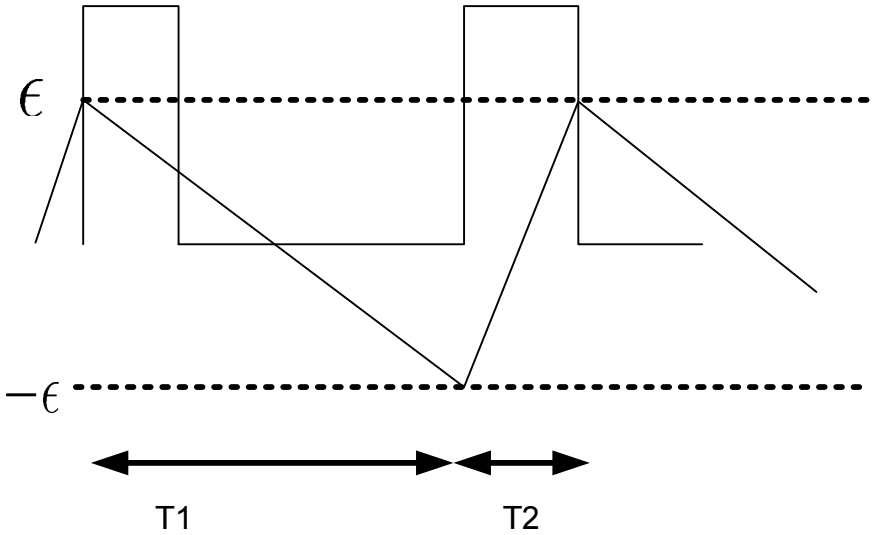


Figure 3.7. Integrator output of the first order sigma delta modulator

$$T_1 = 2\frac{\epsilon}{K(1+v)}$$
$$T_2 = 2\frac{\epsilon}{K(1-v)} \tag{3.57}$$

Then, the period of one cycle of oscillation and the expression for the duty cycle will be as follows,

$$T = T_1 + T_2 = \frac{4\epsilon}{k(1-v^2)}$$

$$\alpha = (the\ high\ period) = \frac{T_1}{T} = \frac{(1+v)}{2} \tag{3.58}$$

Since the formula of the duty cycle shows a relation to the input, this configuration can be used as a modulator. Frequency domain analysis can be done using Fourier series representation of a pulse width modulated signal. For a pulse width modulated

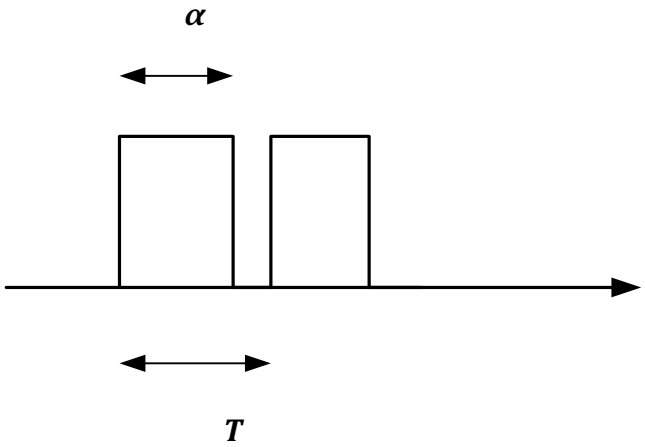


Figure 3.8. Duty cycle modulated wave

signal with constant carrier frequency and a modulated duty cycle the Fourier series expansion is as follows:

$$s(t) = A_0 + \sum_{n=0}^{\infty} A_n cos(\omega_c n + \Phi_n) \tag{3.59}$$

$$A_0 = V_{dc}(\alpha - \tfrac{1}{2})$$

$$A_n = \tfrac{V_{dc}}{(n\pi)} sin(n\pi\alpha)$$

If a sinusoidal signal is used as input :

$$v(t) = Msin(\omega_m t) \tag{3.60}$$

$$\alpha = \frac{1}{2} + \frac{Msin(\omega_m t)}{2} \tag{3.61}$$

The phase 'Φ_n' and the frequency change with the input signal was given in the previous part. It can be seen the period, hence the frequency is modulated with the inverse of the square of the input amplitude. The instantaneous frequency of the carrier wave is as below:

$$f_i = f_c(1 - v^2) \tag{3.62}$$

If the input is a sinusoidal time varying signal '$Msin(\omega_m t)$' then,

$$\omega_i = \omega_c(1 - M^2 sin^2(\omega t)) = \omega_c \left(1 - \frac{1}{2}M^2 + \frac{1}{2}M^2 cos(2\omega_m t)\right) = \omega_o + \omega_\Delta \tag{3.63}$$

$$\omega_0 = \omega_c(1 - \frac{1}{2}M^2) \tag{3.64}$$

$$\omega_\Delta = \frac{1}{2}M^2 cos(2\omega_m t) \tag{3.65}$$

The '$\omega_c + \phi$' expression is in the frequency modulated signal form. In frequency mod-

ulation, the deviation index 'β ' is defined a follows:

$$\beta = \frac{\omega_\Delta}{2\omega_m} \tag{3.66}$$

$$\beta_M = v_m \frac{\pi}{2} \tag{3.67}$$

The 'nth harmonic' of the output square wave is in Euler form as:

$$S_n = A_n \Re e \left\{ e^{jn\omega_c t} e^{jn\beta sin(2\omega_m t)} \right\} \tag{3.68}$$

This expression results in a Bessel series form,

$$S_n = A_n \sum_{k=-\infty}^{\infty} J_k(n\beta) cos(n\omega_c t + n2\omega_m t) \tag{3.69}$$

Besides the frequency dependency of the carrier frequency 'ω_c' ; the amplitude of the Fourier series components are also modulated, which generates also an Amplitude Modulation

$$A_n(t) = \frac{V_{dc}}{n\pi} sin \left[n\frac{\pi}{2}(1 + M sin(\omega_m t) \right] \tag{3.70}$$

Combining these two modulation types, the final expression becomes:

$$\begin{aligned} S_n(t) = & \frac{V_{dc}}{n\pi} sin(n\frac{\pi}{2}) \sum_{k=-\infty}^{\infty} J_k(n\beta) cos(n\beta_M sin(\omega_M t)) \cdot cos(n\omega_c t + n2\omega_M t) \\ & + \frac{V_{dc}}{n\pi} sin(n\frac{\pi}{2}) \sum_{k=-\infty}^{\infty} J_k(n\beta) sin(n\beta_M sin(\omega_M t)) \cdot cos(n\omega_c t + n2\omega_M t) \end{aligned} \tag{3.71}$$

In our design, mostly the baseband and the first harmonic of the carrier wave is of

importance (since the first harmonic contents are in the band of interest) which are

$$S_0(t) = \frac{s(t)Vdc}{2}$$

$$S_1(t) = \frac{V_{dc}}{\pi} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} J_{2n}(\beta) J_k(\beta_M) \cdot cos(\omega_c t + (2n+m)\omega_M t) \tag{3.72}$$

A carrier frequency 'ω_c' 32 MHz and a input signal of 1 MHz with amplitude of 0.5V denoted by 'M', the computed spectrum looks like in Fig. 3.9.

$$\beta = \frac{\omega_\Delta}{2\omega_m} = \frac{1/2M^2\omega_c}{2\omega_m} = \frac{M\omega_c}{4\omega_m} = 4 \tag{3.73}$$

$$\beta_M = M\frac{\pi}{2} = 0.79 \tag{3.74}$$

Although it was shown before that the double integrator with delay is unstable, let's

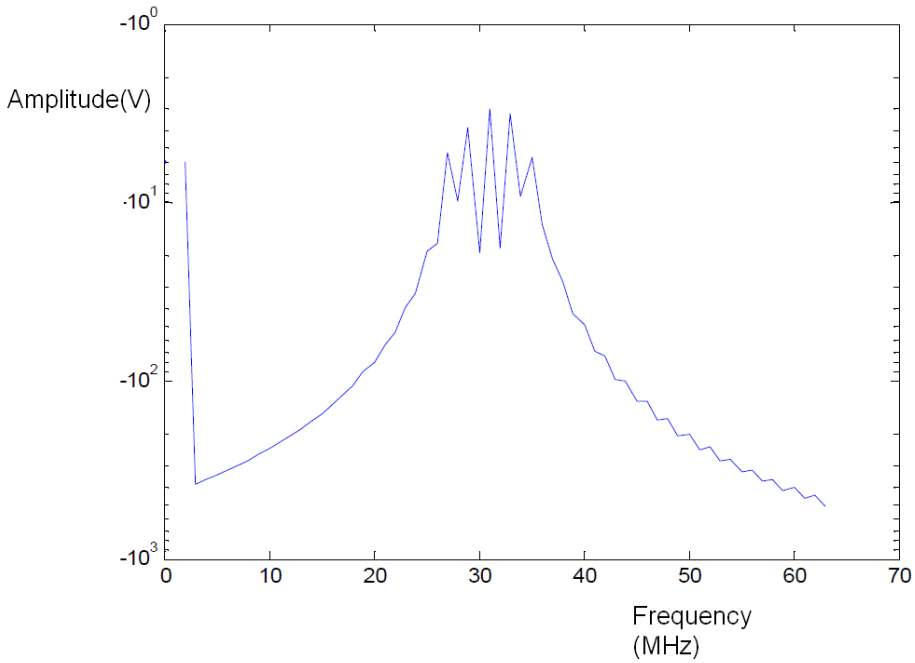


Figure 3.9. Calculated spectrum of the above signals using Eq. 3.72

still investigate a stable second order polynomial type $G(s) = (s+a)(s+b) = s^2 + (a+b)s + ab$ and its spectrum characteristics. Note that a stable $G(s)$ does not necessarily

mean a stable limit cycle. Limit cycle stability also depends on the time delay. Its typical waveform is given in the Fig. 3.10. Since the system has a stable limit cycle the output of the filter is bounded.

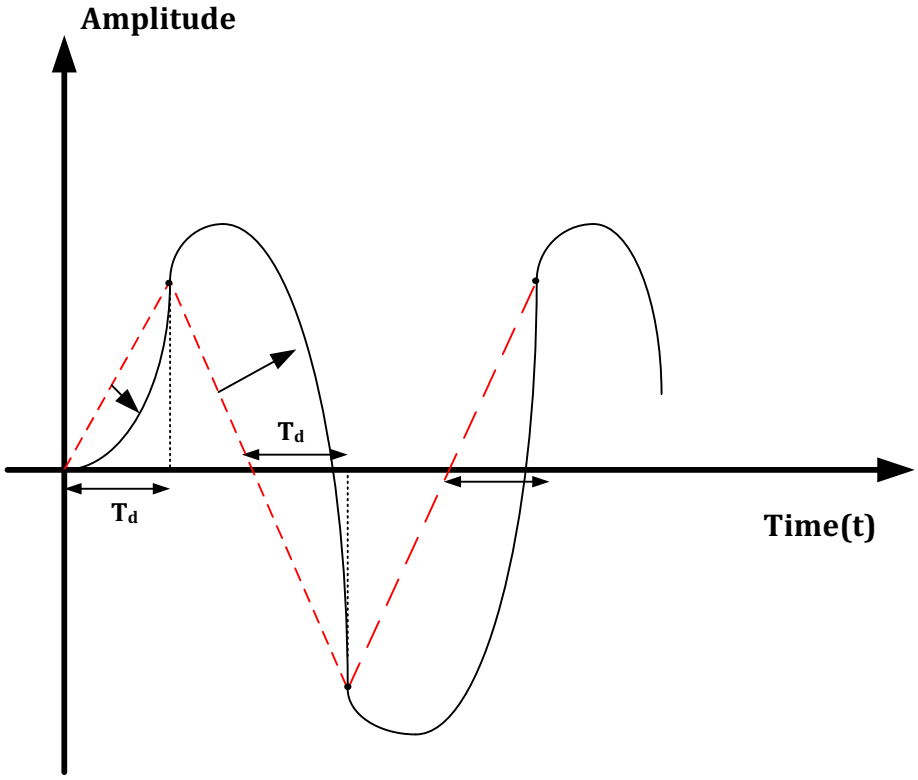


Figure 3.10. Filter outputs of a first order (dashed) and second order(solid) ASDM

3.5. Simulink model for ASDM for behavioral simulations

The behavioral simulations for ASDM's can be done using Matlab Simulink. Since simulink works at discrete time steps, the simulation time should be chosen such that it is much smaller compared to the loop delay. The Simulink model of the first order ASDM constructed in this dissertion is given in Fig. 3.11.

3.6. Frequency Scaling

To operate in any desired frequency, scaling properties may be used. To change the frequency of the limit cycle, delay times and hysteresis values can be modified

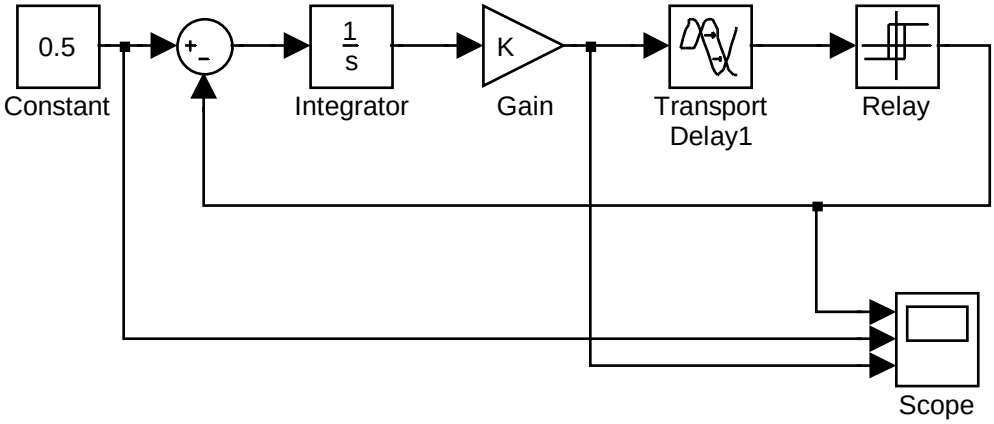


Figure 3.11. Matlab Simulink model for behavioral simulation of first order ASDM

accordingly. The filter DC gain(A_0) should also be scaled to the desired frequency. This property can be used as follows. If a first order ASDM system is designed with a 1 second loop delay and filter DC gain as 1, if changing loop delay to 1 micro second, filter gain should be changed to 10^6.

3.7. Effect of Finite Slope of the Nonlinearity

Unfortunately, in real circuit design, ideal relay characteristics are not achievable. The real transfer characteristics of saturation type. The finite slope of these character-

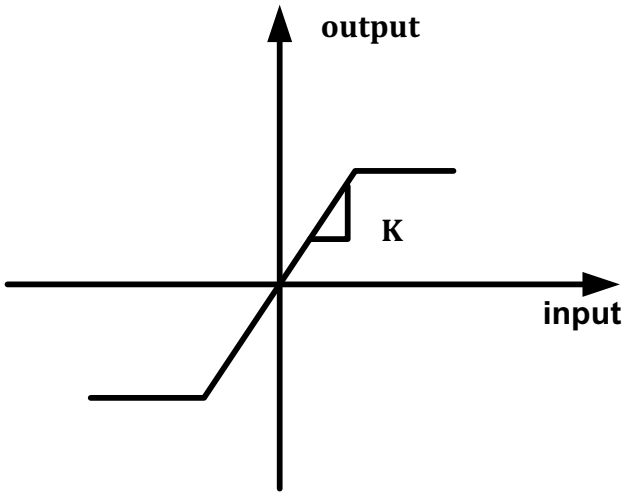


Figure 3.12. Filter outputs of a first order (dashed) and second order(solid) ASDM

istics may have an effect on the operation of the circuit. If the delay is not large enough

to let the filter output reach the saturation region, the oscillation may die out. The condition of oscillation can be found precisely to replace the nonlinearity by a linear function with slope 'K' ; and investigate the Nyquist stability criterion. For the first order filter with delay and no hysteresis:

$$G(s)K = -1 \tag{3.75}$$

$$KT_d \geq \pi/2 \tag{3.76}$$

In the designs it will be of great importance to use high gain comparators if the delay is not controllable.

3.8. Spectrum of behavioral simulation of first order ASDM

The spectrum of the behavioral simulation of an ASDM with a limit cycle frequency is given in Fig. 3.13. As it can be seen for a 1 MHz input signal with a bandwith of 10 MHz simulated spectrum can give a signal to noise ratio about 90 dB when limit cycle frequency is 90 dB. So large SNR values can be achievable. If the system has an element with distortion e.g creating a 3rd harmonic the spectrum in Fig. 3.14 is obtained. As it can be seen the possible nonlinearity in the filter or input signal creates odd harmonics which creates a noise floor. So, in order to achieve high SINAD values, the linearity of the ASDM should be as high as possible. One interesting thing is the case when both 3rd order distortion and a DC offset is present in both time. This time second order harmonics will exist in the spectrum and the magnitude is directly depended on the magnitude of the offset voltage.

In this section, using the describing function approach, an approximate oscillation frequency was found for a first order ASDM. The time-domain approach was utilized to derive an oscillation condition. Then, Tsypkin's frequency domain approach was investigated in order to calculate the oscillation frequency more accurately. The same approach was also applied to find the oscillation criteria. Also, the comparator with hysteresis was exchanged with a delayed comparator in order to be closer to practical

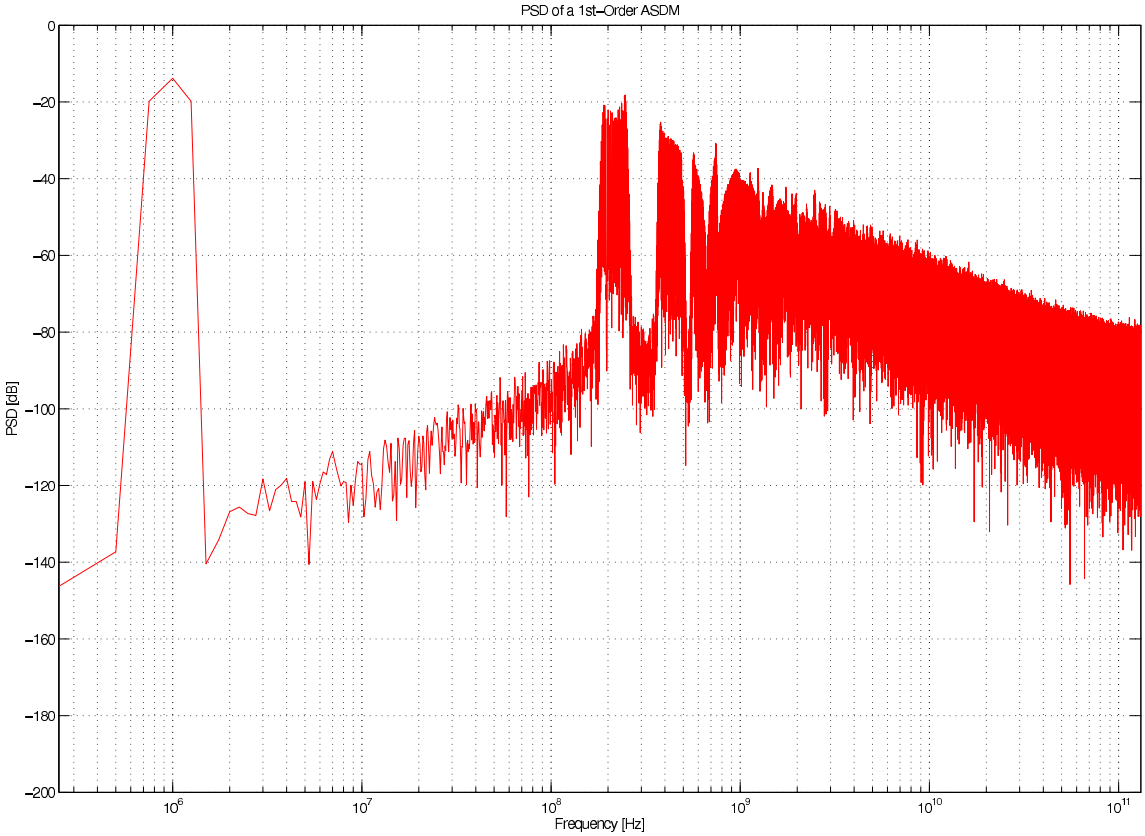


Figure 3.13. Spectrum of the Simulink simulated first order ASDM

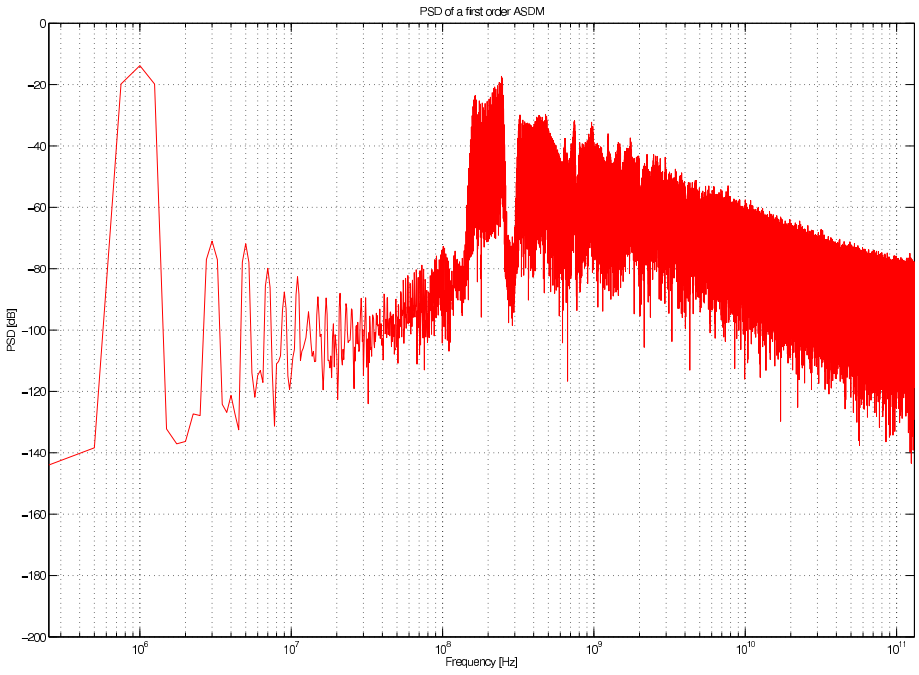


Figure 3.14. Spectrum of the Simulink simulated first order ASDM with odd order distortion

implementation. Finally, spectral analysis was utilized to study the characteristics of oscillation in more detail.

4. DECIMATION FILTERS IN $\Sigma - \Delta$ ADC's

4.1. Introduction

In sigma delta modulators oversampling is used to spread the quantization noise over much higher frequencies than the in-band. The limit cycle frequency which is usually much higher than the input bandwidth in ASDM's, is also a similar concept. This time, the intermodulated signal components are pushed away from in band. In both sigma delta modulators, the output is a 1-bit signal with a high rate. Also this high bit stream contains noise at high frequencies. In order to make it usable, the high frequency noise should be removed by low pass filtering. Secondly, the bit rate should be lowered to a more useful value. This process is called decimation filtering. A typical decimation filtering operation is shown in Fig. 4.1.

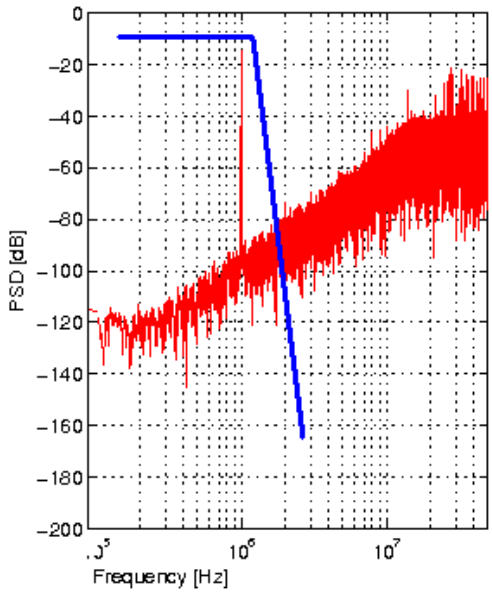


Figure 4.1. Decimation filter frequency response shown on the PSD of a synchronous sigma delta modulator output graph

4.2. Digital Filter Basics

In synchronous $\Sigma - \Delta$ ADC's digital filtering is used, to get rid of the high frequency noise components due to the oversampling. The first method to realize a digital low-pass filter is to use conventional FIR filtering where the block digram is shown in Fig. 4.2. This type of a filter is a non-recursive filter. The signal and its delayed versions are summed after multiplications with distinct coefficients to get the desired filter function.

$$H(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + \cdots + h_n z^{-n} \tag{4.1}$$

FIR filters are easy to build and are always stable. Therefore they are preferred to

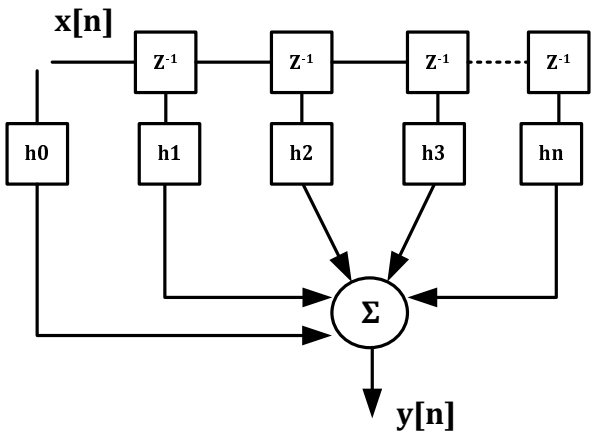


Figure 4.2. Conventional FIR filtering

be used after $\Sigma - \Delta$ converters as a decimator. The second type of the digital filter is the Infinite Impulse Response(IIR) filter. This is a recursive filter since it uses past values of the output. The block diagram is given in Fig. 4.3. The IIR filter unlike the FIR filters is hard to design and may not stable. Its phase response is not linear. Both these architectures, however, use a lot of multiplications which consume a large area. Number of multiplication elements is less in IIR than FIR realizations. In both of the filters, power consumption is high due to switching.

There is a third type of filter 'Half Band Filter', which is also used with ADC's. Half band filters split the input band to two equal bands. They are mostly used in sub-band coding in video and audio.

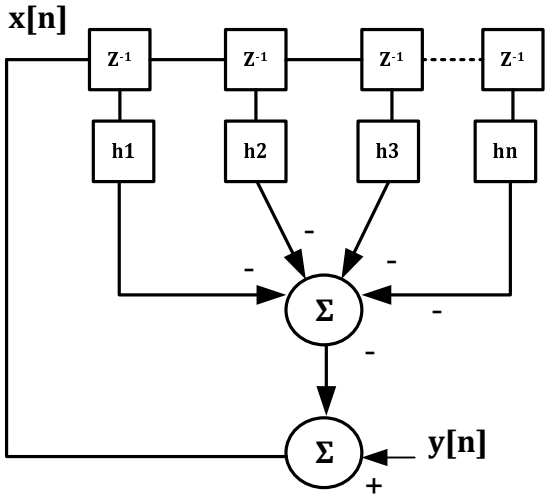


Figure 4.3. IIR filter

4.3. Cascaded Integrator Comb (CIC) Filters

Decimation filters which are mostly designed as FIR filters are digital averagers. Mostly they are implemented as 'sinc' filters. Because of the large areas needed to make shift and multiply operations, in the above filters, CIC filters, are preferable.

The CIC filter [26] overcomes power and area problems. The operation consists of 'N stages' of integrators which are built by accumulators and succeeding 'N stages' of comb filters. Since signal will slow down after integration stages, sampling with a lower frequency than the original data rate can be performed. The block diagram of a CIC filter is given in Fig 4.4. Each discrete time integrator, which indeed are accumulators,

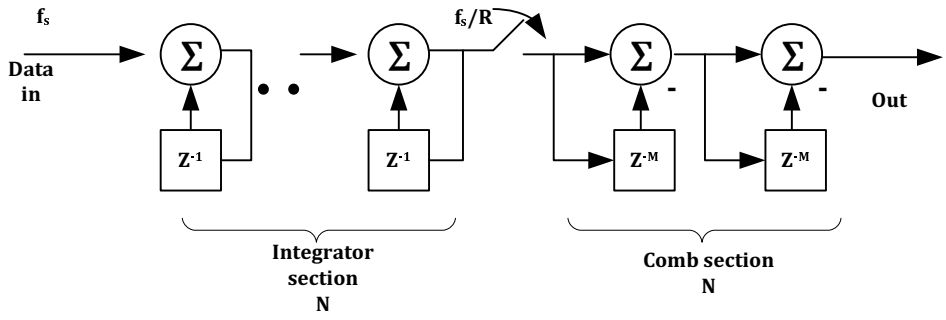


Figure 4.4. Block diagram of CIC filtering

has the transfer function:

$$H_i(z) = \frac{1}{1 - z^{-1}} \tag{4.2}$$

Each of the comb sections, which are high-pass filters, has the transfer function:

$$H_c(z) = 1 - z^{-RM} \tag{4.3}$$

If these are combined together, one obtains the combined transfer function of:

$$H_{CIC}(z) = \frac{(1 - z^{-RM})^N}{(1 - z^{-1})^N} = \left[\sum_{k=0}^{RM-1} z^{-k}\right]^N = [1 + z^{-1} + z^{-2} + \cdots + z^{-RM-1}]^N \tag{4.4}$$

The variable 'N' shows number of the cascaded integration stages; 'R' is the value by which factor the frequency is reduced; 'M' is the delay of each comb section. The 'R times M value is an important design parameter called the differential delay.

The frequency response of the filter is given in Fig. 4.6 . It is worth noting that the necessary 'sinc' filters for decimation can be easily built using this technique. As

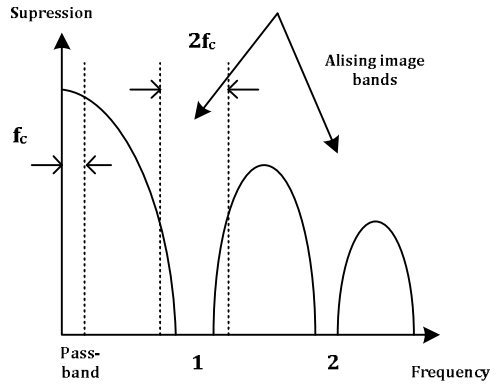


Figure 4.5. Frequency response of CIC filters

it can be observed in Fig. 4.6, the filter has zeros on multiples of 'fc', where fc is the lower sampling frequency. The integration order gives the desired suppression value. For example, if one uses a fourth order integration instead of first the magnitude of the side lobes will be smaller. This type of filter also brings bits to a parallel form. The

number of output bits is a function of design parameters. It can be easily calculated with (4.5).

$$B_{out} = N \log_2 RM + B_{in} \tag{4.5}$$

If a '$sinc^3$ ' decimation filter is to be achieved, three integration and three comb filtering stages should be employed. This time, 'N' becomes three; choosing the 'M' value as one and a decimation amount of eight gives a number of bits at the output stage at as 7. Taking into account that 2's complement coding is used, additional one bit is needed. That will count up to 8 bits [27].

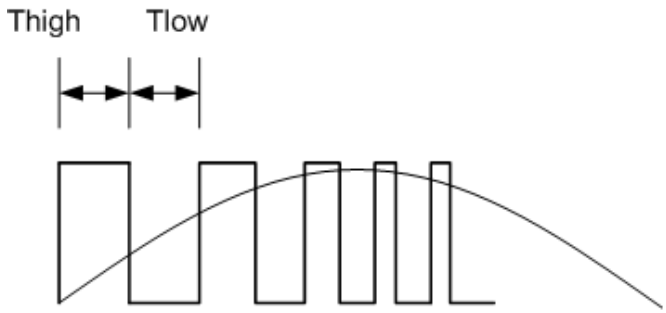


Figure 4.6. Resolution information in the pulse duration of PWM

4.4. Filtering and Down Sampling of PWM Modulated Signals

The PWM modulated input signal at the output of the ASDM is still a continuous time signal. An carries infinite information in its duty cycle. To get a digital value of the input signal, time intervals at a specific high-low pattern should be measured. The value of the input signal corresponds to the digital value of the duration of the high time minus the low time. In classical SDM coding the output rate is fixed and the resolution information can be extracted by averaging several succeeding pulses. Since low resolution information information is output at the modulator and the according to $\Sigma - \Delta$ coding the resolution information is sent over a time period serially.

The case in the ASDM is different. At each high-low package an instant value of input signal is PWM coded. The decoding of this code resembles much to a flash

converter operation which do not compare levels of amplitude but amount of time duration. For accurate digital conversions exact measurements of the pulse withs is needed. The resolution of this time measurement divided to the one period modulated signal is the number of distinguishable steps thus resolution. This is usually dependent to how fast the pulses can be count and is strictly technology dependent. As the dimensions of the transistors shrink with the down scaling technology lower delays, thus increased resolutions can be achieved.

4.5. Analog Filtering of Digital Signals and Time to Digital Converters(TDC)

Asynchronous $\Sigma-\Delta$ modulator output is still an analog signal. This signal should be sampled before or inside the decimation and filtering process. Sampling before the decimator requires a switch operating at limit cycle frequency which is very high most of the time. If the rate of the pulse is slowed down, sampling at a lower frequency can be performed. One way to achieve this is the method of CIC filtering which is investigated in the previous section. Since the ADC is asynchronous, the integrators hence the accumulators in the CIC filter should be build in an analog or digital manner as given in Fig. 4.7.

Another way to convert a signal to digital is to use the Time to Digital converters

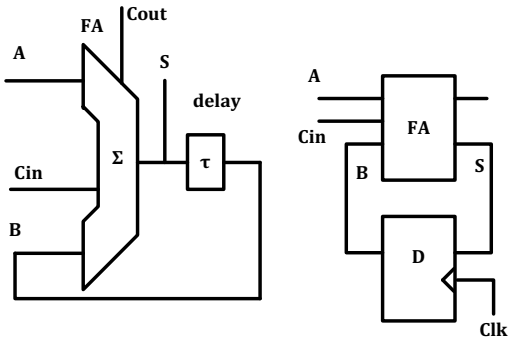


Figure 4.7. Analog accumulator with delay line(left) , digital accumulator (right)

[28]. The signal passes several delay elements and at each tap it is sampled with a D flip-flop. The outputs of the flip-plops are averaged and the resulting digital signal is fed to the original decimation filter.

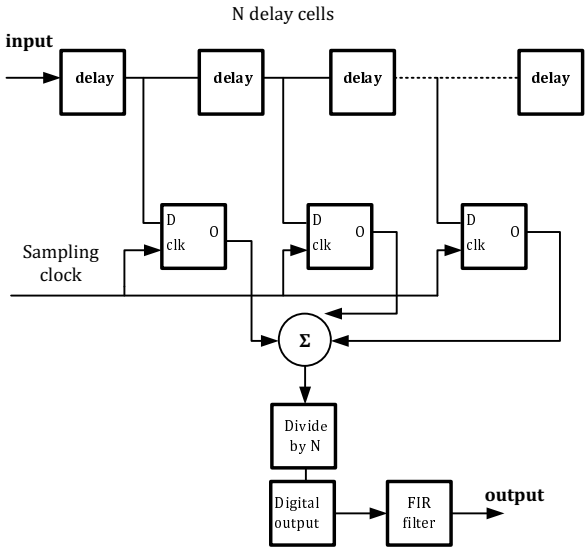


Figure 4.8. Block diagram of the TDC

4.6. Conclusion

There are two ways to convert an PWM signal to a digital code. In both ways the signal is discretized in time. If signal is directly sampled for a 200 MHz limit cycle frequency and 6 bit information a sampling clock of 64 x 0.2 GHz = 12.8 GHz clock is needed. That shows up limit cycle frequency is also directly influential to the number of bits. So for a limit cycle of 50MHz and 6 bit resolution a 64 x 0.05 = 320 MHz is needed.

The proposed architecture uses inherent accumulator delay and the need of an high external clock and sampling operation is eliminated. For a 6 bit resolution with a limit cycle of 50MHz, delay of the accumulator should be less than 20 nsec/64 = 312.5 psec. A 5-bit resolution at the same limit cycle frequency gives a minimum of 20 nsec / 32 = 625 psec.

5. CIRCUIT IMPLEMENTATION

5.1. Introduction

The implementation considered in this dissertation basically consists of two main sections. The first part is the $\Sigma - \Delta$ modulator which is analog; the second part is the decimation filter which has both analog and digital parts. Three modulators have been designed: one first order, one second order, and one third order. If enough separation between the in band and limit cycle Bessel components has been achieved, the performance of the ASDM is bounded by the noise floor created by the total distortion of the components used. Increasing the filter order to third order only adds more components which will increase the distortion. Since third order modulator advantages are very limited compared to the second order, third order modulator is not carried to the chip layout. The block diagram for the analog part in the chip is given in Fig. 5.1. In this part the key contributions are:

- Improved current-mode comparator with adjustable delay.
- Novel current-mode first and second order ASDM implementation.

The first stage in all the modulators is the voltage to current (V-I) converter which is denoted as 'g_m' in the figures. The second block is the current-mode integrator with the capacitors used for integration. The integrator block also amplifies the signal. After the integration blocks a current comparator is used. In the second order modulator, a feedforward architecture is used. The main design consideration for the modulator part is the linearity of the modulator circuit. Current-mode circuits have received more attention recently, due to their reduced power consumption and increased bandwidths [29], [30]. In order to get a large input bandwidth which requires high limit cycle frequency current-mode circuits are utilized. As it will be shown in the next sub-section the integrator linearity is very crucial thus gm-C integration is needed. The main building blocks necessary for sigma-delta modulators are filters of multiple orders and a quantizer. Filters are constructed with integrators, and quantizers with comparators.

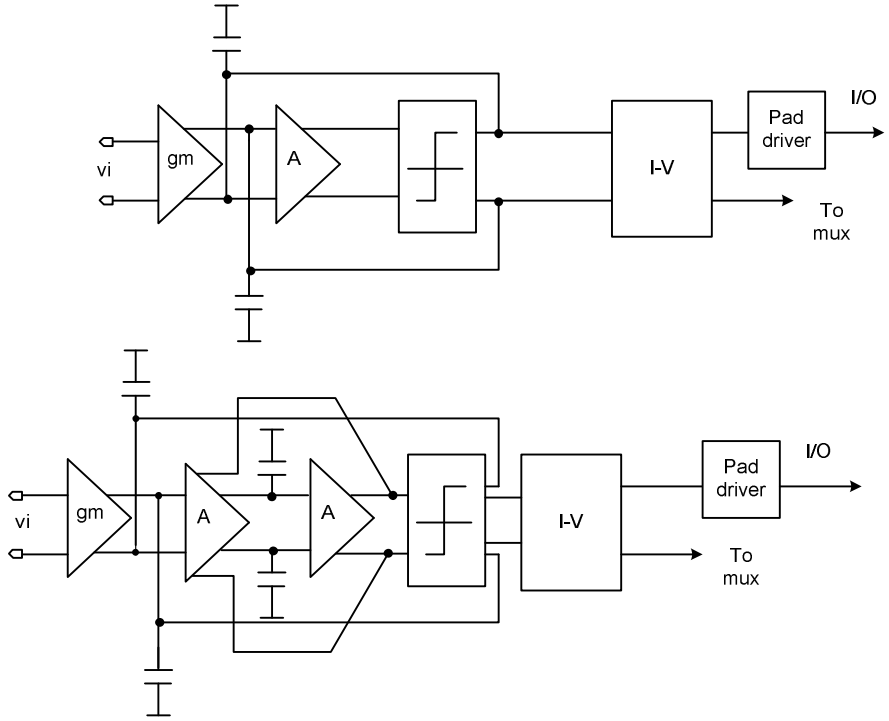


Figure 5.1. Designed analog circuits showing its building blocks

Spurious Free Dynamic Range (SFDR) is also an important performance metric in $\Sigma - \Delta$ modulators [44]. One way to improve SFDR is to use a differential signal due to its ability to suppress second order noise and distortion components. The main cause of the degradation in the asynchronous sigma delta converter is the nonlinearity of the building blocks. Current mode circuits bring the opportunity to increase the linearity by decreasing the voltage swings. Also they have the advantage of operating at high speeds and consume lower power.

In this thesis Austrian Micro Systems (AMS) $0.35\mu m$ technology is used through all the design. Mentor Graphics and its CAD tools are used for design, chip layout and simulations.

5.2. The Impact of Linearity of the Components used in ASDM to the Total Performance

A first order ASDM basically consist of three building blocks, i.e voltage to current converter, integrator and comparator. These blocks are indeed amplifiers and have some nonlinearity. The effect of the building blocks nonlinearities on the whole

modulator can be better studied with Fig. 5.2. The dependencies of the distortions introduced into the loop can be studied with the help of (5.1).

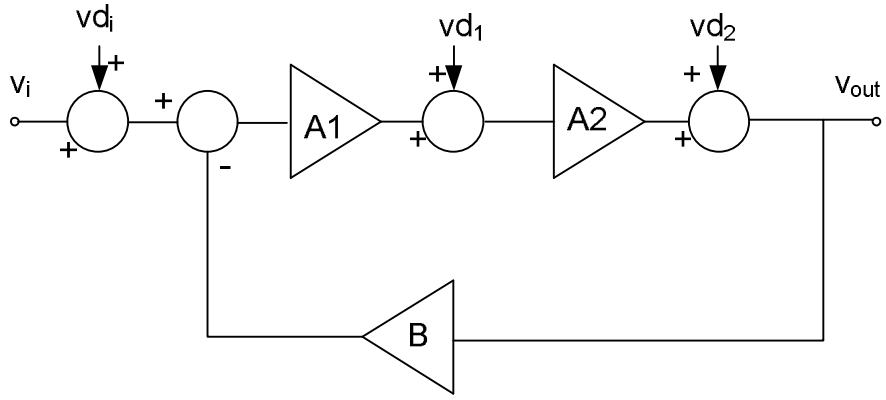


Figure 5.2. Block diagram of a closed loop system with several gain stages

$$v_{out} = \frac{A_1 A_2}{1 + A_1 A_2 B}(v_i + vd_i) + \frac{A_1}{1 + A_1 A_2 B}(vd_1) + \frac{1}{1 + A_1 A_2 B}(vd_2) \qquad (5.1)$$

As it can be seen distortion coming from input, i.e, the voltage the current converters distortion is not suppressed inside the loop. Secondly, the integrator distortion is suppressed by an amount of $1 + A_1 B$. Since the block is an integrator its gain is not the open loop gain for a 1MHz signal, in fact is around 2 in the implementation in this dissertation. So, integrator nonlinearity is also not much suppressed by the loop. The nonlinearity of the comparator is much suppressed from the loop because of the high gain of the comparator. So, the linearity of the voltage to current converter and the integrator should be as high as possible.

5.3. Voltage to Current Converter

Voltage to current (V-I) converter is the first stage of the modulator and its linearity is very crucial. In order to get a high SFDR and also Signal to noise and distortion ratio (SINAD), the harmonics of the converter should be greatly eliminated. Many V-I converters have been presented up to date [31]-[43]. The converters [31]-[39] using classical approaches achieve a maximum of 60 dB SFDR. Approaches [40] and [41] provide higher SFDR. The proposed converter in [43] uses the source resistor

and output current differencing methods both and can eliminate the third and fifth harmonics completely. The diagram of the converter is given in Fig. 5.3. The converter

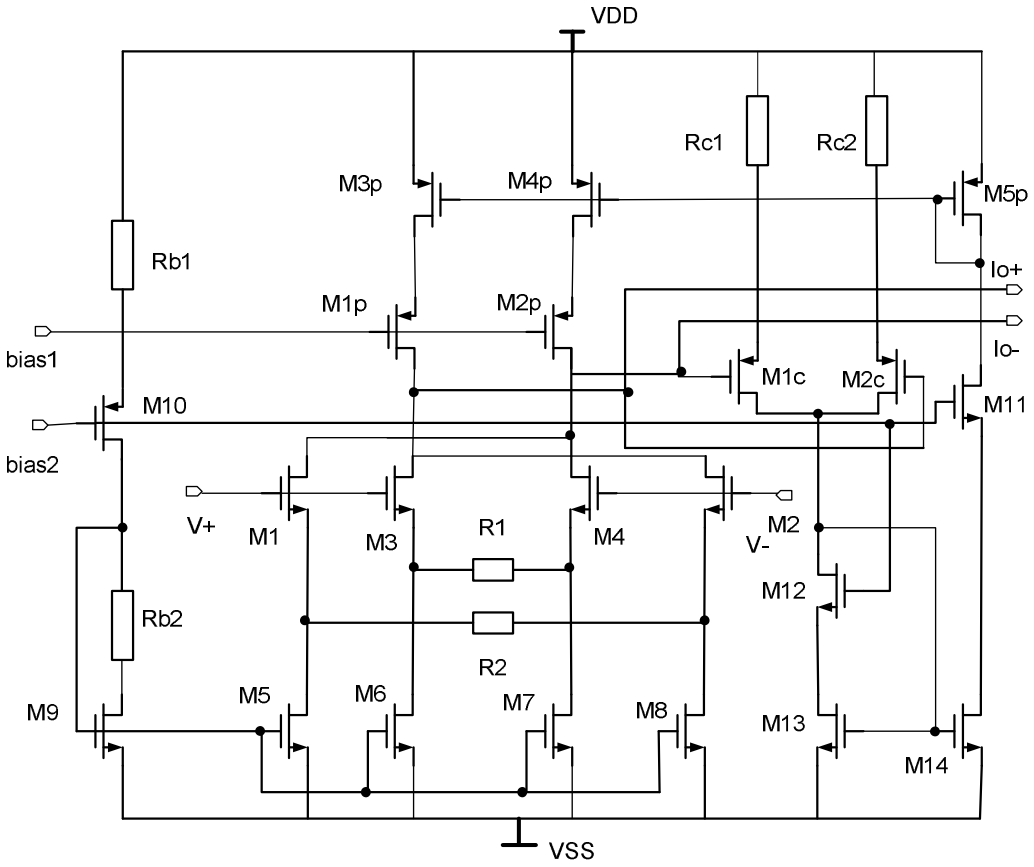


Figure 5.3. Voltage to current converter used in the modulators

is the mix of resistor degenerated differential pair and cross-coupled differential pair. Transistors M1 to M4 are forming the cross coupled differential pair with their current sources. The resistors R_1 and R_2 are degeneration resistors and are separate to increase the degree of freedom. Transistors M1c, M2c, M12, M13 and M14 are forming the common mode circuit. Using the component ratios given in [43], it can be seen that the third and fifth harmonics are minimized. The Power Spectral Density (PSD) of the simulation is given in Fig. 5.4. The sizes of the circuit components are adjusted to suppress the harmonics of the output here are suppressed by more than 70 dB. In fact, in the real chip, a noise floor is generated because of the mismatch between the components which is the main limitation of the performance.

The layout of the V-I converter is given in Fig. 5.5.

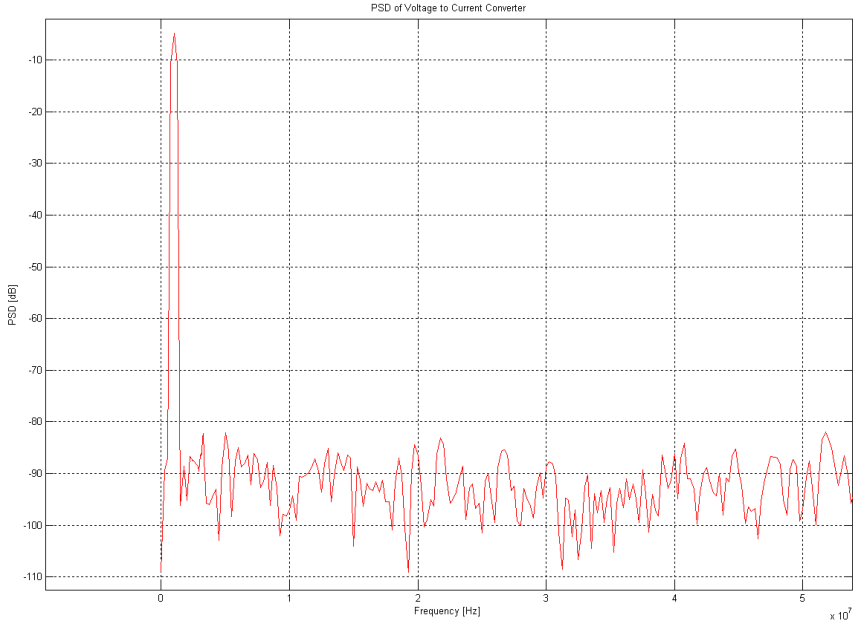


Figure 5.4. Voltage to current converters harmonics

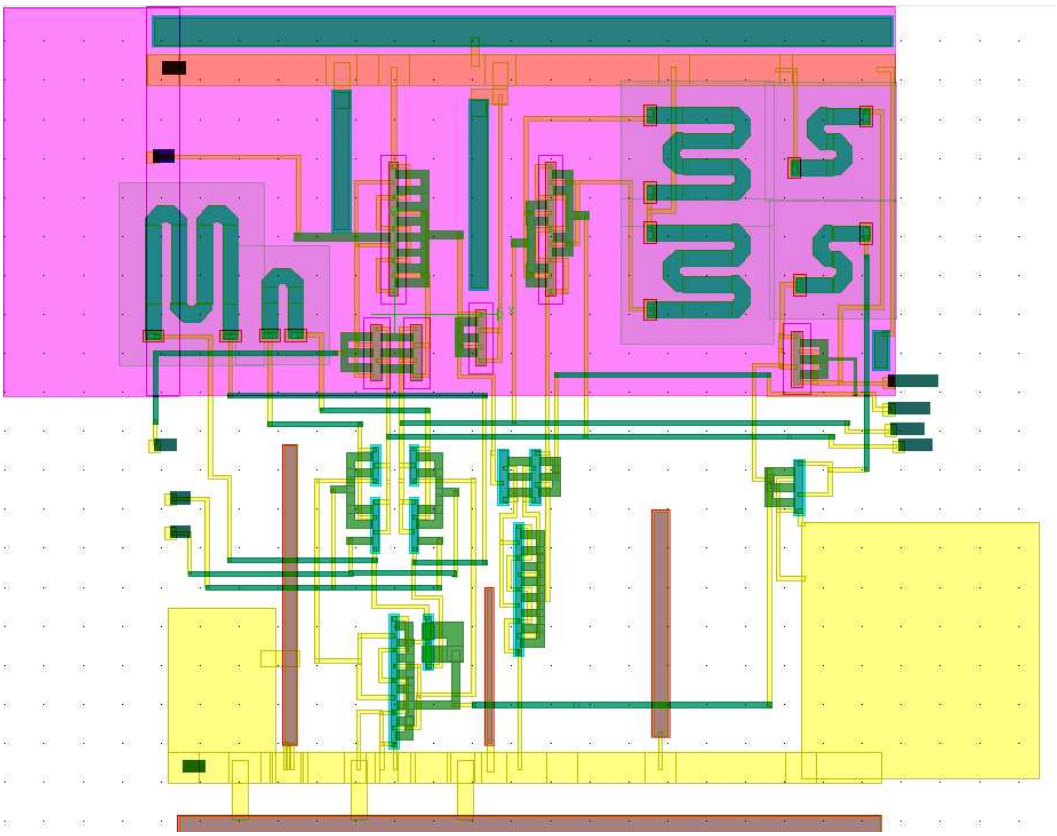


Figure 5.5. Voltage to current converter layout used in the modulators

5.4. Current-mode Integrator

Integrators are the main building blocks of $\Sigma-\Delta$ modulators. Any filter function is realizable by using integrators. Current-mode integrators are more advantageous than their voltage-mode counterparts in aspects of supply voltage reduction, power, bandwidth and also Third Harmonic Intermodulation (IM3) distortion. The integrator proposed in [45] provides very good specifications like low IM3 distortion, therefore is an excellent one to use. In real circuit design, an ideal integrator is very hard to realize because of the nonidealities. Since the circuit has finite input resistance, the realized function will be in fact a low-pass filter. However, placing the low-pass filter pole near zero provides an ideal like integrator. The input-output transfer function for differential and common-mode gains are:

$$\begin{aligned} A_{dif} &= \frac{I_{o+} - I_{o-}}{I_{i+} - I_{i-}} = \frac{\omega_u}{s + (A_n - A_p)\omega_u} \\ A_{CM} &= \frac{I_{o+} - I_{o-}}{I_{i+} - I_{i-}} = \frac{\omega_u}{s + (A_n + A_p)\omega_u} \\ \omega_u &= \frac{g_{mo}}{C_I} = \frac{g_m}{C_I A_N} \end{aligned} \tag{5.2}$$

The expression 'ω_u' represents unity current-gain frequency of the integrator. It is wise to select '$A_n = A_p$' , so that '$A_{diff} = \frac{\omega_u}{s}$' which is an ideal integrator. The gain expressions in 5.2 are derived by first order analysis. However, it is known that second order effects in electronic circuits may have a deep impact. The small signal model showing non-idealities for one of the differential input is given in Fig. 5.7. The final expression for the gain of one differential input, obtained from the small signal model with second order effects taken into account is given below [46]:

$$\begin{aligned} A_{diff} &= A_0 \frac{(1 - s/z_1)}{(1 + s/p_1)(1 + s/p_2)} \\ A_0 &= \frac{g_m - g_{ds}}{2gds} \\ z_1 &= \frac{g_m - g_{ds}}{2C_{gd}} \\ p_1 &= \frac{2g_{ds}}{C_I + 4C_{gd}} \end{aligned} \tag{5.3}$$

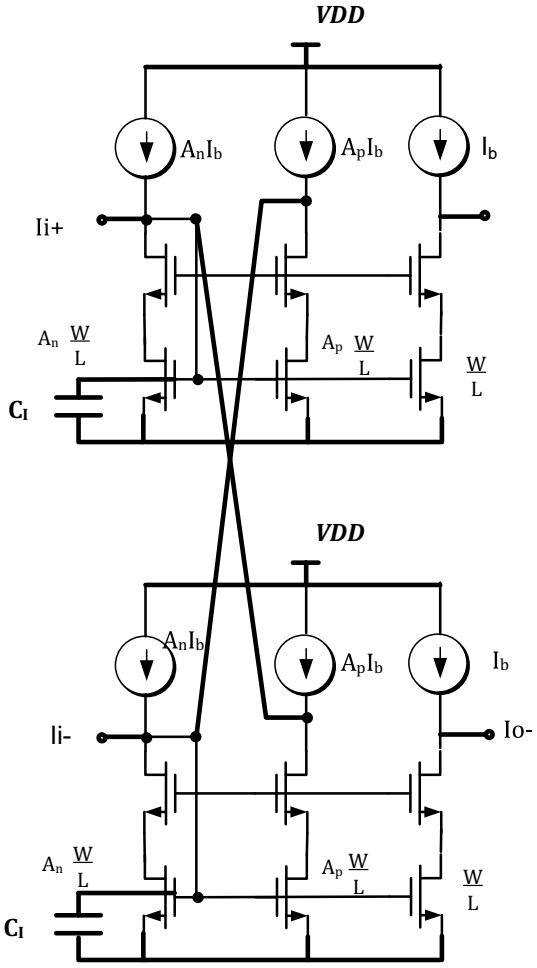


Figure 5.6. Current-mode integrator proposed in [45]

The right hand plane zero (RHZ) is due to the direct signal path through C_{gd} at high frequencies. Fortunately, since there are two complementary signal paths, RHZ's of the differential signal cancel out and has no effect on the differential current gain. The second pole also cancels out due to the differential signaling. The final differential gain is:

$$\begin{aligned} A_{diff} &= \frac{A_0}{(1+s/p_1)} \\ A_0 &= \frac{g_m - g_{ds}}{2gds} \\ p_1 &= \frac{2g_{ds}}{C_I + 4C_{gd}} \end{aligned} \tag{5.4}$$

This creates a wide range of linear operation area. The ultimate point of limitation in the transfer function is the second order effects caused by the current sources. As it can be observed from Eq. 5.4, the pole cannot be at zero but can be placed near to zero. One observation is that to increase the DC gain (A_0) of the integrator and also the place of pole 'p_1', the value 'g_m/g_{ds}' should be increased. So, small values of 'g_{ds}'s are desirable. Building the top current sources as cascode can serve this purpose. The final integrator used is given in Fig. 5.8 .

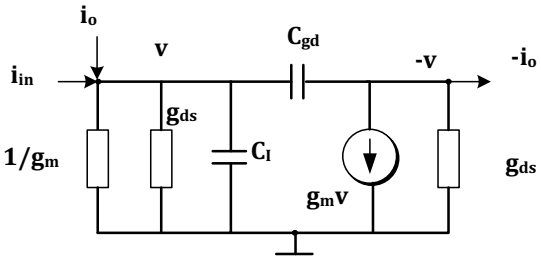


Figure 5.7. Small signal model of the current-mode integrator

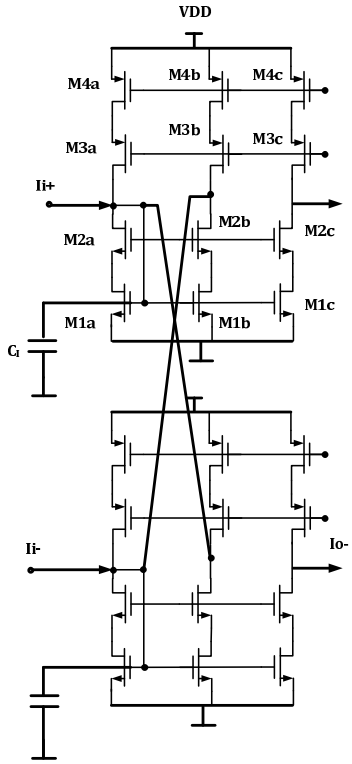


Figure 5.8. The integrator used for better gain(A_0) and transfer characteristics

In order to maintain correct operation in corner cases channel lengths were chosen

as two times the minimum, based on data from simulations. The dimensions of the transistors are given in Table 5.1. The simulation results are given in the results section. The layout of the used integrator used is presented in Fig. 5.9.

MOS	W/L ($\mu m/\mu m$)
$M1_{a,b,c}$	6/0.7
$M2_{a,b,c}$	3/0.7
$M3_{a,b,c}$	3/0.7
$M4_{a,b,c}$	3/0.7

Table 5.1. Transistor aspects of the integrator

.

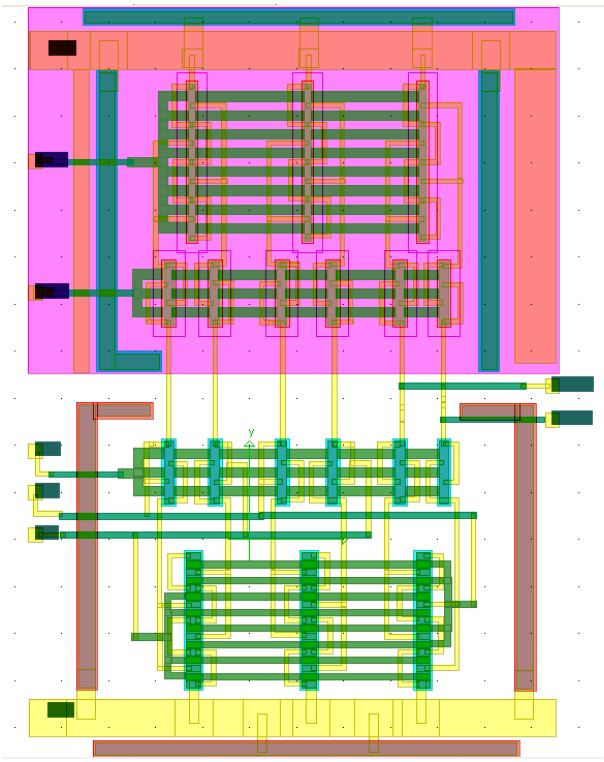


Figure 5.9. The layout of the integrator used in the first order $\Sigma - \Delta$ modulator

The simulated frequency characteristics as provided in Fig. 5.10 confirms the predicted behavior.

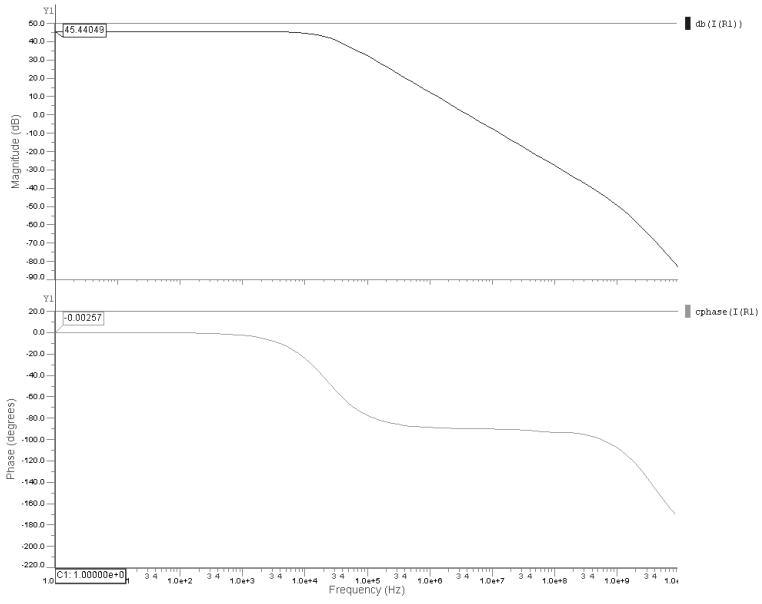


Figure 5.10. The AC response of the integrator

The PSD of the integrator depicted in Fig. 5.11, shows a suppression of more than 70dB for the third and fifth harmonics.

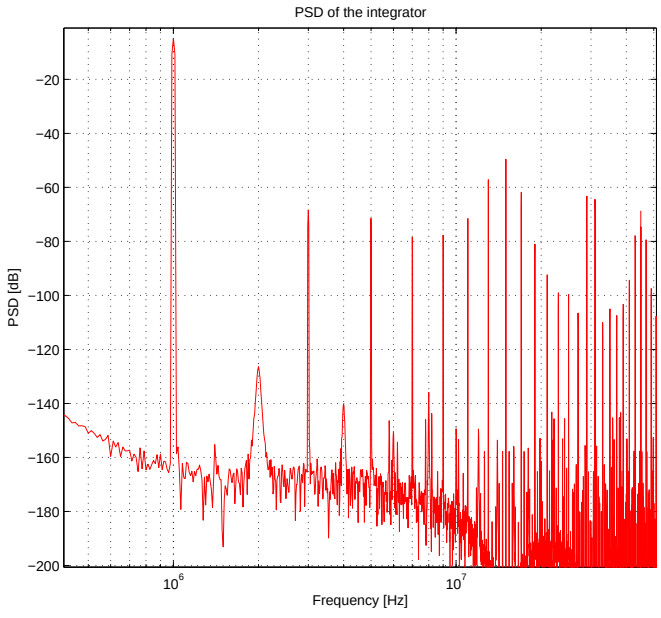


Figure 5.11. The PSD of the integrator showing more than 70dB suppression of spurious harmonics

5.5. Current Comparator with Current Output

The next block necessary for building an ASDM is the quantizer. Quantizers can be constructed with a single comparator or a combination of comparators depending on the number of quantization levels. In this design, 1-bit quantization is used. As the circuit is designed in current-mode, a current mode comparator is necessary.

Different current comparators have been proposed until now. The first proposed comparator was based on current mirrors, which operate in a class AB amplifier fashion. By large output resistances of the current mirror, small input currents are turned to large voltage variations. Since additional stages are needed for for rail to rail output, bandwidth is very limited [47]. One other disadvantage is the worse response time, i.e. large delays. The comparator proposed in [48] and given in Fig. 5.12 solves most of these problems and requires simpler circuitry. It uses the principle of charging an inverter input capacitance by current until output state is changed. This mechanism is shown in Fig. 5.13. The output of the inverter $M_3 - M_4$ is low initially. Upon the application of the current pulse, the input capacitance of the inverter begin to discharge until the switching threshold is reached. The complete circuit then prevents the charging of the input node by turning ON the transimpedance loop of M_1 and M_2 and providing a low resistance path to ground or supply voltage(VDD). The transistors M_1 and M_2, also bias the inverter near the middle of the transfer characteristics. In the next cycle, when input pulse turns to low from high value, inverter input capacitance will discharge until the switching threshold is crossed in the opposite direction. Typical transient response curves of $I_{in} - I_{out}$ and Vin are given in Fig. 5.14 .

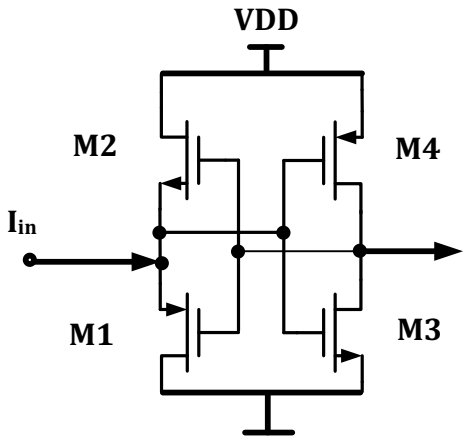


Figure 5.12. Comparator proposed in [48]

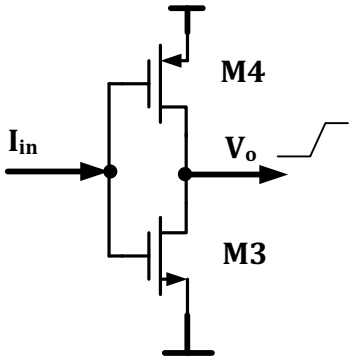


Figure 5.13. Comparator proposed in [30]

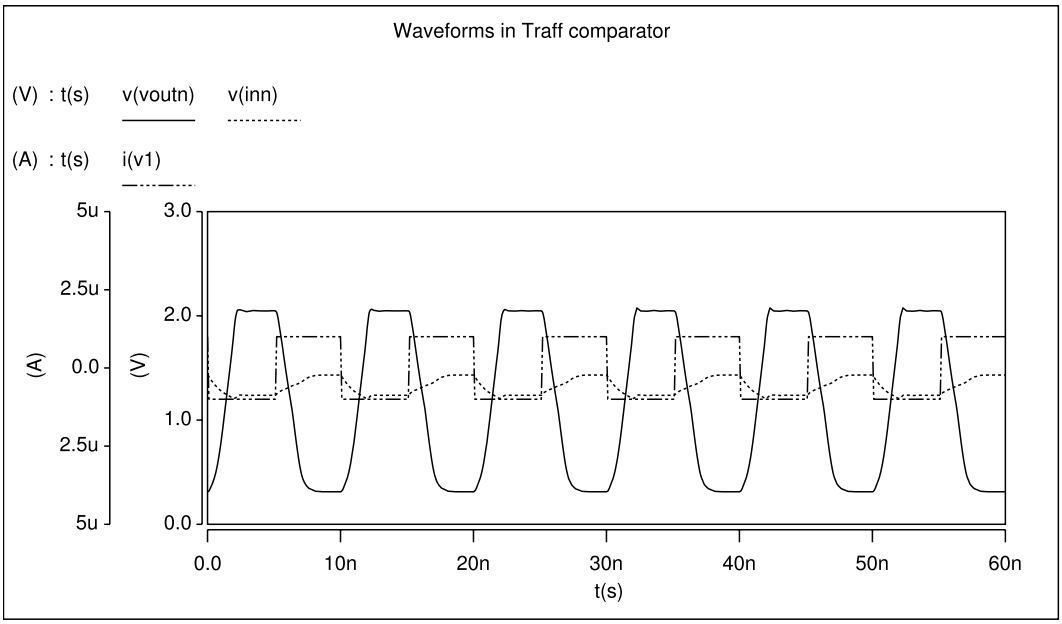


Figure 5.14. Waveforms of Traff comparator Vin, Iin and Vout, when squarewave input of $\pm 1 \mu A$ is applied

The voltage can be converted to current again by a Voltage to Current(V-I) converter as in Fig. 5.15 Although the input-output current characteristics of the com-

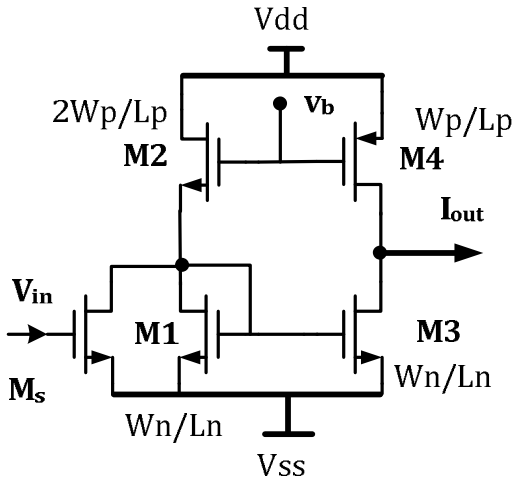


Figure 5.15. Voltage to current converter

parator in [48] is a saturation nonlinearity with round-offs near the saturation limit, the complete comparator with the V-I converter shows no rounded corners. This can be observed in Fig. 5.16 . One problem observed is the small dead-zone region created by the voltage to current converter in the overall transfer function near zero input. The circuit which will take the difference of the currents in both channels will solve this problem, which will be explained in the next subsection. One major problem of this type of comparator is the large delay caused by bringing the input trans-impedance loop transistor out of the sub-threshold region. In the next section, a modification to reduce the delay is given.

5.5.1. Comparator with Adjustable Delay

Several methods to reduce the delay of the comparator have been proposed. Two important ones are [49] and [50]. In [49], a biasing scheme of input transistors is given to make them always ON in a class AB like fashion. In [50], a resistive feedback is used to decrease the amount of delay. The proposed delay adjustment will be explained in the following subsection.

In most comparison applications, steepness of the transfer curve is important.

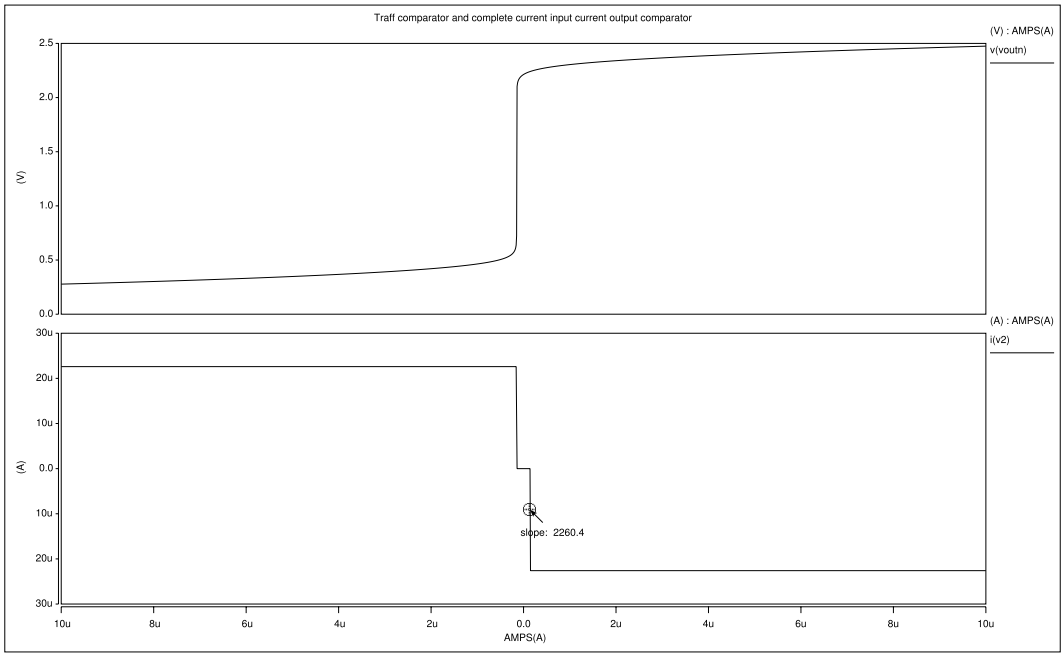


Figure 5.16. Transfer curves of the: a)Traff comparator(voltage output) and (b)the whole comparator with V-I converter

Therefore, a sufficient number of inverters are put after the comparator part. In this design, an additional latch is added after the comparator (instead of a regular inverter). This latch is cross coupled between the two channels of the comparator as shown in Fig. 5.17. Considering that a differential signal is applied to the comparator, the latch output will toggle upon the state change of the two comparators. The sizes of the transistors are selected so that the comparator will be able to drive the latch. The action of this additional latch is to favor positively the change of the comparator output. However, this additional circuitry creates a new behavior since the inverter and input transistors are coming to balance after the output change in the original configuration. In the new circuit, the input transistors are pulled more aggressively to sub-threshold and saturation because of the latch. However, the latch brings some advantages: the signals on separate channels are non overlapping and their pulse widths do not change by the amount of the feedback applied. This will prevent the creation of extra second order distortion in the $\Sigma - \Delta$ modulator output. The second modification is to apply a positive feedback as proposed in [51] with a pmos transistor in order to decrease the amount of delay. The amount of feedback can be adjusted with the gate voltage of the transistor. At $v_{control} = Vss$, maximum amount of feedback, thus minimum delay

has been achieved. The change of input voltage 'V_{in}' when a $\pm 1\mu A$ square input is

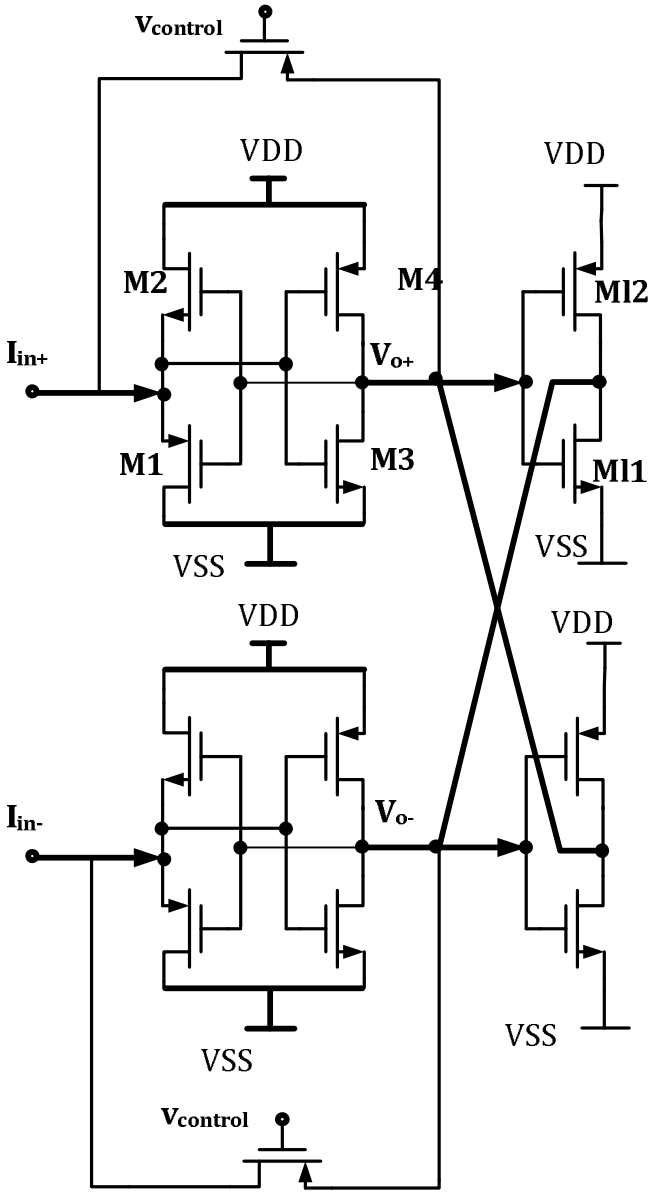


Figure 5.17. Latch and feedback circuit added to the original comparator

given in Fig 5.18. As it can be seen, after the switching threshold is reached, every comparator settles to a different 'V_{out}' value. The time to reach the switching point is approximately the same, except the additional region created to jump to the settling value. Delay can be greatly reduced to the orders of 1 ns with transistor channel lengths as $0.7\mu m$ and with appropriate widths, but this delay is a critical value. Therefore, it will be wiser to use it in a safe operating region. This configuration does not require complex biasing as in the comparator of [49] which is prone to suffer from component

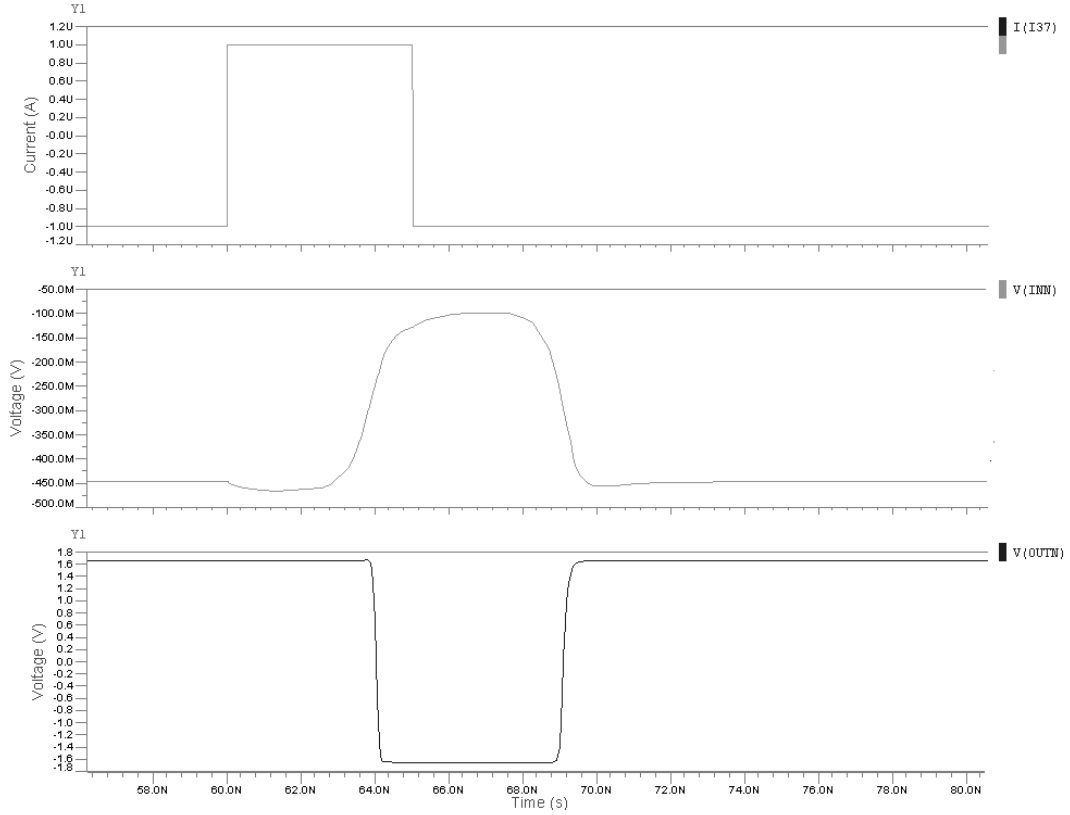


Figure 5.18. Input and output voltages of the comparator upon application of 1 μ A square input current

mismatch. To avoid any possible mismatch in the feedback circuit (pmos transistors), separate control voltages for the two channels can be used.

In order to get a steeper transfer function, 3 inverters are added which do not contribute to delay very much. At the end, voltage is converted to current with the V-I converter of Fig. 5.15. To ensure fully differential operation and reject common mode, two channel currents are subtracted from each other with a current differencing circuit. The schematic of the complete comparator is given in 5.19. The adjustable delay comparator is used in the ASDM circuit as a delay element preceding the quantizer. Note that in Chapter 3, analysis for nonlinear loops containing delayed integrators was performed. The comparator delay can be represented in the block diagram as a delay element before the ideal comparator. Therefore, it can be thought that the transport lag term will be included to the loop filter transfer function. Adjustable delay will give the chance to observe different limit cycle frequencies and the change of spectra

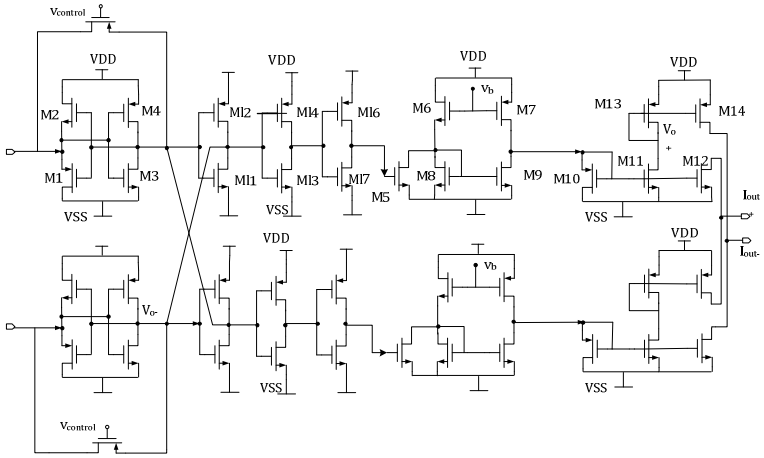


Figure 5.19. The complete current comparator consisting of: the comparator, voltage to current converter and current differencing parts

according to them.

One final circuitry is added to the comparator for proper operation. That is the 'Current Differencing' unit(M10,M11,M12,M13,M14 and the counterpart mosfets for the other channel). It basically takes the difference of two outputs coming from the comparator.

5.6. 2's Complement Encoder and Pre-delay Circuit

The filter is designed to have a 15-bit data path. The maximum achievable SNR value gives about 11 bits. The output of the $\Sigma-\Delta$ modulator is a PCM signal toggling between '± 1'. In order to use it in a filter, its 2's complement should be taken, which is a simple task. After the $\Sigma-\Delta$ modulator, the output voltage is propagated to the filter section. The $\Sigma-\Delta$ modulator output has to be transformed to 2's complement form. The translation is depicted in Table 5.2.

Table 5.2. 2's complement encoding of the $\Sigma-\Delta$modulator output

$\Sigma-\Delta$modulator output	2's complement encoded form
$+1$	000000000000001
-1	111111111111111

Since there is a delay in the full adders of analog accumulator in the next section, the input thus the outputs of the 2's complement block should be encoded to compensate such a delay. So, every output bit of the encoder is shifted by the delay of a full adder which can be seen in Fig. 5.21.

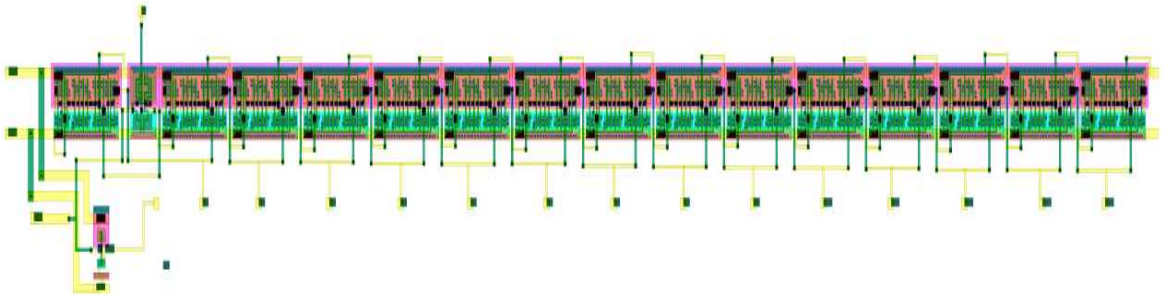


Figure 5.20. 2's complement encoder and predelay circuit layout

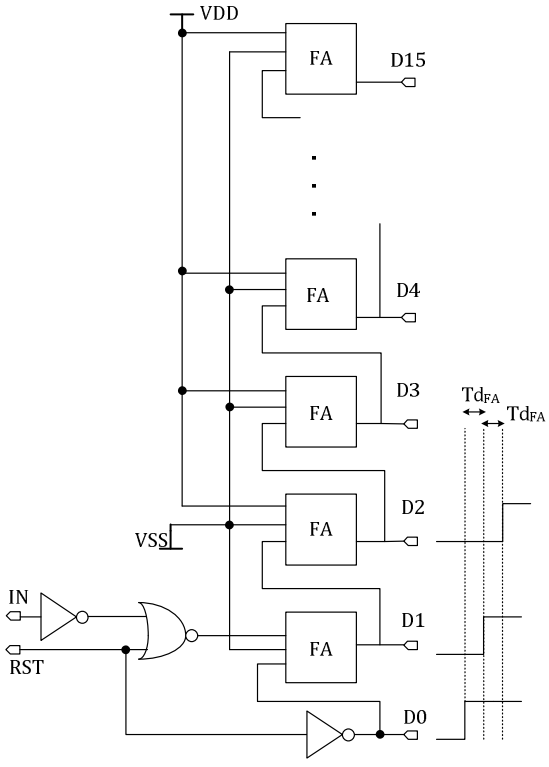


Figure 5.21. 2's complement encoder and predelay circuit diagram

5.7. Creating Pulse Delay with Current Starved Inverter

In order build an accumulator based on a full adder and a delay line, a pulse delay element is needed. Basically, there are two methods for doing this. One is to use an inverter with a capacitive load; the other is to use a current starved inverter. The second method is preferred due to its smaller size. The basic diagram of a current starved inverter with its bias circuit is shown in the Fig. 5.22 . In the filter design,

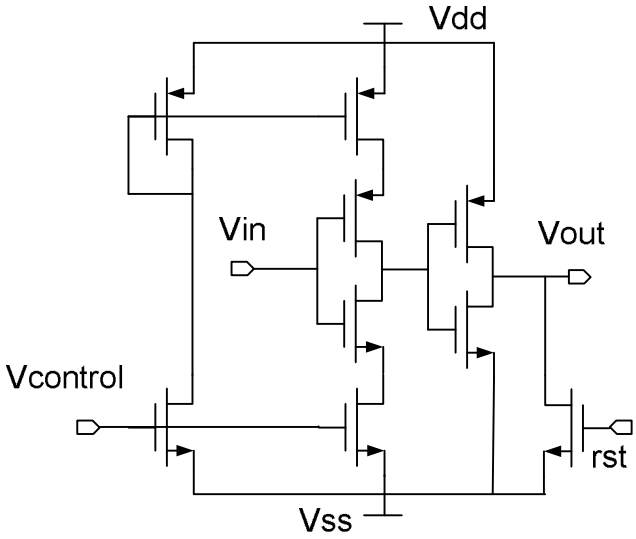


Figure 5.22. Current starved inverter with its control bias circuit to generate delayed pulses

the voltage signal to be delayed is a rectangular pulse of magnitude Vdd and Vss. According to the requirements of the asynchronous $\Sigma - \Delta$, the transistors are sized to give a adjustable delay range from 50 psec. to 470 psec. The layout is given in Fig. 5.23.

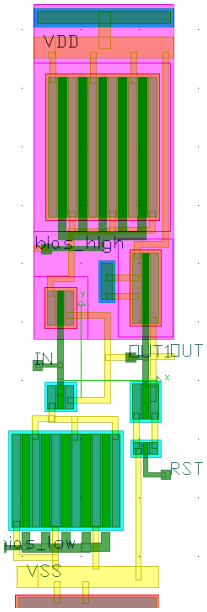


Figure 5.23. Layout for the current starved inverter

5.8. Accumulator

An analog 15-bit accumulator which will count input pulses is constructed using the delay element and a full adder. 15 one-bit analog accumulators as in Fig. 5.24 are cascaded to obtain the 15-bit analog accumulator in of Fig. 5.25.

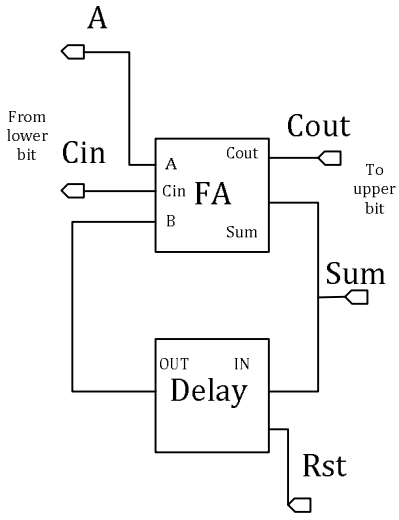


Figure 5.24. 1-bit analog accumulator

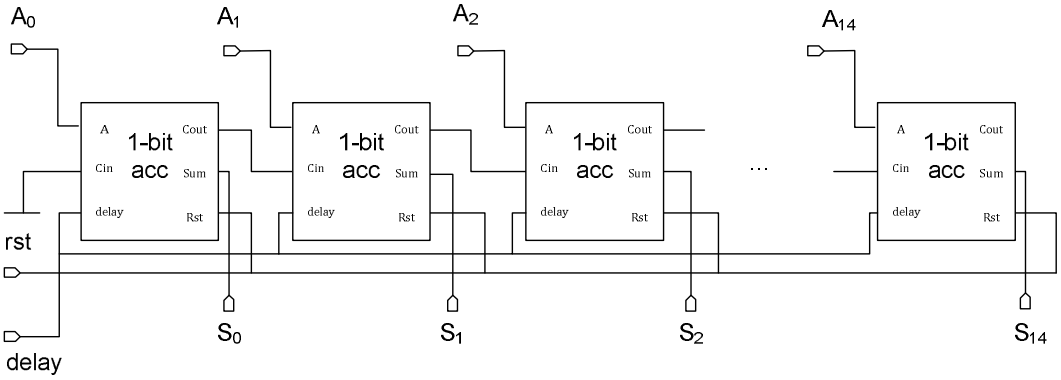


Figure 5.25. 15-bit analog accumulator using cascaded 1 bit structures

5.9. Sampler

After the integration stages, the information signal is undersampled by a 15 bit register using a clock. The circuit diagram and associated layout are depicted in Fig. 5.26 and Fig. 5.27 respectively.

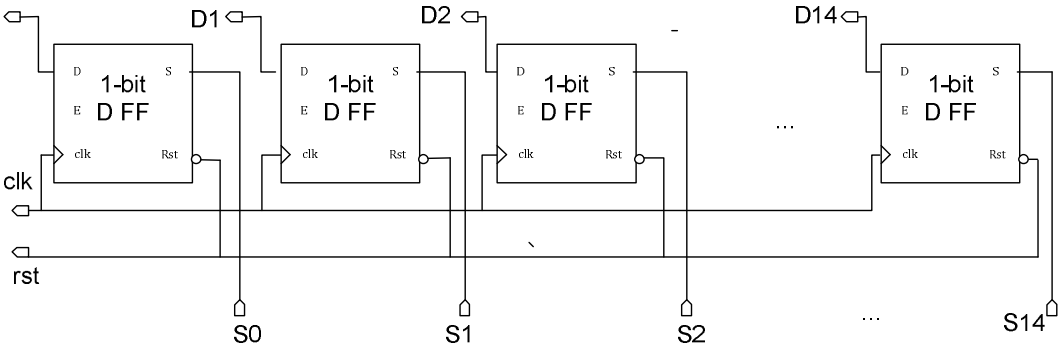


Figure 5.26. 15 bit sampling register

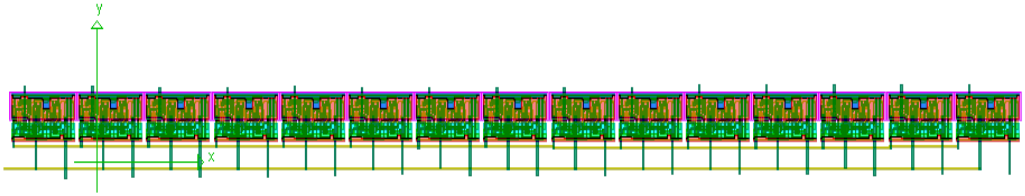


Figure 5.27. 15 bit sampling register layout

5.10. Phase Restorer

Since the pulses coming from the output of the ASDM are encoded with a delay the output bits after the integration stages are still shifted in time. A circuit for correcting the phase difference is needed. One way to do is to pass the bits through unequal delay lines. The signal with largest delay should pass through a minimum delay line and the with smallest delay should pass a maximum delay line. Schematic of the used restorer circuit is given in Fig. 5.28.

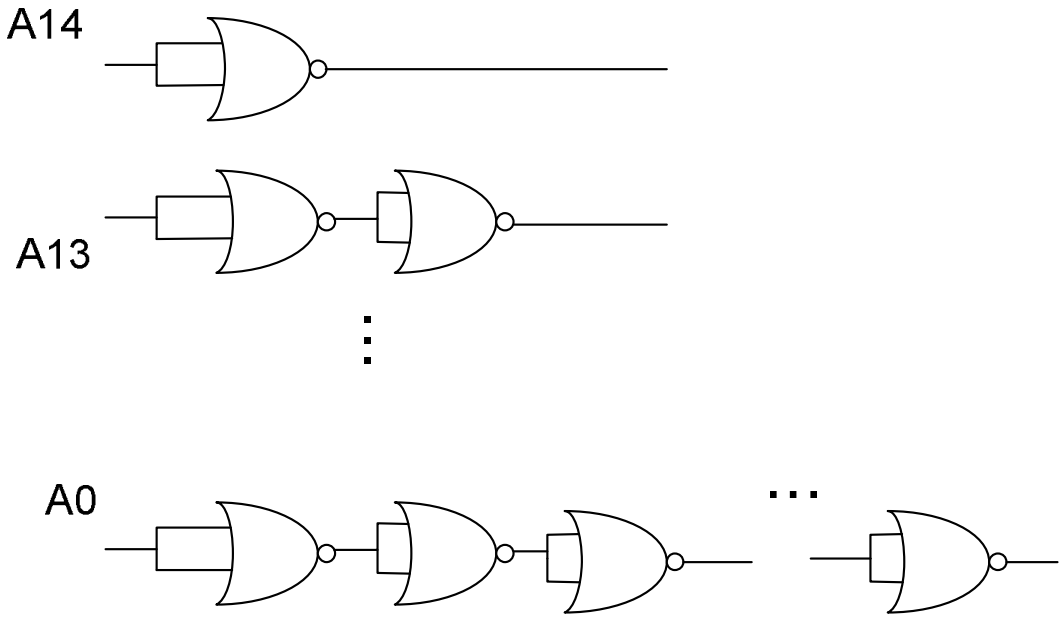


Figure 5.28. Phase restorer circuit

5.11. Comb Filter

A 15-bit comb filter whose circuit diagram and layout are provided in Fig. 5.29 and Fig. 5.30 respectively, is built by cascading 15 1-bit structures.

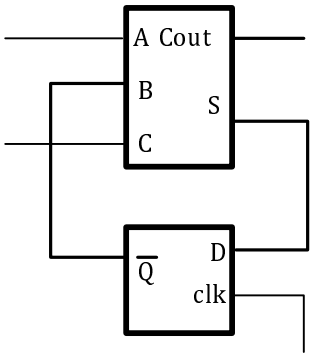


Figure 5.29. 1-bit comb filter

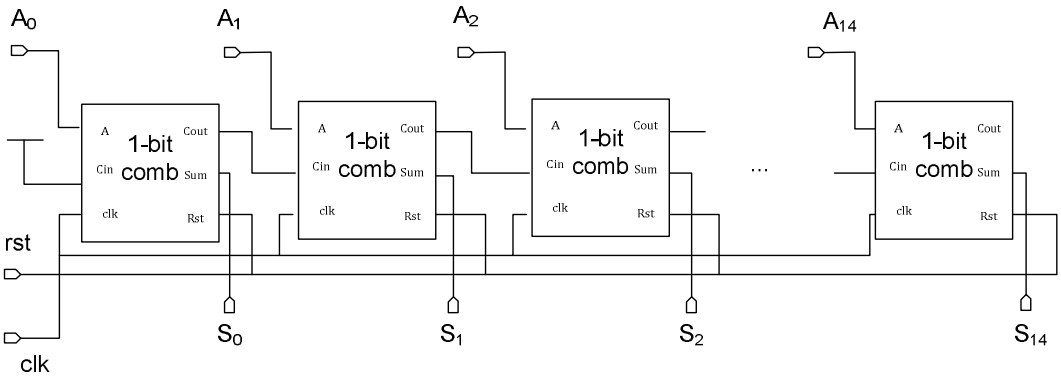


Figure 5.30. 15-bit comb filter

The layout of a one stage 15 bit comb is given in Fig. 5.31.

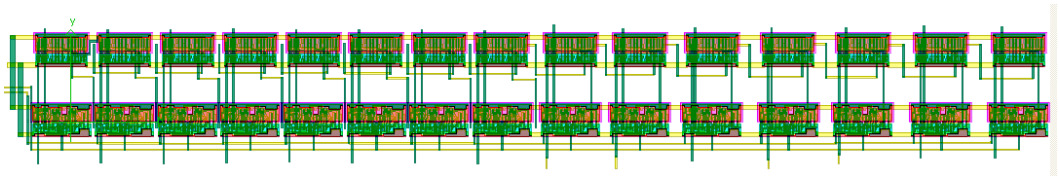


Figure 5.31. 15-bit comb filter layout

5.11.1. Problem of Generated Glitches in the Integrators

An asynchronous accumulator which will hold its input for a certain time period can be constructed using a full adder and delay element. Its synchronous counterpart is built using a full adder and a D flip-flop. There is some difference in their operation

principles. While the synchronous version holds the stored data in the flip-flop one clock cycle, in the asynchronous accumulator the data is stored as long as the delay elements delay value. If the input pulse duration is smaller than this value, the data will be lost after the delay time. If the input duration is larger, the one-bit accumulator will generate a carry for the succeeding bits accumulator. Since the built accumulators

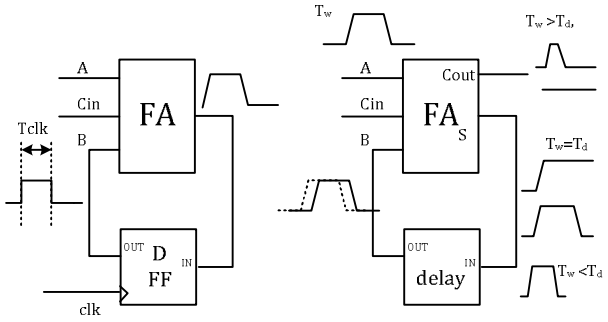


Figure 5.32. Demonstration of possible glitch problem caused by asynchronous data

are working asynchronously any non-overlapping input pulse in the full adder will create shorter pulses then the delay of the current starved inverter. Very short pulses can create some reliability problems in the data accumulation thus wrong output bits. This problem is solved by inserting glitch preventing circuits between several stages of the filter.

6. CHIP DESIGN OF THE ADC

A prototype of the asynchronous sigma delta ADC was fabricated using AMS 0.35 μm technology. The chip consist of two main sections:the modulator section which is analog and the filter section which is mostly digital. In the analog part, one first order and one second order ASDM's are designed. There is a separate I/O pin for both ASDM's to make measurements of their output voltages. There is also a copy of ASDM voltages going to a 3-1 multiplexer. The third input of the multiplexer is a user defined signal coming from outside the chip for test purposes. The multiplexer will select one of the inputs according to its 2 bit selection lines which will be coming from outside the chip. The designed second order modulator is a feed-forward second order ASDM. The complete analog part with the multiplexer is given in Fig. 6.1.

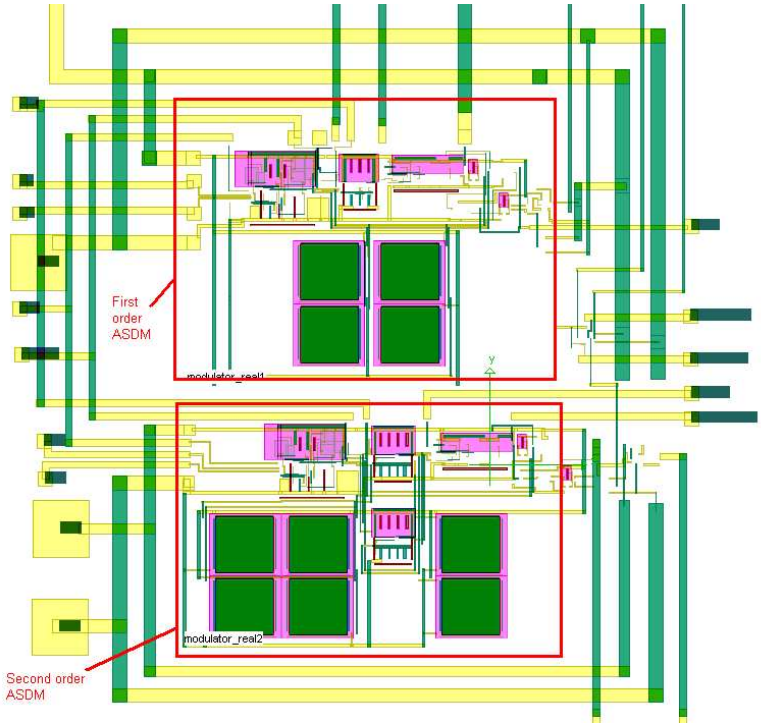


Figure 6.1. The complete modulators part ASDM in the prototype

The first order modulators size is 500 x 360 μm xμm. The capacitors area is 190 x 190 μm x μm. The second order ASDM occupies a chip area 600 x 360 μm xμm.

Capacitor area is 280 x 190 μm x μm. The total analog modulator occupies 600 x 720 μm xμm. The power consumption of the first order modulator is 4.5mW and the power consumption of the second order modulator is 5.2 mW.

6.1. Filter Part

The peak SNR value for the 10 MHz bandwidth is 75 dB. The corresponding number of bits is about 11 bits. There is also a selectable analog input. For future applications which may have an input with higher SNR value the filter is designed to have 15-bits. However, as explained in Chapter 4 the maximum effective bits that can be resolved is dependent to the delay of the full adders in the filter; thus achieved bits are much lower than this value. Sufficient suppression of the harmonics generated by the limit cycle carrier wave is achieved by third order 'sinc' decimation filtering. The schematic of the whole filter is given in Fig. 6.2, whereas the layout is depicted in Fig. 6.3. The filter part occupies an area of 1400 x 2000 μm xμm.

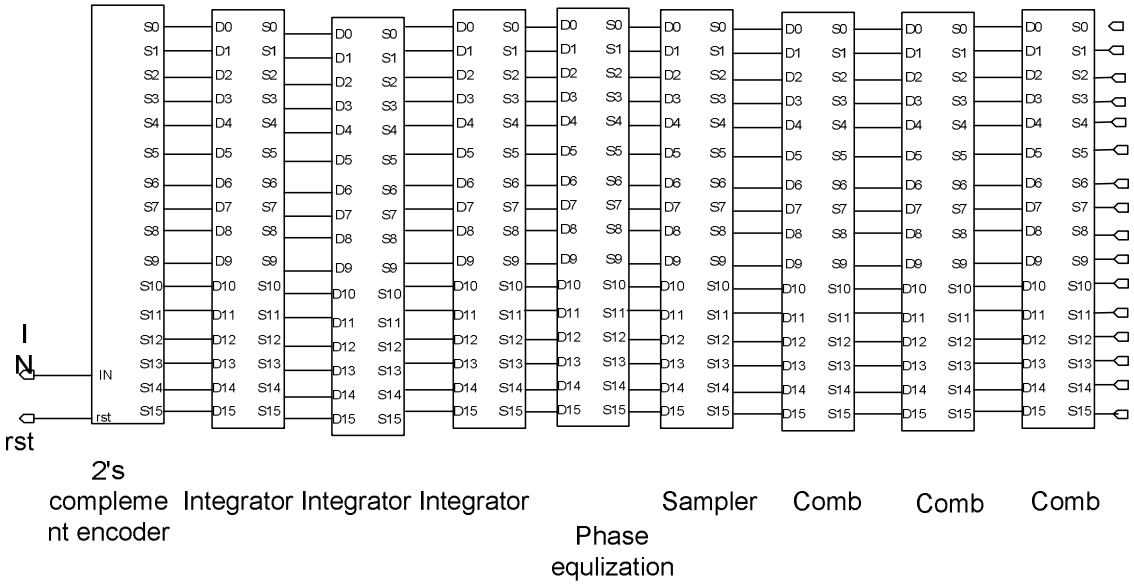


Figure 6.2. Block diagram of the filter section

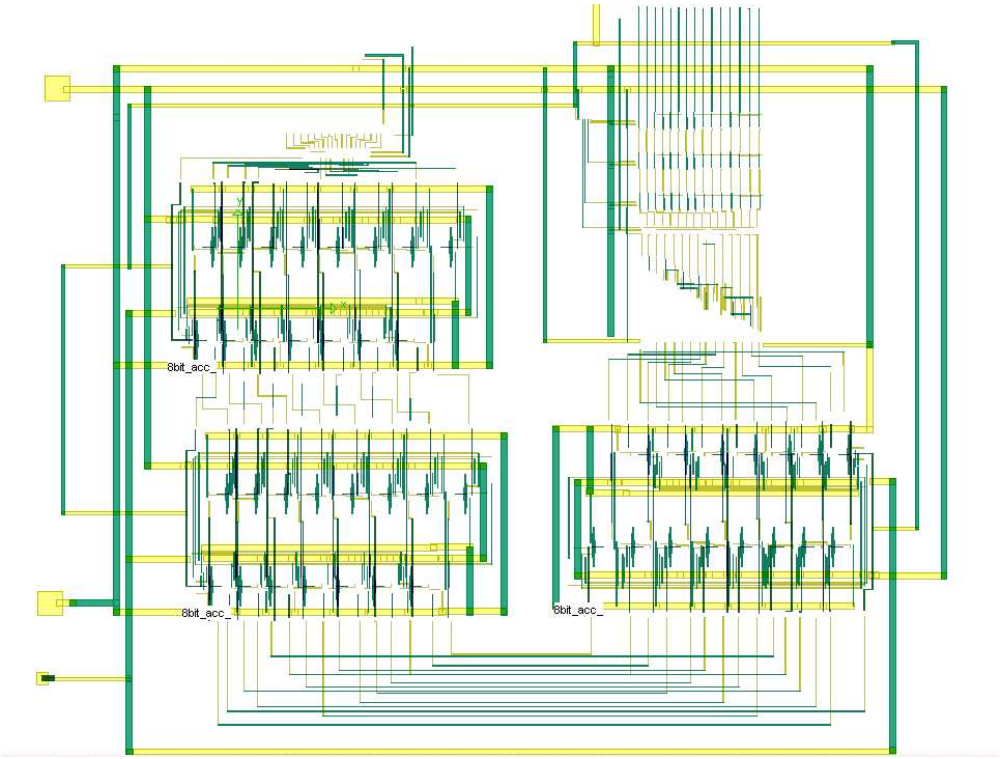


Figure 6.3. Layout of the filter section

Finally, the full chip layout is given in Fig. 6.4.

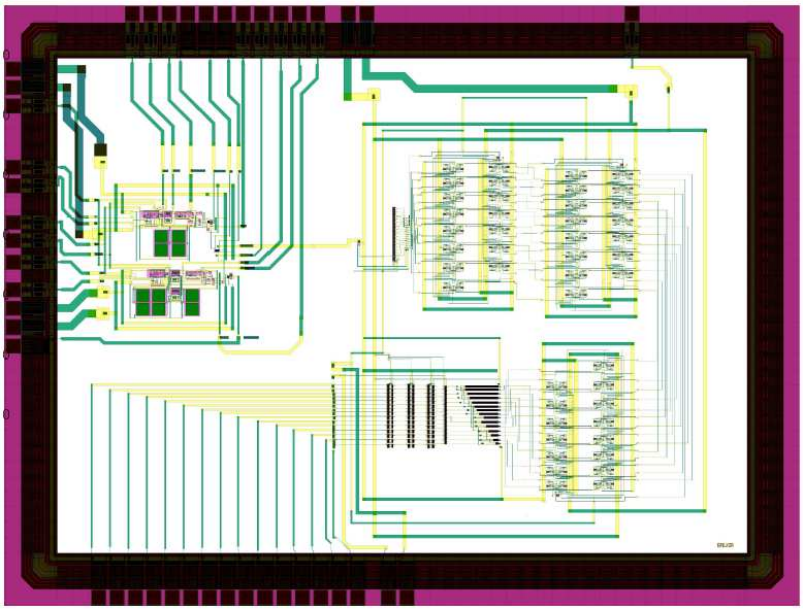


Figure 6.4. The full chip layout with I/O pads

7. RESULTS AND DISCUSSION

7.1. Introduction

In these sections, schematic and post-layout simulation results of the prototype are given. This section is divided into three sub-sections. The first part is about the results of the analog modulator. The results of the output SINAD and SFDR are given in tabular and graphic forms and a comparison with the state of the art circuits is performed. The next section is for the filter results. The overall performance of the ADC is provided. The number of available bits and its dependence to the signal parameters are given. In the last section, the usefulness of the asynchronous ADC is discussed.

7.2. ASDM Part

In the first order modulator, the variable delay comparator given in the previous sections is used. As an adjustable delay comparator is used, the limit cycle frequency can be changed. The range of limit cycle frequencies in first and second order modulators are 50 MHz to 210 MHz. There is 10 % reduction of the limit cycle frequency in post layout simulations, caused by the parasitic capacitances. The maximum available limit cycle frequency in the post-layout simulations is about 190 MHz. Fortunately, the upper-bound of the frequency can be as much as possible depending on the size of the input inverter and the positive feedback circuit in the comparator. However, this increases power consumption in the comparator. At high frequencies, integrator bandwidth limit is exceeded and creates distortion when modulation index is high. Optimum performance has been taken when limit cycle frequency is 180 MHz and below. For a 1MHz test signal, limit cycle frequency above 120 MHz is high enough to assure suppression of the Bessel harmonics. For the modulator section, working at higher limit cycle frequency is most of the time advantageous; since it is preferred that the Bessel components die out in the band of interest. However, technology bandwidth limitations should be taken into account to get optimum linearity.

The Power Spectral Density (PSD) of the schematic simulation for modulation indexes 80% and 30% are given in Fig. 7.1 and Fig. 7.2 respectively. It can be observed that after 20MHz the Bessel components die out. The achieved SFDR is about 75 dB. The noise floor at -80 to -100 dB is observed in the spectrum that is created by the distortion of the circuit elements and Bessel components. As it can be seen when modulation index is 80%, Bessel components grow and limit the input bandwidth. That currents in the circuit are adjusted such that 80% modulation index corresponds to maximum linear region of the input voltage to current converter. The simulated peak SNR value is 75 dB for the schematic and 74.5 dB for the post layout simulation. The SFDR change versus input amplitude level is given in the Fig. 7.3. After modulation index reaches 0.8, the performance decreases abruptly due to the distortion and Bessel components. For the second order modulator implemented the schematic simulations of the design shows that the limit cycle frequency is between frequencies 50 and 210 MHz. In the Fig. 7.4 and Fig. 7.5 circuit simulation PSD of output signal

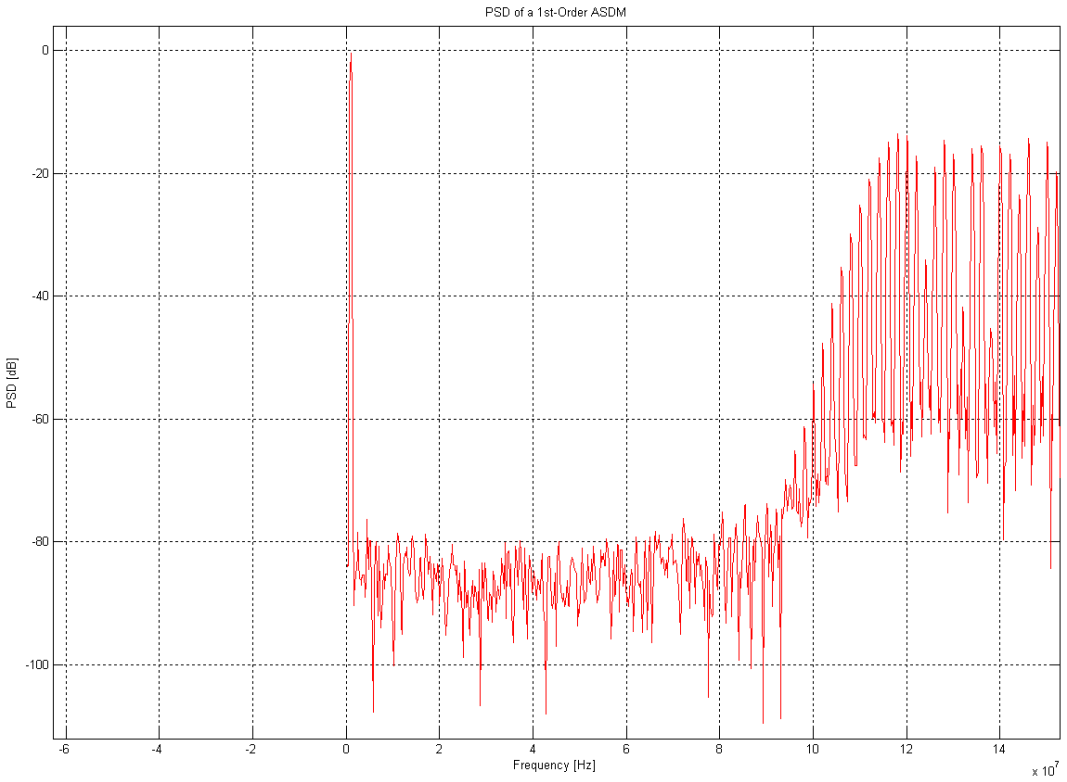


Figure 7.1. Spectrum of the circuit simulation first order modulator: % 80 modulation index for 1MHz sinusoidal test signal applied

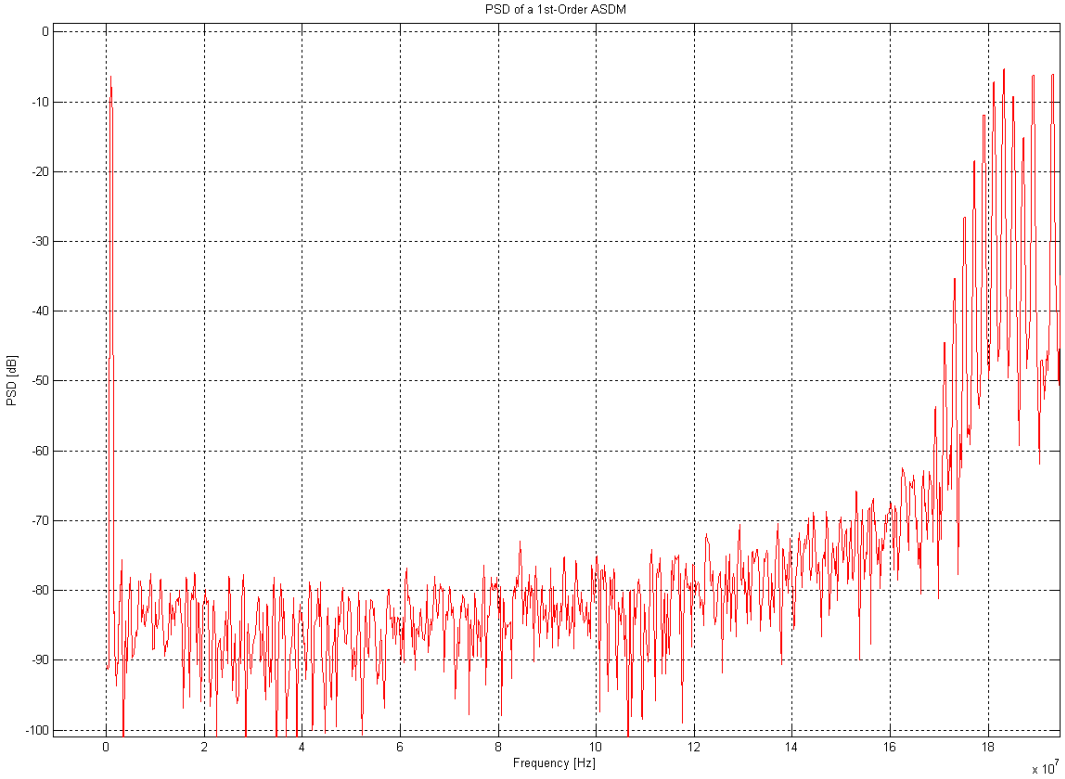


Figure 7.2. Simulation of the first order ASDM spectrum with modulation index of 0.3

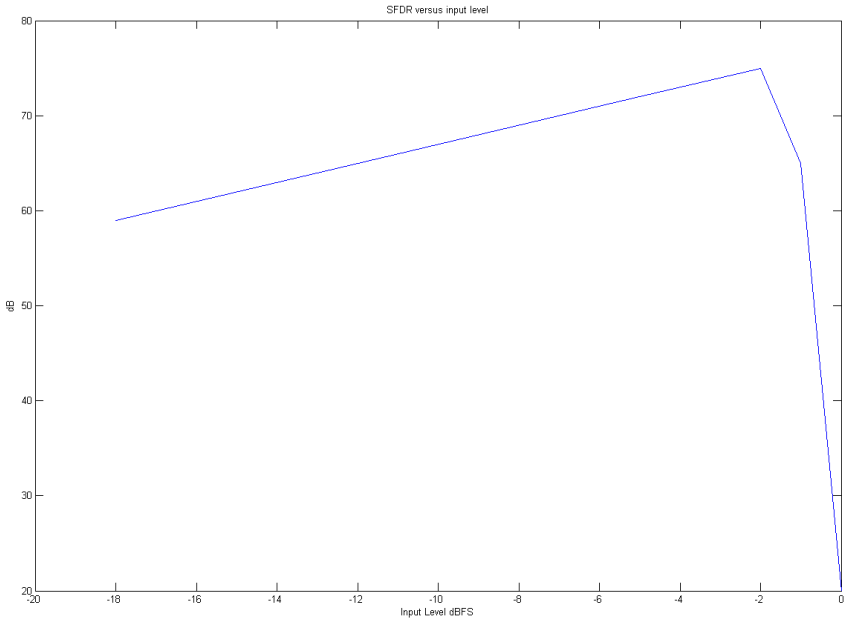


Figure 7.3. SFDR variation with the input signal amplitude

for modulation 0.5 and 0.8 is given.

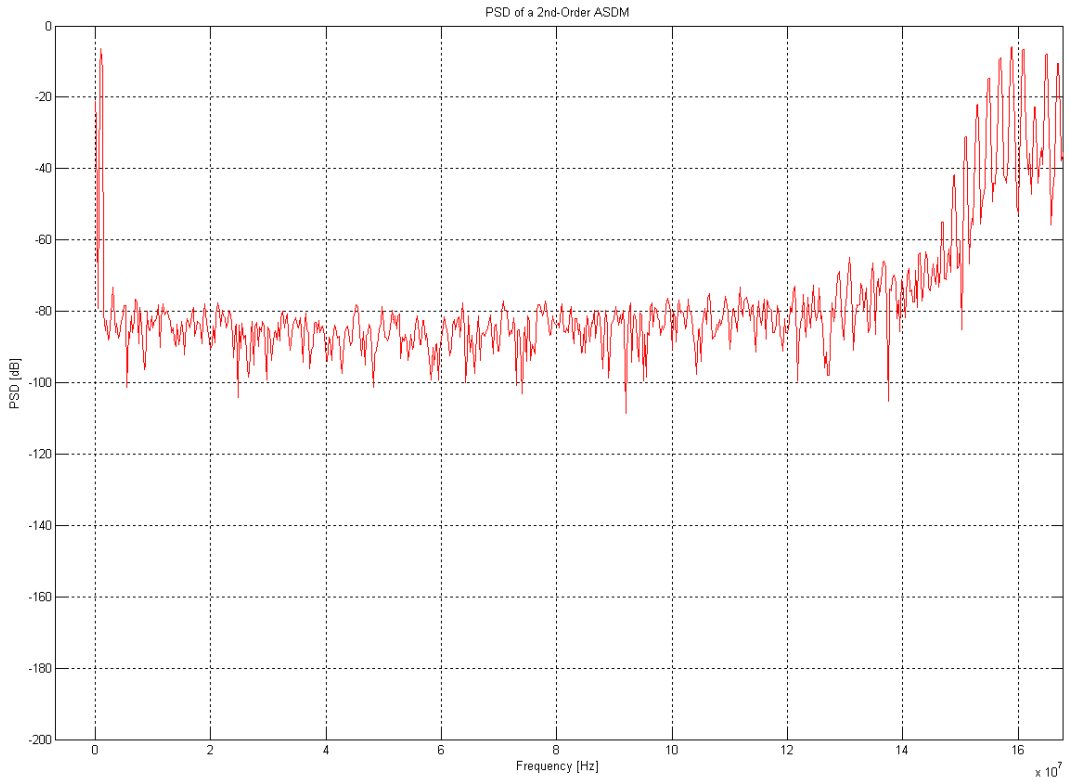


Figure 7.4. Simulated spectrum of the second order ASDM: 50% modulation depth and 1MHz sinusoidal input signal

The achieved maximum SNR is 75 dB while the bandwidth is about 15 MHz. For bigger modulation indexes for the second order modulator (e.g 50%), it is observed that they are filtered more compared to first order modulator and the spectrum is clearer compared to the first order implementation. Compared to [16], which is the only compatible known; implementation similar performance results have been achieved. In [16] prototype measurements are given. The mismatch in the prototype will degrade its performance by increasing the noise floor. That above mentioned implementation was implemented in 0.18 μm and operating at 1.8 V; whereas this prototype is in 0.35 μm, which have similar SFDR achievements. The speed is limited to 0.35 μm technology parameters. Limit cycle frequencies larger than 500 MHz can be achievable with smaller technologies, but this will give no performance improvement. After a certain amount of Bessel suppression the performance is determined by the linearity of the $\Sigma - \Delta$ loop. Since there will be always some nonlinearity of the components, there will be a SNR degradation compared to ideal models. As it will be explained in

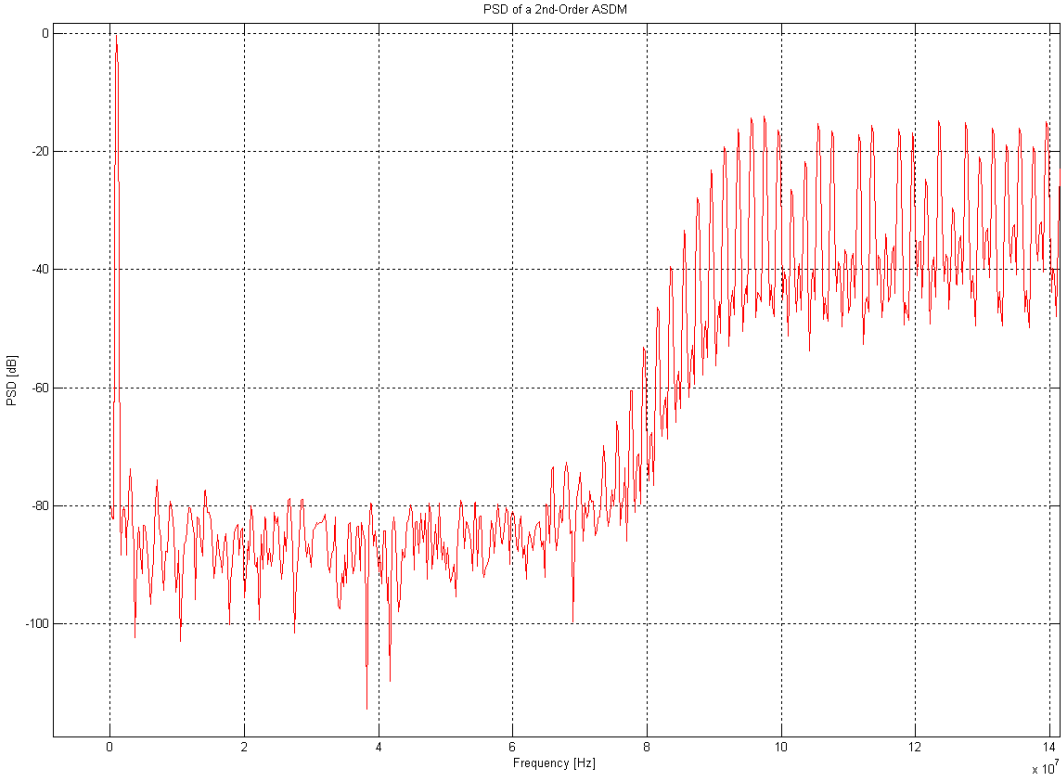


Figure 7.5. Simulated spectrum of the second order ASDM: % 80 modulation depth and 1MHz sinusoidal input signal

the following section, the limit-cycle frequency also determines the amount of bits that can resolved. A high limit cycle frequency requires either an increased high sampling rate or counting rate, depending on the method to be preferred to filter and decode the modulator output.

In this implementation, frequency is adjustable in a large range. In the second order implementation one less voltage to current converter is used compared to the other work that will bring some extra power and area savings. It can be seen from the layouts that building higher orders of feed-forward architectures are simple, but it should be known that some local feedback loops should be used for orders greater than two. The performance results of the prototype modulator is given in Table 7.2.

Table 7.1. Summary of simulated performance of the layout

0.35 μm, 3.3 V CMOS	First order ASDM	Second Order ASDM
Area	0.18 mm2	0.216 mm2
Maximum center frequency	180 MHz	180 MHz
SFDR [0 - 10MHz]	75dB	74dB
SNR [1k - 10 MHz]	70dB	70dB
Current consumption	1363 μA	1509 μA

Performance of the ASDM with the state of the art synchronous sigma delta modulators can be compared with Figure of Merit(FOM). The formula used to calculate modulator figure of merit is:

$$FOM = \frac{Power\ consumption}{2^{(ENOB)} * Bandwidth} \tag{7.1}$$

The number of bits (ENOB) is related to the SNR value as:

$$ENOB = \frac{(SNR - 1.76dB)}{6.02} \tag{7.2}$$

In Table 7.2 FOM comparison of different sigma delta modulators are given. As it can be seen, the other [16] is superior in FOM value due to its lower power consumption. The area value is coarsely 4 times because of the dimension difference of the transistor. If 0.18 μm technolgy had been used power will be at least half of the current value. One half ratio comes from the supply reduction, a further reduction may be attained because the current of the comparator can be cut by 4 because lower capacitances. This table also demonstrates the superiority of the ASDM among CT $\Sigma - \Delta$ modulators working at the above 100 MHz range.

Table 7.2. Summary of simulated layout performance

Reference	Wu[52]	Hong[53]	Whe[54]	Ouz[16]	This work
Area (mm^2)	1.25	1	0.7	0.04	0.18
Maximum operating frequency	160M	320 M	640M	140M	190M
Technology(μm)	0.25	0.18	0.18	0.18	0.35
SFDR [0 - 10MHz]	62dB	80dB	87 dB	75 dB	75dB
SNR [1k - 10 MHz]	62dB	80dB	87dB	70 dB	70dB
Power consumption(W)	8m	36m	100m	1.4m	4.5m
Bandwidth(Hz)	2M	10M	10M	8M	10M
FOM	1.94p	0.22p	0.273p	0.034p	0.1p

7.3. Filter Results

As it was outlined in the filter chapter, there are two methods to filter the signal of the $\Sigma - \Delta$ modulator output. The first method is to sample the PWM signal and count high and low periods based on a clock. The second method which was used in this dissertation is to count high and lows according to an analog delay and sample the signal after counting with a lower sample rate. Despite its advantage to relax the sampling frequency the resolution of this depends on the minimum countable duration. Since the duration is counted by the step of digital full adders delay. The minimum countable pulse is the full adder delay when delay element is minimized. In the technology used, the delay of the full adder is about 500 psec. Thus a 200 MHz signal which has 5nsec period of high and low can be resolved by 10 steps. It will be necessary to lower the limit cycle frequency to achieve more resolution. A 50 MHz limit cycle will lead to 40 step= 5.3 effective bits. However, at lower limit cycle frequencies the bandwidth of the modulator is low (about 5 MHz) and the SNR value is 60 dB. However, this SNR value is not useful since filter cannot resolve 10 bits. Output code versus input voltage can be seen in Fig. 7.6 for this configuration.

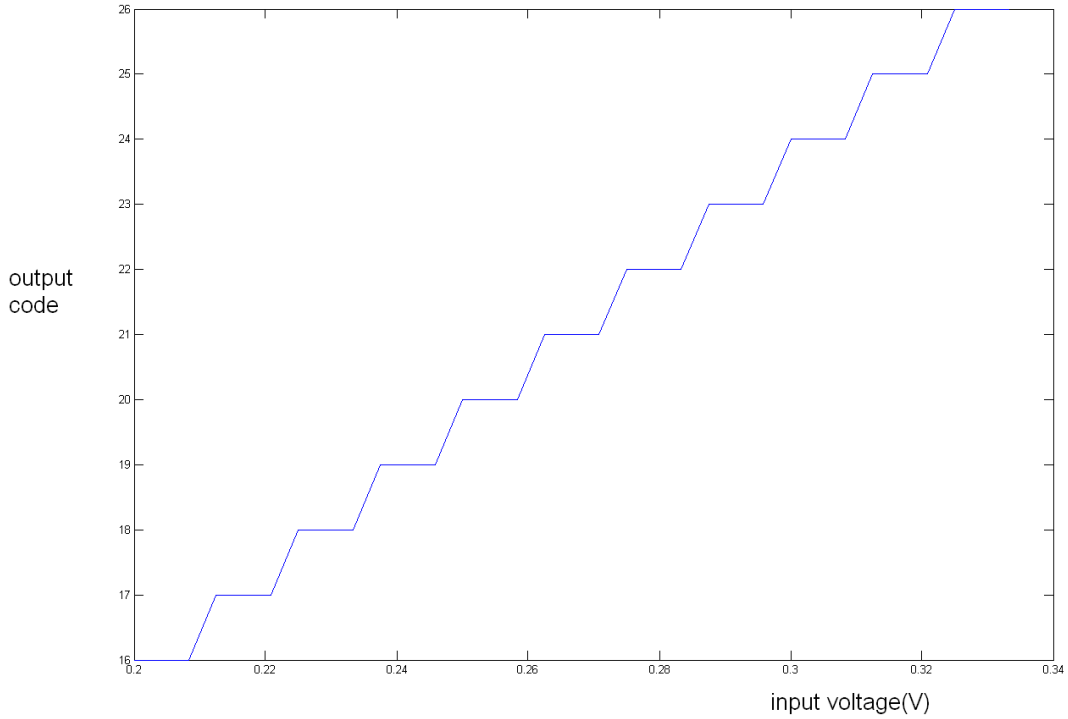


Figure 7.6. Simulated output code of the complete ADC

The figure of merit can be calculated for the complete ADC and a table with the state of the arts ADC's is provided in Table7.3.

Table 7.3. Summary of ADC FOM's

Reference	Kamran[55]	Choi[56]	Del Rio[57]	This work
Technology(μm)	0.18	0.35	0.35	0.35
Method	Subranging	Flash	$\Sigma - \Delta$	Asynchronous $\Sigma - \Delta$
Power consumption(W)	70m	500m	100m	24.5m
Bandwidth(Hz)	31.5M	630M	10M	10M
ENOB	7.8	6	14	5.3
FOM	5p	6.2p	3 p	63p

The SNR value at the output of the modulator is quite high for even first order implementation. But because of the low resolution that can be extracted from the filter,

the FOM value at the end of the filter is quite large compared to other topologies. With smaller size technologies this value can be cut down by a ratio of 4 that means number of bits can be increased by an amount of two bits.

8. CONCLUSION AND FUTURE WORK

In this thesis, possible aspects such as resolution, power, bandwidth of asynchronous sigma delta ADC's are investigated. This type of ADC requires more detailed mathematical analysis than synchronous ones. However, high SFDR is achievable even with first order modulators. In order to increase the performance, current mode implementation of the modulators which are not present up to this time is presented. To increase the selected topology's performance, a delay improved current comparator which can work at high speeds,is presented. The maximum operating frequency of the modulator and the available resolution of the ADC was shown to be only technology depended. Instead of the used 0.35μm technology, smaller technologies will increase limit cycle frequency further. But increase in limit cycle despite its assistance to achieve high SINAD values at the modulator output, will decrease the resolution since the minimum countable pulse rate in a given technology is constant. So, there is a trade-off between modulator SINAD and bits that can be resolved by the filter. An optimum operating frequency satisfying both requirements can be found. The advantages and disadvantages of this implementation given in this dissertation were presented. Up to this time, no asynchronous decimation filter for this type of modulators has been built. Therefore, achievable digital bits were questionable and this discouraged the use of asynchronous $\Sigma - \Delta$ ADC's. In this thesis these questions were answered. The results were given in the preceding section and related discussion has been done. A prototype of the layout has been implemented, but not measured yet. As a future work necessary measurements will be done on the fabricated prototype chip. As a future work, more performance improving circuit topologies will be investigated which can lead to build higher SNR modulators. There are possibilities to make improvements in the filter section in the future.

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