10-BIT 60 MS/s TWO-STEP FLASH ADC DESIGN

by

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ABSTRACT

10-BIT 60 MS/s TWO-STEP FLASH ADC DESIGN

Two step flash ADCs have widespread use in electronic circuits, since they can achieve decent resolutions in high speed applications. Their two step structure requires coordination of many analog blocks that is ensured by control signals. Generating and delivering these control signals as clock signals are as important as the design of the analog blocks. In this thesis analog design of a two-step flash ADC which is used as a test circuit for an automation tool that can synthesize the necessary clock signals is presented. The design procedures of the blocks in 10-bit 60 MS/s two step flash ADC are examined. The overall design is realized by using UMC 180nm technology. Finally the simulation results obtained by using Mentor Graphics tools and MATLAB are presented. The performance of the ADC is evaluated using ENOB as a figure of merit. Resolutions up to eight bits are attained in typical case simulations. Comparison with the literature is also made by using energy per conversion values.

ÖZET

10-Bit 60 MS/s İKİ BASAMAKLI FLASH ADC TASARIMI

İki basamaklı flaş ADC'ler makul bit sayılarında yüksek hızlara ulaşabildiklerinden, yüksek hızlar istenildiğinde yaygın olarak kullanılmaktadır. İki basamaklı yapıları bir çok analog blokun uyumlu çalışmasını gerektirmektedir. Bu da kontrol sinyallerine ihtiyaç duyulmasına sebep olur. Bu kontrol sinyallerinin, saat sinyalleri olarak üretilmesi ve dağıtılması da devrenin analog bloklarının tasarımı kadar önemli bir problemdir. Bu tezde bahsedilen saat sinyallerinin otomatik olarak sentezlenmesini sağlayacak bir araç üretilmesine imkan vermek için iki basamaklı bir flaş ADC, test devresi olarak tasarlanmıştır. Test devresi olarak kullanılacak 10-bit 60 MS/s iki basamaklı flaş ADC'de kullanılan analog blokların tasarımları detaylı olarak incelenmiştir. Tüm devre tasarımı UMC 180nm teknolojisi kullanılarak gerçekleştirilmiştir. Sonuç olarak, Mentor Graphics ve MATLAB kulanılarak elde edilen benzetim sonuçları incelenmiştir. Tasarlanan ADC'nin performansı ENOB kullanılarak değerlendirilmiştir ve sekiz bite kadar ulaşan çözünürlük değerleri elde edilmiştir. Çevirme başına düşen enerji değerleri kullanılarak literatürdeki diğer iki basamaklı ADC'lerle bir karşılaştırma yapılmıştır.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

g_m	Transconductance
V_T	Threshold voltage
V_{gs}	Gate to source voltage
W	Channel Width
L	Channel Length

LIST OF ACRONYMS/ABBREVIATIONS

A/D	Analog to Digital
ADC	Analog to Digital Converter
CM	Common Mode
CMFB	Common Mode Feedback
CS	Current Steering
D/A	Digital to Analog
DAC	Digital to Analog Converter
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
MS/s	Mega Sample per second
NMOS	Negative-Channel Metal Oxide Semiconductor
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
PMOS	Positive-Channel Metal Oxide Semiconductor
S&H	Sample and Hold
SNR	Signal to Noise Ratio

1. INTRODUCTION

Analog to digital converters (ADC) are widely used in almost all electronic systems recently. The reason behind their widespread use is that digital signals are simpler to process and transmit. Although digital data processors and transceivers are readily available, signals that are dealt with are usually analog. Therefore, majority of electronic systems employ ADCs as front end circuitry.

There are many different ways to convert an analog signal to digital code, according to overall system requirements. However, it is possible to classify them into two main categories such as Nyquist rate and oversampling ADC's. Nyquist rate ADCs are high speed but low accuracy converters, whereas oversampling counterparts are high accuracy but low speed converters. Beside this accuracy-speed trade off based classification, there are also subcategories of each group depending on the methodology of conversion. These subcategories are shown in Figure 1.1 with speed vs. accuracy trade off.

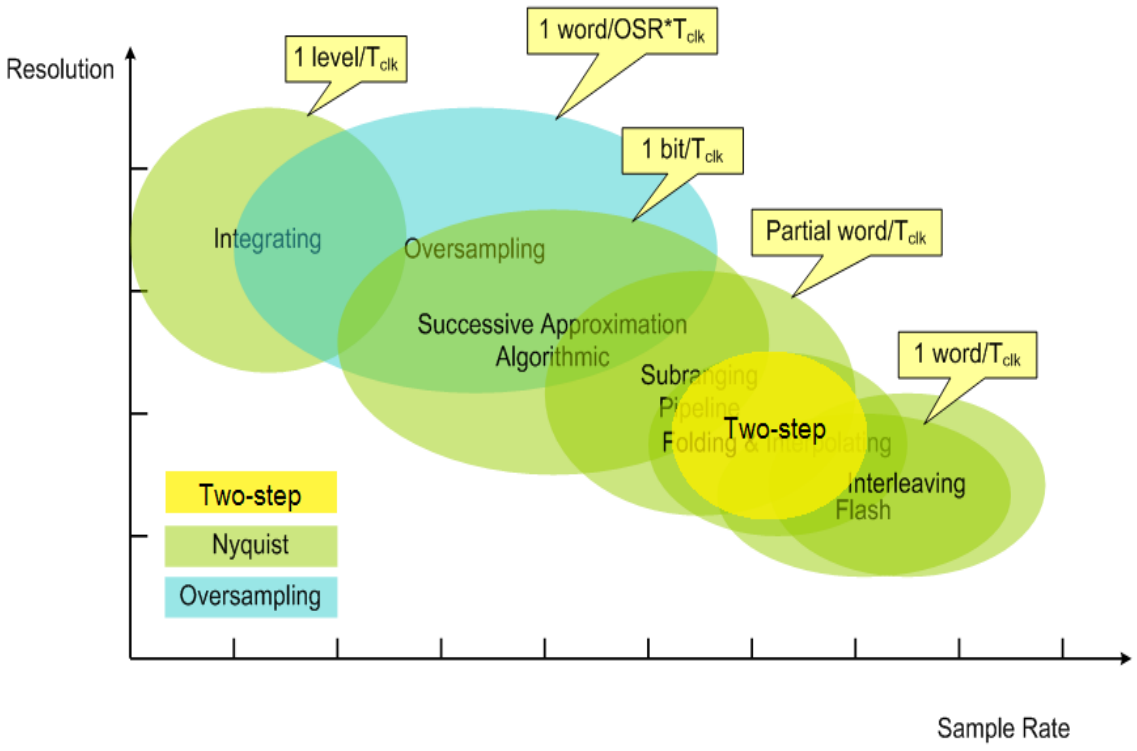


Figure 1.1. Accuracy-speed trade off graph for ADCs [1].

1.1. Flash Converters

Flash converters are the best candidates for high speed data conversion as shown in Figure 1.1. The analog input signal is compared with all 2^{N-1} threshold levels in a parallel manner, where N is the number of bits of the converter. This simple process is accomplished with 2^{N-1} comparators that use same number of threshold voltages generated by a resistor string. All these comparators give a set of N bit logical codes, so called thermometer code, which is converted to binary digital code by a simple decoder.

Figure 1.2 is an example of four bit flash converter. There are 15 comparators and 15 threshold references as shown. Simple Kelvin divider is used to create equally separated reference voltages for comparators [2].

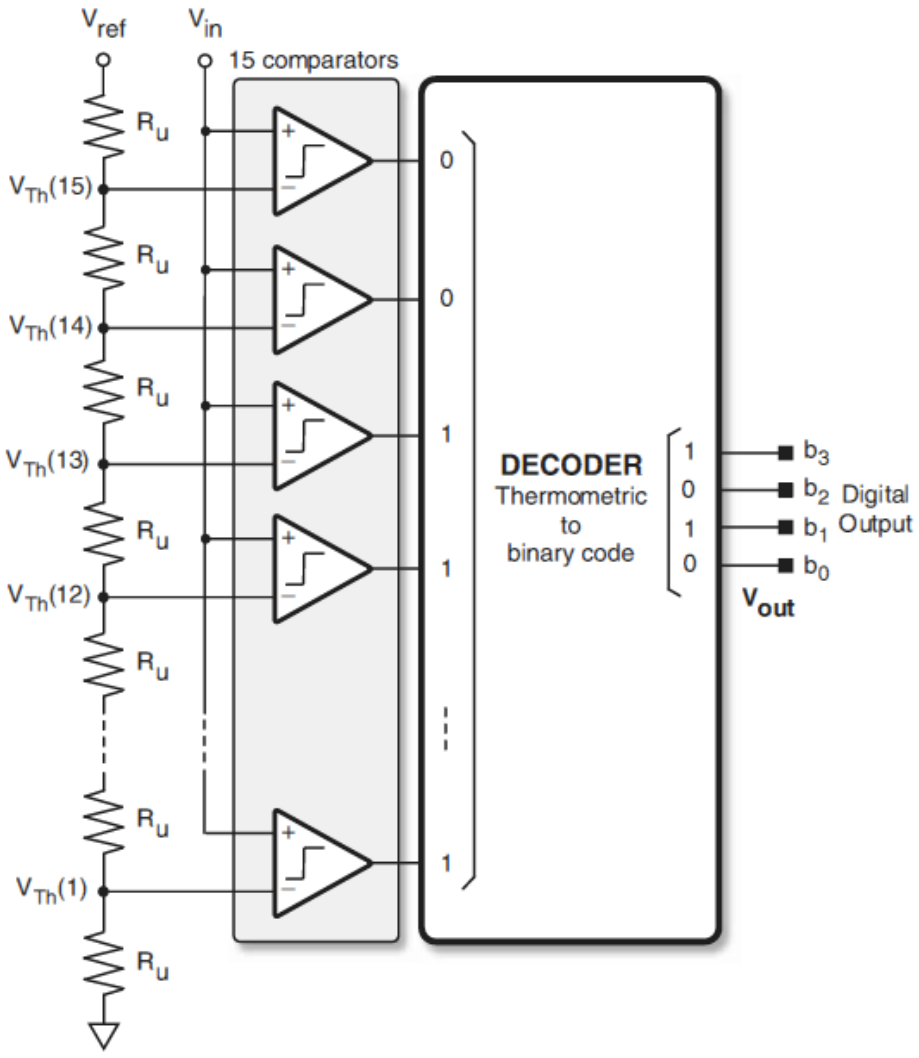


Figure 1.2. Block diagram of a 4-bit flash converter [2].

Flash converters exploit parallel operation of high speed comparators in order to obtain high speed conversion. However, they are not suitable for high accuracy since the number of comparators increases exponentially with the number of bits. They cannot exceed six or seven bits of resolution mainly because of area and power considerations. Two-step flash ADC's are commonly used to obtain higher resolutions at the expense of slightly lower speed, using more or less same procedure.

1.2. Two-Step Flash Converters

Two-step flash converters relieve the area and power requirements of simple flash converters while approaching their speed values at the expense of increased complexity and necessary control signals.

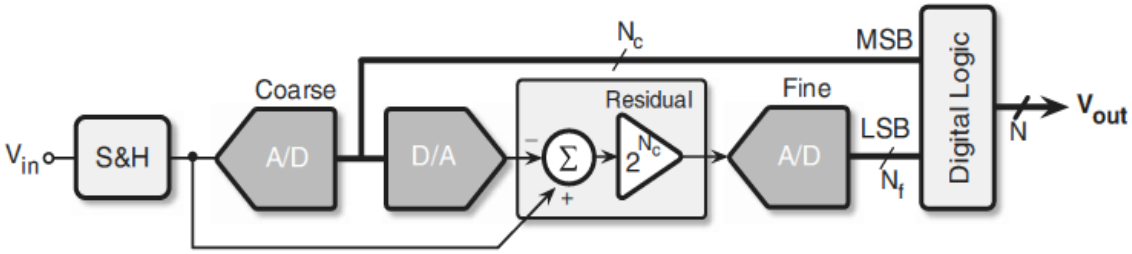


Figure 1.3. Block diagram of a two-step flash converter [2].

Two simple flash converters are used to have higher resolution in two-step flash converters as seen in the Figure 1.3. These converters are usually called coarse and fine converters. Sample and hold block at the front end of the architecture assures the same input signal for both converters. Digital to analog converter regenerates the analog signal converted by the coarse converter. This regenerated analog signal is subtracted from the sampled signal to create the input of the fine converter which is called residual. The residue signal is commonly amplified to ease the requirements of fine converter. Finally, a digital decoder forms the binary digital code at the end of the system. Resolution, N, of a two-step converter becomes:

$$N = N_c + N_f \tag{1.1}$$

where N_c is the number of bits of the coarse converter, and N_f is the number of bits of the fine converter.

In this thesis, 10 bit 60 MS/s two-step flash converter which is insensitive to process variations is designed as a test circuit for an analog clock tree synthesis tool. In Figure 1.4, block diagram of designed ADC is shown. The designed architecture can be called as pipeline two step flash converter where “pipeline” implies both converters work at the same time.

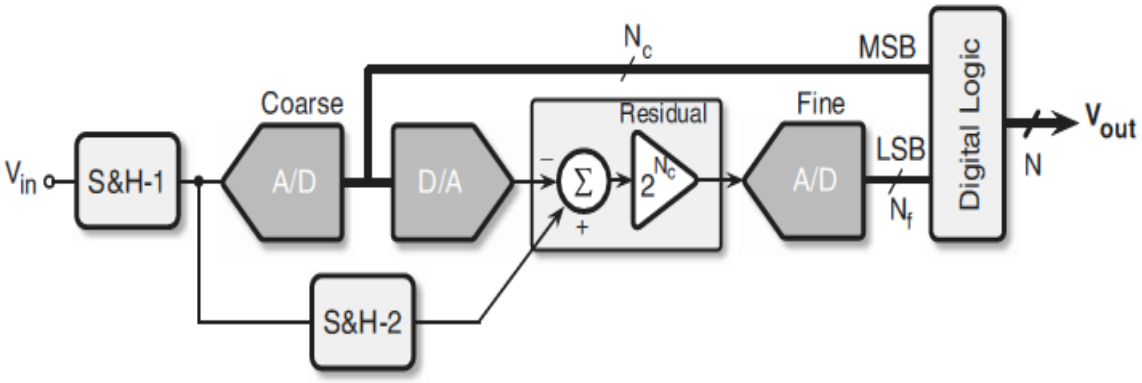


Figure 1.4. Block diagram of designed pipeline two-step flash converter [2].

Pipelined and two-step converter designs in the literature are examined in order to study specific techniques used in ADC design. A Two-channel architecture using one multiplying DAC for each channel is reported in [3]. This architecture has 6 bit resolution at very high speed. Two identical fine converters are also employed in this architecture for two-channel operation. However, the total power consumption of the ADC is kept relatively low, since two-channel operation relieves the speed requirements of the blocks employed in each channel. Digital error correction is also utilized to compensate errors coming from coarse conversion. In order to have overall resolution of six bits, 3-bit coarse converter and 4-bit fine converters are used. One extra bit generated in the fine conversion is used for error correction.

Subranging is a common methodology used in pipelined ADC design. A 12-bit 100 MS/s pipelined ADC design is realized in [4] exploiting some useful techniques besides subranging. First of all, multiple residue amplifiers are employed to decrease the input range of each amplifier. This way, linearity requirement of the residue generation is relieved. Reference level generations for comparators are also optimized. Residues are used to generate the reference voltage levels for the next stage. These reference levels are generated in a redundant manner for digital error correction circuit.

Two fine converters are used for fine conversion in [5]. These two sub-converters are operated in ping pong mode. One sub-converter is used to process one sampled data, while the other sub-converter is used for the next sampled data. This way, comparison time for each fine comparator is doubled. Again, 1-bit redundancy is employed in the fine converters to correct possible errors. Besides, bootstrapped switches are utilized in S&H circuit in order to reduce errors originated from switching.

Three, time interleaved S&H units are used to relieve the speed requirement of this very important block in [6]. Operational amplifiers are used in almost all sample and hold circuits. High speed operation of these circuits demands very high speed operational amplifiers which are very challenging to design using robust architectures. Therefore, using time interleaved S&H units is a very advantageous way to obtain high sampling rates. Reference levels used for coarse conversion are selected by switch units instead of a traditional DAC to decrease power consumption. Finally, a digital error correction circuit exploiting redundancy is used.

Multiple pre-amplifier arrays before the converter blocks are employed in [7]. In order to select the output of the proper pre-amplifier array multiplexers are used. This methodology eliminates the DAC and residue generator; therefore it decreases the power consumption of overall ADC. Besides, the high speed operation of multiplexers in comparison to DAC and residue generators makes high sampling rates possible.

The design of analog blocks shown in Figure 1.4 is introduced in the next chapter. Third chapter will demonstrate the simulation results of the system with the synthesized clocks. Comparison between the designed ADC and examined ADCs from the literature is also presented in third chapter. Finally, the last chapter summarizes the thesis.

2. DESIGN OF ANALOG BLOCKS

In this chapter, the design of each block represented in Figure 1.4 is examined. The speed and accuracy requirements of the blocks can be calculated through the performance of overall ADC like the followings:

$$Resolution = \frac{Input\ voltage\ range}{2^{\#\ of\ \ bits+1}} \cong 0.44\ mV \tag{2.1}$$

$$Conversion\ time\ \leq \frac{1}{Sampling\ frequency} \leq 16.6\ ns \tag{2.2}$$

It must be taken into account that conversion time is shared by all blocks in each step. The amount of time allocated for each block is decided by the clock tree automation tool according to necessary requirements of the main architecture.

2.1. Sample and Hold

Sample and Hold is the front-end block of the whole ADC where analog input signal is received. Time required to process the analog input by other blocks is provided by this block. In other words, sample and hold captures the value of the analog signal and keeps this value same for all the other blocks to work. Indeed, this sampling and holding time determines the frequency of operation. Besides, its precision limits the resolution of the ADC since errors coming from sample and hold block change the value to be converted and deteriorate all other blocks.

Two different topologies are designed for the different needs of two sample and hold blocks shown in Figure 1.4.

2.1.1. First Sample and Hold Block

The basic architecture designed for first sample and hold block is demonstrated in Figure 2.1. This is a well-known architecture and commonly known as flip-around sample and hold.

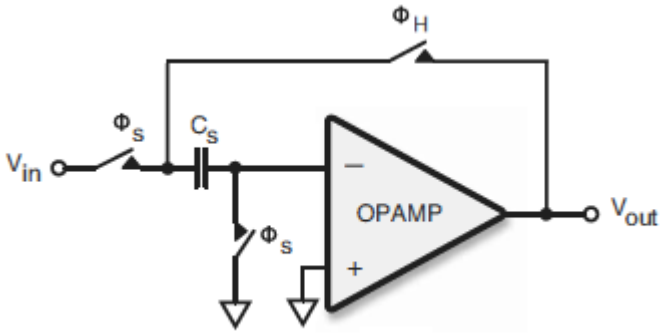


Figure 2.1. Flip-around sample and hold architecture [2].

Input signal is captured on sampling capacitor with two switches as seen in Figure 2.1. Then, the sampled signal is connected to the output of the circuit via another switch. Advantages of this architecture can be listed as robustness and simplicity. However, simulation results showed that this simple architecture is not good at dealing with the common switching problems such as clock feedthrough and charge injection [8]. Errors coming from these switching problems are eliminated by some useful techniques.

First of all, fully differential architecture is adopted. Therefore two sampling capacitors and a fully differential amplifier are used in contrast to Figure 2.1. Although this increased the complexity and area/power requirements of all blocks in ADC, fully differential signal processing also increases the noise suppressing performance of ADC.

Another method used to eliminate switching problems is bottom plate sampling [9]. Figure 2.2 demonstrates modified switching schema for bottom plate sampling. Only one branch of fully differential system is shown for simplicity and integrity.

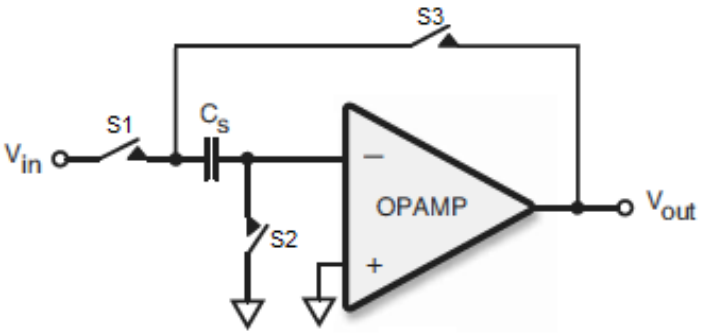


Figure 2.2. Flip-around sample and hold architecture with bottom plate sampling.

The first sampling switch S1 in Figure 2.2 is opened slightly later compared to S2 which is the other sampling switch. This way no charge is injected, since the bottom plate of the sampling capacitor is already open when input switch (S1) is opened. Besides, charge injected from S2 is constant, i.e. independent of input signal, and canceled through differential architecture. S3 switch must not be closed at same time with other two switches, therefore it requires non-overlapping clock phases. The only drawback of bottom plate sampling is the need of one more clock phase; nevertheless, all the required clock phases are generated with an automation tool.

Last, dummy switches which are always short circuited are added to all nodes for every switch [10]. The opposite of control signals applied to real switches are applied to dummy switches to cancel charge injected from the former. These dummy switches are designed to have the size which is half of real switches in order to maximize the cancellation of undesired signals. Figure 2.3 demonstrates the use of dummy switches.

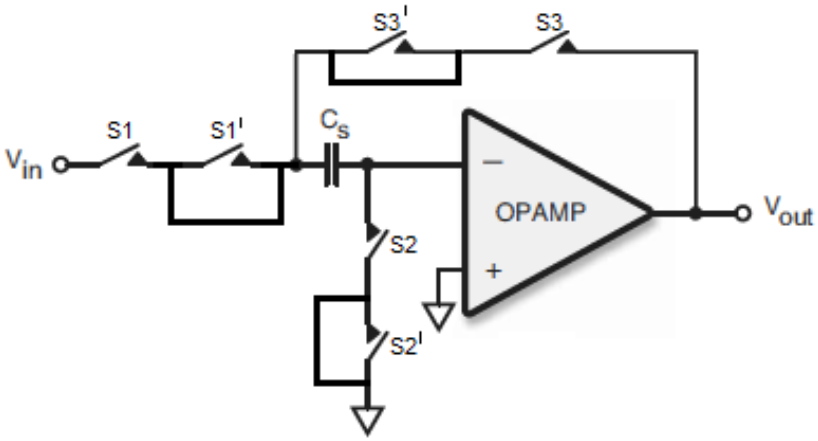


Figure 2.3. Flip-around sample and hold architecture with bottom plate sampling and dummy switches.

All switches are designed as transmission gates. PMOS and NMOS transistors in transmission gates have equal size for each switch in order to minimize the charge injection by canceling the charges coming from complementary clock signals [10].

Instead of an OPAMP as shown in Figure 2.2 a fully differential OTA is used, since it is convenient to use an OTA with a capacitive load which is the case for the sample and hold block.

2.1.1.1. OTA Design. A fully differential folded cascode OTA design is used in sample and hold block. The folded cascode OTA is a commonly used architecture for its robustness and high intrinsic gain which makes it a good candidate for closed loop systems. In this thesis, techniques used to make this OTA insensitive to process variations will be examined.

The designed ADC must operate decently in both corner cases namely slow and fast as mentioned before. Therefore, all analog blocks are designed to have proper operation in these process corners.

First of all, gain and phase margin values are optimized to work in all three operating points such as typical, fast and slow through basic equations of folded cascode OTA. The designed folded cascode OTA has gain and phase margin values to ensure proper operation in both corner cases as shown in Figure 2.4. There is a trade-off between slow corner phase margin and fast corner gain here. Increasing the DC gain of OTA would result in unstable operation for slow corner, whereas decreasing it deteriorates the closed loop operation for fast corner.

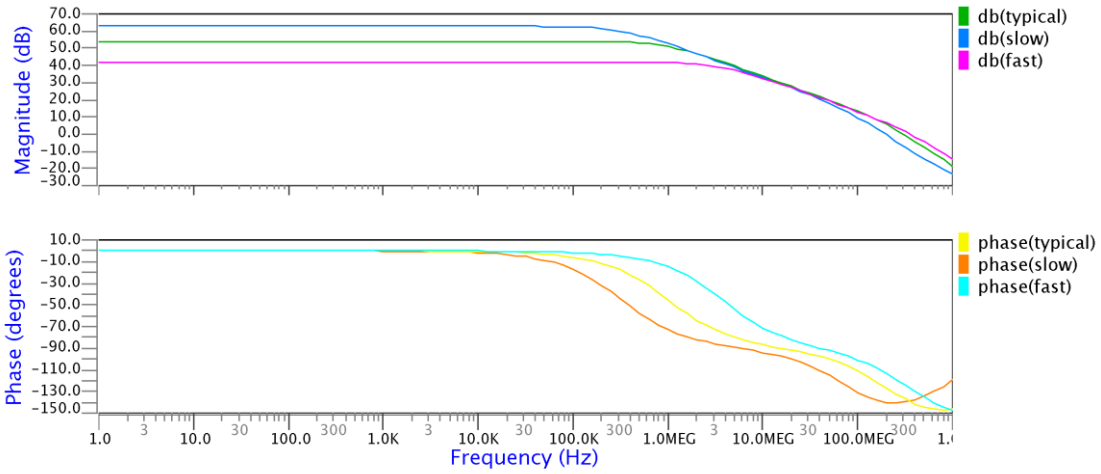


Figure 2.4. AC simulation results of the designed OTA for all corner cases.

Process variations do not only change AC characteristics of the folded cascode OTA, but also change the DC operating point dramatically, especially the output common mode. Therefore, a common mode feedback (CMFB) circuitry is needed for folded

cascode OTA like all other fully differential amplifiers. The architecture shown in Figure 2.5 is used to detect the common mode output voltage and generate a feedback signal for OTA [11]. Two equal resistors used to detect the common mode have large enough values in order not to load the output of the OTA. The gain of the CM Sense amplifier is kept around five to ten which ensures enough strength for common mode feedback. Another important point is that the overall common mode feedback must be negative to work as intended.

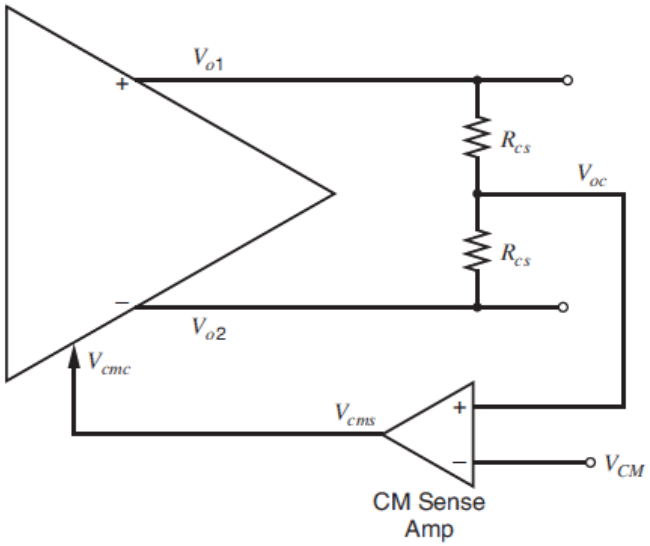


Figure 2.5. Common mode feedback (CMFB) circuitry [11].

The circuit shown in Figure 2.6 is used as common mode sense amplifier. Its performance is independent of corner case characteristics of transistors. Two stage cascaded architecture is used in order to have enough gain, and negative feedback.

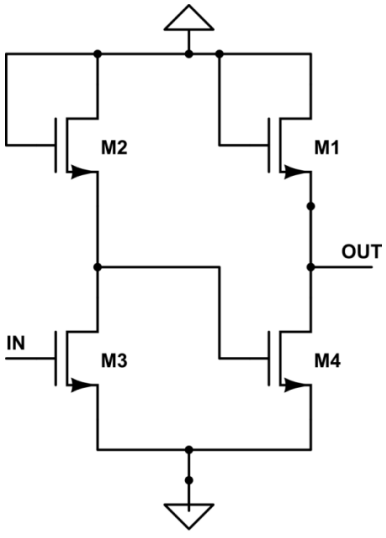


Figure 2.6. Common mode sense amplifier circuit.

The total gain of common mode sense amplifier can be calculated as the product of each stage gain like the following:

$$A_v = \frac{g_{m3}}{g_{m2}} x \frac{g_{m4}}{g_{m1}} \tag{2.3}$$

Figure 2.7 shows output response of common mode sense amplifier while the output common mode of OTA is swept for all three operating points.

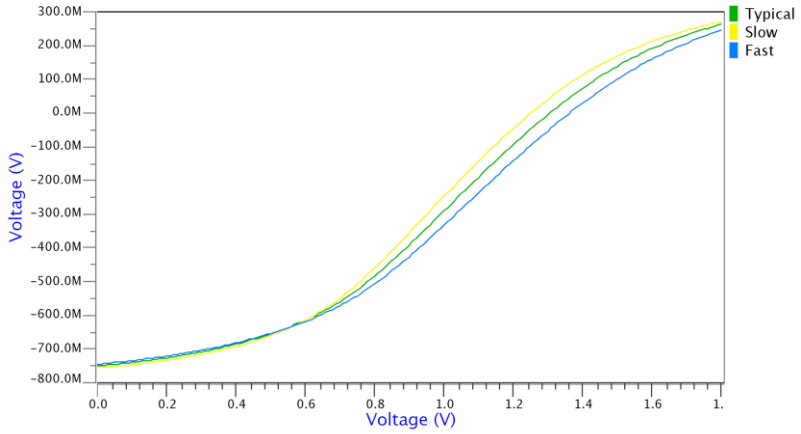


Figure 2.7. Output response of common mode sense amplifier.

Finally, transient simulation result for sample and hold circuit is shown in Figure 2.8, yet overall performance of sample and hold block is evaluated by SNR value. SNR values between 60 dB and 70 dB are achieved which ensure proper operation for 10 bit ADC. Figure 2.9 shows FFT results that are used to calculate these SNR values.

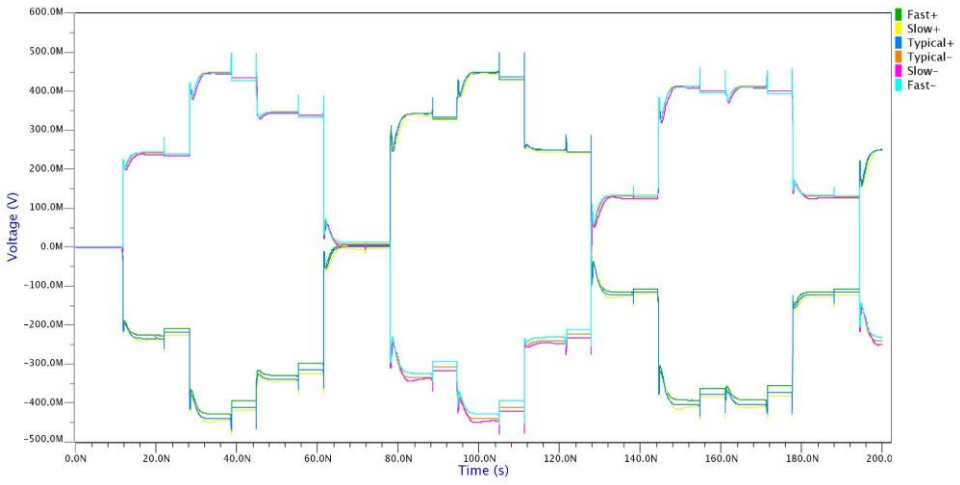


Figure 2.8. Transient simulation of sample and hold circuit.

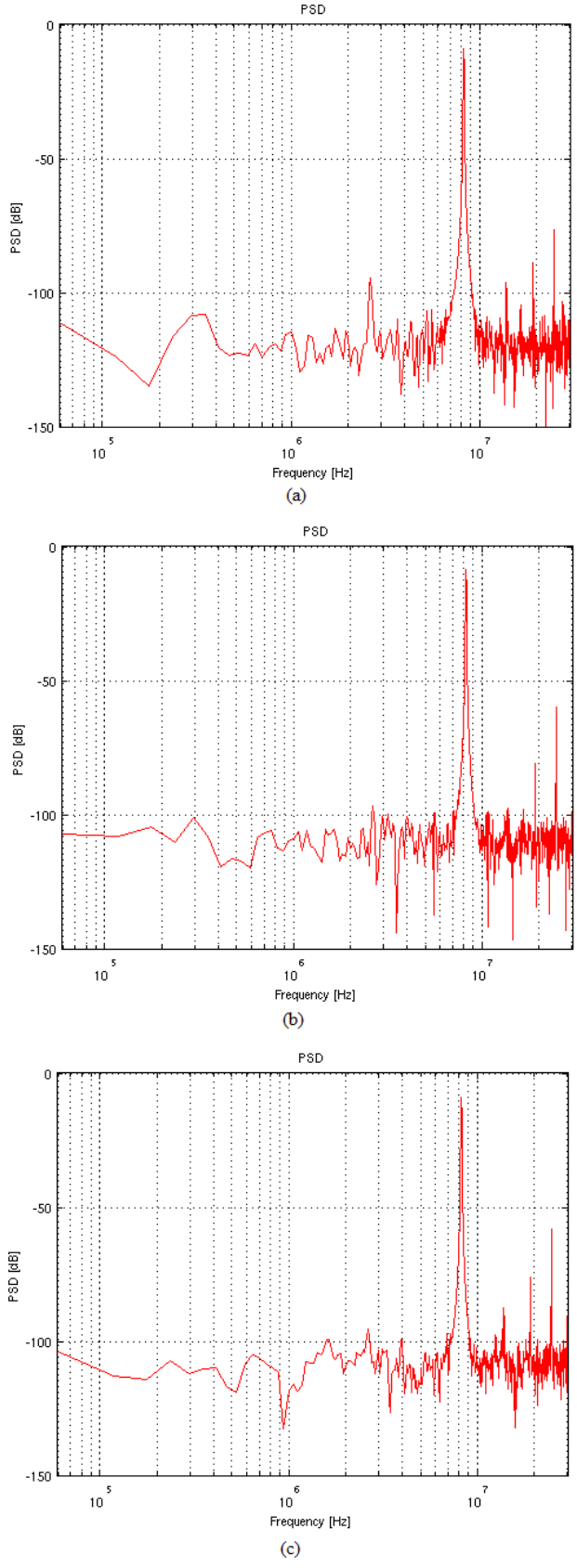


Figure 2.9. FFT results of sample and hold circuit for (a) typical, (b) slow, (c) fast.

2.1.2. Second Sample and Hold Block

Second sample and hold block is needed to enable pipelined operation which means concurrent operation of two converter blocks. This block holds analog signal value for the fine converter while the first sample and hold captures next analog value to be processed by the coarse converter. In the absence of second sample and hold block, converters would have to wait each other to process a new sample.

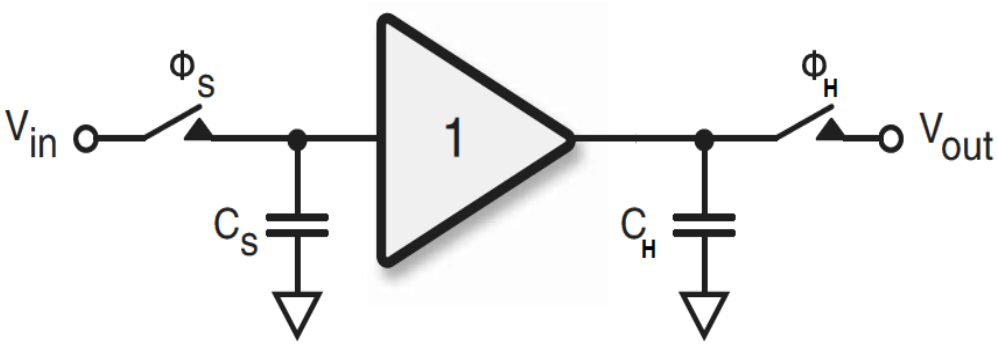


Figure 2.10. Second sample and hold block architecture.

In Figure 2.10, the architecture which is used as the second sample and hold block is presented. Only one branch of fully differential architecture is demonstrated again for simplicity. The architecture is very simple and robust. Its proper operation relies on the closed loop performance of the buffer circuit and non-overlapping control signals applied to input and output switches.

Two identical blocks are used in a manner called ping pong, which means only the output of one block is used at once. While the output of one block is used by the residue generator, the other one captures the next sampled voltage value. This operation makes the pipelined operation of two-step conversion possible.

Fully differential folded cascode OTA which is presented in the previous section is used with feedback as the buffer circuit shown in Figure 2.7. Simulation results of second S&H block is demonstrated in Figure 2.11.

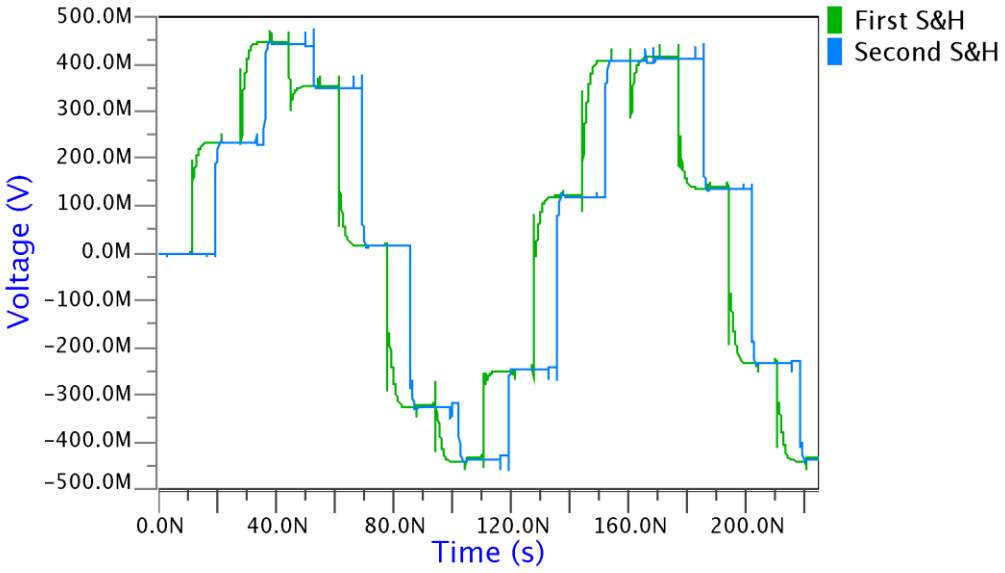


Figure 2.11. Transient simulation results for second sample and hold block.

2.2. 5-bit A/D Converter

Two step flash converters usually employ two different simple A/D converter block namely coarse and fine converters. This way, area and power requirements of the first conversion step are kept less challenging thanks to error correction circuitry. Redundant bits included in the fine conversion are used to correct the faults of the coarse conversion. However, in our design, two identical five bit converters are employed in order not to use an error correction circuit, which can suppress errors also stemming from clocking defects. The converters are still called coarse and fine converters for consistency with literature.

The designed five bit converter which is used as both coarse and fine A/D shown in Figure 1.4 works according to the principle explained in Section 1.1. It consists of 31 reference levels and 31 corresponding comparators. Reference voltage generation is rather straightforward, since they are generated by a Kelvin divider including 32 equal resistors. The value of resistors is carefully chosen according to matching, power consumption and kick-back noise which will be explained in detail [12]. Matching of these resistors strongly affects the overall static performance the ADC; therefore, trade-off between matching and insensitivity to kick-back noise determines the value of these resistors.

The performance of each comparator simply decides the performance of the five bit converter in terms of speed and accuracy, since there is not much flexibility for the choice of resistor values.

2.2.1. Comparator Design

Comparators decide whether the captured analog input (by sample and hold block or calculated by residue generation) is above each reference level or not. This way, 31 bit thermometer code is generated to constitute the binary code.

There are two possible architectures which can be used as comparators in flash converters; namely voltage amplifiers and regenerative positive feedback architectures. These architectures are examined in the next two sections.

2.2.1.1. Voltage Amplifiers. Comparators can also be modeled as very high gain voltage amplifiers; therefore, usual voltage gain architectures are also used as comparators. The resolution of this type of comparators can be increased by increasing static gain using well-known methods like cascoding. Resolutions below 1mV can be achieved by 60-70dB static gain, since they are reversely proportional as in the equation below:

$$Static\ resolution = \frac{Input\ voltage\ range}{Static\ gain} \tag{2.4}$$

Input voltage range in the equation is the difference between the voltage levels that digital circuitry following the comparators can accept as logic high and low. Although simple voltage gain architectures can achieve required static gain values, dynamic gain is the actual parameter which determines the trade-off between speed and resolution for this type of comparators [13]. Figure 2.12 shows the relationship that is derived for voltage gain architectures using their small signal equations.

The resolution values calculated in previous section cannot be achieved within the target conversion time by these architectures as seen in Figure 2.12.

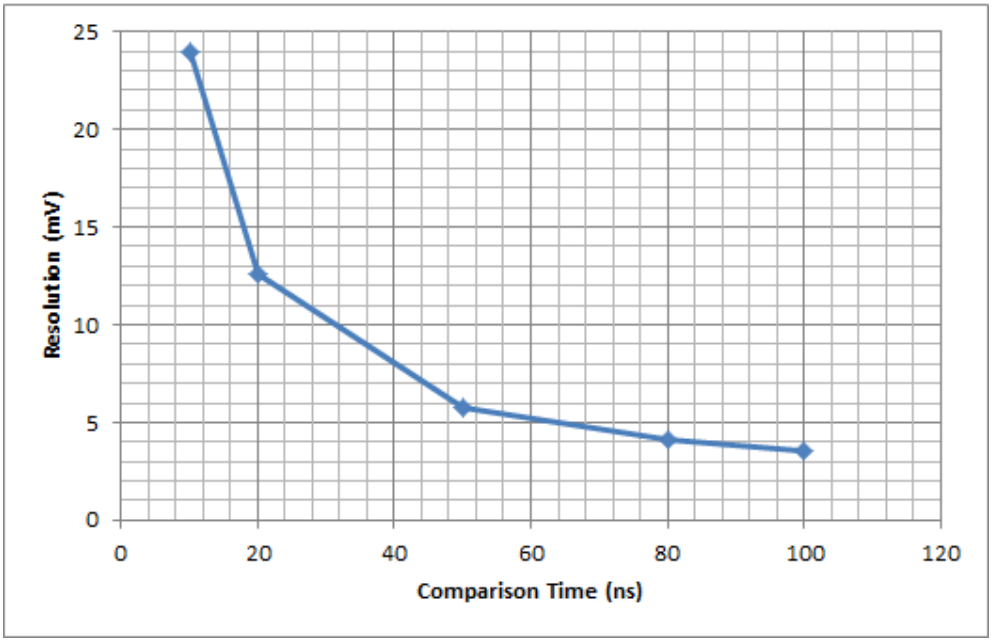


Figure 2.12. Relationship between conversion time and resolution for voltage gain comparators.

2.2.1.2. Regenerative Positive Feedback Comparators. Voltage amplifiers are usually designed to have linear and stable operation, however comparators do not have to be stable or linear. Therefore positive feedback can be exploited to obtain very high gain architectures so that resolution is not limited by dynamic gain. Eliminating the dynamic gain limitations, offset resulting from transistor mismatches is a more important limitation for regenerative comparators. Transistor mismatches can be defined as the differences originating from process variations between identically designed transistors. These differences can be modeled through the following relationship:

$$\sigma^2(\Delta V_{TO}) \approx \frac{\alpha^2 V_{TO}}{WxL} \tag{2.5}$$

$$\sigma^2\left(\frac{\Delta\beta_0}{\beta_0}\right) \approx \frac{\alpha^2 \beta_0}{WxL} \tag{2.6}$$

Including these equations, the relationship between comparison time and resolution is derived for regenerative comparators. Same power consumption with voltage gain architectures is assumed and only the effects of the mismatch of input pairs are included in the derivations for the sake of simplicity and generality. This type of comparators is proper candidates for our requirements as seen in Figure 2.13.

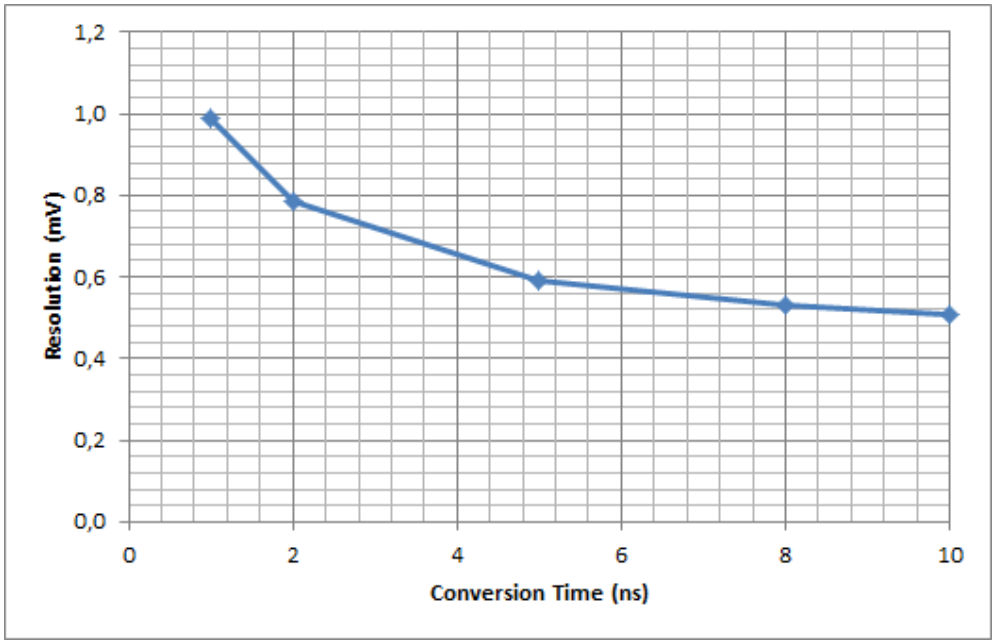


Figure 2.13. Relationship between conversion time and resolution for regenerative comparators.

Regenerative comparators necessitate clock signals to reset the output value. In the absence of the reset mechanism, very large hysteresis would occur and only large enough values could change the output state of the comparator once it decides [13]. In the reset phase two output nodes are usually brought to same level in order to make another conversion possible without hysteresis.

Cross-coupled transistors are used quite often to create positive feedback in regenerative comparators. Figure 2.14 shows the transistor level design of the core of the comparator employing cross-coupled transistors.

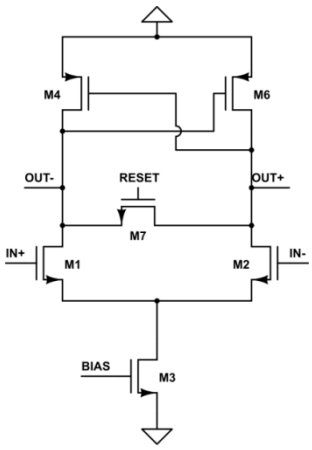


Figure 2.14. Core of the comparator.

In this simple architecture, the most important problem is the kick-back noise [14]. Kick-back noise can be defined as large glitches occurring at the input of comparator when the clock goes from high to low or vice versa. These glitches, which are shown in Figure 2.15, deteriorate especially reference voltages used in flash converters, and cause comparators to make wrong decisions. In our design, charge created by the instant change of both output voltage and the clock signal leaks to the input through the parasitic capacitances of input and reset transistors. Reducing the size of the transistors can lessen the effect of kick-back noise; however, matching requirements of these transistors contradicts this solution.

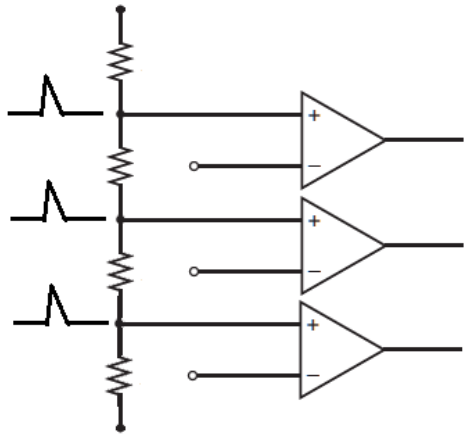


Figure 2.15. Glitches caused by kick-back noise.

The use of pre-amplifier stages is the most common way to decrease the effect of kick-back noise [9]. Differential pairs with simple architectures and low gain are used as pre-amplifiers to isolate the inputs of the comparators from the effects of resetting. In our case a pre-amplifier which can receive four inputs is needed since the fully differential architecture is adopted. The speed of the pre-amplifier should be higher than the speed of the comparator in order not to make settling errors which can affect the decision. Figure 2.16 shows the overall comparator design including four input preamplifier.

Transient simulation result of the designed comparator is presented in Figure 2.17, to review its speed and resolution. Small glitches seen in this figure originate from kick-back noise; nevertheless they are small enough for proper operation of comparator. In this simulation inputs are modeled with ideal voltage sources with 1kΩ series resistors in order to see the effect of kick-back noise.

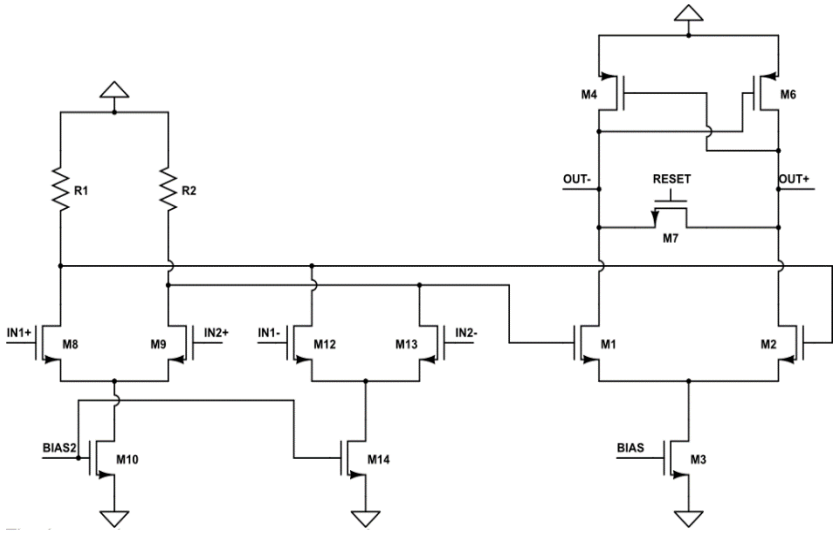


Figure 2.16. Regenerative comparator with four input pre-amplifier

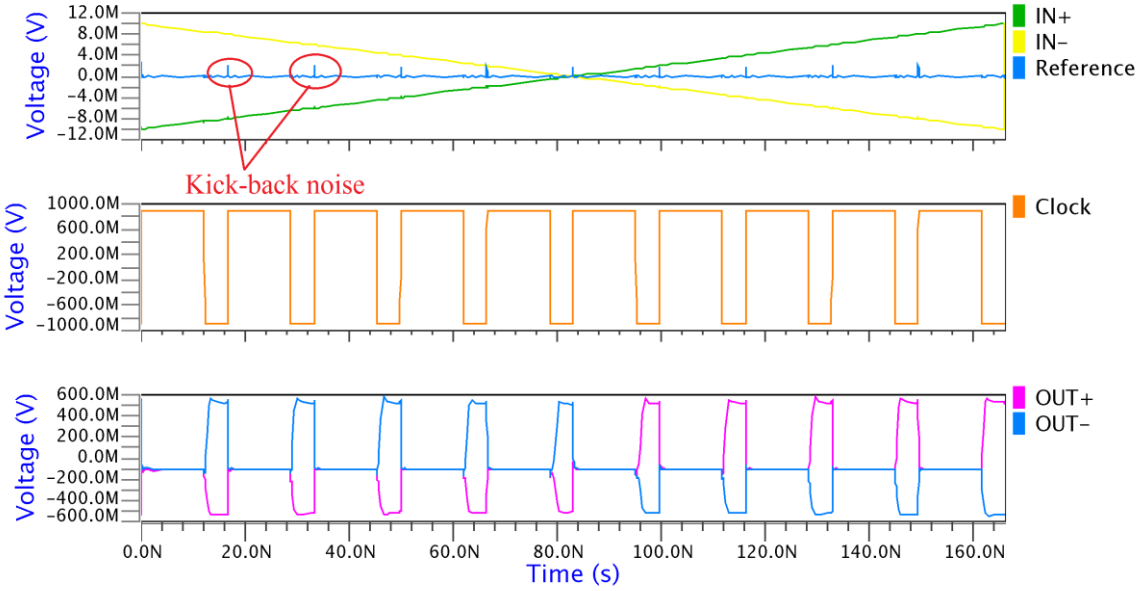


Figure 2.17. Transient simulation result of the comparator.

2.3. 5-bit D/A Converter

Digital to analog converter (DAC) block comes right after the coarse converter block in Figure 1.4. Analog signal converted in the first step is regenerated by this block in order to calculate the residue voltage for fine conversion. DAC block must convert 31 bit thermometer code that corresponds to five bit binary code at the output of the coarse

converter to analog voltage with 10 bit accuracy, because of the absence of error correction circuitry. On the other hand, overall conversion time that is calculated before determines the operation frequency of DAC. Trade-off between resolution and conversion rate for different DAC architectures is presented in Figure 2.18.

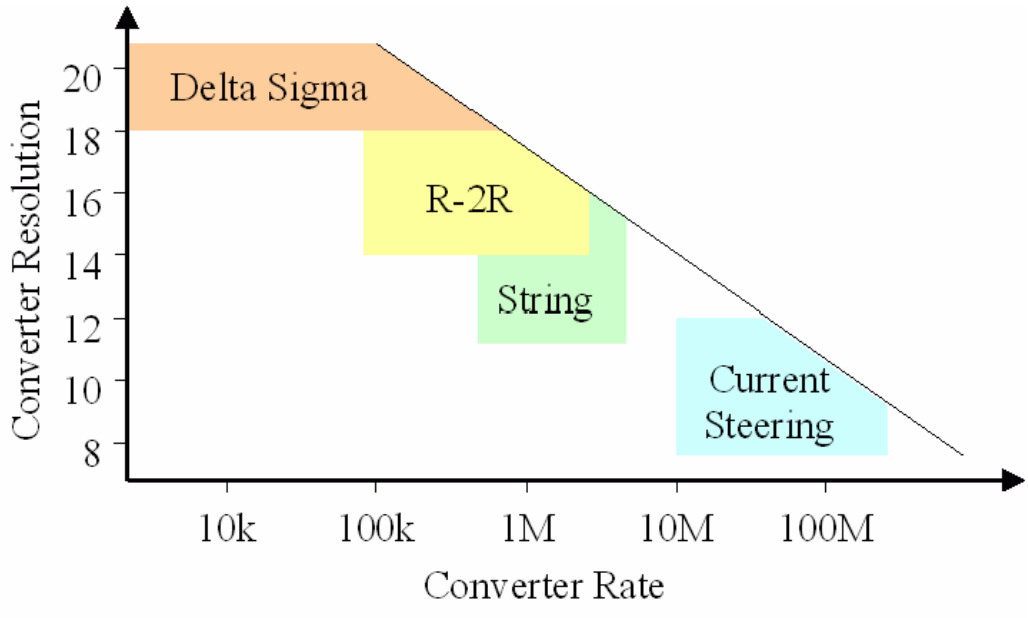


Figure 2.18. Resolution vs. conversion rate trade-off for graph for DACs [15].

Current steering (CS) DAC is evidently the proper option for our purpose as seen in Figure 2.18. Replica current sources, simple switches and output resistors constitute the basic architecture of CS DACs as shown in Figure 2.19.

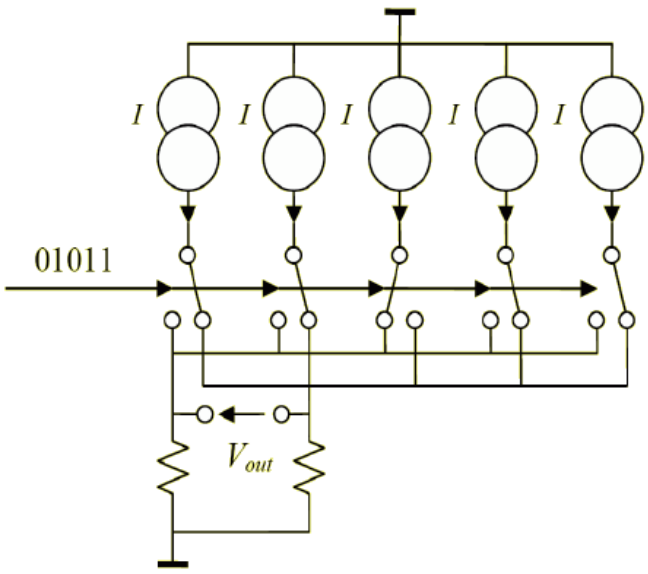


Figure 2.19. Current Steering DAC [15].

These replica currents are generated by current mirrors and simple differential pairs are used as switches shown in Figure 2.19. There are certain issues in designing CS DACs such as switching problems, output resistance modulation and mismatch errors.

Switching problems resembling the ones examined in previous sections are also valid for CS DAC. Charges flowing through the parasitic capacitances of the switching transistors can create glitches at the output of the DAC. This problem has almost same mechanism with the kick-back noise in regenerative comparators. In this case, reducing the size of switching transistors is a straightforward solution, since there is no matching requirement on these transistors. Therefore, using minimum length transistors with small enough width solves almost entirely the switching problems. The remaining glitches result in extended settling time which can be tolerated.

Another important issue is output resistance modulation depending on the input code [16]. The output resistance of the DAC changes according to the number of switches open for one branch. This change in output resistance obviously causes errors, since the output voltage directly depends on the output resistance of the DAC. Increasing the output resistance of each current source can decrease the effect of modulation as the equivalent resistance of all open units become incomparable with the output resistance. The best way to do this is employing cascode transistors for current mirrors. The drawback of this approach is obviously decreased voltage head room at the output which should be taken into consideration.

Last but not least, errors originated from the mismatches between replica currents are an issue to handle in designing CS DACs. In our case 31 identical currents are needed to have ideal output response; however these currents have small differences in reality. These differences stem from the process mismatches between current mirroring transistors. Formulas modeling these mismatches are already given in section 2.2.1.2. Using those, area requirement of the current mirroring transistors is calculated like the following [11]:

$$WxL = \frac{\alpha^2 \beta_0 + 4\alpha^2 V_{TO}/(V_{gs}-V_t)^2}{2(\frac{\sigma(I)}{I})^2} \tag{2.7}$$

In order to achieve desired resolution, selecting proper values for $\sigma(I)/I$ determines overdrive voltage vs. area trade-off. Increasing overdrive voltage easily decreases the required area for one transistor, but also decreases the voltage head room at the output. Considering that cascode transistors already decrease the voltage head room, size of the transistors can be calculated by leaving a safety region for the output voltage.

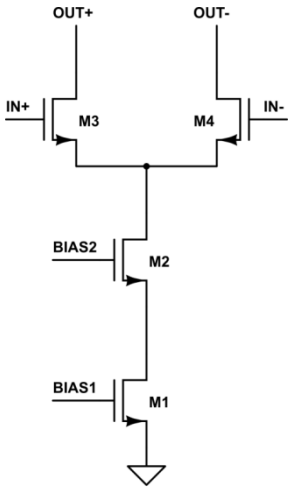


Figure 2.20. Schematic of each unit in DAC.

The designed five bit D/A converter consists of 32 identical units shown in Figure 2.20 in order to have differential output. One of these 32 units is used as a dummy block, and has always same input to steer the current to a particular branch. Figure 2.21 demonstrates the output response of five bit D/A converter when a digitally coded sinusoidal signal is applied to the input.

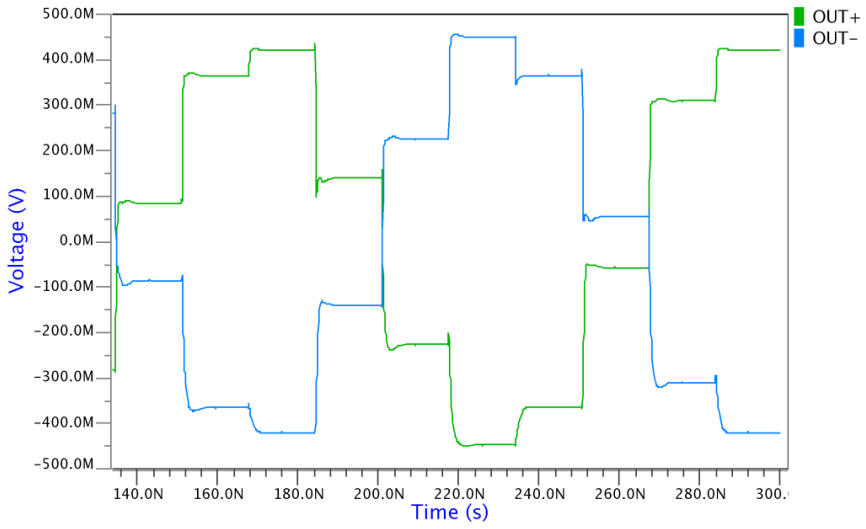


Figure 2.21. Transient simulation result of the D/A converter.

In order to calculate the resolution of D/A converter, SNR value is calculated through FFT result. The result of the FFT analysis is demonstrated in Figure 2.22, and the resolution is calculated as 4.95 bits with a SNR of 31.6 dB.

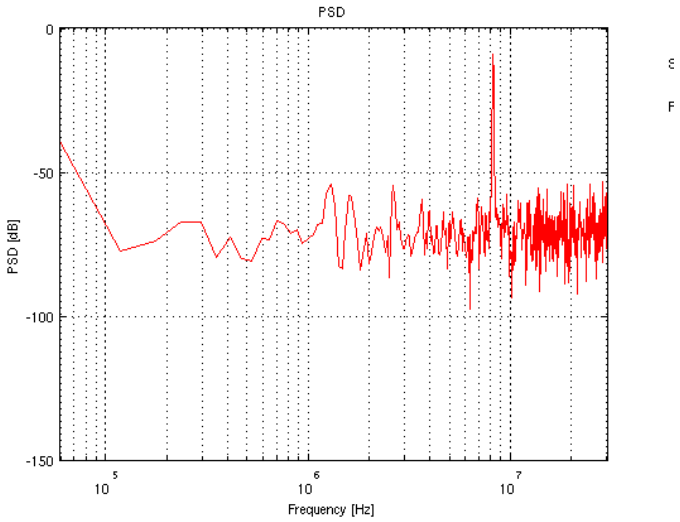


Figure 2.22. FFT result of the D/A converter.

2.4. Residue Generator

Residue generator comes right before the fine A/D converter in Figure 1.4. Output of the five bit D/A converter should be subtracted from the output of the second sample and hold block in order to obtain the residual that is to be converted by fine A/D converter. Residue generator can be defined as a subtractor for this reason.

Subtractor architectures consisting only passive elements could not reach the required frequencies because of their high settling times. Besides, closed loop capacitive subtractor architectures [17] could not give the required accuracy because of linearity problems. Instead of these architectures, analog averaging methodology is utilized since both signals are fully differential. Average of two signals coming from opposite branches is equal to the half of desired subtraction. This attenuation by two is compensated by a closed loop gain circuitry without nonlinearity problems thanks to small input range.

Both of the signals are buffered first in order not to deteriorate the output signals of the D/A converter and S&H block. These two buffered signals are averaged by resistors and capacitors. Finally, the calculated average signal is amplified by a closed loop gain

stage. Only one branch of averaging is represented in Figure 2.23 for the sake of simplicity and consistency.

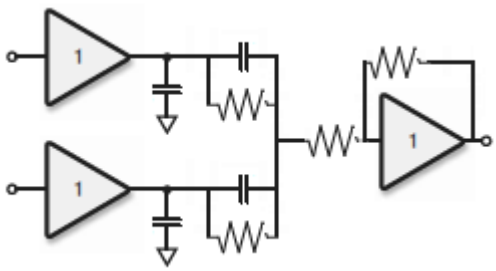


Figure 2.23. Residue generator

Same buffer configuration used in the second sample and hold block is also utilized in the residue generator. The design of folded cascode OTA connected in buffer configuration is examined in Section 2.1.1.1 before. SNR values between 55 dB and 65 dB are achieved for corner cases, thanks to process insensitive design of folded cascode OTA.

3. SIMULATION RESULTS

The performance of the designed ADC using automatically synthesized clock signals will be evaluated in this chapter. Effective number of bits (ENOB) is used as a figure of merit. ENOB is commonly used to evaluate or compare the performance of ADCs in the literature. Formula used to calculate ENOB is like the following:

$$ENOB = \frac{SNR-1.76}{6.02} \tag{3.1}$$

where SNR is given in dB and constant 1.76 comes from the assumption of sinusoidal input signal.

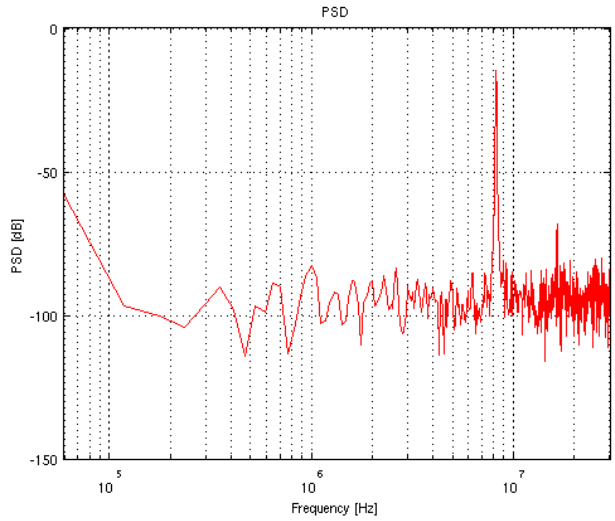
SNR is calculated through FFT that is taken by MATLAB. A sinusoidal input is used with a frequency which is not a submultiple of sampling frequency. This way the repetitions of same samples are avoided. Number of samples taken within one period of input signal is chosen around seven. 1024 samples are used to take the FFT and outputs corresponding to initial 1μs are discarded for settling of the internal signals.

In Table 3.1, ENOB values calculated from the SNR results shown in Figure 3.1 and Figure 3.2 are listed.

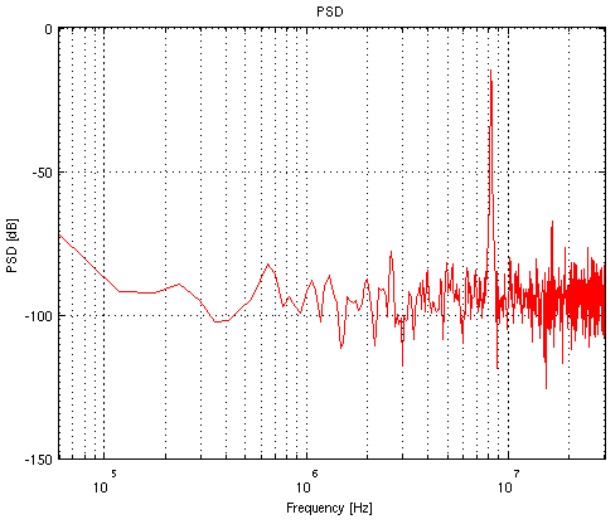
Table 3.1. ENOB values for different clock sets.

	Typical	Slow	Fast
With Target Clocks	7.78	7.63	6.61
With Synthesized Clocks	7.63	7.00	6.75

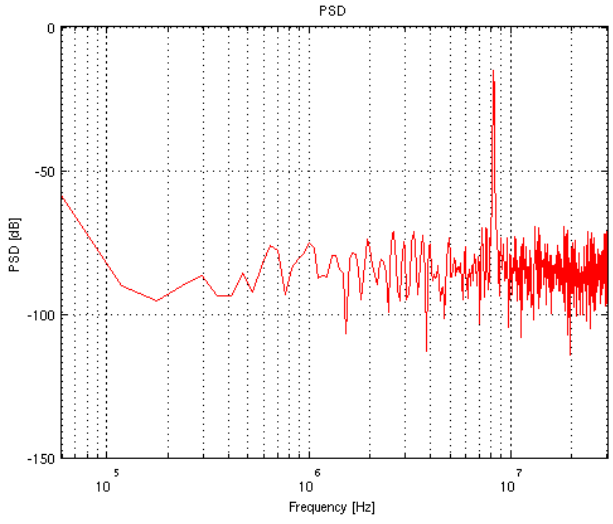
In order to compare the ADC presented in this thesis and examined ADCs from the literature, energy per conversion step is used as a figure of merit. Energy per conversion step is commonly used in the literature and can be defined as:



(a)



(b)



(c)

Figure 3.1. SNR results with target clock signals for (a) typical, (b) slow, (c) fast corners.

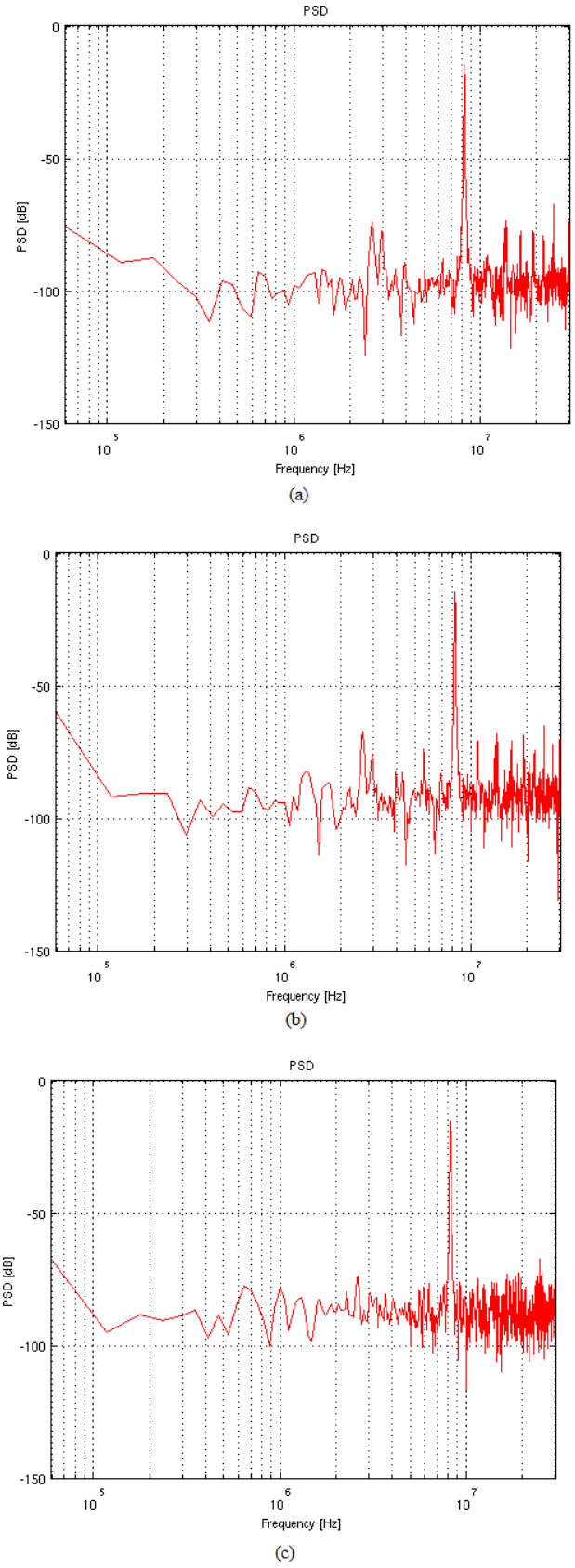


Figure 3.2. SNR results with synthesized clock signals for (a) typical, (b) slow, (c) fast corners.

$$Energy\ per\ conversion\ step = \frac{Power\ consumption}{2^{ENOB}\ x\ Sampling\ rate} \quad (3.2)$$

Table 3.2 lists calculated energy per conversion step values for reviewed ADCs and the presented ADC. This table also includes other important characteristics of the listed ADCs.

Table 3.2. Performance of the designed ADC with other ADCs from the literature.

Reference	Resolution	Sampling frequency	SNR (dB)	ENOB	Power (mW)	FOM (pJ/cs)	Tech.
[3] Chen H.W. 2009	6-bit	1 GS/s	33.8	5.32	49	1.24	0.13
[4] Wu Q. 2006	12-bit	100 MS/s	62	10	520	5	0.35
[18] Murden F. 1995	12-bit	50 MS/s	68	11	575	5.6	1
[5] Clara M. 2002	10-bit	160 MS/s	53.3	8.56	190	3.1	0.18
[6] Zjajo A. 2003	12-bit	80 MS/s	66.3	9.7	100	1.1	0.18
[19] Lin T. C. 2002	8-bit	50 MS/s	48.3	7.7	64	6	0.35
[7] Huang H. 2007	5-bit	1GS/s	31.4	4.92	63	2.4	0.18
This work	10-bit	60 MS/s	48,7	7,8	75	5.6	0.18

The energy per conversion step of the designed ADC is comparable with ADCs which are designed using older technologies. However, ADCs which are designed using newer technologies have better energy per conversion step values relative to ADC presented in this work. This difference can be explained by two important facts in terms of power dissipation and accuracy.

First of all, accuracy of the designed ADC is lower than the reported ADCs listed in Table 3.2. The reason behind this, error correction and calibration circuitries are employed in those ADCs. These circuitries increase the accuracy of the two-step and pipelined ADCs without increasing power consumption levels dramatically.

The effect of the error correction and calibration circuits can be seen as high ENOB values in Table 3.2. However, error correction techniques are not employed in our design, since they can suppress clocking errors. Although this is an advantageous side effect for ordinary ADC design, suppressing clocking errors is not a desirable aspect in our case, since the overall design is used to test the performance of clocking network. Therefore, it can be assumed that the use of error correction techniques would further decrease the energy per conversion step value of the designed ADC.

The dissipated power of the designed ADC is slightly higher than the reported ADCs when the sampling rate is also taken into account. The most common way to decrease the power consumption is the use of open loop systems instead of power hungry closed loop counterparts. Closed loop topologies are employed in both second S&H and residue generator blocks in this work. Therefore, adopting open loop systems can be stated as a future work in order to decrease the overall power consumption of the designed ADC.

Finally, higher sampling rates seem to be realizable for the technology used according to Table 3.2. Sampling rate of the first S&H block is the main limitation on the overall speed of the ADC. Two possible solutions can be proposed to solve this problem. Using different architectures to improve the performance of the employed OTA is the obvious solution. However, this increases the complexity of the OTA and complicates the proper operation in both corner cases. Therefore, utilizing smart A/D conversion concepts seems to be a better solution. Smart A/D conversion techniques employ open loop systems along with calibration circuitries. The inherent high speed operation of open loop systems can increase the sampling rates of the ADC presented in this work.

4. CONCLUSION

10 bit 60 MS/s two step flash ADC design using UMC 180nm technology is presented in this thesis. The ADC is designed to be process insensitive, since the overall design is used as a test circuit for an analog clock tree synthesis tool which can create proper clock signals for all corner cases. The designed ADC circuit should also operate in these conditions in order to test the performance.

The details of the each analog block are examined respectively. Procedures used to design process insensitive analog blocks are also explained in relevant sections. A process insensitive fully differential OTA design which is used in different blocks is especially introduced.

Finally simulation results obtained with synthesized clock signals are listed in the chapter 3. ENOB values up to eight bits are achieved in typical case. These results have also shown that the designed ADC has decent performance in both corner cases. Resolutions more than 6.5 bits are obtained even for corner case simulations. Comparison between the designed ADC and the ADCs from the literature is made by using energy per conversion step as a figure of merit. This comparison showed that the designed ADC has a performance close to the ADCs that are designed by using older technologies. However, recent designs have better performance than the ADC presented in this thesis. Possible reasons behind this inferior performance are stated as the use of error correction circuitries and the use of open loop systems.

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