FABRICATION AND CHARACTERIZATION OF A PLANAR WATER GATED TRANSISTOR UTILIZING ULTRA THIN SINGLE CRYSTALLINE SILICON FILM

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ABSTRACT

FABRICATION AND CHARACTERIZATION OF A PLANAR WATER GATED TRANSISTOR UTILIZING ULTRA THIN SINGLE CRYSTALLINE SILICON FILM

In this thesis, the fabrication and characterization of a planar water-gated thin film transistor are explained and analyzed. Silicon-on-insulator (SOI) wafer is used to build the device. Two different gate structures are used and tested. Firstly, the measurements are realized with the usual probe gate immersed into the water droplet as a reference. Then the novel planar gate structure is used. In the fabrication process, first the 16-nm thick silicon on top of the SOI wafer is patterned to build the channel area of the transistor. After that aluminum is evaporated on top of it to make the drain, source and planar gate contacts at one step. Finally, photoresist is spin coated on the drain and source electrodes to insulate them from the water droplet. After forming the transistor structure, a water droplet is dripped onto the channel area. It has contact to the gate electrode and channel, but not to the drain and source electrodes. Thanks to the this liquid-solid interface, an electrical double layer is formed on the channel, which serves as a perfect gate insulator since it is uniform, pin-hole free, very thin and has a high dielectric constant. Fabricated transistors are tested and characterized. Since the silicon used is p-type, negative voltages are applied. The transistor works between 0 V and -0.7 V. Using the probe gate structure, a maximum drain current of 99.49 μA is established with an on-off ratio of 232000 and threshold voltage of 0.27 V. In the planar gate structure this values are 19.15 μA, 2150 and 0.31 V respectively. However the transistor parameters of the planar gate structure can be improved by the future developments.

ÖZET

ÇOK İNCE TEK KRİSTALLİ SİLİSYUM FİLM KULLANAN YATAY SIVI KAPILI TRANSİSTÖRÜN ÜRETİMİ VE BELİRLENMESİ

Bu tezde, yatay sıvı kapılı bir ince film transistörün üretimi ve belirlenmesi açıklanıp analiz edilmiştir. Cihazı üretmek için yalıtkan üstü silikon (SOI) pul kullanılmıştır. İki farklı kapı yapısı kullanılmış ve test edilmiştir. İlk olarak referans olması amacıyla, su damlasının içine batırılan klasik ince tel kapıyla ölçümler gerçekleştirilmiştir. Daha sonra özgün yatay kapı yapısı kullanılmıştır. Üretim aşamasında öncelikle transistörün kanal bölgesini oluşturmak için SOI pulun üzerindeki 16 nm kalınlığında silisyum şekillendirilmiştir. Daha sonra üzerine tek seferde kaynak, savak ve yatay kapı kontaklarını yapmak için alüminyum buharlaştırılmıştır. Son olarak kaynak ve savak elektrotlarının üzerine, bunları su damlasından izole etmek için, döndürmeli fotorezist kaplanmıştır. Transistör yapısını oluşturduktan sonra, kanal bölgesi üzerine bir su damlası damlatılmıştır. Su damlası kapı elektroduna ve kanala temas etmekte, fakat kaynak ve savak elektrotlarına temas etmemektedir. Bu katı-sıvı arayüzü sayesinde kanal üzerinde mükemmel bir kapı yalıtkanı olarak hizmet eden bir elektrik çift katman oluşmaktadır, çünkü bu katman düzgün, deliksiz, çok incedir ve yüksek dielektrik sabitine sahiptir. Üretilen transistörler test edilip karakterize edilmiştir. Kullanılan silisyum p tipi olduğu için negatif gerilimler uygulanmıştır. Transistör 0 V ile -0.7 V arasında çalışmaktadır. İnce tel kapı yapısını kullanarak 99.49 μA maksimum savak akımı, 232000 açık-kapalı akım oranı ve 0.27 V eşik gerilimi elde edilmiştir. Yatay kapı yapısında bu değerler sırasıyla 19.15 μA, 2150 ve 0.31 V olarak ölçülmüştür. Ancak yatay kapı yapısının transistör parametreleri gelecekteki geliştirmelerle iyileştirilebilir.

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LIST OF SYMBOLS

Al	Aluminum
C_{d}	Diffuse layer capacitance
C_{dl}	Double layer capacitance
C_{i}	Gate insulator capacitance per area
C_{s}	Stern layer capacitance
d	Distance between two plates of a capacitor
g_{m}	Transconductance
H_2O	Water
HNO_3	Nitric acid
I_{d}	Drain current
$I_{\mathrm{d,V_{g_{max}}}}$	Drain current at maximum gate voltage
$I_{\mathrm{d,V_{g_{min}}}}$	Drain current at minimum gate voltage
$I_{\mathrm{d_{lin}}}$	Drain current at linear region
$I_{\mathrm{d_{sat}}}$	Drain current at saturation region
I_{sd}	Source-to-drain current
L	Length of the semiconductor channel
n	n-type doping concentration
NH_4F	Ammonium fluoride
p	p-type doping concentration
p^{++}	p-type high concentration doping
q	Elementary charge
Si	Silicon
SiO_2	Silicon dioxide
SnS_2	Tin(IV) sulfide
V_{dd}	IC power-supply pin
V_{sd}	Source-to-drain voltage
V_{sg}	Source-to-gate voltage
V_{th}	Threshold voltage

W	Width of the semiconductor channel
ZnO	Zinc oxide
ϵ_0	Permittivity of vacuum
ϵ_r	Relative permittivity
μ_n	Electron mobility
μ_p	Hole mobility
Ω	Ohm
Ψ_1	Electrical potential at the OHP
Ψ_2	Electrical potential at the IHP
ρ	Resistivity

LIST OF ACRONYMS/ABBREVIATIONS

DI	Deionized (water)
EDL	Electrical double layer
FET	Field effect transistor
HMDS	Hexamethyldisilazane
IBM	International Business Machines
IHP	Inner Helmholtz plane
ISFET	Ion-sensitive field effect transistor
MEMS	Micro-electro-mechanical systems
MOSFET	Metal-oxide-semiconductor field effect transistor
OFET	Organic field effect transistor
OHP	Outer Helmholtz plane
P3HT	Poly(3-hexylthiophene-2,5-diyl)
PBTTT	Poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene)
PR	Photoresist
SC	Semiconductor
SIMOX	Separation by implantation of oxygen
SOI	Silicon-on-insulator
SOITEC	Silicon-on-insulator Technology
TFT	Thin film transistor
UV	Ultraviolet
VLSI	Very-large-scale integration
WG-FET	Water-gated field effect transistor

1. INTRODUCTION

At Bell Telephone Laboratories, J. Bardeen and W. H. Brattain were working on finding a smaller, more efficient, more reliable, more durable and cheaper replacement for the vacuum tubes [1]. In 1948 when they built the first transistor, they didn't only invent a better amplifier than the vacuum tube, but also a digital circuit element that will find itself a place in almost every electronic device in the future [2]. The device they created has evolved and evolved through the years, as a result there are numerous sub-types of the transistor now. Even a paper about the transistor consisting of one single atom has been published in year 2012 [3].

For instance, there are transistors containing an organic semiconductor as their channel material instead of the usual inorganic ones like silicon or germanium. Different types of semiconductor polymers like PBTTT [4] and P3HT [5] are used to build such transistors. Other than that, there are also ion-sensitive field effect transistors (ISFET) which are mostly used for sensing purposes. They have a solution on top of their channel area, which is practically used as the gate electrode. A nanoscale pH sensor sensing the change of pH in this solution [6] is an example to this type of transistor. Another special kind of the field effect transistor is the thin-film transistor (TFT), which usually contains a thin deposited layer of semiconductor as the channel region. The semiconductor used can be inorganic or organic as well. It is shown that some basic digital circuits can be designed using organic thin-film transistors [7]. Using thin-films may enable compatibility with optoelectronics, too. A thin-film field effect transistor using a single-crystalline thin-film transparent oxide semiconductor is fabricated [8] and this transparency provides promising combination with optoelectronic devices.

Thanks to the variety of the available transistors, specific devices for specific application areas can be produced. The fabricated transistor, which is described and analyzed in the following chapters of this thesis, is a novel combination of an inorganic thin-film transistor and an ISFET. The thin-film semiconductor of the transistor is not

produced through deposition though. The thin silicon film on a silicon-on-insulator (SOI) wafer is used, which is single-crystalline and thus advantageous in terms of mobility and stability. Through dripping a water droplet on top of this silicon, the gate insulator is created. This design looks similar to an ISFET. However the fabricated device is not primarily designed as a sensor, but as a field effect transistor (FET) and it performs well as a transistor. Additionally, this similarity to an ISFET makes the transistor a prospective candidate for possible sensor compatibility.

1.1. Silicon-on-Insulator Wafer

A silicon-on-insulator wafer is a modified version of the usual single crystalline silicon wafers. Unlike a usual silicon wafer, it contains a thin single crystalline silicon film on top of a thin insulator layer, which is usually silicon dioxide. These thin layers of silicon and insulator are located on a thick bulk silicon [9].

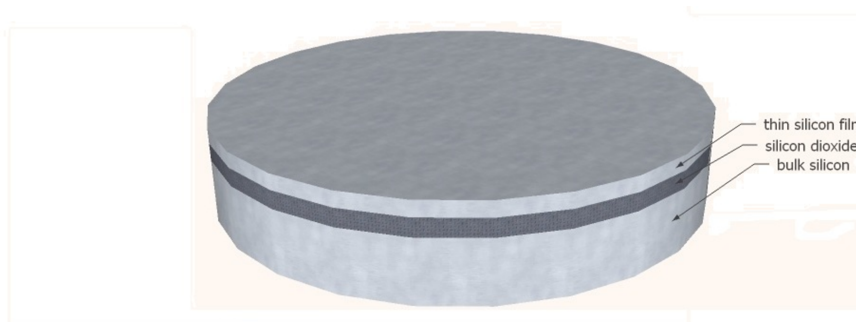


Figure 1.1. A silicon-on-insulator wafer (not to scale).

SOI wafers may simplify the fabrication and improve the performance for specific designs of MEMS and VLSI. Having an insulator layer between the channel region silicon and bulk silicon enhances the characteristics of the fabricated device by reducing parasitic effects [10]. Thanks to these advantages SOI wafers find themselves a place in the industry, too. Some technology companies are using SOI wafers to build their transistors. In 2011, a multicore server processor was built from SOI transistors by IBM [11]. It was an eight-core processor fabricated in 45-nm SOI technology with 11 levels of metal and contained more than one billion SOI transistors.

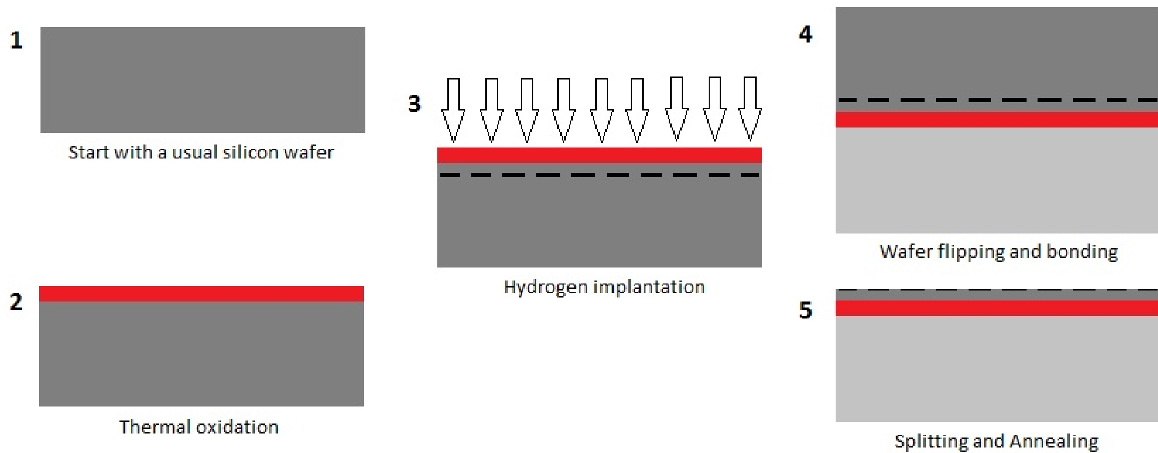


Figure 1.2. Production of SOI wafer by Smart Cut method.

There are several ways to produce silicon-on-insulator wafers. One method is growing the topmost silicon directly on the insulator layer, which is called as the seed method. The epitaxial growth of silicon is enabled by the vias through the insulator from the bulk silicon. Another production method is called separation by implantation of oxygen (SIMOX) and it uses an oxygen ion beam implantation process to implant the oxygen molecules under the surface. Then the wafer is annealed at high temperature to create the buried SiO_2 layer [12]. Finally, the last method that will be mentioned here is achieved through wafer bonding. As shown in Figure 1.2, in this method a silicon wafer is thermally oxidized and then hydrogen atoms are implanted under the silicon dioxide layer. Then it is bonded to another silicon wafer and the bulk under the hydrogen implanted layer is cut away [13]. The hydrogen implantation enables the splitting of the wafer to be precise and smooth. After that a heat treatment is applied to give the SOI wafer its final form. This method is referred as the Smart Cut method.

The SOI wafers used in this project are purchased from the company SOITEC and they use the Smart Cut method to produce them. They have several types of SOI wafers for specific application areas. The ones that are used in this work to build the water-gated transistor have 16 nm p-type single crystalline silicon film on top of 145 nm SiO_2 layer. The resistivity of the top silicon layer is 10 Ω·cm and from this

resistivity value, the doping concentration can be found using the Equation 1.1, where ρ is the resistivity, q is the elementary electric charge, μ_n and μ_p are the mobility of an electron and a hole respectively and n and p are the n-type and p-type doping concentrations.

$$\rho = \frac{1}{q(\mu_n n + \mu_p p)} \tag{1.1}$$

Since the silicon is p-type, the acceptor atom concentration is dominant over the donor atom concentration, so the $\mu_n n$ part of the equation can be neglected, which leads to

$$\rho = \frac{1}{q\mu_p p} . \tag{1.2}$$

When the ρ, q and μ_p values are inserted into the Equation 1.2, the acceptor atom concentration is found as $p = 1.4 \times 10^{15}\,\text{cm}^{-3}$, which means that the single crystalline silicon used to build the transistor is lightly doped.

1.2. Motivation and Novelty

In today's world, almost every electronic device contains millions, if not billions, of MOSFET's inside and the production of these classical MOSFET's requires very expensive facilities. Also as the device sizes get smaller and smaller, building a uniform, pin-hole free gate insulator becomes more difficult. However some application areas don't require such small devices or fast performance. Bigger or slower transistors, which satisfy the needs of these application fields, can be produced at a much lower price.

A water-gated transistor can be an alternative to the MOSFET where high performance is not a necessity. When the water droplet is placed directly on the semiconductor, then this liquid-solid interface brings several advantages. First of all, the very thin electrical double layer, which is formed at this interface, behaves as a perfect gate insulator. The liquid covers the top of the semiconductor uniformly and the resulting

gate insulator becomes pin-hole free. This double layer has relatively high dielectric constant ($\epsilon_r = 80.1$) compared to the frequently used silicon dioxide ($\epsilon_r = 3.9$) as well. Its small thickness combined with its high dielectric constant presents a better gate insulator capacitance and thanks to this improvement the introduced transistor can function below 0.7 V, which may make it suitable for low power applications. This voltage level is desirable for another aspect, too. Since the device has water in design, the possibility of hydrolysis is dangerous for the proper functioning of the device. However the water gets hydrolyzed at 1.23 V [14] and working below 0.7 V eliminates this possibility. On top of these advantages, water-gated transistors can easily be compatible with biosensors, since these sensors require fluidic interfaces.

Previously, a water gated organic FET device was introduced as a cheap and simple alternative [15]. It uses a semiconductor polymer thin film in the channel region. A water droplet is used as the gate insulator and a probe is immersed into the water as the gate electrode. However organic materials have a certain life time and stability problems due to polymer degradation. Also the mobility and performance of the polymer devices are very low compared to the inorganic semiconductor devices.

The water-gated transistor, which is fabricated and characterized throughout this thesis, uses an inorganic semiconductor, single crystalline silicon, to overcome the problems associated with organic materials. Silicon has higher mobility, is stable throughout the time and less sensitive to environmental conditions.

In addition to the mentioned desirable properties of the fabricated water-gated transistor, a planar gate electrode structure is integrated as well. This structure was used with success in an organic transistor previously [16]. This planar gate design simplifies the integration of several devices on the same die. Otherwise for every transistor a probe top gate should have been used separately. Also the gate electrode is fabricated at the same time when drain and source electrodes are being built, which makes the fabrication of the transistor more practical.

1.3. Outline of the Thesis

Up to this point in Chapter 1, various transistor types that are associated with the fabricated transistor of this work are briefly presented, along with some familiarizing examples. Following this, silicon-on-insulator wafer is introduced and the SOI wafer used in this work is presented. Finally the motivation behind this project and its novelty are told.

In Chapter 2, different types and applications of water-gated FET's are described. Then the theory behind the field effect transistors and especially the water-gated FET's is explained along with their principal of operation and electrical characteristics. The electrical double layer, which is the key concept of the water-gated devices, is presented. After that, a short introduction to the band structures is made to clarify why an annealing step is needed to establish an ohmic contact between the metal and the semiconductor.

In Chapter 3, both structures of the fabricated transistor, planar gated and probe gated, are described and the fabrication process is explained step by step.

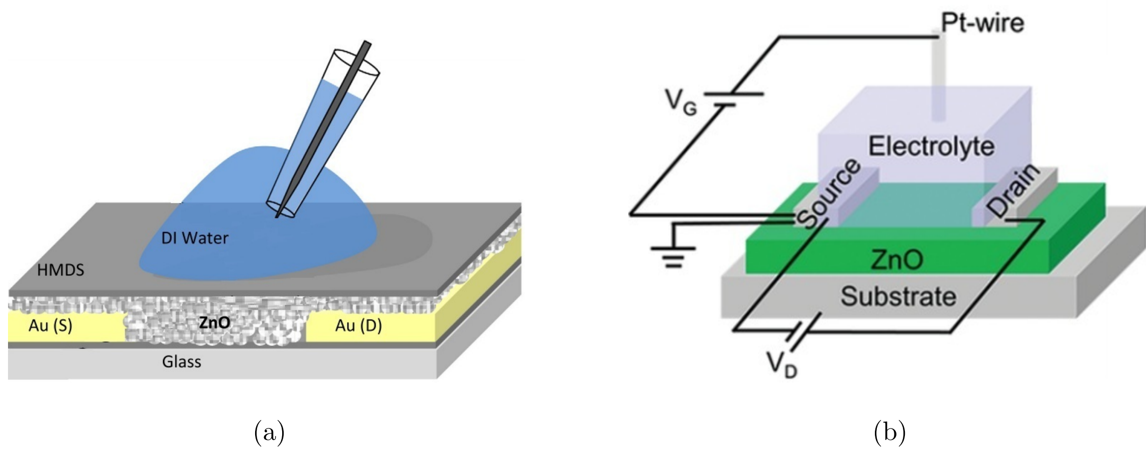
In Chapter 4, the measurements of the planar gated and probe gated transistors are presented after introducing the measurement equipment. Then, using these measurement results, the transistors are characterized and compared in terms of their performance.

In Chapter 5, the document is concluded with a brief summary of the measurement and characterization results, which is followed by an introduction of the possible future works of the project.

2. THEORY

2.1. Water-Gated Field Effect Transistors

A water-gated field effect transistor (WG-FET) is a special type FET, which contains water on its gate insulator or uses the water directly as the gate insulator. The gate electrode is mostly a needle probe immersed into the water from top. Dripping the water droplet onto the gate insulator isolates the water from the channel and in most of the designs from the drain and source electrodes as well. This isolation enables the transistor to be more stable, since the possibility of hydrolysis and current leakage through the water are avoided. However the voltage that is needed to modulate the channel becomes very high in that case because of the insulator layer. In the other type, where the water is placed directly on the channel, the electrical double layer in the liquid-solid interface behaves as the gate insulator, which is very thin and consequently needs lower gate voltage. The drawback of this design is the possibility of hydrolysis above 1 V and current leakage.



(a) (b)

Figure 2.1. WG-FET's with (a) water placed on the insulator layer [17] and (b) water placed on the channel [18].

Both types of WG-FET's can be used according to the needs of the desired application. Two transistors using ZnO as the inorganic semiconductor material can

be seen in Figure 2.1. In the first one, the water droplet is placed on the nonconductive HMDS layer [17]. However in the second one, the liquid is dripped directly on the ZnO layer [18]. Both of them use a top probe gate electrode to modulate the drain current.

In addition to these WG-FET's that use inorganic semiconductors in their channel region, organic devices were introduced as well. A low-power and fast-switching organic FET with ionic liquids was fabricated using an organic rubrene crystal as the channel semiconductor [19]. An ionic liquid electrode is placed on the rubrene directly and this enables the transistor to work at low voltages and consequently to consume low power.

Containing water in its own design makes the water-gated transistor a perfect candidate for sensing applications as well. The content of the liquid that is placed on the channel may change the characteristic of the transistor and so specific molecules can be sensed by specific characterization changes. A biosensor was built using a WG-FET that contains deposited polysilicon thin film as the channel [20]. On this channel, 8.5 nm gate oxide is grown and on top of the gate oxide the liquid containing the C-reactive protein is placed and then this protein is sensed by the transistor. Another similar sensor was built using graphene [21]. A liquid-gated graphene field effect transistor was used as a pH sensor. Organic semiconductor WG-FET's can be used as biosensors as well. In 2013, a biosensor based on a planar water gated organic FET was introduced [22]. It has a planar gate electrode that is fabricated at the same time with the drain and source electrodes, which simplifies the fabrication and adds compactness to the device.

2.1.1. Principle of Operation

Field effect transistors, in general, are devices with the feature that the current between two terminals can be controlled by small changes in the voltage at the third terminal. Thanks to this feature, they can be used for amplification or switching purposes. The controlling of the current in the channel region, the semiconductor part between two terminals, is achieved by the field effect phenomenon, which can

be described as the change of the conductivity in the channel by an applied electric field [23].

As the other types of the FET, water-gated field effect transistors contain three main terminals; the source and drain, which are placed at the two sides of the channel and the gate, which controls the current flowing through the channel. There stands also a gate insulator between the gate and channel. When a voltage is applied to the gate, after a certain value, a conductive channel is created by the charge carriers. However, a reverse voltage applied to the gate causes the channel to close.

The WG-FET fabricated in this project utilizes a 16 nm single crystalline p-type silicon film as the channel material. The silicon used is lightly doped, as a result at zero gate voltage the conductivity of the channel is low. However when a negative voltage is applied to the gate, due to the field effect phenomenon, more holes (positive charge carriers) are drawn towards the channel and consequently the conductivity of the channel increases. In this situation, when another negative voltage is applied to the drain terminal, a current starts to flow from source to drain, since in most cases the source is grounded. The magnitude of the current depends on both voltages, V_{gs} and V_{ds}. At constant V_{gs}, when the magnitude of V_{ds} is increased, the current also increases up to a point, but then it saturates. So the saturation current is dependent on the gate voltage.

2.1.2. Electrical Characteristics

A field effect transistor basically has three operating regimes. In cut-off, a very small current is flowing through the transistor and it is mostly considered as off in this situation. In linear region, the current is determined by the drain and gate voltages and in the saturation region the current reaches its maximum value for the selected gate voltage. The field effect transistors are usually operated at linear or saturation regime. For this to happen, the magnitude of the gate voltage should be above a minimum voltage value, which is named as the threshold voltage [24].

A main difference between the ordinary MOSFET and the WG-FET fabricated in this project is the modes in the channel at various gate voltages. Whereas the classical MOSFET has accumulation, depletion and inversion modes, the WG-FET works only in accumulation. Unlike the MOSFET, it has only a p-type silicon in the design and the transistor behavior is obtained through modification of the hole concentration in the channel. This type of channel modulation is called as electric field doping [25]. At the off state, that is zero gate voltage applied, the channel remains lightly doped, but under negative gate voltage holes are collected in the channel, which increases the conductivity. Another difference is the off-current. In the cut-off regime, the WG-FET has a small current since it doesn't have inversion mode.

The design of the FET, where the gate insulator is placed between the gate electrode and semiconductor channel, contributes to a plate capacitor, since a vertical electric field is applied between the gate and channel. The dielectric material of the capacitor is the gate insulator, whether it is a solid material or created by electrical double layer (EDL). In the WG-FET designed in this work, it is the thin EDL. This capacitance per unit area then can be given as

$$C_{\mathrm{i}} = \frac{\epsilon_{\mathrm{r}}\epsilon_0}{d} \tag{2.1}$$

where ϵ_0 is the permittivity of vacuum, ϵ_{r} is the relative permittivity of the insulator layer and d is the dielectric thickness.

The drain current I_{d} of the WG-FET follows two main regimes according to varying gate and drain voltages, as the source electrode is grounded. As mentioned above, the transistor usually operates either in linear or in saturation region. The WG-FET operates in linear region, if the magnitude of the drain voltage is less than the magnitude of the difference between gate voltage and threshold voltage, as indicated in Equation 2.2. Otherwise, the WG-FET operates in saturation region.

$$|V_{\mathrm{ds}}| < |V_{\mathrm{gs}} - V_{\mathrm{th}}| \tag{2.2}$$

The current values in both regimes can be determined according to the Equation 2.3 and Equation 2.4 for linear and saturation regions respectively.

$$I_{\mathrm{d_{lin}}} = \frac{W}{L}\mu_{\mathrm{p}} C_{\mathrm{i}}[(V_{\mathrm{gs}} - V_{\mathrm{th}})V_{\mathrm{ds}} - \frac{V_{\mathrm{ds}}^2}{2}] \tag{2.3}$$

$$I_{\mathrm{d_{sat}}} = \frac{W}{2L}\mu_{\mathrm{p}} C_{\mathrm{i}}(V_{\mathrm{gs}} - V_{\mathrm{th}})^2 \tag{2.4}$$

In both of these equations, W is the width and L is the length of the channel, μ_{p} is the mobility of the holes in silicon and C_{i} is the insulator capacitance per unit area.

When a WG-FET is fabricated, some other characteristics like the transconductance, threshold voltage, maximum drain current and on/off ratio are also of interest. A high transconductance, a high on/off ratio, a high maximum drain current and a low threshold voltage are expected from a transistor.

The transconductance of a transistor can be described as the change of the output current with respect to the changes in the input voltage. In this case, it can be expressed as in the Equation 2.5.

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{gs}}} \tag{2.5}$$

The transconductance can be calculated for specific voltage values in small signal analysis. Therefore a definite transconductance of the transistor fabricated in this project cannot be calculated, since it has not been used for small signal analysis yet. The derivation of the drain current with respect to the gate voltage without the small signal analysis can result in misleading values.

The threshold voltage of a transistor can be found with a simple yet consistent method introduced in 1999 [26]. In this method two different $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves are needed two determine the threshold voltage. In one of them the measurement is made

as the drain voltage V_{ds} is equal to V_{dd}. In the other one V_{ds} is about one tenth of V_{dd}, which ensures that the transistor doesn't operate in saturation region. Then the linear region in the curve of the latter is extrapolated until the x-axis and the current value corresponding to that voltage value intersecting the x-axis is used in the first curve. The voltage value in the first curve that the transistor had at the previously determined current value is the threshold voltage.

The on/off ratio of a WG-FET is especially important for the switching usage of the transistors in digital circuits. It means the ratio of the on current to the off current. The on current mentioned here is the drain current flowing, when the maximum gate and drain voltages are applied. It is referred as the maximum drain current as well. However, the off current is measured when the gate voltage is zero and the drain voltage is maximum. The on/off ratio can be expressed briefly as in the Equation 2.6.

$$\text{on/off ratio} = \frac{I_{\text{d,V}_{\text{gmax}}}}{I_{\text{d,V}_{\text{gmin}}}} \tag{2.6}$$

2.1.3. Electrical Double Layer

When a solid surface is contacted directly to water or another liquid, as in the case of this work where water is dripped onto silicon, a discontinuity occurs at the interface and two different phases form. The charges separate at the interfacial region between the two phases [27] and this separation combined with the charged surface is referred as the electrical double layer, which can extend from 0,1 nm to 100 nm depending on the concentration of the solution [28].

As shown in Figure 2.2, in order EDL to occur a charged solid surface in contact with a liquid is needed. When the surface is charged, a balancing contour charge occurs in the liquid and these charges concentrate near the surface as can be predicted. Consequently a new liquid layer is formed near the surface, which is different than the rest of the liquid [29].

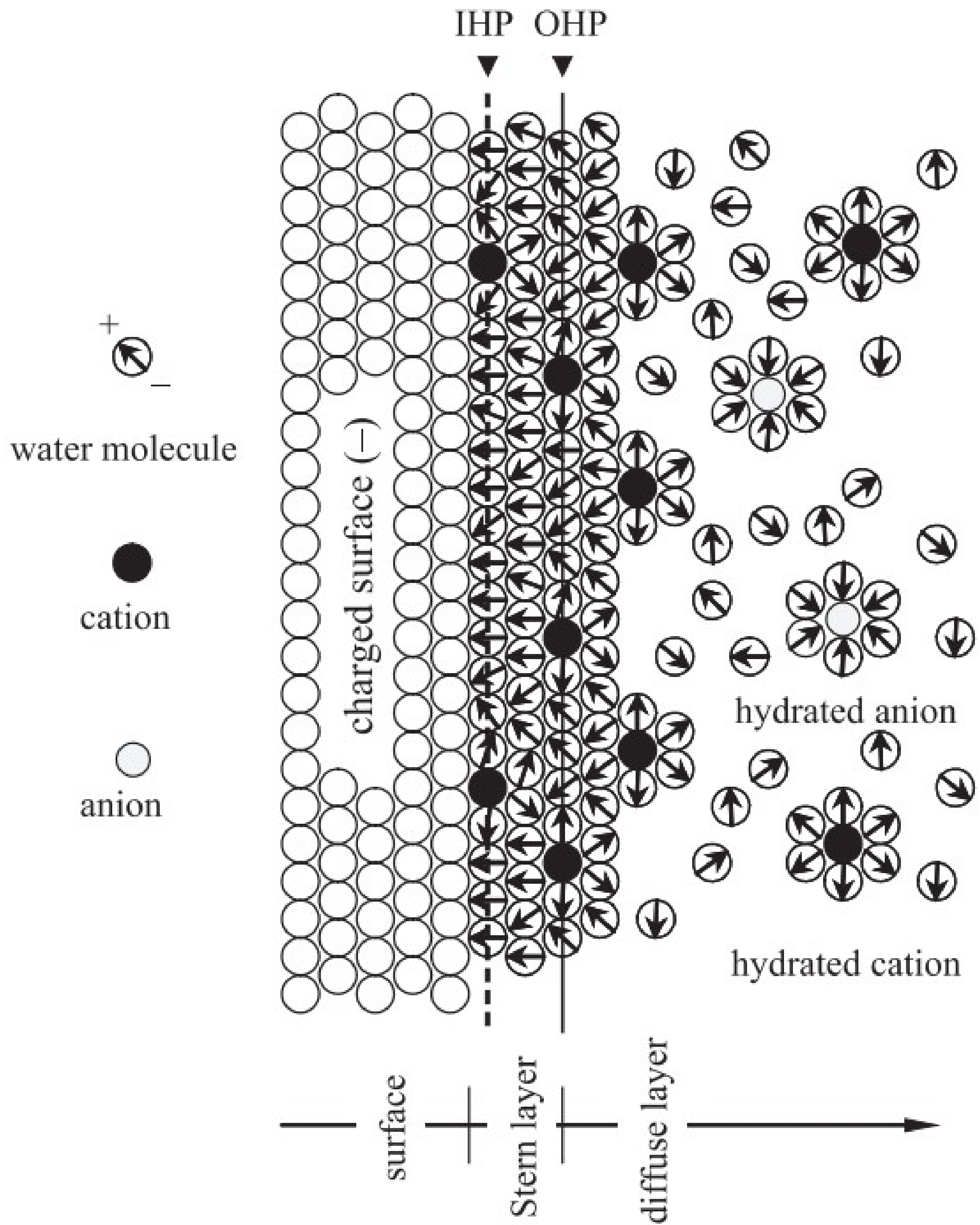


Figure 2.2. Schematic model of the EDL on a negatively charged surface [28].

Several theorems were suggested about the electrical double layer and the most basic one is the Helmholtz Double Layer theorem which appeared in 1879. He suggested that the ions are placed in a compact layer in contact with the charged solid surface. After that, Gouy and Chapman developed this idea by offering a diffuse double layer, in which the ions extend to a distance from the surface of the solid. With that concept, they improved the theorem by suggesting that the charges are not located in rigid layers, which doesn't occur in the nature as well. According to them, the ions in the rest of the liquid follow Boltzmann distribution. However this assumption does not always provide the correct solution for regions close to the surface, although it fits well to the bulk solution [30].

The last major change to the theorem was made by Stern in 1924. Although some other new developments were reported in the following years, his version is the milestone of the electrical double layer. He combined two different ideas about the double layer, in which he expressed that there exists a rigid charged surface with a cloud of oppositely charged ions in the liquid. Two planes are determined in the double layer then. The first one is the inner Helmholtz plane (IHP), which passes through the centers of adsorbed ions and is located very close to the surface as can be seen in Figure 2.2. The second plane is the outer Helmholtz plane (OHP) and it passes through the centers of the hydrated ions that are in contact with the metal surface. These hydrated ions are in this case the cations that are surrounded by water molecules and don't have any direct contact to the surface [31]. The electrical potentials at the IHP and OHP are written as Ψ_2 and Ψ_1 respectively and the potential profile of the situation in Figure 2.2 can be observed in Figure 2.3.

The capacitance associated with the EDL can be separated in two parts with this modeling. The Stern layer capacitance, which lies between the IHP and OHP is connected in series with the diffuse layer capacitance which extends from the OHP into the bulk solution.

$$C_{\mathrm{dl}} = \frac{C_{\mathrm{s}} C_{\mathrm{d}}}{C_{\mathrm{s}} + C_{\mathrm{d}}} \tag{2.7}$$

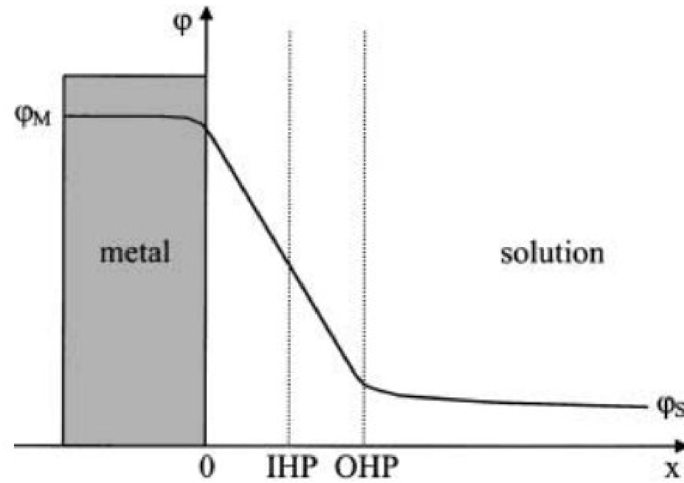


Figure 2.3. Potential profile in the double layer formed at a metallic electrode charged negatively [29].

As can be interpreted from Equation 2.7, smaller capacitance of these two is dominant and determines the double layer capacitance. C_{d} is dependent on the surface charge density and electrolyte concentration, whereas C_{s} shows minimal dependency. As a result, under high electrolyte concentration C_{s} is smaller and determines the C_{dl}. Otherwise C_{d} is the dominant part [28].

When this thin electrical double layer capacitance is used as the gate insulator, as in this project where the EDL isolates the gate and channel from each other, the device gains the advantage of functioning at very low voltages, since the EDL capacitance is relatively larger than its solid competitors. Although the value of the EDL capacitance varies according to the solid material, electrolyte and its concentration, some experimental measurements were done to determine its value for specific designs. The double layer capacitance was measured as $C_{\mathrm{DL}} = 14.6\,\mu\mathrm{F/cm}^2$ for a pentacene ultra-thin film OFET operating with water [32]. The design had a bottom gate for precise measurement of the EDL capacitance as well. Another EDL capacitance measurement was achieved using carbon nanotubes in propylene carbonate electrolytes and the measurement result turned out to be around $C_{\mathrm{DL}} = 10\,\mu\mathrm{F/cm}^2$ [33]. These two different examples of EDL capacitance can give an idea about the range of it.

2.1.4. Planar WG-FET

The novel water-gated field effect transistor fabricated in this project is planar gated, which means that the gate electrode is placed in the same plane as the drain and source electrodes and fabricated at the same time. As the gate insulator, a deionized (DI) water droplet is used because of the several advantages that are mentioned in the thesis previously.

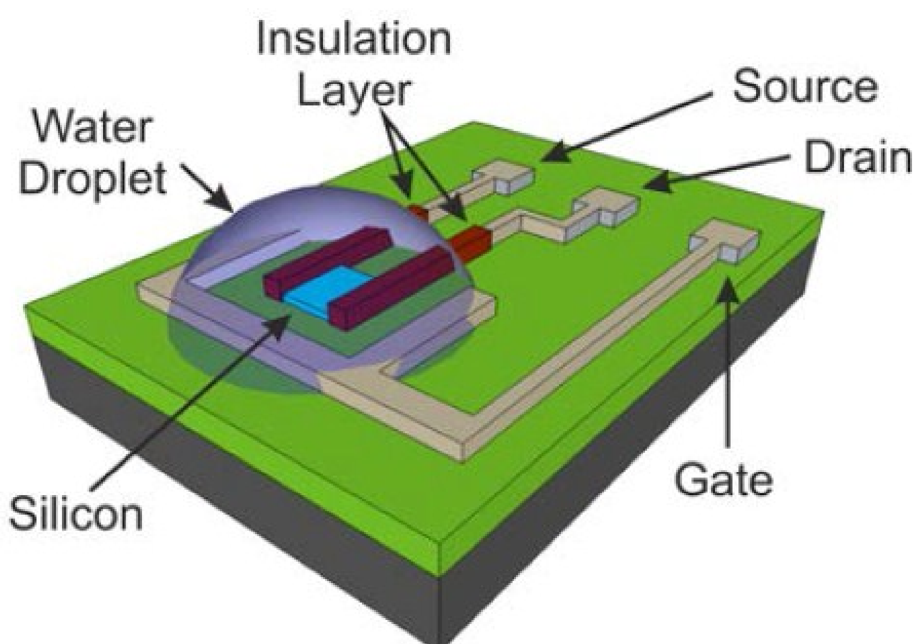


Figure 2.4. Planar water-gated field effect transistor fabricated in this project.

This planar gate design can be seen in Figure 2.4. The regions of the source and drain electrodes, where they contact the DI-water droplet, are covered with insulator to prevent any possible current leakages through the water. The U-shape of the gate electrode around the silicon channel is in contact with the water and its charge density determines the ion distribution over the silicon channel. Accordingly the conductivity of the channel is modulated and a current between the source and drain electrodes is established. Further information about the water-gated FET, its fabrication process and characterization are given in the following chapters.

2.2. Band Diagrams of Metal-Semiconductor Junctions

The band diagram of a material is a plot which shows the important energy levels of the material such as the fermi level, intrinsic level, valence band and conduction band as a function of the distance throughout the material. When two different materials or two pieces of a same material with different doping concentrations are brought into contact, the behavior of these energy levels in the band diagram gives an idea about the characteristics of the resulting device [34].

When a metal and a semiconductor are in contact, the energy band of the semiconductor bends according to the work function of the metal and the doping type and concentration of the semiconductor. In Figure 2.5, the bending of the band diagrams of p-type and n-type semiconductors before and after contacting to a metal with high and low work functions is shown [35]. When the semiconductors are contacted to the metal and no voltage is applied, then the fermi levels of these two align. Other levels such as the valence and conduction bands bend near the contact, but they stay same through the bulk regions of the semiconductor. In the first and the last case of the figure, a Schottky barrier is formed and the resulting device behaves as a Schottky diode. However in the other two cases the contact is ohmic and can flow current in both directions through a low resistance. The formation of the Schottky barrier is desirable for rectifying purposes, whereas the ohmic contact is needed for the interconnections or the contact pads of the semiconductor devices.

2.2.1. Establishment of Ohmic Contact

In this work, the drain and source terminals of the transistor are formed through the evaporation of aluminum on top of lightly doped p-type single crystalline silicon. For the proper functioning of the transistor, the aluminum contacts must flow the current with low resistance in both directions, into the silicon and from the silicon. However as can be seen in part d of the Figure 2.5, the contact between the aluminum that has a low work-function and the lightly doped p-type silicon is not ohmic.

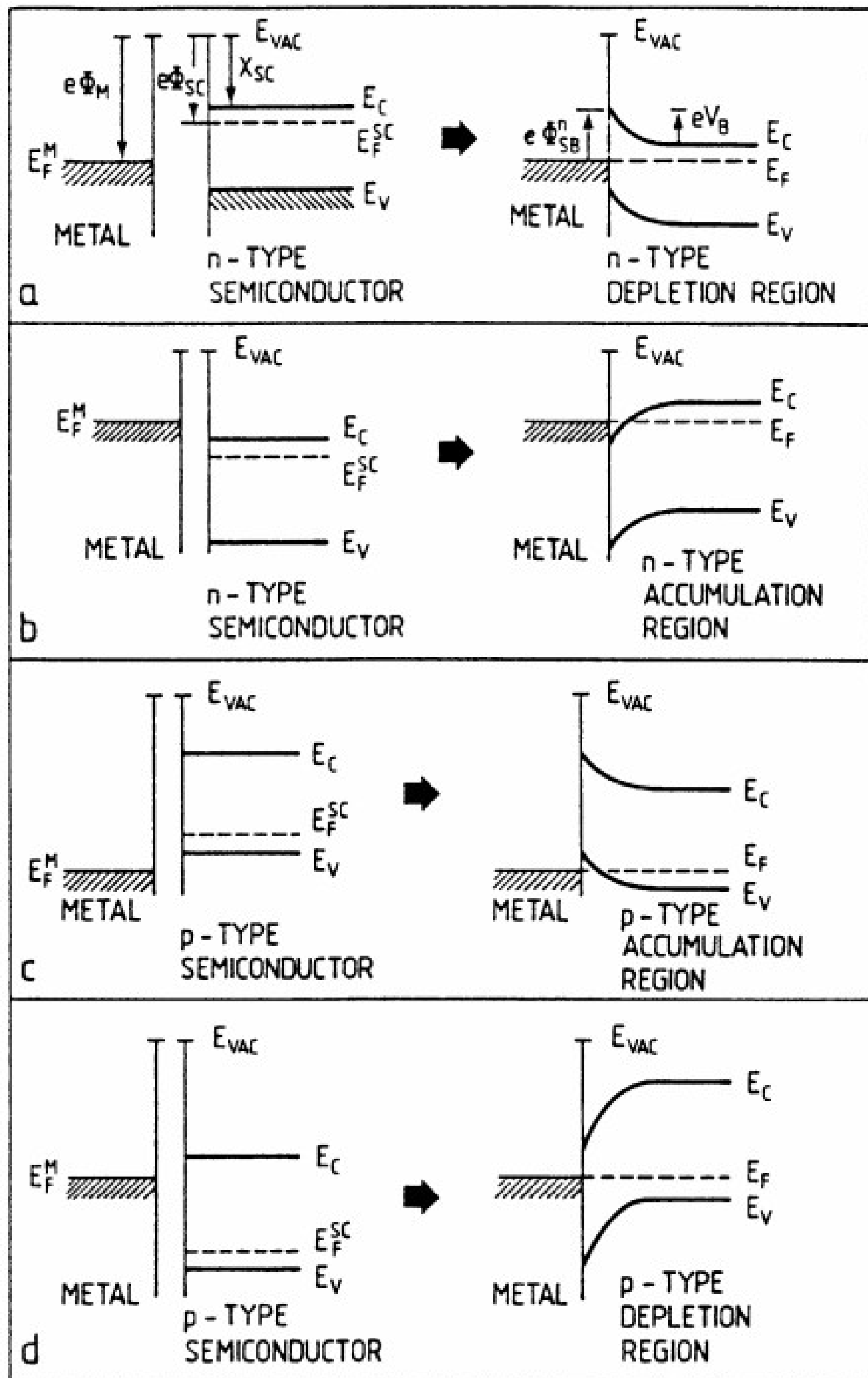


Figure 2.5. Band bending before and after the contact of (a) high work-function metal & n-type semiconductor (b) low work-function metal & n-type SC (c) high work-function metal & p-type SC (d) low work-function metal & p-type SC [35].

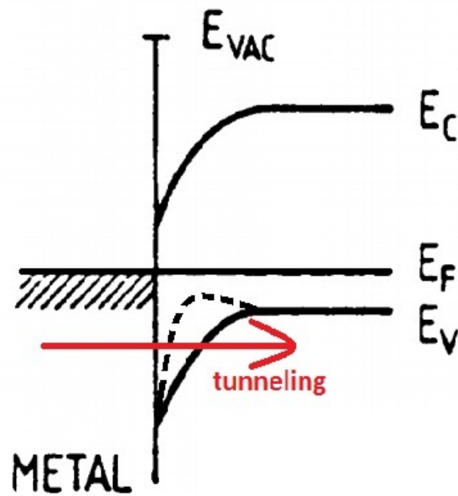
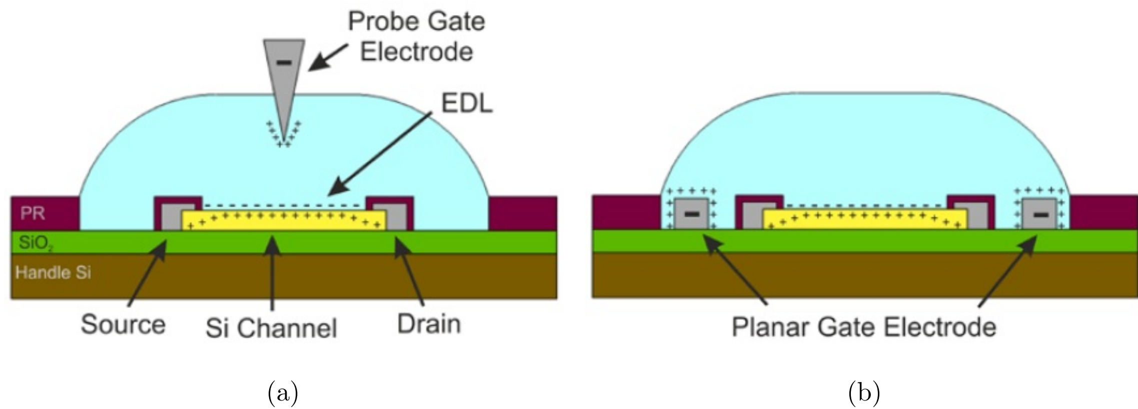


Figure 2.6. The band diagram after annealing (dashed line) that enables tunneling.

In such situations where the p-type silicon is contacted to a low work-function metal, an ohmic contact can be established by creating a thin highly-doped p^{++} region on the surface of the silicon under the metal [36], which provides a charge carrier transport system named as tunneling. Tunneling is a quantum mechanical phenomenon that refers to the motion of the particles through a barrier, through which they could not pass according to classical physics [37]. When the silicon wafer is annealed after evaporating aluminum on top of it, then some of the Al atoms diffuse into the silicon and since aluminum is a p-type dopant for the silicon, a p^{++} region is created right under the metal. With this method ohmic contacts are established.

3. STRUCTURE OF THE FABRICATED DEVICE

A brief presentation of the fabricated water-gated field effect transistor was given in Section 2.1.3 and the cross-sectional view of the transistor seen from the top view in Figure 2.4 can be found in Figure 3.1 for probe and planar gated structures. The transistor is built on top of a 145-nm SiO_2 layer which is placed on thick bulk silicon. Source and drain terminals are fabricated from aluminum evaporated to the both sides of the silicon channel. The length and width of the resulting channel are 500 μm and 10 mm respectively, which gives a W/L ratio of 20.



(a)

(b)

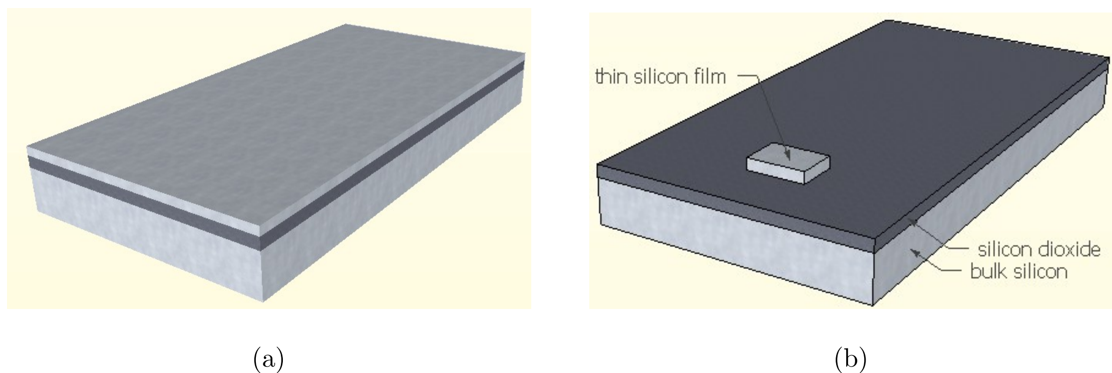
Figure 3.1. Structure of the transistor (a) using the probe gate and (b) planar gate.

The borders of the water droplet that will be dripped onto the channel is determined by an insulator pool. The areas of the drain and source electrodes that contact with the water are also covered by this insulator. For the probe gate design, an electrode is immersed into the water. A similar top gate design was previously reported in a SnS_2 channel transistor [38]. On the other hand for the planar gate design, the gate electrode is evaporated around the channel at the same time as the drain and source electrodes. Fabricating the gate electrode at the same layer with the drain and source electrodes was shown in a ammonia gas sensor built from graphene [39]. However it is not utilized as a WG-FET, but as a sensor. The fabrication process of the WG-FET designed in this work is explained in more detail in the following section.

3.1. Fabrication

3.1.1. Photolithography and Wet Etching of Silicon

The first fabrication step of the water-gated field effect transistor is the photolithography and wet etching of the silicon. The 12″ SOI wafer is first cut into small pieces such that two transistors can be fabricated on one piece. Then these pieces are cleaned and covered with photoresist (PR) using a spin coater. Also an adhesion promoter is used to improve the adhesion of the photoresist to the silicon surface. Following this, using the silicon mask, the samples are exposed to UV light and then brought into the photoresist developer for 1 minute. The samples are hard baked for 2 hours such that photoresist can stand the wet etchant as well.



(a) (b)

Figure 3.2. SOI wafer (a) before and (b) after the wet etching of silicon.

The channel region of the transistor is built through the wet etching of the 16-nm thin single crystalline silicon film as in the Figure 3.2. Isotropic silicon etchant, also called as the trilogy etch, is used to etch the silicon. It consist of nitric acid, water and ammonium fluoride ($126\,HNO_3 : 60\,H_2O : 5\,NH_4F$) [40]. The samples are put in this wet etchant for 40 seconds and then the photoresist is removed using acetone. The microscope image of the resulting silicon channel can be seen in Figure 3.3.

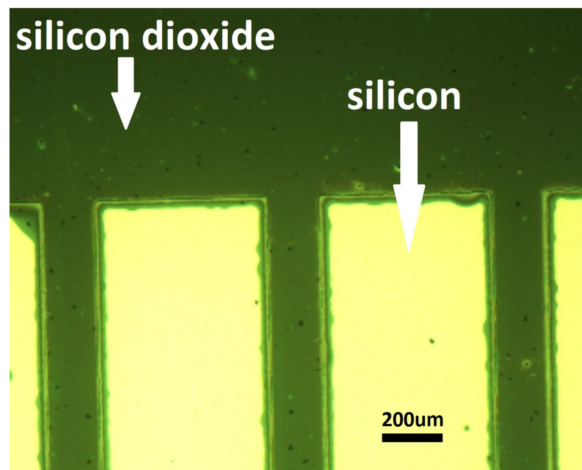


Figure 3.3. The micrograph of the sample after silicon etching.

3.1.2. Aluminum Evaporation

After the silicon etching, samples are placed in the vacuum chamber for aluminum evaporation. Then, 500 mg aluminum is put into a tungsten coil and a current of 40 A is applied through this coil to evaporate the aluminum. This operation is achieved in a pressure of 3×10^{-6} Torr to extend the mean free path. Mean free path is the average distance a particle can overtake until it hits another one [41]. Having a long mean free path is important, because the evaporated aluminum atoms can reach to the samples easier and more efficiently then. At the end of the aluminum evaporation, the samples are coated with aluminum that has a thickness of around 200 nm.

3.1.3. Photolithography and Wet Etching of Aluminum

Following the aluminum evaporation, the photolithography and wet etching of aluminum take place. The photolithography process is the same as the one of the silicon except that this time no hard bake is needed. Also the photoresist developer behaves as a selective etchant for aluminum, so no other wet etchant is necessary. When the samples are left in the PR developer, after 1 minute the photoresist is shaped and then aluminum starts to be etched. After around 20 minutes aluminum is also etched and the drain, source and gate electrodes are built as in Figure 3.4.

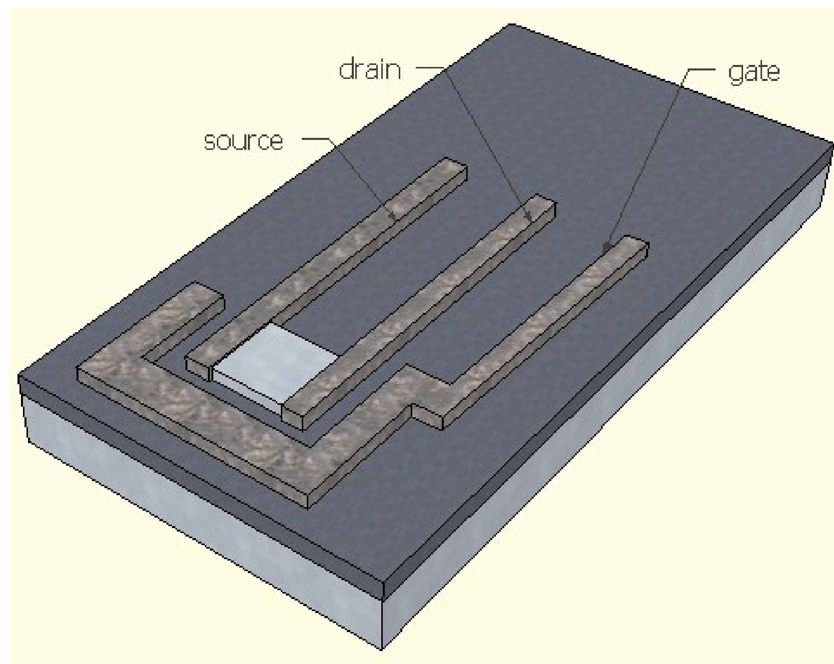


Figure 3.4. The sample after the wet etching of aluminum.

The micrograph of the sample after the wet etching of the aluminum can also be seen in Figure 3.5. The drain and source electrodes are not placed exactly up to the edges of the silicon, but 2 μm wider to decrease possible problems that may arise through misalignment of the masks.

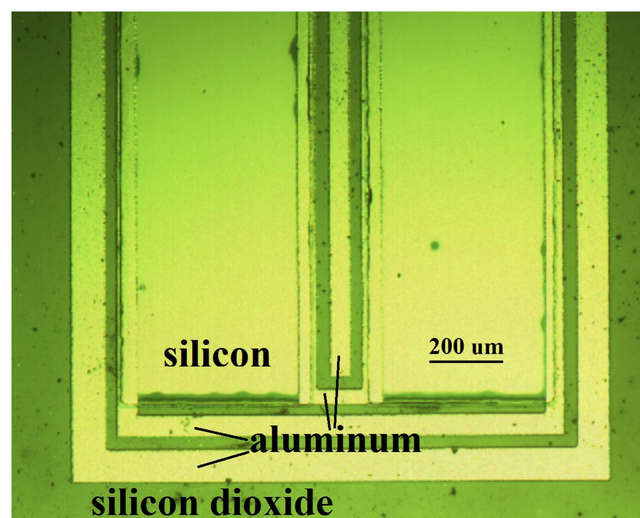


Figure 3.5. The micrograph of the sample after the wet etching of aluminum.

3.1.4. Thermal Annealing

After the aluminum electrodes are shaped on the silicon film, a thermal annealing step is needed to establish an ohmic contact. Thermal annealing is realized on a heater that uses four halogen lamps and is located in a vacuum chamber. During and after the annealing, a constant argon flow is provided to protect the materials from oxidation. The pressure is kept constant at 3 Torr.

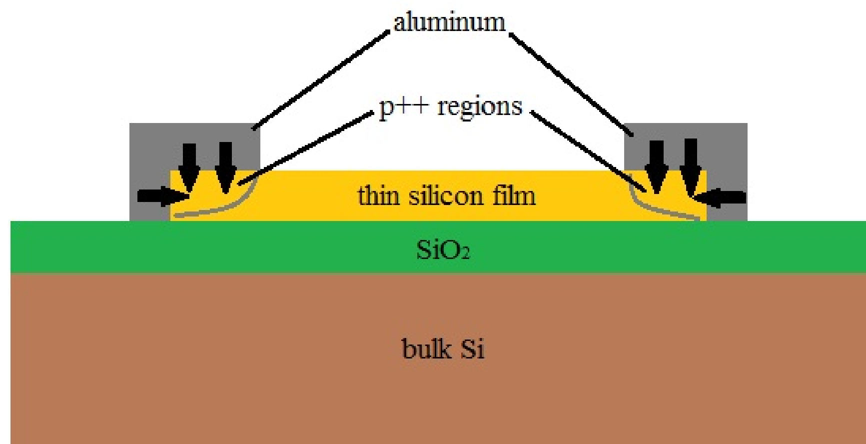


Figure 3.6. Diffusion of aluminum atoms into silicon during annealing.

After the sample is placed on the heater, halogen lamps are turned on for 15 minutes. In this duration the temperature firstly ramps up to 450° C and remains constant at that value. After 15 minutes is completed, halogen lamps are turned off and temperature slowly goes down for 1 hour. Then the sample is taken from the chamber.

As shown in Figure 3.6, aluminum atoms diffuse into silicon during annealing. Aluminum is a p-type dopant for silicon and this diffusion creates a p^{++} region under the metal. Thanks to this region and the tunneling phenomenon, the contact between the metal and semiconductor becomes ohmic in both directions.

3.1.5. Photoresist as Insulator Layer

After the annealing process, the third and last photolithographic mask of the design is used to shape the photoresist layer, which is used for insulating purposes. PR is coated on the drain and source electrodes where they contact the water droplet in order to prevent any leakage current through the water.

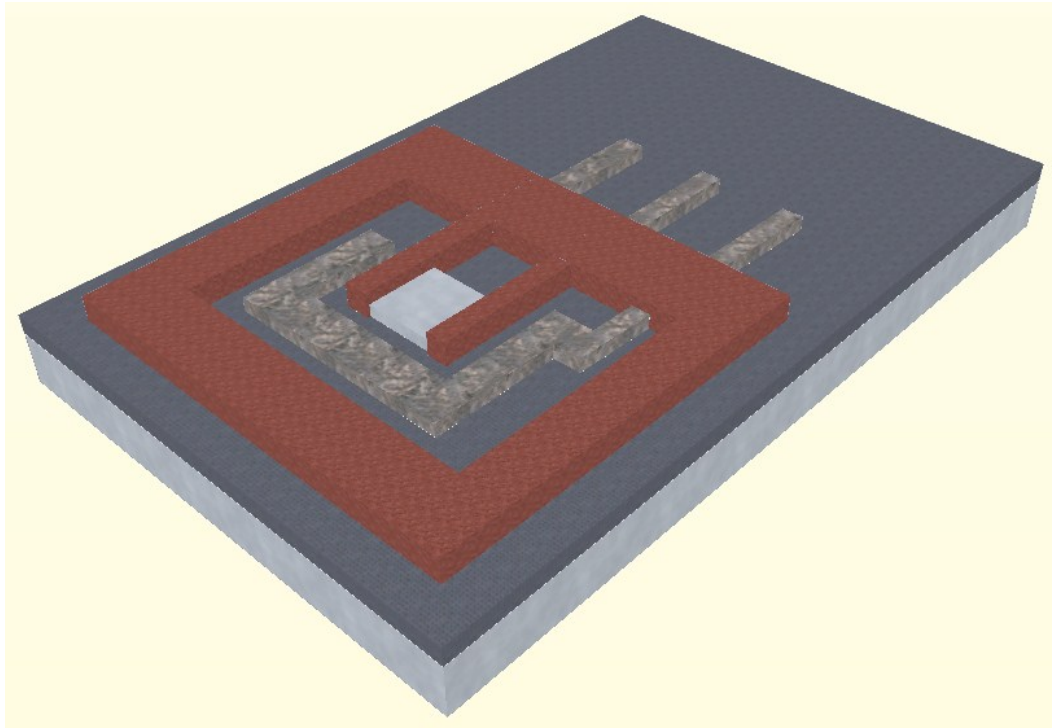


Figure 3.7. The sample after the photolithography of the photoresist.

Photoresist is also deposited around the gate electrode to build a small pool, where the water droplet can be placed. This final structure can be seen in Figure 3.7 and its microscopic image is in Figure 3.8. In the microscopic image, the insulating photoresist layer can be recognized from its reddish color. As can be seen, drain and source electrodes are covered with PR, whereas the PR on the gate electrode and semiconductor channel is removed such that they can contact to the water droplet.

Since the SiO_2 layer of the SOI wafer is very thin, the contacts to the electrodes should be taken carefully to avoid any deformation of that layer, since such a de-

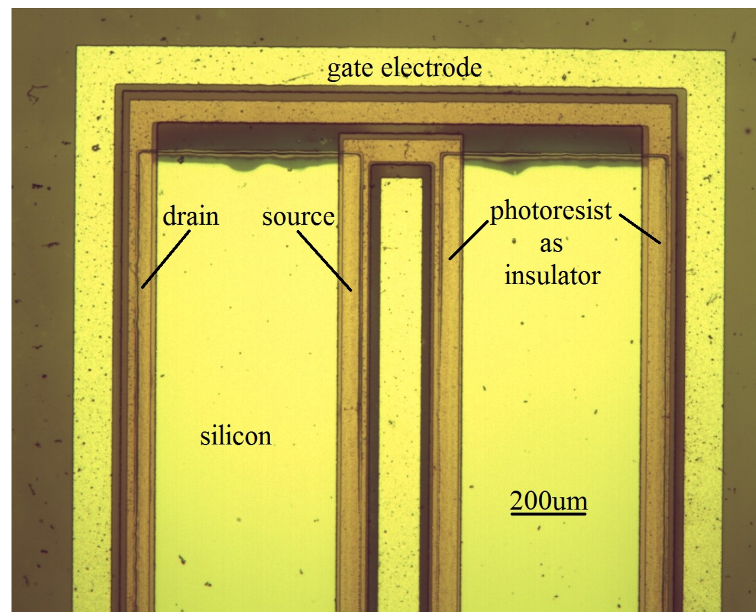


Figure 3.8. The micrograph of the final device.

formation can cause the device to have a contact to the bulk silicon, which would ruin the functioning of the transistor. For this reason, the contacts are made through silver-epoxy paint without touching the tungsten wires to the sample as can be seen in Figure 3.9.

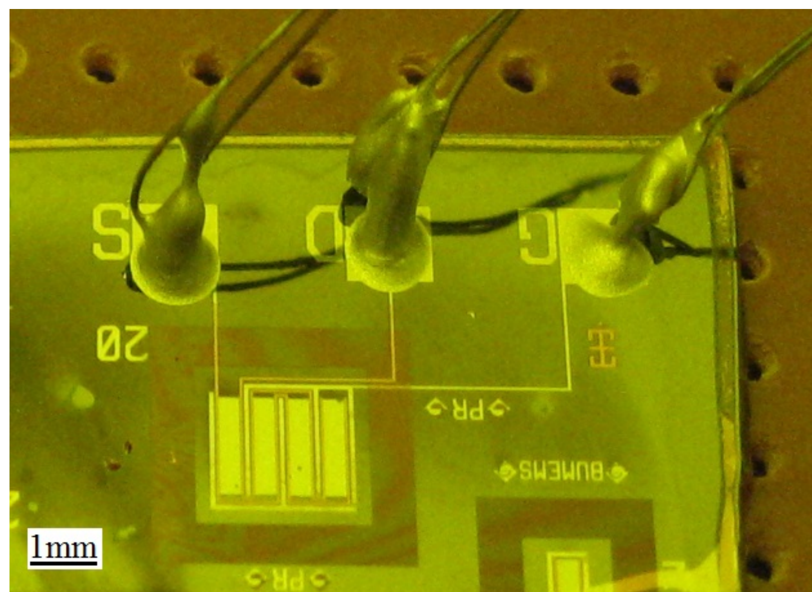


Figure 3.9. Final form of the transistor with silver-epoxy contacts.

4. MEASUREMENTS AND CHARACTERIZATION OF THE DEVICE

4.1. Measurement Equipment

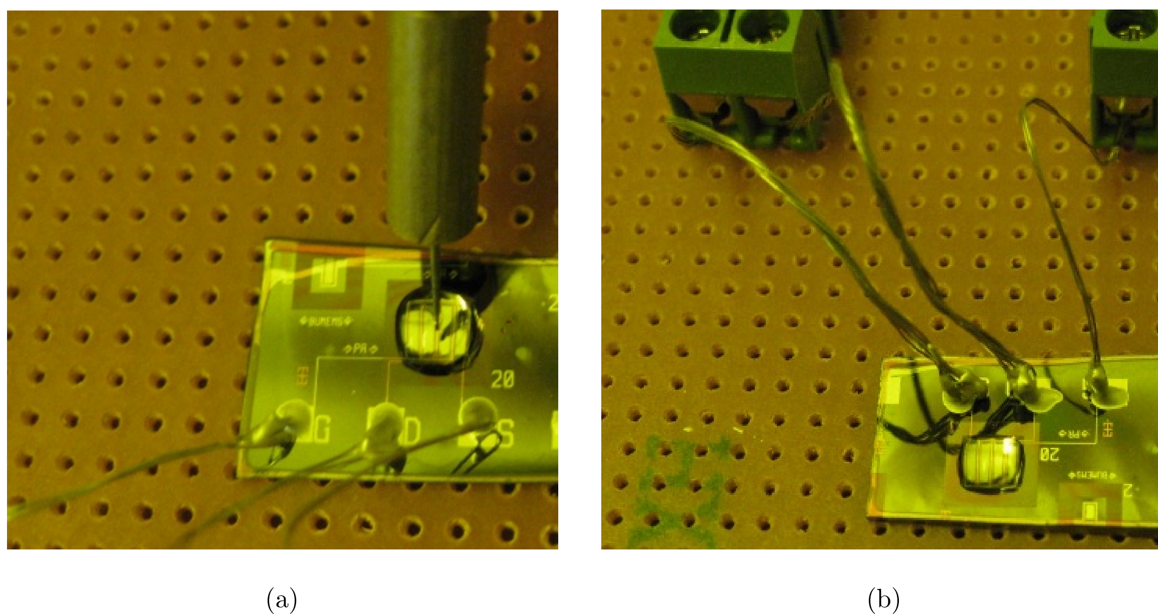
4.1.1. Keithley Characterization System

In this work, all measurements of the fabricated water-gated field effect transistors are done with Keithley 4200SCS semiconductor characterization system, which can be seen in Figure 4.1. It has four probes that can supply or measure current or voltage and these probes are connected to the drain, source, planar gate and probe gate electrodes of the transistor. The system has fast, normal and quiet modes for the measurement [42] and the quiet mode provides higher accuracy and lower noise.

Figure 4.1. Keithley 4200SCS semiconductor characterization system.

4.1.2. Probes

As mentioned in Section 3.1.5, connecting the transistor to the semiconductor characterization system was achieved carefully to avoid the deformation of the thin oxide layer. In Figure 4.2 these contacts can be observed. Three tungsten wires are brought close to the drain, source and planar gate electrodes but not touched. Silver epoxy paint is then used to contact the tungsten wires with electrodes. In addition, the probe gate electrode is directly connected to the semiconductor characterization system.



(a) (b)

Figure 4.2. Gate structure and contacts of the (a) probe and (b) planar gated transistors.

The gate structures of the probe gated and planar gated transistors can also be seen in Figure 4.2. Water droplet is dripped in the photoresist pool in both of the cases. In the first one, the planar gate electrode is not contacted to anywhere, instead the tungsten probe gate is immersed into the water. However in the second case no such external connection is needed, the planar gate electrode is used, which is more practical and compact.

4.2. Kelvin Contact Measurement

As explained in detail in the Section 3.1.4, a thermal annealing step is needed during the fabrication to establish ohmic contact between the metal and semiconductor. In order to be sure that the contacts become ohmic, a Kelvin contact measurement setup is annealed with the transistor as well. The cross-bridge Kelvin resistor structure [43] eliminates all the resistances during the measurement but the contact resistance.

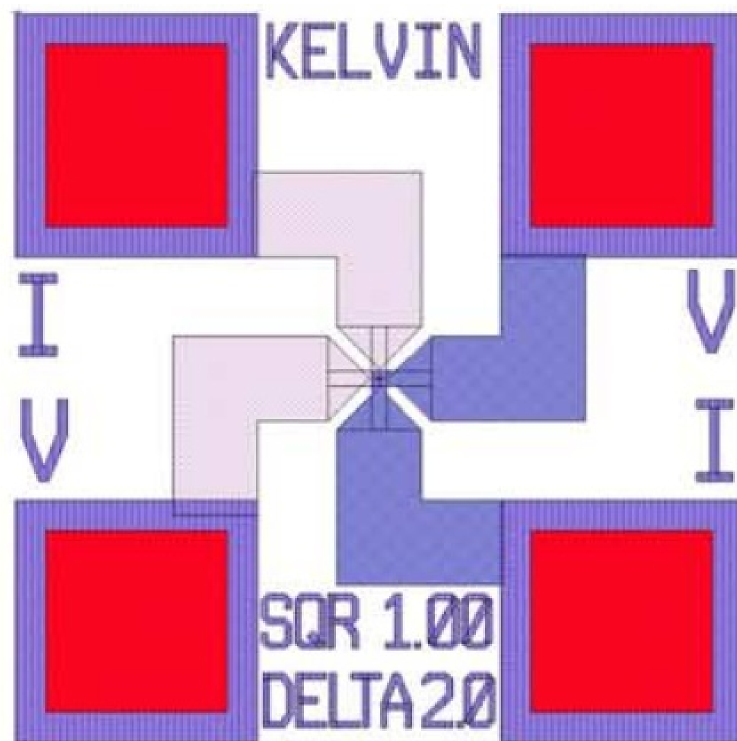


Figure 4.3. Kelvin contact measurement layout [43].

The layout of the cross-bridge Kelvin resistor structure is shown in Figure 4.3. This structure is fabricated and annealed with the transistor and then contacts are taken using silver epoxy paint as in the Figure 4.4.

Since this setup measures only the contact resistance between the metal and semiconductor [44], the value of the measured resistance can determine whether the contact is ohmic or not. The four pads of the Kelvin contact measurement structure

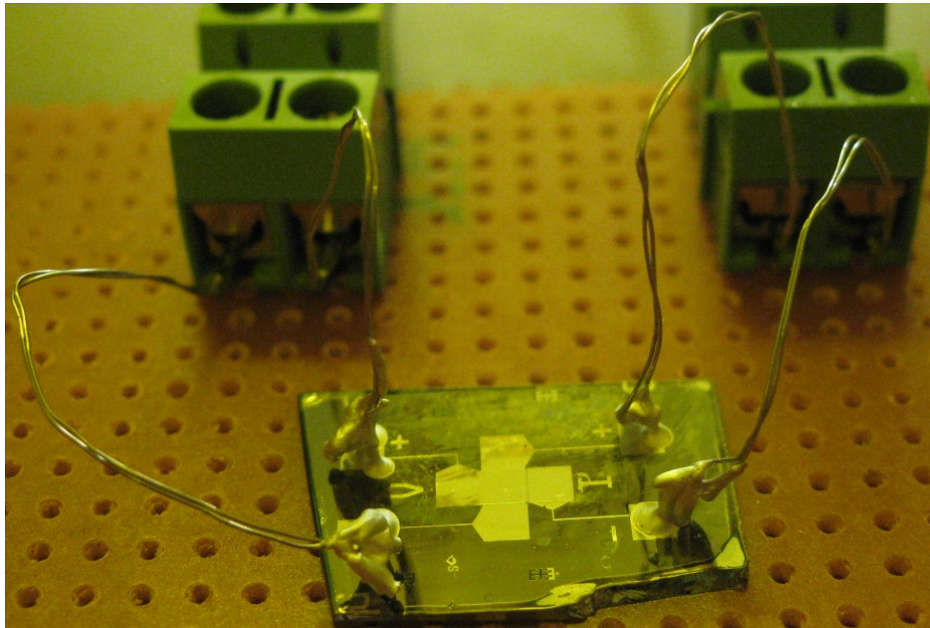


Figure 4.4. Kelvin contact measurement setup.

are connected to Keithley Characterization System and seven different measurements are done. The average resistance value resulting from these measurements is about 5 Ω, which means that the ohmic contact is achieved.

4.3. Measurements of the Probe and Planar Gate Design

The water-gated field effect transistor fabricated in this work is not only characterized using the planar gate, but also the probe gate like the usual WG-FET's available. Since the silicon used in the channel region is p-type, negative voltages are applied to the transistor. A potential difference of 1.23 V between any terminals must have been avoided to prevent the hydrolysis and thanks to the high double layer capacitance the transistor operates under 0.7 V well. In addition to the $I_{\mathrm{sd}} - V_{\mathrm{sd}}$ curve, on which the transistor behavior is observed, $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curves for two different V_{sd} values are also measured to obtain some device characteristics like the threshold voltage and on-off ratio. In Figure 4.5 the transistor behavior of the probe gated WG-FET is seen. It has a maximum drain current about $I_{\mathrm{sd}} = 100\mu\mathrm{A}$. In Figures 4.6 and 4.7 the $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curves are shown with $V_{\mathrm{sd}} = -0.07\mathrm{V}$ and $V_{\mathrm{sd}} = -0.7\mathrm{V}$ respectively.

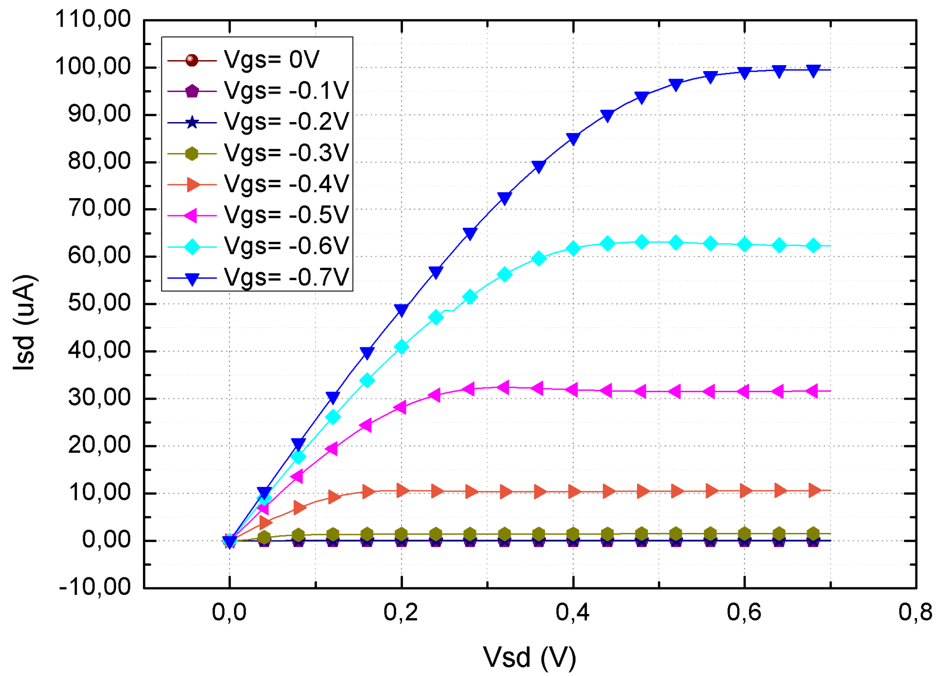


Figure 4.5. $I_{\text{sd}} - V_{\text{sd}}$ curve of the probe gate design.

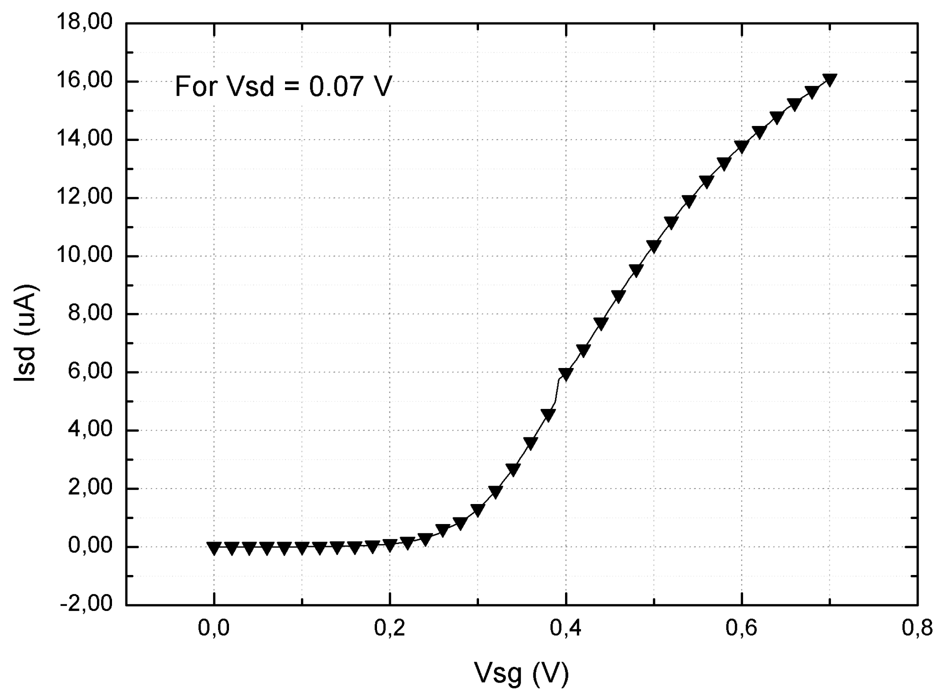


Figure 4.6. $I_{\text{sd}} - V_{\text{sg}}$ curve of the probe gate design for $V_{\text{sd}} = -0.07\text{V}$.

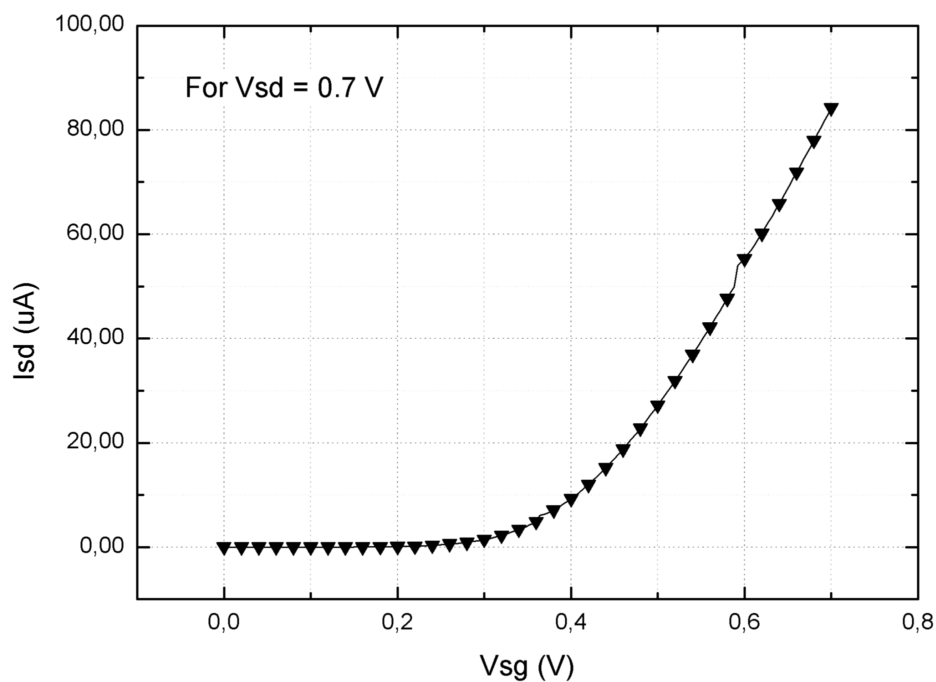


Figure 4.7. $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curve of the probe gate design for $V_{\mathrm{sd}} = -0.7\mathrm{V}$.

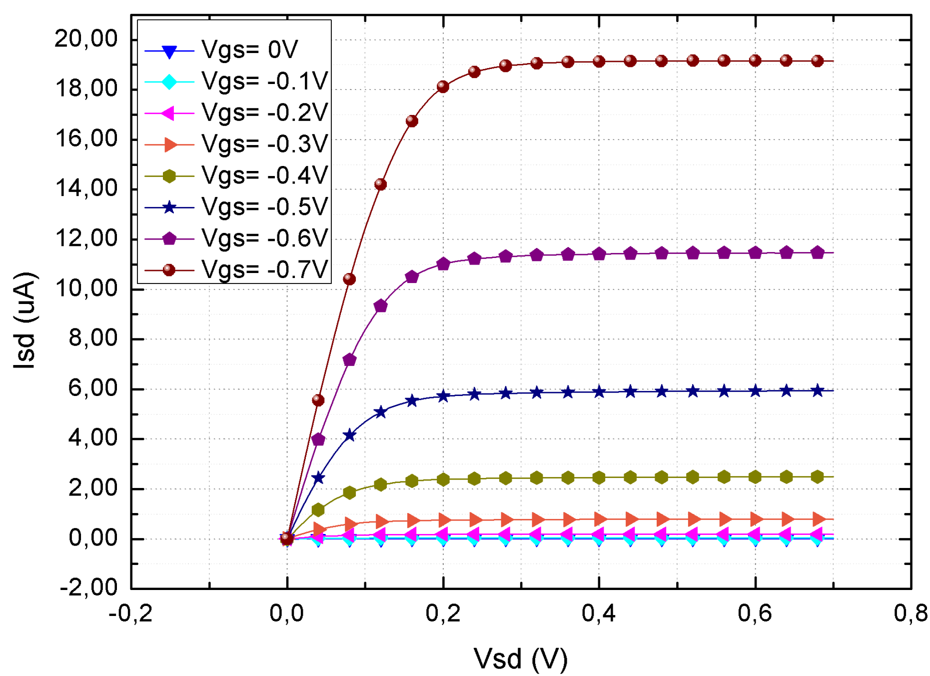


Figure 4.8. $I_{\mathrm{sd}} - V_{\mathrm{sd}}$ curve of the planar gate design.

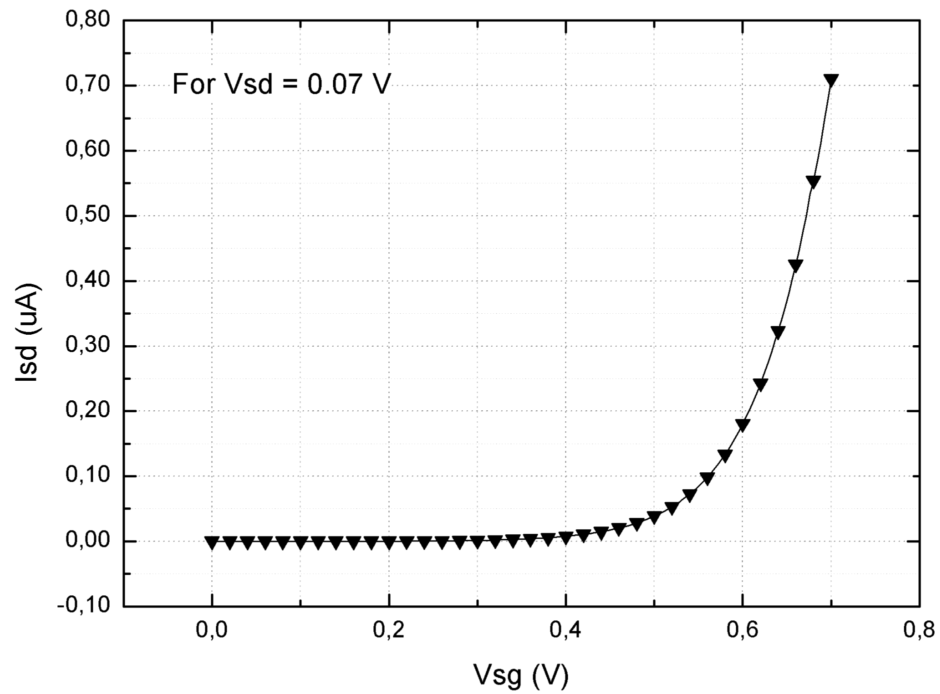


Figure 4.9. $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curve of the planar gate design for $V_{\mathrm{sd}} = -0.07\mathrm{V}$.

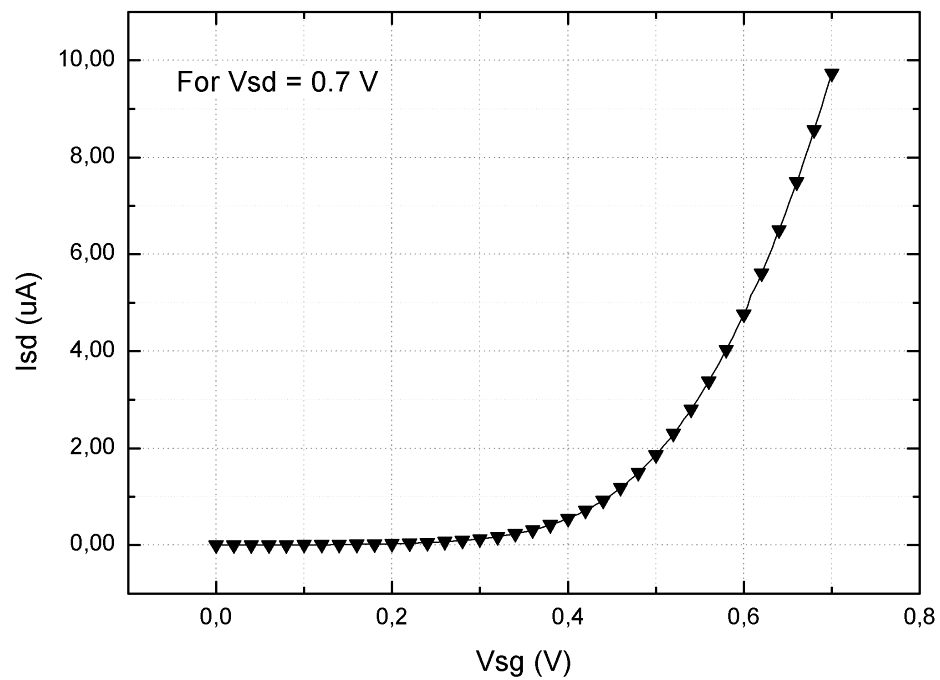


Figure 4.10. $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curve of the planar gate design for $V_{\mathrm{sd}} = -0.7\mathrm{V}$.

The same measurements were made for the planar gated design as well. In Figure 4.8 the transistor behavior of the planar gated WG-FET is seen. It has a maximum drain current about $I_{\mathrm{sd}} = 20\mu\mathrm{A}$. In Figures 4.9 and 4.10 the $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curves are shown with $V_{\mathrm{sd}} = -0.07\mathrm{V}$ and $V_{\mathrm{sd}} = -0.7\mathrm{V}$ respectively.

4.4. Transistor Parameters

4.4.1. On-off Ratio

The definition and calculation method of the on-off ratio was given in the Section 2.1.2. Accordingly the on-off ratios of the two types of the WG-FET can be calculated. The on-off ratio is defined as

$$\text{on/off ratio} = \frac{I_{\mathrm{d,V_{g_{max}}}}}{I_{\mathrm{d,V_{g_{min}}}}} \tag{4.1}$$

and when the corresponding values are inserted into the Equation 4.1, the on-off ratio of the probe gated design is found as

$$\text{on/off ratio(probe gated)} = 232000. \tag{4.2}$$

Using the same method, the on-off ratio of the planar gated design is also found as

$$\text{on/off ratio(planar gated)} = 2150. \tag{4.3}$$

4.4.2. Threshold Voltage

Determining the threshold voltage is explained thoroughly in the Section 2.1.2 and the threshold voltages of the probe and planar gated WG-FET's will be found with this method. Firstly, the linear regions in the $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curves of the probe and planar gated WG-FET's with $V_{\mathrm{sd}} = -0.07\mathrm{V}$ are extrapolated as can be seen in Figures 4.11 and 4.12 respectively.

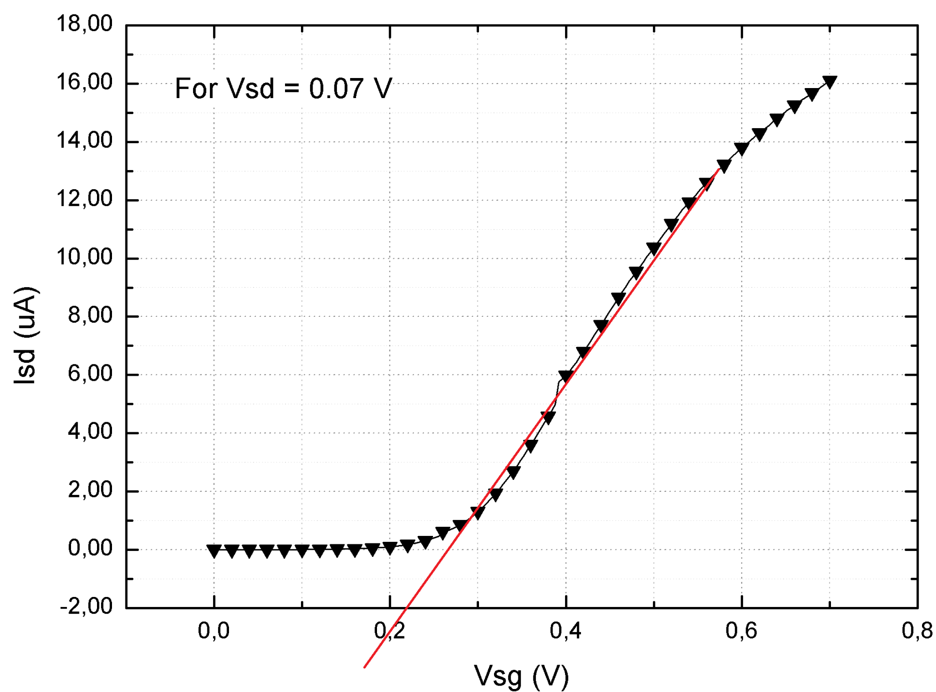


Figure 4.11. Extrapolation of the $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curve in probe gated design.

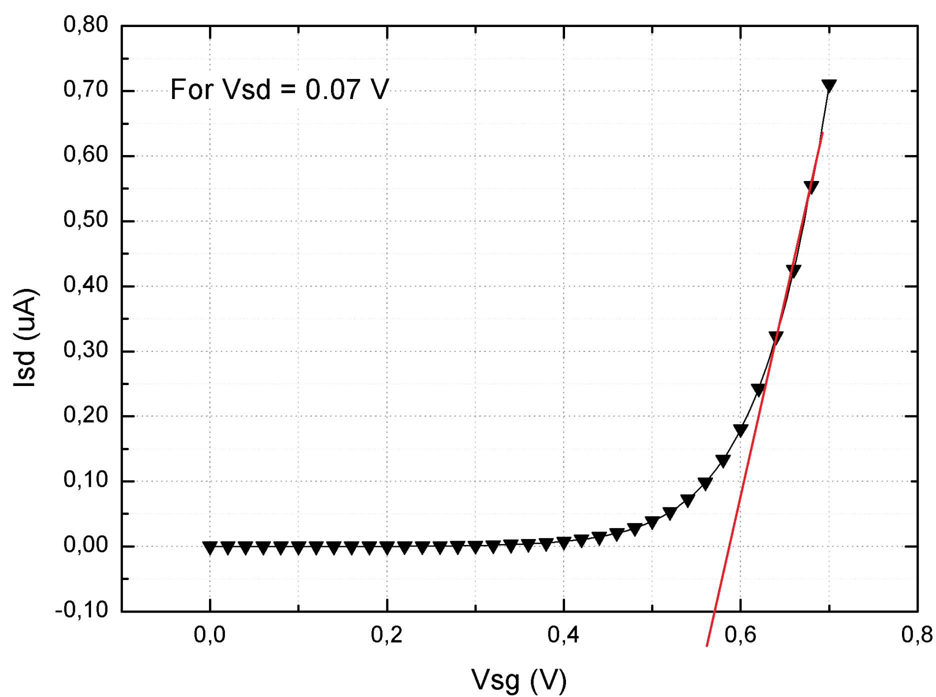


Figure 4.12. Extrapolation of the $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curve in planar gated design.

The red line in Figure 4.11 intersects the x-axis at 0.276 V and the current value corresponding to this voltage value is 789.93 nA. Now this current value is carried out to the other $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curve and its corresponding voltage gives the threshold voltage, which is $V_{\mathrm{th}} = 0.27\,V$ for the probe gated transistor.

The same procedure is realized for the planar gated transistor as well. The red line in Figure 4.12 intersects the x-axis at 0.584 V and the current value corresponding to this voltage value is 141.98 nA. This value is also carried out to the other $I_{\mathrm{sd}} - V_{\mathrm{sg}}$ curve and its corresponding voltage value determines the threshold voltage, which is $V_{\mathrm{th}} = 0.31\,V$.

4.4.3. Comparison of the Gate Structures

As all the measurements indicate, both the probe gated and planar gated WG-FET's are operating well. A brief comparison of the transistor parameters of them can be seen in Table 4.1.

Table 4.1. Comparison of probe and planar gated WG-FET's.

Transistor Parameter	Probe-gated WG-FET	Planar-gated WG-FET
max. drain current	99.49 μA	19.15 μA
on-off ratio	232000	2150
threshold voltage	0.27 V	0.31 V

As represented in Table 4.1, the threshold voltage values are very close to each other. However there is a huge difference between the on-off ratios. The on-off ratio of the probe gated transistor is about 100 times greater than the one of the planar gated transistor. The main source of this big difference is the off-currents of the transistors, because the on-current of the probe gated transistor is only five times greater than the one of the planar gated transistor. This means that the off-current of the planar-gated transistor is about 20 times greater than the one of the probe gated transistor. This

big difference can be explained by the distance of the probe and planar gate electrodes to the semiconductor channel. The distance of the probe gate to the channel is in millimeter range, whereas the one of the planar gate is only 20 μm. Being so close to the channel increases the gate leakage current and consequently the off-current.

5. CONCLUSIONS AND FUTURE WORK

In this project, a water-gated field effect transistor with planar and probe gates is fabricated, analyzed and characterized. 16-nm thick single crystalline silicon is used as the channel material. A water droplet is placed directly on the semiconductor channel and an electrical double layer is formed there, which is utilized as the gate insulator. It is advantageous to use the EDL as the gate insulator since it is uniform, pin-hole free, very thin and has a high dielectric constant. Thanks to this property the transistor functions below 0.7 V.

Two different gate structures are used in order to compare the novel planar gate design with the usual probe gate structure. The characteristics of the planar gated WG-FET are not as good as the probe gated transistor, but they are still much better than the characteristics of its organic planar gated competitors. Also the planar gated WG-FET fabricated in this project is prospective for improvement.

The smaller on-off ratio of the planar gated transistor arises from the higher off-current. The reason for the high off-current is the position of the planar gate. Since it is very close to the channel, the gate to source leakage current becomes higher compared to the probe gated design. As a future work this problem can be solved. Already a new mask set is prepared with different gate-to-channel distances, gate widths and gate shapes to optimize the structure of the planar gate.

The work achieved in this project is very promising in terms of future applications and compatibility with other systems. For example, the usage of the water droplet as the gate insulator enables the WG-FET to find itself a place in biomedical applications. By changing the content of the liquid that is dripped on the channel or by implementing specific molecules on the channel, the WG-FET can be used as a biosensor. In addition to that, if not used as a sensor, it can be used as a circuit element connected to a biosensor because of its compatibility with liquid environment.

Although the transistor is functioning well by itself, combining it with other circuit elements or other fabricated WG-FET's in this work enables us to understand its behavior more precisely. Several simple analog or digital circuits can be created using this transistor in the future.

Another possible future work to be achieved with this transistor is microfluidic channel integration. When a circuit with more transistors are built in the future, it wouldn't be practical to drip water on top of each transistor. Instead, a microfluidic channel passing through all the transistors on a die would simplify the progress. Also a microchannel would eliminate the problem that the water droplet dries out after some time.

APPENDIX A: LAYOUT IMAGES OF THE WG-FET

In the following pages, the layout designs of the WG-FET are presented. In addition the to whole layout design, separate masks for each layer are also shown.

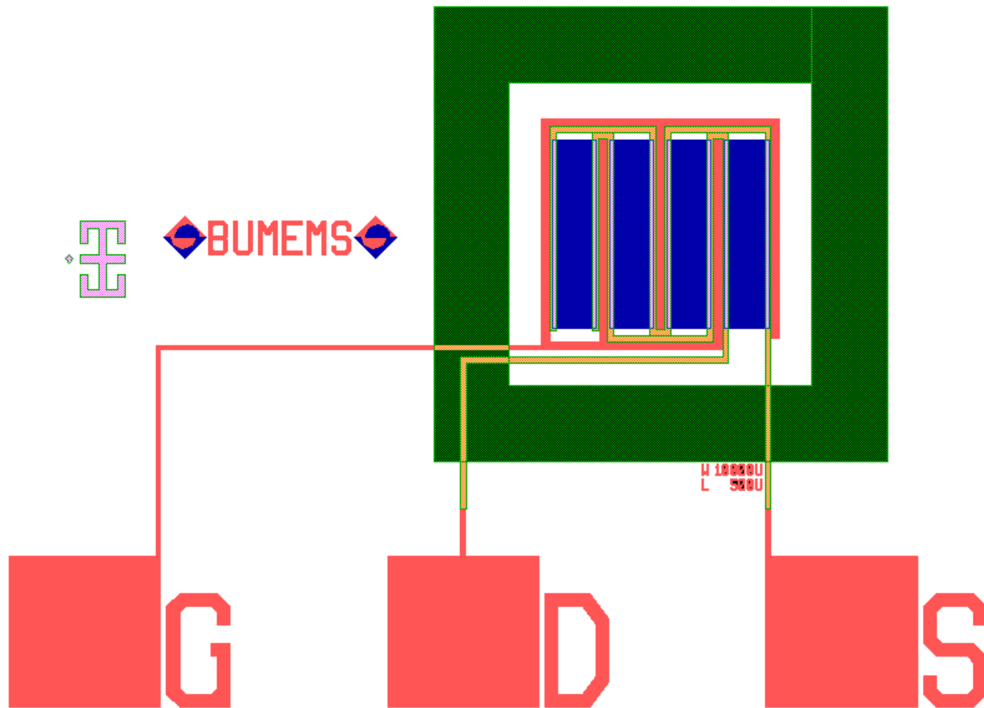


Figure A.1. Layout design of WG-FET.

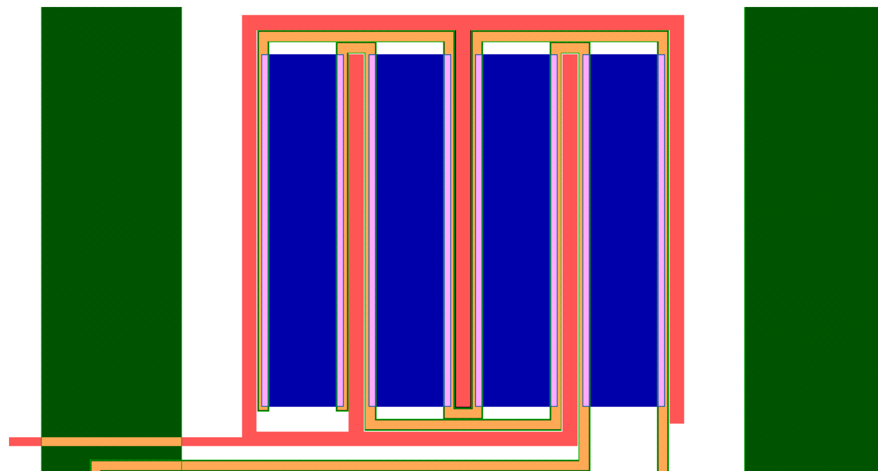


Figure A.2. Closer view of the layout design of WG-FET.

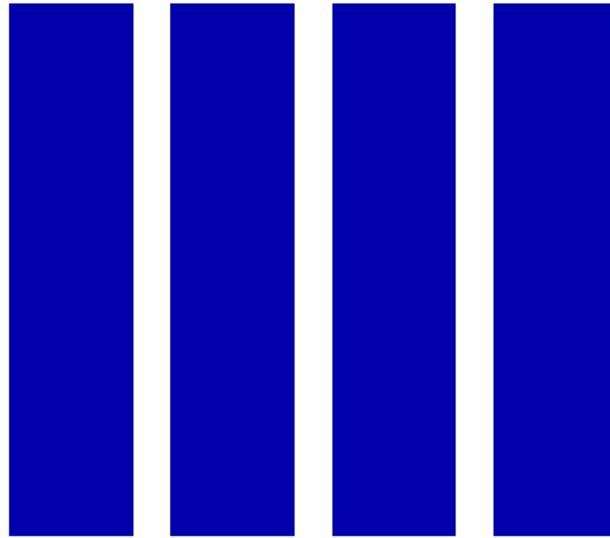


Figure A.3. Layout design of silicon mask.

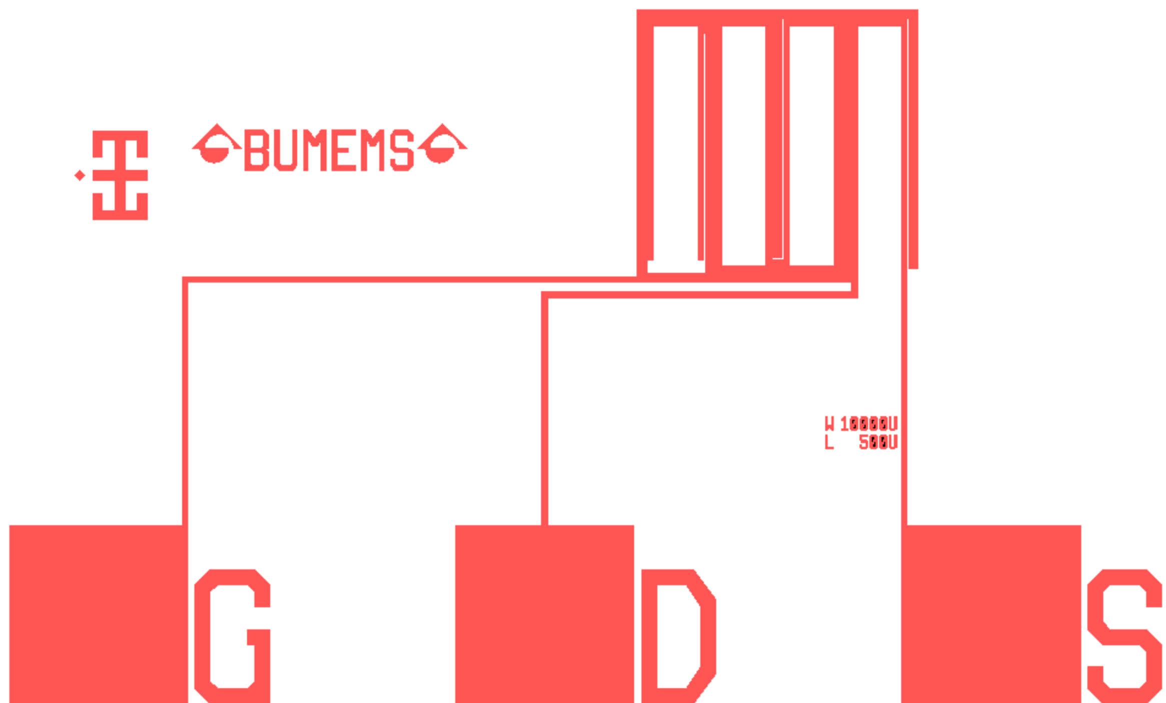


Figure A.4. Layout design of aluminum mask.

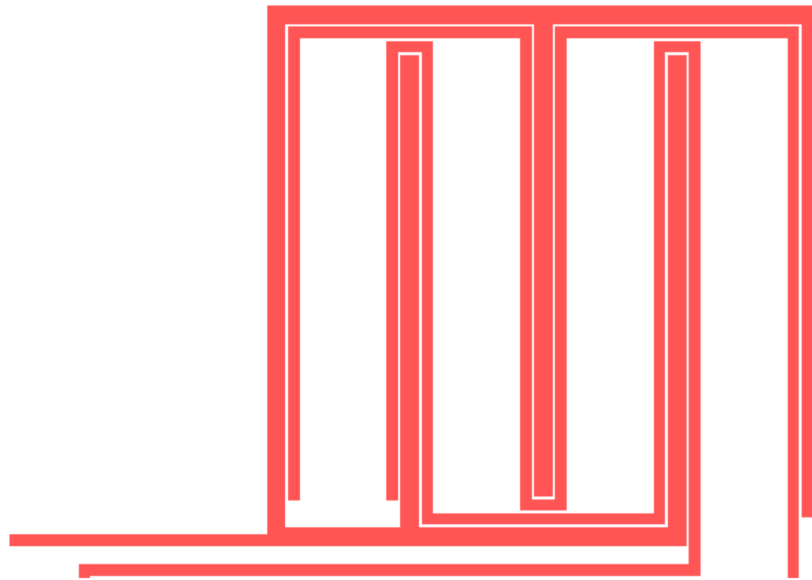


Figure A.5. Closer view of the layout of aluminum mask.

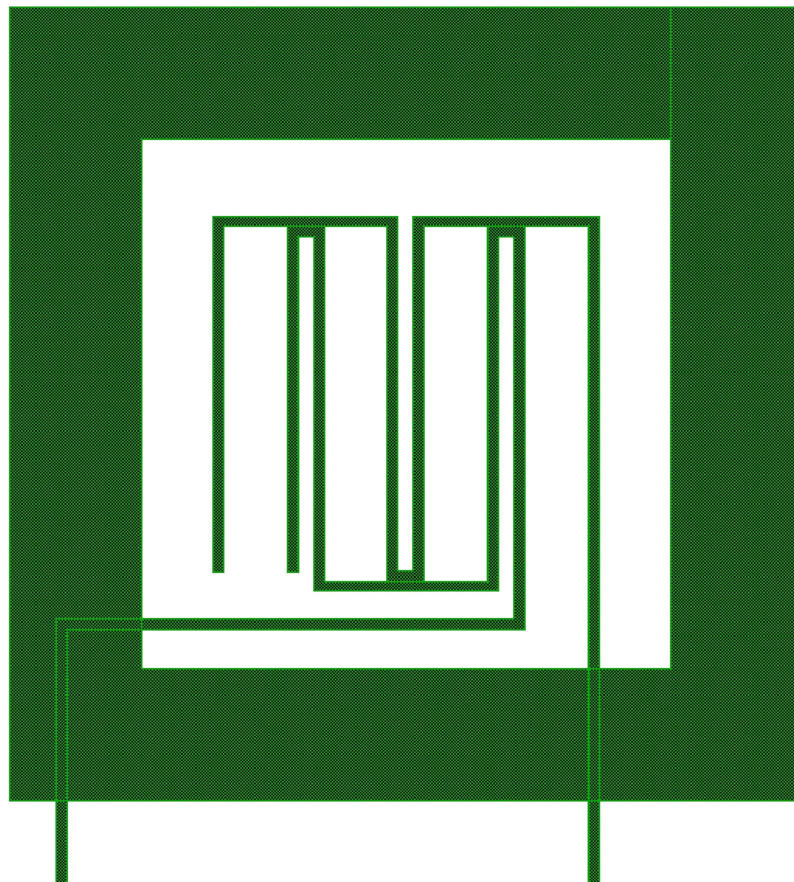


Figure A.6. Layout design of photoresist mask.

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