CMOS OSCILLATOR DESIGN BY USING A METAMATERIAL-BASED SPLIT RING RESONATOR

by

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To memory of my dear grandfather...

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ABSTRACT

CMOS OSCILLATOR DESIGN BY USING A METAMATERIAL-BASED SPLIT RING RESONATOR

High purity oscillators are of great importance in communication, radar, or medical instrumentation systems. In today's integrated circuit technology, low quality factor of inductors and capacitors define the limits of the phase noise of oscillators.

In order to demonstrate an alternative to low quality resonators, this work presents a design of complementary cross coupled oscillator by using a metamaterial-based Split Ring Resonator (SRR). SRRs having unique properties can exhibit very high quality factors which enable the design of low phase noise low power oscillator. Prior to oscillator design in this document, a lumped element model of SRR is also provided and verified with the measurement results. For demonstration, the proposed complementary cross coupled oscillator by using SRR is designed using 180nm Silicon-On-Insulator (SOI) process which operates at 1.8GHz center frequency. Post-layout simulation results show that the oscillator phase noise is -179.5dBc/Hz and -180.8dBc/Hz at 100kHz and 1MHz offset frequencies, relatively. The total power consumption is 8.1mW at $1.8V$ supply voltage.

ÖZET

METAMALZEME TABANLI AYRIK HALKA REZONATÖRÜ İLE CMOS OSİLATÖR TASARIMI

Yüksek saflıkta osilatörler, iletişim, radar veya tıbbi enstrümantasyon sistemlerinde büyük önem taşırlar. Günümüzün entegre devresi teknolojisinde, düşük kalite faktörlü endüktörler ve kondansatörler, osilatörlerin en düşük faz gürültüsünün sınırlarını belirlemektedirler.

Bu çalısma, düşük kaliteli rezonatörlere bir alternatif göstermek amacıyla, metamalzeme tabanlı Ayrık Halka Rezonatörü (SRR) kullanılarak tasarlanan bütünleyici çapraz bağlı bir osilatörü sunmaktadır. Eşsiz metamalzeme özelliklerine sahip olan SRR'lar çok yüksek kalite faktörleri gösterebildikleri için düşük faz gürültülü ve düşük güçlü osilatör tasarımını mümkün kılabilirler. Bu dökümanda osilatör tasarımından önce, SRR'nin toplu öğeli eleman modeline yer verilmiştir ve ölçüm sonuçları ile doğrulanmıştır. Örnek olarak, SRR'lı bütünleyici çapraz bağlı osilatör 180nm Yalıtkan Üstü Silisyum (SOI) işlemi kullanılarak tasarlanmıştır ve 1.8GHz merkez frekansında çalışır. Çizim sonrası simülasyon sonuçları osilatör faz gürültüsünün 100kHz ve 1MHz sapma frekanslarında sırasıyla -179.5dBc/Hz ve -180.8dBc/Hz olduğunu gösteriyor. Toplam güç tüketimi 1.8V besleme geriliminde 8.1mW olmuştur.

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A	Surface area
$BW_{-3\text{dB}}$	−3dB Bandwidth
C	Capacitor *or* Capacitance
C_g	Gap capacitance
C_{db}	Small signal drain-bulk capacitance of a MOS transistor
C_{gd}	Small signal gate-drain capacitance of a MOS transistor
C'_{ox}	Gate oxide capacitance of a MOS transistor
C_s	Surface capacitance
C_{SRR}	Total capacitance of split ring resonator
F	Empirical fitting factor
f	Frequency
f_0	Resonant frequency *or* oscillation frequency
f_c	Corner frequency
g	Gap width of split ring resonator
G_m	Transconductance of a cross coupled pair
g_m	Transconductance of a transistor
GND	Ground connection
G_{osc}	Equivalent conductance of an oscillator
G_p	Equivalent parallel conductance
h	Height of any material
I_{BIAS}	Bias current
i_d	Small signal drain current of a transistor
I_D	DC drain current of a transistor
I_{TANK}	Peak current value of a resonator at resonance
i_x	Test current
L	Inductor *or* Inductance
L_{SRR}	Total inductance of split ring resonator
$L(\omega_m)$	Phase noise of an oscillator at a given offset frequency

M_i	Any MOS transistor with index i
n	Coupling coefficient of transformer
P_{diss}	Dissipated power
P_{sig}	Ouptut signal power
Q	Quality factor
Q_T	Quality factor of tank
R	Radius of split ring resonator
R_L	Loss of unit length inductor
R_{osc}	Equivalent resistance of an oscillator
R_p	Equivalent parallel resistance
R_{pair}	Equivalent resistance of a differential cross coupled transistor pair
R_{shu}	Substrate loss
R_{SRR}	Total loss of split ring resonator
TL_i	Any transmission line with index i
TF_i	Any transformer with index i
V_{DD}	Supply voltage
V_{gs}	Small signal gate-source voltage of a transistor
V_{GS}	DC gate-source voltage of a transistor
V_{OUT+}	Output voltage (plus node)
V_{OUT-}	Output voltage (minus node)
V_{OV}	Overdrive voltage of a transistor
V_T	Threshold voltage of a transistor
V_x	Test voltage
w	Metal width
w_0	Resonant frequency in radians
$(\frac{W}{L})_N$	Aspect ratio of a NMOS transistor
$(\frac{W}{L})_P$	Aspect ratio of a PMOS transistor
$\Delta\omega_0$	Offset frequency
ε	Permittivity

ε_0	Free space of permittivity
ε_r	Dielectric constant of any material
μ	Permeability
μ_0	Free space of permeability
μ_n	Electron mobility

LIST OF ACRONYMS/ABBREVIATIONS

ADS	Advance Design System
BW	Bandwidth
CMOS	Complementary Metal-Oxide Semiconductor
CSRR	Complementary Split Ring Resonator
CMRR	Common Mode Rejection Ratio
C.Xcoupled	Complementary Cross Coupled
DC	Direct Current
EM	Electro-Magnetic
FBAR	Film Bulk Acoustic Resonator
FET	Field-Effect Transistor
FOM	Figure of Merit
FR4	Flame Retardant 4
IC	Integrated Circuit
IOT	Internet-of-things
LC	Inductor-Capacitor
LHF	Left Handed Material
MOS	Metal-Oxide Semiconductor
NMOS	n-Channel Metal-Oxide Semiconductor
NRMGC	Negative Resistance Multiple-Gate Circuit
PMOS	p-Channel Metal-Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
PSS	Periodic Steady State
RF	Radio Frequency
RLC	Resistor-Inductor-Capacitor
SAW	Surface Acoustic Wave
SOI	Silicon-On-Insulator
SRR	Split Ring Resonator

1. INTRODUCTION

Oscillators are signal generating circuits which constitute a substantial part of integrated circuit blocks in analog, digital and mixed-signal designs. They provide periodic signals for timing in digital circuits and translate frequency in radio frequency (RF) circuits. Thus, being an important part of the main blocks of electronic systems, they have been used in many areas such as wireless communication [1–4], microprocessors [5] and sensor applications [6, 7]. Especially, internet-of-things (IOT) applications are anticipated to substantially increase the wireless sensors deployment [8] which also increases the requirement of more communication channels. This results in increasing demand of low phase noise and low power consumption year by year. For oscillators, it is well known that providing low phase noise with a very low power consumption has been a challenging task with the frequency selective networks used. These frequency selective networks are critical part of oscillators since the quality factor of such networks directly affect the phase noise performance. To overcome this obstacle, new methods have been proposed and demonstrated to achieve low phase noise and low power consumption oscillator designs [9–14]. Although new provided methods enhance the performance of oscillators, the low quality factor of the frequency selective networks will always be a limiting factor for phase noise performance of oscillators.

As frequency selective networks, inductor-capacitor (LC) resonators are among one of the most popular ones, and thus LC cross coupled oscillators. There are various LC cross coupled oscillator designs in literature [15–17]. The reason of their popularity comes from simple structures of LC resonators and the availability of inductors and capacitors in today current integrated circuit (IC) processes as well as their low-cost. However, these oscillators suffer form low quality factors of IC inductors and capacitors. Thus, efforts have been focused on new ways of increasing the quality factor of resonators [18–20].

So far, several high quality resonator oscillators have been proposed in literature. Surface Acoustic Wave (SAW) resonator oscillators are proposed in [21–23]. In

addition, thin Film Bulk Acoustic Resonator (FBAR) oscillators have also been so popular [24,25]. However, in this work, to overcome this limiting factor, metamaterial-based resonators have been adopted as they are low-cost and high quality resonators. Metamaterials, also called left handed materials (LHF), exhibit negative index of refraction as experimentally verified in [26]. They interact with electro-magnetic waves and can be used used to control or detect them. It is possible to configure new geometrical designs having negative permeability μ and negative permittivity ε which can not be realized by positive index materials. With this unique properties, they are used in many applications such as telecommunication, energy harvesting, sensing, and medical instrumentation [27,28]. Among these designs, Split-Ring Resonator (SRR) or its dual Complementary Split-Ring Resonator (CSRR) are two widely used metamaterial-based resonators. The planar structure of SRR exhibits a negative real part of μ, whereas its counterpart shows a negative real part of ε [29]. This negative property of SRR and CSRR help them confining high electro-magnetic (EM) energy at resonant frequency without a high loss resulting in high quality factor resonators. This high quality factor makes these resonators are popular among oscillator designs [29,30].

In literature, there are few works similar to the one in this document. An oscillator is designed in [29] with a differential loaded on chip CSRR with a Figure of Merit (FOM) of -182.4dBc/Hz. Although this work shows that an on-chip metamaterial based resonator can have a high quality factor, its resonant frequency is at a very high frequency of 96GHz. This is an expected result as the smaller the size of the resonator, the resonant frequency gets higher. The design uses a cross coupled architecture in an IC technology.

There are also other works using SRR or CSRR in oscillator designs which are operating at around 5.5GHz using discrete components [31]. Another work in [30], differs from that work with lumped-element modelling of the SRR structures. In that work, the measurements of transmission line loaded SRRs with backplate and no backplate are given and the lumped element modelling of them are explained in detail. Although, the models given are not enough for our circuit, they are used as starting point when utilizing our SRR model in this work.

1.1. Motivation

The work presented in this thesis, comprises a complementary cross coupled oscillator and a split ring resonator as a frequency selective network. The main reason of choosing these two structures is because it is aimed to achieve a biosensor which detects different materials dropped on SRR. In order to be successful, a low phase noise low power oscillator design is required since the oscillator has to detect small frequency shifts caused by different liquid materials which can only be done by a high quality resonator such as SRR.

Due to this intended biosensing application, a complementary cross coupled architecture is adopted in oscillator design. As it is a differential structure, naturally, it has advantages over single-ended topologies such as [32]:

- Even harmonics do not exist which lowers the total harmonic distortion and thus improves linearity
- For a given input sinusoidal, the harmonics amplitude is smaller than that of a single-ended
- Higher voltage swings can be achieved at low power
- Shows improved CMRR and PSRR due to lack of signal return path to ground

Furthermore, using a complementary architecture lowers the requirement of power consumption by doubling the total transconductance of the oscillator for the same transconductance transistors when compared to single-ended one. The differential structure also uses SRR with no backplate available which shows no transmission at resonance.

To detect very small shifts in frequency, SRR is chosen as a frequency selective network due to its high quality factor. By this property, a low phase noise oscillator that dissipates very low power can be designed. In design stage, to further lower the phase noise of the oscillator, in addition to use of SRR, some other methods are also surveyed [33–35]. In addition to its high quality factor, its resonant frequency changes

by dropping different liquid materials into its split or its gap which makes it very useful for biosensing applications such as disposable contact lens-based sensors [36]. SRR used in this work will be implemented as an off-chip resonator having a resonant frequency of 2.1GHz. It will be connected to oscillator chip core by using probes. Placing the probes as close as possible to oscillator core chip, the connection losses is intended to be minimized. Although it is an off-chip resonator for now, the future work will be aimed to use it as an on-chip resonator.

Another important aspect in this thesis is the lumped element modelling of SRR. In our design, a transmission line loaded SRR is used. Transmission lines behave as antennas forming magnetic coupling to SRR. Thus, the model needs to include SRR model as well as its magnetic coupling to the transmission lines. A lumped element model have been introduced in [37]. Further improvements are also given in [38, 39]. These models includes basic LC resonators as well as transmission line models. However, they present a simple cell of transmission line loaded SRR which cannot model our SRR completely. They are also not directly related to physical structure of SRR. They requires combining simple cells and fitting the parameters. On the other hand, model introduced in [30] is directly related to physical structure of SRR and is used as an intermediate stage in modelling. In this work, by modelling all transmission lines and eliminating all other components, the resistance-inductor-capacitor-only (RLC-only) model is introduced.

An electrical lumped element model is a crucial part of the design. Without a model, one needs to use only scattering parameters of the resonator which has several disadvantages. Firstly, with scattering parameters embedded in the simulator, transient simulations can be misleading. Instead, a lumped element model is a convenient way to run simulation independent of simulator type. Secondly, a lumped element model gives flexibility of tuning the SRR parameter on demand. For example, one can try to use different length of transmission lines or use transmission line on a different substrate. SRR gap, or transmission line distance effects can easily been observed. Finally, when using biosensing applications, one can simulate the ring as if a material is dropped to the gap by changing the gap capacitance parameter of the model.

1.2. Organization

In 2, a literature review on oscillators is presented. Especially, frequency selected networks and use of metamaterials as frequency selected networks are reviewed.

In Chapter 2, a detailed SRR structure is given. Its theory with calculation of the key parameters of SRR are shown. The proposed lumped element model design steps are described in detail. The simulation results of the final model are compared with measurement results. Lastly, the quality factor of the proposed model and the measured SRR is calculated and compared.

In Chapter 3, a complementary cross coupled oscillator design procedure is presented using the proposed SRR model in previous chapter. Also, the designed oscillator is laid out and the important key points of drawing layout of the oscillator are given.

Then, in Chapter 4, pre- and post- simulation results are given and compared to consider layout parasitics effect on circuit performance. An application example is also simulated and explained. Finally, a FOM calculation of final design is done two FOM comparison tables are given.

Finally, in Chapter 5, all work through this document is concluded with a general overview. Lastly, recommendations for future researches are given. What should be the next step is suggested and the possible problems of future work that can be encountered are introduced along with the solution ideas.

2. SPLIT RING RESONATOR THEORY AND MODELLING

In this chapter, split ring resonator structure and its theory is explained. Its superiority over other resonators is proven numerically. Furthermore, a lumped element model of a SRR is introduced to be able to use it in circuit designs in a more convenient way. Finally, simulation results are compared with measurement results and quality factor, Q, calculation of resonators is shown.

2.1. Theory of SRR

Split ring resonators are made of metamaterials that provides a high-Q factor. SRRs can have rectangular [40] or circular [30] shapes, yet all have at least a gap, which is their main design parameter. Figure 2.1 shows a structure of a circular SRR having one gap of width g, radius R, metal width w and a height h.

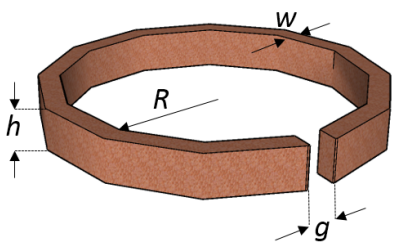


Figure 2.1. Split Ring Resonator (SRR).

SRR shows resonance at a certain frequency because it acts as an artificial magnetic dipole. While the gap acts as a capacitor, the ring itself acts as a inductor which

corresponds to a LC tank resonator. At resonance, that magnetic dipole lags the magnetic field by 180° that results in negative permeability. Along with the positive permittivity, a magnetic plasma is formed where propagating waves become evanescent waves. Thus, energy cannot propagate and is confined in the resonator. The wave is perfectly reflected to establish a standing wave. This leads to low energy loss and high-Q structure [29].

The most important specification of SRR, which is its resonant frequency, can be found by analyzing its physics. The capacitance is related to the gap, g, shown in Figure 2.1 which actually acts as a parallel plate capacitor. In addition to that gap capacitance, a surface capacitance is also comparable and not to be neglected [41]. Inductance, on the other hand, can be found by analyzing the ring itself. Once the total capacitance, C_{SRR} and inductance, L_{SRR} are found, it is straightforward to calculate resonant frequency, f_0:

$$f_0 = \left(\frac{1}{2\pi\sqrt{LC}} \right) \tag{2.1}$$

It is also possible to vary f_0 by increasing the gap capacitance. The gap capacitance can be considered as parallel plate capacitor:

$$C = \varepsilon \frac{A}{g} \tag{2.2}$$

where, A is the surface area of the gap walls, and g is the distance of gap and ε is the permittivity of the gap. Any material put into the gap increases ε which is given as:

$$\varepsilon = \varepsilon_0 \varepsilon_r \tag{2.3}$$

where, ε_0 is free space permittivity of air and ε_r is dielectric constant of any material. This in turn, increases the gap capacitance, decreasing the resonant frequency f_0.

On the other hand, a more detailed calculation of the total inductance and capacitance of SRR is given in [41]. Inductance is calculated as:

$$L_{SRR} = \mu_0 R_m \left(\log \frac{8R_m}{h+w} - \frac{1}{2} \right) \tag{2.4}$$

where, R is radius of SRR, w is width of metal, μ_0 is the free space permeability and $R_m = R + w/2$.

Total capacitance is the sum of gap capacitance, C_g and the surface capacitance C_s:

$$C_{SRR} = C_g + C_s \tag{2.5}$$

where

$$C_g = \varepsilon_0 \frac{hw}{g} + C_0 \tag{2.6}$$

$$C_s = \frac{2\varepsilon(h+w)}{\pi} \log \frac{4R}{g} \tag{2.7}$$

where ε_0 is the free space permittivity and C_0 is fringing field capacitance and defined as $C_0 = \varepsilon_0(h + w + g)$.

The SRR used in this work, on the other hand, is a transmission line loaded SRR without a backplate as can be seen in Figure 2.2. This 2-port structure comprises the ring and the transmission lines which can fabricated on any composite substrate. In this structure, transmission lines behave as antennas and are needed to excite the

ring to obtain resonance characteristics determined by physical ring dimensions and coupling of the transmission lines to the ring.

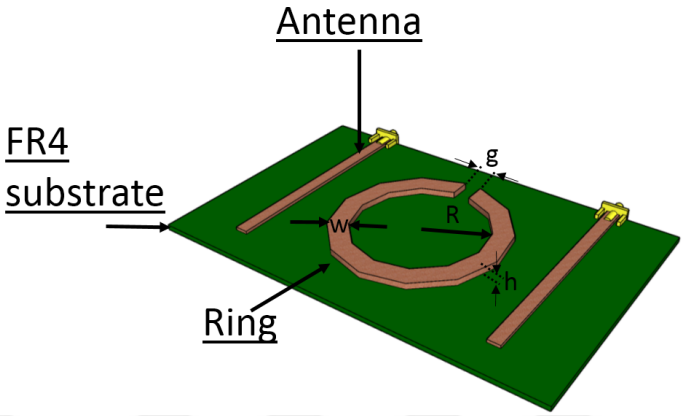


Figure 2.2. Transmission line loaded Split Ring Resonator (SRR).

2.2. Lumped Component Model of SRR

To design a cross coupled oscillator with scattering parameters of a measured SRR is a difficult task and not very convenient. To be more confident with the design of the oscillator, SRR is modelled with lumped components, namely capacitors and inductors. In this way, it is more convenient to analyze and play with SRR parameters. In this chapter, a lumped component model of SRR is designed called full-lumped-component model. Before showing the final model, an intermediate stage model in [30], called half-lumped-component model, is explained which is used as a intermediate step to constitute the final full-lumped-component model. In this work, both models are tried to fit a measured SRR having dimensions of $R = 6.85$mm, $w = 4$mm, $g = 1.65$mm implemented on a 1.57mm thick FR4 epoxy glass substrate having permittivity of $\varepsilon_r = 4.4$. Finally, the measurement results of the SRR and the simulation results of models are compared to each other. The full-lumped-component model is later used in a cross coupled oscillator design in Chapter 3.

2.2.1. Half-Lumped-Component Model

The model is named as half-lumped-component model because the SRR is modeled with lumped components such as inductors and capacitors along with transmission lines and transformers as in Figure 2.3. TL_1 and TL_2 are transmission lines excited from ports P_1 and P_2. They represent the first 14mm part of the antennas whose end points correspond to the closest points of the SRR to the antennas. TL_3 and TL_4 are transmission lines acting as open circuit stub. They represent the remaining 16mm part of the antennas. TF_1 and TF_2 are transformers representing magnetic coupling of SRR to the antennas with a coupling coefficient n. In addition, the only lumped components, C_{SRR}, L_{SRR}, and R_{SRR} are electrically characterizing SRR ring itself as total capacitance, total inductance and loss of the ring, respectively.

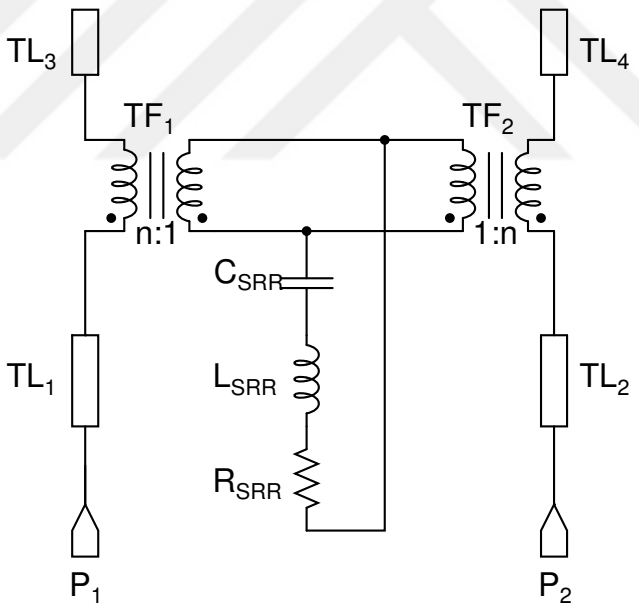


Figure 2.3. Half-Lumped-Component model of SRR.

The model is designed in Advance Design System software (ADS). Transmission lines are modeled by real substrate parameters and their real physical dimensions. Transformer coupling coefficient, n is found empirically. Total capacitance and inductance are initially calculated from Equations 2.4 and 2.5, respectively. The loss of the ring, R_{SRR}, is determined by the Q of the resonator. Then, by ADS tuning tool, the

model is fitted better to measurement results (see Figure 2.10). The model parameters are found as $C_{SRR} = 139fF$, $L_{SRR} = 41.69nH$, $R_{SRR} = 1.5\Omega$ and $n = 0.221$

2.2.2. Full-Lumped-Component Model

In [29] and [37], several lumped component models are explained in detail and some examples are given which show that we can model a SRR as a parallel LC tank resonator. However, without including the transmission lines and magnetic coupling of SRR to them, models are not adequate to represent the transmission line loaded SRRs. Although the model explained in Chapter 2.2.1 covers these effects, it is still not adequate all the time for several reasons:

- Model of transmission line and transformer components are not exactly the same for all simulators which prevents the use of SRR model freely in any simulator.
- Using a transmission line requires exact knowledge of the properties of the substrate that the SRR is mounted on which can vary even from manufacturer to manufacturer.
- Transient simulations do not always give exact results when using transmission lines or transformers in a circuit.

Thus, a SRR model is designed comprised only lumped components, namely, inductors, capacitors and resistors (RLC). To achieve this goal, the transmission lines and transformers shown in Figure 2.3 are replaced by RLC models. First, transmission lines TL_1 and TL_2 and then open circuit stubs TL_3 and TL_4 are designed. Then by impedance transformation, transformers TF_1 and TF_2 are eliminated.

2.2.2.1. TL_1 and TL_2 Modelling. As transmission line loaded SRR is a reciprocal structure, TL_1 and TL_2 are equivalent to each other. They are 14mm length, 3mm width 50Ω transmission lines mounted on FR4 substrate. The transmission line is modelled by using T-network in ADS. The lumped component model of TL_1 can be seen in Figure 2.4.

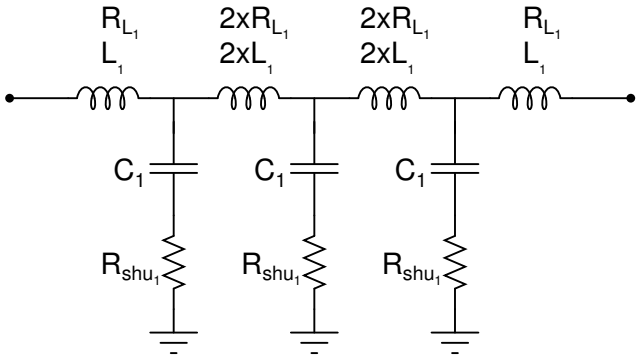


Figure 2.4. Lumped component model of TL_1.

The scattering parameters comparison of TL_1 and its lumped component model is shown in Figure 2.5.

As can be seen in Figure 2.5(a) and Figure 2.5(b), return loss and insertion loss of lumped component T-network model is well fitted with the transmission line model. The error of the model in magnitude of the return loss and the insertion loss is $\pm$1dB within the bandwidth of 6GHz. The phase response is also very close to model as shown in Figure 2.5(c). The phase error of the model is $\pm 10^{\circ}$ with a $\pm$0.4GHz frequency error at 180° phase shift. The Smith Chart is also given in Figure 2.5(d) for further verification that this model is valid up to 6GHz.

In the lumped component model, the design parameters are found as $L_1 = 270$pH, $R_{L_1} = 0.7\Omega$, $C_1 = 2$pF and $R_{shu_1} = 0.632\Omega$ where L_1 is unit length inductance, R_{L_1} is loss of unit length inductor, C_1 is shunt capacitance to ground and R_{shu_1} is substrate losses, respectively.

2.2.2.2. TL_3 and TL_4 Modelling. Again due to the reciprocal structure, TL_3 and TL_4 are equivalent to each other. They are 16mm length, 3mm width 50Ω transmission lines mounted on FR4 substrate. The transmission line is modelled by using T-network in ADS. The lumped component model of TL_3 can be seen in Figure 2.6.

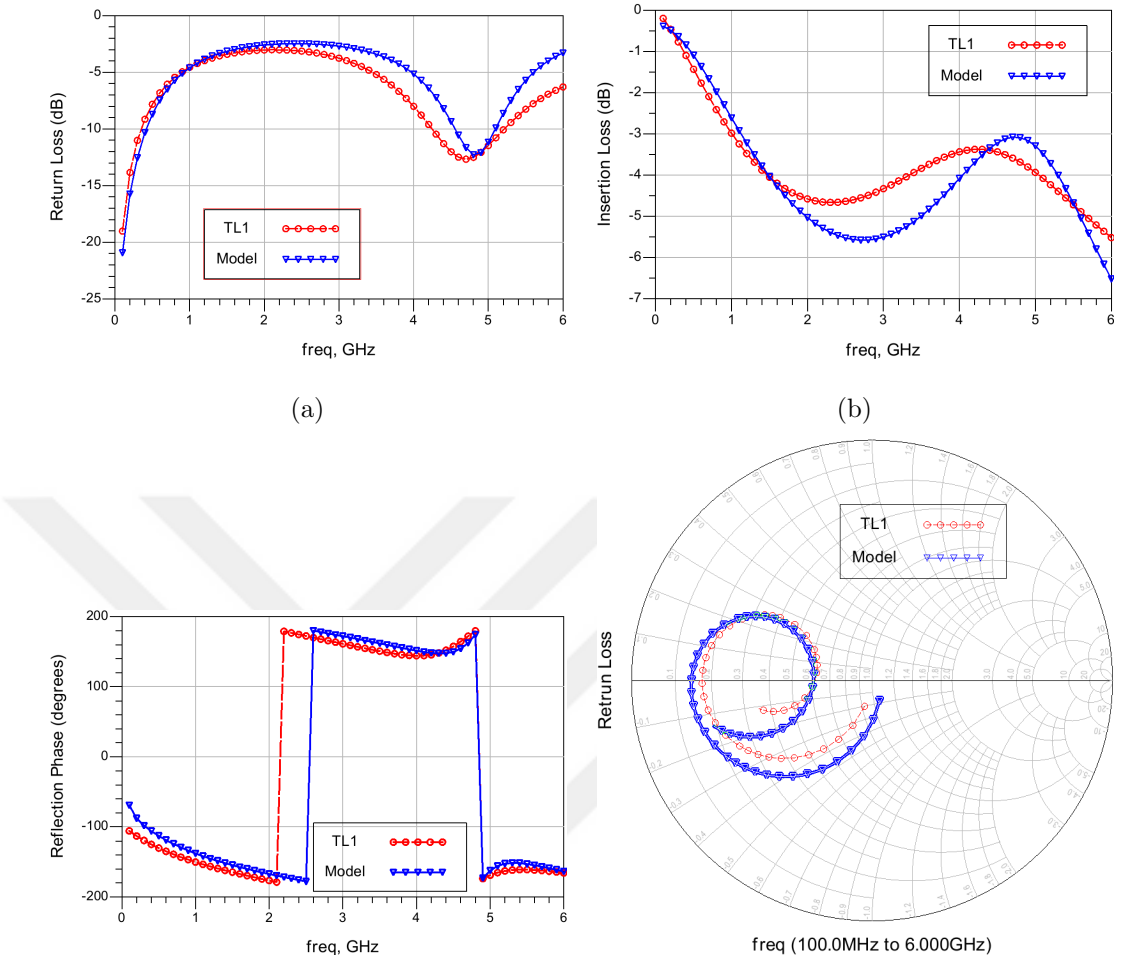


Figure 2.5. Scattering parameters comparison of TL_1 and T-network lumped model.

The scattering parameters comparison of TL_3 and its lumped component model is shown in Figure 2.7.

As can be seen in Figure 2.7(a) and Figure 2.7(b), return loss and insertion loss of lumped component T-network model is well fitted with the transmission line model. The error of the model in magnitude of the return loss and the insertion loss is again $\pm$1dB within the bandwidth of 6GHz. The phase response is also very close to model as shown in Figure 2.7(c). The phase error of the model is $\pm 10^{\circ}$ with a $\pm$0.4GHz frequency error at 180° phase shift. The Smith Chart is also given in Figure 2.7(d) for further verification that this model is valid up to 6GHz.

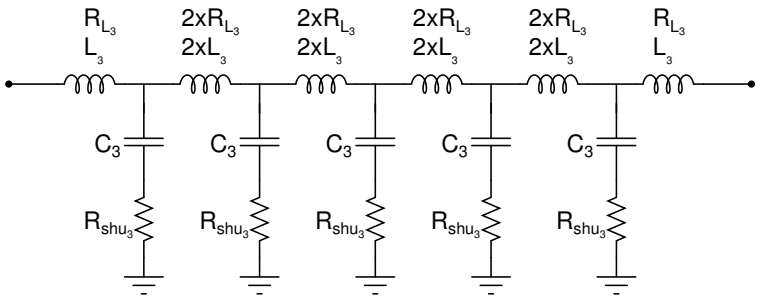


Figure 2.6. Lumped component model of TL_3.

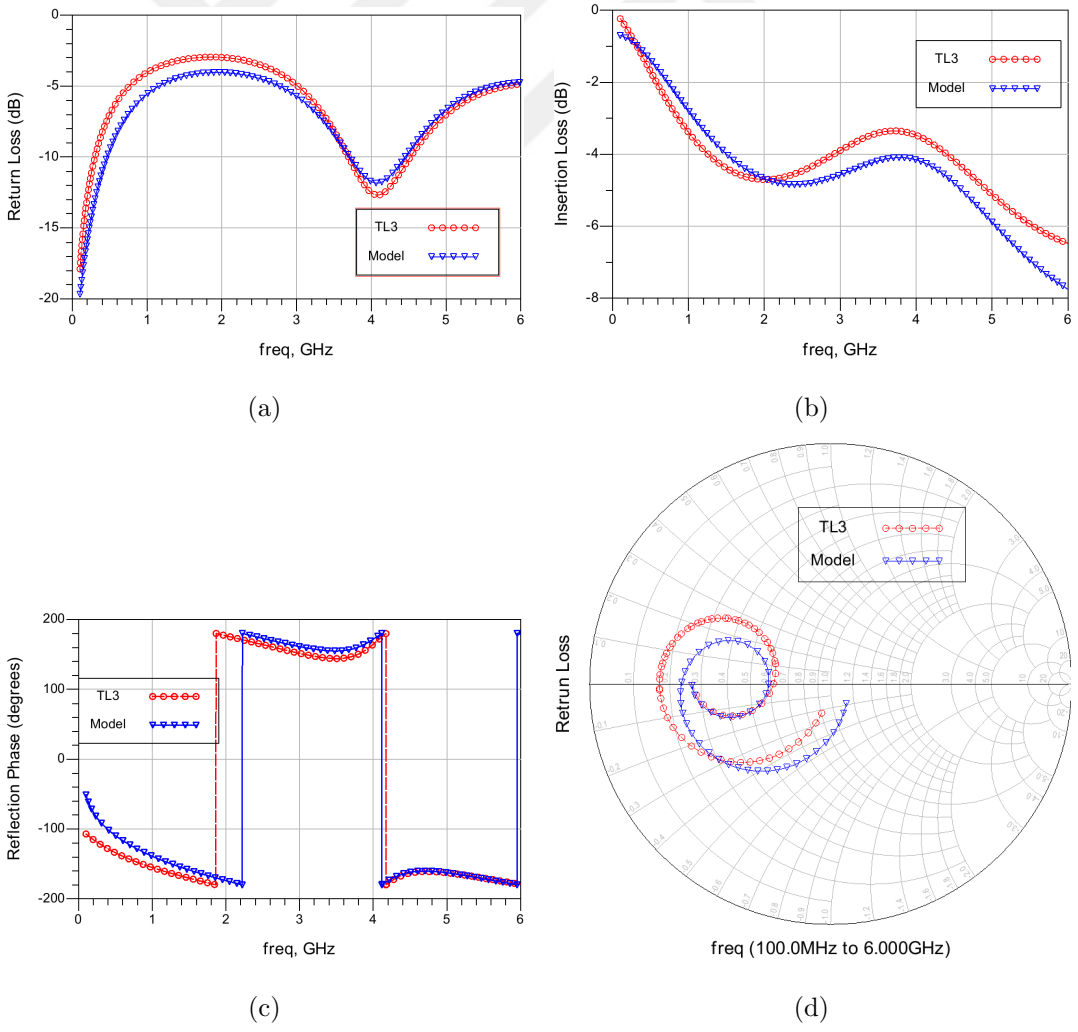


Figure 2.7. Scattering parameters comparison of TL_3 and T-network lumped model.

In the lumped component model, the design parameters are found as $L_1 = 240$pH, $R_{L_3} = 0.8\Omega$, $C_3 = 1.2$pF and $R_{shu_3} = 3.1\Omega$ where L_3 is unit length inductance, R_{L_3} is loss of unit length inductor, C_3 is shunt capacitance to ground and R_{shu_3} is substrate losses, respectively.

2.2.2.3. Transmission Line Loaded SRR Model. Full lumped component model comprises lumped component models of TL_1 and TL_3, and a parallel LC resonator tank which represents the ring itself including magnetic coupling effects.

A simple parallel LC resonator tank can be seen in Figure 2.8 representing core ring of the SRR with lumped components L_{SRR}, C_{SRR} and R_{SRR}.

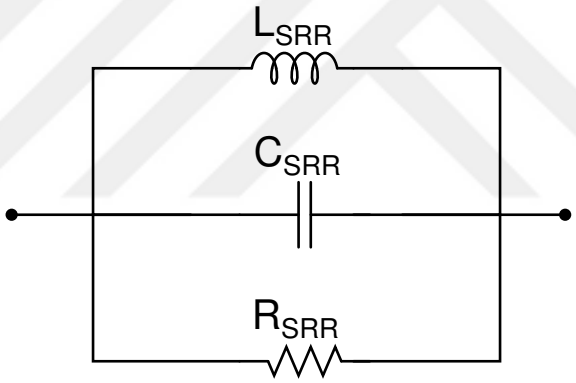


Figure 2.8. Parallel LC tank resonator representing SRR core.

Another important aspect of this model is to eliminate transformer by impedance transformation method. The total capacitance and inductance of SRR explained in Chapter 2.2.1 can be transformed as follows:

$$C \rightarrow \frac{C}{n^2} \tag{2.8}$$

$$L \rightarrow n^2 L \tag{2.9}$$

where, n is the coupling coefficient of transformer.

Applying Equations 2.8 and 2.9, the capacitance value found in Section 2.2.1 increases to pF levels while inductance value decreases to pH levels since n is less than 1.

By combining all three models as in Figure 2.9, the final lumped component model of transmission line model is obtained. In the final lumped component model, the design parameters for the transmission lines are found as $L_1 = 350$pH, $R_{L_1} = 0.12\Omega$, $C_1 = 2.2$pF, $R_{shu_1} = 5\Omega$, $L_3 = 250$pH, $R_{L_3} = 2.1\Omega$, $C_3 = 1.9$pF and $R_{shu_3} = 3.13\Omega$. On the other hand, the core SRR ring parameters are found as $L_{SRR} = 184$pH, $C_{SRR} = 31.5$pF and $R_{SRR} = 1.1$kΩ.

2.2.3. Simulation Results of SRR Model

The scattering parameters comparison of half-lumped-component model, full-lumped-component model and measurement results of SRR are shown in Figure 2.10.

Figure 2.10(a) shows return losses where the full-lumped-component model fits the measurement results better. The error of the full-lumped-component model in magnitude of the return loss is ±3dB. Furthermore, as can be seen in Figure 2.10(b), the resonant frequencies of both models and measured SRR are close to each other and all of them are around 2.1GHz. From this graph, one can also deduce that the SRR has a very high quality factor which is calculated and explained in detail in Section 2.2.4. In Figures 2.10(c) and 2.10(d), the reflection and transmission phase responses can be seen. The phase responses are also consistent with measurement that 180° phase shift can be seen at resonant frequencies with a ±40° phase error.

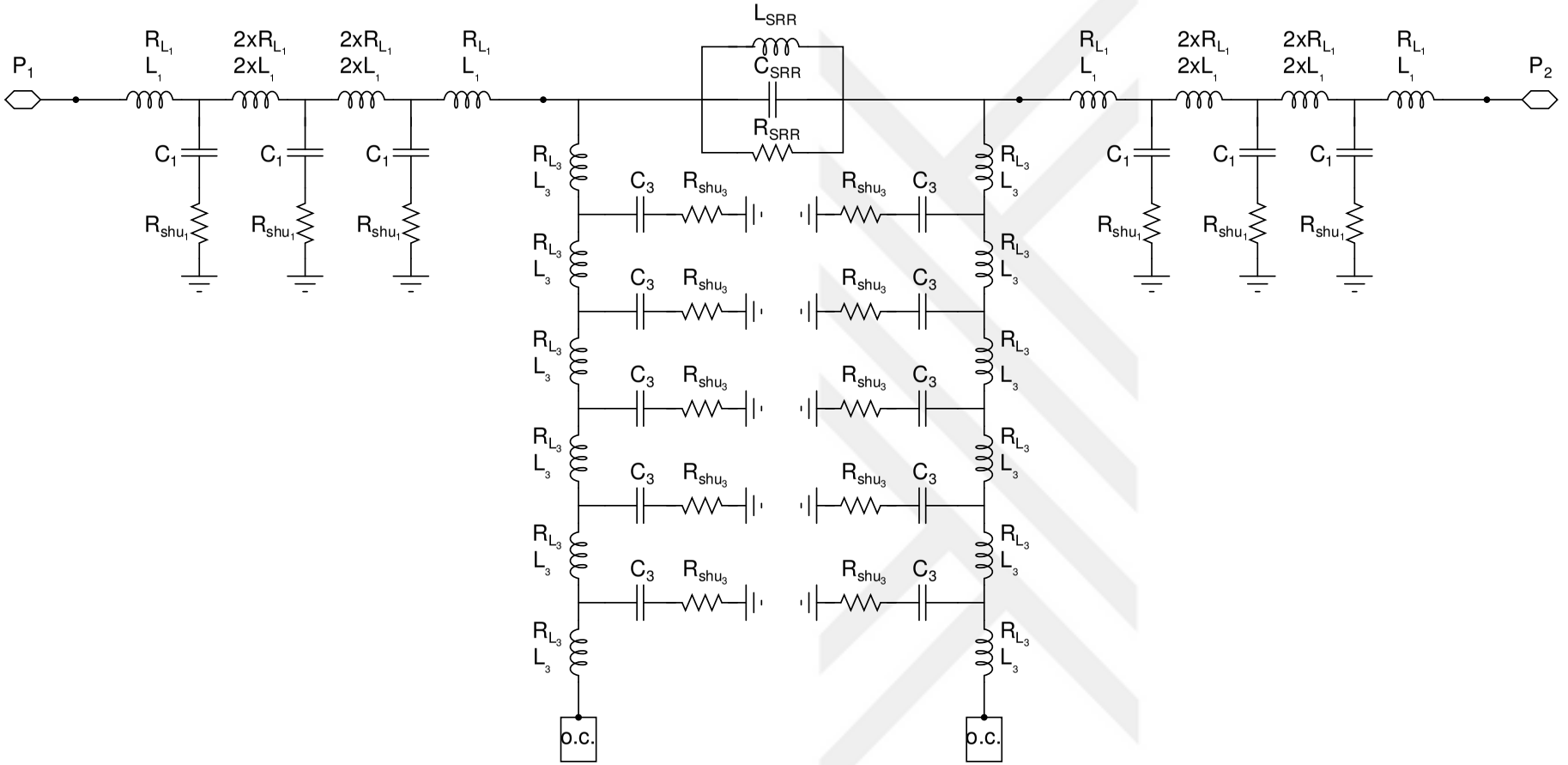


Figure 2.9. Full-lumped-component model of transmission loaded SRR.

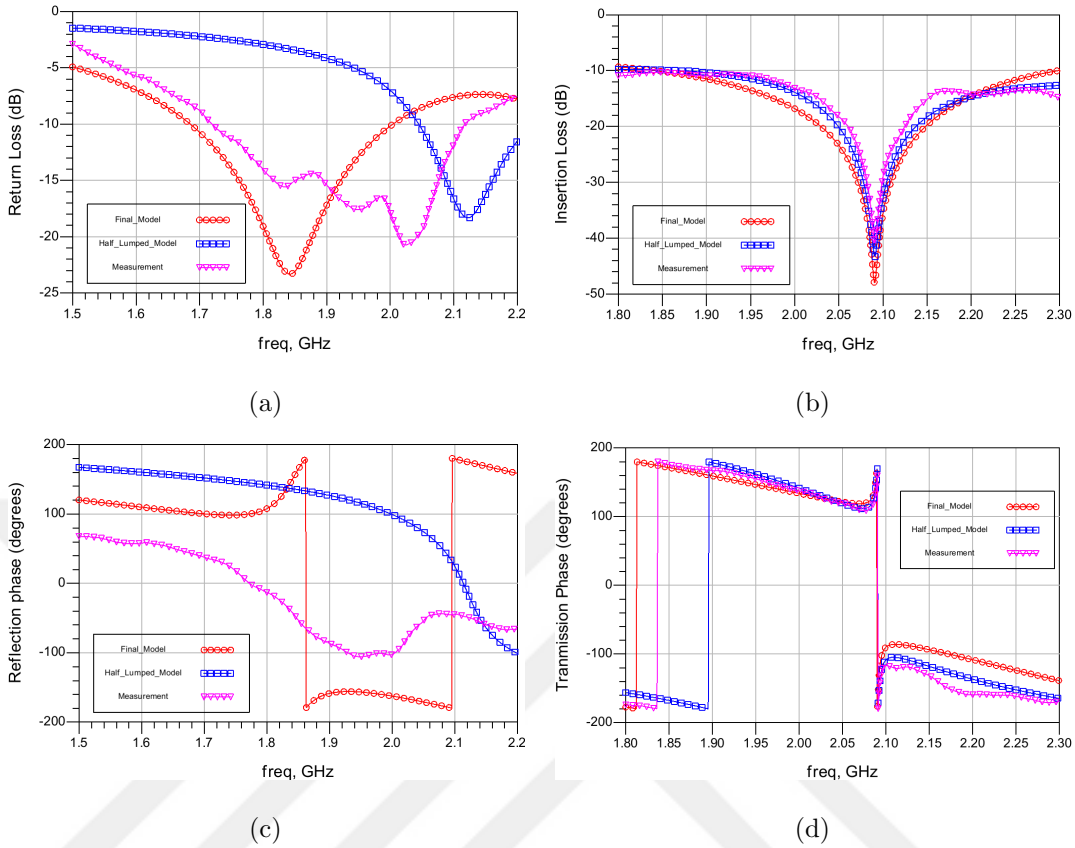


Figure 2.10. Scattering parameters comparison of models and measurement.

2.2.4. Quality Factor Calculation of SRR

Quality factor, Q, is an implication of how much energy is lost during transferring of the energy back and forth between the capacitance and the inductance of a resonator and it is simply formulated [42] as :

$$Q = 2\pi \frac{energy\ stored}{energy\ dissipated\ per\ cycle} \tag{2.10}$$

Q also determines the sharpness of the magnitude of a transfer function. More specifically, it can also be calculated by -3dB bandwidth method which is also valid

for parallel LC resonator tanks and can be formulated as follows [32]:

$$Q_T = \frac{\omega_0}{2f_c} = \frac{\omega_0}{BW_{-3\text{dB}}} \tag{2.11}$$

where, Q_T is quality factor of the tank, ω_0 is the resonant frequency, f_c is the corner frequency at 3dB and $BW_{-3\text{dB}}$ is the 3dB bandwidth of the resonator.

The Q of the SRR and its model is found using Equation 2.11 and it is summarized in Table 2.1.

Table 2.1. Quality Factor of SRR and its lumped component model.

	f_0 **[GHz]**	$BW_{-3\text{dB}}$ **[MHz]**	Q **Factor**
Measurement	2.091	4.93	424
Full-Lumped-Model	2.091	4.77	438
Half-Lumped-Model	2.091	5.77	363

Furthermore, its equivalent parallel resistance at resonance can be found by setting up the simulation bench in Figure 2.11

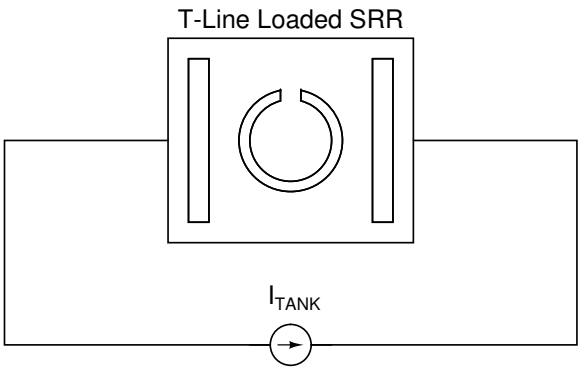


Figure 2.11. Finding equivalent parallel resistance of T-Line loaded SRR.

By running an AC simulation in ADS applying 1V, the equivalent parallel resistance can be calculated as follows:

$$R_{SRR} = real(\frac{1}{I_{TANK}}) = 182\Omega \tag{2.12}$$

where I_{TANK} is the peak current value at resonance of SRR.

High quality factor and high parallel equivalent resistance of the SRR are very important for good oscillator performance. With this resonator, a very low phase noise and a low power oscillator can be designed. In the next chapter, the oscillator design using the SRR model designed in Section 2.2.2 is explained and its performance is discussed.

3. CROSS COUPLED OSCILLATOR PRINCIPLES AND DESIGN

As described in Chapter 1, oscillators constitute a crucial block in integrated circuits and have been widely used in most radio frequency radio communication systems as well as biosensing applications which is the main motivation of this work. This chapter starts with an introduction of negative transconductance oscillators. Then, cross coupled oscillator architectures are compared and a complementary cross coupled oscillator is designed by using final-lumped-element model of the SRR. Phase noise concept is also explained. Finally, the final architecture is proposed and the layout of the design is given.

3.1. Working principle of Negative Transconductance Oscillators

An ideal inductor-capacitor (LC) oscillator, shown in Figure 3.1, can oscillate easily without any damping. However in reality, there is a parallel equivalent resistance as in Figure 3.2 that leads to damping of the oscillating signal.

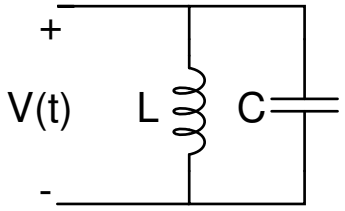


Figure 3.1. An ideal LC oscillator.

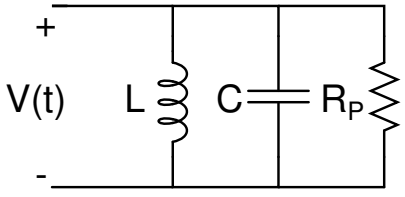


Figure 3.2. A dumped LC oscillator.

Thus, one needs to compensate the equivalent parallel resistance of an oscillator with an equivalent negative resistance. If one can achieve such a circuit as in Figure 3.3, an oscillating signal without any damping can be achieved.

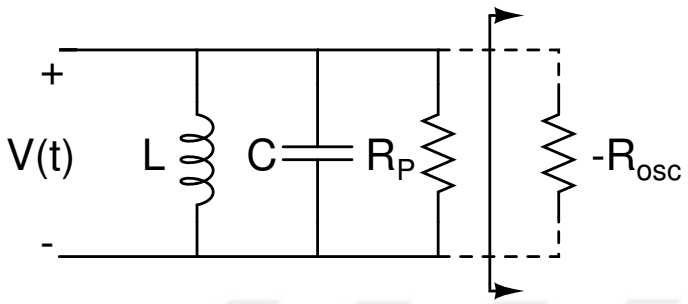


Figure 3.3. A $-Gm$ LC oscillator.

From Figure 3.3, one can deduce the oscillation condition easily. Once the negative resistance, $-R_{osc}$, cancels out the equivalent parallel resistance, R_p, the oscillation occurs forever. For oscillation to start, the following condition has to be satisfied [42]:

$$-R_{osc} \leq R_p \tag{3.1}$$

or in terms of conductances

$$-G_{osc} \geq G_p \tag{3.2}$$

where $-G_{osc}$ is negative transconductance and G_p is equivalent parallel conductance of the tank.

Since there is no known negative resistance yet, a cross coupled transistor pair in Figure 3.4 can be used to obtain a negative resistance, $-R_{osc}$ or a transconductance, $-G_m$.

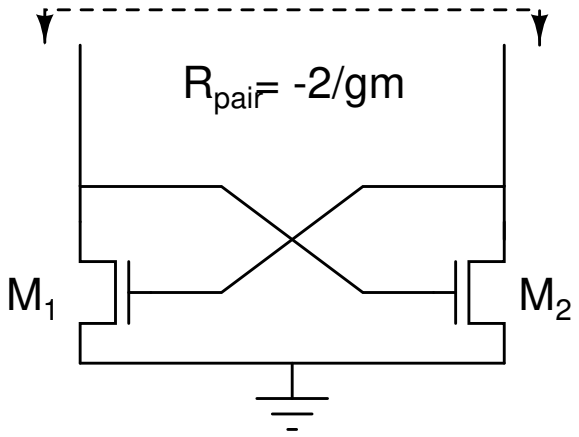


Figure 3.4. Cross coupled transistor pair.

3.1.1. $-G_m$ Calculation

To calculate impedance of the cross coupled pair, a test source can be connected between the drain of the transistors as in Figure 3.5

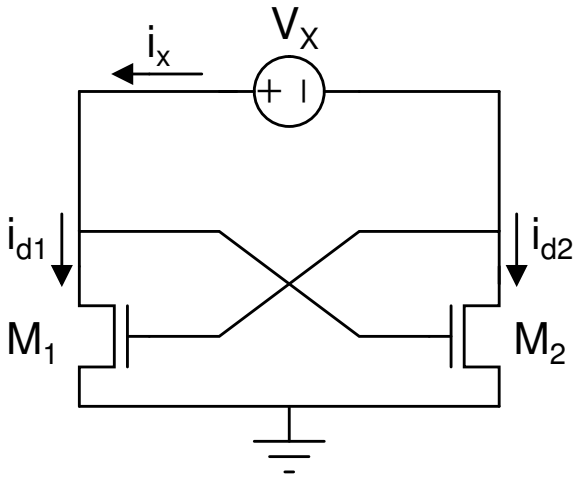


Figure 3.5. Cross coupled pair with test source.

Since M1 and M2 transistors are identical, they have equal small signal transconductance values, g_m=g_{m1}=g_{m2}, and $i_x = i_{d1} = -i_{d2}$.

Thus, drain currents can written as

$$i_x = g_m v_{gs1} = -g_m v_{gs2} \tag{3.3}$$

Equation 3.3 can be rewritten as

$$g_m v_{gs1} - g_m v_{gs2} = 2i_x \tag{3.4}$$

$$g_m(v_{gs2} - v_{gs1}) = -2i_x \tag{3.5}$$

which gives, transconductance of cross coupled pair, G_m

$$G_m = \frac{i_x}{(v_{gs2} - v_{gs1})} = -\frac{g_m}{2} \tag{3.6}$$

3.2. Cross Coupled Oscillator Architectures

There are 3 major cross coupled oscillator architectures, namely NMOS-only, PMOS-only and Complementary cross coupled oscillators. There are always design trade-offs between them in terms of area, phase noise, power consumption. NMOS-only structure in Figure 3.6 has superiority over PMOS-only structure in Figure 3.7 in terms of area for a given transconductance value. Due to higher electron mobility in NMOS transistors, smaller sizes of NMOS transistors can be used for the same current or g_m value. In addition to this, larger PMOS transistors mean more drain-source and drain-bulk capacitance which decreases the frequency tuning range of the oscillator. On the other hand, PMOS transistors have lower flicker noise which is an advantage for lower phase noise [43].

On the other hand, the complementary cross coupled architecture in Figure 3.8 provides faster switching between cross coupled transistors for a given current value.

This is because, one can obtain a higher transconductance at a given current. Furthermore, it has the best rise and fall time symmetry resulting in less upconversion of 1/f noise. This structure also leads to less overdrive voltages on transistors due to stacking of PMOS and NMOS transistors. In NMOS-only or PMOS-only structures transistors have large overdrive voltages which results in stronger velocity saturation [9].

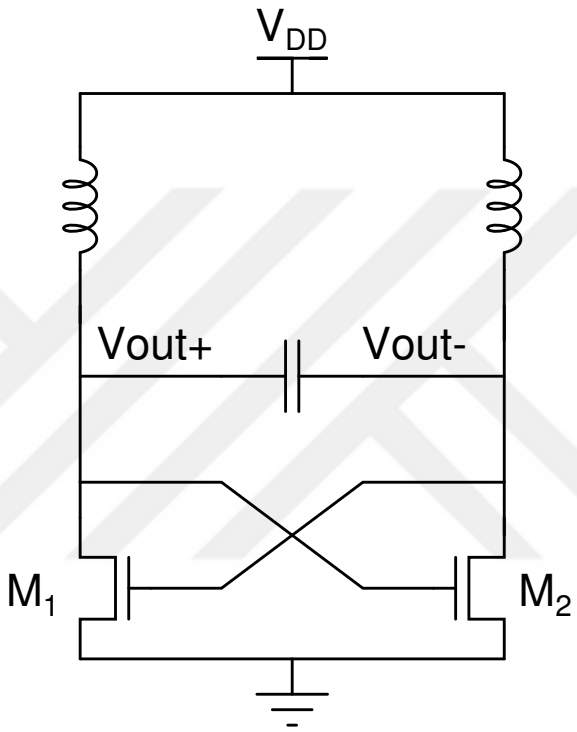


Figure 3.6. NMOS-only Cross Coupled Oscillator Architecture.

3.3. Design Methodology

In this work, our purpose is to design an oscillator detecting very small frequency shifts which can only be achieved by a very low phase noise oscillator. The other challenging topic is that the oscillator should consume very low power because of its intended usage area, i.e medical microelectronics. Having a very high-Q split ring resonator mentioned in Section 2.2.4 helps us accomplish such design goals. In this chapter, complete design procedure is given explaining each design step in detail. How much the design could achieve the desired goals is also shown with all simulation steps and results.

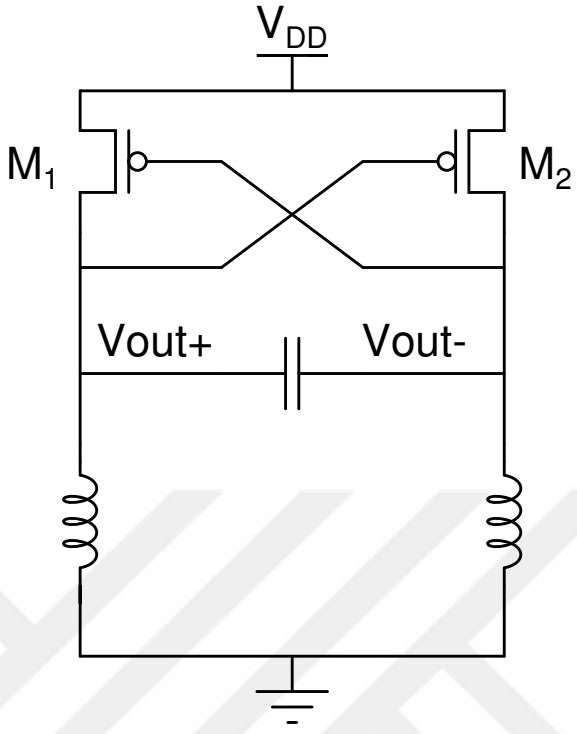


Figure 3.7. PMOS-only Cross Coupled Oscillator Architecture.

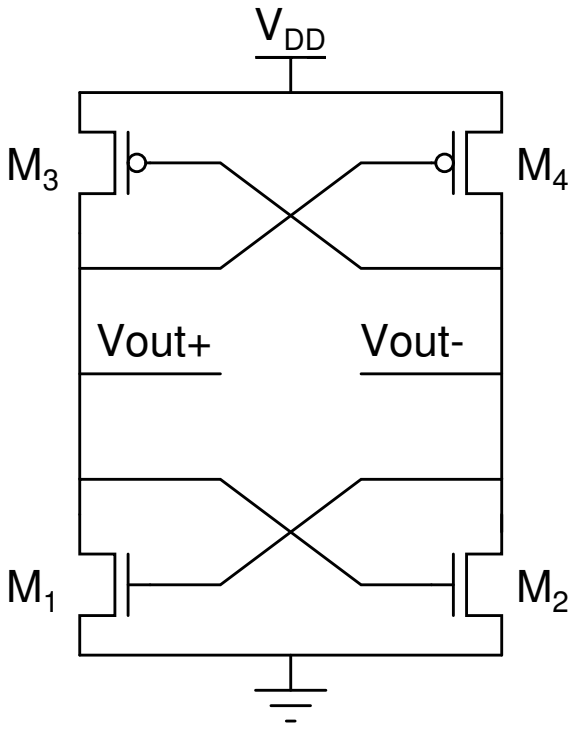


Figure 3.8. Complementary Cross Coupled Oscillator Architecture.

3.3.1. Complementary Cross Coupled Oscillator Design

Complementary cross coupled oscillator architecture is adapted in this design because of its various superior properties over other architectures mentioned in Section 3.2. In this design, instead of an on chip low-Q LC tank, an off chip high-Q split ring resonator (SRR) is used. A representative schematic diagram can be seen in Figure 3.9.

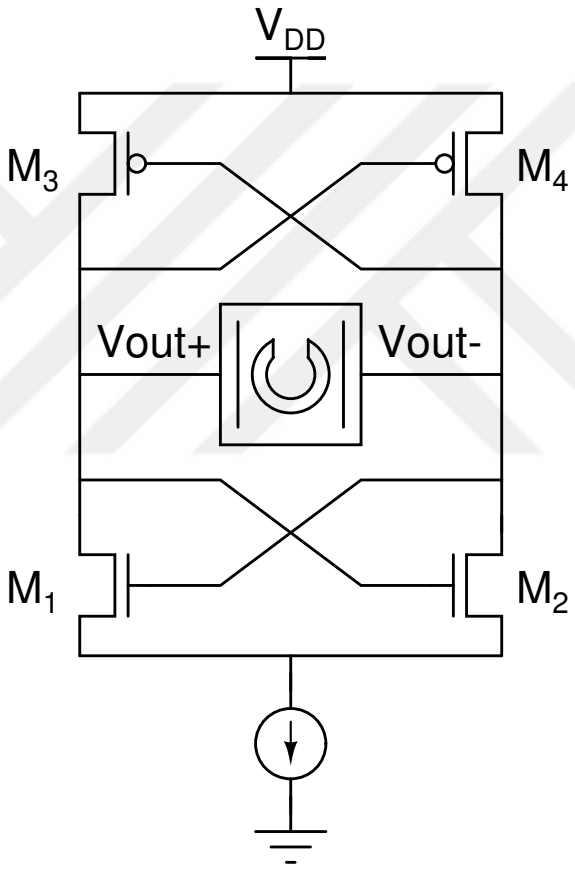


Figure 3.9. Complementary cross coupled oscillator with SRR.

As calculated in Section 2.2.4, the SRR used in this work has a very high Q value of 438 and a equivalent parallel resistance R_{SRR} of 181Ω.

Since the values for Q and R_{SRR} have been found earlier, one must continue with finding minimum g_m value of each transistor. One superiority of the complemen-

tary cross coupled topology over NMOS-only or PMOS-only architectures is that for the same oscillator transconductance, G_m, the former consumes less power. If g_m of each NMOS and PMOS transistors is chosen equal, the equal transconductance of the complementary cross coupled oscillator is doubled as follows:

Let each NMOS and PMOS cross coupled pairs have equivalent transconductance values of $\frac{g_{m1}}{2}$ and $\frac{g_{m3}}{2}$, respectively.

Then, the complementary architecture equivalent transconductance, G_m, is

$$G_m = \frac{g_{m1}}{2} + \frac{g_{m3}}{2} \tag{3.7}$$

If transistors are chosen such that g_{m1}= g_{m3}=g_m, then

$$G_m = \frac{g_m}{2} + \frac{g_m}{2} \tag{3.8}$$

$$G_m = g_m \tag{3.9}$$

To satisfy oscillation condition Equation 3.1 has to be satisfied as follow:

$$\frac{1}{G_m} = \frac{1}{g_m} \leq R_{SRR} = 182\Omega \tag{3.10}$$

$$g_m \geq 5.52mS \tag{3.11}$$

From g_m value found in Equation 3.11, DC drain currents, I_D of transistors are calculated as follows:

$$gm = \frac{2I_D}{V_{OV}} \tag{3.12}$$

$$I_D = \frac{g_m V_{OV}}{2} \tag{3.13}$$

Choosing V_{OV} as 0.8V for 1.8V supply voltage

$$I_D = \frac{5.52 \times 0.8}{2} = 2.21mA \tag{3.14}$$

which means total minimum 4.42mA DC bias current through all circuit.

From I_D values found in Equation 3.14, transistors width and length values can be determined as:

$$I_D = \frac{1}{2}\mu_n C'_{ox}(\frac{W}{L})_N(V_{GS} - V_T)^2 \tag{3.15}$$

for an NMOS transistor. That is:

$$\left(\frac{W}{L}\right)_N = 31 \tag{3.16}$$

For the used 0.18μm process, PMOS transistor width and length values are:

$$\left(\frac{W}{L}\right)_P = 124 \tag{3.17}$$

However, these calculations do not take into account the gate-drain capacitance C_{gd} and drain-bulk capacitance C_{db}. Thus, when the circuit with these values are implemented in Cadence, the required minimum g_m cannot be satisfied to start oscil-

lation. To ensure oscillation to start, larger transistors are chosen so that the g_m value is adjusted as 1.5 times the minimum required value which is 7.7mS.

Also the total current is increased to 4.5mA to obtain better phase noise at 1MHz offset frequency. Phase noise at 1MHz offset frequency versus total bias current can be seen in Figure 3.10. Increasing current after the dashed vertical line does not improve the phase noise substantially as can be seen in Figure 3.10(a). Furthermore, Figure 3.10(b) shows how the phase noise improvement saturates after the bias current reaches the value of 4.5mA. Thus, there is no reason for further increase of bias current.

In addition to saturation of phase noise, differential output voltage is also saturated as in Figure 3.11.

One can further increase the bias current to obtain better phase noise which in turn requires larger transistors and thus more parasitic capacitances resulting in larger area but almost the same phase noise. Phase noise is further explained in Section 3.3.2.

3.3.2. Phase Noise of Cross Coupled Oscillator

Phase noise is the one of the most important design parameters for an oscillator. It is because higher phase noise leads strong noise sidebands around the oscillation frequency limiting the measurement accuracy of it. In this work, a very low phase noise is expected due to a very low-Q SRR which helps us detect very small frequency changes by varying the oscillation frequency of SRR as mentioned in Section 2.1. Oscillator is not naturally noiseless because of the flicker noise of transistors and thermal noise of all circuit elements but it is possible to minimize these effects by understanding and covering concept of phase noise [44]. The reasons of phase noise have been defined several times by different people. One of the most popular one, Leeson's model of phase noise is adapted in this work.

According to Leesons's heuristic proportionality [33, 44], phase noise of a cross coupled oscillator at a given offset frequency, $L(\omega_m)$, can be defined as:

$$L(\omega_m) = 10\log\left[\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega_0}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega_0|}\right)\right] \tag{3.18}$$

where ω_0, $\Delta\omega_0$, P_{sig}, Q, F are fundamental oscillating frequency, offset frequency, output signal power, quality factor of a resonator and empirical fitting factor, respectively.

As can be seen in Equation 3.18, Q of the resonator plays a very important role for low phase noise as its square is inversely proportional with the phase noise. Also, the higher the P_{sig}, the lower the phase noise will be. In other words, as the output voltage increases, phase noise will be lower which, in return, leads to more bias current and increased power consumption.

3.4. Final Design and Layout

In this chapter, final design of the oscillator is shown with its all simulation results. Layout of the design is considered and post-layout simulation results are also given.

3.4.1. Final Architecture

The proposed architecture in Figure 3.12 is designed in 0.18μm silicon-on-insulator (SOI) process.

The width and length values of M1/M2 NMOS and M3/M4 PMOS transistors are chosen as :

$$\left(\frac{W}{L}\right)_N = \frac{12}{0.18} \tag{3.19}$$

and

$$\left(\frac{W}{L}\right)_P = \frac{44}{0.18} \tag{3.20}$$

respectively so that G_m of oscillator is 7.7mS which is almost 1.5 larger than the minimum required value of 5.5mS as shown in Equation 3.11.

Final current is also adjusted to 4.5mA to obtain best phase noise at 1MHz offset frequency as simulated in Figure 3.10(b).

Another important aspect of final design is the current mirror. Instead of short circuiting to ground, a current mirror is used as shown in Figure 3.9 with M5 and M6 transistors. A short can also sustain a steady state oscillation. However, after start up, as the differential oscillation voltage crosses the threshold voltage, V_T, in one cycle, two of the transistors M1 and M4 go into triode region while other ones go into deep saturation. Drain source transconductance, g_{ds}, of FETs in triode region adds more loss to the resonator because current flowing through resonator is in phase with the voltage at resonant frequency. In the next cycle, the other pair of transistors add another loss which, in overall, lowers the average Q of resonator.

Now consider using a current mirror. If W/L of FETs are chosen in start-up condition such that $V_{GS} - V_T < V_{DS}$, differential voltage drives M1 and M4 into triode region while M2 and M3 are off. Thus, no current can flow through g_{ds} of the triode FET preventing loading of the resonator. In the other cycle, the roles are changed and M1 and M4 are off while M2 and M3 are in triode region [10].

A trick which can be used in the current mirror is connecting a capacitor in parallel with current source transistor, M5. This technique is applied to lower the phase noise originating from the mirror itself. It is called the noise filtering technique. In LC oscillators, while current sources set the biasing current, they also show high impedance in series with the cross coupled transistor pairs and sum of the currents of differential pair flows through the current mirror. If a capacitor is connected in

parallel with the current mirror, an alternative path is created to that currents. As the capacitance is larger, the duty cycle of the differential pair current reduces which also reducing the drain current of the NMOS and PMOS differential pair transistors at differential zero crossing. Thus, the voltage variations at the current mirror node attenuates reducing the channel length modulation of M5. This leads to lower phase noise providing less upconversion of $\frac{1}{f}$ noise [45]. Noise filtering technique can be applied by connecting a capacitor C_1 in parallel to M5 as in Figure 3.13.

How a capacitor can lower the the phase noise can be seen in Figure 3.14. The Figure 3.14 shows phase noise at 1MHz offset offset frequency with increasing capacitance value parallel to the current mirror transistor.

Yet, in this work, the current source transistor M5 and M6 is, fortunately, large enough so that parasitic C_{gd} and C_{db} capacitances help improve phase noise inherently. Thus, no additional capacitance is used in this work and the final schematic in Figure 3.12 is adapted.

3.4.2. Layout

Drawing the layout of a cross coupled oscillator should be taken seriously, especially at radio frequencies. After laying out the circuit, extra parasitic capacitances, resistors, long interconnect lines behaving as transmission lines can affect the oscillator causing shift of oscillation frequency substantially, increase phase noise or even completely deteriorate the circuit.

During layout, the first aim is to place the transistors. They are placed as close as possible to decrease both area and the routing metal lengths so that one can minimize the parasitics. Although resonator placement is also important, in our case it is not a concern since an off-chip resonator is used. Still output nodes of the oscillator are connected with a wide routing metal so that inductance and resistance of the line is minimized. V_{DD} and GND routing metals are also important. Since no additional parasitic resistance and inductance is wanted, they are also connected with wide enough

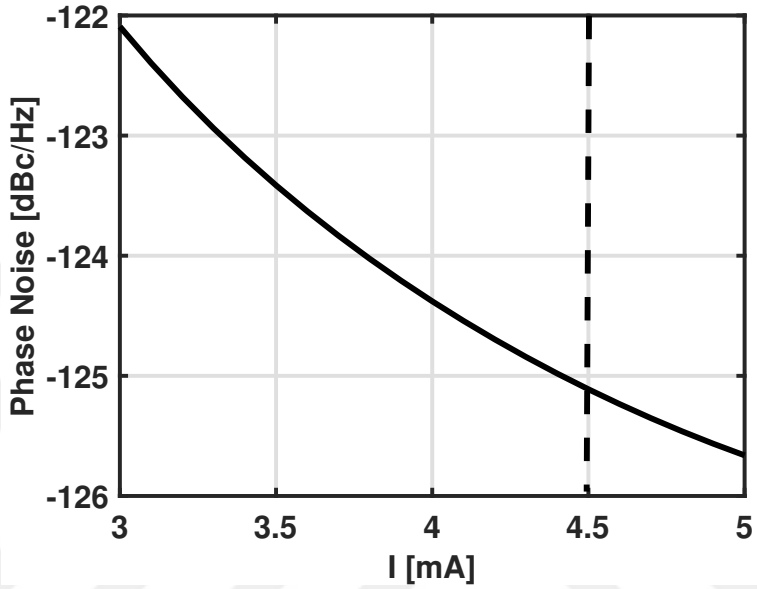
routing metals. Finally, to reduce parasitics further, all nodes are connected to pads with top and the fourth metal layer.

The other concern is whether the metal routings have enough width to carry the current. The bias current is divided in DC operating condition and cross coupled transistors carry only half. However, when oscillating, all of the bias current flows through one side for each half cycle of the period. In our case, bias current is 4.5mA and drain and source of all NMOS and PMOS are connected with metals having current carrying capability of that much current. Drain and sources of NMOS and PMOS transistor pairs are connected with 1.2μm metal-2 which can carry 4.9mA current at 125°C. Also, the multi-fingered transistors help carrying enough current by dividing it into their finger numbers. Since V_{DD} and GND routing metals are laid out wide, there is no problem in terms of current carrying capacity. Finally, since no current flow through gates, they are not our concern in terms of current.

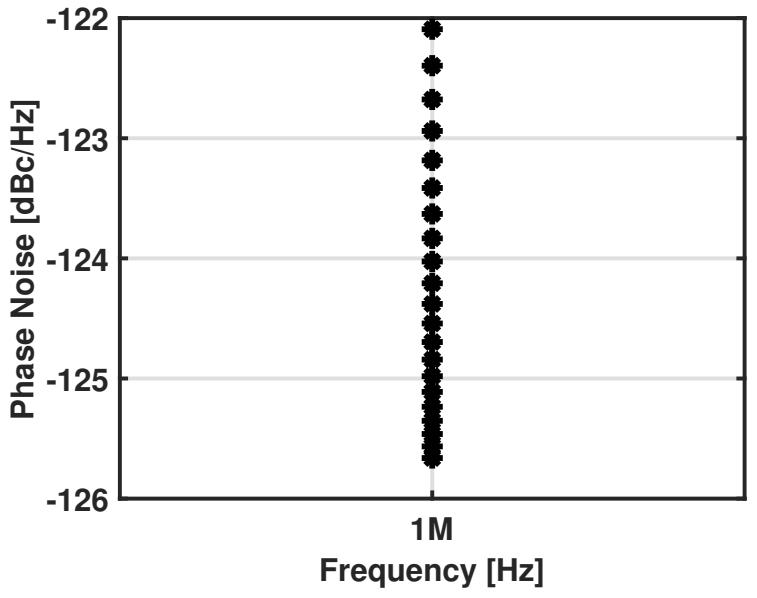
After the design is finalized, the circuit is laid out in two ways by employing the concerns mentioned above. The difference between two layouts in Figure 3.15 and Figure 3.16 is that the latter is laid out including pads. This is applied to see effect of probe pads in addition the layout parasitic resistance and capacitances.

The oscillator core shown in Figure 3.15 covers 18μm $\times$ 25μm area. As can be seen, V_{DD} and GND lines are 1.2μm width which is drawn intentionally as well as drain and source of FETs routing metals.

On the other hand, to connect off chip resonator, SRR, to oscillator output nodes, probe pads are thought to be best option to minimize the routing effects. As can be seen in Figure 3.16, probe pads are included in the layout covering 80μm$\times$94.3μm area. However, probe pads have still capacitive effects which are need to be considered in this work. With post-layout simulation results in Chapter 4, these effects are explained in detail.



(a)



(b)

Figure 3.10. Phase noise @1MHz offset frequency vs bias current.

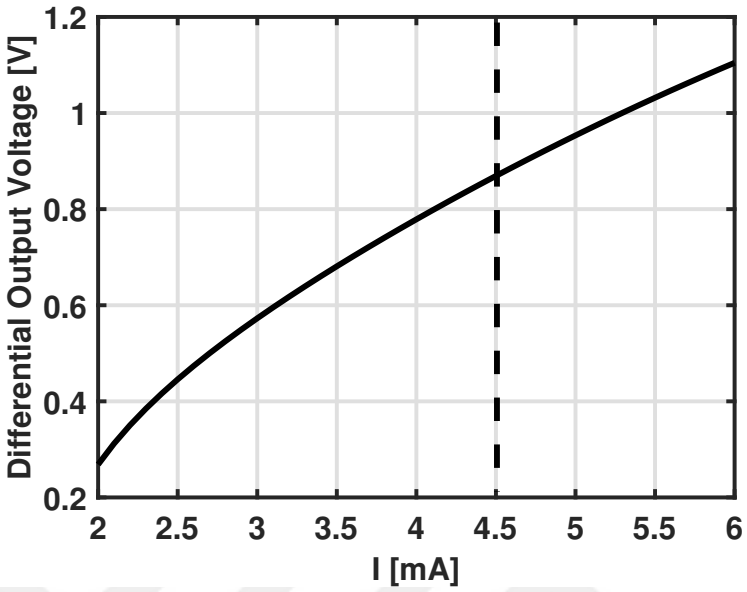


Figure 3.11. Peak value of differential output voltage vs bias current.

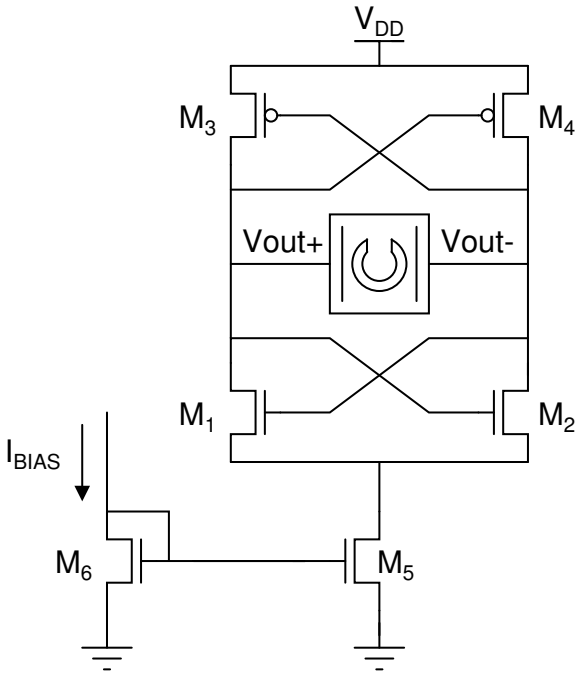


Figure 3.12. Final cross coupled oscillator schematic.

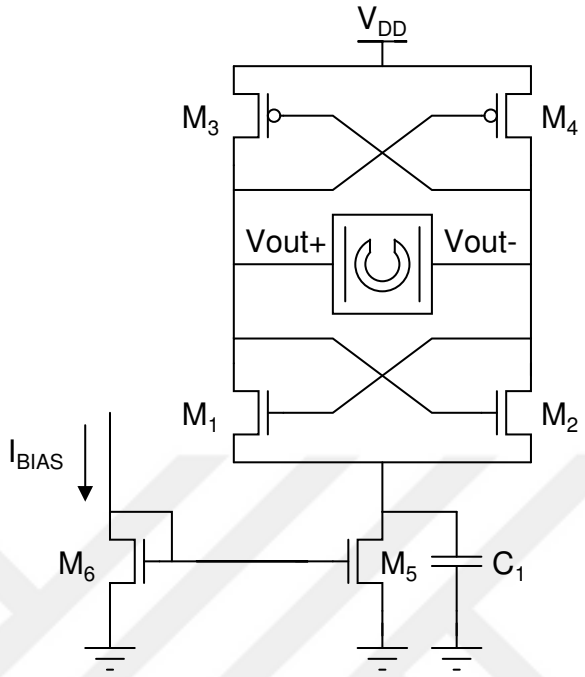


Figure 3.13. Cross coupled oscillator with noise filter.

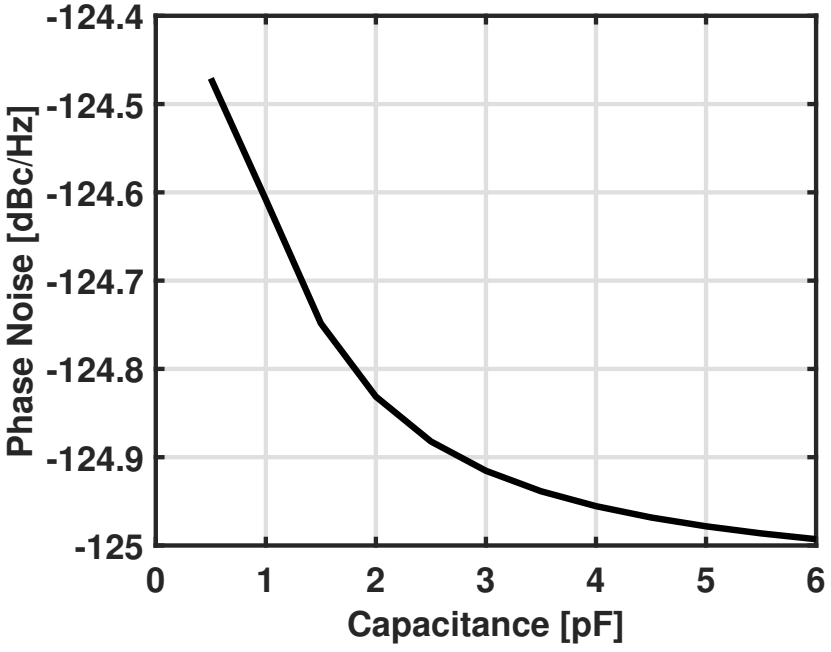


Figure 3.14. C_1 value sweep vs phase noise.

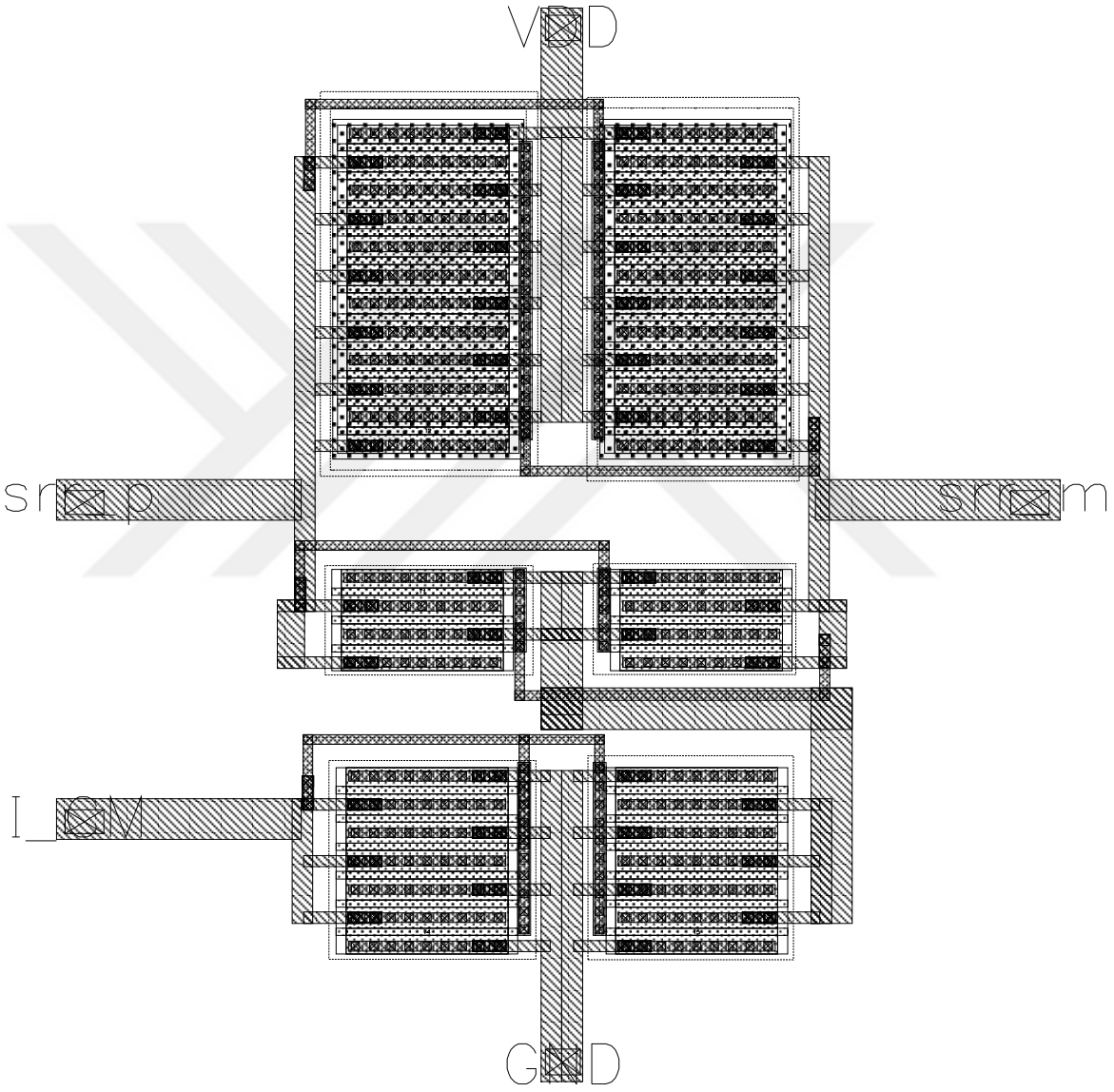


Figure 3.15. Final layout of oscillator without probe pads.

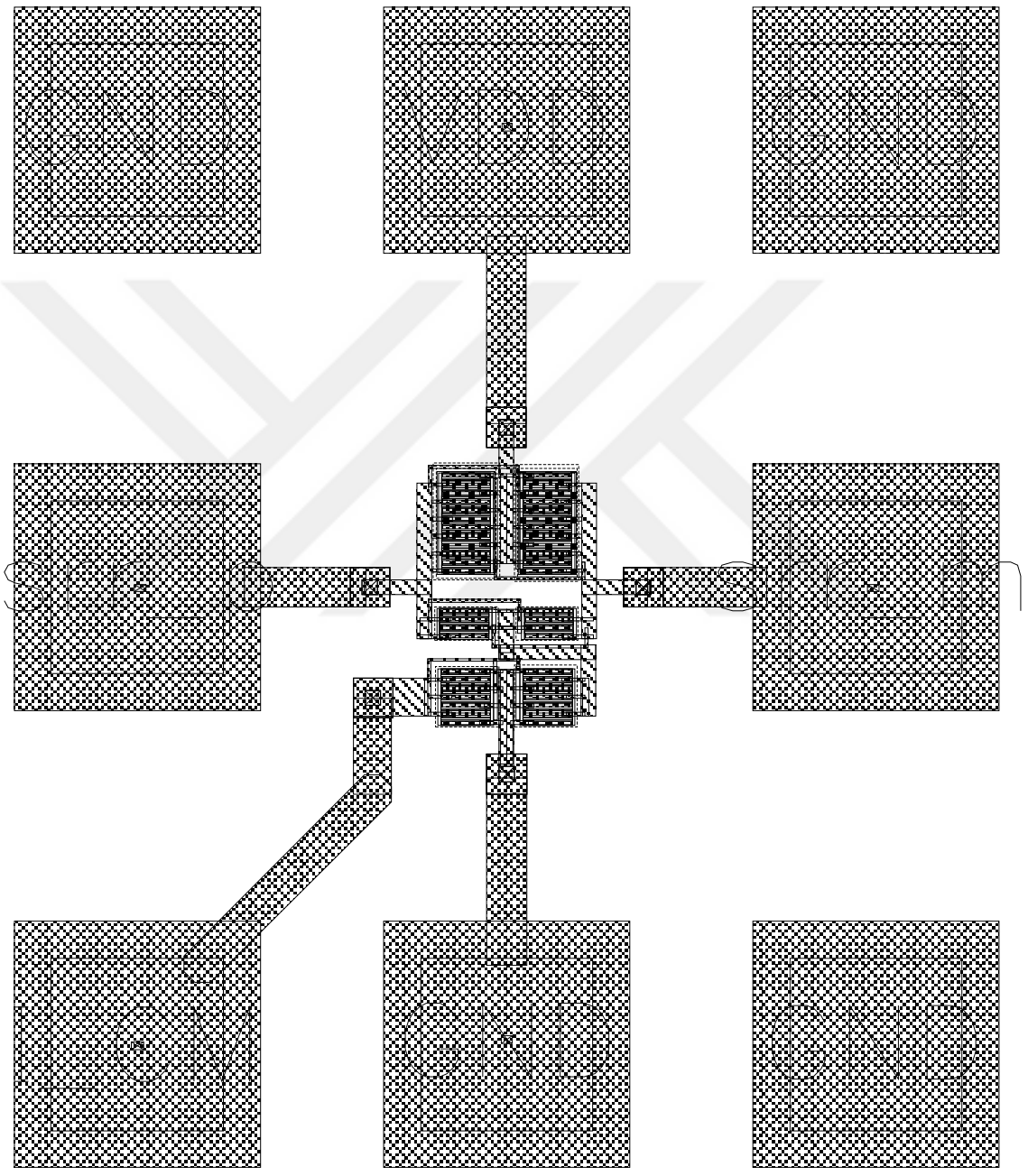


Figure 3.16. Final layout of oscillator with probe pads.

4. PRE- AND POST- LAYOUT SIMULATION RESULTS

With a very high-Q off chip split ring resonator, a low phase noise low power complementary cross coupled oscillator is designed in this work. After finalizing the design in Section 3.4.1, all simulation results are provided with all details in this chapter along with post-layout simulation results. The simulation results are given in three separate sections. First one is the schematic simulation results. The second one is the simulation results of the circuit after layout parasitic extraction is done. The third one is, on the other hand, the simulation results after parasitic extracting of layout including probe pads of the die are done. All of the extractions are done in Assura Quantus QRC.

4.1. Schematic Simulation Results

The schematic simulation results of Complementary Cross Coupled Oscillator with SRR shown in Figure 3.12 are given in this section. The simulations are run in Cadence SpecteRF. DC, transient, periodic steady state (PSS) and phase noise (pnoise) analysis are done to cover all aspects of the circuit.

In Figure 4.1, the fundamental and the higher order harmonics of the differential output voltage in dB scale can be seen. As can been seen fundamental oscillation frequency is 1.809GHz which is 33dB higher than third order harmonic component and 56dB than that of fifth order. Even harmonics are cancelled at differential output voltages and not of concern.

The low phase noise is obtained expected due to a high-Q resonator is shown in Figure 4.2. The phase noise is observed from 1kHz to 100MHz offset frequencies, $\Delta\omega_0$. Also some of the phase noise values at important offset frequencies are summarized in Table 4.1.

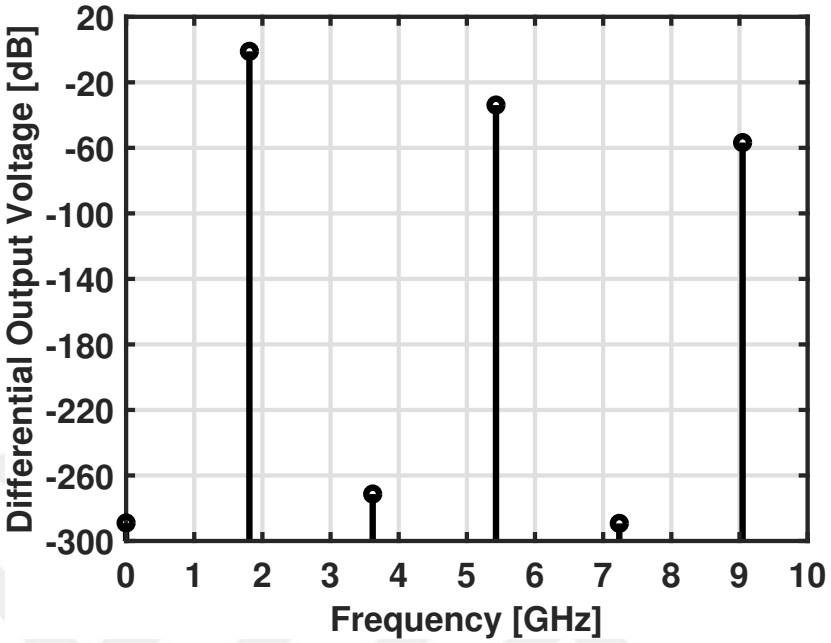


Figure 4.1. Fundamental and higher order components of differential output signal of schematic simulation.

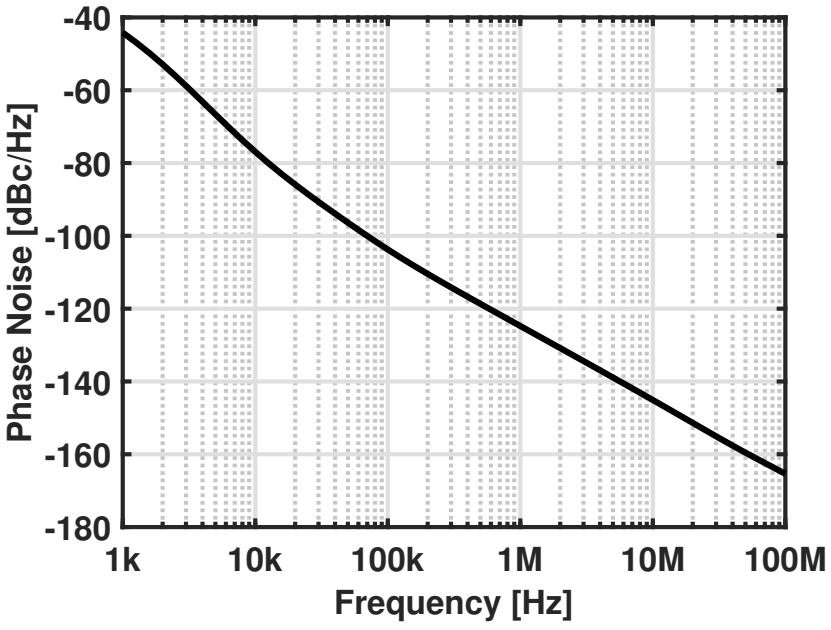


Figure 4.2. Phase noise versus vs offset frequency of schematic simulation .

Table 4.1. Phase noise in schematic simulation.

	Phase Noise (dBc/Hz)
$\Delta\omega_0 = 10$kHz	-76.9
$\Delta\omega_0 = 100$kHz	-103.8
$\Delta\omega_0 = 1$MHz	-124.8
$\Delta\omega_0 = 10$MHz	-145.1
$\Delta\omega_0 = 100$MHz	-165.4

The transient output differential voltage waveform can also be seen in Figure 4.3. The peak differential output voltage is limited to 0.9V as shown in Figure 3.11 as explained in Section 3.3.1

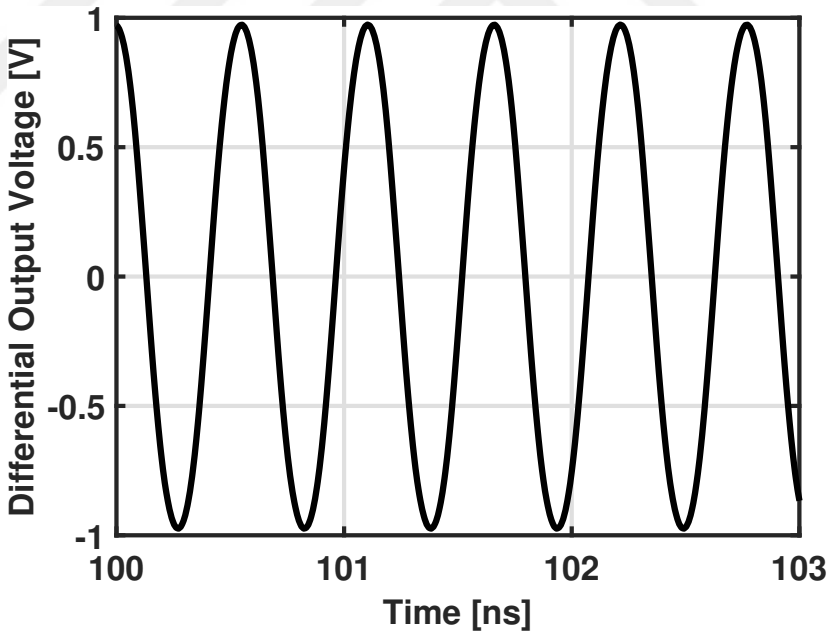


Figure 4.3. Differential output voltage waveform of schematic simulation.

4.2. Post-Layout Simulation Results without Pads

The first layout is drawn without pads. The same simulations are done as in Chapter 4.1 in Cadence SpectreRF with the same analysis tools.

In Figure 4.4, the fundamental and the higher order harmonics of the differential output voltage in dB scale can be seen. As can been seen fundamental oscillation frequency shifted down to 1.798GHz which is 32dB higher than third order harmonic component and 58dB than that of fifth order. Even harmonics are again cancelled. The voltage shift to a lower frequency is an expected result since as explained in Section 2.1, extra parasitic capacitance lowers the oscillation frequency.

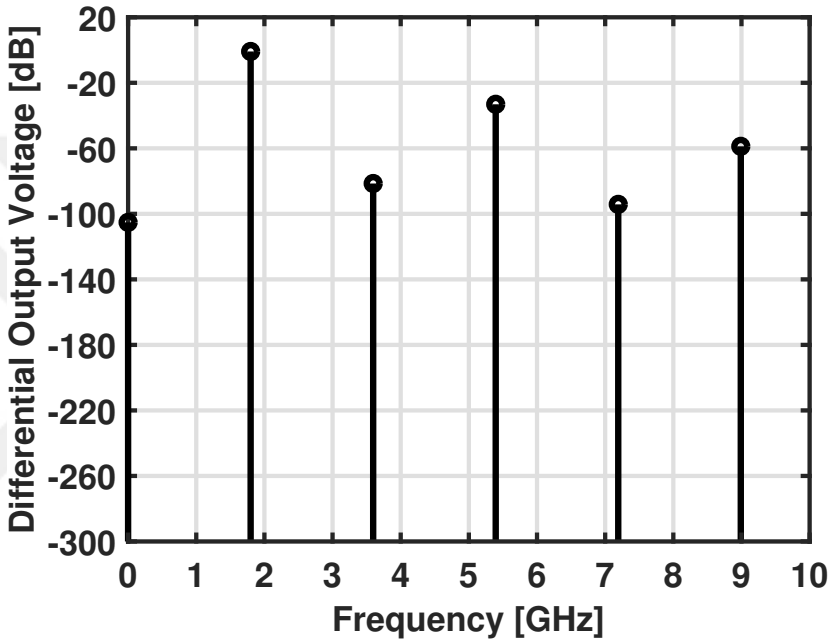


Figure 4.4. Fundamental and higher order components of output signal of layout without pads simulation.

Due to parasitics, a worse phase noise is obtained especially for lower offset frequencies. Phase noise increased 1dBc/Hz at 1kHz and 0.2dBc/Hz at 100kHz. On other hand, at higher frequencies, phase noise stays almost the same. The phase noise simulation and a summary of results be seen in Figure 4.5 and in Table 4.2, respectively.

The transient output differential voltage waveform can also be seen in Figure 4.6. The peak differential output voltage is limited to 0.9V as in schematic simulation result.

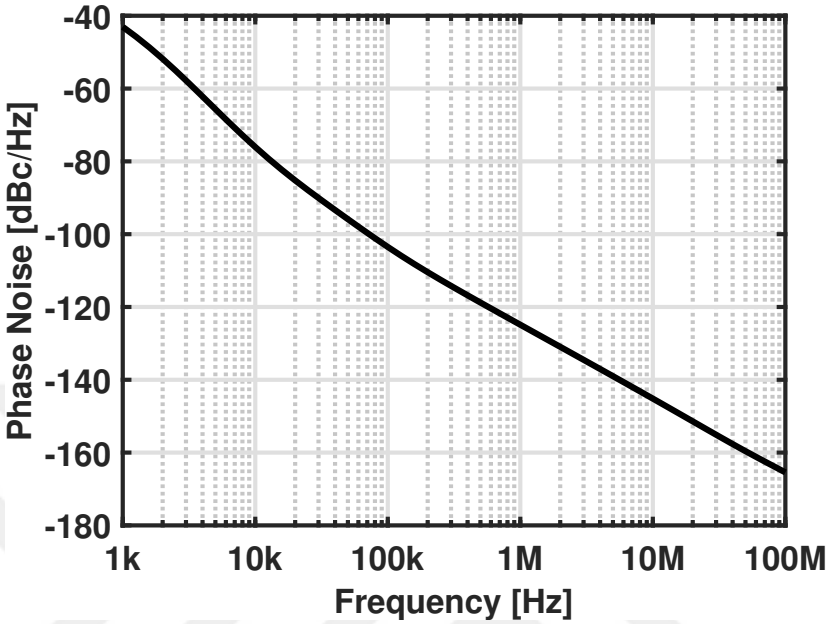


Figure 4.5. Phase noise at various offset frequencies of layout without pads simulation.

Table 4.2. Phase noise in layout without pads simulation.

	Phase Noise (dBc/Hz)
$\Delta\omega_0 = 10$kHz	-76.1
$\Delta\omega_0 = 100$kHz	-103.5
$\Delta\omega_0 = 1$MHz	-124.8
$\Delta\omega_0 = 10$MHz	-145.1
$\Delta\omega_0 = 100$MHz	-165.4

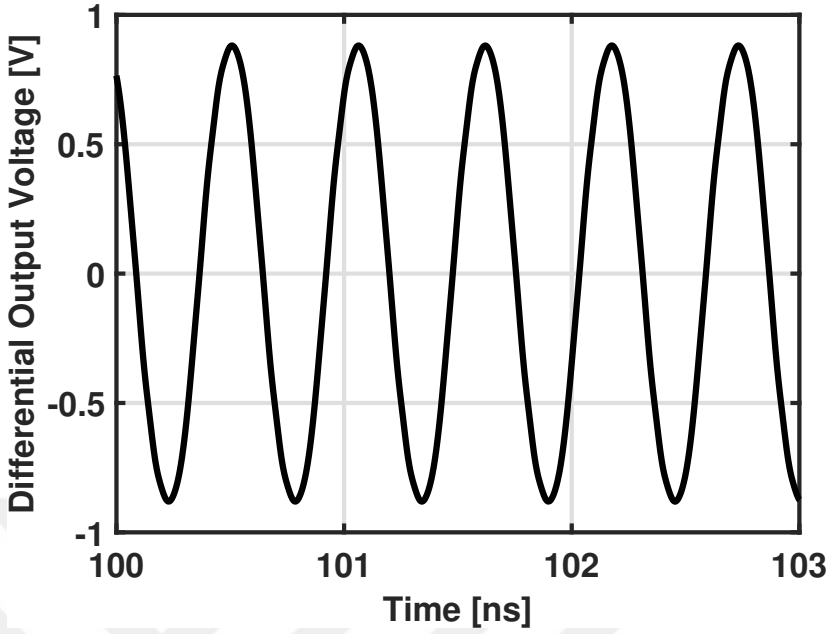


Figure 4.6. Differential output voltage waveform of layout without pads simulation.

4.3. Post-Layout Simulation Results with Pads

The second and the final layout is drawn with pads. To extract pad parasitics and do post-layout simulations to verify the circuit is one of the most critical steps before going tape-out. The same simulations are done as in Sections 4.1 and 4.2 in Cadence SpectreRF with the same analysis tools.

In Figure 4.7, the fundamental and the higher order harmonics of the differential output voltage in dB scale can be seen. As can been seen fundamental oscillation frequency shifted down to 1.796GHz which is 32dB higher than third order harmonic component and 55dB than that of fifth order. Even harmonics are again cancelled. More voltage shift to a lower frequency is an expected result due to pads causing more extra parasitic capacitance as explained in Sections 2.1 and 3.4.2.

The simulation and a summary of results be seen in Figure 4.8 and in Table 4.3, respectively.

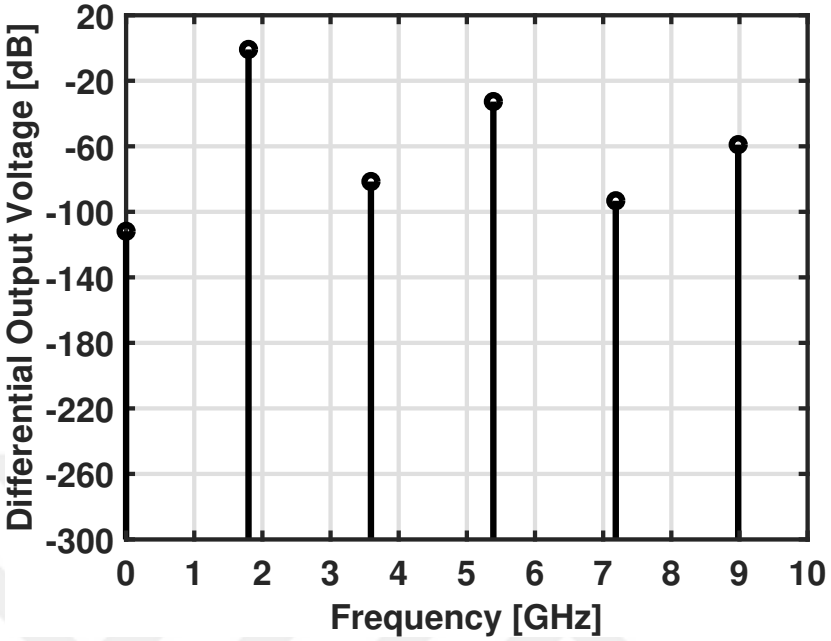


Figure 4.7. Fundamental and higher order components of output signal of layout with pads simulation.

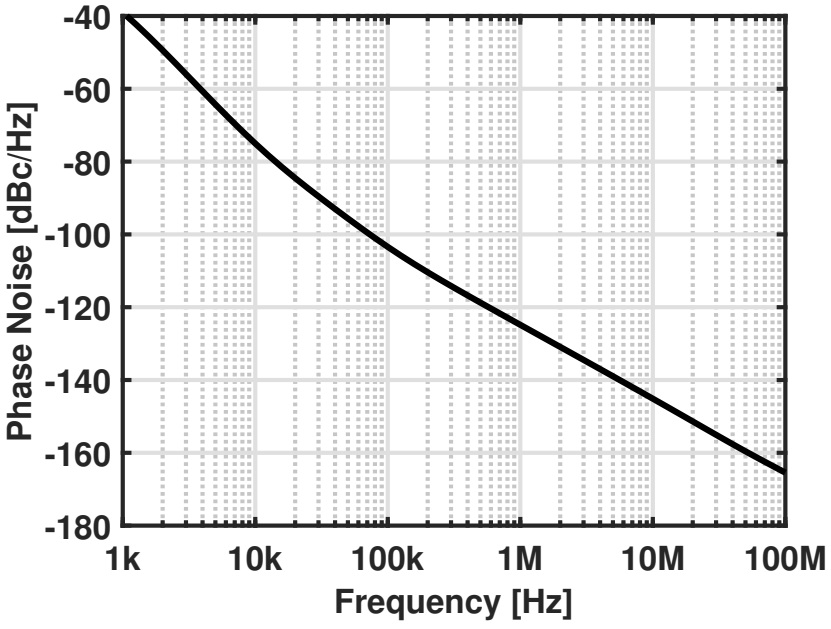


Figure 4.8. Phase noise at various offset frequencies of layout with pads simulation.

Table 4.3. Phase noise in layout with pads simulation.

	Phase Noise (dBc/Hz)
$\Delta\omega_0 = 10$kHz	-75.0
$\Delta\omega_0 = 100$kHz	-103.4
$\Delta\omega_0 = 1$MHz	-124.8
$\Delta\omega_0 = 10$MHz	-145.1
$\Delta\omega_0 = 100$MHz	-165.4

The output differential voltage waveform can also be seen in Figure 4.9. The peak differential output voltage is limited to 0.9V again.

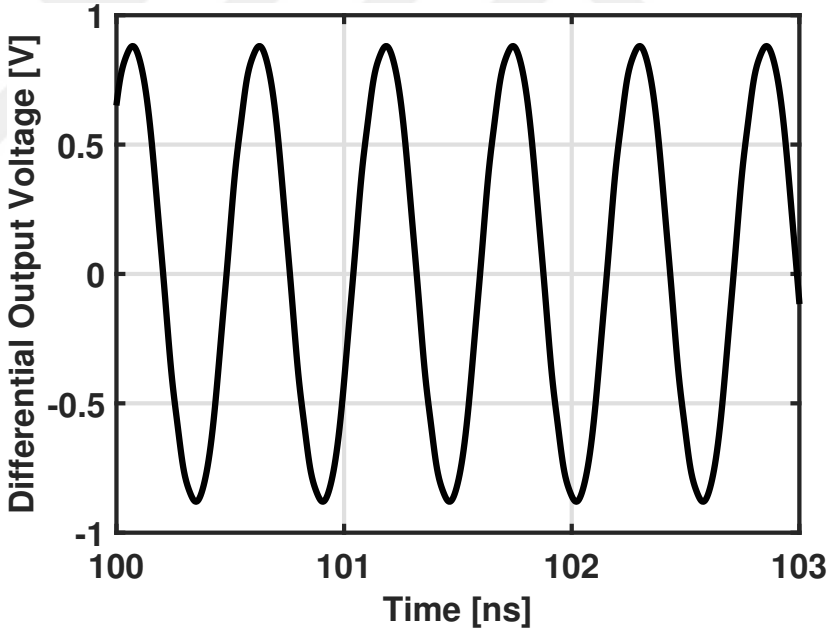


Figure 4.9. Differential output voltage waveform of layout with pads simulation.

The resonator current and the single ended voltage waveform of both output nodes can also be seen in Figure 4.10. The resonator current has almost a square wave waveform whereas output node voltages have a sinusoidal waveform. This is due to resonator suppression of higher order harmonics of current.

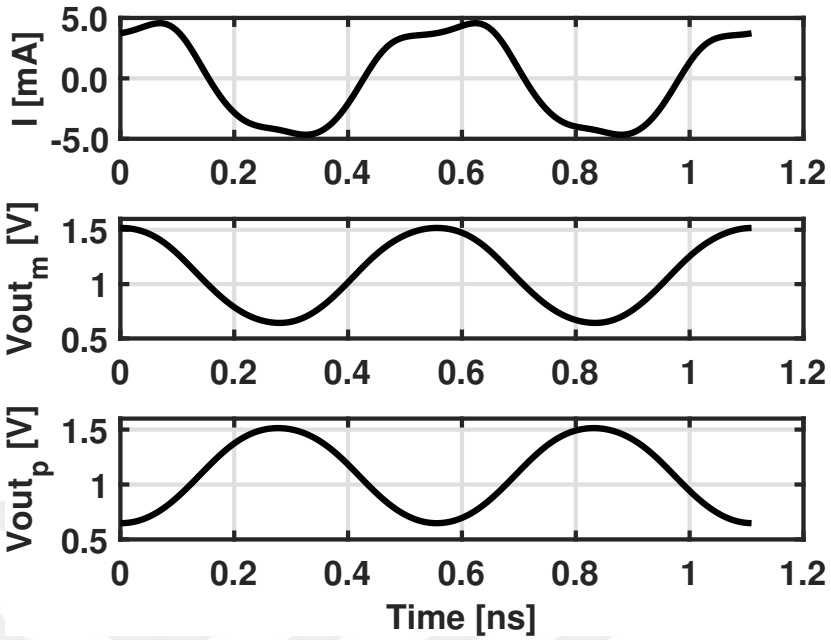


Figure 4.10. Resonator current and both output voltages of two output nodes .

4.4. Comparison of Pre- and Post- Layout Simulation Results

In this chapter, the differences between pre- and post- layout simulation results are shown and discussed.

Figure 4.11 shows the fundamental component of the output voltage. As can be seen, after the final layout including pads, the oscillation frequency is shifted 13.2MHz.

In addition to that, phase noise also changed. Figure 4.12, focuses phase noise at 100kHz offset frequency.

Although, the difference in pre- and post- layout simulation is not so much, one can increase DC bias current to improve phase noise to get better phase noise (see Equation 3.18).

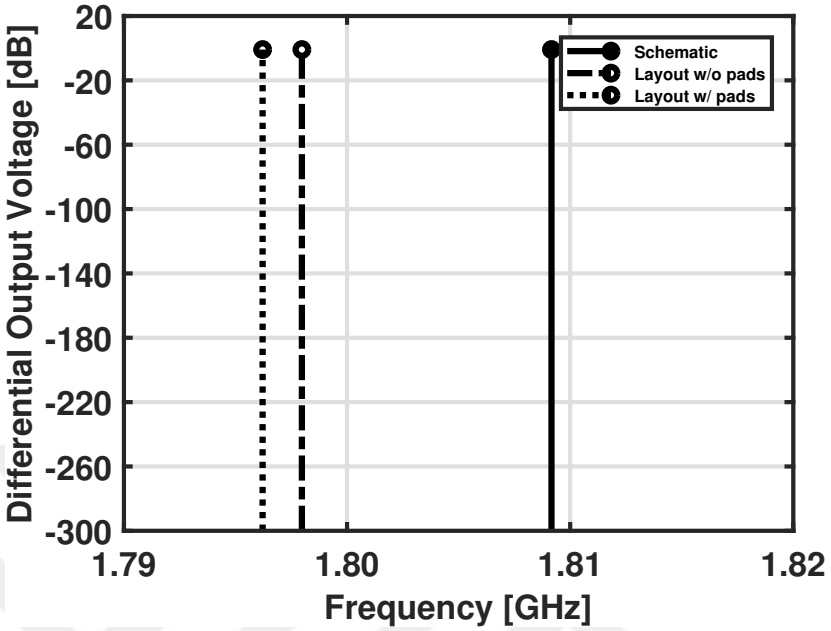


Figure 4.11. Fundamental component frequency shift of output voltage .

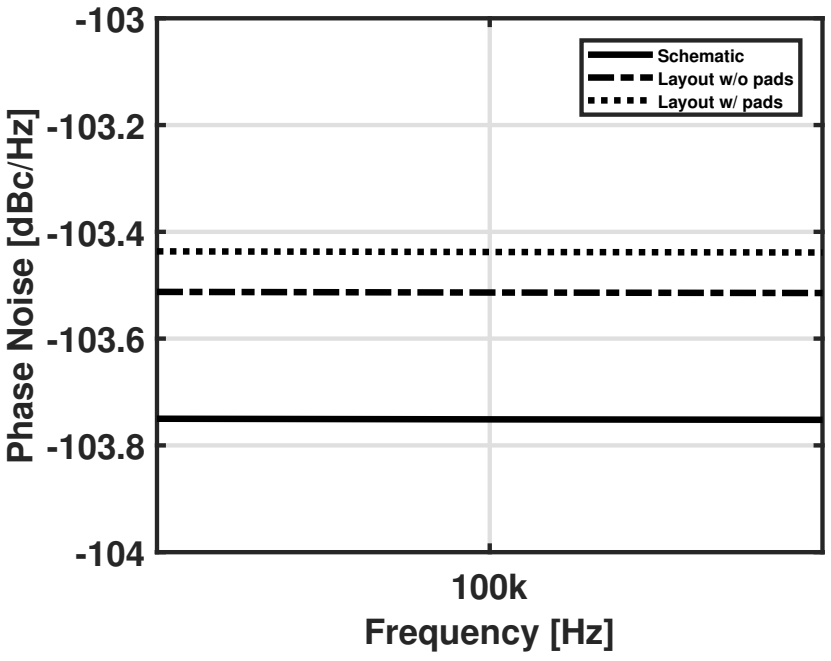


Figure 4.12. Phase noise difference between pre- and post- layout simulations.

4.5. Applications

As explained before, this oscillator is intended to used to detect different materials in a fluid by dropping it to the SRR gap. This changes the SRR resonant frequency by increasing the capacitance of the gap. To simulate this situation, the proposed lumped element model of SRR is used which is explained in Section 2.2.2. The core capacitor is changed to simulate these capacitance changes. The pad extracted circuit is used for simulations. In Figure 4.13, the frequency shift due to the capacitance change can be seen. By increasing gap capacitance of SRR 500fF at each step, the capacitance is totally increased by 2pF which corresponds to a 21.2MHz shift.

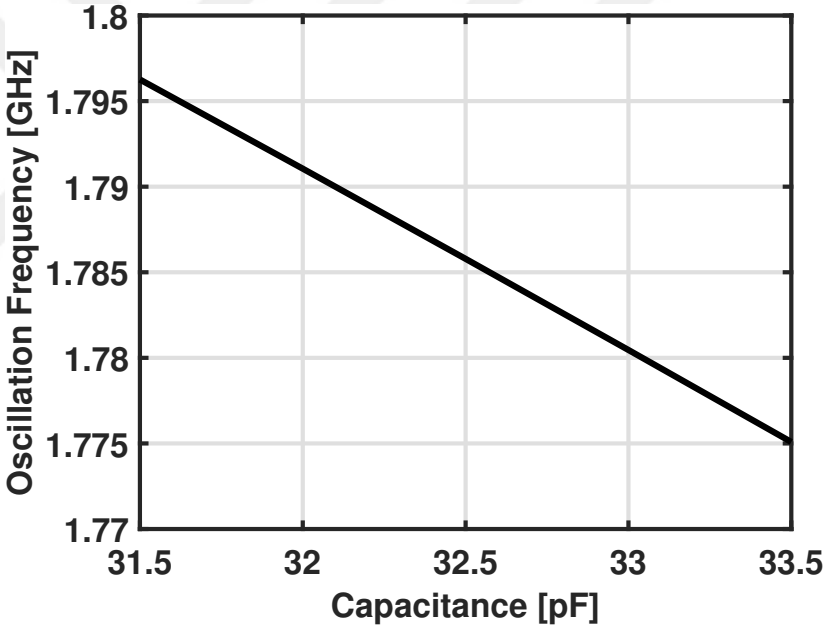


Figure 4.13. Frequency shift by changing gap capacitance of SRR.

Another application consideration is the quality factor variation. Each SRR can have different quality factors due to manufacturing variations. Also, by dropping fluid to the gap, the SRR quality factor can degrade substantially. In Figure 4.14, phase noise at 1MHz offset frequency is given for different the quality factor values of SRR to see the effects of quality factor variation on the phase noise performance of the oscillator. Also, some of the phase noise values for different quality factor values are summarized in Table 4.4. As can be seen from Figure 4.14 and Table 4.4, phase noise

performance does not degrade as long as the quality factor of SRR is approximately greater than 100.

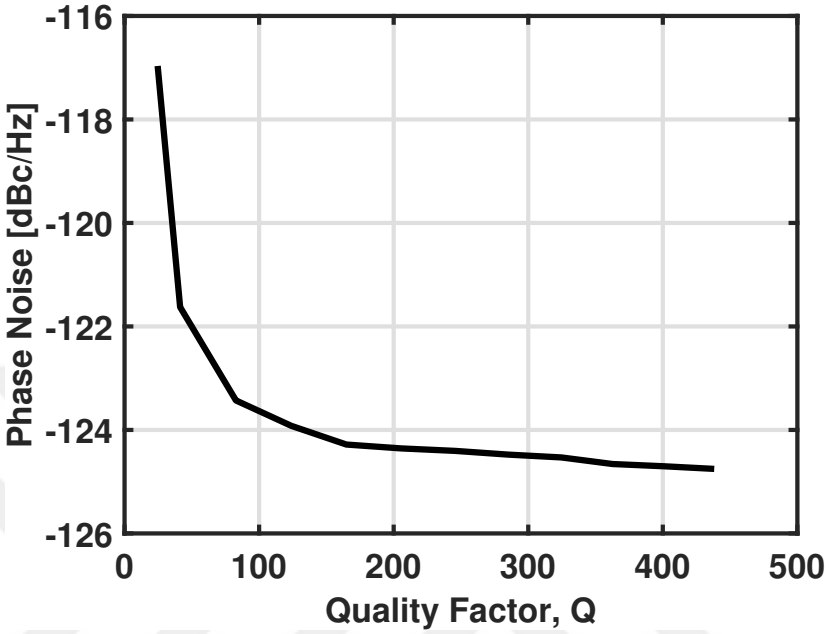


Figure 4.14. Q factor value sweep vs phase noise.

Table 4.4. Phase noise at 1MHz offset frequency for different Q values.

Q	**Phase Noise** (dBc/Hz)
40	-121.6
80	-123.4
160	-124.2
240	-124.4
438	-124.8

4.6. Figure of Merit

A widely used Figure of Merit (FOM) repeated for convenience in Equation 4.1 is adapted for FOM calculations and performance comparisons [29].

$$FOM = L(\omega_m) + 20\log(\Delta\omega_0/\omega_0) + 10\log(P_{diss}/1mW) \tag{4.1}$$

where $L(\omega_m)$, ω_0 and P_{diss} are phase noise at an offset frequency $\Delta\omega_0$, oscillation frequency and power dissipation of oscillator at DC, respectively.

For this work, after pad and layout extraction, FOM is calculated at 1MHz offset frequency as:

$$FOM = -124.8 + 20\log(1MHz/1.796GHz) + 10\log(8.1mW/1mW) \tag{4.2}$$

$$FOM = -180.8dBc/Hz \tag{4.3}$$

and at 100kHz offset frequency as:

$$FOM = -103.48 + 20\log(100kHz/1.796GHz) + 10\log(8.1mW/1mW) \tag{4.4}$$

$$FOM = -179.5dBc/Hz \tag{4.5}$$

Table 4.5 summarizes the performance of similar cross coupled oscillators at 1MHz offset frequency. As described in Table 4.5, the proposed transmission line loaded SRR-metamaterial based complementary cross coupled oscillator shows the state-of-art performance when compared to other SRR-metamaterial based oscillators and traditional LC tank resonators. The oscillators in [29, 46] are the only similar oscillators to proposed one in this work. They are also designed with a SRR-metamaterial based resonators which are, however, on chip resonators. Thus, their operating frequencies, f_0, are at 96GHz and 76GHz, respectively. This is an expected result since the smaller

SRR/CSRR structures shows higher resonant frequencies. Although, they have higher operating frequencies, the phase noise at 1MHz offset frequency is much lower than that of this work. On the other hand, LC tank based oscillator in [47] demonstrates a better FOM since it uses a different technique to lower the phase noise. In [47], a negative resistance multiple-gate circuit (NRMGC) is implemented to lower phase noise -5dBc/Hz which increases the layout area and makes circuit complicated. Also, implementing these technique to our work, a better phase noise and FOM can be reached easily. In [10, 48], a worse or equal performance oscillator are demonstrated. Although these latter examples, especially [10], demonstrates almost equal performance oscillator, our work is superior at 100kHz offset frequency as seen in Table 4.6.

Since SRR has a very steep transfer function, it is expected that the oscillator shows better performance at lower offset frequencies. As offset frequency increases, the noise in the skirts are almost same as other LC tank resonators. As can be seen in 4.6, our work has better FOM than that in [10, 48] at 100kHz offset frequency which proves our claim. On the other hand, although oscillator in [47] is still shows better performance, it is more close to this work at 100kHz.

Table 4.5. Oscillator Performance Summary and Comparison at 1MHz Offset Frequency.

Parameters	**[10]**	**[29]**	**[46]**	**[47]**	**[48]**	**This Work**	**Unit**
f_0	1.2	96	76	2.73	2.22	1.8	GHz
V_{DD}	2.5	1.2	1.0	0.9	1.8	1.8	V
P_{diss}	9.3	7.5	2.7	2.7	18.5	8.1	mW
Phase Noise at 1MHz	-129	-81.6	-75.0	-122.3	-122.5	-124.8	dBc/Hz
FOM	-180.9 [1]	-172.5	-168.3	-186.3	-176.3	-180.8	dBc/Hz
Architecture	NMOS-only	NMOS-only	NMOS-only	PMOS-only	NMOS-only	C.Xcoupled	
Technology	CMOS 350	CMOS 65	CMOS 180	CMOS 180	CMOS 65	SOI 180	nm

[1] Computed from given graphs

Table 4.6. Oscillator Performance Summary and Comparison at 100kHz Offset Frequency.

Parameters	**[10]**	**[29]**	**[46]**	**[47]**	**[48]**	**This Work**	**Unit**
f_0	1.2	96	76	2.73	2.22	1.8	GHz
V_{DD}	2.5	1.2	1.0	0.9	1.8	1.8	V
P_{diss}	9.3	7.5	2.7	2.7	18.5	8.1	mW
Phase Noise at 100kHz	-102	N/A	N/A	-98	-99.9	-103.5	dBc/Hz
FOM	-173.9 [1]	N/A	N/A	-181.9 [1]	-173.6	-179.5	dBc/Hz
Architecture	NMOS-only	NMOS-only	NMOS-only	PMOS-only	NMOS-only	C.Xcoupled	
Technology	CMOS 350	CMOS 65	CMOS 180	CMOS 180	CMOS 65	SOI 180	nm

[1] Computed from given graphs

5. CONCLUSION

In this work, a complementary cross coupled oscillator with transmission line loaded SRR is designed. The SRR used in this oscillator design is an an off-chip SRR-metamaterial based resonator with high quality factor. High quality factor is required to obtain low power low phase noise oscillator which is very suitable for wireless communication as well as biosensing applications among which the latter is the main motivation of this work.

Before using the transmission line loaded SRR in design, a lumped element model is proposed to use the resonator more confidently. Prior to modelling, different lumped elements models are examined. However, none of them are adequate for this work. Thus, a final RLC-only model is obtained by using a intermediate stage model in [30]. In addition to this, the model helps us gain more insight into SRR structure.

Before starting oscillator design, various oscillator architectures are also examined. Instead of feedback oscillators such as Colpitts and Clapp oscillators, the negative g_m oscillators are considered. Due to the SRR used in this work having no transmission characteristics at resonance makes us to use negative g_m oscillators. NMOS-only, PMOS-only and complementary cross coupled architectures are investigated. Due the superior properties of complementary cross coupled architecture, it is adopted. By this architecture, one can obtain a lower power dissipation circuit. Also with IC technologies compatible with low voltage supplies, it can be implemented in this work. Finally, by using the proposed lumped element model and adopting complementary cross coupled architecture, the oscillator is designed. Design procedure is given step by step and the designed oscillator is analyzed in terms of its performance parameters.

The proposed oscillator is designed in 180nm SOI process. The layout area is $80\text{um} \times 94.3\text{um}$ including pads. The resonator is an off-chip resonator and it is intended to be connected to oscillator output pads by using probes to minimize the routing parasitics between the oscillator core and the SRR. The minimization of parasitics are

important because they can lower the quality factor of resonator. The oscillator has a phase noise of 103.5dBc/Hz and 124.8dBc/Hz at 100kHz and 1MHz offset frequencies, respectively. The oscillator core DC current consumption is 4.5mA at a DC supply voltage of 1.8V. Thus, the power consumption is 8.1mW. FOM is calculated as -180.8dBc/Hz at 1.8GHz oscillation frequency.

5.1. Future Work

The main motivation of this work is to demonstrate a low power low phase noise oscillator with a transmission line loaded SRR. A natural extension of this work is implementing this SRR as an on-chip resonator. However, the problem is that when implementing this SRR in an IC technology, the main concern will be the preserving the high quality factor of SRR. As given in [29], the implemented differential transmission line loaded CSRR has a Q of 513 which shows us that this is a reasonable goal. To preserve this high quality, the parasitics resistance should be decreased. This can be achieved by paralleling the metal lines through all SRR structure which decreases the resistance of the lines. Since there exists eight or more metal layer processes, the paralleling all lines can be tried. Another difference is the more smaller structure of SRR when implementing it as a on-chip resonator. This causes frequency shift to very high frequencies. This is due to smaller inductance of on-chip SRR. With inductors covering small area in an IC, the inductance value of SRR decreases substantially. To shift the resonant frequency back, the new ways of increasing capacitance value can be tried. As IC technologies provide, with multiple layer metal structures, fingered splits can be tried to increase total effective capacitance. Furthermore, more splits can be lower the resonant frequency to the desired point. The ring can be splitted from two or more points.

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