DC-DC BUCK CONVERTER FOR TRIBOELECTRIC ENERGY HARVESTING APPLICATIONS

by

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ABSTRACT

DC-DC BUCK CONVERTER FOR TRIBOELECTRIC ENERGY HARVESTING APPLICATIONS

Energy harvesting applications are getting more popular day by day. Self-sufficient circuits which do not require any supply, are more than a luxury for many situations. Usage of the battery can be expensive and not useful because of its large size and the impracticality that results from a need for replacing it in a certain period. Therefore, investments and research on energy harvesting applications are increasing.

Energy can be harvested in many different ways. One of them is triboelectric energy harvesting. With this technique, AC voltage is obtained from triboelectric nanogenerators but its open-circuit voltage can be high as $100V$. Therefore, a system consisting of a bias-flip rectifier, DC-DC buck converter, and a switched capacitor converter is required to obtain usable energy at a low voltage level. This system gradually converts the harvested energy to lower levels.

DC-DC buck converter delivers the 70V energy stored in the capacitor to the switched capacitor converter as 10V DC voltage. The goal is to deliver low input energy ($10\mu - 30\mu$J) of which voltage is $70V$ to the output as efficiently as possible.

In this thesis, an asynchronous buck converter operating in PFM mode is proposed. The sub-blocks are designed to prevent a breakdown caused by high voltage. A specific start-up circuit is designed to start the operation of the proposed buck converter. Each sub-block is shown with its layout and nearly 70% efficiency is obtained.

ÖZET

TRİBOELEKTRİK ENERJİ HASATLAYICI UYGULAMALAR İÇİN DC-DC BUCK DÖNÜŞTÜRÜCÜ

Enerji hasatlama uygulamaları gün geçtikçe daha popülerleşiyor. Birçok uygulama için kendi kendini besleyebilen uygulamalar çoğu durumda bir lüksten ziyade bir ihtiyaca dönüştü. Büyük boyutu ve sürekli değiştirilme gereksiniminden dolayı batarya kullanımı maliyetli ve kullanışsız hale geldi. Bu nedenle, daha az maliyetli ve kullanışlı olan enerji hasatlama uygulamaları alanındaki yatırımlar ve araştırmalar artmakta.

Enerji hasatlamak için birçok yöntem bulunmaktadır. Bunlardan biri triboelektrik enerji hasatlama yöntemidir. Bu yöntemde, triboelektrik çeviricilerden AC gerilim elde edilir ve bu gerilimin değeri 100V gibi yüksek mertebeleri bulabilmektedir. Dolayısıyla, yüksek voltajı kullanılabilir hale getirebilecek rektife devre, DC-DC buck dönüştürücü ve kapasitör anahtarlamalı DC-DC dönüştürücüden oluşan bir sistem gerekmektedir. Bu sistem kademeli olarak yüksek voltajı düşük seviyelere indirger.

DC-DC buck dönüştürücü, giriş kapasitöründe 70V olarak depolanan enerjiyi kapasitör anahtarlamalı DC-DC dönüştürücüye 10V DC olarak verir. Amaç, voltajı $70V$ olan düşük giriş enerjisi ($10\mu - 30\mu$J) olabildiğince verimli bir şekilde $10V$'a dönüştürmektir.

Bu tezde, PFM modunda çalışan asenkron bir buck dönüştürücü sunulmuştur. Alt bloklar, yüksek voltaj nedeniyle bozulmayı önleyecek şekilde tasarlanmıştır. Buck dönüştürücüsünü çalıştırabilmek için bir başlatma devresi tasarlanmıştır. Her alt blok, transistör seviyesi çizimleri ile birlikte gösterilmiş ve yaklaşık %70 verimlilik elde edilmiştir.

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LIST OF ACRONYMS/ABBREVIATIONS

CAD	Computer-aided Design
CCM	Continuous Conduction Mode
CMC	Current Mode Control
DCM	Discontinuous Conduction Mode
ESR	Equivalent Series Resistance
HSS	High Side Switches
LDO	Low Dropout
LSS	Low Side Switches
NMOS	n-type Metal Oxide Semiconductor
Opamp	Operational Amplifier
PMOS	p-type Metal Oxide Semiconductor
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
RC	Resistor–Capacitor
TENG	Triboelectric Nanogenerators
VMC	Voltage Mode Control
ZVD	Zero Voltage Detector

1. INTRODUCTION

Information may be the most powerful asset in today's world. Also, obtaining it has equal importance. Integrated circuits are the essential tools for collecting data from the environment due to their low power usage, small size, and durability. Although the improvements in battery systems are significant for the last decades, they are still not good enough. Batteries, which provide energy to integrated circuits, need to be replaced. They are not durable enough. Moreover, the size of a battery is an obstacle for the products to be smaller. Therefore, systems working without a battery can be more useful. To illustrate, if the temperature data from different locations in a rain forest where humans cannot reach easily is desired to be collected, thousands of integrated circuits have to be placed around the forest. Since it is not easy to collect them all to replace their battery, it is wiser to use a system to harvest energy from the environment.

Depending on the application, different kinds of energy harvesters can be used: thermal, mechanic, solar [6]. Triboelectric energy harvesters are one of these applications used to harvest vibration energy from the surrounding environment. Triboelectric energy conversion devices, defined as triboelectric nanogenerator (TENG), are growing fast. They have many advantages such as high efficiency, light-weight, low cost, and easy fabrication [7]. However, the open-circuit voltage of these harvesters is above $100V$. They are not directly usable because most of the integrated circuits (sensors, transmitters, etc.) use low voltages and get damaged in case of a high supply voltage. Therefore, a harvester circuit must be designed and placed between a TENG and target circuits to convert input power to low voltage levels. Hence, a TENG can be used as a sustainable and usable energy source.

With the periodic process of sliding apart and closing, TENG generates an AC output [8], which is similar to the piezo harvester. In the literature, a bias-flip rectifier is used to convert AC voltage to DC. The converted energy is stored in a capacitor with a buck converter. A circuit used in piezo energy harvesting applications is shown

in Figure 1.1.

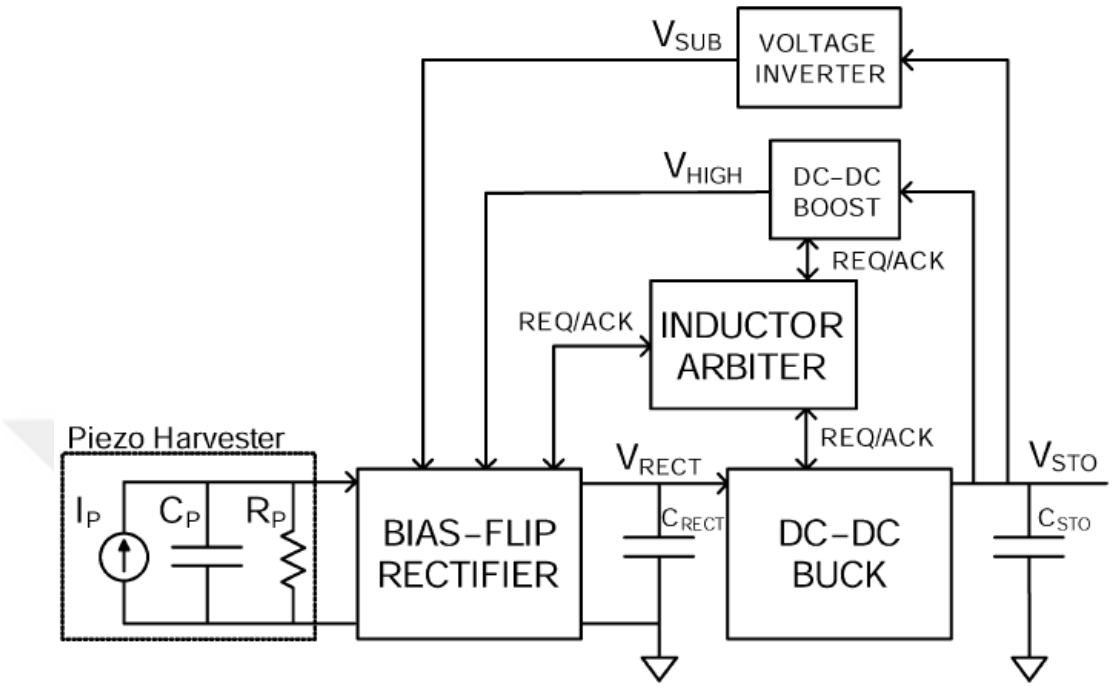

Figure 1.1. The architecture of the bias-flip rectifier system [12]

TENG can give output voltage at a higher level than piezoelectric energy harvesters of which size is the same [9]. Therefore, another method is proposed. If a buck converter converts the output voltage to an intermediate voltage level and a switched capacitor converter is connected to the output of the buck converter, higher efficiency can be obtained. Because it results in a lower ratio of input to output voltage.

The integrated circuit of this new method consists of three blocks: a bias rectifier, a dc-dc buck converter, and a switched capacitor converter. A bias-flip rectifier system is used to convert AC voltage to DC. DC-DC buck converter, which is the topic of this thesis, converts DC voltage to a lower level and transfers it to the switched capacitor converter for further conversions. Finally, a usable output voltage is obtained.

In this thesis, a high voltage DC-DC buck converter is designed for this harvester circuit. The designed buck converter must be able to work with high voltage levels. Otherwise, high voltage can destroy the circuit and decrease the conversion efficiency

severely. Also, this buck converter is designed for low power application. In other words, the size of the used TENG is low and harvested energy is low. Hence, the proposed design should work in case of low harvested energy by consuming power as small as possible.

2. DC-DC BUCK CONVERTERS

2.1. DC-DC Conversion Methods

DC-DC converters are the blocks converting the available DC input voltage to another usable DC output voltage level. It is significant to have higher power conversion efficiency, but also having steady output voltage is equally important too. Generally, a feedback mechanism is used to obtain steady voltage at the output. By sensing the output, the transferred energy from input to output is adjusted so that even if the input voltage changes, the output voltage remains within the desired levels.

Regulation of the output voltage when output current varies is called as load regulation. It is another important parameter to evaluate the system by its rate at which output can be corrected in case of sudden changes in load current. Temperature is also a considerable parameter; however, its effect on the system usually is not drastic [1]. When we consider all of these conditions, it is seen that some systems are superior. There are mainly two types of regulators, linear regulators and switching regulators.

2.1.1. Linear Regulators

Linear regulators which are also called as 'series-pass regulators' or simply 'series regulators' produce regulated output. A transistor placed between input and output rails acts as a variable resistor. The resistance of this transistor is adjusted with a feedback mechanism so that the desired output voltage can be obtained. An example of an LDO regulator is shown in Figure 2.1. Excess voltage is simply $V_{IN} - V_{OUT}$ and it is dropped across the transistor itself. These regulators are step-down regulators in principle and suffer from having poor efficiency.

Average input and output currents are the same in a linear regulator. Therefore, as shown in Equation 2.1, the efficiency cannot be higher than the ratio of input and output voltages. For instance, 12V to 5V down conversion cannot have higher efficiency

than 42%.

$$\eta = \frac{P_O}{P_{IN}} = \frac{V_{OUT} I_{OUT}}{V_{IN} I_{IN}} = \frac{V_{OUT}}{V_{IN}} \tag{2.1}$$

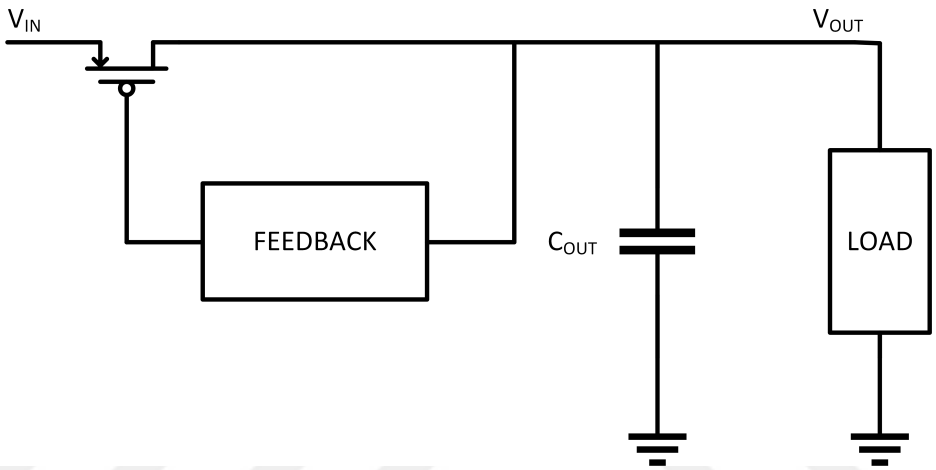

Figure 2.1. Low dropout linear regulator

2.1.2. Switching Regulators

Switching regulators are a type of power supplies using switches. Switches are not held in partially conducting mode as in linear regulators. Instead, they are either on or off and switched repetitively. A switching regulator is shown in Figure 2.2. Input power is transferred to the output and stored in the capacitor and inductor when the switch is at position 1. For the switch position of 2, the stored energy in inductor and capacitor is transferred to the output. If all the elements in the circuit are ideal and have no resistance, the power conversion efficiency becomes 100%.

A modern switching power supply's efficiency can typically range from 65 to 95%. Since traditional regulators like linear regulators provide poorer efficiencies, they are slowly but surely getting replaced by switching regulators [1].

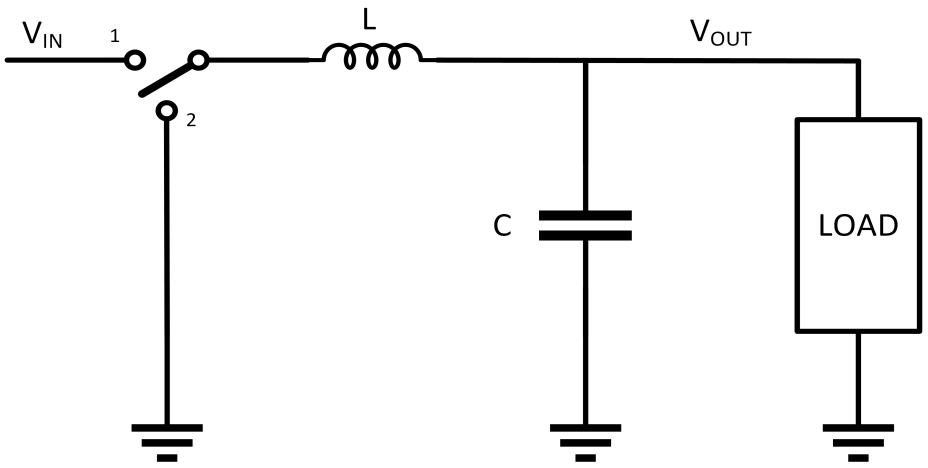

Figure 2.2. Switching regulator

2.2. Principles of Buck Converters

Buck converter is a type of switching regulators. It consists of two switches: An inductor, and A output capacitor, which are given in Figure 2.3. A controller adjusts the timing of the switches and their positions. The switch connected to the input is called a high side switch (HSS). Usually, PMOS is used. If NMOS is used, it becomes harder to drive because the voltage of the source is as high as the input voltage. Gate voltage must be even higher [2]. In Figure 2.3, there is another switch connected to the ground. It is called a low side switch (LSS) and buck converters are categorized into two groups: Synchronous and Asynchronous. If the buck converter has LSS, it is called synchronous. Instead of LSS, a diode can be used. These buck converters are called as non-synchronous (asynchronous). However, usage of the diode gives a larger voltage drop than NMOS. Hence, LSS is commonly used to increase conversion efficiency.

When the switch is closed, current flows through the inductor from the input terminal to the output terminal and increases the output voltage. Inductor current increases gradually during this period and the energy is stored at the inductor and the capacitor. When the switch is open, the current flows from ground to the output and it starts to decrease. The stored energy is transferred to the output. Inductor current/voltage is shown in Figure 2.4. V_{ON} is the voltage at the input terminal of the

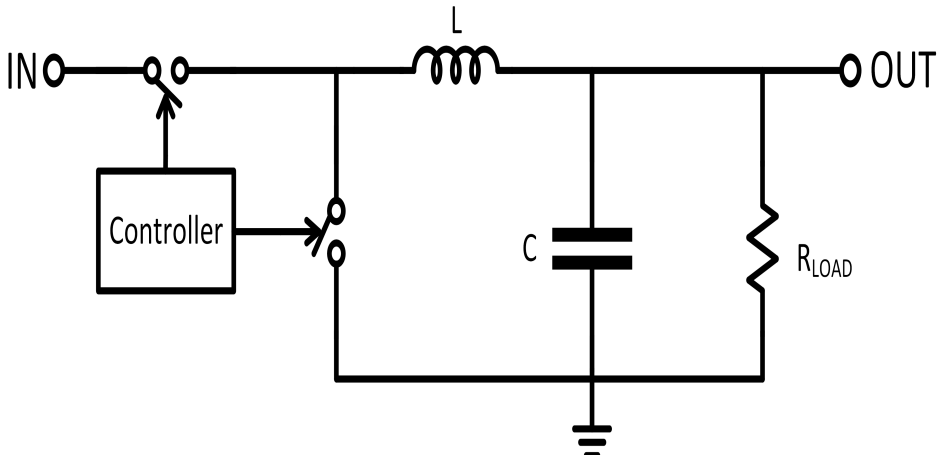

Figure 2.3. Conventional buck converter

inductor when HSS is ON, LSS is OFF. V_{OFF} is the voltage when HSS is OFF and LSS is ON. V_{OFF} is negative since the current flows from the ground to the input terminal.

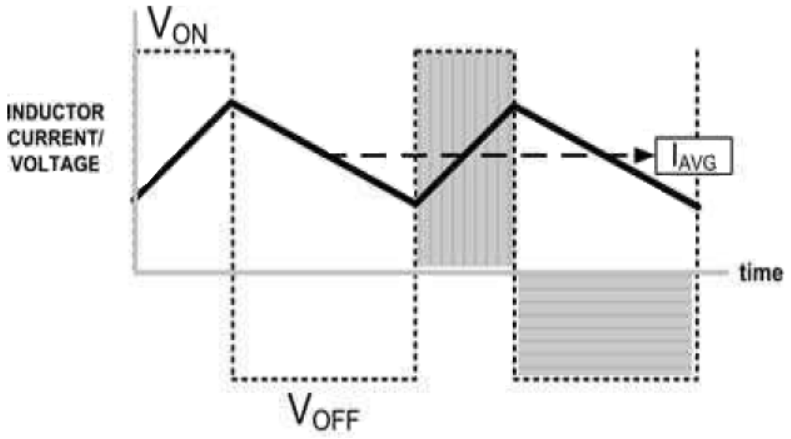

Figure 2.4. Inductor current [1]

The slope of the inductor current can be found with the following equations if the components are ideal.

$$Slope_{rising} = \frac{\Delta I}{\Delta t} = \frac{\Delta V}{L\Delta t} = \frac{V_{IN} - V_{OUT}}{L} \tag{2.2}$$

$$Slope_{falling} = \frac{\Delta I}{\Delta t} = \frac{\Delta V}{L\Delta t} = \frac{V_{OUT}}{L} \tag{2.3}$$

2.3. Operation Modes

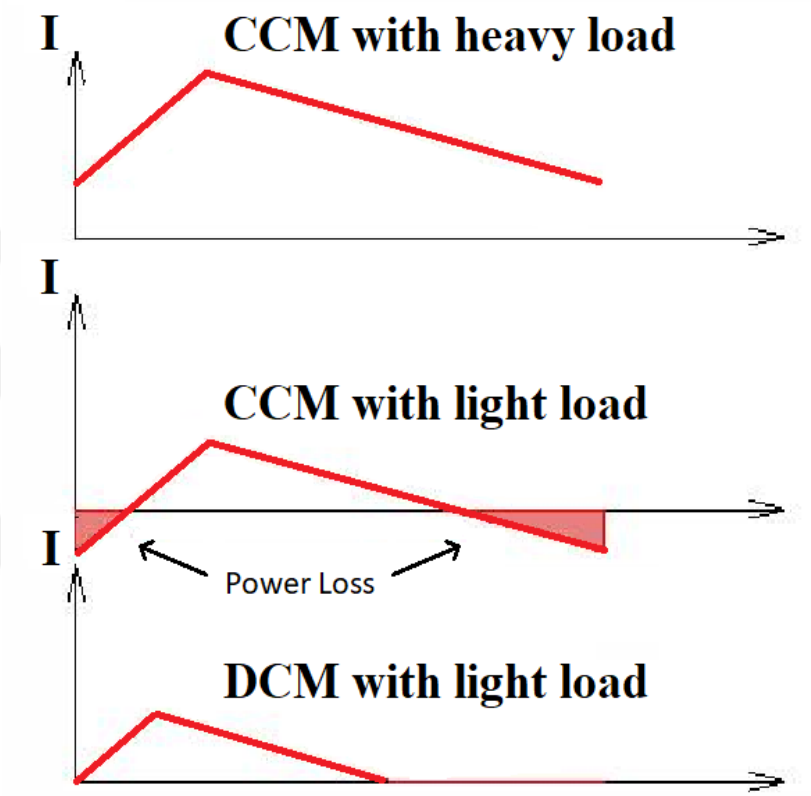

Figure 2.5. Inductor current a) CCM with high current load, b) CCM with low current load, c) DCM with light load

According to the characteristics of the inductor current, buck converters' operation modes are categorized mainly as continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The operation shown in Figure 2.4 is an example of CCM and the average current given to the output is shown with I_{avg}. The inductor current never reaches zero in CCM. However, if the load current decreases, meaning I_{avg} also decreases, the inductor current becomes as in Figure 2.5.b. When the inductor current reaches zero, the current starts to flow from drain to source of LSS. Hence, the shaded area is a power loss. If LSS is turned off, the current does not flow to the

ground. This mode is called DCM and inductor current is shown in Figure 2.5.c. To sum up, the current never reaches zero in CCM, on the contrary, it reaches in DCM.

2.4. Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM)

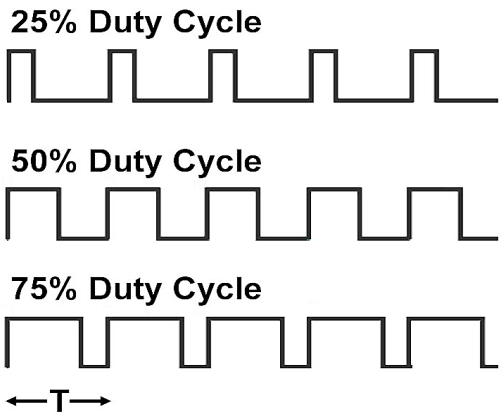

Figure 2.6. PWM signal with different duty cycles

Pulse width modulation is a technique to adjust the duty cycle for delivering the power to the load. An example of a PWM signal with a different duty cycle is given in Figure 2.6. 75% duty cycle results in three times larger power than 25% duty cycle. PWM generator topology in a buck converter is given in Figure 2.7. The error amplifier compares the feedback signal with the reference voltage. The result is compared with a generated ramp signal. The output of the signal is given in Figure 2.8. If the error voltage is high, the HSS is turned on less so that output and error signal does not increase more.

A pulse, of which duration is constant, is generated in pulse frequency modulation. This pulse turns on the HSS, so the frequency of this pulse and the power is delivered to the output are proportional. If the frequency of this pulse is increased, more current and power will be delivered to the output as shown in Figure 2.9.

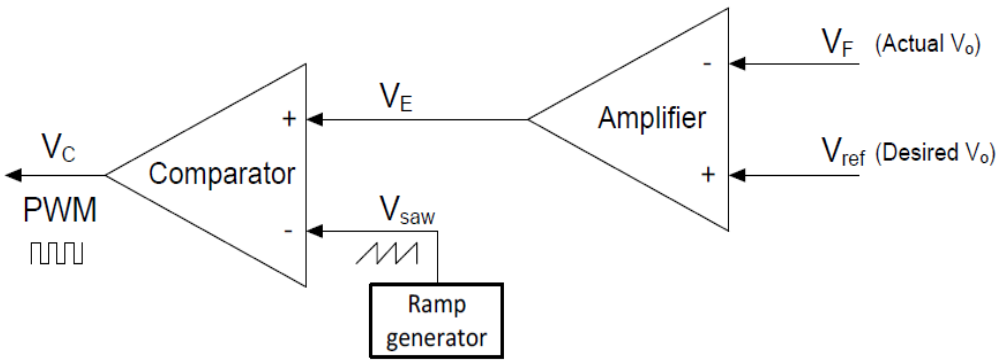

Figure 2.7. PWM signal generator

PWM is used in moderate and high power applications where the duty cycle is larger, while PFM is used in low power applications. If PWM is used for low power applications, switching loss due to the usage of clock dominates the system and reduces the efficiency drastically. PWM is band-limited since there is a fixed-clock but it makes easier to eliminate the voltage fluctuations with a low pass filter. PFM does not have a constant clock. In the case of random load fluctuations, continuous change in control frequency results in higher harmonic distortions and high electromagnetic interference [10].

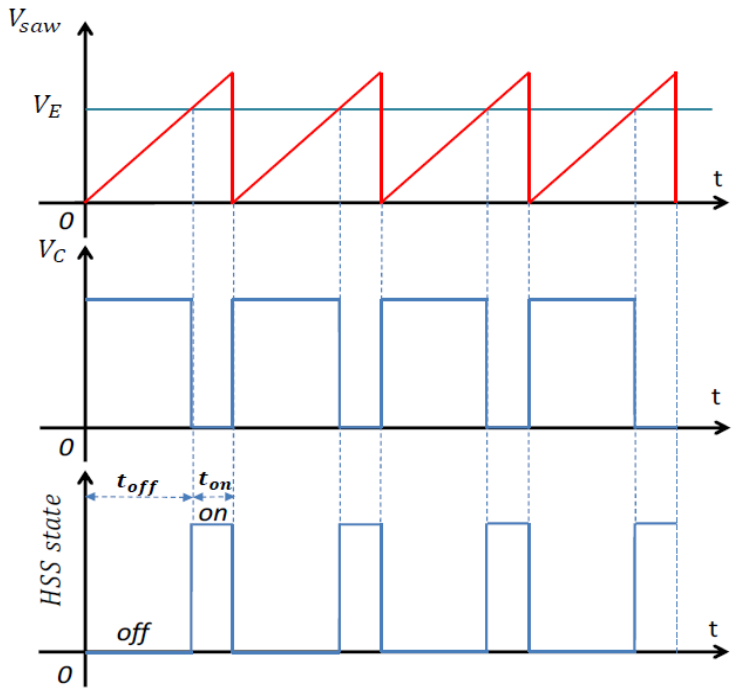

Figure 2.8. PWM signal and HSS control signal

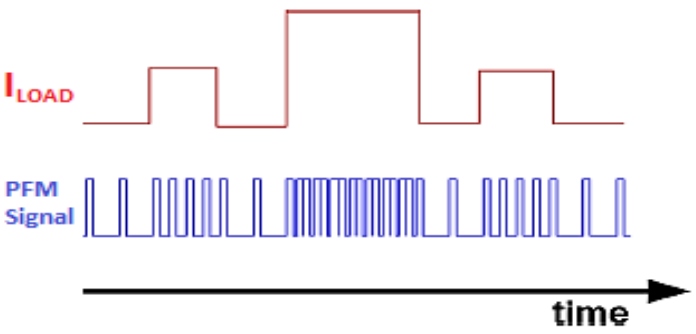

Figure 2.9. PFM for different frequencies

2.5. Feedback Control Loop

There are two types of feedback control topology, which are: Voltage Mode Control and Current Mode Control. The output voltage is regulated with a feedback mechanism to sustain it at the desired level. In order to adjust on/off time of HSS and LSS, the inductor current is sensed in the current mode, while the output voltage is sensed in the voltage mode.

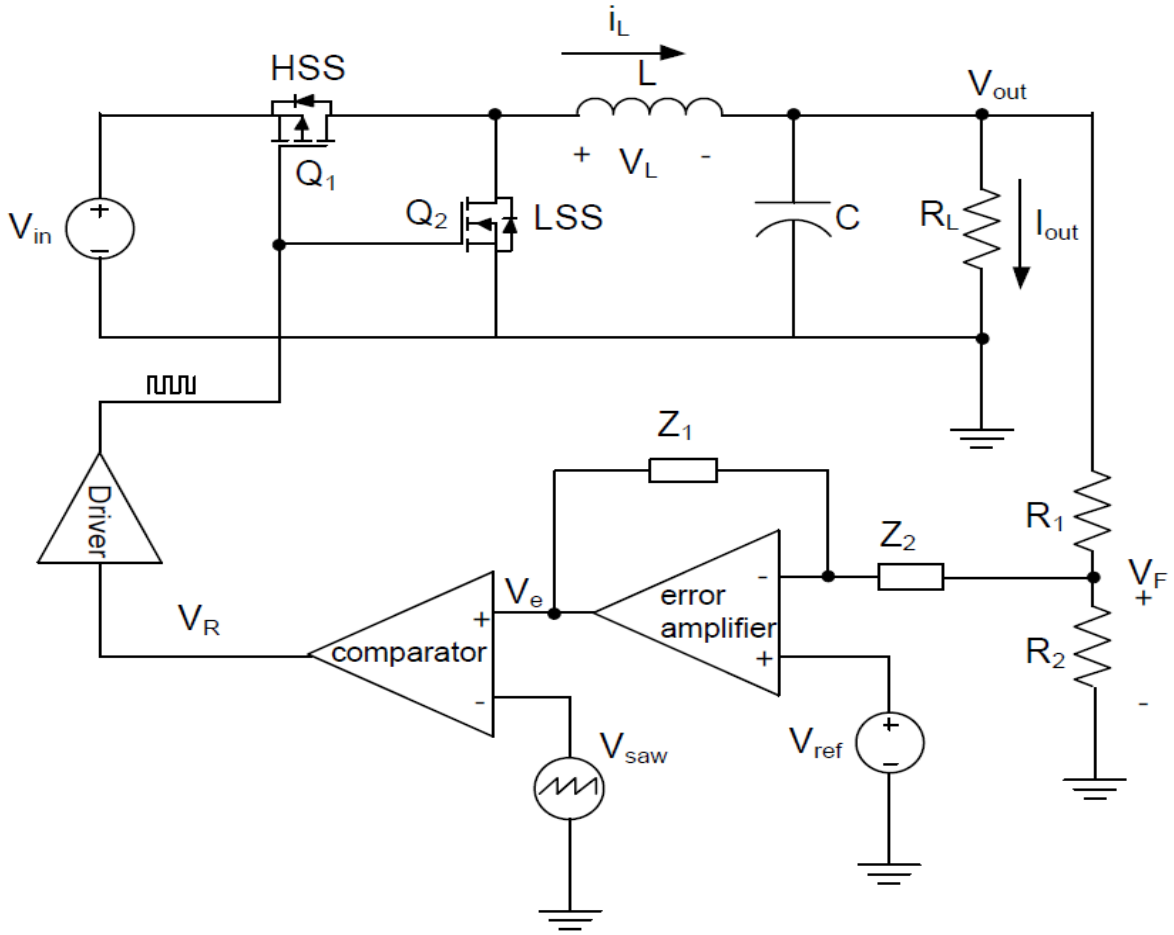

Figure 2.10. PWM buck converter with voltage mode control feedback [2]

2.5.1. Voltage Mode Control (VMC)

The topology of the voltage mode control buck converter is given in Figure 2.10. The output voltage is divided and sensed by an error amplifier. The sensed voltage is

compared with the reference voltage in the error amplifier. The signal is amplified and sent to the plus terminal of the comparator as a voltage error. Sawtooth wave signal is generated and applied to the negative input terminal of the comparator. The error voltage generates the PWM signal as in Figure 2.8 by comparing the sawtooth signal. When the error signal is low, a low duty cycle is achieved, and vice versa.

2.5.2. Current Mode Control (CMC)

The ramp current used in the PWM is not generated in current mode control buck converters. Instead, the ramp signal is generated by benefiting from the nature of the inductor or using the transistor current. The placement of the sense resistor is complicated and affects the overall conversion efficiency. There are two different feedback loops. The first one is the inner feedback loop which senses inductor current and regulates the peak current. The second loop is the external loop which senses and regulates the output voltage.

Current mode controlled buck converter is given in Figure 2.11. Inductor current is sensed and given to the comparator with a resistance. The error voltage is compared with $R_S I_L$ and the output is given to the SR latch. When the sensed voltage exceeds the reference voltage, the SR latch's output becomes zero. A generated clock signal is given to the SR latch in order to reset it and prepare the SR latch for the next cycle.

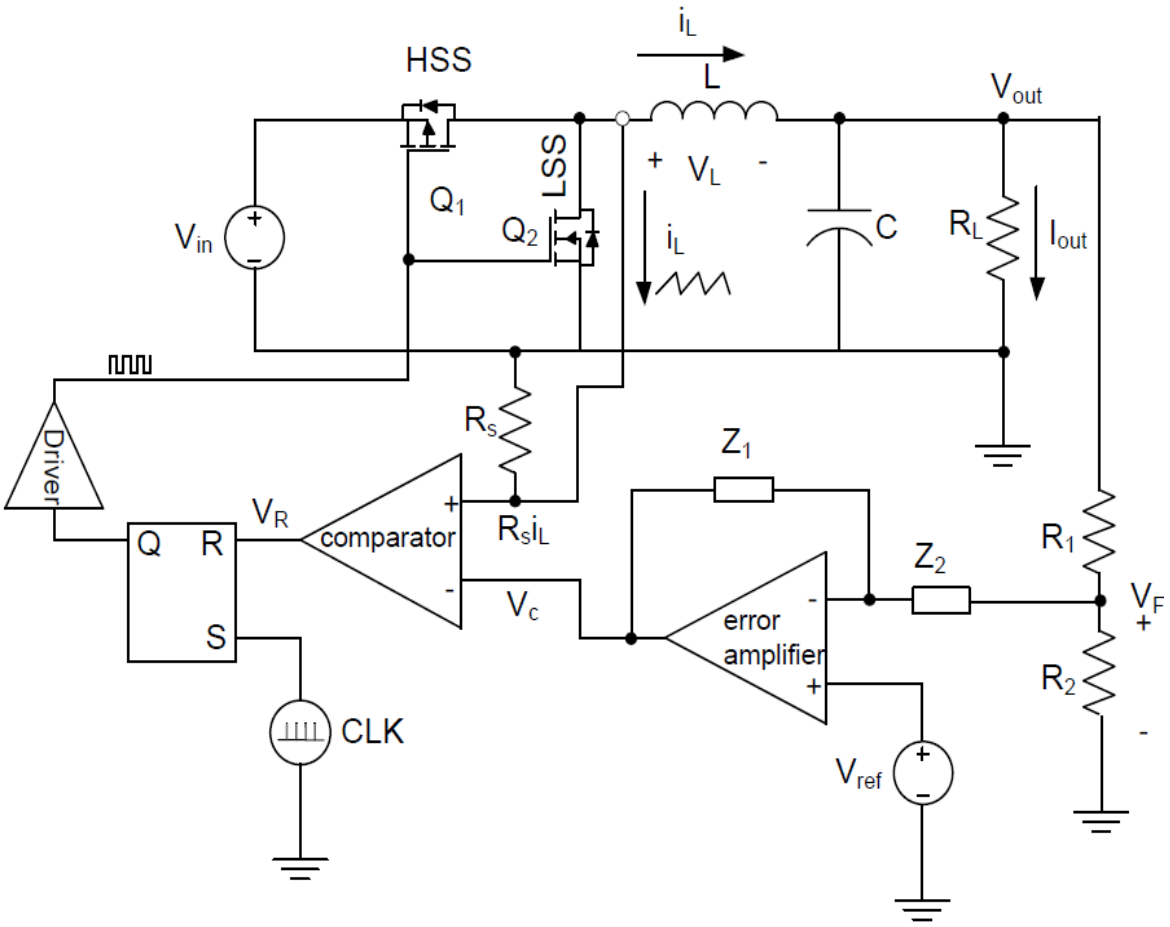

Figure 2.11. PWM buck converter with current mode control feedback [2]

2.6. Power Loss

The efficiency in a buck converter is the main concern of the designers. Even if the topology of the buck converter changes, the common main power loss source are the switches themselves. The main power flows through these switches to the output. Any resistance or voltage drop at the current path is a loss. The total loss in the switches can be determined by conduction and switching loss which are obtained as follows:

$$P_{SwitchLoss} = P_{con} + P_{sw} \tag{2.4}$$

For HSS (PMOS), conduction loss (P_{conHSS}) and switching loss (P_{swHSS}) can be described as:

$$P_{conHSS} = I_{out}^2 R_{DS(on)} D \tag{2.5}$$

$$P_{swHSS} = \frac{V_{IN}.I_{out}}{2}(t_r + t_f)f_{sw} + (C_{DS} + C_{DG})f_{sw}V_{in}^2 \tag{2.6}$$

where I_{out} is the output current, $R_{DS(on)}$ is the on-resistance of the transistor, D is the duty cycle that HSS is turned on, t_r and t_f are rise and fall time, $C_{DS} + C_{DG}$ is the parasitic capacitance at the drain terminal of HSS (PMOS), f_{sw} is the switching frequency. For LSS, $(1 - D)$ is used instead of D in Equation 2.5 because the current flows through LSS for $(1 - D)$. Moreover, V_F which is Schottky diode voltage drop is used instead of V_{IN} [11].

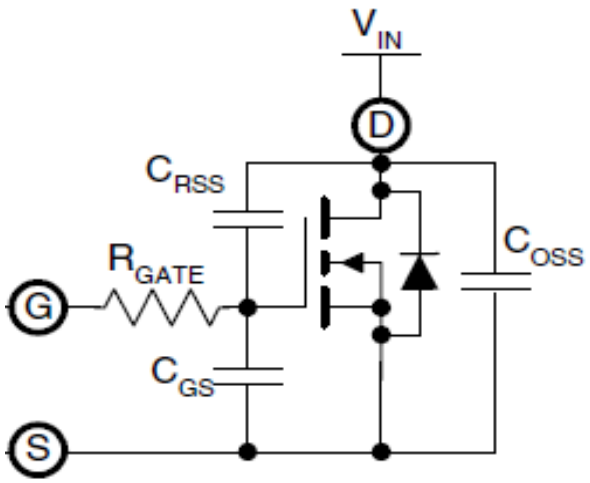

Figure 2.12. An example of HSS [3]

An example of HSS is given in 2.12. If V_{GS} voltage increased, V_{DS}-I_D graph is obtained as shown in Figure 2.13, where $C_{ISS} = C_{GS} + C_{RSS}$. When V_{GS} reaches V_{TH}, C_{ISS} begins to charge and I_D rises linearly. During t_2 NMOS sustains the entire input voltage across itself. In t_3, V_{DS} begins to fall and the gate current charges C_{GD}. During this time current is constant while V_{DS} is decreasing. $I_D \times V_{DS}$ is large for the shaded area which is the switching loss area. The loss in t_1, t_4, and t_5 is much less compared to this area. Therefore, it can be safely ignored [3]. The similar situation is observed in LSS. LSS is turned on when the current becomes zero and starts to flow in other direction. Turning on/off situations are shown in Figure 2.14.

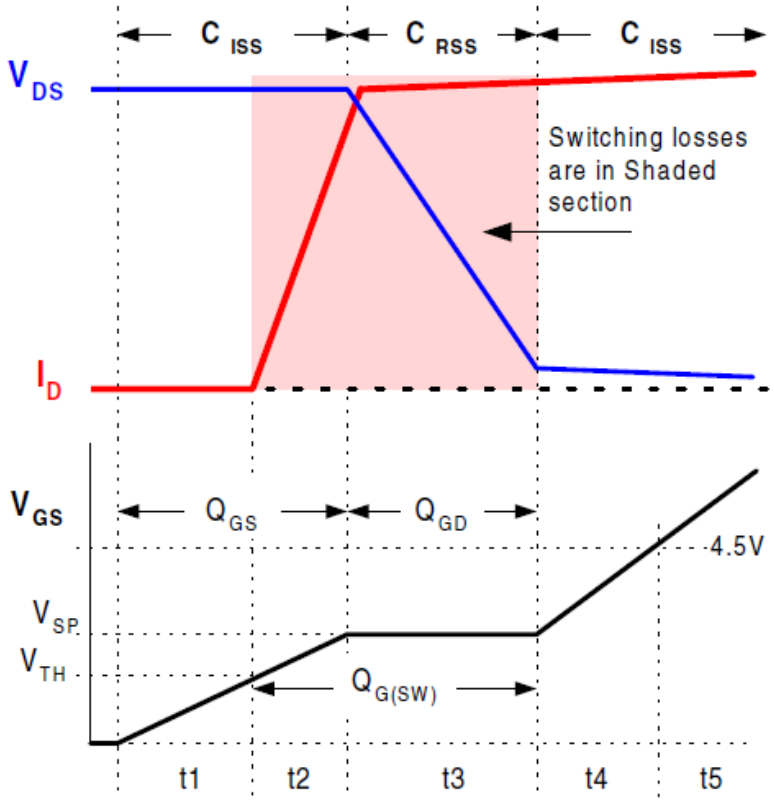

Figure 2.13. High side switching loss [3]

2.7. Stability

A compensation circuit should be added to the error amplifier, or else variation at the output may result in an unstable circuit. In order to design a good compensation circuit, there are a few design rules to follow, which are enlisted below.

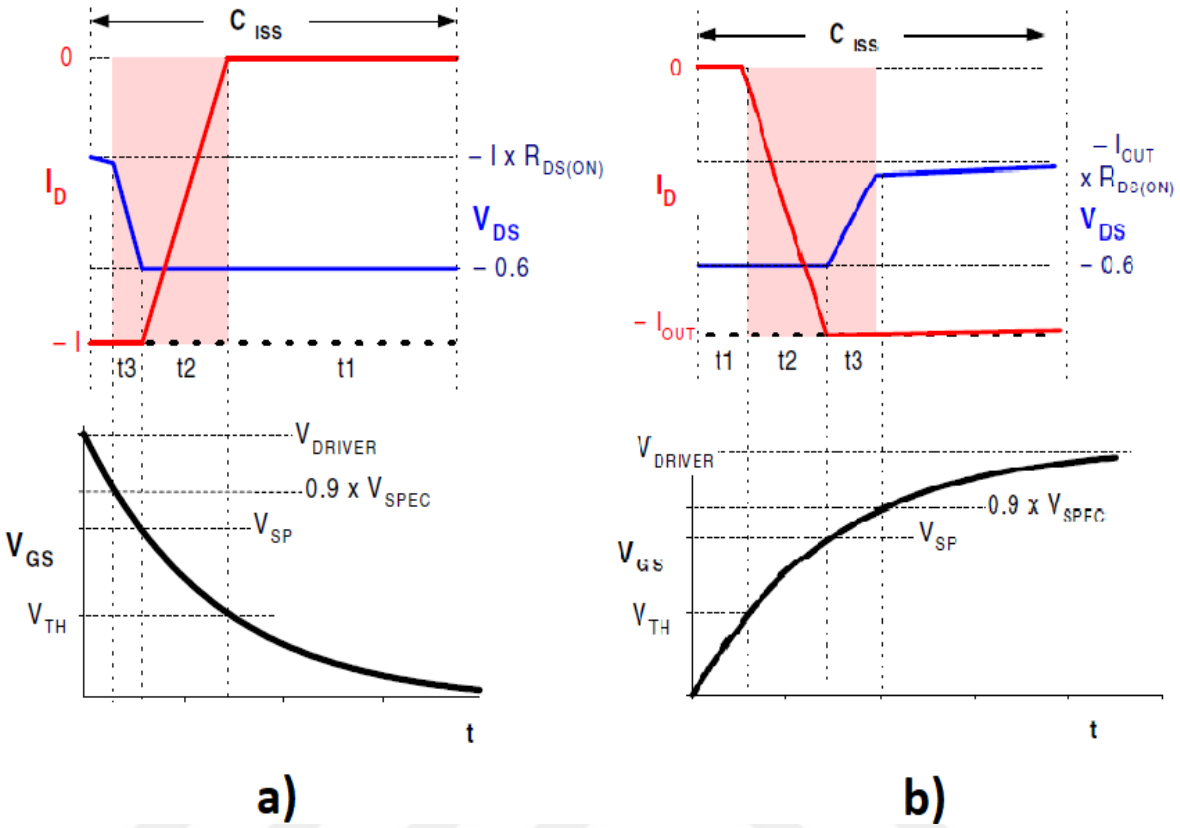

Figure 2.14. Low side switching loss waveforms. [3] a)Turn on switching loss. b)Turn-off switching loss

- The phase margin should be at least 45° to 60° [3].
- The system should have gain margin maximum $-6dB$ to $-12dB$. Less than $-12dB$ is better.
- The cross over frequency should be less than switching frequency. Otherwise, the switching noise and the ripples are reflected in the output. Preferably, 0.2 or 0.2 of f_{sw} is used as crossover frequency [3].

Lower phase margin results in faster transient response and shorter settling time while it causes ringings and overshoots. There is a trade-off between these specifications. Generally, the phase margin is chosen as 60°. Bode plot of the open-loop system gain is shown in Figure 2.15. F_{LC} is the double pole of an LC filter. A zero is located at F_{ESR} due to the output capacitor and its ESR. This system may be unstable and requires a compensation circuit.

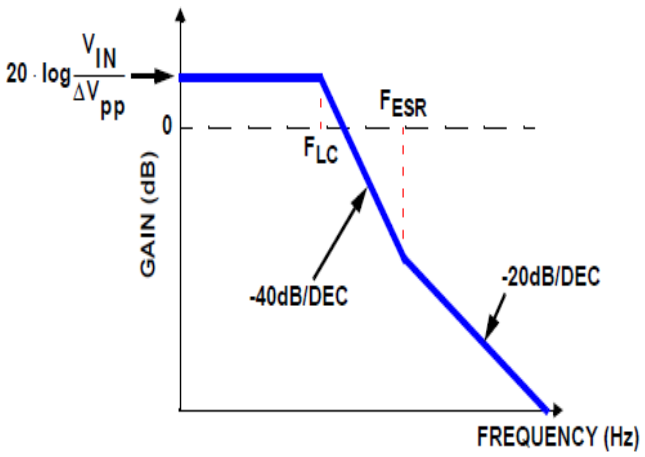

Figure 2.15. Open-loop system gain [3]

Three types of compensation circuit are used in the buck converter; type-I, type-II, and type-III. Type-I is referred to as single-pole compensation which is not useful because of its limited bandwidth and low phase margin. Type-II and type-III are more preferable. If F_{ESR} is low, the phase boost provided by ESR can be used. Hence, type-II compensation is preferred. However, if F_{ESR} is high, meaning ESR is small, type-III is preferred due to its 180° phase boost.

2.7.1. Type-I Compensation

Type-I compensator is given in Figure 2.16. It is a simple integrator Opamp creating a pole at the origin. R_{BIAS} is used to adjust the steady-state value of the output but does not have an effect on amplifier gain. The transfer function is given in Figure 2.17.

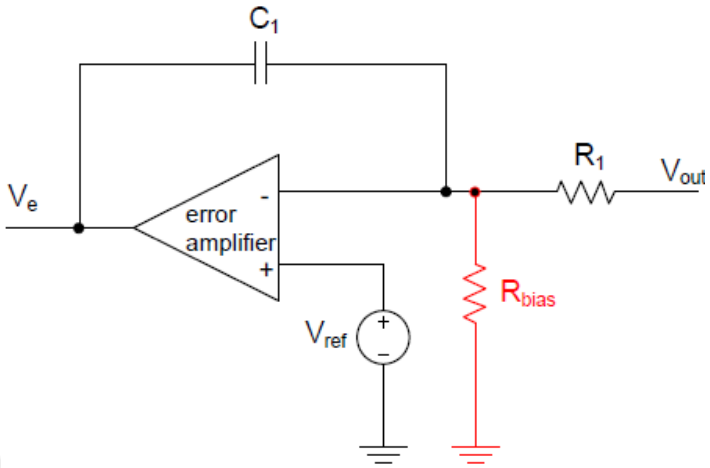

Figure 2.16. Type-I compensation circuit [3]

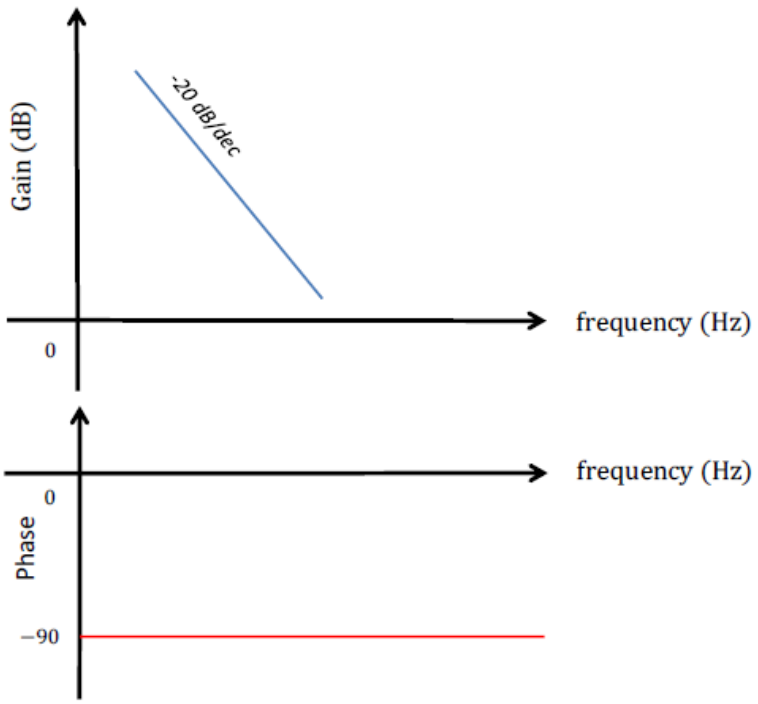

Figure 2.17. Bode plot of type-I compensation circuit [3]

2.7.2. Type-II Compensation

When ESR is high and provides enough phase boost, type-II compensation is preferred. Schematic of the type-II compensator is given in Figure 2.18. R_1 and C_1 create a pole while R_2 and C_2 create a zero. Also, the parallel combination of C_1 and $R_2 + C_2$ create a pole. The bode plot and the locations of the poles and zeros are given in Figure 2.19. The integral part is used to obtain high gain at lower frequencies resulting in low DC error. By employing zero, 90° phase boost is provided. Moreover, the increased crossover frequency causes the bandwidth to widen and fast transient response of the system is obtained.

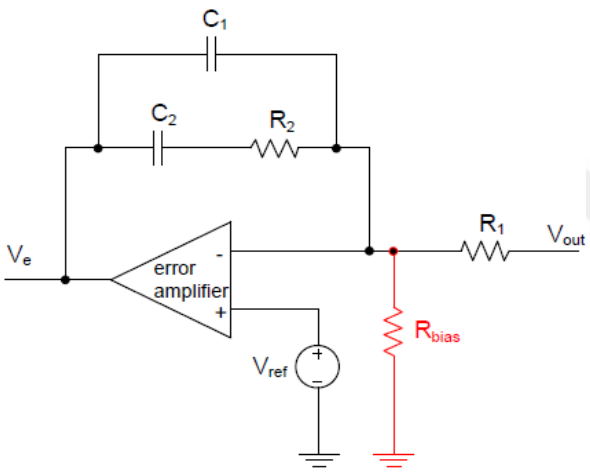

Figure 2.18. Type-II compensation circuit [3]

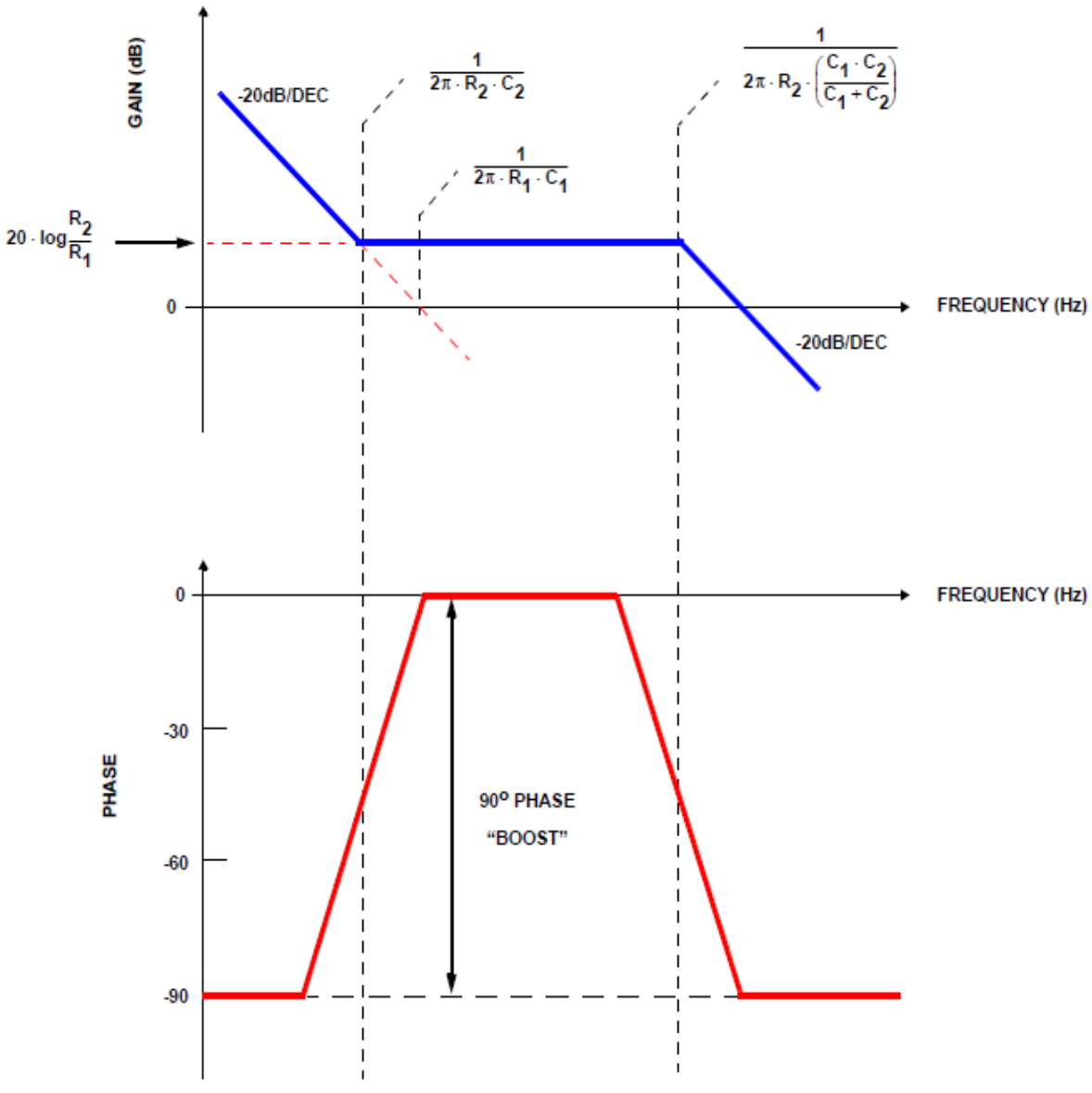

Figure 2.19. Bode plot of type-II compensation circuit [3]

2.7.3. Type-III Compensation

If ESR is small and cannot provide the necessary phase boast, type-III compensation is preferred. Schematic of the type-III compensator is given in Figure 2.20. The compensator provides a pole at the origin and two pole-zero pairs. The bode plot and the locations of the poles and zeros are given in Figure 2.19. Similar to type-II, the integral part is used to obtain high gain at lower frequencies. By employing two zeros, 180° phase boost is provided and the crossover frequency increases.

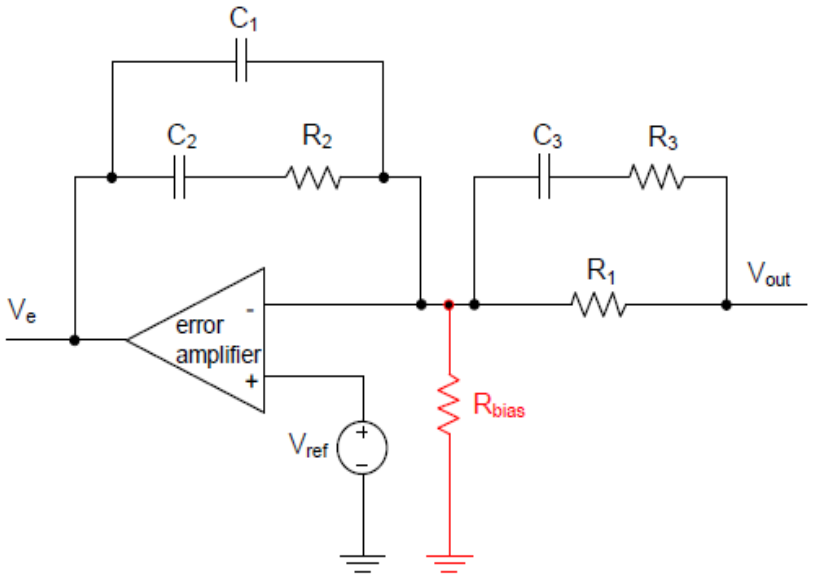

Figure 2.20. Type-III compensation circuit [3]

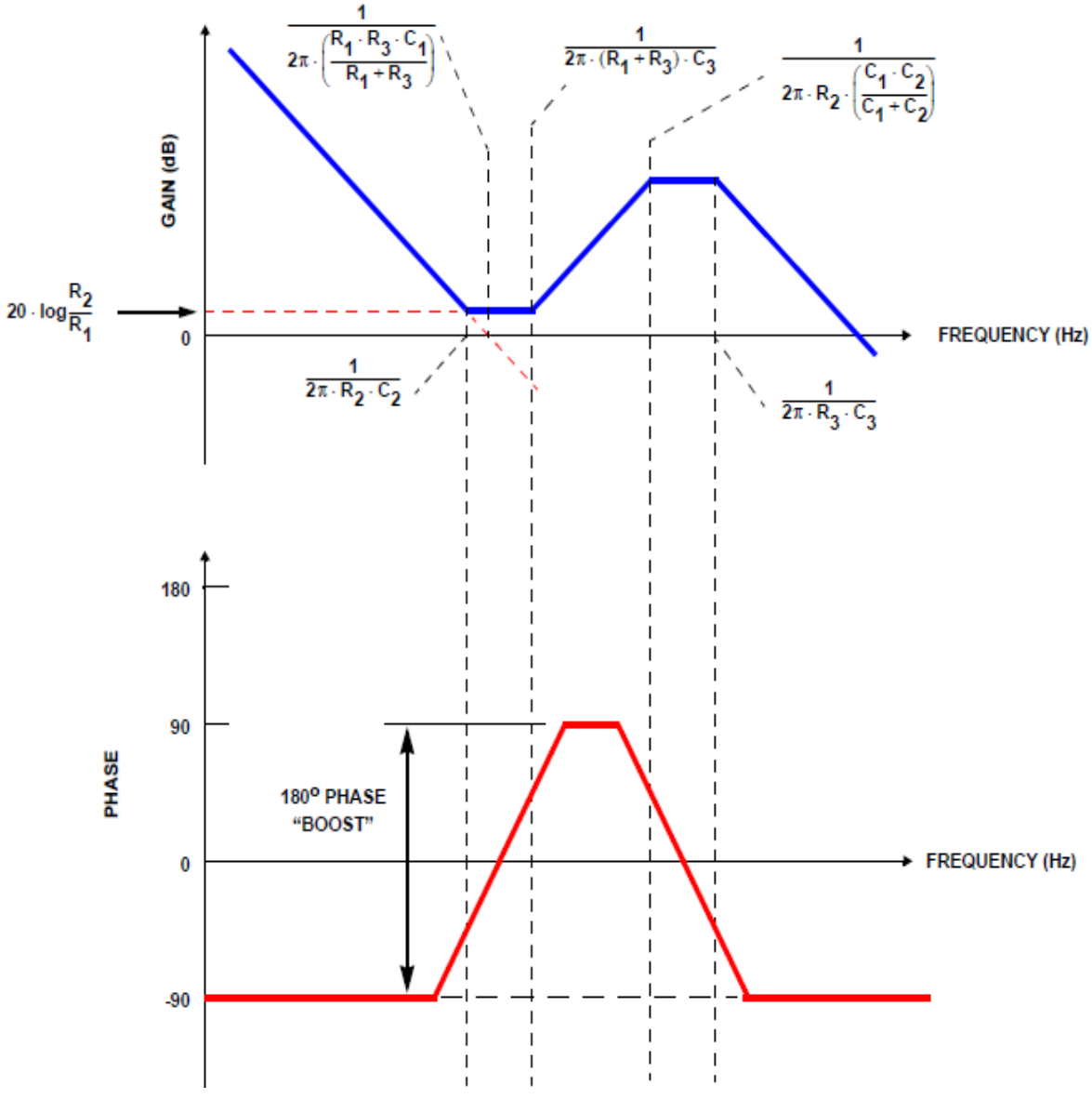

Figure 2.21. Bode plot of type-III compensation circuit [3]

3. 70V to 10V DC-DC BUCK CONVERTER FOR LOW POWER ENERGY HARVESTING APPLICATIONS

3.1. Introduction

The proposed buck converter is a part of a system that converts harvested energy by triboelectric nanogenerators (TENG) to 2V. The top-level design consists of three blocks: Bias-flip Rectifier System, DC-DC Buck Converter, and Switched Capacitor Converter. The architecture is given in Figure 3.1. As a bias-flip rectifier system, the circuit similar to [12] is used. The harvested energy is stored in the C_{IN} capacitor. The buck converter converts the energy stored in C_{IN} to $10V$ DC. The switching capacitor converter receives the converted energy and delivers it to the load as $2V$ so that usable energy is obtained for low power integrated circuits.

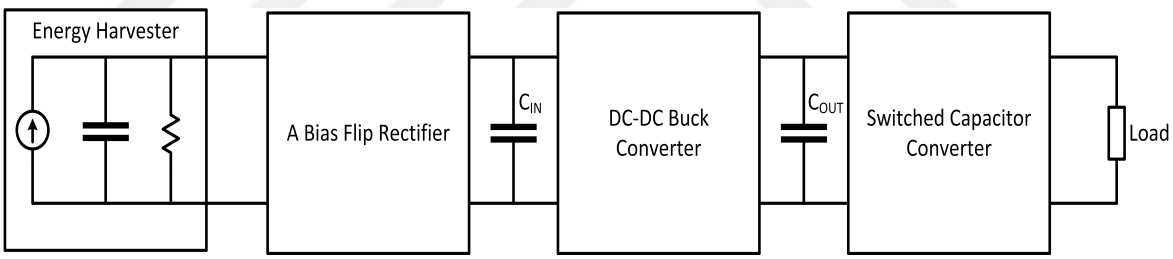

Figure 3.1. Triboelectric energy harvesting circuit

The size of used TENG, which is produced at the cleanroom of Bogazici University Micro Electro Mechanical Systems Laboratory (BUMEMS), is small so it cannot provide high power. The designed bias-flip rectifier circuit and TENG charges $10\eta F$ capacitor (C_{IN}) from $0V$ to $70V$ in roughly $5s$. Therefore, it better to charge a capacitor up to a certain voltage level and transfer the energy to the output only for a brief time so that a large current can be delivered to the load. If the power is delivered to the output for $7 - 8ms$ or more, low power circuits like a temperature sensor can successfully operate.

$5V$ is used in the sub-blocks as a voltage source. The whole system supply itself without requiring an external voltage supply. However, $5V$ is generated in a switched capacitor converter which is the last block of the converter. Therefore, the sub-blocks cannot work because they do not initially have any available power. To overcome this difficulty, an LDO regulator is designed in the bias-flip rectifier system. LDO provides only limited power to the system. It is not a good idea to use the power obtained by LDO too much because it converts harvested energy to $5V$ in an inefficient way.

There are a few challenges to overcome. First of all, the available power is low as it is mentioned before. Secondly, it is a high power application. If the transistors are not biased correctly, a breakdown occurs easily. Lastly, the sub-blocks do not have the initial supply power to operate at the beginning of the conversion.

3.2. Architecture

To begin with, the design specifications are determined and given in Figure 3.1. A bias-flip rectifier circuit is connected to the input of the buck converter and it charges the input capacitor up to $70V$. When the input capacitor is charged to $70V$, a start signal is given to the buck converter and the conversion starts.

Table 3.1. The design parameters of the proposed buck converter

Parameters	**Values**
Maximum Input Voltage	$70V$
Output Voltage	$10V$
Maximum Output Voltage Ripple	$\pm 10\%$
Maximum Output Current	$150\mu A$
Minimum Efficiency	70%

Buck converter is controlled with pulse frequency modulation (PFM) because the available power is low. The schematic of the buck converter is given in Figure 3.2. The output voltage is sensed by a voltage divider circuit and the sensed voltage is given

to the plus terminal of the comparator. The comparator compares the sensed voltage and the reference voltage. A reference voltage is already generated inside the switched capacitor converter block by a bandgap voltage reference circuit. The buck converter's reference voltage is also provided by the same circuit. When V_{SENSED} is smaller than V_{REF}, pulse generator block gives a pulse for certain time. If V_{REF} is still larger than V_{SENSED}, after a certain time, another pulse is given to the level shifter. If V_{SENSED} is larger than V_{REF}, no pulse is generated at all. Pulse generator, comparator, and voltage sense provide a PFM like in Figure 2.9.

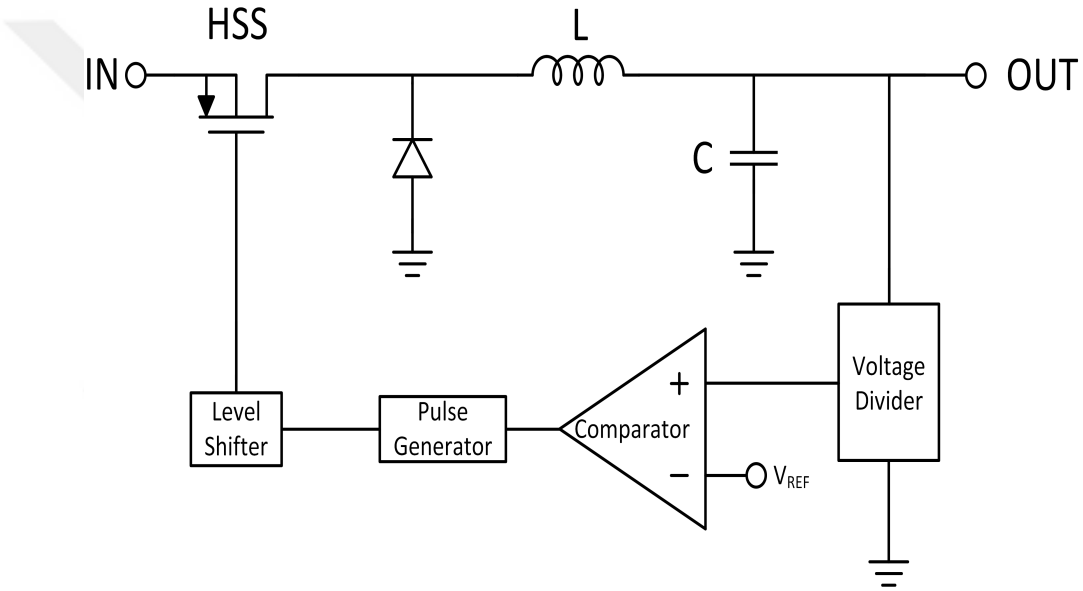

Figure 3.2. Blocks of the proposed buck converter

The level shifter is required for HSS. In TSMC 0.18μm BCD technology, the voltage difference between the source and gate voltage should not exceed $5V$. Otherwise, a breakdown occurs in the transistors and damages the circuit severely. Therefore, a circuit is required to adjust the gate voltage of HSS. If the output of the pulse generator is $5V$, the gate voltage of the PMOS (HSS) must be equal to the source voltage turn HSS off. If the output of the pulse generator is $0V$, the gate voltage should be $5V$ lower than the source terminal.

Instead of using a freewheeling diode, an NMOS (LSS) can be used. However, an NMOS brings additional complexity to the circuit. In order to turn off the LSS, it

will be necessary for zero current or a voltage detector circuit. Addition of these extra blocks brings extra current consumption and prevents an increase in efficiency since the available voltage is too low. Hence, asynchronous buck converter topology is preferred and a freewheeling diode is used. The detailed analysis will be done in "Comparison of Asynchronous and Synchronous Buck Converter" section in the next chapter.

One thing to notice in the design is that the buck converter starts to convert energy when $C_{IN} = 70V$ and stops when it becomes $10V$. Because of the decreasing energy in the input capacitor, the input-output voltage ratio decreases as the buck continues to operate. It is stated in Equation 2.2 that the slope of the rising inductor current depends on input-output voltage difference. Therefore, the slope decreases with decreasing input voltage. Since the pulse width generated in the pulse generator is constant, the peak current and the transferred energy to the output in each pulse decreases. As a result, the switching frequency increases as the input voltage decreases. It brings a larger switching loss. This is the drawback of the topology. However, the stored energy in the input capacitor is proportional to the square of the voltage ($\frac{1}{2}CV^2$). It means that lesser power is stored for the low input voltage so this drawback does not affect the efficiency crucially. Until the input voltage gets smaller, a large portion of the power is delivered to the output with high efficiency.

3.3. Sub-blocks

3.3.1. Input Capacitor

It is desired to deliver power to the output for at least $7 - 8ms$ long. If the conversion is assumed to be done in 100% efficiency, minimum input capacitor which stores the required energy is found as follows,

$$\begin{aligned} \textit{Stored Energy in } C_{in} &= \textit{Delivered Energy to the Load} \\ \frac{1}{2}CV_{in}^2 &= V_{out}I_{out} \times t \end{aligned} \tag{3.1}$$

$$C_{in} = 2\frac{V_{out}I_{out} \times t}{V_{in}^2} = 2\frac{10V \times 150\mu A \times 8ms}{70^2V} \\ = 4.9\eta F \tag{3.2}$$

Minimum input capacitor value would be $4.9\eta F$ if the conversion efficiency was 100%. However, there is a power loss in the converter that must be taken into account. On the one hand, a smaller capacitor may not be sufficient; on the other hand, the larger the input capacitance is, the longer it takes to charge. The input capacitor value is chosen as $10\eta F$ because it is not too large to charge and too small to provide output for less than $8 - 9ms$

3.3.2. Level Shifter

As the buck converter operates, the input energy is transferred to the output, resulting in decreasing input voltage. The turn-on voltage of HSS should be $5V$ lower than input voltage even if the input voltage changes. It is better to benefit from charge pump topology. The level shifter [4] in Figure 3.3 is used.

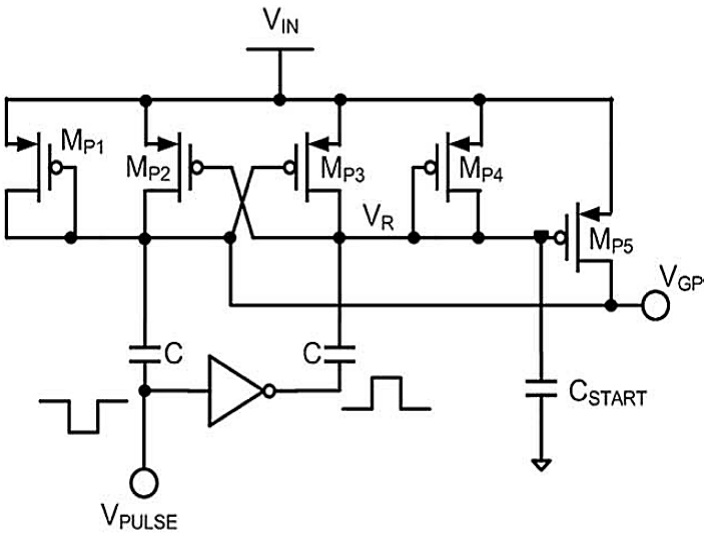

Figure 3.3. Level shifter in the literature [4]

In this topology, V_{GP} is directly connected to one of the latches and it is forced to follow input voltage changes. The circuit works only for applications where fast switching occurs. Otherwise, the output voltage always rises and reaches V_{IN} because of the diode-connected transistors.

V_{PULSE} charges the capacitor and V_{GP} becomes equal to V_{IN}. When V_{PULSE} becomes zero, V_{GP} becomes equal to $V_{IN} - V_{DD}$, where V_{DD} is the supply voltage of the inverter. M_{P5} is used to speed up the rising transient response of V_{GP}. Because of the large parasitic capacitance, C values are chosen as large. Otherwise, the desired drop cannot be provided due to charge sharing. Large capacitance results in slow output changes so it is a good idea to charge V_{GP} with M_{P5}, especially for high-speed applications. However, the proposed buck is used for a low power energy harvesting application. It is not a power-hungry circuit, meaning that it operates slowly. Therefore, another topology is proposed which is shown in Figure 3.4.

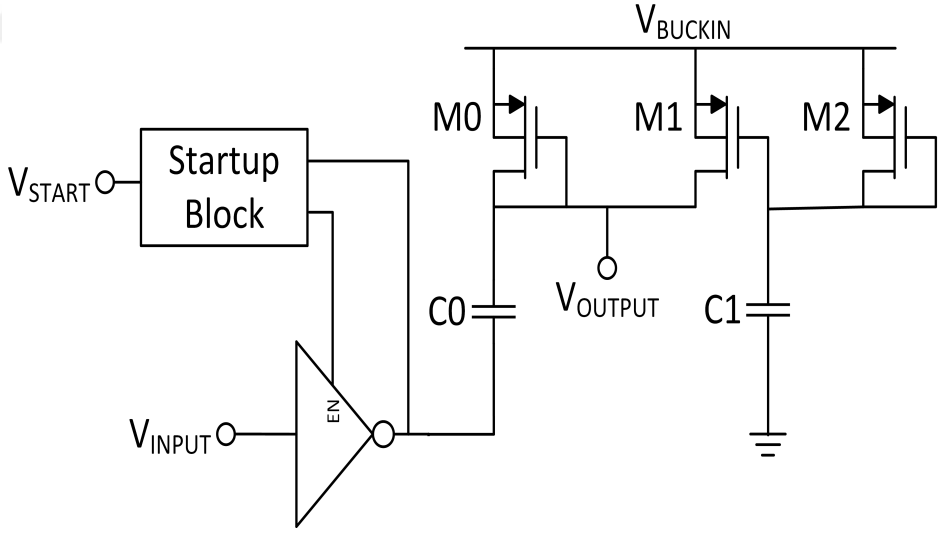

Figure 3.4. The proposed level shifter

When the output of the inverter is $5V$, the capacitor is charged. When it is $0V$, it is discharged by leaving a $5V$ voltage drop at V_{SG} of $M0$. W/L of diode-connected M_0 and M_2 are too small to prevent the voltage to rise quickly. $M1$, $M2$, and C_1 do not have any effect during the operation of the converter.

V_{BUCKIN} is the input voltage of the converter. From 0V to 70V, it is charged by a bias-flip rectifier system. During that time, V_{OUTPUT} must be equal to V_{BUCKIN}, meaning the source voltage of the PMOS (HSS) must be equal to its gate voltage. Otherwise, HSS is turned on and the current flows through it. The input capacitor cannot be charged. To prevent this situation to occur, $M1$, $M2$, and C_1 are connected as shown in Figure 3.4. Sizes of M_0 and M_2, values of C_0 and C_1 are the same. A large transistor, M_1, is used to make V_{OUTPUT} following V_{BUCKIN} during the charging period. If V_{BUCKIN} increases, it makes a voltage difference between gate and source terminals of M_1 so C_0 charges quickly. When the conversion starts, V_{BUCKIN} decreases gradually so that M_1 is never turned on again. This topology works for only this application, where V_{BUCKIN} charges slowly and never increases again during level shifter's operation.

Capacitor values are chosen by considering parasitic capacitance of gate terminal of PMOS (HSS) connected to the output of the level shifter. If there were no load, the output voltage drop becomes $5V$. However, because of the charge sharing between C_0 and the parasitic capacitance, the voltage drop is less than $5V$. The more the values of C_0 is, the more the voltage drop is. There is a trade-off. If the C_0 is large, charging and discharging take longer resulting in larger switching loss in HSS. Moreover, more charge is discharged to the ground resulting in higher energy dissipation. Therefore, it is better to choose C_0 small. $15pF$ is chosen because it results in $3.5V$ voltage drop when the inverter's output is $0V$.

The start-up block is used to turn on HSS at the beginning of the conversion. It is supplied by an LDO regulator. Because the way LDO regulators convert power is inefficient, this energy is not used in any other block of the buck converter. It is responsible for charging C_0 to $5V$ for once and discharge again so that V_{OUTPUT} becomes $65V$, where $V_{BUCKIN} = 70V$. The start-up block is shown in Figure 3.5.

NAND2 gate receives "start signal" directly and the inverse of "start signal" with a delay. The system gives high impedance to the output. When "start signal" changes from $0V$ to $5V$, the output becomes $5V$ until delayed inverse of "start signal" is $0V$. The duration of the pulse should be enough to charge the output capacitor. The values

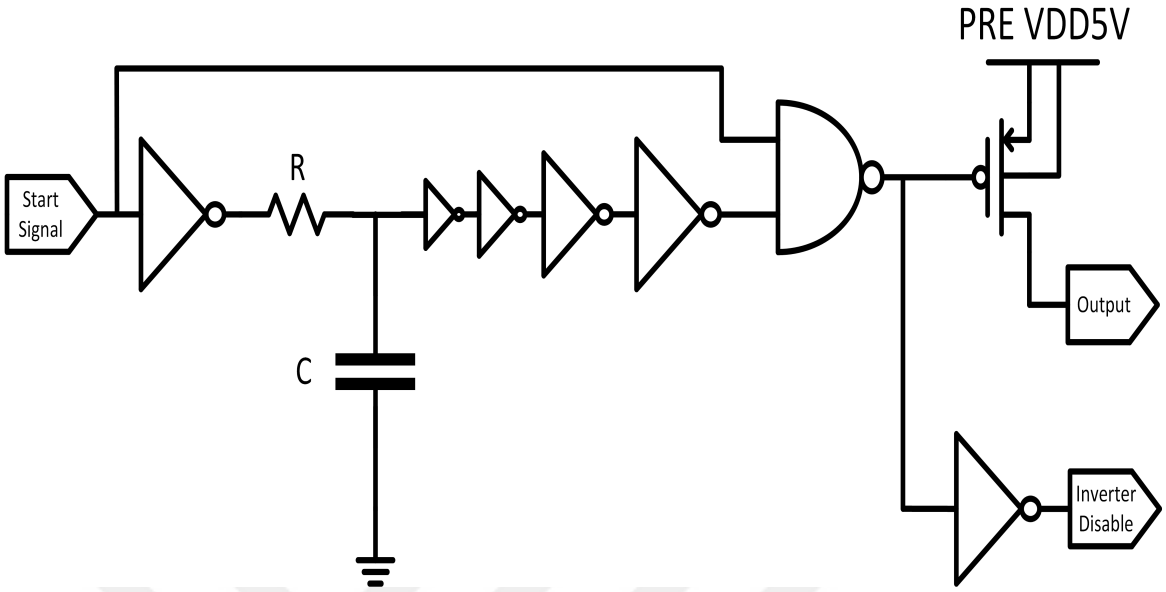

Figure 3.5. Start up block of the level shifter

of the resistor and the capacitor determine the delay if the inertial delays of the gates are neglected. PMOS connected to the output is turned on for this delay long.

There is a drawback about this circuit. Since the output of the resistor-capacitor circuit (RC circuit) changes its state slowly, a direct current path is established in the inverter connected to its output for a long time. Both of PMOS and NMOS of the inverter are turned on at the same time. If W/L ratio of transistors of the inverter is chosen small, this current and power loss can be minimized.

A tri-state inverter is required for this application to separate normal operation and start-up operation of the buck converter. A tri-state inverter used commonly in the literature is shown in Figure 3.6. A drawback of this circuit is the higher V_{OL} and higher fall time because it has an additional cascoded NMOS. IF the output of the inverter is connected to a higher voltage than $0V$, the voltage drop will be less than calculated. An alternative circuit is proposed in Figure 3.7.

When the start-up circuit supplies $5V$ to the level shifter's capacitor, NMOS and PMOS must be turned off. If an NMOS (M_{N5}) is connected between two inverters as in

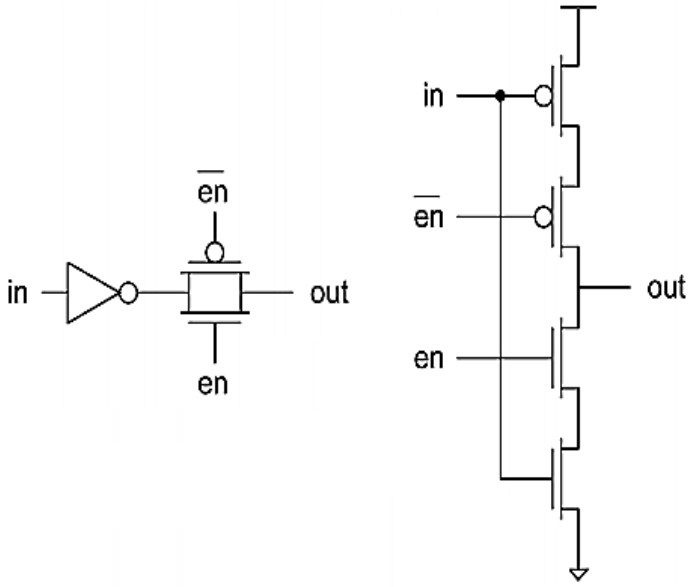

Figure 3.6. Tristate inverter in the literature

Figure 3.7, the output inverter can be turned off. The problem is that, when the start-up signal arrives, the supply voltage of the digital blocks ($VDD5V$) is zero. Therefore, the current flows through the body diode of PMOS to $VDD5V$. A PMOS with bulk regulation M_{P3} is cascoded in order to blockade this path. Thanks to bulk regulation, the bulk is always connected to the highest potential. In a start-up operation, the highest potential is the output itself, not $VDD5V$ which is zero initially. Another PMOS (M_{P2}) is connected with its bulk regulation circuit to the first inverter. It is connected there as a measure. It is not required but in a possible case, if an undesired start-up signal comes during operation of the buck converter, M_{N5} is turned on and the direct current path is established between V_{DD} and ground through M_{P0} and M_{N5}.

A diode may also be connected instead of M_{P1} in order to prevent unwanted discharge. However, the usage of a diode results in a larger voltage drop ($0.7V$) across its terminals than a PMOS. The output of the inverter becomes $4.3V$ instead of $5V$ during the operation of the buck converter, assuming $VDD5V = 5V$. As a result, V_{SD} of $M0$ in Figure 3.4 becomes less than $5V$ and the HSS is turned on with less V_{SG} voltage.

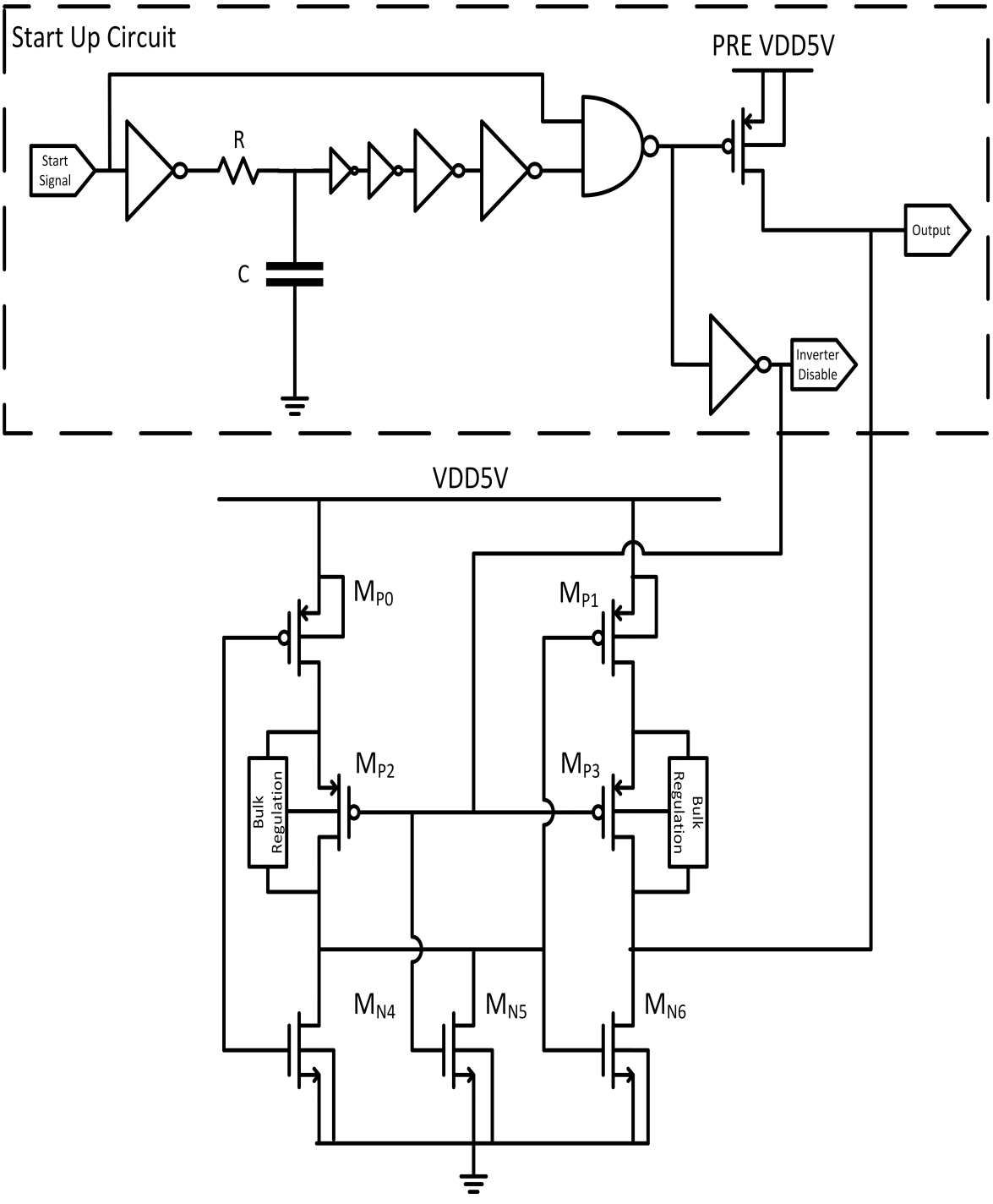

Figure 3.7. The proposed digital block of the level shifter

The bulk regulation circuit is given in Figure 3.8. In the literature, it is used commonly [13], [14]. The bulk of the transistors connect the bulk to the highest voltage through body diodes.

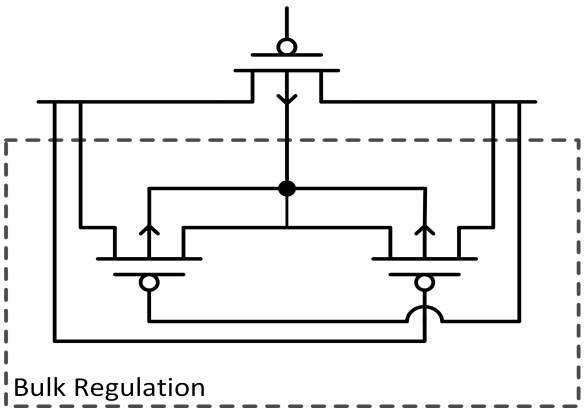

Figure 3.8. Bulk regulation

The start-up circuit pulls the output voltage $V_{IN} - 3.5V$, not $V_{IN} - 5V$ due to charge sharing. Initially, the input power is transferred to the output without any additional controlling circuit since there is no available supply power in the sub-blocks. Therefore, PMOS (HSS) is turned on until V_{SG} equals to V_{TH}.

Before the conversion starts, the input voltage is $70V$. With the start signal, the gate voltage becomes $66.5V$ and the HSS is turned on. The HSS is turned off when V_{SG} is lower than the threshold voltage. For $V_S = 67$, HSS is turned off. The decrease in the energy stored in the input capacitor (C_{IN}) is calculated in Equation 3.3 and found as $2.06\mu J$.

$$\begin{aligned} E_{decreased} &= \frac{1}{2}C_{IN}V_{initial}^2 - \frac{1}{2}C_{IN}V_{final}^2 \\ &= \frac{1}{2}(10\eta F)(70^2V - 67^2V) = 2.06\mu J \end{aligned} \tag{3.3}$$

$$E_{Transferred\ from\ C_{IN}} = E_{Delivered\ to\ the\ Load} + E_{Stored\ in\ C_{OUT}} + E_{Conduction\ Loss} \quad (3.4)$$

This energy is transferred to the output as given in Equation 3.4. $2.06\mu J$ energy delivered to the load strongly depends on the design of the switched capacitor converter which is connected to the output of the buck converter and the conduction loss. The output voltage must not be more than $11V$ due to a possible breakdown. Also, it should not be less than $8V$ or else the switched capacitor converter cannot provide enough power to the sub-blocks of the buck converter to operate. It can be found by Cadence's CAD tool that $C_{OUT} = 12\eta F$, the output voltage becomes $9V$ which is acceptable for the switched capacitor converter to supply power to the buck converter.

The layout of the level shifter's digital blocks is given in Figure 3.9. The layout of the analog part (two capacitors and three PMOSs connected to them), is given in Figure 3.10.

3.3.3. Inductor

The value of the inductor determines the slopes of rising and falling inductor current. Neglecting the power loss, the rising and falling slopes are found in Equation 2.2 and 2.3. The inductor limits the peak current. The larger the current is, the more the V_{DS} voltage of HSS is. So it is better if a larger inductor is used because of the lower conduction loss in the switches. A $1mH$ inductor is used in the design as an off-chip component.

3.3.4. Output Voltage Sense

Output voltage sense circuit is simply a voltage divider, which divides the output by 8. Using resistors as a voltage divider is not a good idea. To illustrate, if $1M\Omega$ is used, $10\mu A$ current loss occurs in the voltage divider for $10V$ output voltage. If the

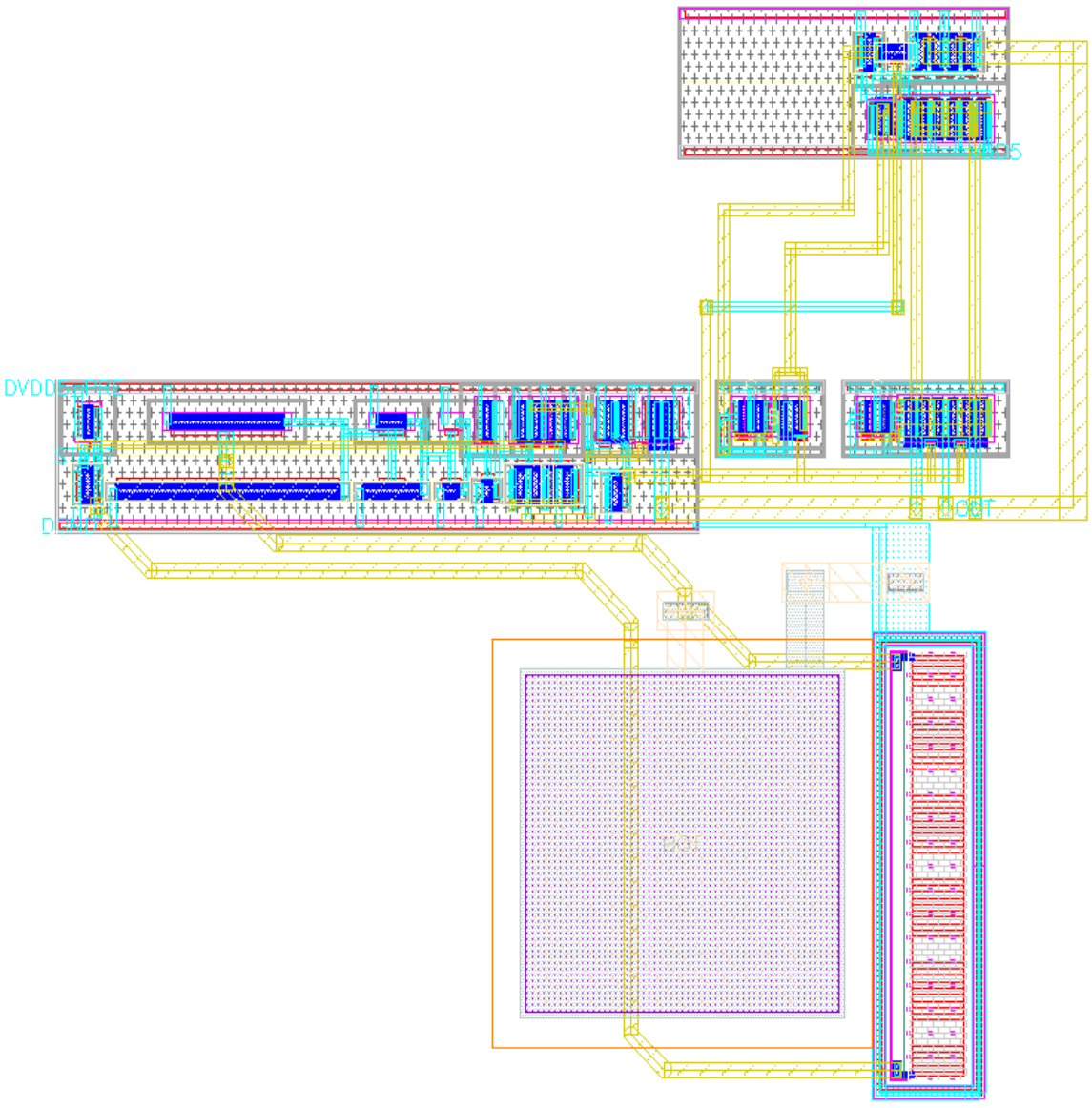

Figure 3.9. The layout of the digital blocks of the level shifter

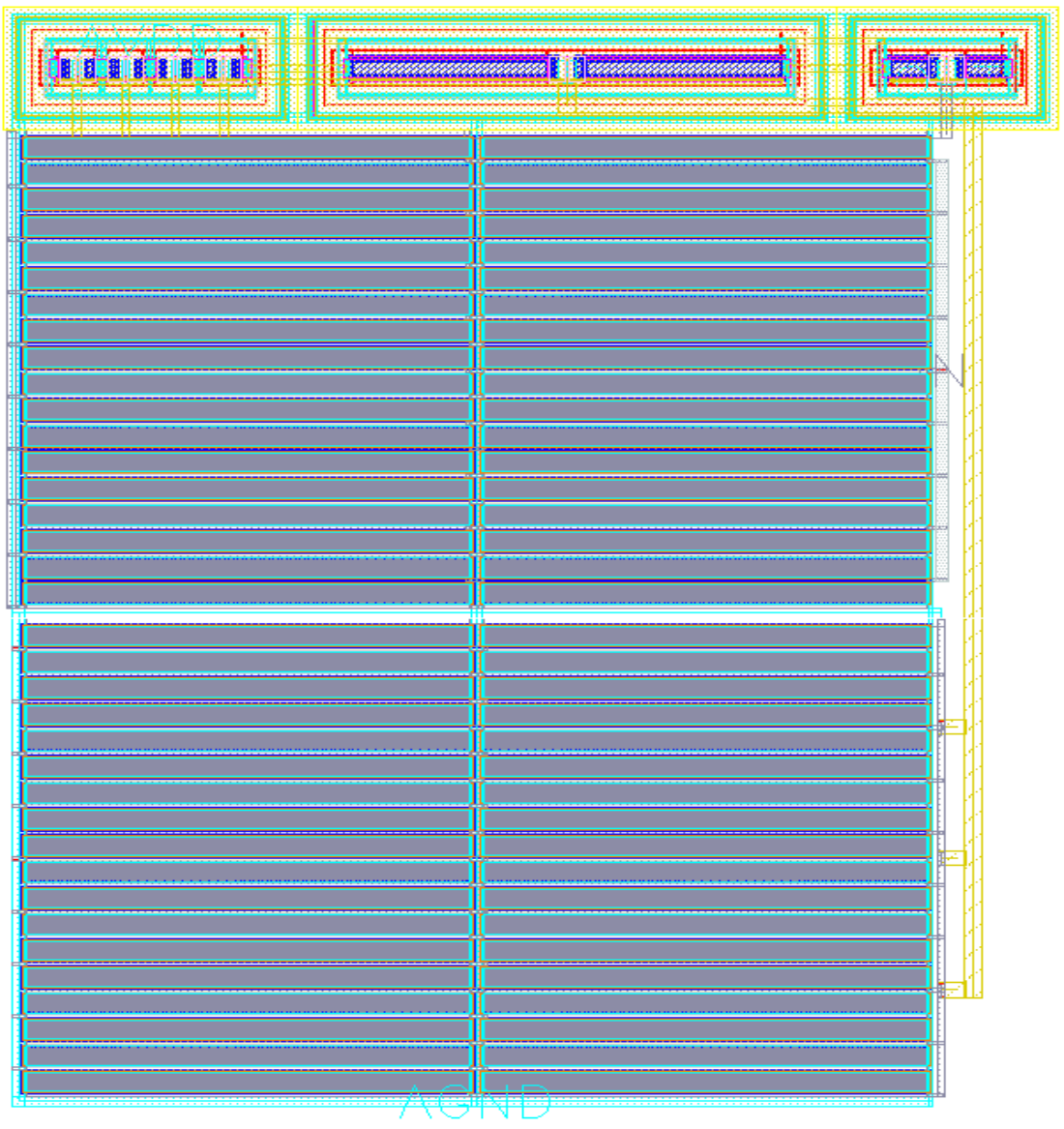

Figure 3.10. The layout of the analog block of the level shifter

current transferred to the load is $150\mu A$, approximately 6.7% power will be lost. If the output current is lower like $40\mu A$, it means 20% power loss. Moreover, $1M\Omega$ resistor covers a large area in the chip and there is a huge parasitic capacitance which prevents the division occurring fast. Larger resistors also create matching problems.

The voltage divider is designed with the diode-connected transistors as shown in Figure 3.11. The transistor's length and width are not chosen as minimum size due to the fabrication process variation. Also, they are not too large because of the parasitic capacitance they have. High voltage devices cannot be used in the circuit because they are large devices employing a large parasitic capacitance. For low currents like $1\mu A$, the sensing becomes too slow to react to the changes in the output. Therefore, low voltage devices ($5V$ PMOS) is used because of small parasitic capacitance. However, even if V_{SG} or V_{SD} voltage does not exceed $5V$, the bulk and substrate voltage difference can reach $10V$. The proposed solution is to use low threshold PMOS devices. These devices have high voltage n-well, which is durable for high substrate-bulk voltage difference. The layout of the PMOS voltage divider is given in Figure 3.12.

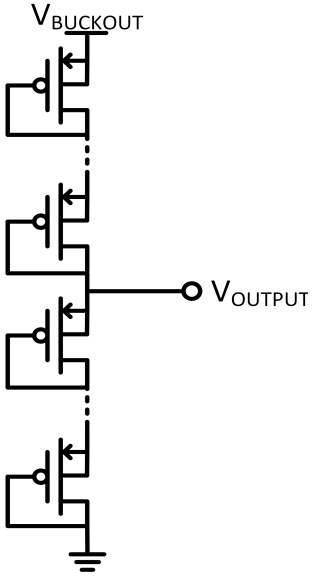

Figure 3.11. PMOS voltage divider circuit

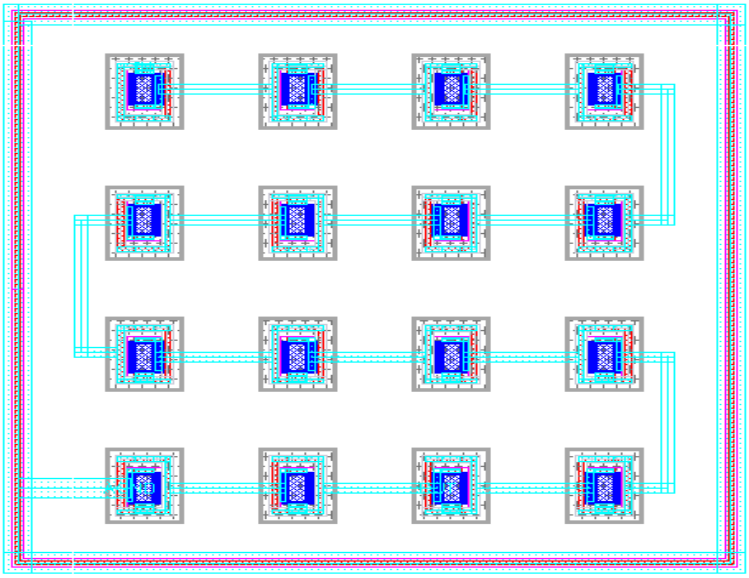

Figure 3.12. The layout of PMOS voltage divider circuit

3.3.5. Comparator

The comparator is a simple Opamp with current consumption of the branches shown in Figure 3.13, and its layout in Figure 3.14. The overdrive voltage is chosen as $0.2V$. The biasing voltage is generated with a resistor because the precision is not as crucial as the duration of the pulse. The Opamp is used only as a comparator. If the bias voltage is not precise or supply dependent, the parameters of the comparator will change. However, as long as it is not slow to react to the changes in the output voltage, there will be no significant problem.

3.3.6. Pulse Generator

The schematic of the pulse generator is given in Figure 3.15. After $5V$ is given to D terminal of the latch, the circuit resets it. The pulse is generated as shown in Figure 3.16. Its duration is determined by the RC circuit and the inertial delay of the blocks. There is an array of capacitors in the circuit. It is controlled for test purposes only. After the fabrication, the efficiency will be measured for different width of pulses.

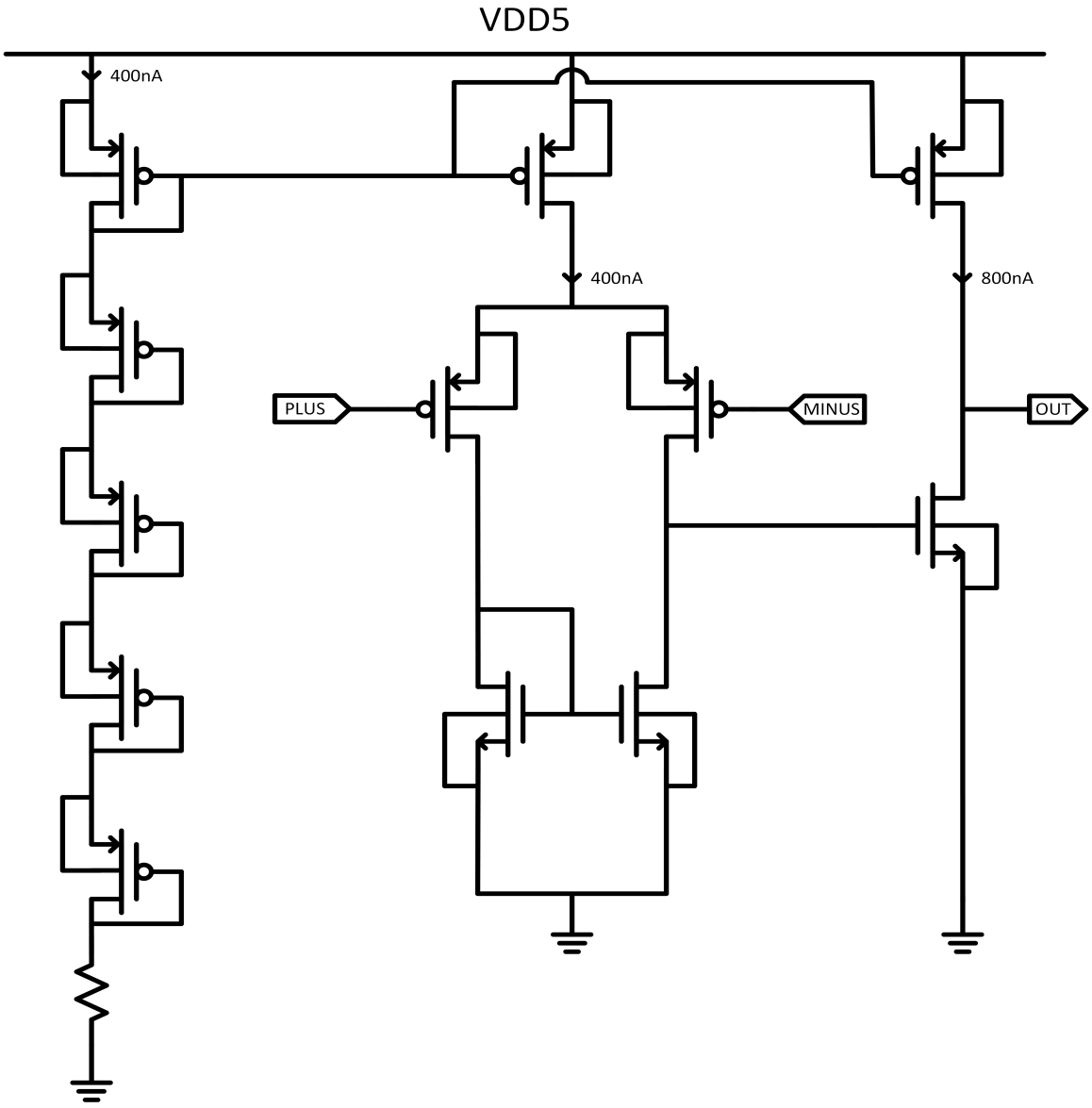

Figure 3.13. Schematic of the Opamp

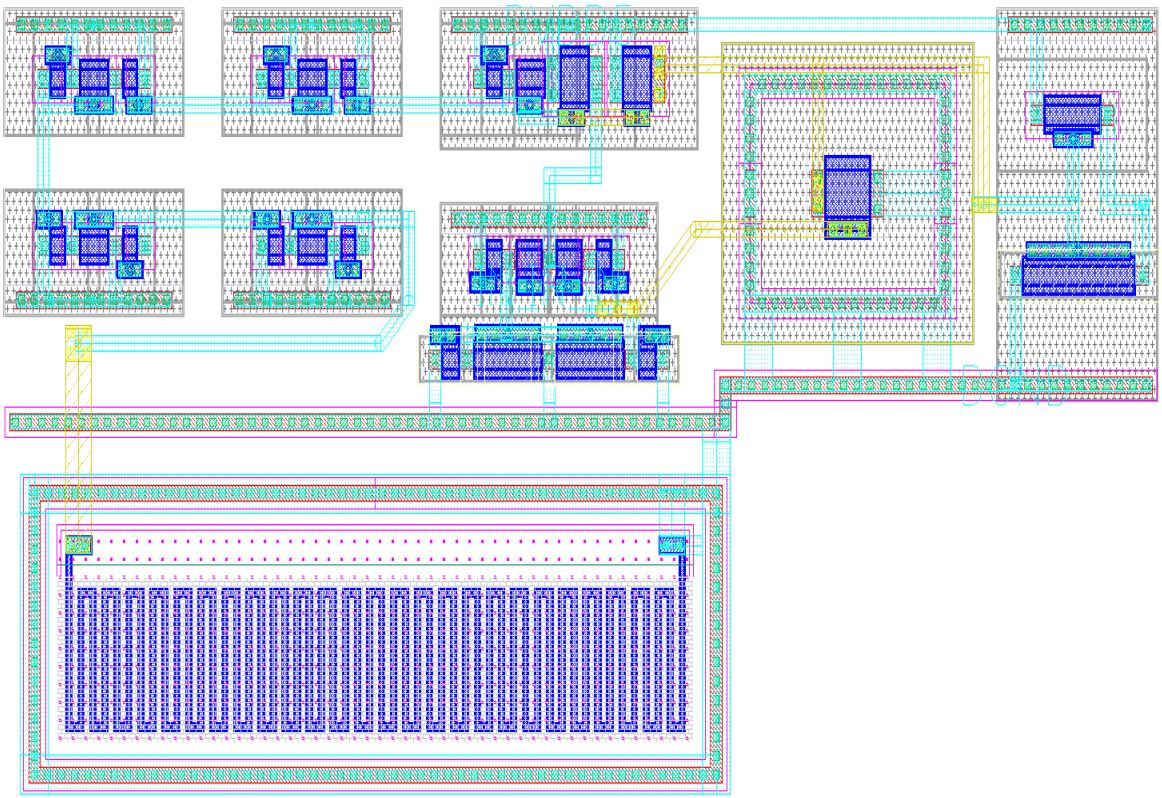

Figure 3.14. The layout of the Opamp

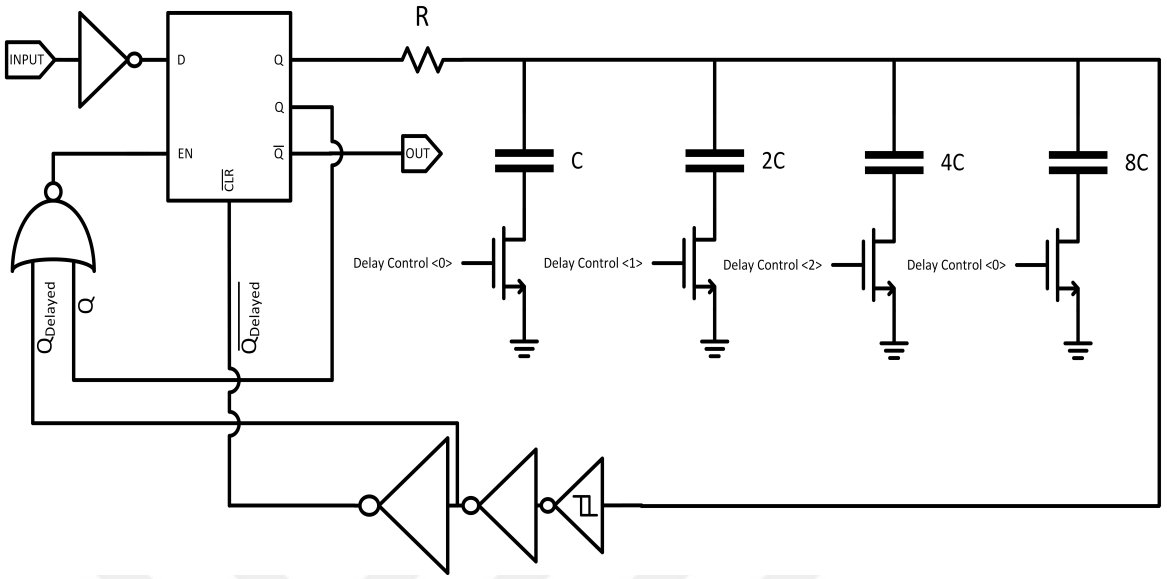

Figure 3.15. Schematic of the pulse generator

A Schmitt trigger inverter is connected to the output of the RC circuit. It is used for preventing the next pulse to be received for a certain time. When $Q_{Delayed}$ is $5V$, thanks to the Schmitt trigger, it will not be $0V$ immediately after resetting the latch. After reset signal arrives $Q_{Delayed}$ will be $0V$ with a certain delay caused by the Schmitt trigger. As a result, D-latch stays disabled longer. If it is a standard inverter, D-latch will be enabled right after resetting the D-latch. In case of coupling or a kickback in the comparator due to its high resistance at the input terminals, D-latch may be set to $5V$ again as an error. It disrupts the operation of the buck converter and the HSS is turned on again. Therefore, it is a good idea to give certain time to the system for settling.

Operation of a Schmitt trigger inverter is given in Figure 3.17. When Q is set to $5V$, the HSS is turned on. $Q_{Delayed}$ also starts to increase. When it reaches V_{Hi}, the system resets the latch and Q becomes zero by turning the HSS off. After resetting the latch, the output voltage of the Schmitt trigger inverter starts to decrease. When it reaches V_{Li}, $Q_{Delayed}$ becomes $0V$ and D-latch becomes ready to receive the next input signal.

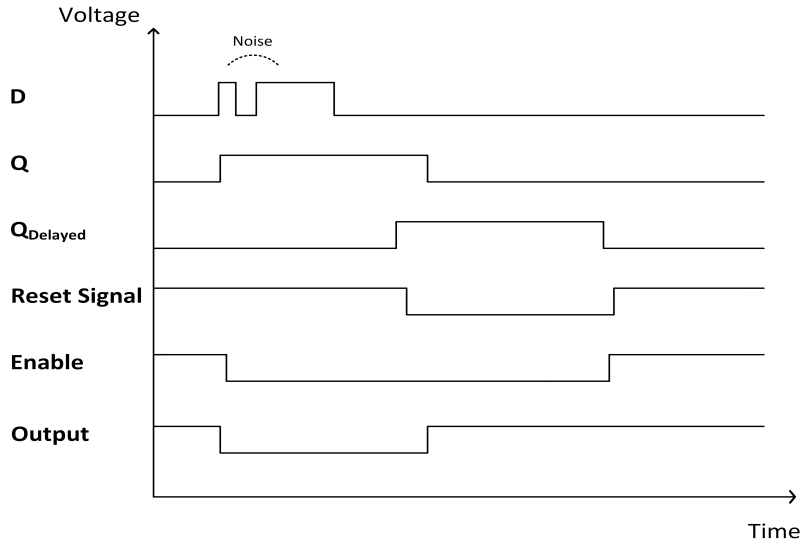

Figure 3.16. Generated signals in the pulse generator

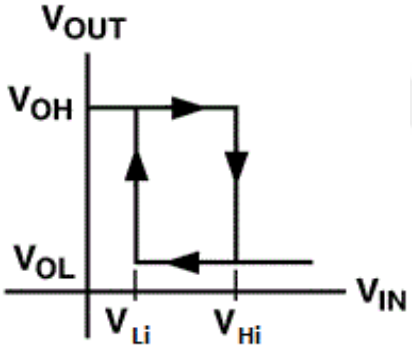

Figure 3.17. Operation of the Schmitt trigger inverter

In the literature, the Schmitt trigger inverters are already researched and the circuit is shown in 3.18 [5] is used. As explained in [5], the following equations are obtained,

$$\frac{(W/L)_1}{(W/L)_3} = \left(\frac{V_{DD} - V_{H_i}}{V_{H_i} - V_{TN}}\right)^2 \tag{3.5}$$

$$\frac{(W/L)_4}{(W/L)_6} = \Big(\frac{V_{L_i}}{V_{DD} - V_{L_i} - |V_{TP}|}\Big)^2 \tag{3.6}$$

These equations are used to size the transistors according to the desired V_{H_i} and V_{L_i}. The transistors' lengths are chosen large so as to prevent large current loss from V_{DD} to the ground while PMOS and NMOS are turned completely or partially on at the same time. However, usage of small W/L increases on-resistance of the transistors and total delay of the circuit. It is required to be taken into account while adjusting the RC delay.

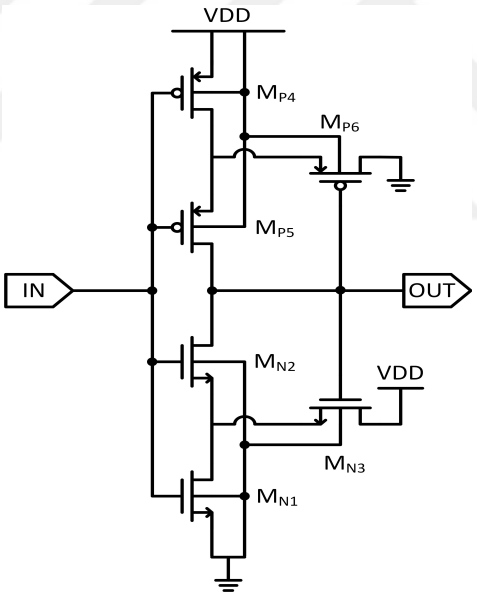

Figure 3.18. Schematic of the Schmitt trigger inverter [5]

The layout of the pulse generator is given in Figure 3.19.

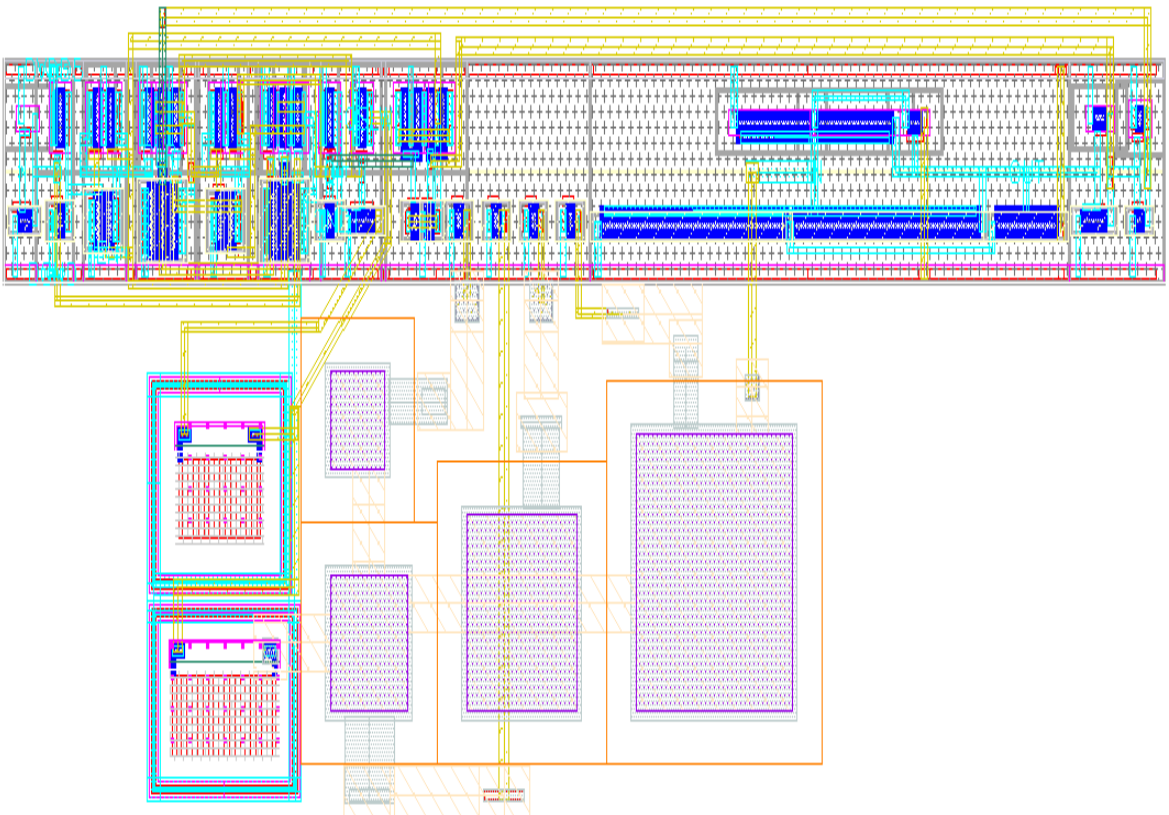

Figure 3.19. The layout of the pulse generator

3.3.7. The High Side Switch and Freewheeling Diode

The high side switch is chosen so as to make the voltage drop small. A PMOS is chosen as HSS. Increasing W/L ratio of PMOS decreases the voltage drop. However, it also increases the parasitic capacitance and it gets slower to switch. As a result switching loss increases. In this thesis, W/L parameters are chosen as $1mm/450nm$, where $450nm$ is the minimum length of $70V$ transistors. Its layout is given in Figure 3.20. As a freewheeling diode, the body diode of a large NMOS is used. Since it is not used as a transistor, W/L ratio is not chosen as large as HSS. It is chosen as $330um/1.5um$. The layout is given in Figure 3.21.

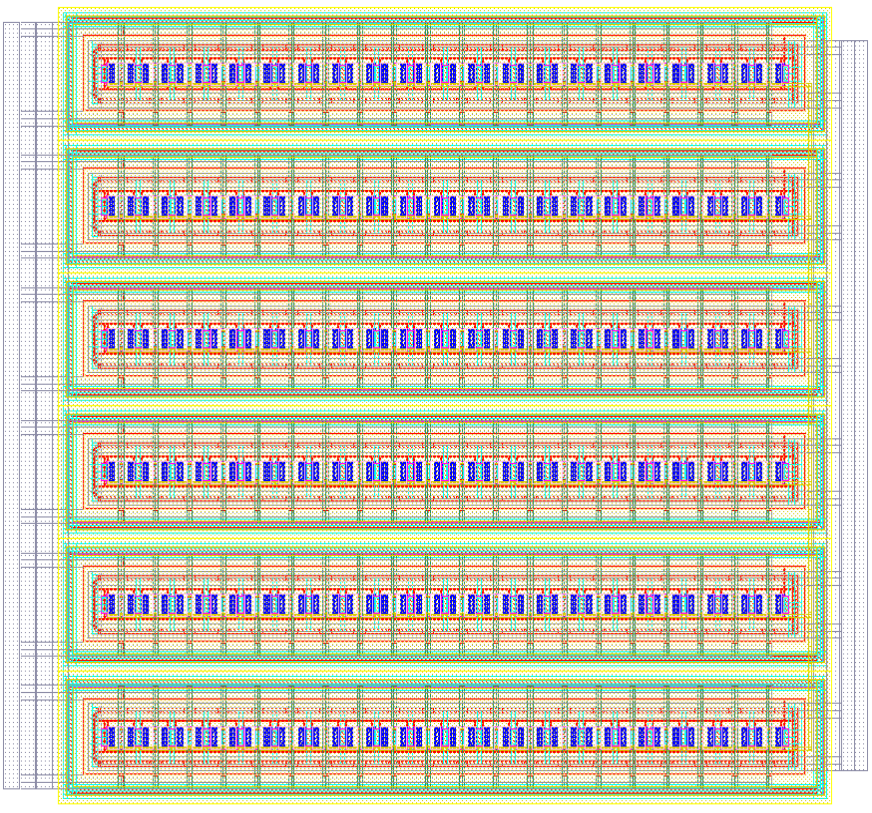

Figure 3.20. The layout of the high side switch

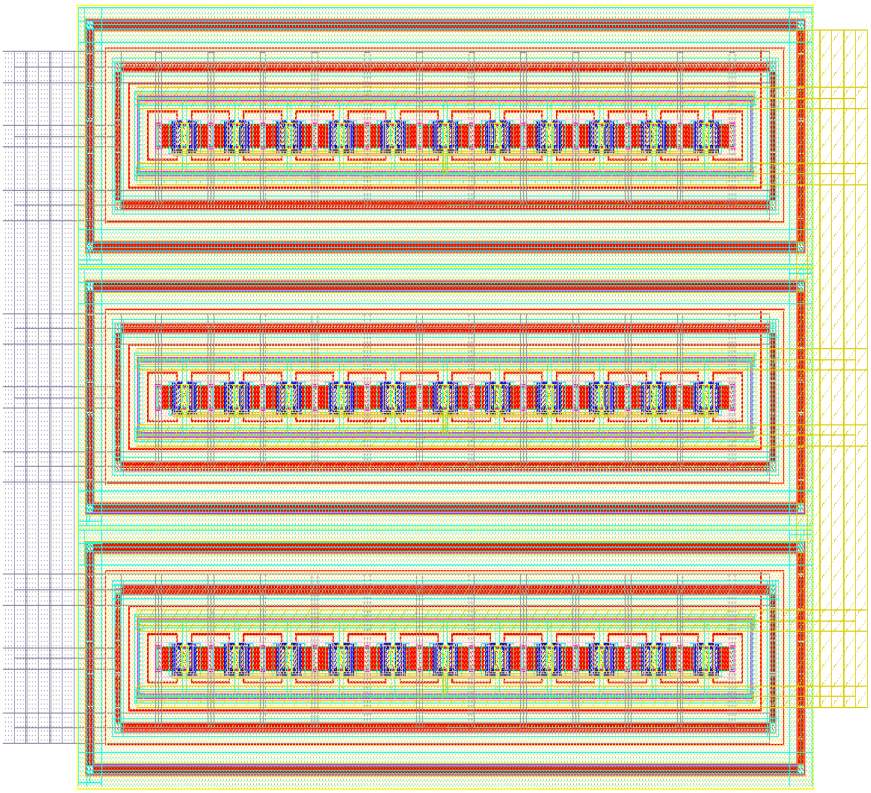

Figure 3.21. The layout of the freewheeling diode

3.4. Duration of the Pulse

It is crucial to adjust the duration of the pulse. If the pulse is short, HSS is turned on for a short time. In this case, a higher number of switching must be done to deliver the same amount of energy, contrary to longer pulses. The more the switching, the greater the energy loss. Therefore, it is advised to keep the pulses long as much as possible. However, long pulse width results in large voltage ripples which may cause the output voltage to exceed the desired level. A breakdown may occur in the load or switched capacitor converter due to an excessive output voltage. To sum up, the pulse width should be chosen as large as possible, but not too long to cause more than +10% voltage ripple.

3.4.1. Calculation of the Required Pulse Width

In DCM mode inductor current is shown in Figure 3.22. t_{pulse} is the duration of the pulse turning the HSS on. At the time t_{off}, the inductor current becomes 0V and it starts to saturate. i_L is the inductor current and i_{out} is the current transferred to the output. In this circuit, i_{out} is maximum $150\mu A$. The area under $i_L - i_{OUT}$ gives the total amount of transferred charges to the capacitor. The rising slope of the inductor current can be found as follows,

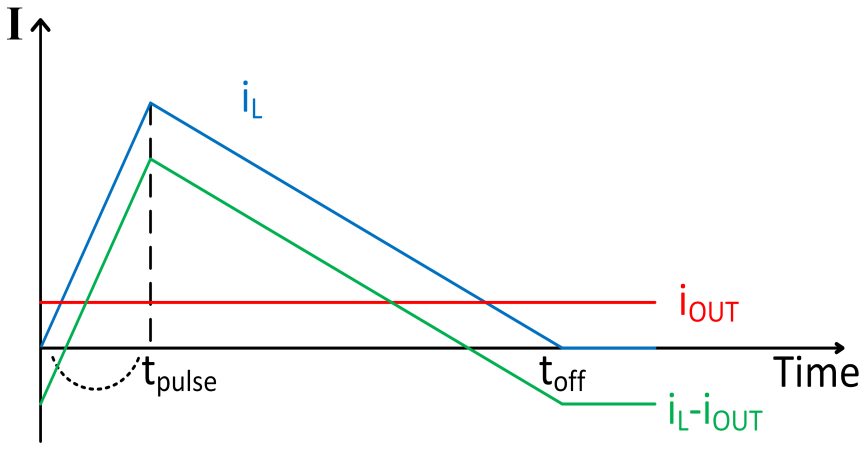

Figure 3.22. Inductor current in DCM

$$V = L\frac{dI}{dt} \tag{3.7}$$

$$\begin{aligned}\left(\frac{dI}{dt}\right)_{rising} &= \frac{\Delta V}{L} = \frac{[67V - V_{SD_{HSS}} - R_{DC,inductor}i_L - (10V + \Delta V)]}{1mH} \\ &\approx 57 \times 10^3 A/s\end{aligned} \tag{3.8}$$

where $V_{SD_{HSS}}$ is the voltage drop between the source and drain terminals of the PMOS, $R_{DC,inductor}i_L$ is the voltage drop due to the DC resistance of the inductor, and $10V + \Delta V$ is the output voltage. The minimum value of the ΔV is $-0.8V$ and maximum is $0.8V$ depending on the charge at the capacitor. The input voltage $67V$ is the voltage remaining in the capacitor after the operation of the start-up circuit ends. The result can be found by an approximation of the large input voltages because the input-output voltage is large enough. The slope of the falling inductor current can be found similarly.

$$\begin{aligned}\left(\frac{dI}{dt}\right)_{falling} &= \frac{\Delta V}{L} = \frac{[(10V + \Delta V) - (-V_{Diode} - R_{DC,inductor}i_L)]}{1mH} \\ &\approx 10.7 \times 10^3 A/s\end{aligned} \tag{3.9}$$

Voltage drop in the diode is $0.7V$. The result can be approximated again. Peak inductor current and the relation between t_{pulse}-t_{off} can be calculated as below.

$$\begin{aligned}i_{peak} &= Slope_{rising} \times t_{pulse} = Slope_{falling} \times (t_{off} - t_{pulse}) \\ t_{off} &= 6.32 t_{pulse}\end{aligned} \tag{3.10}$$

With the calculated values in Equation 3.8, 3.9, and 3.10, the required pulse width is found as follows,

$$\begin{aligned} Q_{Delivered\,to\,C_{OUT}} &= C_{OUT}V \\ \frac{1}{2}i_{peak} \times t_{off} - 150\mu A \times t_{off} &= C_{OUT}(V_{max} - V_{min}) \\ \frac{1}{2}(57k \times t_{pulse})(6.32 \times t_{pulse}) &= 15\eta F(10.8 - 9.2) \end{aligned} \tag{3.11}$$

$$\begin{aligned} 1.80 \times 10^5 t_{pulse}^2 + 0.15 \times 10^{-3} t_{pulse} - 24 \times 10^{-9} &= 0 \\ t_{pulse} &= 365ns \end{aligned} \tag{3.12}$$

3.4.2. Finding the Values of the Components for the Required Pulse Width

In the previous section, the required pulse width is calculated as $365ns$. Pulse width is generated in the pulse generator. The delay coming from the comparator does not have a huge effect on the output voltage. It just allows the output voltage to decrease more. But it is tolerable. On the other hand, if an extra delay is generated in the pulse generator, it results in excessive output voltage. Therefore, the pulse generator block is critical.

The inertial delays of the digital blocks are small compared to $365ns$. Each inverter is 4x larger than the previous one. The smallest inverter is the Schmitt trigger inverter because it is connected to the RC circuit. To prevent power loss, it is important to make its W/L ratio as small as possible. W/L of NMOSs (M1 and M2) are 1/15 and W/L of PMOSs (M4 and M5) are 1/6. The length of the transistors is long, and the inverter may be expected to operate slow. However, the transition from one stable state to another in Schmitt trigger is, indeed, very fast because of positive feedback during the transitions [5]. The sum of inertial delays of the digital gates is as small as

$20 - 40ns$ as calculated by CAD, Cadence Virtuoso. So it can be said that this delay can be neglected. Even variations during the fabrication may cause that much delay to the circuit. Therefore, the pulse width is adjusted only by the RC circuit.

The calculated maximum delay is $365ns$, however, it is better if the delay is much lower than this limit. The RC circuit is designed to achieve $300ns$ delay. The transistor of the Schmitt trigger is designed for $V_{Hi} = 3.45V$ and $V_{Li} = 1V$ with the Equations in 3.5 and3.6. The detailed analysis can be found in [5].

An array of capacitors and a resistor are used as an RC circuit. The array of capacitors provides controlling the value of capacitance in the RC circuit for testing purposes. If the capacitor of the RC circuit is low, there will be small power loss. Hence, minimum capacitance in the array is chosen as $40fF$ and the maximum is $320fF$. Poly salicide resistor is used which provides high resistivity in a small amount of area. Timing of the RC circuit is found with the Equation 3.13, where τ is the time constant, V_∞ is the steady-state value, V_1 is instant value, and V_0 is the initial value [15].

$$\Delta t = \tau \frac{V_\infty - V_0}{V_\infty - V_1} \tag{3.13}$$

The rise time of the RC circuit until the input of the Schmitt trigger becomes V_{Hi} and fall time to become V_{Li} are given in Equations 3.14 and 3.15.

$$\Delta t_{rise} = RC \frac{4.7V - 0}{4.7V - V_{Hi}} \tag{3.14}$$

$$\Delta t_{fall} = RC\frac{0 - V_{Hi}}{0 - V_{Li}} \tag{3.15}$$

It takes t_{rise} for the output of the Schmitt trigger to become $0V$ and t_{fall} to become $5V$ again. t_{rise} is the pulse width and t_{fall} is the duration of the time that D-latch stays disabled. It is important that steady-state voltage is not calculated as $5V$ because supply voltage is lower. The pulse is generated when the output voltage of the buck converter is low. The output voltage is around $9.4V$ instead of $10V$. Therefore, switched capacitor converter provides approximately $4.7V$.

4. POST LAYOUT SIMULATION ANALYSIS AND RESULTS

4.1. Top-Level Simulation Analysis of the Proposed Asynchronous Buck Converter

The transient analysis is done to make sure the buck converter works within the given specifications. Switched capacitor converter is modeled and connected to the output of the buck. It divides the input by two without any power loss and supplies the sub-blocks of the buck converter with $30\mu s$ delay. Also, $67k\Omega$ resistor, resulting in $150\mu A$ load current, is connected to the output as a load. An additional load capacitor is not connected because the output capacitor of the buck is too large to neglect the load capacitance.

The first transient simulation is done for an ideal $1mH$ inductor with 5Ω DC resistance. A $10\eta F$ capacitor is charged to $70V$. The start-up signal is given to the circuit and the transient response of the circuit is shown in Figure 4.1. Equivalent series resistance (ESR) of the output capacitor is $100m\Omega$. Since ESR is much low compared to dc resistance of the inductor, energy dissipation in ESR is also expected low. Total input energy given to the circuit is calculated in Equation 4.1 by subtracting final energy in the input capacitor from initial stored energy.

$$\begin{aligned} E_{IN} &= E_{initial} - E_{final} \\ &= \frac{1}{2} C_{IN} V_{initial}^2 - \frac{1}{2} C_{IN} V_{final}^2 \\ &= \frac{1}{2} 10\eta F (70^2 - 10^2) \\ &= 24\mu J \end{aligned} \tag{4.1}$$

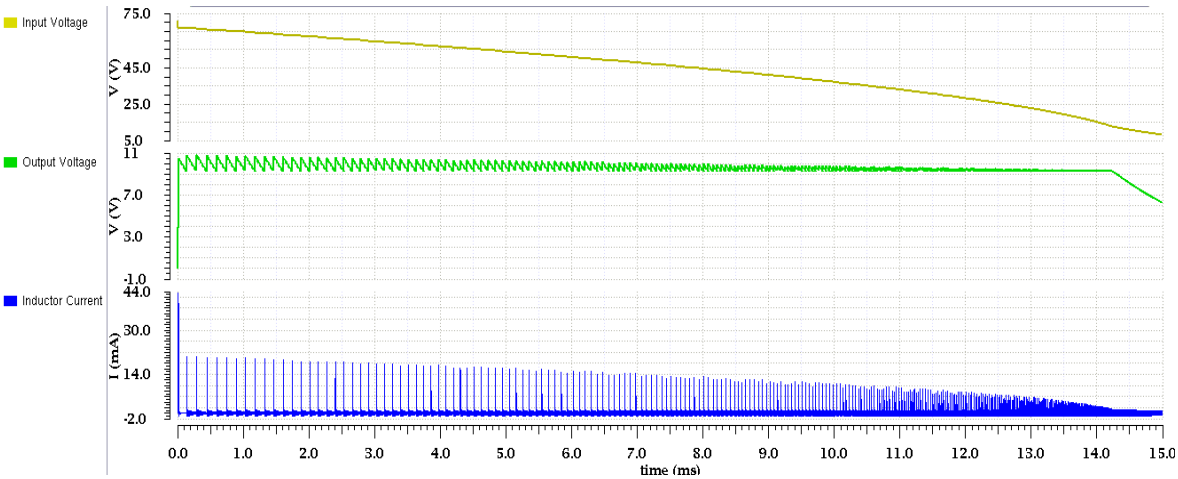

Figure 4.1. Transient analysis of schematic of the buck converter with an ideal inductor

With the given start signal, $3.5V$ drop occurs at the gate of the PMOS (HSS) and current starts to flow to the output. It stops when $V_{SG} = V_{TH}$ and inductor current settles down. As seen in Figure 4.2.a, input voltage drops to $67V$ at the start. A model of switched capacitor converter is supplied by initially transferred energy and the $5V$ supply voltage is given to the sub-blocks. When the supply voltage is enough for sub-blocks to run properly, the buck converter starts to operate.

The pulse width is constant during the operation of the buck converter. As depicted in Equation 2.2 and 2.3, the peak of the inductor current depends on the voltage difference between the input and the output voltages. This difference gets smaller due to the decreasing input voltage as the buck converter continues to operate. Therefore, the ripple at the output voltage gets smaller. Also, the switching frequency and power loss increase. As shown in Figure 4.2, the voltage swing is larger at the start while it is smaller at the end.

For $24\mu J$ given energy, the efficiency is found as 82.8%. For output voltages below of $9V$ at the end of the operation is calculated as loss because it is beyond specified limits. 17.2% of the energy is dissipated as shown in Figure 4.3. Most of the power is dissipated in HSS. Due to 5Ω DC resistance, the inductor is the second largest source

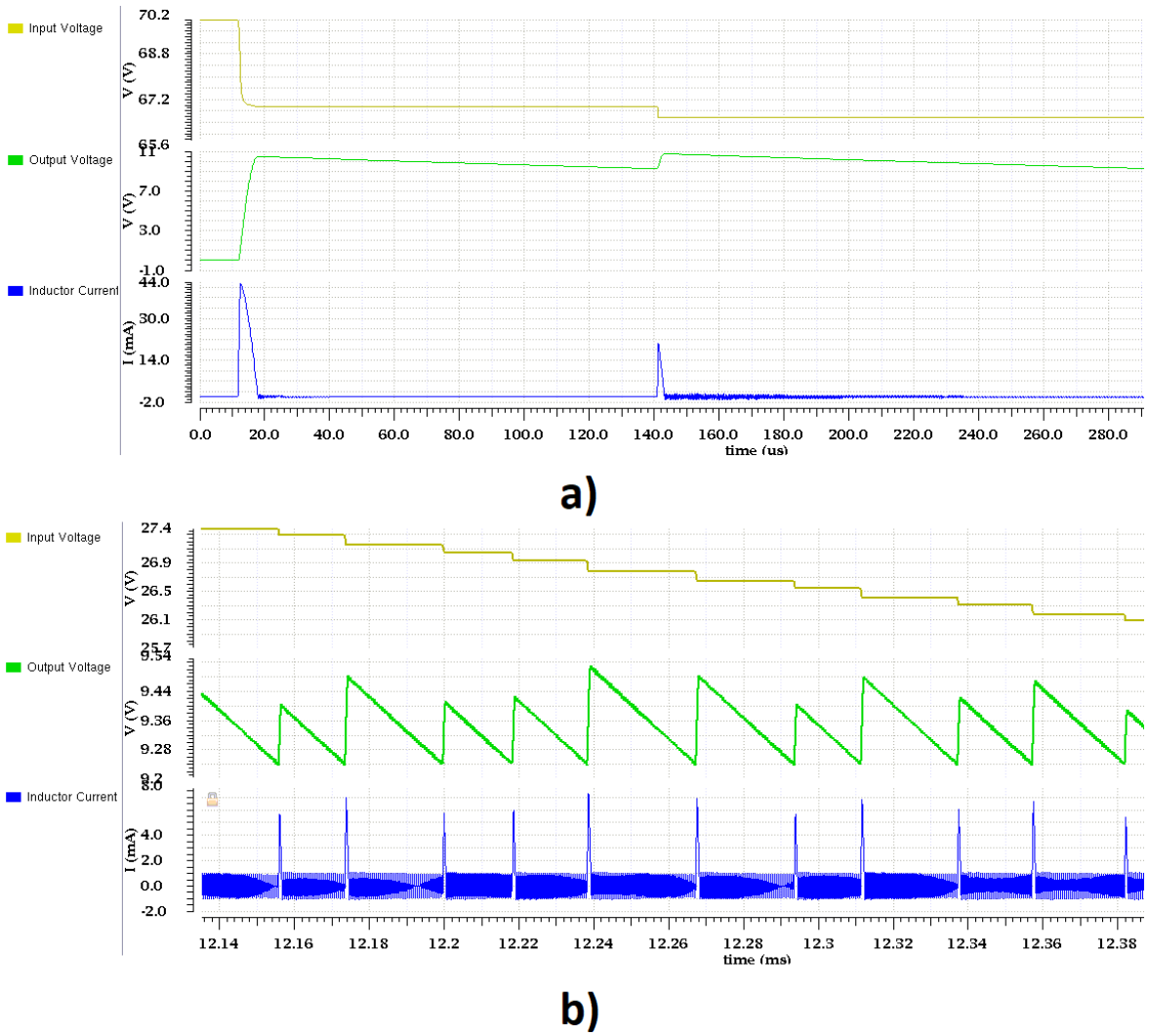

Figure 4.2. Transient analysis of schematic of the buck converter with an ideal inductor: a) Beginning of the operation b) End of the operation

of power loss. As expected, the loss in the diode is not too much because of the high output voltage.

A second transient simulation is done with a model of an inductor. As an inductor, spice model of Taiyo Yuden CBC3225T102KR $1mH$ is used. Its model is shown in Figure 4.4. The DC resistance is 13Ω, which is higher than 5Ω. The transient simulation result is shown in Figure 4.5 and 4.6. Because of the large parasitic capacitance of the inductor model, current spikes are observed as seen in Figure 4.6. The efficiency is calculated as 71.4%. 29.6% of the energy is dissipated as shown in Figure 4.7.

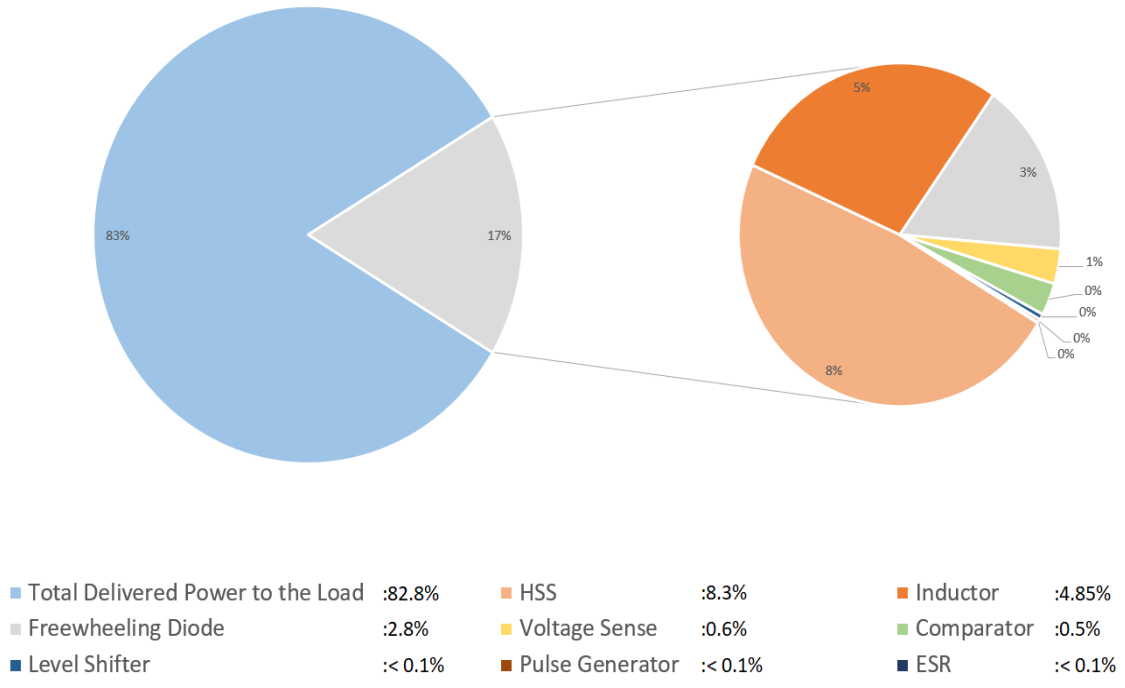

Figure 4.3. Power dissipation in the buck converter with an inductor ($L = 1mH$, $R_{DC} = 5\Omega$)

More power is dissipated in the inductor due to its higher DC resistance. Higher resistance also increases the dissipated power in the HSS because more switching is required for less transferred energy. However, dissipated power in the freewheeling diode is reduced. If the dissipated energy in the inductor increases, the inductor current reaches zero faster. Hence, the current flows through the diode for a shorter time, reducing dissipated power in the freewheeling diode.

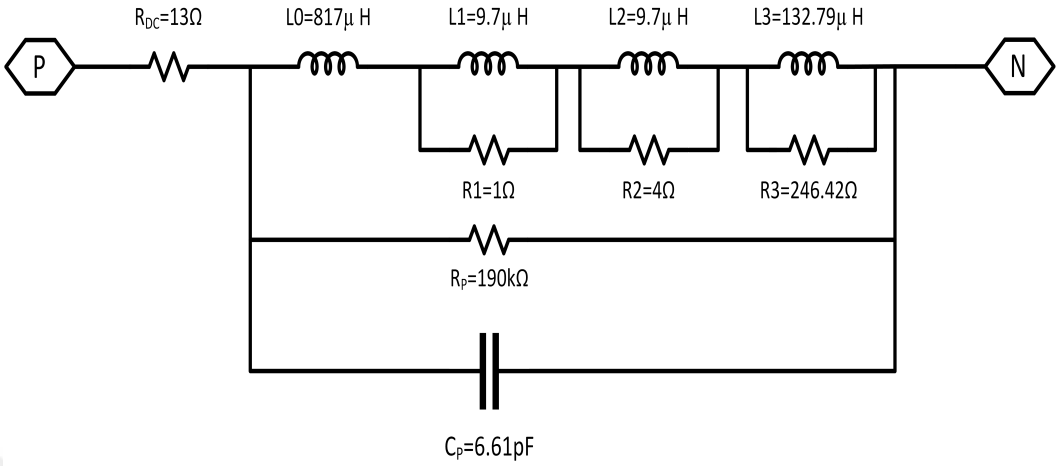

Figure 4.4. Spice model of CB2012T1R0 $1mH$ inductor

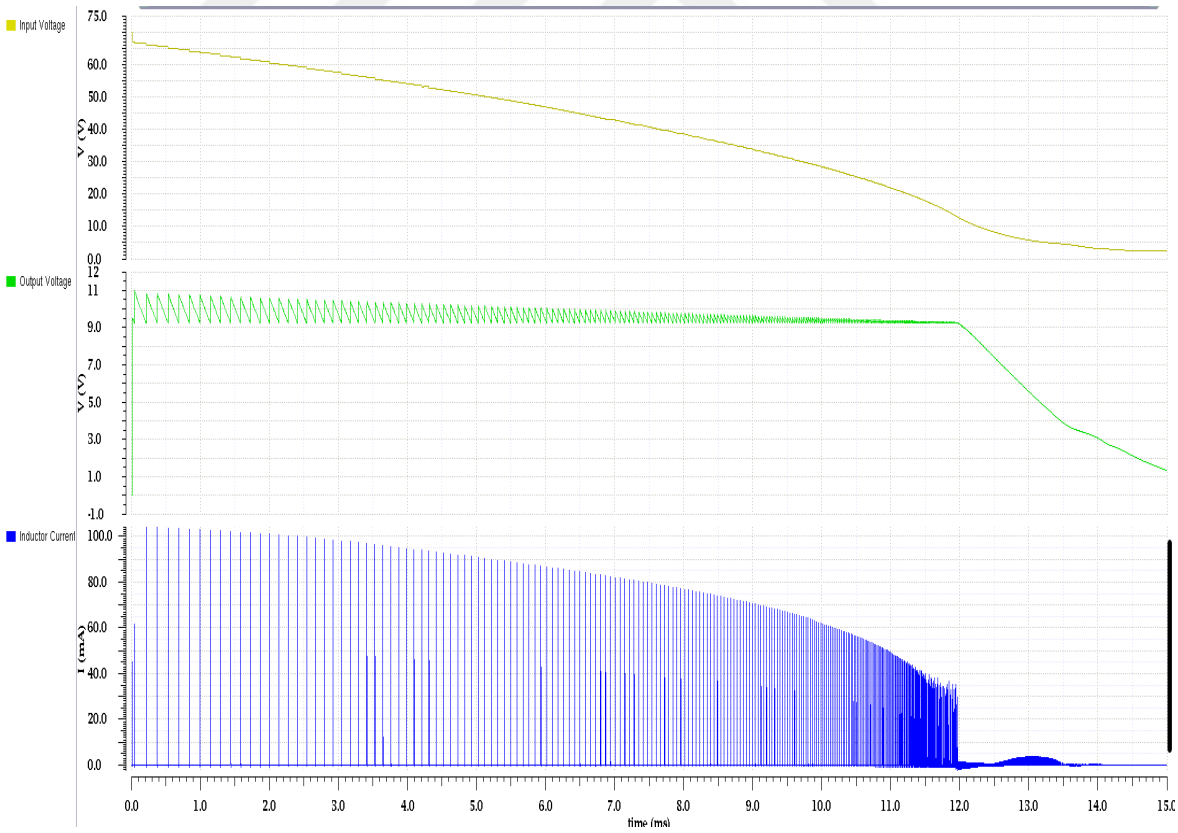

Figure 4.5. Transient analysis of the schematic of the buck converter with the model inductor

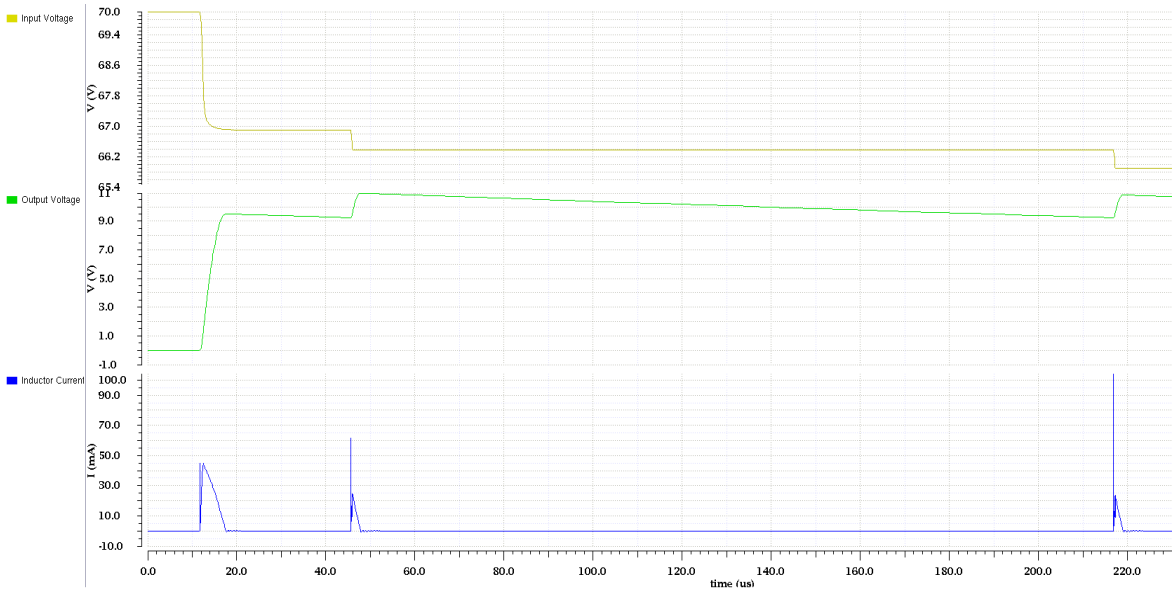

Figure 4.6. Beginning of the buck converter's operation with the model inductor

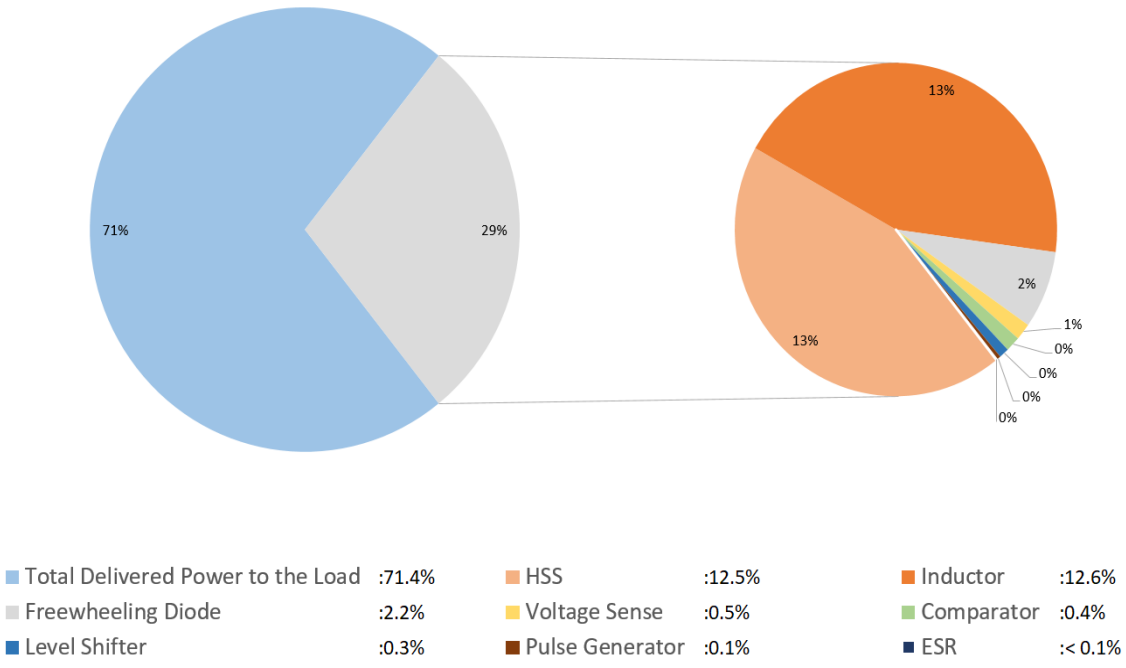

Figure 4.7. Power dissipation in the buck converter with the model inductor

Last transient analysis is done for the layout of the buck converter with the same model of the inductor. The layout of the circuit is shown in Figure 4.8. The transient simulation result is given in Figure 4.9. The calculated efficiency is 68.9%. The layout brings additional parasitic capacitance in the circuit, which slows down the operation of the buck converter. When the Opamp, the pulse generator, and the level shifter operate slowly, switching loss is increased. Therefore, the calculated efficiency in post-layout simulation is 2.5% lower than the efficiency in the simulations without the layout.

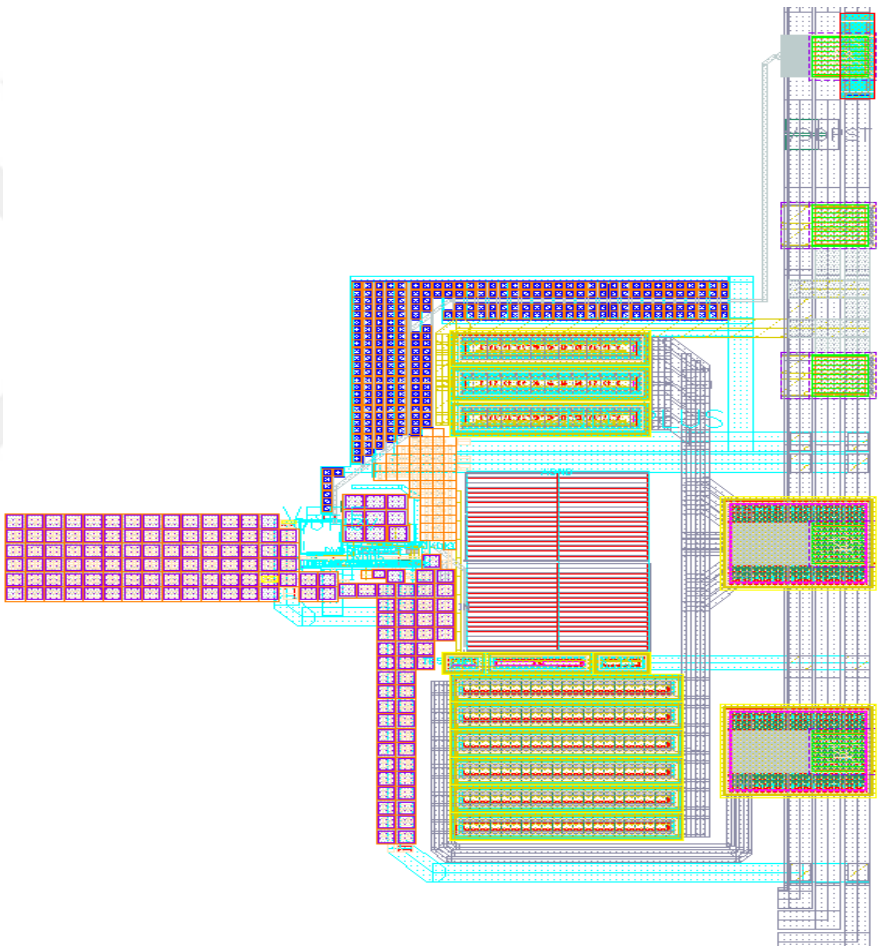

Figure 4.8. The layout of the proposed buck converter

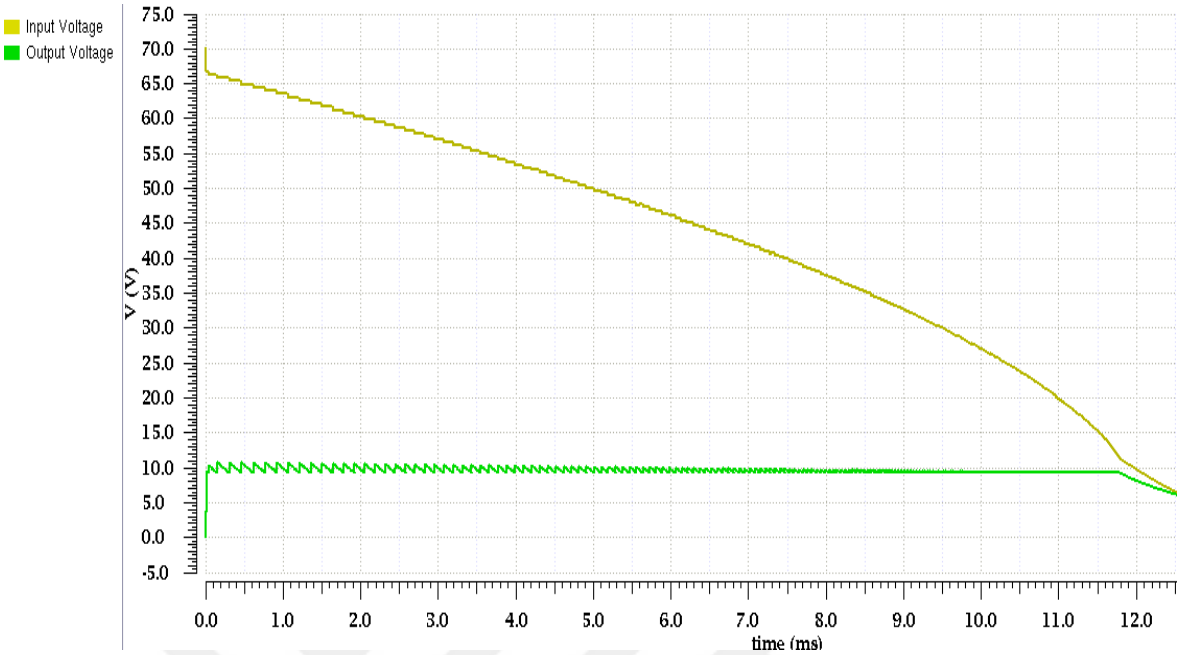

Figure 4.9. Transient post-layout simulation result of the proposed buck converter

4.2. Comparison of Asynchronous and Synchronous Buck Converter

The usage of LSS is crucial for the efficiency in a conventional buck converter. However, there are some reasons to use a freewheeling diode instead of LSS, which are listed below.

- If the output voltage is high, more energy is transferred to the output. When the voltage drop between the terminals of LSS is taken into account for Equation 2.3, a new equation is obtained in 4.2. It means that the inductor current transferred to the load will not be affected much by V_{DS} for high output voltages. $10V$ can be considered as a high voltage for a buck converter.
- Switching loss in switches as described in Chapter 2 is larger for slower circuits. The proposed buck converter does not operate fast, so using LSS causes a larger switching loss.

$$Slope_{fall} = \frac{\Delta I}{\Delta t} = \frac{\Delta V}{L\Delta t} = \frac{V_{OUT} - (-V_{DS})}{L} \tag{4.2}$$

A synchronous buck converter is also designed in order to compare it with the asynchronous one.

4.2.1. Design of the Synchronous Buck Converter

Every component is kept the same with the ones in the asynchronous buck converter, except the pulse generator. As a freewheeling diode, a body diode of a large NMOS is used in the asynchronous buck. The same NMOS is used as LSS by controlling its gate terminal instead of connecting it to the ground. A zero voltage detector (ZVD) circuit is added to the circuit to detect when the inductor current becomes $0A$. The NMOS (LSS) is turned on and off depending on the voltage of the node that LSS and inductor are connected to. The potential of this node will be called as V_{COIL}. If V_{COIL} is negative, meaning that current flows from source to drain, LSS is turned on. If it is positive, the current can flow from source to drain (ground) and LSS must be turned off.

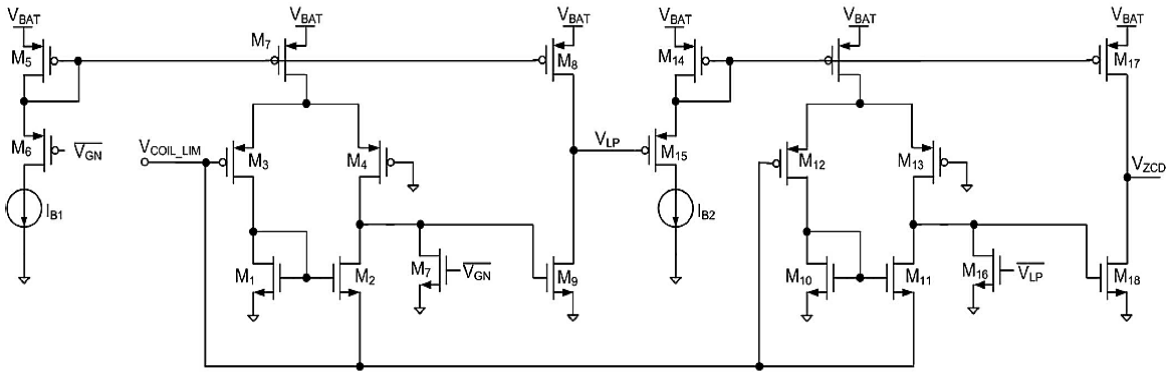

Figure 4.10. Zero-current-detector [4]

In the literature, there are different topologies for ZVD. One of them is two-stage ZVD [4], which is shown in Figure 4.10. In a buck converter, the coil voltage crosses zero for two times. The first transition may occur too fast because the slope is determined by the peak current in the inductor. The second transition occurs much slower. Since the peak inductor current is not too high $(20 - 25mA)$ and the parasitic capacitance of the switches is large, the first transition is not too sharp. Therefore, only the first stage is used in Figure 4.10. The schematic of the ZVD is shown in Figure 4.11. The current consumption is large for this block because zero voltage must be detected fast and in high accuracy. However, ZVD does not have to be enabled during the whole operation. It can be enabled only after HSS is turned off and can be turned off after turning off LSS.

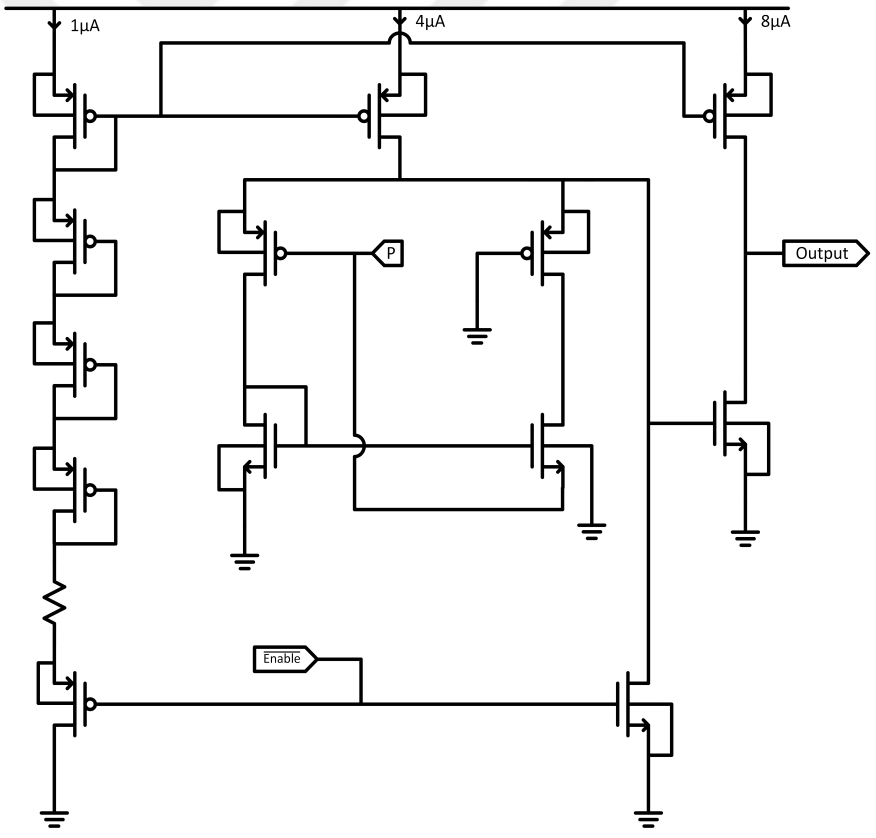

Figure 4.11. Zero-voltage-detector

Another important point is that the coil voltage must be limited because it can reach $70V$ and damage the ZVD. therefore, a voltage protection circuit is placed before ZVD. It is shown in Figure 4.12. The voltage protection circuit is enabled by making

$\overline{ENABLE} = 5V$. When it is enabled, ZVD is disabled. To sense the voltage by ZVD, voltage protection circuit must be disabled so that the voltage will be sensed. The Zener diode is used to prevent limited coil voltage to exceed $5V$, especially for the start-up phase.

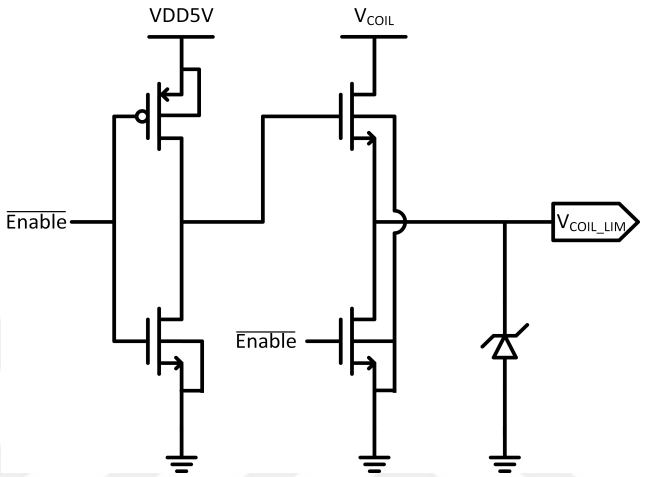

Figure 4.12. Voltage protection circuit for ZVD

ZVD is enabled immediately after HSS is turned off. It is connected to LSS as shown in Figure 4.13. The enable signal and inverse of it are generated in the pulse generator circuit. ZVD is disabled to prevent power loss when it is not needed. On the other hand, if ZVD becomes disabled, its output becomes high impedance. NAND2 prevents LSS from opening when ZVD is disabled by forcing LSS to turn off.

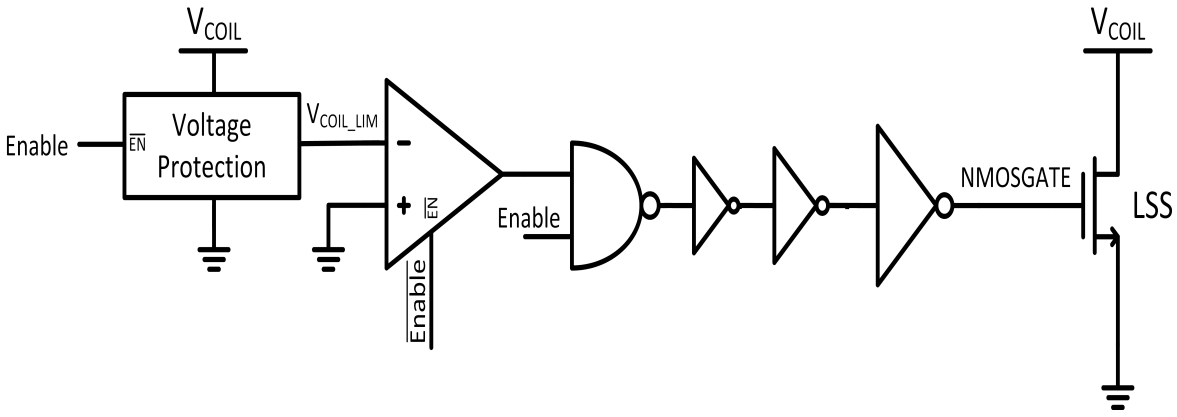

Figure 4.13. The driver of LSS

Pulse generator circuit for the asynchronous buck converter is shown in Figure 4.14. There is a small difference from the previous design. First of all, the enable signal is generated. This signal and inverse of it are given to the voltage protection circuit and the ZVD. When the coil voltage is sensed and the NMOS (LSS) is turned on, a "reset" signal is generated and given to the SR latch. In the asynchronous buck converter, the reset signal is provided by a Schmitt trigger circuit. However, in the synchronous buck converter, it is generated by ZVD. Therefore, an NMOS is connected to the input of the Schmitt trigger inverter and pulls its input voltage to the ground when the reset signal arrives. As a result, more power is saved due to the rapid turning off. When ZVD turns off LSS, the enable signal becomes off so that the voltage protection is enabled while ZVD is disabled.

4.2.2. Simulation Result and Discussion

Transient analysis is done for the synchronous buck converter. Input and output voltages are shown in Figure 4.15. In Figure 4.16, the coil voltage - inductor current is shown. As it is seen, NMOS is turned on while the inductor current is falling and the voltage drop is $0.35V$ on average instead of $0.7V$. The efficiency is found as 70.8%. 29.2% of the energy is dissipated as shown in Figure 4.17. Most of the power is dissipated in the inductor due to the DC resistance of the inductor. Loss in the diode decreased by 0.21%. It is not significant because inductor current decreases fast. The time in which LSS is turned on is short. Also, a certain time is needed to detect after the coil voltage crosses $0V$ because of the delay. As a result, it is better to use asynchronous buck converter.

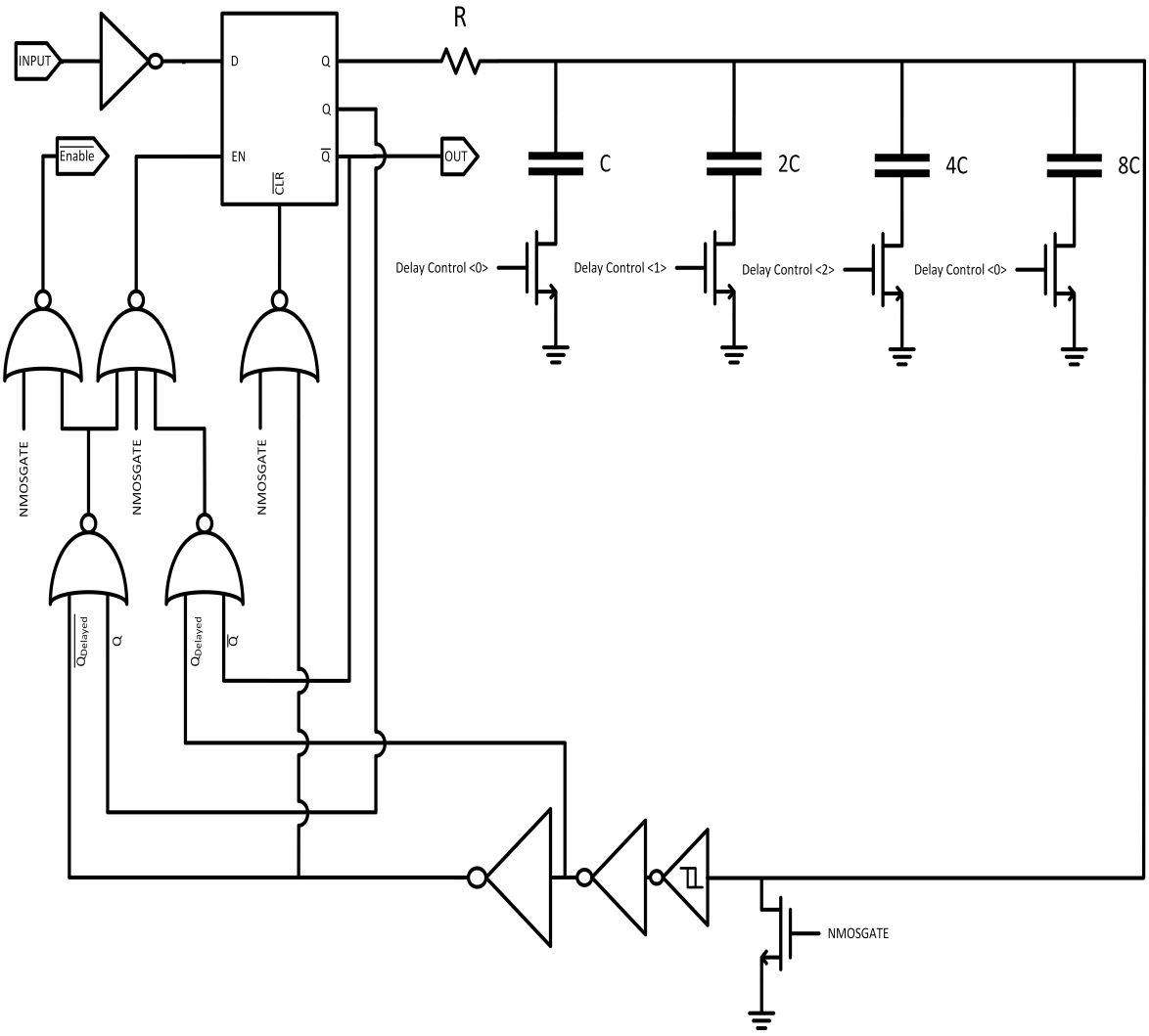

Figure 4.14. Pulse generator for the synchronous buck converter

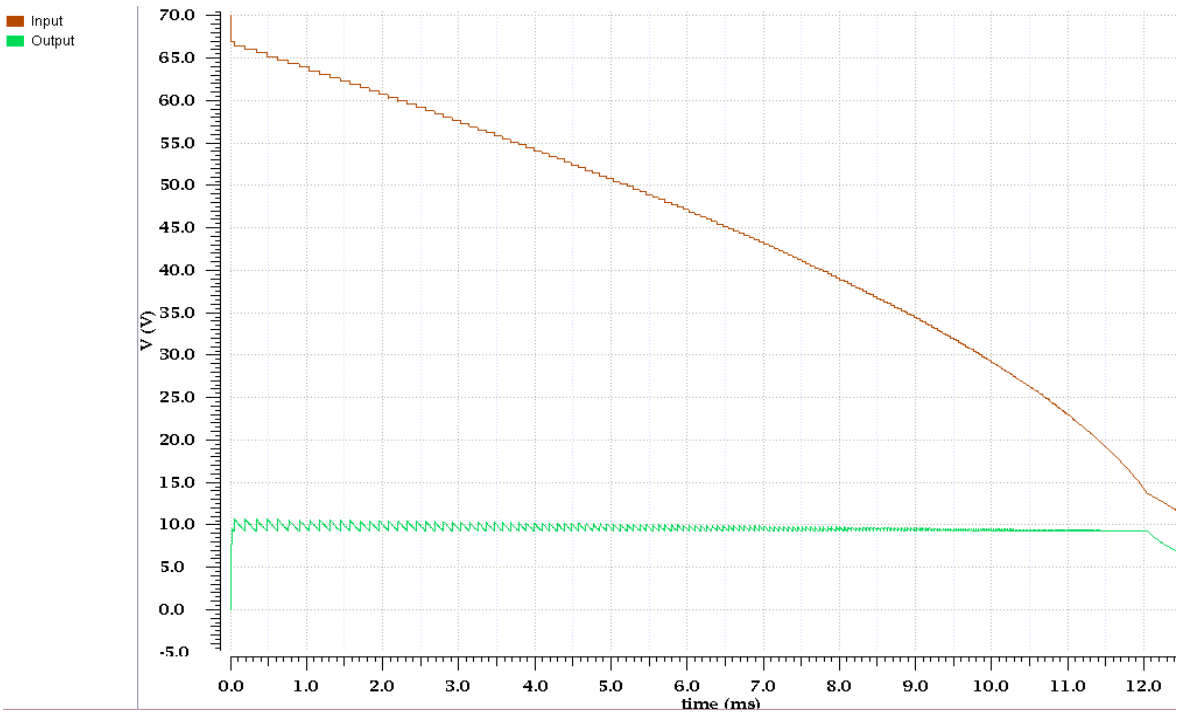

Figure 4.15. Transient analysis of schematic of the synchronous buck converter with the model inductor

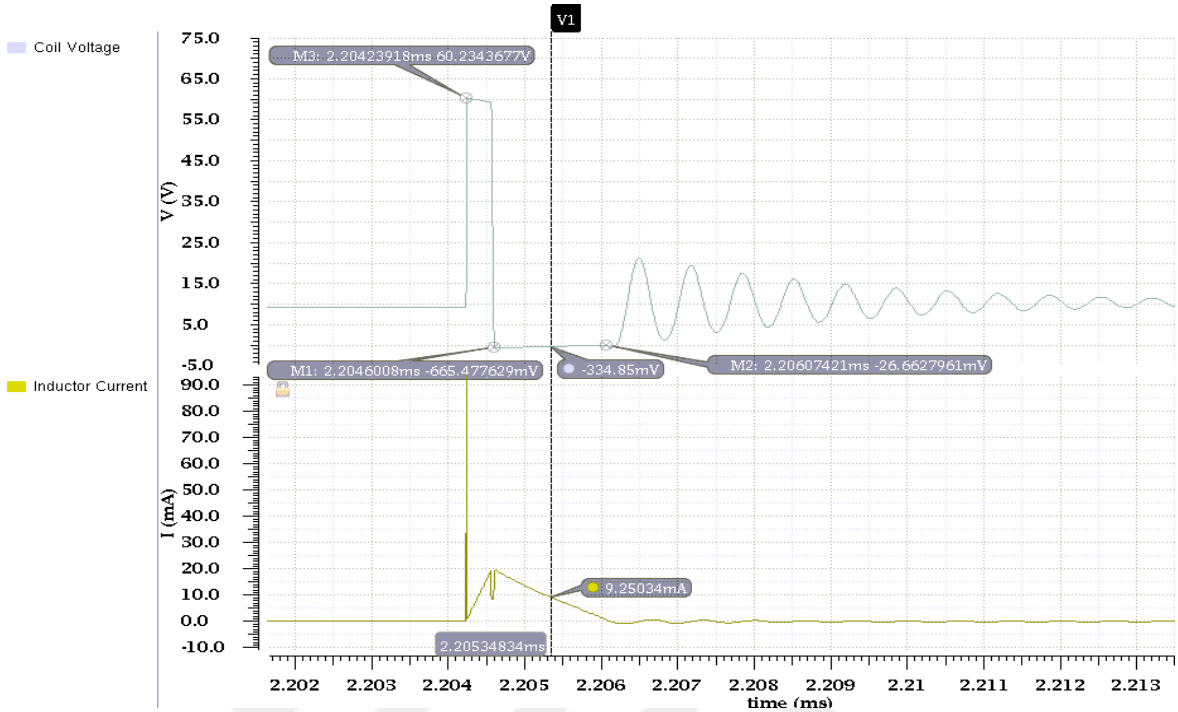

Figure 4.16. Coil voltage and inductor current in the synchronous buck converter with the model inductor

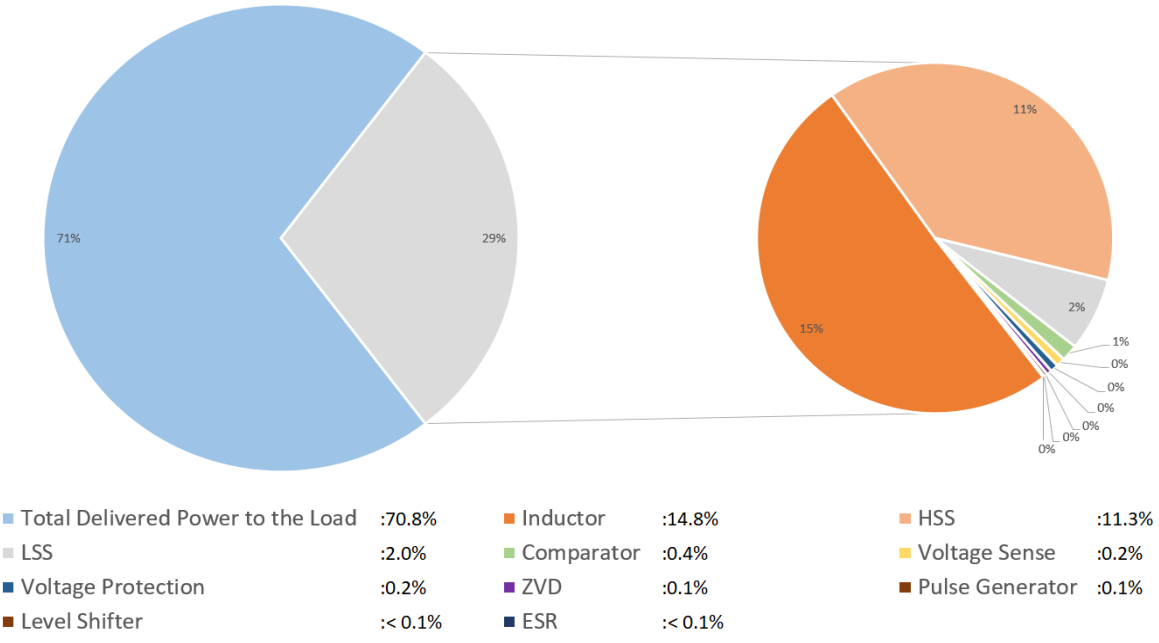

Figure 4.17. Power dissipation in the synchronous buck converter with the model inductor

5. CONCLUSION AND FUTURE WORK

A PFM DC-DC buck converter is proposed for low power high voltage applications in this study. The sub-blocks of the buck converter are explained. The power conversion efficiency is calculated for $70V$ input energy stored in a $10\eta F$ capacitor. It is found that $24\mu J$ is transferred to the output with the efficiency of 71%. Depending on the inductor model, it can be higher or lower.

Synchronous buck converter is also designed with same components of the asynchronous buck converter by making a few adjustments. The efficiency is found similar for both topologies. Therefore, the asynchronous converter is preferred due to simplicity and robustness.

5.1. Future Work

The proposed topology will be fabricated in TSMC $0.18\eta m$ BCD technology. The measurement of the integrated circuit will be done and the simulation results will be validated.

The buck converter is proper for low power application. It may not work in the high available power. For example, at the start of the operation, HSS is turned on until the input voltage decreases $3.5V$ or VDD supply voltage ($5V$) is provided to the sub-blocks. If the input power is large and harvesting occurs continuously, $3.5V$ voltage drop at the input does not occur. In this case, if the supply voltage does not provide to the circuit output voltage exceed the desired level and break down may occur. Improvements may be done in a start-up mechanism.

The system does not have any current or voltage limiter so it becomes more likely to encounter a breakdown if the input voltage or other components' values are much different from the calculated ones. Research is done and some techniques are implemented as a limiter but they were not good enough. Because the circuit is a

low power application, the power loss due to a limiter circuit is crucial. Besides, high voltage in the components is a challenge to apply limiter circuits. In the future, research may be conducted on limiter circuits for high voltage and low power applications.

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