YILDIRIM BEYAZIT UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

MODELING AND ANALYSIS OF MODULAR MULTILEVEL CONVERTER BASED STATIC SYNCHRONOUS COMPENSATOR

M.Sc. Thesis by
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Department of Electronics and Communication Engineering

June, 2016

ANKARA

MODELING AND ANALYSIS OF MODULAR MULTILEVEL CONVERTER BASED STATIC SYNCHRONOUS COMPENSATOR

A Thesis Submitted to the

Graduate School of Natural and Applied Sciences of Yıldırım Beyazıt University

In Partial Fulfillment of the Requirements for the Master of Science in

Electronics and Communication Engineering, Department of Electronics and Communication Engineering

by

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June, 2016

ANKARA

M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitle **''Modeling and Analysis of Modular Multilevel Converter based Static Synchronous Compensator''**completed by **Mehmet Zahid EREL** under supervision of **Assoc. Prof.Dr. Kamil Çağatay Bayındır** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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MODELING AND ANALYSIS OF MODULAR MULTILEVEL CONVERTER BASED STATIC SYNCHRONOUS COMPENSATOR

ABSTRACT

This thesis is concentrated on the modeling and analysis of the modular multilevel converter based on static synchronous compensator (MMC-STATCOM). In order to obtain the most suitable switching method for MMC-STATCOM, Scalar PWM methods such as level-shifted carrier based PWM methods and phase-shifted carrier based PWM method are compared considering equivalent switching count in a phase leg without any control structures. Moreover, Nearest Level Control method is also implemented to the MMC and that of performance analysis is discussed. Taking into account overall control parts of the MMC; active and reactive power control, DC-link voltage control, output current control and also submodule capacitor voltage balancing methods are concerned. Finally, submodule capacitor voltage balancing methods such as; sort and selection method related to direct modulation and Phase-shifted PWM based control method are implemented to the MMC-STATCOM and also compared to each other considering static mode and dynamic mode of the MMC-STATCOM having both inductive and capacitive mode ranges.

Keywords: MMC-STATCOM, Simulation, Dynamic Mode, Submodule Capacitor Voltage Balancing, Control

STATIK SENKRON KOMPENZATOR TABANLI MODÜLER ÇOK SEVİYELİ DÖNÜŞTÜRÜCÜNÜN MODELLENMESİ VE ANALİZİ

ÖZET

Bu tez çalışması statik senkron kompenzatör tabanlı modüler çok seviyeli dönüştürücünün (MÇSD-STATKOM) modellenmesi ve analizi üzerine yoğunlaşmıştır. MÇSD-STATKOM için en uygun anahtarlama metodunu elde etmede, seviye kaydırmalı taşıyıcı tabanlı DGM metodları ve faz kaydırmalı taşıyıcı tabanlı DGM metodu gibi basamaklı darbe genişlik modülasyon yöntemleri herhangi bir kontrol yapısı kullanılmadan tez faz bacağında eşit anahtarlama sayısı göz önünde bulundurularak karşılaştırıldı. Ilave olarak, en yakın seviye kontrol metoduda MÇSD' ye uygulandı ve onun performans analizleri ilgili tabloda verildi. MÇSD' nün tüm kontrol bölümleri ele alındığında, aktif ve reaktif güç kontrolü, DC bara gerilim kontrolü, çıkış akım kontrolü ve aynı zamanda altmodül kapasitor gerilim dengeleme metodları ele alınmıştır. Sonuç olarak, direk modülasyonla ilgili olan sıralama ve seçme metodu ve faz kaydırmalı DGM tabanlı kontrol metodu gibi altmodül kapasitor gerilim dengeleme metodları statik senkron kompenzatör tabanlı modüler çok seviyeli dönüştürücüye uygulandı ve aynı zamanda hem indüktif hemde kapasitif mod sıralı MÇSD-STATKOM'un statik ve dinamik modları göz önünde bulundurularak karşılaştırma yapıldı.

Anahtar Kelimeler: MÇSD-STATKOM, M-STATKOM, Simülasyon, Statik Mod, Dinamik Mod, Altmodül Kapasitör Gerilim Dengeleme, Kontrol

ACKNOWLEDGEMENTS

Initially, I want to thank my supervisor Assoc. Prof. Dr. Kamil Çağatay Bayındır, for helping me to prepare this thesis and to choose this topic. I want also to thank my family for their supports.

2016, 28 June **Mehmet Zahid EREL**

CONTENTS

ABBREVIATIONS

AC	Alternative Current
APOD	Alternative Phase Opposition Disposition
CHB	Cascaded H-Bridge
DC	Direct Current
DSCC	Double Star Chopper Cell
FC	Flying Capacitor
FFT	Fast Fourier Transform
HVDC	High-Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LS	Level-shifted
MMC	Modular Multilevel Converter
MMC-STATCOM	Modular Multilevel Converter Statcom
NPC	Neutral-Point-Clamped
NLC	Nearest Level Control
PD	Phase Disposition
POD	Phase Opposition Disposition
PLL	Phase-Locked Loop
PR	Proportional Resonant
PS	Phase-Shifted
PWM	Pulse-Width Modulation
RMS	Root Mean Square
SHE	Selective Harmonic Elimination
SM	Submodule
STATCOM	Static Synchronous Compensator
SVC	Space Vector Control
THD	Total Harmonic Distortion
VSC	Voltage Source Converter

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LIST OF SYMBOLS

V_{up}	Upper arm voltage
i_{up}	Upper arm current
i_{cc}	Circulating current
f_{c_eq}	Equivalent switching frequency
f_c	Carrier frequency
ma	Modulation amplitude
mf	Modulation frequency
N	Number of submodule per arm
i_d	Active current component
i_q	Reactive current component

CHAPTER 1

INTRODUCTION

There are a few types of multilevel converter topologies. These are called as: Neutral-Point-Clamped, Flying Capacitor, Cascaded H-Bridge and Modular Multilevel Converters. Nevertheless, fundamental concepts are identical, some differences can be observed in terms of control structures. When comparing with other multilevel converter concepts, modular multilevel converter has specific properties with regard to capacitor voltage balancing and multicarrier PWM modulation methods. In this dissertation, Modular Multilevel Converter topology is analyzed in detail. Different submodule or cell topologies can be used in modular multilevel converter applications. By connecting the cascaded submodules in series or shorting out, desired output voltage waveform can be obtained in staircase structure considering modularity and scalability of the converter. Thus; modular multilevel converter topology can be implemented to medium and high voltage applications. STATCOM is one of the application areas of the Modular multilevel converter. In this dissertation, STATCOM based on modular multilevel converter is hereafter called MMC-STATCOM is studied.

In literature, MMC-STATCOM applications are tested in many aspects. One of the different testing scenarios is to provide voltage to the offshore wind farm and eliminate the flicker [1]. Under different load condition, MMC-STATCOM is tested. Balancing load condition is used to support the simulation results [2]. Additionally, unbalanced load structure is used to prove the compensation effect and different than other four wire topologies is preferred [3]. The submodule can be modeled in different ways. Mathematical modeling is preferred and reactive current detection method is used [4]. Different capacitor voltage balancing methods are implemented to MMC-STATCOM. Direct modulation capacitor voltage balancing method is used and MMC-STATCOM is tested according to static mode and dynamic mode in [5,6]. Half-bridge and full-bridge submodule structures can be used in statcom applications. Full-bridge submodule structure has been used in delta

connection in [7,8]. Model predictive controller has been used in replace of current tracking controller. Hence; the faster and accurate response is obtained in [9]. To improve the dynamic response of the system a new capacitor voltage balancing method in cooperate with the averaging control is proposed and proved under different load conditions in [10]. In [11], enhanced capacitor voltage balancing strategy which consists of the control of active power loop, arm and individual capacitor balancing methods is suggested. Moreover, distribution statcom structure is implemented to the MMC. Two controller structure which are static var generation and compensation conditions have been proposed and results obtained have been validated with the help of simulation cases [12].

The first chapter is regarding to introduction of the thesis. In here, review of multilevel converter topologies and that of application areas are briefly explained. In chapter two, power circuit analysis and operation principle of the MMC are given. The analysis of the half-bridge based submodule topology is given and that of internal dynamic analysis is explained in detail. In chapter three, control strategies of the MMC are given in detail. Capacitor voltage balancing methods and modulation methods are discussed. Analysis and comparison of the switching methods are also mentioned. In chapter four, proposed control structures and proposed modulation methods are given. In chapter five, VSC based statcom structure, modeling of MMC-STATCOM, working principle of the MMC-STATCOM, simulation studies and performance comparison analysis, MMC design procedures and operation modes of the MMC-STATCOM are given. In chapter six, conclusion part is given.

1.1 Review of Multilevel Converter Topologies

The concept of multilevel converters has been a topic of research for more than four decades and is still a hot topic. The most common used multilevel converters can be grouped as follows:

1. Diode-Clamped (Neutral-Point-Clamped) Multilevel Converter (NPC)
2. Flying Capacitor (Capacitor-Clamped) Multilevel Converter (FC)
3. Cascaded H-Bridge (CHB)
4. Modular Multilevel Converters (MMC).

1.1.1 Neutral-Point-Clamped Multilevel Converter

Diode-clamped multilevel converter was suggested by Nabae, Takahashi, and Akagi in 1981 [13]. The NPC was initially suggested as a three-level inverter as shown in Figure 1.1 [14].

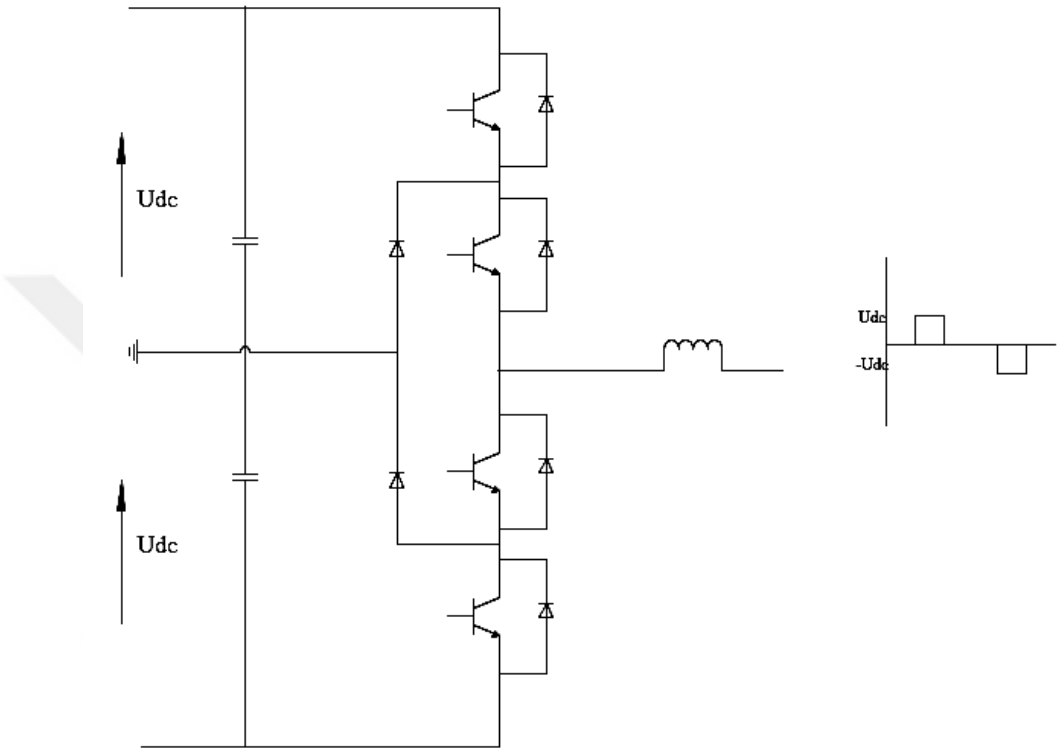


Figure 1.1 Single-phase three-level diode-clamped converter at left and output phase voltage waveform at right

To obtain N-level NPC, N-1 capacitors are required. Thus, N- level phase voltage and 2N-1 level phase-to-phase voltage can be obtained. The output voltage waveform quality has a better harmonic distortion when compared to two-level VSCs. NPC topology can be extended to more than three voltage levels. But, it has some drawbacks. If the number of output voltage level is increased, the number of needed clamping diodes increases. Therefore, increasing complexity and capacitor voltage balancing problems can be encountered as the number of voltage level increased [15].

1.1.2 Flying Capacitor Multilevel Converter

The topology of the Flying Capacitor Multilevel Converter was suggested by Meynard and Foch in 1992 [16]. A single phase of a flying capacitor multilevel converter is presented in Figure 1.2 [14]. When compared to NPC, it has more number of capacitors called ‘floating capacitors’. It also requires to be pre-charge of the floating capacitors before operated. Due to energy storage in the floating capacitors, Fying capacitor converter has ride through capabilities during outages and deep voltage sags. However, while rising the number of level, the number of required capacitors are to be increased. Such a large number of capacitors can lead to complexity in the control and cost problem. Additionally, footprint of the system which is undesired condition in the industry, also increases. Thus, the number of levels is generally limited to four [17].

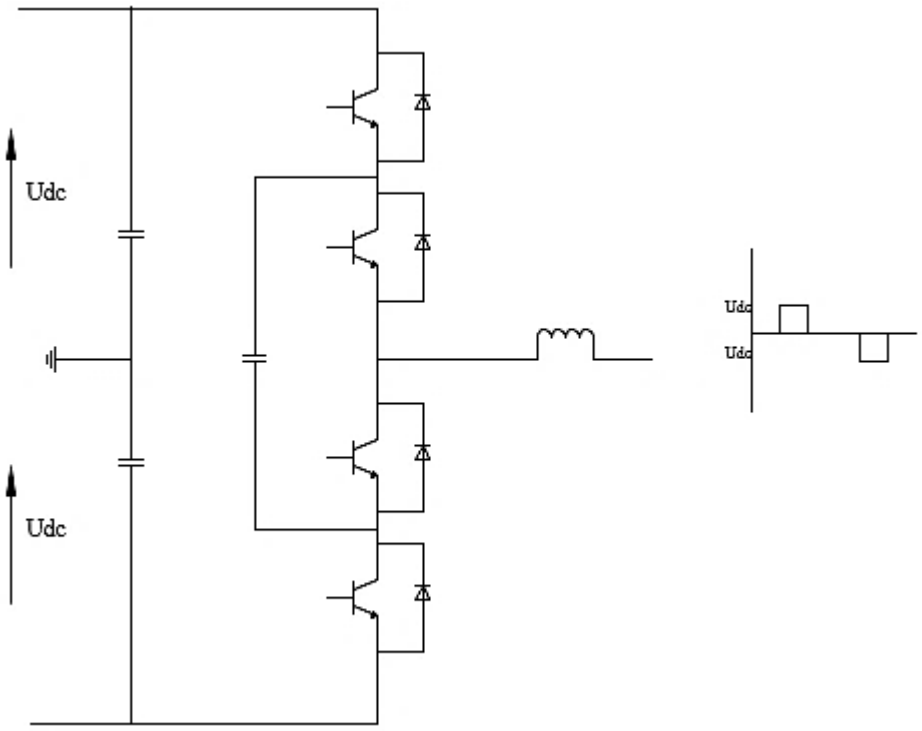


Figure 1.2 Flying capacitor multilevel converter at left and output phase voltage waveform at right

1.1.3 Cascaded H-Bridge Multilevel Converter

The Cascaded H-Bridge topology comprises of single phase full bridge inverter cells with separate DC sources as shown in Figure 1.3 [14]. Each converter cell capable of generating three voltage levels namely both polarities of the DC link voltage and zero condition. Switching states regarding to these output voltages are presented in Table 1.1. The basic pros of the CHB over the other topologies can be listed as in below.

1. Modular structure
2. Do not require any extra clamping diodes and capacitors
3. When compared to the FC and NPC topologies, CHB converter topology has least number of components for the same output voltage level condition.

The main drawback of this topology is the requirement of the isolated DC sources, thus; making it difficult for using higher levels in bidirectional power applications [15], [18].

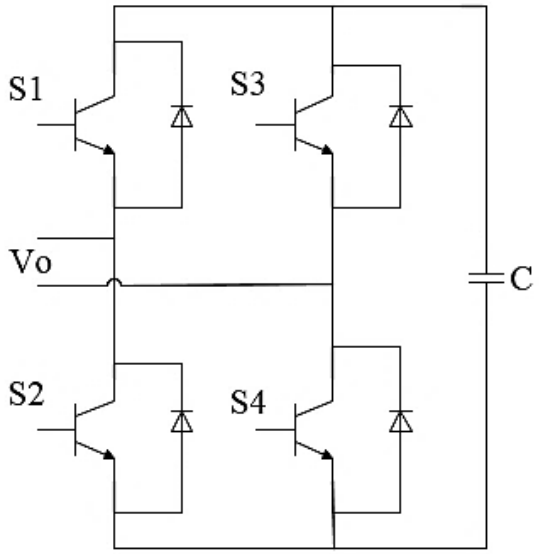


Figure 1.3 A Single phase of CHB converter structure

Table 1.1 Switching states for CHB converters

S1	S2	S3	S4	Vo
1	1	0	0	Vc
0	0	1	1	-Vc
1	0	1	0	0
0	1	0	1	0

1.1.4 Modular Multilevel Converter

Modular multilevel converter topology was initially suggested by Lescinar and Marquardt in 2003 [19]. The modular multilevel converter topology has been a topic of rising significance for medium and high-voltage applications. Typical application areas of the MMC can be classified as;

1. High voltage direct current transmission systems
2. Medium-voltage motor drives
3. Power Quality applications
4. Other application areas.

About each application areas is mentioned briefly.

1.1.4.1 High Voltage Direct Current Transmission Systems

It is significant to express that HVDC system constitutes an important place in transmitting electrical energy with a flexible and efficient way. It has more advantages that can be summarized as in below.

1. Considering transmitting distance, no limits
2. Very fast control of the power flow
3. Bi-directional power flow can be provided
4. HVDC transmissions have a high credibility rate, shown by more than three decades [20]

5. The main important feature of the HVDC system is synchronization of the two grids with frequencies of 60 Hz and 50 Hz, normally it is not possible with AC system applications.

HVDC transmission is still a developing technology. Today's most popular topic in multilevel converter applications is back-to-back MMC based HVDC as illustrated in Figure 1.4 [21].

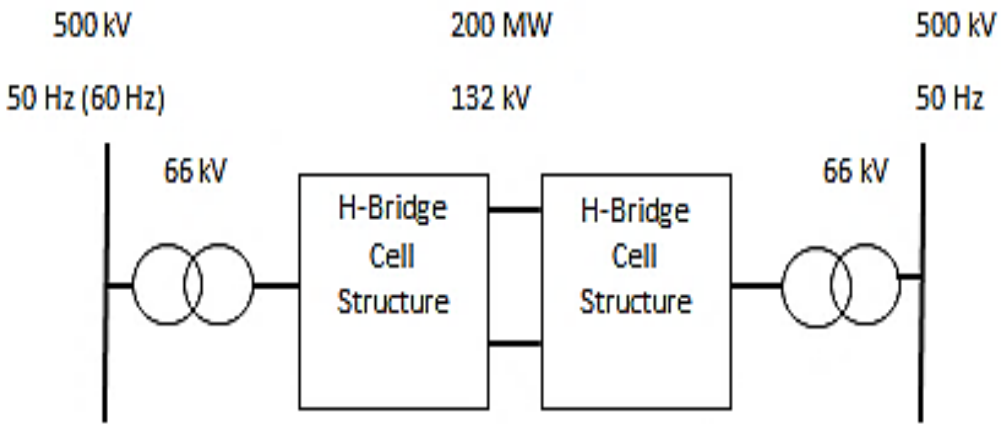


Figure 1.4 Circuit diagram of the back-to-back MMC based HVDC

1.1.4.2 Medium-Voltage Motor Drives Applications

Medium-voltage motor drives is another member of the MMC applications. One of the main technical difficulties of the medium-voltage motor drive applications is the high magnitude of the capacitor voltage ripple in low-speed operations due to floating capacitors. The magnitude of the voltage ripple is inversely proportional with the motor frequency [22].

1.1.4.3 Power Quality Applications

STATCOM is a static synchronous shunt compensator used to support AC power grids that have a poor power factor and voltage regulation problems in a transmission or distribution network. Thanks to provide flexible control, STATCOM is applied to multilevel converters and in so far as high modularity and low harmonic distortion on the output voltage waveform, modular multilevel converter is preferred for STATCOM applications. MMC-based shunt active power filter is suggested in [23]. A new dynamic voltage restorer based on MMC is suggested in [24]. Another example for power quality applications can be given as MMC-based unified power-flow controller [25].

The other application areas of the MMC can be given as interconnection with the railway electric traction systems and also in the electric ships [26]. Integrated energy storage systems based on MMC and that of interface between the photovoltaic panel and grid application [26] can be given as example of the application areas of the modular multilevel converter.

CHAPTER 2

OPERATION PRINCIPLE OF MODULAR MULTILEVEL CONVERTER

2.1 Power Circuit Analysis and Operation Principle of Modular Multilevel Converter

The schematic representation of the three-phase grid connected Modular Multilevel Converter topology is illustrated in Figure 2.1. It is related to the series connection of the submodules or cells.

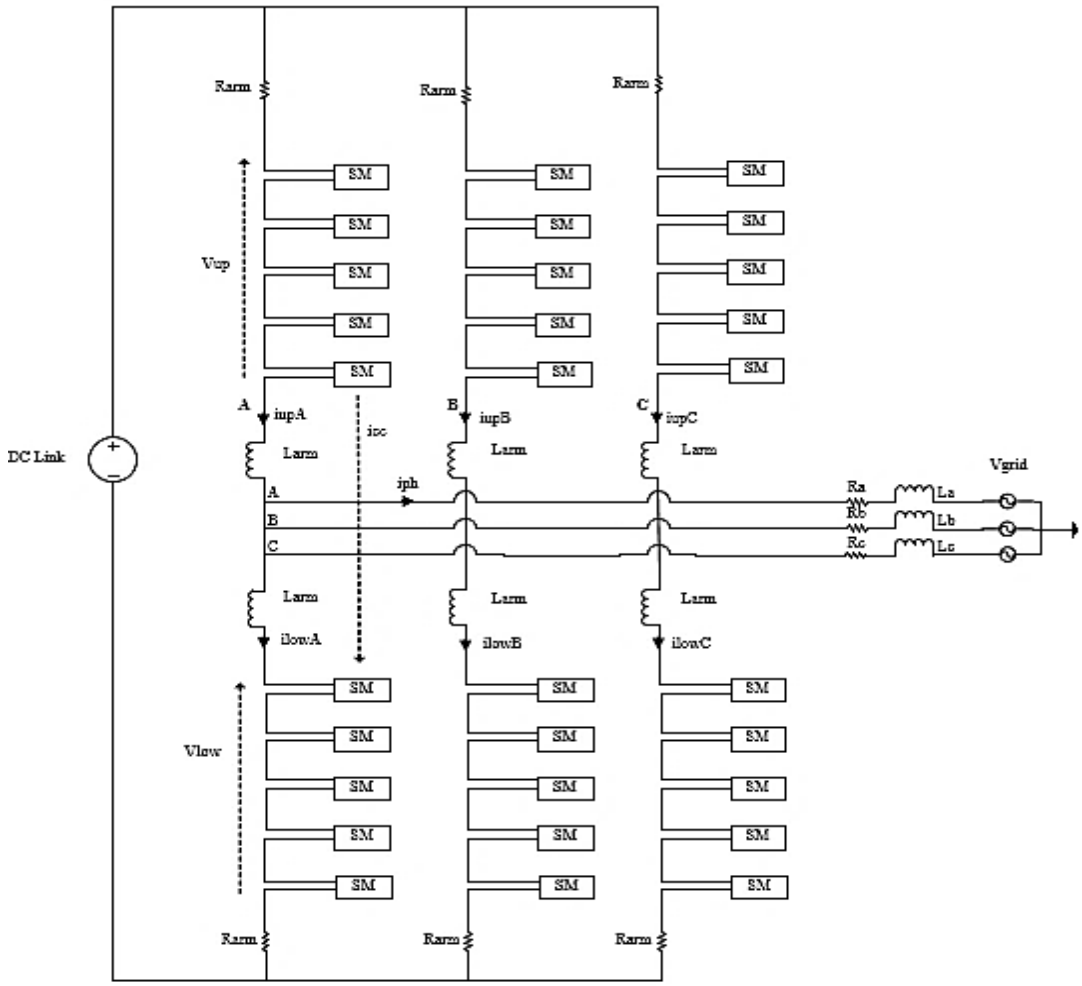


Figure 2.1 Circuit topology of the MMC

Each submodule of the Modular Multilevel Converter contains a capacitor and two IGBTs with anti-parallel diodes as shown in Figure 2.1 as known Double Star Chopper Cell Topology [27], is preferred in this thesis also hereafter called ‘‘Half-Bridge Cell’’. The series connection of the submodules consists of a phase leg of the MMC. Each phase leg is comprised of upper arm and lower arm also the number of submodules in each arm is equal to each other. Each phase arm is comprised of N identical submodules with cascaded structure, an arm inductor, Larm and an arm resistor, Rarm. Arm inductor is used for eliminating the fault currents in the converter. Arm resistor ought to be selected as low as possible due to converter power losses [28]. AC side terminal of the MMC is the common connection point between the arms.

The structure of the submodules can be formed in different circuitry. The half-bridge circuit, the full-bridge circuit or named as chopper-cell and bridge-cell and the unidirectional cell circuit structures are shown in Figure 2.2. The half-bridge circuit structure is preferred in this dissertation due to low switching losses and easy capacitor voltage balancing implementation. Submodules are inserted or bypassed depending on the switching positions in each half-bridge circuit. Two switches work in complementary way otherwise lead to short circuit condition. If the upper switch is ON and the lower switch is OFF, submodule is inserted in the arm. Thus; the terminal voltage of the Submodule is equal to the capacitor voltage, Vc. If the upper switch is OFF and the lower switch is ON position, submodule is bypassed in the arm. Therefore; the terminal voltage of the submodule is equal to zero.

Depending on the arm current direction, submodule capacitor voltages are affected. When the arm current direction is positive, submodule capacitors are charged otherwise capacitor voltages are discharged. Considering the switching states and direction of the arm current, terminal voltage of the submodule capacitor and charge/discharge status are indicated in Figure 2.3 [41] and Table 2.1 [41].

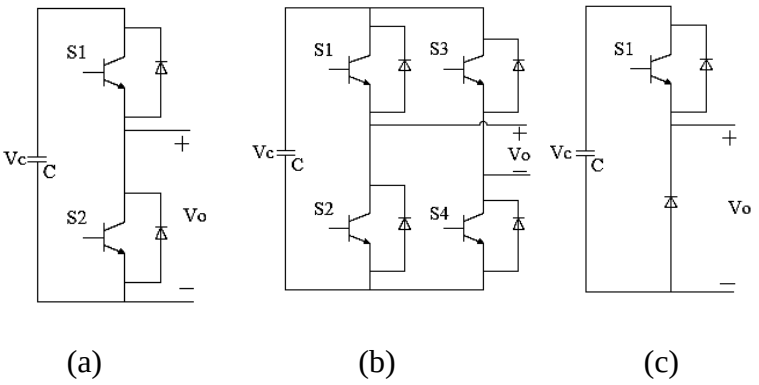


Figure 2.2 a) Half-bridge circuit, b) Full-bridge circuit, c) Unidirectional cell [65]

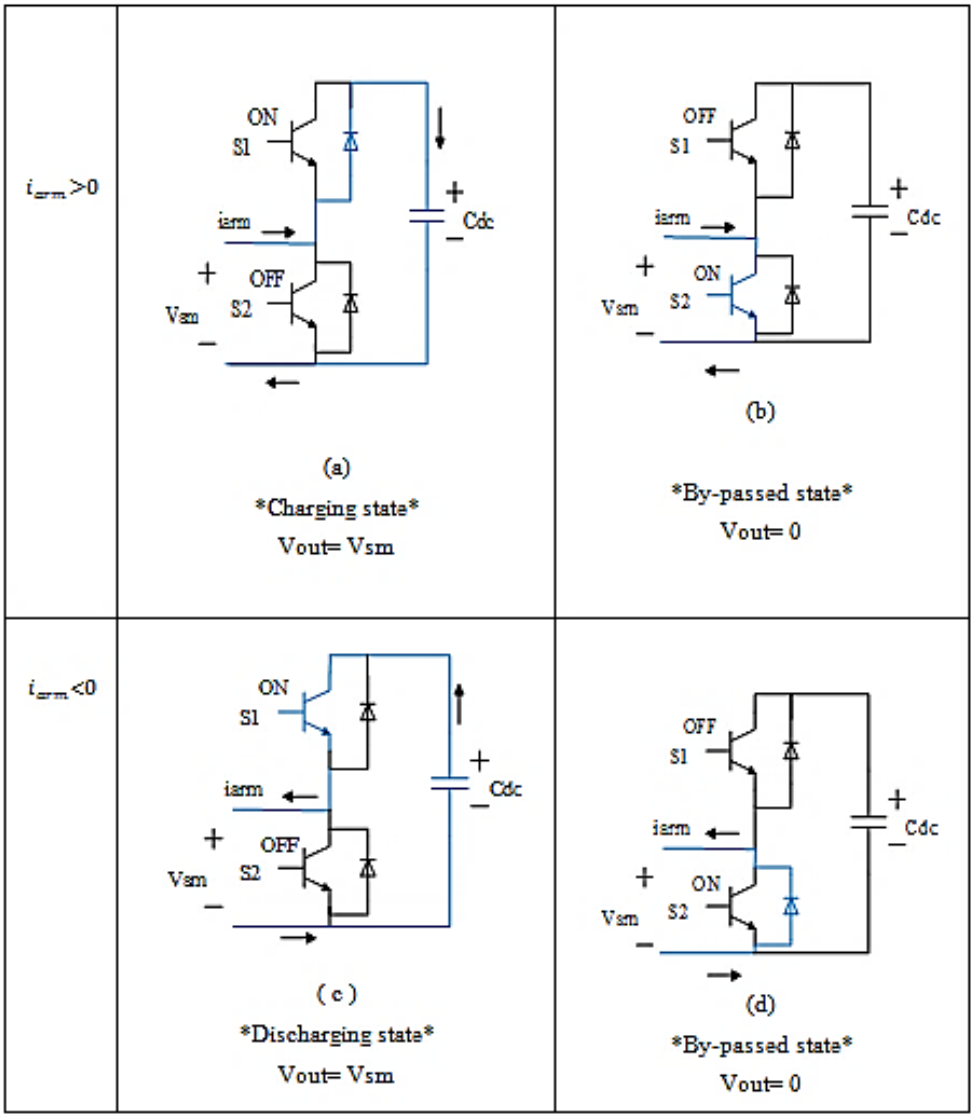


Figure 2.3 Submodule states and current paths [41]

Table 2.1 Switching states of the half-bridge based submodule

S1	S2	Arm Current Direction	Submodule Terminal Voltage	Status of the SM Capacitor
1	0	$i_{arm}>0$	Vsm	Charging
0	1	$i_{arm}>0$	0	By-Passed
1	0	$i_{arm}<0$	Vsm	Discharging
0	1	$i_{arm}<0$	0	By-Passed

In comparison with other multilevel converter structures, the main advantageous of the Modular Multilevel Converter can be summarized as in below [26]:

1. Modularity and making it easy to scale in any voltage level by using cascaded structure
2. Higher efficiency. Thanks to low switching frequency
3. Low THD performance. Due to use many submodules in the arm
4. High reliability. Due to use redundant submodules in the event of submodule failure
5. Absence of AC filters and DC link capacitors. Due to all the submodules share the common DC link.

2.2 Analysis of the Modular Multilevel Converter

Single phase MMC circuit structure is depicted in Figure 2.4. In here, DC link is named as V_{dc} and taking reference neutral point V_{dc} can be divided into two equal part, $\frac{V_{dc}}{2}$.

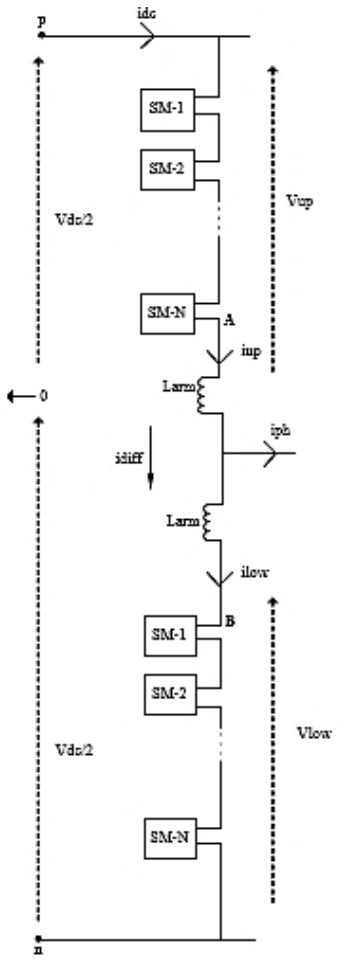


Figure 2.4 Circuit structure of a phase leg

In a phase leg of the MMC, V_{up} and i_{up} represent upper arm voltage and upper arm current, respectively. V_{low} and i_{low} indicate as lower arm voltage and lower arm current, respectively. i_{ph} represents the output phase current and i_{diff} is expressed as circulating current which is originated from the phase difference between the phase legs. Equations are taken from reference [26].

The number of the submodules in a phase arm is equal to N. If the submodule capacitor is represented as C_{SM}, arm capacitance, C_{arm}, is given as in Equation (2.1). Thus; the each arm voltages has N+1 level ranges from zero to V_{dc} with $\frac{V_{dc}}{N}$ level crossings.

$$C_{arm} = \frac{C_{SM}}{N} \tag{2.1}$$

The mathematical modelling of the output phase voltage is expressed as in Equation (2.2) and (2.3) for upper arm and lower arm, respectively.

$$V_{a0} = \frac{V_{dc}}{2} - (V_{up} + L_{arm}\frac{di_{up}}{dt} + R_{arm}i_{up}) \tag{2.2}$$

$$V_{a0} = -\frac{V_{dc}}{2} + (V_{low} + L_{arm}\frac{di_{low}}{dt} + R_{arm}i_{low}) \tag{2.3}$$

Arm currents are continuous currents which is sinusoid based. Each arm current has two fundamental components. These are half of the output current at the fundamental frequency and circulating current component as shown in Equation (2.4) and (2.5). Considering steady-state condition, DC link current is divided equally between the three phase legs. Additionally, circulating current component is equal to the one third of the DC link current.

$$i_{low} = \frac{i_{ph}}{2} + i_{diff} = \frac{i_{ph}}{2} + \frac{i_{dc}}{3} \tag{2.4}$$

$$i_{low} = -\frac{i_{ph}}{2} + i_{diff} = -\frac{i_{ph}}{2} + \frac{i_{dc}}{3} \tag{2.5}$$

It is important to mention that i_{up}, i_{low} and i_{ph} are the branch currents. However, circulating current component can not be directly measured.

Considering Kirchhoff current law, output phase current and circulating current component are defined as in Equations (2.6) and (2.7).

$$i_{ph} = i_{up} - i_{low} \tag{2.6}$$

$$i_{diff} = \frac{(i_{up} + i_{low})}{2} \tag{2.7}$$

DC part of the circulating current is responsible for active power transferring otherwise AC component is the undesired component and it must be suppressed. The methods regarding to eliminating of the circulating AC component is addressed in detail in following sections.

2.3 Internal Dynamic Analysis of the Half-Bridge Based Submodule in Modular Multilevel Converter

Arm currents and submodule capacitor voltages are affected from each other. For proper operation, arm currents and capacitor voltages should be controlled. Regarding Equations are taken from reference [66].

Submodule capacitor current is obtained with the help of multiplication of the switching function with arm current component as shown in Equation (2.8)

$$i_c(t) = S(t) i_{arm}(t) \tag{2.8}$$

In here, $S(t)$ represents the switching function, $i_c(t)$ and $i_{arm}(t)$ are expressed as capacitor current and arm current, respectively. Arm current components include harmonics at fundamental frequency and two times of the fundamental frequency. According to Equation (2.8), capacitor current is related with the arm current component so that harmonics of arm current are observed on submodule capacitor current. Due to the fact that submodule capacitor voltage is affected from the submodule capacitor current, dominant harmonics are also seen on capacitor voltages and lead to capacitor voltage ripple.

Output voltage of the submodule is related with the capacitor voltage and switching function. The relationship is defined as in Equation (2.9).

$$v_{0\_SM}(t) = v_C(t)S(t) \tag{2.9}$$

Normally, the sum of the output voltages of the submodules is equal to the DC link voltage. However, in addition to the DC link voltage, second order capacitor voltage ripple is observed as indicated in Equation (2.10) [22].

$$v_{up}(t) + v_{low}(t) = V_{dc} + \Delta v_{ripple} \tag{2.10}$$

Δv_{ripple} is observed on arm inductors and leads to circulating currents as shown in Equation (2.11). Thus; arm currents can be rearranged as expressed in Equations (2.12) and (2.13).

$$i_{cc}(t) = \frac{\Delta V_{ripple}}{j2\omega 2L_{arm}} \tag{2.11}$$

$$i_{up} = \frac{I_{dc}}{3} + \frac{i_{ph}}{2} + i_{cc} \tag{2.12}$$

$$i_{low} = \frac{I_{dc}}{3} - \frac{i_{ph}}{2} + i_{cc} \tag{2.13}$$

In here, ΔV_{ripple} and i_{cc} represent the second order capacitor voltage ripple and circulating current component, respectively.

CHAPTER 3

ANALYSIS OF MMC CONTROL STRATEGIES

Control and switching methods of the modular multilevel converter can be considered in a similar manner with other conventional two level VSCs to a certain extent. Output current control, DC link voltage control and active, reactive power control methods are basically similar to two level VSCs. Nevertheless, It has some different aspects as well. As a matter of fact that, MMC has floating capacitors requiring extra capacitor voltage balancing methods. If this capacitor voltage balancing is not succeeded, operation and stability of MMC can not be achieved.

High Internal currents namely circulating currents may occur between phases and submodules of MMC. Due to this, output voltage waveforms may be distorted. Moreover, the presence of high internal currents in the converter requires another control method, circulating current suppression method that will be explained in following section. Circulating current component is not seen in the power transfer to the output and should be kept as low as possible via properly selected arm capacitance and arm inductance value. Additionally, low circulating current value results in efficiency improvement in the converter.

Many strategies have been suggested so as to keep floating capacitor voltage to a desired value and eliminate the AC component existing in current wave. Two of the most popular control strategies for capacitor voltage balancing and circulating current AC component eliminating are discussed in following section. These switching and balancing methods have been proposed in [19] by Lescinar and Marquardt. The other one is based on phase-shifted PWM and suggested in [30] by Hagiwara and Akagi. Overall control parts can be listed as in below.

1. Active and Reactive power control of the MMC
2. DC link control of the MMC
3. Circulating current control of the MMC
4. Capacitor voltage balancing of the MMC.

3.1 Active and Reactive Power Control of the MMC

The most commonly used power flow control method is dq synchronous reference frame. To be able to analysis dq synchronous reference frame, the complex power is given in Equation (3.1). Using complex power, active and reactive ones can be obtained [69] as in Equations (3.2) and (3.3).

$$S_{dq} = \frac{3}{2} V_{dq} I_{dq}^{*} = \frac{3}{2} (V_d + jV_q)(i_d - ji_q) \quad \textbf{(3.1)}$$

$$P = \frac{3}{2} (V_q i_q + V_d i_d) \quad \textbf{(3.2)}$$

$$Q = \frac{3}{2} (V_q i_d - V_d i_q) \quad \textbf{(3.3)}$$

When PLL aligns d-axis with grid voltage vector, E_q becomes zero. Thus, power terms shown in Equations (3.2) and (3.3) reduce to the Equations (3.4) and (3.5) as shown in below [69]. Moreover, reference active and reactive currents are indicated as in Equations (3.6) and (3.7). In here, i_d^{*} and i_q^{*} define the active and reactive currents, respectively. P^{*} and Q^{*} express the active and reactive powers, respectively.

$$P = \frac{3}{2} (V_d i_d) \quad \textbf{(3.4)}$$

$$Q = -\frac{3}{2} (V_d i_q) \quad \textbf{(3.5)}$$

$$i_d^{*} = \frac{2}{3V_d} P^{*} \quad \textbf{(3.6)}$$

$$i_q^* = -\frac{2}{3V_d} Q^* \quad \textbf{(3.7)}$$

Taking into consideration that the power Equations, the only variable to control power is either i_d for active power or i_q for reactive power. In Equations, V_d value is constant. The powers which are active and reactive are controlled linearly with changing i_d or i_q, respectively.

Output power control of the modular multilevel converter is identical to conventional two or three level converters' power flow control methods. Overall scheme of the decoupled based active and reactive power control method is illustared in Figure 3.1. Initially, in order to synchronize the converter output current with the grid voltage, PLL block is used. Measured grid voltages are the inputs of the PLL block and the output is the signal that is the phase angle of the grid voltage as seen in Figure 3.1and Figure 3.2.

Grid voltage and current values are seperated based on dq synchronous reference frame and also sent controller as feedback. I_d current is controlled to follow DC link voltage and active power. I_q current is controlled to follow reactive power. Afterwards, reference current values (i_d^*, i_q^*) are obtained from reference power values (P^*, Q^*) and sent to controller. Both components used are controlled with PI controllers. Then, reference voltage values based on dq rotating reference frame is transformed to the abc stationary reference frame.

Overall scheme of the phase-shifted PWM based active and reactive power control method is illustrated in Figure 3.2. In this control method, P^* and Q^* represent the instantaneous active and reactive powers [32]. *Vs* indicates the supply voltage. As seen in Figure 3.2, application of the active and reactive power control method differs from decoupled based active and reactive ones.

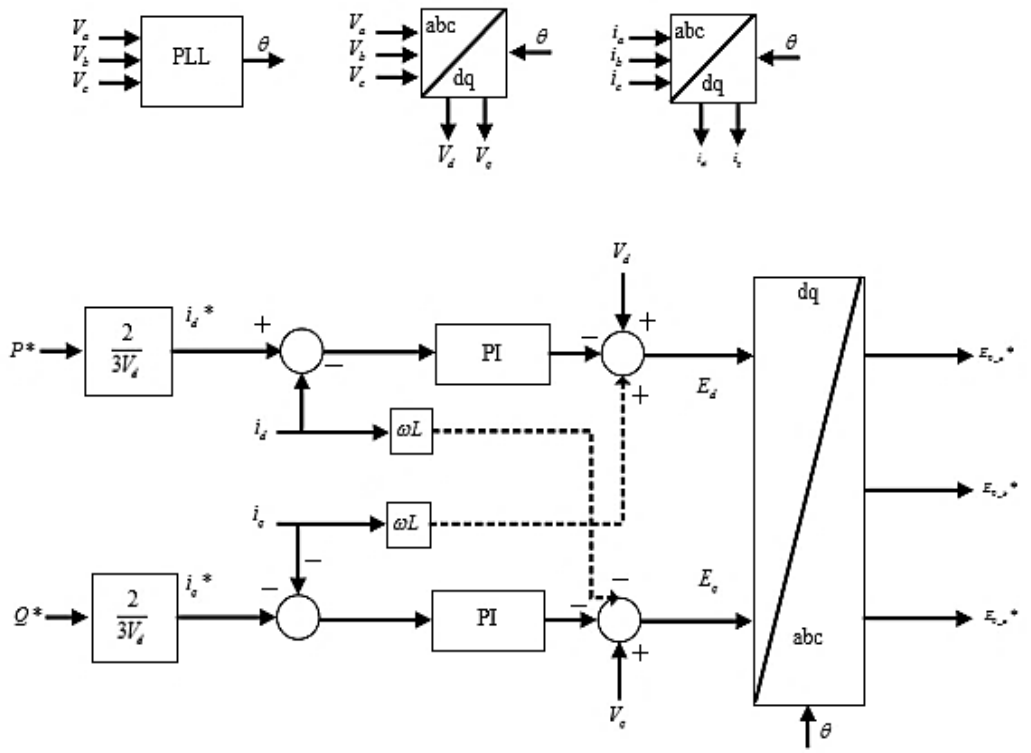


Figure 3.1 Decoupled based active and reactive power control method [31]

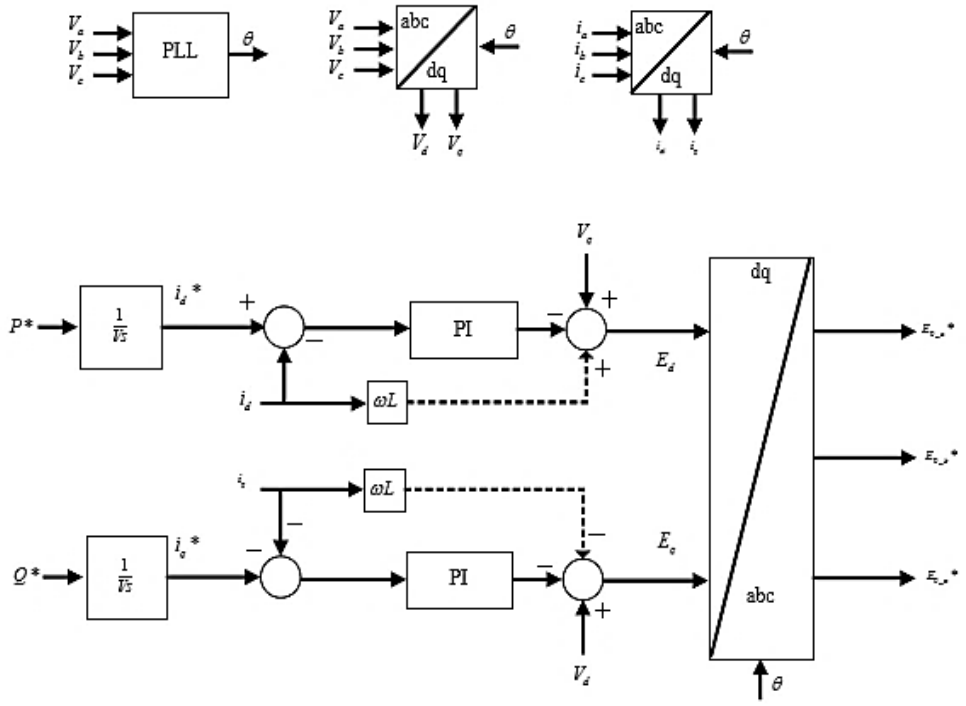


Figure 3.2 Phase-shifted PWM based active and reactive power control method [27]

In this thesis other control methods have been briefly mentioned and these are proportional resonant controller and predictive current control method. In this proportional resonant based control method transfer function of the controller is designed to make steady-state error zero at this stage where current reference is related with fundamental frequency value. The unique aspect of the proportional resonant controller is that it does not require two different controllers for positive and negative sequence components under unbalanced conditions. Overall control scheme is illustrated in Figure 3.3 [33].

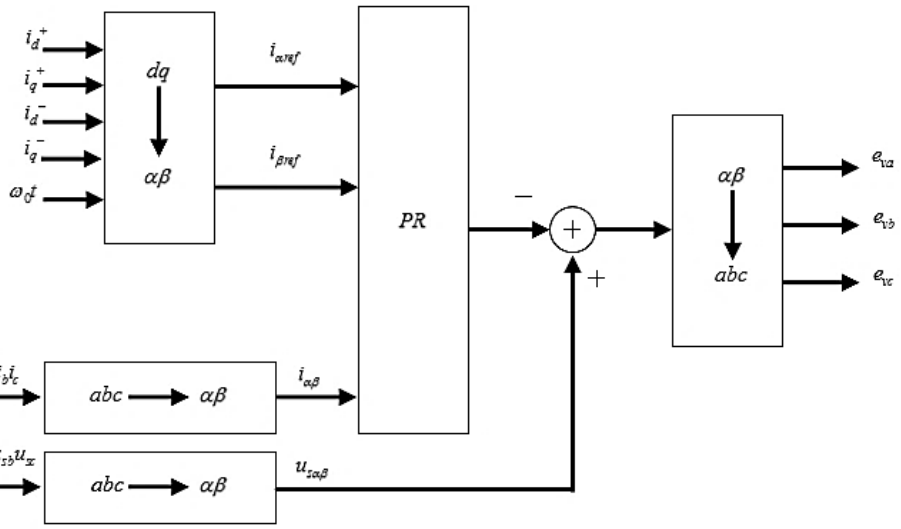


Figure 3.3 Proportional resonant based overall control method [33]

Another method mentioned in the literature is the predictive current control method [34-36]. In this method, firstly, matematical model of the modular multilevel converter is formed. According to the parameters to be controlled cost function is determined. Afterwards, the cost function value is calculated using mathematical model for all possible switching states and switching condition is applied when result is equal to minimum value. In this method, the whole controller parameters can be controlled simultaneously. On the other hand, determining the optimum cost function is the difficult part of the system. Another disadvantage of this method is required too much calculation in order to track optimization problem.

3.2 DC Link Control of the MMC

The DC link voltage of the MMC is formed by the sum of the submodule voltages inserted in a phase leg. Moreover, bulky DC link capacitor is not used as in other VSC systems. DC link voltage controller arranges the active current reference (i_d*) and also controls the power exchange among two sides which are DC and AC of the MMC [40].

Given that, at any one time instant the number of inserted submodules in a phase leg is equal to N, the equivalent DC link capacitance is determined as in Equation (3.8) where coefficient 3 comes from the number of MMC legs.

$$C_{dc\_eq} = 3\frac{C_{SM}}{N} \tag{3.8}$$

DC link voltage control is seen in Figure 3.4. The open loop transfer function of the system is given in Equation (3.9)[42].

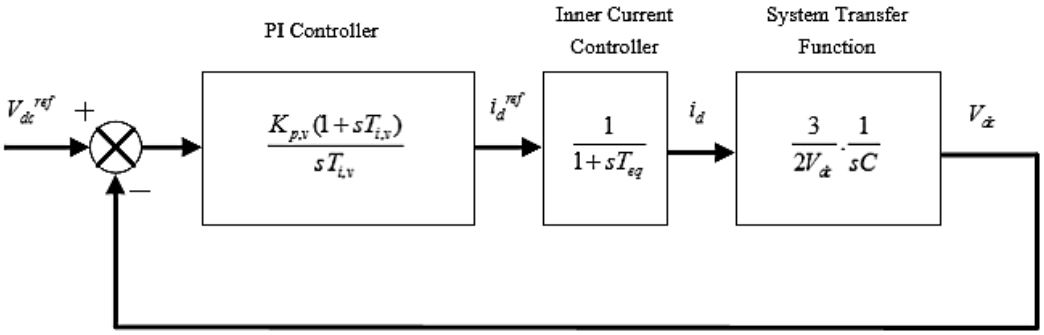


Figure 3.4 DC link voltage control

$$G_{volt} = \frac{K_{p,v}(1+sT_{i,v})}{sT_{i,v}} \cdot \frac{1}{1+sT_{eq}} \cdot \frac{3V_d}{2V_{dc}} \cdot \frac{1}{sC} \tag{3.9}$$

The controller parameters can be defined as in Equations (3.10) and (3.11). Tuning parameter, a, is determined within the range of 2-4 [42].

$$T_{i,v} = a^2 T_{eq} \tag{3.10}$$

$$K_{p,v} = \frac{2V_{dc}C}{3V_d T_{eq}} \tag{3.11}$$

3.3 Circulating Current Control of the MMC

3.3.1 Circulating Current Control Based on Direct Modulation

Circulating current control is one of the most crucial parts of the control system in the MMC. As in the Equation (3.12)[29], it consists of a dc component of the circulating current which is equal to one third of the DC link current and AC component of the circulating current. DC component of the circulating current is responsible for active power transferring to the the output terminal of the converter.

$$i_{cc} = i_{cc,dc} + i_{cc,ac} = \frac{i_{dc}}{3} + i_{cc,ac} \tag{3.12}$$

Considering AC part of the circulating current control system, the role of the AC part is to provide reactive power flow among the MMC legs. However, when it is taken into consideration, it leads to decreasing the efficiency of the MMC. Because of this, converter needs higher rated passive elements. Unless circulating current suppression is provided successfully, it can not be cost effective for the industrial applications. The AC component of the circulating current originates from the variations in the capacitor voltages of the submodules among the upper and lower arms of a phase leg. Additionally, phase difference between the MMC legs can be caused to the circulating current. Moreover, circulating current AC component can not be completely eliminated due to existing phase difference between the MMC legs. Thus, AC component of the circulating current ought be suppressed as far as possible. To eliminate the AC component of the circulating current, arm inductor value is so crucial, thus it should be selected suitable for MMC. Moreover to this, capacitor voltage ripple can lead to circulating current and AC component of the circulating current is also inversely proportional with the submodule capacitor voltages. Therefore, submodule capacitor voltages should be selected with an appropriate

value taken into account the cost effective condition for industrial applications. Circulating current based equivalent circuit of the MMC is illustrated in Figure 3.5.

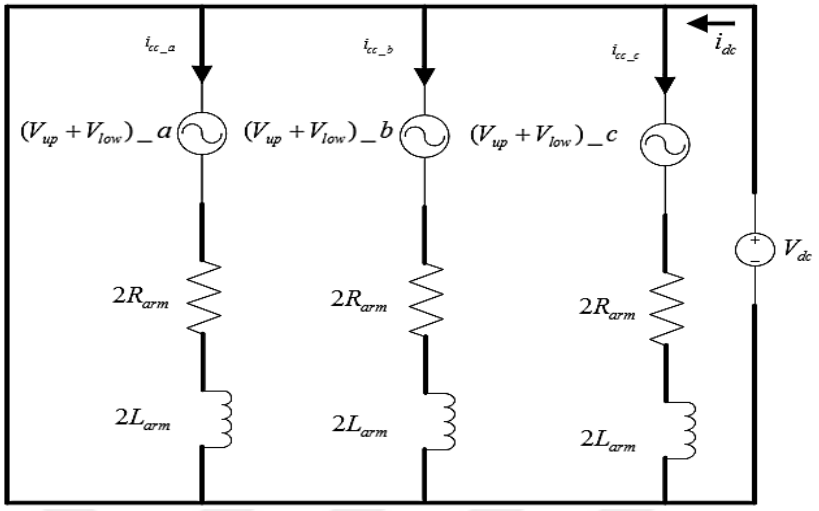
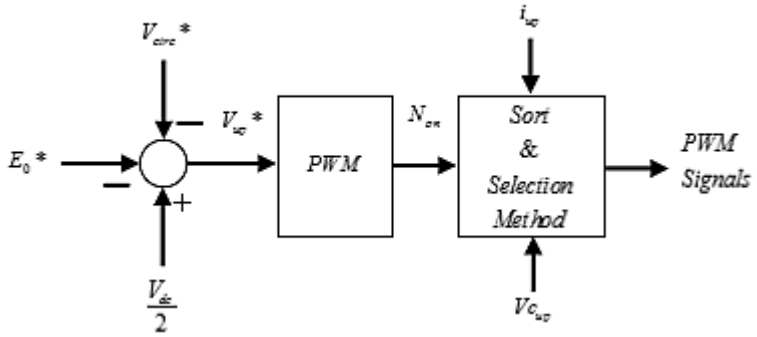


Figure 3.5 Circulating current based equivalent circuit of the MMC [70]

The circulating current dynamic can be explained by Equation (3.13) as in below.

$$2R_{arm}i_{cc} + 2L_{arm}\frac{di_{cc}}{dt} = V_{dc} - (V_{up} + V_{low}) \quad \textbf{(3.13)}$$

In this Equation (3.13), the only variable parameter is the sum of the arm voltages. Circulating current ought to not appear in the output control. Thus, control signal of the circulating current should be added as minus sign to upper and lower arm output voltage control signals as seen in Figure 3.6.



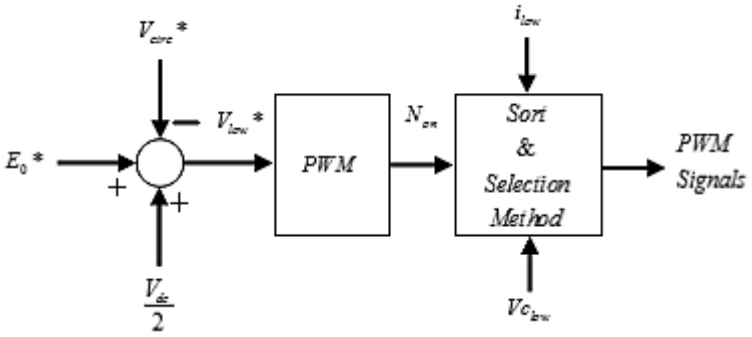


Figure 3.6 Overview of the upper and lower arm control signal including circulating current component [29]

In Figure 3.7, the structure of the circulating current elimination is illustrated as follows.

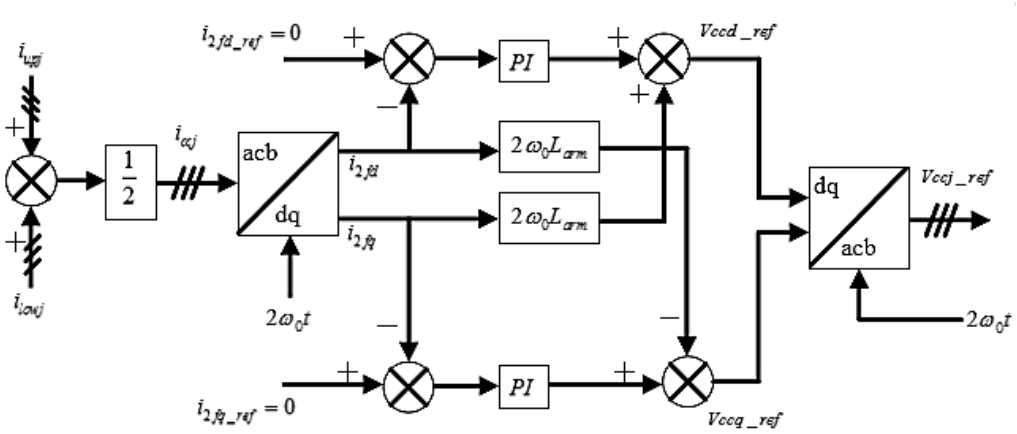


Figure 3.7 Circulating current second harmonic suppression structure [45]

The determination of the circulating currents using arm currents for three phase can be illustrated in Figure 3.8.

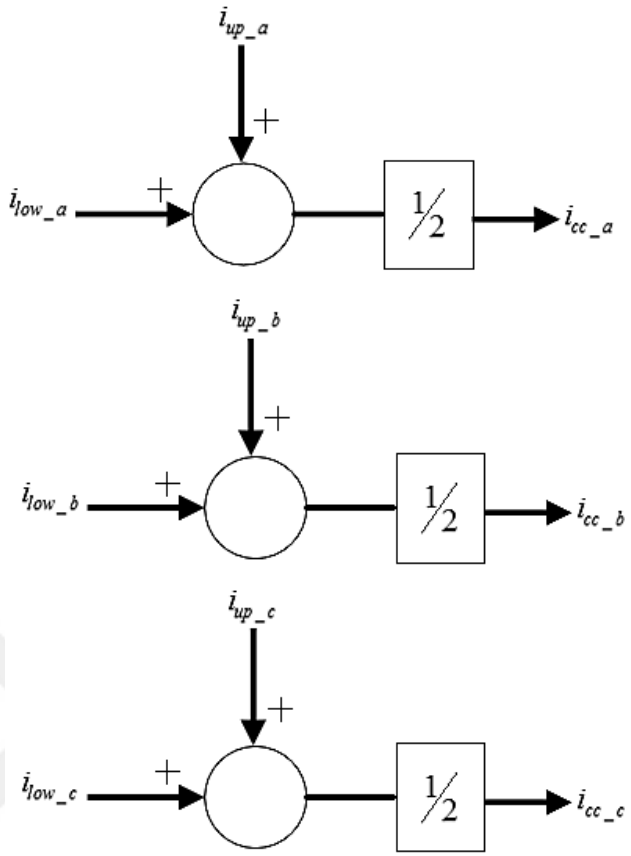


Figure 3.8 Determination of the circulating currents using arm currents

In circulating current second harmonic suppression structure, three phase circulating current components are transformed from abc stationary reference frame to the rotating dq reference frame. Notice that, the dominant AC component of the circulating current is related to the second harmonic. Moreover, second harmonic structure is in the form of negative sequence. PI controllers are used in this structure. The aim of the PI controllers is to follow the reference d and q parameters of the circulating current which are substantially set to zero. Then, reference currents are added and removed with the cross coupling terms for d and q parameters, respectively. Afterwards, the final reference signals are back convert to the abc stationary reference frame.

3.3.2 Circulating Current Control in Phase-Shifted PWM Based Control Method

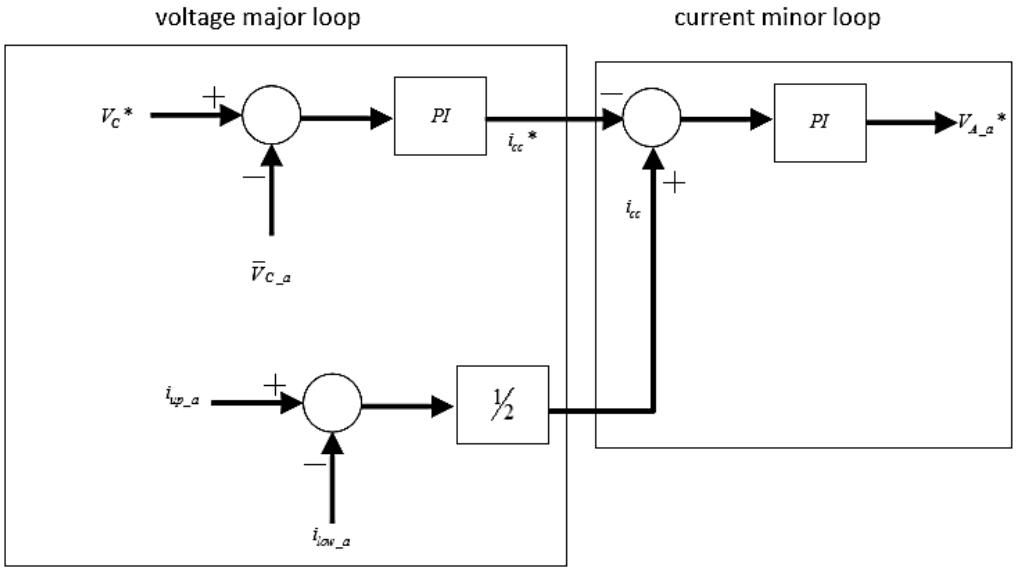


Figure 3.9 Phase-shifted PWM based circulating current control structure [30]

In phase-shifted PWM based control method, circulating current control is applied in averaging part of the capacitor voltage balancing method. As so in the direct modulation based circulating current control method, second harmonic is the dominant one and it has to be suppressed if it is desired to obtain good efficiency.

The working principle of the circulating current control structure is explained as follows:

1. The exact submodule capacitor voltage value of a phase leg is calculated by summing up of all the submodule capacitor voltages and then dividing it by the number of submodules in the MMC leg, also equal to 2N and compared with the reference submodule capacitor value
2. Error among the reference submodule voltage and real capacitor voltage value is detected
3. Obtained error is given to the PI controller block to produce a reference value for the circulating current control
4. The real circulating current value is calculated depending on the Equation (3.12)

5. Then, error between the exact value and reference value is determined.

Finally the error signal is sent to the PI controller block and averaging control signal is generated.

3.4 Capacitor Voltage Balancing Methods of the MMC

Capacitor voltage balancing structures are grouped as direct modulation based methods and Phase-shifted PWM based control method.

3.4.1 Analysis of Direct Modulation Based Capacitor Voltage Balancing Methods

Direct modulation methods can be grouped as sort and selection method and reduced switching frequency sort and selection method. In these methods, the aim is to charge the submodules with the lowest capacitor voltages and on the other side, discharge the submodules with the highest capacitor voltages depending on the arm current direction.

Initially, sort and selection method is explained and also shown in Figure 3.10. For each switching instant,

1. The submodule capacitors in a phase leg are measured and then indexed as in Equations (3.14) and (3.15) below

$$Vc\_up = [Vc\_up1, Vc\_up2, ..., Vc\_upn] \quad \textbf{(3.14)}$$

$$Vc\_low = [Vc\_low1, Vc\_low2, ..., Vc\_lown] \quad \textbf{(3.15)}$$

By indexing the submodule capacitor voltages from high to low, the N submodules with highest or lowest voltage are clearly determined for switching instant [44].

2. The direction of the arm current is determined

When the arm current is positive, all the submodules which are on-state ones charges. The last submodules are turned on which are included in the indexed array, but the other submodules are turned off. This condition results in submodule capacitor voltage rising with the lowest capacitor voltage. However, when the arm

current is negative, discharging condition is valid for all the submodules which are on-state. The first submodules are turned on which are included in the indexed array, but the other submodules are turned off. This condition results in submodule capacitor voltage decreasing with the highest capacitor voltage [46].

3. The desired number of submodules in on-state are calculated
4. The correct submodules are selected
5. According to selection of submodules, gate pulses are formed.

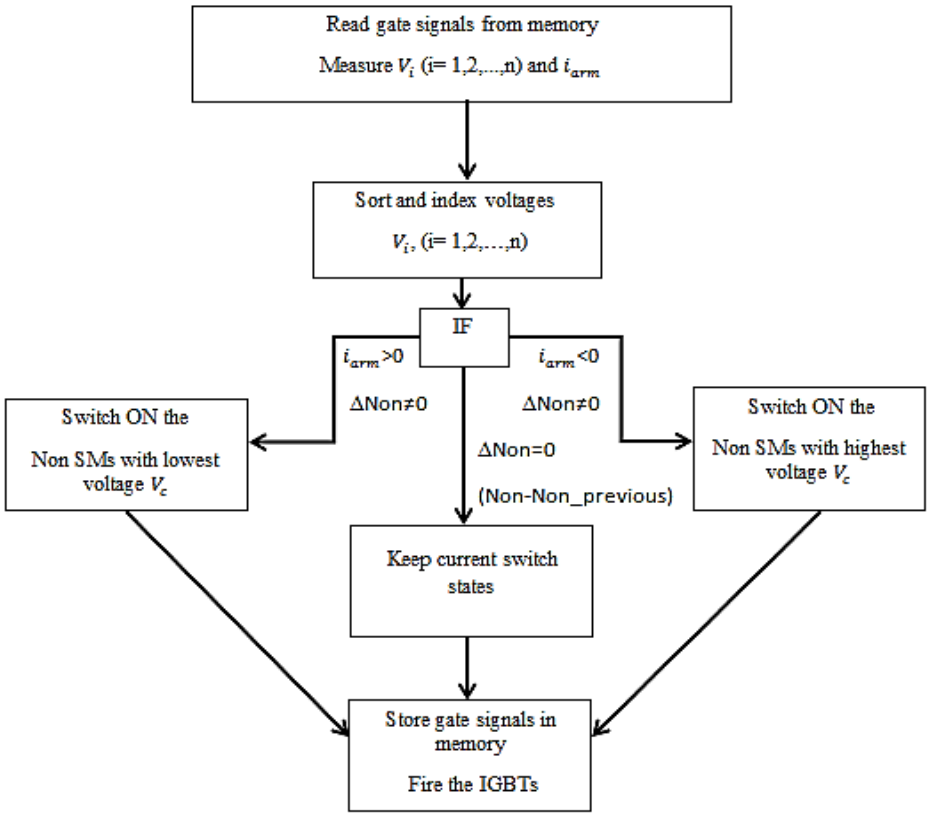


Figure 3.10 Sort and Selection method for MMC applications

Reduced switching frequency (RSF) sort and selection method is the other method that is suggested in [47]. The main purpose of this method is to decrease the switching number of the converter.

RSF sort and selection method can be clarified as follows and also shown in Figure 3.11.

1. While ΔNon changes during algorithm, $\Delta Non = Non(i) - Non(i-1)$ is calculated; $Non(i-1)$ means the previous time step of $Non(i)$
2. If ΔNon is positive, depending on the arm current polarity, additional submodules to the on-state conditions should be inserted to the current path. When comparing with sort and selection method, the unique part of this method is that only off-state submodules are considered for the selection, on the other hand sort and selection method performs the selection among all the submodules, both on-state and off-state submodules
3. If ΔNon is negative, depending on the arm current polarity, related submodules which are currently inserted ones, should be changed their condition to bypassed mode. When comparing with sort and selection method, the unique part of this method is that only the on-state submodules are considered for the selection. On the other hand, sort and selection method performs the selection among all the submodules, both on-state and off-state ones
4. If ΔNon is zero, submodules conditions are not changed.

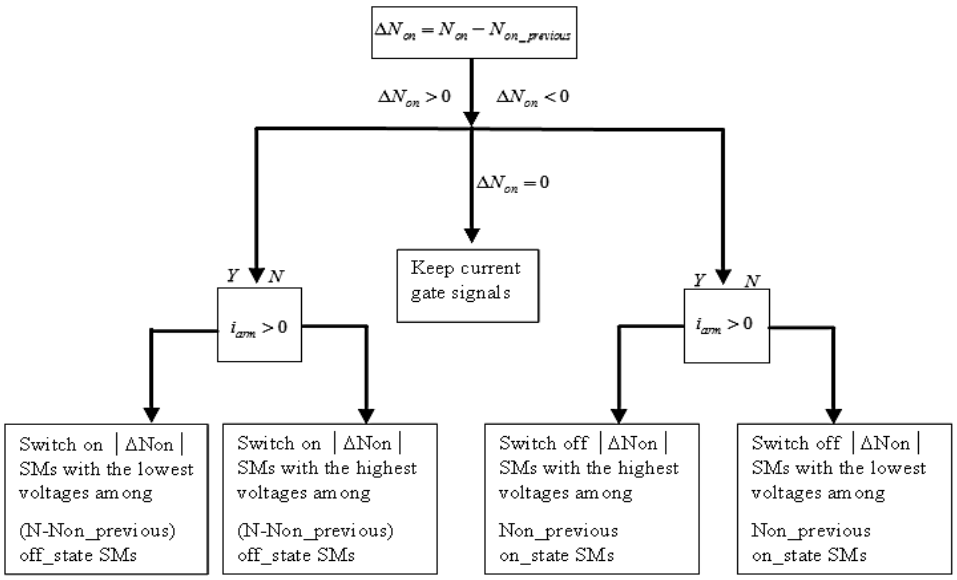


Figure 3.11 RSF sort and selection method [45]

3.4.2 Analysis of the Phase-Shifted PWM Based Capacitor Voltage Balancing Method

Lately, a novel strategy of the capacitor voltage balancing method has been proposed in [30] by Hagiwara and Akagi. The aim of the strategy is based on the equal arm energy share among the submodule capacitors. Considering direct modulation based sort and selection methods, each arm is represented by one reference voltage. On the other hand, in phase-shifted PWM based control method, each submodule is represented by its own voltage reference that is the main difference part of the Akagi method. Moreover, only phase-shifted carriers are used in this method.

Phase-shifted capacitor voltage balancing method can be represented in three groups as follows:

1. Averaging control part
2. Balancing control part
3. Arm balancing part.

Voltage commands of the upper and the lower arms are given in Figure 3.12 and Figure 3.13, respectively.

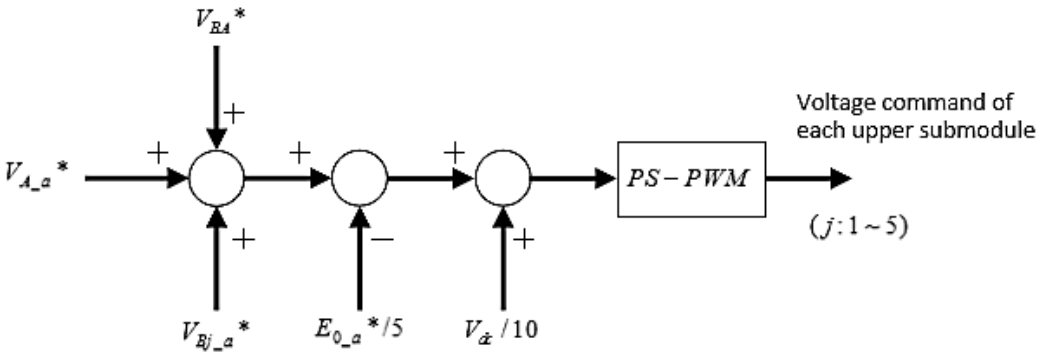


Figure 3.12 Voltage command of the upper arm

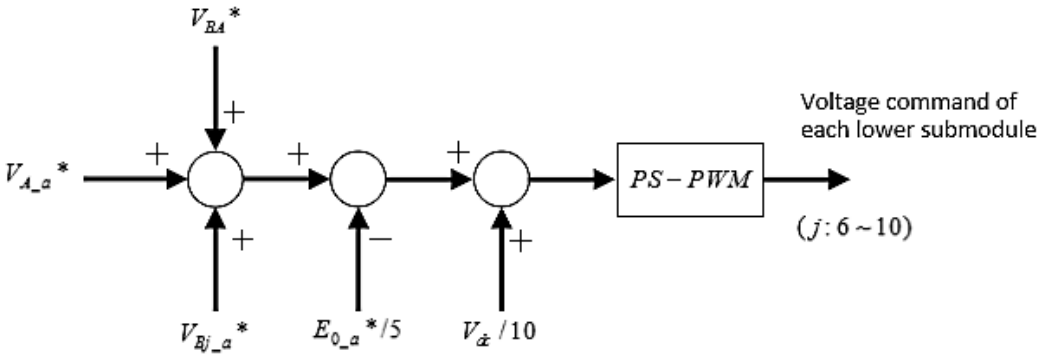


Figure 3.13 Voltage command of the lower arm

In here, V_{A_a}* means the reference averaging control signal, V_{Bj_a}* represents the reference individual balancing control signal and V_{BA}* also represents the reference arm balancing control signal. $V_{dc}/10$ indicates the feed-forward control of the arm control signals. PS-PWM is used for this capacitor voltage balancing method. Then, the output voltage control signal is compared with a triangular waveform having a maximum value of V_{dc}/N and minimum value of zero and that of carrier frequency f_c .

3.4.2.1 Averaging Control

The averaging control part of the capacitor voltage balancing method has to be applied to each leg of the MMC. The main purpose of the averaging control is to keep the submodule capacitor voltage at a desired value. The block diagram of the averaging control is given as in Figure 3.9. In here, Vc* is the submodule capacitor voltage reference and $\overline{Vc}\_a$ is the average voltage of all the submodule capacitors in a phase leg and defined as in Equation (3.16). i_{cc}* is the circulating current reference command. i_{up_a} and i_{low_a} are the arm current commands. Finally, V_{A_a}* is the final voltage command provided from the averaging control block.

$$\overline{Vc}\_a = \frac{1}{2}\sum_{j=1}^{2N} Vcj\_a \qquad \textbf{(3.16)}$$

The circulating current reference can be acquired from the Equation (3.17) as in below [30].

$$i_{cc}^{*} = K_1(Vc^{*} - \overline{Vc}\_a) + K_2\int(Vc^{*} - \overline{Vc}\_a)dt. \quad \textbf{(3.17)}$$

$V^{*}_{A\_a}$ is generated from the averaging control part and the Equation (3.18) [30] can be described as follows:

$$V_{A\_a}^{*} = K_3(i_{circ\_a} - i_{circ}^{*}\_a) + K_4\int(i_{circ\_a} - i_{circ}^{*}\_a)dt. \quad \textbf{(3.18)}$$

According to the voltage major loop part of the averaging control, if the reference submodule capacitor voltage value is bigger than the average voltage command value, then the circulating current reference increases and it forces to the circulating current to track the reference command signal. Moreover, average capacitor voltage command will track its reference capacitor voltage command separately from the load current [30].

3.4.2.2 Individual Balancing Control

Individual balancing method has to be formed in every submodule. The aim of this method related to the arm current direction is to keep the individual capacitor voltage at desired value. The block diagram of the individual capacitor voltage balancing is seen in Figure 3.14.

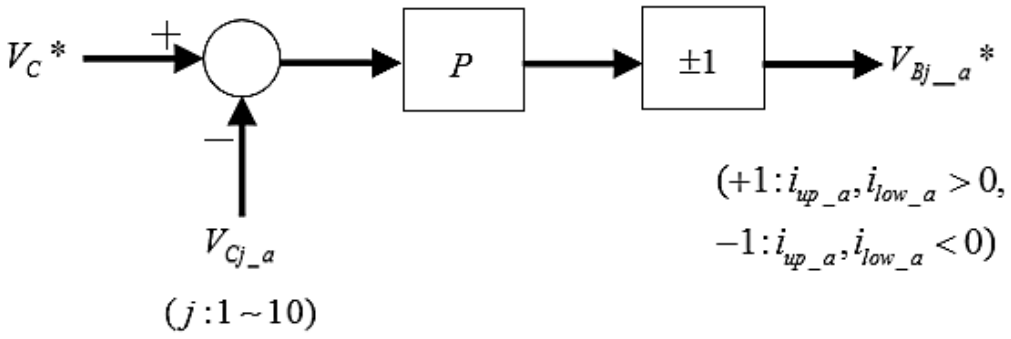


Figure 3.14 Block diagram of the individual capacitor voltage balancing method [30]

In here, V_C* and V_{Cj_a} represent the reference individual submodule capacitor value and each submodule capacitor value from 1 to 10 for phase a, respectively. P indicates the proportional control component and $V_{Bj\_a}*$ indicates the output control signal for individual balancing control.

Proportional control component is used for individual balancing control. The working principle of the individual balancing method is that when the polarities of the arm currents are positive, $V_C* \geq V_{Cj\_a}$ will be valid and also active power can be handled from the DC link. In other words, if the polarities of the arm currents are negative, $V_C* < V_{Cj\_a}$ will be valid.

Eventually, $V_{Bj\_a}*$, for j=1-5 is illustrated [30]as in Equation (3.19) when positive and negative of the upper arm current.

$$V_{Bj\_a}* = \left\{ P(V_C* - V_{Cj\_a}) \ (i_{up} > 0), \ -P(V_C* - V_{Cj\_a}) \ (i_{up} < 0) \right\} \quad \textbf{(3.19)}$$

While, $V_{Bj\_a}*$ for j=6-10 is illustrated [30] as in Equation (3.20) when positive and negative of the lower arm current.

$$V_{Bj\_a}* = \left\{ P(V_C* - V_{Cj\_a}) \ (i_{low} > 0), \ -P(V_C* - V_{Cj\_a}) \ (i_{low} < 0) \right\} \quad \textbf{(3.20)}$$

3.4.2.3 Arm Balancing Control

Arm balancing control method is illustrated in Figure 3.15. The purpose of this method is to eliminate the voltage difference between the average voltage of the both arms submodule capacitor voltages [27].

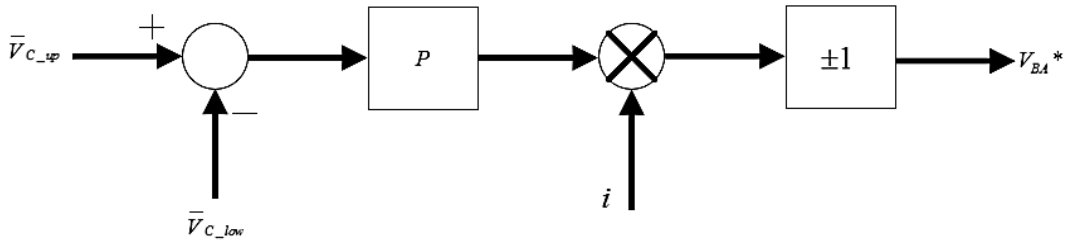


Figure 3.15 Arm balancing method [27]

In here, $\overline{V}_{C\_up}$ and $\overline{V}_{C\_low}$ define the average submodule capacitor voltages of the positive and negative arms, respectively. P indicates the proportional control and i means the supply current. V_{BA}* represents the output control signal for the arm balancing control method.

3.5 Analysis of Modulation Methods for MMC

Modular multilevel converters are classed in two categories in terms of switching methods: low frequency and high frequency switching. In low frequency switching converters have low switching count and thus high efficiency. But, drawback side of these low switching frequency methods are the dynamic response. At the same time, Nearest Level Control (NLC) can also applied to MMC studies particularly with high submodule numbers due to low harmonic distortion succeded. On the other hand, in high frequency switching, a reference output voltage waveform can be obtained such as sinusoidal is compared in magnitude with a high frequency triangular waveform and thus switching signal is generated. The unique part of this switching method is low output current and voltage harmonic distortion. Due to low harmonic distortion, converters does not need bulky and costly passive filters. Depending on different loading conditions, fast dynamic response is given compared with low frequency switching methods. Nevertheless, high frequency switching methods have higher switching loss than the low frequency switching methods. For sure, selecting suitable arm inductor and capacitor values for modular multilevel converter, losses can be decreased. The switching methods for modular multilevel converters are shown in Figure 3.16.

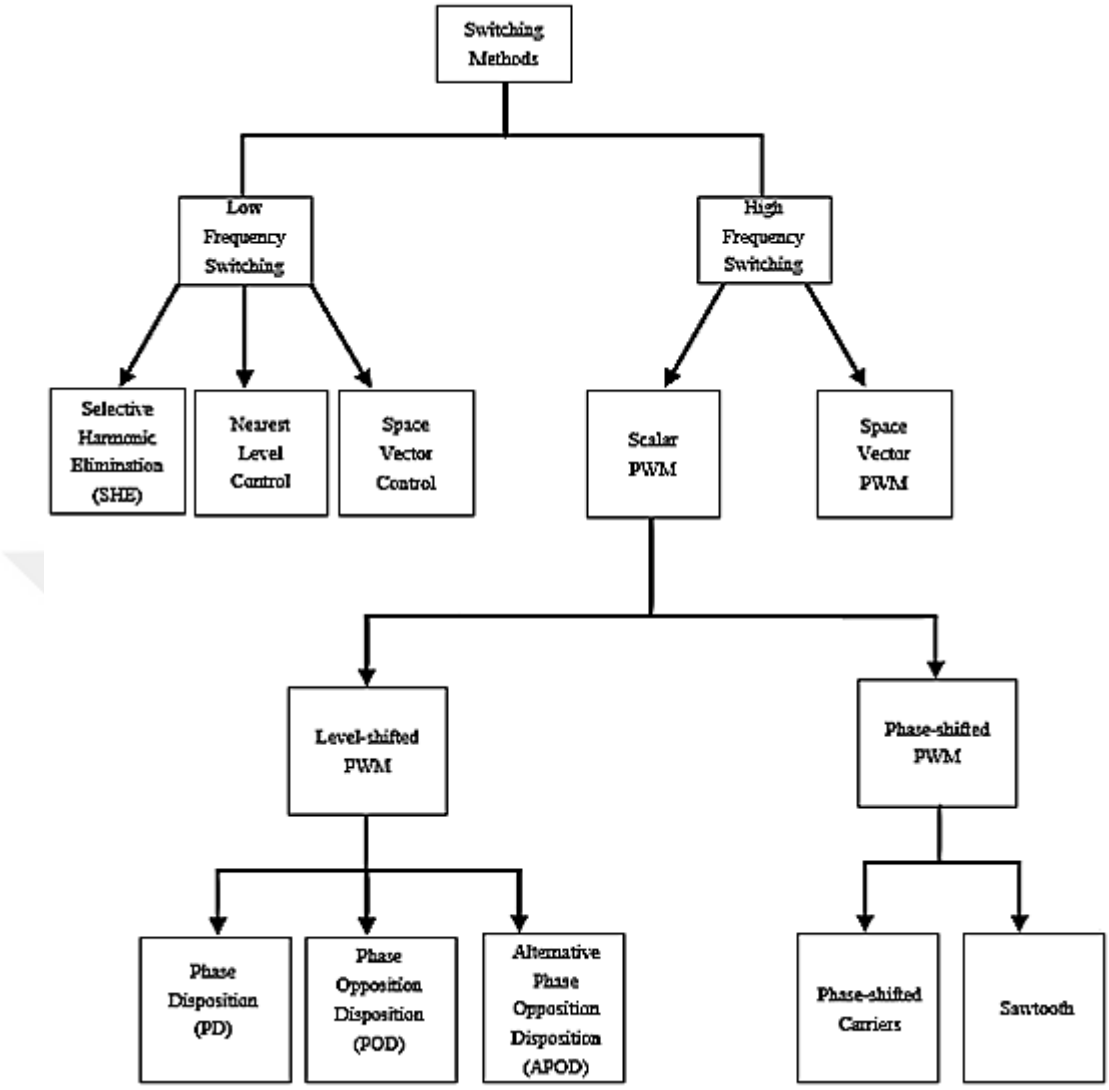


Figure 3.16 Modular multilevel converter switching methods[43]

Depending on the obtained output voltage level, N+1 level and 2N+1 level phase voltages can be discussed.

3.5.1 N+1 Level Switching

Considering N+1 level switching case, at every swiching cycle, the on-state submodules per leg are equal to N, also means number of submodules per arm. In other words, if the number of on-state submodules in upper arm is equal to n_U , lower arm on-state submodules number is found as $n_L = N - n_U$ Level crossings are

determined based on submodule capacitor voltage, V_{dc}/N. Assuming that submodule capacitor voltages are ideal, measured voltage between the inductances of both arms is always zero as seen in Figure 3.17.

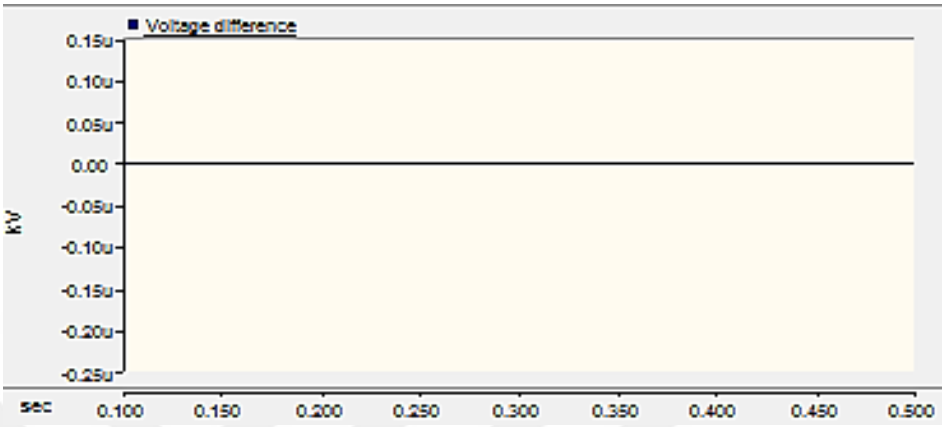


Figure 3.17 Voltage difference between A and B points

N+1 level output phase voltage can also attained in two different ways.

1. Using single voltage reference for both arms
2. Using two varied voltage references for both arms.

When used single voltage reference in a phase leg, output voltage reference is obtained by comparing with sinusoidal voltage reference and carrier triangular carriers. Then, depending on the Equation which is $N = n_U + n_L$, submodules that can be on state are determined [48],[49].

When using two different voltage reference for both arms, each arm voltage level is determined as comparing with carriers respectively. Equation, $N = n_U + n_L$ is valid for both situation.

3.5.2 2N+1 Level Switching

In this circumstances, the number of submodules per leg that are on-state not equal to N every switching cycle that can be N-1, N+1 or N. In the event of N-1 or N+1 level, since differences between the arm voltages, varied voltage can be observed on among upper and lower arm inductance as seen in Figure 3.18. In addition to N-1 or N+1 level, N interval voltage level is observed at the output voltage. Thus, Level transient is determined by Vdc/2N for 2N+1 level switching method which is equal to half of the submodule capacitor voltage.

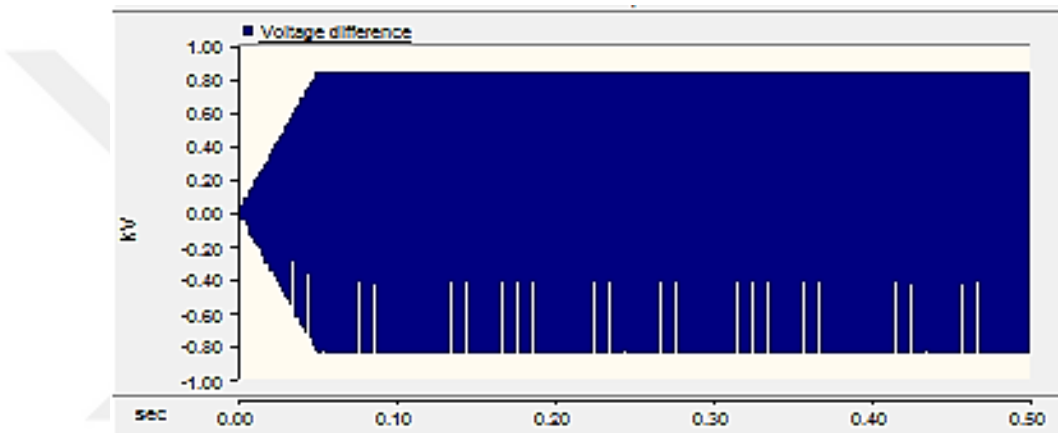


Figure 3.18 Voltage difference between the A and B points

3.5.3 Level-shifted PWM Methods

In level-shifted PWM method, N identical carriers with amplitude of submodule capacitor voltage namely, V_{dc}/N are stacked up on top of each other ranging from 0 to V_{dc} band. The number of submodules in each arm is also equal to the carrier waveforms.

In level-shifted PWM case, equivalent switching frequency for MMC is equal to the carrier frequency, as illustrated in Equation (3.21) and also level-shifted carriers are shown in Figure (3.19).

$$f_{c\_eq} = f_c \tag{3.21}$$

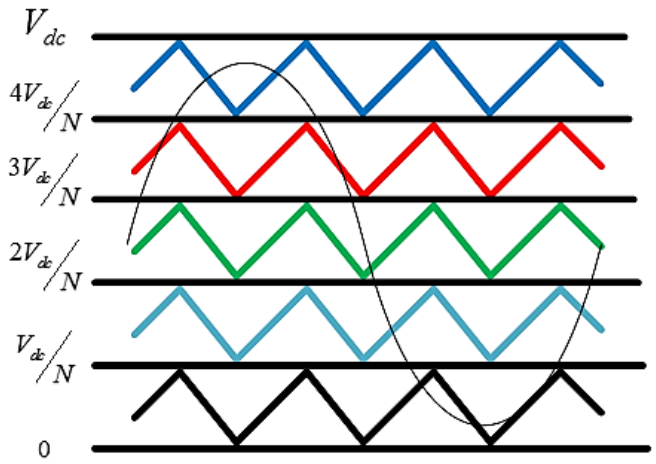


Figure 3.19 Carrier sets for level-shifted PWM method in 6 level MMC

That can be given two example to obtain N+1 level output voltage for level-shifted PWM methods. First one is that using single sinusoidal voltage reference in a phase leg. Additionally, carriers are set ranging from $-V_{dc}/2$ to $V_{dc}/2$ and also N triangular carriers which have the same phase difference are used for this modulation case. Carrier sets are shown in Figure 3.20 [50].

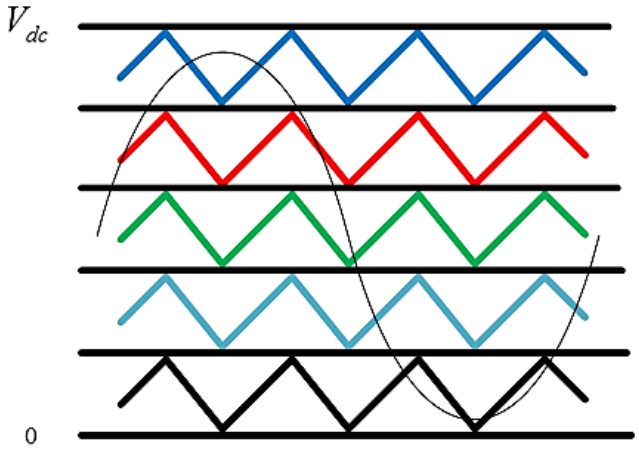


Figure 3.20 N+1 level modulation using single carrier set and sinusoidal voltage reference in 6 level MMC

Taken into account second modulation case for level-shifted methods, two different carrier sets and sinusoidal voltage references are used for both arms to obtain the output phase voltage in N+1 level as illustrated in Figure 3.21 [46]. Sinusoidal voltage reference which belongs to the upper arm is compared with N identical carriers with amplitude of submodule capacitor voltage, V_{dc}/N, ranging from 0 to V_{dc} [46]. Other sinusoidal voltage reference which relates to the lower arm is compared with carrier set having a phase difference of 180 degrees relative to the first carrier set ranging from 0 to V_{dc}.

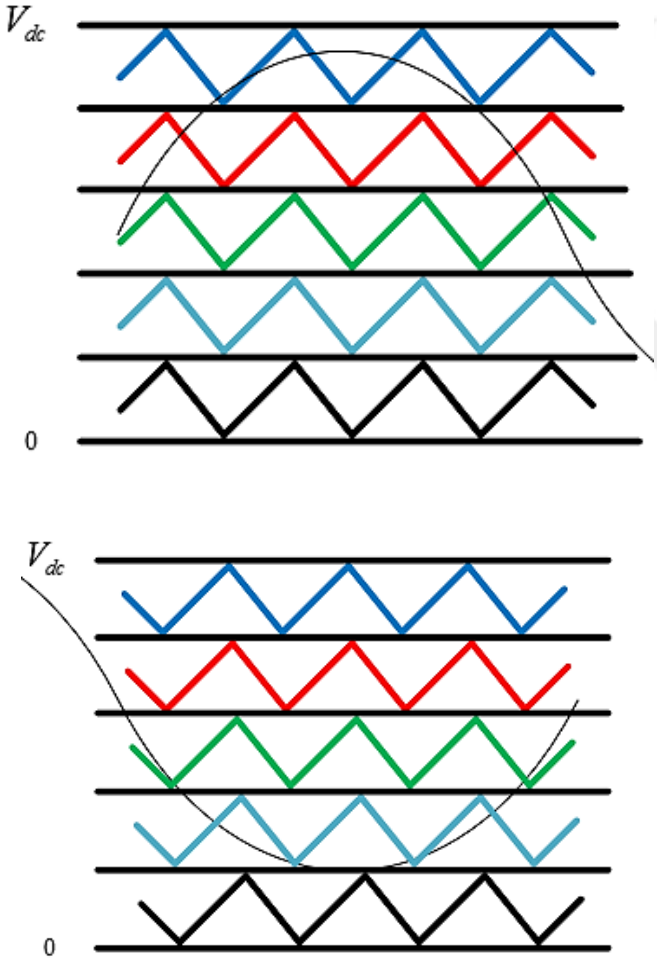


Figure 3.21 N+1 level modulation using different carrier sets and different sinusoidal voltage references for upper and lower arm in 6 level MMC [48]

There are different types of level-shifted methods formed according to the phase difference between carrier waveforms. The methods that can be classified as Phase disposition (PD), phase opposition disposition (POD) and the last one is alternative phase opposition disposition (APOD). First one is PD PWM method is illustrated below.

3.5.3.1 Phase Disposition (PD) Method

All of the carrier waveforms used in a carrier set have the same frequency and also identical phase disposition.

In order to get N+1 voltage level, used carrier sets for upper and lower arm have 180 degree phase difference between each other. N+1 level PD-PWM in a phase leg with N=5 is demonstrated in Figure 3.22.

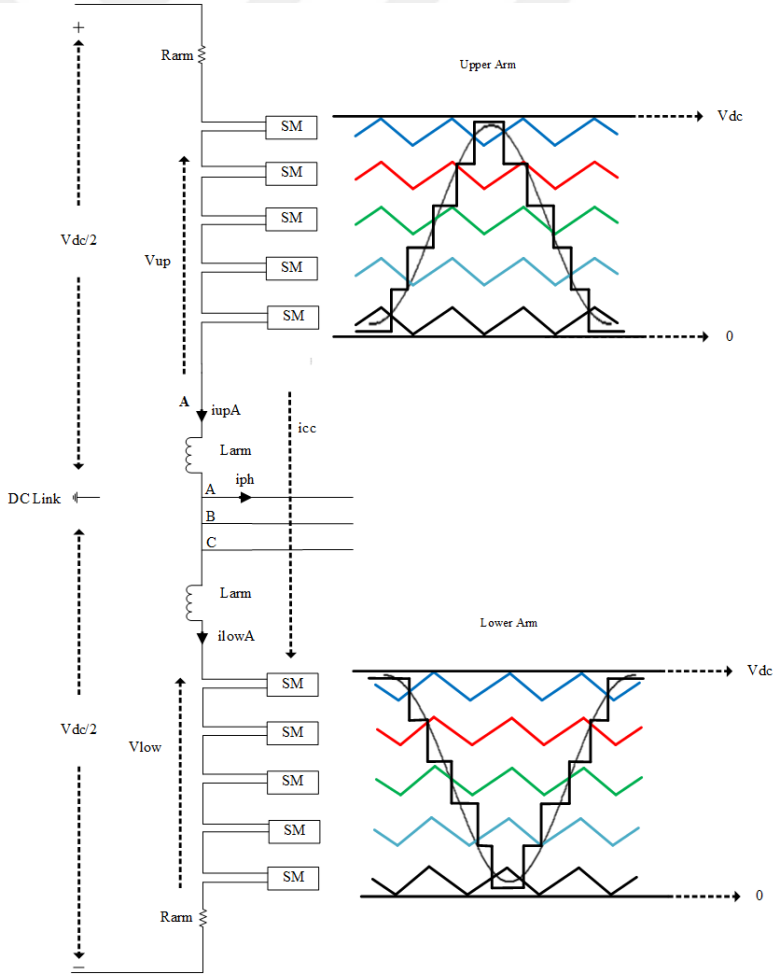


Figure 3.22 N+1 level PD-PWM method in a phase leg in 6 level MMC

Considering 2N+1 level PD-PWM method, submodules in both arms are switched with the carriers that have no phase difference between each other. 2N+1 level PD-PWM in a phase leg with N=5 is illustrated in Figure 3.23.

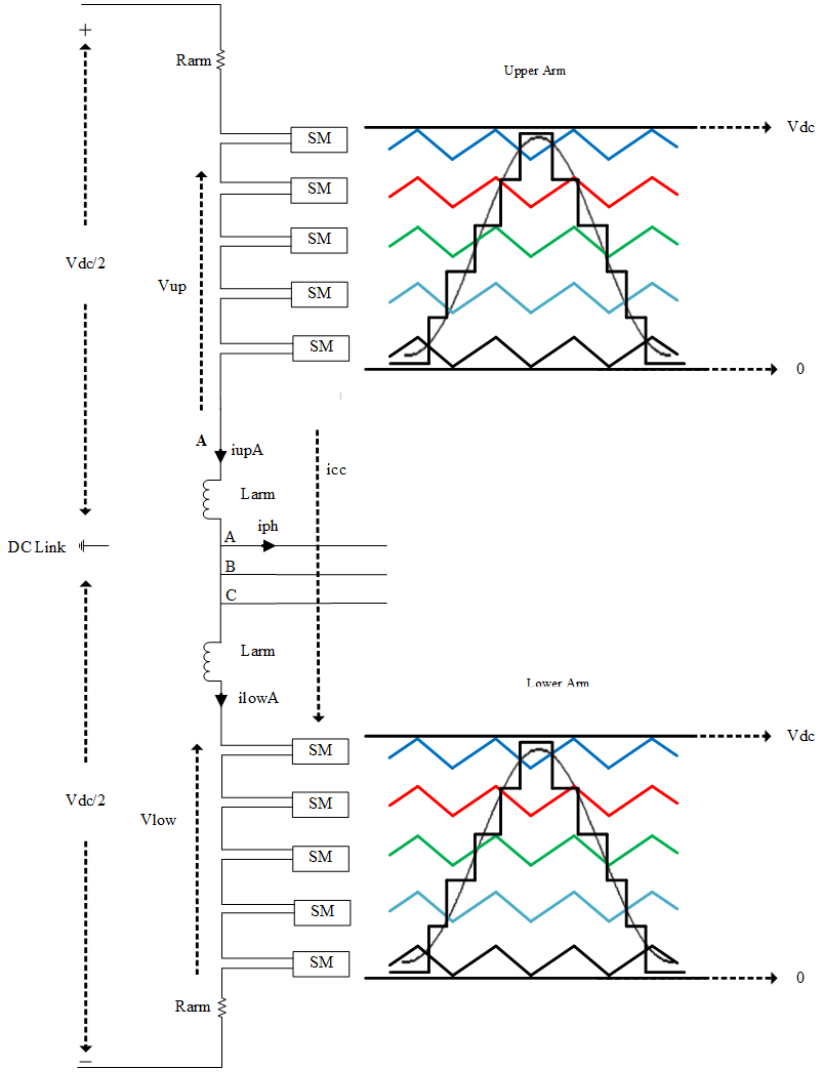


Figure 3.23 2N+1 level PD-PWM method in a phase leg in 6 level MMC

3.5.3.2 Phase Opposition Disposition (POD) PWM Method

The other level-shifted technique is phase opposition disposition PWM method which is similar to PD-PWM. However, the lower carrier waveforms have 180 degrees out of phase. Thus; N+1 level and 2N+1 level switching can be implemented to the MMC for POD method depending on the phase difference between the upper and lower carrier waveforms. In order to get N+1 voltage level, used carrier sets for upper and lower arm have 180 degree phase difference between each other as shown in Figure 3.24. In 2N+1 level switching, lower arm has no phase difference with regard to upper arm as illustrated in Figure 3.25.

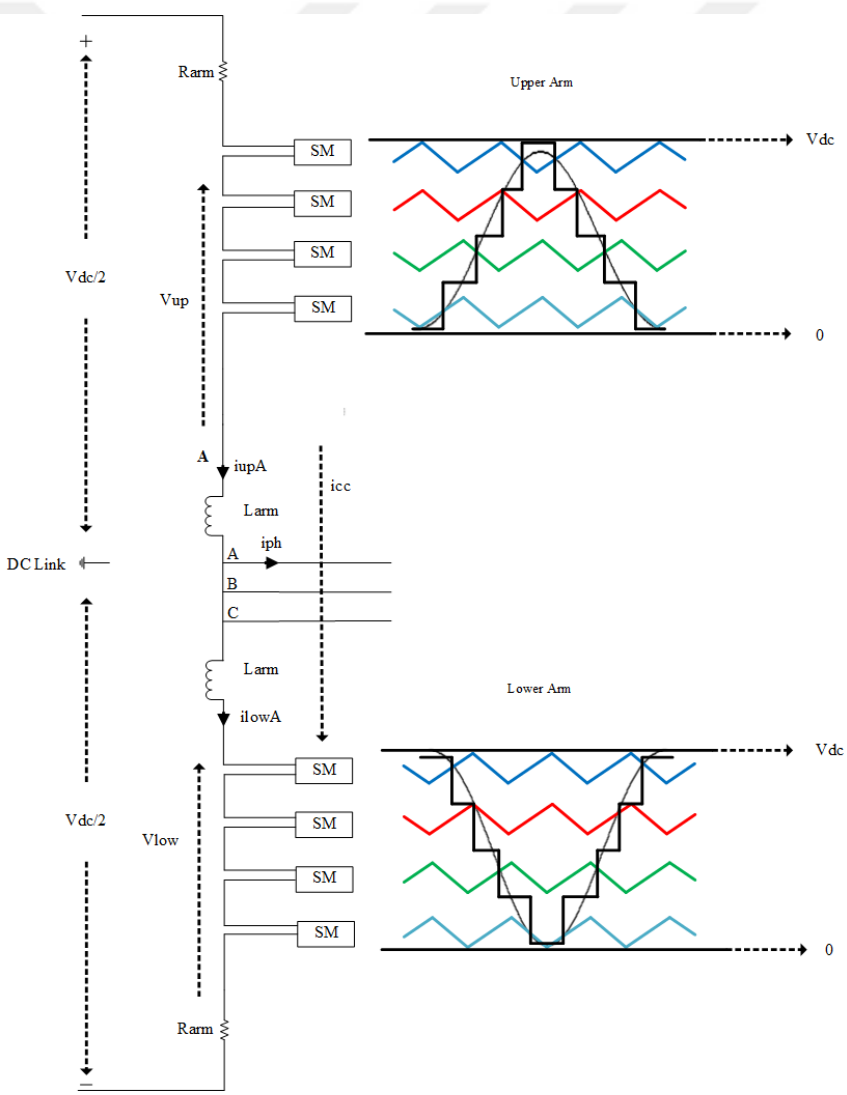


Figure 3.24 N+1 level POD-PWM method in 5 level MMC

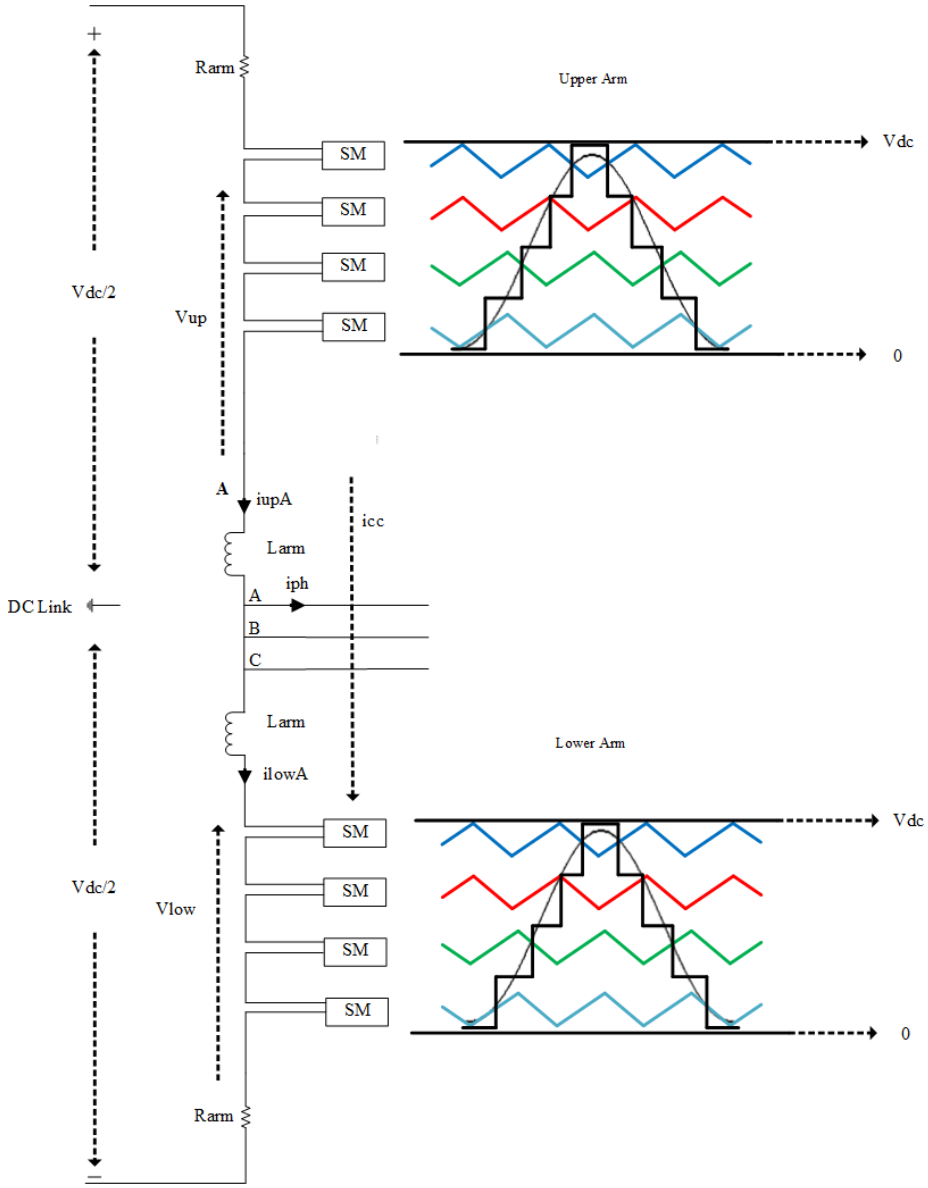


Figure 3.25 2N+1 level POD-PWM method in 5 level MMC

3.5.3.3 Alternative Phase Opposition Disposition (APOD) PWM Method

In Alternative Phase Opposition Disposition technique, every other carrier waveform has 180 degrees out of phase with their adjacent. Therefore; N+1 level and 2N+1 level switching can be applied to the MMC for APOD method depending on the phase difference between both carrier waveforms. In order to obtain N+1 voltage level, used carrier sets for upper and lower arm have 180 degrees phase difference

between each other as shown in Figure 3.26. In 2N+1 level switching, lower arm has no phase difference in comparison with upper arm as demonstrated in Figure 3.27.

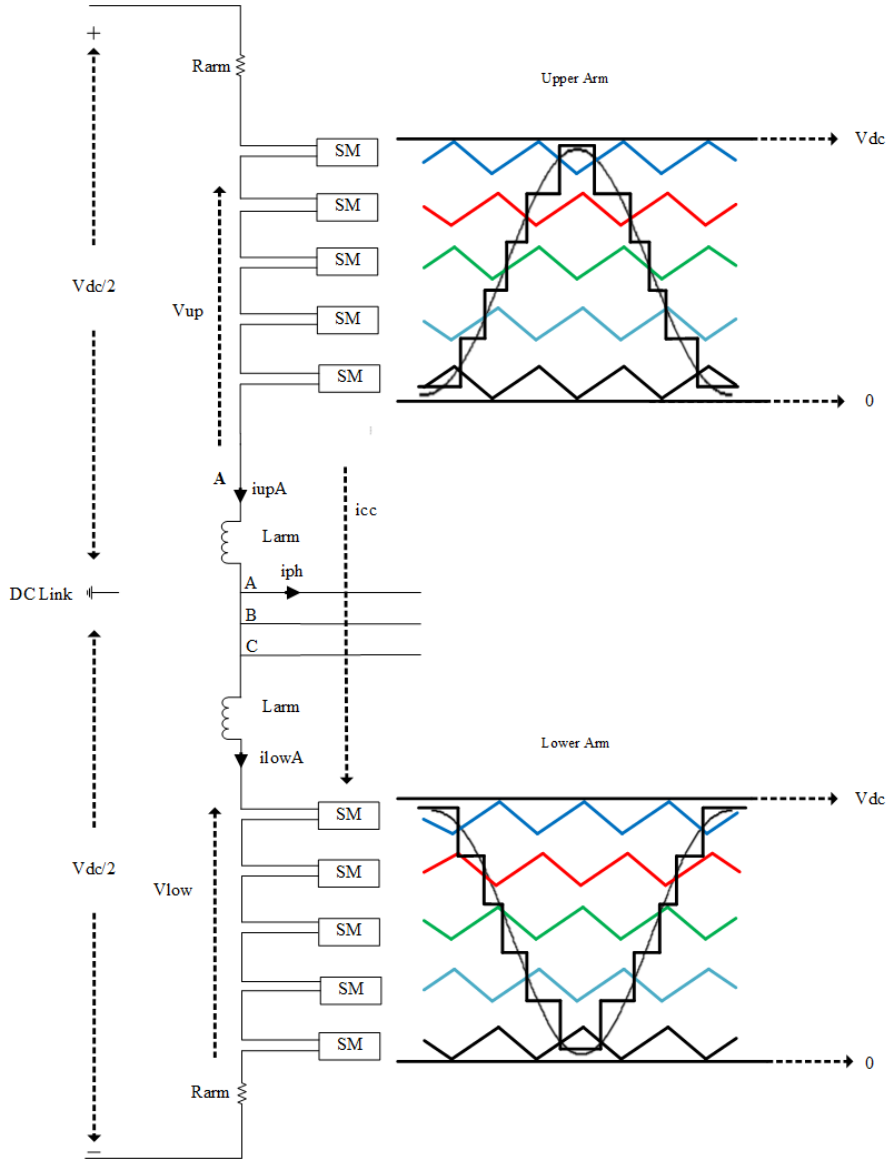


Figure 3.26 N+1 level APOD-PWM method in 6 level MMC

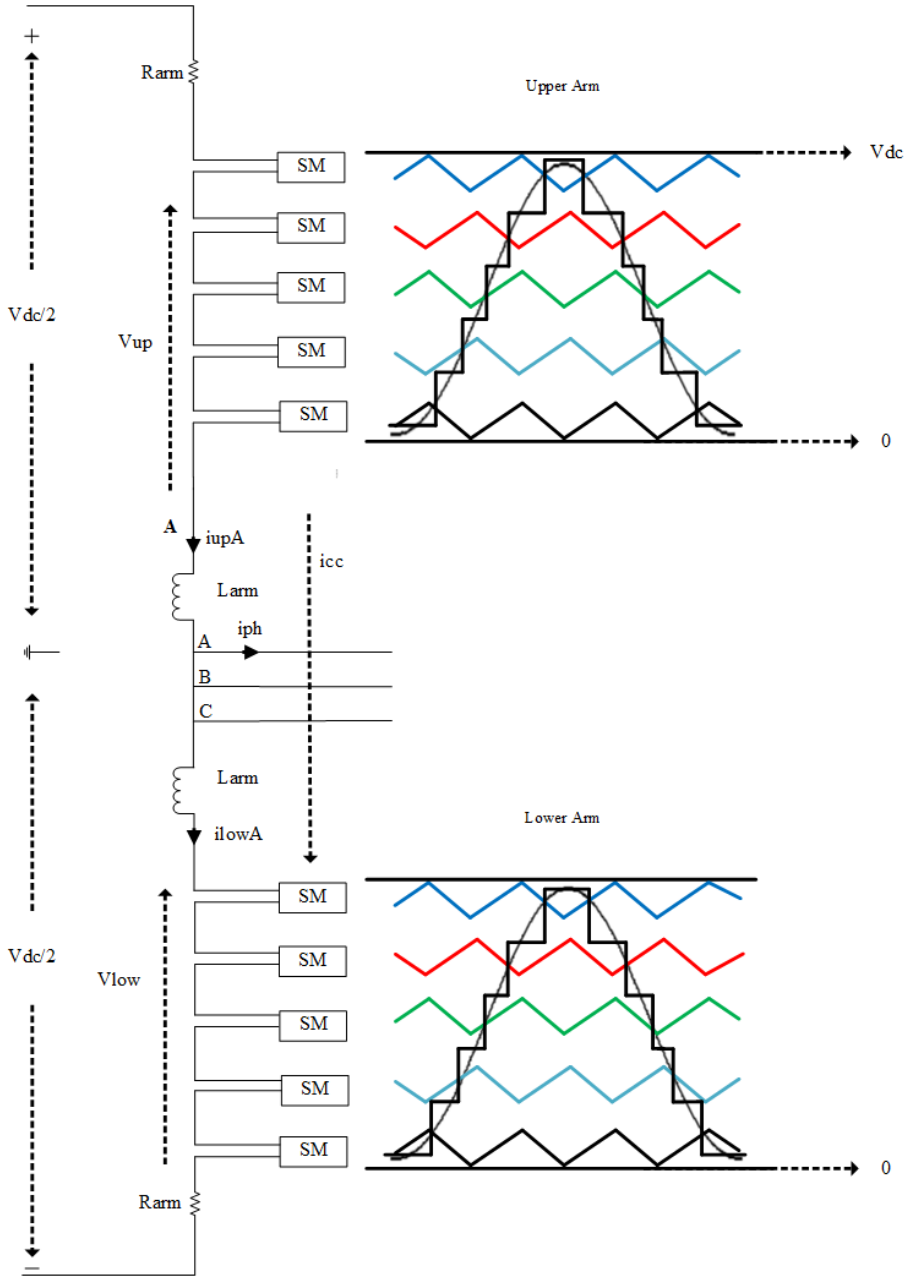


Figure 3.27 2N+1 level APOD-PWM method in 6 level MMC

3.5.4 Phase-shifted PWM Method

In Phase-shifted PWM method, N identical triangular carriers are arranged with an angle of $2\pi/N$, between each other as illustrated in Figure 3.28. Each carrier has peak-to-peak amplitude of V_{dc} and carrier frequency of f_c.

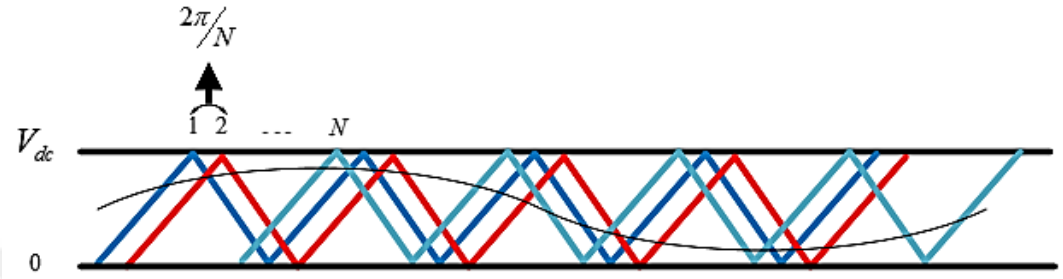


Figure 3.28 Phase-shifted carriers

In this modulation technique, one carrier for each submodule is used in the converter arm. The phase between both arms carrier sets are determined as in Equations (3.22) and (3.23), respectively.

$$\theta_{up}(i) = \frac{2\pi}{N}(i-1) + \theta \quad \textbf{(3.22)}$$

$$\theta_{low}(i) = \frac{2\pi}{N}(i-1) \quad \textbf{(3.23)}$$

In these Equations, i means the number of carrier and theta means that the phase difference between both arms carrier sets. Depending on theta, harmonic succeded of the MMC can be changed. N+1 and 2N+1 level switching for phase-shifted PWM can be obtained with adjusting theta [50]. Theta can be changed ranging from 0 to π/N degree. Depending on N being even or odd, It is possible to acquire N+1 or 2N+1 level output phase voltage level. In N+1 level phase-shifted PWM method, if N is odd, theta should be π/N as shown in Figure 3.29.

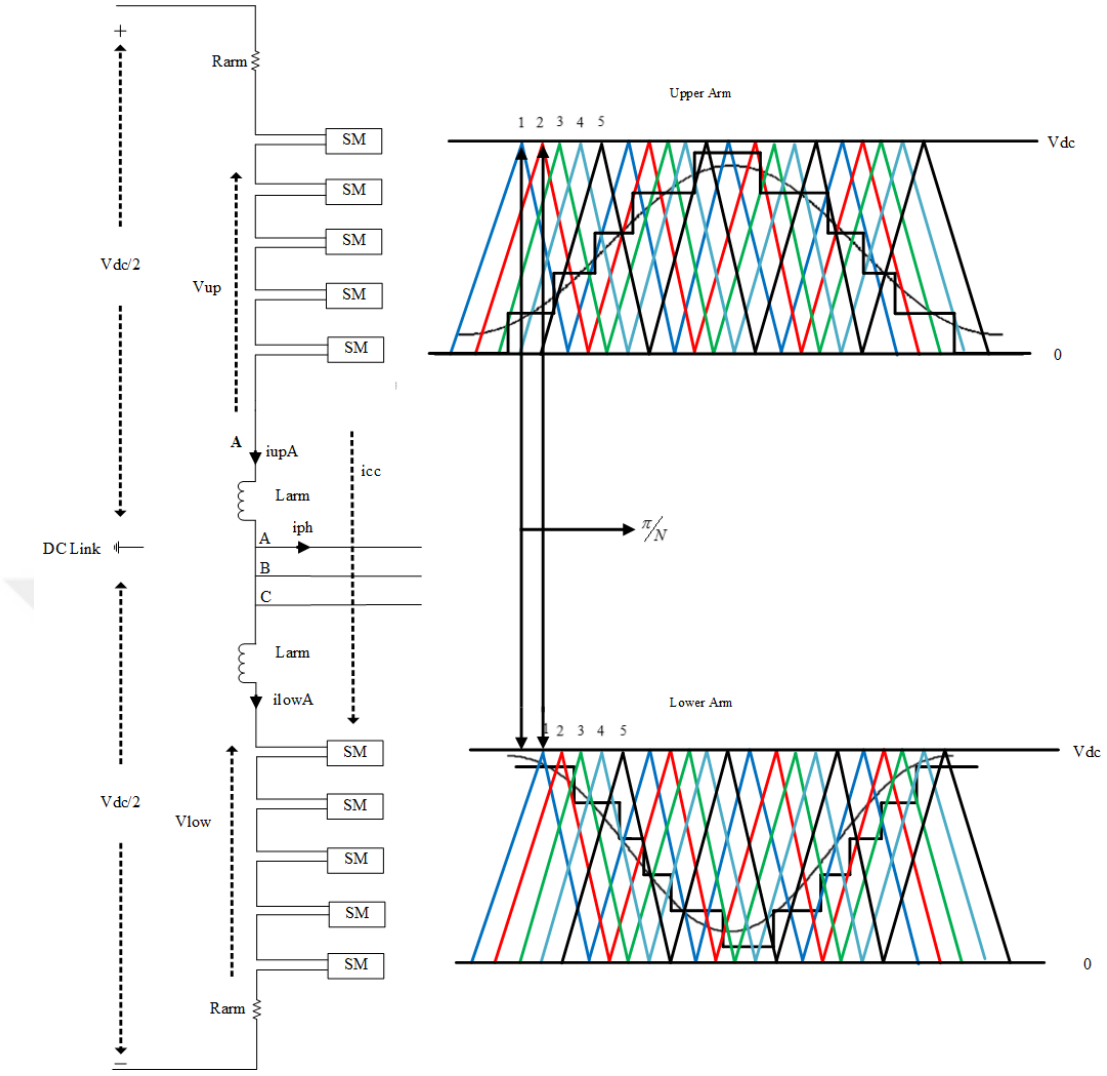


Figure 3.29 PS carrier sets for N+1 level switching when N is odd

In other words, If submodule number per arm, *N*, can even, theta should be 0 as illustrated in Figure 3.30.

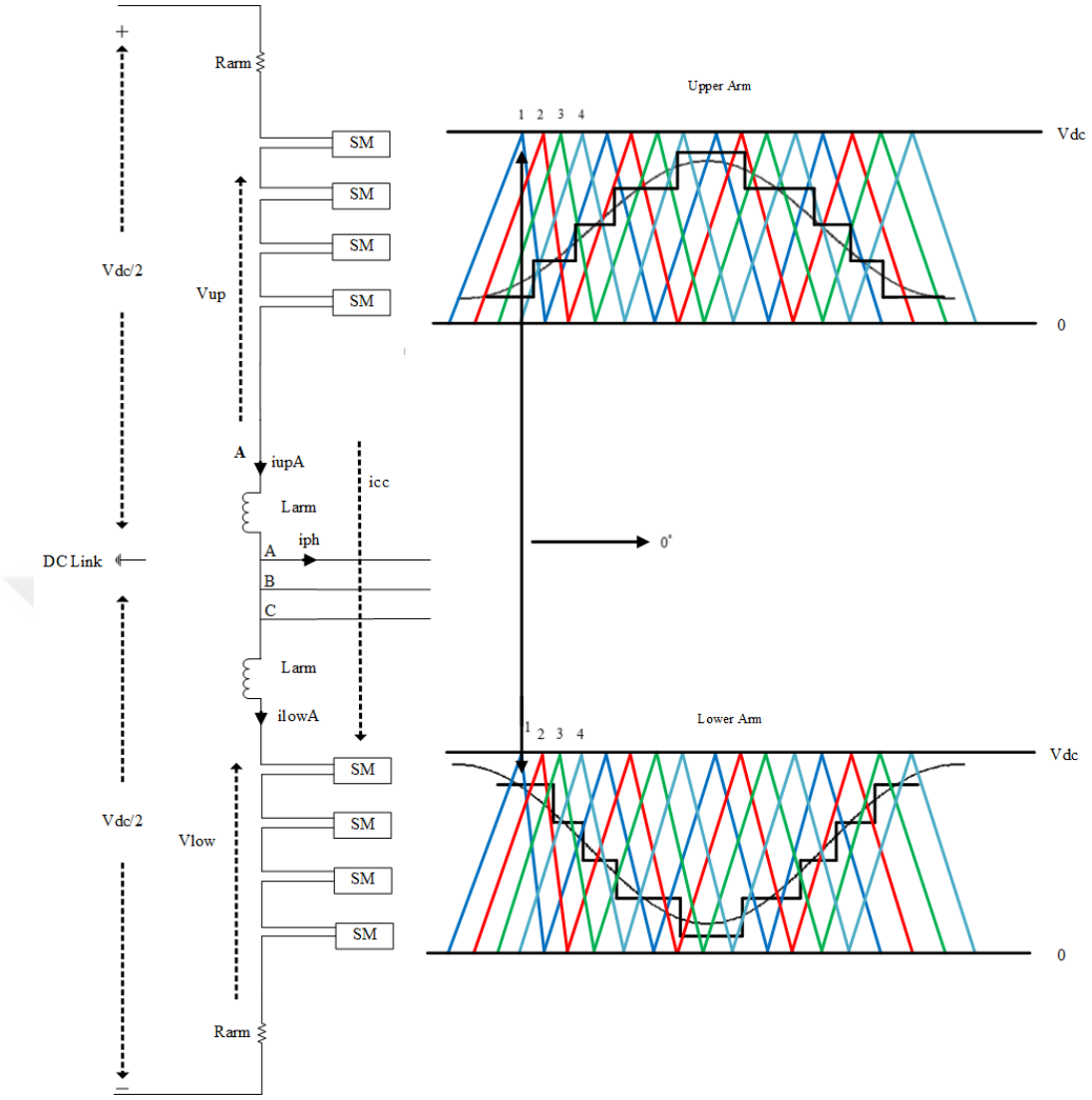


Figure 3.30 PS carrier sets for N+1 level switching when N is even

In N+1 level switching, converter equivalent switching frequency, $fcsw, eq$, is equal to the number of carriers times the frequency of the triangular carriers, as shown in Equation (3.24).

$$fcsw, eq = Nfc \tag{3.24}$$

In 2N+1 level phase-shifted PWM method, if N is odd, theta should be 0 as shown in Figure 3.31. However, If submodule number per arm, *N*, is even, theta should be π/N as illustrated in Figure 3.32.

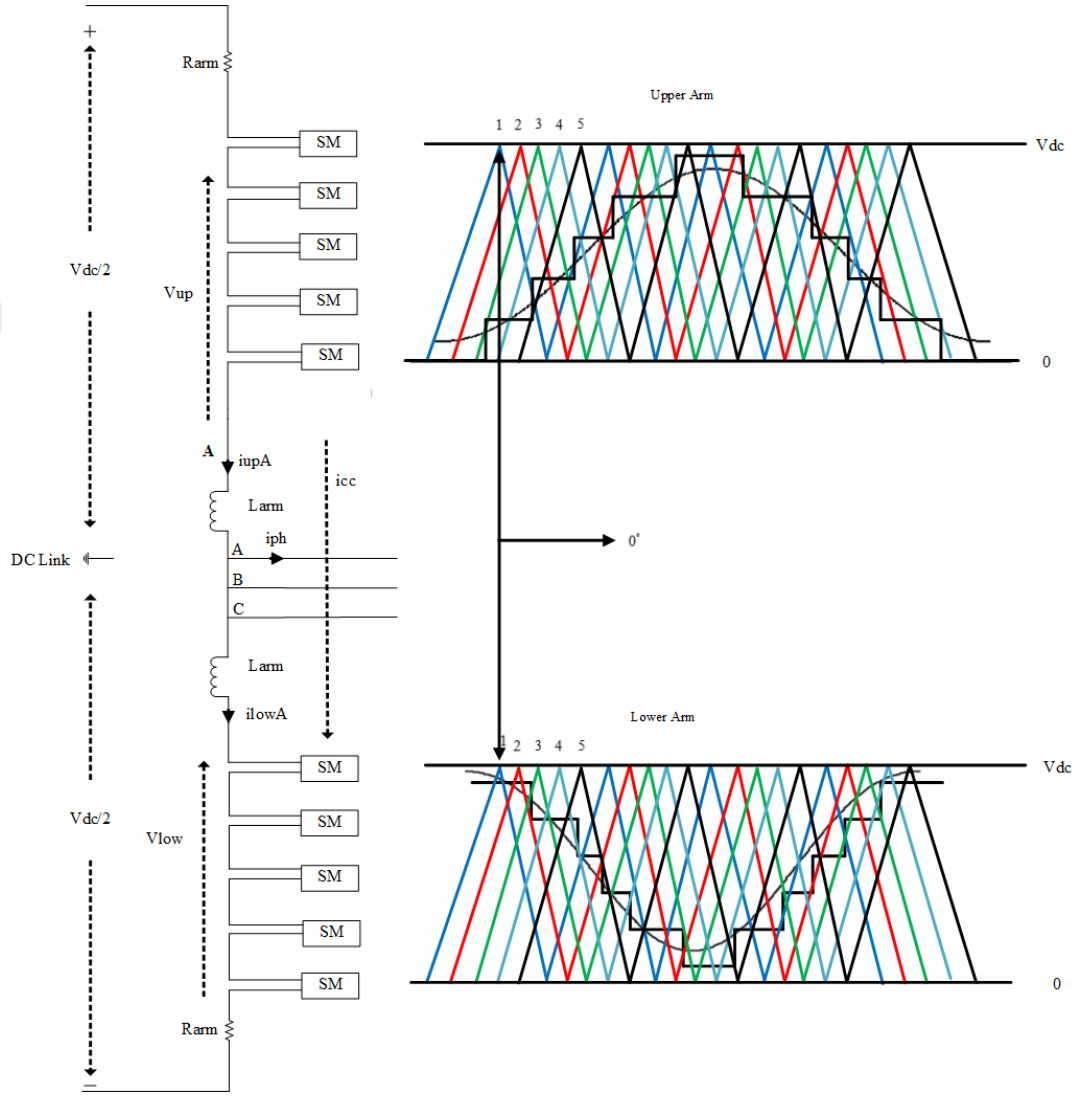


Figure 3.31 PS carrier sets for 2N+1 level switching when N is odd

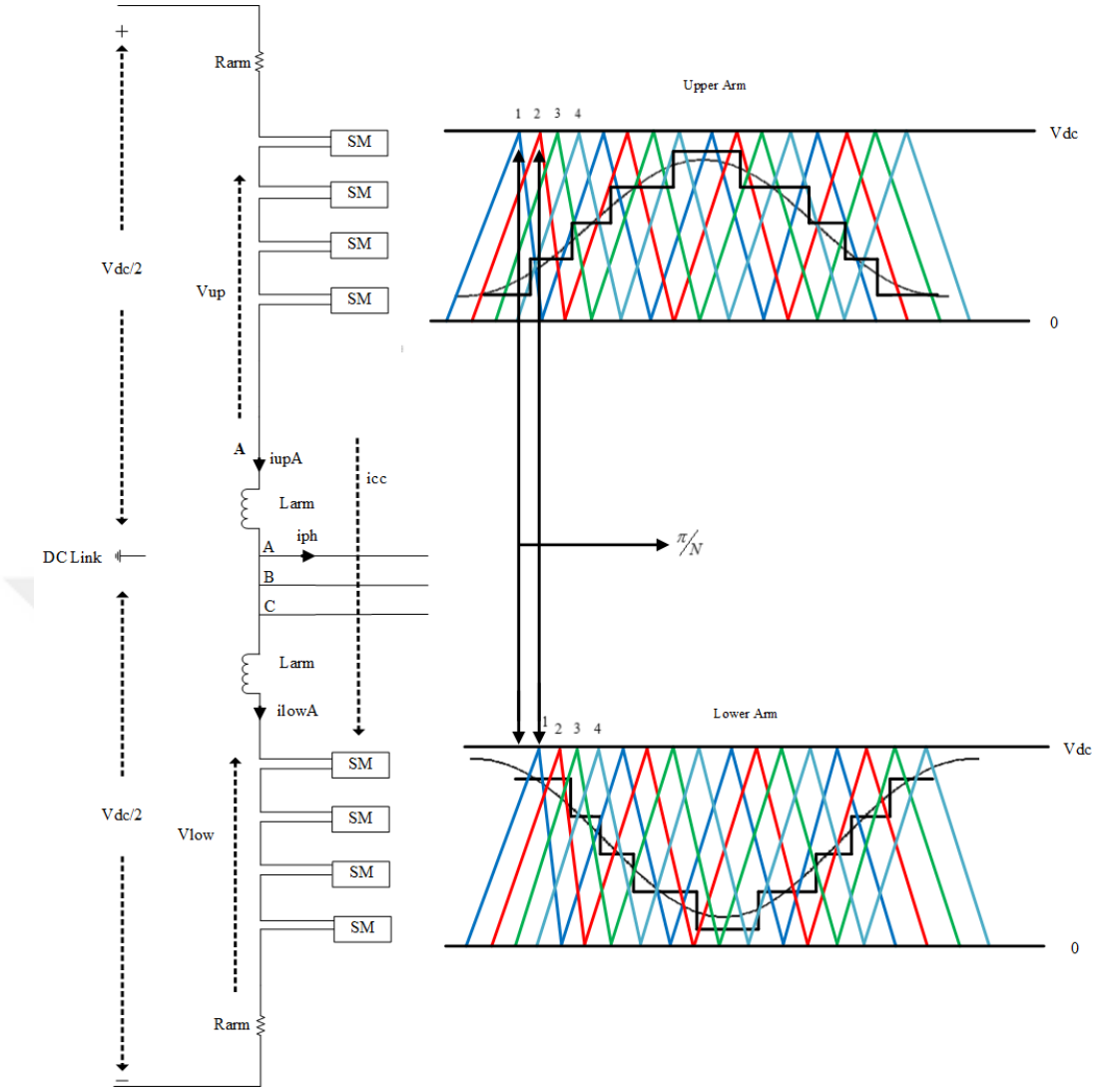


Figure 3.32 PS carrier sets for 2N+1 level switching when N is even

In 2N+1 level switching, converter equivalent switching frequency, $fcsw,eq$, is equal to twice the number of carriers times the frequency of the triangular carriers, as shown in Equation (3.25).

$$fcsw,eq = 2Nfc \tag{3.25}$$

3.5.5 Selective Harmonic Elimination Method

One of the members of the low frequency switching method is the selective harmonic elimination (SHE) method related to the harmonic elimination theory [51], [52]. The switching angles are pre-calculated to adjust the desired amplitude of basic component and eliminate the predominant low frequency harmonics in the output voltage [53]. Output voltage waveform for a three level converter whose switching angles are determined by selective harmonic elimination method is illustrated in Figure 3.33 [67].

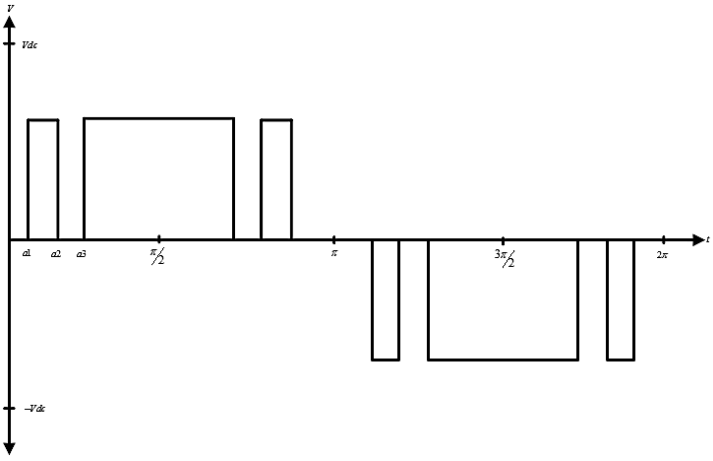


Figure 3.33 Output voltage waveform for a three level converter

3.5.6 Space Vector Control Method

Space vector control method can be applied to MMC similarly as in multilevel converter methods. In this method, the submodule sets related to both arms of the MMC are considered like separate converters.

In this method, for each switching cycle, vector is occured with in complex space vector. Desired reference voltage is obtained by selecting vectors among the complex space vectors and applying a switching period in certain time. That can be shown in Equations (3.26) and (3.27).

$$V_1 t_1 + V_2 t_2 + V_3 t_3 = V^* T_S \quad \textbf{(3.26)}$$

$$t_1 + t_2 + t_3 = T_S \quad \textbf{(3.27)}$$

In order to minimize the harmonics, three vectors are selected which are the closest to the reference vector. Then, duty cycle ratio is determined. In the final stage, among the redundant vectors which have the lowest switching number are selected and applied respectively.

Considering its advantages, like easy digital implementation and the possibility of optimizing the switching sequences, it can be remarkable modulation technique for multilevel converters. Nevertheless, the complexities of the algorithm for the calculation of the state vectors and computational costs with the number of levels increased are the drawback side of the space vector control [41] Thus, it can not be preferred in this dissertation.

3.5.7 Nearest Level Control Method

Nearest level control method has been suggested in [54], where the output voltage level closest to desired voltage waveform is considered. Comparing to SHE method, NLC method has easy implementation, less computational difficulty and also lower switching frequency [26]. Thus, low THD value is achieved at output voltage. Generally, this modulation technique can be preferred at least 10 submodules in the converter [55, 56].

Both the reference voltage waveform and output voltage level which is available are compared to each other and as a result of that sampled waveform is obtained. In here, the nearest output voltage level is formed as in Equation (3.28). Another step is that how many numbers of SMs shall be switched on by means of the round function,

$$n_{nl} = \frac{1}{V_c} round(V_{ref}) \quad \textbf{(3.28)}$$

Waveform synthesis and control block scheme of the method are seen in Figure 3.34 and Figure 3.35, respectively [68].

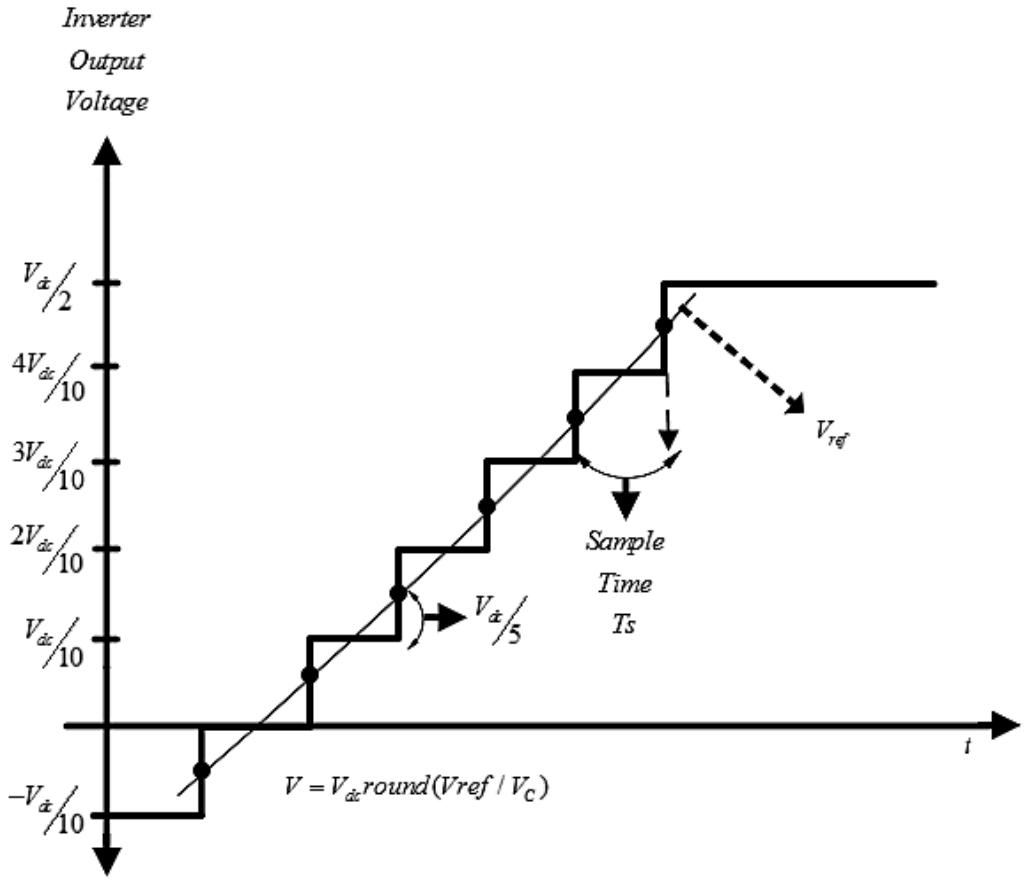


Figure 3.34 Waveform synthesis of the method

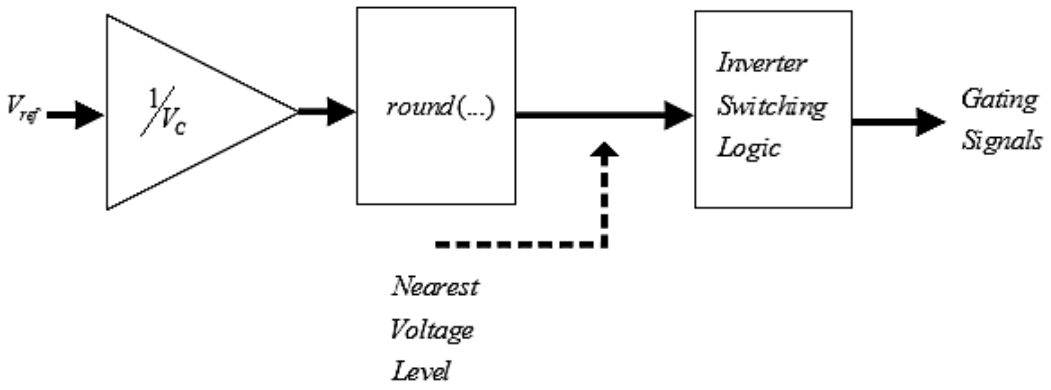


Figure 3.35 Control block scheme

3.6 Analysis and Comparison of the Switching Methods

3.6.1 Performance Analysis of PWM Methods

This section gives an assessment of performance analysis in terms of comparing PWM methods based on output line-to-line voltages and output currents waveform quality in both N+1 level and 2N+1 level modulation techniques. In comparing, carrier based modulation techniques in high frequency switching method which are grouped as two categories as PS-PWM and LS-PWM are discussed. Moreover to this, nearest level modulation technique which belongs to low frequency switching method is also included in performance analysis of modulation methods. The assessment is done without using any control and submodule capacitor voltage balancing algorithm. Thus, it is intended to discuss with their most basic form of modulation techniques. In order to evaluate Scalar PWM methods in a fair switching, equivalent switching frequency in a phase leg is considered. Thus, modulation amplitude and modulation frequency values are taken according to Equations (3.29) and (3.30). In order to analyze individual harmonic distortion (%) of the line-to-line voltage, harmonics are handled from first to127th harmonic due to 2N+1 level modulation frequency value also equivalent to 80 for level shifted PWM methods.

In case of level increasement, performance analysis of modulation methods is evaluated. Thus, both 5 level and 6 level MMC is handled as shown in Figure 3.36 and Figure 3.37. Initially, 5 level MMC with four submodules per arm is analyzed with regard to output line-line voltage and output current waveform quality. Then, depending on increasing of the submodules per arm, N=5, THD analysis of the line-to-line output voltage and output current characteristics are discussed for both N+1 and 2N+1 level modulation techniques.

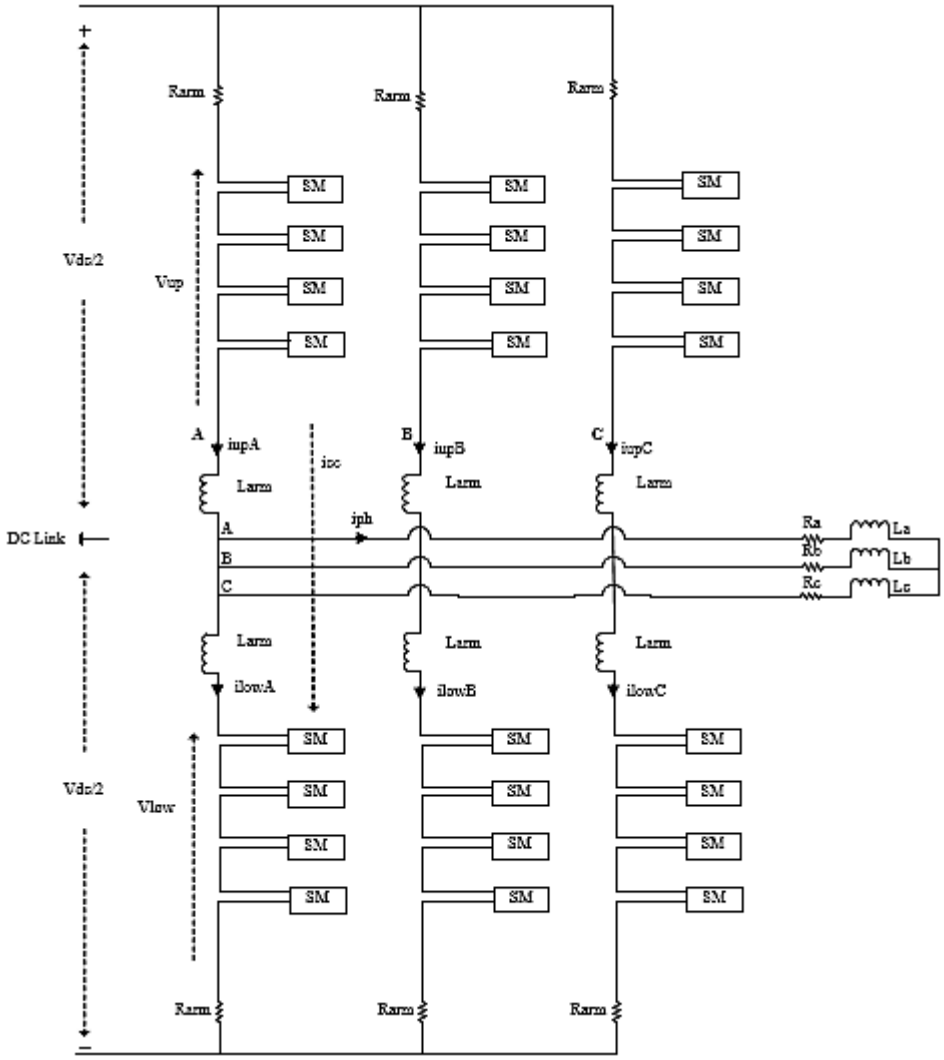


Figure 3.36 5 level Modular Multilevel Converter

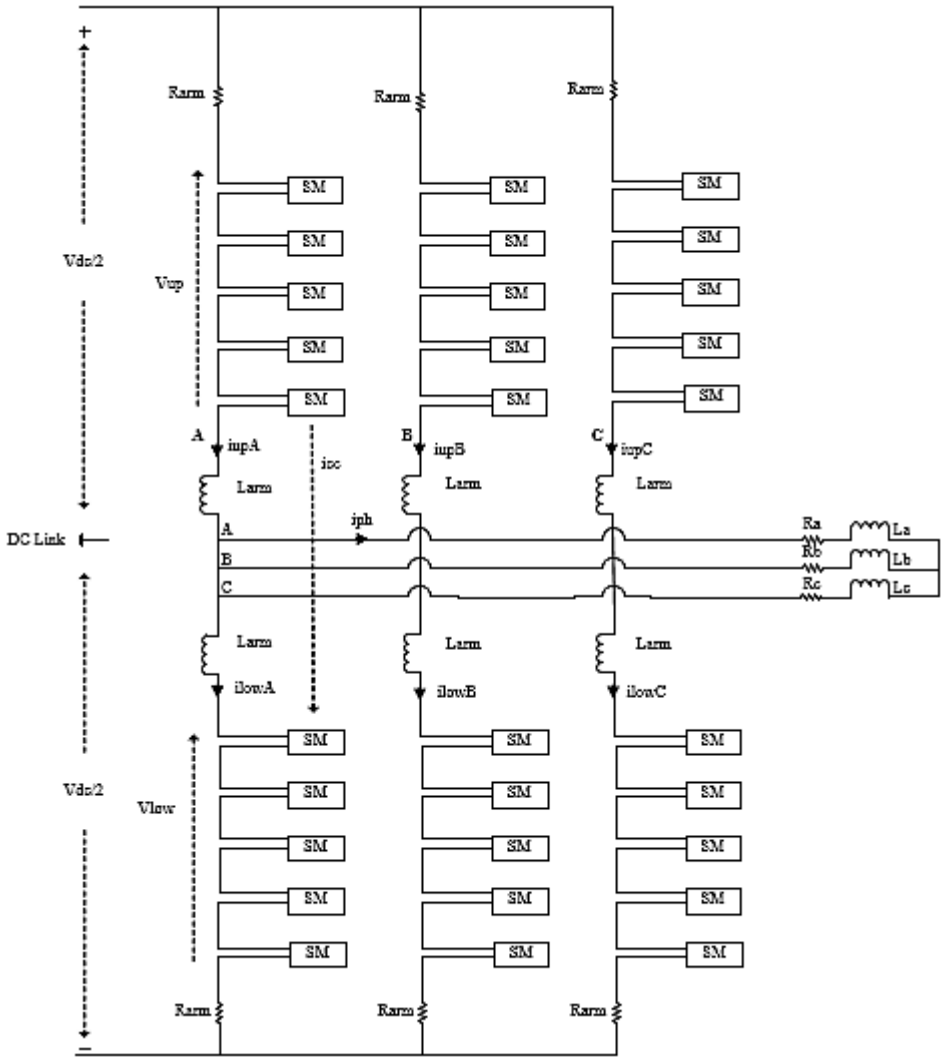


Figure 3.37 6 level Modular Multilevel Converter

3.6.1.1 Analysis of N+1 Level Line-to-line Voltage and Output Current in 5 Level MMC

In Figure 3.38 to Figure 3.42, output line voltages of N+1 level modulation methods are given. In Figure 3.43 to Figure 3.47, output line-to-line voltages of N+1 level modulation techniques are given. In here, unipolar switching occurs for PD-PWM; whereas POD, APOD and PS-PWM methods represent bipolar switching in N+1 level line-to-line voltage analysis. Thus, FFT analysis is done as shown in Figure 3.48 to Figure 3.52. According to FFT analysis, dominant harmonics for level shifted PWM methods are centered almost their carrier frequency or switching

frequency. Although, that carrier frequency of PS-PWM method is different than other level shifted methods, dominant harmonics are observed about its switching frequency as in level shifted PWM methods. Due to unipolar switching case in PD-PWM, individual harmonic distortion (%) of the line-to-line voltage represents the better condition than other modulation techniques as shown in Figure 3.53 to Figure 3.57. Additionally, Total Harmonic Distortion (%) values are given in Table 3.2. Moreover, output current waveforms are also investigated. PD-PWM technique gives the best result in terms of performance analysis among the modulation methods as well and is seen in Figure 3.58 to Figure 3.62.

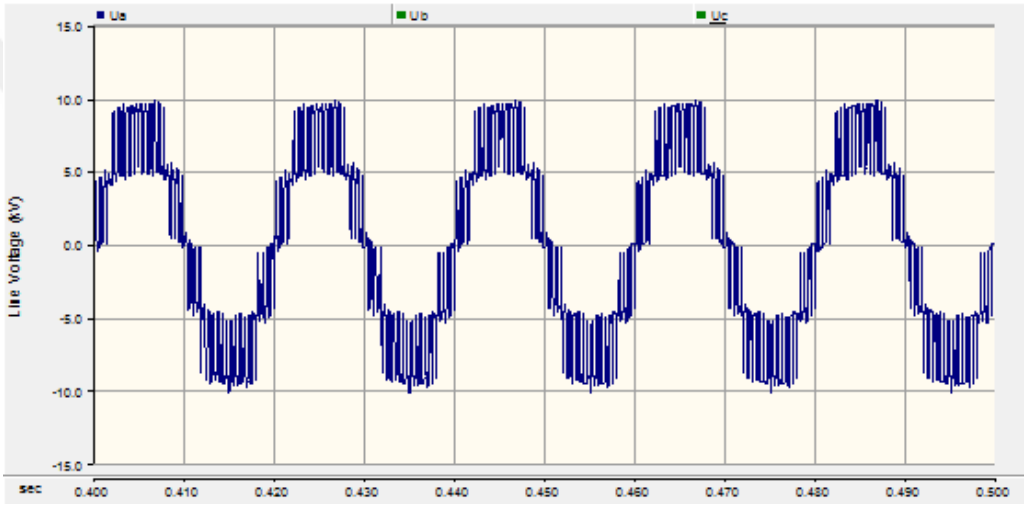


Figure 3.38 Output line voltage of N+1 level PD-PWM

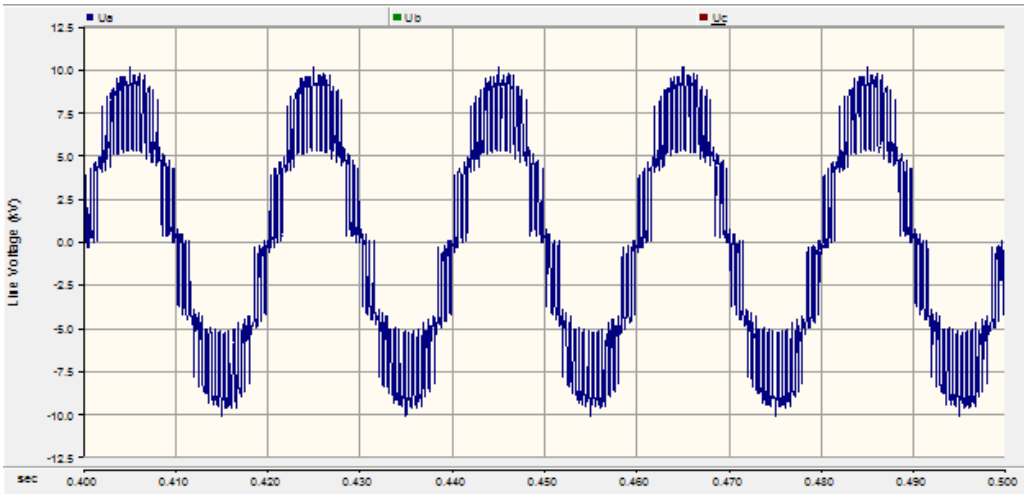


Figure 3.39 Output line voltage of N+1 level POD-PWM

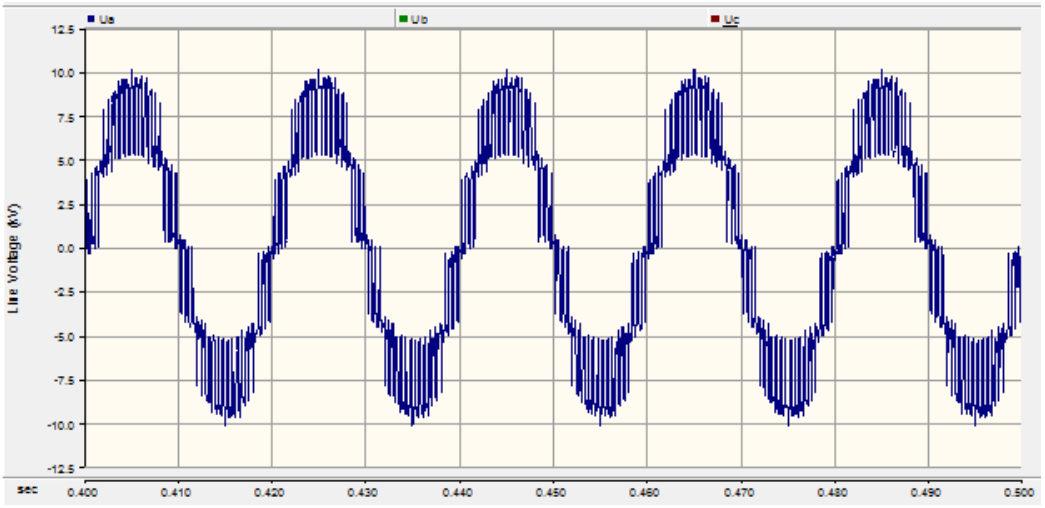


Figure 3.40 Output line voltage of N+1 level APOD-PWM

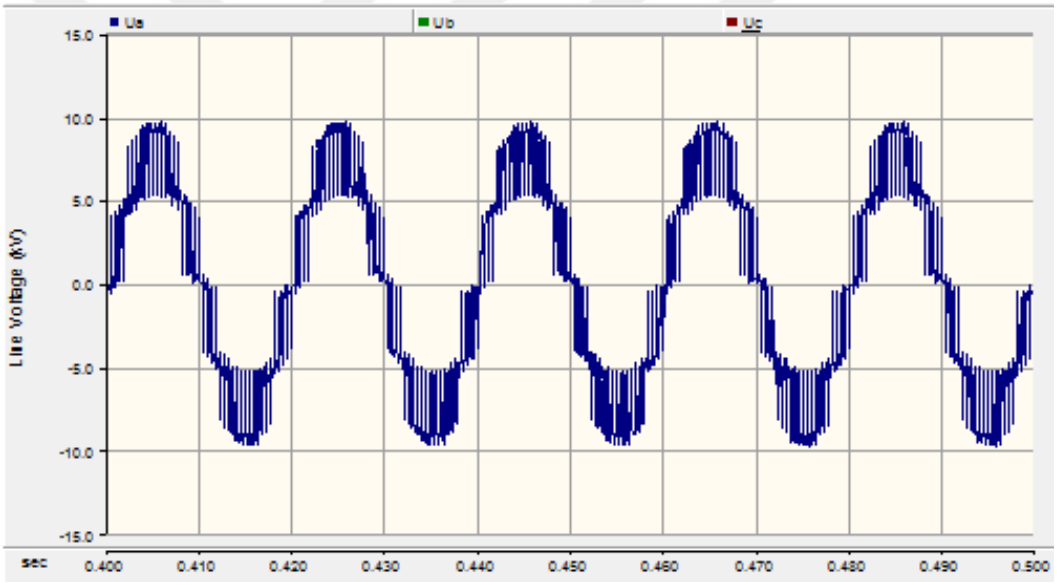


Figure 3.41 Output line voltage of N+1 level PS-PWM

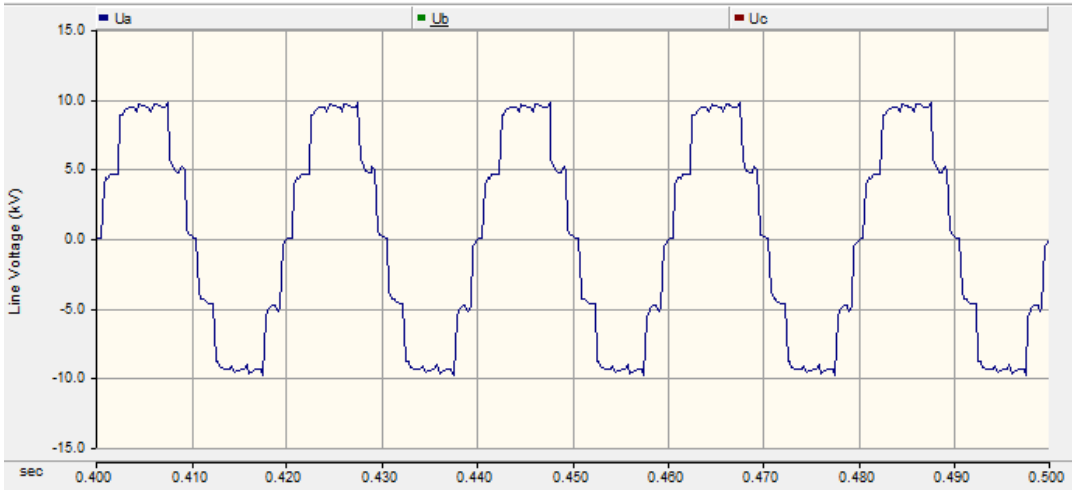


Figure 3.42 Output line voltage of N+1 level NLC

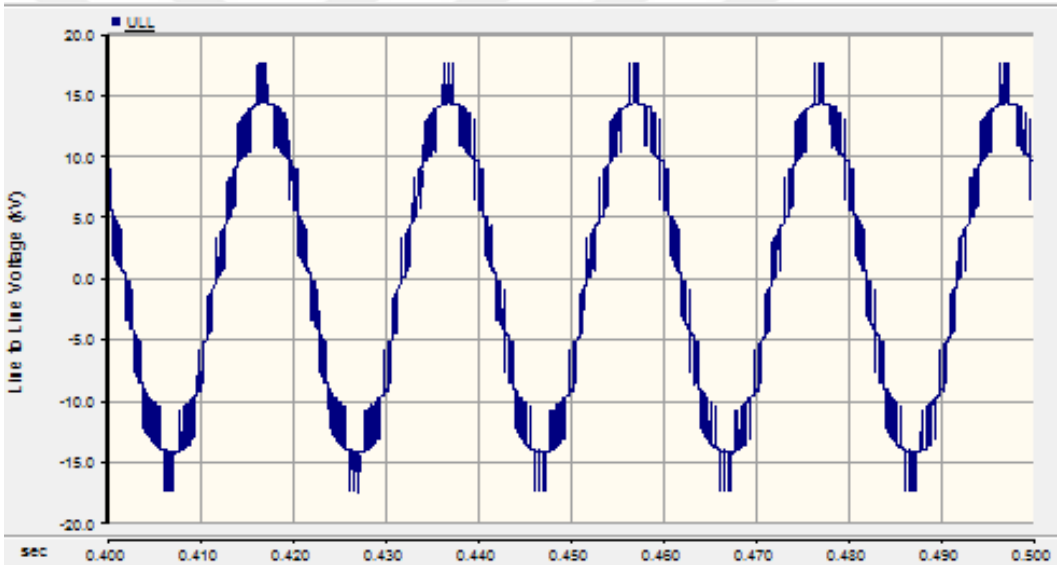


Figure 3.43 Output line-to-line voltage of N+1 level PD-PWM

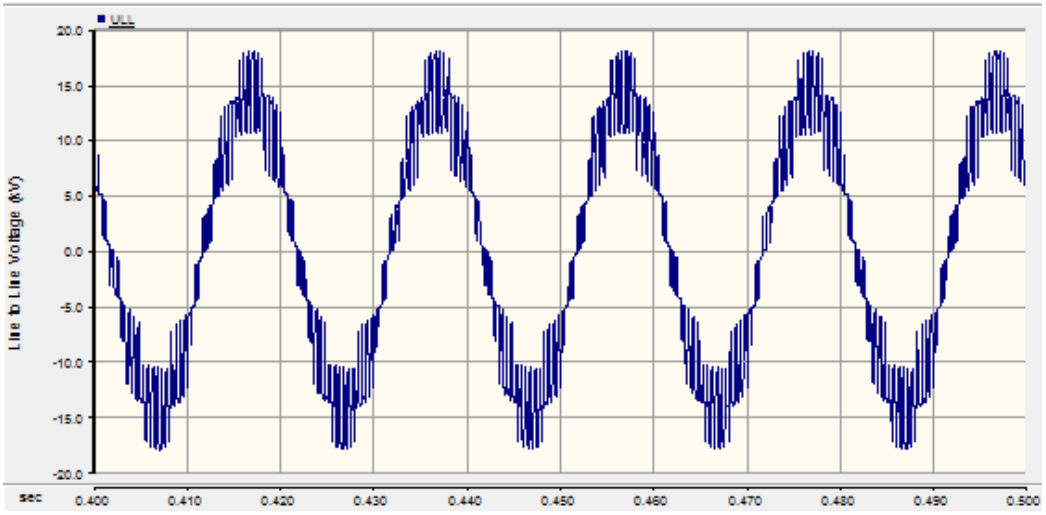


Figure 3.44 Output line-to-line voltage of N+1 level POD-PWM

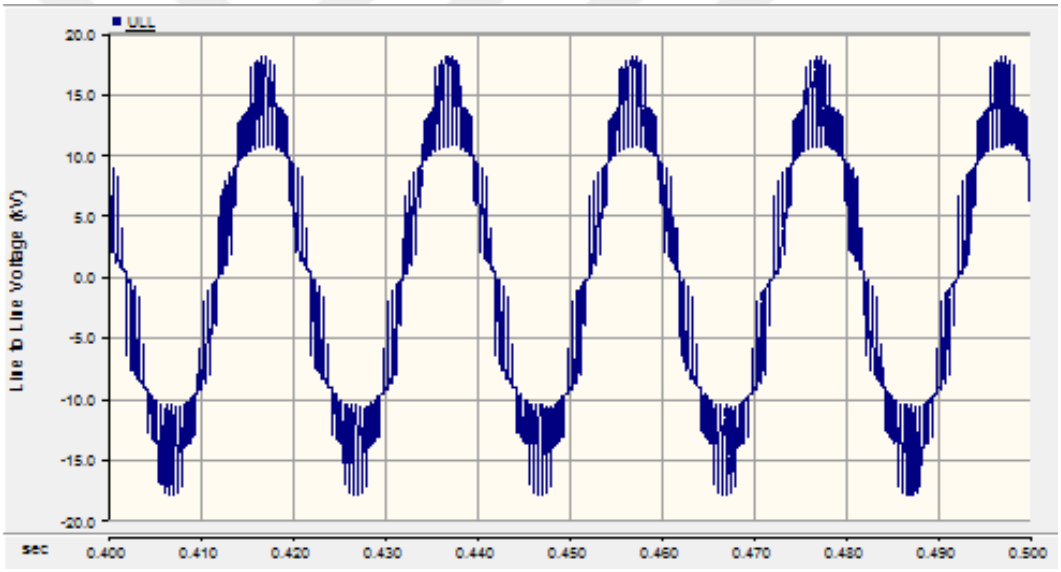


Figure 3.45 Output line-to-line voltage of N+1 level APOD-PWM

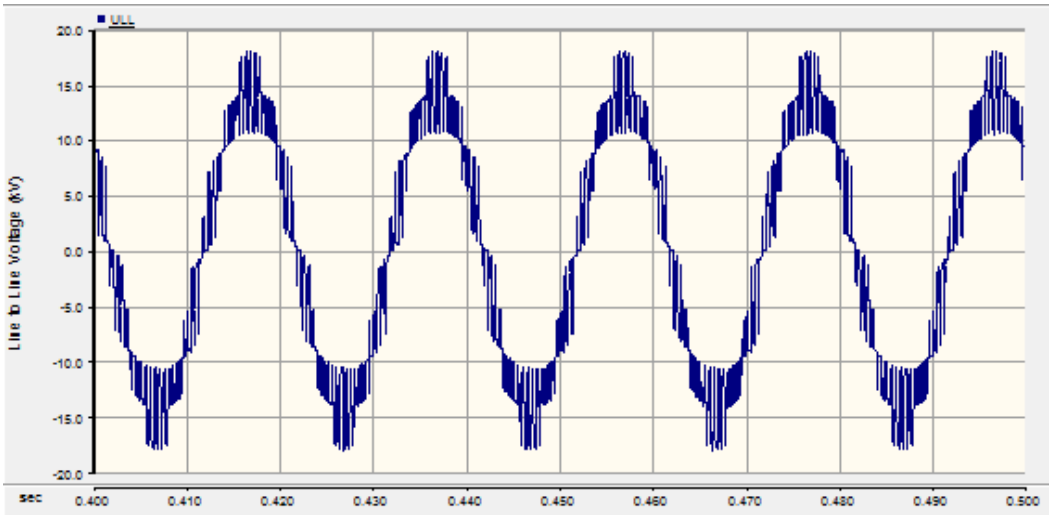


Figure 3.46 Output line-to-line voltage of N+1 level PS-PWM

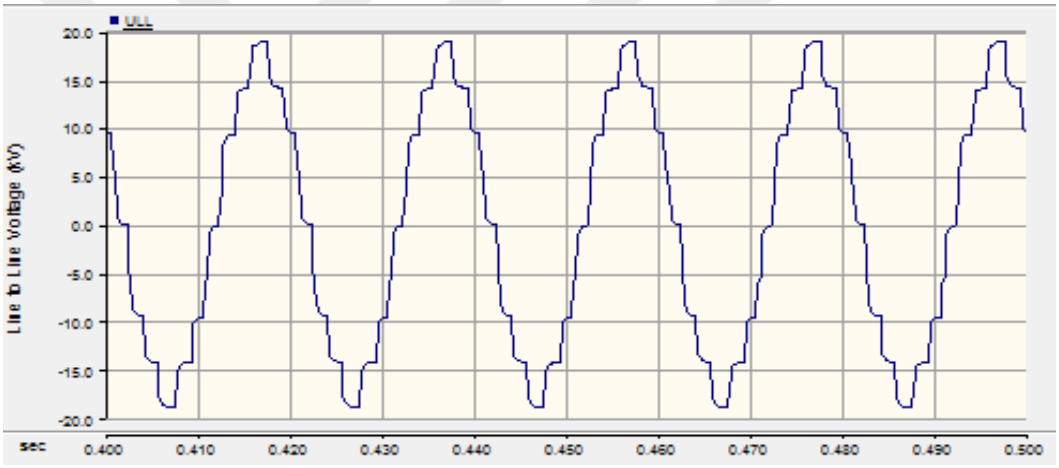


Figure 3.47 Output line-to-line voltage of N+1 level NLC

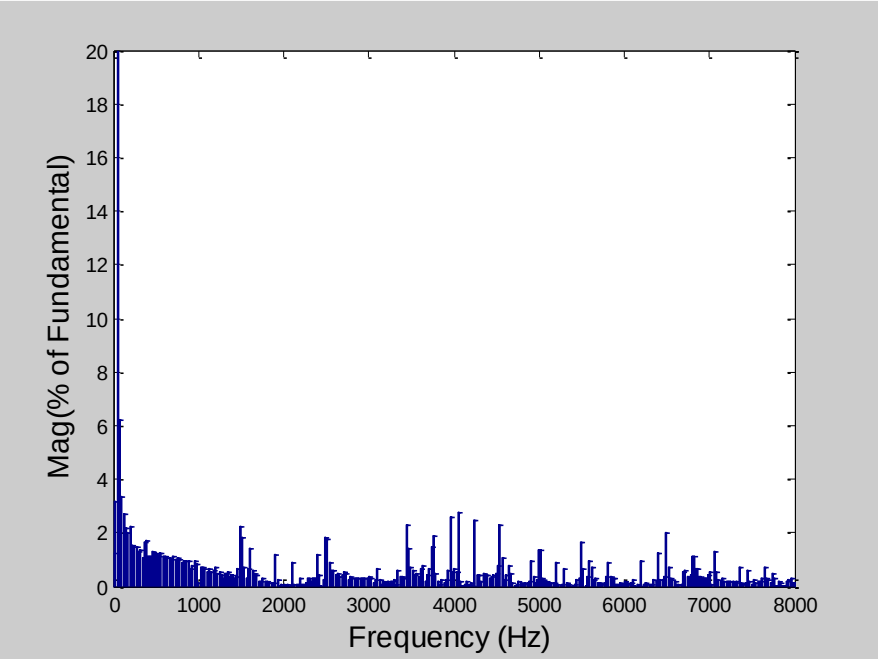


Figure 3.48 FFT analysis of the line-to-line voltage of N+1 level PD-PWM

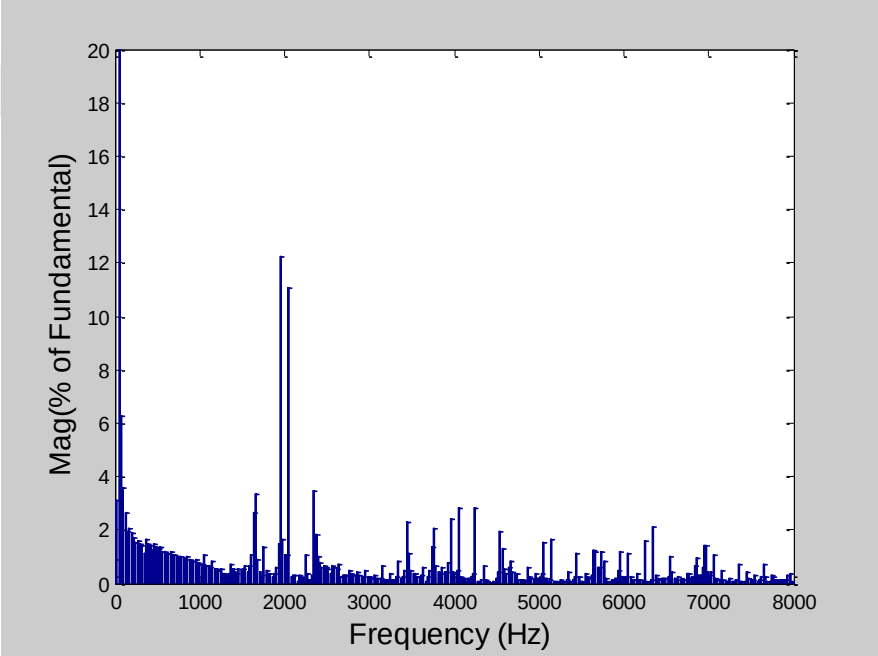


Figure 3.49 FFT analysis of the line-to-line voltage of N+1 level POD-PWM

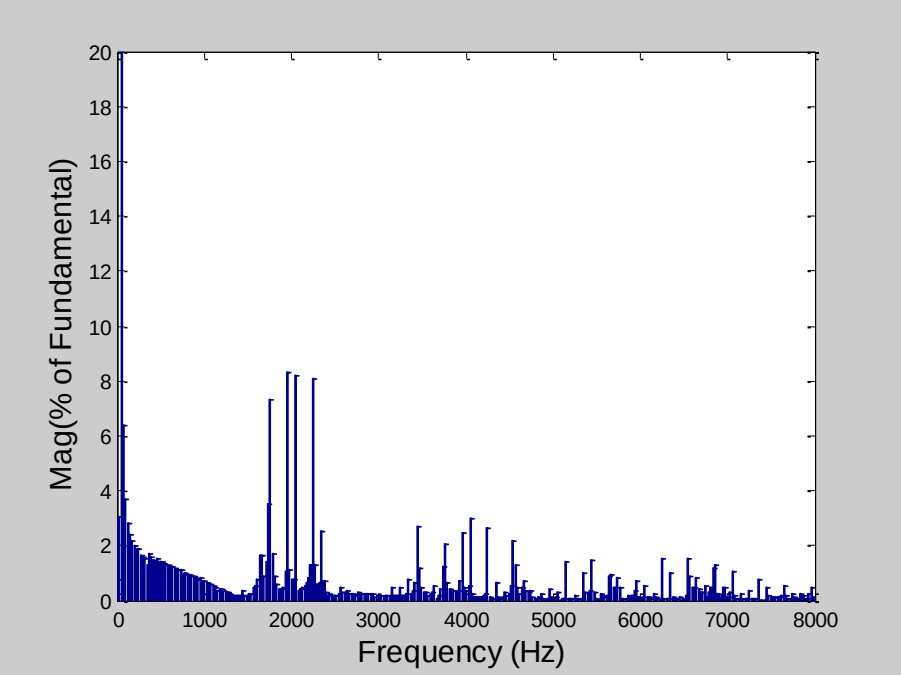


Figure 3.50 FFT analysis of the line-to-line voltage of N+1 level APOD-PWM

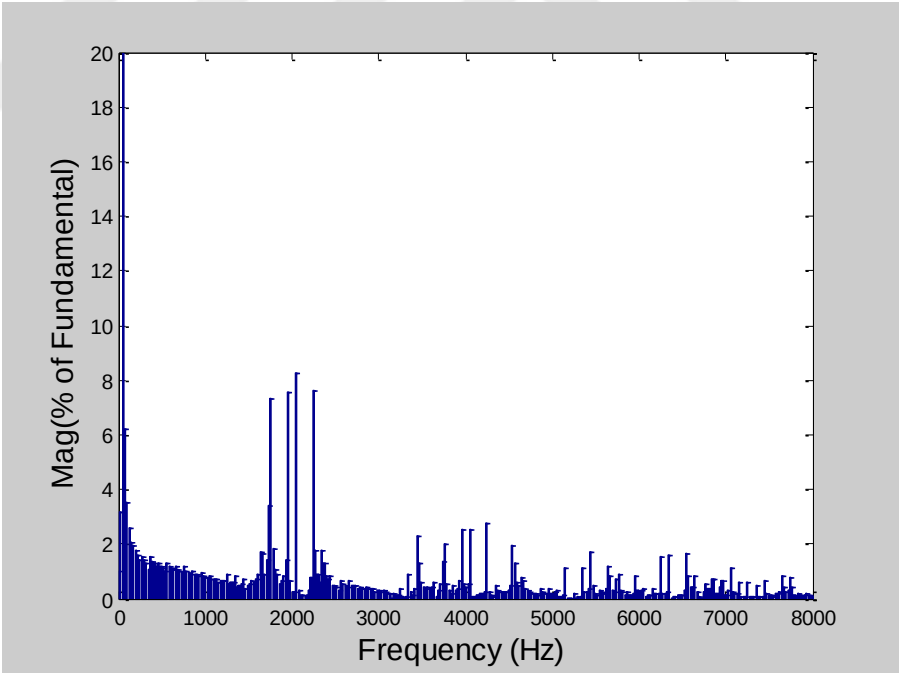


Figure 3.51 FFT analysis of the line-to-line voltage of N+1 level PS-PWM

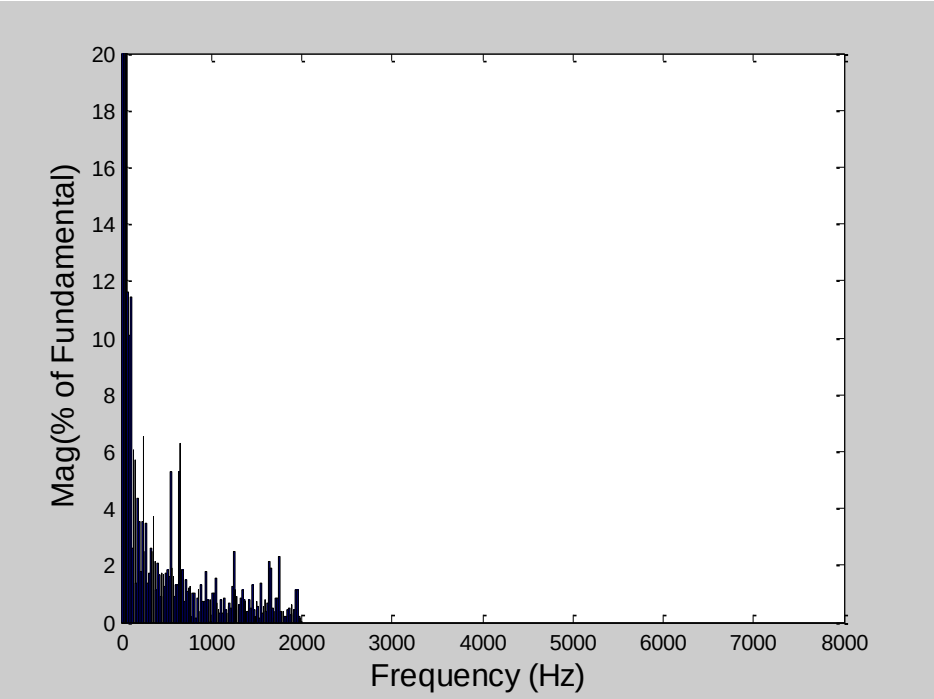


Figure 3.52 FFT analysis of the line-to-line voltage of N+1 level NLC

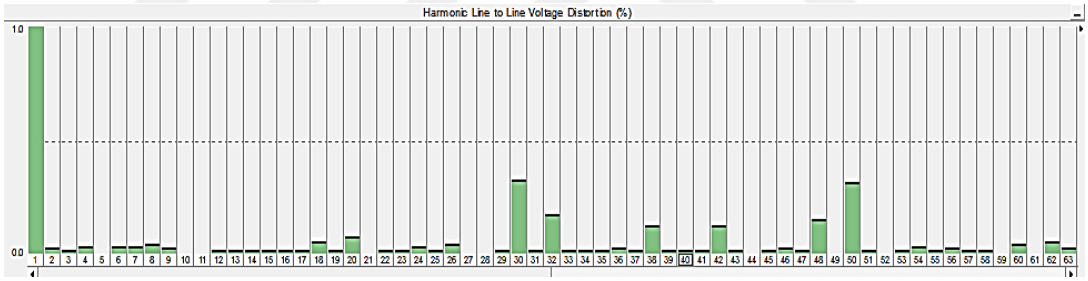


Figure 3.53 Individual harmonic distortion (%) of the line-to-line voltage of N+1 level PD-PWM

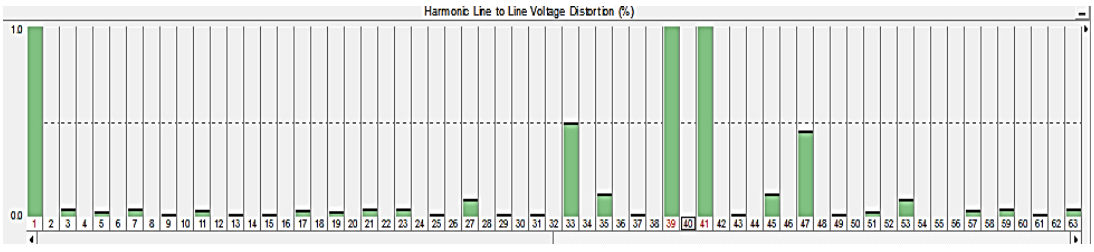


Figure 3.54 Individual harmonic distortion (%) of the line-to-line voltage of N+1 level POD-PWM

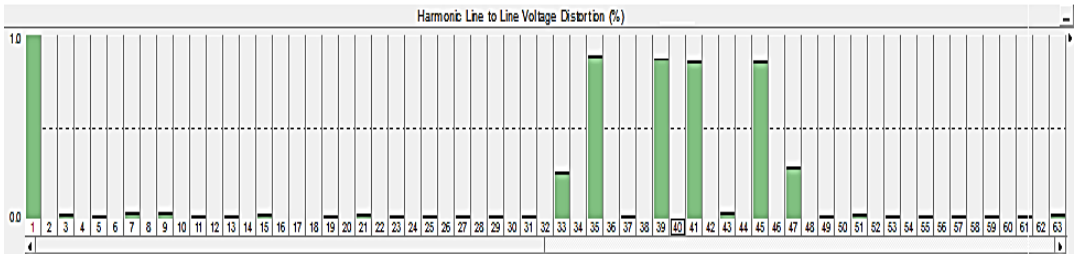


Figure 3.55 Individual harmonic distortion (%) of the line-to-line voltage of N+1 level APOD-PWM

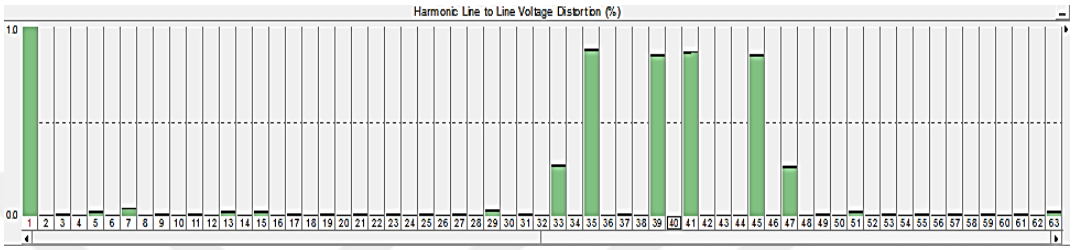


Figure 3.56 Individual harmonic distortion (%) of the line-to-line voltage of N+1 level PS-PWM

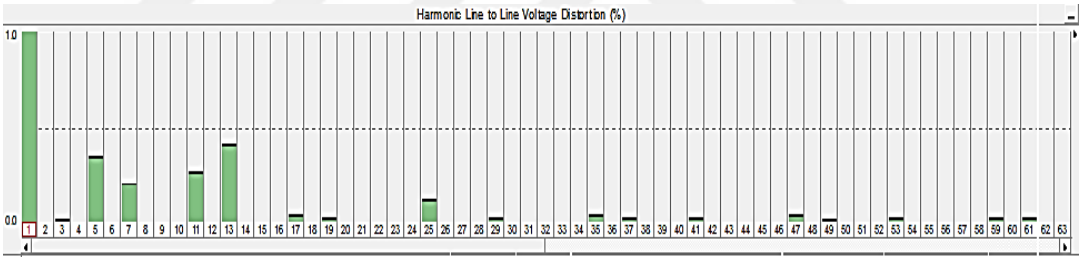


Figure 3.57 Individual harmonic distortion (%) of the line-to-line voltage of N+1 level NLC

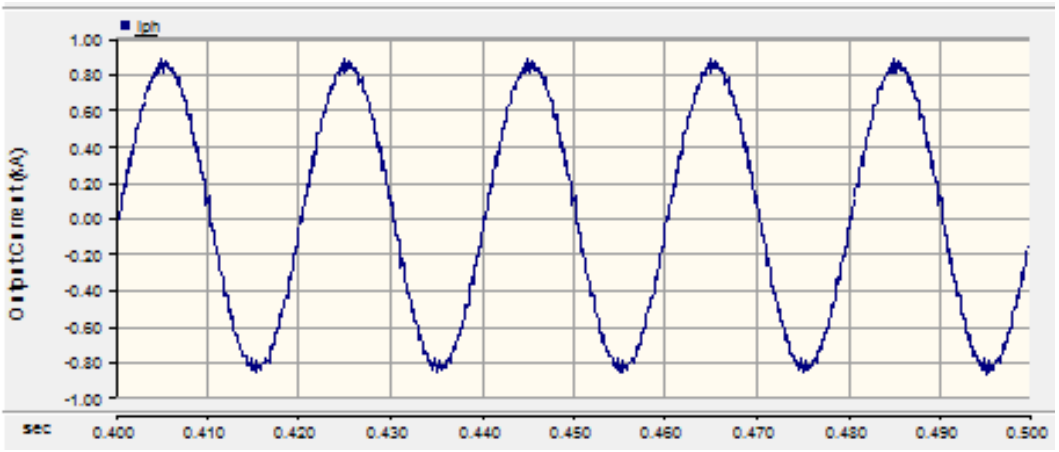


Figure 3.58 Output current of N+1 level PD-PWM

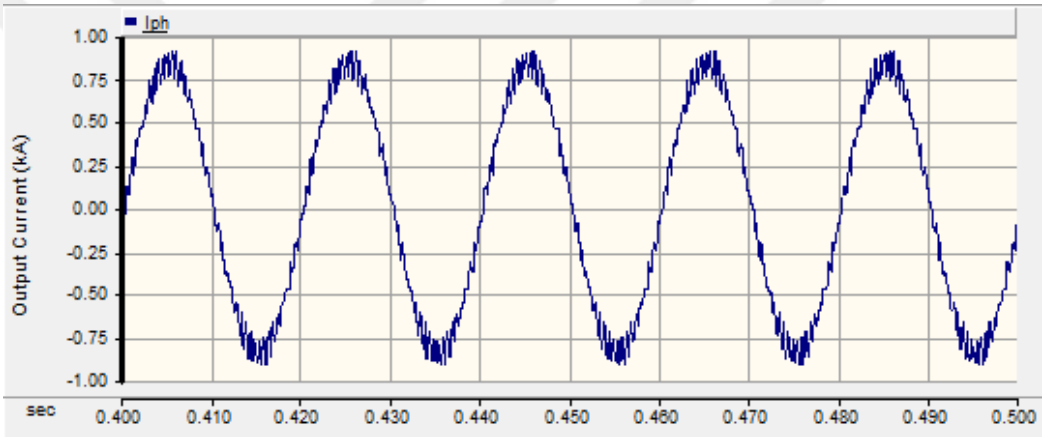


Figure 3.59 Output current of N+1 level POD-PWM

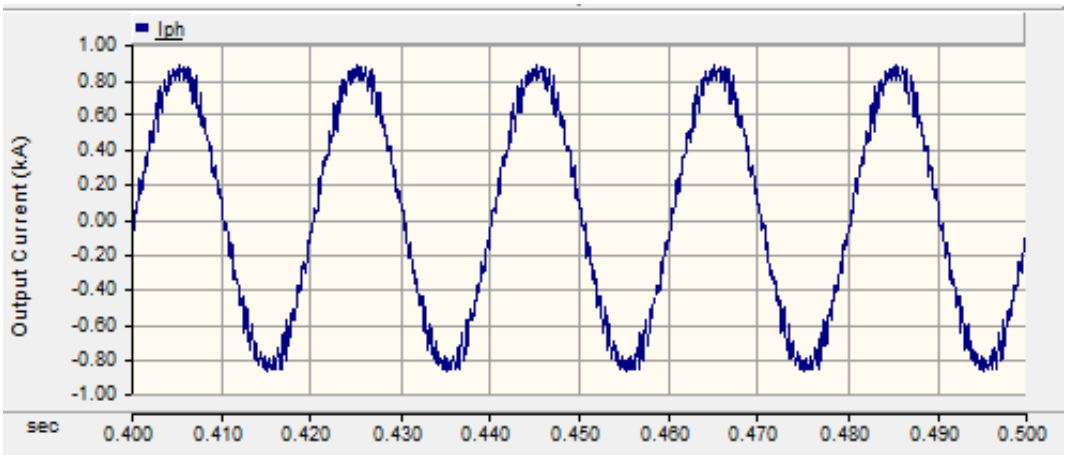


Figure 3.60 Output current of N+1 level APOD-PWM

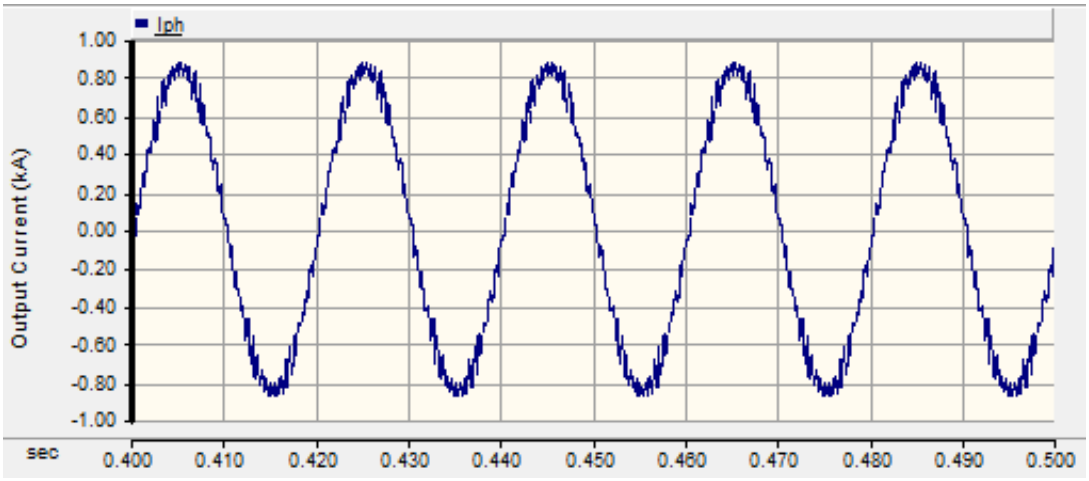


Figure 3.61 Output current of N+1 level PS-PWM

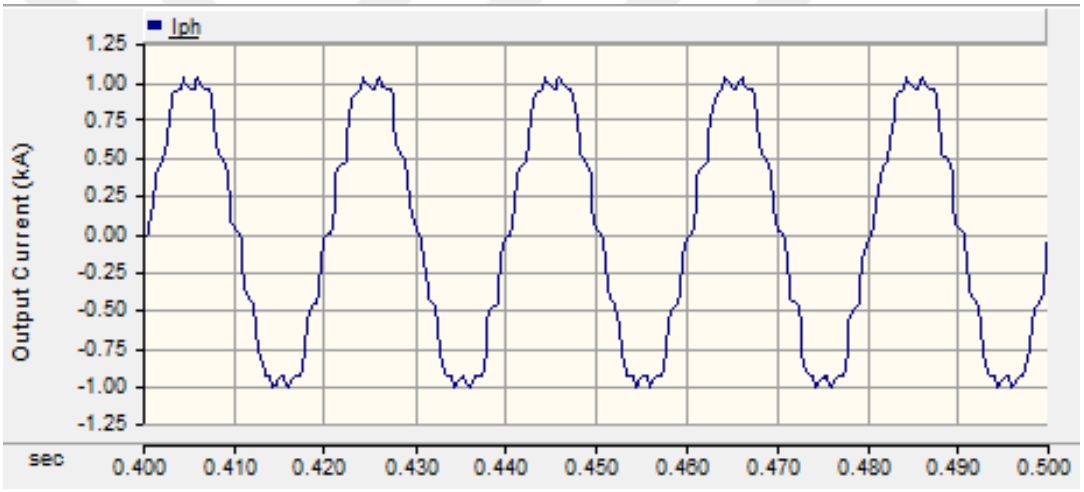


Figure 3.62 Output current of N+1 level NLC

3.6.1.2 Analysis of 2N+1 Level Line-to-line Voltage and Output Current in 5 Level MMC

In Figure 3.63 to Figure 3.67, output line voltages of 2N+1 level modulation methods are given. In Figure 3.68 to Figure 3.72, output line-to-line voltages of 2N+1 level modulation techniques are given. According to 2N+1 level line-to-line voltage, all scalar PWM switching methods give unipolar switching waveform. FFT analysis is done as shown in Figure 3.73 to Figure 3.77. Considering 2N+1 level switching case, the whole modulation methods like PD, POD,APOD and PS methods give similar

performance analysis in terms of THD analysis about 6.77 % as shown in Table 3.1. When NLC method examined, THD is observed about 5.47 % as shown in Table 3.1. According to FFT analysis, dominant harmonics for level shifted PWM methods are centered almost twice of the carrier frequency. Although, taken into account for PS-PWM method, dominant harmonics are centered about twice of the number of carriers times the carrier frequency. The analysis of the individual harmonic distortion of the line-to-line output voltages is done as seen in Figure 3.78 to Figure 3.82. Therefore, harmonics which are dominant ones are centered sidebands of the twice of modulation frequency. However, that of NLC method is observed nearly sidebands of the fundamental frequency.

Output current waveform is investigated, all scalar PWM methods give the similar results about 1.41 % THD as shown in Figure 3.83 to Figure 3.86 and also NLC has nearly 3.92 % THD in the output current as illustrated in Figure 3.87.

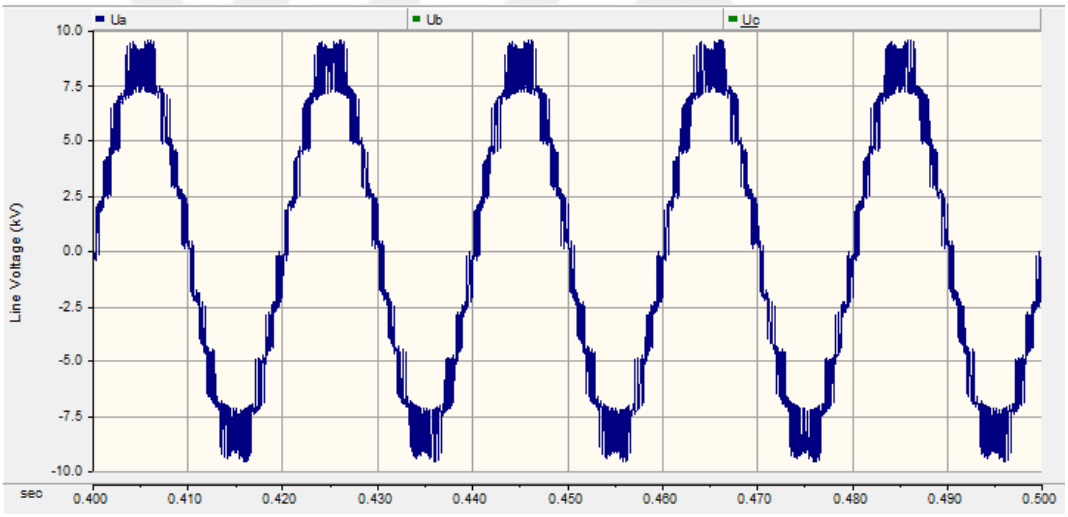


Figure 3.63 Output line voltage of 2N+1 level PD-PWM

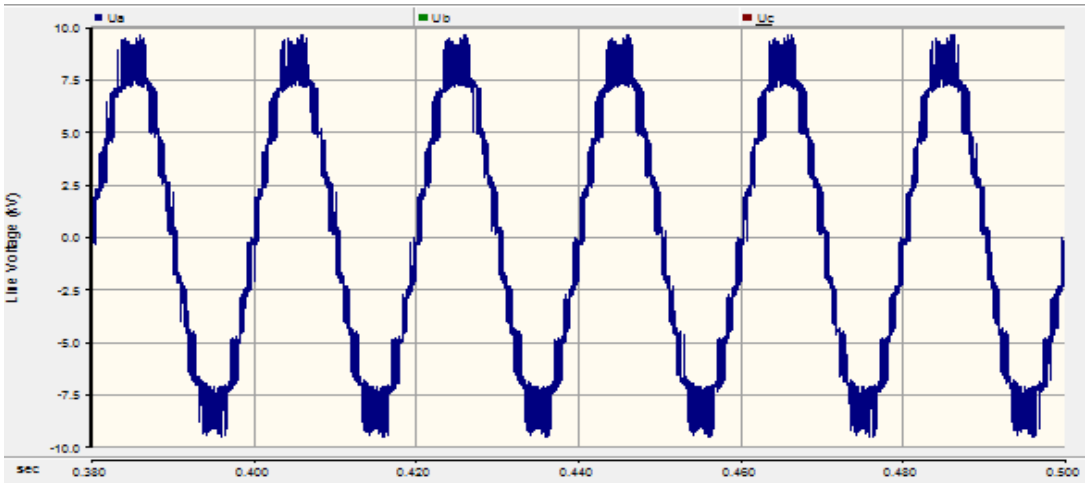


Figure 3.64 Output line voltage of 2N+1 level POD-PWM

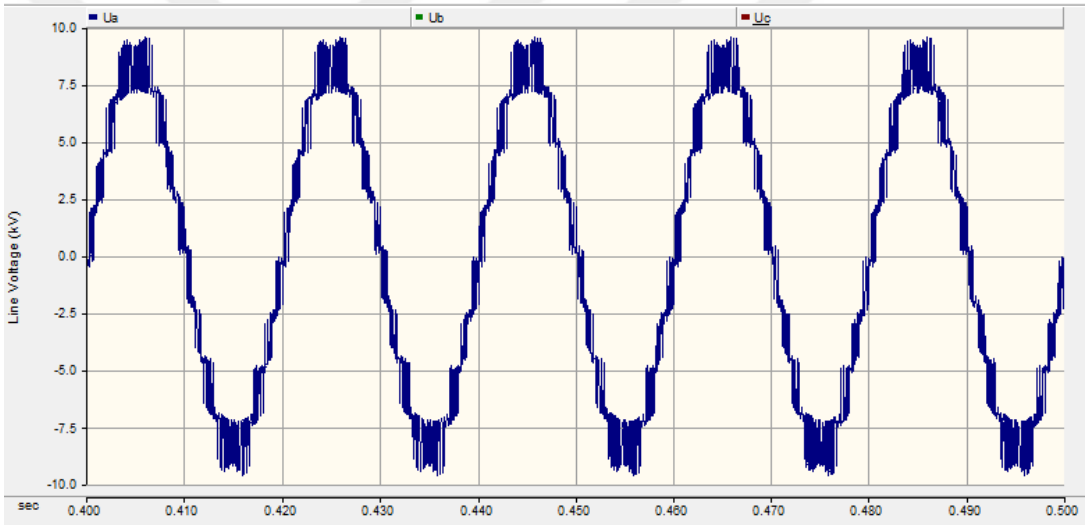


Figure 3.65 Output line voltage of 2N+1 level APOD-PWM

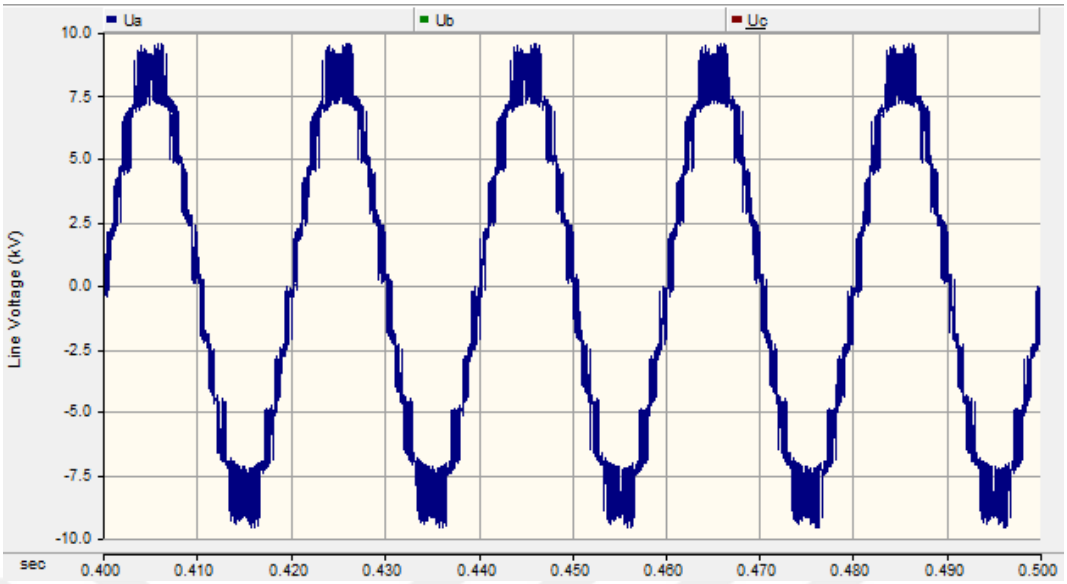


Figure 3.66 Output line voltage of 2N+1 level PS-PWM

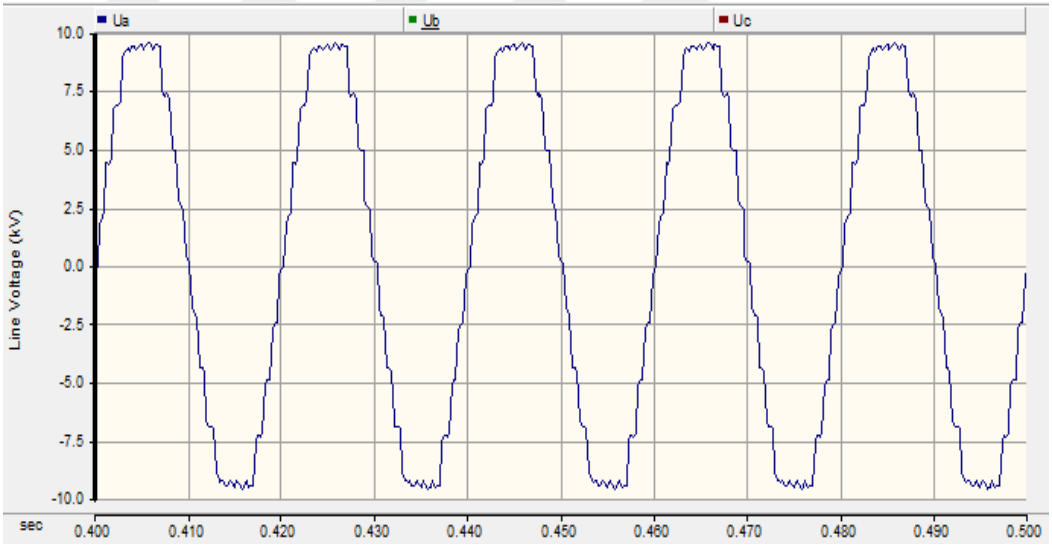


Figure 3.67 Output line voltage of 2N+1 level NLC

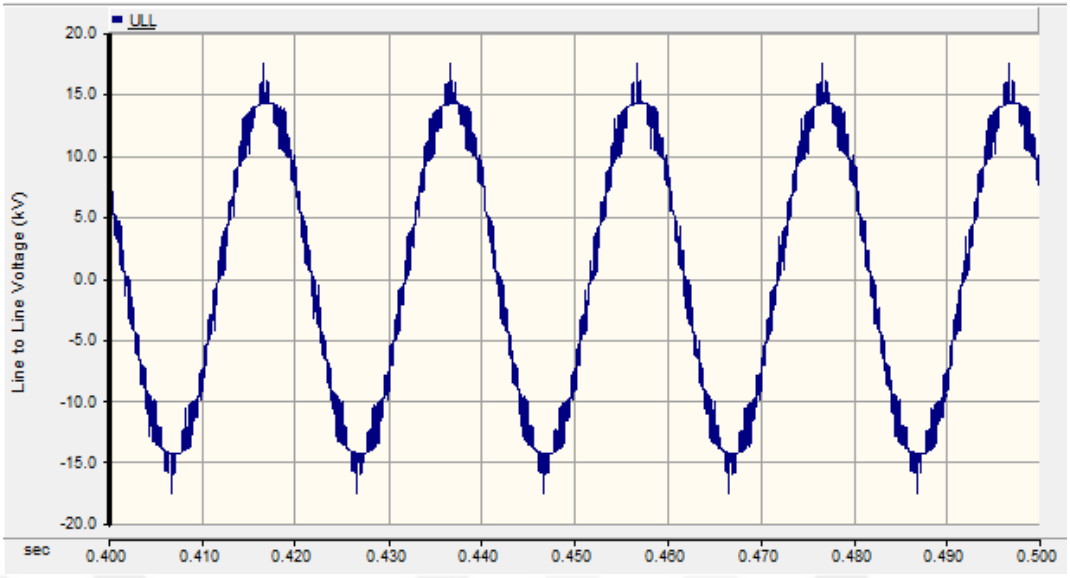


Figure 3.68 Output line-to-line voltage of 2N+1 level PD-PWM

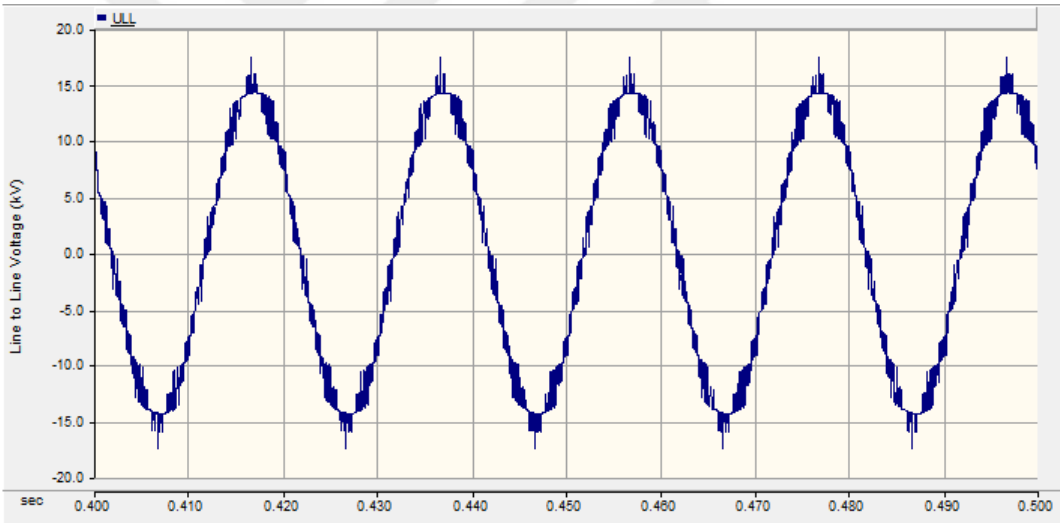


Figure 3.69 Output line-to-line voltage of 2N+1 level POD-PWM

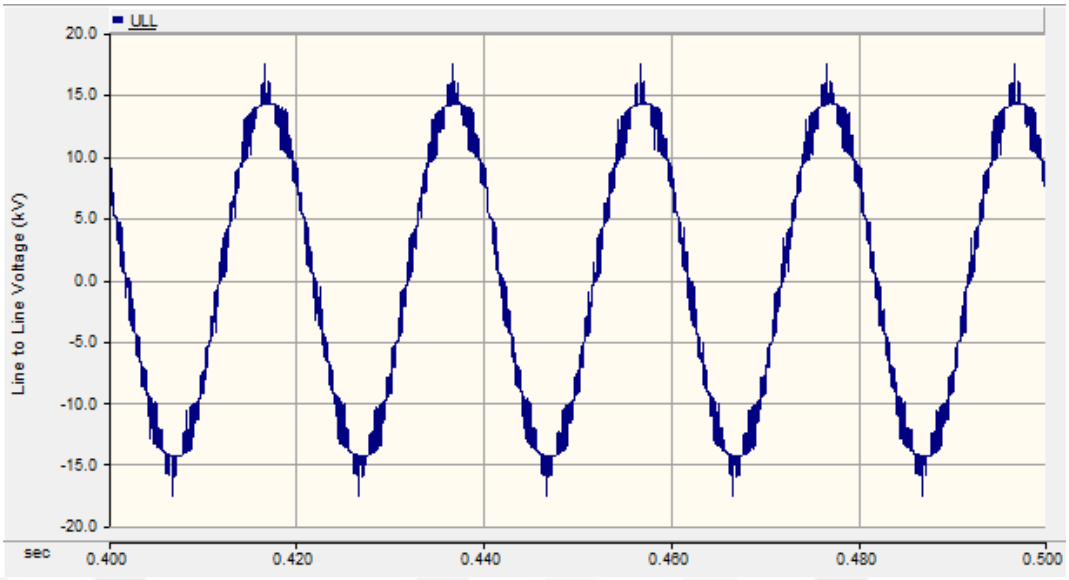


Figure 3.70 Output line-to-line voltage of 2N+1 level APOD-PWM

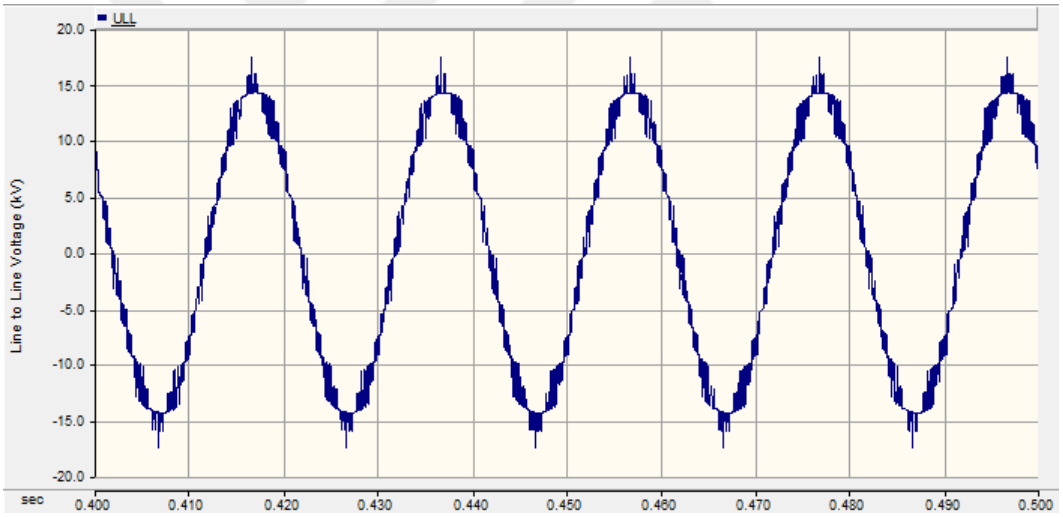


Figure 3.71 Output line-to-line voltage of 2N+1 level PS-PWM

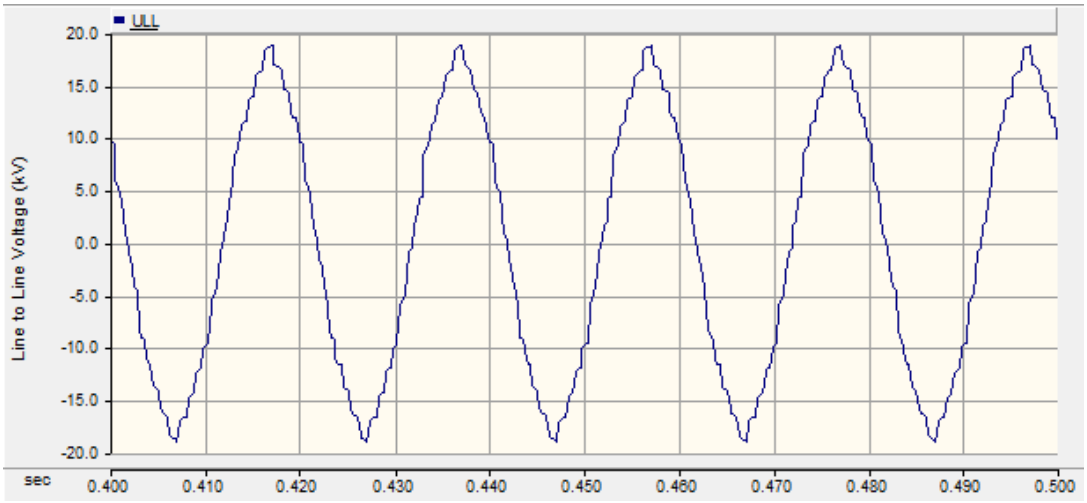


Figure 3.72 Output line-to-line voltage of 2N+1 level NLC

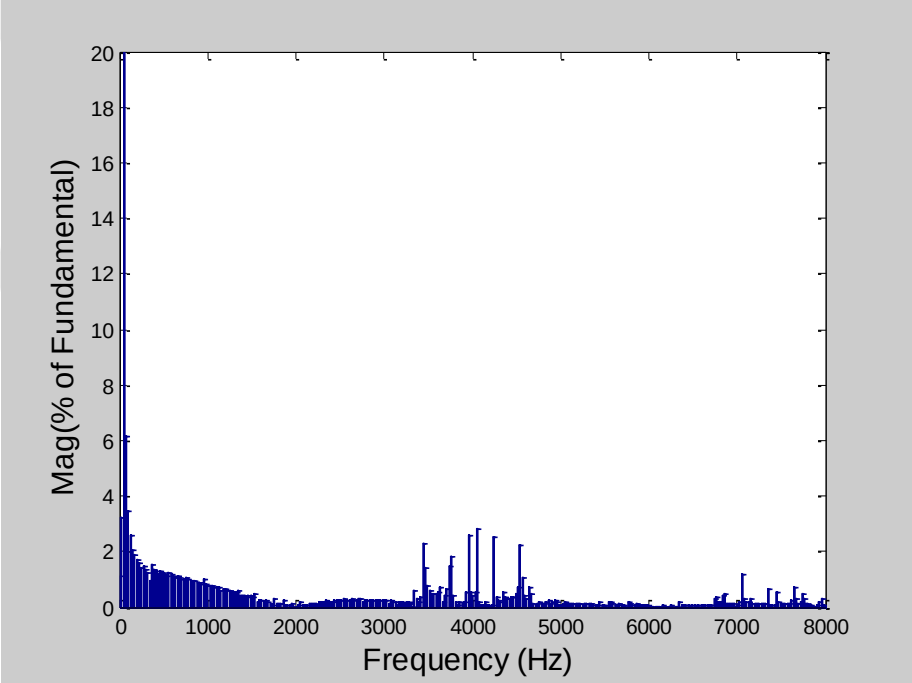


Figure 3.73 FFT analysis of the line-to-line voltage of 2N+1 level PD-PWM

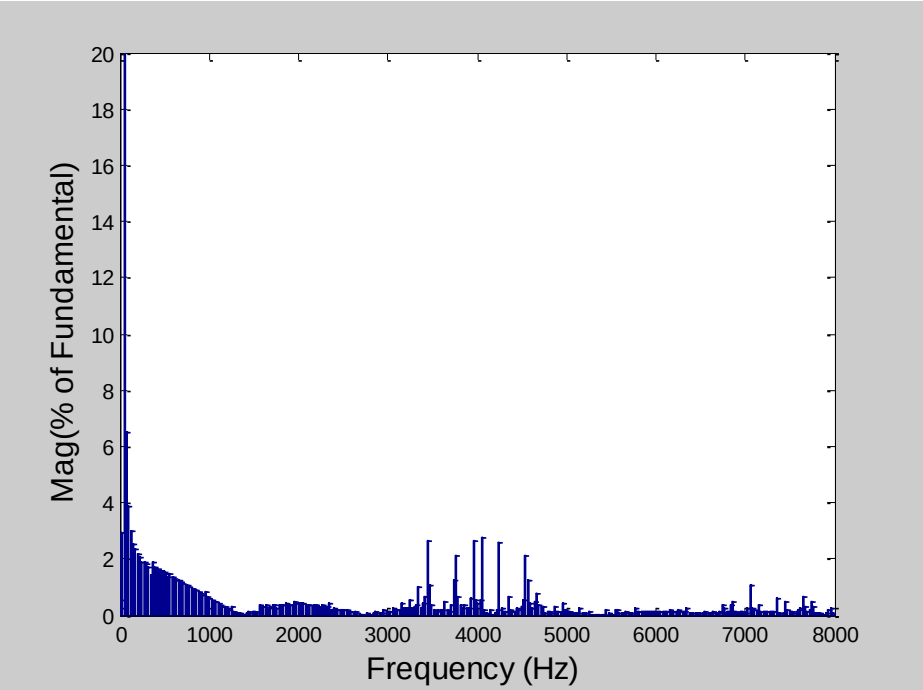


Figure 3.74 FFT analysis of the line-to-line voltage of 2N+1 level POD-PWM

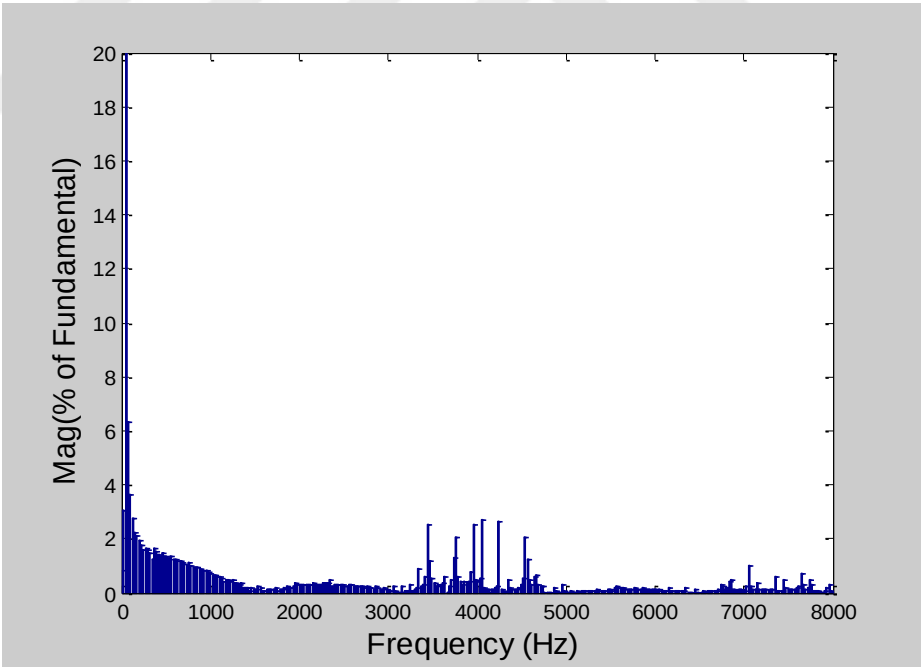


Figure 3.75 FFT analysis of the line-to-line voltage of 2N+1 level APOD-PWM

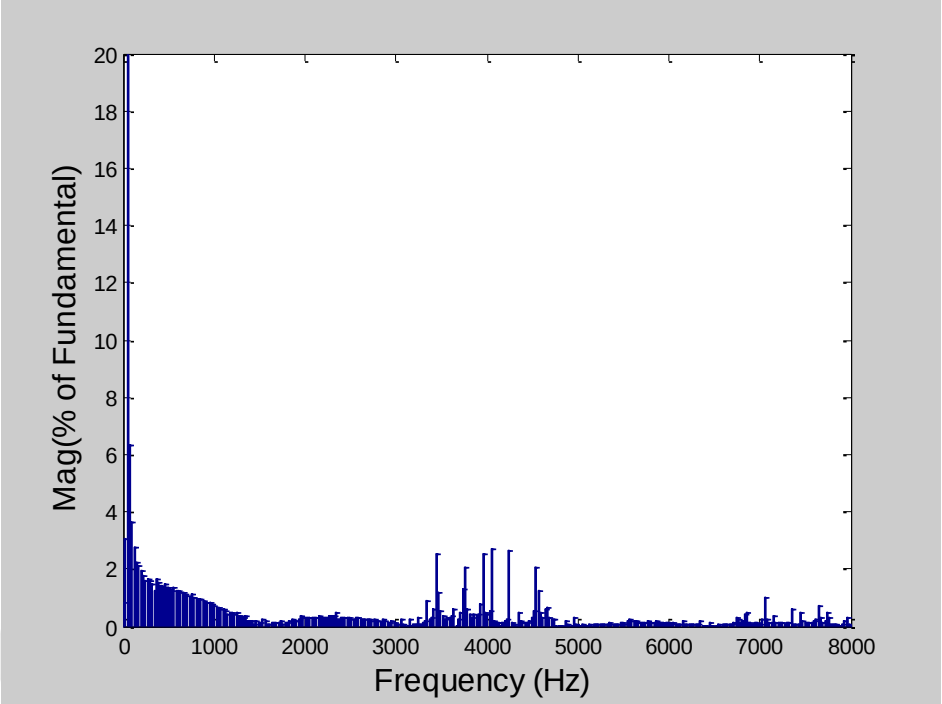


Figure 3.76 FFT analysis of the line-to-line voltage of 2N+1 level PS-PWM

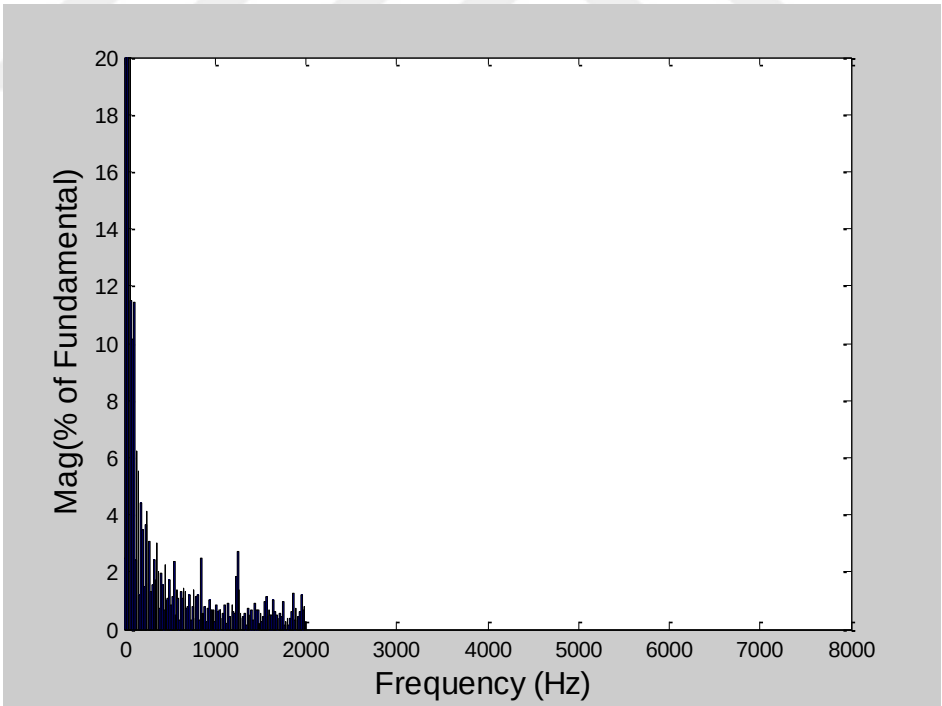


Figure 3.77 FFT analysis of the line-to-line voltage of 2N+1 level NLC

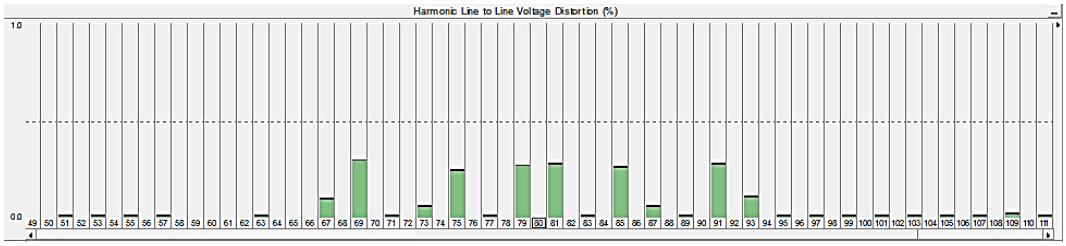


Figure 3.78 Individual harmonic distortion (%) of the line-to-line voltage of 2N+1 level PD-PWM

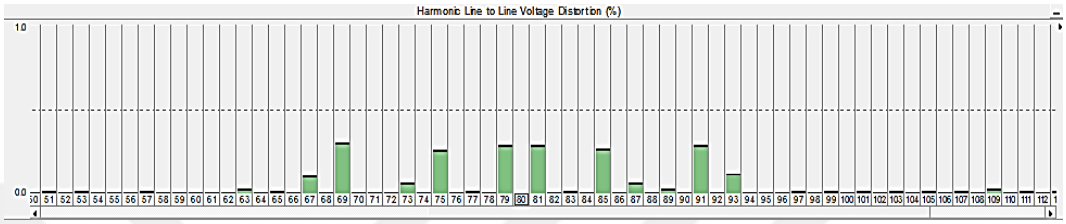


Figure 3.79 Individual harmonic distortion (%) of the line-to-line voltage of 2N+1 level POD-PWM

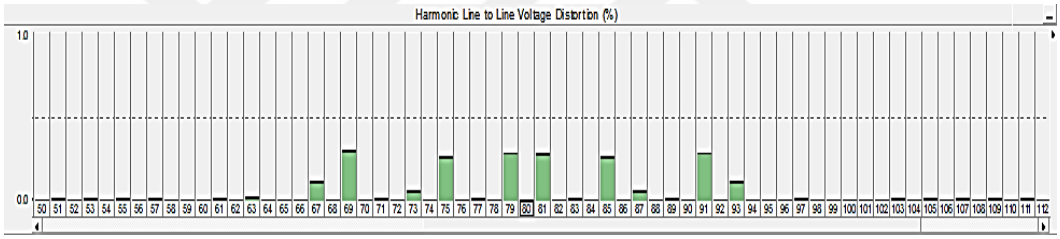


Figure 3.80 Individual harmonic distortion (%) of the line-to-line voltage of 2N+1 level APOD-PWM

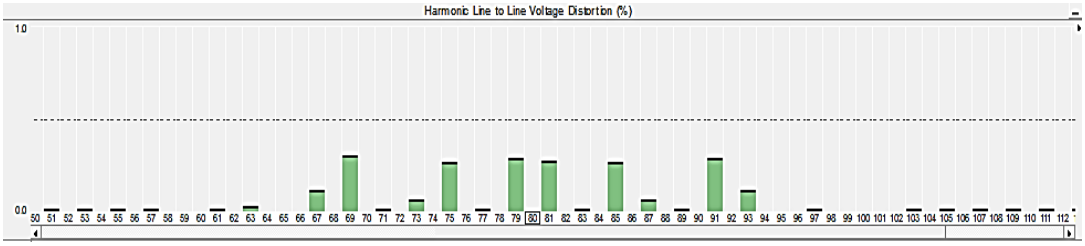


Figure 3.81 Individual harmonic distortion (%) of the line-to-line voltage of 2N+1 level PS-PWM

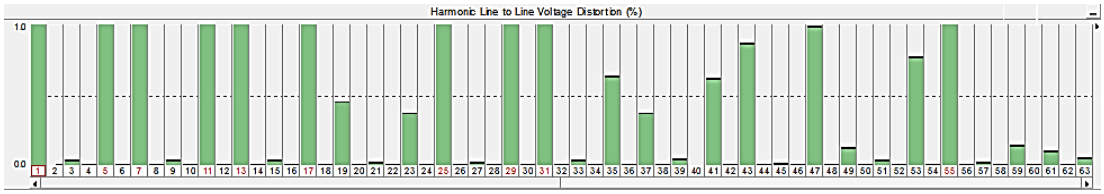


Figure 3.82 Individual harmonic distortion (%) of the line-to-line voltage of 2N+1 level NLC

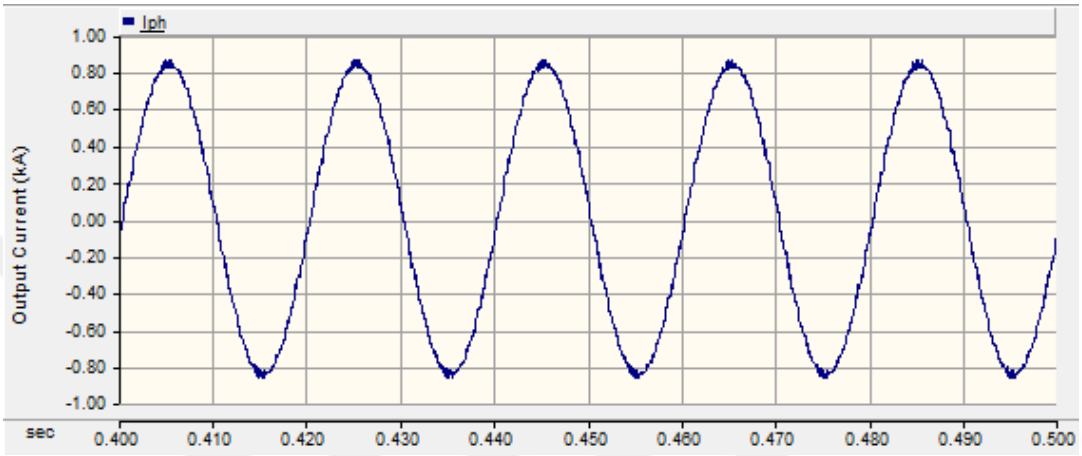


Figure 3.83 Output current of 2N+1 level PD-PWM

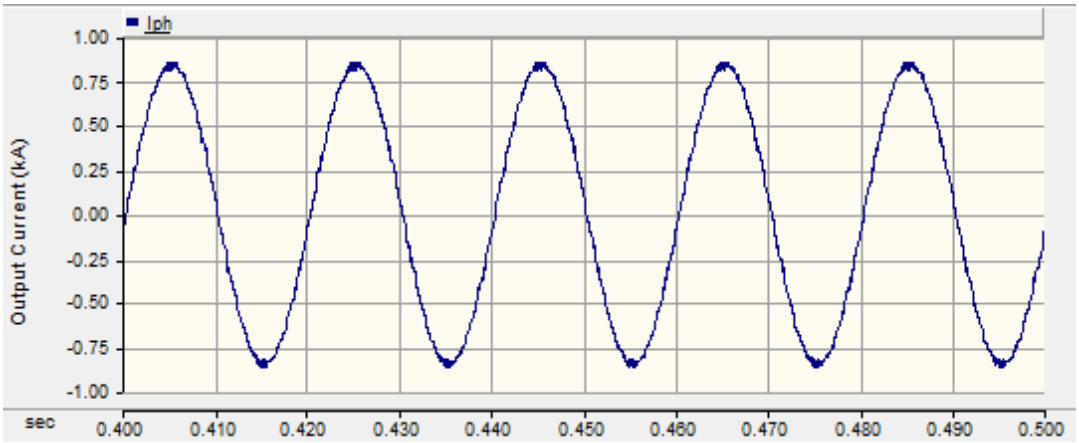


Figure 3.84 Output current of 2N+1 level POD-PWM

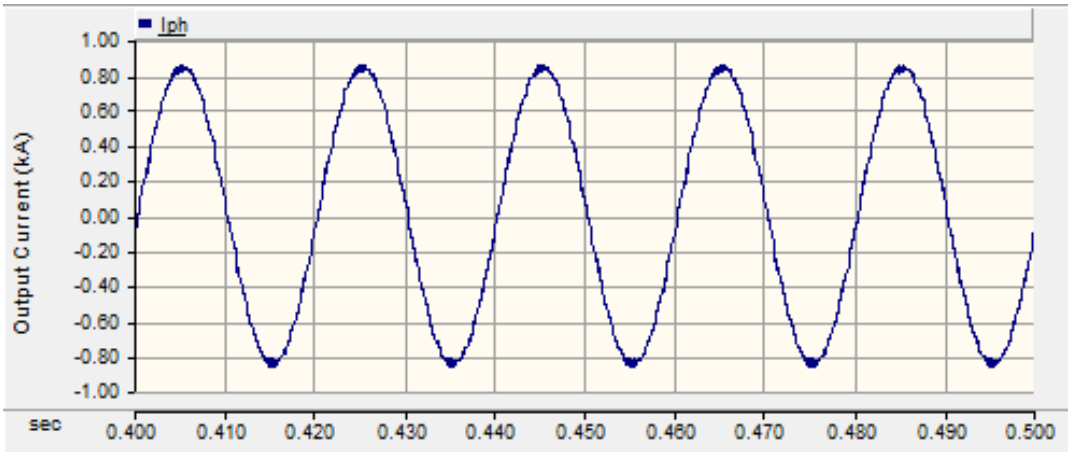


Figure 3.85 Output current of 2N+1 level APOD-PWM

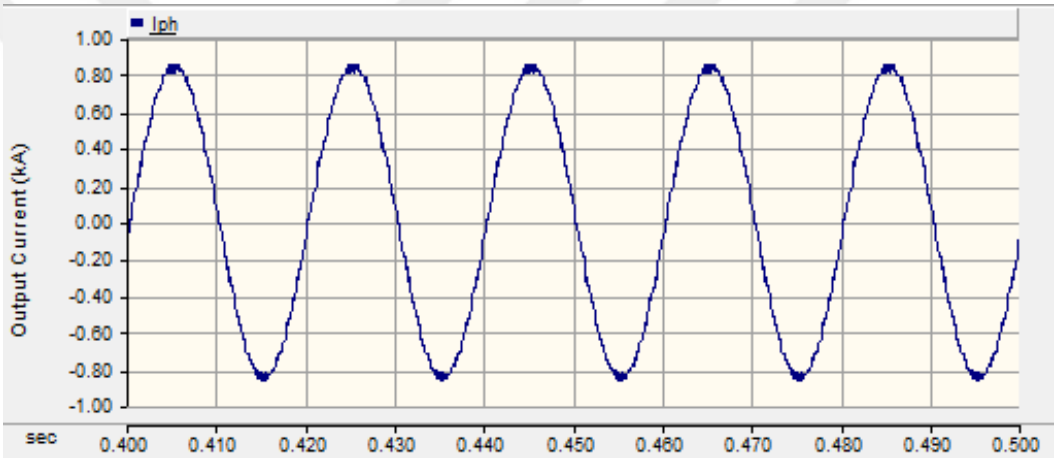


Figure 3.86 Output current of 2N+1 level PS-PWM

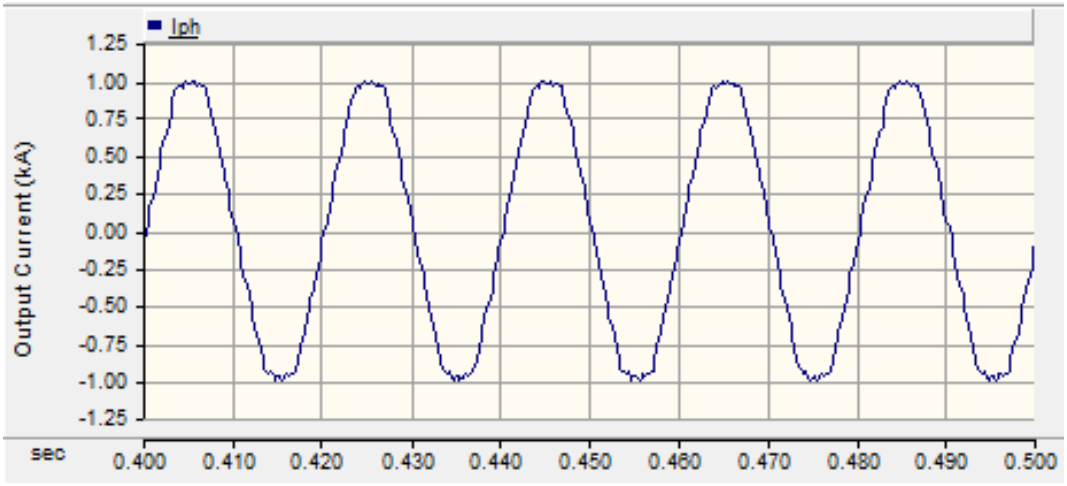


Figure 3.87 Output current of 2N+1 level NLC

3.6.1.3 Analysis of N+1 Level Line-to-line Voltage and Output Current in 6 Level MMC

In Figure 3.88 to Figure 3.91, output line voltages of N+1 level modulation methods are given. In Figure 3.92 to Figure 3.95, output line-to-line voltages of N+1 level modulation techniques are given. FFT analysis is done as shown in Figure 3.96 to Figure 3.99. Moreover, individual harmonic analysis is implemented to all modulation methods as shown in Figure 3.100 to Figure 3.103.Under N+1 level switching, performance analysis of APOD-PWM and PS-PWM are identical to each other. However, PD-PWM has better results. PS-PWM and APOD-PWM have about 12.19 % THD in the line-to-line output voltage as given in Table 3.4. Nevertheless, PD-PWM has nearly 8 % THD in the line-to-line output voltage. NLC method has 8.07 % THD in the output line-to-line waveform. According to FFT analysis, dominant harmonics for level shifted PWM methods are centered almost their carrier frequency or switching frequency. Although, that carrier frequency of PS-PWM method is different than other level shifted methods, dominant harmonics are observed about its switching frequency as in level shifted PWM methods. Considering NLC method dominant harmonics are centered sidebands of the fundamental frequency. Moreover, output current waveforms are also investigated, PD-PWM technique gives the best result in terms of performance analysis among the modulation methods about 2.26 % THD in the current waveform analysis. APOD

and PS give the similar results nearly 4% THD in the output current waveform. NLC method has 5.96 % THD in the current waveform analysis.

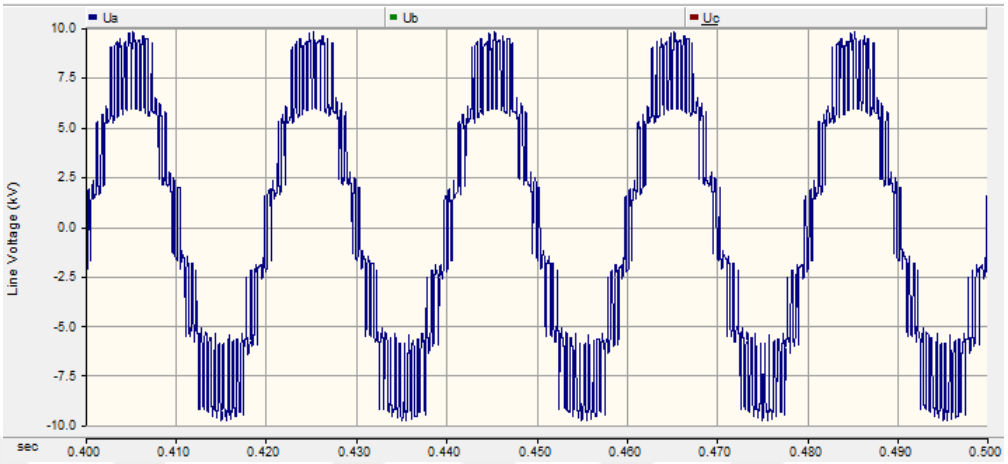


Figure 3.88 Output line voltage of N+1 level PD-PWM

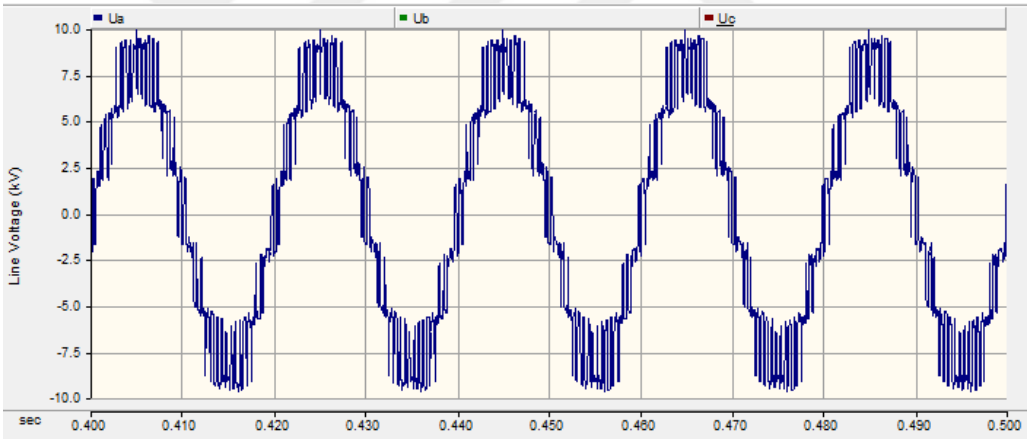


Figure 3.89 Output line voltage of N+1 level APOD-PWM

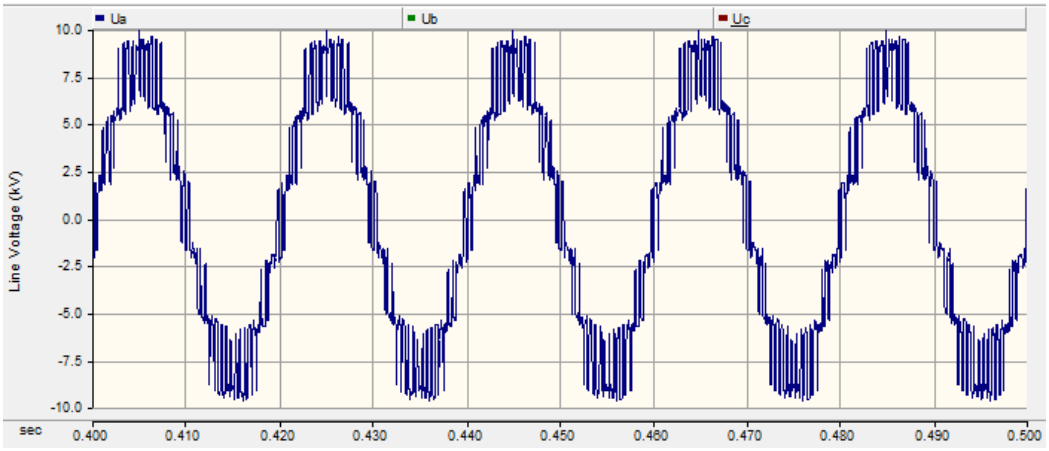


Figure 3.90 Output line voltage of N+1 level PS-PWM

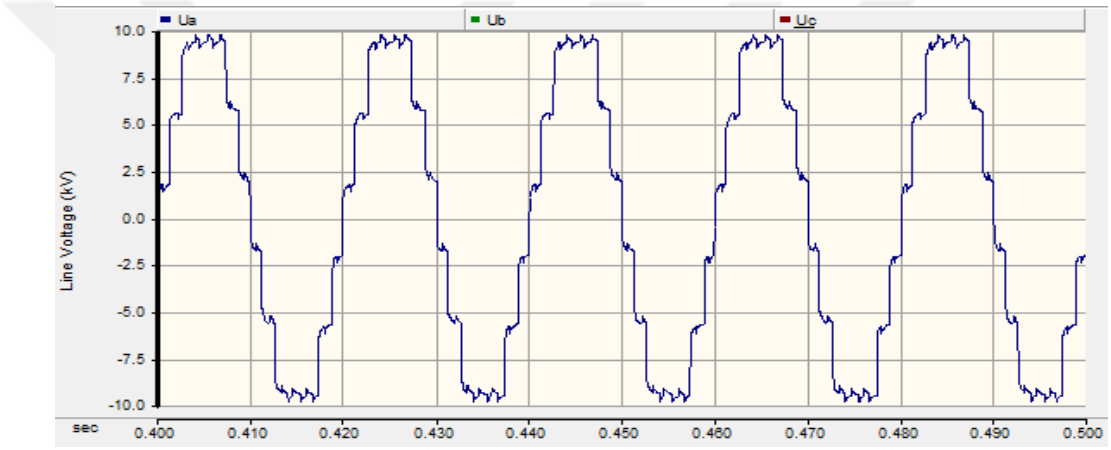


Figure 3.91 Output line voltage of N+1 level NLC

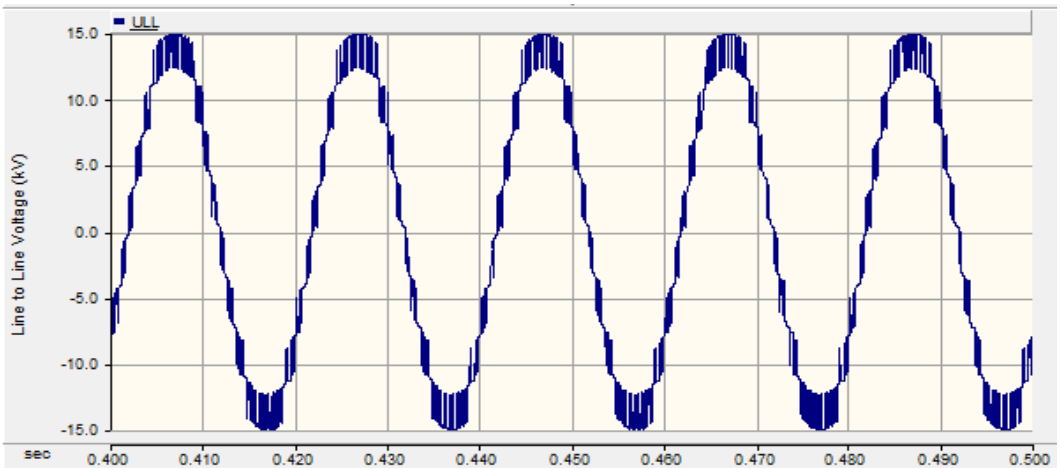


Figure 3.92 Output line-to-line voltage of N+1 level PD-PWM

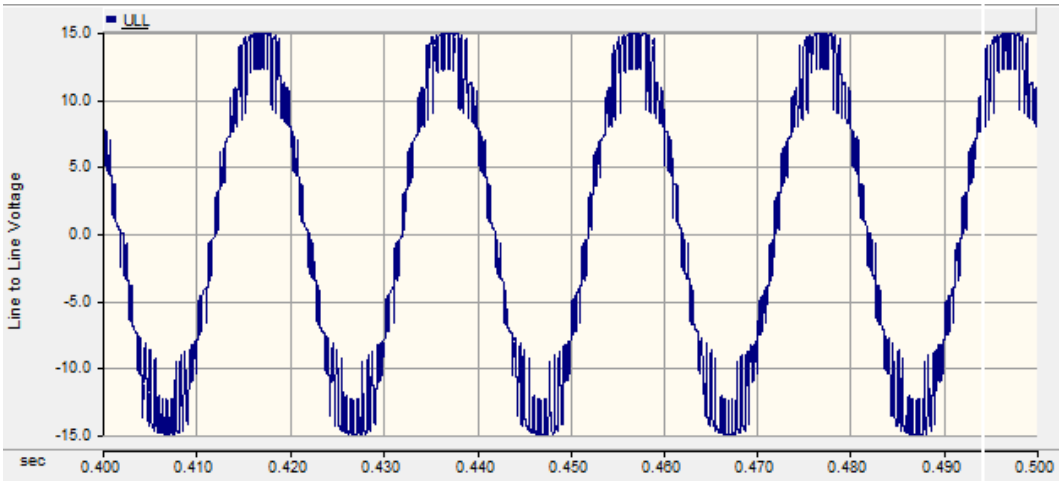


Figure 3.93 Output line-to-line voltage of N+1 level APOD-PWM

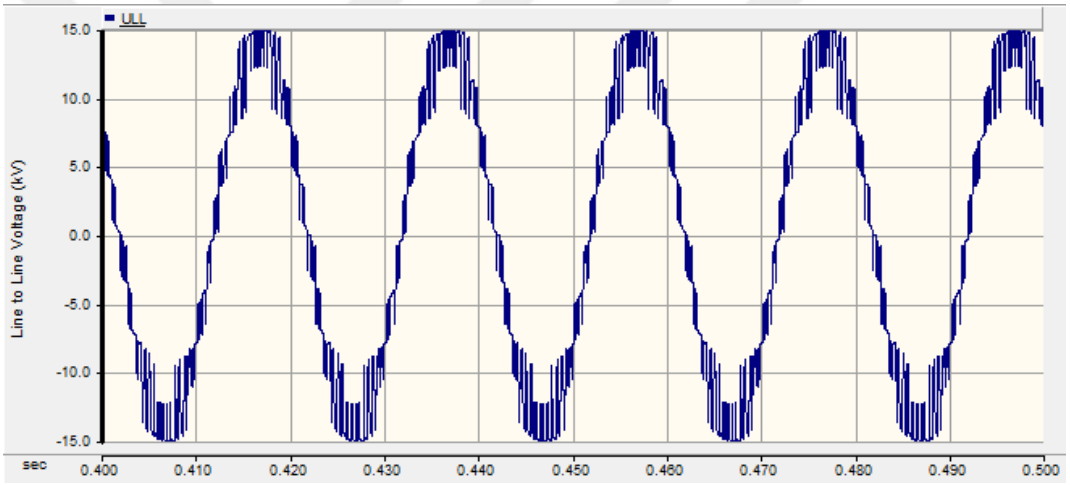


Figure 3.94 Output line-to-line voltage of N+1 level PS-PWM

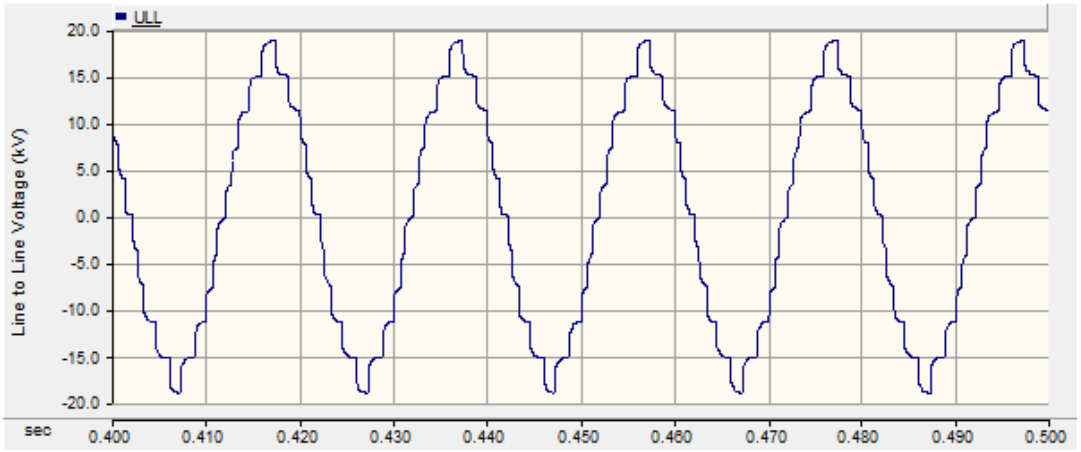


Figure 3.95 Output line-to-line voltage of N+1 level NLC

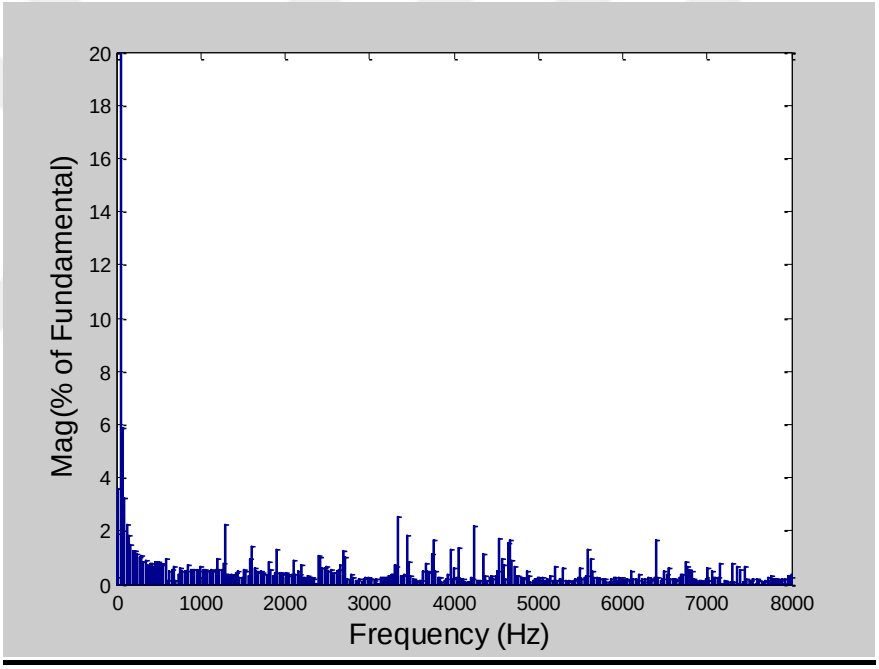


Figure 3.96 FFT analysis of the line-to-line voltage of N+1 level PD-PWM

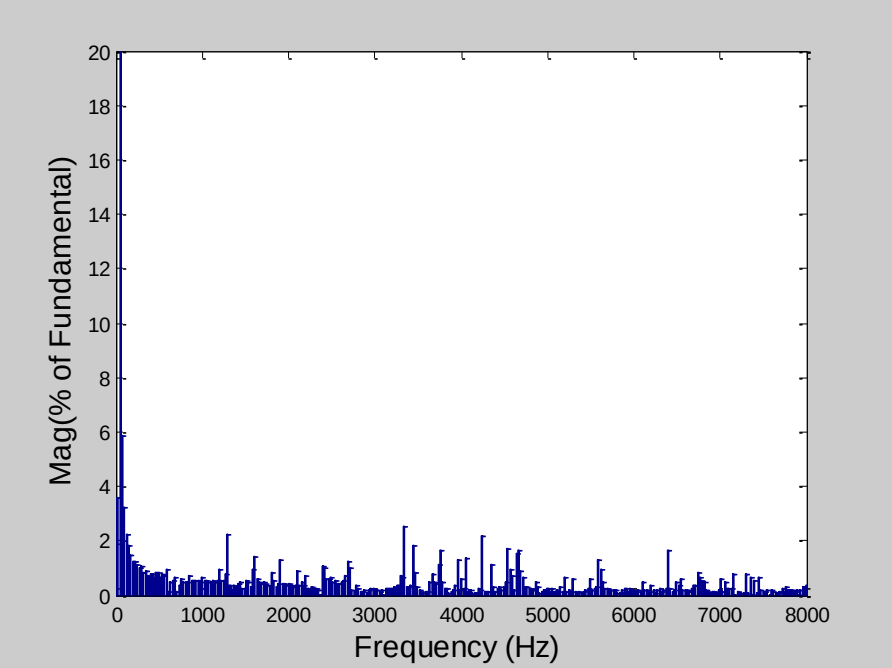


Figure 3.97 FFT analysis of the line-to-line voltage of N+1 level APOD-PWM

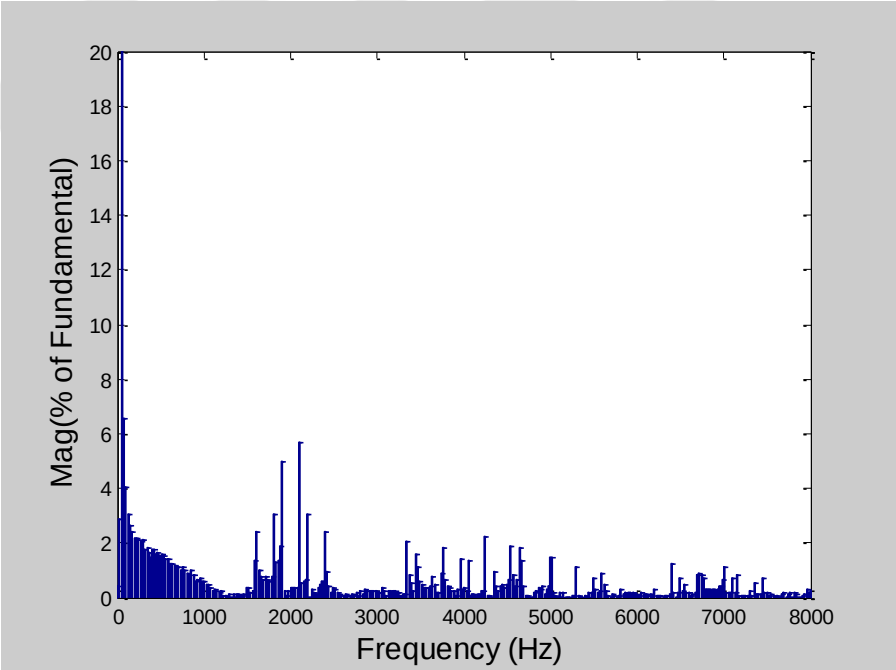


Figure 3.98 FFT analysis of the line-to-line voltage of N+1 level PS-PWM

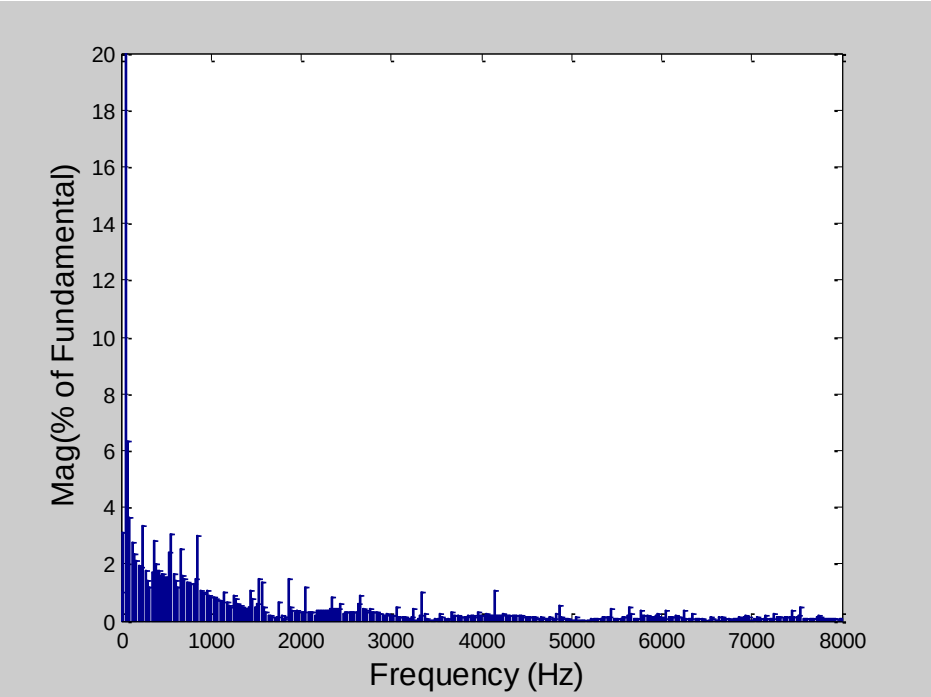


Figure 3.99 FFT analysis of the line-to-line voltage of N+1 level NLC

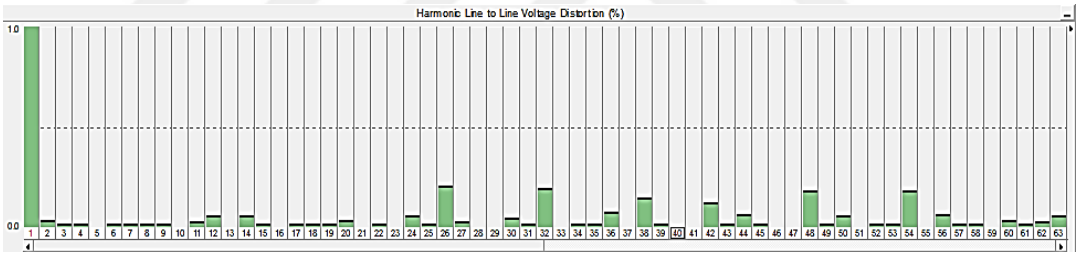


Figure 3.100 Individual harmonic distortion (%) of the line-to-line voltage of N+1 level PD-PWM

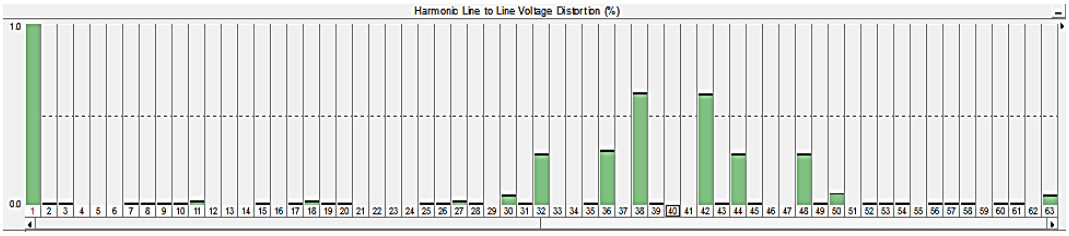


Figure 3.101 Individual harmonic distortion (%) of the line-to-line voltage of N+1 level APOD-PWM

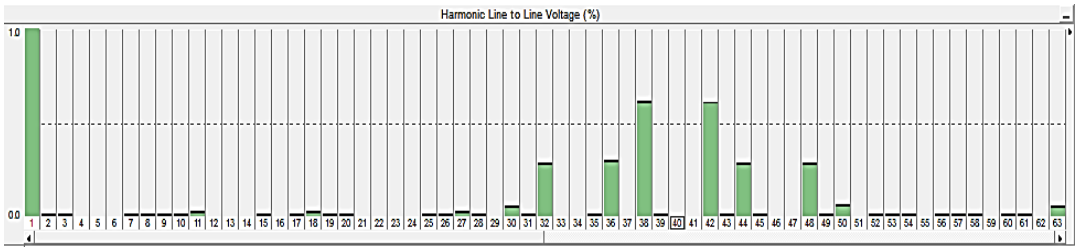


Figure 3.102 Individual harmonic distortion (%) of the line-to-line voltage of N+1 level PS-PWM

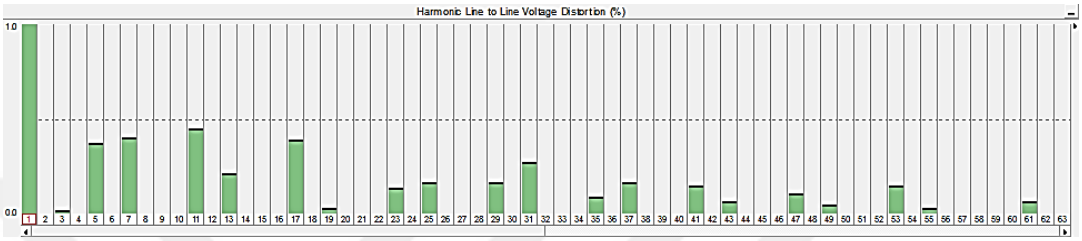


Figure 3.103 Individual harmonic distortion (%) of the line-to-line voltage of N+1 level NLC

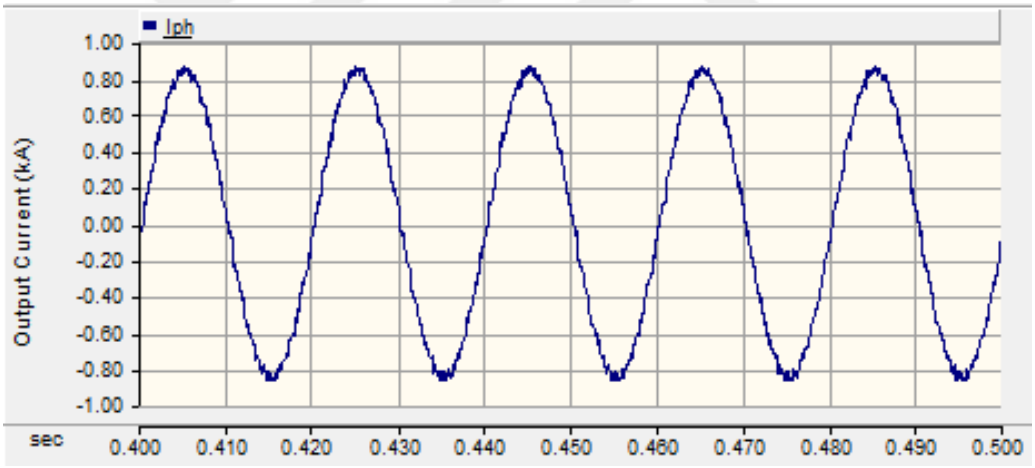


Figure 3.104 Output current of N+1 level PD-PWM

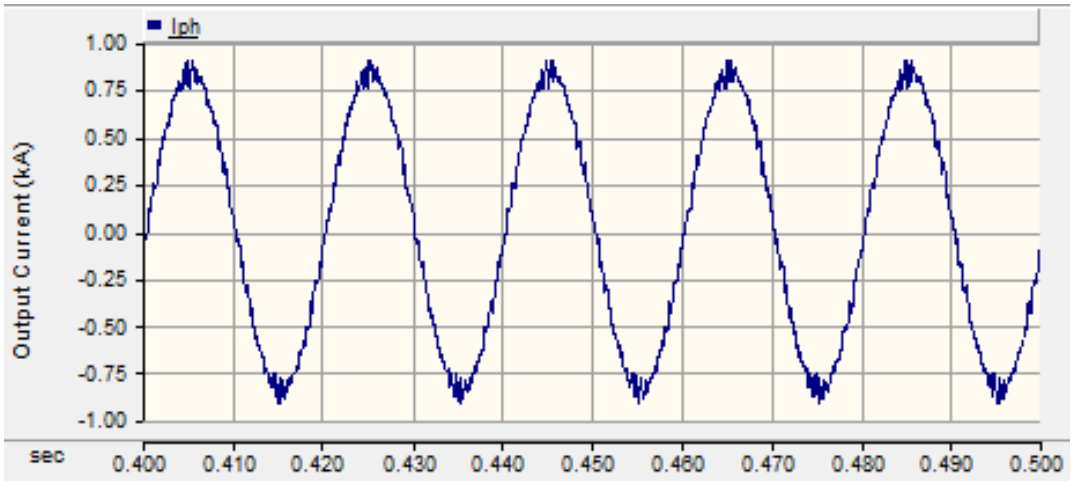


Figure 3.105 Output current of N+1 level APOD-PWM

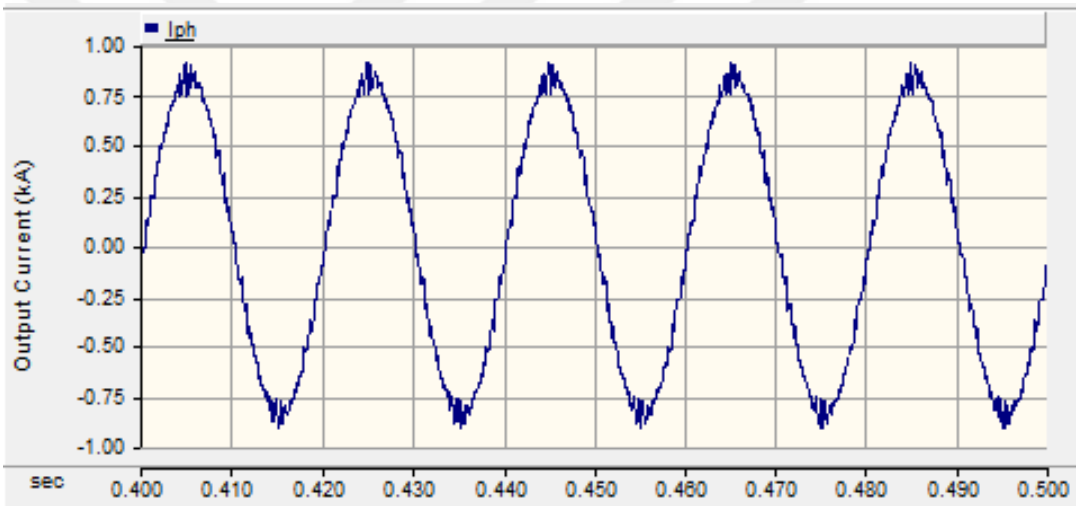


Figure 3.106 Output current of N+1 level PS-PWM

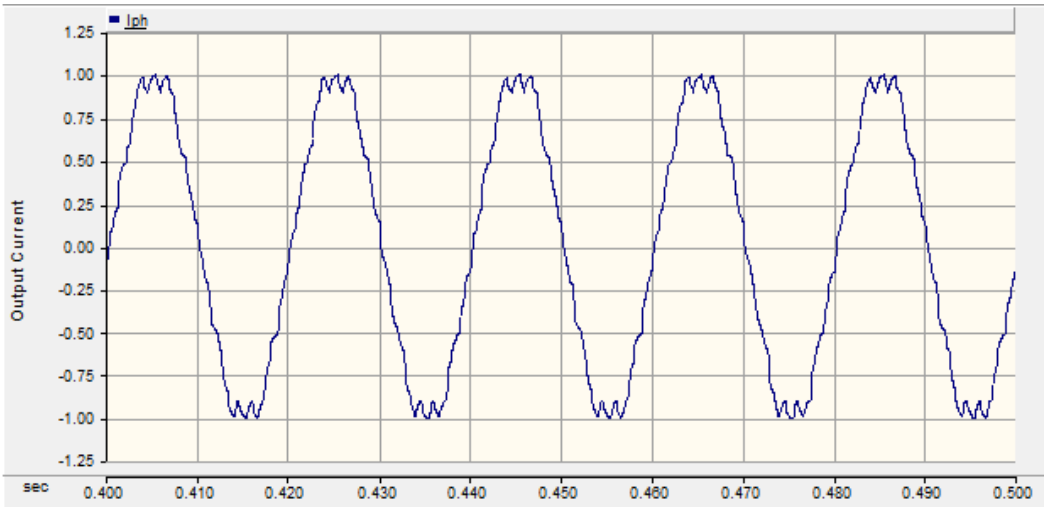


Figure 3.107 Output current of N+1 level NLC

3.6.1.4 Analysis of 2N+1 Level Line-to-line Voltage and Output Current in 6 Level MMC

In Figure 3.108 to Figure 3.111, output line voltages of 2N+1 level modulation methods are given. In Figure 3.112 to Figure 3.115, output line-to-line voltages of 2N+1 level modulation techniques are given. According to 2N+1 level line-to-line voltage, all scalar PWM switching methods give similar results. FFT analysis is done as shown in Figure 3.116 to Figure 3.119. Considering 2N+1 level switching case, modulation methods like PD, APOD and PS methods give similar performance analysis in terms of THD analysis about 6.28 % THD as shown in Table 3.4. When NLC method examined, THD is observed about 7.59 %. According to FFT analysis, dominant harmonics for level shifted PWM methods are centered almost twice of the carrier frequency. Although, taken into account for PS-PWM method, dominant harmonics are centered about twice of the number of carriers times the carrier frequency. The analysis of the individual harmonic distortion of the line-to-line output voltages is done. Therefore, harmonics which are dominant ones are centered sidebands of the twice of modulation frequency and obtained results are seen in Figure 3.120 to Figure 3.122. Dominant harmonics for NLC method are also shown in Figure 3.123.

Output current waveform is also investigated, all scalar PWM methods give the similar results about 1.29 % THD as shown in Figure 3.124 to Figure 3.126 and also NLC has nearly 5.12 % THD in the output current as illustrated in Figure 3.127.

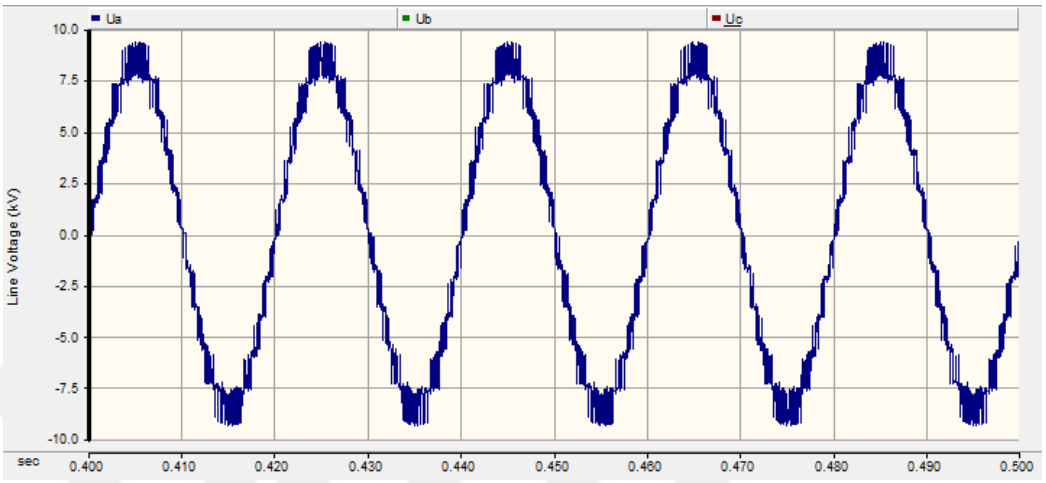


Figure 3.108 Output line voltage of 2N+1 level PD-PWM

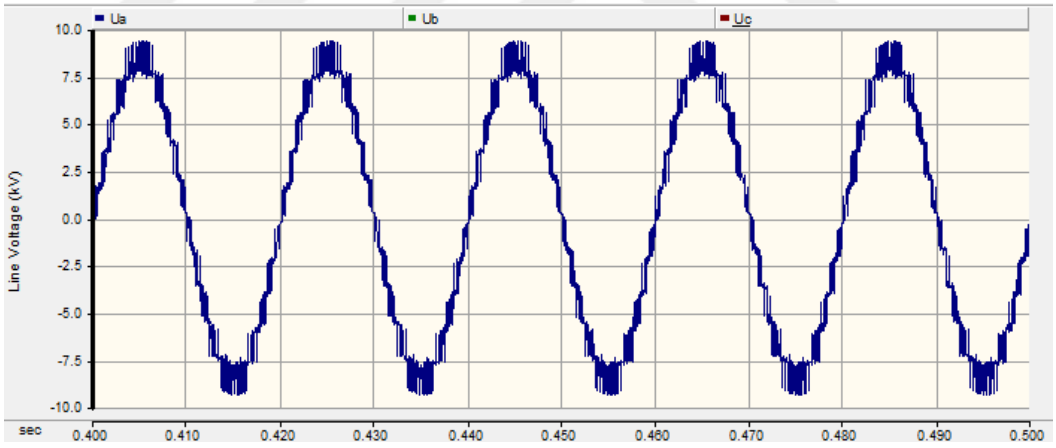


Figure 3.109 Output line voltage of 2N+1 level APOD-PWMs

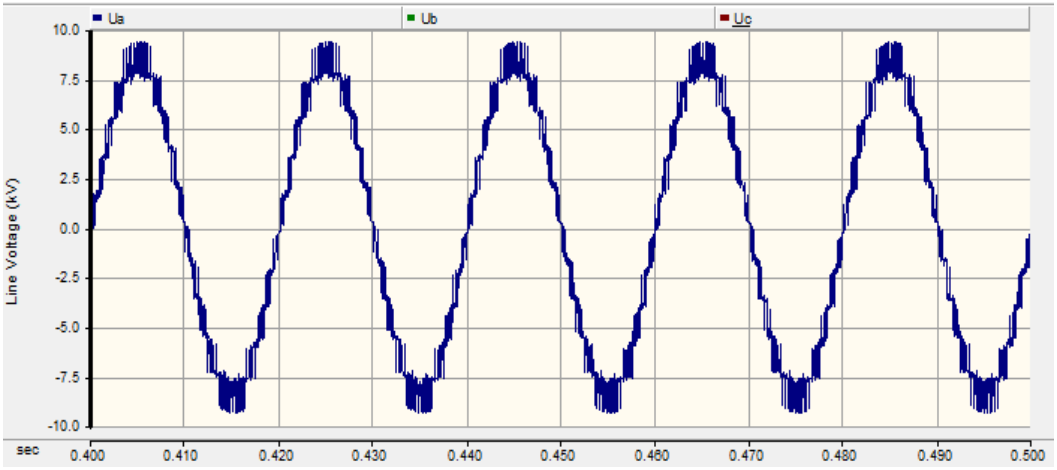


Figure 3.110 Output line voltage of 2N+1 level PS-PWM

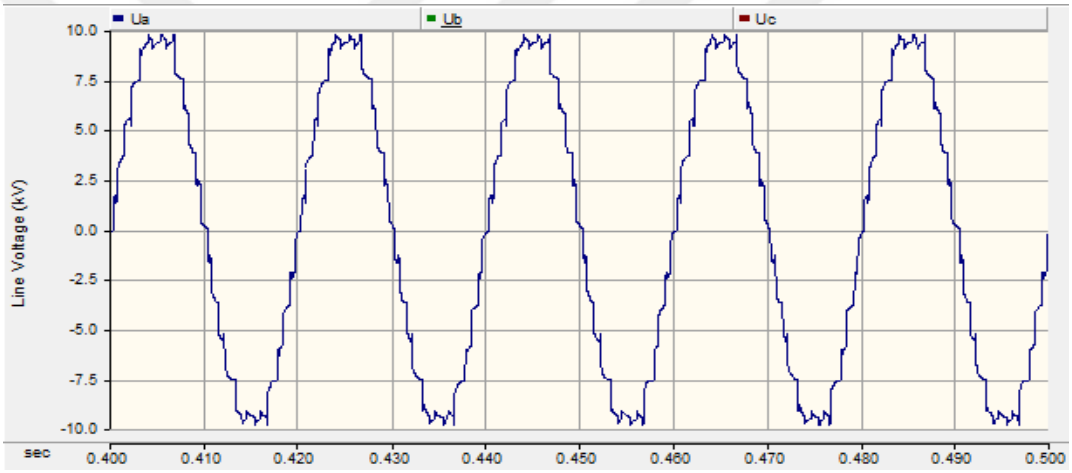


Figure 3.111 Output line voltage of 2N+1 level NLC

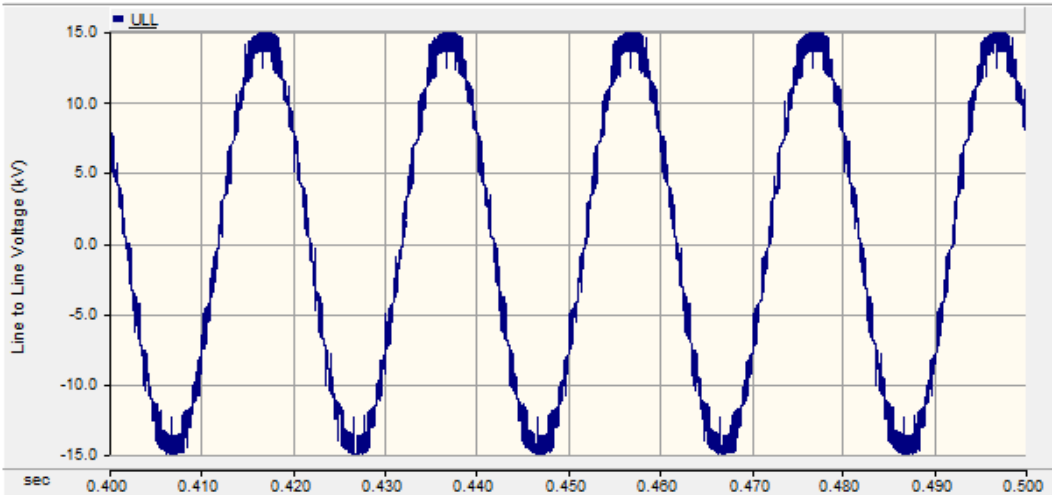


Figure 3.112 Output line-to-line voltage of 2N+1 level PD-PWM

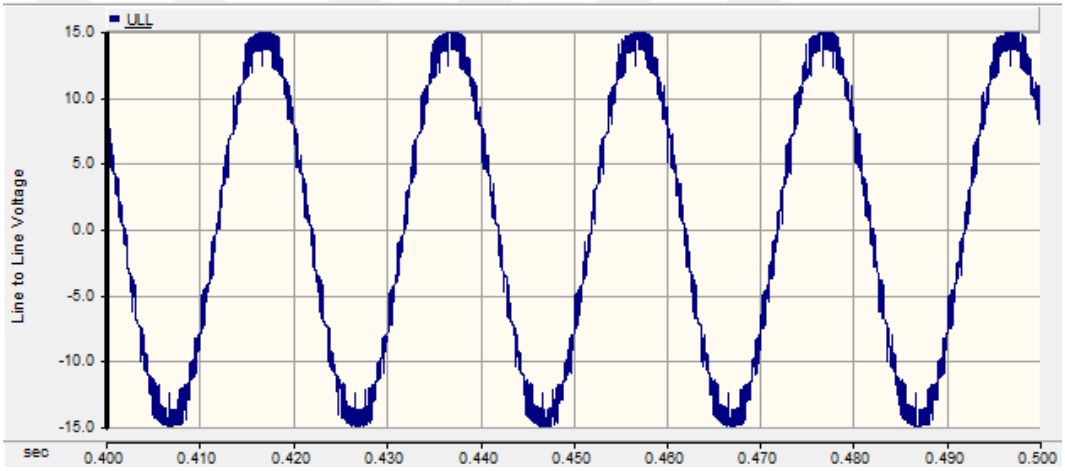


Figure 3.113 Output line-to-line voltage of 2N+1 level APOD-PWM

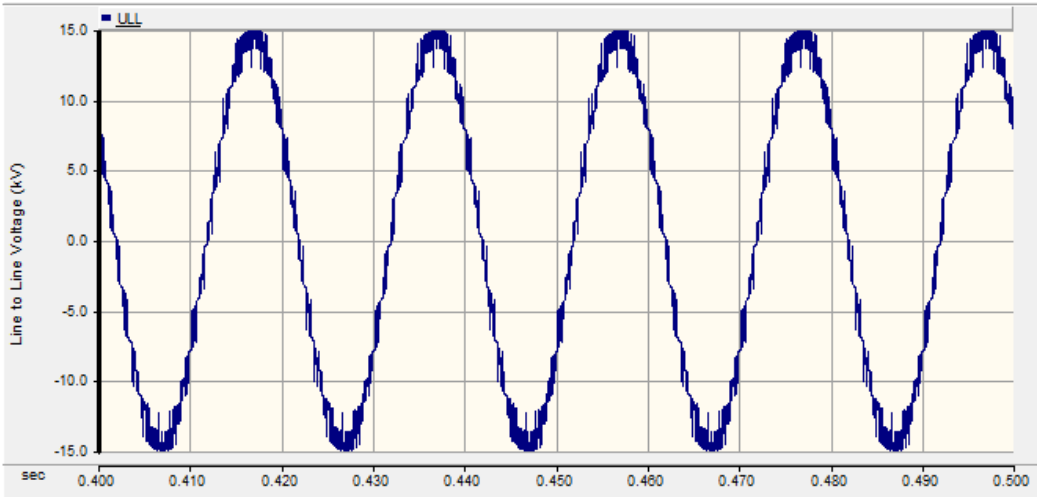


Figure 3.114 Output line-to-line voltage of 2N+1 level PS-PWM

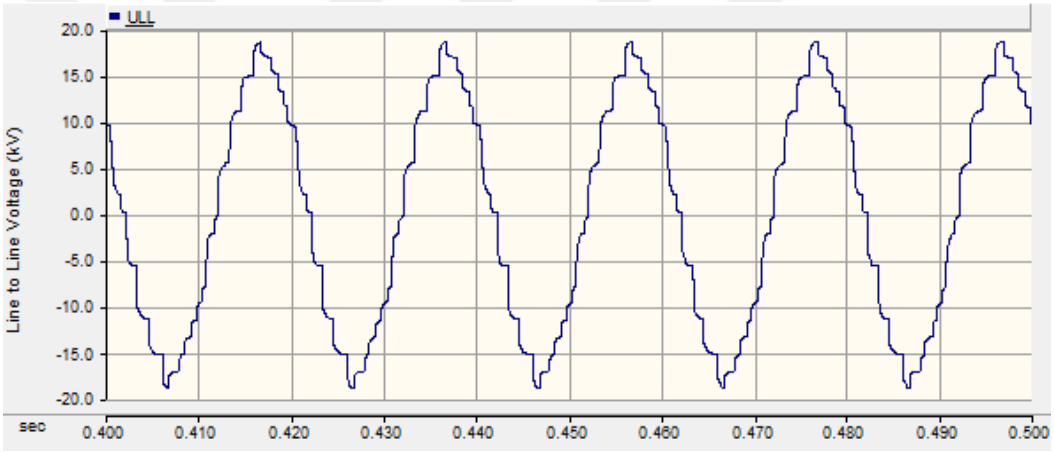


Figure 3.115 Output line-to-line voltage of 2N+1 level NLC

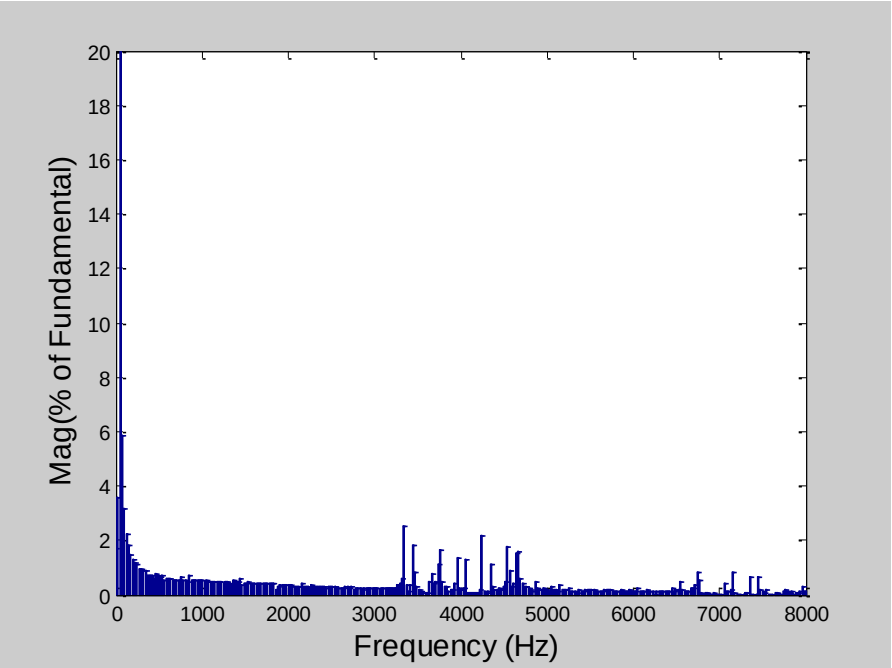


Figure 3.116 FFT analysis of the line-to-line voltage of 2N+1 level PD-PWM

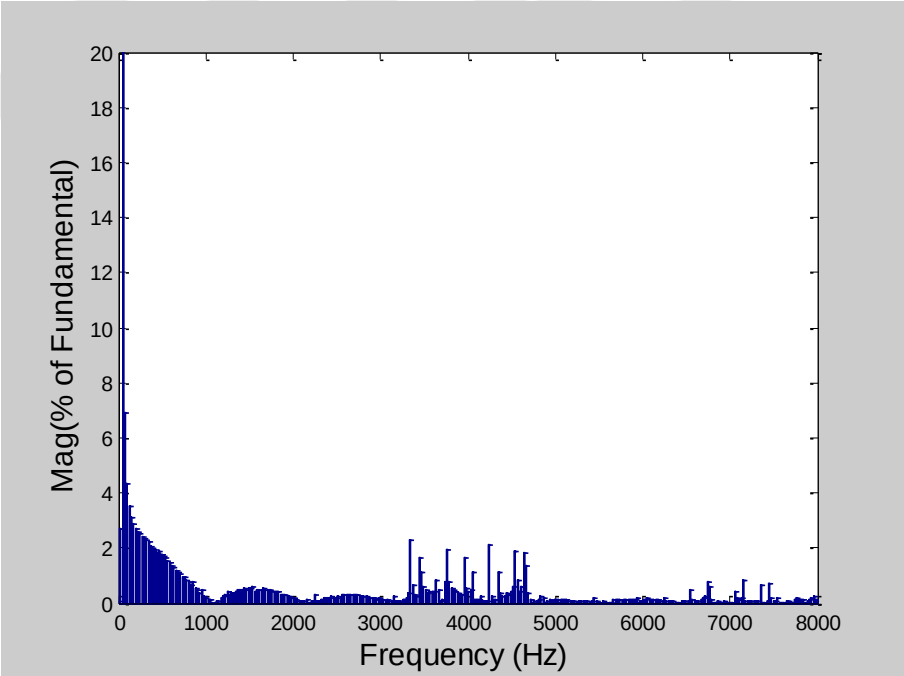


Figure 3.117 FFT analysis of the line-to-line voltage of 2N+1 level APOD-PWM

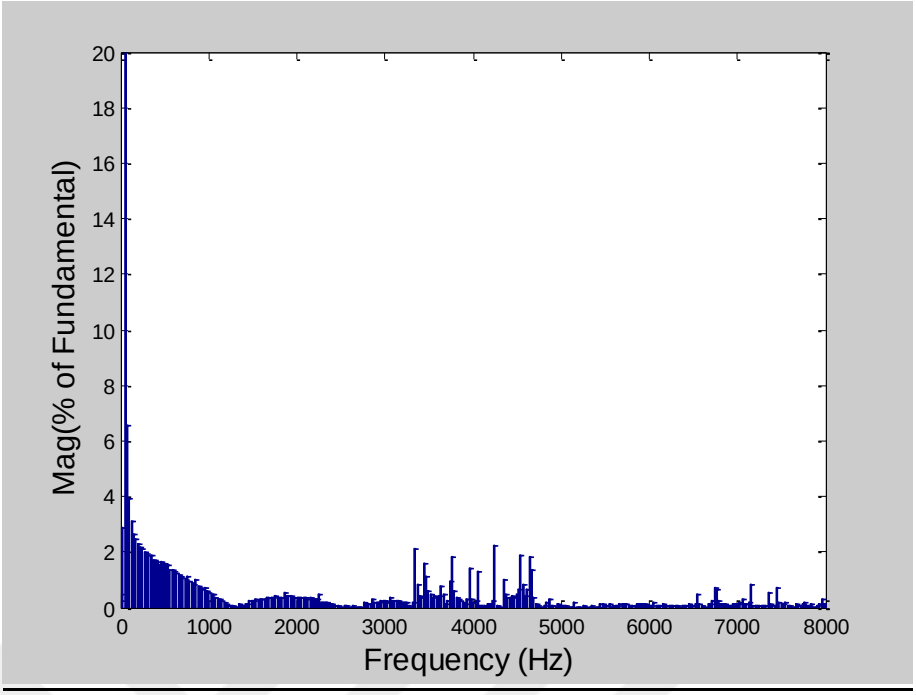


Figure 3.118 FFT analysis of the line-to-line voltage of 2N+1 level PS-PWM

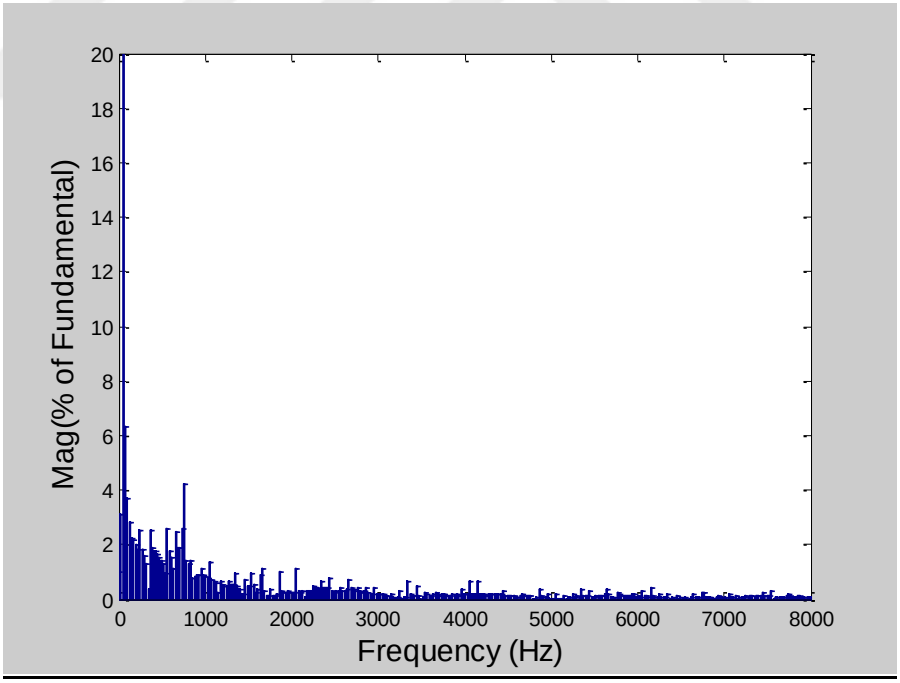


Figure 3.119 FFT analysis of the line-to-line voltage of 2N+1 level NLC

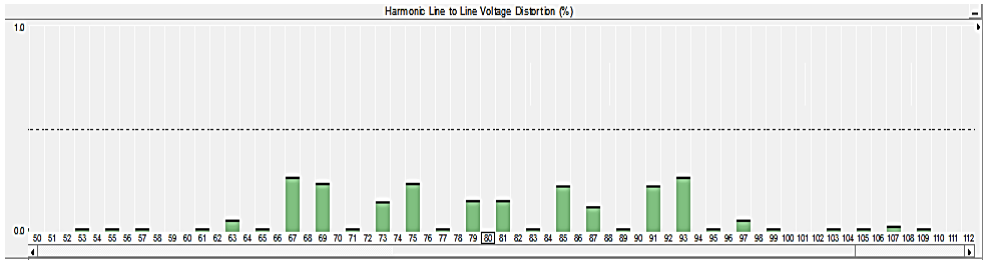


Figure 3.120 Individual harmonic distortion (%) of the line-to-line voltage of 2N+1 level PD-PWM

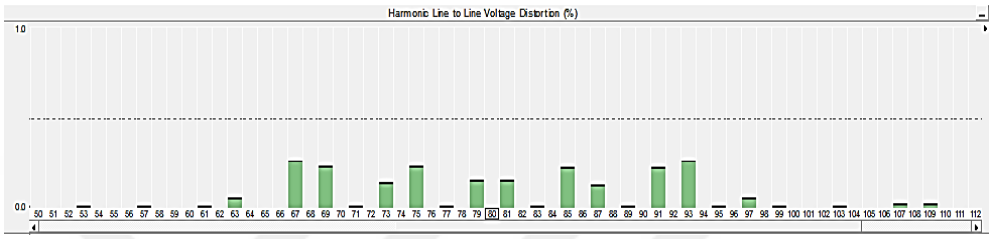


Figure 3.121 Individual harmonic distortion (%) of the line-to-line voltage of 2N+1 level APOD-PWM

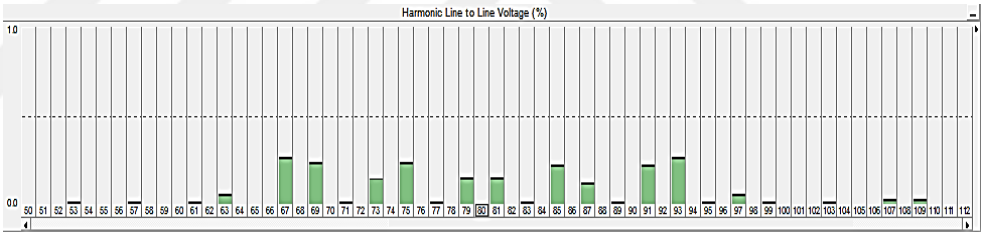


Figure 3.122 Individual harmonic distortion (%) of the line-to-line voltage of 2N+1 level PS-PWM

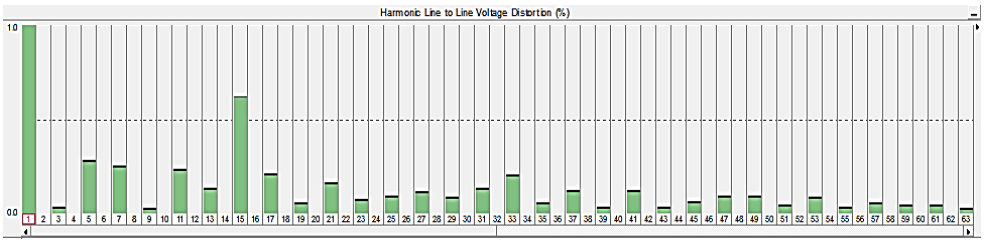


Figure 3.123 Individual harmonic distortion (%) of the line-to-line voltage of 2N+1 level NLC

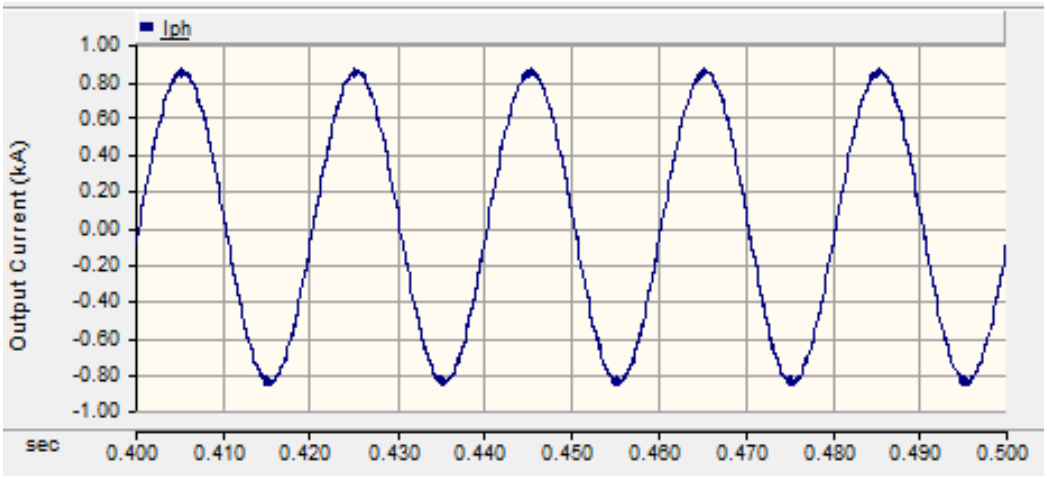


Figure 3.124 Output current of 2N+1 level PD-PWM

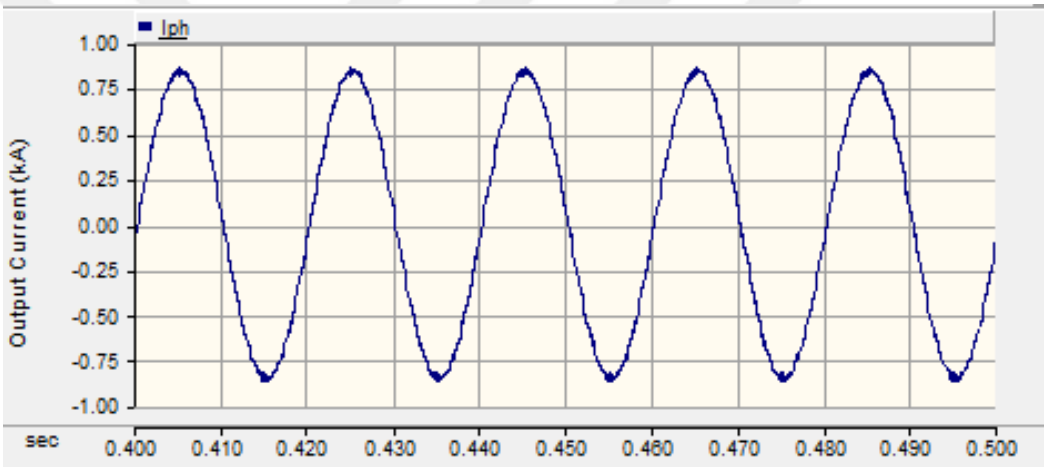


Figure 3.125 Output current of 2N+1 level APOD-PWM

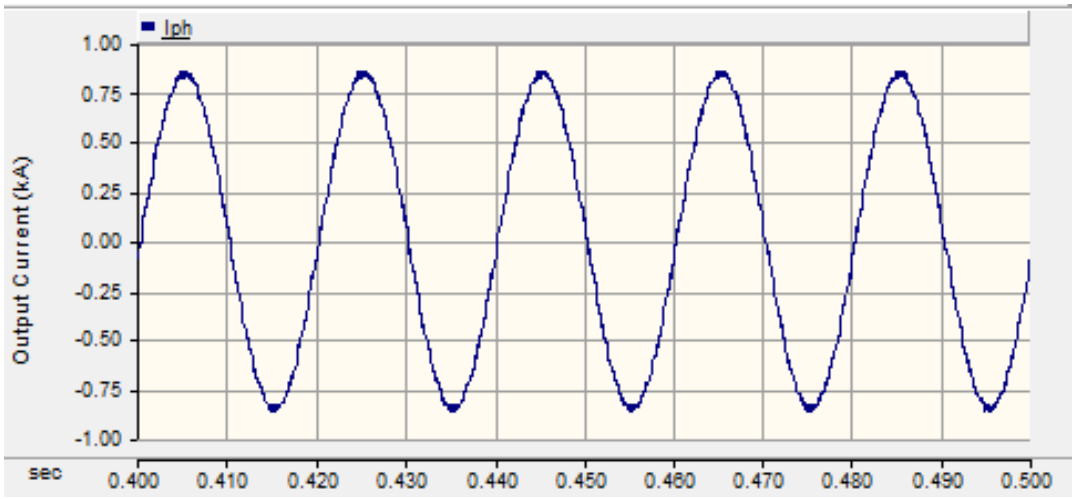


Figure 3.126 Output current of 2N+1 level PS-PWM

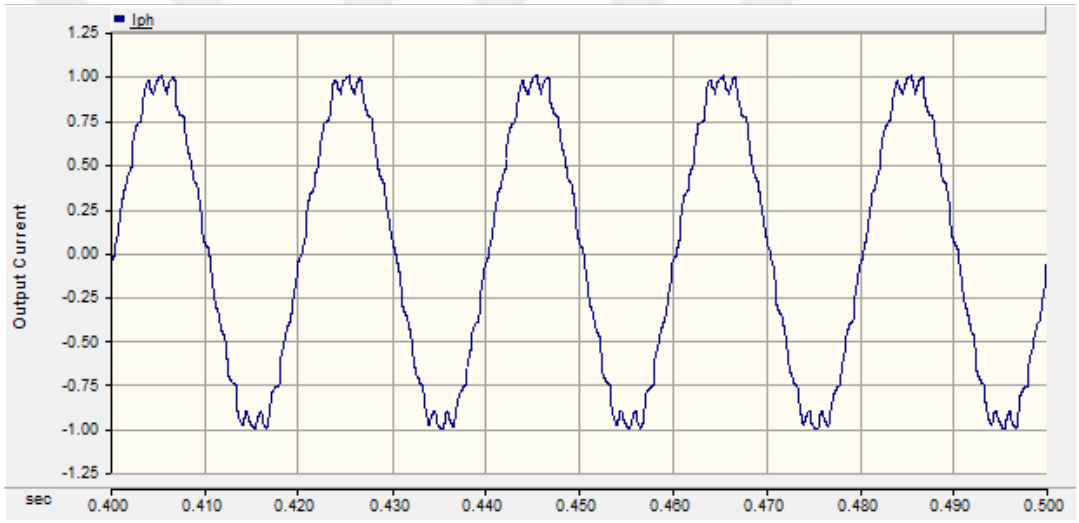


Figure 3.127 Output current of 2N+1 level NLC

In this chapter, modulation methods are investigated in detail for 5 level and 6 level multilevel modular converter. The comparing is done without using any control and submodule capacitor voltage balancing algorithm. Scalar PWM methods are compared and also NLC method is discussed for N+1 level and 2N+1 level switching. For 5 level MMC, results regarding to line-to-line output voltage are shown in Table 3.2. Additionally, output current analysis is summarized as shown in Table 3.3 for 5 level MMC. All of the results are given in Table 3.4 and Table 3.5 for

line-to-line output voltage and the current, respectively. The results are listed as follows;

1. In terms of total harmonic distortion, better results are obtained for 6 level MMC both line-to-line output voltage and output current waveform analysis.
2. Considering N+1 level case, PD-PWM has lower THD values for line-to-line output voltage and output current waveform analysis
3. For 2N+1 level case, all scalar PWM methods give the similar results
4. Locations of dominant harmonics for N+1 level and 2N+1 level line-to-line output voltages are identical to each other for LS and PS methods when used equal switching frequency in a phase leg also shown in Table 3.1
5. To discuss the individual harmonic distortion % THD of the line-to-line output voltage, modulation frequency value is calculated according to Equation (3.29), frequency of the carrier signal is divided by the fundamental frequency and amplitude modulation index value is proportional to the deviation between the carrier and reference waveform as in Equation (3.30) [71].

$$mf = \frac{fcr}{fm} \tag{3.29}$$

$$ma = \frac{Dev(ref)}{Dev(cr)} \tag{3.30}$$

In here, ma and mf represent the amplitude modulation index and frequency modulation index, respectively. Additionally, fcr and fm indicate the frequency of the carrier signal and fundamental frequency, respectively.

Table 3.1 Locations of output line-to-line voltage harmonics in scalar PWM methods

	N+1 Level V_{L-L}	2N+1 Level V_{L-L}
LS (PD,POD and APOD)	f_c	$2xf_c$
PS	Nxf_c	$2Nxf_c$
NLC	f_m	f_m

Table 3.2 Voltage THD comparison of all modulation methods in 5 level MMC

		ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)
		0.9	2000	0.9	2000	0.9	2000	0.9	500	0.9	50
Voltage	**Level**	**PD-PWM (THD %)**		**POD-PWM (THD %)**		**APOD-PWM (THD %)**		**PS-PWM (THD %)**		**NLC (THD %)**	
Line-to-Line Voltage	**N+1**	9.39		19.61		18.90		18.79		11.11	
	2N+1	6.77		6.77		6.77		6.77		5.47	

Table 3.3 Current THD comparison of all modulation methods in 5 level MMC

		ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)
		0.9	2000	0.9	2000	0.9	2000	0.9	500	0.9	50
Current	**Level**	**PD-PWM (THD %)**		**POD-PWM (THD %)**		**APOD-PWM (THD %)**		**PS-PWM (THD %)**		**NLC (THD %)**	
Output Current	**N+1**	2.64		6.77		6.56		6.51		8.73	
	2N+1	1.41		1.41		1.41		1.41		3.92	

Table 3.4 Voltage THD comparison of all modulation methods in 6 level MMC

		ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)
		0.9	2000	0.9	2000	0.9	2000	0.9	400	0.9	50
Voltage	**Level**	**PD-PWM (THD %)**		**POD-PWM (THD %)**		**APOD-PWM (THD %)**		**PS-PWM (THD %)**		**NLC (THD %)**	
Line-to-Line Voltage	**N+1**	8.00		-		12.19		12.19		8.07	
	2N+1	6.28		-		6.28		6.28		7.59	

Table 3.5 Current THD comparison of all modulation methods in 6 level MMC

		ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)	ma	fc(Hz)
		0.9	2000	0.9	2000	0.9	2000	0.9	400	0.9	50
Current	**Level**	**PD-PWM (THD %)**		**POD-PWM (THD %)**		**APOD-PWM (THD %)**		**PS-PWM (THD %)**		**NLC (THD %)**	
Output Current	**N+1**	2.26		-		4.00		4.00		5.96	
	2N+1	1.29		-		1.29		1.29		5.12	

CHAPTER 4

PROPOSED CONTROLLER STRUCTURES for MODELED MMC-STATCOM

Proposed control parts belonging to PS-PWM based control method and direct modulation based sort and selection method are discussed in this section. The whole control parts related to direct modulation are shown in Figure 4.1, and all of them will be discussed in following chapter**.** Additionally, PS-PWM based control method will be explained thoroughly and also illustrated in Figure 4.2.

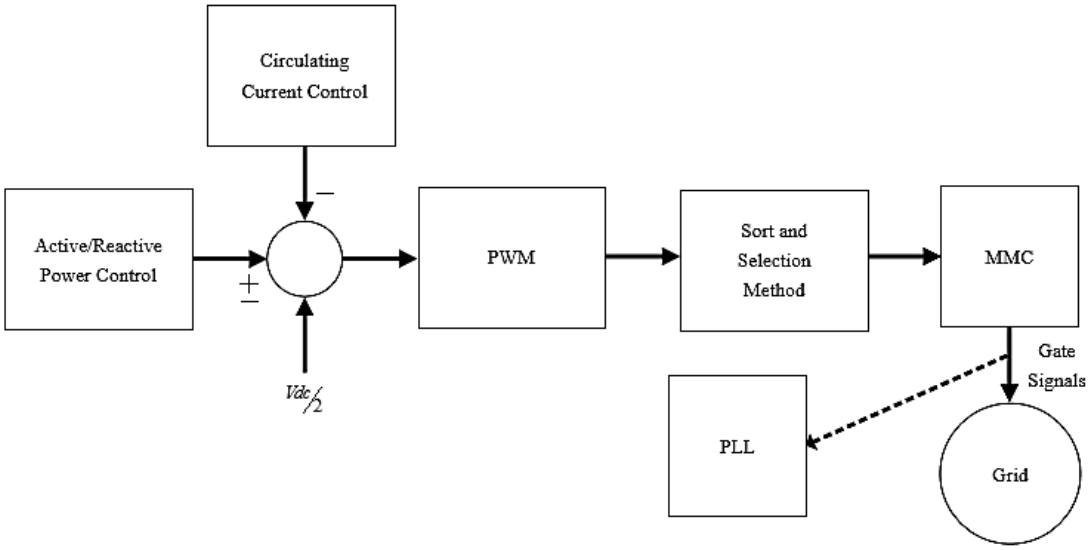


Figure 4.1 Overall control parts for direct modulation based sort and selection method

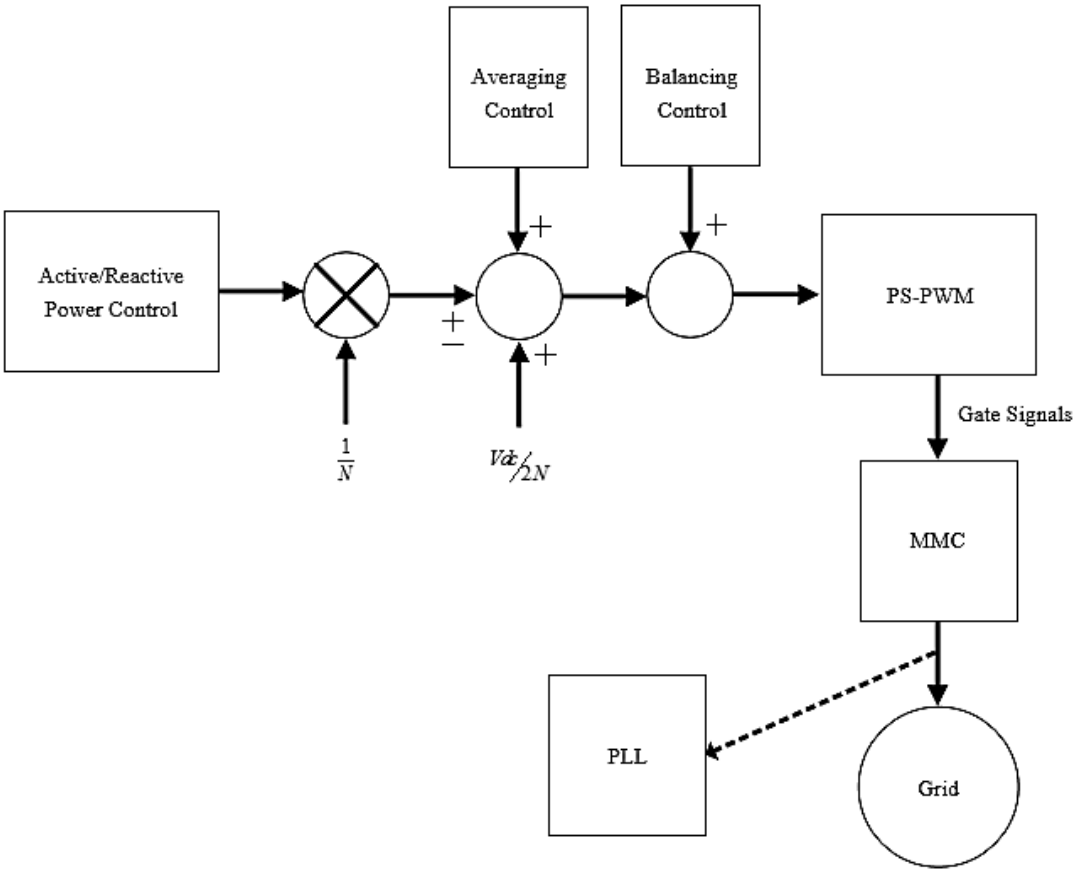
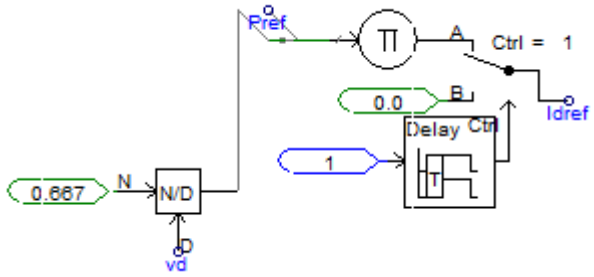


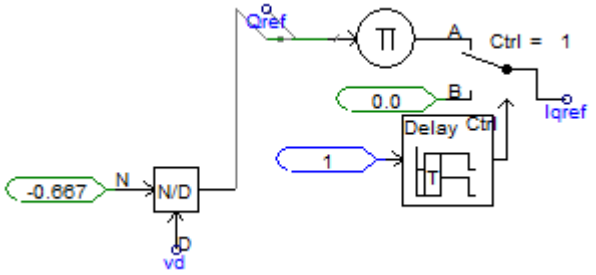
Figure 4.2 Overall control parts for PS-PWM based control method

4.1 Active and Reactive Power Control of the MMC

The Half-bridge cell (double star chopper cell)[30] of the MMC behaves as a rectifier when $p > 0$, an inverter when $p < 0$, an inductor when $q > 0$, and a capacitor when $q < 0$ [30]. In statcom applications, $p = 0$, $q > 0$ or $q < 0$ conditions are considered and both inductive and capacitive modes are implemented to the outer loop control part. Application of the outer loop control part in PSCAD environment is shown in Figure 4.3. In here, P_{ref} and Q_{ref} represent the reference active and reactive power. v_d and v_q are indicated the d and q components of the grid voltage. i_d^* and i_q^* are pointed out the reference as active and reactive currents, respectively.



(a)



(b)

Figure 4.3 PSCAD block of the outer loop control part, (a) active power, (b) reactive power

Regarding to outer loop control part, Delay block is preferred for two power control blocks and the function of this block is to eliminate overcurrents. Accordingly, switching is not applied to IGBTs during 0.1s to charge the dc capacitors through the diodes [57].

Active and reactive power control diagram of the MMC are divided into two groups as outer loop control part and inner loop control part. Inner loop control structure is designed to be different for both PS-PWM based control method and direct modulation based control methods as illustrated in Figure 4.4 and Figure 4.5, respectively. The main purpose of the inner loop control structure is current control.

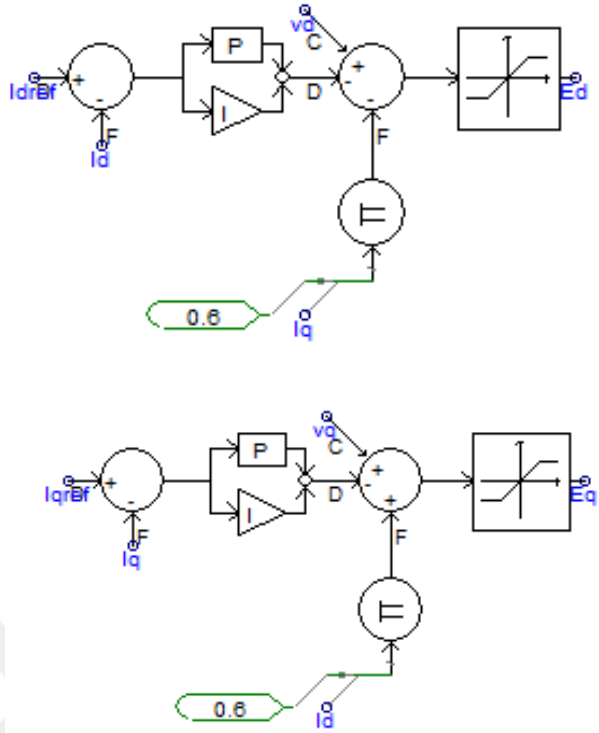


Figure 4.4 Proposed inner loop control structure for PS-PWM based modulation in PSCAD environment

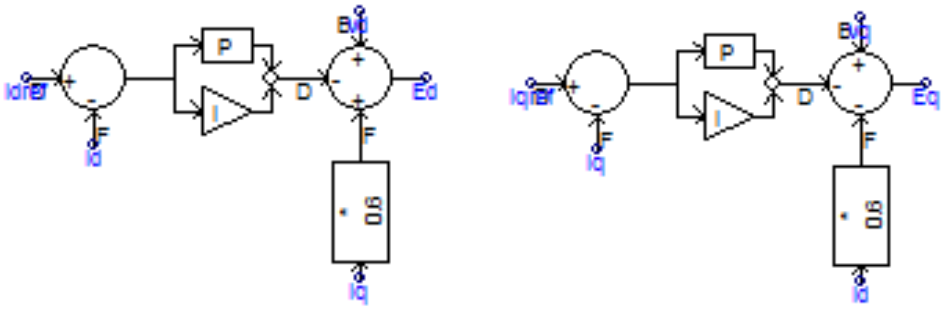


Figure 4.5 Proposed inner loop control structure for direct modulation based control method in PSCAD environment

4.2 DC Link Control of the MMC

DC link voltage control in PSCAD environment is illustrated in Figure 4.6. DC link control is implemented to the active current control component. In here, measured DC link voltage is compared with a reference DC link voltage. DC link voltage is calculated as 19kV. Additionally, PI parameters of the DC link control are taken as 0.8 for K_P, 10 for K_I.

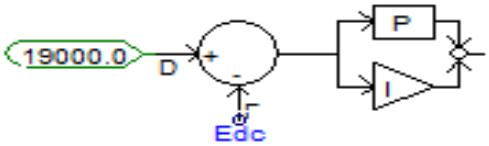


Figure 4.6 PSCAD implementation of the DC link voltage control

4.3 Capacitor Voltage Balancing Methods

Direct modulation based sort and selection method and Phase-shifted based control method are the proposed capacitor voltage balancing methods for the MMC-STATCOM applications and also depicted in Figure 4.7. Each method is discussed in following sections in detail.

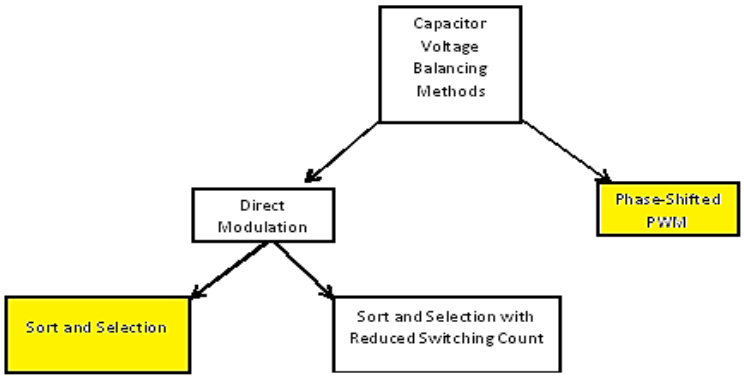


Figure 4.7 Capacitor Voltage Balancing Methods

4.3.1 Direct Modulation Based Capacitor Voltage Balancing Structure

4.3.1.1 Sort and Selection Method

Each part of the sort and selection method is explained as in Figure 4.8. Additionally, PSCAD environment of the sort and selection method is given in Figure 4.9. While formed sort and selection method blocks, reference [59] is utilized. In Figure 4.8, submodule capacitor voltages are sampled and kept constant at value V_{dc}/N in the first block. Second block is regarding to sorting of all the submodule capacitor voltages ascending or descending order in a phase leg. Sorted submodule voltages are selected regarding to the arm current direction in the third block. Finally, selected submodules are sent to the last block in order to produce switching states for the SMs.

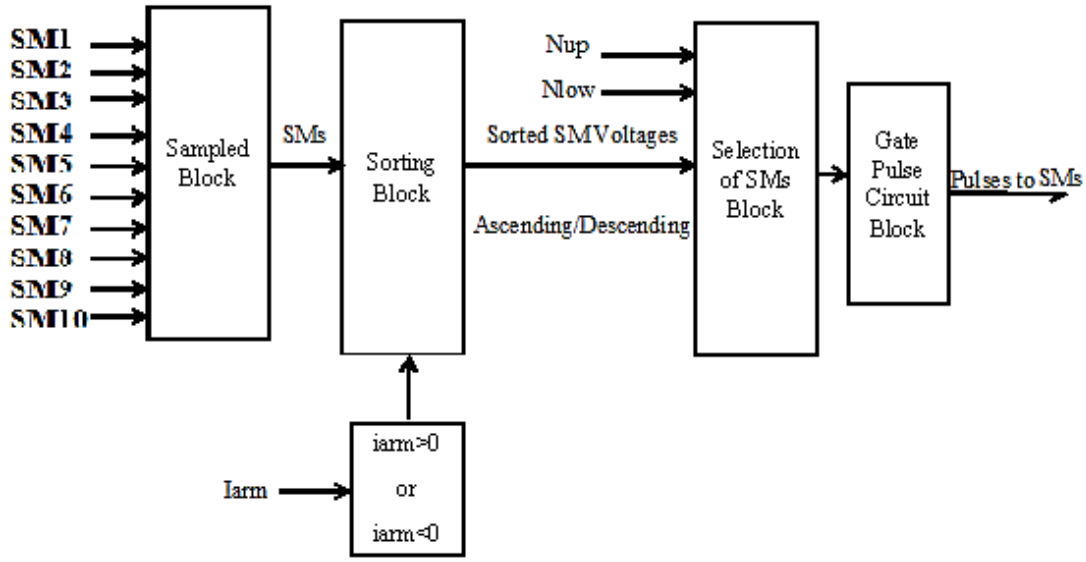


Figure 4.8 Each part of the sort and selection method [61]

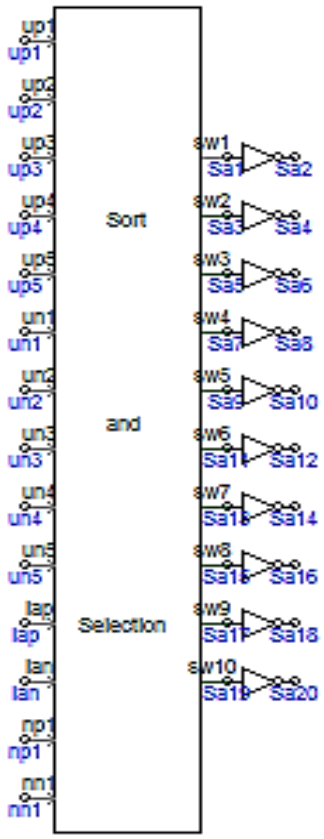


Figure 4.9 Application of the sort and selection method in PSCAD environment

4.3.2 Phase-Shifted PWM Based Capacitor Voltage Balancing Structures

Proposed capacitor voltage balancing structures regarding to Phase-shifted PWM based control method are classified as averaging control and individual balancing control. Each control structure is discussed in following sections.

4.3.2.1 Averaging Control Structure

Averaging control structure is composed of the voltage major loop and the current minor loop as in given Figure 3.9. In this structure, circulating current control is included. Thus, in order to minimize the circulating current drawbacks, controller gains are selected appropriately. PSCAD implementation of the averaging control part is demonstrated in Figure 4.10. PI parameters are also represented in Table 4.1.

Table 4.1 PI parameters of the averaging control structure

Proportional gain of the averaging control part	K_1	0.3 A/V
Integral gain of the averaging control part	K_2	150 A/(V-s)
Proportional gain of the current control	K_3	1.5 V/A
Integral gain of the current control	K_4	150 V/(A-s)

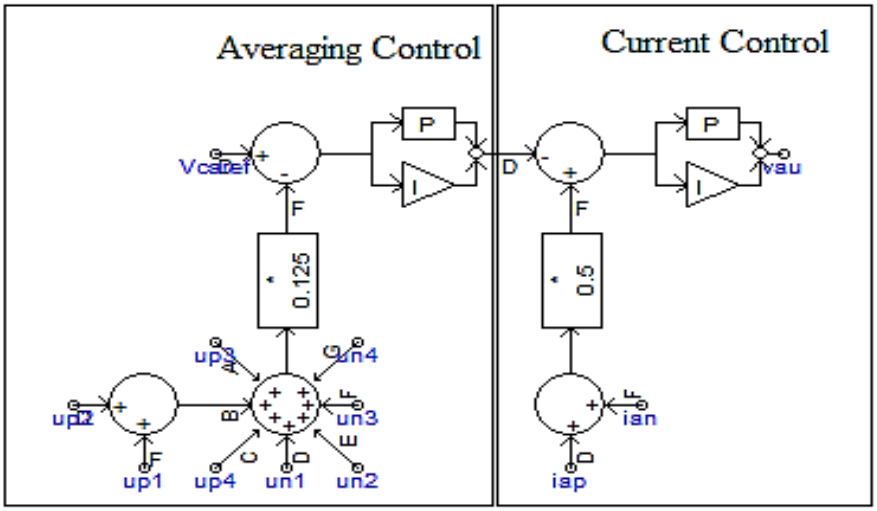


Figure 4.10 PSCAD implementation of the averaging control structure

4.3.2.2 Individual Balancing Control Structure

Individual balancing control structure has to be formed in each submodule. The aim of this method is that depending on the arm current direction to keep the individual capacitor voltage at desired value.

When the reference voltage of the submodule capacitor value is higher than the real submodule capacitor value, the arm current charges the capacitor. Thus, the energy should be transferred from the DC link to the submodule capacitor. When the arm current has negative polarity, submodule capacitor will be discharged due to low reference submodule capacitor value. PSCAD implementations of the individual

balancing control structure and determination of the arm current polarity for both arms are seen in Figure 4.11.

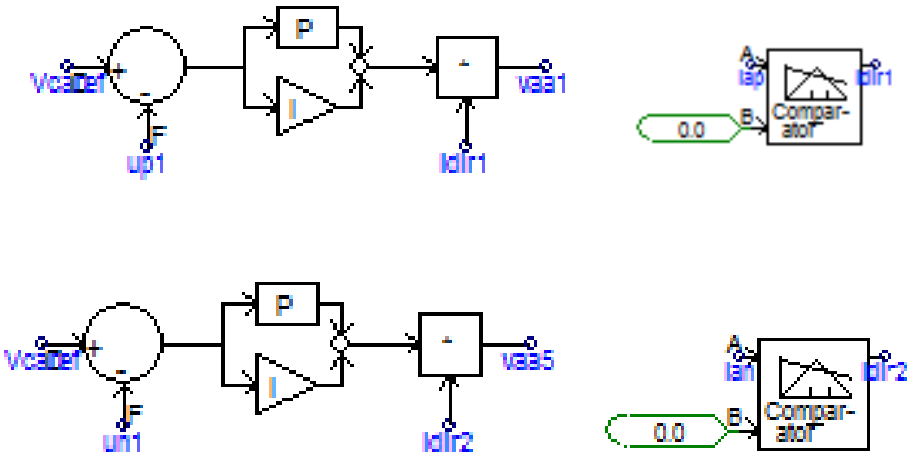


Figure 4.11 Individual Balancing Control blocks at left and determination of the arm current polarity at right

In individual balancing control blocks, proportional gain of the PI blocks are taken as 0.01 for both arms of the MMC.

4.4 Proposed Modulation Methods

Scalar PWM methods are known as Level-shift and Phase-shift methods in high frequency switching applications. Among the level-shifted PWM methods, PD-PWM method is preferred due to better harmonic success and Phase-shifted carriers are handled for the MMC-STATCOM applications as shown in Figure 4.12.

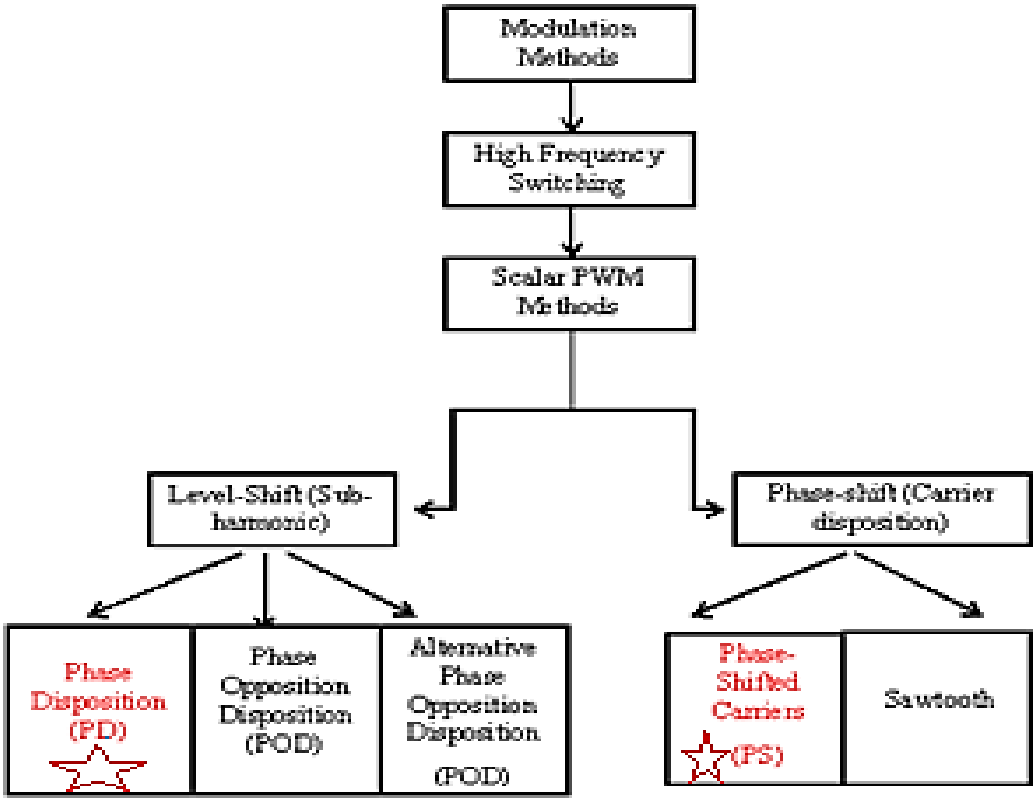


Figure 4.12 Proposed modulation methods for MMC-STATCOM

4.4.1 Phase-Shifted PWM Method

2N+1 level Phase-shifted PWM method is proposed in MMC-STATCOM applications. PSCAD implementation of the 2N+1 level Phase-shifted PWM carriers are illustrated in Figure 4.13. One carrier for each submodule is used in the converter arm for phase-shifted method.

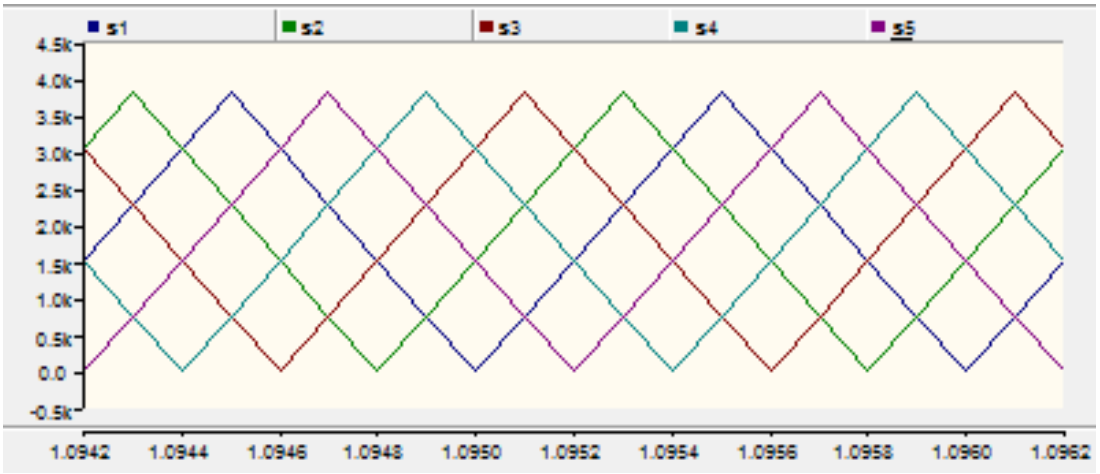


Figure 4.13 PSCAD implementation of the 2N+1 level carrier sets for PS-PWM method

In 2N+1 level switching, converter equivalent switching frequency, $fcsw, eq$ is shown in Equation (4.1), in which fc represents the frequency of the triangular carriers and N indicates the number of carriers.

$$fcsw, eq = 2Nfc \quad \textbf{(4.1)}$$

Parameters belonging to the PS-PWM carrier waveform are represented as in Table 4.2.

Table 4.2 Parameters of the PS-PWM based carrier waveform

Switching level	2N+1- Level
***fc* (carrier frequency) Hz**	1000 Hz
***fsw* (switching frequency) Hz**	$fsw, eq = 2Nfc = 10000$ Hz
ma(Modulation Amplitude)	0.9
mf (Modulation frequency)	20

4.4.2 Phase Disposition PWM Method (PD-PWM)

Considering N+1 level and 2N+1 level PD-PWM method, 2N+1 level PD-PWM application is preferred in direct modulation based capacitor voltage balancing application due to better line-to-line output voltage harmonic performance. 2N+1 level PD-PWM carriers are used as shown in Figure 4.14. Considering 2N+1 level switching, carrier sets belonging to upper and lower arm have 0 degree phase difference between each other. Parameters belonging to the PD-PWM carrier waveform are given as in Table 4.3.

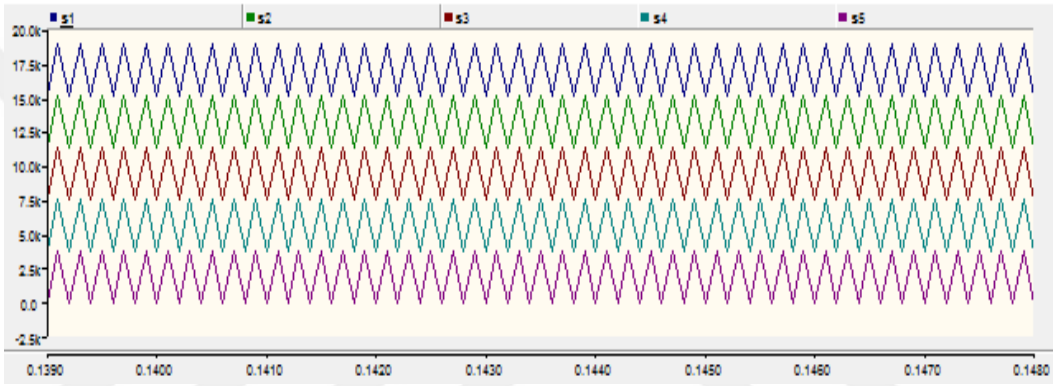


Figure 4.14 2N+1 level PD-PWM carrier sets

Table 4.3 Parameters of the PD-PWM carrier waveform

Switching level	2N+1- Level
***fc* (carrier frequency) Hz**	5000 Hz
***fsw* (switching frequency) Hz**	$fsw, eq = 2fc = 10000$ Hz
ma(Modulation Amplitude)	0.9
mf (Modulation frequency)	20

CHAPTER 5

MODELING OF MODULAR MULTILEVEL CONVERTER BASED STATCOM

5.1 VSC Based STATCOM System

The static synchronous compensator (STATCOM) is a shunt connected reactive compensator which can produce or absorb reactive power. One-line diagram of the STATCOM is illustrated in Figure 5.1. In here, coupling transformer, VSC, leakage inductor and DC capacitor are included to the system.

Step-down transformer is used to connect the STATCOM to the AC grid. VSC is the most crucial part of the STATCOM system. The main function of this converter is to generate AC voltage with a low harmonic distortion from a DC capacitor. Leakage inductor provides independent control of the powers which are active and reactive. The last one is DC capacitor works as an energy storage apparatus that gives the DC voltage to the system.

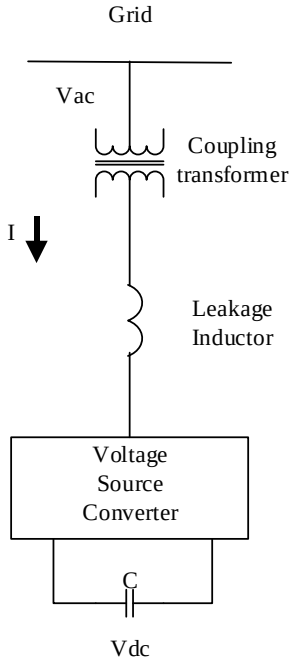


Figure 5.1 One-line diagram of the STATCOM system [60]

5.2 Modeling of MMC-STATCOM

Power circuit structure of the three-phase MMC-STATCOM is illustrated in Figure 5.2.

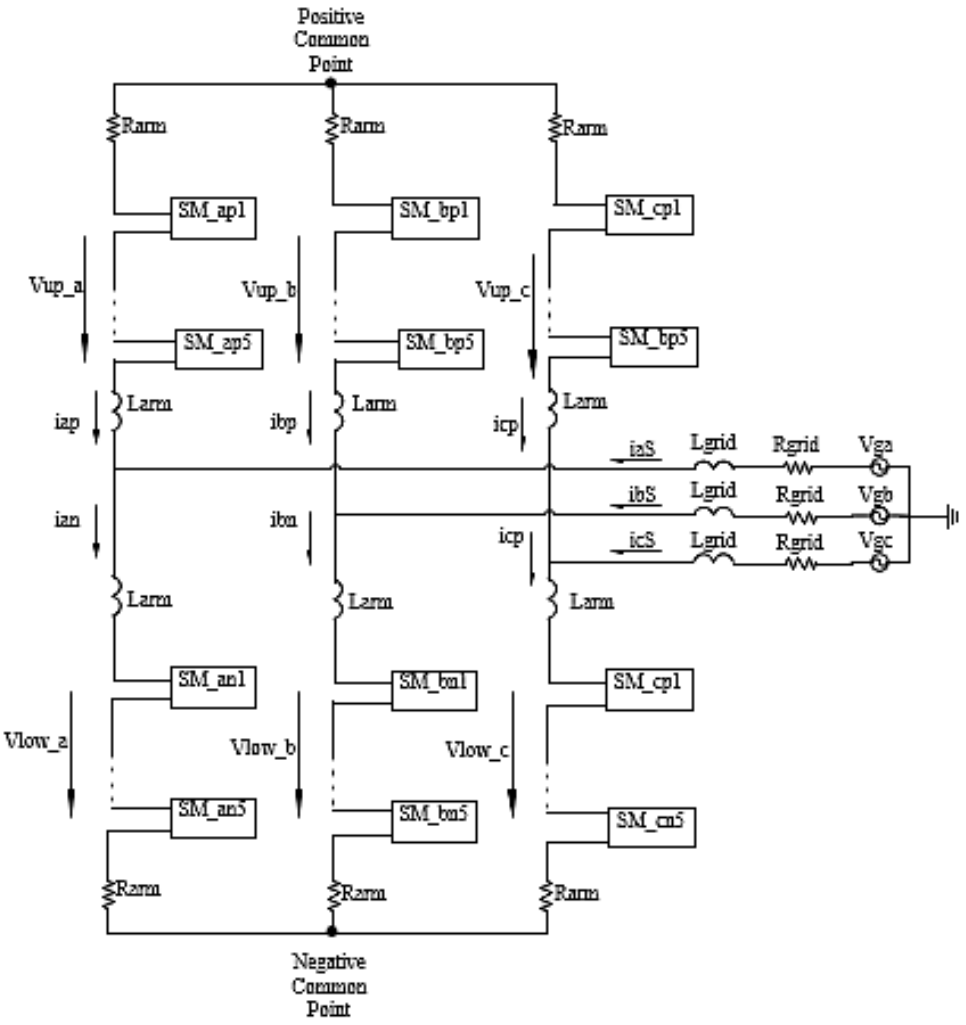


Figure 5.2 Power circuit structure of the three-phase MMC-STATCOM

The MMC-STATCOM is consisted of upper and lower arm converters with half-bridge based submodule structure. Each arm composed of 5 submodules and 6 level (11 level in line-to-line) is produced in a phase leg. The conditions of the common points are floating due to absence of DC Source. Thus; System works as a static synchronous compensator.

5.3 Working Principle of MMC-STATCOM

Single-phase equivalent circuit structure of the MMC-STATCOM is seen in Figure 5.3.

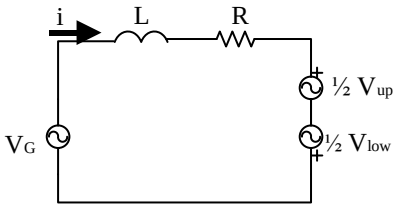


Figure 5.3 Single-phase equivalent circuit structure of the MMC-STATCOM [12]

In here, R defines the total resistance of the system and L defines the total inductance of the system between the grid side and output side of the converter as indicated in Equations (5.1) and (5.2). Moreover, V_G means grid voltage and $V_{up,}V_{low}$ represent the arms voltage of the converter. i indicates the current received by the MMC-STATCOM.

$$L = \frac{L_{arm}}{2} + L_{grid} \tag{5.1}$$

$$R = \frac{R_{arm}}{2} + R_{grid} \tag{5.2}$$

Considering an ideal STATCOM system, active power should be zero and the current behaves reactive. Thus, active and reactive power capacity of the STATCOM can be defined as in Equations (5.3) and (5.4).

$$P_{ST} = 0 \tag{5.3}$$

$$Q_{ST} \cong V_G \frac{V_{G-}V_{ST}}{X} \tag{5.4}$$

According to circuit structure of the MMC-STATCOM, the active and reactive power exchange between the grid and MMC-STATCOM can be controlled

depending on the phase and magnitude of the output voltage, ($\frac{V_{low} - V_{up}}{2}$). When the amplitude of the output voltage is greater than the Grid voltage, (V_G), the current direction will be from MMC-STATCOM to Grid side as a leading reactive current and STATCOM releases capacitive reactive power to the AC grid. However, when the amplitude of the output voltage is lower than the grid voltage, the current direction will be from grid side to MMC-STATCOM as a lagging reactive current. In this case, STATCOM absorbs inductive reactive power from the AC grid [12]. There will be no reactive power exchange when the amplitude of the output voltage is equivalent to the grid side voltage.

5.4 Simulation Studies And Performance Comparison Analysis In MMC-STATCOM

5.4.1 Overview of the Simulated System

DC/AC, ± 5 MVAR, 10.5 kV, is handled for the simulated MMC-STATCOM system. Power circuit structure of the system is depicted in Figure 5.4 and the single line diagram of the proposed system is given in Figure 5.5. MMC-STATCOM circuit parameters are also given in Table 5.2. Static and dynamic modes of the MMC-STATCOM are analyzed thoroughly in following sections.

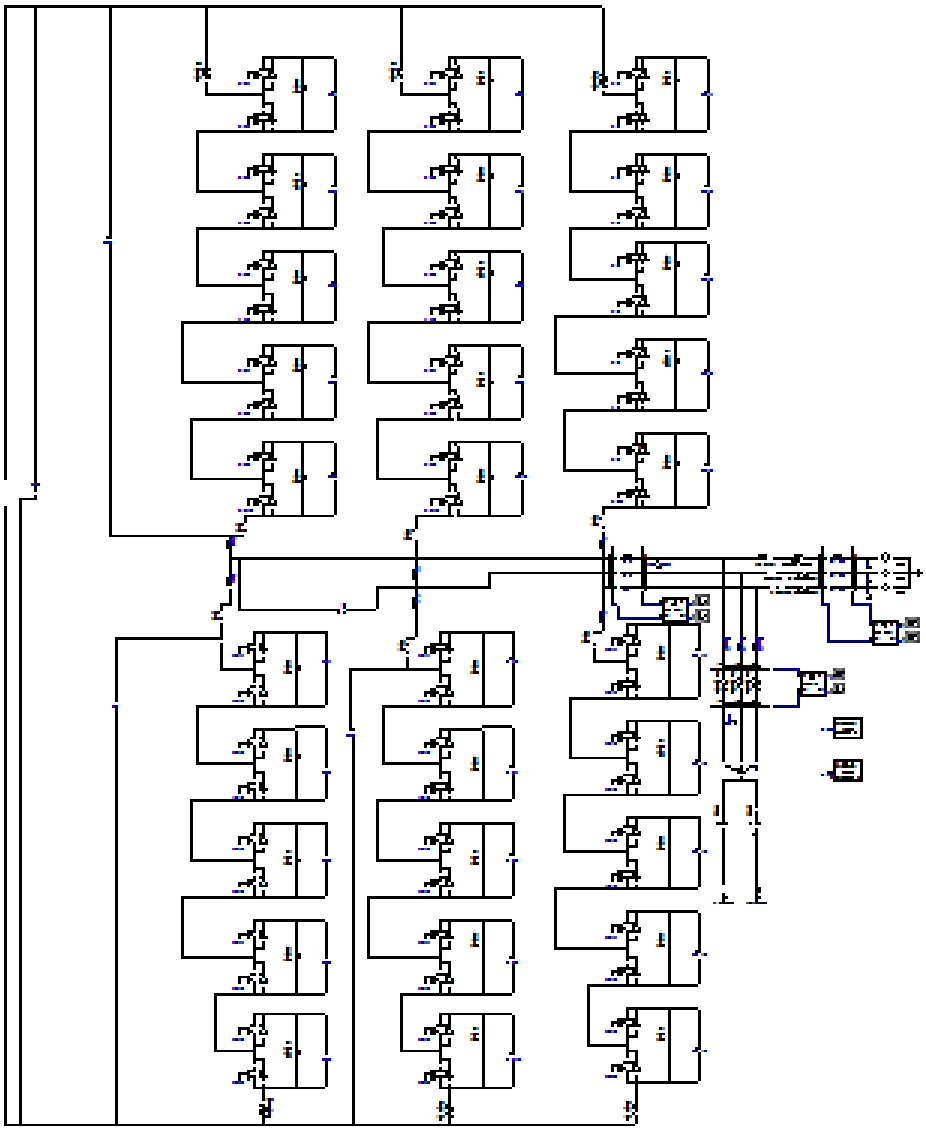


Figure 5.4 Simulated System in MMC-STATCOM

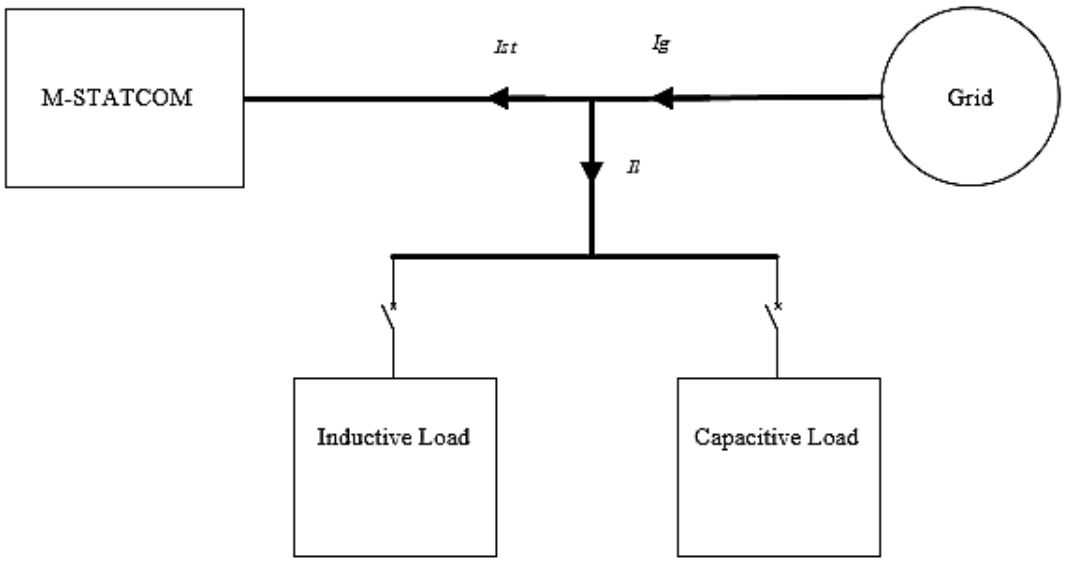


Figure 5.5 Single line diagram of the proposed system

To assess performance of the MMC-STATCOM, inductive and capacitive loads are included to the system. The assessment is performed for both while inductive and capacitive loads are together and also separately. In this system, 6 level MMC is considered in application of STATCOM. 5 MVAR inductive load and -5 MVAR capacitive load are handled. Among the medium voltage level values, 10.5 kV is selected.

5.4.2 Design Parameters for MMC-STATCOM

Depending on the capacitor voltage ripple and circulating current resonance affect, submodule capacitor and arm inductor value is selected. Initially, the medium-voltage level value is determined. Then, modulation index value is decided. It can be varied from 0 up to $\frac{2}{\sqrt{3}}$. The modulation index is selected as 0.9. Depending on the modulation index value, DC link voltage is calculated as seen in Equation (5.5) [28]. Afterwards, the number of submodules per arm is decided and then, the most important parameters, submodule capacitance and arm inductance value is determined, respectively.

$$V_{dc} = \frac{2}{\sqrt{3}} x V_{AC\_LL,rms} x \frac{2}{m} \quad \textbf{(5.5)}$$

5.4.2.1 Deciding on the Number of Submodules Per Arm

Determining the number of submodules per arm constitutes an important place in the MMC. Because, when N is increased, performance of the multilevel modular converter changes in ascending order. Moreover, higher output voltage and power levels can be obtained.

The submodule capacitor voltage, $\frac{V_{dc}}{N}$, is limited by the voltage level of the power semiconductor. 1700V, 3300V, 4500V and 6500V IGBT technologies are utilized in power electronics applications. Submodule voltage is restricted about 3.5-4 kV in 6500 V IGBT applications. Thus, 6500 V IGBT is preferred. After selected the power semiconductor, the number of submodules per arm, 5, is determined with the ratio of the DC link voltage to the max voltage ratio of the IGBTs.

It is important to mention that, while determining the number of submodules per arm, arm current value is not exceeded to the max current ratio of the IGBTs as shown in Table 5.1. Maximum current rating of the IGBTs is taken as a reference from [63**]**.

Table 5.1 Max current and max voltage rating of the IGBTs

1700V IGBT		3300V IGBT		4500V IGBT		6500V IGBT	
Vdc_link	Ic(A)	Vdc_link	Ic(A)	Vdc_link	Ic(A)	Vdc_link	Ic(A)
900	3600	1800	1500	2800	1200	3600	750
900	2400	1800	1200	2800	900	3600	600
900	1800	1800	800	2800	800	3600	500
900	1600	1800	400	2800	600	3600	400
900	1200	1800	-	2800	400	3600	250

5.4.2.2 Selection of the Submodule Capacitor

Upper arm voltage and that of voltage modulation index k can be represented as in Equations (5.6) and (5.7), respectively.

$$v_{up}(t) = \frac{V_{dc}}{2} - v_{low}(t) = \frac{V_{dc}}{2} - v_{0\_p}\sin(wt) \quad \textbf{(5.6)}$$

$$k = \frac{2.v_{0\_p}}{V_{dc}} \quad \textbf{(5.7)}$$

The energy change of the voltage source can be indicated as in Equation (5.8),

$$\Delta W_{source(k)} = \frac{2}{3}.\frac{S}{k.\omega}.(1-(\frac{k.\cos\varphi}{2})^2)^{\frac{3}{2}} \quad \textbf{(5.8)}$$

In here, S is the apparent power of the converter. If the converter arm occurs of N submodules, the energy change of the single submodule can be expressed as in Equation (5.9),

$$\Delta W_{source(k)} = \frac{2}{3}.\frac{S}{k.\omega.N}.(1-(\frac{k.\cos\varphi}{2})^2)^{\frac{3}{2}} \quad \textbf{(5.9)}$$

Submodule capacitor voltage calculation is determined by the Equation (5.10). Considering submodule capacitor value has $\pm\in$ voltage ripple, the energy of the submodule capacitor can be represented as in Equation (5.11). Total energy rate per MVA is calculated as in Equation (5.12). The total stored energy ratio in the capacitor varies between 10 J/kVA and 50 J/kVA. In lower values, advantage side is the cost. On the other hand, higher voltage ripples is observed on the DC link circuit.

$$V_{SM} = \frac{V_{dc}}{N} \quad \textbf{(5.10)}$$

$$W_{SM} = \frac{1}{2}.C_{SM}.V_{SM}{}^2 = \frac{1}{4.\in}.\Delta W_{SM} \quad \textbf{(5.11)}$$

$$W_{totalconv.rate} = \frac{W_{SM}.2N.3}{S} \quad \textbf{(5.12)}$$

Consequently, the voltage ripple value from 0 up to 1($0 < \in < 1$) can be selected at any desired value. Thus; submodule capacitor can be written as shown in Equation (5.13),

$$C_{SM} = \frac{\Delta W_{Source}}{2. \in .V^2_{SM}} \quad \textbf{(5.13)}$$

According to the many researchers, arm capacitance value should be selected being not higher than 1.5 mF [28]. Additionally, arm capacitance value can not be selected lower than 0.5 mF due to increase the capacitor voltage ripple [28].

5.4.2.3 Selection of the Arm Inductance

Arm inductors are used for suppressing the circulating currents stemming from the phase difference between the phases in the converter arm and fault currents such as short circuit condition between the DC terminals. Moreover, arm inductors also work as a filter eliminating the circulating currents on the output current. Between the existing even-order harmonics, second-order harmonic is the dominant one. If the second-order harmonic component is not eliminated, it will lead to increasing losses and higher current rating requirements of the MMC [64]. Arm capacitor calculation is expressed as in Equation (5.14). Determination of the arm inductance is also indicated as in Equation (5.15).

In here, L_{armr} is the arm inductance where resonance consists, ω is the angular frequency, h is the harmonic order and m_a represents the modulation index.

$$C_{arm} = \frac{C_{SM}}{N} \quad \textbf{(5.14)}$$

$$L_{armr}\,|_{C_{armr}=C_{arm}} = \frac{1}{C_{arm}\omega^2}\frac{2(h^2-1)+m_a{}^2h^2}{8h^2(h^2-1)} \quad \textbf{(5.15)}$$

Table 5.2 MMC-STATCOM circuit parameters

Symbol	Parameter	Value	Unit
Q_L	Inductive reactive power	5	MVAR
Q_C	Capacitive reactive power	-5	MVAR
N	Submodules per arm	5	-
f_{c_PD}	PD-PWM carrier frequency	5000	Hz
f_{c_PS}	PS-PWM carrier frequency	1000	Hz
R_{arm}	Arm resistance	0.1	Ω
L_{arm}	Arm inductance	2	mH
C_{SM}	Submodule capacitance	1.5	mF
R_{grid}	Grid equivalent resistance	0.0015	Ω
L_{grid}	Grid equivalent inductance	0.25	mH
V_{grid}	Grid voltage (line-to-line)	10.5	kV
V_{DC}	DC link voltage	19	kV
f_g	Grid side frequency	50	Hz

5.5 Active and Reactive Power Control of the MMC-STATCOM

Depending on the introduction of the instantaneous active and reactive power theory [61], Both theory can be defined in dq coordinate system as in Equations (5.16) and (5.17).

$$P(t) = u_d(t)i_d(t) + u_q(t)i_q(t) = \sqrt{3}vi_d \quad \textbf{(5.16)}$$

$$Q(t) = u_q(t)i_d(t) + u_d(t)i_q(t) = \sqrt{3}vi_q \quad \textbf{(5.17)}$$

Finally, instantaneous active and reactive power exchange between the AC grid and MMC-STATCOM is controlled by regulating i_d and i_q currents, separately. In case of i_d is positive, MMC-STATCOM drawn active power and regarding capacitors are charged. When i_d is negative, MMC-STATCOM gives active power to the AC grid and regarding capacitors are discharged. Considering i_q current, when i_q is positive, MMC-STATCOM releases capacitor reactive power to the AC grid. otherwise, inductive reactive power condition is valid for MMC-STATCOM [62].

5.6 Analysis of Operation Modes of the MMC-STATCOM

Static mode and dynamic mode of the MMC-STATCOM are investigated to prove a properly operation in following sections. Phase-shifted PWM based control method is handled for analysis of the static mode and dynamic mode.

5.6.1 Static Mode of the MMC-STATCOM

5.6.1.1 Inductive Loading Condition

To analyse of the steady-state characteristics of the Modular Multilevel Converter based STATCOM, inductive load is included into the system whose inductive reactive power is equal to the 5 MVAR. MMC-STATCOM is in deactivated condition as shown in Figure 5.6. On the other hand, MMC-STATCOM is in activated conditions from Figure 5.7 to Figure 5.13. When inductive load is used, the current signal of the grid lags behind the voltage signal of the grid around 90° out of phase which affect the power quality. By the virtue of the incorporate in the MMC-STATCOM, grid side compensation is achieved about unity power factor as illustrated in Figure 5.7. Under capacitive mode of the MMC-STATCOM, statcom and load side currents and voltages are illustrated in Figure 5.8 to Figure 5.9, respectively. Load, grid and statcom side of the currents are 3.5 times enlarged in order to analyze more clearly. Considering reactive power analysis in Figure 5.10, MMC-STATCOM gives capacitive reactive power to the AC grid. According to that, i_d and i_q currents are illustrated in Figure 5.11. As seen from Figure 5.12, DC link voltage control is achieved around 19 kV in capacitive mode of the MMC-

STATCOM. In Figure 5.13, upper capacitor voltages are shown. Accordingly, capacitor voltage balancing is not distorted when inductive load is added into the system.

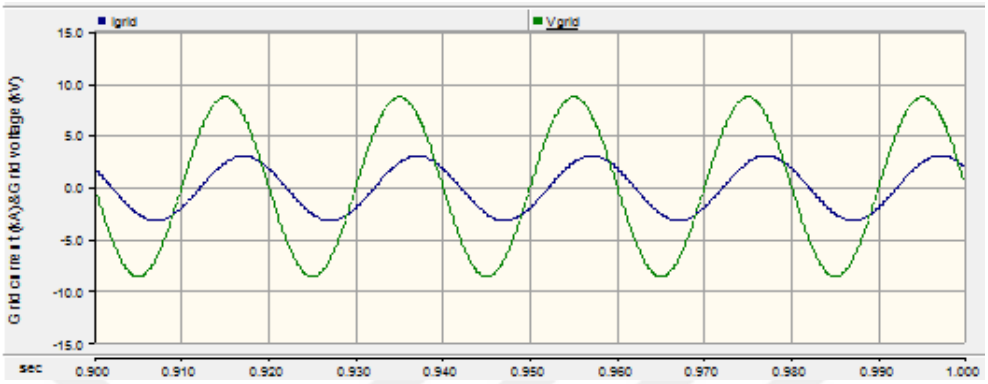


Figure 5.6 Grid side current and voltage

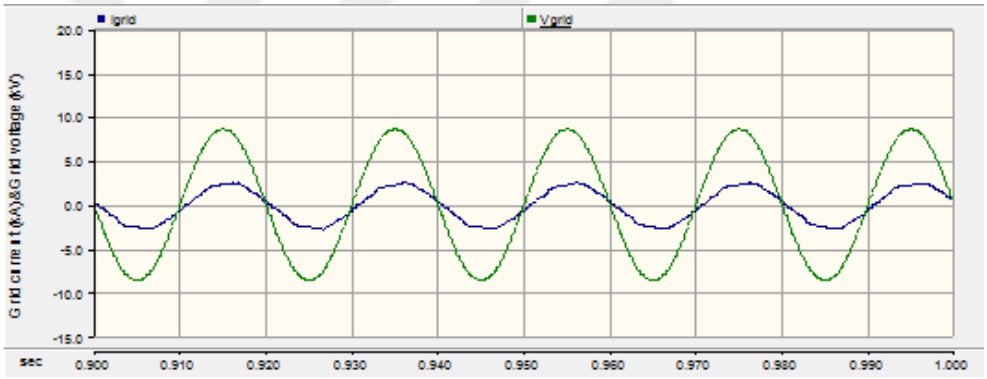


Figure 5.7 Grid side current and voltage

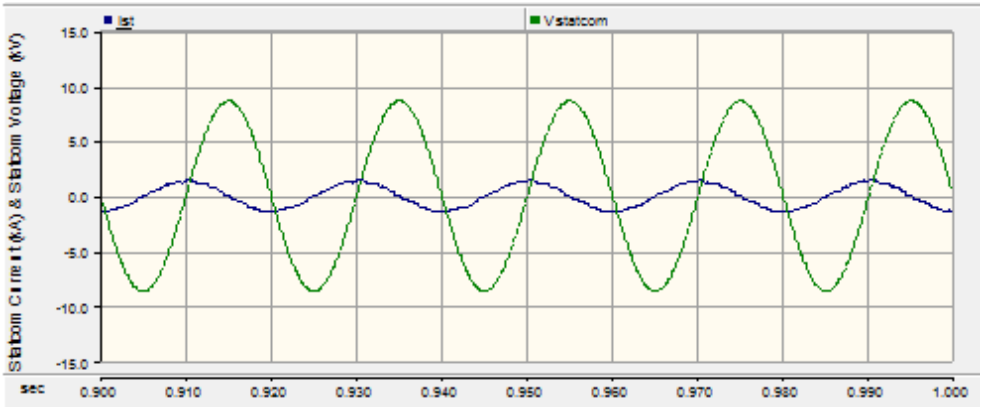


Figure 5.8 Statcom side current and voltage

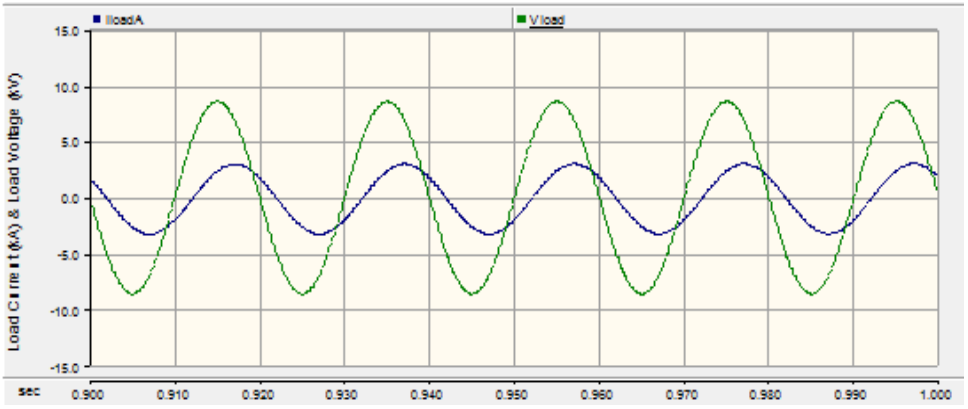


Figure 5.9 Load side current and voltage

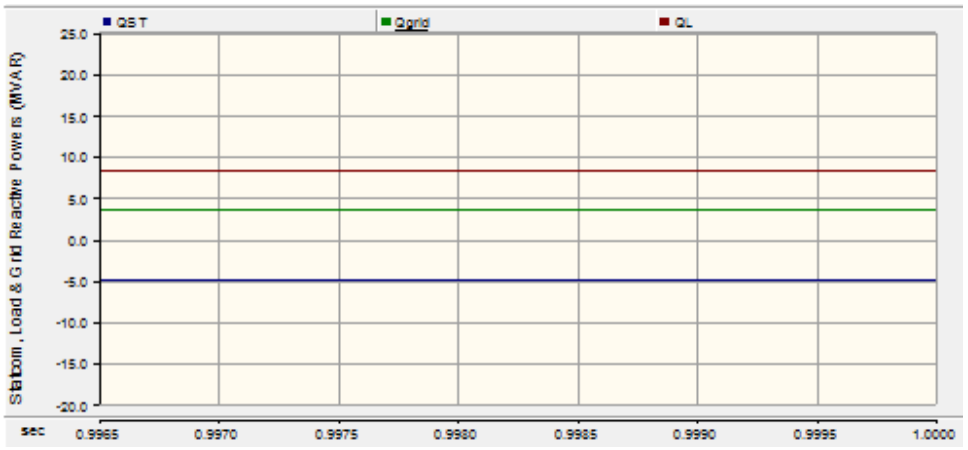


Figure 5.10 Statcom, load and grid side reactive powers

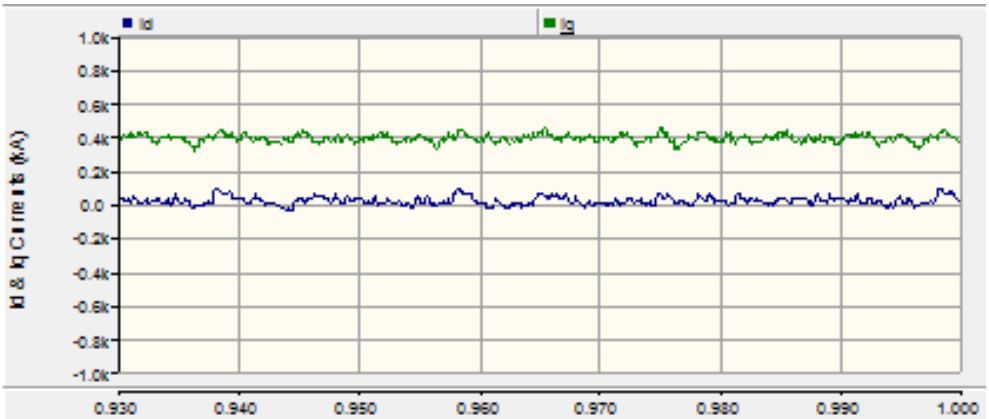


Figure 5.11 id and iq currents

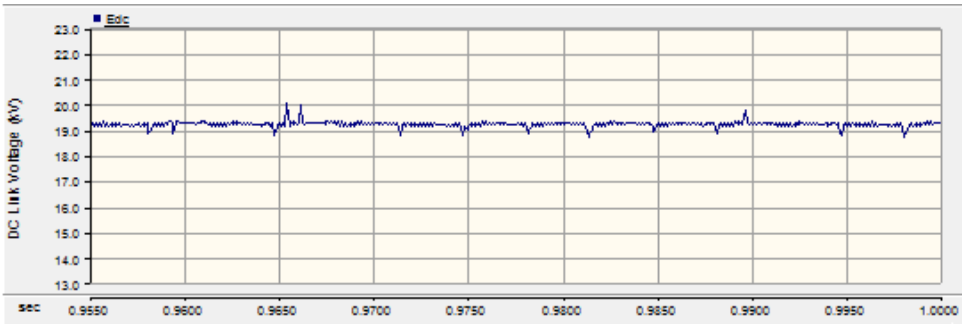


Figure 5.12 DC link voltage

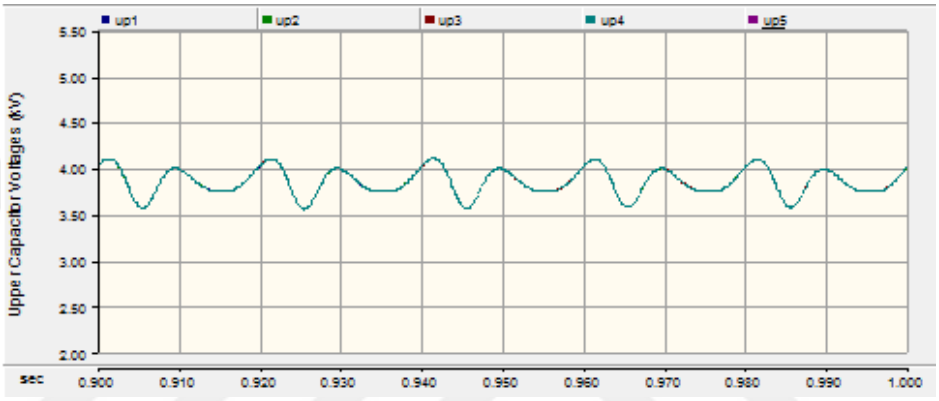


Figure 5.13 Upper capacitor voltages

5.6.1.2 Capacitive Loading Condition

Given that, steady-state characteristics analysis of the MMC-STATCOM, capacitive load is added into the systems whose capacitive reactive power is equal to the -5 MVAR. MMC-STATCOM is in deactivated condition as shown in Figure 5.14. On the other hand, MMC-STATCOM is in activated conditions from Figure 5.15 to Figure 5.21.When capacitive load is used, the current signal of the grid stay ahead of the voltage signal of the grid around 90° out of phase which affect the power quality. On account of the incorporate in the MMC-STATCOM, grid side compensation is achieved about unity power factor as illustrated in Figure 5.15. Under inductive mode of the MMC-STATCOM, statcom and load side currents and voltages are illustrated in Figure 5.16 to Figure 5.17, respectively. Load, grid and statcom side of the currents are 3.5 times enlarged in order to analyze more clearly. Considering reactive power analysis in Figure 5.18, MMC-STATCOM takes inductive reactive

power from the AC grid. According to that, i_d and i_q currents are illustraed in Figure 5.19. As seen in Figure 5.20, DC link voltage is stabilized at 19 kV. Thus, DC link voltage control is achieved under inductive mode of the MMC-STATCOM. In Figure 5.21, upper capacitor voltages are shown. Accordingly, capacitor voltage balancing is successed when capacitive load is added setting up around 3.8 kV.

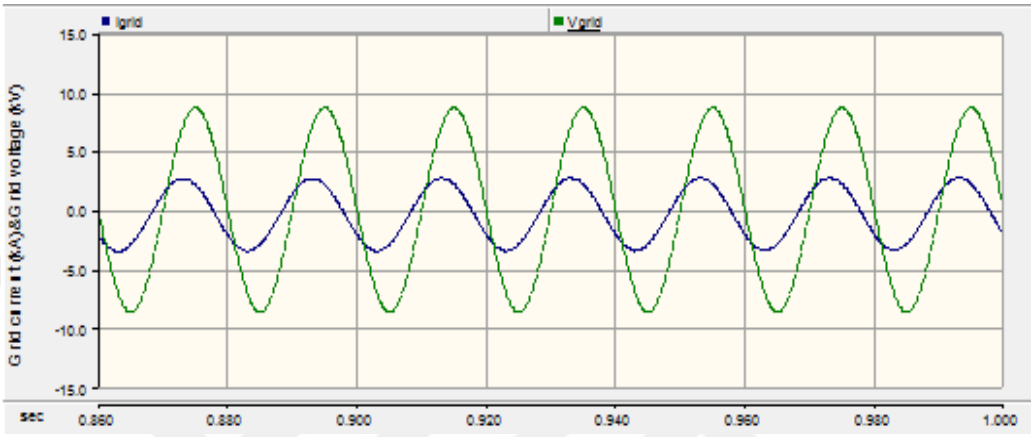


Figure 5.14 Grid side current and voltage

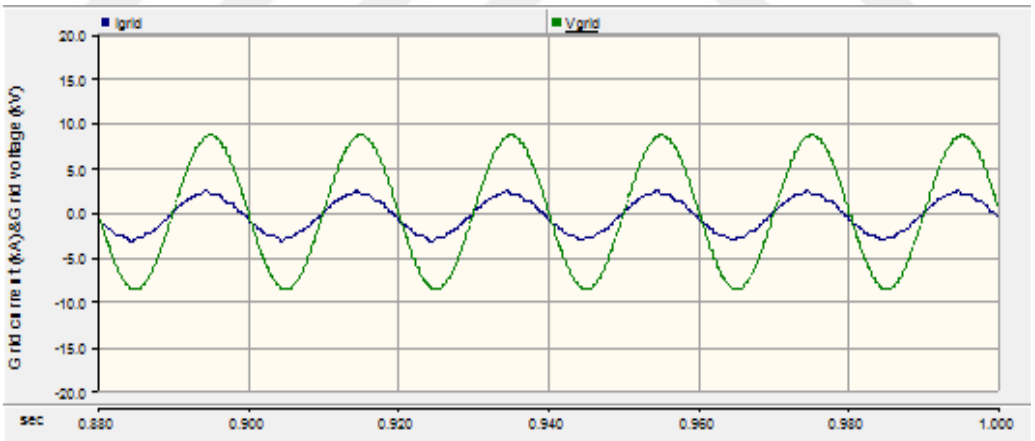


Figure 5.15 Grid side current and voltage

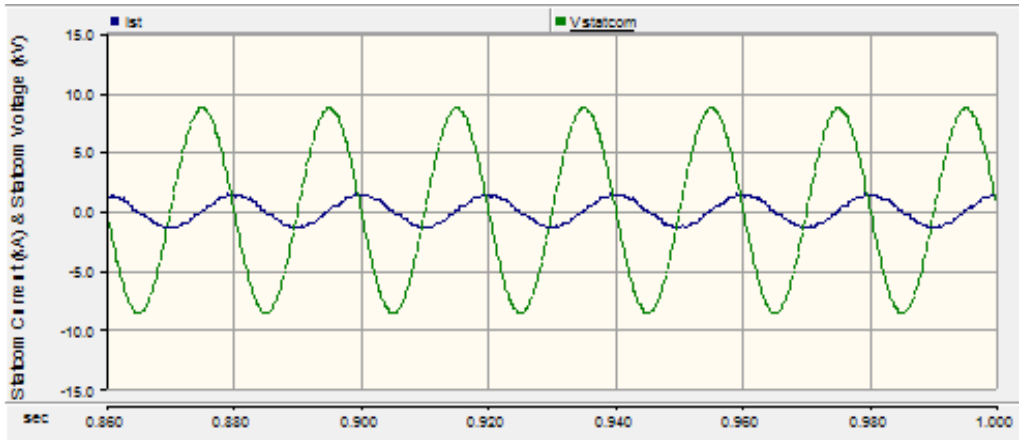


Figure 5.16 Statcom side current and voltage

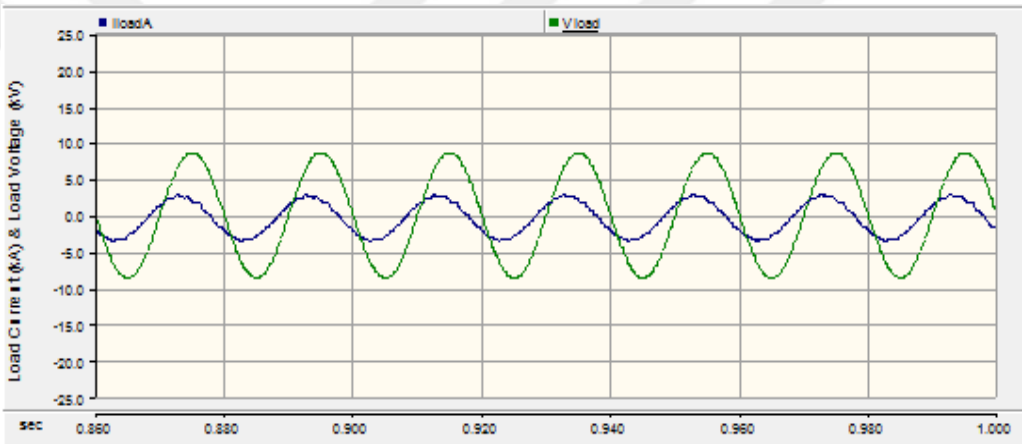


Figure 5.17 Load side current and voltage

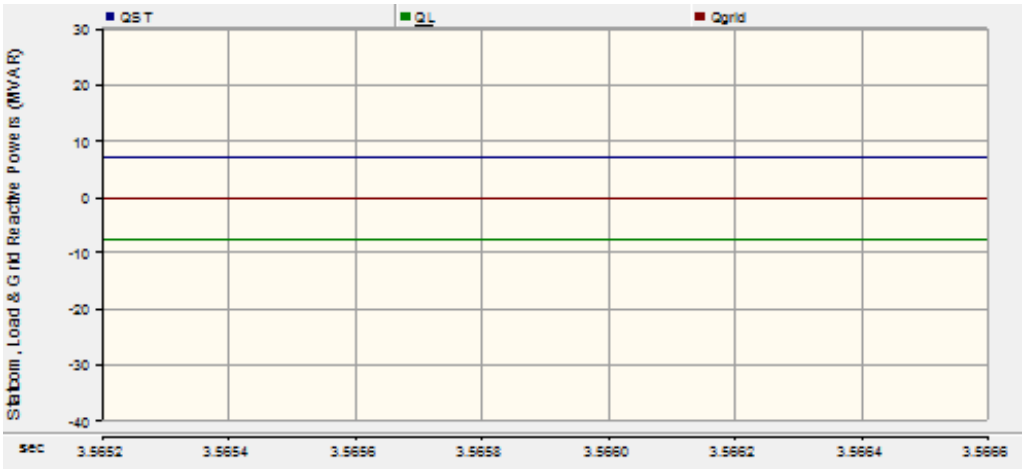


Figure 5.18 Statcom, load and grid side reactive powers

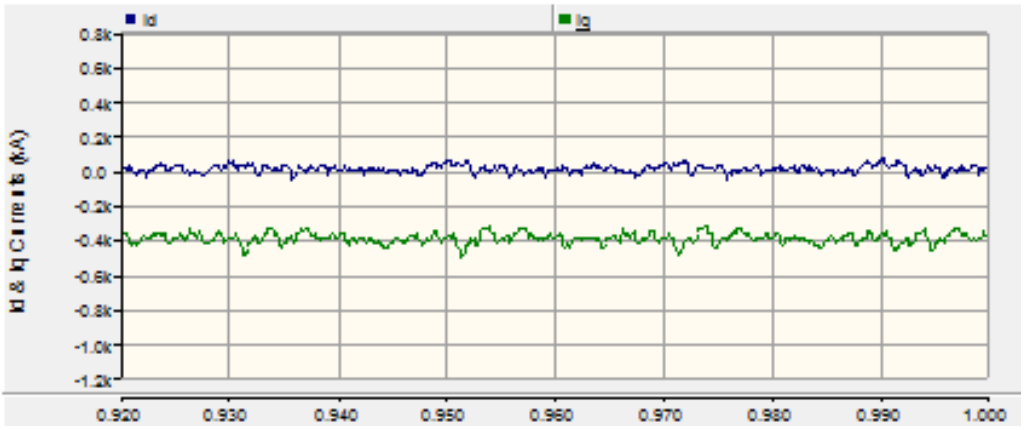


Figure 5.19 id and iq currents

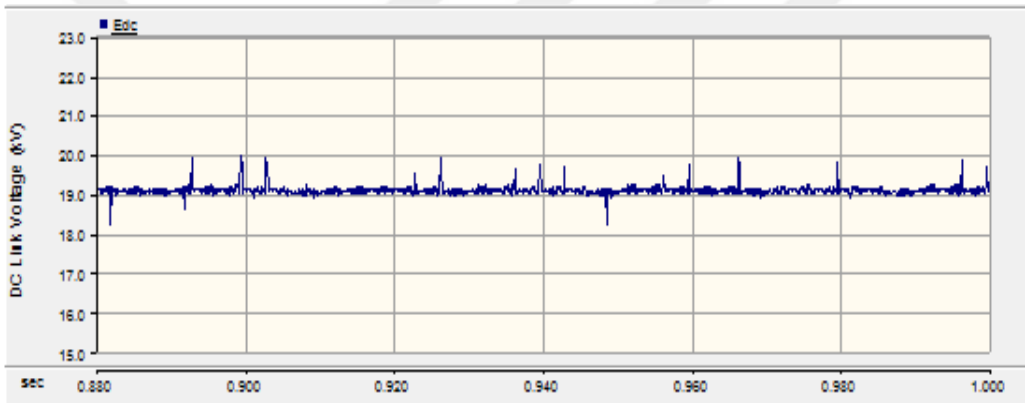


Figure 5.20 DC link voltage

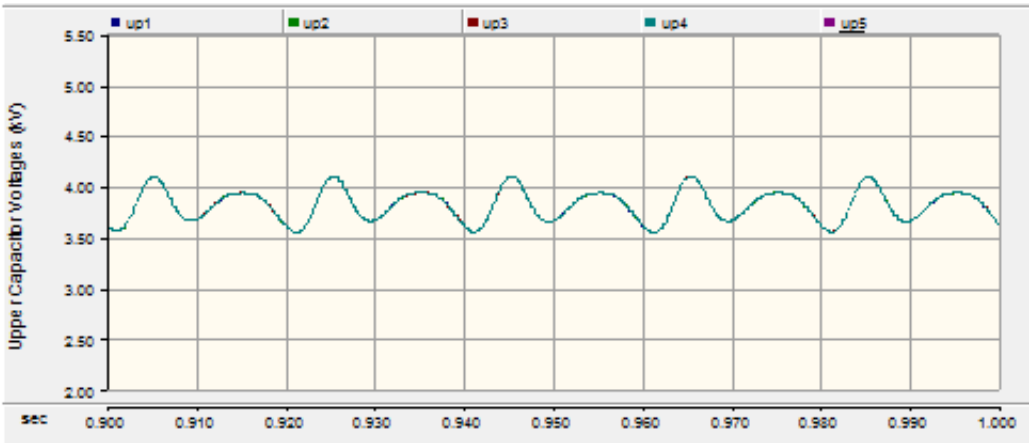


Figure 5.21 Upper capacitor voltages

5.6.2 Dynamic Mode of the MMC-STATCOM

In order to prove the dynamic characteristics of the MMC-STATCOM, transition from inductive mode to capacitive mode of the MMC-STATCOM is analyzed before and after 0.5s. Without MMC-STATCOM is activated, grid side current and voltage have phase difference about 90° among each other as leading or lagging as shown in Figure 5.22, respectively. On the other hand, MMC-STATCOM is in activated conditions from Figure 5.23 to Figure 5.27. Moreover, grid side of the current is 3.5 times enlarged in order to analyze more clearly. Owing to the MMC-STATCOM activated, compensation is achieved in between source current and voltage as shown in Figure 5.23. Inductive mode range is discussed from 0s to 0.5s. On the other hand, capacitive mode range is examined from 0.5s to 1s as shown in Figure 5.24. Accordingly, i_d and i_q currents are illustrated in Figure 5.25. DC link voltage control is not distorted during transition time as shown in Figure 5.26. Consequently, upper capacitor voltages are well-balanced as illustrated in Figure 5.27.

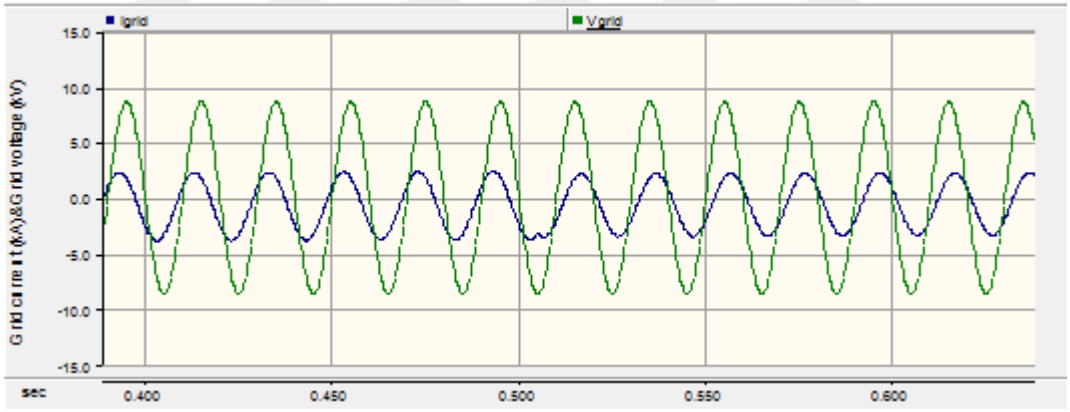


Figure 5.22 Grid side current and voltage

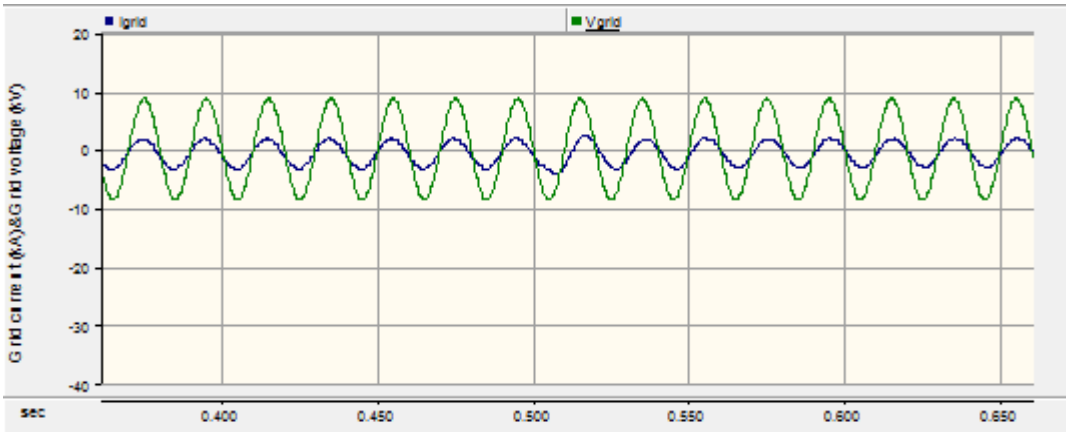


Figure 5.23 Grid side current and voltage

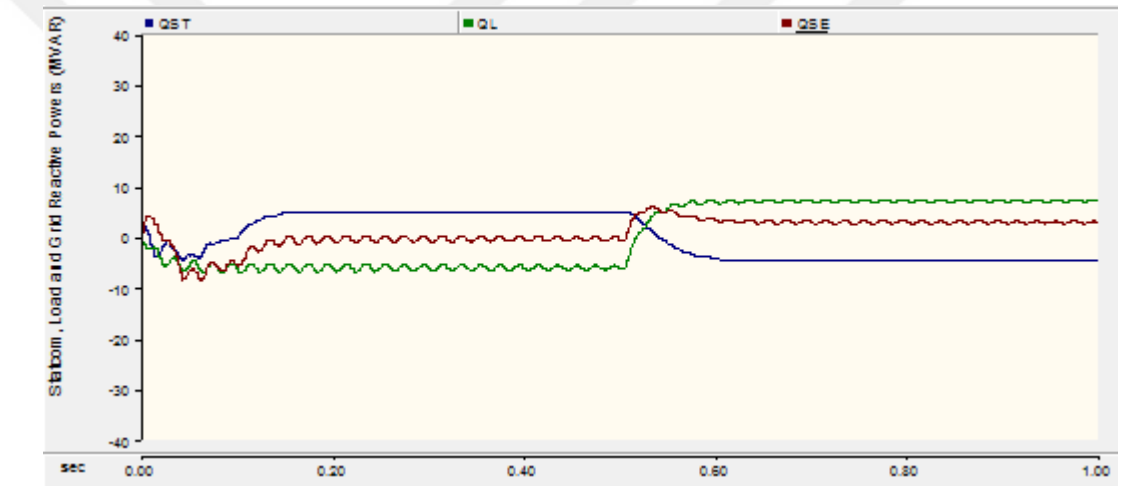


Figure 5.24 Statcom, load and grid side reactive powers

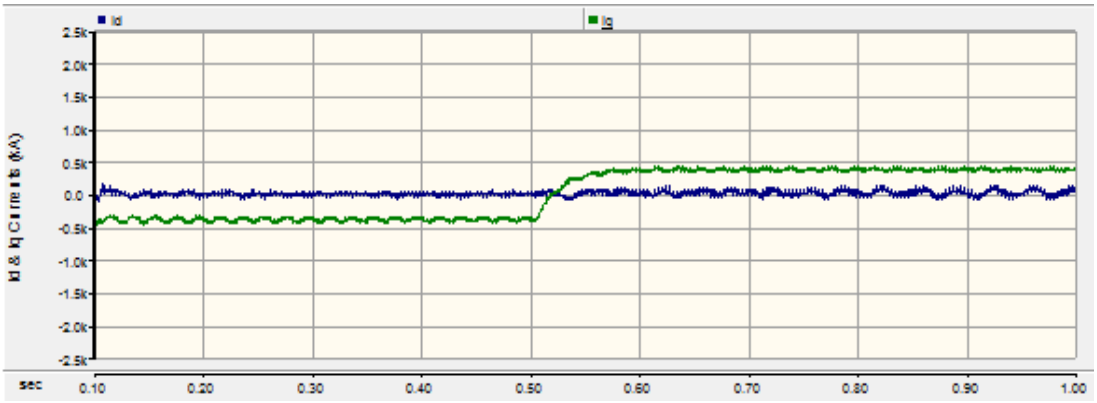


Figure 5.25 id and iq currents

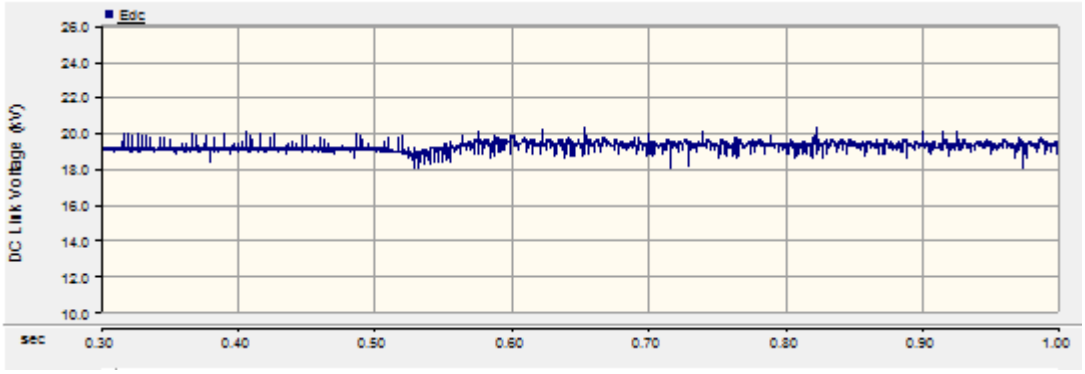


Figure 5.26 DC link voltage

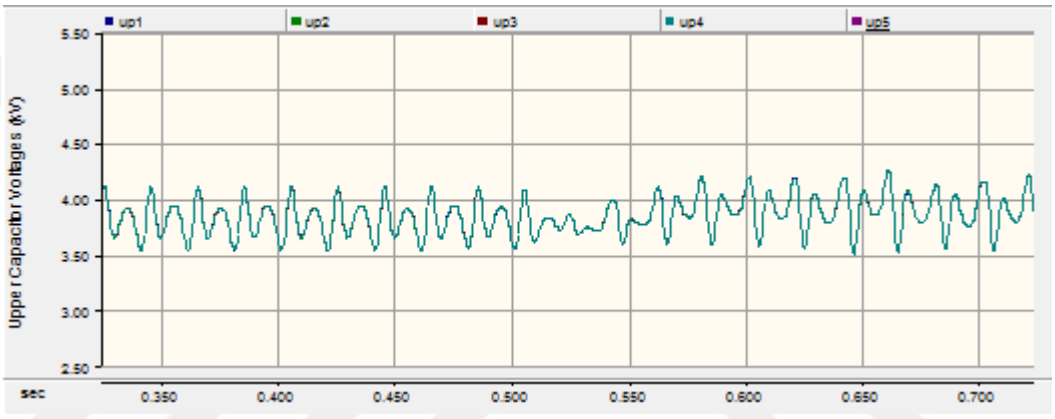


Figure 5.27 Upper capacitor voltages

5.7 Perfomance Comparison Analysis

Statcom voltages and currents are compared in using sort and selection method and Phase-Shifted PWM based control method when considered both capacitive mode range and inductive mode range of the MMC-STATCOM. While comparing both balancing methods, equivalent switching count [29] is considered in a phase leg taken into account a fair comparing. Among the level-shifted PWM methods, Phase-disposition (PD) PWM is preferred in sort and selection method and that of carrier frequency is taken 5000 Hz. On the other hand, Phase-shifted carriers are used in Phase-shifted PWM based control method and that of carrier frequency is taken 1000 Hz due to equivalent switching frequency in a phase leg.

Considering capacitive mode range of the MMC-STATCOM, that of voltages and current regarding to sort and selection method are illustraed in Figure 5.28 to Figure 5.30, respectively. Among the statcom voltages, that of after arm inductor conditions are analyzed. In other respects, taken into account inductive mode range of the MMC-STATCOM, that of voltages and current regarding to sort and selection method are illustrated in Figure 5.31 to Figure 5.33, respectively. In phase-shifted PWM based control method, capacitive mode of the MMC-STATCOM considering that of voltages and current is analyzed as in Figure 5.34 to Figure 5.36, respectively. In Figure 5.37 to Figure 5.39, inductive mode of the MMC-STATCOM related to phase-shifted PWM based control method are illustrated. Consequently, performance analysis for both control method considering capacitive mode and inductive mode ranges are seen in Table 5.3.

5.7.1 Voltage and Current Analysis of the Capacitive Mode Range of the MMC-STATCOM in Sort and Selection Method

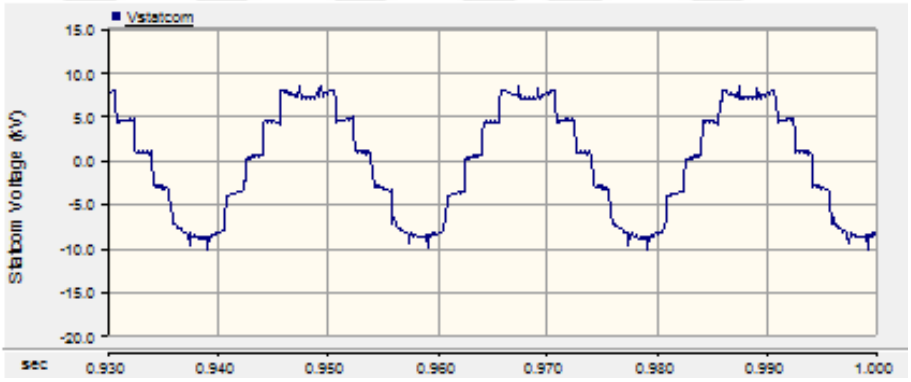


Figure 5.28 Statcom voltage before arm inductor in capacitive mode range using direct modulation sort and selection method

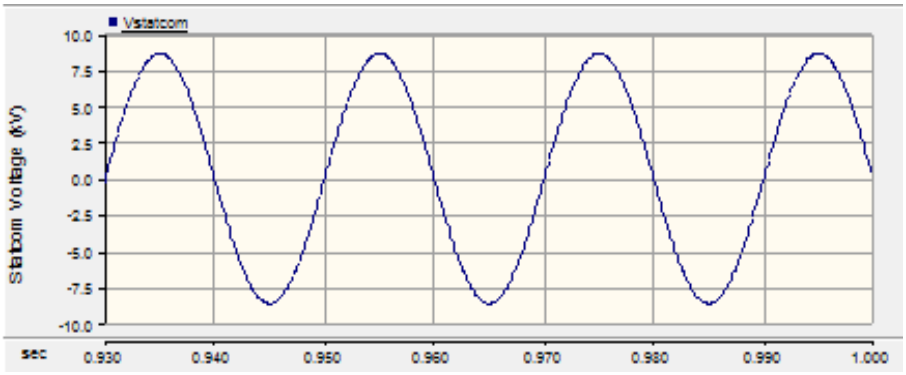


Figure 5.29 Statcom voltage after arm inductor in capacitive mode range using direct modulation sort and selection method

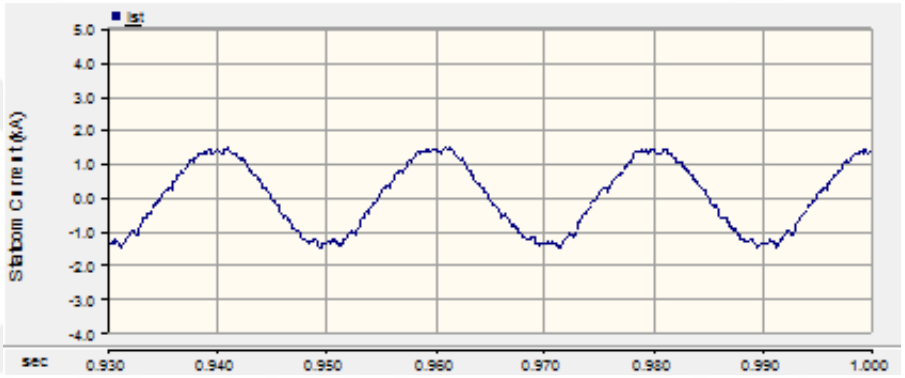


Figure 5.30 Statcom current in capacitive mode range using direct modulation sort and selection method

5.7.2 Voltage and Current Analysis of the Inductive Mode Range of the MMC-STATCOM in Sort and Selection Method

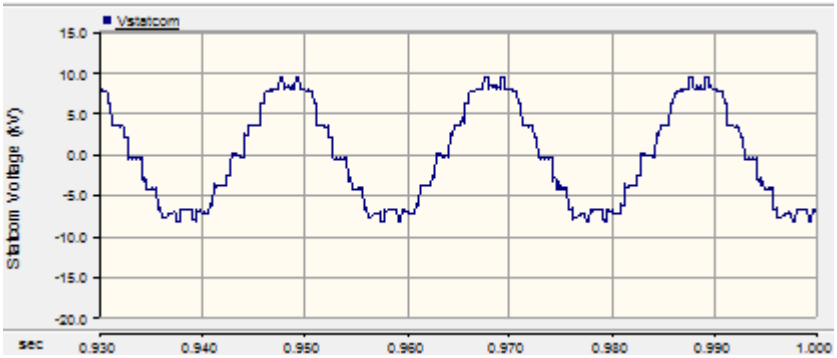


Figure 5.31 Statcom voltage before arm inductor in inductive mode range using direct modulation sort and selection method

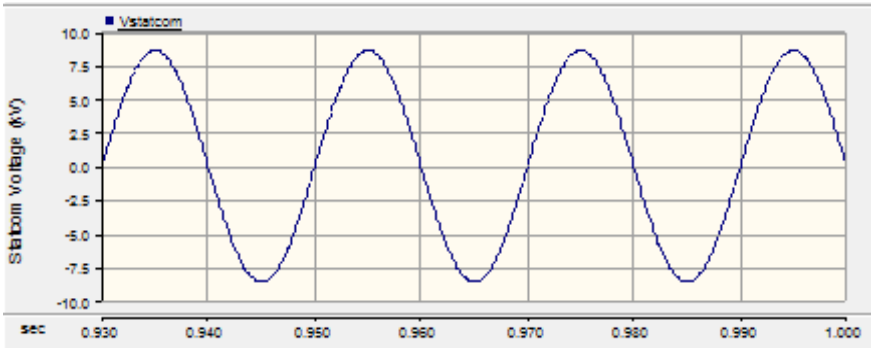


Figure 5.32 Statcom voltage after arm inductor in inductive mode range using direct modulation sort and selection method

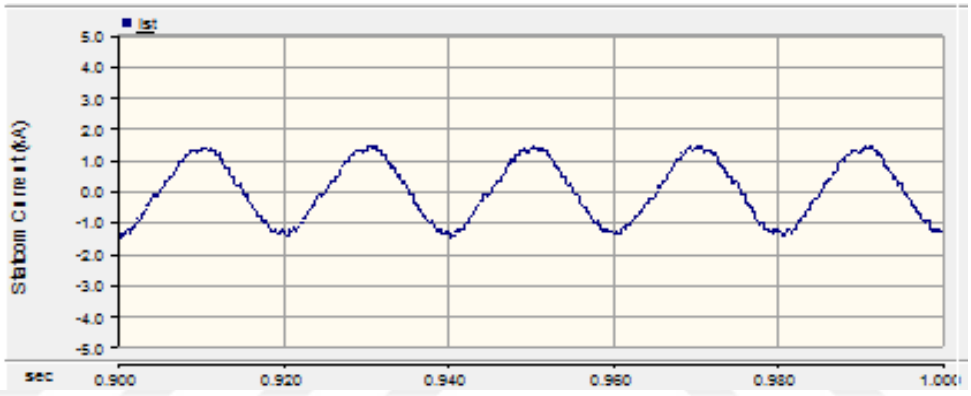


Figure 5.33 Statcom current in inductive mode range using direct modulation sort and selection method

5.7.3 Voltage and Current Analysis of the Capacitive Mode Range of the MMC-STATCOM in PS-PWM Based Control Method

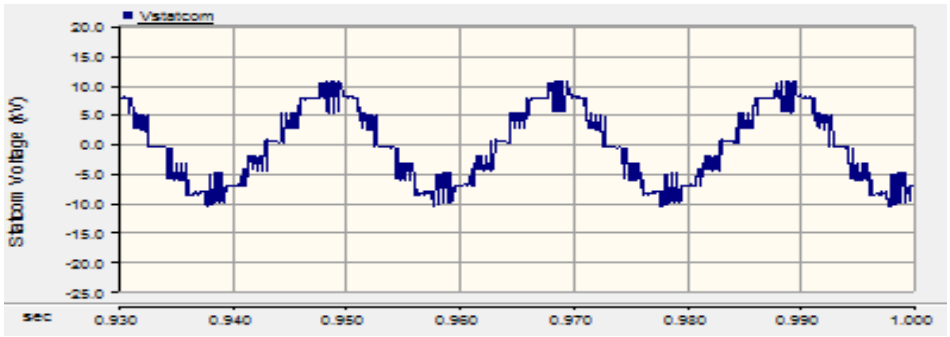


Figure 5.34 Statcom voltage before arm inductor in capacitive mode range using phase-shifted PWM balancing

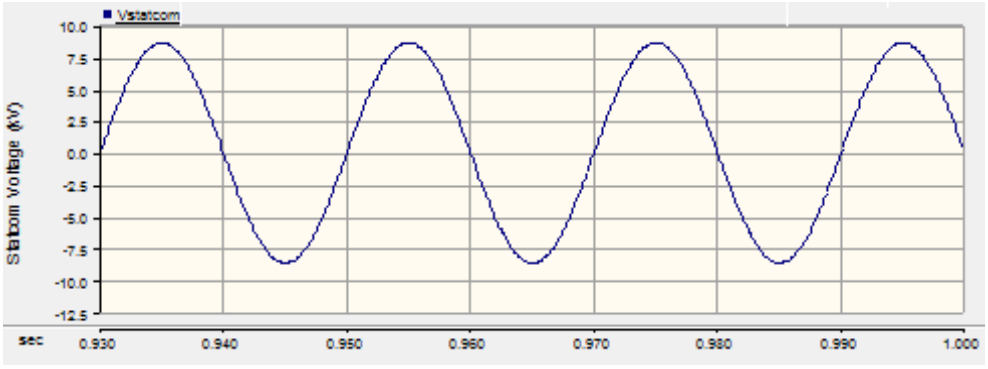


Figure 5.35 Statcom voltage after arm inductor in capacitive mode range using phase-shifted PWM balancing

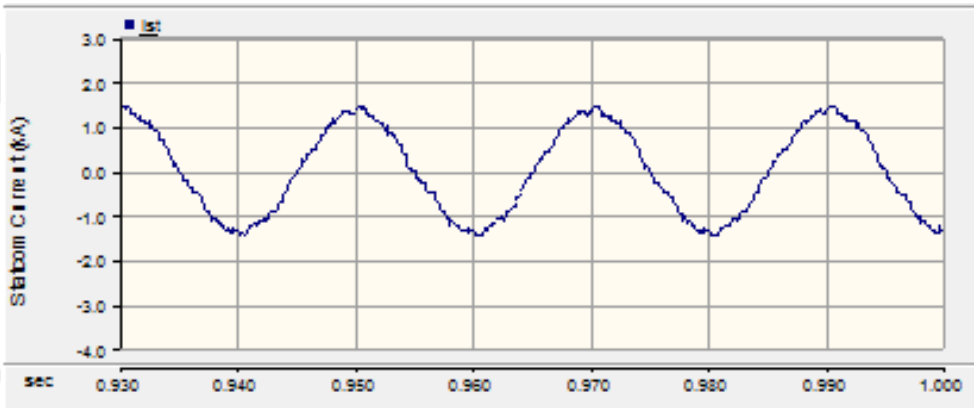


Figure 5.36 Statcom current in capacitive mode using phase-shifted PWM balancing method

5.7.4 Voltage and Current Analysis of the Inductive Mode Range of the MMC-STATCOM in PS-PWM Based Control Method

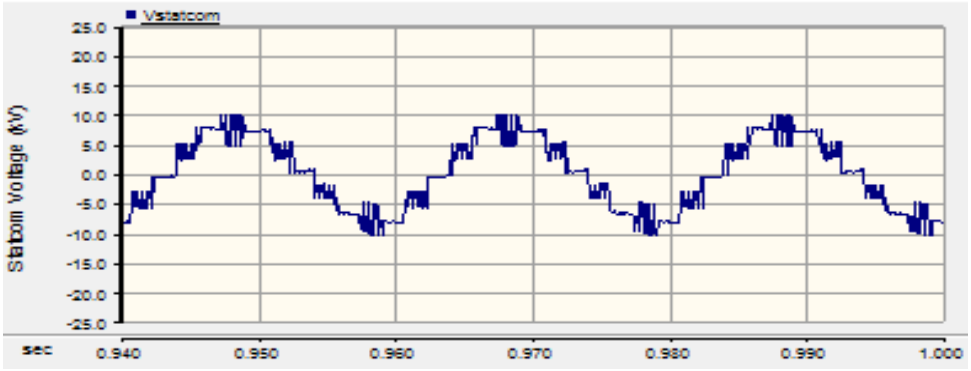


Figure 5.37 Statcom voltage before arm inductor in inductive mode using phase-shifted PWM balancing

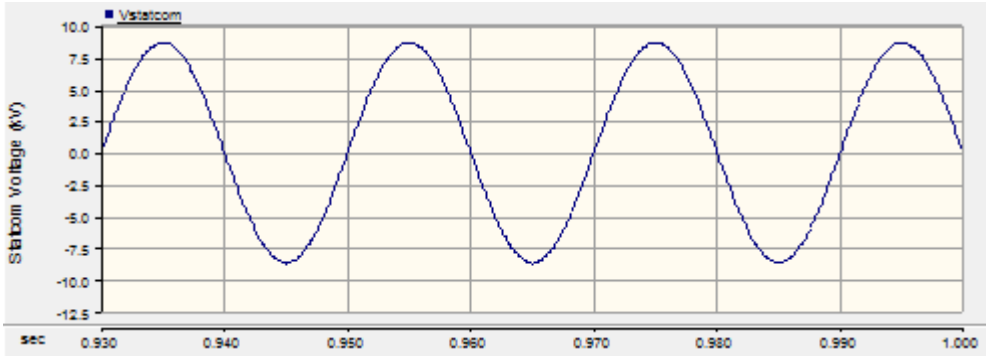


Figure 5.38 Statcom voltage after arm inductor in inductive mode using phase-shifted PWM balancing

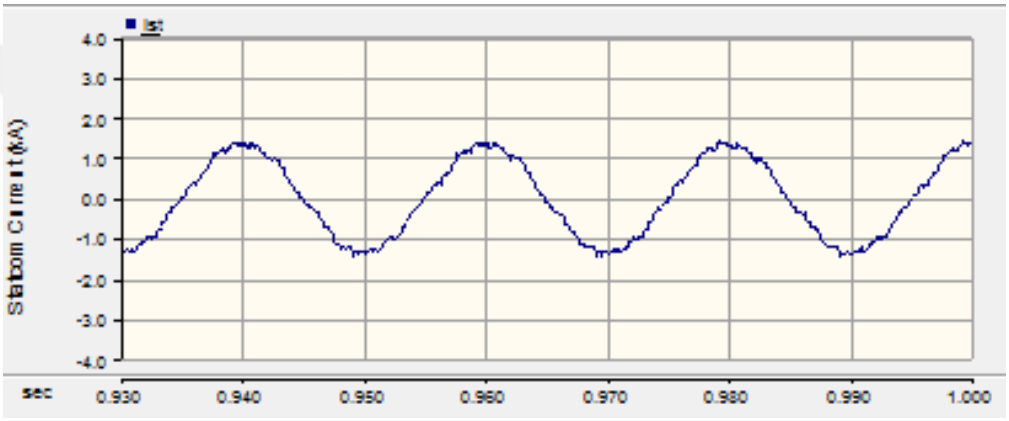


Figure 5.39 Statcom current in inductive mode using phase-shifted PWM balancing method

Table 5.3 Performance analysis of the capacitor voltage balancing methods in MMC-STATCOM

	Sort and Selection Method (2N+1 level PD-PWM)		**Phase-Shifted PWM Based Control Method (2N+1 level PS-PWM)**	
Mode	**Statcom current (Ist) (THD %)**	**Statcom Voltage (Vst) (THD %)**	**Statcom current (Ist) (THD %)**	**Statcom Voltage (Vst) (THD %)**
Capacitive Mode Range	4.05	6.38	4.02	4.81
Inductive Mode Range	6.03	6.86	4.07	4.89

As seen in Table 5.3, Phase-Shifted PWM Based Control Method has lower THD (%) value than Sort and Selection Method both capacitive mode and inductive mode of the MMC-STATCOM in terms of voltage and current analysis. Moreover, less time is spent for simulation studies.Thus; Phase-shifted PWM based control method can be preferred in MMC-STATCOM applications.

5.8 Application Issues for the MMC STATCOM

5.8.1 Example Projects

A STATCOM which is used Modular Multilevel Converter named SVC PLUS. The MMC provides reduced footsize, fast response time and minimized losses for STATCOM applications. SVC PLUS applications can be reviewed in many aspects and that can be grouped as; Utility applications, Grid Access applications, Mobility application and Industrial application. Considering utility applications, Kikiwa substation at New Zealand requires ± 50 MVAR SVC and Mocuba substation at

Mozambique requires ±35 MVAR SVC can be indicated as examples. One of the two SVC PLUS technologies in utility applications which is Kikiwa substation in New Zealand is illustrated in Figure 5.40 [8]. For Grid Access applications, Greater Gabbard wind farm at UK with a capacity of 500 MW and Thanet offshore wind farm at UK having a capacity of 300 MW can be given as examples. Taken into account Mobility application, E.ON at Germany, SVC PLUS technology can be handled as Static Frequency Converter in traction supplies. For Industrial application, SVC PLUS technology can be integrated to enhance flicker performance at ThyssenKrupp (USA).

Figure 5.40 One of the two SVC PLUS units at Kikiwa, New Zeeland

5.8.2 Selection of IGBT semiconductors

IGBT is the most preferred power semiconductor in high voltage converter applications. The reason is that in addition to low switching losses, requiring simple, flexible and low power demand circuit driver. IGBTs are produced in two different ways as Asymmetric and Reverse-Conducting. Principally, reverse-conducting IGBTs are the most preferred technology in industrial applications due to need parallel diode for controllable switch. IGBT which has 1700 V and more than 1700 V rated voltage are called as High Voltage IGBT (HV-IGBT). HV-IGBTs are produced as module or press-pack. Module IGBT is preferred in STATCOM and AC motor drive applications due to the ease of assembly and provide electrical isolation

as shown in Figure 5.41 [71]. On the other hand, Press-Pack IGBT is preferred in modern High Voltage applications due to the serial connection in converter structures and ability of short circuit during faulty condition as illustrated in Figure 5.42 [71]. The list of IGBTs which have the highest rated voltage as shown in Table 5.4.

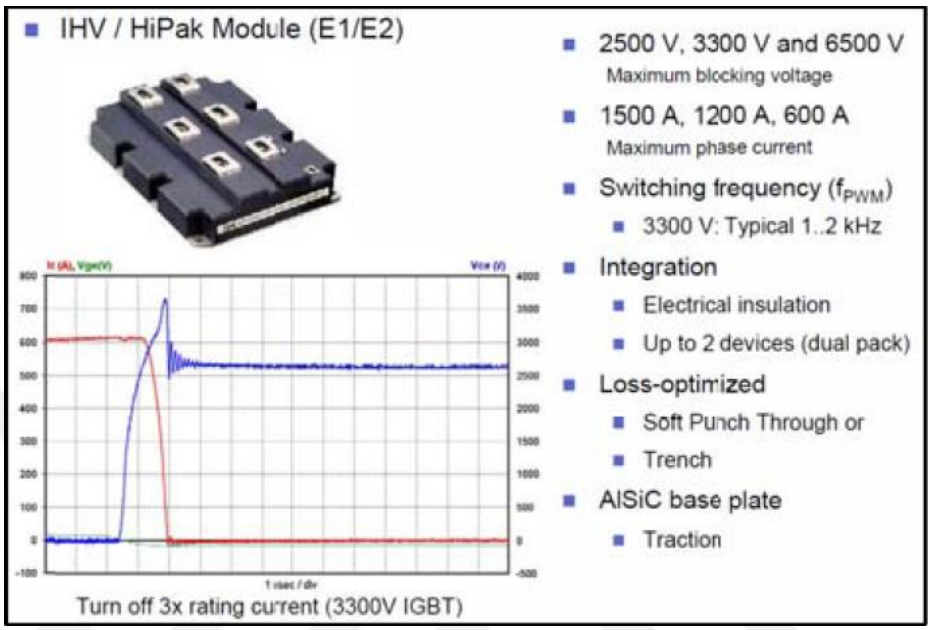


Figure 5.41 Module IGBT

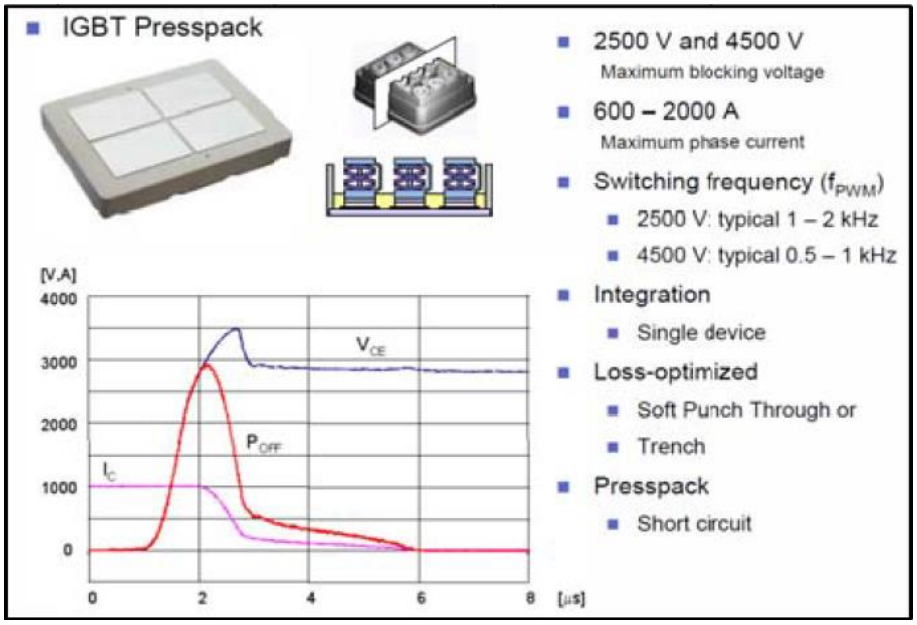


Figure 5.42 Press-Pack IGBT

Table 5.4 The list of IGBTs which have the highest rated voltage

V_{CES}	I_C	Pack	Manufacturer	Structure
3300 V	1500 A	Module	Mitsubishi Dynex Infineon ABB Hitachi	Reverse-Conducting
4500 V	1500 A			
6500 V	750 A			
2500 V	2000 A	StakPak	ABB	
4500 V	2000 A			
2500 V	1200 A	Press-Pack	Westcode	Asymmetric
4500 V	1800 A			
6500 V	900 A			
2500 V	2250 A			
4500 V	2400 A			

5.8.3 HVDC Capacitors

Power capacitors use in VSC-HVDC systems. EPCOS is one of the most known brand among the power capacitor manufacturers and that of power capacitor and transmission module is illustrated in Figure 5.43 [72]. An example of the DC storage capacitor used in SVC PLUS applications is shown in Figure 5.44 [72]. Main characteristics are expressed as in below [73];

1. Energy density 10 percent higher than that of gas-impregnant types
2. Values of the capacitance are more than 10000 μF
3. Voltages of the capacitor can endure to 4000 V DC

4. Capacitors can be endure to high voltage and current peaks.

Main application areas of the EPCOS power capacitors are traction converter systems and HVDC systems.

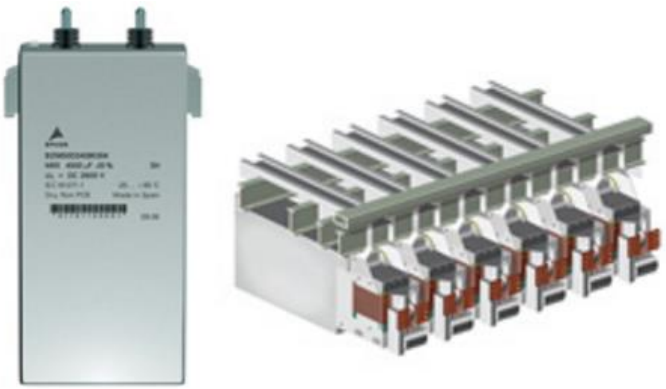


Figure 5.43 EPCOS HVDC power capacitor at left and VSC-HVDC transmission module at right

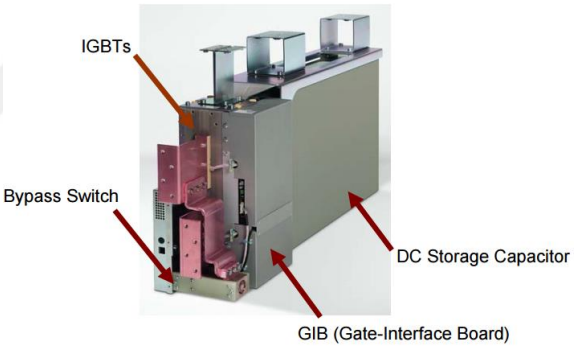


Figure 5.44 SVC PLUS power module with DC storage capacitor

5.8.4 Control Systems

Control features of the SVC PLUS are illustrated in Figure 5.45 and that of local and remote control structure with HMI is shown in Figure 5.46. Control and protection structure is illustrated in Figure 5.47. Finally, advanced control structure is seen in Figure 5.48.

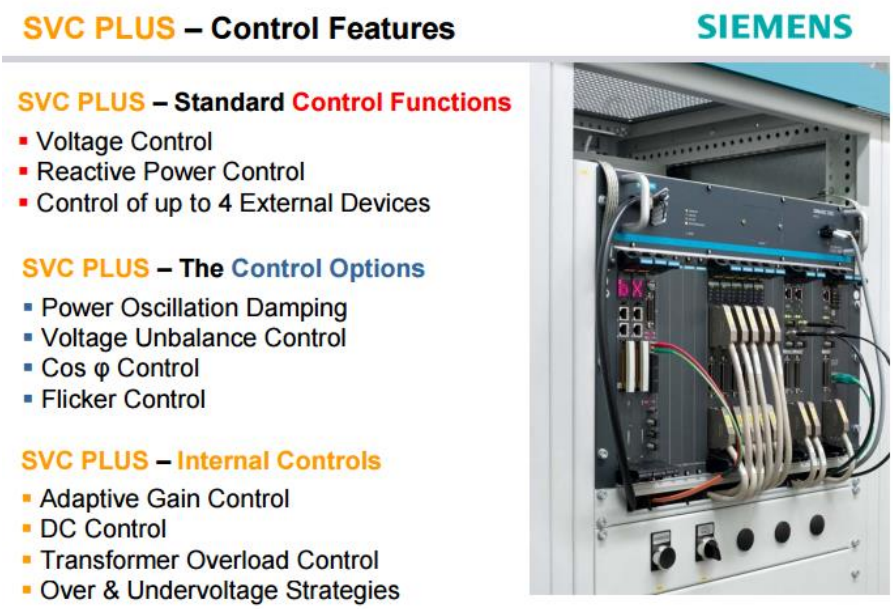


Figure 5.45 Control features of the SVC PLUS [74]

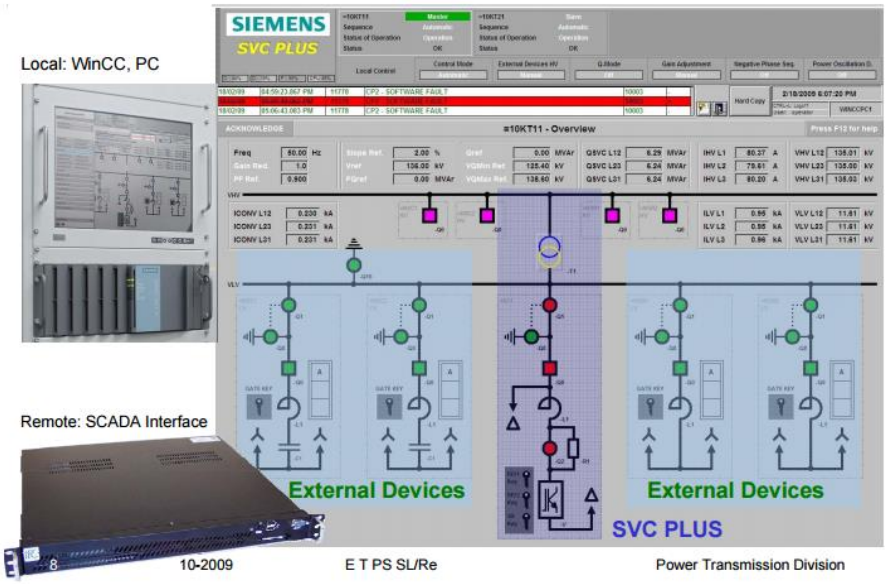


Figure 5.46 SVC PLUS local and remote control with HMI [74]

Figure 5.47 SVC PLUS control and protection structure [74]

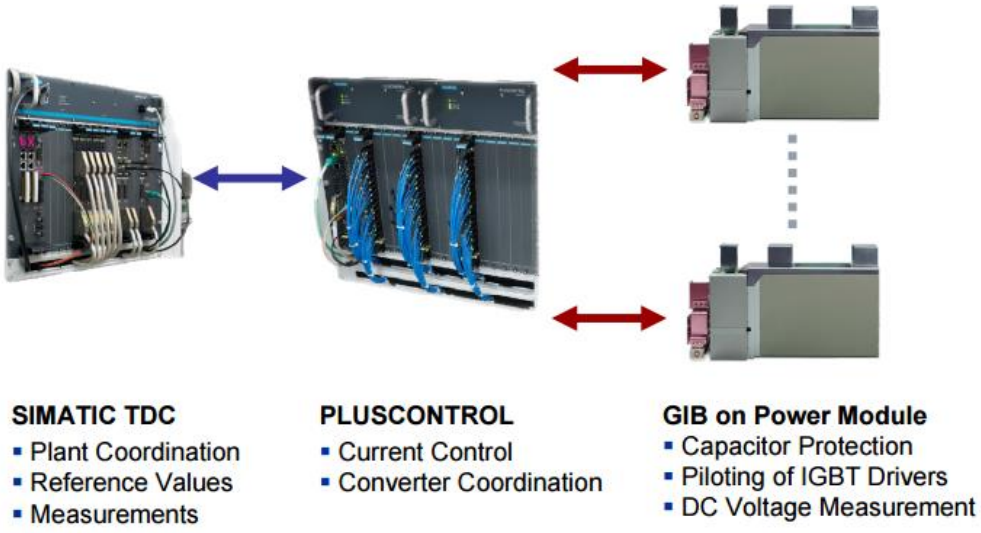


Figure 5.48 SVC PLUS advanced control system structure [74]

CHAPTER 6

CONCLUSION

Considering voltage source converters, technical limitations are encountered when higher voltage and power levels. Thus, Multilevel converter structures are emerged. The unique aspect of the multilevel converters can be pointed out as lower switching frequency due to low voltage stress on the power switches. Diode-clamped (Neutral-point-clamped), Flying capacitor (Capacitor-Clamped), Cascaded H-Bridge converters are represented in multilevel converter structures. However, the foot-print of the system in these multilevel converters are so high and higher efficiency is required. Hence, modular multilevel converter structure is proposed. Modular multilevel converter has some characteristic features such as modular and easy scalability structure for higher voltage and power level applications when compared to the other multilevel converters. Additionally, higher reliability is seen under faulty condition due to use of redundant submodule.

In this dissertation, Modular Multilevel Converter based STATCOM application in PSCAD environment is studied. Initially, Scalar PWM methods in high frequency switching including level-shifted carrier based PWM methods and phase-shifted carrier based PWM method are compared using equivalent switching count in a phase leg without any control structures. While comparing, N+1 level and 2N+1 level switchings were taken into consideration. Hereby, as the number of level is increased, performance of the MMC is getting better. Accordingly, among the level-shifted PWM methods, the lowest THD % value was obtained in PD-PWM method. Thus, PD-PWM method was preferred in direct modulation based sort and selection algorithm. On other hand, including to low frequency switching methods, Nearest Level Control structure was implemented to the MMC. Nevertheless, it was not included in to the comparison due to fundamental frequency switching property. Modular Multilevel Converter has many application areas. Between them, STATCOM is preferred in this thesis. Capacitor voltage balancing methods which are sort and selection method and Phase-shifted PWM based control method are

reviewed in MMC-STATCOM. Static mode and dynamic mode of the MMC-STATCOM are examined. Initially, a capacitive load whose capacitive reactive power is equal to - 5 MVAR, implemented to the MMC-STATCOM. Under capacitive loading condition, MMC-STATCOM is operated in inductive mode range. In this loading condition, Inductive reactive power is absorbed from the AC grid. Without MMC-STATCOM activated, the current signal of the grid stay ahead of the voltage signal of the grid around 90° out of phase which affect the power quality. Therefore, MMC-STATCOM was required and it was integrated to the system. As a result, grid side compensation was achieved about unity power factor. Secondly, an inductive load whose inductive reactive power was equal to 5 MVAR, implemented to the MMC-STATCOM. Under inductive loading condition, MMC-STATCOM was operated in capacitive mode range. Capacitive reactive power was released to the AC grid in capacitive mode range. Without MMC-STATCOM activated, the current signal of the grid lags behind the voltage signal of the grid around 90° out of phase which distorts the power quality. Accordingly, MMC-STATCOM was participated into the system and grid side compensation was succeeded in this application. Dynamic mode of the MMC-STATCOM was handled in this study. In here, transition from inductive mode range to the capacitive mode range was analyzed in both conditions, activated and deactivated of the MMC-STATCOM. Grid side voltage and current, active and reactive currents (i_d and i_q), DC link voltage and upper arm submodule capacitor voltages were evaluated in dynamic mode range.

Performance comparison analysis was done in MMC-STATCOM using submodule capacitor voltage balancing methods which are sort and selection method and phase-shifted PWM based control method. During comparison, inductive mode range and capacitive mode range of the MMC-STATCOM were discussed. As a conclusion, lower THD% value is acquired in phase-shifted PWM based control structure than direct modulation based sort and selection method both inductive mode and capacitive mode ranges. As a future work, Reduced switching frequency sort and selection method can be implemented to the MMC-STATCOM. Secondly, MMC-STATCOM can be tested under unbalanced loading condition. Thirdly, nearest level control method can be implemented to the MMC-STATCOM.

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[04.08.2016].

RESUME

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