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MODELING AND SIMULATION OF A CASCADED H-BRIDGE MULTILEVEL SINGLE SOURCE INVERTER

By

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APPROVAL PAGE

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

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This is to certify that I have read this thesis and that in my opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

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ABSTRACT

Multilevel inverters such as flying capacitor, diode-clamped, and cascaded H-bridge inverters are very popular particularly in medium and high power applications. This work focuses on a cascaded H-bridge module using a single DC source in order to generate an eleven-level output voltage, and eliminate 11^{th} order harmonic distortion. Two different cases have been investigated, the first case without isolation transformer while the second case with isolation transformer, and the later gives more accurate result, both the cases proved to be within desired result. The anticipated topology reduces the number of dc sources and switching elements. Different modulation techniques can be used for the multilevel inverter, but in this work features modulation techniques known as selective harmonic elimination (SHE) is utilized. This modulation technique reduces the number of carriers with reduction in Switching Losses, Total Harmonic Distortion (THD), and increases Power Quality (PQ). Based on the simulation result obtained for both cases, it appears SHE has the ability to eliminate selected harmonics by chopping off part of the fundamental component. The performance evaluation of the proposed cascaded multilevel inverter is done using PSIM and THD of 0.94% was obtained. Finally a laboratory experiment of 500 watt pulse width modulation 2-level power inverter was carried out.

Key words- Cascaded H-Bridge Inverter, Harmonic Elimination, Power Quality.

KASKAD H-KÖPRÜLÜ ÇOK SEVİYELİ TEK KAYNAKLI EVİRİCİLERİN MODELLEMESİ VE SİMÜLASYONU

Gaddafi Sani SHEHU

Yüksek Lisans Tezi – Elektrik ve Bilgisayar Mühendisliği
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Tez Yöneticisi: Prof. Dr. Tankut YALÇINÖZ

ÖZ

Çok seviyeli eviriciler olan uçan kapasitör, diyot-kenetli ve kaskad H-köprü eviriciler özellikle orta ve yüksek güç uygulamalarında çok popülerdirler. Bu çalışma, on bir - seviyeli çıkış gerilimi üretmek ve 11. mertebeden harmonik bozulmasını ortadan kaldırmak için tek DC kaynağı kullanarak bir kaskad H-köprü modülünü incelemektir. İki farklı durum incelenmiştir. Bu durumlardan ilkinde izolasyon trafosuz evirici daha sonraki durumda ise evirici izolasyon trafolu olarak incelenmiş ve ikinci durumda daha doğru sonuç vermiştir. Her iki durumda da eviricinin istenen sonuçları verdiği kanıtlanmıştır. Beklenen topoloji DC kaynaklarının ve anahtarlama elemanlarının sayısını azaltmıştır. Farklı modülasyon teknikleri çok seviyeli evirici için kullanılabilir, ancak bu çalışma da selektif harmonik eliminasyon (SHE) olarak bilinen modülasyon tekniği kullanıldı. Bu modülasyon tekniği taşıyıcıların sayısını azaltarak anahtarlama kayıplarını, toplam harmonik bozulmayı (THD) azaltır ve güç kalitesini artırır. Her iki durum için elde edilen simülasyon sonuçlarına göre, bu SHE temel bileşeninin parçalara bölmesi ile seçilen harmoniklerin ortadan kaldırma yeteneğine sahip olduğu görülmektedir. Önerilen kaskad çok seviyeli eviricinin performansı PSIM kullanılarak değerlendirilmiştir ve % 0.94 THD elde edilmiştir. Son olarak 500 wattlık tek fazlı darbe genişlik modülasyonlu 2-seviyeli güç eviricisinin deneysel bir laboratuvar çalışması yürütülmüştür.

Anahtar Kelimeler - Kaskad H-köprü Evirici, Harmonik Eliminasyon, Güç Kalitesi.

DEDICATION

To my late mother

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LIST OF SYMBOLS AND ABBREVIATIONS

SYMBOL/ABBREVIATION

Ω	Ohms
μ	Micro
μF	Micro farad
AC	Alternating current
C	Capacitor
DC	Direct current
F	Farad
Fig.	Figure
Hz	Hertz
IGBT	Insulated gate bipolar transistor
KA	Kilo ampere
KHz	Kilo hertz
KV	Kilo volt
L	Inductor
MOSFET	Metal oxide semiconductor field effect transistor
MW	Mega watt
R	Resistor
R_L	Load resistor
RC	Resistor-Capacitor
RL	Resistor-Inductor
RLC	Resistor-Inductor-Capacitor
V	Voltage

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

A multilevel inverter has a practical approach for eliminating harmonics from the output voltage; different topologies have been reported in the literatures [1-3]. The cascaded multilevel inverter with proper configuration can vigorously operate many of the application such as residential, industrial, renewable energy interface, and electric vehicles. Conventionally, each phase of a cascaded bridge requires "n" DC sources for 2n+1 level to produce desired level [4]. The problem of voltage unbalance that occurs in conventional multilevel inverter, for the application that required long cable and multiple dc sources, will be overcome with a proposed topology [5]. This work focuses of an 11-level cascade H-bridge multilevel inverter that utilized a single DC voltage source, for its operation to enhance eleven levels voltage steps. The topology is advantageous for high to medium power applications because it supplies sinusoidal voltage at higher switching frequencies with a low switching stress, and low total harmonic distortion (THD).

The multilevel inverters offer several advantages as compared to the hard-switched two-level pulse width modulation inverters, such as their capabilities to operate at high voltage with lower dv/dt per switching, high efficiency, low electromagnetic interference etc. [6]. To produce multilevel sinusoidal voltage output using single DC inputs, the semiconductor devices must be switched on and off in such a way that the fundamental voltage is obtained as desired along with the elimination of certain number of higher order harmonic, in order to have low harmonic distortion in the ac output voltage. For switching

the semiconductor devices, proper selection of switching angles is essential. The switching angles at fundamental frequency, in general, are obtained from the solution of nonlinear Transcendental equations characterizing harmonics contents in the output ac voltage; these equations are known as selective harmonic elimination (SHE) equations [7].

As the SHE equations are nonlinear transcendental in nature, their solutions may have simple, multiple and even no roots for a particular value of modulation index (m). Moreover, a big challenge is how to get all possible solution sets where they exist using simple and less computationally complex method. Iterative numerical techniques have been implemented to solve the SHE equation producing only one solution set, and even for this, a proper initial guess and starting value of modulation index for which the solution exists are required. In general, it is difficult to guess the initial solution and the value of modulation index for which solution exists [8].

Traditional method to determine the switching angles with less complexity are proposed in [9]. Once these solution sets are obtained, the switching angles producing minimum total harmonic distortion and power quality (PQ) in the output ac voltage are selected for switching the inverter [10]. Another important issue for the multilevel inverter is the more voltage steps, the less harmonic contents in its output. Increase the number of steps in an inverter not only result in additional number of components, but also result in a more complex control system [3]. Therefore it is a tradeoff between voltage steps and complexity of the inverter. In an effort to mitigate this problem, two schemes of 3^n and $3^{n-1}+2$ voltages were presented, where 'n' is the number of the individual H-bridge, each of the new scheme introduce has its advantage and draw back [4].

From Fig.1.1, the circuit comprises of three H-bridge inverter modules that are both supplied by a single DC source. Selective Harmonic Elimination (SHE) is the modulation technique used to control the IGBT such that each of the module generate three voltage level (+E, 0, -E) at certain specified time interval [10].

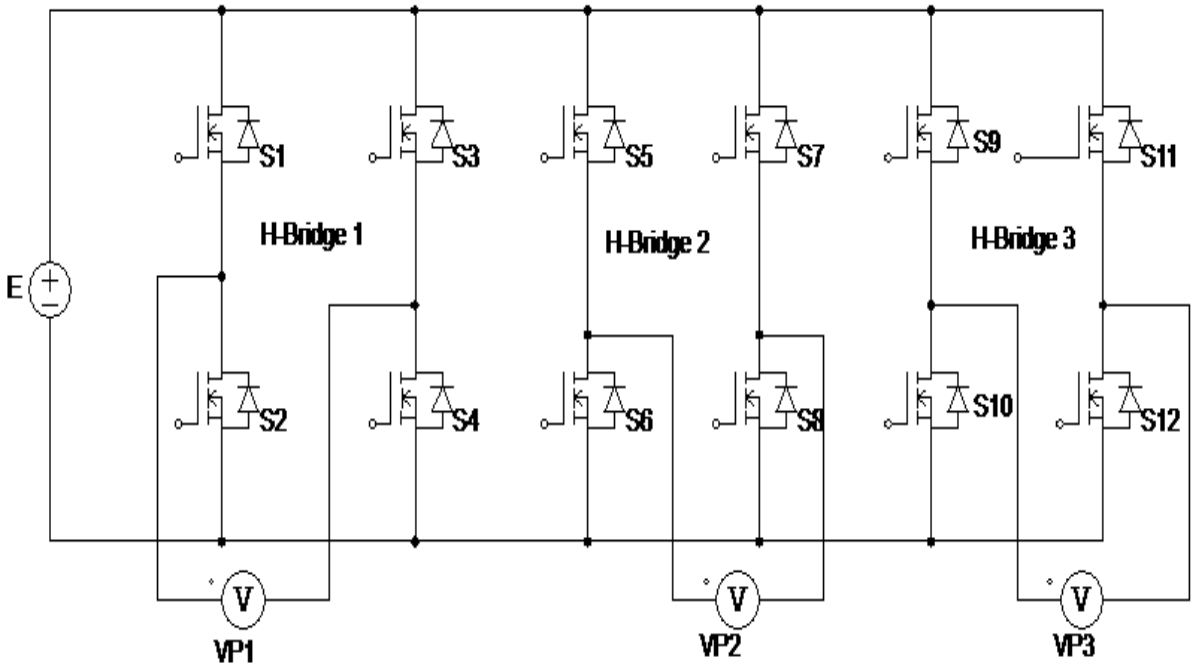


Fig.1.1 Propose Cascaded H-Bridge Multilevel Inverter

1.2 MOTIVATION

Numerous applications have begun to require higher power apparatus in recent years [1]. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power inverter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources interface. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application [7].

A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows:

● Staircase waveform quality: Multilevel inverters generate output voltages with very low distortion, also reduce the dv/dt stresses; thereby reducing electromagnetic compatibility (EMC) problems.

● Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [12].

● Input current: Multilevel converters can draw input current with low distortion.

● Switching frequency: Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM.

Unfortunately, multilevel inverters do have some disadvantages:

● One particular disadvantage of multilevel inverters is the greater number of power semiconductor switches needed, with each switch requiring a related gate driver circuit.

● Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple sources readily available. Although this disadvantage will be overcome or minimize with the proposed inverter.

1.3 OBJECTIVE OF RESEARCH

Fundamentally, this research work is based on developing a model of a modular structured cascaded H-bridge multilevel inverter with a single DC-source, based on selective harmonic elimination (SHE) Modulation Techniques. Mathematical model derivation will be carried out to show the switching angle of gating signals, and these angles will be carefully arranged so that better and quality power output will be produced.

A harmonic analysis will be carried out to justify the performance of the inverter under the proposed switching strategy. In order to validate the performance of the inverter, a simulation will be carried out using PSIM Software. The objectives of this research can be summarized as follows:

- To design and simulate an 11-level inverter using the cascaded H-bridge topology with a single DC source,
- To study the inverter output harmonic level using the SHE modulation technique,
- To study the inverters output voltage level and the total harmonic distortion under different load condition.

1.4 OUTLINE

This thesis comprises of six chapters; Chapter one is the introduction, objectives and outline. Chapter two is the literature review and present related issues to multilevel inverters, inverter topologies, and various modulation techniques available. Chapter three discusses the simulation software, modelling and control techniques used, and switching analysis. Also chapter four contains simulation result and discussion while Chapter five present experimental study. The last chapter is the conclusion and recommendation for future research work.

CHAPTER 2

LITERATURE REVIEW

2.1 OVERVIEW OF MULTILEVEL INVERTER

The concept of multilevel inverters has been introduced since 1975 [11]. The term multilevel began with the three-level inverter. Subsequently, several multilevel inverter topologies have been developed [1, 2]. However, the elementary concept of a multilevel inverter is to achieve higher power by the use of a series power semiconductor switches, with several lower voltage dc sources. The power conversion is performed by synthesizing a staircase voltage waveform as shown in Fig. 2.1. Different sources such as batteries, and renewable energy sources can be used bias the inverter, as either multiple or single sources.

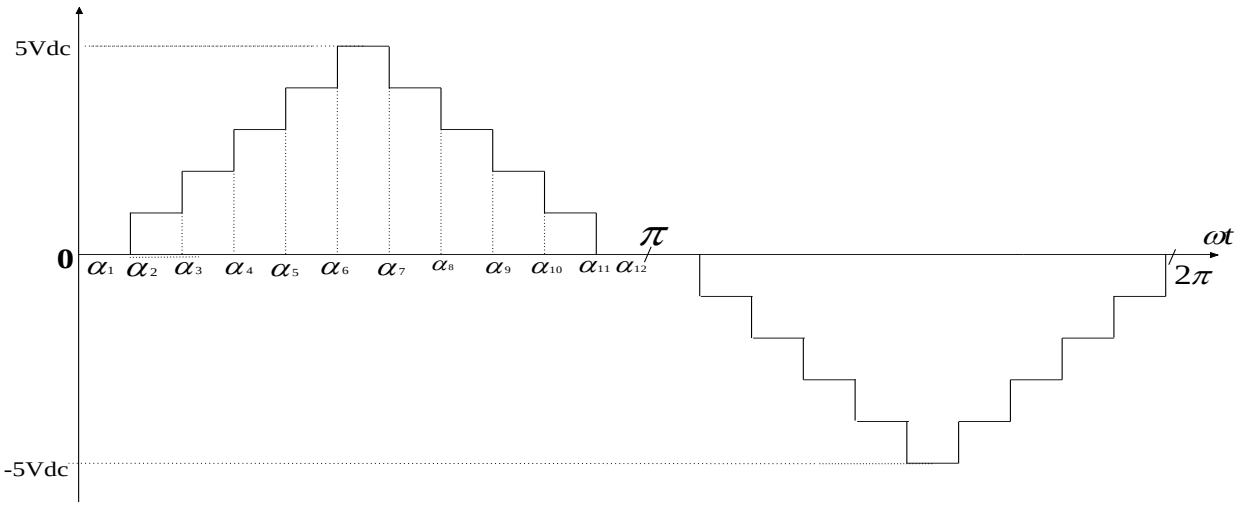


Fig. 2.1 waveforms and switching method of 11 level inverter

A continuous work to develop higher-voltage and higher-current power semiconductors to drive high power systems still goes on. In this way, the last-generation devices are suitable to support high voltages around 6.5 KV and currents of 2.5 KA) [2].

However, currently there is tough competition between the use of classic power converter topologies using high-voltage semiconductors and new inverter topologies using medium-voltage devices to level of 1 to 30 MW, and Voltage 34 KV [1]. Presently, multilevel inverters are a good solution for power applications due to the fact that they can achieve high power using mature medium-power semiconductor technology.

The most common multilevel inverter topologies are the neutral-point clamped inverter (NPC), flying capacitor inverter (FC), and cascaded H-bridge converter (CHB) [13-17]. These inverters can be classified as voltage source or current source inverters depend on its applications. Fig.2.2 shows classification of the inverter.

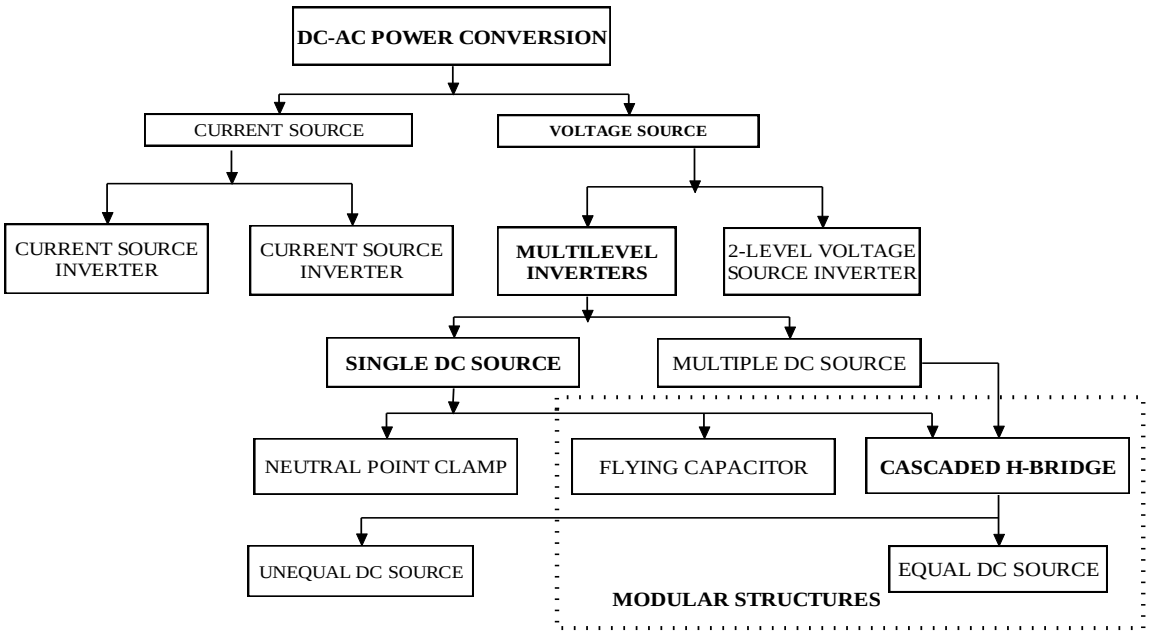


Fig. 2.2 High power conversion classification

In the 1980s, power electronics concerns were focused on the inverter power increase (increasing voltage or current) [15]. In fact, current source inverters were the main focus for researchers in order to increase the current. However, other research group began to work on the idea of increasing the voltage instead of the current. In order to achieve this objective, authors were developing new inverter topologies.

In 1981, Nabae et.al, presented the first NPC pulse width modulation (PWM) inverter, also named the diode-clamped inverter [15]. These multilevel inverters present

different characteristics compared with NPC, such as the number of components, modularity, control complexity, efficiency, and fault tolerance. Depending on the application, the multilevel inverter topology can be chosen taking into account these factors as shown in table 2.1.

Table 2.1 comparison of multilevel inverter factors [2]

COMPARISON OF MULTILEVEL INVERTER TOPOLOGY DEPENDING ON IMPLEMENTATION FACTORS			
Specific requirement	NPC	FC	CHB
	Clamping diode	Additional capacitor	Isolated dc sources
Modularity	Low	High	High
Design and implementation complexity	Low	Medium (capacitors)	High (input transformer)
Control concerns	Voltage balancing	Voltage setup	Power sharing
Fault tolerance	Difficult	Easy	Easy

These factors make multilevel inverters very attractive to the industry, and nowadays researchers all over the world are spending great efforts trying to improve multilevel inverter performances such as the control simplification, and the performance of different optimization algorithms in order to enhance the THD of the output signals, for power quality system [1, 2].

Moreover, abundant modulation techniques and control paradigms have been developed for multilevel inverters such as pulse width modulation (PWM), sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others.

This chapter reviews state of the art of multilevel power inverter technology, multilevel inverter structures and modulation paradigms are discussed including the pros and cons of each technique. Particular concentration is addressed in modern and more practical industrial applications of multilevel inverters.

2.2 APPLICATIONS OF MULTILEVEL INVERTERS

Multilevel inverters are today considered very attractive solution, for medium-voltage high-power applications. In fact, several major manufacturers commercialize NPC, FC, or CHB topologies with a wide variety of control methods, each one strongly depending on its application. Particularly, the NPC has found an important market in more conventional high-power ac motor drive applications like conveyors, pumps, fans, and mills, among others, which offer solutions for industries including oil and gas, metals, power, mining, water, marine [1-4]. A summary of multilevel inverter-driven applications and the topology involve is illustrated in Fig. 2.3.

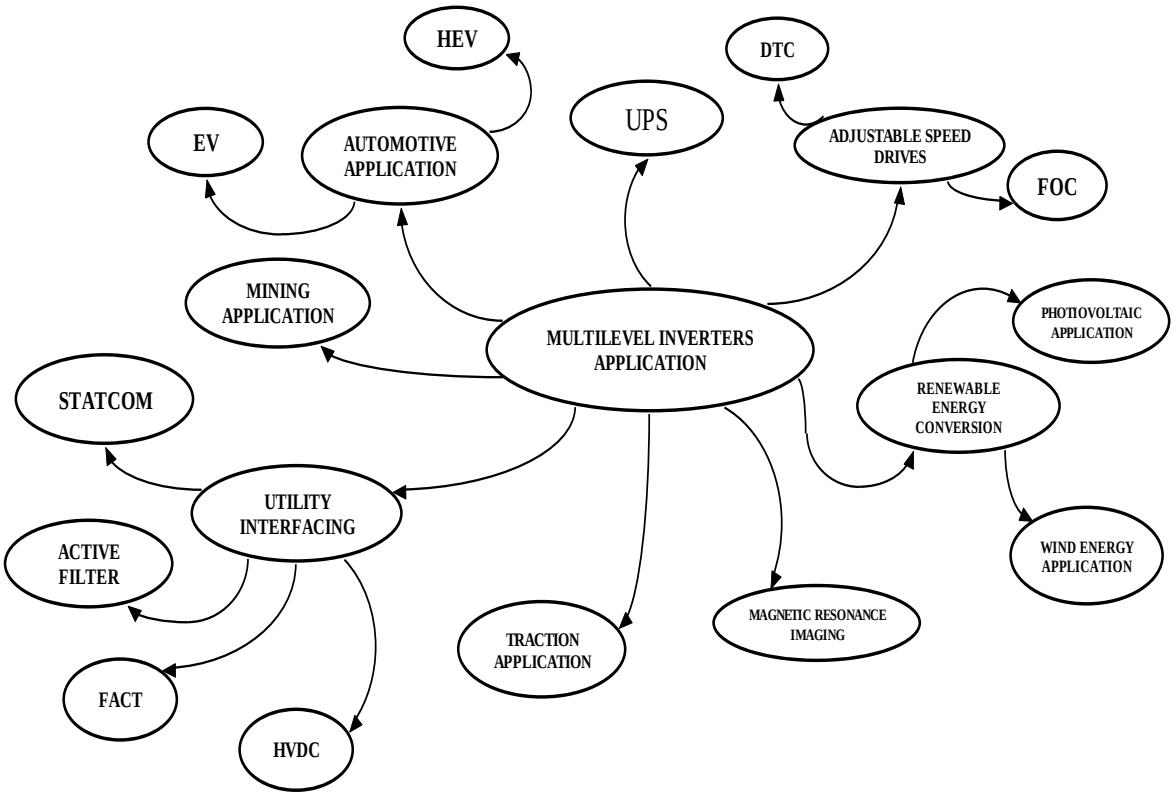


Fig. 2.3 multilevel inverter-driven applications overview

It's worth mention that, most of the stated inverter topologies can be used in any of the stated applications, though some specific topologies appear to be more efficiency and reliable in some specific area of applications [3].

2.3 TOPOLOGIES OF MULTILEVEL INVERTERS

As previously mentioned, three different major multilevel converter structures have been applied in industrial applications, and mention in several literature, cascaded H-bridges converter with separate dc sources, neutral-point clamped, and flying capacitors are three major multilevel inverter and used in various applications are briefly discussed.

2.3.1 Neutral-Point Clamped Multilevel Inverter (NPCMI)

The diode-clamped multilevel inverter uses capacitors in series to divide up the DC bus voltage into a set of voltage levels [17]. An example of a single-phase four-level Diode-Clamped Inverter is shown in Fig. 2.4. To produce N-levels of the phase voltage, an N-level diode-clamp inverter needs N-1 capacitors on the DC bus. Thus, for a four-level inverter the DC bus consists of three capacitors C_1, C_2 and C_3. For a DC bus voltage of Vdc, the voltage across each capacitor is Vdc/3. Consequently the voltage stress for each power device is limited to one capacitor voltage level Vdc/3, through the clamping diodes [18].

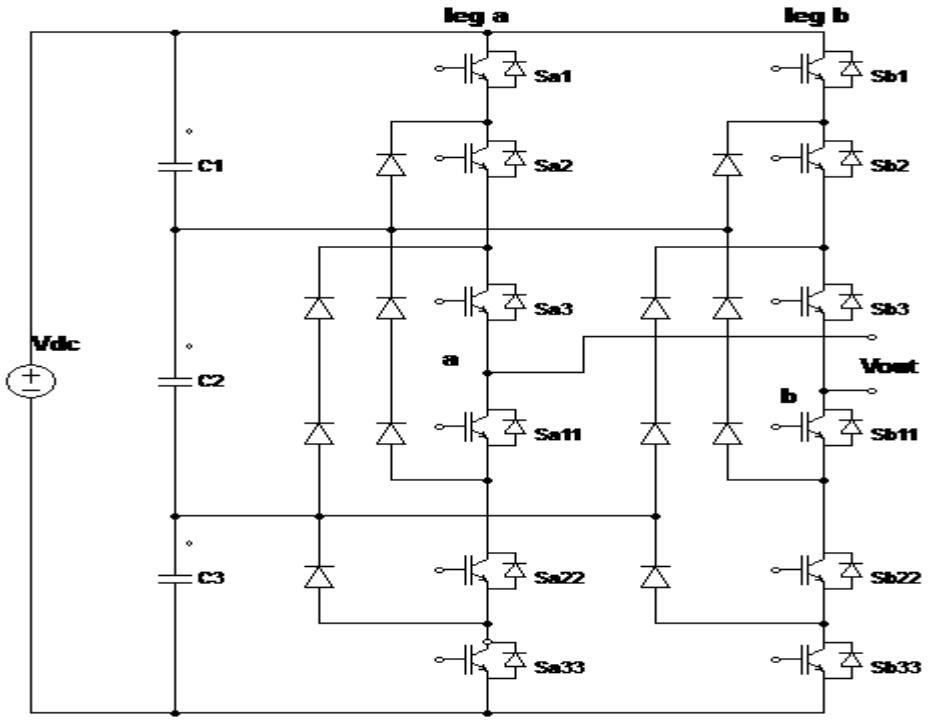


Fig. 2.4 single-phase four-level NPCMI [10]

The NPCMI output voltage synthesis is relatively straight forward, too explain how the staircase voltage is synthesized, point "o" is considered as the output voltage reference point. Using the four level inverter shown in Fig. 2.4 as an example, there are four switch combinations to generate four level voltages across "a" and "o".

(1) For voltage level $V_{ao} = V_{dc}$, all upper switches S_{a1} through S_{a3} are turned on.

(2) For voltage level $V_{ao} = 2V_{dc}/3$, two upper switches S_{a2} and S_{a3} and one lower switches S_{a11} are turned on.

(3) For voltage level $V_{ao} = V_{dc}/3$, the upper switches S_{a3} and two lower switches S_{a11} and S_{a22} turned on.

(4) For voltage level $V_{ao} = 0$, all lower switches S_{a11} through S_{a33} are turned on.

Table 2.2 Four-level DCMI voltage levels and their switch states [10]

Output Vao	Switch combination					
	S_{a1}	S_{a2}	S_{a3}	S_{a11}	S_{a22}	S_{a33}
V4 = Vdc	1	1	1	0	0	0
V3= 2Vdc/3	0	1	1	1	0	0
V2 = Vdc/3	0	0	1	1	1	0
V1 = 0	0	0	0	1	1	1

Advantages:

- All of the phases share a common DC bus, which minimizes the capacitance requirements of the inverter. For this reason, a back-to-back topology is practical to be implemented for high-voltage back-to-back inter-connection or an adjustable speed drive application.
- The capacitors can be pre-charged as a group.
- Efficiency is high for fundamental frequency switching.

Disadvantages:

- Real power flow is difficult for a single inverter because the intermediate DC levels will tend to overcharge or discharge without precise monitoring and control.
- The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.
- Not suitable for redundancy.

2.3.2 Flying Capacitor Multilevel Inverter (FCMI)

Meynard et al, introduced a flying-capacitor-based inverter in 1992. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place [17]. The circuit topology of the flying capacitor multilevel inverter is shown in Fig. 2.5. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Table 2.3 shows a list of all the combinations of phase voltage levels that are possible for the four-level, where '0'represent 'OFF' and '1' represent 'ON'.

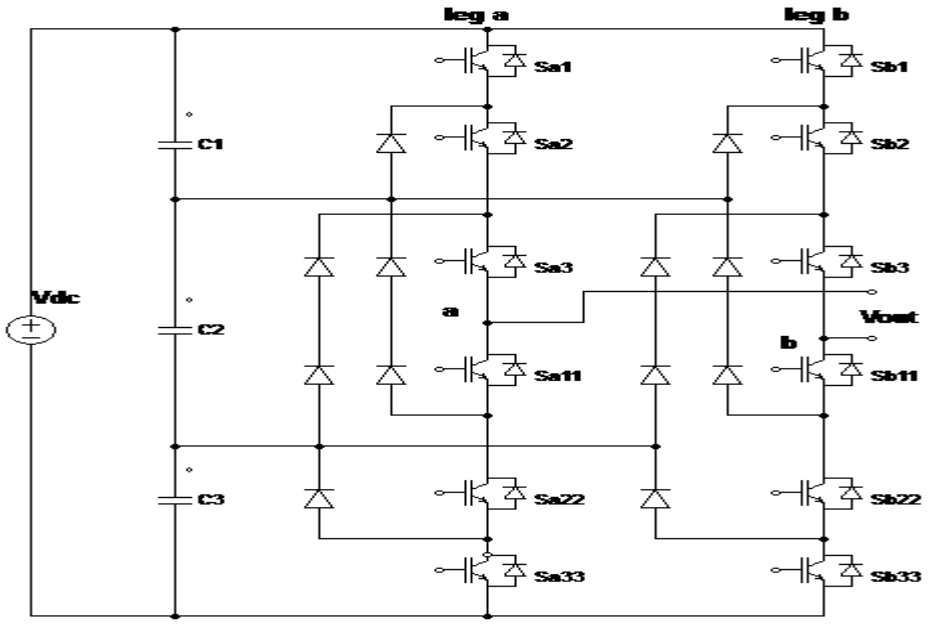


Fig. 2.5 Circuit diagram of single-phase four-level FCMI [10]

Unlike the diode-clamped inverter, the flying capacitor inverter does not require all of the switches that are on (conducting) be in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies [19]. These redundancies allow a choice of charging and discharging specific capacitors, and can be incorporated in the control system for balancing the voltages across the various levels.

Table 2.3. Possible switch combination for the four-level FCMI [10]

Output Vao	Switch combination					
	S_{a1}	S_{a2}	S_{a3}	S_{a11}	S_{a22}	S_{a33}
V4 = Vdc	1	1	1	0	0	0
8V3= 2Vdc/3	1	1	0	1	0	0
V2 = Vdc/3	1	0	0	1	1	0
V1 = 0	0	0	0	1	1	1

Several applications of FCMI as well as it is numerous advantages and disadvantages are reported in [18, 20].

Advantages:

- Phase redundancies are available for balancing the voltage levels of the capacitors.
- Real and reactive power flow can be controlled.
- The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.
- It requires a single isolated dc supply voltage source.

Disadvantages:

- Control is complicated to track the voltage levels for all of the capacitors. Also, precharging all of the capacitors to the same voltage level and startup are complex.
- Switching utilization and efficiency are poor for real power transmission.
- The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

2.3.3 Cascaded H-Bridge Multilevel Inverters (CHBMI)

The CHBMI conventionally required separate DC sources, and hence is well suited for various renewable energy sources such as photovoltaic, fuel cell and biomass. This configuration is also recently becomes very popular in AC power supply and adjustable speed drive applications [7]. A single-phase N-level configuration of such inverter is shown in Fig. 2.6. Each module consists of a separate DC source associated with a single-phase

full-bridge inverter. The terminal voltage of each module is connected in series to form an output voltage V_{out}. The output voltage is synthesized by the sum of each DC source from each module, i.e. V out = E_1+ E_2+ E_3 [21]. By different combinations of the four switches, S_{11} through S_{41}, each module can generate three different voltage outputs, +E, -E, and zero.

The number of output phase voltage levels is defined in different way from those of two previous inverters. In this topology, the number of module (*m*), which is equal to the number of DC sources required, depends on the number of levels (*n*) of the CHBMI. It is usually assumed that N is odd, as this would give an integer-valued M. The number of output phase voltage levels is defined by: *m= (n-1)/2* [22].

In another literature the number of output phase voltage levels *m* in a cascade inverter is defined by *m* = 2s+1, where s is the number of separate DC sources [3].

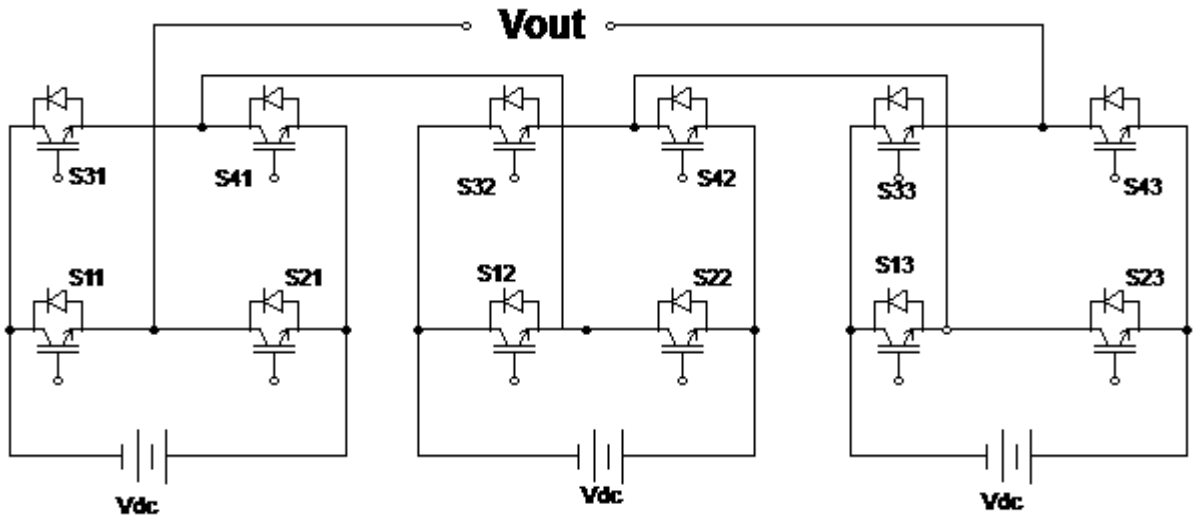


Fig. 2.6 Single-phase structure of a CHBMI

Fig. 2.6 shows a conventional seven-level modular Structured Inverter with three separate DC sources. There are many possible switch combinations that can synthesis stair case waveform for CHBMI. The number of switch combinations is proportional with the system's level (N). The relationship between the number of switch combinations and the system's level is expressed by [10]:

Number of voltage level $n = 2k + 1$ …… (2.1)

Where *n* is the number voltage steps and k is the number of independent DC source

Number of switch combinations = 2^{n-1} …… (2.2)

For example, the number of switch combinations for seven-level inverter is 64 different configurations. Hence, the flexibility in voltage synthesizing for this topology is more than NPCMI and FCMI. As illustrated in Fig. 2.6, this topology requires the least number of components among all multilevel inverters discuss earlier to achieve the same voltage levels. Table 2.4 lists a possible combination of the voltage levels and their corresponding switch states.

Table 2.4 Possible switch combination for MSMI based seven-level inverter [27]

LOAD VOLTAGE	+3E	+2E	+E	0	+E	+2E	+3E
S_{11}	1	1	1	1	0	0	0
S_{21}	0	0	0	1	1	1	1
S_{31}	0	0	0	0	1	1	1
S_{41}	1	1	1	0	0	0	0
S_{12}	1	1	1	1	0	0	0
S_{22}	0	0	1	1	0	1	1
S_{32}	0	0	0	0	1	1	1
S_{42}	1	1		0	1	0	0
S_{13}	1	1	1	1	0	0	0
S_{23}	0	1	1	1	0	0	1
S_{33}	0	0	0	0	1	1	1
S_{43}	1	0	0	0	1	1	0

In addition this topology can avoid extra clamping diodes or voltage balancing capacitors. Moreover modularized circuit layout and packaging are possible because each level has a standard structure. However, with the need of separate DC sources for real power conversions, the application of cascaded inverter can be somewhat limited [4].

Advantages:

- There is automatic voltage sharing across the switches in a module due to the usage of independent voltage sources. Therefore, reduces restriction in the switching sequence.
- The number of possible output voltage levels is more than twice the number of DC sources (n = 2k + 1).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages:

- Separate dc sources are required for each of the H-bridges. This will limit its application, and increase the device cost and size.

2.4 OTHER MULTILEVEL INVERTER STRUCTURES

Besides the three basic multilevel inverter topologies previously discussed, other multilevel converter topologies have been proposed [20]; however, most of these are "hybrid" circuits that are combinations of two of the basic multilevel topologies or slight variations to them. Additionally, the combination of multilevel power converters can be designed to match with a specific application based on the basic topologies. In the interest of completeness, some of these will be identified and briefly described.

2.4.1 Generalized Multilevel Topology

Existing multilevel converters such as diode-clamped and capacitor-clamped multilevel inverters can be derived from the generalized converter topology called P2 topology proposed by Peng [21], as illustrated in Fig. 2.7. The generalized multilevel inverter topology can balance each voltage level by itself regardless of load characteristics, active or reactive power conversion and without any assistance from other circuits at any number of levels automatically. Thus, the topology provides a complete multilevel topology that embraces the existing multilevel converters in principle.

Fig. 2.7 shows the P2 multilevel inverter structure per phase leg, each switching device, diode, or capacitor's voltage is 1V. Any inverter with any number of levels, including the conventional bi-level converter can be obtained using this generalized topology [3, 21].

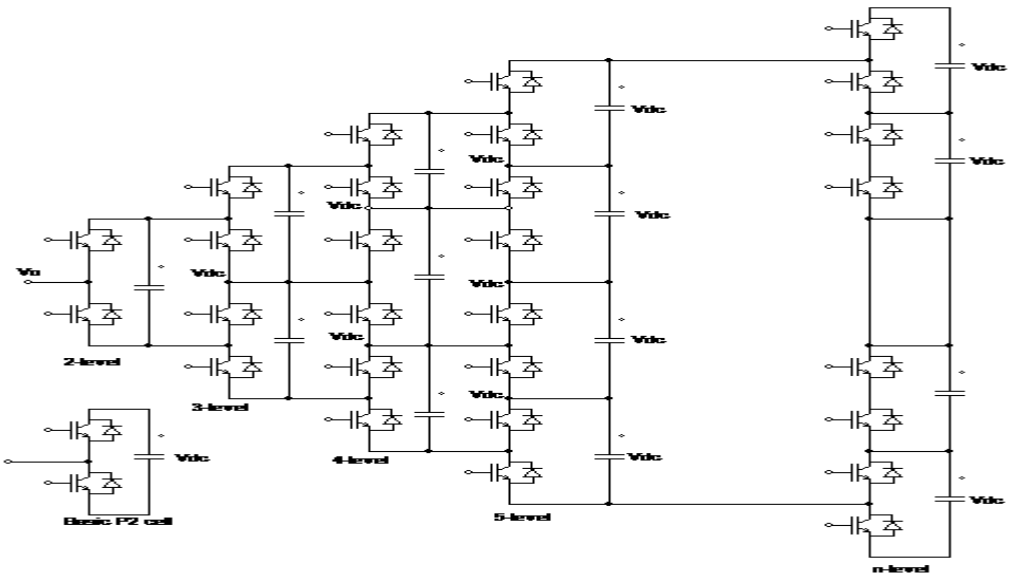


Fig. 2.7 Generalized P2 multilevel converter topology for one phase leg. [21]

2.4.2 Mixed-Level Hybrid Multilevel Inverter

To reduce the number of separate DC sources for high-voltage, high-power applications with multilevel inverters, diode-clamped or capacitor-clamped inverters could be used to replace the full-bridge cell in a cascaded inverter. The Fig. 2.8 shows the nine-level cascade inverter integrates a three-level diode-clamped inverter as the cell. The original cascaded H-bridge multilevel inverter requires four separate DC sources for one phase leg and twelve for a three-phase inverter. If a five-level inverter replaces the full-bridge cell, the voltage level is efficiently doubled for each cell [22]. In order to achieve the same nine voltage levels for each phase, only two separate DC sources are needed for one phase leg and six for a three-phase inverter [4]. The configuration has mixed-level hybrid multilevel units because it embeds multilevel cells as the building block of the cascade inverter. The advantage of the topology is, it needs less separate DC sources, while the disadvantage of this topology is complicated control strategy due to its hybrid structure.

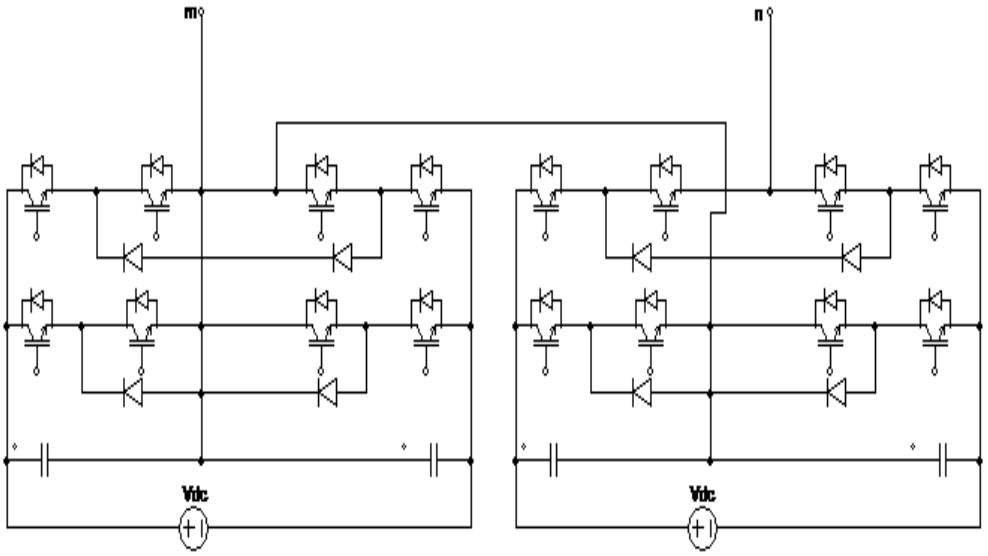


Fig.2.8 Mixed-level hybrid configuration using the three-level diode-clamped inverter [4].

2.4.3 Back-To-Back Diode-Clamped Inverter

Two multilevel inverters can be connected in a back-to-back procedure and then the arrangement can be connected to the electrical system in a series-parallel plan as shown in Fig. 2.9, Both the current needed from the utility and the voltage supplied to the load can be controlled at the same time. This series-parallel active power filter has been referred to as a universal power conditioner [18, 22], when used on electrical distribution systems and as a universal power flow controller [23] when applied at the transmission level.

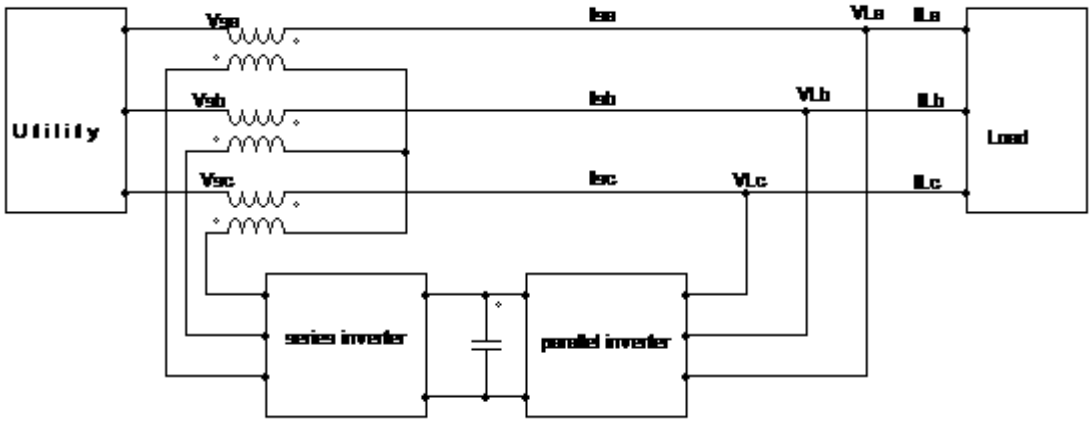


Fig.2.9 Series-parallel connection to electrical system of two back-to-back inverters [18].

2.4.4 Soft-Switched Multilevel Inverter

The soft-switching methods can be realized for diverse multilevel inverters to reduce the switching loss and to increase efficiency. For the cascaded inverter, because each inverter cell is a bi-level circuit, the implementation of soft switching is not at all different from that of conventional bi-level inverters. For a flying capacitor or neutral point clamped inverters, soft-switching circuits have been proposed with different circuit arrangements. One of soft switching circuits is a zero-voltage-switching type which includes auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations [4, 21] as shown in Fig. 2.10.

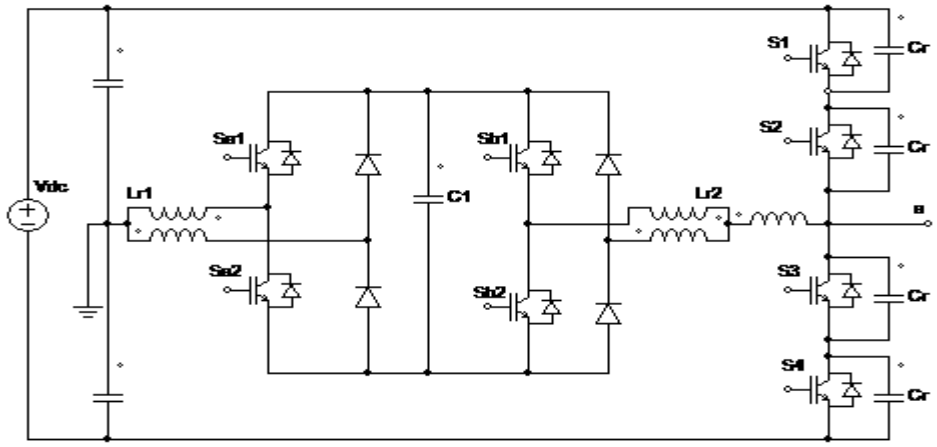


Fig. 2.10 Zero-voltage switching capacitor-clamped inverter circuit [4].

2.5 MULTILEVEL INVERTER MODULATION TECHNIQUES

Multilevel inverter modulation and control systems have attracted much exploration and progress over the last decade [1, 2]. Among the motives are the challenge to extend traditional modulation methods to the multilevel inverter case, the inherent of extra complexity of having more power electronics devices to control, and the likelihood to take advantage of the extra degrees of freedom provided by the additional switching states generated by these topologies. As a result, a large total number of different modulation algorithms have been established, each one with exclusive structures and problems, depending on the application [18].

A classification of the modulation methods for multilevel inverters is presented in [24]. The modulation algorithms are divided into two main groups depending on the

domain in which they operate, the state-space vector domain, in which the operating principle is based on the voltage vector generation, and the time domain, in which the method is based on the voltage level generation over a time frame. In addition, the different methods are labeled depending on the switching frequency they produce.

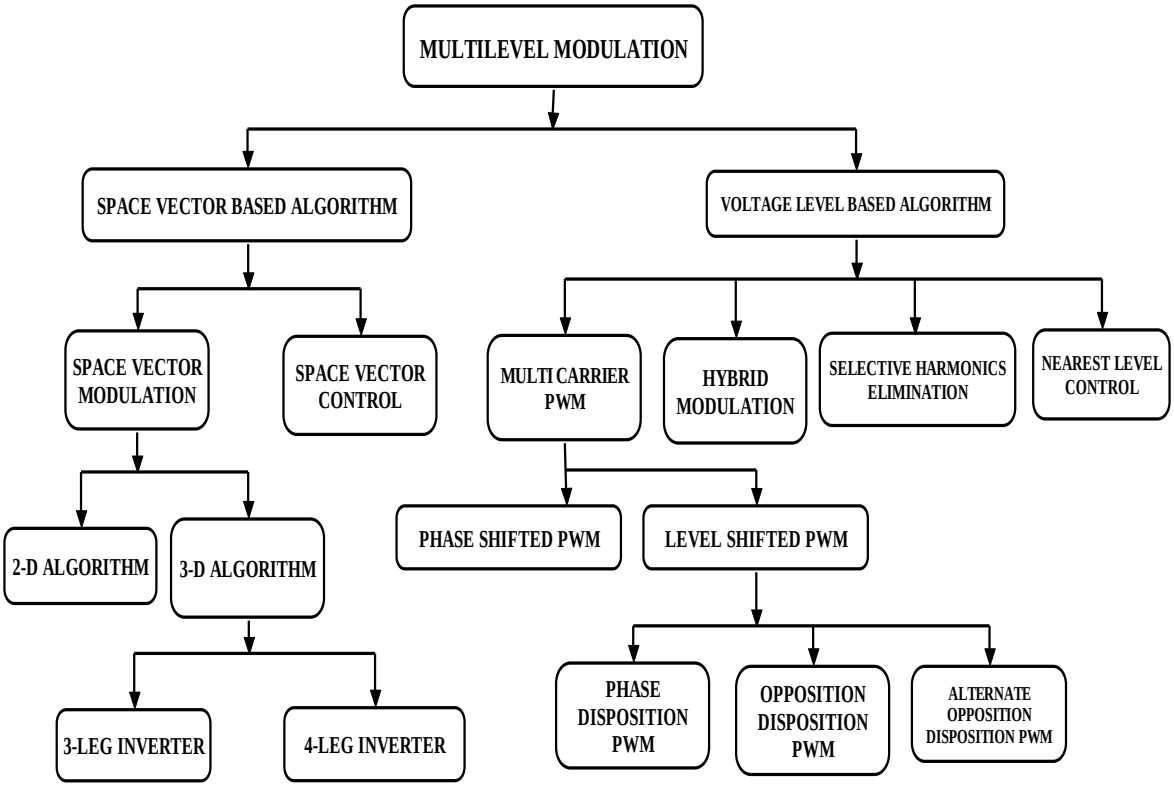


Fig. 2.11 Multilevel inverter modulation classification

In addition, in Fig. 2.11 the different methods are labeled depending on the domain to which the assign to operated [1]. The three multilevel PWM methods most discussed in the literature have been multilevel carrier-based PWM, selective harmonic elimination, and multilevel space vector PWM; all are extensions of traditional two-level PWM strategies to several levels [4].

2.5.1 Multilevel Inverter Carrier-Based PWM

The Fig.2.12 shows conventional pulse width modulation techniques have been modified and extended to control multilevel inverter topologies. This technique is called multilevel PWM because it uses more than one carrier signal to generate the control signal [10], [29].

Numerous different two-level multilevel carrier-based PWM techniques have been extended by previous authors as a means for controlling the active devices in a multilevel inverter. The most common and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase. Fig. 2.12 illustrates one of the three carrier-based techniques used in conventional inverter that can be applied in a multilevel inverter: sinusoidal PWM (SPWM), third harmonic injection PWM (THPWM), and space vector PWM (SVM). SPWM is a very popular method in industrial applications [26].

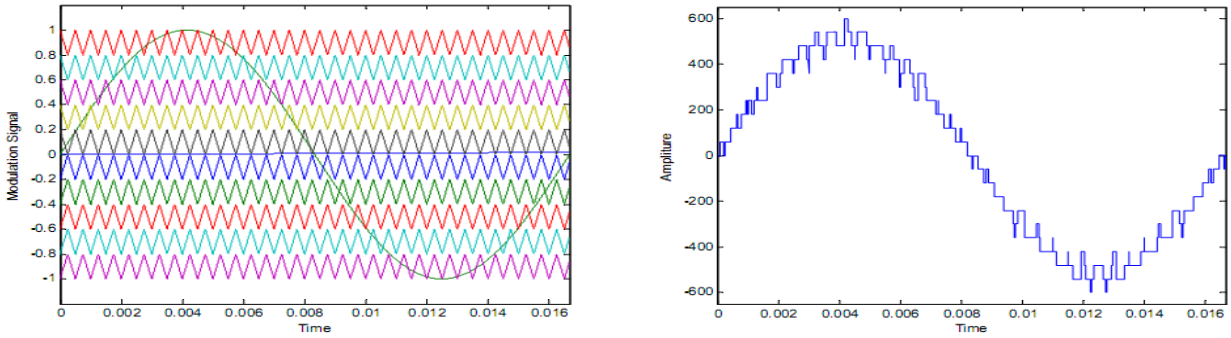


Fig. 2.12 Sinusoidal PWM (SPWM) and the output waveform [4]

In order to achieve better dc link utilization at high modulation indices, the sinusoidal reference signal can be injected by a third harmonic with a magnitude equal to 25% of the fundamental [4]. The dc utilization means the ratio of the output fundamental voltage to the dc link voltage. Other interesting carrier-based multilevel PWM are sub harmonic PWM (SHPWM) and switching frequency optimal PWM (SFO-PWM) [3].

Another method of multilevel inverter carrier-based PWM is level shift PWM (LS-PWM), it is achieved by super imposing the carrier signal on one another. This method is further classified into three based on the carrier signal orientation. The three sub-classes are alternate phase opposition (APOD), phase opposition disposition (POD-PWM) and phase disposition (PD) [4].

2.5.2 Multilevel Space Vector PWM

Choi [14] was the first author to extend the two-level space vector pulse width modulation technique to more than three levels for the diode-clamped inverter. Most of the techniques presented are precisely designed for a particular number of inverter levels.

In this modulation technique, a reference voltage (V_{ref}) is expressed in a vector form and by matching it with discrete switching states, the reference voltage simulated at the inverter output [26]. The space vector modulation (SVM) algorithm is basically a PWM strategy with the difference switching times, which are computed based on the three phase space vector representation of the reference and the inverter switching states rather than the per-phase in time representation of the reference and the output levels as in previous analyzed methods [27]. As the number levels increases, the complexity in the algorithm and mathematical computation also increase [10]. Fig.2.13 shows three-level space vectors voltage for a three-level inverter plane.

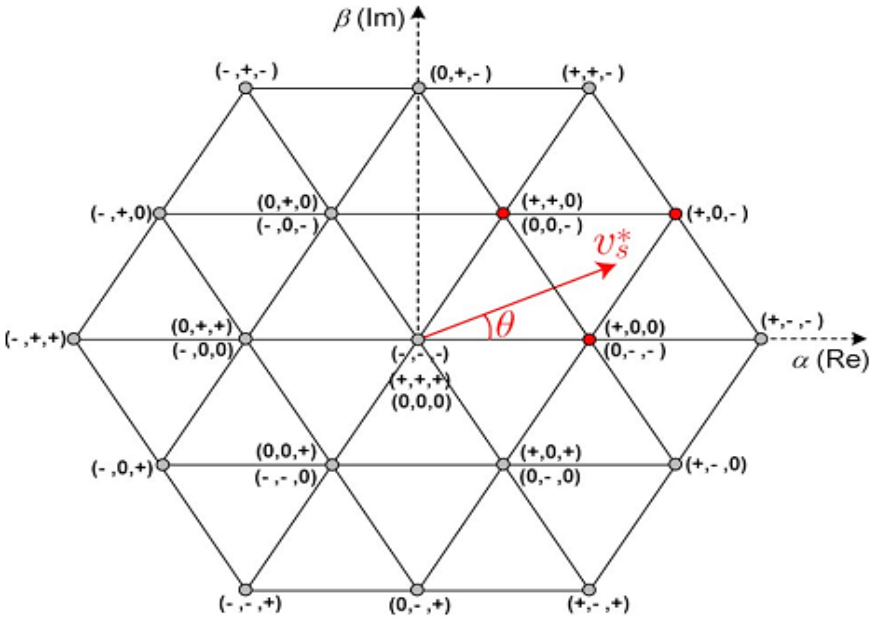


Fig. 2.13 Three-level plane voltage space vectors for a three-level inverter [1]

In the Fig. 2.13, for example the zero vector can be obtained in three way: connecting three phase output to the positive bus bar (Va = Vb = Vc = +Vdc), corresponding to the switching state (+, +, +); or to the neutral point (Va = Vb = Vc = 0), corresponding to the state (0, 0, 0); or to the negative bus bar (Va = Vb = Vc = -Vdc), corresponding to the switching state (-, -, -) [27].

In a research carried out by Franquelo et al, a new algorithm was presented which uses simple mathematical procedure to compute the use of lookup tables, co-ordinate or trigonometry [28]. Another advantage of this space vector modulation (SVM) technique is it addresses the issue of increased computation level.

2.5.3 Selective Harmonic Elimination (SHE-PWM)

Inverters for very high-power applications are usually controlled with low switching frequency algorithms, below 1 kHz at lower modulation index (m< 1), but can be extended to higher frequency for higher modulation index (m> 3) [10, 27]. Selective harmonic elimination SHE, is a low switching frequency PWM method developed for traditional inverters in which a few switching angles per quarter fundamental cycle are predefined and precalculated via Fourier analysis to ensure the elimination of undesired low-order harmonics [32].

Principally, in selective harmonic elimination, the Fourier coefficients or harmonic components of the predefined switched waveform with the unknown switching angles are made equal to zero for those undesired harmonics, while the fundamental component is made equal to the desired reference amplitude at certain modulation index. This set of equations is solved offline using numerical methods to obtaining a solution for the switching angles. The concept has also been extended for multilevel waveforms and is usually applicable to open loop system [29, 30].

With *m* switching angles in a quarter-cycle, *m* control degrees of freedom are obtained, from which *(m*-1) can be used to eliminate undesired harmonics and the last one to control the amplitude of the fundamental component for reference tracking [29]. As with traditional SHE, this can be achieved by computing the corresponding coefficient Fourier series expression of the output waveform, which happens to be a non-linear transcendental equation below.

$$Hn = \begin{cases} \frac{4E}{n\pi}\sum_{k=1}^{m}(\cos n\alpha k) & for\ odd\ n \\ 0, & for\ even\ n \end{cases} \quad \ldots\ldots\ldots\ldots\ldots \quad (2.3)$$

Where Hn the harmonic of the amplitude waveform and α is is the switching angles. Note that $\alpha_1 < \alpha_2 < \alpha_3 < \ldots\ldots\ldots < \alpha_m < \pi/2$, the harmonics that will be eliminated are set to zero. With this operation a voltage depict in Fig. 2.14 will be realize.

The principal limitation with the application of SHE-PWM techniques has be the difficulty in solving the non-linear equations associated in the harmonic elimination approach. These equations contain trigonometric terms, are transcendental in nature and therefore exhibit multiple solutions

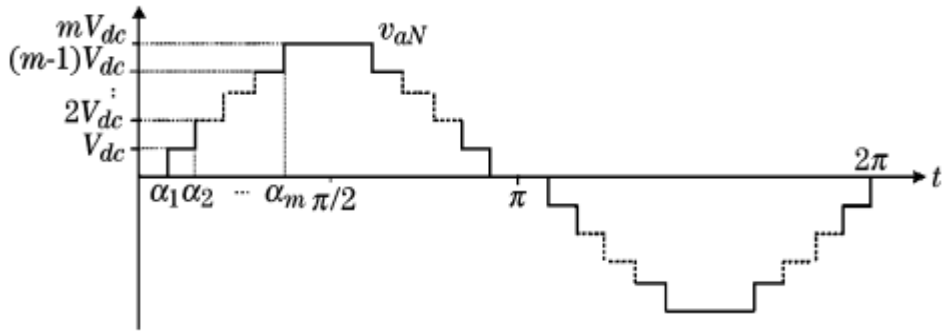


Fig. 2.14 Multilevel selective harmonic elimination waveform

To obtain convergence with numerical techniques which involve iterative procedures as in Newton Raphson method, the starting values must be selected considerably close to the exact solution [17]. Mathematical resultant method which uses the concept of polynomials, optimization techniques or hybrid genetic algorithm, can be used to approximate the switching angles [32]. The drawback of this method is it restriction to open loop systems and the complexity in finding the switching for a higher number of levels.

CHAPTER 3

MODELING AND CONTROL

3.1 POWERSIM

Powersim (PSIM) is a simulation software specifically designed for power electronics and motor drives. With fast simulation and friendly user interface, PSIM provides a powerful simulation environment for power electronics, analog and digital control, magnetics, and motor drive system studies [33].

PSIM includes the basic package, as well as the following add-on options:

Motor Drive Module, SimCoder[2] Module, Digital Control Module, Renewable Energy Package SimCoupler Module, MagCoupler Module, Thermal Module, and MagCoupler-RT Module

- ✓ The Motor Drive Module: has built-in machine models and mechanical load models for motor drive system studies.
- ✓ The Digital Control Module: provides discrete elements such as zero-order hold, z-domain transfer function blocks, quantization blocks, digital filters, for digital control system analysis.
- ✓ The SimCoupler Module: provides interface between PSIM and Matlab/Simulink[3] for co-simulation.
- ✓ The Thermal Module: provides the capability to calculate semiconductor devices losses.
- ✓ The MagCoupler Module: provides interface between PSIM and the electromagnetic field analysis software JMAG[4] for co-simulation.
- ✓ The MagCoupler-RT Module: links PSIM with JMAG-RT[4] data files

- ✓ The SimCoder Module: provides automatic code generation capability for DSP hardware.

In addition, PSIM supports links to third-party software through custom DLL blocks, Fig. 3.1 shows the overall PSIM environment.

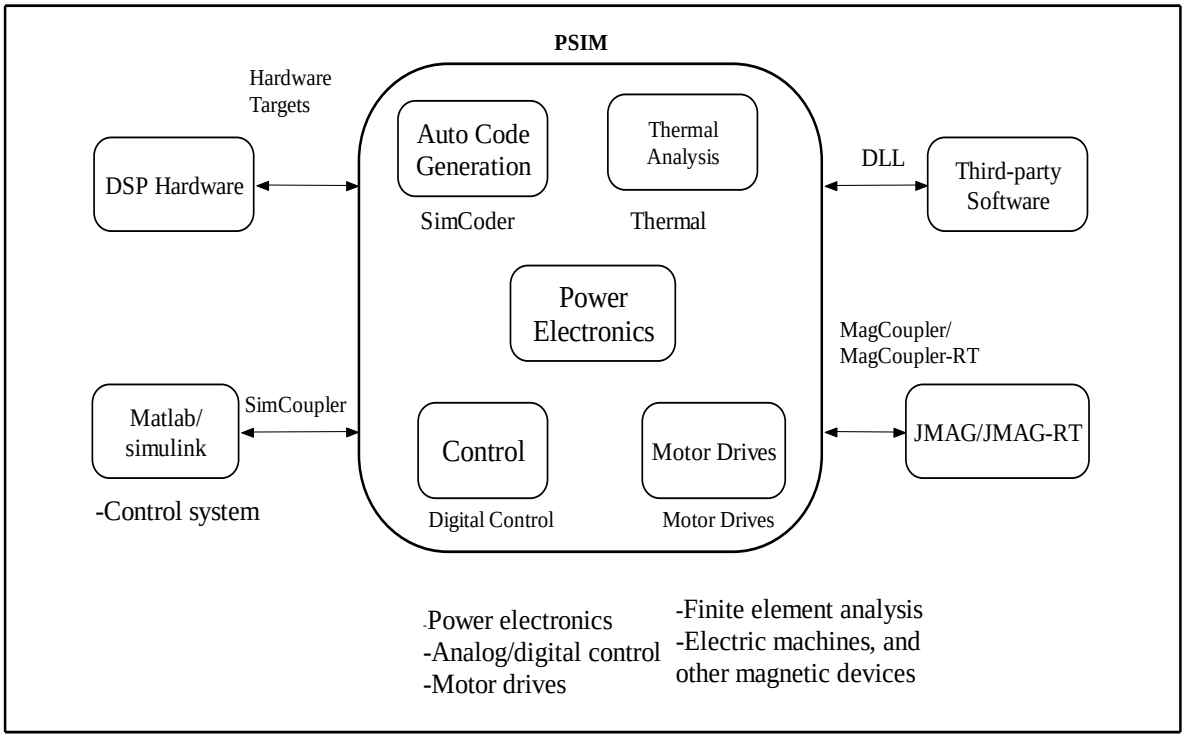


Fig. 3.1 PSIM general information structure [34]

The PSIM simulation environment consists of the circuit schematic program PSIM, the simulator engine, and the waveform processing program Simview. PSIM is one of the fastest simulators for power electronics simulation. It achieves fast simulation while retaining excellent simulation accuracy. This makes it particularly efficient in simulating converter systems of any size, and performing multiple-cycle simulation [33].

PSIM can simulate control circuit in various forms: in analog circuit, s-domain transfer function block diagram, z-domain transfer function block diagram, custom C code, or in Matlab/Simulink. PSIM's control library provides a comprehensive list of components and function blocks, and makes it possible to build virtually any control scheme quickly and conveniently.

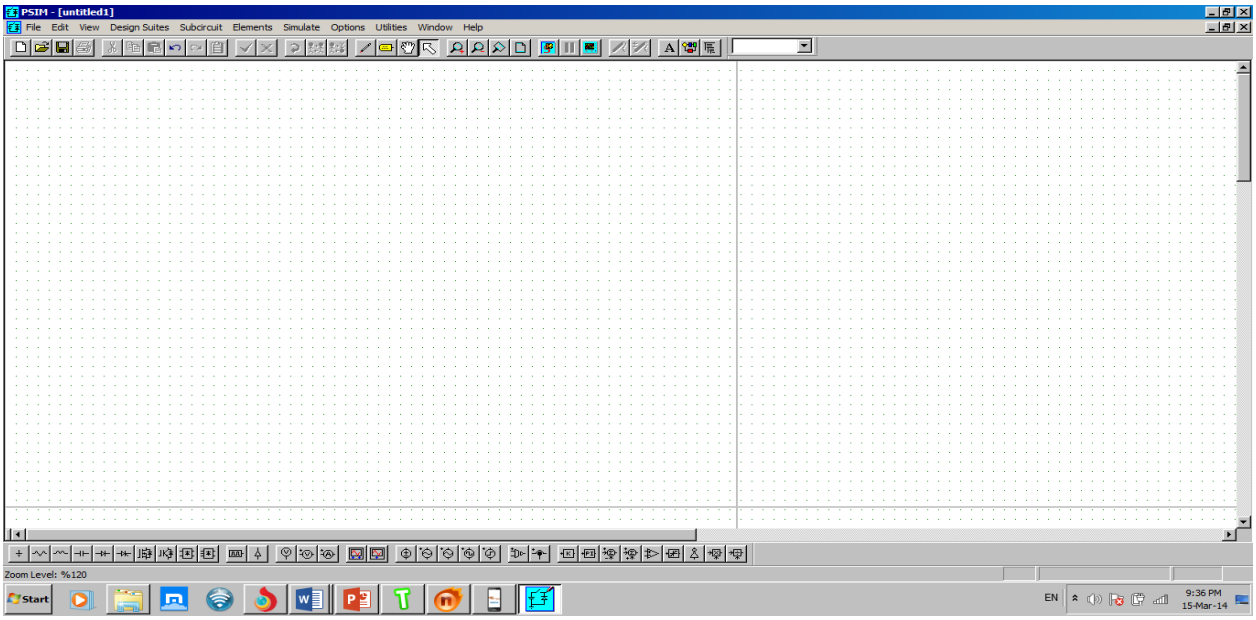


Fig. 3.2 PSIM simulation environment

PSIM is the engine of the simulation environment. It uses a strong algorithm dedicated to electrical circuits (piecewise method, generic models and a fixed time-step).

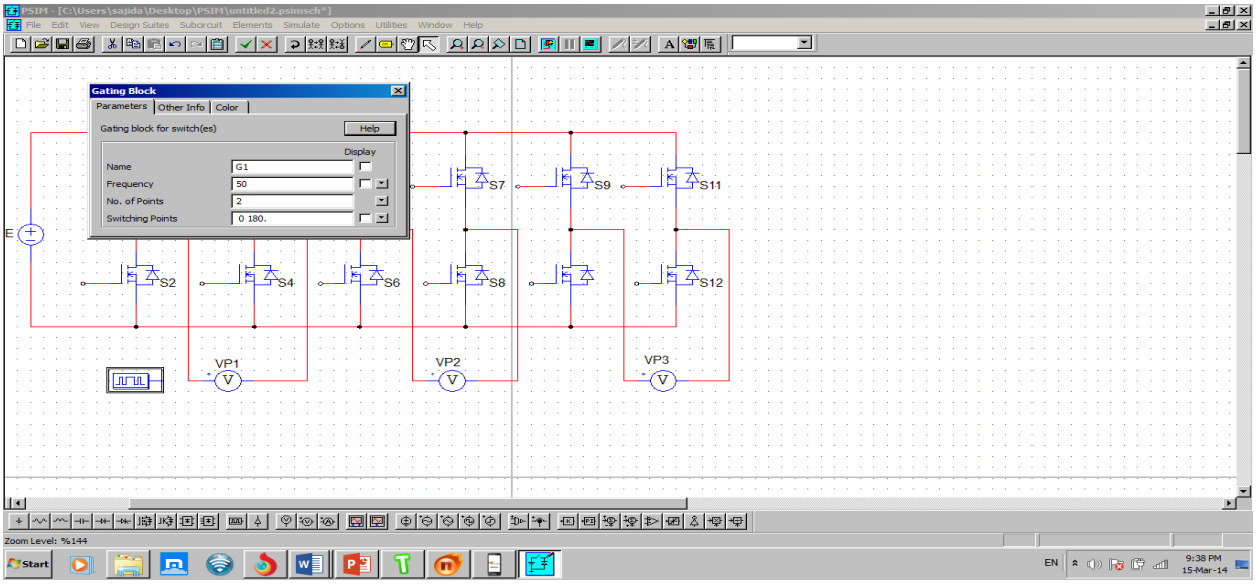


Fig. 3.3 PSIM simulation environment with displaying power component

The fast simulation tolerates repetitive simulation runs and considerably reduces the design cycle. Simulation results are displayed and evaluated in Simview as shown in the Fig. 3.4 and 3.5.

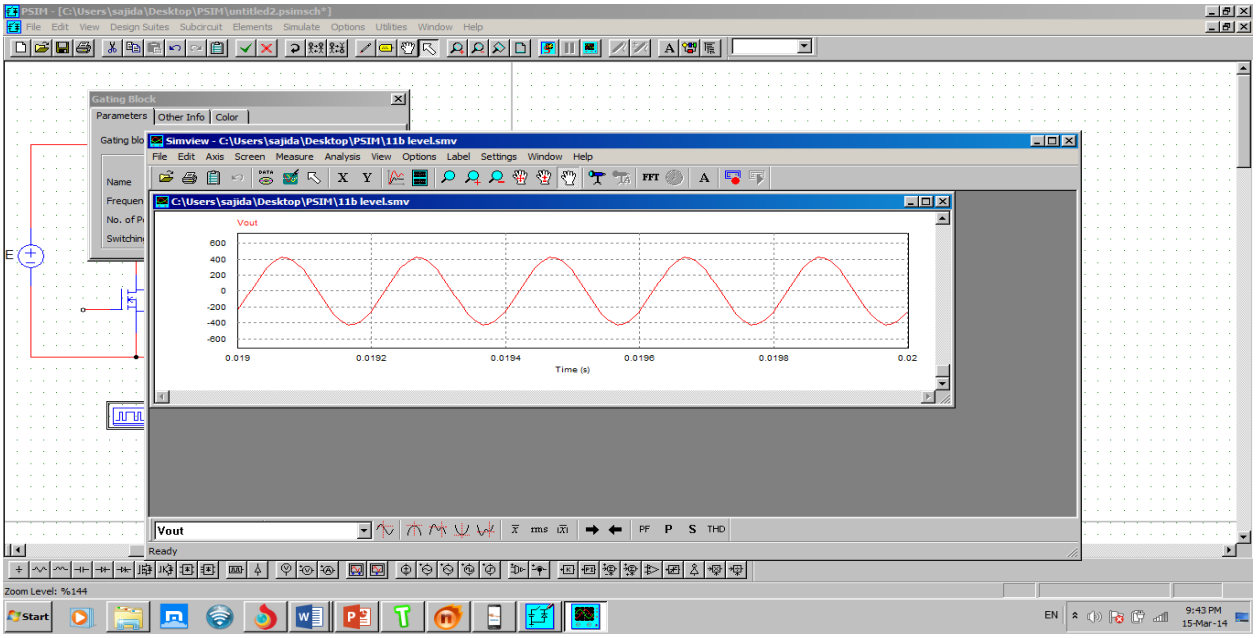


Fig. 3.4 PSIM simulation Simview

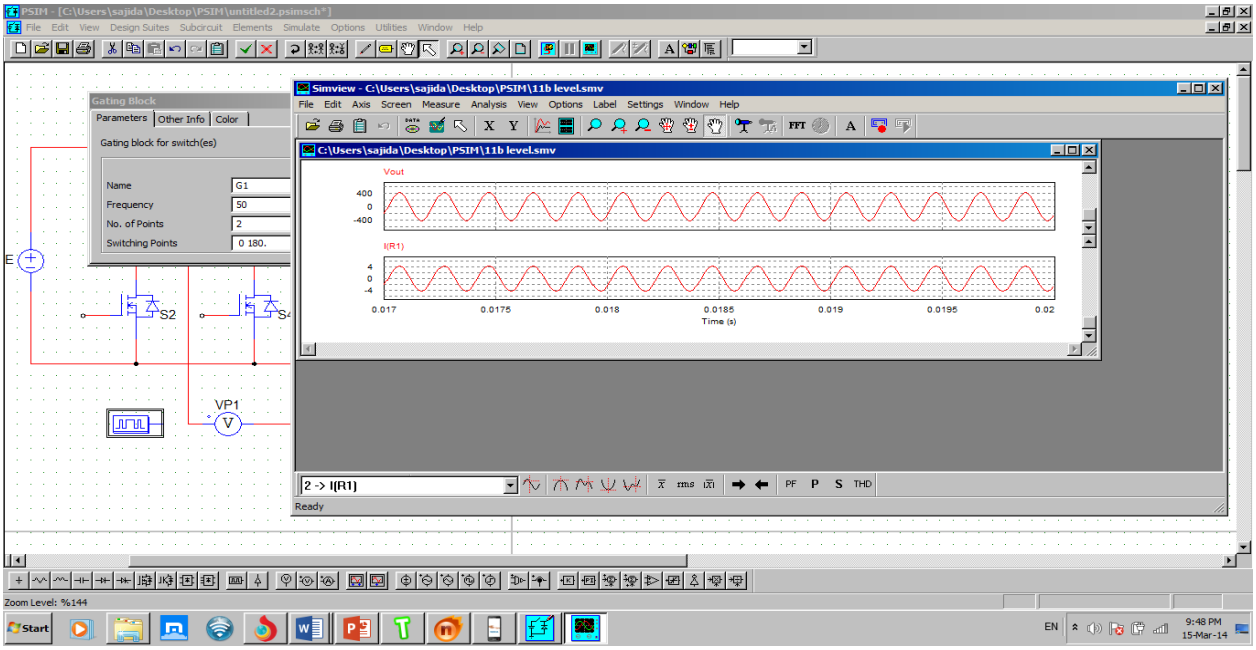


Fig. 3.5 PSIM simulation Simview with multiple results

Several waveform processing functions, such as multiple screens and line styles, are provided. Post-processing functions such as addition/subtraction and average/rms value calculation are also provided [34]. PSIM runs in Microsoft Windows XP/Vista on personal computers. The minimum RAM memory requirement is 128 MB.

3.1.1 Powersim Simulation Component

3.1.1.1 Power Electronic Switch

The MOSFET switch devices used in this research, are voltage-controlled and not current-controlled, and have a positive temperature coefficient, stopping thermal runaway. The on-state-resistance has no theoretical limit; hence on-state losses can be far lower. The device also has a body-drain diode, which is particularly useful in dealing with limited freewheeling currents [33]. The positive features of high current and voltage rating, high switching speed, low losses, short circuit withstand capability and easily driven gate source junction [42]. Self-commutated switches, in the switch mode except PNP bipolar junction transistor (BJT) and p-channel MOSFET, are turned on when the gating signal is high (when a voltage of 1V or higher is applied to the gate node) and the switch is positively biased (collector-emitter or drain-source voltage is positive). It is turned off whenever the gating signal is low or the current drops to zero.

The MOSFET selection in this research is based on the following assumption:

- High frequency applications (>200 kHz)
- Wide line or load variations
- Long duty cycles
- Low-voltage applications (<250V)

3.1.1.2 Gating Block

The gating block is one of the central blocks used, a switch gating block defines the gating pattern of a switch or a switch module. The gating pattern can be specified either directly (the element is called Gating Block in the library) or in a text file (the element is called Gating Block (file) in the library).

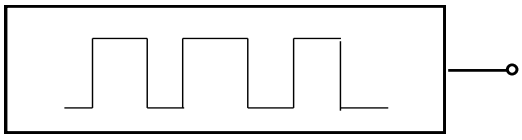


Fig. 3.6 Gating block symbol

It should be note that, a switch gating block can be connected to the gate node of a switch only, it cannot be connected to any other elements.

Table 3.1: Attribute of gating block [34]

Parameters	Description
Frequency	Operating frequency of the switch or switch module connected to the gating block, in Hz
No. of points	Number of switching points (for the gating block element only)
Switching points	Switching points, in deg. If the frequency is zero, the switching point in second. (for the gating block element only)
File for gating table	Name of the file that stores the gating table (for the gating block (file) element only)

The number of switching points is defined as the total number of switching actions in one period. Each turn-on or turn-off action is calculated as one switching point. A switch will have two number of switching points, if turned on and off once in one cycle [33, 34]. For the Gating Block (file) element, the file for the gating table must be in the same directory as the schematic file. The gating table file has the following format: G1 G2 ... ... Gn.

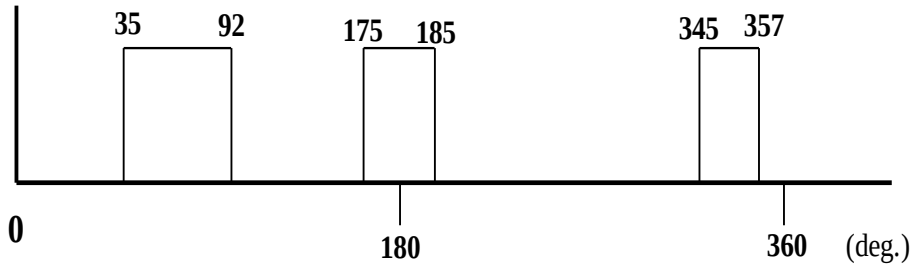


Fig. 3.7 Pattern for six point parameter [33]

The gating pattern has 6 switching points (3 pulses). The corresponding switching angles are 35^o, 92^o, 175^o, 187^o, 345^o, and 357^o, respectively.

3.1.2 Simulation of a Circuit

To simulate for example one-quadrant chopper circuit the file name “chop.sch”:
The step by step procedure that guide opening this file for simulation “chop.sch” is as follows.

- Start PSIM from the File menu, select Open to load the file “chop.sch”.
- From the Simulate menu, choose Run PSIM to start the simulation. Simulation results will be saved to File “chop.txt”.
- If the option Auto-run SIMVIEW is not selected in the options menu, from the Simulate menu, select Run SIMVIEW to start SIMVIEW. If the option is selected, SIMVIEW will be launched automatically. In SIMVIEW, select curves for display.

3.1.3 Simulation Control

An essential part in the PSIM simulation parameter controls the accuracy of the simulation as well as reaching steady state. By choosing Simulation Control in the Simulate menu in SIMCAD, the following simulation control parameters can be modified given in the Table 3.2.

Table 3.2 Simulation control Parameter [34]

SIMULATION CONTROL PARAMETERS	
Time Step	Simulation time step, in sec.
Total Time	Total simulation time, in sec.
T print	Time from which simulation results are saved to the output file. No output is saved before this time.
I print	Print step. If the print step is set to 1, every data point will be saved to the output file. If it is 10, only one out of 10 data points will be saved. This helps to reduce the size of the output file.
I load	Flag for the LOAD function. If the flag is 1, the previous simulation values will be loaded from a file (with the “.ssf” extension) as the initial conditions.
I save	Flag for the SAVE function. If the flag is 1, values at the end of the current simulation will be saved to a file with the “.ssf” extension.

With the SAVE and LOAD functions, the circuit parameters such as voltages or currents, and other quantities can be saved at the end of a simulation period, and loaded back as the initial conditions for the next simulation session. This affords the flexibility of running a long simulation in several shorter stages with different time steps and parameters. Components values and parameters of the circuit can be changed from one simulation term to the other. The circuit topology, however, should remain the same [33].

In PSIM, the simulation time step is fixed through the simulation. In order to guarantee accurate simulation outcomes, the time step must be selected appropriately. The factors that limit the time step in a circuit include the switching period, widths of waveforms, and intervals of transients. It is suggested that the time step would be at least one amount smaller than the smallest of the above parameters. The acceptable maximum time step is automatically designed in PSIM. It is compared with the time step set by the user, and the smaller value of the two will be used in the simulation. If the selected time step is different from the one set by the user, it will be saved to the file "message.doc" [35].

3.1.4 Fast Fourier Transform (FFT) Analysis

A Fast Fourier Transform block computes the fundamental component of the input signal. The FFT algorithm is based on the radix-2/decimation-in-frequency technique. The number of sampling points within one fundamental period should be 2^N (where N is an integer), the maximum number of sampling points allowed is 1024 [34]. The output gives the peak amplitude and the phase angle of the input fundamental component. When using FFT for harmonic analysis, one should make sure that the following requirements are satisfied:

- The waveforms have reached the steady state.
- The length of the data selected for FFT should be the multiple integer of the fundamental period.

For a 60-Hz waveform, for example, the data length should be restricted to 16.67 ms (or multiples of 16.67 ms). This can be done by clicking on x axis in Simview, de-selecting Auto-scale in Range, and specifying the starting time and the final time. The FFT analysis is only performed on the data that are displayed on the screen [34].

3.2 MODELING ANALYSIS

In Fig. 3.8, the block diagram gives representation of the whole system, it is categorized into four sub-section namely power supply, gate driver, switching device, output part.

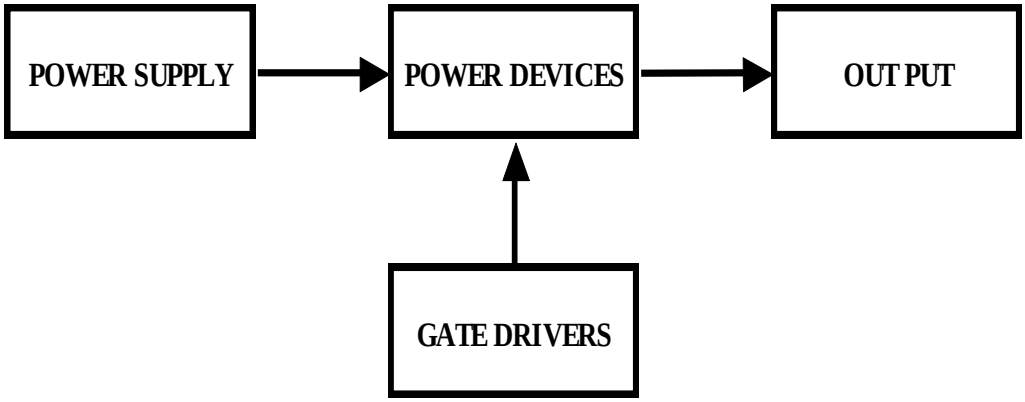


Fig. 3.8 The inverter block diagram

The simulation and the determination of input to output (I/O) relations are a fundamental task in this study and design process of the multilevel inverters. These I/O relations become essential for the development of suitable models, which allows us to obtain all the necessary data about the inverter prior to the implementation stage. The modeling of multilevel inverters is not a trivial task since they are made up of linear and nonlinear components [2].

3.2.1 Cascaded H-Bridge Modules

The proposed cascaded H-Bridge inverter model used in this research consists of three parallel connected H-bridge modules, fed through a single DC voltage source supply. Two cases of topologies are consider for the simulation, the first case without isolation transformer while the second case with isolation transformer as shown in Fig. 3.9 and Fig.3.10. Each of the H-bridge modules has four semiconductor switches and is configured in such a way, that it generate a quasi-square voltage waveform (+E, 0, -E) at its output terminal. E is the main DC source from the supply unit. S_1, S_2, S_3 …S_{12}, are the semiconductor switches. G_1, G_2, G_3 ….G_{12}, represent the gating signals used for controlling

the MOSFET on and off. VP1, Vp2, and VP3 are the output terminals of the respective bridges. The total output voltage of the inverter in the fig. 3.9 below is given by;

$$Vout = Vp_1 + Vp_2 + Vp_3 \quad \text{..... (3.1)}$$

And also the total output voltage of the inverter in Fig. 3.25 is given by;

$$Vout = Vp_1 + Vp_2 + 3Vp_3 \quad \text{.....(3.2)}$$

The eq. (3.2) provides higher voltage due to increase in the isolation transformer turn ratio in third bridge.

The proposed system in Fig. 3.10 comprises of three transformers with series connected secondary side. Transformer 1 and 2 were designed to have 1:1 winding ratio, and transformer 3 to have 1:3 winding ratio, producing an output voltage across the load given by eq. (3.2).

The transformer not only provide isolation between the load and DC source, but also provide the means of increasing the number of output voltage step and quality signal, without need of additional inverter bridge or DC source.

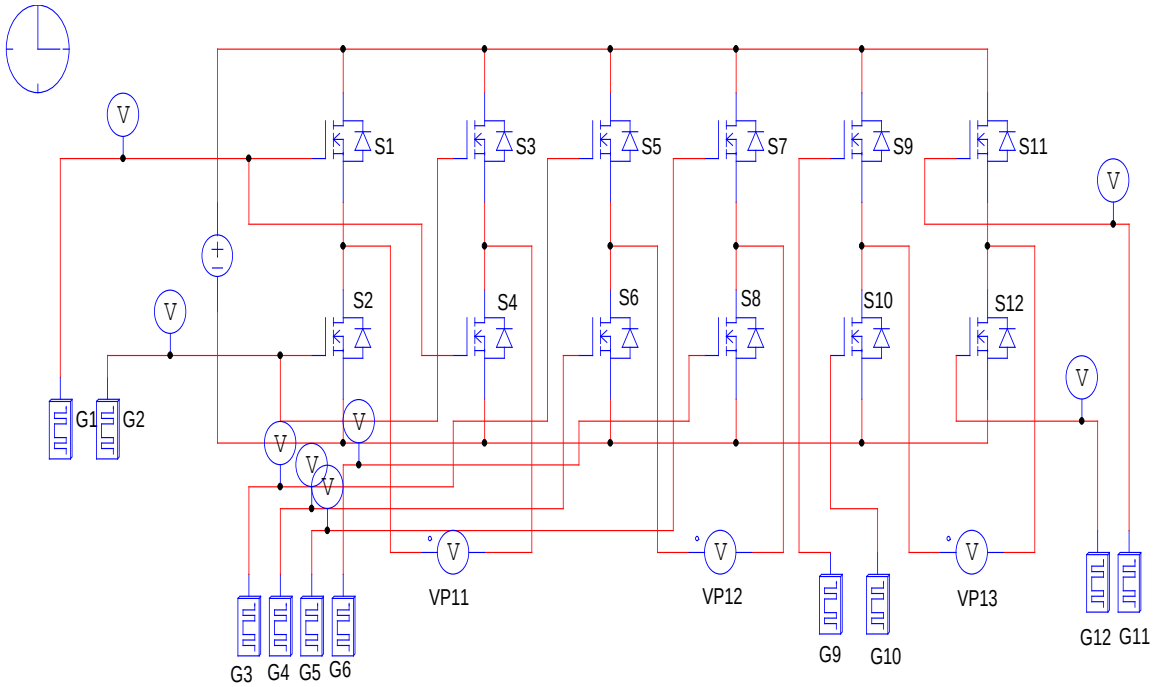


Fig. 3.9 Cascaded H-bridge without isolation transformer

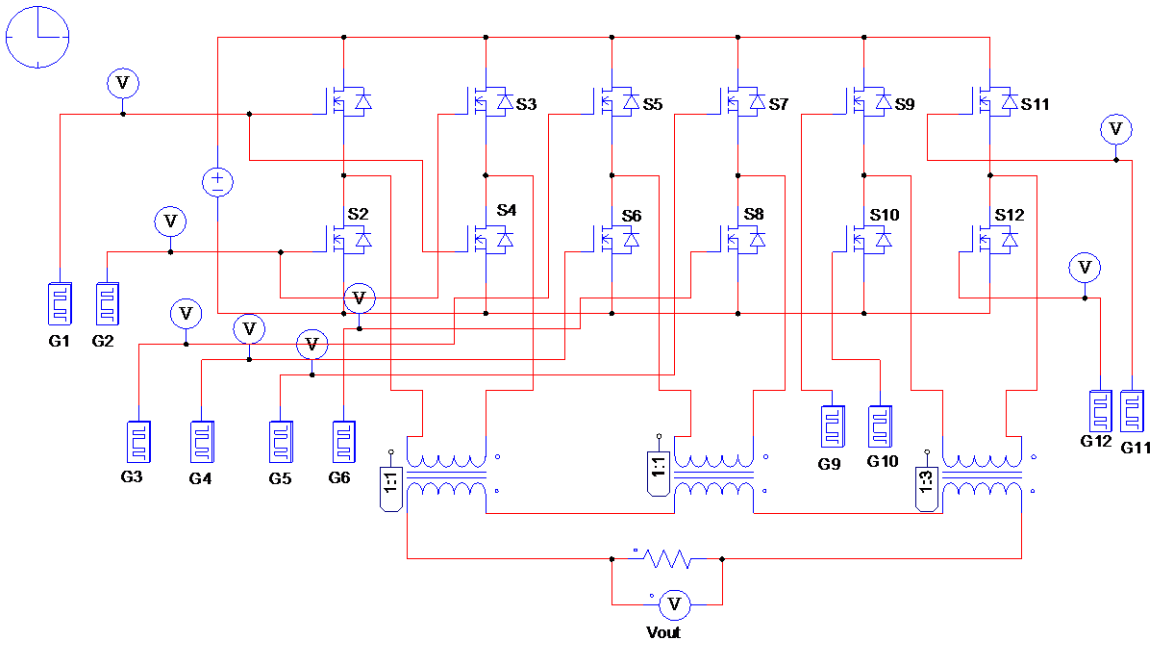


Fig. 3.10 Cascaded H-bridge with isolation transformer

3.3 SWITCHING ANGLES ANALYSIS

The modulation technique employed on any kind of the inverter topology plays a major role in determining the properties of its output waveform [24, 25]. The selective harmonic elimination method is the modulation technique used in generating the 11-level of output voltage. Therefore, the switching angles needs to be carefully chosen such that the selected odd harmonics are eliminated. This technique apart from producing an output with a lower total harmonic distortion THD it also reduces the amount of electro-Magnetic interference EMI and switching losses caused by high switching frequency modulation techniques [6, 17].

For a stepped waveform such as the one depicted in Fig. 2.1 above, the Fourier series expansion is given by [24].

$$V(wt) = \frac{4Vdc}{n\pi}\sum_{n=1,2,3\ldots}^{\infty}\{\cos(n\alpha_1) + \cos(n\alpha_2) + \cdots + \cos(n\alpha_s)\} \times \sin(nwt) \quad \ldots\ldots (3.3)$$

Where n= 1, 2, 3……

Ideally given a desired fundamental voltage *V*, one want to determine the switching angles, $\alpha 1, \alpha 2, \alpha 3, \ldots\ldots\ldots \alpha s$, so that the voltage total harmonic distortion will be minimum.

From eq. (3.3), the magnitude of the Fourier coefficients when normalized with respect to *V* is as follows:

$$V = \frac{4Vdc}{\pi}\{\cos(\alpha_1) + \cos(\alpha_2) + \cdots + \cos(\alpha_s)\} \quad \ldots\ldots\ldots\ldots \quad (3.4)$$

The amplitude of the fundamental component is controlled by the modulation index (*m*) and is given by the expression;

$$\text{Modulation index } (m) = \frac{V}{Vdc} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.5)$$

The number degrees of freedom available equal to ***S***, one degrees of freedom is used to choose the value of *V* and the remaining degree of freedom is used to eliminate selected order harmonic component. With this operatio2n, lower order odd harmonic (*S*-1) will be eliminated (where *S* is the number of switching angle) [35, 36].

Therefore, 3rd, 5th, 7th, 11th, 13th, 17th, 19th, 23rd, order harmonics will be all be eliminated in this case.

Using eq. (3.4) and (3.5), hence we can write the magnitude of the harmonic components, including the fundamental as;

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cdots \ldots\ldots\ldots + \cos(\alpha_{12}) = \frac{M\pi}{4} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.6)$$

$$\cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \cdots \ldots\ldots + \cos(3\alpha_{12}) = 0 \quad \ldots\ldots\ldots\ldots \quad (3.6a)$$

$$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cdots \ldots\ldots\ldots + \cos(5\alpha_{12}) = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.6b)$$

$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cdots \ldots\ldots\ldots + \cos(7\alpha_{12}) = 0 \quad \ldots\ldots\ldots\ldots\ldots \quad (3.6c)$$

$$\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cdots \ldots\ldots + \cos(11\alpha_{12}) = 0 \quad \ldots\ldots\ldots\ldots \quad (3.6d)$$

$$\cos(13\alpha_1) + \cos(13\alpha_2) + \cos(13\alpha_3) + \cdots \ldots\ldots + \cos(13\alpha_{12}) = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.6e)$$

$$\cos(17\alpha_1) + \cos(17\alpha_2) + \cos(17\alpha_3) + \cdots \ldots\ldots\ldots + \cos(17\alpha_{12}) = 0 \quad \ldots\ldots\ldots\ldots \quad (3.6f)$$

$$\cos(19\alpha_1) + \cos(19\alpha_2) + \cos(19\alpha_3) + \cdots \ldots\ldots\ldots + \cos(19\alpha_{12}) = 0 \quad \ldots\ldots\ldots\ldots \quad (3.6g)$$

$$\cos(23\alpha_1) + \cos(23\alpha_2) + \cos(23\alpha_3) + \cdots \ldots\ldots\ldots + \cos(23\alpha_{12}) = 0 \quad \ldots\ldots\ldots\ldots\ldots \quad (3.6h)$$

The above non-linear transcendental equation are then solved to find the approximate close value of the switching angles, capable of eliminating the inverter lower order harmonics at chosen modulation index. Due to the non-linearity of the equations it is not possible to find exact the solution using ordinary mathematical methods, the numerical solution algorithm are presented in [24], [36-40]. In this research the analytical approach demonstrated and cited above was used to shows he number of available degree of freedom for both fundamental and harmonic component, due to some initial condition constrain and

switching angle limitation which are presented also presented in [9], [40]. Another approach was employed in order to obtain best switching angles with lowest THD as described in [9]. Half–Equal-Phase (HEP) is Method used to arrange the main switching angles in a best possible way, it is used to obtain the output waveform wider and better, in the area between 0 – π/2 which are determine by the formula.

$$\alpha_i = i \frac{90^0}{\frac{m+1}{2}} = i \frac{180^0}{m+1} \qquad \text{..... (3.7)}$$

$where\ i = 1, 2, \ldots . \frac{m-1}{2}$, and m is the inverter level.

Adjustment in the eq. (3.8) was made to extend the switching angle between 0 - 2π, so that it accommodate all possible switching angle combination, since our system is an open loop, where $i = 0,1,2,3, \ldots \ldots \ldots \ldots 24.$

3.4 TOTAL HARMONIC DISTORTION (THD) ANALYSIS

Calculating (THD) is an important phenomena, because converter is the largest source of harmonics, it's useful to determine its extent for being a factor used in accessing power quality of an inverter output, THD is obtained from the relation,

$$THD = \frac{\sqrt{\sum_{n=i}^{\infty} Vn^2}}{V_1} \mathbf{x\ 100} \qquad \text{..... (3.9)}$$

In the above equation, V_1 is the fundamental component, V_n is the amplitude of the nth order odd harmonic. Using the eq. (3.9) the exact amount of harmonic distortion present in a signal can only be calculated over an infinite range, which is practically impossible. Therefore, ranges of harmonics need to be specified, first consideration was given to harmonic appeared below eleven order and vice versa. Eq. (3.9) applied throughout analysis in determine THD performance.

CHAPTER 4

RESULT AND DISCUSSION

4.1 DESIGN VERIFICATION USING PSIM

In an effort to verify the proposed multilevel inverter design procedure perform in the previous section; the circuit in Fig. 3.9 and Fig. 3.10 were set up in PSIM software platform package, both circuit was supply with 100V DC as an input voltage supply. The PSIM model behavior was demonstrated in Fig. 4.1.

Fig. 4.1 Psim model

The model consist of three program; PSIM-schematic program were the actual circuit schematic configuration are assemble and edited, PSIM-simulator is internal analysis generator, and SIMIEW is wave processing program that allow output result to be further process. The Fig 3.10 comprises three isolation transformers at specified turn ratio, the transformer serve not only an isolation of ac load from dc supply, but also provide the means to amplify the magnitude of the output voltage without additional inverter bridge module or DC sources supply. The Fig.3.10 is used to analyses output voltage waveforms using different load condition, and their corresponding harmonics contain level.

On the other hand Fig. 3.9 topology without an isolation transformer, has been used to investigate the terminal voltage of each inverter bridge module, find sum of the terminal

Voltage output, the gating signal, and harmonic contain at fundamental and switching frequency of 5 kHz.

The following simulation results are considered for discussion in this chapter;

I. Comparison of gating signal at 50 Hz and 5 KHz.

II. Terminal voltage at each module for case without isolation transformer as in (I) above.

III. Total output voltage and THD analysis for case with isolation transformer as in (I).

IV. Resistive load analysis for case with and without isolation transformer.

V. Total output voltage and THD analysis for case with isolation transformer.

VI. Resistive load analysis for case with isolation transformer.

VII. Inductive load analysis for case with isolation transformer.

VIII. Capacitive load analysis for case with isolation transformer.

IX. Resistive-Inductive load analysis for case with isolation transformer.

X. Resistive-Capacitive load analysis for case with isolation transformer.

XI. Inductive-Capacitive load analysis for case with isolation transformer.

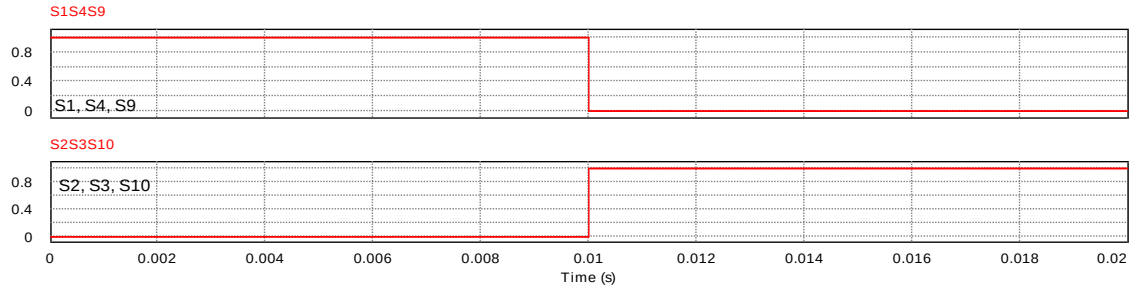
XII. Resistive-Inductive-Capacitive load analysis for case with isolation transformer.

4.2 THE GATING SIGNAL COMPARISON

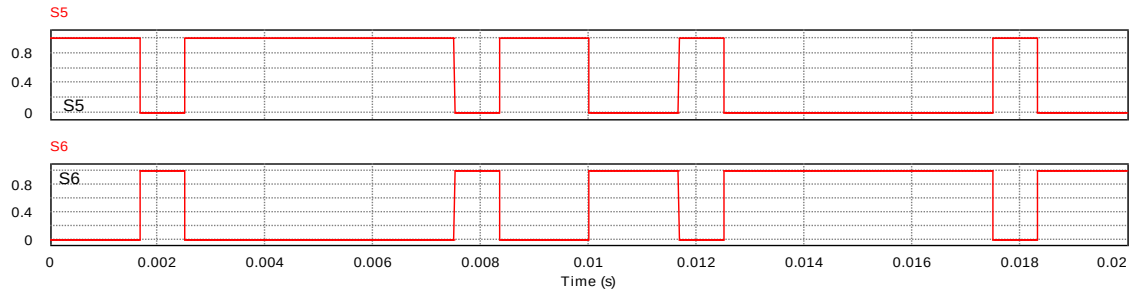
The obtained gating signal is applied to control the twelve IGBT's ON and OFF state. In any H-bridge modules, switches on the same leg are always operated complementary to avoid short circuiting the dc source, as well as protecting the device from damage. The efficiency of the multilevel inverter parameters, such as switching losses and harmonic reduction, principally depend on control signal and modulation strategies, which can be classified according to the switching frequency used, in this case selective harmonic elimination, which are based on fundamental and high switching frequencies. For the control signal two cases was consider, the first case at fundamental frequency of 50 Hz, while the second case at 5 kHz switching frequency as shown in Fig. 4.2 and Fig. 4.3.

4.2.1 Case1: Gating Signal at Frequency of 50 Hz

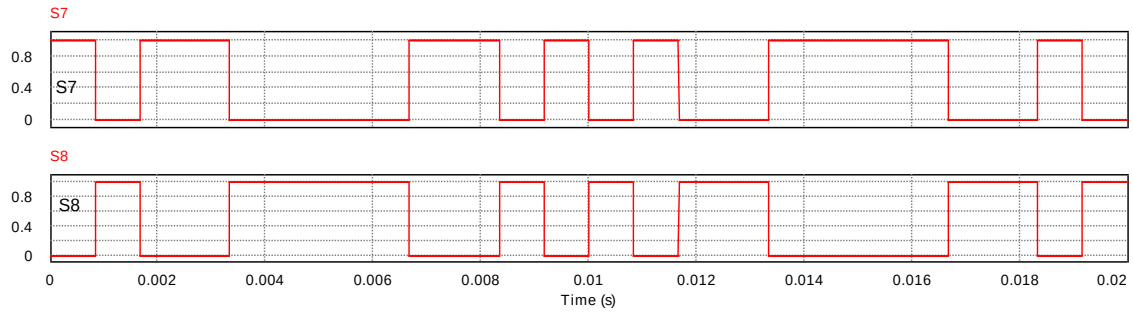
For this case frequency of 50 Hz is presented, and is referred to as low switching frequency, and has an attribute of low switching stress to the power devices. But the frequency is associated with poor quality output in some high power application.



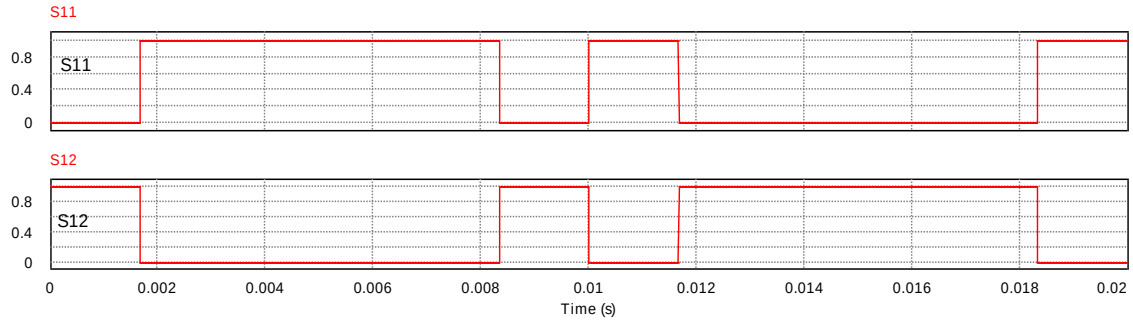
(a) Switching signal of $S1S4S_9$ and $S_2S_3S_{10}$



(b) Switching signal of S_5S_6



(c) Switching signal of S_7S_8

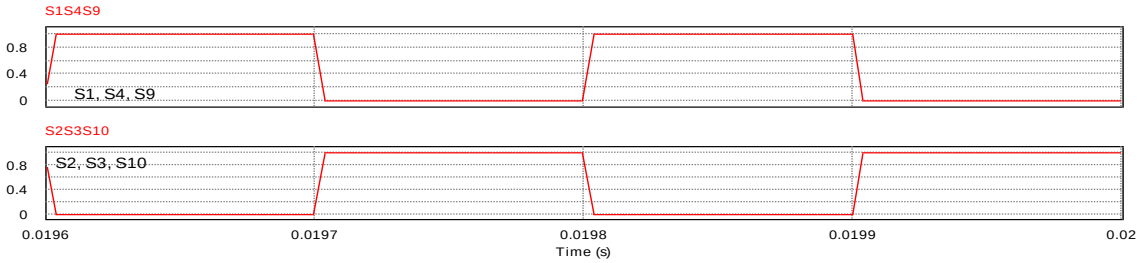


(d) Switching signal of $S_{11}S_{12}$

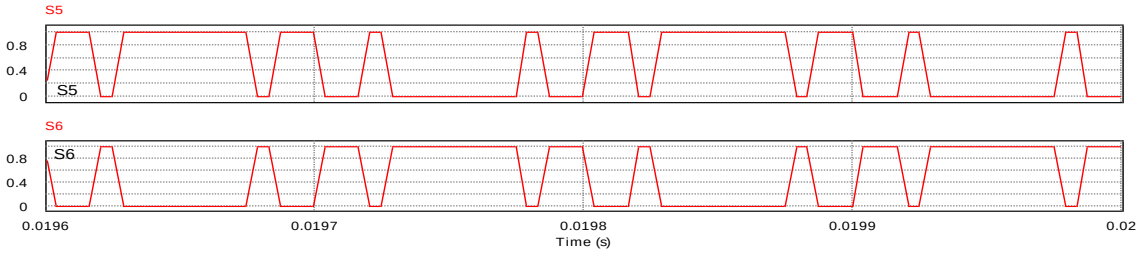
Fig. 4.2 Switching angle diagram for all the switching devices at 50Hz

4.2.2 Case 2: Gating Signal at Frequency of 5 KHz

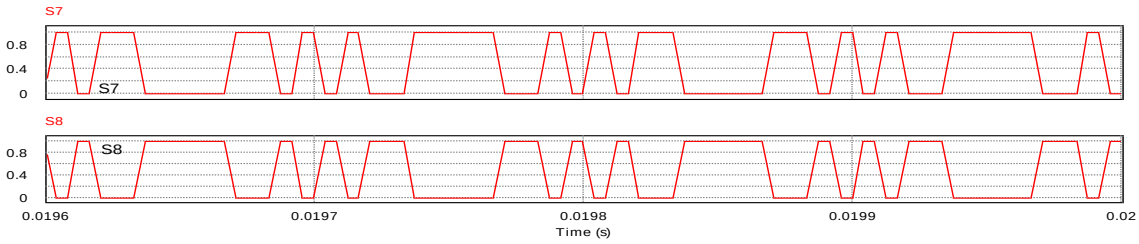
For the second case study, the switching frequency of 5 kHz is consider, so that high range of bandwidth and better output power are realized, as shown in Fig. 4.3.



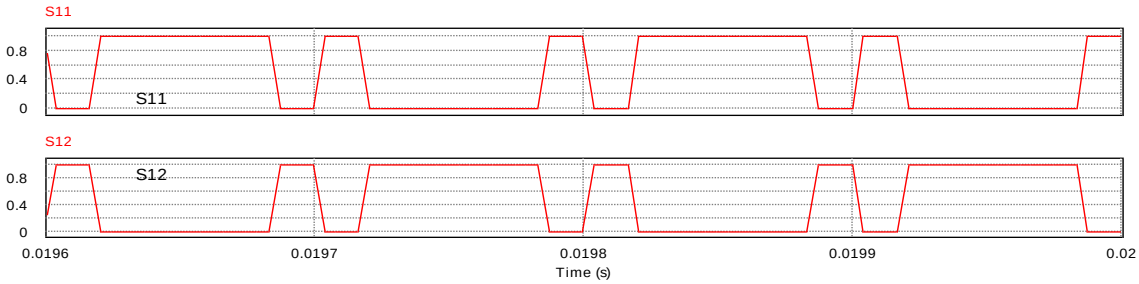
(a) Switching signal of $S1S4S_9$ and $S_2S_3S_{10}$



(b) Switching signal of S_5S_6



(c) Switching signal of S_7S_8



(d) Switching signal of S11S12

Fig. 4.3 Switching angle diagram for all the switching devices at 5 kHz

The two control signal when compare shows similarity pattern, only that at 5 kHz the control signal are better, and repeated higher than at 50 Hz, which mean higher bandwidth at higher frequency, this will result in better quality output waveform. Case 2 will be used mostly in our simulation due to better output quality is realized.

The gating signals are than transformed into binary sequence, where high was taken as logic 1 and low was represented by logic 0. The IGBT conduction states during the positive and negative half cycle in both H-bridges are given in Table 4.1.

Table 4.1 Selected switching combination for the terminal voltage

Voltage	Switching states											
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
+E	1	0	0	1	1	0	1	0	0	1	0	1
-E	0	1	1	0	0	1	0	1	1	0	1	0

4.3 TERMINAL VOLTAGE OF EACH MODULE FOR CASE WITHOUT ISOLATION TRANSFORMER

The Fig. 3.9 is the multilevel H-Bridge cascade inverter; it consists of three parallel connected H-bridge modules, fed through a single DC source supply. Each of the module has four semiconductor switches and configure such that it can generate a quasi-square wave (+E, 0, -E) at its output terminal.

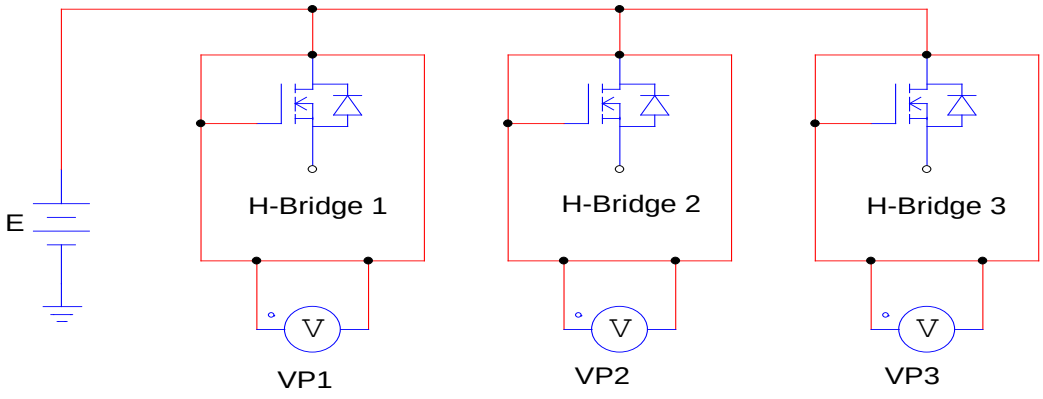
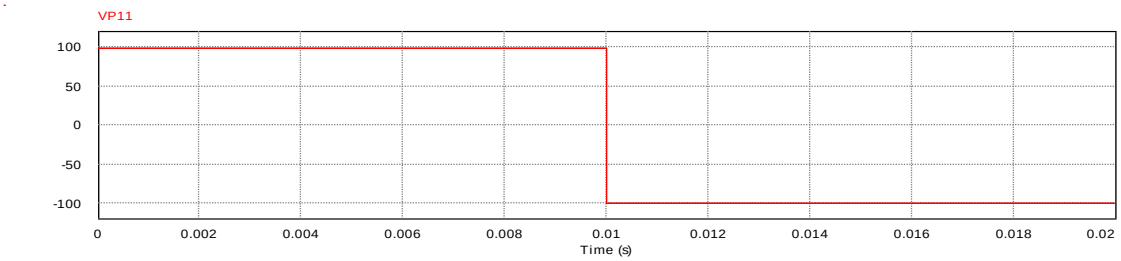


Fig. 4.4 Three H-bridge model

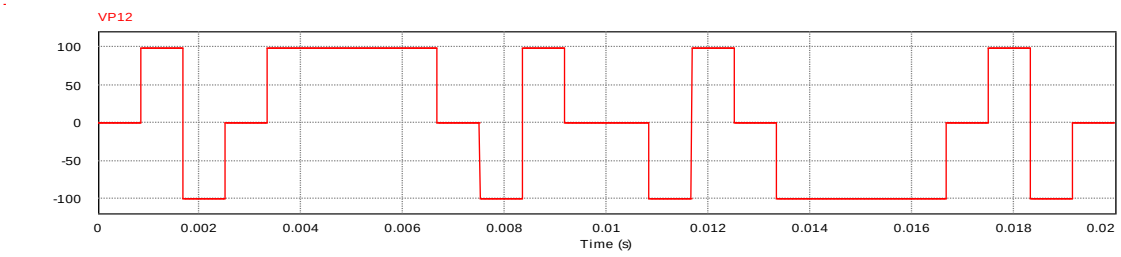
From the topology connection in Fig. 4.4, E is the main DC source from the supply unit. S1, S2…….. S12, are the semiconductor switches. G1 G2…… G12, represent the gating signal used for controlling the IGBT on and off state as describe above in both cases. Also from Fig. 4.4 model each H-bridge has an output VP*i* for *i* = 1, 2, 3 that produce output in respect to each bridge module. The simulation result of inverter terminal voltage as mention earlier will be presented in two case, case 1 at 50 Hz while case 2 a 5 kHz switching frequency.

4.3.1 Case 1: Terminal Voltage at 50 Hz

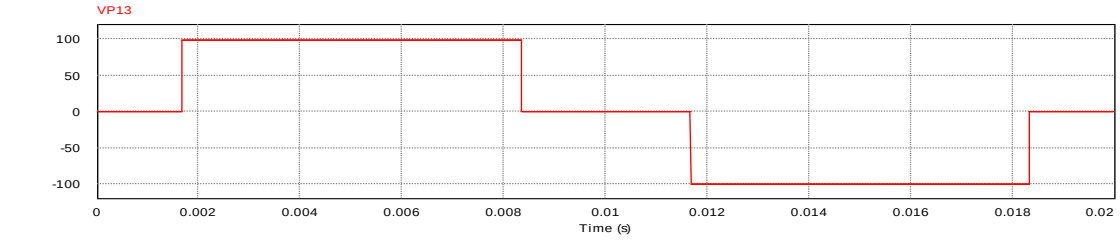
In the first case study Cascaded H-bridge without isolation transformer is used, Fig. 4.5 show generated individual H-bridge voltage waveform (Vp_1, Vp_2, and Vp_3), and combine terminal voltage in a single SIMVIEW which allow us to view the overlapping of each bridge over other.



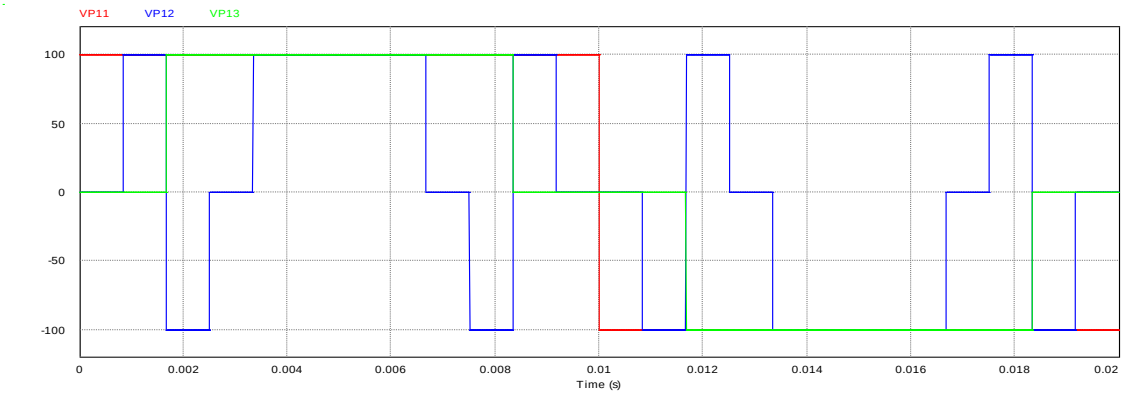
(a) Simulated output terminal voltage for H-bridge 1 (Vp_1)



(b) Simulated output terminal voltage for H-bridge 2 (Vp_2)



(c) Simulated output terminal voltage for H-bridge 3 (Vp_3)

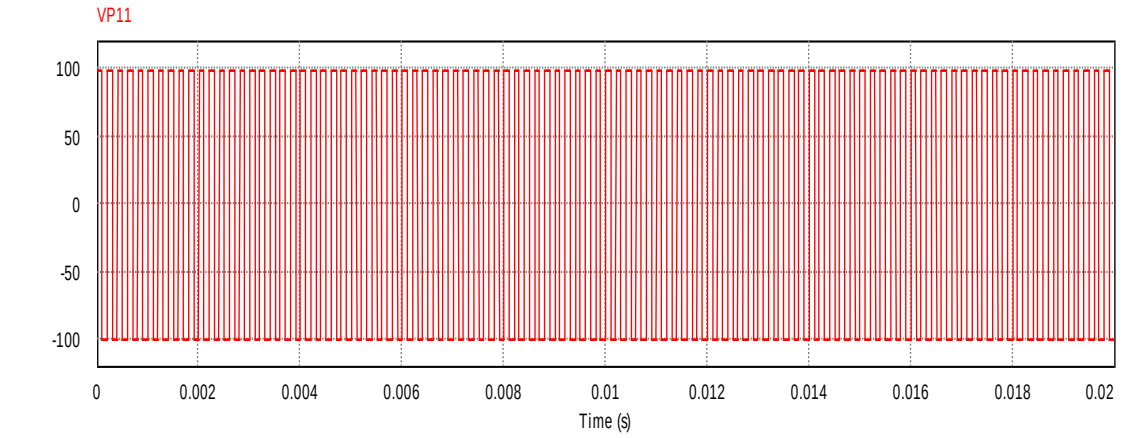


(d) Simulated output terminal voltage for bridge module Vp_1, Vp_2, Vp_3 combine in Simview

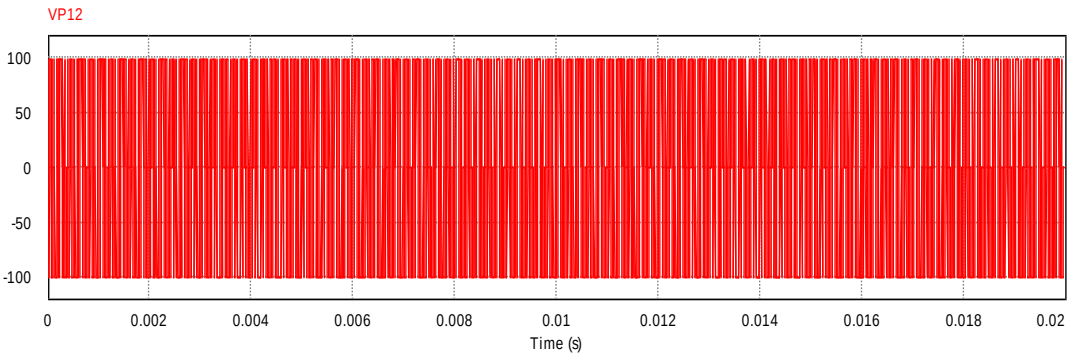
Fig. 4.5 Output voltage at case without an isolation transformer at 50 Hz.

4.3.2 Case 2: Terminal Voltage at 5 KHz

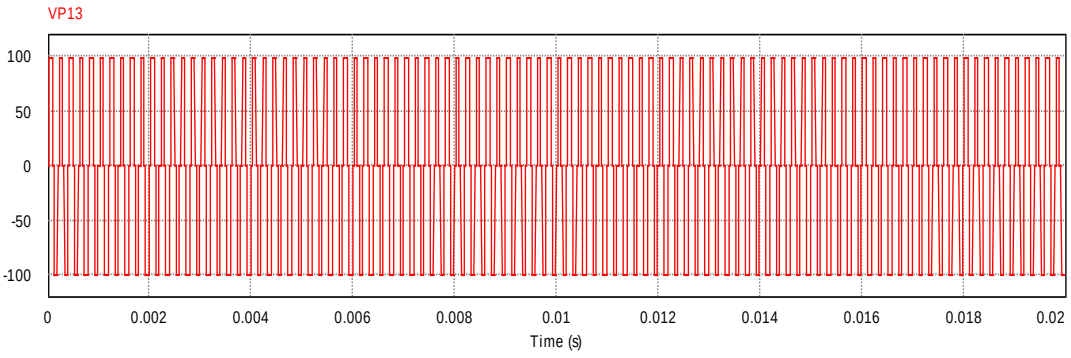
Using the same configuration of Fig. 4.4, that is without isolation transformer at the above mention frequency, the terminal voltage waveform (Vp_1, Vp_2, and Vp_3), and combine terminal voltage in a single SIMVIEW which allow us to view the overlapping of each bridge over other.



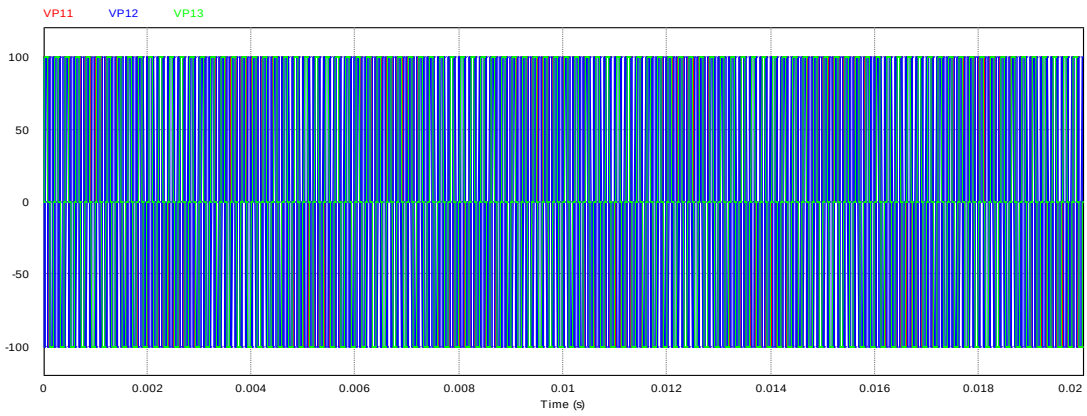
(a) Simulated output terminal voltage for bridge H-bridge 1 (Vp_1)



(b) Simulated output terminal voltage for H-bridge 2 (Vp_2)



(c) Simulated output terminal voltage for H-bridge 3 (Vp_3)



(d) Output terminal voltage for bridge module Vp_1, Vp_2, Vp_3 combine in Simview

Fig. 4.6 Simulated output voltage at case without an isolation transformer at 5 KHz.

From the above two cases the result Fig. 4.5 and 4.6 shows how the change in frequency effect the terminal voltage, with the result of case 2 having higher number of cycle generated per H-bridge. These voltages were fed into the primaries side of the transformer to produce an eleven level waveform output signal.

4.4 TOTAL OUTPUT VOLTAGE AND THD ANALYSIS FOR CASE WITHOUT ISOLATION TRANSFORMER

The total output voltage of the multilevel inverter without an isolation transformer was given in Eq. (3.1), two cases of gating signals are consider for the simulation, case 1 at frequency of 50 Hz and case 2 at frequency of 5 kHz. The model representing the scenario is given in Fig. 4.7.

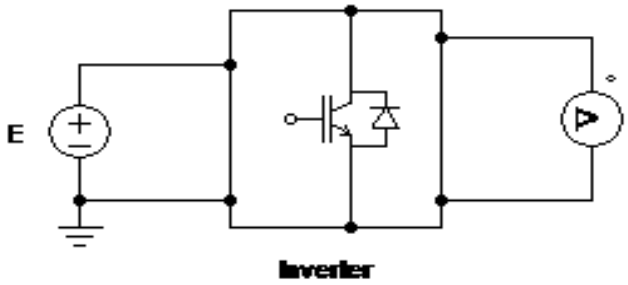
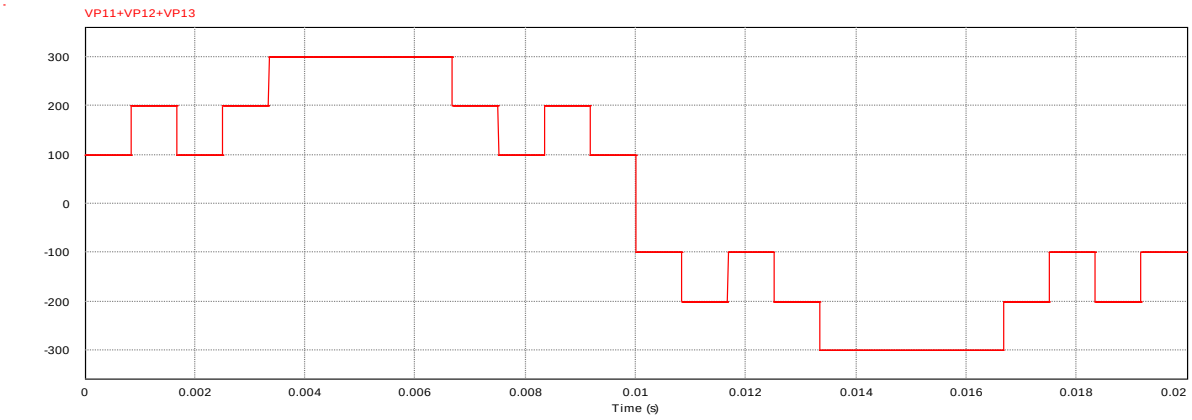


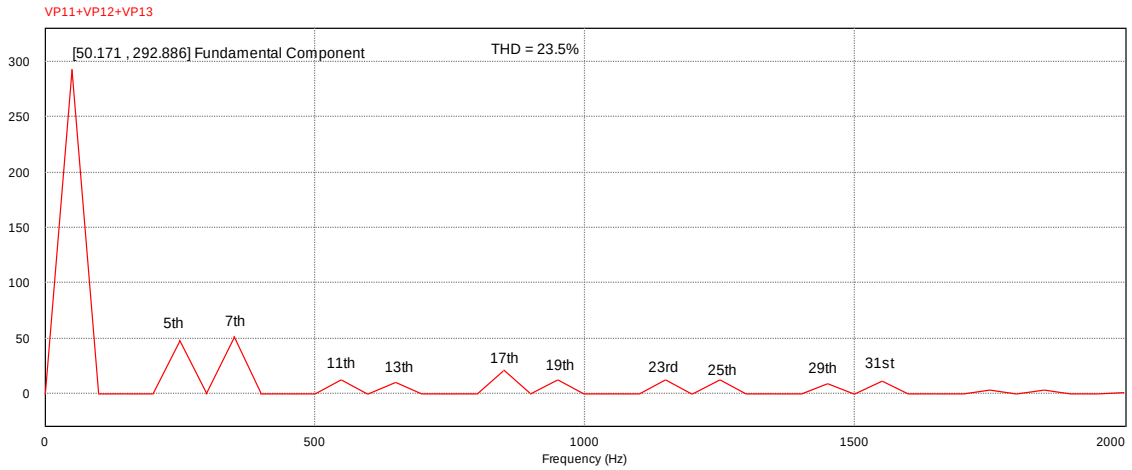
Fig. 4.7 Inverter model without transformer

4.4.1 Case 1: Total Output Voltage and THD Analysis at 50 Hz

The Fig. 4.8 shows the total output voltage and THD analysis when the multilevel inverter is operated at fundamental frequency of 50 Hz without isolation transformer. From the voltage waveform plot the staircase wave generated is a little bit ambiguous to understand how many the number of voltage level are depicted.



(a). Sum of the total output voltage of Vp_1, Vp_2, Vp_3 at 50 Hz



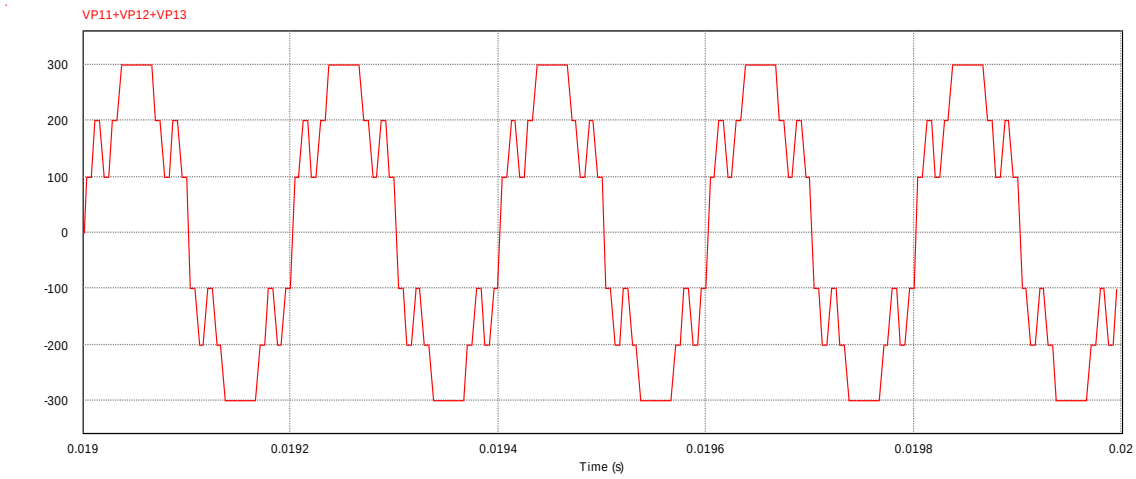
(b). FFT analysis of the inverter without isolation transformer f_{sw} = 50 Hz and THD = 23.5%

Fig. 4.8 Voltage and FFT analysis of inverter without transformer, THD =23.5%.

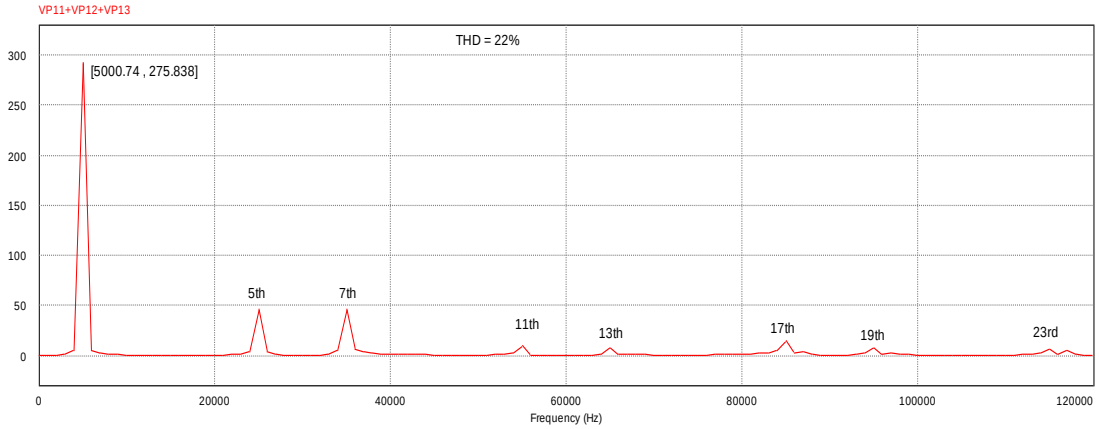
The output voltage waveform produced harmonic of 23.5% which is consider high harmonic among classes of multilevel inverter topology, this result show the structure lack power quality.

4.4.2 Case 2: Total Output Voltage and THD Analysis at 5 KHz

Using the same model in Fig. 4.7, but in this case the gating signal frequency was operated at high switching frequency of 5 KHz



(a) Sum of the total output voltage of Vp_1, Vp_2, and Vp_3 at 5 kHz



(b) FFT analysis of the inverter without isolation transformer f_{sw} = 5 kHz and THD = 22%

Fig. 4.9 Simulated output voltage and FFT analysis of inverter without transformer at 5 kHz, THD = 22%

From the above cases, voltage waveform and FFT analysis spectrum shows the magnitude of fundamental component and that of harmonic at the above frequencies. In both cases, the fundamental component amplitude is much higher than that of harmonic order component. Both the two cases lack quality voltage waveform, but there is slight reduction in THD from 23.5% to 22% as calculated. It can also be observed that the triple harmonics are concealed out automatically, only the non-triple harmonics are present at lower amplitude.

4.4.3 Resistive Load Analysis without Transformer

For the purpose of analysis the multilevel inverter without isolation transformer was simulated using a resistive load as shown in the model in Fig. 4.10, the load resistor R_L of 100Ω and 500Ω were used to investigate the output voltage waveform and harmonic contain.

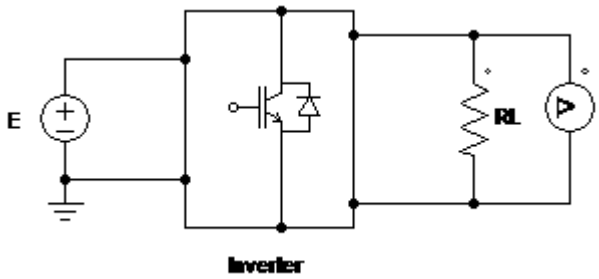
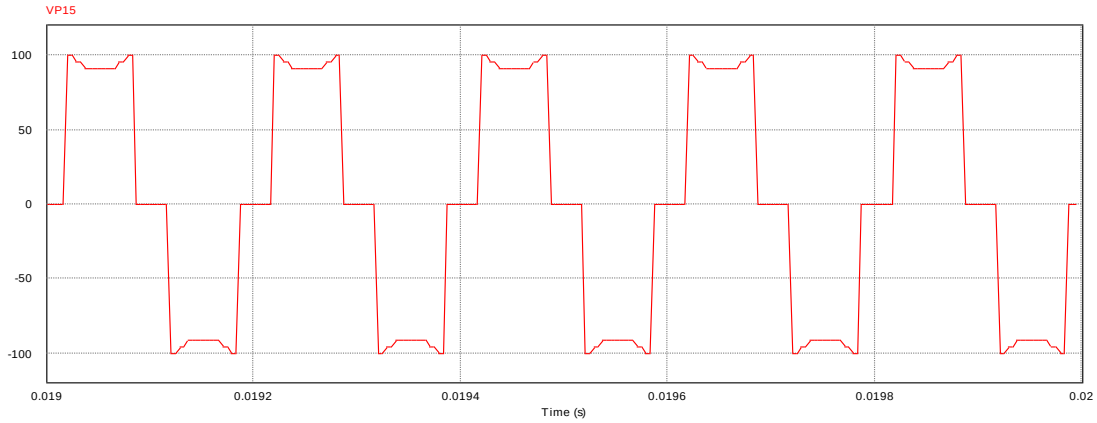
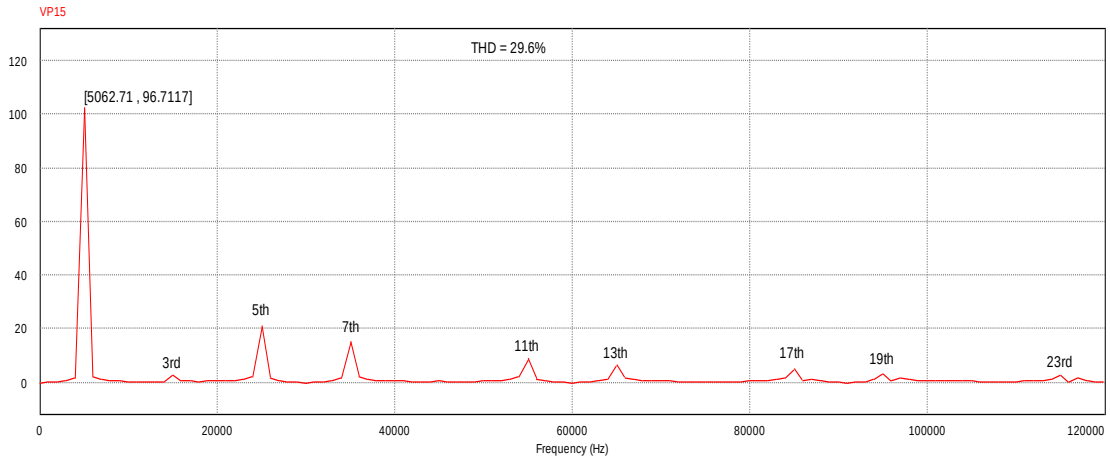


Fig. 4.10 Inverter model without transformer and R_L

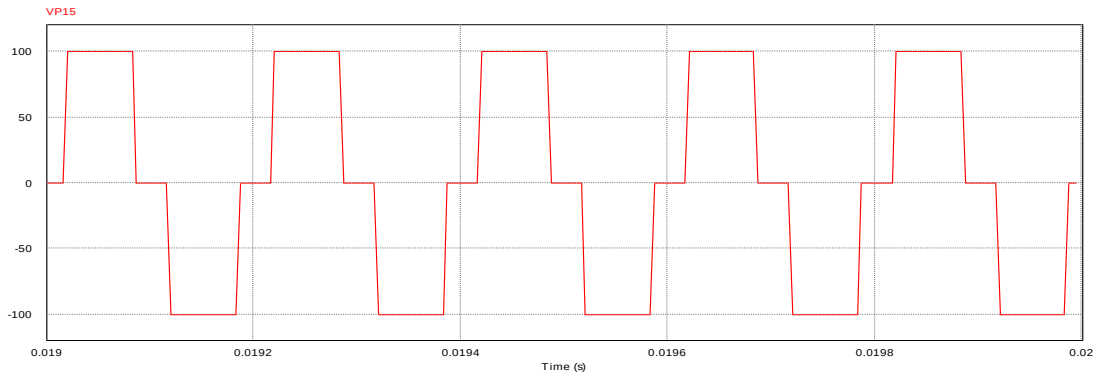


(a) Voltage output waveform of the inverter without transformer, R_L=100Ω

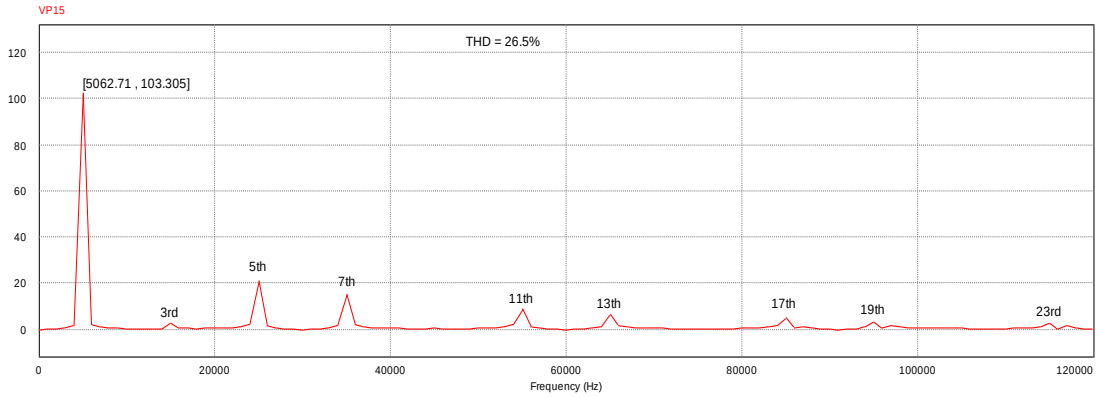


(b) FFT analysis of the inverter without isolation transformer

Fig. 4.11 Voltage and FFT analysis of inverter without transformer f_{sw} = 5 kHz, R_L=100Ω, THD = 29.6%.



(a) Voltage output waveform of the inverter without transformer, R_L=500Ω



(b) FFT analysis of the inverter without isolation transformer

Fig. 4.12 Voltage and FFT analysis of inverter without transformer f_{sw} = 5 kHz, R_L=500Ω, THD = 26.5%.

Although from the FFT spectrum of the two cases there are slight reductions in THD amplitude from 29.6% to 26.5% with increase in load resistance. But the voltage waveform is a little bit distorted and this will lead to poor power quality. Therefore the structure without isolation transformer is not the favorable configuration in this simulation.

4.6 TOTAL OUTPUT VOLTAGE AND THD ANALYSIS FOR CASE WITH ISOLATION TRANSFORMER

From the previous voltage and FFT analysis result shows that, all the odd triplen harmonic (3^{rd} 9^{th} 15^{th} 21^{st} 27^{th} 33^{rd}) are cancelled out automatically, only non-triplen remain with minimum amplitude compare with that of fundamental component amplitude. It's also observed that, the output voltage waveforms are distorted to some level. Due to these reasons, the structure of the inverter was modified to include isolation transformer as shown in Fig. 3.10.

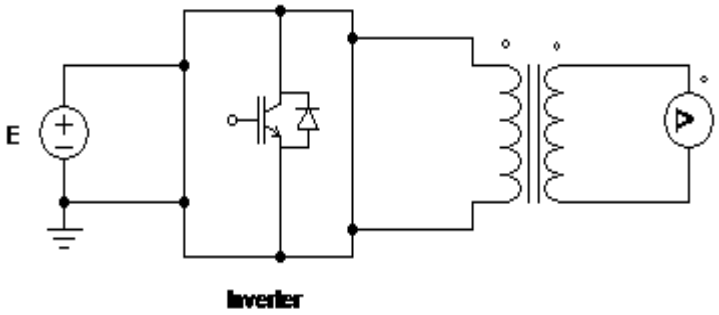
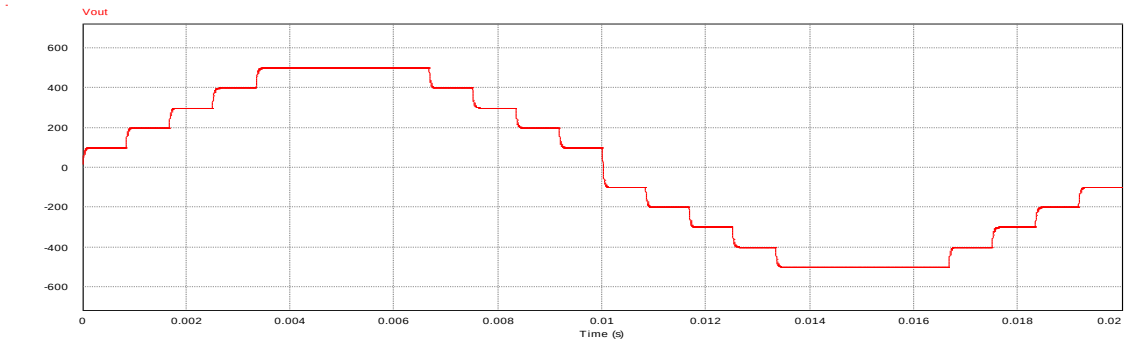


Fig. 4.13 Inverter model with isolation transformer

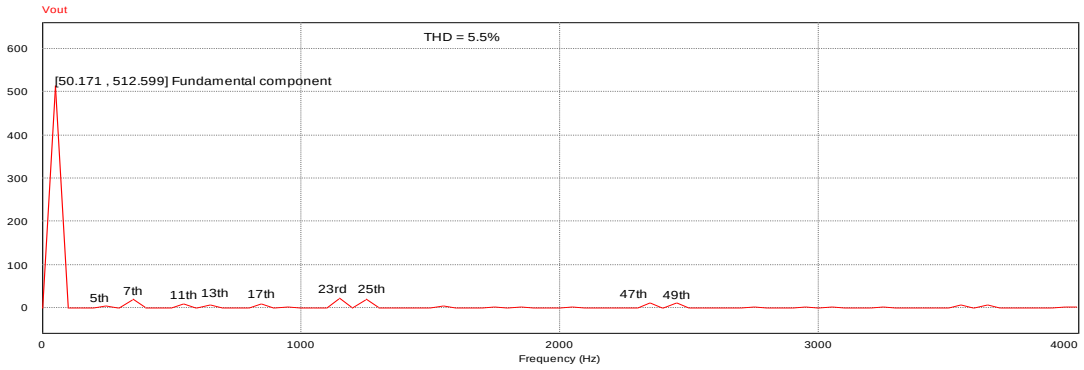
This section of discussion and analysis focuses on different load condition simulation cases, to include resistive load, inductive load, capacitive load, and combination of both. Fig. 3.10 is further model to simpler form to ease realization assessment as shown in Fig. 4.13. Since at the beginning terminal voltage for each H-bridge are investigated and was fed through the secondary side of the transformer, now we only consider the total output as given in eq. (3.2) for two cases of gating signal discussed previously case 1 at 50 Hz, and case 2 at 5 KHz.

4.6.1 Case 1: Total Output Voltage and THD Analysis at 50 Hz

The structure was simulated using a load resistance of 100 Ω to avoiding floating of the transformer output terminal during the simulation.



(a) Voltage output waveform of the inverter with isolation transformer



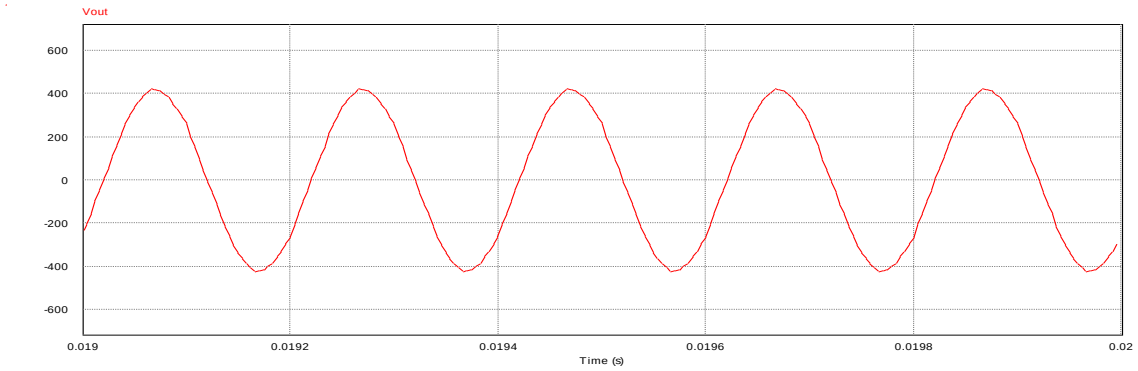
(b) FFT analysis of the inverter without isolation transformer

Fig. 4. 14 Voltage and FFT analysis of the inverter with isolation transformer f_{sw} = 50 Hz and THD = 5.5%

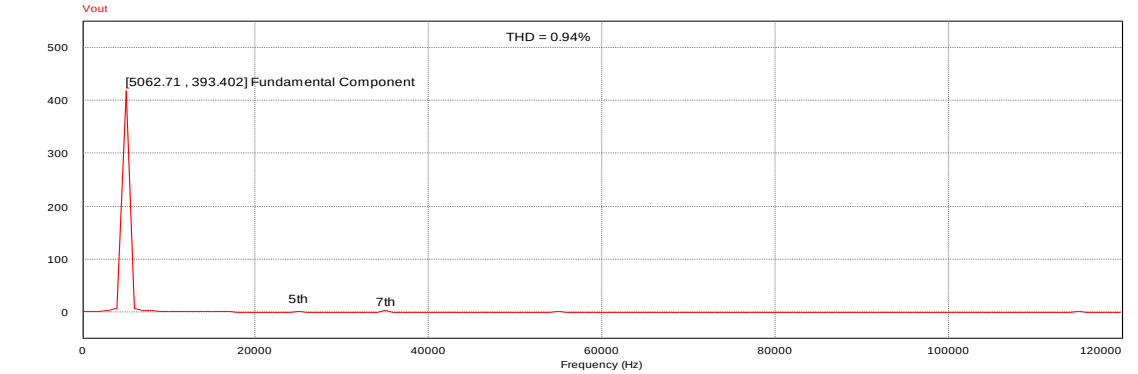
Comparing the output voltage waveform of Fig. 4.14 and that of Fig. 4.8 having the same frequency but different structure, significant improvements in both the voltage waveform quality and harmonic contain was observed in this case THD = 5.5%.

4.6.2 Case 2: Total Output Voltage and THD ANALYSIS AT 5 KHz

The same simulation was carried out with the same parameter but in this case at 5 kHz.



(a) Voltage output waveform of the inverter with isolation transformer, R=100Ω



(b) FFT analysis of the inverter with isolation transformer, R=100Ω

Fig. 4.15 Voltage and FFT analysis of inverter with transformer at f_{sw} = 5 kHz, THD = 0.94%.

From Fig 4.15 the results show that, almost all the harmonic are eliminated to the minimum level which lead to significant reduction in THD from the two cases of 23.5% to 0.94%, this reduction is due to change in the inverter structure and the switching frequency. The structure with isolation transformer will be used throughout the simulation analysis at 5 kHz because of better output voltage waveform.

4.6.3 Load Analysis with Isolation Transformer

For the purpose to study and analysis the inverter harmonic level and voltage waveform with change in load, the inverter was simulated with a number of resistive loads

from 100Ω - 500Ω in step of 100Ω respectively. Inductive load, capacitive load and combination of both will also be considered. In this scenario the circuit structure of Fig. 3.10 will be consider under the switching frequency of 5 kHz, as model in Fig. 4.16.

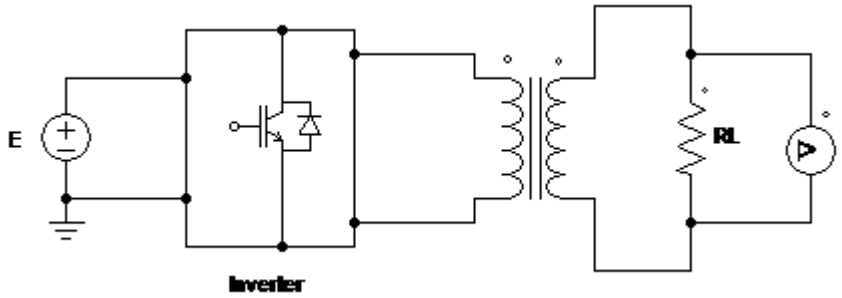
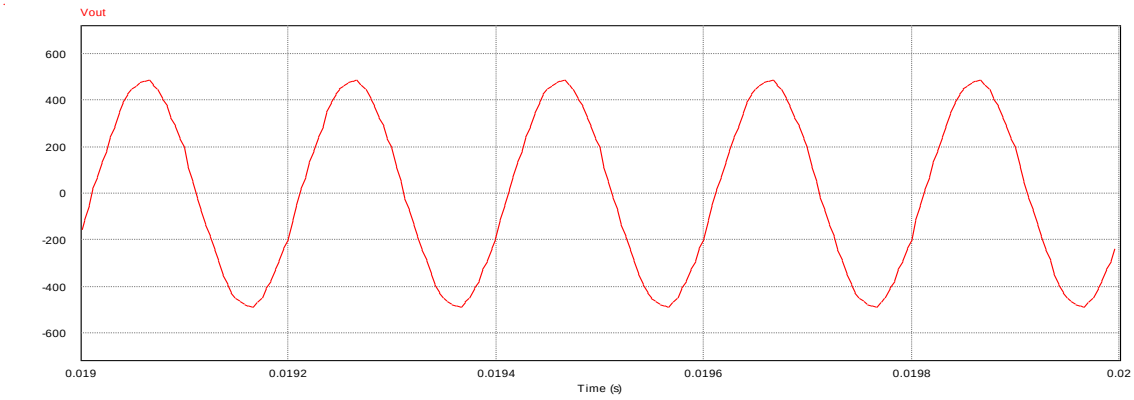


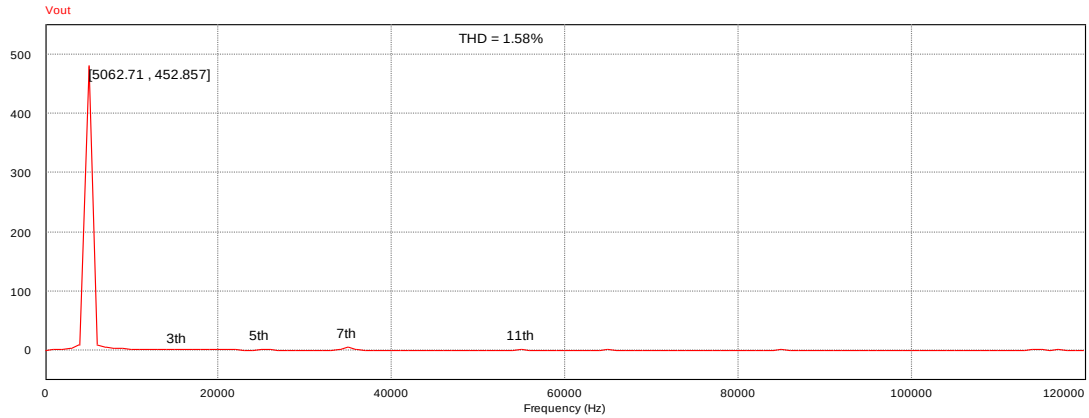
Fig. 4.16 Inverter model with isolation transformer and resistive load

4.6.3.1 Case 1: Resistive Load Analysis

The designed inverter tested on different resistive loads of 100 Ω to 500 Ω in step 100 Ω respectively. The voltage output and corresponding harmonic spectrum are shown for each resistive load, it can be deduced that THD increases with increase in resistive load.

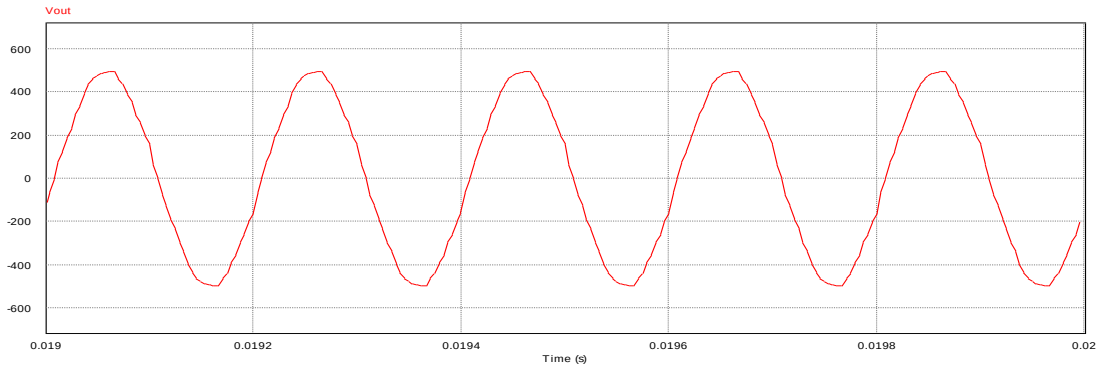


(a) Voltage output waveform of the inverter with isolation transformer, R=200Ω

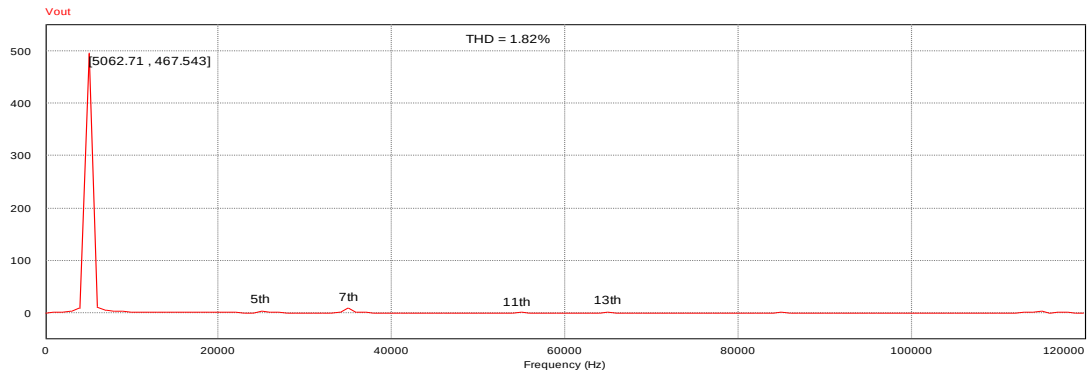


(b) FFT analysis of the inverter without isolation transformer, R=200Ω

Fig. 4.17 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, R=200Ω, THD = 1.58%.

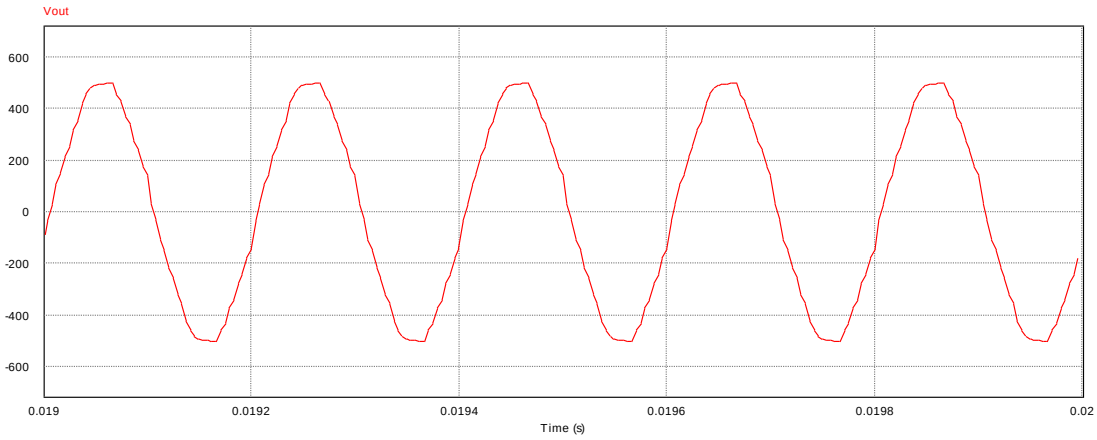


(a) Voltage output waveform of the inverter with isolation transformer, R=300Ω

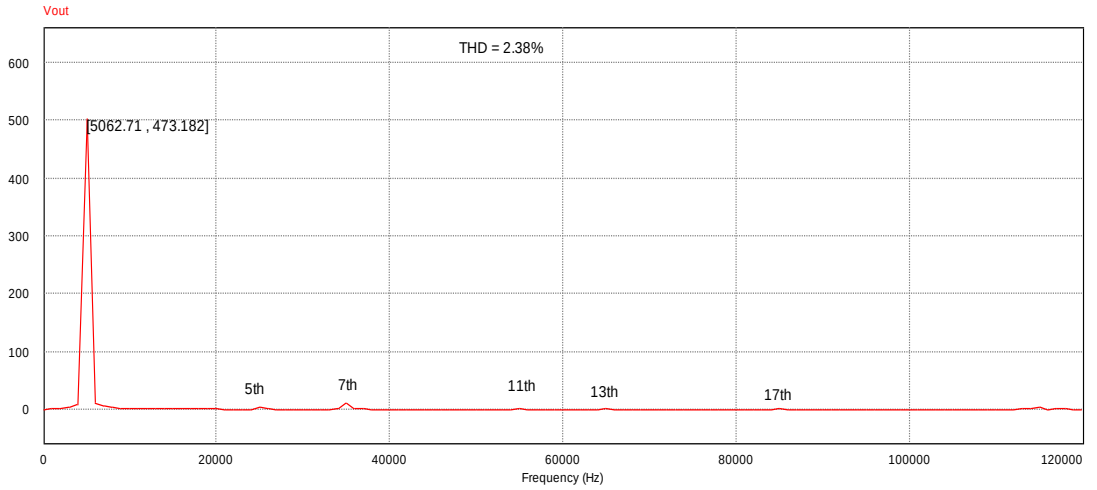


(b) FFT analysis of the inverter without isolation transformer, R=300Ω

Fig. 4.18 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, R=300Ω, THD = 1.82%.

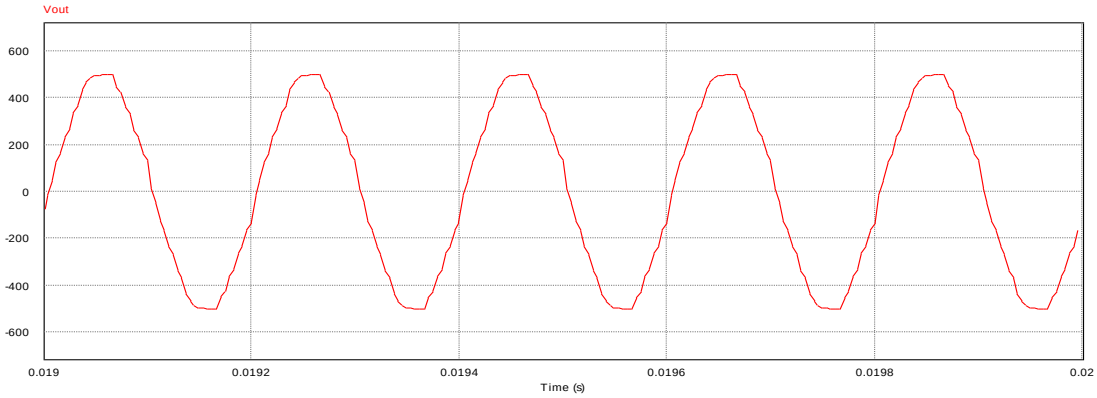


(a) Voltage output waveform of the inverter with isolation transformer, R=400Ω

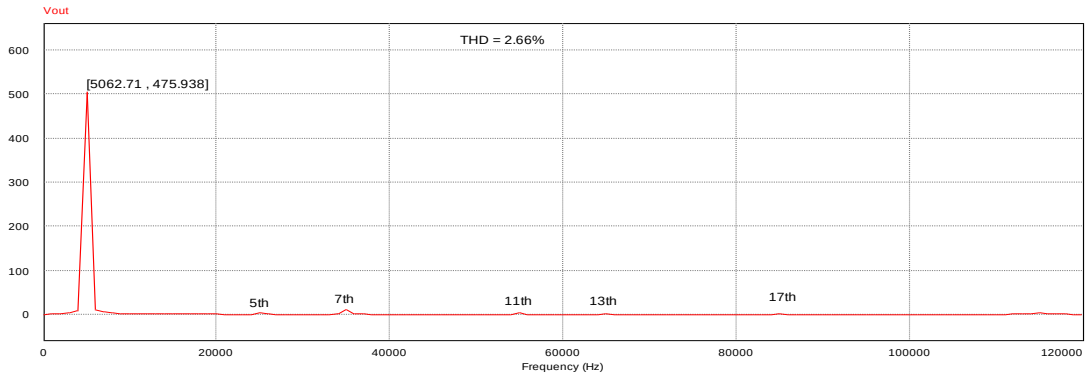


(b) FFT analysis of the inverter without isolation transformer, R=400Ω

Fig. 4.19 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, R=400Ω, THD = 2.38%.



(a) Voltage output waveform of the inverter with isolation transformer, R=500Ω



(b) FFT analysis of the inverter without isolation transformer, R=500Ω

Fig. 4.20 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, R=500Ω, THD = 2.66%.

The results for the above analysis summarize in Table 4.2, resistance values, THDs, with corresponding voltage amplitudes are recoded. Table 4.2 shows that, the output voltages are increasing with increase in load resistances, and it can also be observed that THD increase as the loads is increase.

Table 4.2 Resistive and THD load analysis

R (Ω)	100	200	300	400	500
THD (%)	0.94	1.58	1.82	2.38	2.66
Vout (V)	393.402	452.857	467.543	473.182	475.938

The Fig. 4.21 represent different resistance values against the corresponding THD respectively.

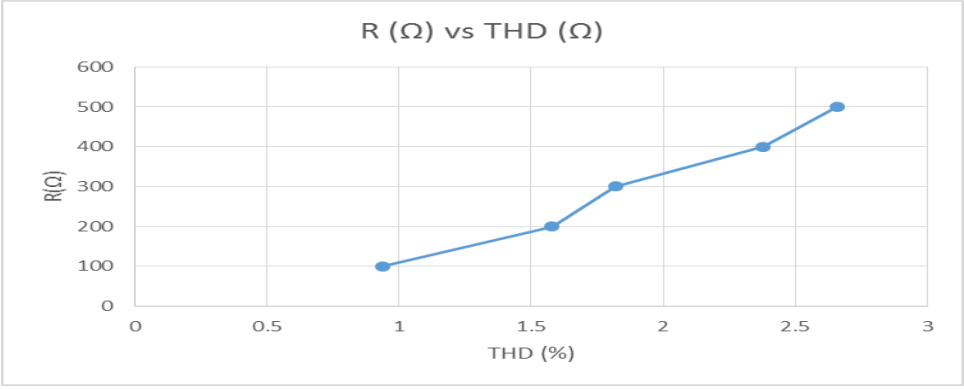


Fig. 4.21 Resistive load against THD values

From Table 4.2, it shows that increase in load lead to increase in THD for resistive load, the graph in Fig. 4.21 further explain the analysis. Another observation is the output voltages also increase with increase in load resistances, this means higher power deliver to the load is anticipated.

4.6.3.2 Case 2: Inductive Load Analysis

Having consider and simulate different value of the resistive load, another simulation using inductive loads have been analysed, with value of inductors of 100 H, 500H and 1000H respectively. Fig. 4. 22 shows the inverter model with the isolation transformer under the inductive load.

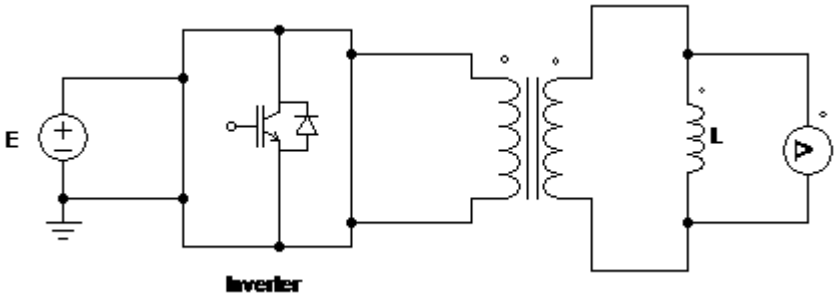
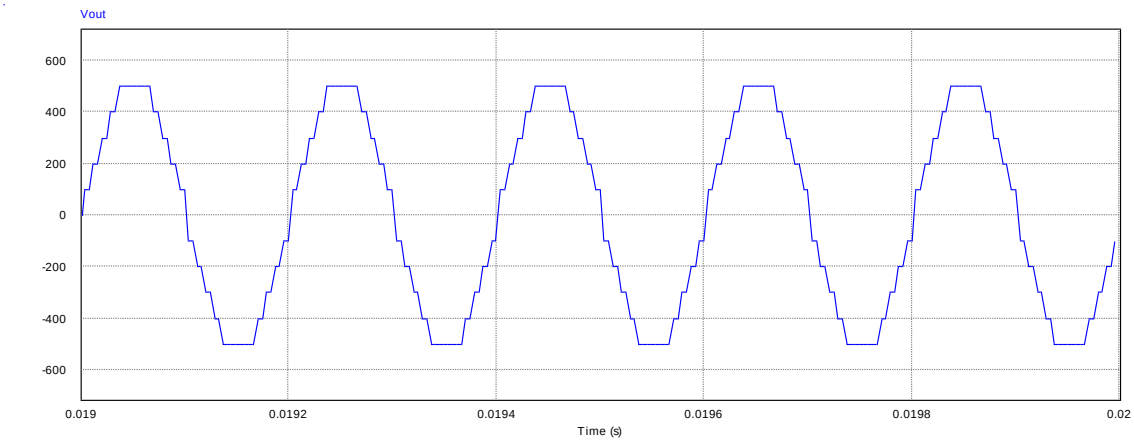
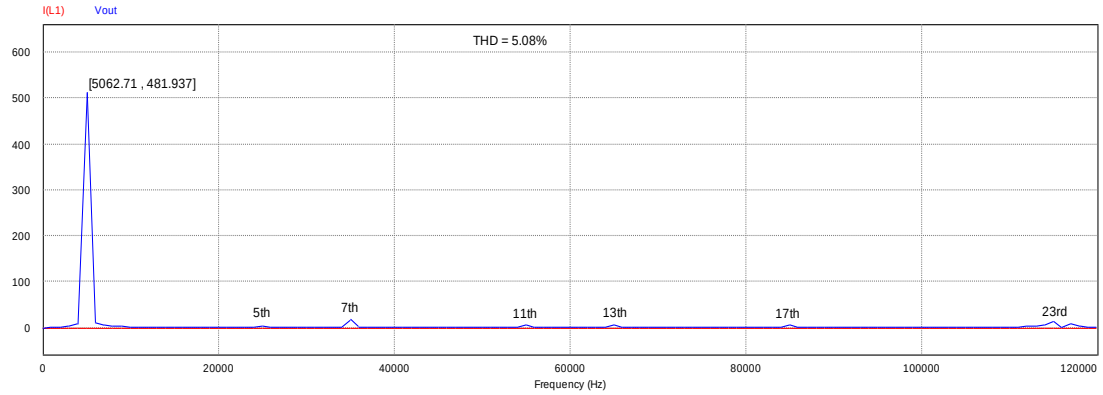


Fig. 4.22 Inverter model with isolation transformer under inductive load

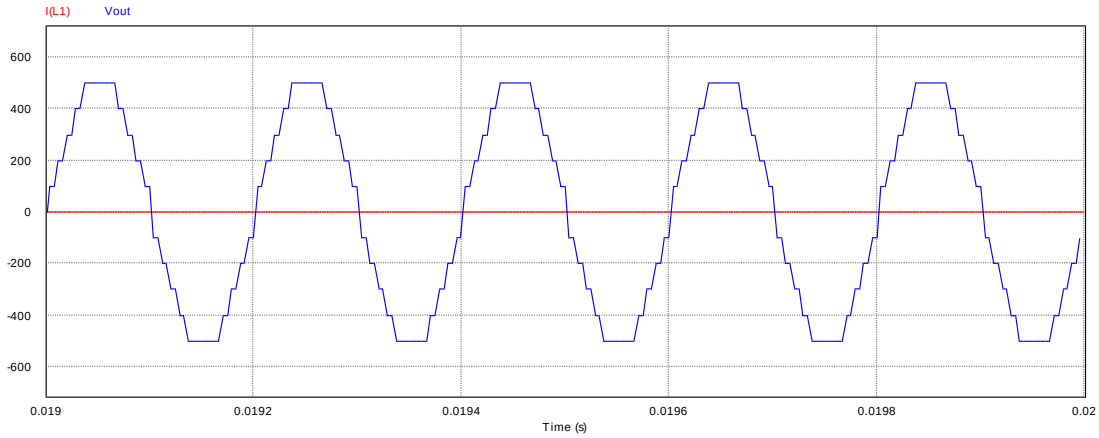


(a) Voltage output waveform of the inverter with isolation transformer, L=100H

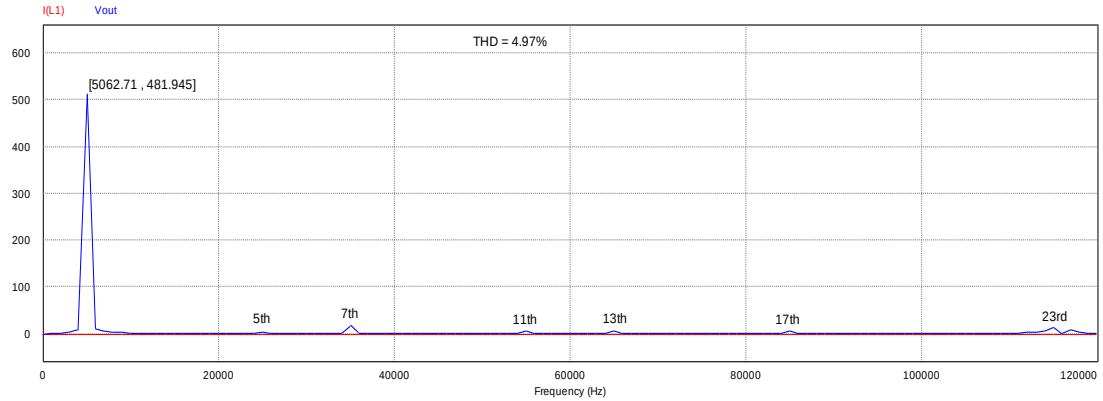


(b) FFT analysis of the inverter without isolation transformer, L=100H

Fig. 4.23 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, L=100H, THD = 5.08%.

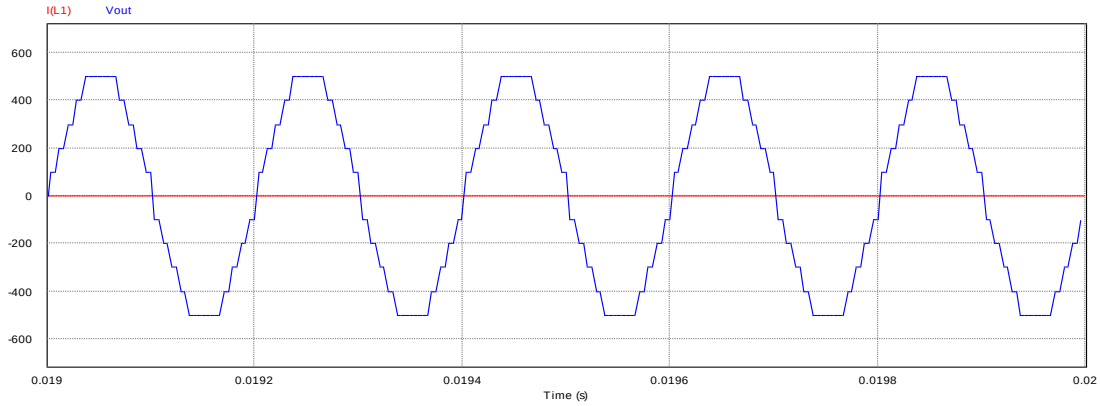


(a) Voltage output waveform of the inverter with isolation transformer, L=500H

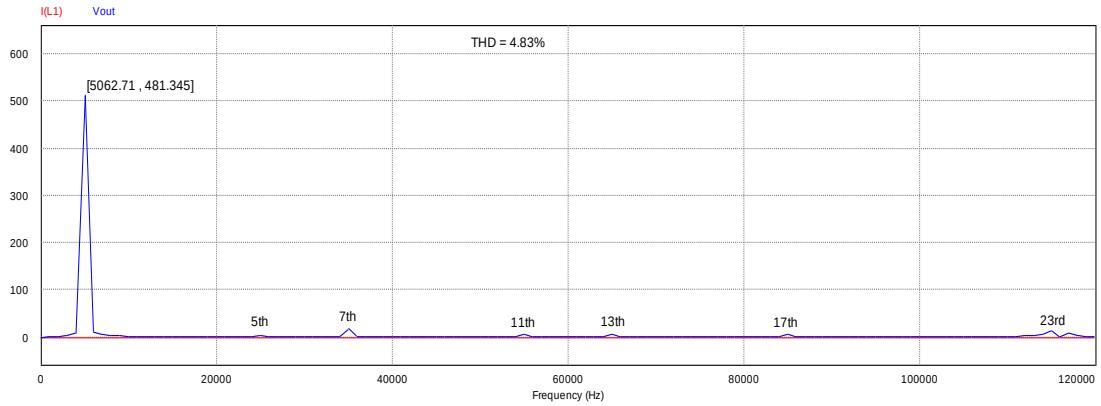


(b) FFT analysis of the inverter without isolation transformer, L=500H

Fig. 4.24 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, L=500H, THD = 4.97%.



(a) Voltage output waveform of the inverter with isolation transformer, L=1000H



(b) FFT analysis of the inverter without isolation transformer, L=1000H

Fig. 4.25 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, L=1000H, THD = 4.83%.

From figure above, a staircase voltage waveform is generated at 5 KHz when a purely inductive load is applied in each case, the voltage output level are maintained as the inductance value is increase unlike in the case with resistive load. The simulation results of different inductance values are tabulated in Table 4.3.

Table 4.3 Inductance and THD load analysis

L (H)	100	500	1000
THD (%)	5.08	4.97	4.83
Vout (V)	481.937	481.945	481.345

From Table 4.3 it can be clearly seen that, voltage output magnitude levels are almost equal with increase of inductance values for purely inductive load. While THD values decrease with increase in inductive loads.

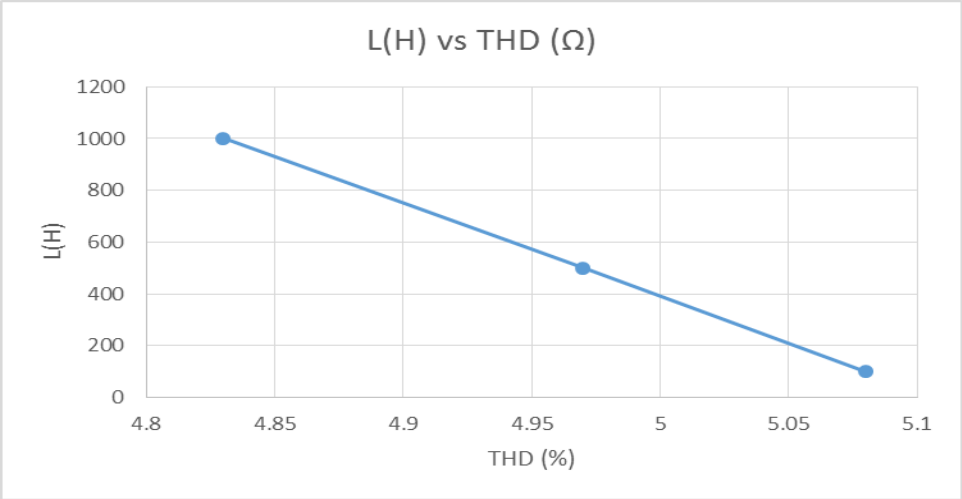


Fig. 4.26 Resistive load against THD values

From Table 4.3, it shows that increase in load lead to decrease in THD for inductive load, the graph in Fig. 4.26 further explain the analysis. But in this case the output voltage remains steady over the range of inductance values.

4.6.3.3 Case 3: Capacitive Load Analysis

Capacitive loads of 100F, 500F, and 1000F are carried out to observe the voltage and current waveform as well as harmonic distortion analysis. The model is given in Fig. 4.27. The capacitor in this simulation is charged to the nominal voltage value and produces a current that lead the voltage.

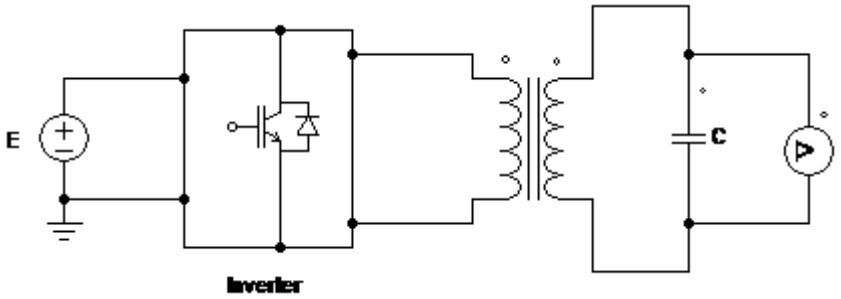
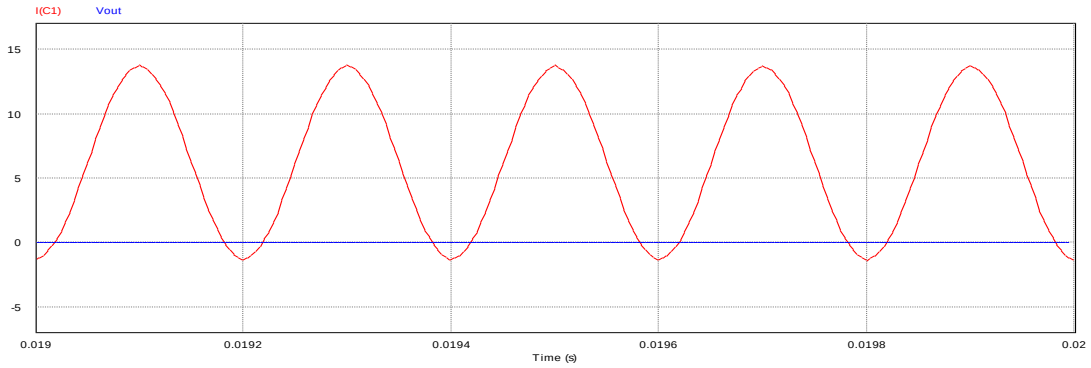
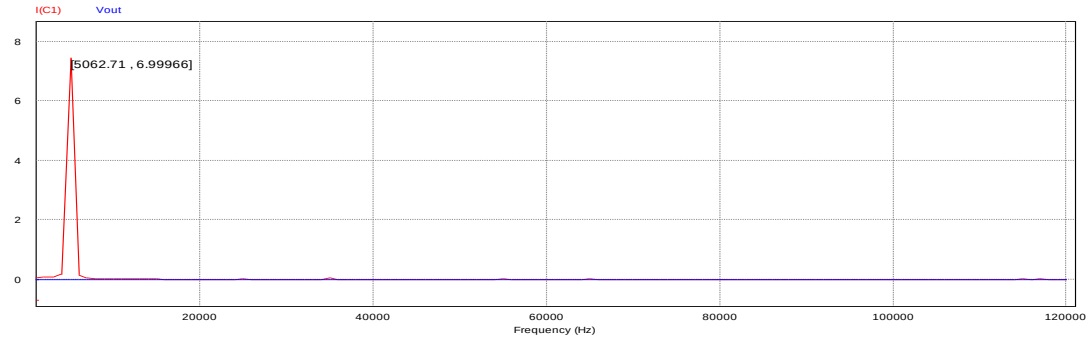


Fig. 4.27 Inverter model with isolation transformer under capacitive load

For this type of load the following current waveform and FFT analysis simulation result are obtained as seen from Fig. 4.28.

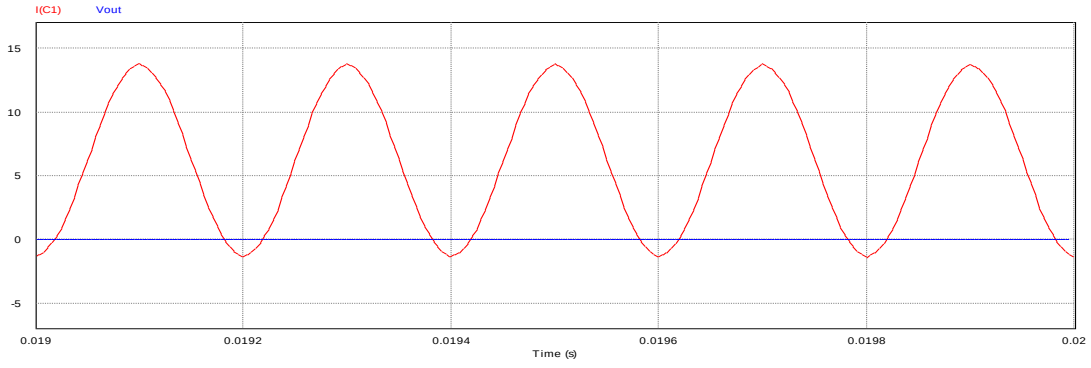


(a) Current and voltage output waveform of the inverter with isolation transformer, C=100F

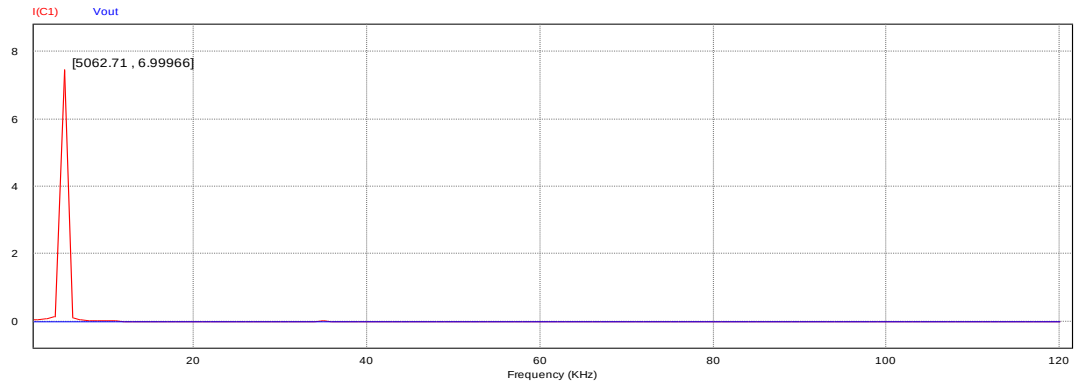


(b) FFT analysis of the inverter without isolation transformer, C=100F

Fig. 4.28 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, C=100F

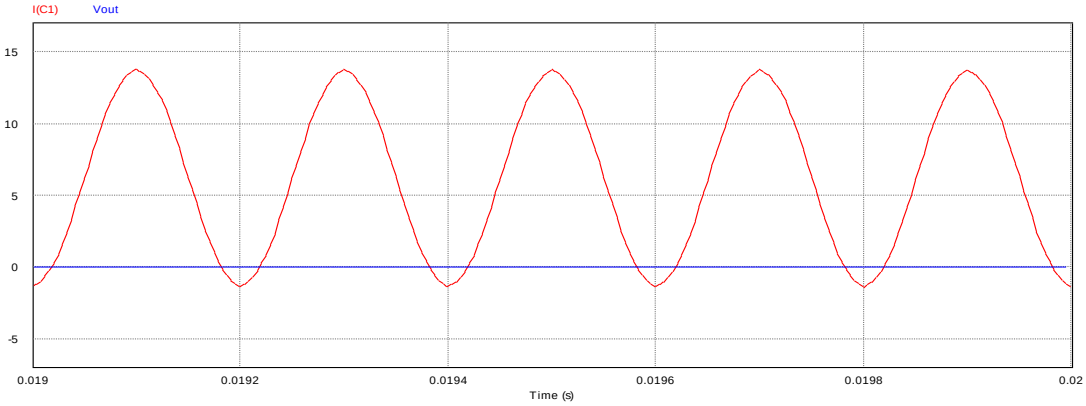


(a) Current and voltage output waveform of the inverter with isolation transformer, C=500F

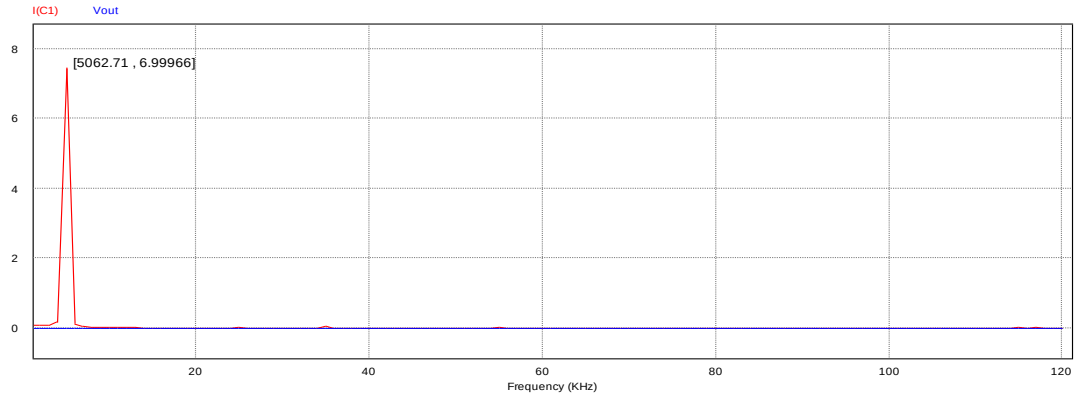


(b) FFT analysis of the inverter without isolation transformer, C=500F

Fig. 4.29 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, C=500F



(a) Current and voltage output waveform of the inverter with isolation transformer, C=1000F



(b) FFT analysis of the inverter without isolation transformer, C=1000F

Fig. 4.30 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, C=1000F

As seen from the FFT analysis, the harmonic level is almost completely suppressed only the fundamental components are available. Because the capacitors served as perfect filter that improve the harmonic distortion to the lowest minimum. In almost all of the current waveform and corresponding FFT analysis plot, a fundamental magnitude values is maintain under different capacitive loads

4.7 COMBINATION OF RESISTIVE, INDUCTIVE, AND CAPACITIVE LOAD ANALYSIS

A combination of resistor-inductor, resistor-capacitor, inductor-capacitor, and combination of both was simulated in each case at 100 nominal values. The value was selected arbitrarily to represent approximate value for the purpose of design and simulation. The actual impedance may vary considerably depending application, in this study nominal impedance is implicitly referring to the frequency response of the circuit under consideration, in which the change in voltage or current waveform, and harmonic level of the inverter is observed.

4.7.1 Case 1: Resistor-Inductor Analysis

For the case of resistor-inductor analysis, the structure was model as show in Fig. 4.31, it provide approximate scenario of the system.

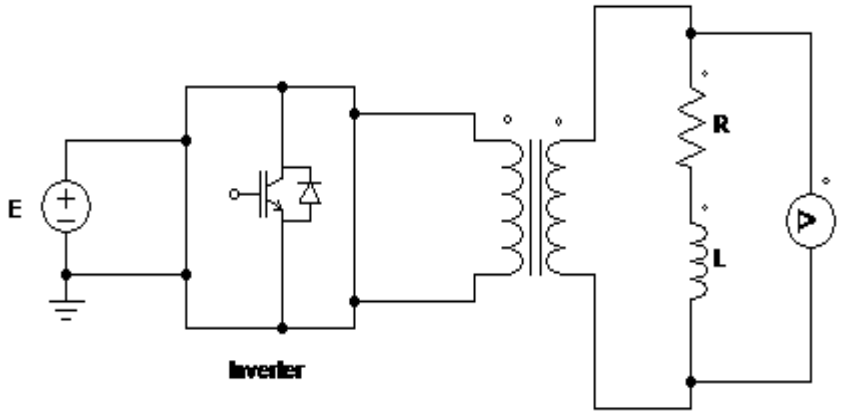
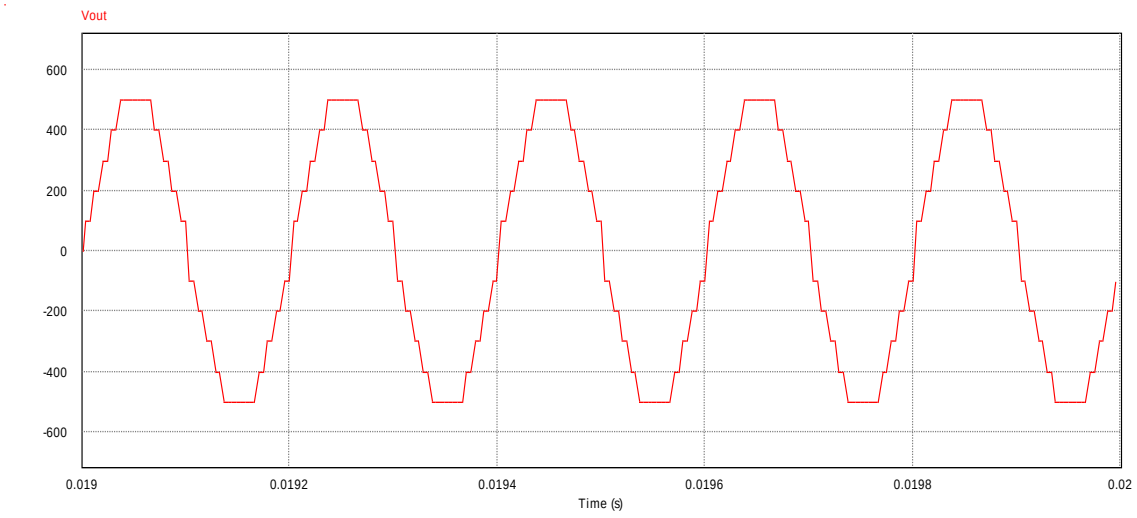
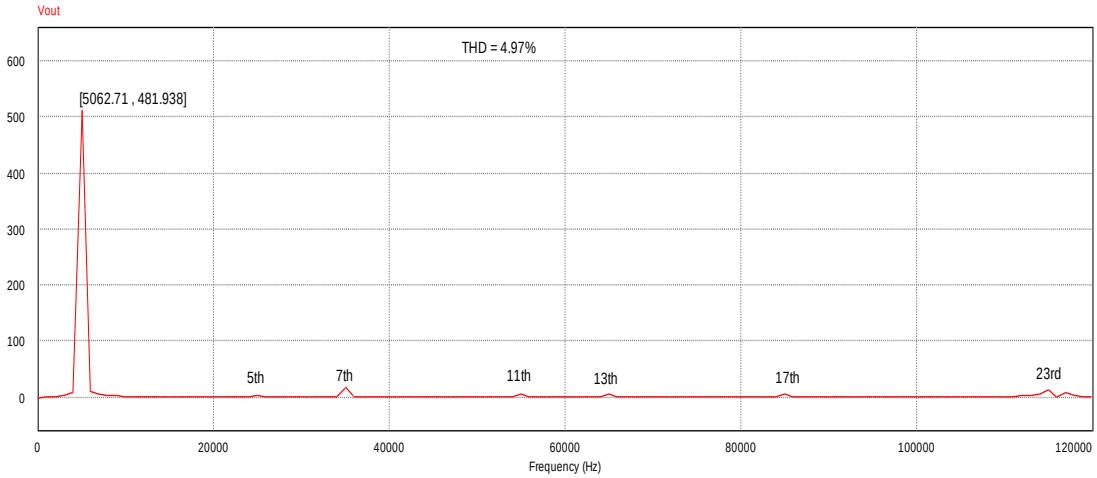


Fig. 4.31 Inverter model with isolation transformer under resistor-inductor load



(a) Voltage output waveform of the inverter with isolation transformer, R=100 Ω, L=100H



(b) FFT analysis of the inverter without isolation transformer, R=100 Ω, L=100H

Fig. 4.32 Voltage and FFT analysis of inverter with isolation transformer f_{sw} = 5 kHz, R=100 Ω, L=100H, and THD = 4.97%.

From the Fig. 4.32 (a) shows voltage waveform under resistor-inductor load, while Fig.4.32 (b) shows the fast Fourier transform (FFT) spectrum of the wave. Based on the plot, it can be seen that, the staircase wave is generated under this loading combination with uniform period. From the FFT analysis it also seen that, the fundamental voltage obtained is much higher in amplitude compared with that of harmonic.

4.7.2 Case 2: Resistor-Capacitor Analysis

In resistor-capacitor the structure model as in Fig. 4.33, with R = 100Ω and C = 100F is used in the simulation.

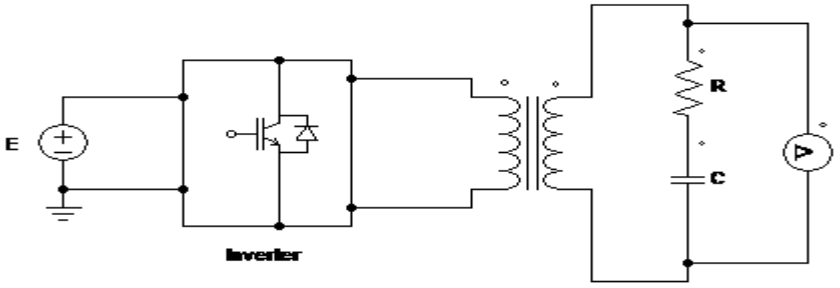
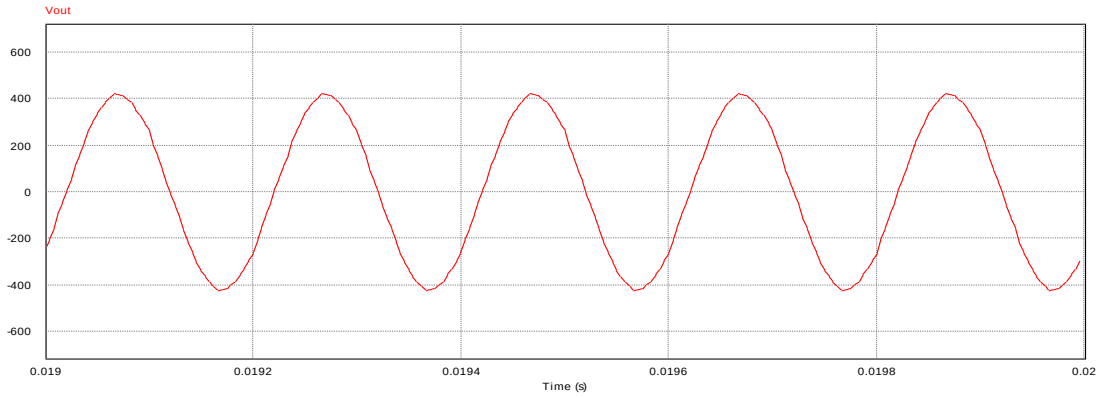
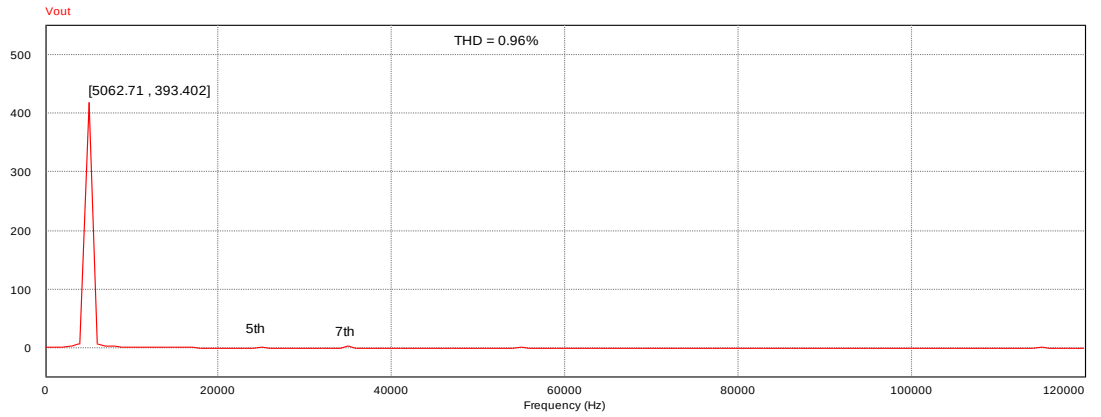


Fig. 4.33 Inverter model with isolation transformer under resistor-capacitor load



(a) Voltage output waveform of the inverter with isolation transformer, R=100 Ω, C=100F



(b) FFT analysis of the inverter without isolation transformer, R=100 Ω, C=100F

Fig. 4.34 Voltage and FFT analysis of inverter with isolation transformer fsw = 5 kHz, R=100 Ω, C=100F, and THD = 0.96%.

From the Fig. 4.34 (a) shows voltage waveform under resistor-inductor load, while Fig.4.34 (b) shows the fast Fourier transform (FFT) spectrum of the wave. The voltage waveform depicts sinusoidal in nature under the load condition, the wave quality is good compared to other combination. From the FFT spectrum plot it can be seen that, almost harmonic component are eliminated, which result in producing THD of 0.96%.

4.7.3 Case 3: Inductor-Capacitor Analysis

As model in the previous case, in this case the circuit structure was approximated and model as shown in Fig. 4.35. The value of L =100 H and C = 100 F is simulated.

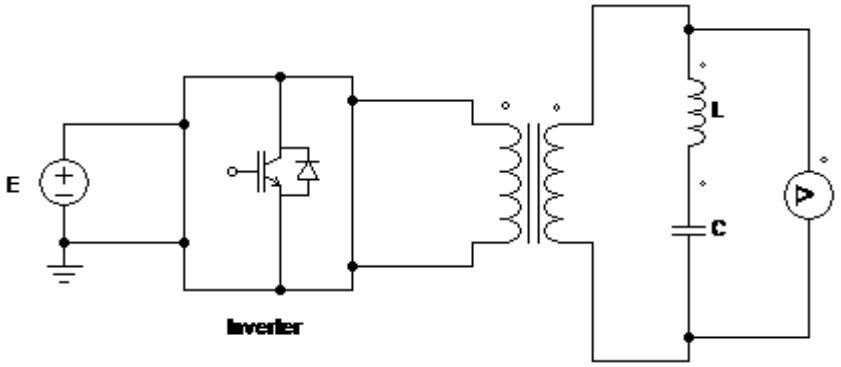
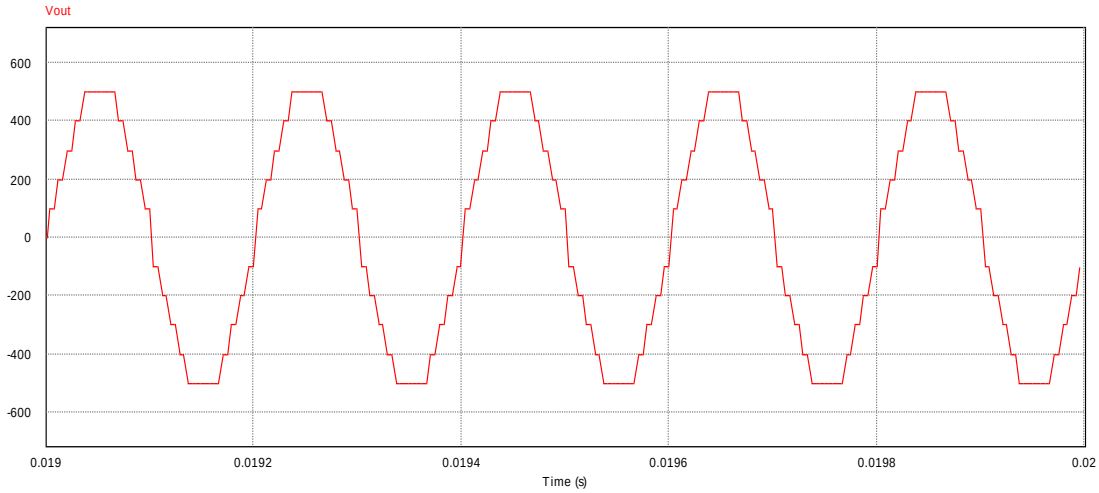
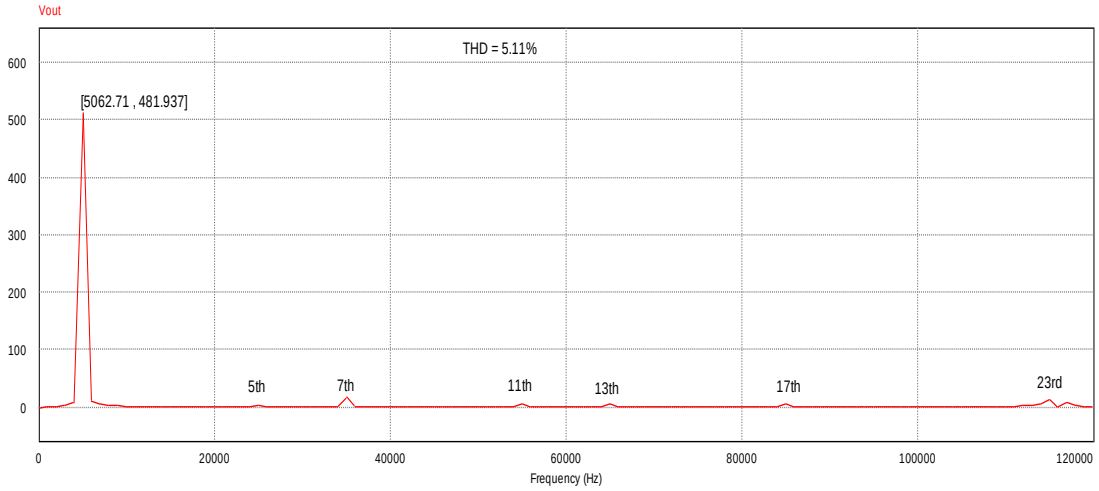


Fig. 4.35 Inverter model with isolation transformer under inductor-capacitor load



(a) Voltage output waveform of the inverter with isolation transformer, L=100 H, C=100F



(b) FFT analysis of the inverter without isolation transformer, L=100H, C=100F

Fig. 4.36 Voltage and FFT analysis of inverter with isolation transformer fsw = 5 kHz, L=100 H, C=100F, and THD = 5.11%

From the Fig. 4.36 (a) shows voltage waveform under resistor-inductor load, while Fig.4.36 (b) shows the fast Fourier transform (FFT) spectrum of the wave. Based on the plot staircase voltage waveform is generated with some distortion is generated under the load condition, this distortion rise the THD to 5.11% in the FFT analysis spectrum plot.

4.7.4 Case 3: Resistor-Inductor-Capacitor Combination Load Analysis

The combination resistor-inductor-capacitor is model as in Fig. 4.37, with R=100Ω, L=100 H, and C=100 F are used in the simulation as given in the model.

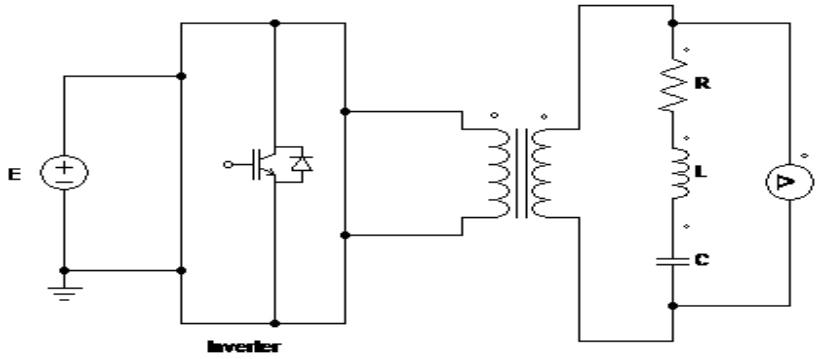
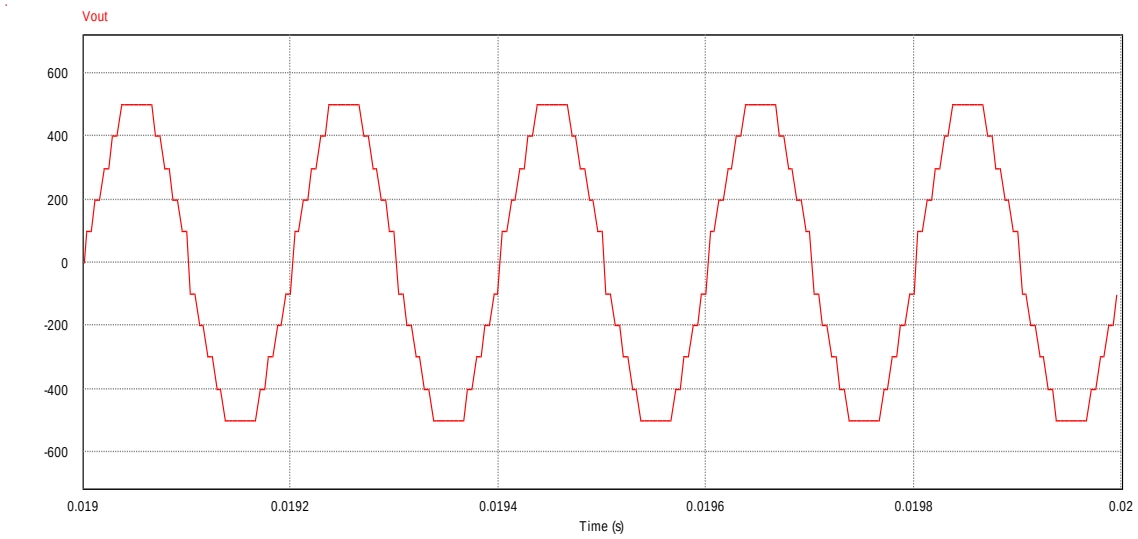
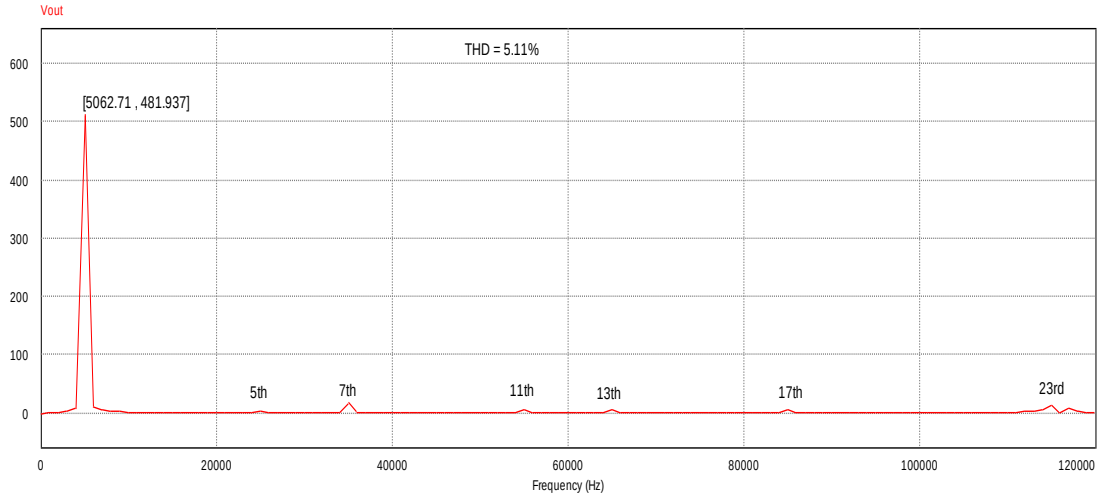


Fig. 4.37 Inverter model with isolation transformer under resistor-inductor-capacitor load



(a) Voltage output waveform of the inverter with isolation transformer, R=100 Ω, L=100 H, C=100F



(b) FFT analysis of the inverter without isolation transformer R=100 Ω, L=100H, C=100F

Fig. 4.38 Voltage and FFT analysis of inverter with isolation transformer fsw = 5 kHz, R= 100 Ω, L=100 H, C=100F, and THD = 5.11%

Simulation of diffirent conbination of load is perform and the result shows the output waveform in either case remain unchange or improve in power quality. Also the harmonic level for both the case is withing the IEEE standard level. The Table 4.4 summerise result under different load condition.

Table 4.4 Combination of different load against THD

Load	RL	RC	LC	RLC
THD (%)	4.97	0.96	5.11	5.11
Vout (V)	481.937	393.402	481.937	481.937

From the waveform figure and table, a case in which inductive load are applied a more staircase waveform output voltage are realise and output voltage level are maintained.

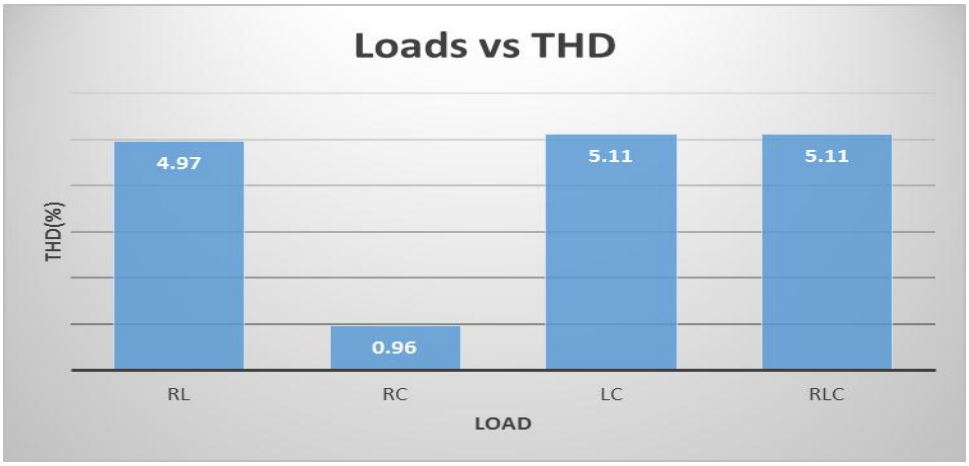


Fig. 4.39 Different conbination load against THD

From Table 4.4 and Fig. 4.39 it clearly shows that combination of resistor-capacitor has the lowest THD compare to the rest, meaning for filter design of this inverter type capacitor filter will be of signifcant choice. For RL, LC, and RLC are having almost similar harmonic contain level. From the Table4.4 we observed that, voltage amplitude value for all the cases are almost within the same range, except under RC load voltage drop compare to the others, but the RC load generate minimum THD values. Finally all the simulation result otained are withing theoritical expectation and provided us with detail characteristic of multlevel inverter performance characteristic under different load condtion prior to implementation.

CHAPTER 5

EXPERIMENTAL RESULT

5.1 INTRODUCTION

A laboratory experiment of 500 watt pulse width modulation 2-level power inverter was carried out. Typically inverter converts DC battery voltage into the conventional household AC voltage allowing electrical device to operate when supply utility authority are not available. This inverter can be a single-phase or three-phase depending on the application. The output signal waveform of the inverter can be square wave, modified sine wave, and pure sine wave. In this experiment a modified sine wave single phase inverter is considered, it produces square wave with some dead spot between the positive and negative cycle. Because of its key advantages such as operation with clean power like utility-supplied electricity, reduction in audible and electrical noise in Fans, fluorescent lights and so on. This type of the inverter usually operated on pulse width modulation techniques, in this techniques gate pulses are controlled by various mechanism. The method in which the low DC is inverted completed in two steps, the first step is conversion of low voltage DC to high voltage DC source, and the second step is the conversion of the high DC source to an AC wave using pulse width modulation [41].

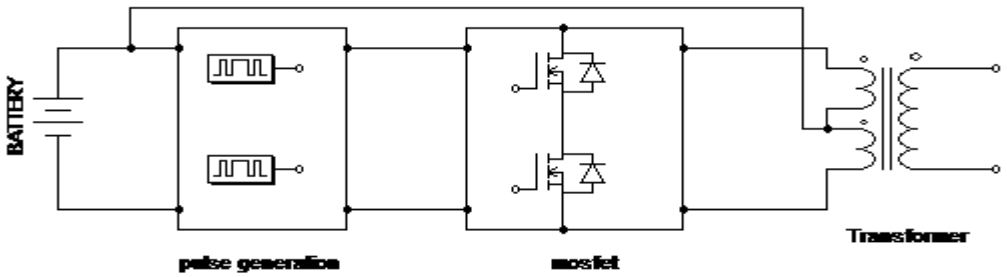


Fig. 5.1 Proposed 500 watt inverter model

Another method to complete the desired outcome would be first to convert the low voltage DC power to AC, and then use a transformer to boost the voltage to 220 volts, the second method was used in the experiment. The proposed inverter is given in Fig. 5.1 representing major four component part include the following DC battery source, the signal frequency generator (driver), the power mosfet block, and the transformer, all these will be discussed later.

5.2 CIRCUIT OPERATION

The Fig. 5.2 depicts the general circuit schematic, it comprises four major component as mention above; the 555 timer configure as an astable mode oscillator generating a frequency of 200Hz, a CD4017 decade counter that divide the frequency of oscillation to 50Hz, a power mosfet that converts low DC power to AC, and the transformer which boost the voltage to 220 volt. The operation of simple but powerful and efficient schematics diagram for a 500 watt modified sine wave inverter circuit was explained below. First the 555 timer device is precision timing circuit capable of producing accurate time delays or oscillation is configured as Astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors R_1, $R_2$and a single capacitor C_2 as shown in the diagram, producing controlled frequency of 200 Hz.

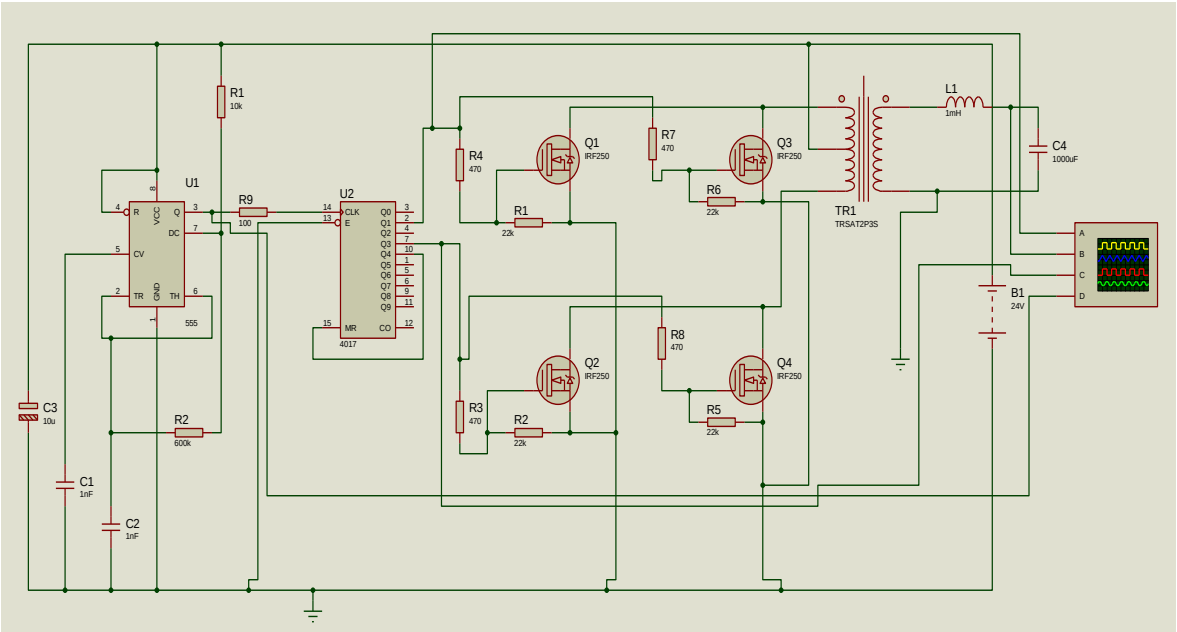


Fig. 5.2 Schematic diagram of the inverter

A decade counter CD4017 is a 5-stage divided by 10 counter, with 10 decoded output and a carry bit. This counter is clear to count by logic "1" on its reset line. It divides the 200Hz frequency produced by 555 timer to a stable 50 Hz this frequency serve as inverter frequency, with need of these two integrated circuit a pulse signal are generated.

Pin 2 and pin 7 of the decade counter CD4017 and fed to the gate of power mosfet as a driver. Pin 15 is the counter reset line; pin 10 is connected reset line to make it high, for the next set cycle of pulse generation, the scenario keep on repeating continuously generating gate pulses.

The IXTQ75N10P logic mosfet are N-channel enhancement mode that required 5 V to switch on fully to the maximum of 100V, they have very low 0.025Ω drain to source resistance. When 'ON' the device can switch high current of 75A. The device produces less heat, but heat sink is require for longer time of operation, this will keeps the whole system efficient. A centre tap transformer of 12-0-12V/ 220V was connected in reverse, using a low voltage side as primary, and high voltage side as secondary to produce the required voltage output level. In general, taking into consideration the transformer rating specification, and the mosfet output property characteristic, this allowed the mosfet to drive the transformer of the inverter efficiently.

5.3 EXPERIMENTAL PROCEDURE

A step by step procedure is follows for the experimental analysis to achieve the desired goal i.e.

I. Software verification using proteus

II. Practical implementation

For First step, the schematic in Fig. 5.2 was design in Proteus software package prior to implementation to investigate the circuit workability. After designing the circuit unit by unit on the software, a circuit simulation was run, some abnormalities was observed that require debugging and troubleshooting, having successfully rectified the problem. Another simulation was run again, the scope software is observed and this result was monitor as presented in Fig. 5.3. As earlier explained, the scope shows individual result in respect of each separate unit on different channel, channel D is the output of 555 timer unit configure as Astable mode, with oscillation frequency of 50% duty cycle, channel A and C are

decade counter pin 2 and pin 7 output pulse that serves as gate driver to the mosfet switching.

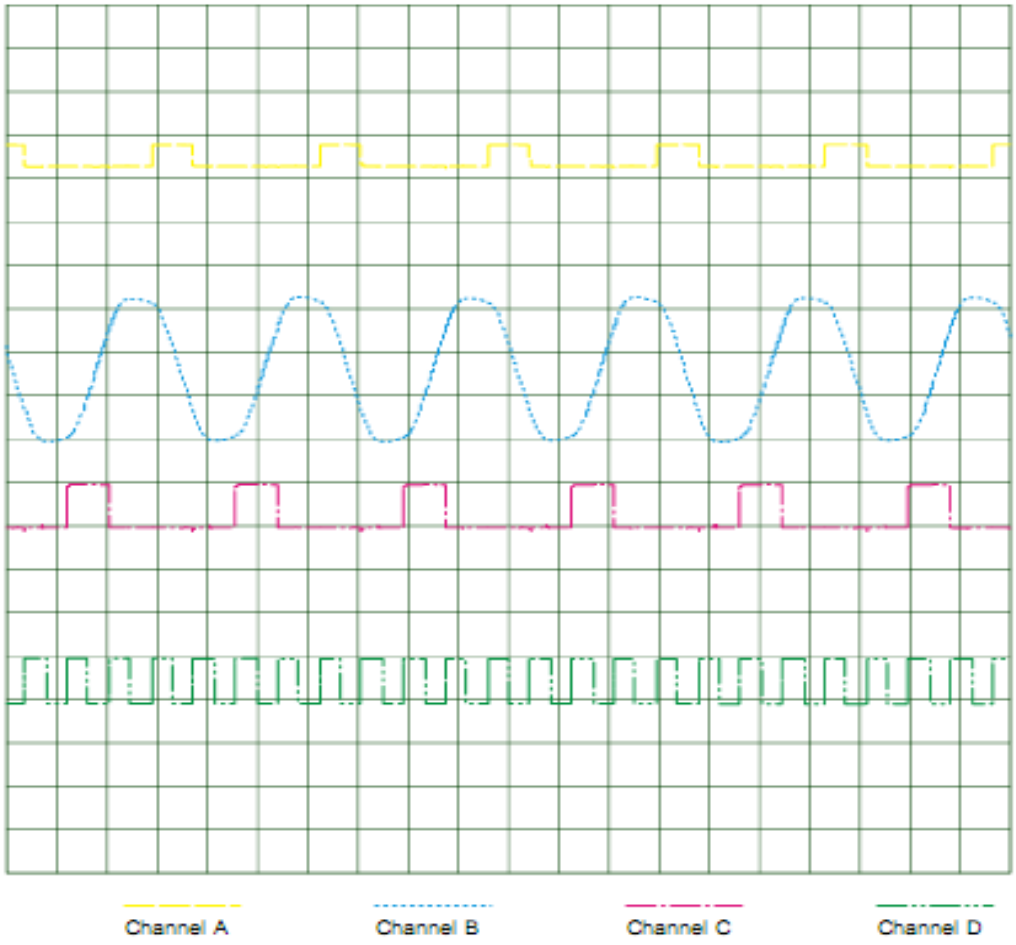
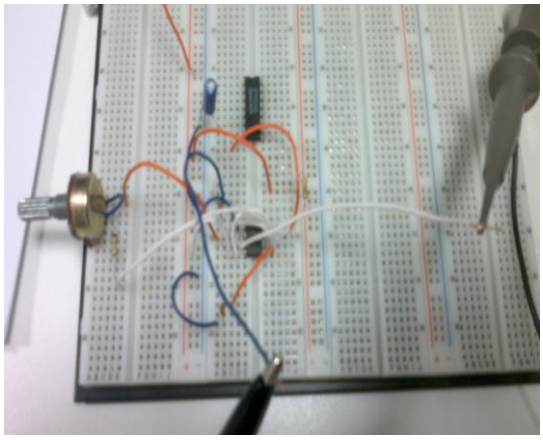


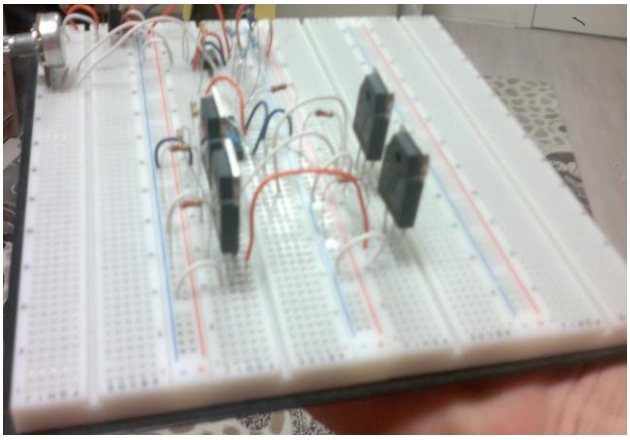
Fig. 5.3 Proteus scope display

Channel B displays the inverter output signal waveform as the transformer output, the output signal waveform look like modified sine wave. This allows us to proceed with practical implementation, since each unit are working effectively.

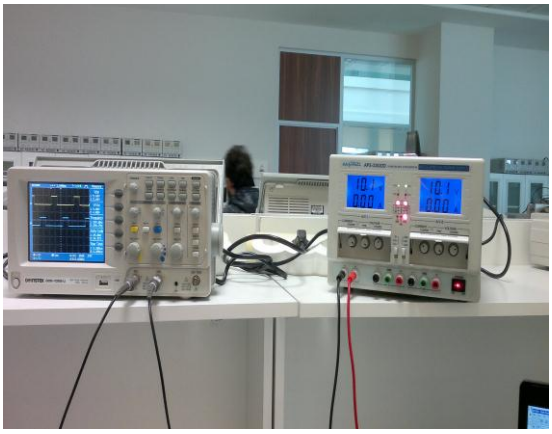
After the circuit has been tested using proteus software package, the second procedure was developed in the laboratory to further ascertain the simulation result. As describe the project experiment is developed unit by unit on the breadboard, necessary precaution was consider not over supply semiconductor devices beyond operating voltage level. The figures below give some pictures capture during the laboratory practical. The variable resistor is attached to adjust the frequency of 50 Hz or 60 Hz depending of country utility.



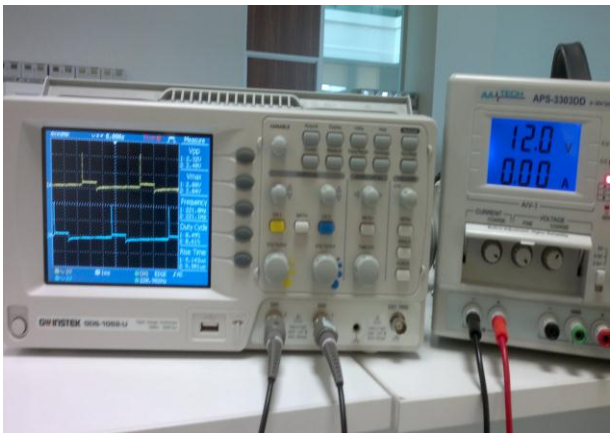
a) gate signal unit



b) complete circuit unit



c) Gate signal unit display



d) mosfet output unit display

Fig. 5.4 Caption of some practical procedure

After successfully testing each unit separately to verify its operation, a complete circuit was constructed on breadboard and again another test was carried out to the whole integrated circuit. A transformer of 500 watt 12 V/220 V was connected to further analysis the inverter on load. Box of 5 x 4 filament bulb of different watt rating was used as load system to investigate the inverter performance.

5.4 EXPERIMENTAL RESULT

The experimental result of voltage waveform and harmonic were captured and displayed using a digital power quality analyzer (FLUKE 34B) and using device FFT features the output harmonic was obtained. Several voltage waveforms are captured for both no-load and load. The experimental results are display as below; the first result capture is shown in Fig. 5.5 the waveform reaches an amplitude of 222 V but contain many ripple, because no filter was connected at the output.

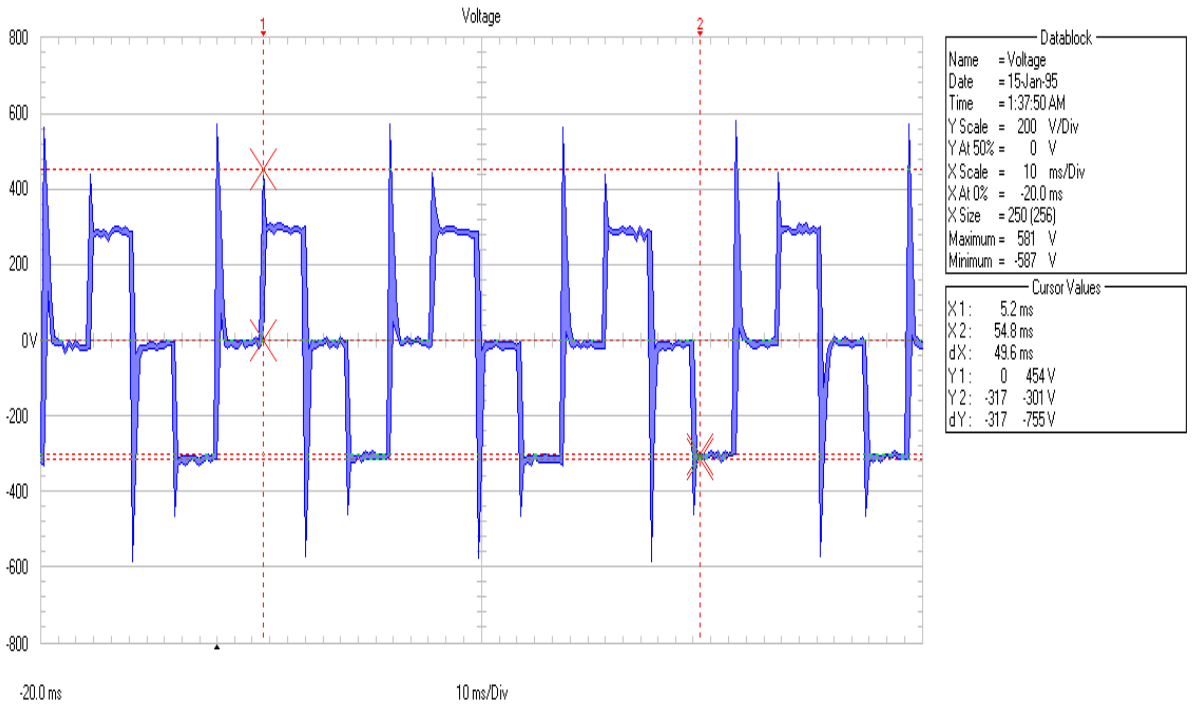


Fig. 5.5 Voltage output at 222V, 50.9 Hz having many ripple on no-load without filter

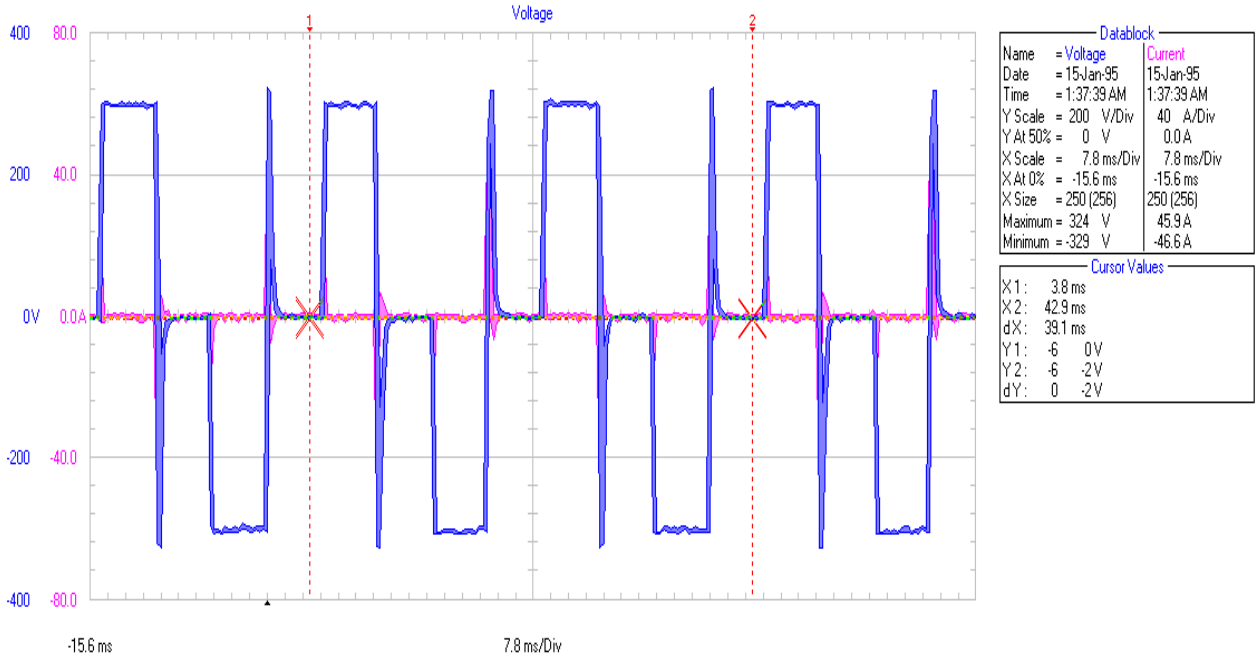


Fig. 5.6 Voltage output at 221.8V, 50.8Hz on load without filter

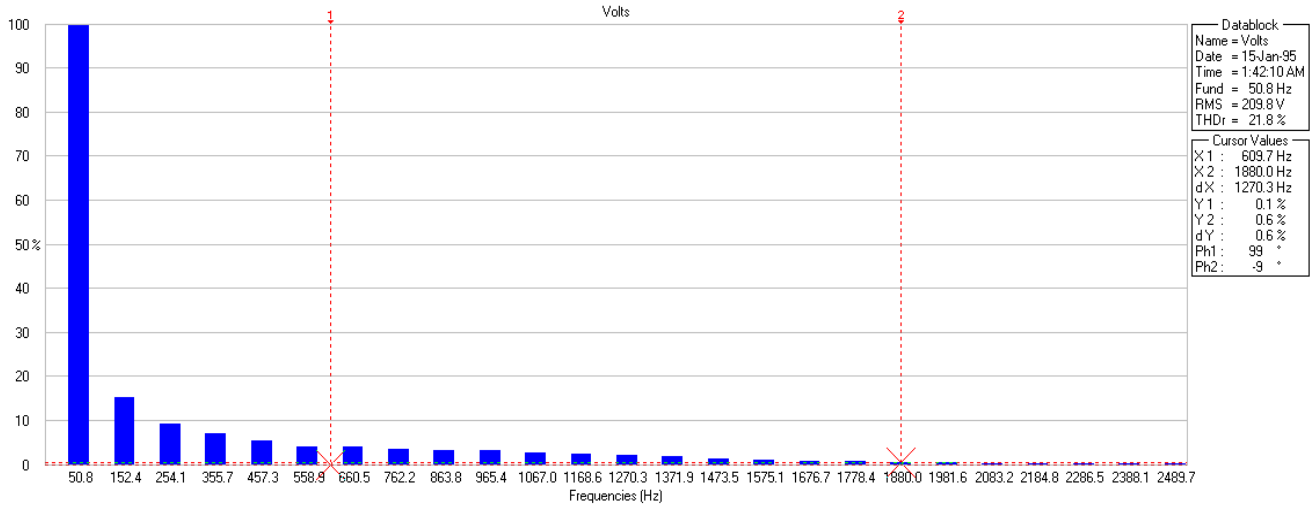


Fig. 5.7 FFT analysis of the voltage output without filter on load THD = 21.8%

The FFT analysis of output voltage on load shows fundamental component reaches 100% voltage level. Having observed the above result a ceramic capacitor filter of 0.01µF, 630V was incorporated and the following no-load and load result was capture and displayed below.

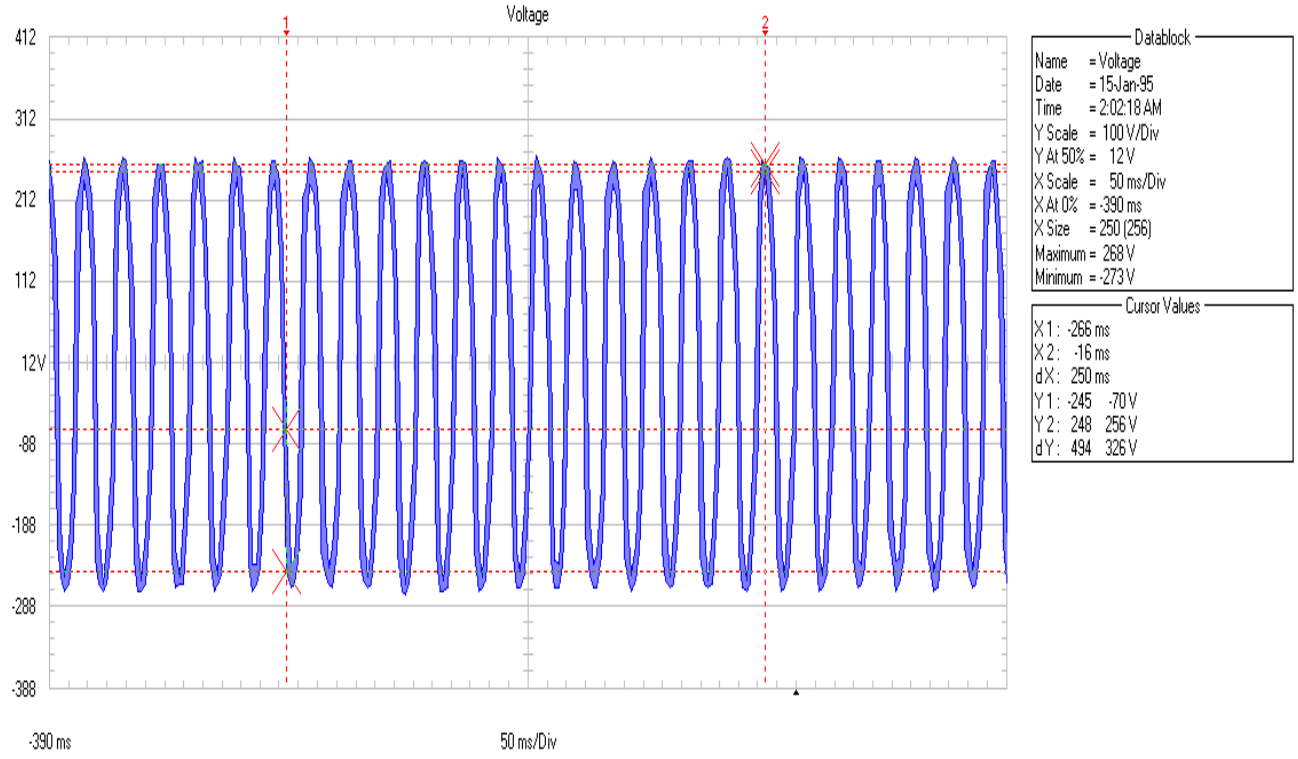


Fig. 5.8 Voltage output at 208.8V, 50.3Hz when capacitor filter is apply on no-load

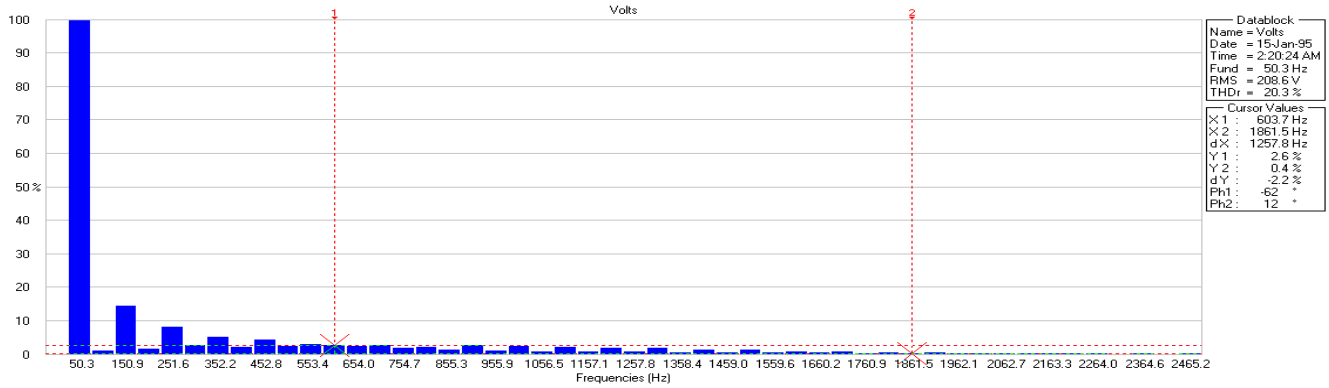


Fig. 5.9 FFT analysis of the voltage output on no-load THD = 20.3%

When the filter are connected across the output terminal a significant improvement in the output voltage waveform quality was observed, the load was apply and the following result are capture with Fluke 43B (Power Quality Analyzer) device for displayed as in Fig 5.10 and Fig 5.11.

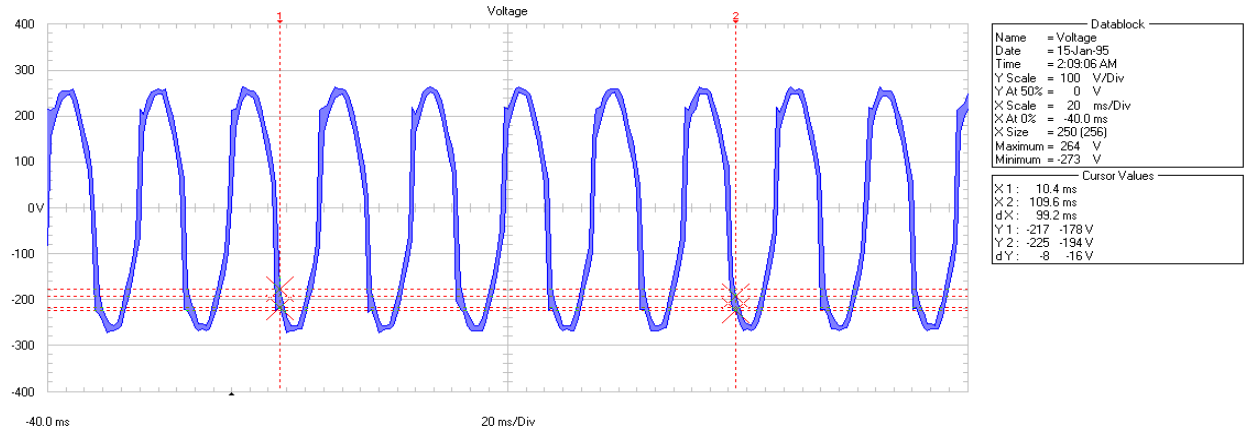


Fig. 5.10 Voltage output at 209.6V, 50.7Hz when capacitor filter are apply on load

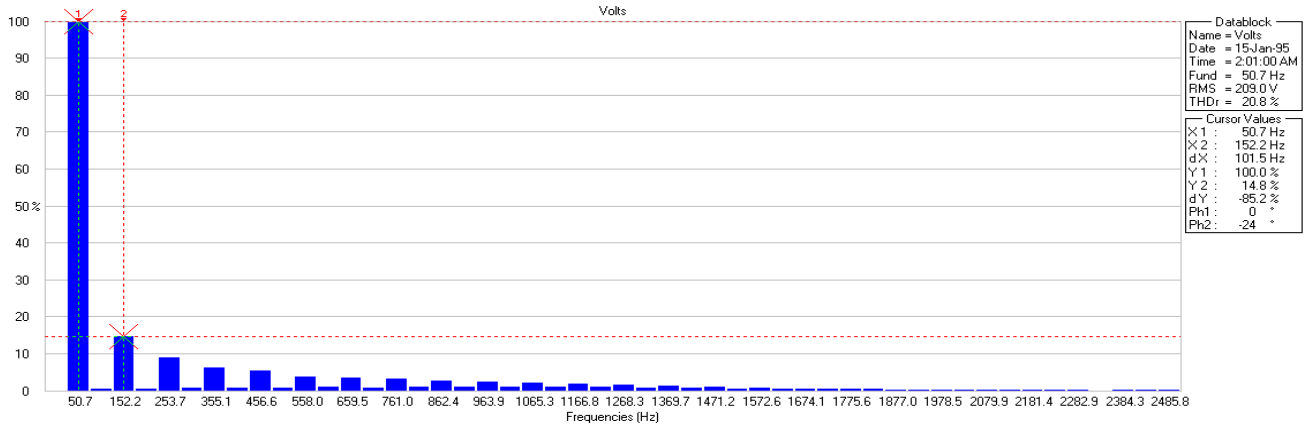


Fig. 5.11 FFT analysis of the voltage output on load THD = 20.8%

From the Fig. 5.11 the fundamental component reaches 100% level as shown by cursor 1 and the first odd harmonic was at 15% as shown by cursor 3, meaning this harmonic will not affect the inverter performance. The voltage waveform is modified sine wave, not purely sine due present of some dead spot to positive and negative cycle voltage waveform. With above result more research on filters may lead to obtain a pure sine wave output voltage with this inverter.

Finally, the experimental analysis of the inverter was successfully carried out in the laboratory, and performance characteristic of the inverter was investigated, the voltage output and harmonic distortion on load and no-load test are within experimental limit.

CHAPTER 6

CONCLUSION AND RECOMMENDATION

6.1 CONCLUSION

An eleven multilevel inverter using cascaded bridge topology with a single DC supply voltage source has been modeled and simulated. Two different cases have been investigated with two different frequencies, the first case without isolation transformer while the second case with isolation transformer. The second case produces better output results, both cases have been proven to be within the desirable results under different load conditions. The harmonic distortions magnitude orders depends upon the category of the inverter structure used and modulation control employed. The reported inverter addresses the issue of using multiple independent dc-link sources to synthesize multilevel output voltage waveforms and it also reduces the number of switching device compare to ordinary conventional multilevel inverter generating the same voltage level. These features make the inverter to be compact in size, less complex and reduced cost of production and maintenance.

Based on the simulation results obtained for both cases, it appears that SHE has the ability to eliminate selected harmonics by chopping of the fundamental component at certain pre-determined angles. The inverter is able to eliminate a certain range number of odd harmonics while the remaining higher frequency order harmonics will be eliminated with small size filter if desired. The triple harmonics order cancelled out automatically due to the proper configuration and symmetry of switching angle pattern arrangement. In addition, it satisfies the IEEE 5% THD within the targeted range, IEEE STD 519 – 1992 harmonic limit.

All simulation results yielded a positive outcome, giving the an upper hand over it counter parts and the possibility to cover wide range of application both in medium and high power application as well as renewable energy interface.

Laboratory experiment of 500 watt single-phase 2-level inverter was successfully carried out, and tested under load and no-load condition, producing positive result that is capable of serving household and offices application.

- In summary, multilevel inverters are considered today as the state-of-art power conversion system for high power- medium voltage and power quality demand applications.
- While single phase 2-level inverters are considered mostly used for residential and offices applications.
- In addition, leading manufacturers in power electronics drive commercialized multilevel inverters covering a wide variety of topology, control method and application.
- The harmonic distortion level of the inverter largely depends on the nature of the structure and loads apply.

Hence based on the results obtained, it can be concluded that, the objectives of the research have been achieved within the limit of simulation and experimental error.

6.2 FUTURE RECOMMENDATION

The followings are some recommendations that can be beneficial for further research on the area of multilevel inverters:

1. Prototype implementation of this multilevel inverter to ascertain various analysis carried out so that commercial version will be available in the market.
2. The control algorithm should be implemented using microcontroller or digital signal processing for better switching speed.
3. The inverter level can be increased by either connecting additional H-bridge module, or using transformer with specified turn ratio.
4. Distribution the IGBT switching stress by utilizing the redundant switching angles.
5. To study and design the inverter using different modulation techniques

6. For 2-level inverter, a powerful pulse width modulation technique or device is required to improve the power quality and reduce distortion.

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