İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

0.1-8GHz CMOS DISTRIBUTED AMPLIFIER

M.Sc. Thesis by
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Programme: Electronics Engineering

JUNE 2007

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0.1-8GHz CMOS DAĞILMIŞ PARAMETRELİ KUVVETLENDİRİCİ

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CONTENTS

LIST OF ABBREVIATIONS

CMOS	: Complementary Metal Oxide Semiconductor
GaAs	: Gallium Arsenide
RF	: Radio Frequency
ESD	: Electrostatic Discharge
SiGe	: Silicon Germanium
BiCMOS	: Bipolar and Complementary Metal Oxide Semiconductor
DA	: Distributed Amplifier
MIM	: Metal Insulator Metal
MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
LNA	: Low Noise Amplifier
MESFET	: Metal Junction Field Effect Transistor
BW	: Bandwidth
CS	: Common-source
CC	: Cascode
CPW	: Coplanar Waveguide
F	: Noise Factor
NF	: Noise Figure
BSIM	: Berkeley Short-channel IGFET Model
NQS	: Non-quasi-static
PSD	: Power Spectral Density
W.I.	: Weak Inversion
S.I.	: Strong Inversion

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LIST OF SYMBOLS

A_{for} : Forward voltage gain
A_{rev} : Reverse voltage gain
C_{gs} : Gate-source capacitance
C_{gd} : Gate-drain capacitance
C_{jd} : Drain-bulk capacitance
f_c : Cutoff frequency of an artificial line
f_T : Unity current gain frequency
f_{max} : Maximum frequency of oscillation
g_m : Transconductance
G_{for} : Forward power gain
G_{rev} : Reverse power gain
N : Number of gain stages
N_{opt} : Optimum number of gain stages
θ : Propagation factor
ω_c : Radial cutoff frequency of an artificial line
Z_g : Input artificial transmission line termination
Z_d : Output artificial transmission line termination
Z_0 : Characteristic impedance
$Z_{0\pi}$: Constant-k π filter section image impedance
$Z_{0\pi m}$: m-derived π filter section image impedance
Z_{0T} : Constant-k T filter section image impedance

0.1-8GHz CMOS DAĞILMIŞ PARAMETRELİ KUVVETLENDİRİCİ

ÖZET

Geniş bantlı kuvvetlendiricilerin ölçüm düzenleri, askeri elektronik, televizyon, radar ve geniş bantlı optik haberleşme gibi birçok kullanım alanı bulunmaktadır. Bu uygulamalar için genellikle dağılmış parametreli kuvvetlendirici yapısı kullanılmaktadır. Çünkü bu yapı klasik kazanç-bant genişliği ilişkisi ile sınırlanmamaktadır.

Dağılmış parametreli kuvvetlendirici yapısında kazanç elemanlarının giriş ve çıkış kapasiteleri, yapay iletim hatlarının içine dahil edilmektedir. Böylece farklı hücrelerin kapasiteleri birbirlerinden ayrılmakta, aynı zamanda çıkış akımları ise hala toplanabilmektedir.

Son on yılda boyut alanında devam eden küçülme sayesinde, eşlenik metal-oksit-yarıiletken (CMOS) teknolojisi dağılmış parametreli kuvvetlendirici gerçekleştirmek için ciddi bir alternatif olmuştur. Ayrıca CMOS dağılmış parametreli kuvvetlendiriciler düşük maliyet ve temel bant devreleriyle tümleştirme avantajlarına da sahiptir.

Bu tezin en genel amacı dağılmış parametreli kuvvetlendirici tasarım tekniklerini araştırmak ve bu teknikleri kullanarak 0.35µm CMOS teknolojisi ile tamamen tümleştirilmiş bir dağılmış parametreli kuvvetlendirici gerçekleştirmektir. Teorik araştırmaları ve benzetim sonuçlarını doğrulamak amacıyla 0.35µm CMOS teknolojisi ile tek uçlu bir kuvvetlendirici tasarlanmış ve üretime gönderilmiştir. Bu kuvvetlendirici 0.1-8GHz aralığında 8±1 dB kazanç sağlamakta ve 1.5V beslemeden 18mA akım çekmektedir. Kuvvetlendiricinin toplam alanı 1.67x0.93 mm^2 dir.

0.1-8GHz CMOS DISTRIBUTED AMPLIFIER

SUMMARY

Wideband amplifiers have many applications such as instrumentation, electronic warfare, television, pulsed radars and broad-band optical communication. For such applications, a distributed amplifier (DA) topology is often employed since it is not limited by the classical gain-bandwidth tradeoff of amplifiers.

In a DA topology input and output capacitances of gain elements are incorporated into the artificial transmission lines. So that the capacitances of different cells are separated while their output currents can still be summed.

In the last decade, Complementary Metal Oxide Semiconductor (CMOS) technology has become a serious alternative for realizing DAs as a result of continuous scaling in the technology. Also CMOS DAs have the advantages of low cost and integration ability with baseband circuits.

The global objective of this thesis is to investigate design techniques for the CMOS DA, and to use these techniques to demonstrate a fully integrated DA using 0.35μm CMOS technology. To verify the theoretical investigations and simulation results, a single ended distributed amplifier was designed in 0.35μm CMOS technology and sent to the fabrication. The amplifier achieves 8±1 dB gain over 0.1-8 GHz band while drawing 18mA from 1.5V power supply. The total area of the amplifier is 1.67x0.93 mm^2.

1. INTRODUCTION

Broadband amplifiers have many applications such as instrumentation, electronic warfare, television, pulsed radars, and broad-band optical communication. For such applications, a distributed amplifier (DA) topology is often employed since it is not limited by the classical gain-bandwidth tradeoff of amplifiers.

Distributed amplifiers (DAs) have been widely used for realizing broadband amplifiers in high-speed GaAs MESFET technologies. Recently, DAs have also been realized in CMOS technology because of the advantages such as low cost and integration ability with baseband circuits.

The distributed amplification concept was first proposed by Percival in 1937 [1], whereas the term "distributed amplifier" first pronounced in a paper by Ginzton et al in 1948 [2].

The basic distributed amplifier consists of a pair of transmission lines, called gate line and drain line, and transistors as shown in Figure 1.1. The gate line is periodically loaded by the MOSFET input capacitance and the drain line is periodically loaded by the MOSFET output capacitance. Also, both lines are terminated in their characteristic impedances at one end.

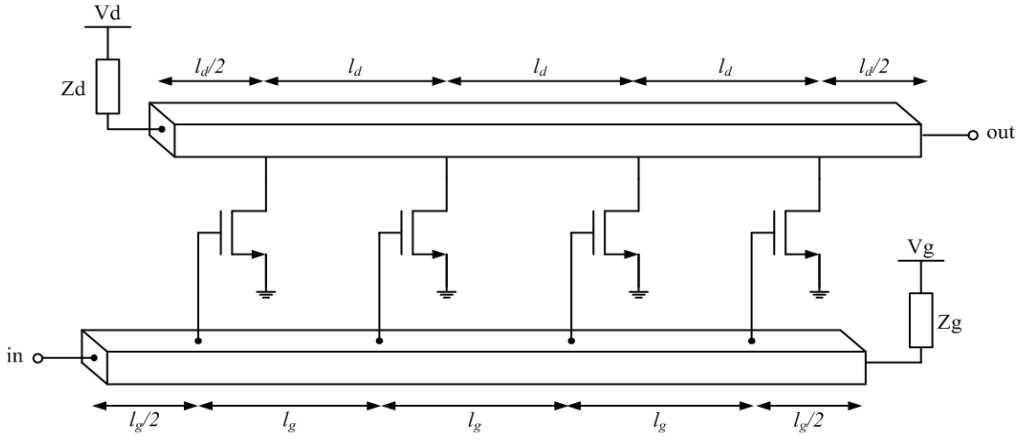

Figure 1.1: A distributed amplifier realized with transmission lines

As the input signal travels on the gate line toward the gate termination Z_g, each transistor is excited by the traveling wave and transfers the signal to the drain line. If the phase velocities on the gate and drain lines are equal then the currents from different stages arrive at the output in phase, therefore these currents are summed completely. On the other hand, the currents flowing toward the drain termination Z_d, arrive out of phase and any remaining signal is absorbed by the drain-line termination.

The transmission lines shown in Figure 1.1 can be approximated by lumped inductors and capacitors as shown in Figure 1.2. In this approach, the gate and drain capacitances of the transistors are absorbed into artificial transmission lines formed by lumped inductors and capacitors. An artificial transmission line has properties similar to that of real transmission line up to its cutoff frequency, f_c. Thus, DA topology allows one to separate the parasitic capacitances of the gain stages while adding their output currents. To achieve good impedance matching over a very wide bandwidth, the characteristic impedances of the gate and drain lines are set equal to the source and load impedances, respectively.

Furthermore, the gain-bandwidth of a DA is not limited by unity-gain frequency f_T, of the transistor since the parasitic capacitances of the transistor are absorbed into the transmission lines or the LC ladder filter to become part of the passive network. Unlike cascaded amplifiers, where the gain of the each stage is multiplied, the gain of the DA is the sum of each stage gain. Thus, the gain is relatively low; however, the distributed capacitance allows the amplifier to achieve very wide bandwidths.

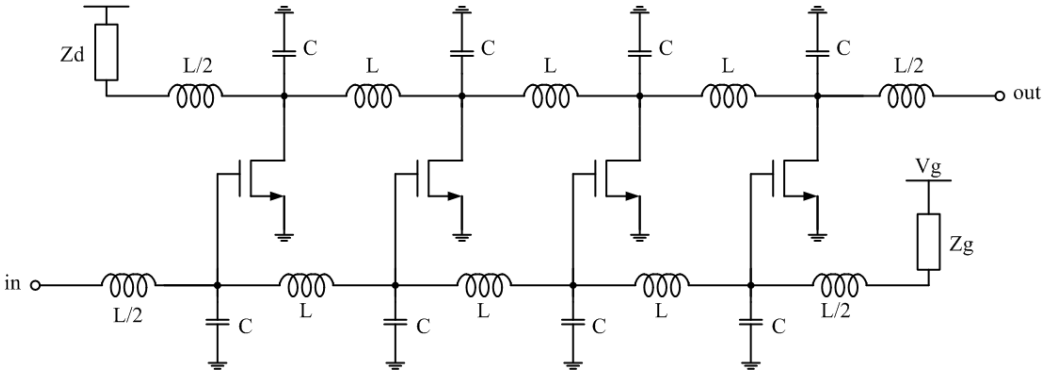

Figure 1.2: A distributed amplifier realized with artificial transmission lines

1.1 Thesis objectives

The global objective of this thesis is to investigate design techniques for the CMOS DA, and to use these techniques to demonstrate a fully integrated DA using a relatively old 0.35μm CMOS technology.

A theoretical study is required which adequately describes the behavior of a distributed amplifier. Therefore, the second objective is to develop analytical expressions, which allow the design and optimization of DAs, and prediction of their performance such as gain, bandwidth and noise figure.

One of the major drawbacks of the DA design in silicon based technologies is the lack of accurate active and passive device models which enable us to evaluate DA performance without much error. Thus, to present RF MOSFET and spiral inductor models which can be incorporated into DA design is another objective of this thesis.

Experimental results are necessary to show the principle of distributed amplification. The final objective of this thesis is therefore to fabricate the designed DA using 0.35μm CMOS process, and practically demonstrate its operating characteristic so that the predicted performance can be confirmed.

1.2 Overview of previous work

Some published reports of CMOS DAs are presented in Table 1.1 which will be discussed briefly in this section. In the table, bandwidth column (BW) refers to the range over which the gain is relatively constant within a certain margin.

The first integrated CMOS DA was presented by Sullivan et al. [3]. Instead of on-chip inductors they proposed to use low loss bond wires as inductors. Integrated in 0.8μm CMOS technology, the amplifier achieved 5 dB gain and 3 GHz bandwidth.

Ballweber et al. [4] realized a 4-stage CMOS DA using on-chip inductors in 0.6μm technology. This amplifier was designed with the help of a computer optimization routine and m-derived filter matching sections were employed before the line terminations. The amplifier presented 6.5dB gain from 0.5GHz to 4GHz.

Ahn et al. [5] designed a differential 4-stage CMOS DA to get rid of the effects of interconnect, bond wire and package parasitics on the performance of the amplifier. Implemented in 0.6μm technology, this amplifier achieved a higher bandwidth than

its single ended version [4], however the gain reduced to 5.5dB, the noise figure increased more than 3 dB, chip area and power consumption increased twofold.

Amaya et al. designed two single ended CMOS DAs [6, 7]. The first one was a 4 stage cascode design in 0.35μm technology and it showed 20dB gain up to 3.5 GHz. The second design was realized in 0.18μm CMOS process and it presented 6 dB gain and 25 GHz bandwidth. This amplifier was also a 4 stage cascode design and coplanar waveguides were used as transmission lines instead of spiral inductors.

Liu et al. also designed two single-ended 3-stage cascode CMOS DAs in 0.18μm technology [8, 9]. Both designs utilized m-derived matching sections and on-chip spiral inductors. The first one [8] achieved 10.6 dB gain and 14 GHz bandwidth whereas the second one [9] achieved 7.3 dB gain and 22 GHz bandwidth.

Zhang et al [10] presented a low power 3-stage cascode DA implemented in 0.18μm CMOS technology. The amplifier dissipates 9 mW and operates with 1.3V supply voltage. This amplifier provides 8 dB gain and 4.2-6.2dB noise figure over 40MHz-6.2 GHz band.

Ker et al [11] showed two Electrostatic Discharge (ESD) protection schemes applied to the DA design in 0.25μm CMOS technology. The amplifier without ESD achieved 5±1 dB gain over 1-11.4 GHz band while other amplifiers having different levels of ESD showed lower gain and bandwidth.

1.3 Organization of Thesis

Chapter 2 will deal with theory of distributed amplification. Background material for DA analysis will be provided first. Next, gain-bandwidth expression of an ideal DA will be calculated. Then, two different analysis of non-ideal DA will be presented. Also a detailed study of noise in DA will be given in Chapter 2.

The aim of Chapter 3 will be to provide an understanding of the high frequency behavior of a MOSFET. The RF-MOSFET model used in this work will be explained in detail and the noise model of MOSFET will be presented in this chapter.

In Chapter 4, a physical model for spiral inductors will be given and the results of the model will be compared with the measured inductor characteristics.

Chapter 5 will present the design procedure of CMOS DAs. Basic gain cell configurations are described and their performances are characterized theoretically. Two designed DAs will be explained in detail and their simulation results will be given.

Finally, Chapter 6 is a review of the thesis and the conclusions will be given in this chapter.

Table 1.1: Overview of the previous publications

Process	BW (GHz)	Gain (dB)	f_c (GHz)	NF (dB)	S11 (dB)	S22 (dB)	Power (mW)	Area (mm^2)	Gain Cell	Inductor	Ref
0.8µm	0.3-3	5±1.2	4.7	5.1	-6	-9	54	0.72x0.32	CS	Bondwire	[3]
0.6µm	0.5-4	6.5±1.2	5.5	6.8	-7	-10	83.4	0.79	CS	Spiral	[4]
0.6µm	1.5-7.5	5.5±1.5	8.5	8.7-13	-6	-9.5	216	1.3x2.2	Diff CS	Spiral	[5]
0.35µm	0.5-3.5	20±1.5	5.5	1.5-3	-15	-15	86.7	0.95x1.8	CC	Spiral	[6]
0.18µm	1-25	6±1	27	6	-10	-10	68.1	1.8-0.9	CC	CPW	[7]
0.18µm	0.5-14	10.6±0.9	18	3.4-5.4	-11	-12	52	1x1.6	CC	Spiral	[8]
0.18µm	0.6-22	7.3±0.8	24	4.3-6.1	-8	-9	52	0.9x1.5	CC	Spiral	[9]
0.18µm	0.04-6.2	8±0.6	7.8	4.2-6.2	-16	-9	9	0.8x1.45	CC	Spiral	[10]
0.25µm	1-11.4	5±1	16.7	4.4-5.6	-10	-15	-	-	CS	Spiral	[11]

CPW: Coplanar Waveguide

CS: Common-source, Diff: Differential, CC: Cascode

2. DISTRIBUTED AMPLIFICATION THEORY

2.1 Definition of image impedance

We begin with the definitions of the image impedances and voltage and current transfer functions for an arbitrary two port network; these results will be used in the analysis of the DAs in the following sections.

For maximum power transfer in cascaded two-ports, each two-port should be terminated by appropriate impedances. This condition can be met by terminating the two-ports with their image impedances so that the impedance is the same when one looks into either direction of each port, as shown in Figure 2.1.

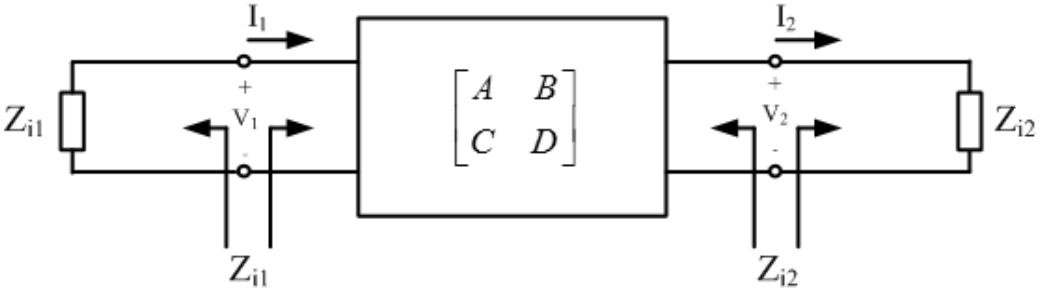

Figure 2.1: Definition of images impedances of two-port network

Image impedances for port 1 and port 2 are defined as [12],

Z_{i1}= input impedance at port 1 when port 2 is terminated by Z_{i2}

Z_{i2}= input impedance at port 2 when port 1 is terminated by Z_{i1}

Image impedances can be given in terms of ABCD parameters as [13],

$$Z_{i1} = \sqrt{\frac{AB}{CD}} \quad \textbf{(2.1)}$$

$$Z_{i2} = \sqrt{\frac{DB}{CA}} \quad \textbf{(2.2)}$$

If the network is symmetrical, then A=D and $Z_{i1}=Z_{i2}=Z_0$. Z_0 is known as the characteristic impedance of the two-port network. When terminated with its image

impedance, the voltage and current transfer functions can be expressed in terms of the two-port parameters as

$$\frac{V_2}{V_1} = \sqrt{\frac{D}{A}}\left(\sqrt{AD} - \sqrt{BC}\right) \tag{2.3}$$

and

$$\frac{I_2}{I_1} = \sqrt{\frac{A}{D}}\left(\sqrt{AD} - \sqrt{BC}\right) \tag{2.4}$$

The propagation factor, $\theta = \theta_r + j\theta_i$ is defined as

$$e^{-\theta} = \sqrt{\left(\frac{V_2}{V_1}\right)\left(\frac{I_2}{I_1}\right)} = \sqrt{AD} - \sqrt{BC} \tag{2.5}$$

The voltage and current transfer characteristics can be rewritten as

$$\frac{V_2}{V_1} = \sqrt{\frac{Z_{i2}}{Z_{i1}}}e^{-\theta} \tag{2.6}$$

and

$$\frac{I_2}{I_1} = \sqrt{\frac{Z_{i1}}{Z_{i2}}}e^{-\theta} \tag{2.7}$$

2.2 Basic filter sections

Figure 2.2 shows two elementary filter sections often used in DAs, known commonly as T-section (a) and π-section (b). These networks pass signals with frequencies below the cutoff frequency while attenuating signals with frequencies above the cutoff frequency. Therefore, they are called low-pass filter sections.

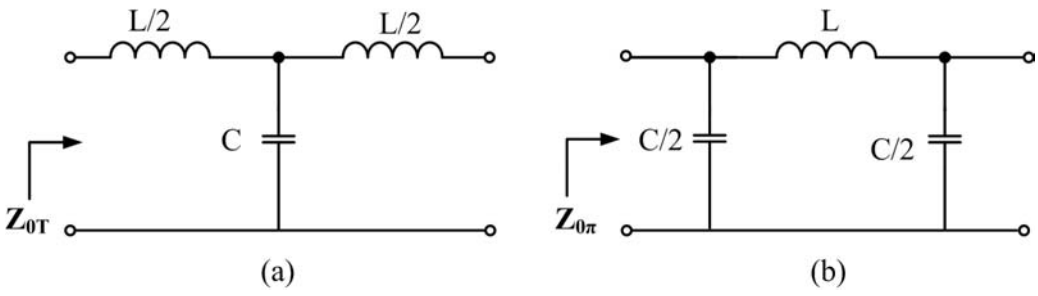

Figure 2.2: Low pass filter sections, (a) T-section, (b) π-section

The image impedances of T- and π-sections are referred to as Z_{0T} and $Z_{0\pi}$, respectively. Using (2.1) and (2.5) leads to

$$Z_{0T} = \sqrt{\frac{L}{C}\left(1-\frac{\omega^2 LC}{4}\right)} = \sqrt{\frac{L}{C}\left(1-\frac{\omega^2}{\omega_c^2}\right)} \tag{2.8}$$

$$Z_{0\pi} = \sqrt{\frac{L}{C}\left(1-\frac{\omega^2 LC}{4}\right)^{-1}} = \sqrt{\frac{L}{C}\left(1-\frac{\omega^2}{\omega_c^2}\right)^{-1}} \tag{2.9}$$

$$\theta = \cosh^{-1}\sqrt{1-\frac{\omega^2}{\omega_c^2}} = \frac{1}{2}\cosh^{-1}\left(1-\frac{2\omega^2}{\omega_c^2}\right) \tag{2.10}$$

where $\omega_c = 2/\sqrt{LC}$ is the cutoff frequency**.** At the cutoff frequency, the image impedances go from real to imaginary, as shown in Figure 2.3**.** Since $Z_{oT}Z_{o\pi} = R^2$, where R is real, the sections are known as constant-k sections.

From Figure 2.3, we see that the image impedance of a constant-k filter changes with frequency significantly. Since the image impedance can not be realized by a finite number of elements, in practice line terminations are realized by a resistor [12]. As a result, impedance mismatch will considerably worsen the performance. This problem can be solved by changing the constant-k sections into m-derived sections. Figure 2.4 shows a half section, which has a series arm with impedance equal to m times that of the prototype constant-k section, but has also the same image impedance Z_{0T}.

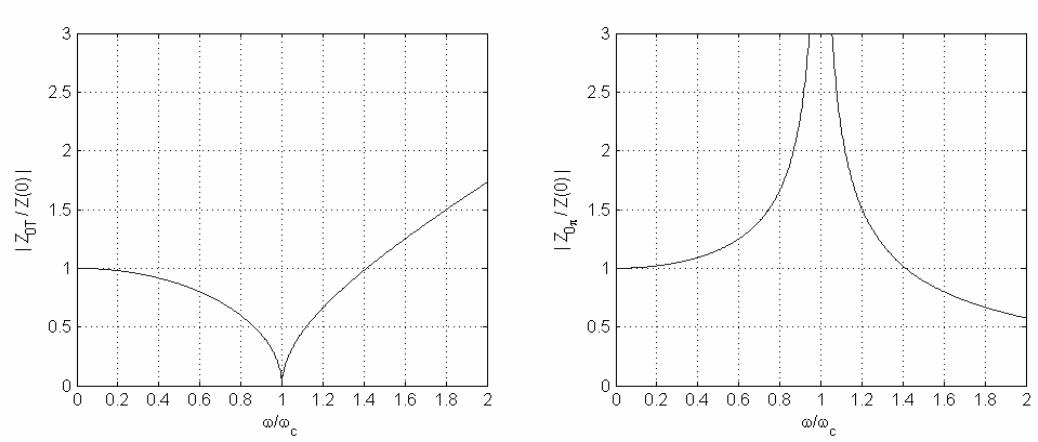

Figure 2.3: Frequency characteristics of low-pass filter sections, (a) T-section, (b) π-section normalized to $Z(0) = \sqrt{L/C}$

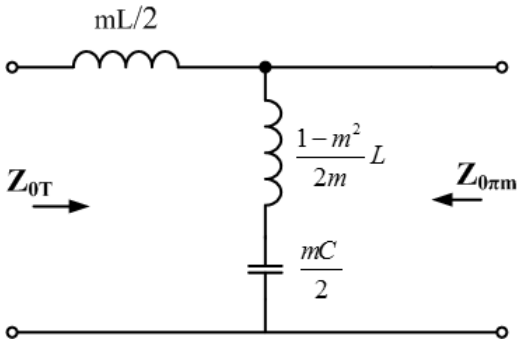

Figure 2.4: Low pass m-derived half section

The shunt arm is now made of an inductor and a capacitor in series, as shown. Accordingly its mid-shunt image impedance, given as $Z_{0\pi m}$ in Figure 2.4 is different from that of the constant-k prototype $Z_{0\pi}$.

$$Z_{0\pi m} = \sqrt{\frac{L}{C}} \frac{1-\omega^2/\omega_0^2}{\sqrt{1-\omega^2/\omega_c^2}} \qquad \textbf{(2.11)}$$

Here, $\omega_0 = \omega_c / \sqrt{1-m^2}$. Equations (2.9) and (2.11) are plotted in Figure 2.5 for m=0.6, where $Z_{0\pi m}$ presents more uniform impedance over the passband ($\omega/\omega_c < 1$) $Z_{0\pi}$ of the constant k prototype. Consequently, if an m-derived half section is employed as a buffer stage to match a resistive load to a constant-k filter, performance will be much better.

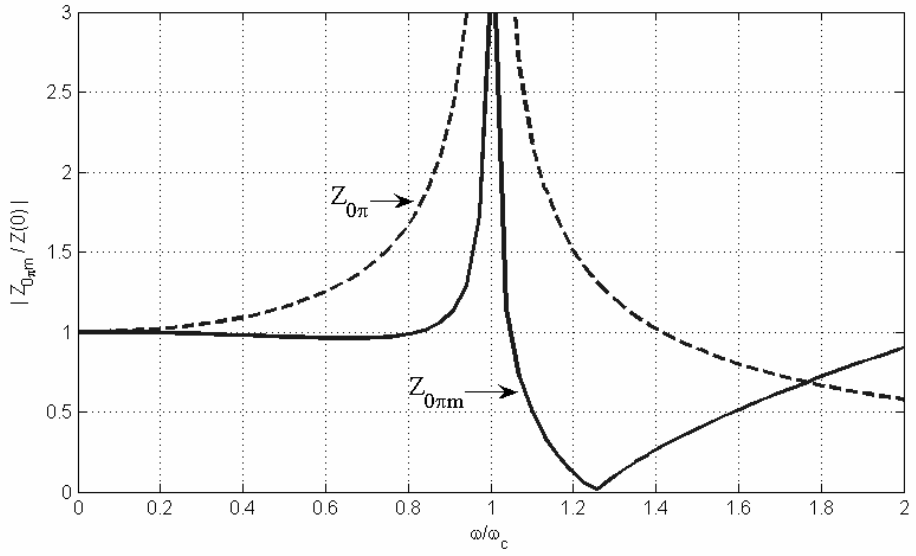

Figure 2.5: $Z_{0\pi m}$ of an m-derived half section shown as the solid curve and $Z_{0\pi}$ of a constant-k section shown as the dashed curve

2.3 Ideal Distributed Amplifier Analysis

In the following analysis, filter sections are assumed to be lossless and for the active devices the unilateral simplified small signal model of a common source (CS) MOSFET, shown in Figure 2.6, is used. In Figure 2.7, an N stage DA is shown for the general case. Each gate source capacitance and drain bulk capacitance is embedded symmetrically between L/2 inductors to form constant-k T-sections. Gate and drain artificial transmission lines are terminated by their image impedances so that no reflection occurs.

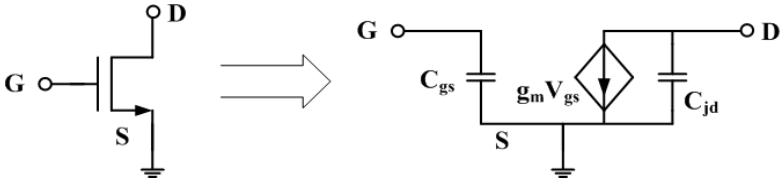

Figure 2.6: Simplified small signal model of CS MOSFET

Since the input capacitance C_{gs} is typically larger than the output capacitance C_{jd}, in order to keep the propagation constants and the characteristic impedances of the two lines equal additional capacitance (C_{add}) is connected in parallel with C_{jd}. Thus, the total capacitance at the drain of a transistor is $C_d = C_{jd} + C_{add}$.

When simplified model of Figure 2.6 is used in Figure 2.7, the resulting circuit schematic of the gate and drain lines are shown in Figure 2.8. Since the unilateral model is used, the two lines are coupled only through the device transconductance.

From (2.6) the voltage at the *kth* gate node of the input line can written as

$$V_{gk} = V_{in}\sqrt{\frac{Z_{0\pi}^{g}}{Z_{0T}^{g}}}e^{-\left(k-\frac{1}{2}\right)\theta_g} \qquad \textbf{(2.12)}$$

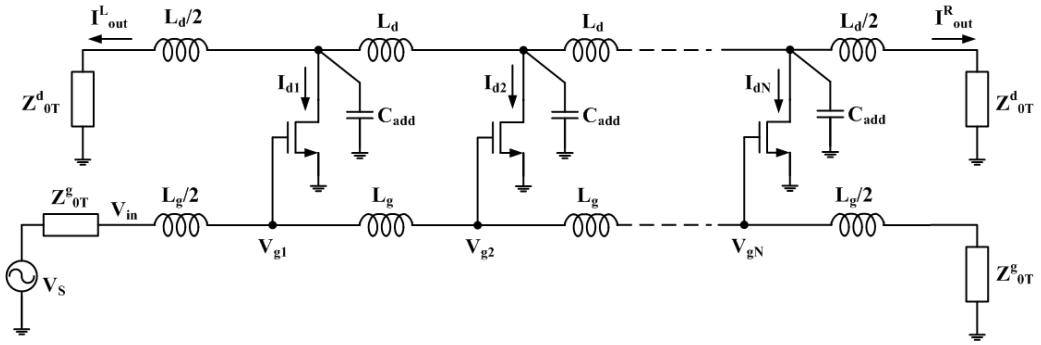

Figure 2.7: Schematic of N-stage DA

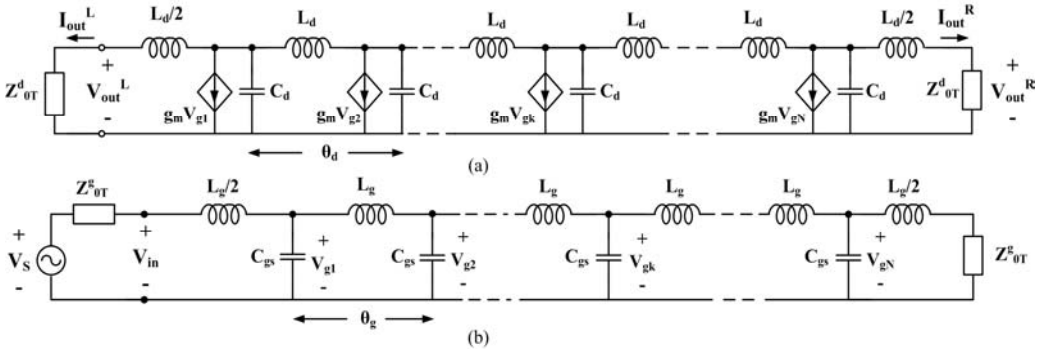

Figure 2.8: A DA with lossless sections and unilateral transistor model, (a) Drain line (b) Gate line

where θ_g is the propagation factor of the gate line and ½ term is due to the half section between the input and gate node of the first transistor.

This voltage produces a current of

$$I_{dk} = -g_m V_{gk} \tag{2.13}$$

at the *kth* drain node on the output line. Substituting (2.12) into (2.13), we get

$$I_{dk} = -g_m V_{in} \sqrt{\frac{Z_{0\pi}^{g}}{Z_{0T}^{g}}} e^{-\left(k-\frac{1}{2}\right)\theta_g} \tag{2.14}$$

Since each transistor sees equal impedances in both directions, only half of this current travels toward the right hand drain load. Then, using (2.7), the total current at the right hand drain load can be written as

$$\begin{aligned} I_{out}^{R} &= \frac{1}{2}\sqrt{\frac{Z_{0\pi}^{d}}{Z_{0T}^{d}}}\left(I_{d1} e^{-\left(N-\frac{1}{2}\right)\theta_d} + I_{d2} e^{-\left(N-\frac{3}{2}\right)\theta_d} + \ldots + I_{d(N-1)} e^{-\frac{3}{2}\theta_d} + I_{dN} e^{-\frac{1}{2}\theta_d} \right) \\ &= \sum_{k=1}^{N} \frac{1}{2} I_{dk} \sqrt{\frac{Z_{0\pi}^{d}}{Z_{0T}^{d}}} e^{-\left(N-k+\frac{1}{2}\right)\theta_d} \end{aligned} \tag{2.15}$$

where θ_d is the propagation factor of the output line and ½ term due to the half section between the output and drain node of the last transistor. Substituting (2.14) into (2.15) and rearranging the terms, we get

$$I_{out}^{R} = -\frac{1}{2} g_m V_{in} \sqrt{\frac{Z_{0\pi}^{g}}{Z_{0T}^{g}}} \sqrt{\frac{Z_{0\pi}^{d}}{Z_{0T}^{d}}} e^{-N\theta_d} e^{\frac{1}{2}(\theta_g - \theta_d)} \sum_{k=1}^{N} e^{k(\theta_g - \theta_d)} \tag{2.16}$$

For maximum gain-bandwidth, propagation constants of gate and drain line should be equal, $\theta_g = \theta_d = \theta$. Also using the (2.8) and (2.9) for characteristic impedances of gate and drain lines, the right hand drain load current becomes

$$I_{out}^{R} = -\frac{g_m V_{in}}{2\left(1-\omega^2/\omega_c^2\right)} e^{-N\theta} N \qquad \textbf{(2.17)}$$

And the right hand drain load voltage is calculated as

$$V_{out}^{R} = I_{out}^{R} Z_{0T}^{d} = -\frac{g_m V_{in} N}{2\sqrt{\left(1-\omega^2/\omega_c^2\right)}} \sqrt{\frac{L_d}{C_d}} e^{-N\theta} \qquad \textbf{(2.18)}$$

The forward voltage gain is defined as

$$A_{for} = \frac{V_{out}^{R}}{V_{in}} = -\frac{g_m N}{2\sqrt{\left(1-\omega^2/\omega_c^2\right)}} \sqrt{\frac{L_d}{C_d}} e^{-N\theta} \rightarrow \left|A_{for}\right| = \frac{g_m N Z_{0\pi}}{2} \qquad \textbf{(2.19)}$$

Thus, without any loss mechanism, the voltage gain of the DA can be increased infinitely by increasing the number of stages without any bandwidth reduction ($N \rightarrow \infty$, $A_F \rightarrow \infty$). However, the increased gain-bandwidth of the distributed amplifier results in larger time delay between its input and output. Another observation is that the gain exhibits a rapid increase as the frequency comes close to the cutoff frequency.

Usually, a distributed amplifier is specified by its power gain. Recalling that V_{in} is equal to $V_S/2$ for a matched line, the power available from the generator is

$$P_{in} = \frac{1}{2}\frac{\left|V_{in}\right|^2}{Z_{0T}^{g}} = \frac{V_S^2}{8Z_{0T}^{g}} \qquad \textbf{(2.20)}$$

and the power dissipated in the right-hand drain load Z_{0T}^{d} is

$$P_{out} = \frac{1}{2}\left|I_{out}^{R}\right|^2 Z_{0T}^{d} \qquad \textbf{(2.21)}$$

Substituting I_{out}^{R} from (2.17) into (2.21), we obtain

$$P_{out} = \frac{V_S^2 g_m^2 N^2}{32\left(1-\omega^2/\omega_c^2\right)^2} Z_{oT}^{d} \qquad \textbf{(2.22)}$$

So that forward available gain is given by the expression

$$G_{for} = \frac{P_{out}}{P_{in}} = \frac{g_m^2 N^2}{4\left(1-\omega^2/\omega_c^2\right)^2} Z_{oT}^d Z_{oT}^g = \frac{g_m^2 N^2 Z_{o\pi}^d Z_{o\pi}^g}{4} \tag{2.23}$$

On the other hand, waves propagating to the left leads to a current flow in the left hand drain termination. This current can be expressed as

$$I_{out}^L = \sum_{k=1}^{N} \frac{1}{2} I_{dk} \sqrt{\frac{Z_{0\pi}^d}{Z_{0T}^d}} e^{-\left(k-\frac{1}{2}\right)\theta_d} \tag{2.24}$$

Substituting (2.14) into (2.24), we get,

$$I_{out}^L = -\frac{1}{2} g_m V_{in} \sqrt{\frac{Z_{0\pi}^g}{Z_{0T}^g}} \sqrt{\frac{Z_{0\pi}^d}{Z_{0T}^d}} e^{\frac{1}{2}\left(\theta_g+\theta_d\right)} \sum_{k=1}^{N} e^{-k\left(\theta_g+\theta_d\right)} \tag{2.25}$$

For maximum gain, $\theta_g = \theta_d = \theta$

$$I_{out}^L = -\frac{g_m V_{in}}{2\left(1-\omega^2/\omega_c^2\right)} e^{\theta} \sum_{k=1}^{N} e^{-2k\theta} \tag{2.26a}$$

$$I_{out}^L = -\frac{g_m V_{in}}{2\left(1-\omega^2/\omega_c^2\right)} e^{-N\theta} \frac{\sinh(N\theta)}{\sinh(\theta)} \tag{2.26b}$$

The voltage at the left hand drain termination and the reverse voltage gain are readily calculated as,

$$V_{out}^L = I_{out}^L Z_{0T}^d = -\frac{g_m V_{in}}{2\sqrt{\left(1-\omega^2/\omega_c^2\right)}} \sqrt{\frac{L_d}{C_d}} e^{-N\theta} \frac{\sinh(N\theta)}{\sinh(\theta)} \tag{2.27}$$

$$A_{rev} = \frac{V_{out}^L}{V_{in}} = -\frac{g_m}{2\sqrt{\left(1-\omega^2/\omega_c^2\right)}} \sqrt{\frac{L_d}{C_d}} e^{-N\theta} \frac{\sinh(N\theta)}{\sinh(\theta)} \tag{2.28}$$

For lossless case θ is purely imaginary, $\theta = j\beta$, then the power dissipated in the left-hand drain load Z_{0T}^d is

$$P_{out} = \frac{1}{2}\left|I_{out}^L\right|^2 Z_{0T}^d = \frac{V_S^2 g_m^2}{32\left(1-\omega^2/\omega_c^2\right)^2} \left(\frac{\sin(N\beta)}{\sin(\beta)}\right)^2 Z_{0T}^d \tag{2.29}$$

Finally, the reverse power gain is

$$G_{rev} = \frac{P_{out}}{P_{in}} = \frac{g_m^2}{4\left(1-\omega^2/\omega_c^2\right)^2}\left(\frac{\sin(N\beta)}{\sin(\beta)}\right)^2 Z_{oT}^d Z_{oT}^g = \frac{g_m^2 Z_{o\pi}^d Z_{o\pi}^g}{4}\left(\frac{\sin(N\beta)}{\sin(\beta)}\right)^2 \quad \textbf{(2.30)}$$

Figure 2.9 shows the ratio of the reverse gain to the forward gain. It is clear that the reverse gain of a DA is high at low frequencies. However, as the frequency increases, the reverse gain starts to decrease and becomes negligible. Also, this ratio is inversely proportional to number of stages (N).

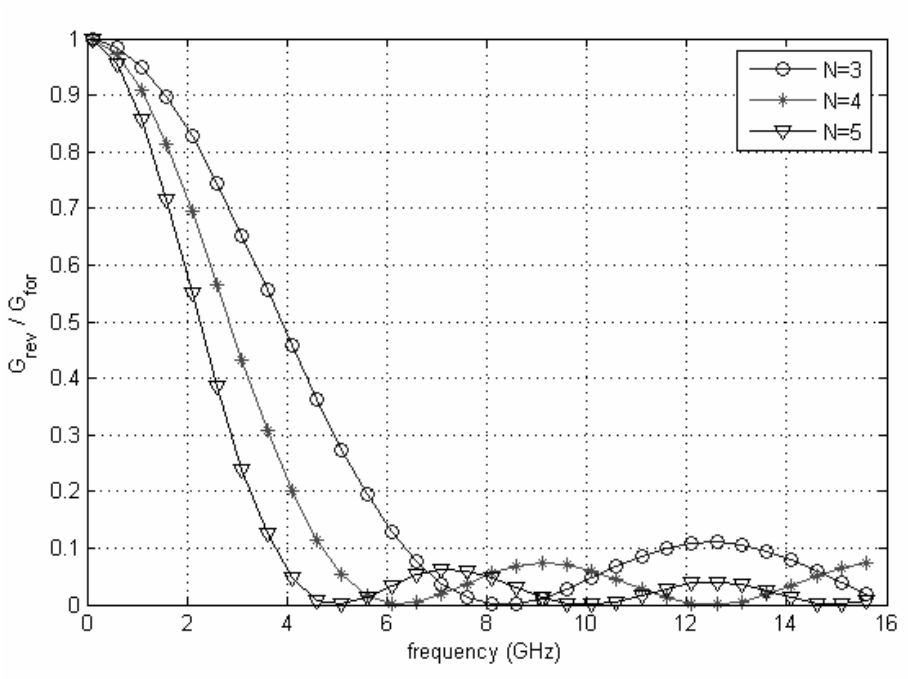

Figure 2.9: Normalised reverse gain to forward gain

2.4 Noise figure of DA

Generally, DAs have not been preferred in low-noise amplifier (LNA) applications because of their high power consumption and high noise figure. This is because in a DA design the aim is usually the highest gain-bandwidth product possible, which results in a non-optimal overall performance when used as an LNA. Furthermore, it is often considered that noise of the gate line termination resistor increases the noise figure of the DA considerably. However, the reverse power gain, given by (2.30), of the DA is small at the midband of the amplifier, so that the noise of the gate termination resistor is significantly isolated from the output. As a result, the noise figure (NF) is limited by a 3-dB noise floor only at very low and very high frequencies [10].

The noise performance of a system is expressed by its noise factor. The noise factor is a measure of the degradation in the signal-to-noise ratio as the signal passes through a system.

The noise factor is defined as

$$F = \frac{Total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source} \quad \textbf{(2.31)}$$

The noise figure (*NF*) is an equivalent representation in dB of the noise factor, that is,

$$NF = 10log(F) \quad \textbf{(2.32)}$$

Figure 2.10 shows the equivalent circuit of DA for noise analysis. From Figure 2.10, noise sources can be identified as

- Noise from the source impedance
- Noise from the gate line termination impedance
- Noise from the drain line termination impedance
- Noise of N MOSFETs

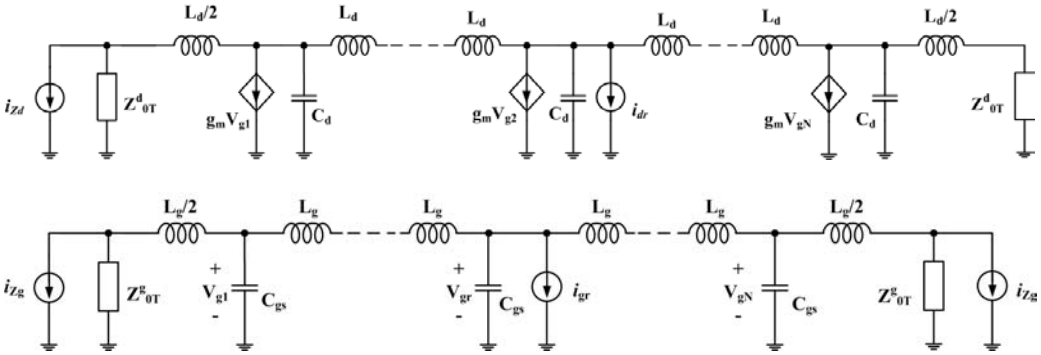

Figure 2.10: Small signal model for noise figure analysis

According to the noise-factor definition (2.31), we need to calculate individual noise powers dissipated in the load.

1) The noise power available from the source impedance, $Z_{0\pi}^{g}$, at the standard temperature is $kT_0\Delta f$, where k is Boltzmann's constant (~1.38x10^{-23} J/K), T_0 is 290K (Kelvin), and Δf is the noise bandwidth in hertz. The noise power dissipated in the output is $G_F kT_0\Delta f$, where G_F is defined by (2.23). Thus, noise power at the output due to source impedance is given by,

$$P_{n,Rs} = kT_0\Delta f \frac{g_m^2 N^2 Z_{o\pi}^{d} Z_{o\pi}^{g}}{4} \tag{2.33}$$

2) The noise power available from the gate termination $Z_{0\pi}^{g}$ is $kT_0\Delta f$. The noise power dissipated in the right-hand drain load is $G_R kT_0\Delta f$, where G_R is defined by (2.30). Thus, noise power at the output due to gate termination impedance is given by,

$$P_{n,Rg} = kT_0\Delta f \frac{g_m^2 Z_{o\pi}^{d} Z_{o\pi}^{g}}{4} \left(\frac{\sin(N\beta)}{\sin(\beta)} \right)^2 \tag{2.34}$$

3) The noise power available from the left-hand drain termination ($Z_{0\pi}^{d}$) is $kT_0\Delta f$. If the drain line is lossless, this noise power is exactly dissipated at the output.

$$P_{n,Rd} = kT_0\Delta f \tag{2.35}$$

4) To be able to find the noise associated with each of the N MOSFETs at the output, we need to find the noise power coming from an arbitrary stage first. Then, we can sum this power over N, since noise of MOSFET is uncorrelated with its neighbors [14].

Consider the gate noise i_{gr} of *rth* stage, where i_{gr} is used to represent the rms value $\sqrt{\overline{i_{gr}^2}}$. Assuming the line is matched at both ends, half of this current travels to the left direction and other half travels to the right direction. Thus, it is amplified by the following stages (i.e. (r+1)th, (r+2)th, …, Nth stages) by forward amplification and by the preceding stages (i.e. (r-1)th, (r-2)th, …,1st stages) by reverse amplification. Noise powers associated with these two paths should be calculated first, and then these powers should be summed together with the noise power coming from the drain noise current i_{dr}, by taking into account the correlation between i_{gr} and i_{dr}.

The current $I_{out}^{for}(r)$ through the output load due to forward amplification of i_{gr} is given by

$$I_{out}^{for}(r) = \frac{1}{2}\left\{I_r e^{-j(n-r+1)\beta_d} + I_{r+1} e^{-j(n-r)\beta_d} + \ldots + I_N e^{-j\beta_d}\right\} e^{j\beta_d/2} \quad \textbf{(2.36)}$$

where I_r, I_{r+1}, etc., are the noise currents at the drain taps of the rth, (r+ l)th, etc., stages, respectively.

$$I_r = \frac{1}{2} g_m i_{gr} Z_{0\pi}^{g} \quad \textbf{(2.37a)}$$

$$I_{r+1} = \frac{1}{2} g_m i_{gr} Z_{0\pi}^{g} e^{-j\beta_g} \quad \textbf{(2.37b)}$$

$$I_N = \frac{1}{2} g_m i_{gr} Z_{0\pi}^{g} e^{-j(N-r)\beta_g} \quad \textbf{(2.37c)}$$

Substituting (2.37) into (2.36), we get

$$I_{out}^{for}(r) = \frac{1}{4} g_m i_{gr} Z_{0\pi}^{g} \left\{ e^{-j(N-r+1)\beta_d} + e^{-j(N-r)\beta_d} e^{-j\beta_g} + \ldots + e^{-j\beta_d} e^{-j(N-r)\beta_g} \right\} e^{j\beta_d/2} \quad \textbf{(2.38)}$$

For maximum gain, phase velocities should be equal, $\beta_g = \beta_d = \beta$

$$I_{out}^{for}(r) = \frac{1}{4} g_m i_{gr} Z_{0\pi}^{g} (N-r+1) e^{-j(N-r+1)\beta} e^{j\beta/2} \quad \textbf{(2.39)}$$

The current $I_{out}^{rev}(r)$ through the output load as a result of reverse amplification of i_{gr} is given by

$$I_{out}^{rev}(r) = \frac{1}{2}\left\{I_{r-1} e^{-j(N-r+2)\beta_d} + I_{r-2} e^{-j(N-r+3)\beta_d} + \ldots + I_N e^{-jN\beta_d}\right\} e^{j\beta_d/2} \quad \textbf{(2.40)}$$

where I_{r-1}, I_{r-2}, etc., are the respective noise currents at the drain taps of the (r-1)th, (r-2)th, etc., stages, given as,

$$I_{r-1} = \frac{1}{2} g_m i_{gr} Z_{0\pi}^{g} e^{-j\beta_g} \quad \textbf{(2.41a)}$$

$$I_{r-2} = \frac{1}{2} g_m i_{gr} Z_{0\pi}^{g} e^{-j2\beta_g} \quad \textbf{(2.41b)}$$

$$I_{1} = \frac{1}{2} g_m i_{gr} Z_{0\pi}^{g} e^{-j(r-1)\beta_g} \quad \textbf{(2.41c)}$$

Substituting (2.41) into (2.40), we get

$$I_{out}^{rev}(r) = \frac{1}{4} g_m i_{gr} Z_{0\pi}^{g} e^{-j(N-r+1)\beta_d} \left\{ e^{-j(\beta_d+\beta_g)} + e^{-j2(\beta_d+\beta_g)} + \ldots + e^{-j(r-1)(\beta_d+\beta_g)} \right\} e^{j\beta_d/2} \quad \textbf{(2.42)}$$

For maximum gain, $\beta_g = \beta_d = \beta$; after some algebraic manipulations, we find

$$I_{out}^{rev}(r) = \frac{1}{4} g_m i_{gr} Z_{0\pi}^{g} e^{-j(N+1)\beta} \frac{\sin((r-1)\beta)}{\sin(\beta)} e^{j\beta/2} \quad \textbf{(2.43)}$$

The total current in the drain load due to the rth stage gate noise current $I_{out}(r)$ is obtained by combining forward and reverse amplification equations as two vectors to give

$$\left|I_{out}(r)\right|^2 = \left(\frac{1}{4} g_m i_{gr} Z_{0\pi}^{g}\right)^2 \left\{ (N-r+1)^2 + \left(\frac{\sin((r-1)\beta)}{\sin(\beta)}\right)^2 + \frac{2(N-r+1)\sin((r-1)\beta)\cos(r\beta)}{\sin(\beta)} \right\} \quad \textbf{(2.44)}$$

Since the drain noise current i_{dr} sees equal impedances in both directions, the current through the output load because of the rth stage drain noise current is given by $\frac{1}{2} i_{dr}$ .To combine this with $I_{out}(r)$, we have to take into account the partial correlation between i_{gr} and i_{dr}. However, for simplicity we first neglect the correlation, analysis considering the correlation will be given later in this section.

Since we neglect the correlation, the total power dissipated in the output load due to gate and drain noise currents is obtained by combining (2.43) with $(\frac{1}{2} i_{dr})^2$. As a result, the output noise power due to the rth stage is

$$P_{out}(r) = \left\{ \left(\frac{1}{4} g_m i_{gr} Z_{0\pi}^{g}\right)^2 f(r,\beta) + \left(\frac{1}{2} i_d\right)^2 \right\} Z_{0T}^{d} \quad \textbf{(2.45)}$$

where

$$f(r,\beta)=(N-r+1)^2+\left(\frac{\sin((r-1)\beta)}{\sin(\beta)}\right)^2+\frac{2(N-r+1)\sin((r-1)\beta)\cos(r\beta)}{\sin(\beta)} \tag{2.46}$$

Noise contribution from N MOSFETs can be obtained by summing (2.45) over N since noise from one transistor is uncorrelated with that from its neighbors. The summed noise power is given by the expression

$$P_{out}^{tot}=\left\{\left(\frac{1}{4}g_m i_{gr} Z_{0\pi}^{g}\right)^2\sum_{r=1}^{N}f(r,\beta)+\frac{1}{4}Ni_d^2\right\}Z_{0T}^{d} \tag{2.47}$$

Substituting drain and gate noise current equations of a MOSFET into (2.47) gives

$$\begin{aligned}P_{out}^{tot}&=\left\{\left(\frac{1}{4}g_m\sqrt{4kT_0\Delta f\delta g_g}\,Z_{0\pi}^{g}\right)^2\sum_{r=1}^{N}f(r,\beta)+\frac{1}{4}N4kT_0\Delta f\gamma g_{d0}\right\}Z_{0T}^{d}\\&=4kT_0\Delta f\left\{\left(\frac{1}{4}g_m Z_{0\pi}^{g}\right)^2\frac{\delta\omega^2C_{gs}^2}{5g_{d0}}\sum_{r=1}^{N}f(r,\beta)+\frac{1}{4}N\gamma g_{d0}\right\}Z_{0T}^{d}\end{aligned} \tag{2.48}$$

Now we have all the information to calculate the noise factor, using (2.33), (2.34), (2.35) and (2.48) in (2.31), we can express the noise factor as

$$\begin{aligned}F=&\frac{kT_0\Delta f\,\frac{g_m^2N^2Z_{o\pi}^{d}Z_{o\pi}^{g}}{4}+kT_0\Delta f\,\frac{g_m^2Z_{o\pi}^{d}Z_{o\pi}^{g}}{4}\left(\frac{\sin(N\beta)}{\sin(\beta)}\right)^2+kT_0\Delta f}{kT_0\Delta f\,\frac{g_m^2N^2Z_{o\pi}^{d}Z_{o\pi}^{g}}{4}}\\&+\frac{4kT_0\Delta f\left\{\left(\frac{1}{4}g_mZ_{0\pi}^{g}\right)^2\frac{\delta\omega^2C_{gs}^2}{5g_{d0}}\sum_{r=1}^{N}f(r,\beta)+\frac{1}{4}N\gamma g_{d0}\right\}Z_{0T}^{d}}{kT_0\Delta f\,\frac{g_m^2N^2Z_{o\pi}^{d}Z_{o\pi}^{g}}{4}}\end{aligned} \tag{2.49}$$

(2.49) can be expressed in a more readable way as

$$F=1+\left(\frac{\sin N\beta}{N\sin\beta}\right)^2+\frac{4}{N^2g_m^2Z_{0\pi}^{g}Z_{0\pi}^{d}}+\frac{\delta\omega^2C_{gs}^2Z_{0T}^{g}\sum_{r=1}^{N}f(r,\beta)}{N^25g_{d0}}+\frac{4\gamma g_{d0}Z_{0T}^{d}}{Ng_m^2Z_{0\pi}^{d}Z_{0\pi}^{g}} \tag{2.50}$$

We can further simplify (2.50) since

$$\sum_{r=1}^{N}f(r,\beta)\approx\sum_{r=1}^{N}(N-r+1)^2\approx N^3/3 \text{ (for large N)}$$

Finally noise factor equation for the simplified case becomes

$$F_{simp} = 1 + \left(\frac{\sin N\beta}{N \sin \beta} \right)^2 + \frac{4}{N^2 g_m^2 Z_{0\pi}^g Z_{0\pi}^d} + \frac{\delta \omega^2 C_{gs}^2 Z_{0T}^g N}{15 g_{d0}} + \frac{4\gamma g_{d0} Z_{0T}^d}{N g_m^2 Z_{0\pi}^d Z_{0\pi}^g} \quad \textbf{(2.51)}$$

In the foregoing analysis, correlation between the gate induced noise and drain thermal noise was neglected. The following analysis calculates the noise factor by taking the correlation into account. This can be accomplished by summing the noise currents of different sources at the output instead of summing the noise powers as we have done so far. Then we can include the correlation when we calculate the total output noise power [15].

For convenience, (2.39) and (2.43) are rewritten below

$$I_{out}^{for} = \frac{(N - r + 1)}{4} g_m i_{gr} Z_{0\pi}^g e^{-j\left(N - r + \frac{1}{2}\right)\beta} \quad \textbf{(2.52)}$$

$$I_{out}^{rev} = \frac{1}{4} g_m i_{gr} Z_{0\pi}^g \frac{\sin((r-1)\beta)}{\sin \beta} e^{-j\left(N + r - \frac{1}{2}\right)\beta} e^{j(r-1)\beta} \quad \textbf{(2.53)}$$

Then, the total output noise current due to the gate noise of rth stage MOSFET is

$$\begin{aligned} I_{out}^{gr} &= I_{out}^{for} + I_{out}^{rev} \\ &= \frac{1}{4} g_m i_{gr} Z_{0\pi}^g e^{-j\left(N + r - \frac{1}{2}\right)\beta} \left[(N - r + 1) e^{j(2r-1)\beta} + \frac{\sin((r-1)\beta)}{\sin \beta} e^{j(r-1)\beta} \right] \end{aligned} \quad \textbf{(2.54)}$$

To simplify the analysis, we group the real and imaginary terms in the parenthesis as

$$I_{out}^{gr} = \frac{1}{4} g_m i_{gr} Z_{0\pi}^g e^{-j\left(N + r - \frac{1}{2}\right)\beta} \left[A(r, \beta) + jB(r, \beta) \right] \quad \textbf{(2.55)}$$

where

$$A(r, \beta) = (N - r + 1)\cos((2r-1)\beta) + \frac{\sin((r-1)\beta)}{\sin \beta} \cos((r-1)\beta) \quad \textbf{(2.56)}$$

$$B(r, \beta) = (N - r + 1)\sin((2r-1)\beta) + \frac{\sin((r-1)\beta)}{\sin \beta} \sin((r-1)\beta) \quad \textbf{(2.57)}$$

The total noise current at the output due to the drain noise of the rth stage is

$$I_{out}^{dr} = \frac{1}{2} i_{dr} e^{-j\left(N - r + \frac{1}{2}\right)\beta} \quad \textbf{(2.58)}$$

Thus, the total output noise current due to the transistor of the rth stage is

$$I_{out}(r) = I_{out}^{gr} + I_{out}^{dr} = \frac{1}{4} g_m i_{gr} Z_{0\pi}^{g} e^{-j\left(N+r-\frac{1}{2}\right)\beta} \left[A(r,\beta) + jB(r,\beta)\right] + \frac{1}{2} i_{dr} e^{-j\left(N-r+\frac{1}{2}\right)\beta} \quad \textbf{(2.59)}$$

From which the absolute value is calculated to find the noise power as

$$\begin{aligned} \left|I_{out}(r)\right|^2 &= \left(\frac{1}{4} g_m i_{gr} Z_{0\pi}^{g}\right)^2 \left[A^2(r,\beta) + B^2(r,\beta)\right] + \frac{1}{4} i_{dr}^2 \\ &\quad + 2\,\mathrm{Re}\left\{\frac{1}{4} g_m i_{gr} Z_{0\pi}^{g} e^{-j\left(N+r-\frac{1}{2}\right)\beta} \left[A(r,\beta) + jB(r,\beta)\right] \frac{1}{2} i_{dr}^{*} e^{j\left(N-r+\frac{1}{2}\right)\beta}\right\} \end{aligned} \quad \textbf{(2.60)}$$

Since $i_{gr} i_{dr}^{*} = jc\sqrt{\left|i_d\right|^2 \left|i_g\right|^2}$, (2.60) can be rewritten as

$$\begin{aligned} \left|I_{out}(r)\right|^2 &= \left(\frac{1}{4} g_m i_{gr} Z_{0\pi}^{g}\right)^2 \left[A^2(r,\beta) + B^2(r,\beta)\right] + \frac{1}{4} i_{dr}^2 \\ &\quad + \frac{1}{4} g_m Z_{0\pi}^{g} c\sqrt{\left|i_d\right|^2 \left|i_g\right|^2} \left[A(r,\beta)\sin(2r-1)\beta - B(r,\beta)\cos(2r-1)\beta\right] \end{aligned} \quad \textbf{(2.61)}$$

The total output noise power density of all transistors is

$$\sum_{r=1}^{N} \left|I_{out}(r)\right|^2 Z_{0T}^{d} = \left\{ \begin{array}{l} \left(\frac{1}{4} g_m i_{gr} Z_{0\pi}^{g}\right)^2 \sum_{r=1}^{N} \left[A^2(r,\beta) + B^2(r,\beta)\right] + \frac{1}{4} N i_{dr}^2 + \\ \frac{1}{4} g_m Z_{0\pi}^{g} c\sqrt{\left|i_d\right|^2 \left|i_g\right|^2} \sum_{r=1}^{N} \left[A(r,\beta)\sin(2r-1)\beta - B(r,\beta)\cos(2r-1)\beta\right] \end{array} \right\} Z_{0T}^{d} \quad \textbf{(2.62)}$$

Again using the definition of noise factor, we get

$$\begin{aligned} F &= 1 + \left(\frac{\sin N\beta}{N \sin\beta}\right)^2 + \frac{4}{N^2 g_m^2 Z_{0\pi}^{g} Z_{0\pi}^{d}} + \frac{\delta\omega^2 C_{gs}^2 Z_{0T}^{g} \sum_{r=1}^{n} \left[A^2(r,\beta) + B^2(r,\beta)\right]}{N^2 5 g_{d0}} \\ &\quad + \frac{4\gamma g_{d0} Z_{0T}^{d}}{N g_m^2 Z_{0\pi}^{g} Z_{0\pi}^{d}} + \frac{4 Z_{0T}^{d} c\sqrt{\gamma\delta\omega^2 C_{gs}^2 / 5} \sum_{r=1}^{N} \left[A(r,\beta)\sin(2r-1)\beta - B(r,\beta)\cos(2r-1)\beta\right]}{N^2 g_m Z_{0\pi}^{d}} \end{aligned} \quad \textbf{(2.63)}$$

where

$$\begin{aligned} \sum_{r=1}^{N} \left[A^2(r,\beta) + B^2(r,\beta)\right] &= \frac{N^3}{3} + \frac{N\left(9 - \cos 4\beta - 8\cos 2\beta\right)}{3\left(3 + \cos 4\beta - 4\cos 2\beta\right)} \\ &\quad + \frac{\cos\left(2\beta(N+1)\right) - \cos\left(2\beta(N-1)\right)}{3 + \cos 4\beta - 4\cos 2\beta} \end{aligned} \quad \textbf{(2.64)}$$

$$\sum_{r=1}^{N} \left[A(r,\beta)\sin(2r-1)\beta - B(r,\beta)\cos(2r-1)\beta\right] = \frac{N\left(\cos\beta - \cos 3\beta\right) + \cos(2N+1)\beta - \cos(2N-1)\beta}{2\left(3\sin\beta - \sin 3\beta\right)} \quad \textbf{(2.65)}$$

In Figure 2.11, noise figure is plotted from (2.63) for different N values. We can see that there is an optimum for the number of stages (N) at a particular frequency.

Figure 2.12 compares the NF equations, (2.50), (2.51) and (2.63), namely the noise figure without correlation, simplified noise figure without correlation and noise figure with correlation, respectively. We see that the difference is so small that simplified NF equation of (2.51) can be used for all purposes.

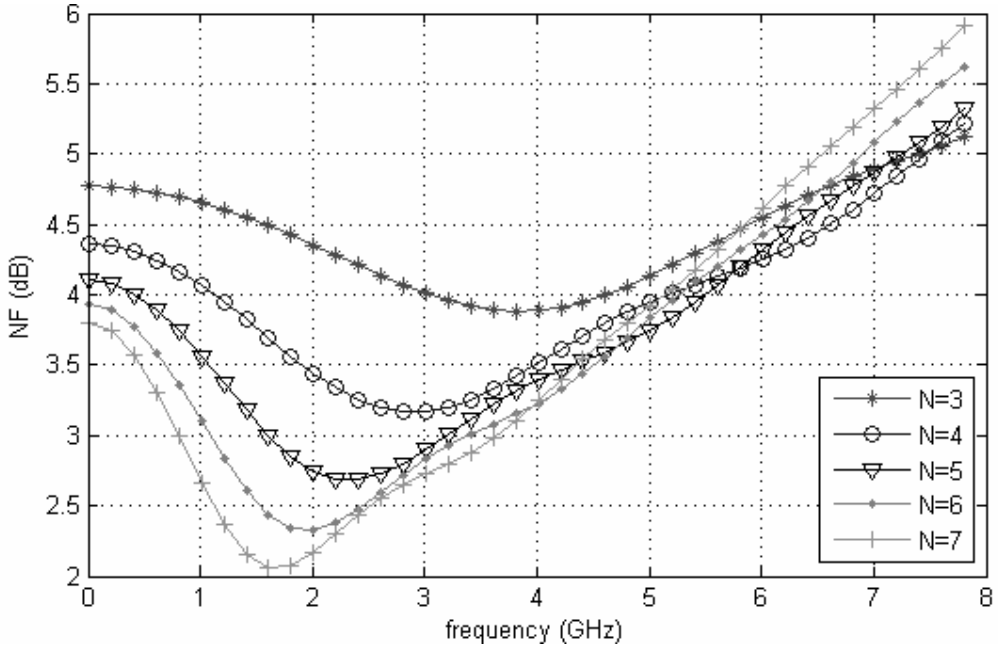

Figure 2.11: Noise figure vs. N (gm =40 mS, γ=4/3, δ=8/3, L_g=L_d=2nH, C_g=C_d=800fF)

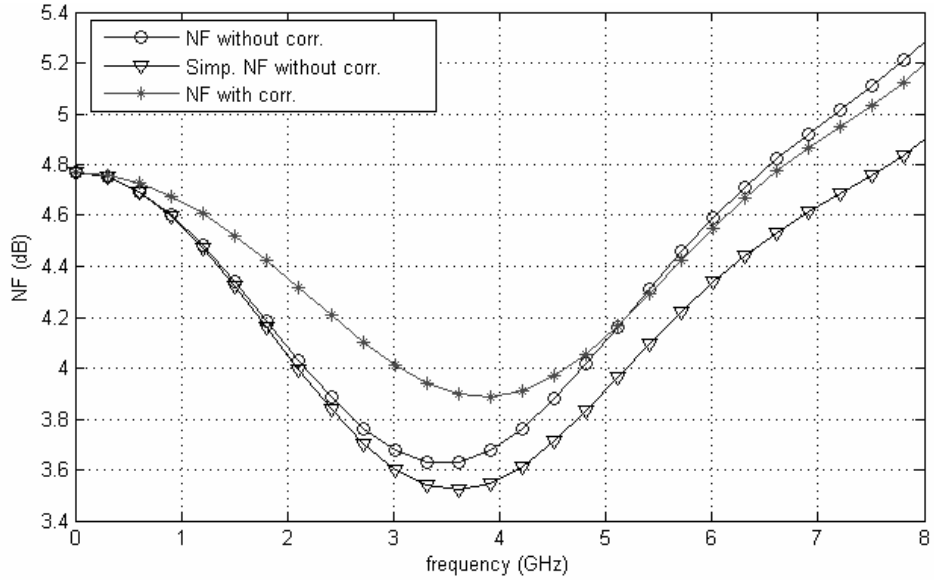

Figure 2.12: Noise figure with different formulas (N=3, gm =40 mS, γ=4/3, δ=8/3, L_g=L_d=2nH, C_g=C_d=800fF)

In (2.63) each term represents a different noise contributor, namely, the source impedance, gate termination impedance, drain termination impedance, gate noise current, drain noise current and correlation term. So the total noise factor is the sum of all the contributors

$$F_{total} = F_{n,Rs} + F_{n,Rg} + F_{n,Rd} + F_{n,ig} + F_{n,id} + F_{n,corr} \quad \textbf{(2.66)}$$

In Figure 2.13, each noise contributor and total noise factor is plotted versus frequency. In the low frequency region the noise term of the gate termination impedance is high, but this term vanishes as the frequency increases. This is because the reverse power gain is high in the low and high frequency regions, but it is small in the midband. For the middle frequency region the drain thermal noise current is dominant, however the gate noise current increases with frequency and at some point it exceeds the drain noise term and becomes the dominant term. Drain termination noise is constant over frequency but its effect on the noise factor is small. Finally, the correlation term is very small which explains the little difference between the NF curves shown in Figure 2.12 . Since the drain thermal noise is dominant in the passband, the noise factor can be estimated as [14]

$$F \approx F_{n,id} = 1 + \frac{4\gamma g_{d0} Z_{0T}^{d}}{N g_m^2 Z_{0\pi}^{d} Z_{0\pi}^{g}} \quad \textbf{(2.67)}$$

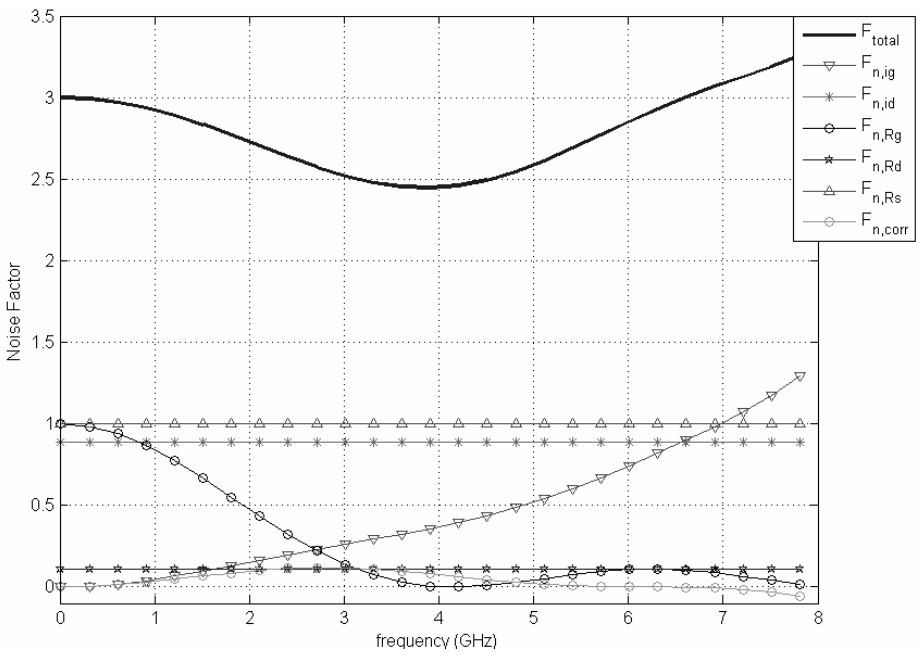

Figure 2.13: Noise factor contributors (gm =40 mS, gd0 = 40 mS, γ=4/3, δ=8/3, L_g=L_d=2nH, C_g=C_d=800fF)

2.5 DA analysis with gate and drain losses

The analysis presented in the previous section is crucial to become familiar with the operation of the DA. However, since the all of the loss mechanisms was neglected, resulting equations fail to evaluate the bandwidth of the amplifier. For this reason, we need to include the losses associated with the transistors in the analysis, as they are the primary loss sources in a typical design.

A simplified small signal model of a common source MOSFET is shown in Figure 2.14. R_g is the effective input resistance, C_{gs}, is the gate-to-source capacitance, g_m is the transconductance, g_{ds} and C_{jd} are the output conductance and capacitance, respectively.

By replacing the MOSFETs in Figure 2.7 with the equivalent circuit of Figure 2.14, we arrive at the equivalent circuits of the gate and drain transmission lines as shown in Figure 2.15.

With the help of (2.12), the voltage across C_{gs} of the k th transistor, V_{gk}, can be expressed in terms of the input voltage as

$$V_{gk} = V_{in}\sqrt{\frac{Z_{0\pi}^{g}}{Z_{0T}^{g}}}e^{-\left(k-\frac{1}{2}\right)\theta_g}\frac{1}{1+j\omega C_{gs}R_g} = V_{in}\sqrt{\frac{Z_{0\pi}^{g}}{Z_{0T}^{g}}}\frac{e^{-\left(k-\frac{1}{2}\right)\theta_g}e^{-j\phi_g}}{\sqrt{1+\omega^2/\omega_g^2}} \qquad \textbf{(2.68)}$$

where $\theta_g = A_g + j\Phi_g$ is the propagation factor, on the gate line. A_g and Φ_g are the attenuation and phase shift per section on the gate line. $\omega_g = 1/R_gC_{gs}$ is the gate radian cutoff frequency and $\phi_g = \tan^{-1}\left(\omega/\omega_g\right)$

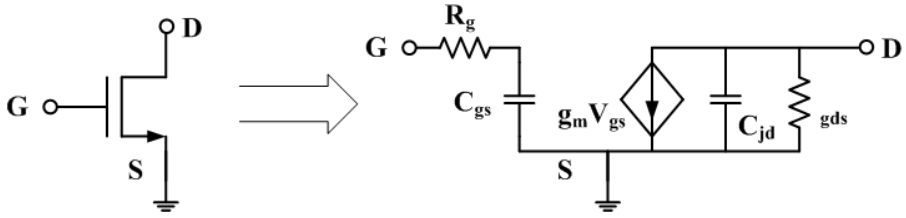

Figure 2.14: Simplified unilateral small signal model with input and output resistances

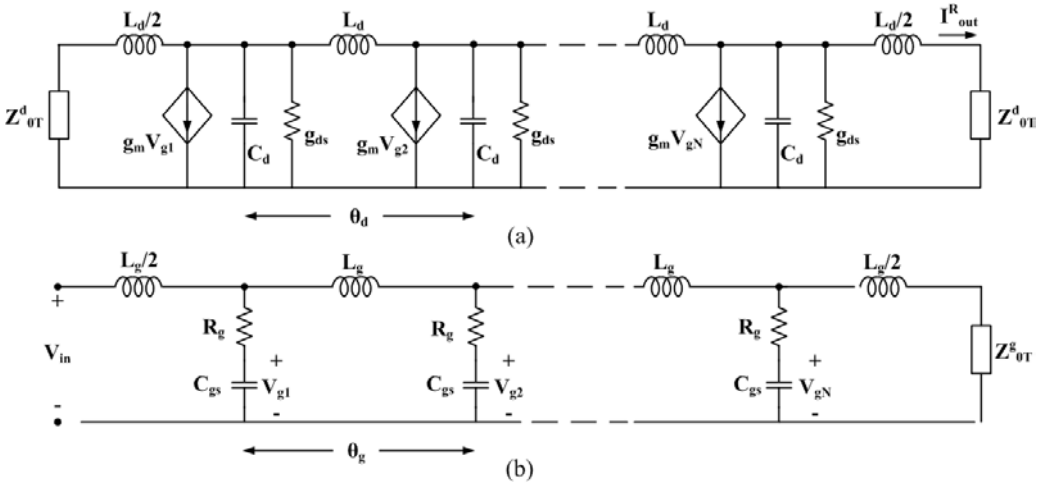

Figure 2.15: Small signal model of DA with input and output resistances of MOSFETs included, (a) Drain line (b) Gate line

From (2.16), the current delivered to the load is given by

$$I_{out}^{R} = -\frac{1}{2} g_m V_{in} \sqrt{\frac{Z_{0\pi}^{g}}{Z_{0T}^{g}}} \sqrt{\frac{Z_{0\pi}^{d}}{Z_{0T}^{d}}} \frac{e^{-N\theta_d} e^{-j\phi_g}}{\sqrt{1+\omega^2/\omega_g^2}} e^{\frac{1}{2}(\theta_g-\theta_d)} \sum_{k=1}^{N} e^{k(\theta_g-\theta_d)} \tag{2.69}$$

where N is the number of sections and $\theta_d = A_d + j\Phi_d$ is the propagation factor on the drain line. A_d and Φ_d are the attenuation and phase shift per section on the drain line. For maximum gain, the phase velocities of the two lines should be equal, $\Phi_g = \Phi_d = \Phi$. Thus, I_{out}^{R} can be expressed as

$$I_{out}^{R} = -\frac{1}{2} g_m V_{in} \frac{e^{-j(N\Phi_d+\phi_g)} e^{NA_d} e^{\frac{1}{2}(A_g-A_d)}}{(1-\omega^2/\omega_c^2)\sqrt{1+\omega^2/\omega_g^2}} \sum_{k=1}^{N} e^{k(A_g-A_d)} \tag{2.70}$$

After some algebraic manipulations, we have

$$I_{out}^{R} = -\frac{1}{2} g_m V_{in} \frac{\sinh\left(\frac{N}{2}(A_d-A_g)\right) e^{-j(N\Phi_d+\phi_g)} e^{-\frac{N}{2}(A_g+A_d)}}{\sinh\left(\frac{1}{2}(A_d-A_g)\right)(1-\omega^2/\omega_c^2)\sqrt{1+\omega^2/\omega_g^2}} \tag{2.71}$$

The output voltage is

$$V_{out}^{R} = I_{out}^{R} Z_{0T}^{d} \tag{2.72}$$

The forward voltage gain is defined as

$$\left|A_{for}\right| = \left|\frac{V_{out}^{R}}{V_{in}}\right| = \frac{g_m Z_{0T}^{d} \sinh\left(\frac{N}{2}\left(A_d - A_g\right)\right) e^{-\frac{N}{2}\left(A_g + A_d\right)}}{2\sinh\left(\frac{1}{2}\left(A_d - A_g\right)\right)\left(1 - \omega^2/\omega_c^2\right)\sqrt{1 + \omega^2/\omega_g^2}} \tag{2.73}$$

If we take the derivative of (2.73) with respect to N and equalize the result to zero, we find the N that maximizes the gain for a given frequency as [16]

$$N_{opt} = \frac{\ln\left(A_d/A_g\right)}{A_d - A_g} \tag{2.74}$$

Therefore, for a particular frequency, there is an optimum for the number of stages beyond which the gain of a distributed amplifier cannot be increased by adding new stages. This is because as the number of transistors is increased, the attenuation on the gate line also increases so the newly added devices receive less energy from the gate line. Moreover, the attenuation on the drain line also increases with number of transistors, so the new transistor attenuates the signal coming from previous stages. As a result, the new transistor not only produces less energy but also attenuates the output signal. Accordingly the gain of the amplifier starts to decrease with further addition of devices [16].

The power gain of the amplifier is calculated with the help of (2.20) and (2.22) as

$$G_{for} = \frac{P_{out}}{P_{in}} = \frac{g_m^2 Z_{0T}^{d} Z_{0T}^{g} \sinh^2\left(\frac{N}{2}\left(A_d - A_g\right)\right) e^{-N\left(A_g + A_d\right)}}{4\sinh^2\left(\frac{1}{2}\left(A_d - A_g\right)\right)\left(1 - \omega^2/\omega_c^2\right)\left(1 + \omega^2/\omega_g^2\right)} \tag{2.75}$$

It is important to investigate the effects of drain and gate line attenuation on the frequency response of the amplifier. When attenuation per section is small, the following expressions for attenuation on gate and drain lines are used [16]

$$A_g = \frac{\left(\omega_c/\omega_g\right)X_k^2}{\sqrt{1 - \left[1 - \left(\omega_c/\omega_g\right)^2\right]X_k^2}} \tag{2.76}$$

$$A_d = \frac{\omega_d/\omega_c}{\sqrt{1 - X_k^2}} \tag{2.77}$$

where X_k = ω/ω$_c$ is the normalized frequency, $\omega_g = 1/R_g C_{gs}$ is gate radian cutoff frequency and $\omega_d = 1/R_{ds} C_{jd}$ is drain cutoff frequency of the transistors.

The attenuation of the gate and the drain lines versus frequency are shown in Figure 2.16. Obviously, as the frequency increases, the gate line attenuation increases more rapidly than the drain line attenuation. Thus, the bandwidth of the amplifier is mainly determined by gate line attenuation. Also, the low frequency gain is controlled by A_d since in low frequency region A_g is zero whereas A_d is not.

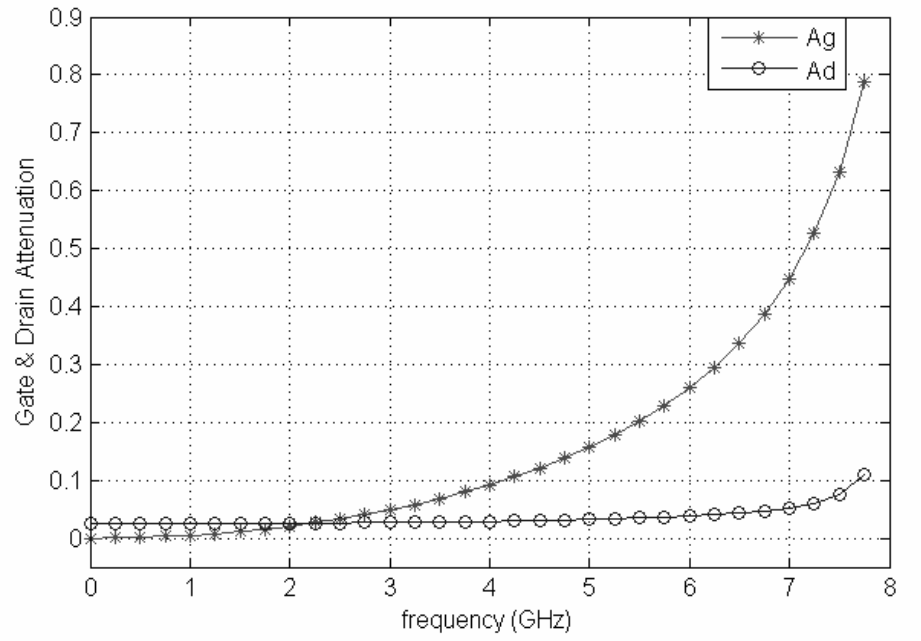

Figure 2.16: Gate and Drain line attenuations vs. frequency

In [16], an approximate expression for the maximum gain-bandwidth product was derived as

$$A_0 f_{1dB} \approx 0.8 f_{\max} \qquad \textbf{(2.78)}$$

where A_0 is the low frequency gain, f_{1dB} is the frequency where the gain A_0 drops by 1 dB and f_{max} is the maximum frequency of oscillation of the transistors.

2.6 Complete DA analysis

The analysis presented in the previous section considers the losses associated with the gate and drain of the transistors. Yet it is incapable of evaluating the performance of an integrated design. Therefore, for a more realistic analysis:

- Unilateral simplified device models should be changed with more accurate bilateral models
- Losses associated with other sources such as inductors should be considered since the high quality inductors are not available in CMOS technologies
- Image impedance match condition at the termination points of the lines should be removed, since the actual termination is realized with a resistor.

The following analysis [17] may be used to correct the deficiencies of the previous analysis. Figure 2.17a shows the elementary circuit of a DA. The transistor can be replaced by its two-port y-parameter representation as shown in Figure 2.17b.

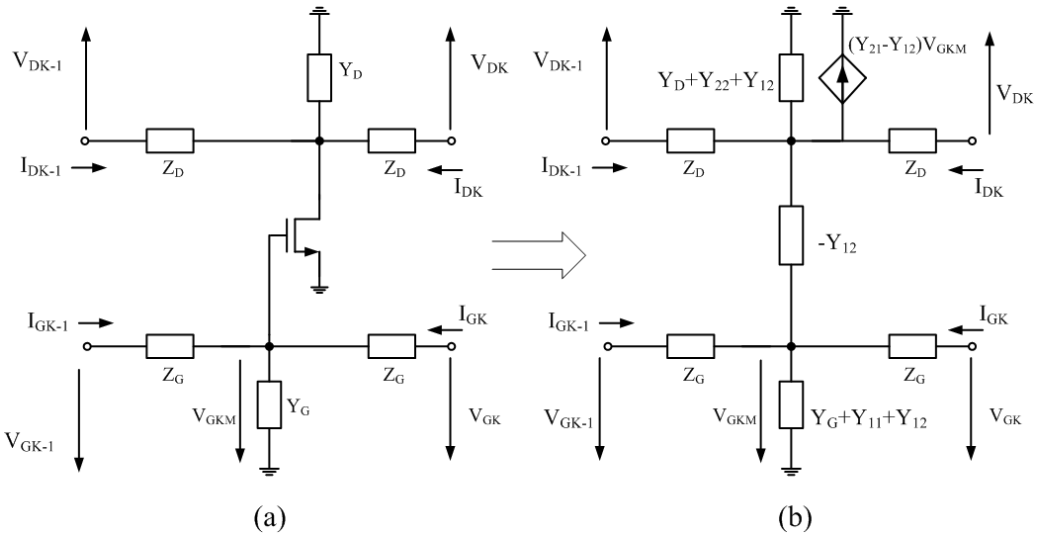

Figure 2.17: (a) Elementary circuit of DA, (b) transistor replaced with y-parameters

From Figure 2.17, the voltages and currents of the 4-port network can be determined with the matrix equation as,

$$\begin{bmatrix} V_{DK-1} \\ I_{DK-1} \\ V_{GK-1} \\ I_{GK-1} \end{bmatrix} = A \begin{bmatrix} V_{DK} \\ -I_{DK} \\ V_{GK} \\ -I_{GK} \end{bmatrix} \qquad \textbf{(2.79)}$$

Here the matrix [A] is defined as,

$$A = A_1 A_2 A_1 \tag{2.80}$$

where A_2 represents the transistor together with Y_G and Y_D admittances, and A_1 represents the Z_D and Z_G on either side of the transistor. Hence,

$$A_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ Y_D + Y_{22} & 1 & Y_{21} & 0 \\ 0 & 0 & 1 & 0 \\ Y_{12} & 0 & Y_G + Y_{11} & 1 \end{bmatrix} \tag{2.81}$$

$$A_1 = \begin{bmatrix} 1 & Z_D & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & Z_G \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{2.82}$$

Consider a 2-stage DA as shown in Figure 2.18 from which we can calculate the forward gain and input impedance of the N-section DA. Formulating the boundary conditions in accordance with the currents and voltages chosen in Figure 2.18, we obtain

$$V_{D0} + R_D I_{D0} = 0 \tag{2.83}$$

$$V_{G2} + R_G I_{G2} = 0 \tag{2.84}$$

$$V_{D2} + R_D I_{D2} = 0 \tag{2.85}$$

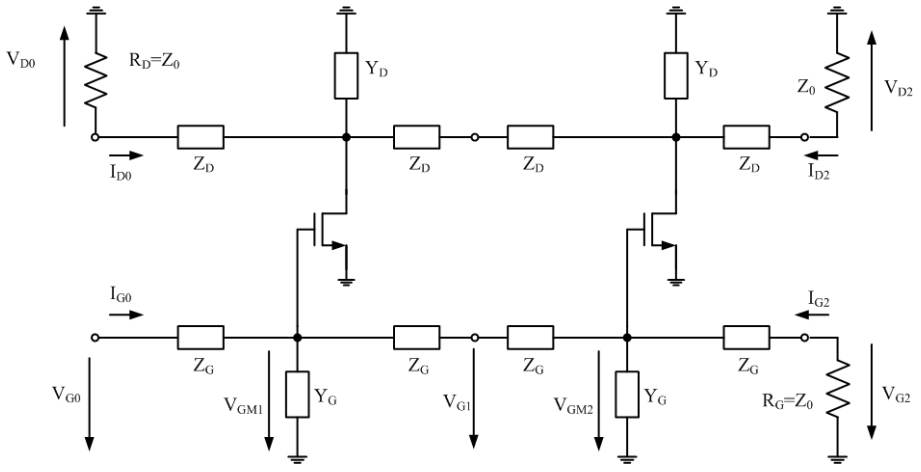

Figure 2.18: Circuit used for the calculation of forward gain and input impedance

Hence, cascading N stages and terminating the lines with R_G and R_D yield the matrix equation

$$\begin{bmatrix} V_{D0} \\ -V_{D0}/R_D \\ V_{G0} \\ I_{G0} \end{bmatrix} = X \begin{bmatrix} V_{Dn} \\ -V_{Dn}/R_D \\ V_{Gn} \\ V_{Gn}/R_G \end{bmatrix} \tag{2.86}$$

where for arbitrary sections,

$$X = \prod_{k=0}^{n} A_k \tag{2.87}$$

and for identical sections,

$$X = A^n \tag{2.88}$$

(2.86) can be simplified as,

$$\begin{bmatrix} V_{D0} \\ -V_{D0}/R_D \\ V_{G0} \\ I_{G0} \end{bmatrix} = X' \begin{bmatrix} V_{Dn} \\ V_{Gn} \end{bmatrix} \tag{2.89}$$

where

$$X' = \begin{bmatrix} A & B \\ C & D \\ E & F \\ G & H \end{bmatrix} = \begin{bmatrix} (X_{11} + X_{12}/R_D) & (X_{13} + X_{14}/R_G) \\ (X_{21} + X_{22}/R_D) & (X_{23} + X_{24}/R_G) \\ (X_{31} + X_{32}/R_D) & (X_{33} + X_{34}/R_G) \\ (X_{41} + X_{42}/R_D) & (X_{43} + X_{44}/R_G) \end{bmatrix} \tag{2.90}$$

From (2.89) the forward voltage gain can be determined as

$$A_{for} = \frac{V_{Dn}}{V_{G0}} = \frac{B + R_D D}{E(B + R_D D) - F(A + R_D C)} \tag{2.91}$$

and the input impedance is readily calculated as

$$Z_{in} = \frac{V_{G0}}{I_{G0}} = \frac{E(B + R_D D) - F(A + R_D C)}{G(B + R_D D) - H(A + R_D C)} \tag{2.92}$$

For calculation of reverse gain and output impedance, the circuit must be driven from the output port as shown in Figure 2.19.

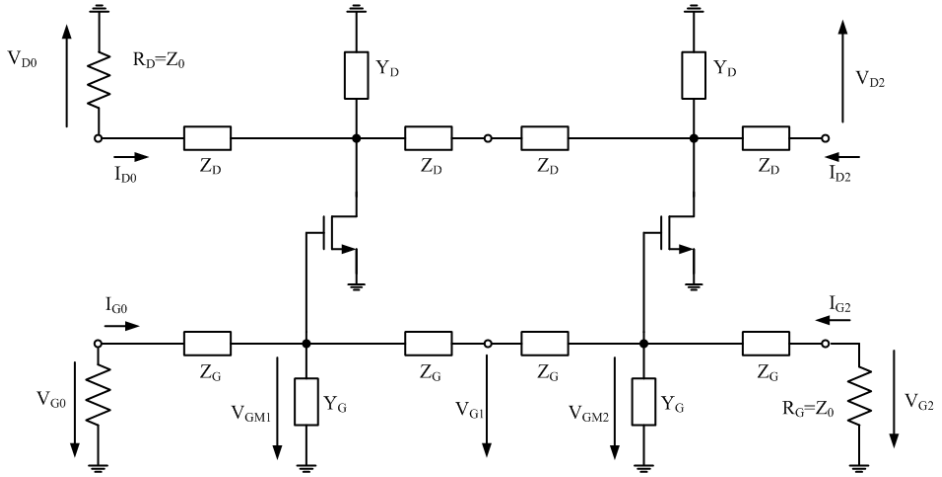

Figure 2.19: Circuit used for the calculation of reverse gain and output impedance

The analysis steps are the same as in the forward case except that A_2 of (2.80), should be changed as,

$$A_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ Y_G+Y_{11} & 1 & Y_{12} & 0 \\ 0 & 0 & 1 & 0 \\ Y_{21} & 0 & Y_D+Y_{22} & 1 \end{bmatrix} \tag{2.93}$$

Thus, the reverse voltage gain and output impedance equations are the same as (2.91) and (2.92). However, note that since A_2 is different, the result will not be same.

$$A_{rev} = \frac{V_{G0}}{V_{Dn}} = \frac{B + R_D D}{E(B + R_D D) - F(A + R_D C)} \tag{2.94}$$

$$Z_{out} = \frac{V_{Dn}}{I_{Dn}} = \frac{E(B + R_D D) - F(A + R_D C)}{G(B + R_D D) - H(A + R_D C)} \tag{2.95}$$

Although, the analysis presented in this section does not give us closed form expressions like the previous analysis. It has several advantages such as:

- Since the transistors are represented by y-parameters, all of the parasitics can be included in the analysis.
- Also the inductor losses can be incorporated into Z_G, Z_D, Y_G and Y_D. Chapter 4 presents a spiral inductor model which can be used for this purpose.
- Finally, since the terminations are realized with resistors, the effect of non-ideal termination of lines can be seen.

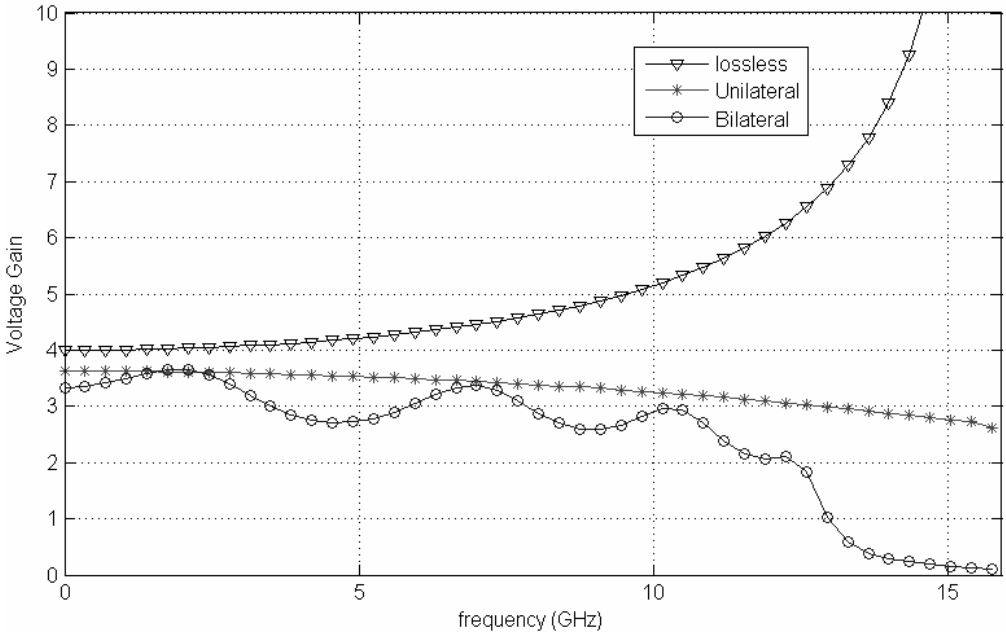

Figure 2.20: Comparison of gain equations (Cg=Cd=400fF, Cgd =50 fF, Lg = Ld =1nH, gm =40mS, Rg =8 Ω, Rds=500 Ω)

Gain equations (2.19), (2.73) and (2.91) are compared in Figure 2.20. It is obvious that the analysis presented in this section is valuable and mandatory

Once the forward and reverse gain, input and output impedance are calculated, they can be transformed into S-parameters [18]. For the setup shown in Figure 2.21a, S_{11} and S_{21} can be expressed as,

$$S_{11} = \frac{Z_1 - Z_{O1}}{Z_1 + Z_{O1}} \tag{2.96}$$

$$S_{21} = \frac{2\sqrt{Z_{O1}}}{\sqrt{Z_{O2}}} \frac{V_2}{V_{S1}} \tag{2.97}$$

If the excitation is placed at port 2 and port 1 is terminated in its normalizing impedance Z_{O1} as shown in Figure 2.21b, then

$$S_{22} = \frac{Z_2 - Z_{O2}}{Z_2 + Z_{O2}} \tag{2.98}$$

$$S_{12} = \frac{2\sqrt{Z_{O2}}}{\sqrt{Z_{O1}}} \frac{V_1}{V_{S2}} \tag{2.99}$$

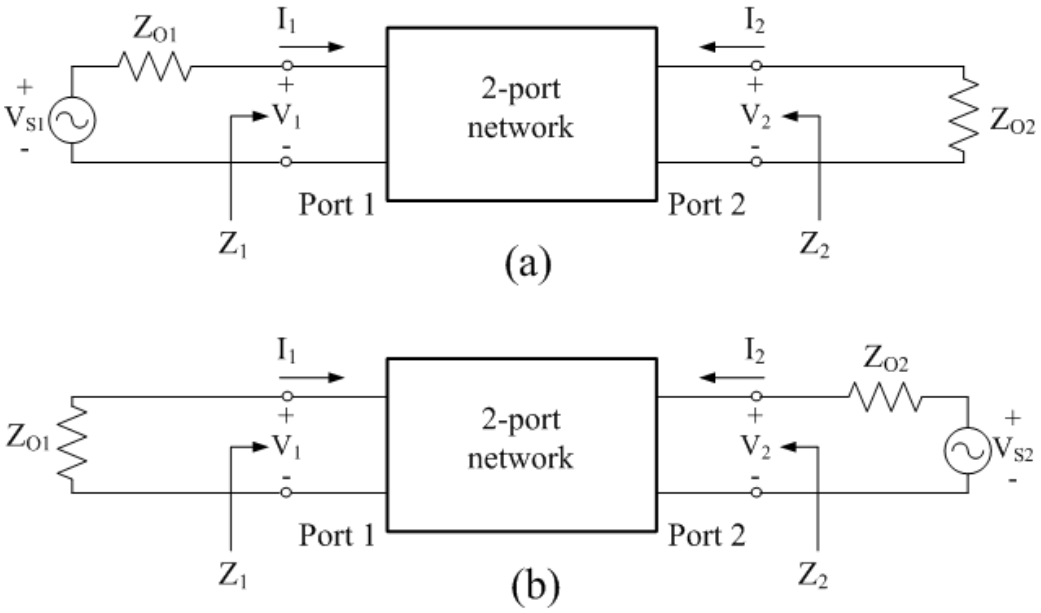

Figure 2.21: (a) Calculation of S_{11} and S_{21}, (b) Calculation of S_{22} and S_{12}

3. RF MOSFET MODELING

BSIM3 (3rd version of Berkeley Short-channel IGFET Model) is the industry standard for CMOS transistor modeling. BSIM3 models DC input-output curves and intrinsic capacitances accurately up to several hundred MHz. However, above 1-GHz the extrinsic components become as important as the intrinsic components. Therefore, an RF model that models the device behavior up to 10-GHz is necessary for the DA design.

The MOSFET model used in this work is based on the BSIM3v3, which is the third version of the third-generation BSIM. However, the model does not include several extrinsic components which affect the high frequency device behavior seriously. One of these components is the gate resistance R_G, which significantly changes the input admittance at RF. As explained in section 2.5, the gate line attenuation of a DA is mainly due to the gate resistance and it determines the amplifier performance at high frequencies. Also, the thermal noise generated by the gate resistance degrades the noise figure. Consequently, the gate resistance should be included in the model in order to evaluate the bandwidth and the noise figure of the DA correctly.

Another important extrinsic component that BSIM3v3 does not model is the substrate resistance. Depending on its value the substrate resistance may lower the output resistance considerably. Thus, the substrate resistance should also be modeled.

BSIM3v3 models the drain and the source intrinsic resistances. However, these resistances are embedded in the model and they only used to calculate the DC voltage drop across them. So they must be modeled outside the BSIM3v3 model to make them visible in AC simulation [19].

3.1 Equivalent Circuit Representation of MOS Transistor

In Figure 3.1, cross section of an NMOS is shown together with its parasitic elements which are gate resistance R_g, source series resistance R_s, drain series resistance R_d, gate-source overlap capacitance C_{gso}, gate-drain overlap capacitance C_{gdo}, gate-bulk

overlap capacitance C_{gbo}, source-bulk junction diode D_{sb}, drain-bulk junction diode D_{db}, and substrate resistances R_{sb}, R_{db}, and R_{dsb}. These elements are referred as the extrinsic part of MOSFET. The remaining part of the transistor without parasitics is called the intrinsic part.

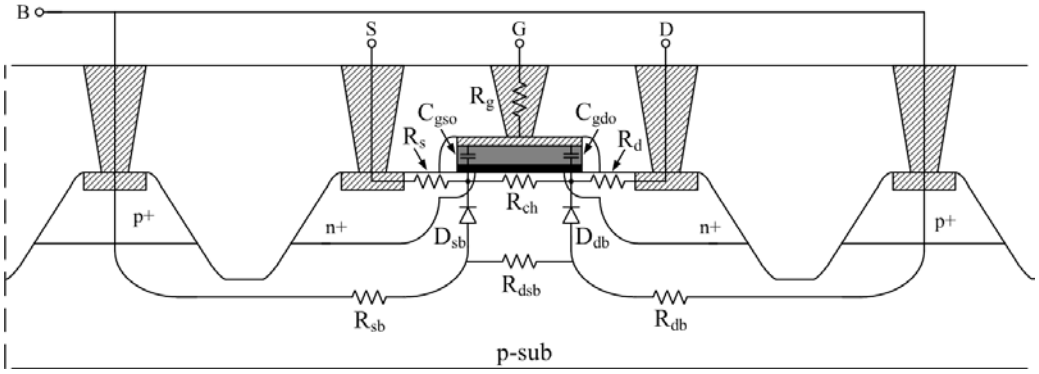

Figure 3.1: Cross section of a MOSFET with parasitics

Figure 3.2 shows the compact model used to model the transistor at RF. The intrinsic transistor is represented by NMOS, which is modeled by BSIM3v3, and the extrinsic elements are added so as to increase the accuracy at RF. The overlap capacitances are included in the core BSIM3v3 model so they are not added to the compact model. Also if a transistor with large number of fingers is used in the design, R_{dsb} can be neglected since it becomes very small compared to R_{sb} and R_{db} [19]. So it is not included in the compact model. The intrinsic source and drain resistances are pulled out of the intrinsic model and added outside of the intrinsic model to make them visible in the AC analysis. Also drain and source diodes are added outside of the intrinsic model since substrate resistances are in series with them.

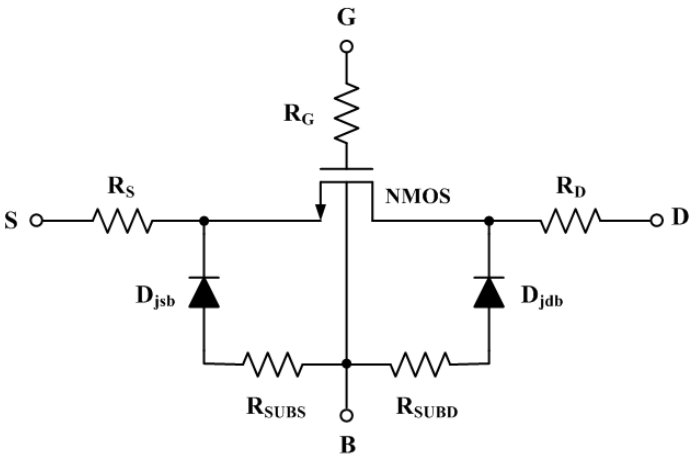

Figure 3.2: RF MOSFET model used in the design

Finally, the gate resistance is modeled as a single resistor in series with the gate of intrinsic device.

With added parasitic components at the gate, at the source, at the drain, and at the substrate, this model can reasonably well predict the high frequency AC small-signal characteristics of short-channel (<0.5μm) devices up to 10 GHz.

3.1.1 High-frequency modeling of gate resistance

Figure 3.3 shows a simple cross section of a MOSFET where the polysilicon gate resistance and the channel resistance are distributed along the channel. The effective gate resistance R_G seen looking into the gate is composed of two parts:

$$R_G = R_{G,poly} + R_{G,nqs} \tag{3.1}$$

where $R_{G,poly}$ is the distributed gate electrode resistance due to the polysilicon gate material and $R_{G,nqs}$ is the Non-quasi-static (NQS) distributed channel resistance seen from the gate [20]. The polysilicon gate resistance is expressed as

$$R_{G,poly} = \frac{R_{Gsh}}{N_f L_f}\left(W_{ext} + \frac{W_f}{\alpha}\right) \tag{3.2}$$

where R_{Gsh} (typically ~8Ω/□) is the gate polysilicon sheet resistance, W_f is the channel width per finger, L_f is the channel length, N_f is the number of fingers, and W_{ext} is the extension of the polysilicon gate over the active region. α is 3 if gate fingers are connected only at one end or α is 12 if gate fingers are connected at both ends. So this resistance can be made negligible by employing transistors with large number of fingers and connecting the gates at both ends.

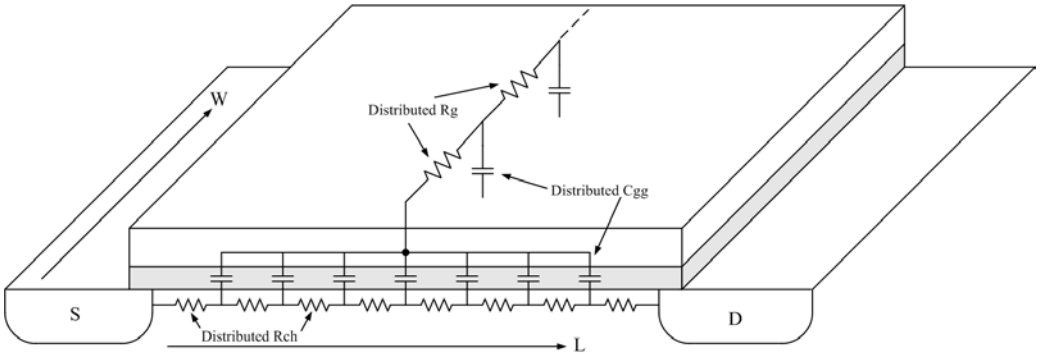

Figure 3.3: Determination of gate resistance

NQS effect occurs when channel charge can not respond to the signal applied to the gate immediately. This effect can be modeled by distributing the channel resistance This distributed resistance in the channel or NQS effect will cause an increase in the effective gate resistance.

Efficient and accurate modeling of the NQS effect in MOSFETs is very challenging. However, the following simple expression can be used to obtain the $R_{G,nqs}$ approximately in the strong inversion regime [20]:

$$R_{G,nqs} \cong \frac{\beta}{G_m} \tag{3.3}$$

where G_m is the transconductance of the device and β is a fitting parameter with a typical value around 0.2.

3.1.2 High frequency behavior and modeling of substrate resistance

The substrate resistance mainly affects the output admittance of a MOSFET at RF. Figure 3.4 shows a CS MOSFET small signal model. For the sake of simplicity, the gate resistance R_g can be neglected as long as $\omega R_g C_{gd} << 1$. Then, R_{out} and C_{out} can be expressed as

$$\frac{1}{R_{out}} = \frac{1}{R_o} + \frac{\omega^2 C_{jd}^2 R_{subd}}{1 + \omega^2 C_{jd}^2 R_{subd}^2} \tag{3.4}$$

$$C_{out} = C_{gd} + \frac{C_{jd}}{1 + \omega^2 C_{jd}^2 R_{subd}^2} \tag{3.5}$$

At low frequencies, $R_{out} \approx R_o$ and $C_{out} = C_{jd} + C_{gd}$

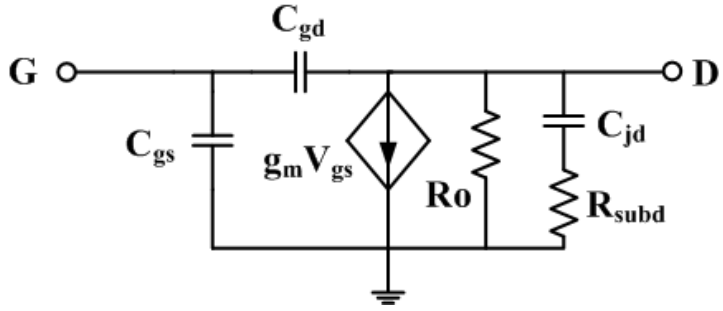

Figure 3.4: Small signal model for the calculation of output resistance with R_{subd}

As the frequency increases,

$R_{out} \rightarrow R_o \parallel R_{subd}$ and $C_{out} \rightarrow C_{gd}$

As a result, R_{out} lowers from R_o to $R_o \parallel R_{subd}$ and C_{out} from (C_{jd}+C_{gd}) to C_{gd}.

The reduction of output resistance leads to the reduction of device power gain in other words f_{max} of transistor. Also as the output resistance becomes comparable with the drain line characteristic impedance, output matching and gain of DA significantly degrade.

It is necessary to examine the effect of R_{subd} on R_{out} and C_{out}. Figure 3.5 shows the change of R_{out} and C_{out} versus frequency as function of R_{subd}. The decrease of R_{out} is less serious for small and large R_{subd} values. However, if R_{subd} is comparable to R_{out}, then the worst situation occurs. Since in a typical layout substrate contacts are placed close to the transistor so as to reduce the substrate coupling and substrate noise, R_{subd} can not be larger than R_{out}. Thus, it is better to minimize R_{subd}. This can be achieved by placing substrate contacts as close to the transistor as the layout rules allow [21].

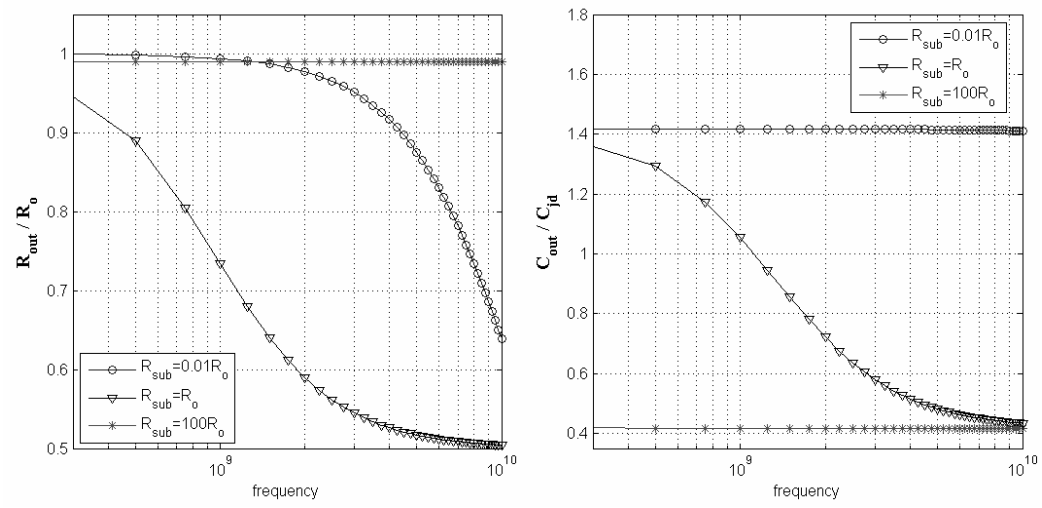

Figure 3.5: Effect of substrate resistance on the output resistance and output capacitance

Analytic calculation of R_{sub} is difficult since in a typical layout there are multiple substrate contacts surrounding the transistor, which causes three dimensional substrate current flow. However, analytical expressions for a specific substrate contact placement can be found in [19].

3.2 Noise Sources in a MOSFET

In MOSFETs, the most important noise sources are thermal noise and flicker noise. Thermal noise of the channel is the dominant of all thermal noise sources and is important for all the frequencies due to its white spectral density characteristics. Although flicker noise is often considered as a low frequency noise source, the effect of flicker noise is important in frequency converting RF circuits such as mixers and oscillators. Induced gate noise is due to the capacitive coupling of the channel thermal noise, and therefore it is mostly observed in high frequencies.

3.2.1 Thermal Noise Modeling

The channel thermal noise comes from the random thermal movements of the carriers in the channel of the device. The channel thermal noise model based on the output conductance was first proposed by van der Ziel [22]. As shown in Figure 3.6, an equivalent drain thermal noise current $\overline{i_d^2}$, in parallel with the channel, is used to represent the total channel thermal noise. The power spectral density of drain thermal noise is

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f \qquad \textbf{(3.6)}$$

where g_{d0} is the drain-source conductance at zero V_{DS}, and γ is a bias-dependent factor, which is equal to unity in the linear region and to 2/3 in the saturation region for long-channel devices.

It has been found that the γ -factor is not a constant for devices with different channel lengths and the γ -factor for short-channel device can be larger than that for long-channel device in the saturation regime owing to both velocity saturation and hot electrons [23].

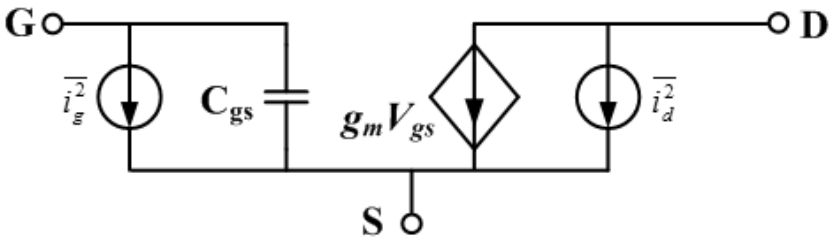

Figure 3.6: MOSFET small signal model with drain and gate noise currents

3.2.2 Induced Gate Noise Modeling

At high frequencies, the channel voltage fluctuations due to thermal noise couple to the gate through the oxide capacitance, leading to a noisy gate current flow. This noise current can be modeled by a noisy current source connected in parallel to the intrinsic gate-to-source capacitance C_{gs} as shown in Figure 3.6. Although this noise is negligible at low frequencies, it can be dominant at radio frequencies. According to van der Ziel, the power spectral density of the induced gate noise power spectral density (PSD) is given by

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{3.7}$$

where the parameter g_g is

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}.$$

and δ is the noise parameter for the induced gate noise with a theoretical value of 4/3 for long channel devices.

Since the physical origin of the induced gate noise is the same as that for the channel thermal noise at the drain, the two noise sources are partially correlated with a correlation factor '*c*'. The correlation factor between the drain thermal noise and the gate induced noise is defined as,

$$c = \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}\,\overline{i_{nd}^2}}} \approx 0.395j \tag{3.8}$$

Although the noise behavior of long channel devices is well understood, the precise behavior of δ in the short channel regime is unknown at present. Given that both the gate noise and drain noise share a common origin, however, it is probably reasonable as a crude approximation to assume that δ continues to be about twice as large as γ. Hence, just as γ is typically 1-2 for short-channel NMOS devices, δ may be taken as 2-4 [23].

4. SPIRAL INDUCTOR MODELING

Figure 4.1 shows the lumped element model of an inductor on silicon substrate. An on-chip inductor is physically a three-port element including the substrate. Although this model does not account for all electromagnetic events in a spiral inductor, it can be used instead of an ideal inductor at the initial phase of a design.

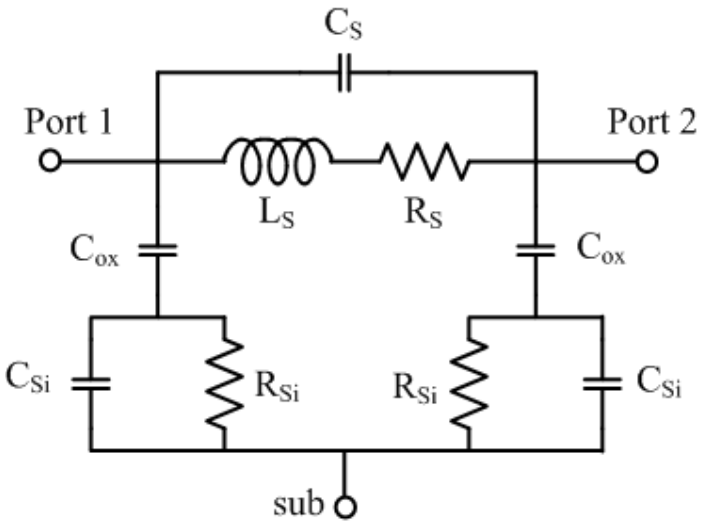

Figure 4.1: Physical model of an inductor on silicon [24]

The series part of the model consists of an inductor (L_S) representing the series inductance, a resistance (R_S) representing the resistive losses due to skin effect and a capacitance (C_S) representing the capacitive coupling between the two ports.

Substrate parasitics C_{ox}, C_{Si} and R_{Si} model the capacitance to substrate, substrate resistive losses and the capacitive events occurring in the substrate, respectively. Although these parasitics are mostly different at each port, they can be assumed to be equal without much error.

In the following subsections calculation methods for the model elements are presented.

4.1 Calculation of series inductance

Many different computation methods for Ls have been proposed in literature and two of them are presented in this section.

4.1.1 Modified Wheeler Formula

Mohan et al [25] obtained a simple expression for planar spiral inductors by modifying the discrete inductor formulas presented by Wheeler [26]. It is given by

$$L_{mw} = K_1 \mu_0 \frac{N^2 d_{avg}}{1 + K_2 \rho} \qquad \textbf{(4.1)}$$

where μ_0 ($4\pi 10^{-7}$ F/m) is the vacuum permeability, $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$ is the fill ratio, $d_{avg} = (d_{out} + d_{in})/2$ is the average diameter and N is the number of turns. The coefficients K_1 and K_2 are layout dependent and their values are given in Table 4.1 for octagonal and square geometries. Figure 4.2 shows square and octagonal spiral geometries commonly used in CMOS technologies.

Table 4.1: Coefficients for modified wheeler expression

Geometry	K_1	K_2
Square	2.34	2.75
Octagonal	2.25	3.55

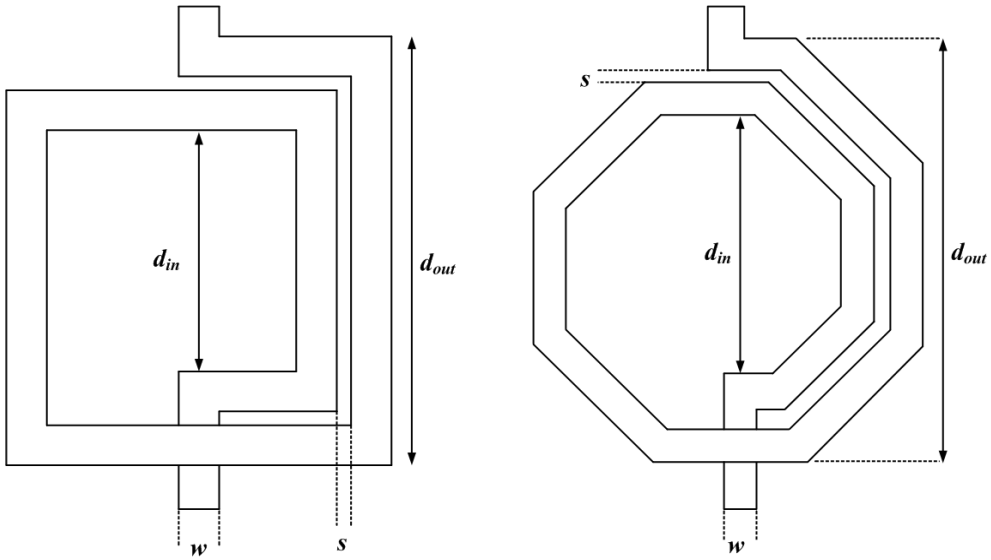

Figure 4.2: Spiral inductor geometries (a) Square (b) Octagonal

4.1.2 Semiempirical inductance formula

Ronkainen et al. [27] derived a semiempirical expression for rectangular inductors given as

$$L = 1.5\mu_0 N^2 d_{out} e^{-\frac{3.7(N-1)(w+s)}{d_{out}}} \left(\frac{d_{out}}{w}\right)^{0.1} \quad \textbf{(4.2)}$$

A close expression can be used for octagonal inductors as

$$L = 1.5\mu_0 N^2 d_{out} e^{-\frac{3.7(N-1)(w+s)}{d_{out}}} \left(\frac{d_{out}}{w}\right)^{0.1} \quad \textbf{(4.3)}$$

where μ_0 is the vacuum permeability, N the number of turns, d_{out} is outer diameter of the inductors, and s and w are the spacing and the width of the inductor traces, respectively.

Comparison of two inductance formulas was carried out on 14 square inductors provided by the foundry and it is found that for all inductors, equation (4.2) gives more realistic results than equation (4.1).

4.2 Calculation of series resistance (R_S)

The series resistance, R_S, represents the resistive losses in the conductor due to skin effect. The series resistance, can be expressed as

$$R_S = \frac{\rho . l}{w . t_{eff}} \quad \textbf{(4.4)}$$

where $t_{eff} = \delta\left(1 - e^{-t/\delta}\right)$ is the effective metal thickness, ρ is the metal resistivity at dc, l is the overall length of spiral, w is the spiral line width, δ is the metal skin depth and t is the metal thickness.

The skin depth is defined as

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \quad \textbf{(4.5)}$$

where ρ, μ, and f represent the resistivity in Ω-m, permeability in H/m, and frequency in Hz, respectively.

4.3 Calculation of series capacitance (C_S)

The series capacitance (C_S) models the parasitic capacitive coupling between input and output ports of an inductor. This capacitance accounts for both the interturn fringing capacitance and overlap capacitance between the underpass and inductor turns. However, the interturn fringing capacitance is very small compared to overlap capacitance since the potential difference between the turns is close to zero [24]. On the other hand the potential difference between the underpass and inductor windings is larger, so that C_S can be approximated by the overlap capacitance as given by

$$C_S = n.w^2.\frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{4.6}$$

where n is the number of crossovers between spiral and underpass, w is the spiral line width. ε_{ox} and $t_{oxM1\text{-}M2}$ are the dielectric constant and the thickness of the oxide between the spiral and the underpass, respectively.

4.4 Calculation of substrate parasitics (C_{OX}, C_{Si} and R_{Si})

The parasitics associated with the substrate are represented by C_{OX}, C_{Si}, and R_{Si}. The capacitance between the spiral and the substrate are modeled by C_{ox}. The ohmic losses occurring in the substrate are modeled by R_{Si} and capacitive effects in the substrate are modeled by C_{Si}. These parasitics are proportional to the area occupied by the spiral and they can be calculated by the following expressions. Note that the area of the spiral is equal to the product of the spiral length (l) and width (w).

$$C_{ox} = \frac{1}{2}.l.w.\frac{\varepsilon_{ox}}{t_{ox}} \tag{4.7}$$

$$C_{Si} = \frac{1}{2}.l.w.C_{sub} \tag{4.8}$$

$$R_{Si} = \frac{2}{l.w.G_{sub}} \tag{4.9}$$

where C_{sub} and G_{sub} are capacitance and conductance per unit area for the silicon substrates and they are extracted from measurement results. ε_{ox} and t_{ox} are the dielectric constant and thickness of the oxide layer between the inductor and the

substrate. C_{sub} and G_{sub} do not change significantly for the inductors produced in the same technology.

4.5 Evaluation of quality factor of an inductor

The quality factor (Q) of an inductor signifies the magnetic energy storage efficiency of that inductor. The Q of an inductor is defined as [28]

$$Q = 2\pi \frac{\left|Peak\ Magnetic\ Energy - Peak\ Electric\ Energy\right|}{Energy\ Loss\ in\ One\ Oscillation\ Cycle} \tag{4.10}$$

First, consider the inductor model with one port and substrate is grounded as shown in Figure 4.3a. Next, shunt substrate parasitics can be embedded in R_P and C_P as shown in Figure 4.3b. Note that R_p and C_p represent the combined effects of C_{ox}, C_{si} and R_{si}, and hence they are frequency dependent. R_p and C_p are expressed as

$$R_P = \frac{1}{\omega^2 C_{OX}^2 R_{Si}} + \frac{R_{Si}\left(C_{OX} + C_{Si}\right)^2}{C_{OX}^2} \tag{4.11}$$

$$C_P = C_{OX}\frac{1 + \omega^2\left(C_{OX} + C_{Si}\right)C_{Si}R_{Si}^2}{1 + \omega^2\left(C_{OX} + C_{Si}\right)^2 R_{Si}^2} \tag{4.12}$$

Then from the Q definition of (4.10), we get

$$Q = \frac{\omega L_S}{R_S}\cdot\left(\frac{R_P}{R_P + [(\omega L_S/R_S)^2 + 1]R_S}\right)\cdot\left(1 - \frac{R_S^2\left(C_S + C_P\right)}{L_S} - \omega^2 L_S\left(C_S + C_P\right)\right) \tag{4.13}$$

The first term of (4.13) is the ratio of the stored magnetic energy to the ohmic loss of the spiral conductor. The second term is due to the energy loss occurring in the substrate. The last term explains the reduction in Q due to the increase in the peak electric energy with frequency and the vanishing of Q at the self-resonant frequency [28].

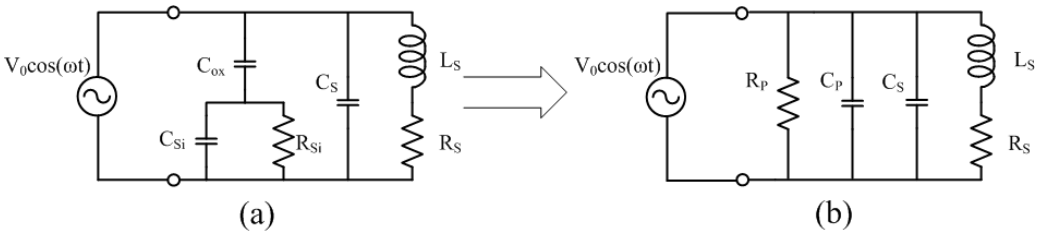

Figure 4.3: Determination of Q from inductor model

Thus, the self-resonant frequency can be found by equating the last term in (4.13) to zero.

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{L_S(C_P + C_S)} - \frac{R_S^2}{L_S^2}} \qquad \textbf{(4.14)}$$

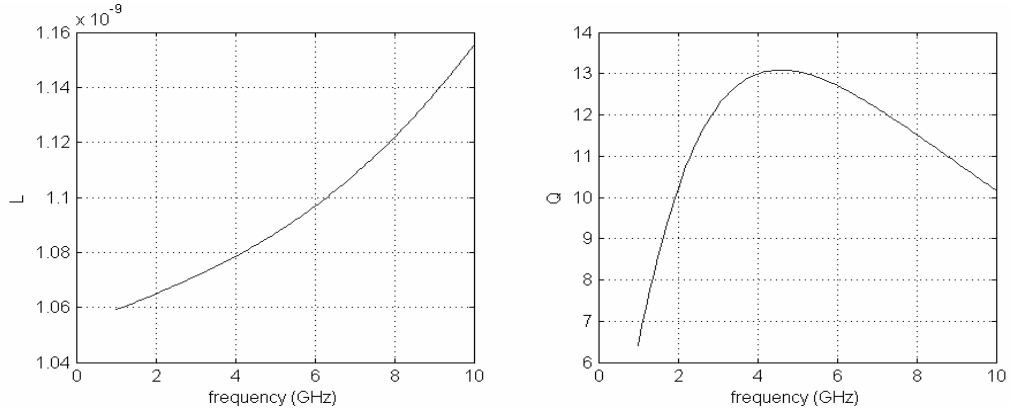

Figure 4.4: Typical series inductance and Q factor calculated by model

Figure 4.4 shows the calculated inductance and Q factor of the inductor whose geometric parameters are given in the first row of Table 4.2. In the table, L_S is the measured inductance value. L_{S1} and L_{S2} are the calculated inductance values from equations (4.1) and (4.2), respectively.

Table 4.2: Comparison of the measured and modeled inductors

w (μm)	s (μm)	N	d_{out} (μm)	d_{in} (μm)	L_S (nH)	Q_{max} (measured)	L_{S1} (nH)	L_{S2} (nH)	Q_{max} (calculated)
20	3	1.75	200	114	1.07	11.9@4.4GHz	0.81	1.05	12.9@4.44GHz
20	3	1.75	250	164	1.52	11.7@3.9GHz	1.18	1.44	11.4@3.21GHz
10	3	1.75	250	204	2.02	10.4@3.9GHz	1.6	1.72	8.7@5.5GHz
10	10	2.75	200	100	2.10	9.9@3.9GHz	1.74	2.01	8.6@4.57GHz
20	3	2.75	250	118	2.42	9.6@2.7GHz	2.06	2.52	10.6@1.92GHz
10	10	2.75	250	150	3.07	8.9@3GHz	2.64	2.93	7.6@3.09GHz
5	3	3.75	150	92	3.25	9.4@4.3GHz	3.01	3.25	7.5@5.7GHz
10	3	2.75	250	178	3.67	9.4@2.7GHz	3.25	3.51	7.9@2.6GHz
5	3	2.75	250	208	4.66	8.3@3.7GHz	4.06	4.28	6.05@4.2GHz
10	3	2.75	300	228	4.85	8.8@2.4GHz	4.29	4.54	7.25@2.1GHz
5	3	2.75	300	258	6.00	7.2@3GHz	5.14	5.42	5.45@3.28GHz
5	3	3.75	250	192	7.25	7.7@2.5GHz	6.71	7.08	5.65@2.54GHz
5	3	4.75	250	176	10.02	7.2@2GHz	9.56	10.08	5.5@1.86GHz
5	3	4.75	300	226	13.30	6.7@1.7GHz	12.58	13.27	5.1@1.5GHz

5. DISTRIBUTED AMPLIFIER DESIGN IN 0.35µm TECHNOLOGY

In this chapter, firstly, common-source and cascode gain cells will be studied and their high frequency performances will be compared, then the detailed design strategy of two distributed amplifier implementations will be presented.

The first design is a 3-stage common source DA in 0.35µm CMOS technology. This amplifier exhibits a gain of 8dB over 0.1-8GHz bandwidth and uses octagonal spiral inductors to realize artificial transmission lines. Power consumption is 25.5mW while operating from a 1.5V supply. Chip area is 0.972 x 1.67mm^2.

The second design is a 3-stage cascode design in 0.35µm SiGe BiCMOS technology and it achieves a gain of 9.2dB over 0.1-9.2GHz bandwidth. Power consumption is 56 mW while driven from a 3.3V supply. Both amplifiers were designed following the design principles presented in Chapter 2.

5.1 Gain Cells for DAs

Figure 5.1 shows three gain cells which can be used in a DA design in CMOS technology. Cascode stage shown in Figure 5.1 (b) is usually preferred in the design because of its well-known advantages:

- improved reverse isolation,
- increased output impedance,
- reduced Miller effect due to C_{gd} of the input transistors.

However, a cascode gain stage has disadvantages such as decreased voltage headroom and increased the noise figure. Moreover, the pole at the cascode node, labeled as A in Figure 5.1 (b), causes a more serious problem for the cascode stage. If a large transistor is selected to improve the gm efficiency, the pole at the node A can reduce the bandwidth, since the current signal at the drain of M1 can be shunted by C_{gs2}, C_{sb2}, and C_{db1} at high frequencies. Note that these capacitances may be very large if large transistors are employed in the design [10].

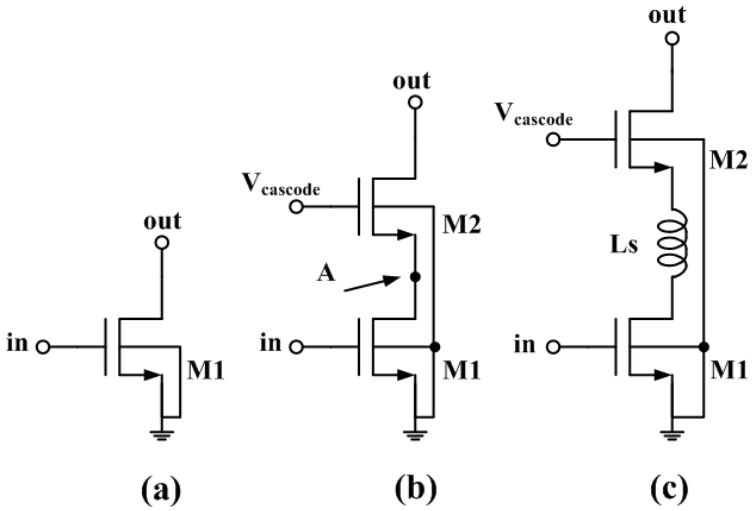

Figure 5.1: Gain cells (a) Common source, (b) Cascode, (c) Cascode with L_S

If C_{gd1} and all resistive losses are neglected, overall transconductance of the cascode stage can be given as

$$Gmcc = \frac{g_{m1}g_{m2}}{g_{m2} + s(C_{gs2} + C_{sb2} + C_{db1})} \tag{5.1}$$

which has a pole at the node A given as,

$$f_A = \frac{g_{m2}}{2\pi(C_{gs2} + C_{sb2} + C_{db1})} \tag{5.2}$$

In order to tune out the capacitance at the node A, a series inductor L_S can be inserted between the common source and common gate transistors as shown in Figure 5.1(c). The effective transconductance of the cascode cell with L_S can be expressed as,

$$Gmcc2 = \frac{g_{m1}g_{m2}}{g_{m2} + s(C_{gs2} + C_{sb2} + C_{db1}) + s^2 L_S C_{db1}(g_{m2} + s(C_{gs2} + C_{sb2}))} \tag{5.3}$$

The poles of the (5.3) are plotted in Figure 5.2. As seen from the figure that the addition of the L_S creates an additional complex conjugate pole pair. Also, as L_S increases, the first pole (f_A) is pushed to higher frequencies while the complex conjugate poles come closer to the origin. There is an optimum L_S value above which gain peaking due to complex conjugate poles reduces the useful bandwidth of the amplifier.

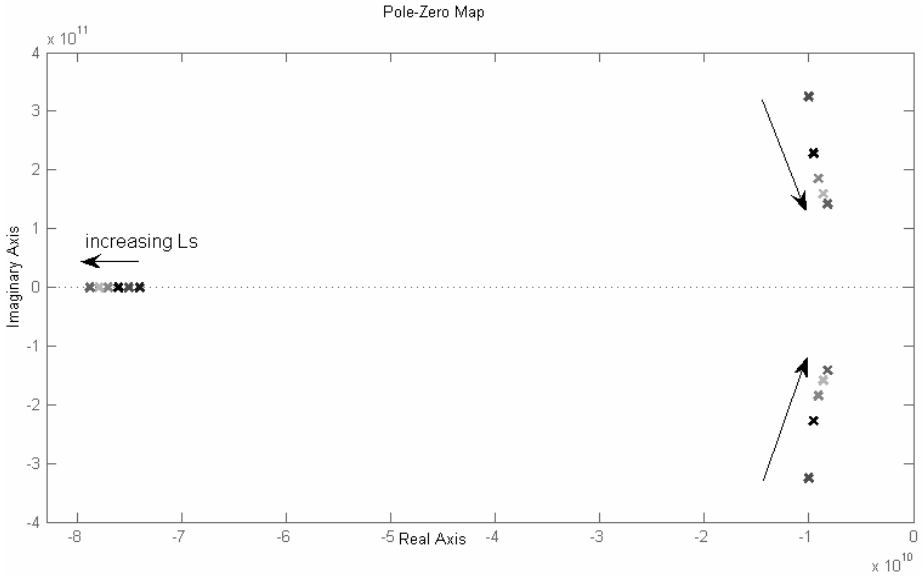

Figure 5.2: Pole-zero map for cascode circuit with Ls

Y_{21} of the gain cells and transconductance of the cascode stage given by (5.1) are plotted in Figure 5.3. It is clear that the regular cascode cell can not be used in a DA design since flat gain over a high bandwidth is desired. However, a cascode cell with appropriate series inductor L_S can be employed in a DA. Note that these results are process dependent such that cascode cell's performance could be acceptable in a different process.

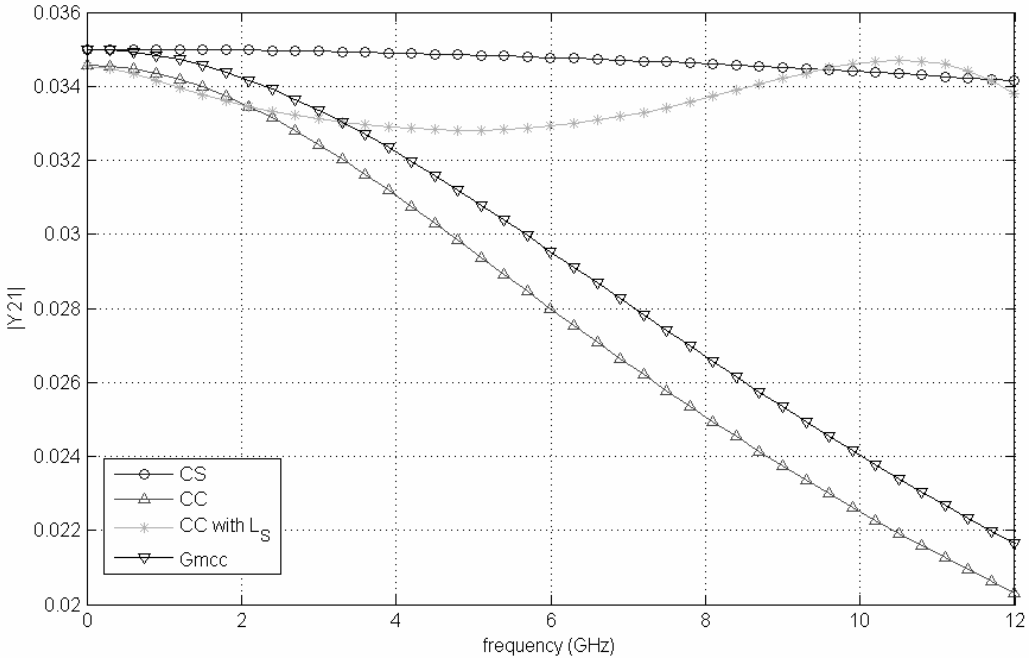

Figure 5.3: Y_{21} of the gain cells (g_{m1}= g_{m2} = 35mS, g_{mb2} = 5mS, C_{gs1} = C_{gs2}=350fF, C_{gd1} = C_{gd2}=55fF, g_{ds1} = g_{ds2}=500µS, Rsub=90Ω, C_{db1} = C_{sb2}=120fF, L_S = 800pH)

5.2 CMOS DA Design

In a DA design, gain, bandwidth and power consumption specs are necessary to start the design. Additionally, chip area can be supplied as design spec. The design targets of this work are 8dB gain, 8GHz bandwidth and maximum current consumption of 20mA. Also, the maximum allowed area is 2 mm^2.

The number of gain stages used in the distributed amplifier must be optimized for the technology in which it is implemented. While increasing the number of stages (N) should increase gain, parasitics of the active and passive elements will limit the gain-bandwidth performance. Also, silicon area should be taken into account while determining the number of stages. Since the silicon area increases proportionally with N, the number of sections (N) was chosen as 3 to be able limit the area below $2mm^2$.

The effect of transistor bias point on the important performance metrics of DA is shown in Table 5.1. For a fixed drain current, if we want to operate in weak inversin (W.I.) region, we need to increase the aspect ratio (W/L) and decrease the overdrive (V_{GS}-V_T). In W.I. region unity gain cutoff frequency (f_T) reduces, so the bandwidth of the amplifier reduces. Yet the gm efficiency (gm/I) increases. As a result, gain of the amplifier increases and the noise figure reduces [10]. Figure 5.4 shows gm/I versus V_{GS} for the technology used in this work.

In addition, increasing the transconductance by increasing transistor size increases the input/output capacitance of the device and the required inductance value for constant line impedances. As the inductance value increase, quality factor and self resonant frequency of the inductor decrease and this can be translated into a decrease in gain-bandwidth.

Table 5.1: DA performance for a fixed current [10]

MOS Bias Trade-offs					DA Performance		
W/L	Op.	V_{GS}-V_T	*gm/I*	f_T	G	NF	BW
↑	W.I.	↓	↑	↓	↑	↓	↓
↓	S.I.	↑	↓	↑	↓	↑	↑

On the other hand, higher f_T and bandwidth are possible in strong inversion (S.I.) region. To bias a MOSFET into S.I. with fixed drain current, we need to decrease the aspect ratio and increase the overdrive. This leads to drop of the gm/I, so that the gain decreases and the noise figure increases.

Although choosing an operating point close to W.I. is more advantageous, it is not possible to obtain 8GHz bandwidth while operating in W.I. in 0.35µm CMOS technology.

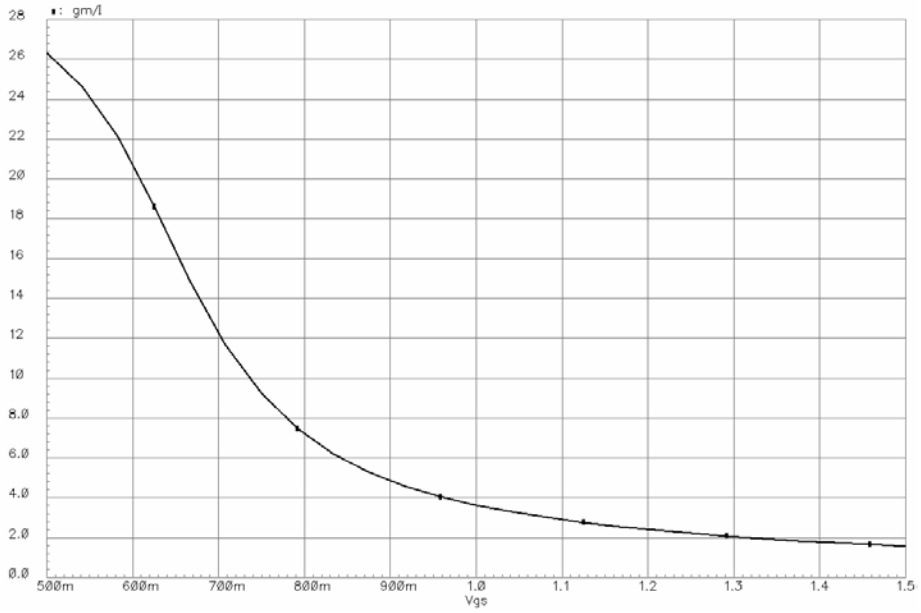

Figure 5.4: The gm efficiency (gm/I) vs. gate source voltage (Vgs)

5.2.1 Design procedure

Assuming $L_g = L_d = L$ and $C_g = C_d = C$, the cut off frequency of the lines can be given as,

$$f_c = \frac{1}{\pi\sqrt{LC}} \tag{5.4}$$

and characteristic impedance of the lines becomes,

$$Z_0 = \sqrt{\frac{L}{C}} \tag{5.5}$$

From (5.4) and (5.5), we can express the capacitance of the lines in terms of f_c and Z_0,

$$C = \frac{1}{Z_0 \pi f_c} \tag{5.6}$$

Since the impedance matching property of the gate and drain lines degrade as the cutoff frequency is approached, f_c should be chosen larger than bandwidth of the amplifier (f_{1dB}). For Z_0=50Ω and f_c =10GHz, we calculate the capacitance and the inductance of the lines using (5.5) and (5.6) as C ≈ 600fF and L ≈ 1.5nH.

Assuming the 25% of the capacitance comes from the inductor parasitics, total gate capacitance is around 450fF. The total gate capacitance of a MOSFET is defined as

$$C_{gg} = W_{eff} L_{eff} C_{ox} \quad \textbf{(5.7)}$$

where W_{eff} is the effective gate width, L_{eff} is the effective gate length. Denoting the drawn values with W_{drawn} and L_{drawn}, effective gate width and gate length can be approximated by

$$W_{eff} \cong W - 2W_{\text{int}} \quad \textbf{(5.8)}$$

$$L_{eff} \cong L - 2L_{\text{int}} \quad \textbf{(5.9)}$$

where W_{int} and L_{int} are width and length offset parameters in Bsim3v3 model, respectively.

C_{ox} (F/m^2) is the oxide capacitance per unit gate area defined by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \textbf{(5.10)}$$

where ε_{ox} = 3.46x10^{-11} F/m is the dielectric constant of the gate oxide (SiO_2), and t_{ox} (m) is the gate oxide thickness.

For the technology used in this thesis, these parameters are L_{drawn} = 0.35μm, W_{int} = 26.76nm, L_{int} = 8.285nm, t_{ox} = 7.7nm and C_{ox}= 4.5x10^{-3} F/m^2.

From (5.7), W_{eff} = 300μm was found for C_{gg} = 450fF. For such a large width, we can take $W = W_{eff}$.

According to (2.78), f_{max} is related to amplifier parameters as

$$f_{\max} \approx 1.25 A_0 f_{1dB} \quad \textbf{(5.11)}$$

which gives f_{max} = 25GHz for f_{1dB} = 8GHz and A_0 = 2.5.

In Figure 5.5, the maximum oscillation frequency (f_{max}) is plotted against drain current for W_{drawn} = 300μm, L_{drawn} = 0.35μm and V_{DS}=1.5V.

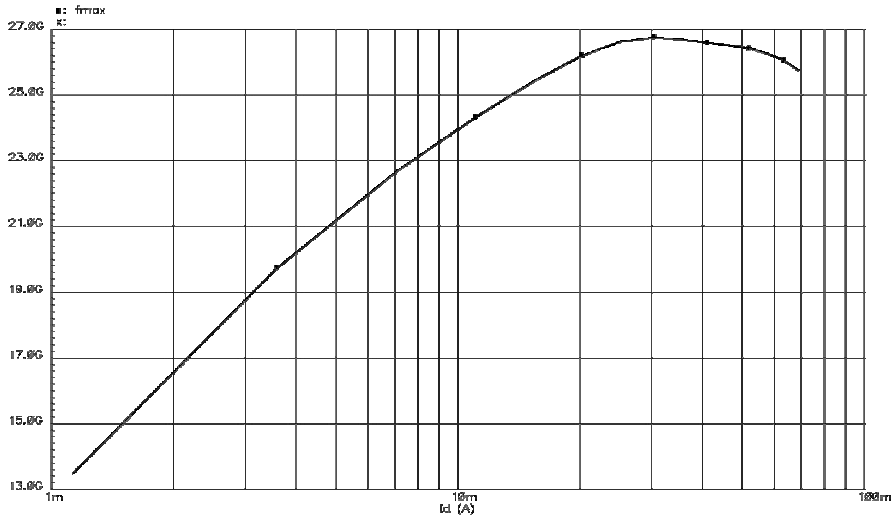

Figure 5.5: f_{max} vs. I_d (W=300µm, L=0.35µm V_{DS} =1.5V)

Using the gain equation of (2.19), we can calculate the necessary transconductance for the transistors,

$$g_m = \frac{NZ_0}{2A_0} \tag{5.12}$$

Equation (5.12) gives the required g_m value as 35mS for N = 3, Z_0 = 50Ω and A_0= 2.5. However, the drain losses reduce of the gain even at low frequencies so that g_m was selected 40mS to have a safe margin. Transconductance of the transistor against its drain current is plotted in Figure 5.6 which shows that the drain current of 5.5mA is necessary for g_m=40mS. Then g_m /I is 7.2 and V_{GS} = 0.8V according to Figure 5.4. Also, according to Figure 5.5, this drain current gives f_{max} of 22GHz.

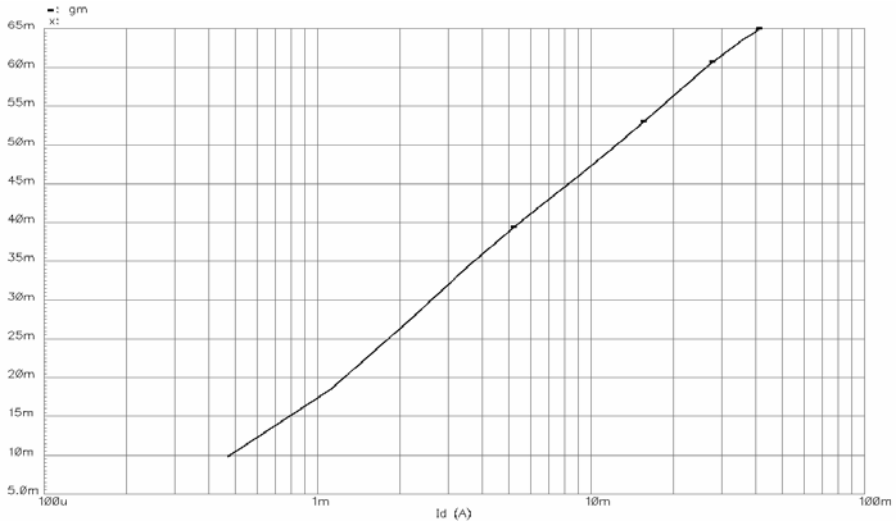

Figure 5.6: g_m vs I_d (W=300µm, L=0.35µm V_{DS} =1.5V)

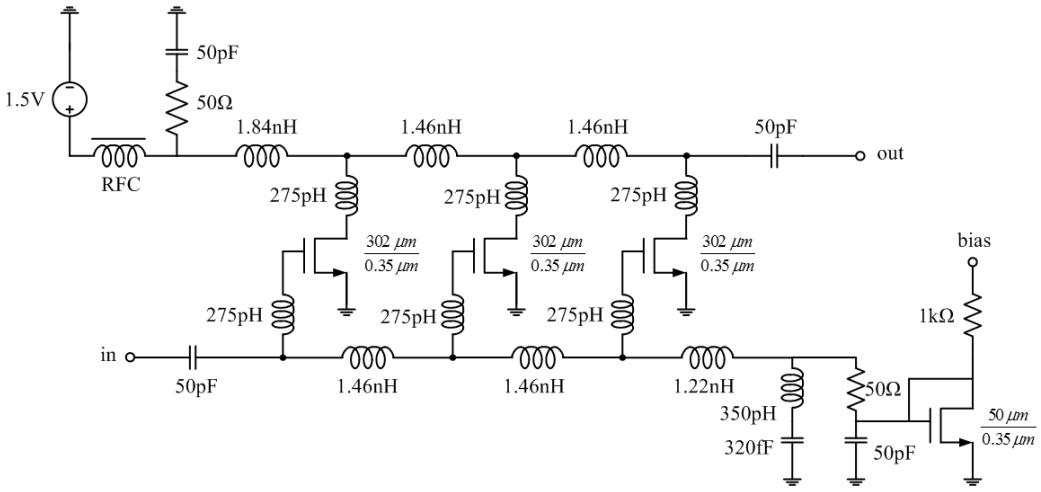

Figure 5.7: CMOS DA with CS gain cells

The final optimized circuit topology of the CMOS DA is shown in Figure 5.7. An m-derived half section was used before the gate line termination resistor for better input impedance matching. Also during the optimization of amplifier, input and output half inductors and additional capacitances at the drain taps were removed and the value of the inductor before the drain termination was increased.

Biasing of the DA is provided by a current mirror and the reference current is supplied by an external source for test purposes.

Small inductors series with the gate and the drain increase the peaking in the gate and drain lines, thus, improves the frequency response of the DA.

All inductors were implemented in top available metal and an octagonal configuration was used to minimize losses due to sharp bends, and to improve the quality factor of these inductors. Metal lines used as interconnects were also modeled as transmission lines to account for the phase shift and losses in signal path. The circuit used a single 1.5V supply, which was provided through a RF-Choke.

OEA's Spiral® tool was used for the synthesis and simulation of the on-chip inductors. Table 5.2 presents the geometry information and the peak Q of the inductors used in the design. L_1 is the inductance of the octagonal section of the inductors; however, if the routings between the inductors are taken into account, the inductance values increase to L_2 value.

Table 5.2: Simulated performance and geometry information of inductors

L_1	L_2	W (μm)	S (μm)	T	d_{in} (μm)	d_{out} (μm)	Q_{max}
250pH	275pH	12	3	1.5	36.6	90.7	16@25GHz
300pH	350pH	15	3	1.5	45.3	111	17@21GHz
1nH	1.22nH	15	3	2.5	72.8	174.8	12.8@8.6GHz
1.35nH	1.46nH	15	3	2.5	92.7	195	12@7GHz
1.6nH	1.84nH	15	3	2.5	115.7	217.7	11@5.4GHz

5.3 CMOS DA Layout

The complete layout of the DA is shown in Figure 5.8. The area of the layout is 1.67x0.932 mm^2. Layout symmetry is vital to ensure phase delay is equal in gate and drain artificial transmission lines. Also, in order to reduce the coupling between the inductors, spacing between the inductors should be enough.

The input and the output capacitances were realized with high quality Metal-Insulator-Metal (MIM) capacitors, whereas bypass capacitors were realized with stack capacitors. Stack capacitor is the parallel combination of MOS capacitor and poly capacitor and it has higher capacitance per unit area but lower quality factor than MIM capacitor.

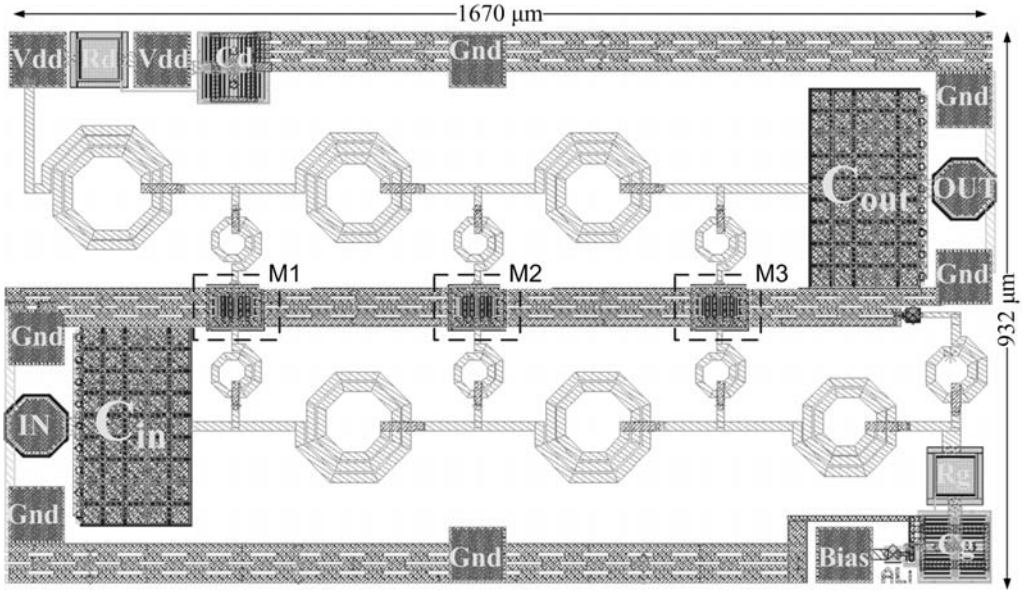

Figure 5.8: Layout of CMOS DA

Termination resistors are realized with polysilicon resistors and dummy poly layers were placed around the resistor in order to decrease etching effects.

NWELL layers were placed under the signal pads so as to reduce the parasitic capacitance to the substrate.

MOS transistor layout should be optimized for maximum f_{max}. This can be done by adjusting the finger width of the transistor. Decreasing the finger width reduces the gate resistance; however, increases the gate-bulk capacitance. So it is better not to use very small finger widths.

Figure 5.9 shows the MOSFET layout which has 72 fingers with 4.2 μm. Dummy polysilicon resistors are placed around the transistor so as to reduce the etching effects at the boundaries.

The effects of the substrate resistance on the performance of the transistor are critical as explained in Chapter 3. Thus, substrate contacts are placed between the transistor sections and around the transistor to reduce the substrate resistance.

Also NWELL guard ring was placed around the transistor to reduce the signal coupling through the substrate.

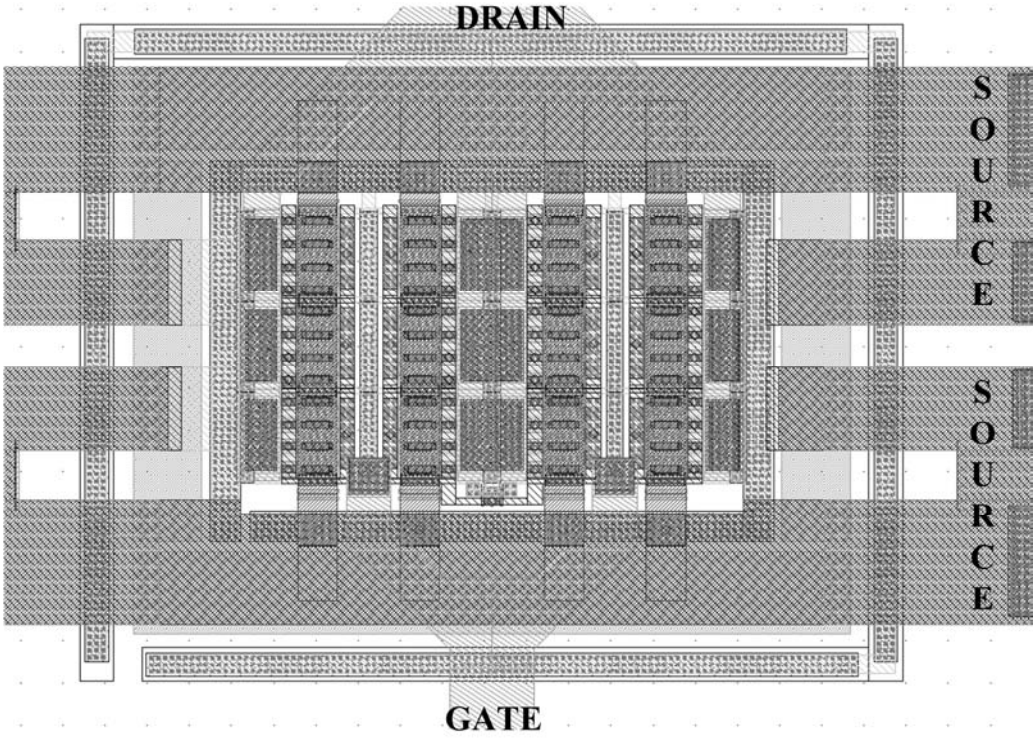

Figure 5.9: MOSFET layout (W=302μm L=0.35μm, finger width 4.2μm, nf =72)

5.4 CMOS DA Simulation Results

In this section simulated performance of the CMOS DA is presented. All small signal and large signal simulations were carried out with SPECTRE circuit simulator. Figure 5.10 shows the S-parameter response of the DA. S21 is 8±1 dB up to 8GHz and S11 and S22 are both less than -10 dB over the bandwidth.

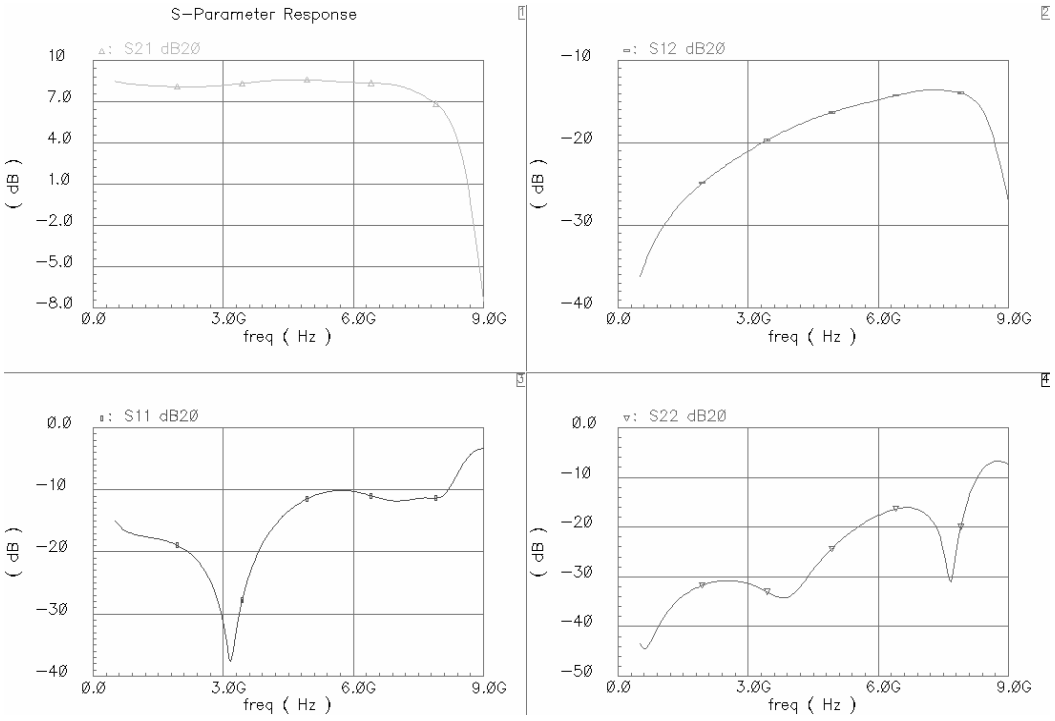

Figure 5.10: Simulated S-parameter response of the DA

Figure 5.11 shows group delay of DA with and without peaking inductors series with gate and drain of MOSFETs. It is clear that although these inductors improve the gain flatness, they deteriorate the group delay performance of the DA.

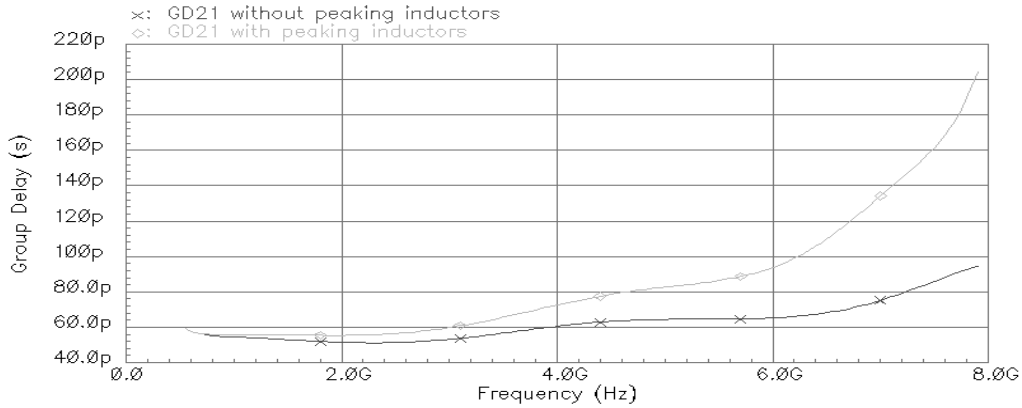

Figure 5.11: Group delay of CMOS DA with/without peaking inductors

Figure 5.12 (a) shows the input referred 1 dB compression point simulation results for a 5GHz input signal. In this simulation, input signal power was increased from -30dBm to 0dBm and input power level where the gain drops by 1dB was found as -4dBm.

Figure 5.12 (b) presents the noise figure simulation of the DA. As expected the noise figure is high at low and high frequencies and minimum at the midband. The minimum noise figure of 3.5 dB was achieved at 4.3 GHz.

Figure 5.13 presents the transient response of the DA for a 2GHz input signal. We can see that the transient response has no significant ringing.

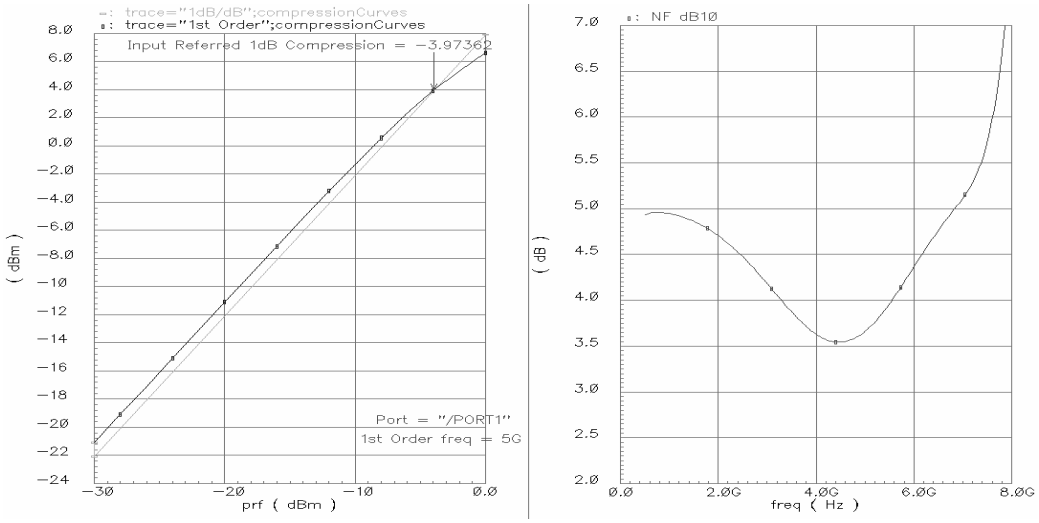

Figure 5.12: Simulated input 1-dB compression point and noise figure of DA

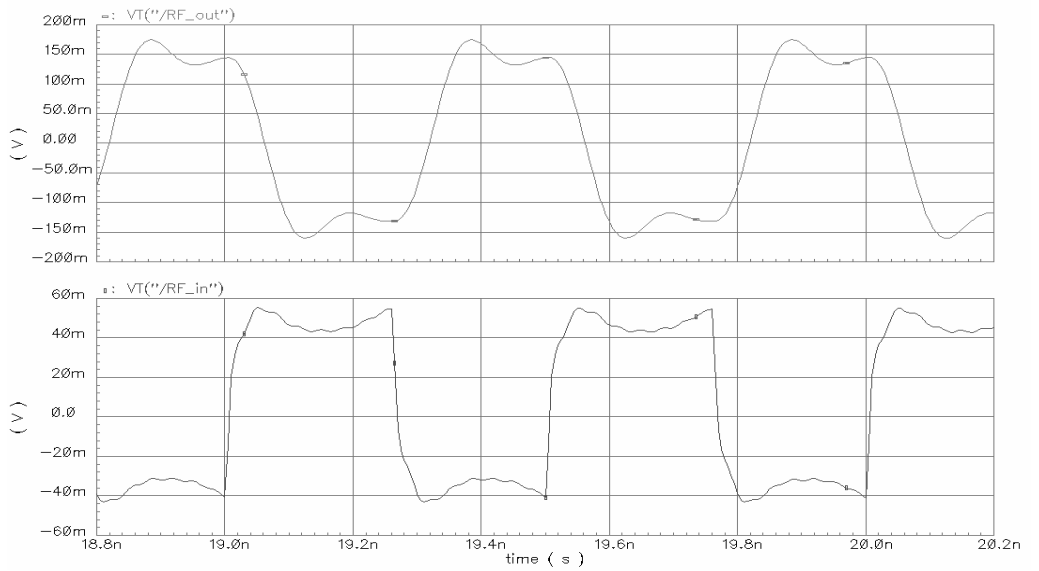

Figure 5.13: Simulated transient response of the DA

5.5 BiCMOS DA Design

As shown in Figure 5.3, simple cascode gain cell's high frequency performance is worse than the CS gain cell. So an additional series inductor is necessary in order to use the cascode cell in the design as shown in Figure 5.1 (c). Alternatively, in a BiCMOS technology, the common gate MOSFET of the cascode cell can be replaced with a common base npn transistor as shown in Figure 5.14. Figure 5.15 shows the simulated maximum available gain of the CS, CMOS cascode and BiCMOS cascode cells for 5.5mA current consumption. As seen in the figure, much better performance can be achieved with the BiCMOS cascode cell.

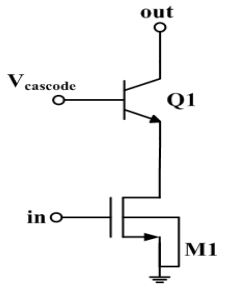

Figure 5.14: Cascode cell in SiGe technology

A 3-stage cascode distributed amplifier was designed and BiCMOS cascode cell was employed as gain stages. Figure 5.16 shows the schematic of the cascode DA designed in BiCMOS technology. The current consumption of the cascode cell is equal to 5.5mA as in the previous design. Thus the input transistor width was not changed. The emitter area (A_E) of npn transistor was scaled so as to get peak f_T.

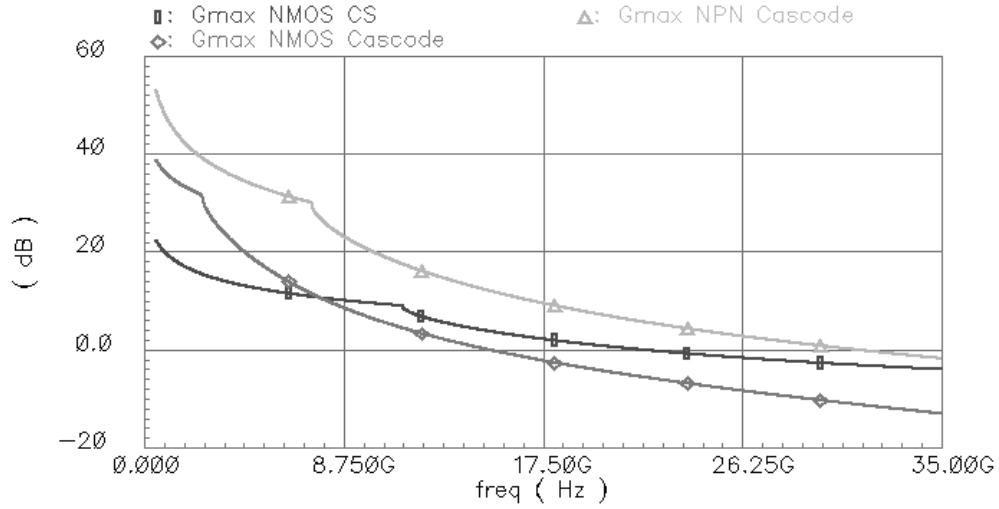

Figure 5.15: Maximum available power gain for CS, Cascode and npn Cascode cells

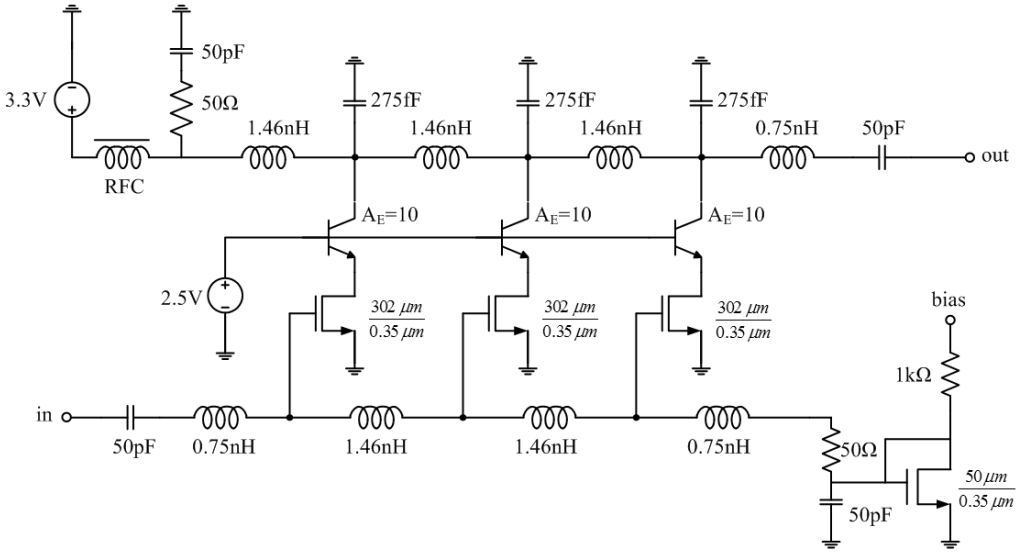

Figure 5.16: BiCMOS DA with cascode gain cells

The addition of a cascode gain cell improves impedance matching and it also reduces the Miller effect in the driver transistor, improving the amplifier's overall frequency response.

The S-parameter response of the cascode DA is shown in Figure 5.17. This amplifier presents 9dB gain over the 9GHz bandwidth. Figure 5.18 shows that the input 1dB compression point is -4.6 dBm and minimum noise figure is 4.2 dB at 5.25 GHz.

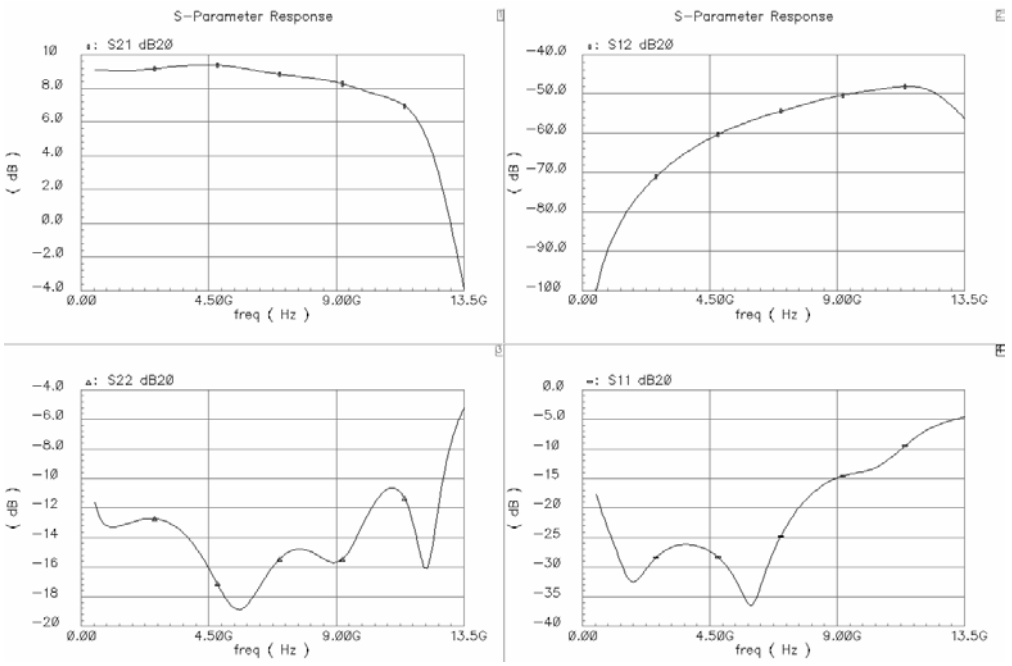

Figure 5.17: Simulated S-parameter response of the cascode DA

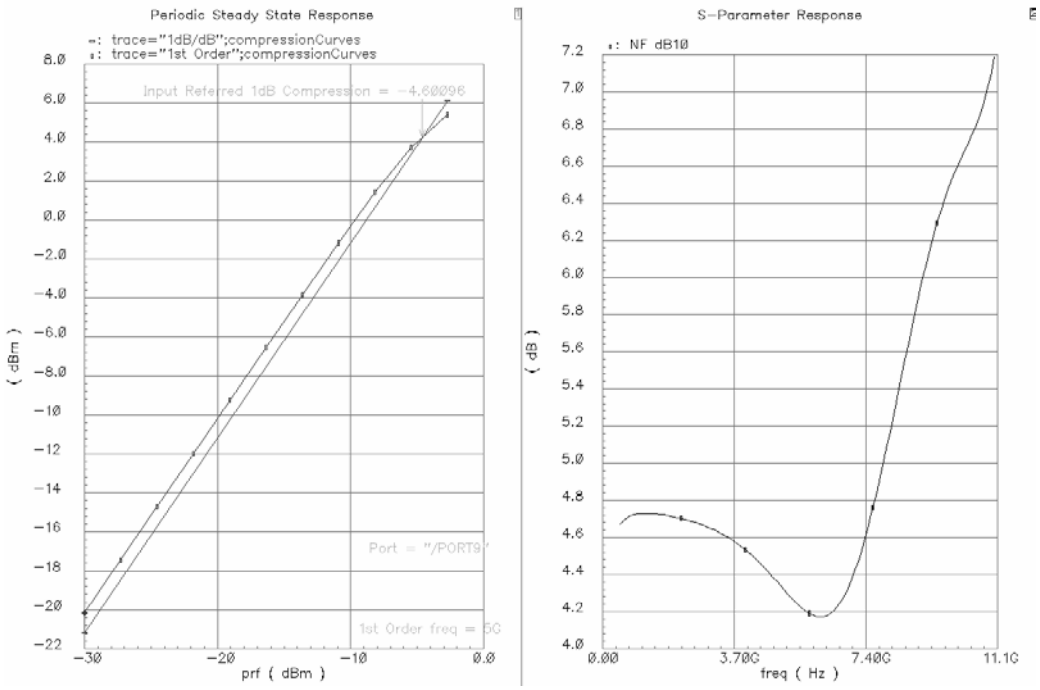

Figure 5.18: Simulated input 1-dB compression point and noise figure of the DA

Figure 5.19 shows the group delay performance of the cascode DA.

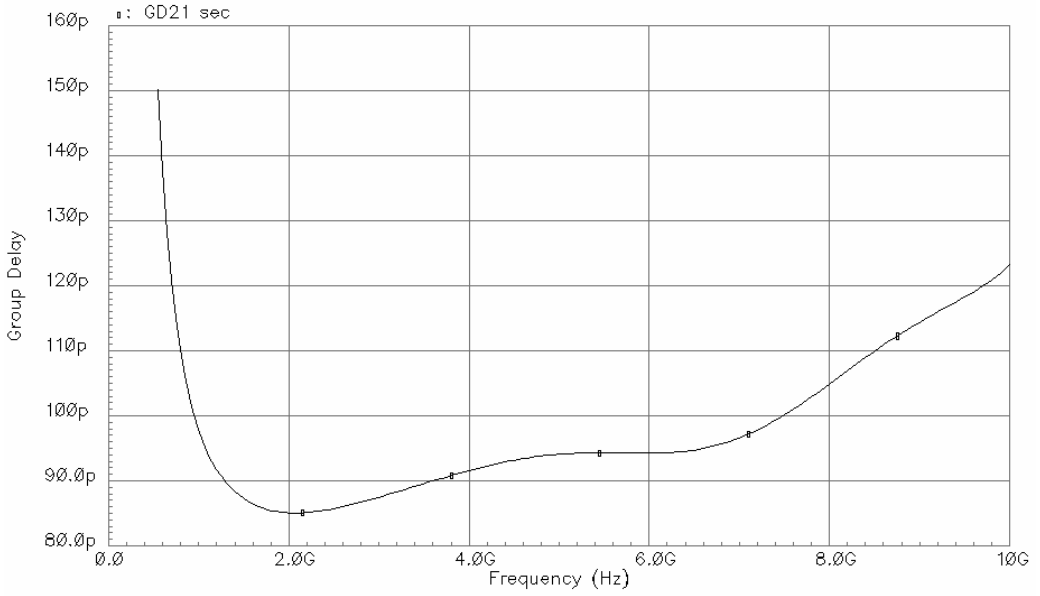

Figure 5.19: Simulated group delay of the cascode DA

Table 5.3 presents the performance comparison of the two DAs. Common source topology has the advantages of low power and slightly low noise. On the other hand, cascode topology has higher gain-bandwidth and much better reverse isolation.

Table 5.3: DA performance comparison

	CS Amplifier	Cascode Amplifier
S21	8 dB	9.2 dB
Bandwidth (1dB)	7.9GHz	9.2GHz
Cutoff frequency	8.6GHz	13GHz
S11	<-10dB	<-10dB
S22	<-10dB	<-10dB
Minimum Noise Figure	3.51 dB	4.19 dB
1dB compression (input)	-4dBm	-4.6dBm
Power	25.5mW	56mW

6. CONCLUSION

In this thesis, the feasibility of CMOS DA in 0.35μm technology has been investigated. Starting from the simplest analysis, more complex and accurate analyses' are presented and a noise figure equation derived by taking into account the correlation between the drain noise and gate induced noise. These analytical expressions were beneficial for the design and optimization of DAs, and prediction of their performance such as gain, bandwidth, and noise figure.

Accurate RF models for active and passive devices are vital for the DA design. Thus, In Chapter 3, MOSFET high frequency behavior was studied and the RF MOSFET model explained in detail. Also, the techniques of modeling on chip spiral inductor were presented in Chapter 4. These models can be incorporated into design so that DA performance can be evaluated accurately.

The most widely used DA gain cell configurations were analyzed and it was shown that simple CMOS cascode gain cell configuration suffers from parasitic capacitance at the cascode node. Two alternative cascode gain cell were shown to be beneficial in design.

A common source DA was designed in 0.35μm CMOS technology following the design procedure presented in Chapter 2. Also RF MOSFET model and inductor model were utilized during the design phase. The amplifier achieved 8dB gain and 8GHz bandwidth. This prototype amplifier was sent to the fabrication.

A cascode DA was designed in 0.35um SiGe BiCMOS process. In this amplifier, the cascode transistor was realized by an npn transistor which helps to decrease the capacitance at the cascode node. This amplifier achieved 9dB gain over 9.2GHz band.

Experimental results are necessary to confirm the theoretical and simulation results. Once the prototype circuit is measured, the fully bipolar DA could be investigated for future work.

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BIOGRAPHY

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