CAPACITANCE-VOLTAGE SPECTROSCOPY IN METAL – TANTALUM PENTOXIDE (Ta_2O_5) – SILICON MOS CAPACITORS

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ABSTRACT

The electronic properties of Al-Ta_2O_5-Si MOS capacitors with oxide layers prepared by RF magnetron sputtering with or without a prior nitridation process in N_2O or NH_3 gas environments at temperature ranges between 700 °C to 850 °C were investigated using Capacitance-Voltage (C-V) Spectroscopy to determine the quality of oxide layer and oxide-silicon interface. The theoretical ideal capacitance-voltage calculations were compared with the experimental capacitance-voltage results in order to evaluate effective oxide charges, Q_{eff} , present inside Ta_2O_5 insulating layer and density of interface trap states, Dit, present at the Ta_2O_5-Si interface. In addition, dielectric constant, doping concentration, flat band voltage values were determined by using the experimental data. Finally, the effects of deposition conditions on Ta_2O_5 MOS capacitors were compared by using a reference sample of a MOS capacitor with native oxide SiO_2.

It has been found that dielectric constant value up to 12 have been reached for Ta_2O_5 insulating layers which increases the capacitance value several times than that of MOS capacitor with native oxide SiO_2. The density of interface trap states, D_{it}, for unnitrided Ta_2O_5 MOS capacitors, values around $1.6x10^{12}$ cm^{-2} eV^{-1} have been detected which is much higher than that of MOS capacitor with native oxide SiO_2. However, prior nitridation process enhances the interface properties and D_{it} values down to $2\text{-}5x10^{11}$ cm^{-2} eV^{-1} have been reached for the nitrided samples which is in the limits for MOS capacitors with high quality insulating layers. In addition, the effective oxide charges, Q_{eff}, for unnitrided samples, values as high as $3x10^{12}$ cm^{-2} were detected. Even though nitridation process enhances interface properties, the effective oxide charges are found to be higher for nitrided samples. Best electrical and interface properties are obtained by nitridation process at 800 °C in N_2O and NH_3. It can be inferred that samples nitrided in N_2O gas at 800 °C improves the dielectric constant above the level of SiO_2 and decreases both Q_{eff} and D_{it} levels to that of native oxide SiO_2.

These results show that a prior nitridation of p-silicon surface is a promising approach to improve both oxide and interface properties of Al-Ta_2O_5-Si MOS devices. However, further investigation is necessary to understand the nature of these oxide charges and interface properties of MOS devices with high dielectric constant oxide layers before integration into large scale fabrication.

ÖZET

RF (yüksek frekans) magnetron püskürtme tekniğiyle hazırlanmış, Al-Ta_2O_5-Si metal-oksit-yarıiletken (MOS) sığaların bir kısmı oksit tabakasının büyütülmesinden önce N_2O ve NH_3 gaz ortamlarında 700-850 °C alttaş sıcaklık aralığında nitrürleme işlemine maruz bırakılmış, ve nitrürlenmiş ile nitrürlenmemiş örneklerin elektriksel özellikleri, oksit tabakasının ve oksit-yarıiletken ara yüzeyinin kalitesi Sığa-Gerilim metoduyla incelenmiştir. Teorik ideal kapasite-gerilim hesaplamaları deneysel kapasite-gerilim ölçümleriyle karşılaştırılmış ve Ta_2O_5 oksit tabakası içindeki etkin oksit yük yoğunluğu, Q_{eff}, ve Ta_2O_5-Si ara yüzeyindeki tuzak yoğunluğu, D_{it}, hesaplanmıştır. Bunun yanı sıra deneysel veriler kullanılarak, dielektrik sabiti, katkılama yoğunluğu, düz bant gerilim değerleri bulunmuştur. Son olarak, oksit büyütme koşullarının Ta_2O_5 MOS sığalar üzerindeki etkisi referans örneği olan SiO_2 MOS sığayla karşılaştırılmıştır.

Sonuç olarak, Ta_2O_5 MOS sığalar için 12 ye varan dielektrik sabitleri elde edilmiştir ki bu değer sığa değerini SiO_2 MOS sığanın sığa değerinden bir kaç kat yukarıya çıkarmıştır. Ara yüzey tuzak yoğunluğu, D_{it}, nitrürlenmemiş örnekler için $1.6x10^{12}$ cm^{-2} eV^{-1} civarında bulunmuştur. Ancak bu değer SiO_2 MOS sığanın ara yüzey tuzak yoğunluğuyla karşılaştırıldığında yaklaşık olarak beş katlık bir artış gözlemlenmiştir. Öte yandan nitrürleme işlemi ara yüzeyin kalitesini arttırmış ve nitrürlenmiş örnekler için D_{it} değeri $2\text{-}5x10^{11}$ cm^{-2} eV^{-1} civarına düşürülmüştür. Etkin oksit yükleri açısından, Q_{eff}, nitrürlenmemiş örnekler için $3x10^{12}$ cm^{-2} ye kadar artan değerler hesaplanmıştır. Nitrürleme işlemi ara yüzey kalitesini arttırsa bile, Q_{eff} değerleri SiO_2 MOS sığayla karşılaştırıldığında hala yüksek olduğu gözlemlenmiştir. En iyi elektriksel ve ara yüzey özellikleri 800 °C'de yapılan nitrürleme işlemi sonuçunda elde edilmiştir. Sonuç olarak, N_2O gaz ortamında 800 °C'de yapılan nitürleme işlemi dielektrik sabitini arttırmış ve etkin oksit yük yoğunluğu, Q_{eff}, ve ara yüzey tuzak yoğunluğu, D_{it}, değerlerini SiO_2 MOS sığanın değerlerine kadar düşürmüştür.

Bu sonuçlar gösteriyor ki, nitürleme işlemi Al-Ta_2O_5-Si MOS sığaların oksit ve oksit-yarıiletken ara yüzey özelliklerini geliştirmede umut vaad eden bir yaklaşımdır. Ancak, büyük ölçeklerde fabrikasyon işlemine geçmeden önce yüksek dielektik sabitine sahip MOS sığalardaki oksit yüklerinin ve ara yüzey tuzak yoğunluklarının incelenmesi ve iyileştirilmesi gerekmektedir.

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CHAPTER 1

INTRODUCTION

In an article written in 1965, Gordon Moore described exponential growth in the number of transistors per integrated circuit and predicted this trend would continue. "Moore's Law" states that the number of transistors on integrated circuits doubles approximately every 24 months, resulting in higher performance at lower cost. This simple but profound statement is the foundation of semiconductor and computing industries. Similarly, to achieve 1 G-bit and higher capacity Dynamic Random Access Memories (DRAMs), the number of capacitors inside a chip must tremendously increase resulting in a miniaturization of device size which causes several different problems with the conventionally used gate insulators.

Native silicon dioxide (SiO_2) is a high-quality electrical insulator and it is used as a barrier material for electrical isolation of semiconductor devices, as a component in Metal- Oxide-Semiconductor (MOS) capacitors of DRAMs. It has been studied in detail by many researchers since it was the only insulating material used for the production of integrated circuits (Nicollian and Brews 1982). The researchers have focused on depositing an electronic grade SiO_2 by using different methods to achieve the best quality electronic devices. Different pre- and post- deposition methods such as rapid thermal annealing (Paskaleva et al. 1995), and nitridation (Croci et al. 2001) were used to increase the electrical quality of SiO_2 insulating layers. Finally, the quality of these devices were examined by using different measurement methods such as Conductance Spectroscopy (Nicollian and Goetzberger 1965, Nicollian et al. 1969, Duval et al. 2001a, Duval et al. 2001b, Duval et al. 2003, De Dios et al. 1990), Capacitance -Voltage (C-V) Spectroscopy (Paskaleva et al. 2003, Paskaleva and Atanassova 2000b), Current-Voltage (I-V) measurements (Paskaleva and Atanassova 2000a) and noise measurements (Fleetwood 1992, Fleetwood et al. 1993).

Once the optimum deposition type and conditions are obtained, researchers have started to produce thinner and thinner layers of SiO_2 in order to increase the minimum cell capacitance. Even tough, the perfect conventional SiO_2-Si structure is used in the production of 256 M-bit and lower capacity DRAMs, for the production of higher capacity DRAMs, the minimum cell capacitance must be studied in detail. Up to now, most of the strategies to satisfy the minimum cell capacitance have been focused

on an increase of the memory cell area as well as on decreasing of the dielectric thickness rather than using high dielectric constant materials. In practice, however, there is not much room for implementation of high capacitance by scaling down the dielectric thickness or expanding the capacitor area for gigabit scale DRAMs. From the thickness point of view, as CMOS devices are built with ever smaller features, the thickness of the conventional SiO_2 gate dielectric must be reduced. Finally, it has been realized that, after this long period of geometric scaling, it has been arrived at a point where the concomitant scaling of the thickness of the silicon dioxide (SiO_2) gate dielectric has left it only a few nanometers thick, beyond which the material no longer possesses its inherent physical characteristics. As the thickness of silicon dioxide approaches less than 1.5 nm, the leakage current becomes higher than 1 A/cm^2 and tunneling current increases significantly so that increase in power dissipation and heat become critical issues. Although great success has been achieved, the current DRAM technology can not be extended to the gigabit scale and beyond because the thickness of the traditionally used native oxide SiO_2 has approached the physical limits of minimum thickness (~1.5 nm). Therefore, finding an alternative to SiO_2 is an enormous challenge for the materials, device and integration research community.

Since conventional gate oxide poses problems as device features are scaled down, it becomes necessary to develop new gate dielectric materials with properties similar to SiO_2 and compatible with current complementary metal oxide semiconductor technology (Manchanda et al. 2001). These materials should meet the following fundamental and practical requirements:

(a) dielectric constant higher than that of silicon dioxides (K=3.9),
(b) thermodynamic stability on silicon,
(c) amorphous after device integration,
(d) low conduction for low leakage (tunneling current less than 10 mA/cm^2) and low power consumption,
(e) high carrier mobility at the dielectric/Si interface. Therefore, low interface state density (D_{it}) ($< 2 \times 10^{11}$ cm^{-2} eV^{-1}),
(f) high breakdown strength and acceptable reliability,
(g) wide band gap,
(h) negligible hysteresis in capacitance-voltage curves.

At this point, high dielectric constant insulating layers have become important to replace the native silicon dioxide used for the gate dielectric of DRAMS. The use of

high-k dielectrics will make it possible to achieve similar charge storage density as conventional dielectrics at relatively larger thicknesses. Many high dielectric constant materials have been reported that could potentially replace SiO_2. These include SiO_xN_y, Ta_2O_5, TiO_2, Y_2O_3, CeO_2, Al_2O_3, La_2O_3, $SrTiO_3$, (Ba,Sr) TiO_3 and silicates of hafnium and zirconium which enable an increase of the packing density of devices without a further reduction of insulator thickness (Manchanda et al. 1998, Chin et al. 2000, Wilk et al. 2000, Albertin et al. 2003, Dwivedi et al. 1998, Han et al. 2003, Suvorova et al. 2003, Mikhelashvili and Eisenstein 2000, Atanassova 1999, Chaneliere et al. 1998 and references there in (7-14)). These materials exhibit the desired high dielectric constants for applications as gate dielectrics in sub 100 nm silicon technology. However, detailed studies need to be performed to evaluate the compatibility of these materials with the rest of the silicon integrated circuit manufacturing processes.

Among all the candidates, Ta_2O_5 layers have received considerable attention because of their potential application as dielectric films for storage capacitors in high density DRAMs (Kim 2000) ,due to the relatively high dielectric constant (20-40) (depending on deposition conditions), high refractive index and adequate dielectric breakdown strength (~10^6 V/cm) (Dimitrova and Atanassova 1998a, Atanassova 1999). Historically, Ta_2O_5 was first studied at 1970's because of its promising properties as an antireflective layer for optical or photovoltaic applications. In the following decades, studies have been focused on the ways of obtaining stable oxide layers and their potential applications. However, the real emergence of tantalum pentoxide as dielectric material happened during the last decade mainly because of an exceptional effort in the development of electronics devices using tantalum oxide films as dielectric layers (Chaneliere et al. 1998, Ezhilvalavan and Tseng 1999). Also, these studies have been motivated by the dramatic scaling down of silicon integrated circuits that has pushed conventional dielectric films close to their physical limit in terms of reduction of thickness and dielectric strength.

Tantalum pentoxide (Ta_2O_5) has useful optical and dielectric properties. It is a fairly stable oxide with an orthorhombic or hexagonal structure, a melting point of 1870 °C and a density of 8.27 g cm^{-3} (Pierson 1992). It is moderately hard with a Vickers hardness of 1400 kg mm^{-2}. It has a refractive index of 2.1-2.2. It is an electrical insulator with a high dielectric constant (25-35). In addition, Ta_2O_5 films find applications in various fields such as dielectric for storage capacitors, gate insulators in metal-oxide-semiconductor (MOS) devices, insulating layer in thin film electroluminescent devices,

sensitive layer in biological and chemical sensors, optical coatings, anti-reflection coatings and coatings for hot mirrors (Ezhilvalavan and Tseng 1999).

The properties of Ta_2O_5 layers depend on stoichiometry, microstructure (grain size distribution), film thickness, characteristics of electrode and homogeneity of the film. Ta_2O_5 film growth method significantly affects above parameters and consequently its dielectric properties. A variety of techniques such as RF magnetron sputtering, reactive sputtering, thermal oxidation, Chemical Vapour Deposition (CVD) (excimer laser assisted, low temperature, low pressure, photo, plasma, electron cyclotron resonance (ECR), Atmospheric Pressure, metal organic (MOCVD), Liquid source), vacuum evaporation, atomic layer deposition, sol-gel method and ion assisted deposition have been examined and used to deposit best quality Ta_2O_5 insulating layers (Liu et al. 2004, Boughaba et al. 2000, Zhang et al. 1998, Four et al. 1999, Mooney at al. 1999, Boyd and Zhang 2000, Duenas at al. 2000, Atanassova and Spassov 1998, Atanassova and Spassov 2002, Atanassova 1999, Atanassova and Spassov 1998, Atanassova and Spassov 2002, Ezhilvalavan and Tseng 1999, Chaneliere et al. 1998, and references there in). Regardless of the method by which they are formed, however, the process must be economical and the resultant films must exhibit the following characteristics; good thickness uniformity, high purity and density, controlled composition stoichiometries, high degree of structural perfection, good electrical properties, excellent adhesion and good step converge.

After deposition, the physical, structural, optical, chemical and electrical properties of tantalum pentoxide films on silicon have been studied in detail (Chaneliere et al. 1998, Ezhilvalavan and Tseng 1999 and references there in). The characteristics of the insulating layers have been examined by using the methods; X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), secondary ion mass spectrometry (SIMS), Fourier transform infrared (FTIR) absorbance, Capacitance-Voltage (C-V) Spectroscopy and Conductance Spectroscopy.

X-ray diffraction (XRD) and structural analyses show that, tantalum pentoxide has a crystalline or an amorphous structure depending on its deposition temperature. It is confirmed that the Ta_2O_5 films annealed below 600 °C do not show any notable crystallization and the crystallization temperature of Ta_2O_5 film grown by reactive sputtering lies between 650 °C and 700 °C (Kimura et al. 1983). The results were also consistent with other reports for anodically or thermally grown Ta_2O_5 film (Harvey and Wilman 1961). More recently, another study reported similar crystallization behavior of

Ta_2O_5 films deposited by LPCVD process (Chiu et al. 1997). It is therefore clear that the crystallization temperature of Ta_2O_5 film does not depend on the method by which the film is grown. Crystalline tantalum pentoxide presents principally two phases; an orthorhombic phase and a hexagonal phase.

The optical properties such as the optical bandgap of tantalum pentoxide were determined by transmission and absorption spectroscopy (Burte and Raush 1995). From transmittance measurements, the bandgap value was found to be 5.28 eV for amorphous films. From absorbance measurements, values ranging from 4.2 to 4.4 eV for amorphous films and 3.9 to 4.5 eV for crystalline films were obtained. Tantalum pentoxide is transparent in the near UV spectral region ($\lambda > 300$ nm), which is an important point for optoelectronic devices that operate in the ultraviolet, such as astronomical charge-coupled device (CCD) imagers and space based photovoltaic devices.

Electrical characterization results show that, the dielectric constant value obtained for tantalum pentoxide depends upon the sample characteristics and the experimental preparation method. It has also been demonstrated that the dielectric constant of Ta_2O_5 layers shows thickness dependence, the dielectric constant decreases significantly with decreasing the Ta_2O_5 layer thickness (Atanassova 1999). The dielectric permittivity of amorphous Ta_2O_5 was found to be in the range 22-28 (Kukli et al. 1995, Devine et al. 1996). But values up to 40 have been reported for non-amorphous Ta_2O_5 films (Nakagawa and Okada 1990). Recent studies have shown that the dielectric constant can be as high as ~60 for crystalline Ta_2O_5 on Si (Chaneliere et al.). Crystalline Ta_2O_5 exhibits a higher dielectric constant than amorphous Ta_2O_5. Moreover, the crystalline phases of tantalum pentoxide show an anisotropic character. Depending upon the crystal orientation, the dielectric constant could vary over a wide range, which would result in uncertainty in the capacitance per unit area if used to produce capacitors. The crystallographic orientation dependence of Si substrates on the dielectric constant of Ta_2O_5 was reported by Seki et al. (Seki et al. 1984). They have noticed that for each substrate, the dielectric constant of deposited Ta_2O_5 increases monotically with its thickness and there was a dependence of the dielectric constant on the substrate orientation. Therefore, an amorphous structure is needed for microelectronics applications, unless the crystal orientation can be controlled in order to obtain the same characteristics from one component to another.

As another issue, the effect of oxidation on the dielectric constant of the Ta_2O_5 films was reported by some researchers (Atanassova et al. 2002a, Atanassova et al. 2002b, Park and Im et al. 1992). They showed that the dielectric constant obtained from an Al-Ta_2O_5-Si capacitor depends on the thickness of the oxide and increases with increasing oxidation temperature.

Another important parameter that affects the dielectric constant of Ta_2O_5 is the formation of an inevitable thin transition layer (in general SiO_2). This thin oxide may drastically reduce the dielectric constant of the system since the dielectric constant of SiO_2 is equal to 3.9, which is about 6 times lower than for amorphous Ta_2O_5. The global dielectric constant of the Ta_2O_5-SiO_2 system can be evaluated by using a simple model which supposes that the two dielectric layers are represented by two capacitors in series with the dielectric constant of silicon dioxide and tantalum pentoxide respectively. The effective dielectric constant of the sandwich (ε_{eff}) is then given by the following equation:

$$\varepsilon_{eff} = \frac{(d_s + d_t)\varepsilon_s \varepsilon_t}{d_t \varepsilon_s + d_s \varepsilon_t} \tag{1.1}$$

where d_s and d_t are the thicknesses of SiO_2 and Ta_2O_5 respectively, and ε_s and ε_t are the dielectric constants of SiO_2 and Ta_2O_5 respectively. For example, if we consider 2 nm of SiO_2 and 15 nm of Ta_2O_5, the effective dielectric constant will be equal to 15.6, substantially lower than the ideal value of ε_t for pure amorphous Ta_2O_5 (ε_t ~26).

In addition, the non-ideal effects such as charges localized inside the oxide layer and at the silicon-insulator interface are of great importance. In the ideal metal-oxide-semiconductor (MOS) system, the oxide layer is assumed to be free of charges, and the insulator-semiconductor interface is assumed to be perfect. However, the deposition conditions, type and the environment causes non-ideal effects in the MOS structure by localizing charges inside the oxide layer or by creating interface trap states at the insulator-silicon interface. The electrically active defects localized in the insulator or at the insulator-semiconductor interface lead to the presence of the following different charges:

(a) oxide trapped charges which are due to electrons and holes trapped in the bulk of the insulator,

(b) mobile ionic charges which are due to ionic impurities present in the bulk of the insulator,

(c) fixed oxide charges which are due to structural defects localized in the insulator, near the insulator-semiconductor interface, and

(d) interface trapped charges due to holes and electrons captured by trapping centers localized at the insulator-semiconductor interface.

The total of the oxide charges present in the oxide layer (the fixed oxide charges, mobile ionic charges and oxide trapped charges) is called as the effective oxide charge and it is represented by Q_{eff}, and the density of interface trap states caused by the lattice mismatch problem between Ta_2O_5 and silicon is represented by D_{it}. The level of Q_{eff} and D_{it} are determining the conduction mechanism through the oxide layer and are directly related with the quality of the device. For example, interface trap states captures charges from the silicon thus, lowering the total capacitance of the system. For this reason, it is crucial to evaluate the number of these charges and the resultant value must be kept as low as possible by optimizing the deposition conditions for the best device performance. There are many studies done for the determination of the level of these charges (Dimitrova and Atanassova 1998a, Dimitrova and Atanassova 1998b, Novkovski et al. 2005, Spassov et al. 2000, Atanassova et al. 2002a, Atanassova and Paskaleva 2002, Atanassova 1999, Ozdag et al. 2005). For the as-deposited samples values up to ~10^{12} $eV^{-1}cm^{-2}$ have been reported. However this level is quite high when compared with the level present in the conventional SiO_2-Si system (~10^{10} $eV^{-1}cm^{-2}$). For this reason, researchers are now focused on the pre- and post-deposition methods such as rapid thermal annealing or rapid thermal nitridation which can enable a decrease on the level of effective oxide charge and interface trap states as low as ~10^{11} $eV^{-1}cm^{-2}$.

Concerning the leakage current density, common values are below 10^{-6} and 10^{-7} A/cm^2 under an applied electric field up to 3$MVcm^{-1}$ (Atanassova and Paskaleva 2003, Paskaleva et al. 2000, Chaneliere et al. 1998). However, these results greatly depend on the deposition methods and parameters like temperature, pressure etc., and on the pre- and post-deposition annealing treatments like annealing technique, gases employed, duration and temperature, presence of an interfacial layer and nature of this layer, which strongly influence the level of leakage current by playing an important role on the quality of the tantalum pentoxide layer. In addition, two main conduction mechanisms, Schottky emission and Poole-Frenkel effect were studied to explain the current transport

in tantalum pentoxide thin films (Atanassova and Paskaleva 2002, Chaneliere et al. 1998).

Chemical analyses result in that tantalum pentoxide is highly resistant to many chemicals depending upon its preparation technique and can in fact be employed as a protective coating material against corrosion.

Even tough so much work has been done on Ta_2O_5, its not completely understood yet. Although Ta_2O_5 is now in the closest position to practical application, process optimization and detailed reliability data of this material need to be established before it can be confidently accepted into mass production and successfully integrated into full fabrication process of microelectronics devices.

1.1 Thesis objective

The objective of this thesis is to examine the electrical characteristics of Ta_2O_5 insulating layers in detail because of its promising properties to replace the native silicon dioxide used for the gate dielectric of DRAMS. The most fundamental device structure for investigation of nearly all the electrical properties of a dielectric material is the metal-oxide-semiconductor (MOS) structure. In this thesis, Ta_2O_5 insulating layer deposited under different preparation conditions on a p-type Silicon (Si) substrate are used to form metal-oxide-semiconductor (MOS) capacitors. Electrical properties of the MOS capacitors are studied in detail using capacitance-voltage (C-V) spectroscopy at 1 MHz. Conductance-voltage and current-voltage measurements were also performed to obtain additional information about the devices.

Using the theory of ideal MOS capacitors, theoretical capacitance-voltage characteristics have been calculated using a computer program. Experimental high frequency capacitance-voltage curve of each sample was compared with the ideal curve of the same sample. Dielectric constant of insulating layer, doping concentration of substrate, flat band voltages, maximum and minimum capacitance values, trapped oxide charges and interface trap density present at Si-Ta_2O_5 interface have been derived from the ideal and experimental high frequency C-V curves. Detailed calculations proposed in the Terman's method were used to calculate the interface trap density present in the band gap of crystalline silicon. The results of MOS capacitors with different Ta_2O_5

insulating layers were compared with a reference sample, which has a native SiO_2 layer with a standard electronic property.

In order to understand the electronic quality of Ta_2O_5 insulating layers deposited on Si substrate and interface quality of Si-Ta_2O_5, two different approaches have been carried out. First, Ta_2O_5 insulating layers were directly deposited on the polished p-type substrate using the magnetron sputtering method with different thickness values. In the second approach, rapid thermal nitridation process under N_2O and NH_3 gas environment has been carried out on the polished p-type silicon substrate. Then, 20 nm thick Ta_2O_5 insulating layers were deposited on the nitrided surface of p-type silicon substrate. Finally, metal (Al) electrodes were evaporated to form the MOS capacitors. Eventually, devices were tested and detailed characterization of devices has been carried out using capacitance-voltage spectroscopy and results were compared with those obtained from the reference MOS capacitor with native oxide SiO_2.

CHAPTER 2

EXPERIMENTAL

2.1 Sample Preparation

The samples that are used in this study are prepared in the form of Al-Ta_2O_5-Si MOS capacitors by using three different deposition methods for each layer present in the structure. The substrate is prepared by using Czochralski method, and then the oxide layer is formed by using the RF-magnetron sputtering method. Finally metal electrodes are formed by using thermal evaporation technique. The samples are deposited at Institute of Solid State Physics, Bulgarian Academy of Sciences, in Sofia, Bulgaria. The schematic view of three groups of samples that are used in this study can be seen in Figure 2.1.

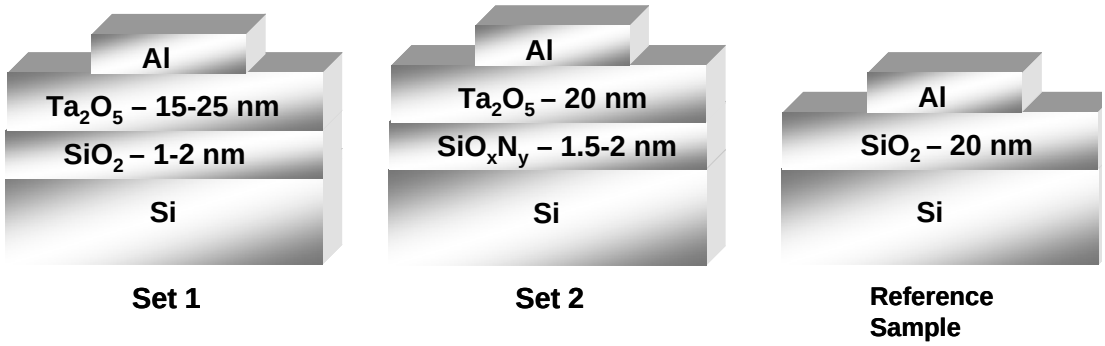

Figure 2.1 Schematic view of MOS structures that are used in this study

Czochralski method is a technique that is used in making single crystal silicon. A 2-3 mm diameter silicon seed crystal is rotated and lowered into a bath of molten Silicon (T> 1400 °C). Because of the temperature difference, some of the melt freezes onto the seed. Finally, the solid seed crystal is rotated and slowly extracted from the pool of molten Si. This method requires a careful control to give crystals desired purity and dimensions. The seed can be sliced into hundreds of smaller pieces that are called wafers and each wafer yields hundreds or thousands of integrated circuits. Depending on the purpose, silicon can be doped during the deposition. In this study, p type

crystalline Si that is formed by doping Si with Boron atoms is used as the substrate part of the MOS structure.

For sample Set 1, tantalum pentoxide films with thicknesses of 15 – 25 nm were deposited on p-type (100), 15 Ωcm Si, by RF magnetron sputtering from a tantalum target in an Ar atmosphere. The system base pressure was $6x10^{-4}$ Pa, the working gas pressure 3 Pa, the RF power density 2.2 W/cm^2, the deposition rate, ν = 9.3 nm/min, and the substrate temperature Ts = 300K. After the deposition, the Ta films were oxidized in dry oxygen at atmospheric pressure at 873 K with an O_2 flow rate of 5.1 min^{-1}. The thickness t_{ox} of the Ta_2O_5 layers was measured by ellipsometry (λ = 632.8 nm) and layers with t_{ox} = 15, 20 and 25 nm were investigated. For the electrical characterization, MOS capacitors were fabricated by evaporation of Al dots with a thickness of 500 nm, through a shadow mask with a gate electrode area of $1.96x10^{-3}$ cm^2. For this group, post metallization annealing was carried out in H_2 at 723 K for 1h.

For sample Set 2, tantalum pentoxide layers of 20 nm were deposited on p-type (100), 3-5Ωcm Si wafer by using RF magnetron sputtering in O_2 gas environment. Before the deposition of Ta_2O_5, a rapid thermal nitridation (RTN) process is applied for 10 seconds in a clean room of class 10 in Germany by using N_2O and NH_3 gases in the temperature range between 700-850 °C. After RTN, a silicon oxynitride layer of thickness ~1.5 nm was detected at the Si surface. The deposition of Ta_2O_5 insulating layer is carried out by using RF-magnetron sputtering technique. However, in this case formation of Ta_2O_5 is directly obtained during sputtering process with a Ta target in an oxygen rich environment. Hence, sputtered Ta atoms react with oxygen and form Ta_2O_5 insulating layer on the substrate. The substrate temperature is held at 220 °C. Lastly, Al electrodes are evaporated with four different gate areas such as $S_1= 2.5x10^{-3}$ cm^2, $S_2= 6.25x10^{-4}$ cm^2, $S_3= 2.25x10^{-4}$ cm^2 and $S_4= 1x10^{-4}$ cm^2, for the examination of the changes in the capacitance and the dielectric constant depending on the capacitor area.

Finally, a reference sample of Al-SiO_2-Si is prepared by thermal oxidation of SiO_2 on p-silicon to compare electrical properties of high dielectric constant insulators with that of conventional oxides.

There are mainly two sets of Ta_2O_5 MOS capacitors with or without nitridation process and a sample of SiO_2 MOS capacitor as a reference conventional oxide that are used in this study. The detailed information about the process conditions of the samples are given in the Table 2.1.

Table 2.1 Deposition parameters of MOS structures used in this thesis

Set 1- Rf Magnetron Sputtered Ta_2O_5 Without Nitridation					
Sample Name	Composition	RTN Process		t_{ox} (nm)	Area (cm^2)
N 3	Al- Ta_2O_5-(SiO_2)-Si	-		15	$1.96x10^{-3}$
N 6	Al- Ta_2O_5-(SiO_2)-Si	-		20	$1.96x10^{-3}$
N11	Al- Ta_2O_5-(SiO_2)-Si	-		25	$1.96x10^{-3}$
Set 2- Rf Magnetron Sputtered Ta_2O_5 With Nitridation					
Sample Name	Composition	RTN Process		t_{ox} (nm)	Area (cm^2)
RN 1	Al-Ta_2O_5-(SiO_xN_y)-Si	N_2O	700 °C	20	$2.5x10^{-3}$-$1x10^{-4}$
RN 2	Al-Ta_2O_5-(SiO_xN_y)-Si	N_2O	800 °C	20	$2.5x10^{-3}$-$1x10^{-4}$
RN 3	Al-Ta_2O_5-(SiO_xN_y)-Si	N_2O	850 °C	20	$2.5x10^{-3}$-$1x10^{-4}$
RN 4	Al-Ta_2O_5-(SiO_xN_y)-Si	NH_3	700 °C	20	$2.5x10^{-3}$-$1x10^{-4}$
RN 5	Al-Ta_2O_5-(SiO_xN_y)-Si	NH_3	800 °C	20	$2.5x10^{-3}$-$1x10^{-4}$
Reference Sample – Thermal SiO_2					
Sample Name	Composition	RTN Process		t_{ox} (nm)	Area (cm^2)
SiO_2	Al-SiO_2-Si	-		20	$1.96x10^{-3}$

2.1 Characterization Techniques

In this section, the experimental method of Capacitance-Voltage Spectroscopy used for the electrical characterization of MOS devices will be explained in detail.

2.2.1 Capacitance Voltage (C-V) Spectroscopy

This method is a fast and accurate method in the determination of electronic quality of MOS devices. It is the first time that this experimental setup, Model 82-DOS Simultaneous C-V System, is established as one of the main goal of this thesis. The experimental setup is shown in Figure 2.2. Model 82-DOS is a computer controlled system of instruments designed to make simultaneous C-V, quasistatic C-V and high frequency (1 MHz) C-V measurements on MOS capacitors. The system includes a Keithley 590 C-V Analyzer for high frequency C-V measurements, and a Keithley 595 Quasistatic C-V Meter for low frequency C-V measurements. Additionally, Keithley 230 Programmable Voltage Source and Keithley 5951 Remote Input Coupler are used to apply voltage and control the communication between the instruments and the computer. A Keithley IEEE 488 Interface card is used to provide General Purpose Interface Bus (GPIB) communication between the instruments and the computer. Software package called Model 82-DOS is used for the control of the experimental setup, data collection and acquisition.

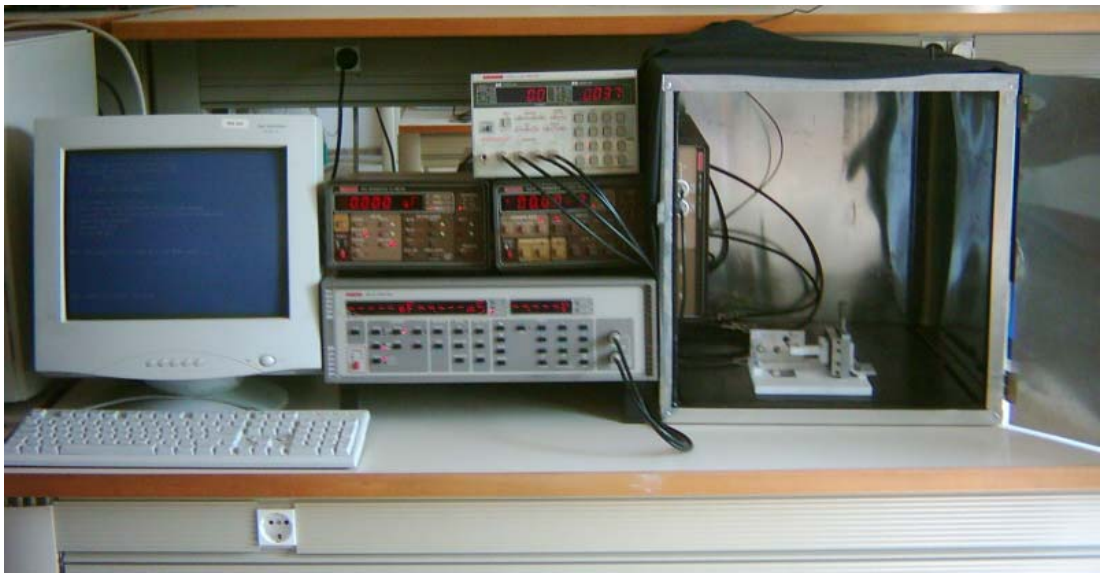

Figure 2.2 Simultaneous Capacitance-Voltage (C-V) Setup

After making necessary connections between the instruments and the computer by using the system block diagram provided in the users' manual, the software is installed by using the disks provided by Keithley. If the system is newly established or a new system configuration is present, there are some necessary steps that have to be done before beginning to the measurement. First of all, leakage current, stray capacitance detection and cable correction by using correction capacitors supplied by Keithley should be performed according to the steps explained in the manual. Later, the necessary modifications must be done on "Material.con" file for the constants defined for the sample studied, because the software is prepared for Al-SiO_2-Si MOS structure. For example, the dielectric permittivity of Ta_2O_5 is rewritten in the file for the place of dielectric permittivity of SiO_2 etc.

For the measurement, the sample is placed in a homemade sample box which is made up of aluminum metal to constitute a Faraday cage. It is important to place the sample in a Faraday Cage where the electric field vanishes inside, because of the sensitiveness of the measurement method which is based on the measurement of the charge or the capacitance versus applied voltage. In addition, the Faraday Cage must be lightproof, since the high quality MOS capacitors are excellent light detectors. The connections (gate and substrate) of the sample to the system are provided by using a homemade and designed probe station with micro manipulators to permit precise motion of the probe wire in two mutually perpendicular directions on the wafer. The probe wire used for the connection of gate is chosen to be gold to provide a good contact. The gold wire is sharpened by the process of electrolysis and sanding to be able to use it for smaller gate contact areas. This design with micro manipulators allows the measurement of different dots on the same wafer which is necessary for the reliable data collection. The contacts are placed on the sample under the optical microscope, which allows the choice of a good contact area. Finally, the sample holder is placed into the Faraday Cage for the measurement.

After placing the sample inside the Faraday Cage, the first step is to run a diagnostic C-V sweep to determine device parameters and to check to see that proper start and stop voltages have been programmed for the accumulation and inversion of the curve. The main menu of the software is shown in Figure 2.3.

By selecting option 3 in the main menu, it is possible to reach the sub menu for the diagnostic C-V measurement which is shown in Figure 2.4.

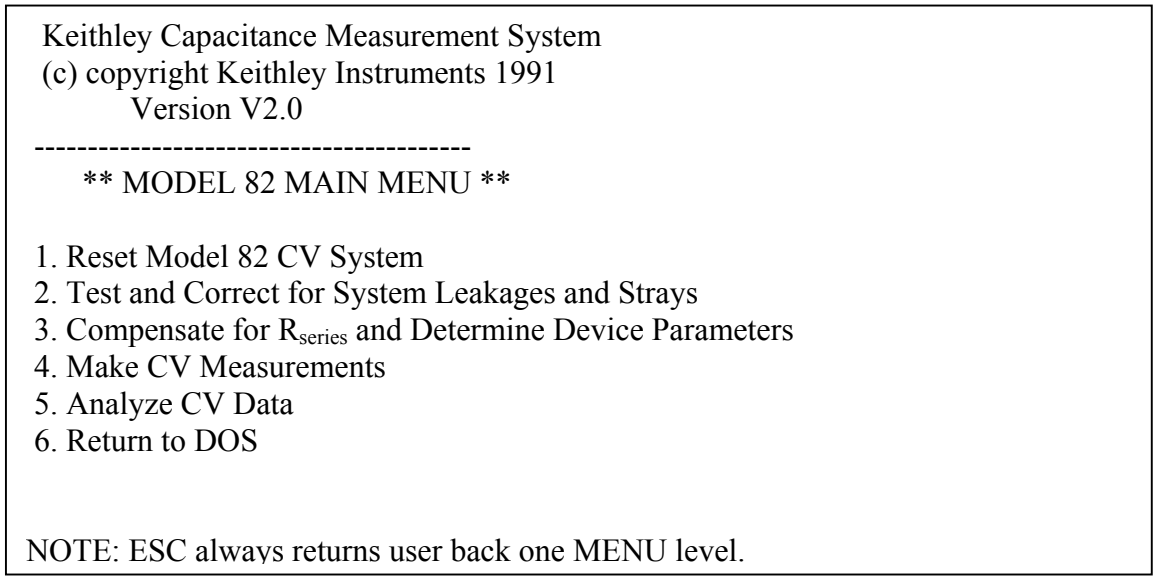

Figure 2.3 Model 82 Main Menu

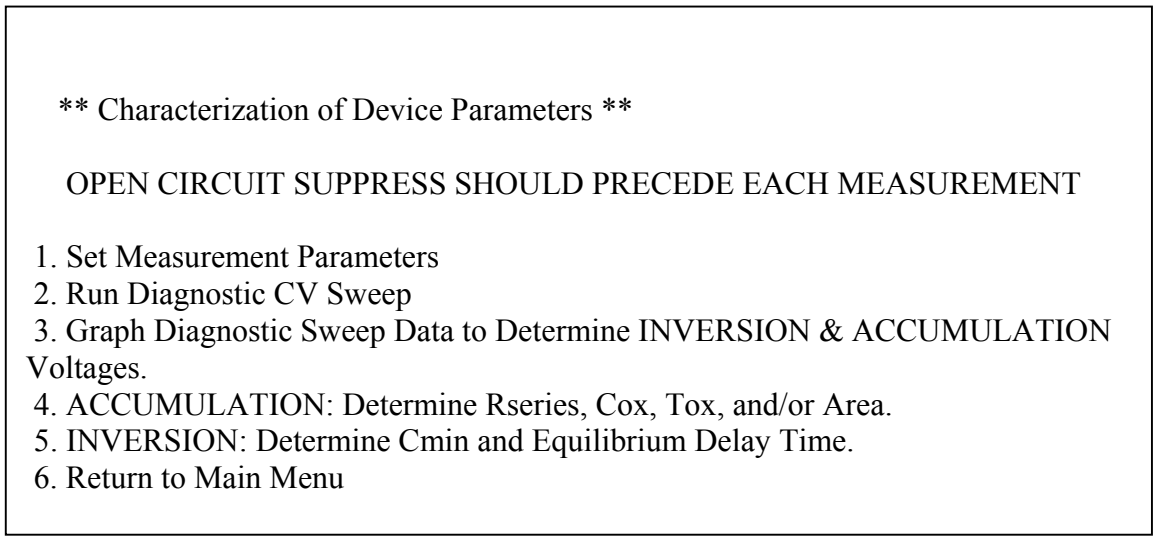

Figure 2.4 Characterization of device Parameters Menu

Before starting the measurement, the most important thing is to set measurement parameters, such as start and stop voltages, delay time, step voltage etc. by selecting option 1 in Figure 2.4. Measurement parameter list is shown in Figure 2.5.

After setting the measurement parameters, it is possible to start the diagnostic C-V sweep. At the end of the sweep, a graph of capacitance versus voltage is plotted. A typical C-V graph can be seen in Figure 2.6. If the sample shows desired capacitance voltage characteristics, then by biasing the sample into accumulation and inversion, important device parameters such as series resistance, oxide capacitance, area or

thickness, minimum capacitance and optimum delay time can be determined using options 4 and 5 in parameters menu shown in Figure 2.4.

** Measurement Parameter List **

Range:	2	Enter R1 for 200pF, R2 for 2nF
Freq :	2	Enter F1 for 100KHZ, F2 for 1MHZ
Model:	1	Enter M1 for parallel, M2 for series
Start V:	2.00 V.	Enter An, -120 <= n <= 120
Stop V:	-2.00 V.	Enter On, -120 <= n <= 120
Bias V:	0.00 V.	Enter Bn, -120 <= n <= 120
TDelay:	0.07 sec.	Enter Tn, 0.07 <= n <= 199.99
Step V:	20 mV.	Enter S10, S20, S50 or S100
CCap:	1	Enter C1 for leakage correction off, C2 for on
Filter:	2	Enter I1 for filter off, I2 for on

Number of samples = 93 Sweep will take = 0.4 minutes.

NOTE: 1) Keep start V and stop V within 40 volts of each other.
2) Keep number of samples within 4 and 1000 points with filter off.
3) Keep number of samples within 50 and 1000 points with filter on.

Figure 2.5 Measurement parameter List Menu

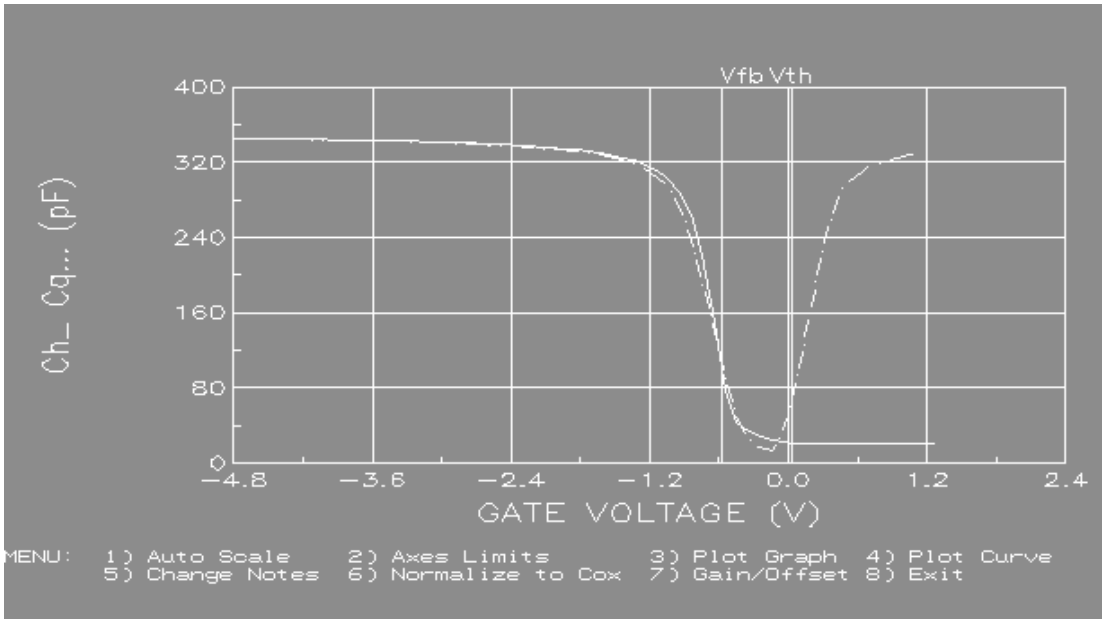

Figure 2.6 High and Low frequency C-V graphics of a MOS device.

Once the optimum device parameters are obtained, it is possible to run a real C-V sweep by selecting option 4 in Figure 2.3. In this case the sub menu for the C-V measurement is shown in Figure 2.7. By selecting option 2 in Figure 2.7, a C-V sweep can be started manually.

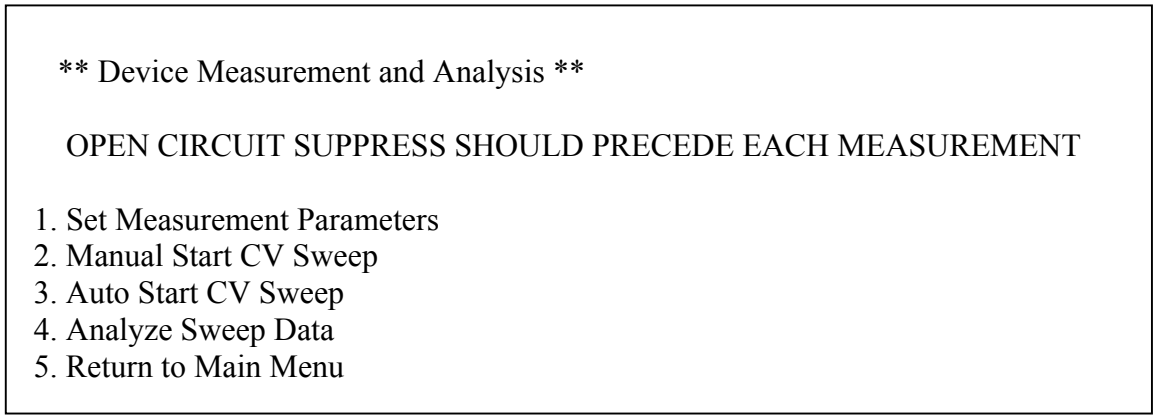

Figure 2.7 Device Measurement and Analysis Menu.

Before starting the measurement, again measurement parameters can be redefined depending on the purpose. For example, step voltage can be chosen as small as possible (10 mV) in order for the program to take as many data points as possible for the reliability of the analysis. At the end of the sweep, option 4 in Figure 2.7 can be chosen for the analysis of the sweep data. The graphs that the software can plot are seen in Figure 2.8 and the analyses are explained in detail in the users' manual.

By using menu in Figure 2.8, the data array can be saved to a file and the graphs can be plotted. However, there is an important point to be careful about the analysis. The software uses both high and low frequency C-V results for the determination of some parameters such as density of Interface trap states (D_{it}). Nevertheless, low frequency C-V measurements of high dielectric constant insulators are a rather difficult task. It should be noted that low frequency C-V characteristics obtained by the ramp voltage or the feedback charge-voltage method have not been successfully investigated for Ta_2O_5 capacitors. This can be explained by the fact that the leakage current is higher than the displacement current for most gate voltages. For this reason, by using the data file obtained at the end of the C-V measurement and by using Terman's method defined for MOS devices, interface trap density value can be analyzed manually. The detailed information about the analysis and the physics of MOS devices will be explained in the next chapter.

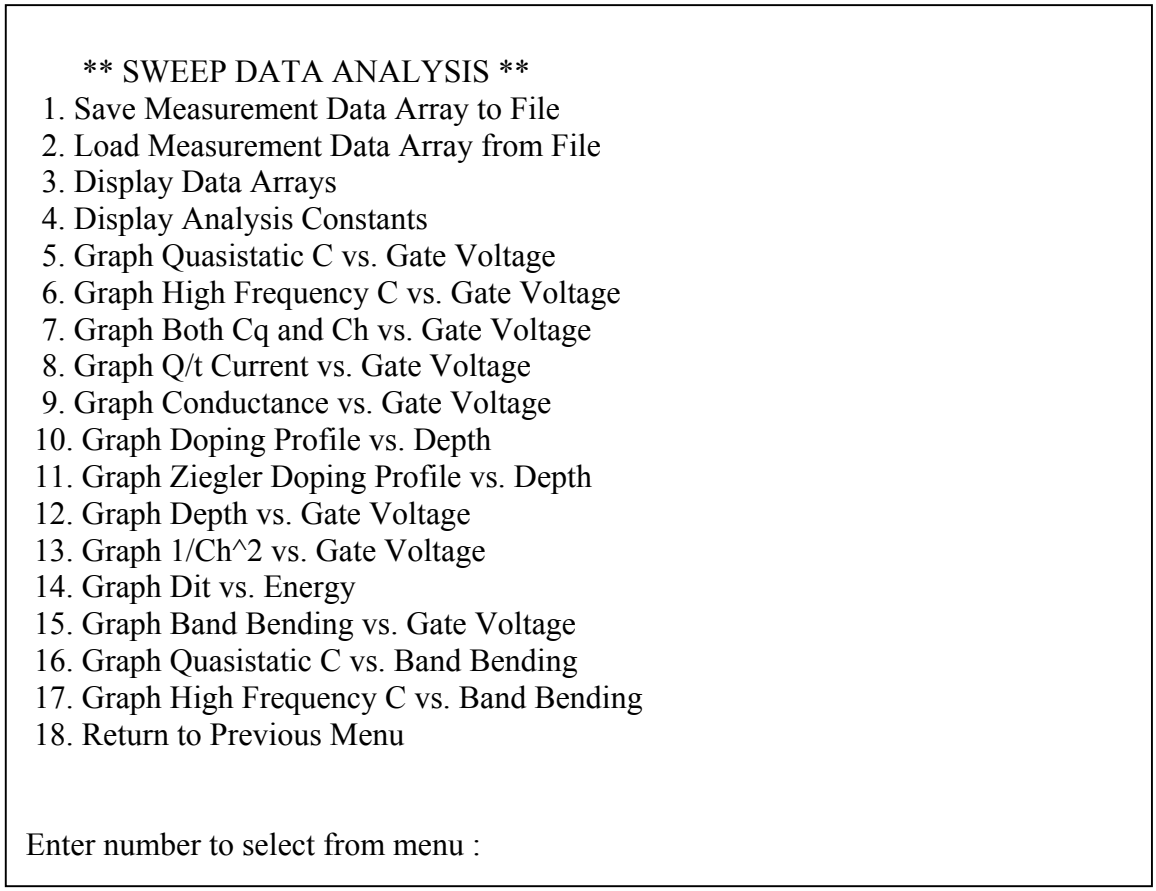

Figure 2.8 Sweep Data Analysis Menu.

The dielectric constant, doping concentration and flat band voltage values were determined from the experimental high frequency C-V curves. Theoretical ideal C-V characteristics were calculated using a computer program and equations defined for MOS devices. The effective oxide charge density, Neff, and the density of interface defect states, Dit, were calculated from the high frequency C-V curves using Terman's method.

CHAPTER 3

PHYSICS OF MOS DEVICES AND ANALYSIS

3.1 Ideal Metal-Oxide-Semiconductor (MOS) Energy Band Diagrams

Metal-oxide-semiconductor (MOS) capacitor is one of the important solid state devices. It is constructed using a p-type or n-type single crystalline semiconductor wafer as substrate. An oxide layer is formed using different deposition methods and finally metal electrode is evaporated on top of the device, which is also called gate electrode. Other end of the substrate has an ohmic contact. In general, a silicon wafer is used for the substrate and native oxide SiO_2 is formed by using dry or wet oxidation process. Finally, aluminum gate electrode is evaporated to complete device fabrication. Cross-section of Metal-Oxide-Semiconductor structure is shown in Figure 3.1, where V_G is the applied gate voltage. For the ideal MOS capacitor, both the oxide and the oxide-semiconductor interface are assumed to be free of charges and defect states. Depending on the polarity and magnitude of the applied gate voltage, the carrier concentration and band structure of semiconductor changes resulting in different electrical characteristics of the MOS capacitor. In general MOS capacitor operates at three different bias conditions.

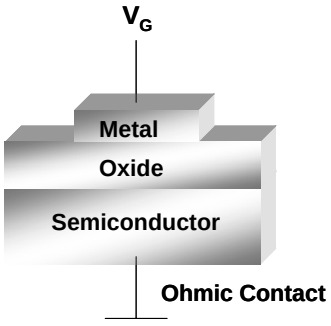

Figure 3.1 Ideal MOS Structure with applied gate voltage V_G

When $V_G = 0$, the structure is in thermal equilibrium. At this condition, the energy band diagram of a MOS structure with a p-type substrate is shown in Figure 3.2, where ϕ_m is

the metal work function, χ_i is the electron affinity of insulator, χ is the electron affinity of semiconductor, E_g is the energy gap of semiconductor, ϕ_B is the potential difference between the metal Fermi level and conduction band of the insulator, ψ_B is the potential difference between the intrinsic Fermi level (E_i) and Fermi level (E_F) inside the bulk, E_C is the conduction band and E_V is the valance band of the semiconductor. The importance of these energy barriers is that they prevent the free flow of carriers from the metal to the silicon or vice versa. Thus the application of a bias across the MOS capacitor does not result in current flow. Rather, an electric field is established in the oxide by surface charge layers that form in the metal and on the silicon-oxide interface.

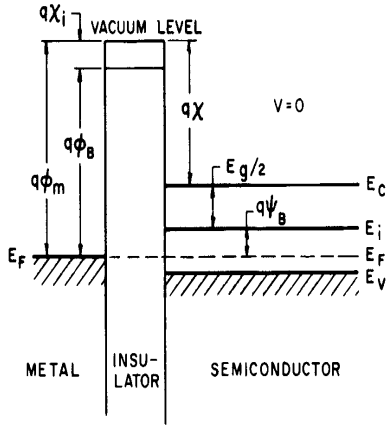

Figure 3.2 Energy-Band diagram of ideal MOS structure in thermal equilibrium constructed from a p-type semiconductor substrate

Depending on the parameters defined above, an ideal MOS structure can be explained as follows:

(a) When the applied gate voltage V_G = 0, then the work function difference ϕ_{ms}, between the semiconductor ϕ_s and the metal ϕ_m becomes zero, which means the energy bands are flat. Then from Figure 3.2, the work function difference can be written as follows:

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - (\chi + \frac{E_g}{2q} + \psi_B) = 0 \qquad (3.1)$$

(b) When a gate voltage $V_G \neq 0$ is applied to an ideal MOS structure, the charges are distributed at the semiconductor-insulator or metal-insulator interface with equal amount and opposite polarities,

(c) It is assumed that under applied gate voltage V_G, there is no charge transfer throughout the insulator, which means that it has an infinite resistance.

When a positive or negative gate voltage is applied to an ideal MOS structure, there are mainly three working conditions present in the semiconductor:

(1) Accumulation: When a negative voltage V_G is applied to metal terminal of MOS structure, the metal part becomes negatively charged and the semiconductor part becomes positively charged**,** then there occurs an internal electric field in the direction of upwards from semiconductor to metal. This electric field piles up holes of p-type semiconductor to the semiconductor-oxide interface, where an accumulation region of holes is obtained. The change in the free carrier concentration at the interface also changes the band diagram of semiconductor at the interface as shown in Figure 3.3. Free electron, n, and hole, p, concentrations of semiconductor at the oxide-semiconductor interface are explained as:

$$p = N_V \exp[-(E_F - E_V)/kT]$$
$$n = N_C \exp[-(E_C - E_F)/kT] \qquad (3.2)$$

where E_F is the Fermi level energy, E_V is the valance band energy and E_C is the conduction band energy. As the hole concentration (p) increases at the interface, E_F-E_V term must decrease. Therefore, the valance band, conduction band and intrinsic Fermi level bends up at the interface. The resulting band diagram and MOS structure in accumulation are shown in Figure 3.3. Then, MOS capacitor in this condition behaves like a parallel plate capacitor and system capacitance becomes equal to that of oxide capacitance, C_{ox}.

(2) Depletion: When a positive voltage V_G is applied to metal terminal of MOS structure, the metal part becomes positively charged and the semiconductor part becomes negatively charged**.** Then, there occurs an internal electric field in the direction of downwards from metal to semiconductor. Under the influence of the electric field holes at the interface of semiconductor are pushed towards the bulk silicon. At the oxide-semiconductor interface, majority carrier hole density decreases. This surface region is called “depletion region” or “space charge region”. Only ionized acceptor atoms fixed to the silicon network remain in the depletion region. They are negatively

charged. Similarly from Equation 3.2, the decrease of hole concentration at the interface causes an increase in (E_F-E_V), which results in the bands to bend down at the semiconductor-oxide interface. At this condition, cross section and energy band diagram of MOS capacitor are exhibited on Figure 3.4.

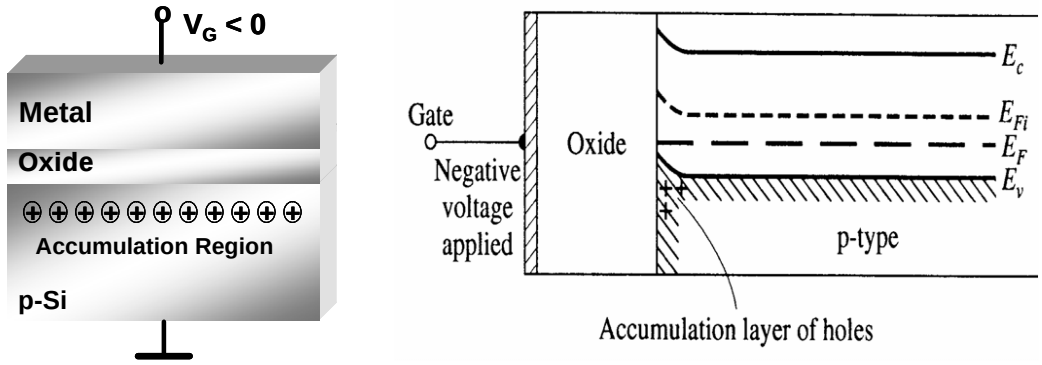

Figure 3.3 Cross-section and energy band diagram of MOS capacitor in accumulation region

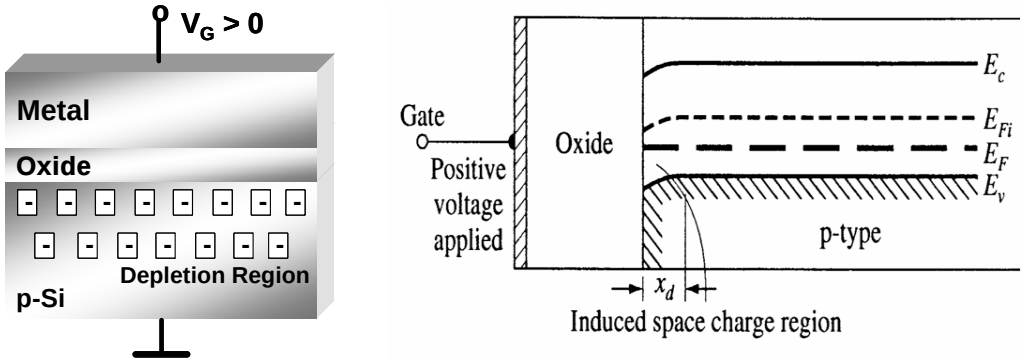

Figure 3.4 Cross-section and energy band diagram of MOS capacitor in depletion region

As we continue to apply positive gate voltages, bands continue bending down and conduction band E_C is getting closer and closer to the Fermi level E_F. At a certain point, electron concentration at the surface of the semiconductor becomes equal to the hole concentration inside the bulk of semiconductor, where intrinsic Fermi level E_i reaches to the Fermi level E_F. At this voltage value of V_G=V_T, surface of semiconductor behaves like an intrinsic semiconductor with equal electron and hole concentrations. This condition is called the **threshold** condition.

(3) Inversion: When voltages V_G higher than positive gate voltages, $V_G > V_T$, are applied to the metal terminal, minority carrier electrons in the bulk of p-type silicon are accelerated towards the semiconductor surface under strong electric field. In this case electron concentration at the surface becomes higher than the hole concentration in the bulk. As a result, energy bands continue bending down. Energy difference between E_C and E_F decreases and semiconductor surface behaves like n-type semiconductor according to Equation 3.2.

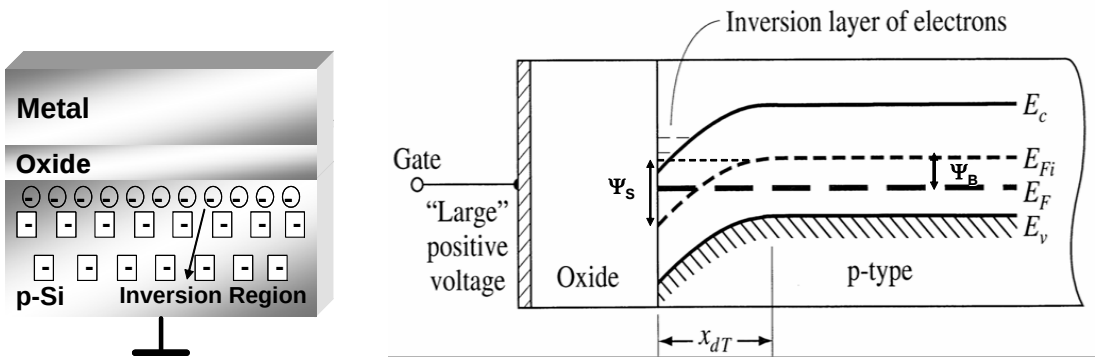

Figure 3.5 Cross-section and energy band diagram of MOS capacitor in inversion region

In order to describe three different cases defined above, two important controlling parameters in this structure are defined. These are the bulk potential ψ_B and the surface potential ψ_S respectively as given in Equation 3.3. Bulk potential is the potential difference between the intrinsic Fermi level and Fermi level inside the bulk, where surface potential is the potential difference between the intrinsic Fermi level inside the bulk and at the interface.

$$\psi_B = \frac{E_F - E_{ib}}{q} \qquad \psi_S = \frac{E_{ib} - E_{is}}{q} \tag{3.3}$$

where the internal parameter ψ_S can be controlled by the external parameter V_G as given in Equation 3.4. By applying a varying gate voltages V_G, the charge concentration at the surface of semiconductor is changed and hence the surface potential and the total capacitance of the system are changed accordingly. Similarly depending on the polarity of the applied gate voltage, the polarity of the surface potential changes.

$$V_G = V_{OX} + \psi_S \tag{3.4}$$

When applied voltage V_G changes from negative values to zero and to positive values, the sign and magnitude of charge on the silicon surface will change. Then this additional change will introduce a capacitance series with the oxide capacitance. The calculation of the total capacitance of the MOS system under different bias conditions will be explained in detail the following section of this chapter in detail.

3.2 Theoretical Capacitance of Ideal MOS Structure

Analysis of the behavior of small signal capacitance variation with bias voltage of a MOS capacitor provides further understanding of the electrical characteristics of the MOS system. The static and differential capacitances differ for the MOS capacitor because the charge on the MOS capacitor varies nonlinearly with the gate voltage. The differential capacitance per unit area can be written as:

$$C'_{diff} = \left| \frac{dQ'_{Si}}{dV_G} \right| \tag{3.5}$$

Similarly, the oxide potential can be written as:

$$V_{OX} = E_{OX} t_{OX} = \frac{\left| Q'_{Si} \right| t_{OX}}{\varepsilon_{OX}} = \frac{\left| Q'_{Si} \right|}{C'_{OX}} \tag{3.6}$$

Writing the oxide capacitance given in Equation 3.6 back in Equation 3.4, and rearranging for Equation 3.5 results in the following Equation;

$$\frac{1}{C'_{diff}} = \frac{1}{C'_{ox}} + \frac{1}{C'_{Si}} \tag{3.7}$$

with

$$C'_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} \qquad C'_{Si} = \frac{dQ'_{Si}}{d\psi_S} \tag{3.8}$$

Equation 3.7 represents the total differential capacitance of the system as the series combination of a constant oxide capacitance caused by the insulating layer and a variable silicon capacitance due to the depletion region which depends on the applied gate voltage through ψ_S as it is seen in Figure 3.6.

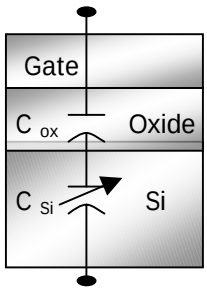

Figure 3.6 Capacitance equivalent circuit of a MOS capacitor, where total capacitance is a series combination of C_{ox} and C_{Si}

The evaluation of C'_{Si} as given by Equation 3.8 requires the expression of depletion region charge Q'_{Si} as a function of ψ_S . The electric field E_{Si}, hence the charge in silicon Q'_{Si} can be obtained from one-dimensional Poisson equation

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_{si}} \tag{3.9}$$

where ρ(x) is the total space-charge density in the depletion region as:

$$\rho(x) = q(N_D^+ - N_A^- + p(x) - n(x)) \tag{3.10}$$

where N_A^- is density of ionized acceptors, N_D^+ is density of ionized donors, p is the free holes, n is the free electrons and q is the electric charge. Free carrier concentrations p(x) and n (x) are expressed as:

$$p(x) = n_i e^{\frac{(E_i(x)-E_F)}{k_B T}} = n_i e^{\frac{(E_i(x)-E_F+E_{ib}-E_{ib})}{k_B T}} = n_i e^{\frac{(E_{ib}-E_F)}{k_B T}} e^{(\frac{-(E_{ib}-E_i(x))}{k_B T})} \tag{3.11}$$

where,

$$\begin{aligned} q\psi_s(x) &= E_{ib} - E_i(x) \text{ ; Surface potential } (\psi(x) = \psi_s(x=0)) \\ -q\psi_b(x) &= E_{ib} - E_F \text{ ; Bulk Potential} \end{aligned} \tag{3.12}$$

Equation 3.12 together with Equation 3.11 gives

$$p(x) = n_i e^{\frac{-q(\psi_b+\psi_s(x))}{k_B T}} = n_i e^{\frac{-q\psi_b}{k_B T}} e^{\frac{-q\psi_s(x)}{k_B T}} = N_A^- e^{\frac{-q\psi_s(x)}{k_B T}} \tag{3.13}$$

similarly

$$n(x) = n_i e^{\frac{q(\psi_b+\psi_s(x))}{k_B T}} = n_i e^{\frac{q\psi_b}{k_B T}} e^{\frac{q\psi_s(x)}{k_B T}} = \frac{n_i^2}{N_A^-} e^{\frac{q\psi_s(x)}{k_B T}} \tag{3.14}$$

Then replace Equation 3.14 and Equation 3.13 back in Equation 3.10 with $N_D^+ << N_A^-$ for p-type semiconductor. ρ (x) becomes

$$\rho(x) = q(-N_A^- + 0 + N_A^- e^{\frac{-q\psi_s(x)}{k_B T}} - \frac{n_i^2}{N_A^-} e^{\frac{q\psi_s(x)}{k_B T}}) \tag{3.15}$$

$$\rho(x) = qN_A^-[-1 + e^{-\frac{q\psi_s(x)}{k_B T}} - \left(\frac{n_i}{N_A^-}\right)^2 e^{\frac{q\psi_s(x)}{k_B T}}] \tag{3.16}$$

By replacing Equation 3.16 back in Equation 3.9 and by using mathematical simplifications, the electric field can be evaluated as follows

$$E_{Si} = -\frac{d\psi_S}{dx} \quad >> \quad -\frac{dE_{Si}}{dx} = -\frac{\rho(x)}{\varepsilon_{Si}} \tag{3.17}$$

solving Equation 3.17 for E_{Si} gives

$$E_{Si} = \pm \frac{\sqrt{2} k_B T}{q L_D} \cdot \sqrt{\left(e^{-\frac{q\psi_s}{k_B T}} + \frac{q\psi_s}{k_B T} - 1 \right) + \left(\frac{n_i}{N_A^-} \right)^2 \left(e^{\frac{q\psi_s}{k_B T}} - \frac{q\psi_s}{k_B T} - 1 \right)} \tag{3.18}$$

where

$$L_D = \sqrt{\frac{k_B T \varepsilon_{Si}}{N_A^- q^2}} \tag{3.19}$$

is the Debye length. The Debye length L_D appears frequently in the following expressions and represents the screening of the potential of ionized acceptors by the mobile free holes. The carrier concentration appears in the denominator of Equation 3.19, therefore for high carrier concentrations, the Debye length is small and the shielding is strong. Then by using the electric field expression given in Equation 3.18, the charge in semiconductor can be found as follows

$$Q'_{Si} = -\varepsilon_{Si} E_{Si} \tag{3.20}$$

$$Q'_{Si} = \pm \frac{\sqrt{2} \varepsilon_{Si} k_B T}{q L_D} \cdot \sqrt{\left(e^{-\frac{q\psi_s}{k_B T}} + \frac{q\psi_s}{k_B T} - 1 \right) + \left(\frac{n_i}{N_a^-} \right)^2 \left(e^{\frac{q\psi_s}{k_B T}} - \frac{q\psi_s}{k_B T} - 1 \right)}$$

where the positive (+) sign applies for accumulation and the negative (-) sign applies for depletion. As it is clearly seen from Equation 3.20, semiconductor charge density changes as a function of surface potential. A plot of Q'_{Si} vs. ψ_S is shown in Figure 3.7 for a p-type Si at room temperature with $N_A = 1.5 \times 10^{15}$ cm^{-3}. It is clearly seen from Figure 3.7 that for negative values of surface potential ψ_S, Q'_{Si} becomes positive which corresponds to the accumulation region. For this region, the first term in Equation 3.20 becomes dominant and so silicon charge becomes $Q'_{Si} \sim \exp(q|\psi_S|/2kT)$. For $\psi_S = 0$ flat band condition results in $Q'_{Si} = 0$. For the depletion region, where $\psi_B > \psi_S > 0$, Q'_{Si} becomes negative. In this case, second term in Equation 3.20 becomes dominant and silicon charge becomes $Q'_{Si} \sim \sqrt{\psi_S}$. Finally, for the inversion region where $\psi_S >> \psi_B$

fourth term in Equation 3.20 becomes dominant and silicon charge becomes $Q'_{Si} \sim \exp(q\psi_S / 2kT)$.

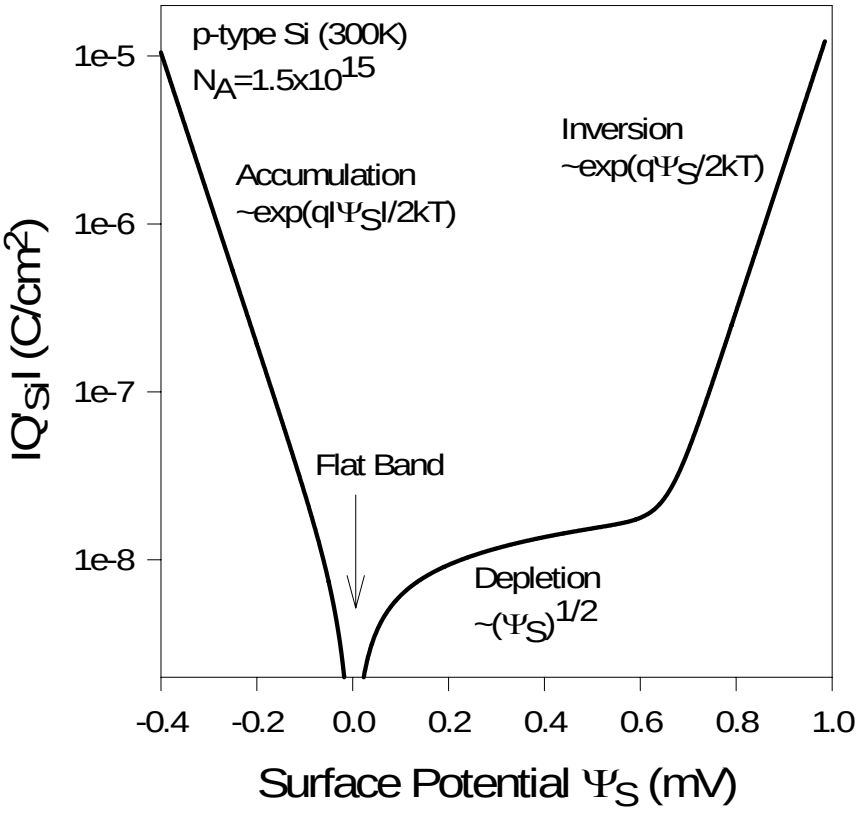

Figure 3.7 Variation of the magnitude of the charge density Q'_{Si} in the semiconductor as a function of the surface potential ψ_S for p-type Si with $N_A=1.5\text{x}10^{15}$ cm^{-3} at room T.

Finally by taking the derivative of Q'_{Si} with respect to ψ_S, the variable silicon capacitance C'_{Si} can be evaluated as follows

$$C'_{Si} = \frac{dQ'_{Si}}{d\psi_S} = \frac{\varepsilon_{si}}{\sqrt{2}L_D} \cdot \left| \frac{\left[1 - e^{-\frac{q\psi_s}{k_BT}} + \left(\frac{n_i}{N_A^-} \right)^2 \left(e^{\frac{q\psi_s}{k_BT}} - 1 \right) \right]}{\sqrt{\left(e^{-\frac{q\psi_s}{k_BT}} + \frac{q\psi_s}{k_BT} - 1 \right) + \left(\frac{n_i}{N_A^-} \right)^2 \left(e^{\frac{q\psi_s}{k_BT}} - \frac{q\psi_s}{k_BT} - 1 \right)}} \right| \tag{3.21}$$

As it is clearly seen from Equation 3.21, the variable silicon capacitance is strongly depended on the surface potential ψ_S. Finally, the total capacitance of MOS system is found by series combination of variable silicon capacitance as given in Equation 3.21 and constant oxide capacitance as given in Equation 3.8. The result is found by Equation 3.22.

$$C'_{dif} = \frac{C'_{OX}.C'_{Si}}{C'_{OX}+C'_{Si}} \tag{3.22}$$

One special condition both for the voltage and the capacitance is the **flat band** condition. In an ideal MOS capacitor, when the applied gate voltage V_G=0, then surface potential ψ_S also becomes zero, which means there is no bending occurred in the energy band diagrams of Si substrate that is bands are flat. The capacitance value in this case is called as flat band capacitance C_{FB}, and the voltage applied to obtain flat band condition is called flat band voltage V_{FB}. In the ideal case the flat band voltage is zero, however, it might take different values other than zero as a result of non-ideal effects which will be explained in detail in the next section. For the calculation of flat band capacitance C_{FB} it is necessary to simplify Equation 3.21. For the flat band condition, Q'_{Si} is zero, but as ψ_S changes from ψ_S=0 at flat band, there will be a change in charge, and hence a value for C'_{Si}. To evaluate Equation 3.21 for small ψ_S, the exponential terms in the denominator require a three term series expansion to prevent the denominator from going to zero if only two terms are used. Therefore, exp ($-\psi_S/k_BT$) becomes, $[1-(q\psi_S/k_BT)+(1/2)(q\psi_S/k_BT)^2]$ and exp (ψ_S/k_BT) becomes, $[1+(q\psi_S/k_BT)+(1/2)(q\psi_S/k_BT)^2]$. The exponentials in the numerator may be represented by the first two terms of the series expansion. The differential capacitance per unit area for $\psi_S \cong 0$ is the flat band capacitance C'_{FB} and is given by Equation 3.23 as

$$C'_{FB} = \frac{\varepsilon_{Si}}{\sqrt{2}L_D}\left[\frac{\left[\frac{q\psi_s}{k_BT}(1+(\frac{n_i}{N_A^-})^2)\right]}{\left[\frac{1}{2}(\frac{q\psi_s}{k_BT})^2(1+(\frac{n_i}{N_A^-})^2)\right]^{1/2}}\right] \tag{3.23}$$

For p-type Si, $(n_i/N^-_A)^2<<1$, and Equation 3.23 becomes

$$C'_{FB} = \frac{\varepsilon_{Si}\sqrt{2}}{\sqrt{2}L_D} = \frac{\varepsilon_{Si}}{L_D} \tag{3.24}$$

Equation 3.24 represents the silicon capacitance in the flat band condition. Then the total capacitance at flat band condition can be calculated by using Equation 3.24 and Equation 3.22, which gives

$$C_{FB}(\psi_S = 0) = \frac{\varepsilon_{OX}}{t_{OX} + (\frac{\varepsilon_{OX}}{\varepsilon_{Si}})L_D} \tag{3.25}$$

As it is previously explained, capacitance characteristics of a MOS device is mainly controlled by the internal parameter surface potential ψ_S by applying an external parameter V_G as given in Equation 3.4. During the measurement of C-V characteristics of a MOS device a constant gate voltage V_G is applied together with a small signal (15 mV peak value) ac voltage V_{ac}. Depending on the frequency of this small signal ac voltage capacitance of the MOS structure in the inversion region can be changed. Figure 3.8 shows the theoretical ideal MOS capacitance versus voltage curves both for low frequency and high frequency calculated by using the theoretical explanation given above. In Figure 3.8, the regions for accumulation, depletion and inversion are shown clearly. For the accumulation region the normalized capacitance value is maximum and equal to oxide capacitance C_{ox} for a given oxide thickness t_{ox}. For the depletion region, as the silicon capacitance increases by the formation of the depletion layer, the total capacitance decreases as given in Equation 3.15. Finally, for the inversion region depending on the frequency of the ac voltage applied it is possible to observe two different behaviors. First, if the frequency is low enough, minority carrier electrons in p-Si can follow the signal so that they form an inversion layer at the oxide-silicon interface. Therefore, the total capacitance increases and reaches back to its maximum value for positive gate voltages. Second, if the applied frequency is high enough (1MHz), then electrons can not follow the signal and can not form an inversion layer at the oxide-silicon interface. In this case, the capacitance reaches its minimum value and stays constant even if the applied gate voltage is increased to higher positive voltages.

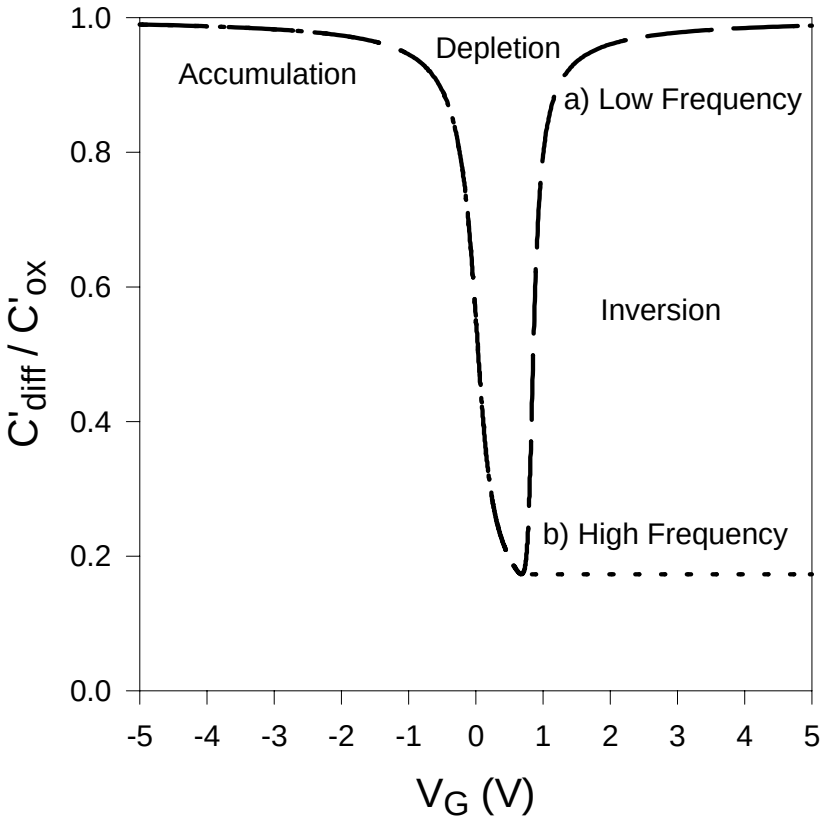

Figure 3.8 Theoretical ideal MOS Capacitance-Voltage curves for a) low frequency, and b) high frequency.

3.3 Non-ideal Effects

In actual MOS capacitors, there are several non-ideal effects and they show their effects on measured capacitance-voltage curves. First non-ideal effect arises from the difference between the work functions of metal and semiconductor due to variation in the doping level of semiconductor material. In order to overcome this difference in the work functions, an external voltage should be applied to the MOS structure. For this bias condition, the energy bands in the energy band diagram are flat and do not vary with distance. This applied voltage to achieve flat bands is called the flat band voltage and is represented by $V°_{FB}$ for the MOS capacitor without oxide or interface charge as given below

$$V^{\circ}_{FB} = \phi_{ms} = \phi_m - \phi_s = (\phi_m - (q\chi + E_g - (E_F - E_V))/q) \tag{3.26}$$

where $q\phi_m$ is the metal gate work function, $q\phi_s$ is the semiconductor work function, $q\chi$ is the semiconductor electron affinity, E_g is the semiconductor energy gap, and $(E_F - E_V)$ is the position of the semiconductor Fermi level above the valance band in the neutral semiconductor bulk.

For example if the gate material is Aluminum and the semiconductor material is silicon with a doping level of N_A=1x10^{15} cm^{-3}, the flat band voltage can be calculated as given in Equation 3.27.

$$V^{\circ}_{FB} = \phi_{ms} = \phi_{Al} - \phi_{Si} = 4.1 - (4.05 + 1.125 - 0.269) = -0.806 \text{ eV} \quad (3.27)$$

The difference in work functions, -0.806 eV represents the amount of band bending. The sign of the difference of the metal and semiconductor work functions gives the polarity connected to the metal to obtain the flat band condition.

Other non-ideal effects are due to charges present in the oxide and at the semiconductor-oxide interface. It has been established that four general types of charges are associated with the oxide/Si system (Casey 1999) as summarized in Figure 3.9. Here, total charge per unit area is represented by Q (C/cm^2) and the number of charges per unit area (the number density) is represented by the symbol N (number/cm^2)

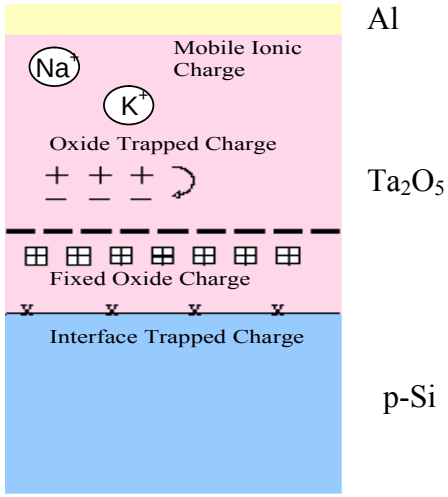

Figure 3.9 Terminology for the names and location of charges in a non-ideal MOS structure

The first type of charge is named as the fixed oxide charge Q_f (and its number density N_f), which is due primarily to the structural defects (such as ionized silicon) in the oxide layer. The density of this type of charge is related to the oxidation process. The second type of charges is the oxide trapped charge, Q_{ot} (and its number density N_{ot}).

These are due to holes or electrons trapped in the bulk of the oxide layer and can arise from the ionizing radiation or avalanche injection. Thus, Q_{ot} can have a positive or a negative value. Third type of charge is called mobile ionic charge, Q_m (and its number density N_m), which is mainly due to ionic impurities such as Li^+, Na^+, and K^+ etc. The sum of these three different charges in the oxide layer is represented by the effective oxide charge Q_{eff} (and its number density N_{eff}) as given in Equation 3.28.

$$Q_{eff} = Q_f + Q_m + Q_{ot} \tag{3.28}$$

Finally, the fourth type of charge causing the non-ideal effects is known as interface trapped charge Q_{it} (and its density per unit area per unit energy D_{it}) located at the oxide-semiconductor interface. It can have a positive or a negative value depending on the location with respect to the Fermi level. They originate from structural disorder, oxidation-induced defects, metal impurities and defects caused by radiation or similar bond-breaking processes. They play a major role in the operation of MOS devices causing an increased recombination of the free carriers in the conduction and valance bands. The levels of the Q_{eff} and D_{it} are the controlling parameters for the device before its application in the microelectronic industry.

In this thesis, main goal is to evaluate the level of these charges present inside the oxide and at the oxide-semiconductor interface to get information about the electronic quality of the oxide layer and oxide-semiconductor interface. For this purpose, high frequency (1 MHz) capacitance-voltage technique together with Terman's Method and Simultaneous C-V method have been used and explained in detail in the following sections.

3.4 Analysis of Non-ideal Effects

3.4.1 Calculation of Flat Band Voltage and Doping Concentration

In the previous section, effective oxide charges causing the non-ideal effect has been described in detail. The effect of these effective oxide charges causes an additional shift of experimental high frequency capacitance-voltage curve along the voltage axis. Therefore, the flat band voltage V_{FB} will be due to these effective oxide charges and the

work function difference between metal and semiconductor as represented in Equation 3.29. In addition, to maintain continuity with common terminology, we continue to call this shift the flat band voltage, V_{FB}:

$$V_{FB} = V^{\circ}_{FB} + \Delta V(\text{due to effective oxide charges}) \tag{3.29}$$

V_{FB} can be directly obtained from two different analyses, from the comparison of experimental and theoretical C-V curves and also from the intercept of experimental $1/C^2$ versus V_G curve. The common method is to obtain flat band voltage V_{FB}, by comparing a measured high frequency C-V curve with the ideal theoretical C-V curve. The theoretical curve is calculated for a device without oxide charges or work function difference, but with the same oxide thickness and doping profile as the experimental device. An example of high frequency experimental and theoretical (ideal) capacitance-voltage curves for a p-type silicon substrate is shown in Figure 3.10. The voltage shift V_{FB} from the ideal C-V curve is shown in the figure at the value of theoretical flat band capacitance which can be calculated by using Equation 3.25.

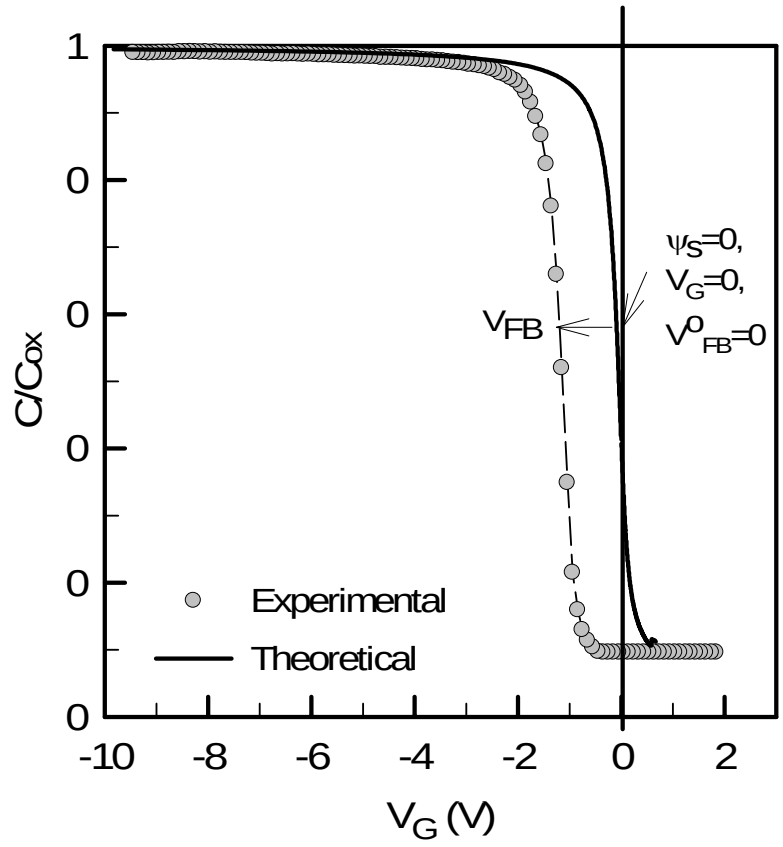

Figure 3.10 Theoretical (ideal) and experimental high frequency capacitance-voltage curves of a MOS capacitor with a p-type silicon substrate

The second method to determine V_{FB} is to plot experimental $1/C^2$ versus V_G curve. $1/C^2$ graph can yield important information about the flat band voltage as well as the doping profile of the sample. An example $1/C^2$ versus V_G graph obtained from high frequency C-V measurement is shown in Figure 3.11 where the intercept point in the voltage axis gives the value of flat band voltage V_{FB}.

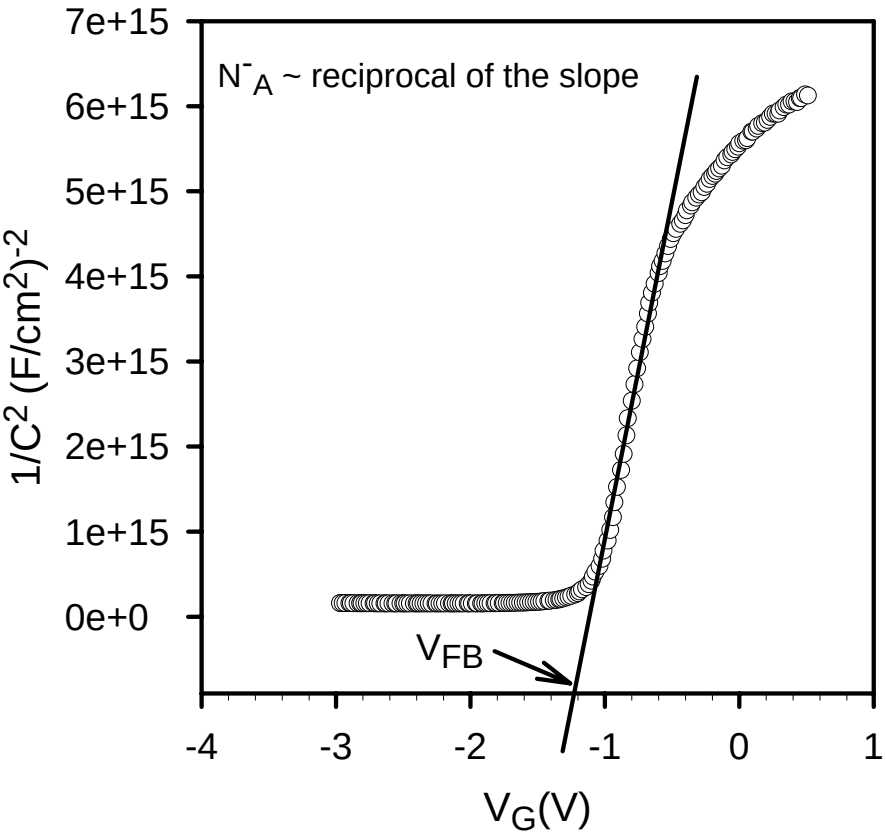

Figure 3.11 $1/C^2$ versus gate voltage V_G graph of a MOS capacitor

and also the doping profile is calculated by using the following equation.

$$N^{-}_{A} = -2(q\varepsilon_{Si}\frac{d}{dV_G}(\frac{1}{C^2}))^{-1} \tag{3.30}$$

which shows that N_A^- is related reciprocally to the slope of a $1/C^2$ versus V_G curve. A positive slope will give a negative N_A^- from Equation 3.30 indicating the acceptors as doping impurities for acceptors, whereas the negative slope gives a positive N for donors. The value of doping level is important and it is used for the calculation of theoretical capacitance of a MOS capacitor.

3.4.2 Calculation of Effective Oxide Charges

The measure of V_{FB} by using high frequency C-V method gives us information about the level of charges present inside the oxide layer and V_{FB} is directly obtained from the experimental and theoretical C-V curves and from the intercept of experimental $1/C^2$ vs. V_G curve as explained in the previous section. Once, the flat band voltage V_{FB} is determined by using one of the methods explained, its value is used to calculate the effective oxide charge Q_{eff} and its number density N_{eff} by using the following equation.

$$N_{eff} = \frac{Q_{eff}}{q} = \frac{C'_{ox}(V^{\circ}_{FB} - V_{FB})}{q} \tag{3.31}$$

where C'_{ox} is the oxide capacitance per unit area measured at strong accumulation.

In this thesis, effective oxide charge calculation is carried out both for Al-SiO_2-Si and Al-Ta_2O_5-Si MOS capacitors by using the procedure explained above and the results will be presented in the following chapter.

3.4.3 Derivation of Density of Interface Trap States (D_{it})

In this section, the calculation of density of interface trap states, D_{it}, with both high frequency C-V method (Terman's Method) and combined high-low frequency C-V (Simultaneous C-V) method will be explained in detail.

3.4.3.1 High Frequency Capacitance-Voltage Method (Terman's Method)

Terman developed and used the high frequency capacitance method for determining interface trap capacitance. In this method, capacitance is measured as a function of gate bias with frequency fixed at a high enough value so that interface traps do not respond to the frequency of small signal ac voltage embedded on dc gate voltage V_G.

Terman's method uses the comparison of an experimental and theoretical capacitance-voltage curve to extract the density of interface trap states. For this reason, a theoretical curve of C/C_{ox} vs. surface potential ψ_S is calculated and plotted by using the procedure explained in the previous section. Then, an experimental high frequency C-V measurement is performed. Finally, experimental C/C_{ox} vs. V_G curve is obtained. Theoretical C/C_{ox} vs. ψ_S and experimental C/C_{ox} vs. V_G plots are exhibited in Figure 3.12 (a) and Figure 3.12 (b) respectively.

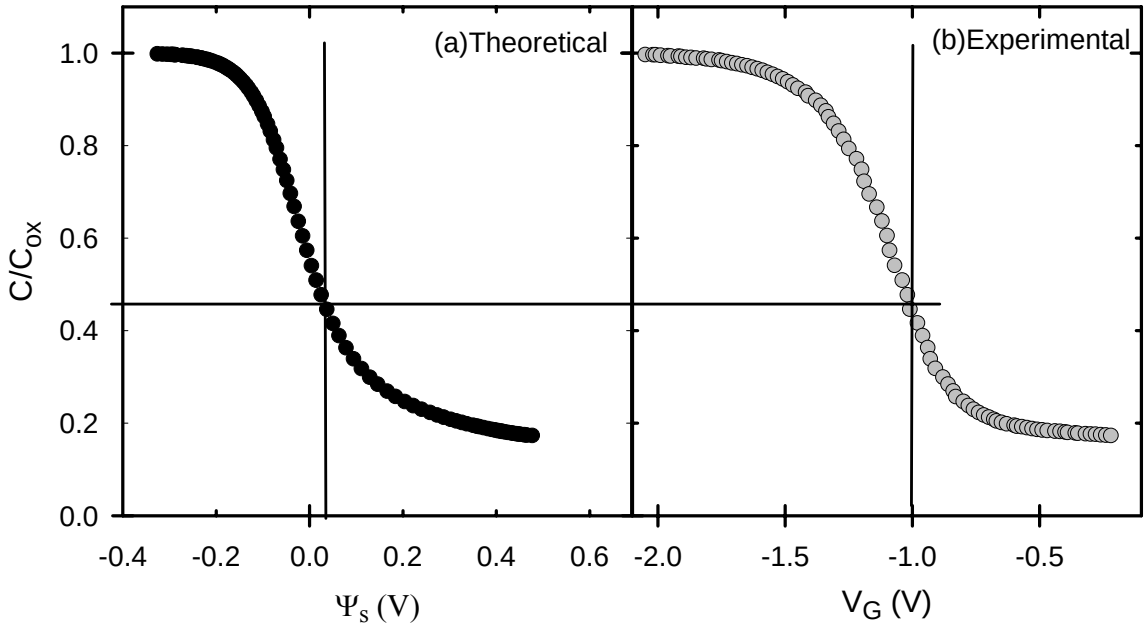

Figure 3.12 A theoretical C versus ψ_S plot compared with a hypothetical C versus V_G plot for a MOS capacitor

For any given high frequency C/C_{ox} value, the same band bending occurs so that ψ_S from the C/C_{ox} versus ψ_S curve corresponds to V_G from the C/C_{ox} versus V_G graph. Knowing ψ_S corresponding to a given high frequency C in the ideal MOS capacitor and measuring V_G corresponding to the same high frequency capacitance in the real MOS capacitor, it is possible to construct a ψ_S versus V_G curve for the MOS capacitor with interface trap states as given in Figure 3.13. It is this ψ_S versus V_G relationship that contains all the information about the density of interface trap states in high frequency C-V measurements.

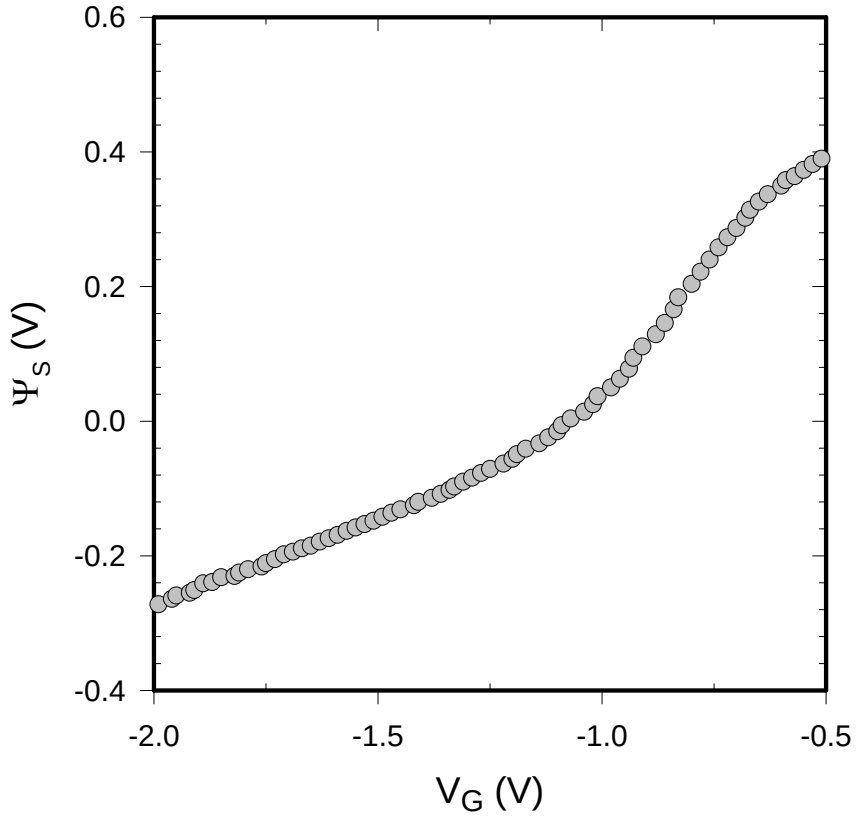

Figure 3.13 The surface potential ψ_S versus gate voltage V_G obtained from the theoretical and experimental high frequency C/Cox curves of a MOS capacitor shown in Figure 3.12.

Using the data presented in Figure 3.12(a) and (b), corresponding ψ_S versus V_G values are obtained carefully for each value of the C/C_{ox} data. The resulting surface potential ψ_S versus gate voltage V_G is presented in Figure 3.13 for the same MOS capacitor. In fact, the amount of stretch out, as measured by $d\psi_S/dV_G$, determines D_{it} level. Thus, by graphical or numerical differentiation of the ψ_S versus V_G curve, the derivative $d\psi_S/dV_G$ is found. In addition, variable silicon capacitance C_{Si} is calculated for each value of surface potential ψ_S by using the procedure given in the previous sections. Then interface trap state capacitance (C_{it}) is calculated using the Equation 3.32.

$$C_{it}(\psi_s) = C_{ox}\left[\left(\frac{d\psi_s}{dV_G}\right)^{-1} - 1\right] - C_{Si}(\psi_s) \tag{3.32}$$

Once C_{it} is found from Equation 3.32, D_{it} ordinarily is inferred using Equation 3.33.

$$D_{it}(\psi_s) = \frac{C_{it}(\psi_s)}{q} \tag{3.33}$$

In this thesis, Al-Ta_2O_5-Si MOS capacitors are investigated by using the high frequency capacitance-voltage method and D_{it} levels are evaluated as explained in this section.

3.4.3.2 Combined High-Low Frequency Capacitance Method (Simultaneous C-V Method)

The package software supplied by Keithly for Model 82 DOS simultaneous C-V system uses the combination of measured low and high frequency C-V curves for the evaluation of D_{it} levels of a MOS structure. Castagne and Vapaille (Nicollian and Brews 1982) were the first to combine high and low frequency C-V curves to obtain a measured C_{Si}. The step eliminates the need for a theoretical computation of C_{Si}, and for the measurement of the doping profile of the device. Then silicon capacitance can be found by Equation 3.34.

$$C_{Si} = \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \tag{3.34}$$

where C_{HF} is the measured high frequency capacitance and C_{ox} is the oxide capacitance measured in strong accumulation. Then Equation 3.34 is combined with Equation 3.35 to get interface trap sate capacitance as given in equation 3.36.

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - C_{Si} \tag{3.35}$$

where C_{LF} is the measured low frequency capacitance.

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \tag{3.36}$$

In this way C_{it} is obtained directly from the measured C-V curves without the uncertainty introduced by a theoretical C_{Si} and without uncertainty as to whether C_{Si} has been calculated for the correct band bending. An example measured C_{HF} and C_{LF} versus V_G graph for native SiO_2 is shown in Figure 3.14.

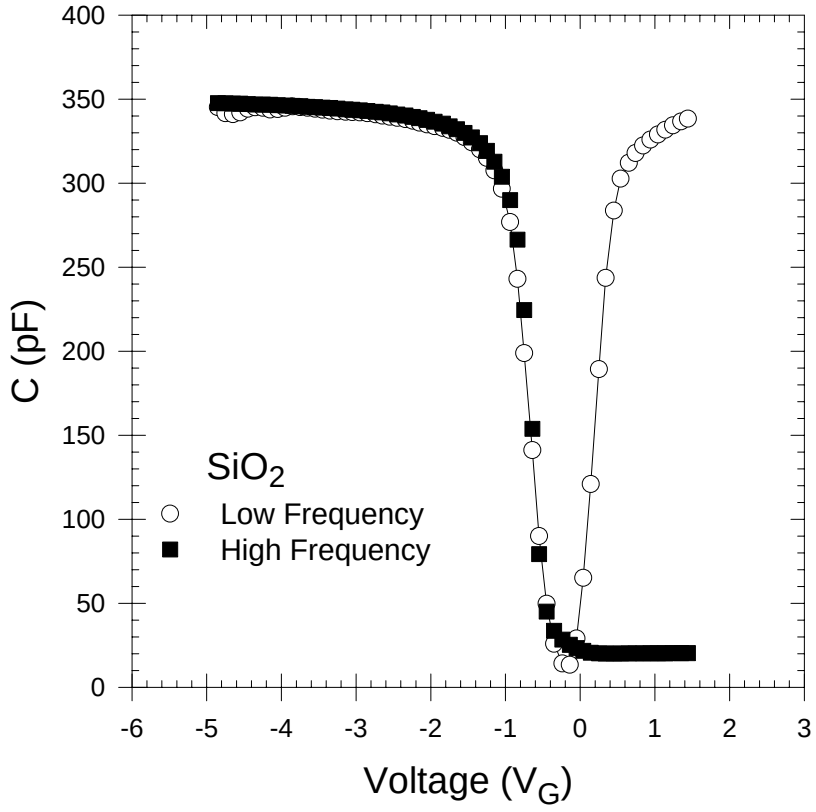

Figure 3.14 Measured C_{HF} and C_{LF} versus V_G curves for native SiO_2 sample

However this method requires a careful measurement of low frequency capacitance which is a rather difficult task for high dielectric constant insulators because of their leaky behavior. Low frequency capacitance is measured by using a charge feedback method which is based on the determination of capacitance with a change in charge with applied voltage and a frequency low enough is needed for the formation of inversion layer by the minority electrons.

In this thesis, only the interface trap states of Al-SiO_2-Si MOS capacitors are evaluated by using both Terman's method and combined high and low frequency method. For the determination of interface trap levels of Al-Ta_2O_5-Si MOS capacitors only Terman's method is used. The details about the results will be given in the next chapter.

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Introduction

Ta_2O_5 insulating layers are important candidate for high dielectric constant applications and especially for Gbit DRAM applications. Therefore, its electronic properties must be appropriately characterized in order to understand its physics. In this thesis, Al-Ta_2O_5-Si MOS structures prepared with RF magnetron sputtering method with or without a nitridation process of silicon surface prior to oxidation were characterized by using the Capacitance-Voltage Spectroscopy. Finally, important device parameters such as doping concentration, flat band voltage, dielectric constant, effective oxide charge and density of interface trap states were derived. The effect of nitridation (with different gas ambient and temperature ranges) on these parameters is studied in detail in order to enhance the electronic quality of Al-Ta_2O_5-Si MOS devices. Finally, the results are compared with the results of the Al-SiO_2-Si MOS capacitors as reference sample.

4.2 Results of Al-SiO_2-Si MOS Capacitors (Reference Sample)

The experimental low and high frequency C-V characteristics of Al- SiO_2-Si (MOS) capacitors constructed on a p-type silicon substrate are shown in Figure 4.1. Native oxide SiO_2 clearly shows the expected characteristics of a MOS device for both low and high frequency conditions. The maximum capacitance value, oxide capacitance C_{ox}, measured at the accumulation region is 350pF, which yields to a dielectric constant of 3.9 calculated by using the oxide thickness given in the Table 2.1. For accumulation and the depletion regions device show the same characteristics independent of the frequency of the small signal ac voltage applied. But for the inversion region, the capacitance value goes back to maximum capacitance C_{ox} for the low frequency and it stays constant at minimum capacitance for the high frequency measurements.

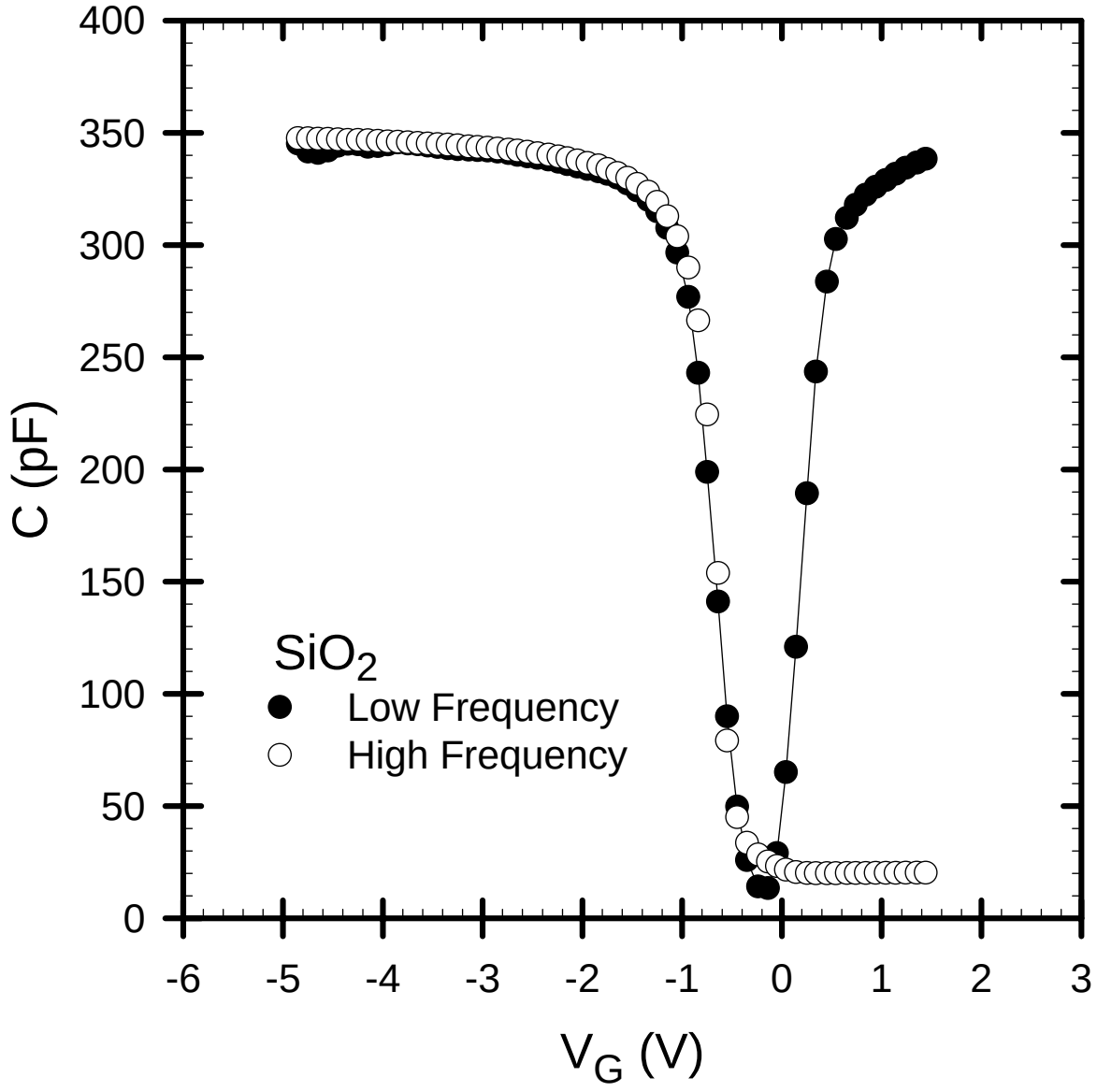

Figure 4.1 Low and High frequency (1 MHz) capacitance-voltage curves of Al-SiO_2-Si MOS capacitors

For the determination of non-ideal effects, it is necessary to calculate theoretical capacitance-voltage behavior of MOS capacitor. For this reason, doping concentration, N_A and flat band voltage values of Al- SiO_2-Si MOS capacitor are extracted by using the experimental high frequency $1/C^2$ versus V_G graph as it is shown in Figure 4.2. The measurements are performed for different dots on the same wafer for the reliable and reproducible data collection. Therefore, the results here represent an average of six different measurements. Finally, the doping concentration is calculated from the slope of the curve as $1.17x10^{15}$ cm^{-3} and the flat band voltage value is found to be -1.31 V from the intercept on the voltage axis.

After obtaining the doping concentration of p-type substrate, theoretical capacitance-voltage behavior of the MOS device is calculated by using the equations defined in the previous chapter. Figure 4.3 represents the theoretical and experimental normalized capacitance-voltage curves plotted for the same Al-SiO_2-Si structure. The flat band voltage shift of -1.31 V is also observed in this graph consistent with that obtained from the intercept of $1/C^2$ versus V_G graph. This voltage shift is caused by the non-ideal effects. Using this voltage shift, the effective oxide charge level is evaluated as $N_{eff}=3.4x10^{11}$ number/cm^2 using Equation 3.31, which is in the limit of good quality oxide layer reported for native SiO_2 layers (Paskaleva et al. 1995, Paskaleva et al. 2000).

Effective oxide charges are not the only non-ideal effects present in MOS capacitors. There is additional non-ideal effect due to interface trap states present at oxide-silicon interface. For the evaluation of density of interface trap levels both Terman's method and simultaneous C-V method are used in order to check the accuracy of the measurement system and software. For this reason, theoretical C/C_{ox} versus surface potential ψ_S and experimental C/C_{ox} versus gate voltage V_G graphs are plotted together as shown in Figure 4.4 (a) and (b) respectively. For each value of C/C_{ox} , corresponding surface potential ψ_S versus gate voltage V_G values are obtained and represented in Figure 4.5. Finally, by using the procedures and equations explained in chapter 3, the density of interface trap states, D_{it}, is evaluated. Figure 4.6 represents the density of interface trap state level as a function of energy in the band gap of cryatalline silicon. The average value of D_{it} level for Al-SiO_2-Si capacitors is found to be $2.5x10^{11}$ $eV^{-1}cm^{-2}$. It is clearly seen that both the software that uses the simultaneous C-V method and Terman's method gives the same level of D_{it} as shown in the graph. As seen from

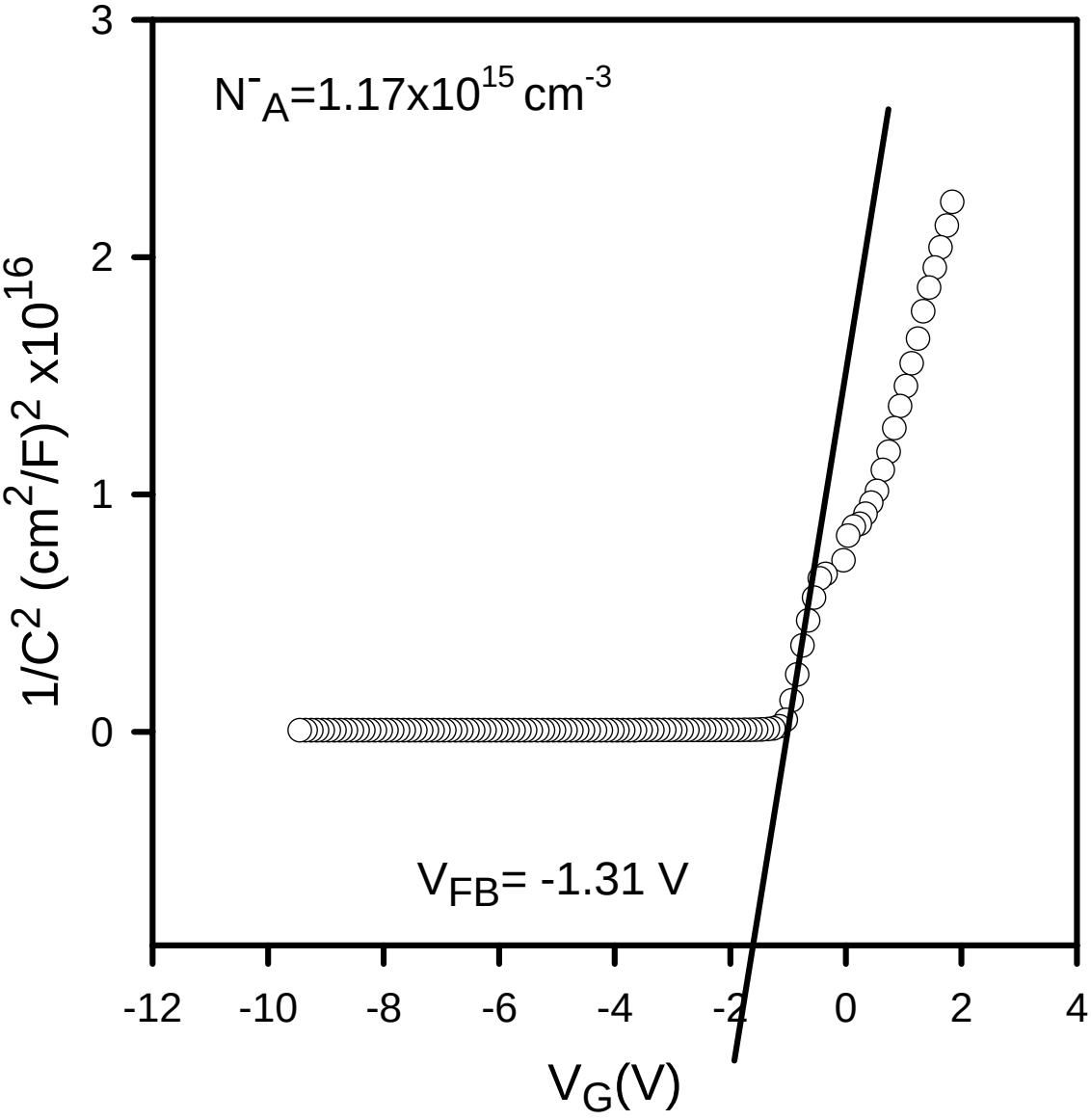

Figure 4.2 Experimental high frequency $1/C^2$ versus gate voltage V_G graph of the Al-SiO2-Si reference sample for the determination of doping concentration and flat band voltage

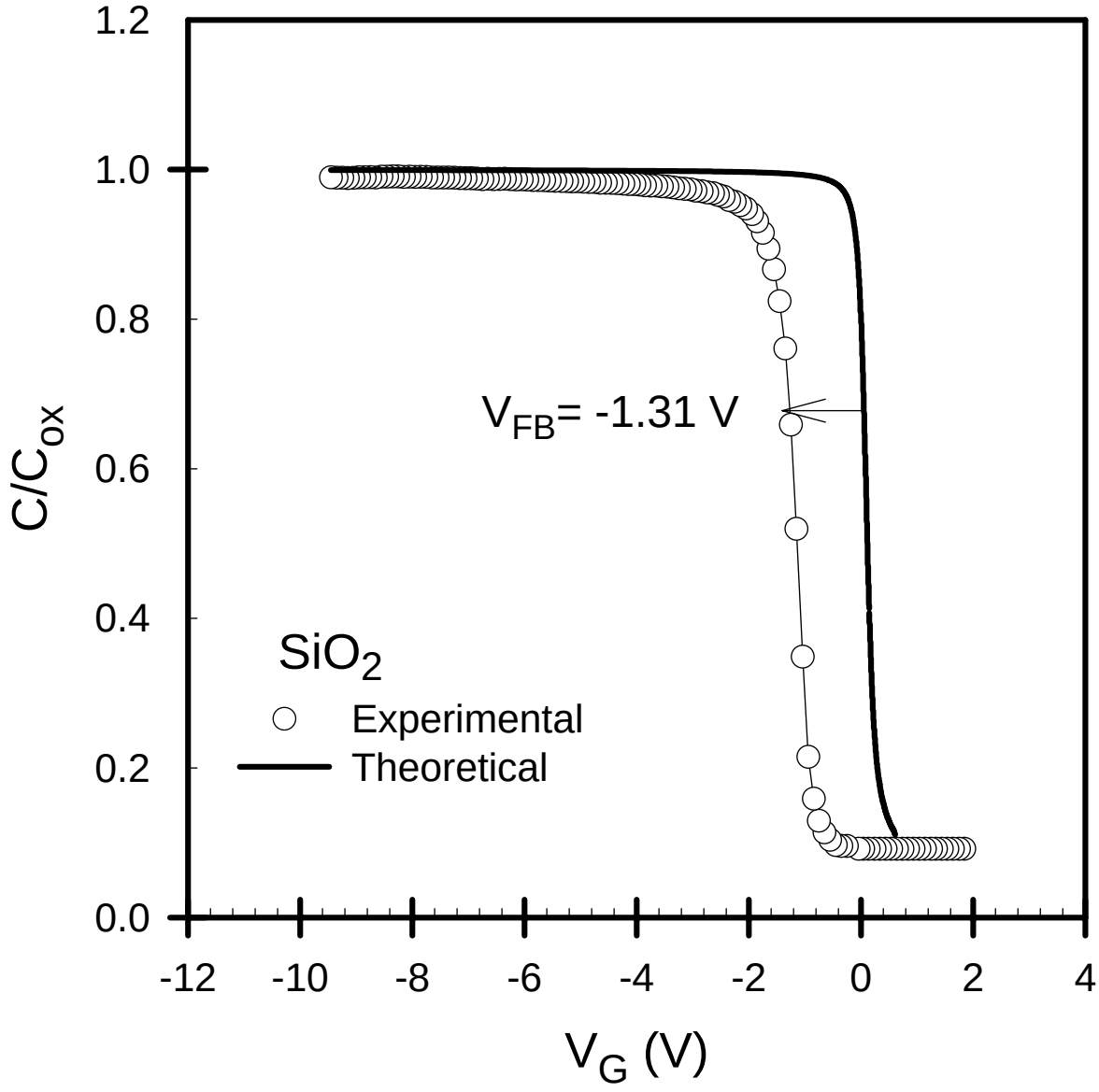

Figure 4.3 Theoretical (ideal) and experimental high frequency (1 MHz) Capacitance-Voltage Curves of an Al-SiO_2-Si MOS capacitor.

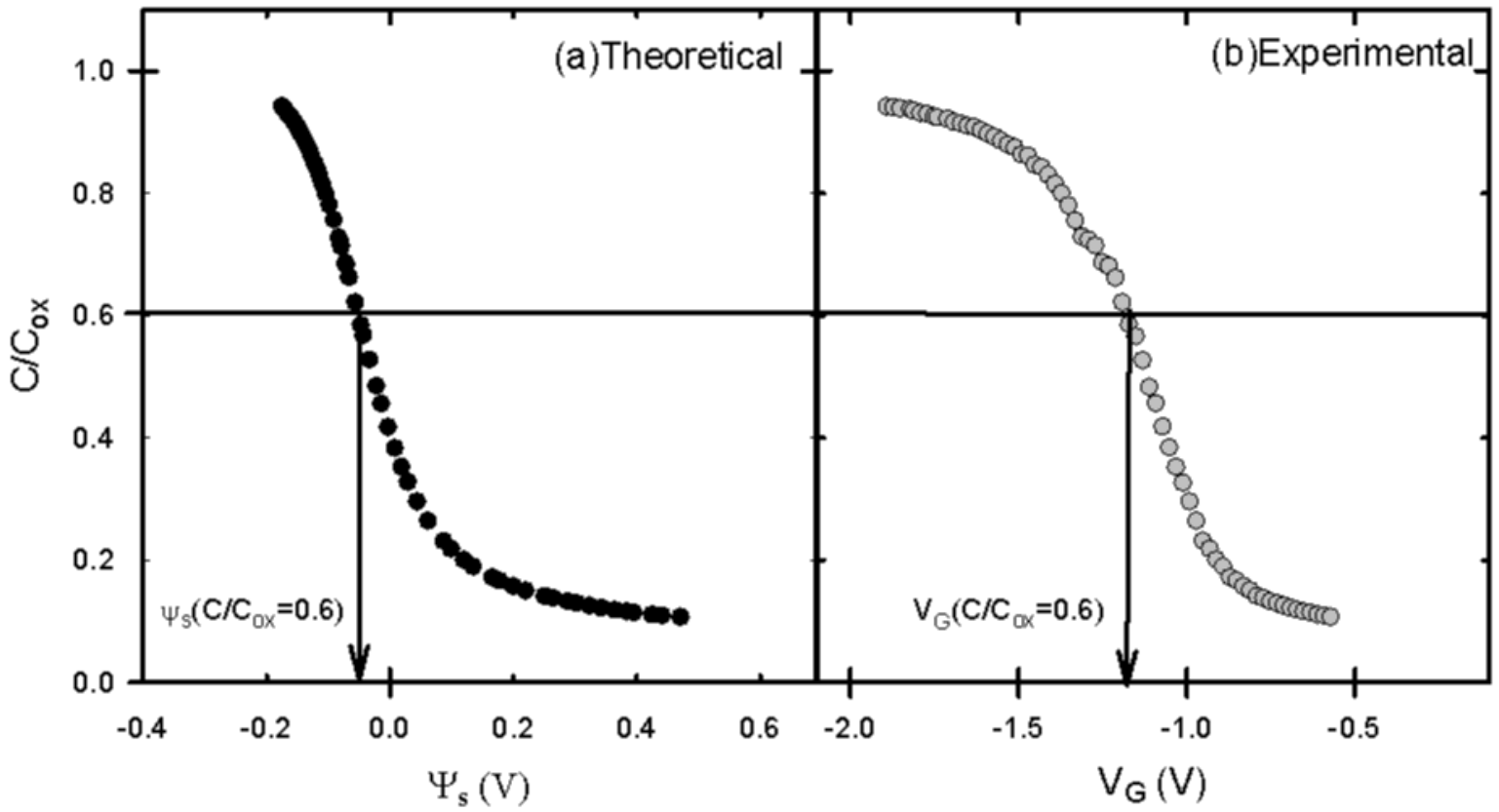

Figure 4.4 (a) Theoretical normalized capacitance versus surface potential and (b) experimental normalized capacitance versus gate voltage graphs for Al-SiO_2-Si MOS capacitor.

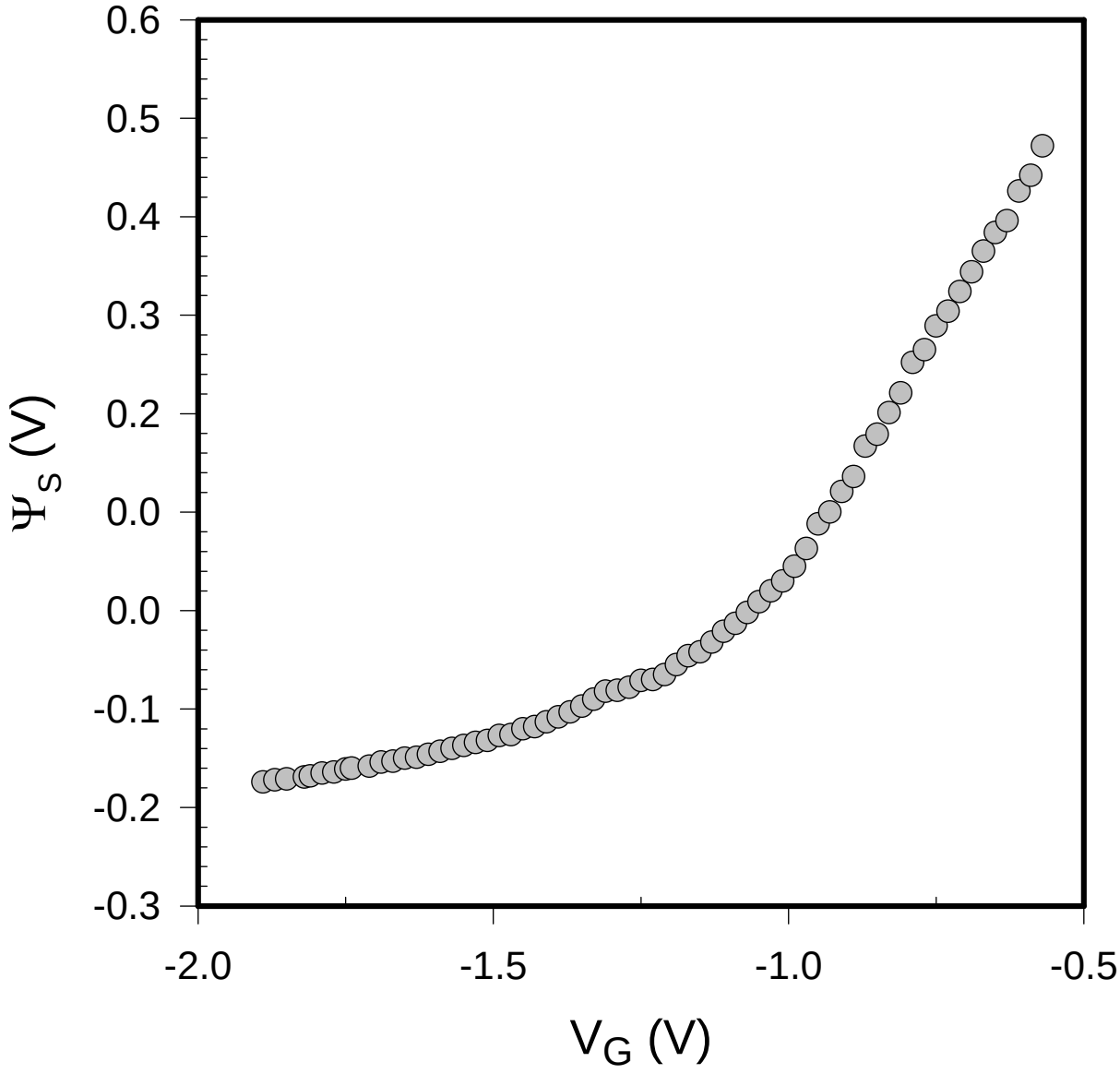

Figure 4.5 Surface Potential ψ_S versus gate voltage V_G graph of an Al-SiO_2-Si MOS capacitor obtained from the theoretical and experimental high frequency C/C_{ox} curves

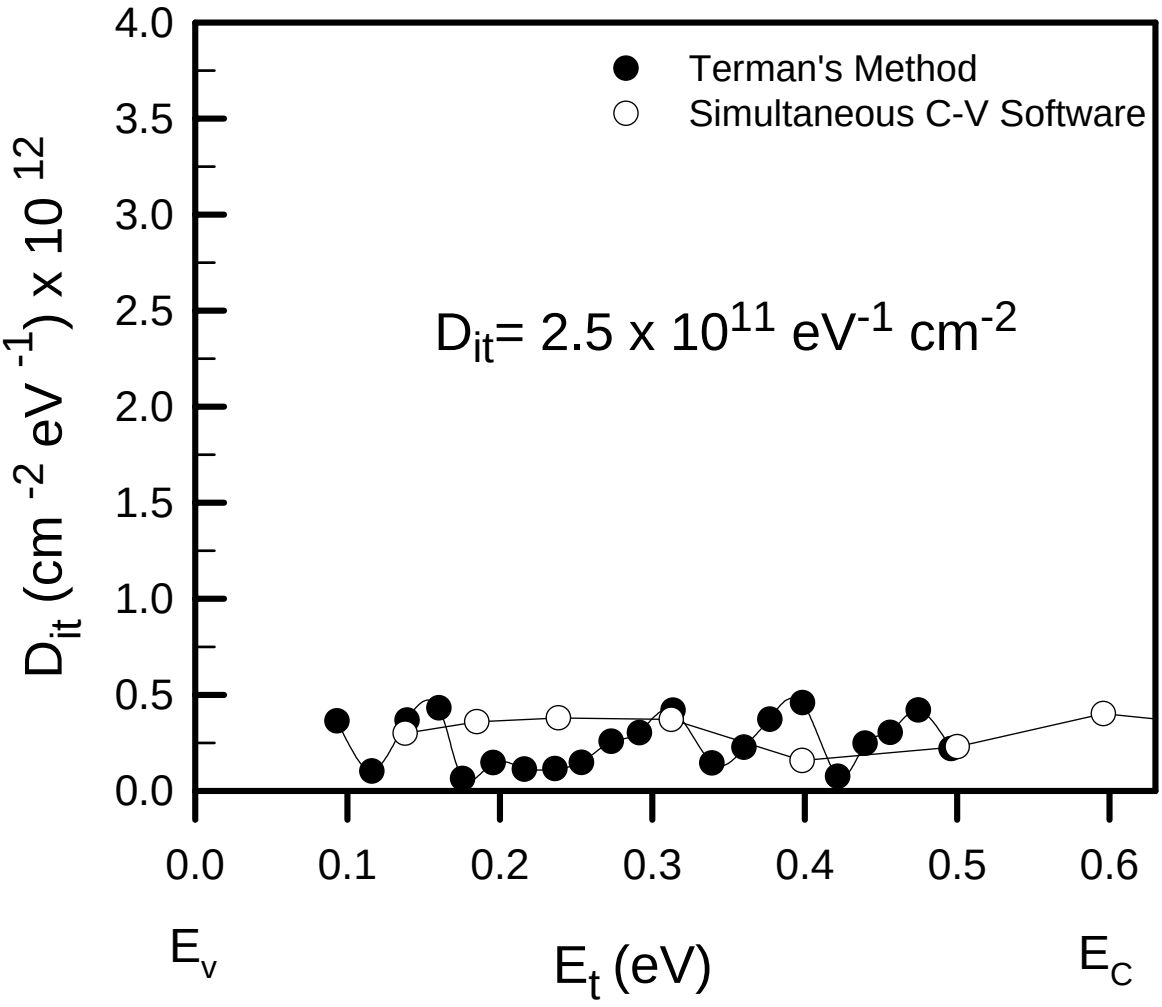

Figure 4.6 Density of Interface trap states as a function of energy in the bandgap of c-Si for Al-SiO_2-Si MOS capacitor calculated both by Terman's method and by simultaneous C-V software.

Figure 4.6, both techniques give almost the same level of D_{it}. However, Terman's method results in little bit noisy data due to human error involved in the calculation process. The values of effective oxide charge and density of interface trap states for Al-SiO_2-Si MOS capacitors will be used as a reference for the results of Set 1 and Set 2 samples prepared using Ta_2O_5 insulating layers.

4.3 Results of Al-Ta_2O_5-(SiO_2)-Si MOS Capacitors (Set 1): The Effect of Oxide Thickness

In order to replace SiO_2 insulating layer by using higher dielectric constant Ta_2O_5 insulating layers, oxide layers were prepared on a similar p-type silicon substrate as described in Chapter 2 and film thicknesses were kept below 50 nm. It is certain that there exist an inevitable SiO_2 layer of (1-2 nm) between Si and Ta_2O_5 as strongly indicated in the literature (Chaneliere et al. 1998, Ezhilvalavan and Tseng 1999). Therefore, resulting films have Ta_2O_5 insulating layer on top of native SiO_2 with 1 nm-2 nm thickness. The experimental high frequency (1 MHz) C-V characteristics of Al-Ta_2O_5-Si (MOS) capacitors with different oxide thicknesses are shown in Figure 4.7 together with that of reference sample with SiO_2 oxide layer. The effect of the oxide thickness is clearly reflected in the magnitude of the oxide capacitance dominating in the accumulation region since the areas of the devices are equal and the dielectric constant did not change significantly at these oxide thicknesses (Atanassova 1999). In addition, experimental high frequency C-V curve of the reference sample Al-SiO_2-Si MOS capacitor is shown as a comparison. It is clearly seen that the effect of dielectric constant for 20 nm thick Ta_2O_5 layer increases the oxide capacitance in the accumulation region more than factor of four. The areas of the dots are kept the same for all the samples shown in Figure 4.7. These results indicate that replacing SiO_2 with Ta_2O_5 increases the dielectric constant above the level of SiO_2.

The values of oxide capacitance C_{ox}, and other parameters derived from the high frequency C-V measurements are summarized in Table 4.1, where the dielectric constant, ε_{ox}, of Ta_2O_5 is 11.7 ± 0.9, in agreement with recent reports (Dimitrova and Atanassova 1998a, Ezhilvalavan and Tseng 1999, Paskaleva et al. 2000, Atanassova 1999). Doping concentration of the p-type Si substrate is obtained from the slope of experimental $1/C^2$ versus gate voltage V_G curve of each sample. These curves are shown in Figure 4.8 for three different MOS capacitors. The doping concentrations of the devices are almost identical and equal to (2.05±0.1) $x10^{11}$ cm^{-3}. In addition, flat band voltage values extracted from the intercept of the slope on the V_G axis are -1.74 V, -1.77 V, and -1.63 V for oxide thicknesses of 15 nm, 20 nm, and 25 nm respectively. These values are also summarized in Table 4.1.

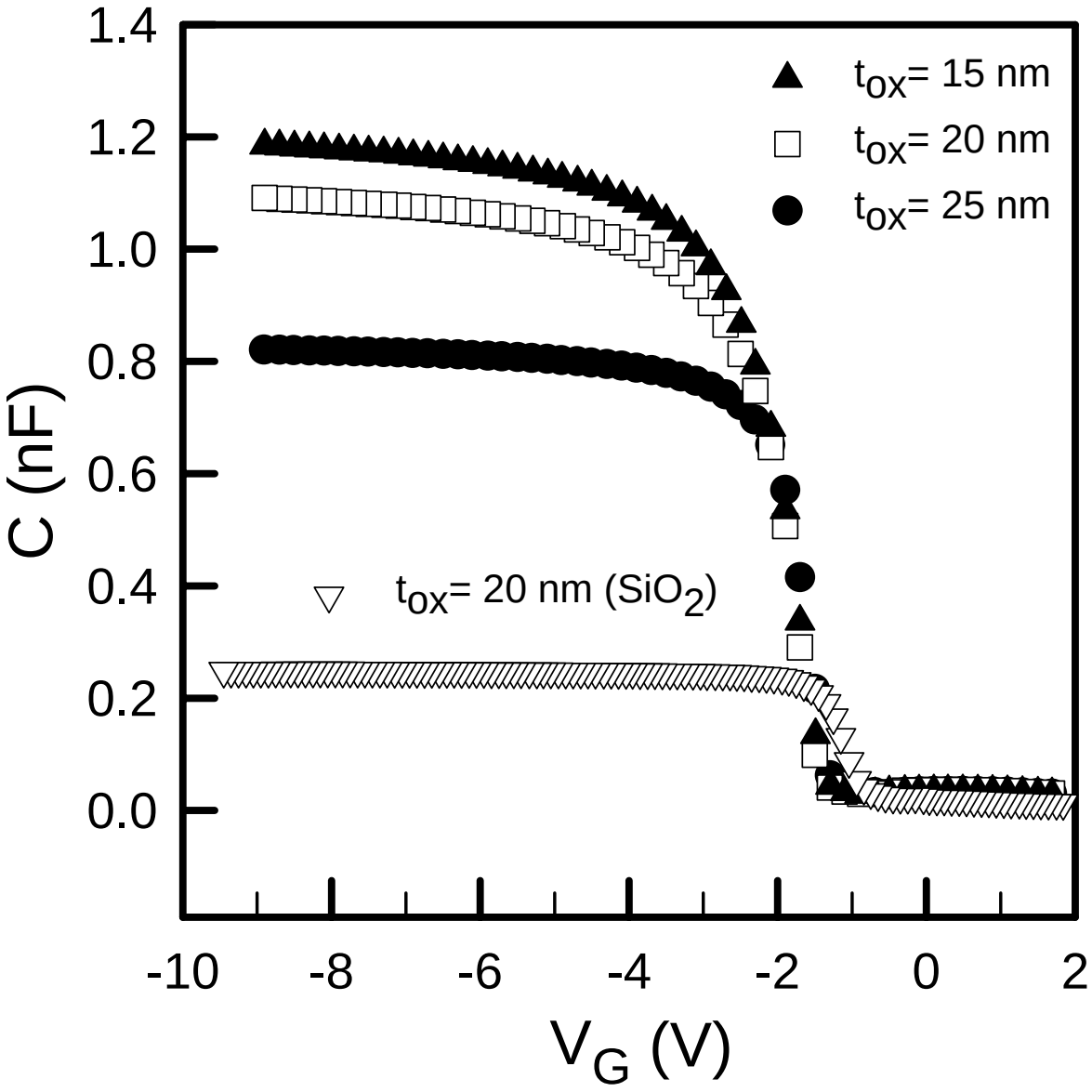

Figure 4.7 High frequency capacitance versus gate voltage characteristics of Al-Ta_2O_5-Si MOS capacitors with different oxide thicknesses and that of the reference MOS sample.

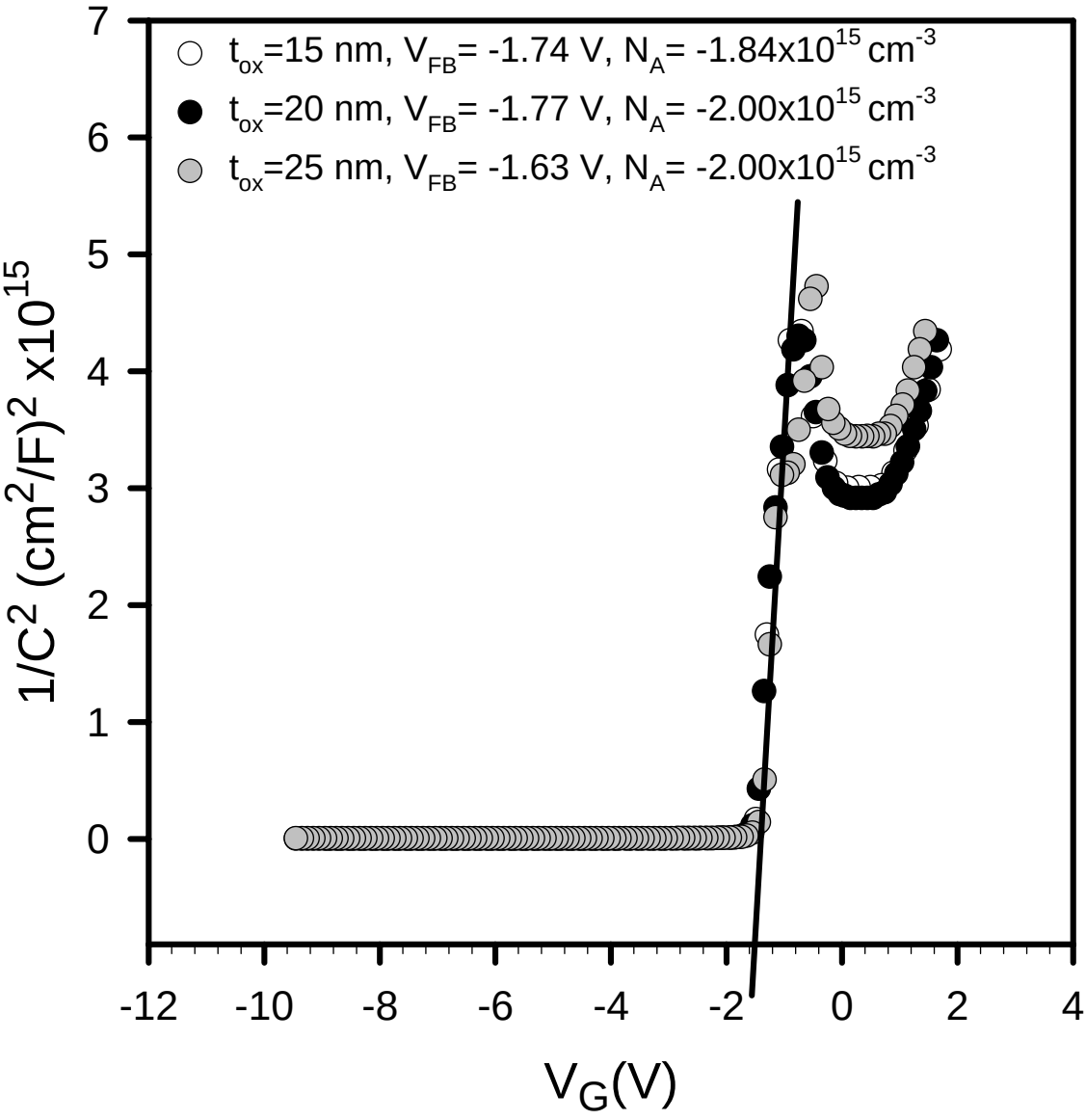

Figure 4.8 Experimental $1/C^2$ versus gate voltage V_G graph of Al-Ta_2O_5-Si MOS capacitors for the determination of doping concentration and flat band voltages for oxide thicknesses 15 nm, 20 nm and 25 nm.

Table 4.1 Summary of the parameters extracted from the high frequency C-V measurements for MOS capacitors with Ta_2O_5 insulating layers. Data presented here are the average of six device characteristics measured from different parts of the substrate wafer

Sample	t_{ox} (nm)	ε_{ox}	C_{ox} (pF)	$N_A(cm^3)$ $x10^{15}$	V_{FB} (volt)	Neff (cm^{-2}) $X10^{12}$
Ta_2O_5	15	10.1	1165	2.04	-1.74	3.11
	20	12.6	1093	1.95	-1.77	3.02
	25	11.8	818	2.15	-1.63	1.90
SiO_2	20	3.9	250	1.17	-1.31	0.34

By using the experimental values of doping concentration N_A of p-type silicon substrate, oxide thickness t_{ox}, dielectric constant ε_{ox} of oxide and metal gate area A, theoretical capacitance-voltage curves for each sample have been calculated. Finally, theoretical C-V curve is normalized to oxide capacitance C_{ox} and shown together with normalized experimental C-V curve in Figure 4.9, Figure 4.10 and Figure 4.11 for MOS capacitors with oxide layers of 15 nm, 20 nm, and 25 nm respectively. It is clearly seen that the experimental normalized C-V curve shifts from the ideal one due to non-ideal effects present in the MOS devices. The flat-band voltage, V_{FB}, values obtained for each sample are also indicated on the normalized capacitance curves. The flat-band voltage, V_{FB}, is a voltage shift from the flat band capacitance C_{FB} of ideal curve at V_G=0 V. The values of V_{FB} are -1.74 V, -1.77 V and -1.63 V for oxide thicknesses of 15 nm, 20 nm, and 25 nm respectively. Using these voltage shifts, the effective oxide charge density, Q_{eff}, and effective number of charges per unit area, N_{eff}, are calculated using Equation 3.31 defined in chapter 3. These are also summarized in Table 4.1. For oxide layers of thickness 15 and 20 nm, N_{eff} is $3.0x10^{12}$ cm^{-2} and decreases to $1.90x10^{12}$ cm^{-2} for a 25 nm thick Ta_2O_5 layer. However the values of N_{eff} are still higher than the native oxide SiO_2 and the proposed level of the metal-oxides which are considered to be an alternative for the native oxide SiO_2 as gate dielectric (Manchanda et al. 2001).

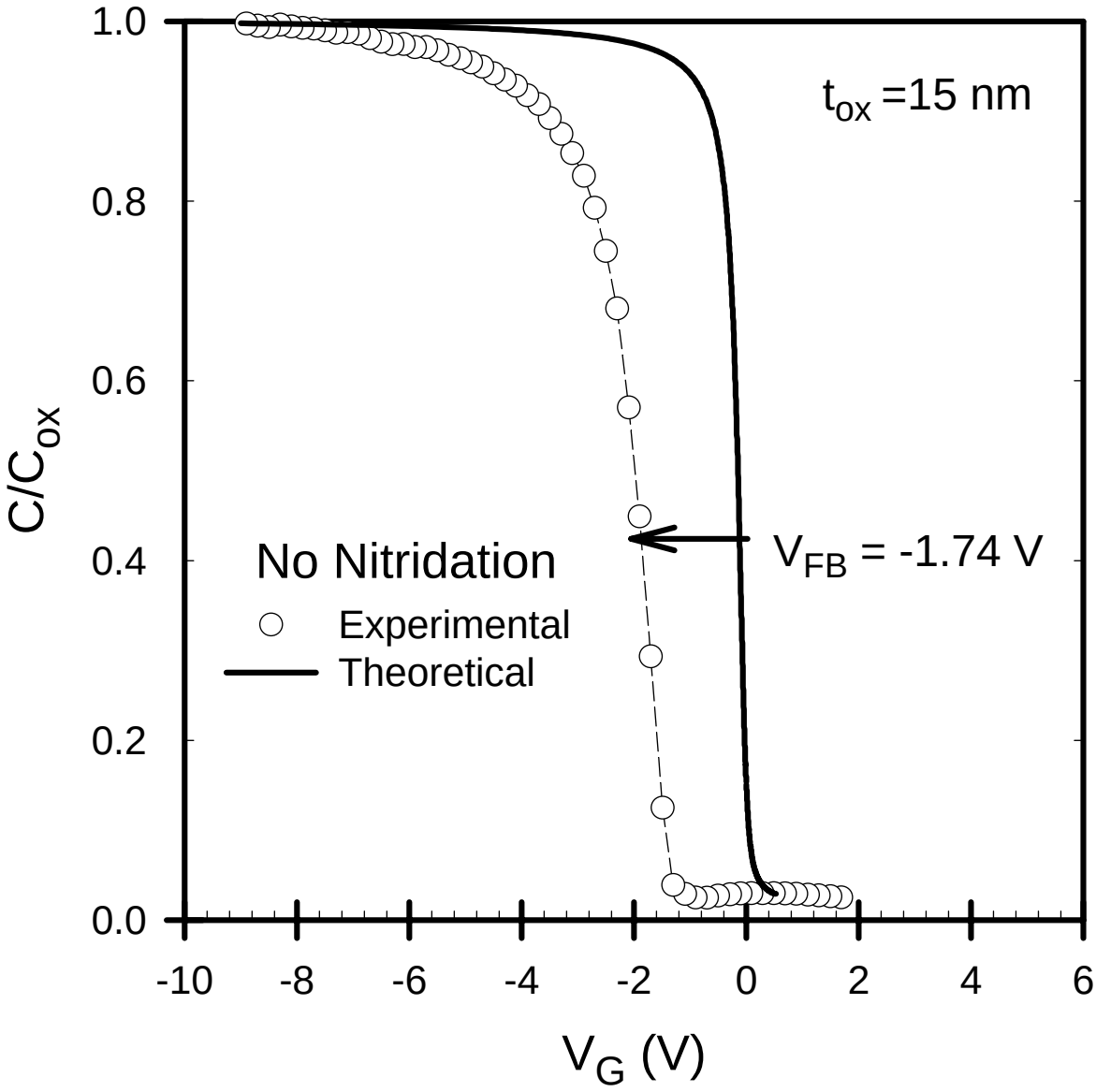

Figure 4.9 Theoretical and experimental high frequency normalized capacitance-voltage curves of Al-Ta_2O_5-Si MOS capacitor with 15 nm Ta_2O_5 insulating layer.

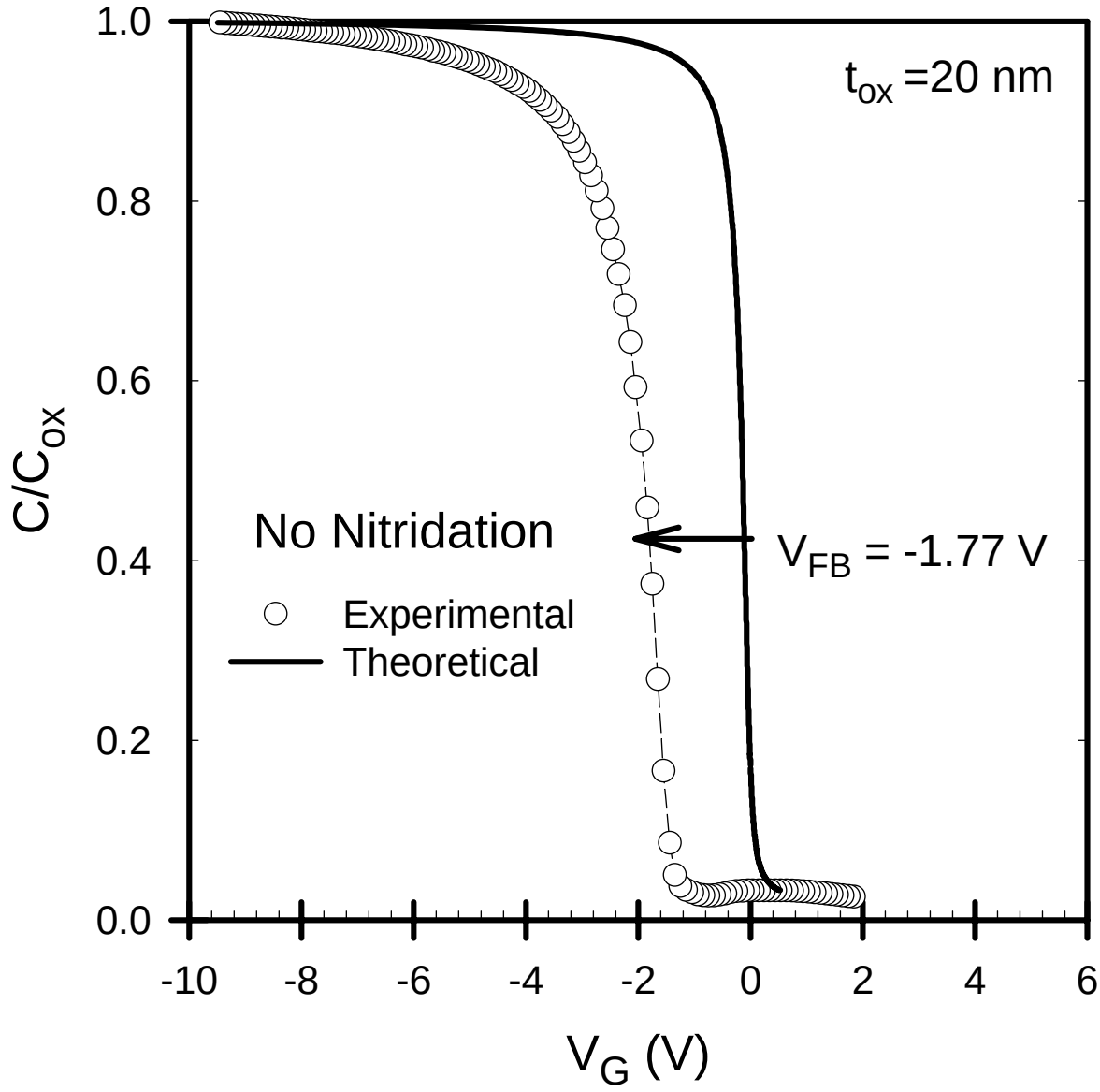

Figure 4.10 Theoretical and experimental high frequency normalized capacitance-voltage curves of Al-Ta_2O_5-Si MOS capacitor with 20 nm Ta_2O_5 insulating layer.

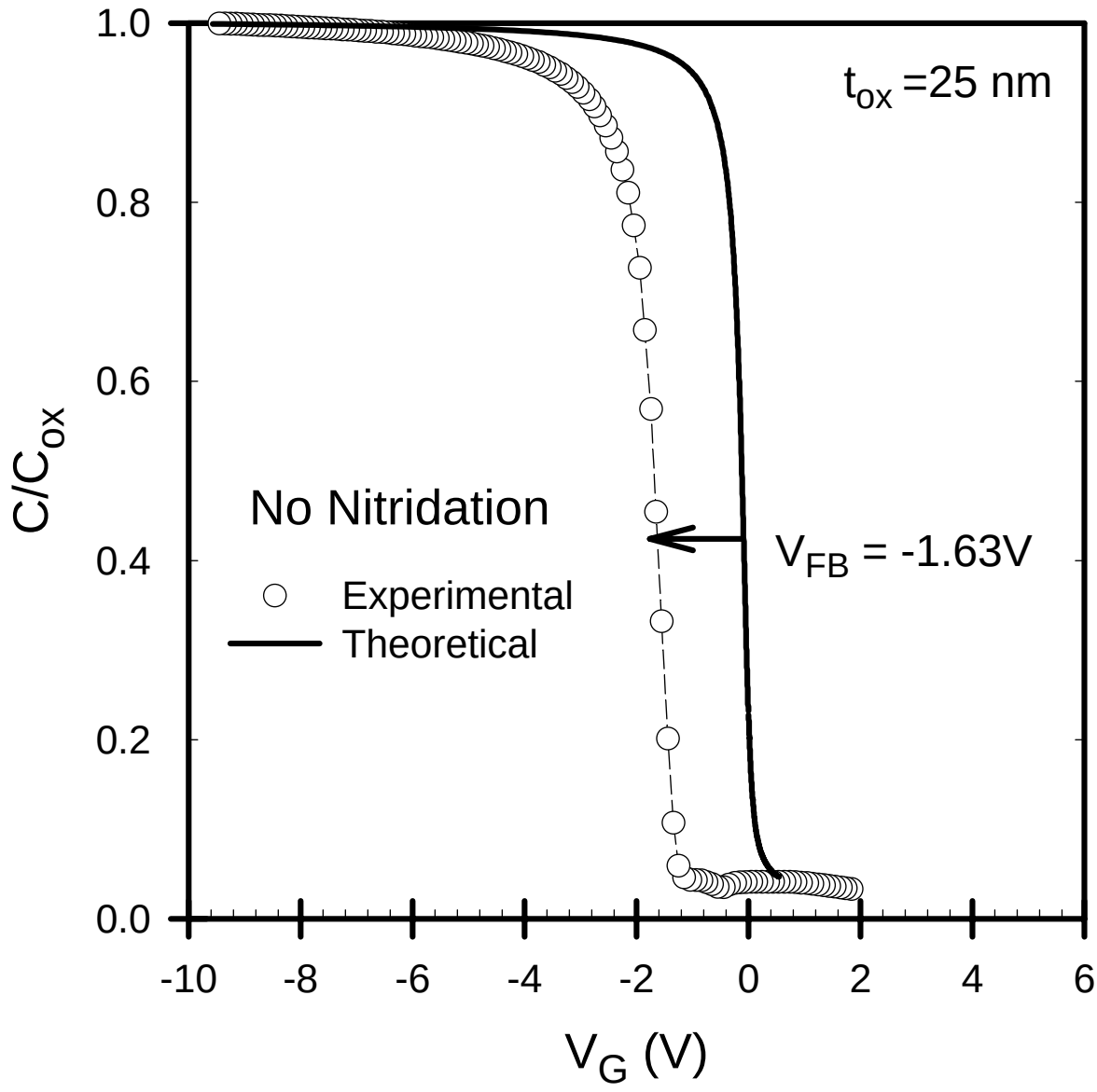

Figure 4.11 Theoretical and experimental high frequency normalized capacitance-voltage curves of Al-Ta_2O_5-Si MOS capacitor with 25 nm Ta_2O_5 insulating layer.

In addition, the shifts between the theoretical and experimental curves are not only due to effective oxide charges but also to states at the oxide-si interface. Using the theoretical and experimental normalized capacitance curves, the surface potential ψ_S versus gate voltage V_G curve was obtained for each sample as described in chapter 3 and in previous section for reference MOS sample. These curves are shown in Figure 4.12 (a) and (b) together with that of the reference sample. Using these curves, the density of interface trap states, Dit, was calculated as described in detail in Terman's method (Nicollian and Brews 1982) given in the previous chapter. The resulting distribution of D_{it} levels of Ta_2O_5 insulating layers are plotted as a function of energy in the band gap of the crystalline silicon in Figure 4.13 together with the D_{it} level of reference sample. It is well known that those interface trap levels occupy the energy levels in the band gap of the crystalline silicon and cause an important recombination path through these levels. For each oxide thickness, an average of six MOS capacitors are shown in Figure 4.13. The value of D_{it} for Ta_2O_5 is significantly higher than that of native oxide SiO_2 and shows a variation around $1.6\pm0.5 \times 10^{12}$ cm^{-2} eV^{-1}. There is no clear functional dependence on the oxide thickness for the thickness levels studied in this thesis. D_{it} levels of MOS capacitors with Ta_2O_5 layers are still above the limit for the requirement of Dit ($<2\times10^{11}$ cm^{-2} eV^{-1}), as specified by a detailed investigation of the possibilities for the replacement of the gate dielectric in technological applications, for device dimensions of less than 50 nm (Manchanda et al. 2001).

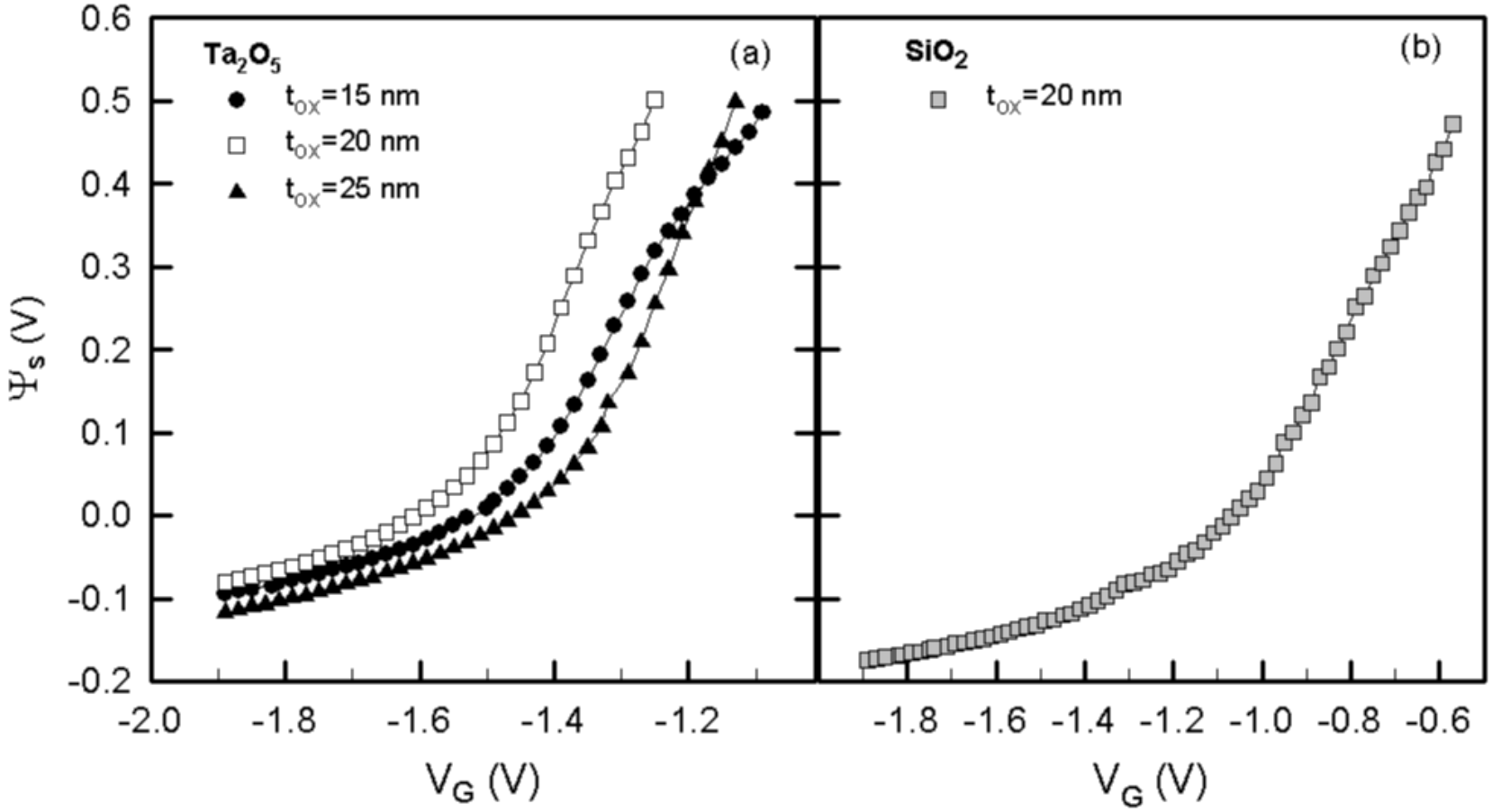

Figure 4.12 Surface Potential versus gate voltage V_G curves for MOS capacitors with a) Ta_2O_5 with t_{ox}=15 nm, 20 nm, and 25 nm and b)SiO_2 with t_{ox}=20 nm

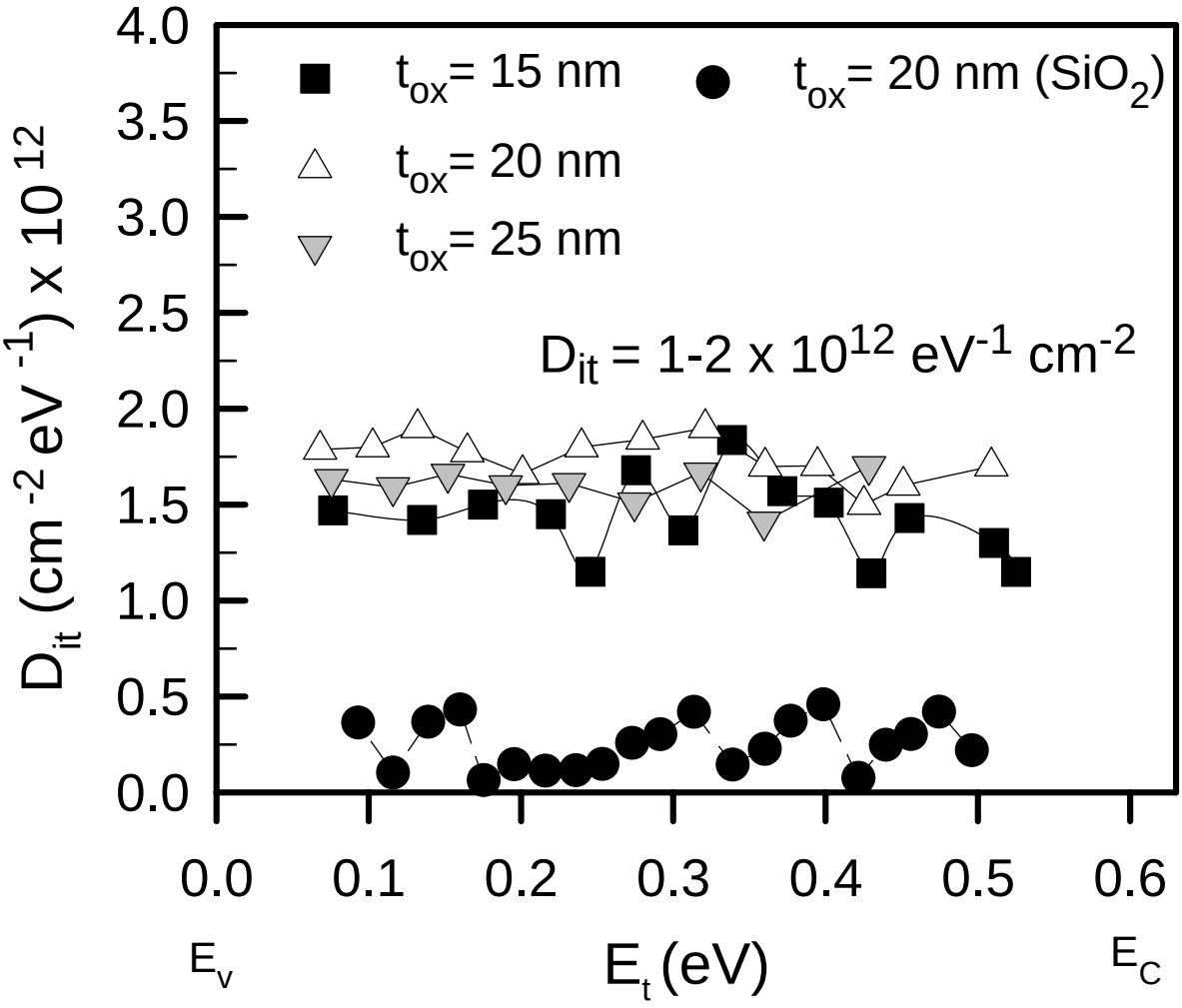

Figure 4.13 Density of interface trap states as a function of energy in the bandgap of c-Si for MOS capacitors with Ta_2O_5 insulating layer of different oxide thicknesses and that of the reference sample with native oxide SiO_2.

4.4 Results of Al-Ta_2O_5-(SiO_xN_y)-Si MOS Capacitors (Set 2): The Effect of Nitridation Process

As explained in the previous section, the electronic quality of Ta_2O_5 oxide layer and Ta_2O_5-Si interface are not in the desired level for the microelectronic industry requirements. In order to improve the quality of Ta_2O_5 oxide layer and Ta_2O_5-Si interface, an alternative nitridation process have been proposed on the p-type silicon substrate prior to the oxidation of p-type substrate (Novkovski et al. 2005). There are two types of nitridation processes have been carried out in this thesis. First one is in N_2O gas environment and the second one is in the NH_3 gas environment. After nitridation process, a 20 nm thick Ta_2O_5 oxide layer has been grown on the nitrided p-type silicon surface. The thickness of the silicon oxynitride (SiO_xN_y) layer formed as a result of nitridation process is about 1.5 nm to 2 nm and grown at different substrate temperatures from 700 °C to 850 °C. Finally, metal gates with different areas were evaporated to form Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors. The results will be presented separately and compared together.

4.4.1 Nitridation of Si Surface by N_2O Gas

Nitridation of p-type silicon substrate in N_2O gas was performed at substrate temperatures of 700°C, 800°C, and 850°C. After this process, 20 nm thick Ta_2O_5 layers were deposited as described in chapter 2. Experimental high frequency capacitance-voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors are presented in Figure 4.14 for three different nitridation temperatures. For each sample with respective nitridation temperatures, detailed analysis of C-V curves has been performed for at least six MOS devices and rough C-V measurements of MOS devices were performed for at least ten different MOS devices on different parts of the same substrate in order to confirm the reproducibility of the results. From the strong accumulation region, oxide capacitance C_{ox}, and dielectric constant ε_{ox} are directly evaluated using the known thickness values. For all devices, oxide thickness and gate area are kept the same. As seen from Figure 4.14, oxide capacitance value is 350 pF for nitridation process of 700 °C. It increases to 400 pF for 800°C and finally decreases back to 350 pF for nitridation process of 850°C.

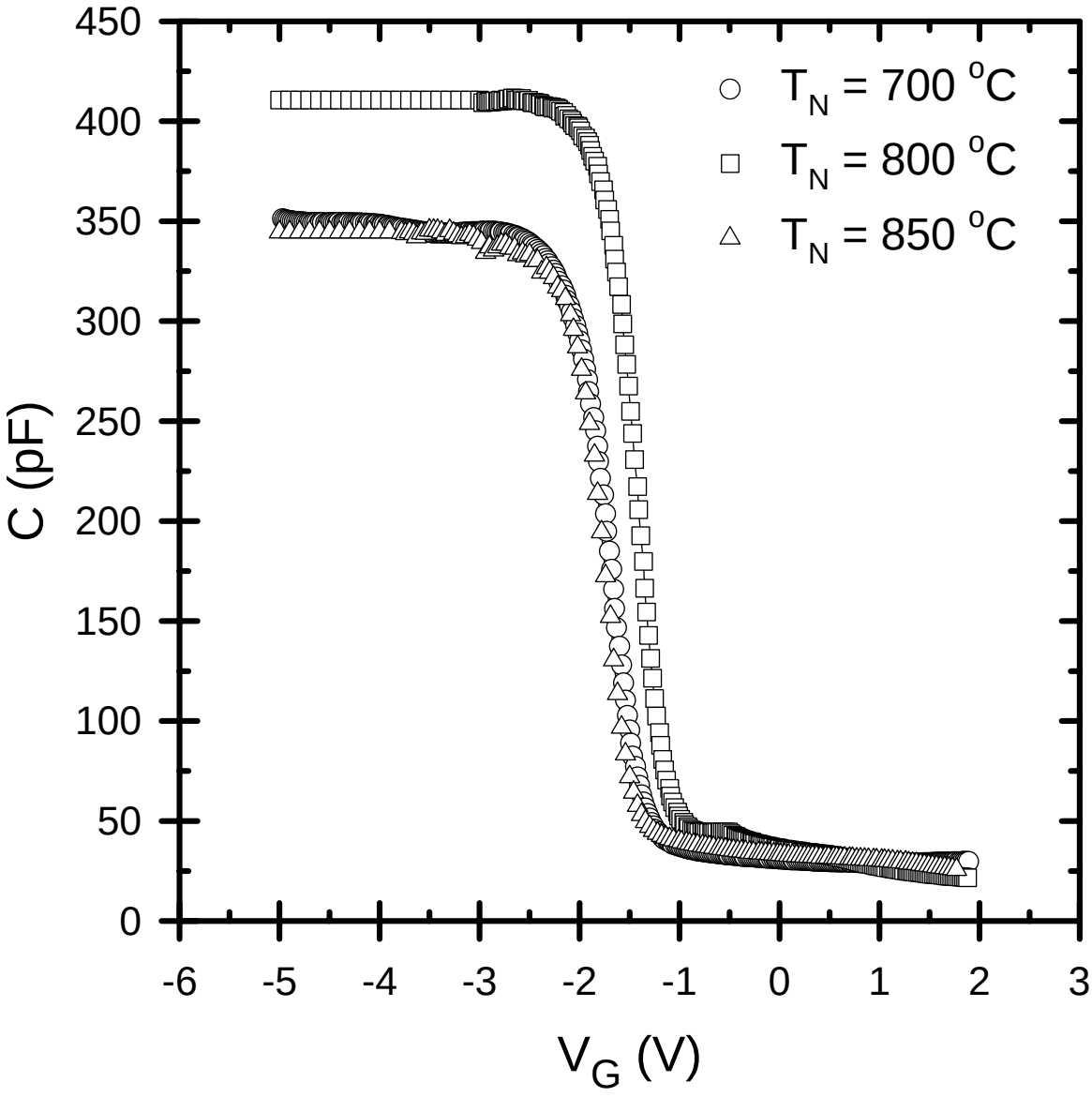

Figure 4.14 High frequency capacitance versus gate voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors for nitridation temperatures of 700°C, 800°C, and 850°C in N_2O gas environment.

For these three temperatures, the highest C_{ox} and correspondingly the highest dielectric constant is obtained for the nitridation temperature of 800°C.

After determining the fundamental characteristics of MOS capacitors using the capacitance values in the accumulation region, experimental $1/C^2$ versus gate voltage V_G graphs were generated in order to determine the doping concentration of p-type substrate used for each nitridation processes and the flat band voltage V_{FB} of each device due to non-ideal effects present in MOS capacitors. $1/C^2$ versus V_G graphs are shown in Figure 4.15 and doping concentration N_A derived from the slope is almost equal to 1.50×10^{15} cm^{-3} for three different samples nitrided at temperatures of 700°C, 800°C, and 850°C. However, the flat band voltages are -1.68 V, -1.42 V, and -1.63 V for nitridation temperatures of 700°C, 800°C, and 850°C respectively.

By using the experimentally determined parameters of ε_{ox}, t_{ox}, gate area A, doping concentration N_A of p-type silicon substrate, theoretical capacitance versus surface potential ψ_S and correspondingly theoretical capacitance versus gate voltage V_G curves were calculated for each MOS device. Finally, the curves were normalized to the oxide capacitance C_{ox} and plotted together with normalized experimental high frequency capacitance-voltage curves of each device. These are shown in Figure 4.16, Figure 4.17, and Figure 4.18 for nitridation temperatures of 700°C, 800°C, and 850°C respectively. It is clearly seen that there exists an almost parallel shift of experimental C-V curve from the theoretical ideal curve indicating the non-ideal effects. In addition, the flat band voltages V_{FB} are also indicated on each figure. It is drawn as a voltage shift from ideal curve to experimental curve at flat band capacitance value when $V_G=0$ for ideal curve. The flat-band voltages, V_{FB} were found to be -1.68 V, -1.42 V and -1.63 V for nitridation temperatures 700°C, 800°C, and 850°C respectively. These values are also consistent with those found from the intercept of $1/C^2$ versus gate voltage V_G in Figure 4.15.

The shifts of experimental C-V curves from the ideal one indicate the degree of the non-ideal effects reflected in experimental results. Using the flat band voltage shifts of each MOS device, the effective oxide charge density, Q_{eff}, and effective number of charges per unit area, N_{eff}, are calculated using Equation 3.31 defined in the previous chapter. These are also summarized in Table 4.2. For oxide layer nitrided at 700°C, N_{eff} is about 9×10^{11} cm^{-2} and decreases to 4×10^{11} cm^{-2} for oxide layer nitrided at 800°C. N_{eff} value again increases to 6×10^{11} cm^{-2} as nitridation temperature increases to 850°C.

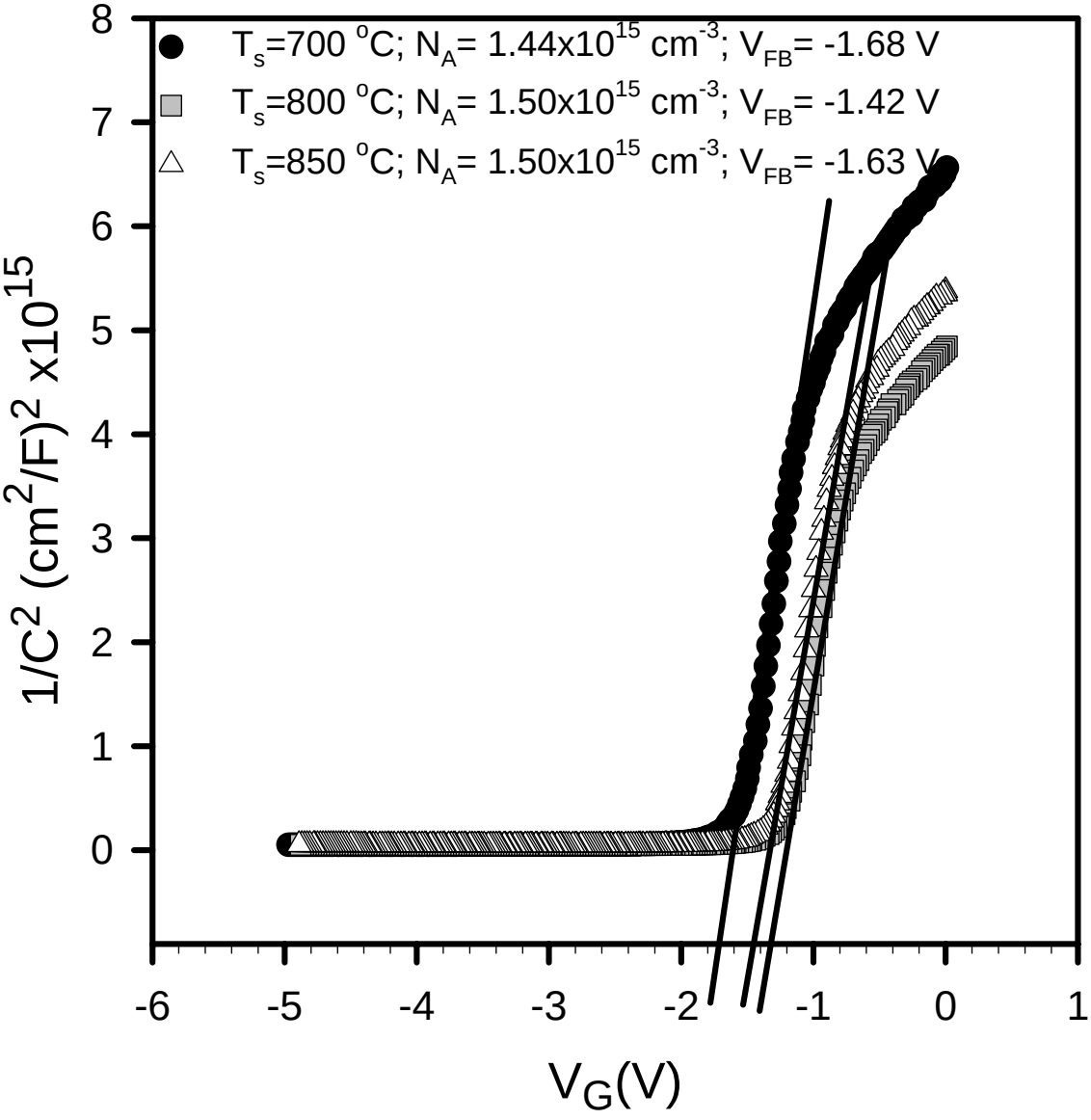

Figure 4.15 Experimental $1/C^2$ versus gate voltage V_G graph of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors for nitridation processes in N_2O at 700°C, 800°C, and 850°C.

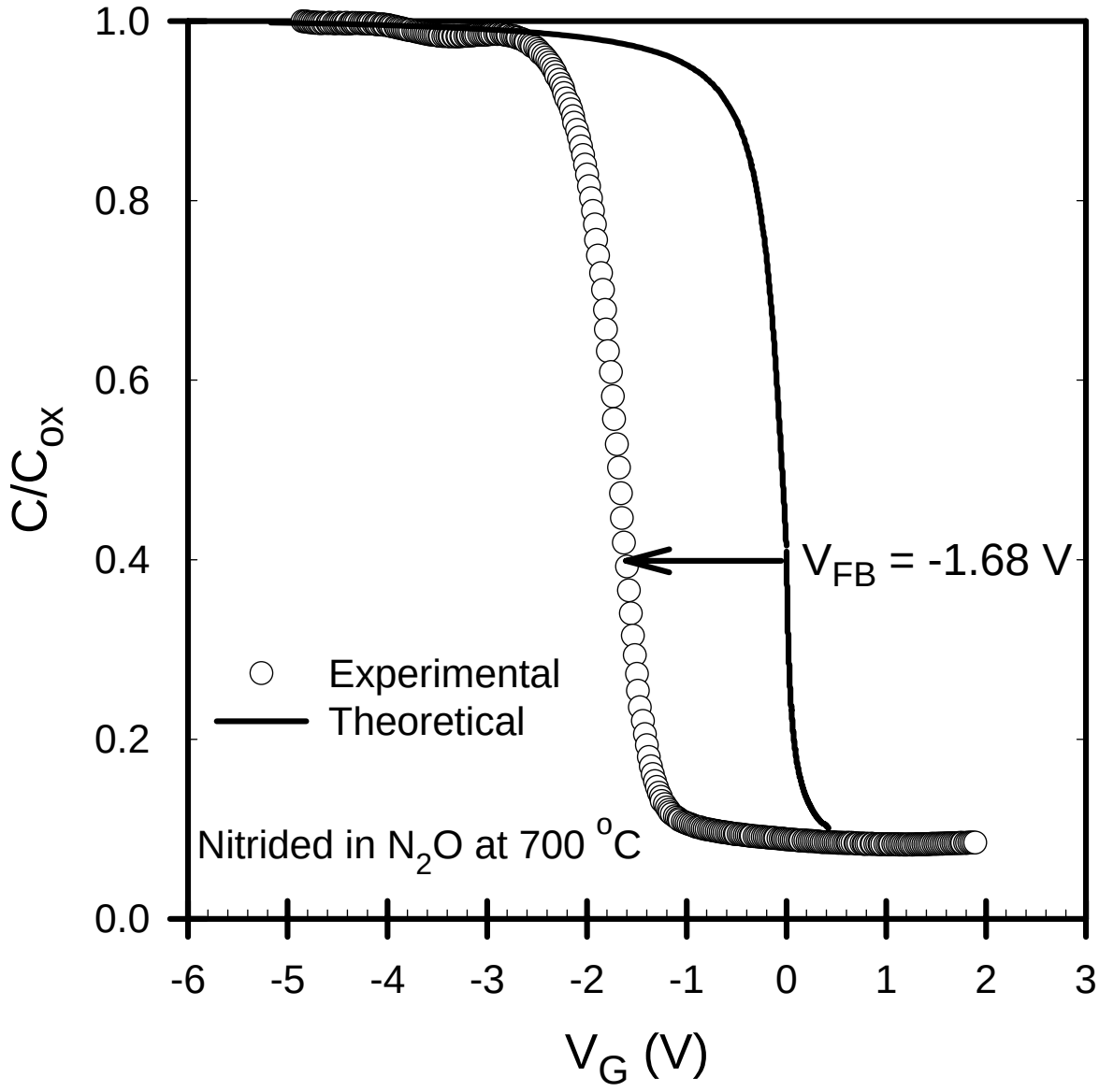

Figure 4.16 Theoretical and experimental high frequency normalized capacitance-voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at 700°C.

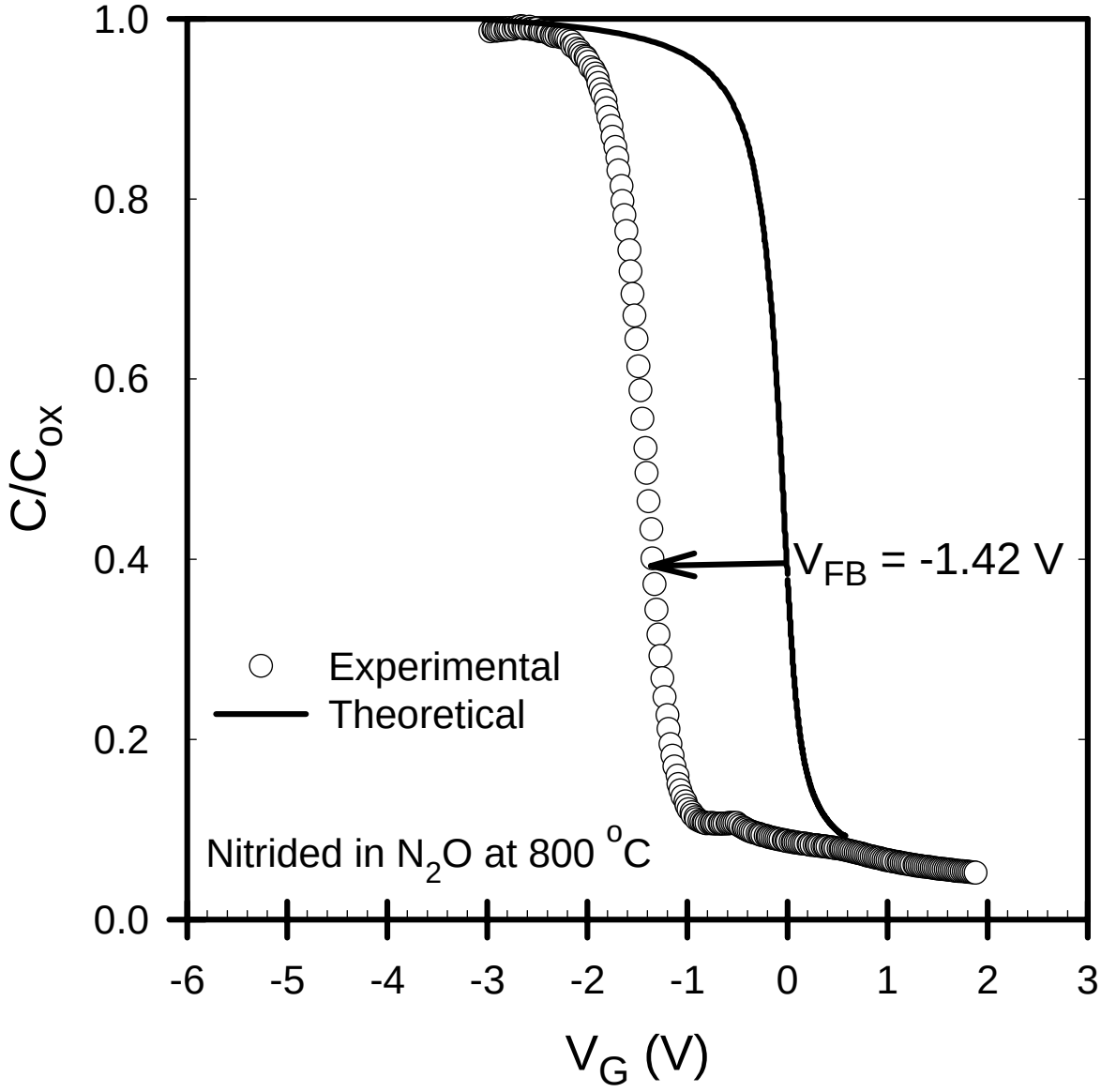

Figure 4.17 Theoretical and experimental high frequency normalized capacitance-voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at 800°C.

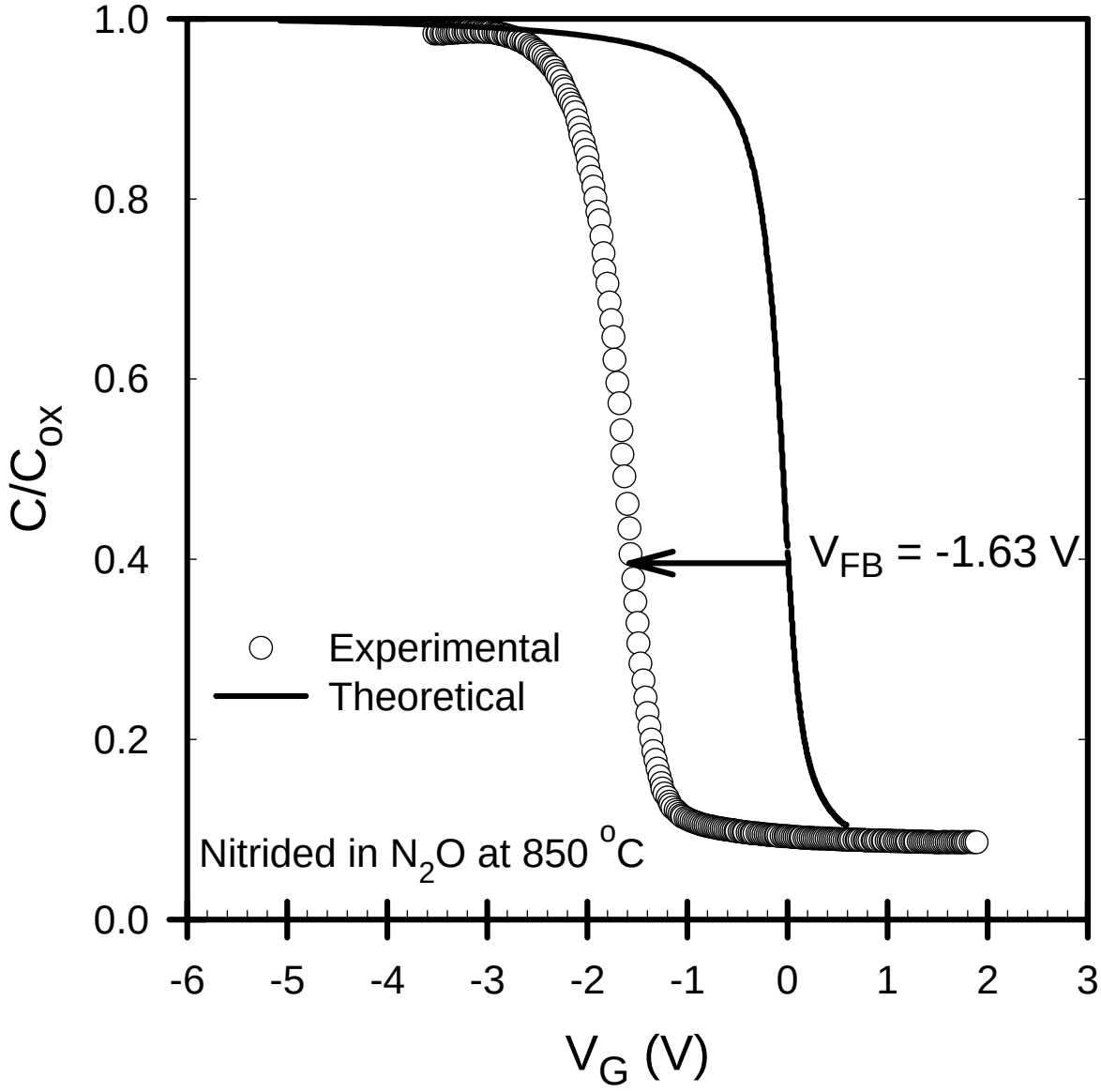

Figure 4.18 Theoretical and experimental high frequency normalized capacitance-voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at 850°C.

As a result, nitridation at 800°C gives the lowest result in terms of the effective oxide charges. As we compare, the level of N_{eff} found here for the nitridation at 800°C, it is almost equal to that found for MOS capacitors with native oxide SiO_2, which was $3.4x10^{11}$ cm^{-2} as given in the previous section. These results indicate that nitridation in N_2O gas at 800°C gives similar electronic quality oxide layer with higher dielectric constant,ε_{ox}, than the native SiO_2.

Table 4.2 Summary of the parameters extracted from the high frequency C-V measurements for MOS capacitors with nitrided Ta_2O_5 insulating layers. Data presented here are the average of six device characteristics measured from different parts of the substrate wafer

	Nitridation in N_2O			Nitridation in NH_3		SiO_2
Nitridation Temperature (°C)	700	800	850	700	800	-
Dielectric constant (ε_{ox})	3.7	4.5	3.2	3.4	6	3.9
Flat Band Voltage (V_{FB}) (volt)	-1.68	-1.42	-1.63	-1.56	-2	-1.31
Effective oxide charge (N_{eff}) $x10^{11}$ (cm^{-2})	9	4	6	6	10	3.4
Density of Interface Trap States (D_{it}) $x10^{11}$ (eV^{-1} cm^{-2})	2-4			3-5		2.5

Furthermore, the shifts between the theoretical and experimental curves are not only due to oxide charges but also to states at the oxide-Si interface. Using the theoretical and experimental normalized capacitance, C/C_{ox}, curves, the surface potential ψ_S versus gate voltage V_G curve was obtained for each sample. These are shown in Figure 4.19. Using Figure 4.19, Equation 3.32 and Equation 3.33 the density of interface trap states, Dit, was calculated using Terman's method as described in Chapter 3.The distribution of D_{it} levels obtained for the Al-Ta_2O_5-(SiO_xN_y)-Si and unnitrided Al-Ta_2O_5-(SiO_2)-Si MOS capacitors are shown in Figure 4.20 , as a function of the energy in the bandgap of the silicon. The level of D_{it} for nitrided sample changes

between $2x10^{11}$ cm^{-2} eV^{-1} and $4x10^{11}$ cm^{-2} eV^{-1} and gives the lowest level for the sample nitrided at 800 °C. When compared to D_{it} level of Set1 samples without nitridation process applied, it can be inferred that nitridation process enhances the quality of oxide-semiconductor interface and lowers the value of D_{it} for high dielectric constant insulators to the level of native SiO_2 as shown in Figure 4.21,which is an important program for the mass production of these devices.

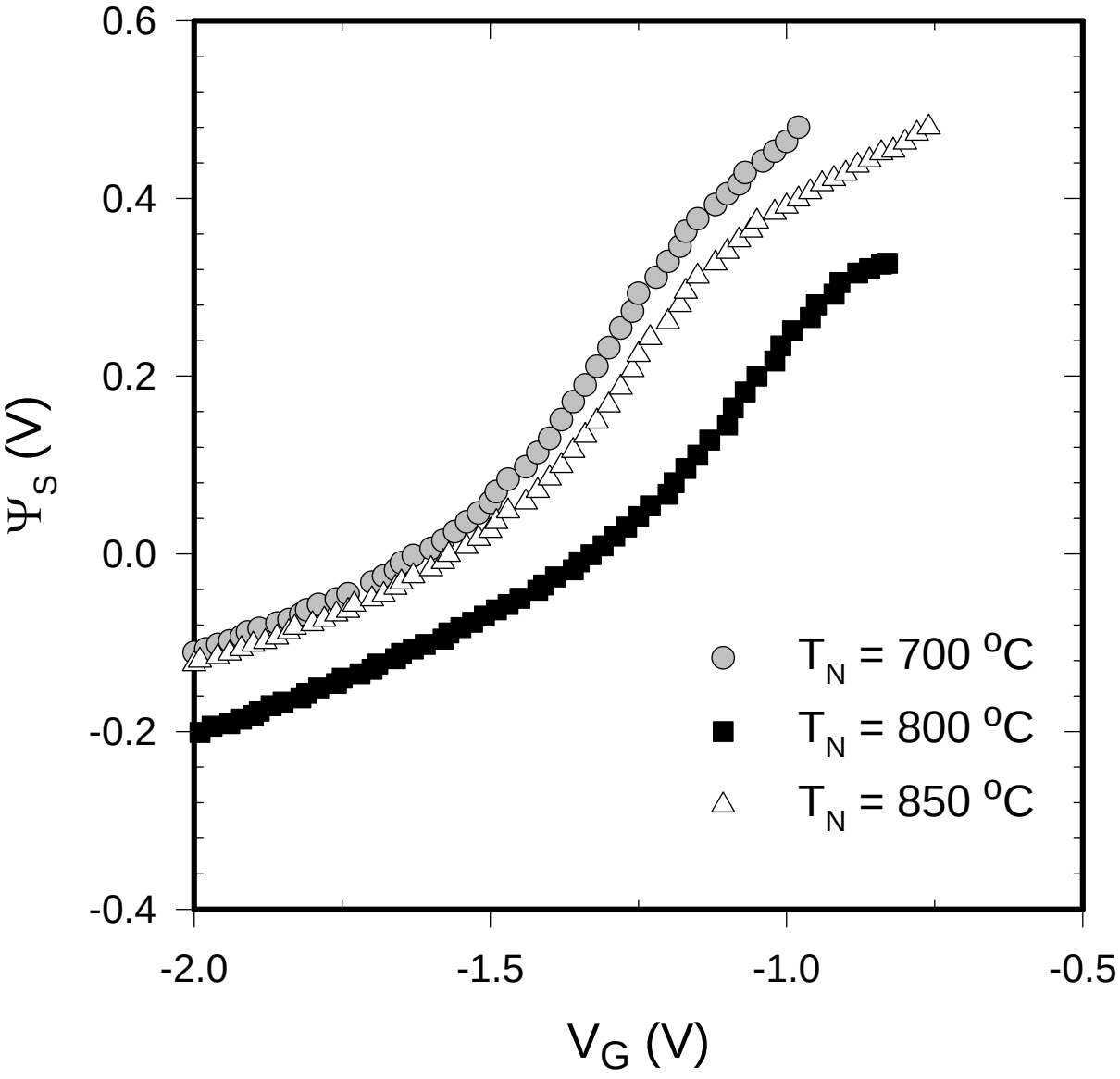

Figure 4.19 Surface Potential ψ_S versus gate voltage V_G curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared with a prior nitridation process in N_2O at 700°C, 800°C, and 850°C.

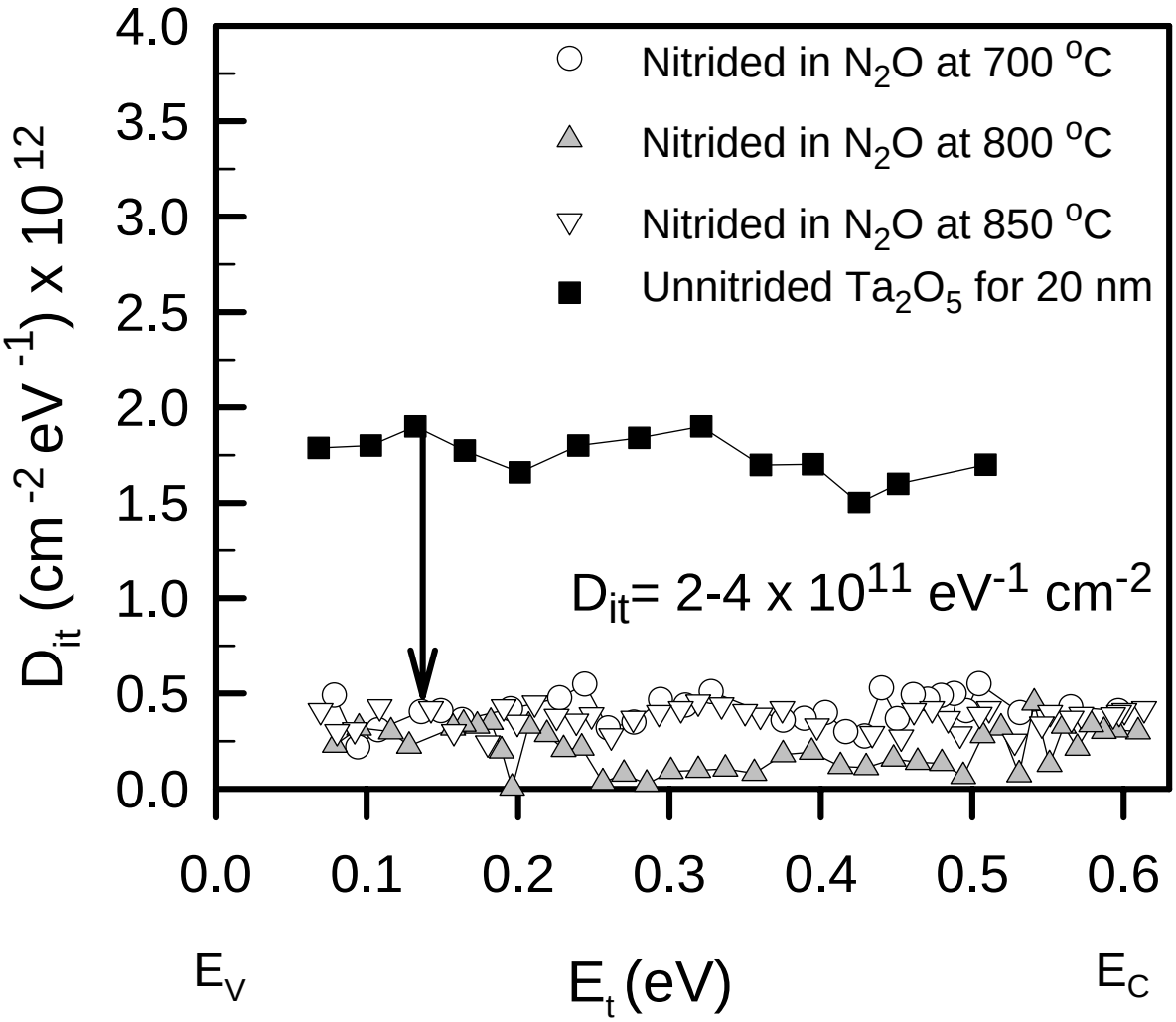

Figure 4.20 Density of Interface trap states as a function of energy in the band gap of c-Si for Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared with prior nitridation process in N_2O at temperatures 700°C, 800°C, and 850°C and that of unnitrided Al-Ta_2O_5-(SiO_2)-Si MOS capacitor with 20 nm thick Ta_2O_5 layer.

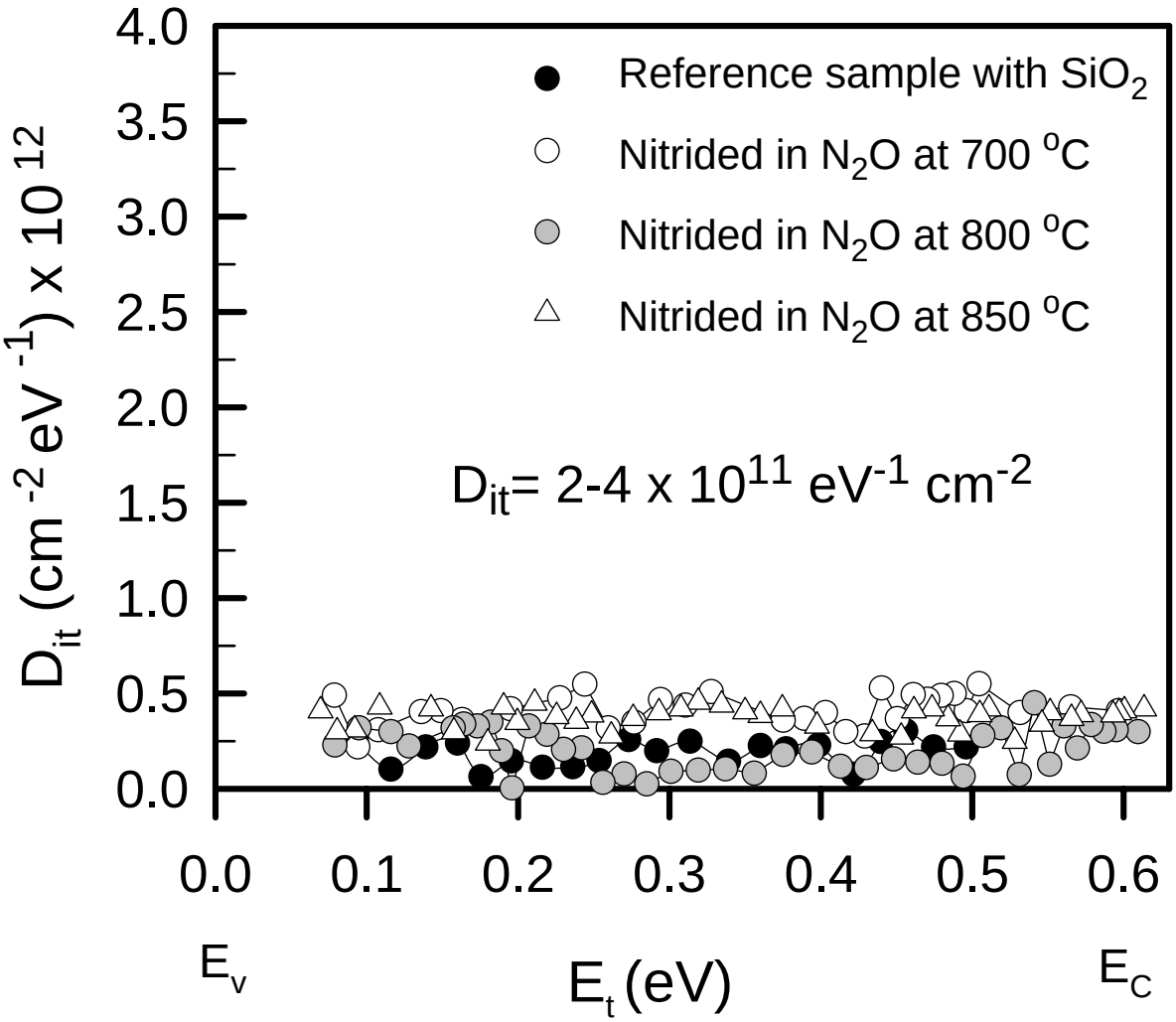

Figure 4.21 Density of Interface trap states as a function of energy in the band gap of c-Si for Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared with prior nitridation process in N_2O at temperatures 700°C, 800°C, and 850°C and that of reference MOS sample with native SiO_2 layer.

4.4.2 Nitridation of Si Surface by NH_3 Gas

As presented in previous section a prior nitridation in N_2O gas improved the oxide and oxide-si interface properties substantially. Second nitridation process of p-type silicon substrate was performed in NH_3 gas at substrate temperatures of 700 °C, and 800 °C. The thickness of the SiO_xN_y layer is around 1.5 nm to 2 nm as experimentally determined after nitridation process. After the nitridation process, a 20 nm thick Ta_2O_5 insulating layer is deposited on top of the nitrided silicon substrate. Finally, metal contacts are evaporated on top of Ta_2O_5 oxide layer to complete the MOS structure. Experimental high frequency capacitance-voltage curves are shown in Figure 4.22 for nitridation temperatures of 700 °C and 800 °C. The gate area and oxide thickness are the same for both devices. It is clearly seen from Figure 4.22 that nitridation process in NH_3 at 800 °C results in higher oxide capacitance and correspondingly higher dielectric constant as derived from the accumulation region. The parameters obtained for these two MOS devices are also summarized in Table 4.2. In order to determine the doping profile and flat band voltages, experimental $1/C^2$ versus gate potential V_G graphs are plotted together in Figure 4.23 for two different nitridation temperatures. The doping concentrations are $1.7x10^{15}$ cm^{-3} and $2x10^{15}$ cm-3 and corresponding flat band voltages are -1.56 V and -2 V for nitridation temperatures of 700 °C, and 800 °C respectively.

After determining experimental parameters such as oxide capacitance C_{ox}, dielectric constant ε_{ox} and doping concentration N_A, theoretical capacitance versus surface potential ψ_S and correspondingly theoretical capacitance versus gate voltage V_G curves were calculated for each device. Then these curves are normalized to the oxide capacitance of each device and both theoretical and experimental C/C_{ox} versus gate voltage V_G curves are obtained. These curves are shown in Figure 4.24 and Figure 4.25 for the nitridation temperatures of 700 °C and 800 °C, respectively. The flat band voltages are indicated in each figure and they are in agreement with the values obtained from the $1/C^2$ versus V_G graphs as shown in Figure 4.23. Using the flat band voltage values caused by the non-ideal effects, the effective oxide charge density, Q_{eff}, and effective number of charges per unit area, N_{eff}, are calculated for each MOS capacitor. For the oxide layer nitrided at 700 °C, N_{eff} is about $6x10^{11}$ cm^{-2} and it increases to $1x10^{12}$ cm^{-2} for nitrided sample at 800 °C, which shows a significant increase in N_{eff} due

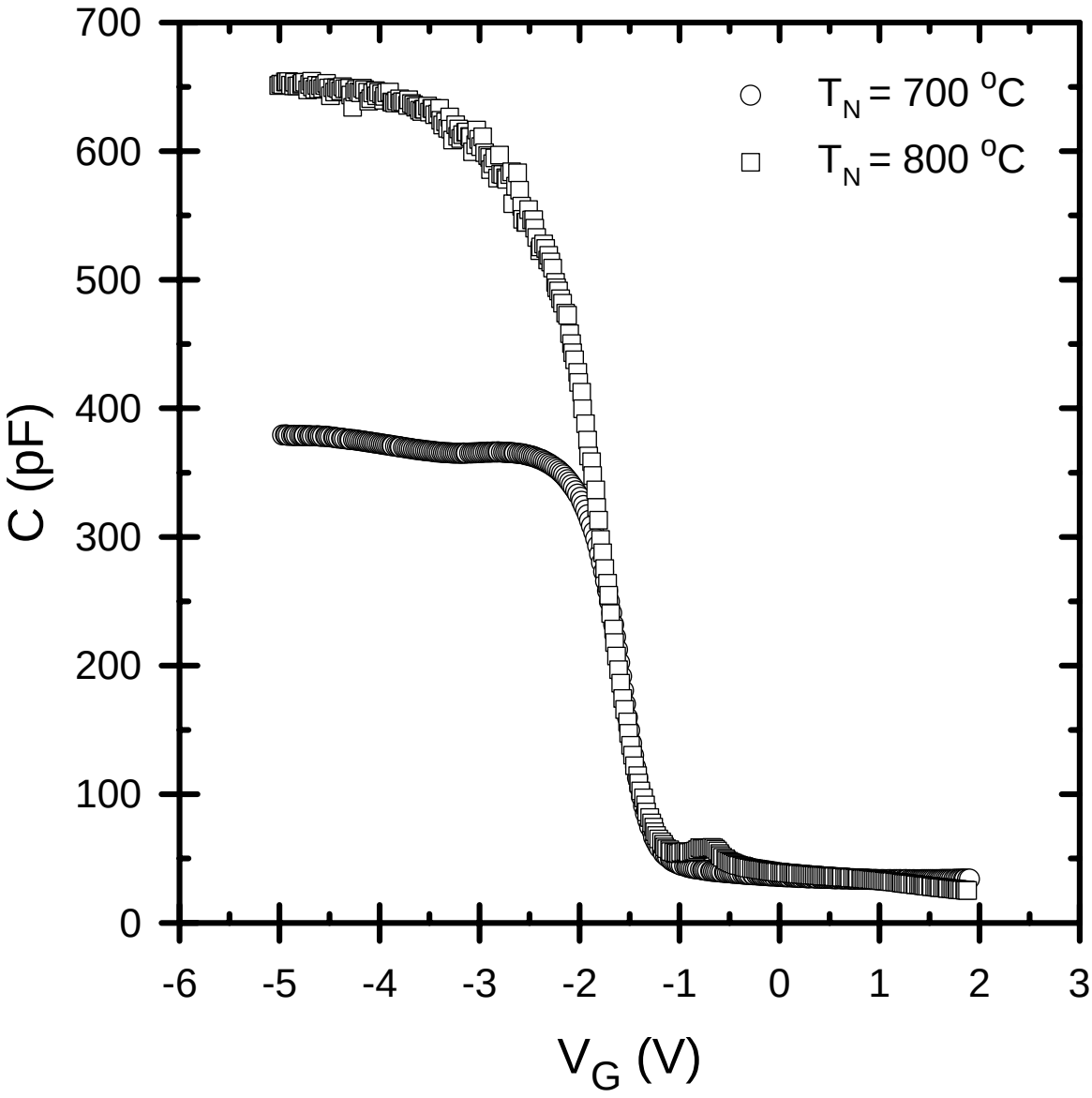

Figure 4.22 Experimental high frequency (1 MHz) capacitance versus gate voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared after a nitridation process in NH_3 gas at 700°C and 800°C.

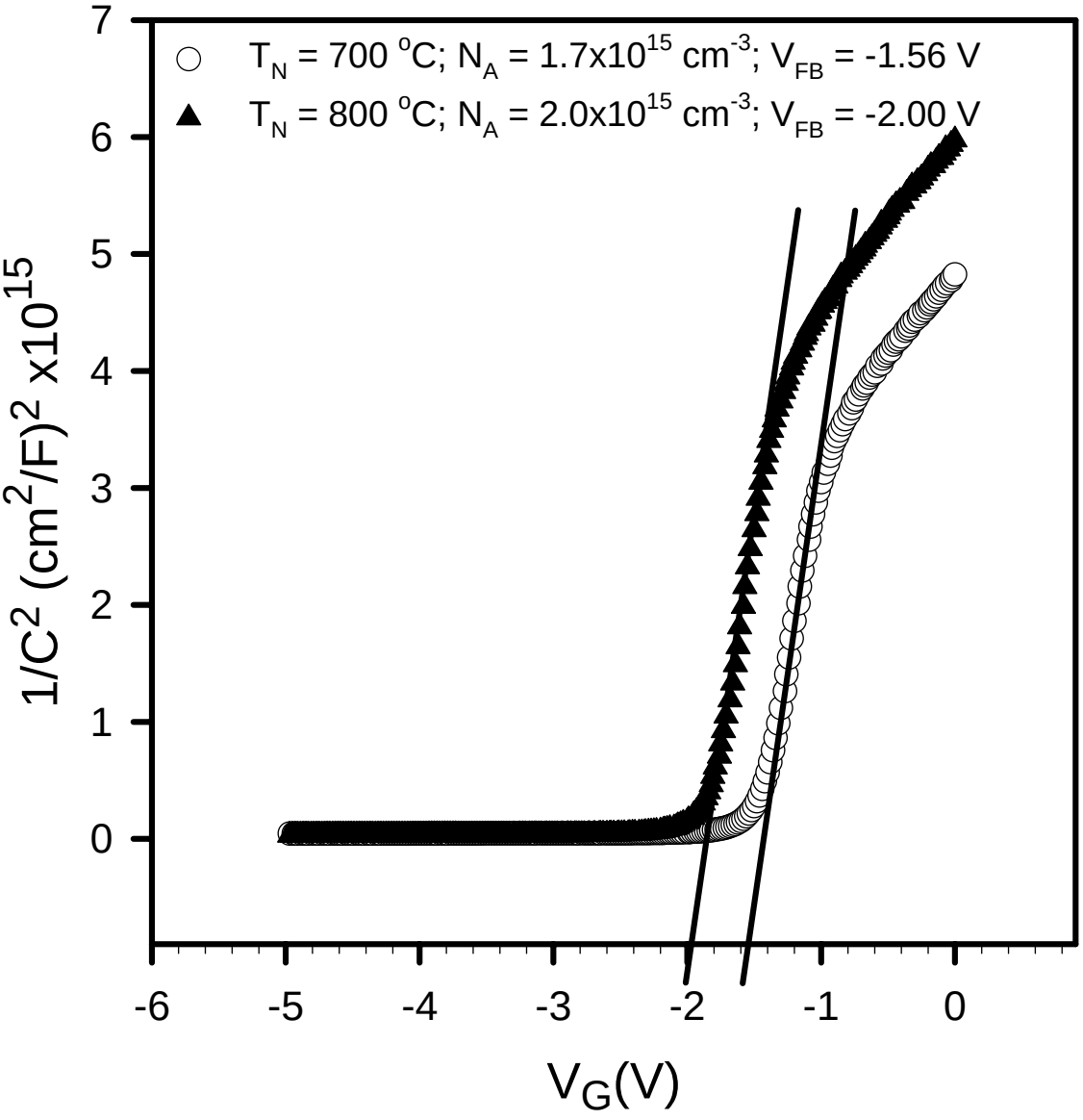

Figure 4.23 Experimental $1/C^2$ versus gate voltage V_G graph of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared after nitridation process in NH_3 at 700°C and 800°C.

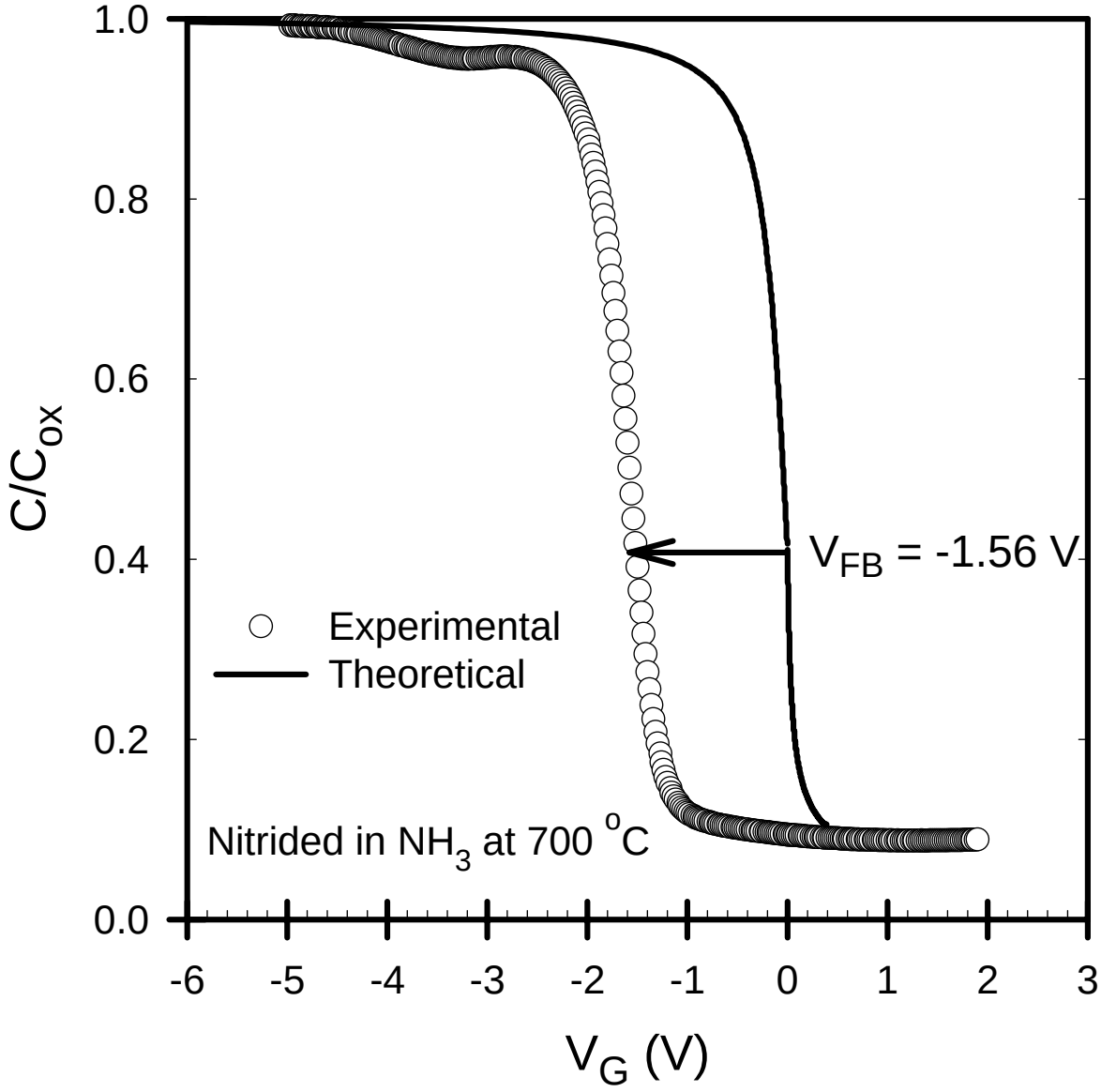

Figure 4.24 Theoretical and experimental high frequency normalized capacitance-voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared after nitridation process in NH_3 at 700°C.

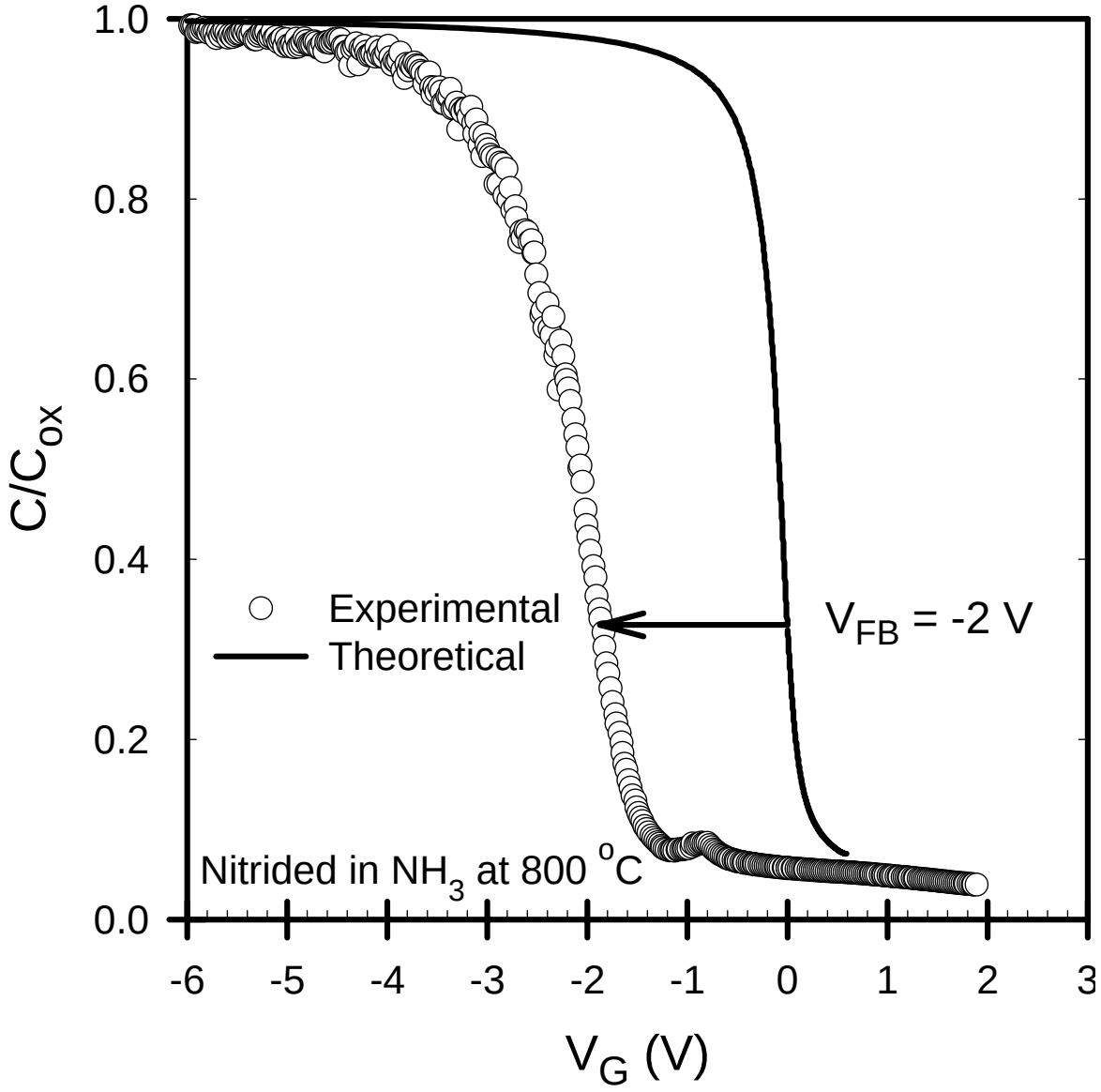

Figure 4.25 Theoretical and experimental high frequency normalized capacitance-voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared after nitridation process in NH_3 at 800°C.

to increasing nitridation temperature.

Furthermore, for the determination of density of Interface trap states, surface potential versus gate voltage V_G graph is obtained by using the ideal normalized C/C_{ox} versus ψ_S and experimental C/C_{ox} versus V_G curves. The resulting surface potential ψ_S versus gate voltage V_G curves are shown in Figure 4.26 for MOS capacitors nitrided at 700°C, and 800°C. Finally, D_{it} levels are obtained for two different nitridation temperatures by using the data in Figure 4.26 and equations given in Terman's method. The distribution of Dit levels are shown in Figure 4.27 as a function of energy. It is clearly seen that there is no clear dependence of the density of interface trap levels on the nitridation temperature in NH_3 gas environment. However, the level of D_{it} is quite low for both devices and almost at the same level with that obtained for the MOS device with SiO_2 native oxide layer. These results indicate that nitridation of p-type substrate in NH_3 gas strongly improves the Ta_2O_5-Si interface but effective oxide charges are still higher than that present in the native oxide SiO_2.

When the results of MOS devices are compared after two different nitridation process conditions, it is found that nitridation temperature at 800°C results in the best oxide and interface properties. Therefore, characteristics of MOS devices prepared with two different nitridation at 800°C are compared in Figure 4.28. Experimental high frequency C-V curves of both devices indicate that nitrided sample in NH_3 gas gives the highest oxide capacitance and correspondingly the highest dielectric constant. The values of ε_{ox} are 4 and 6 for N_2O and NH_3 nitrided samples respectively. The levels of D_{it} are almost comparable for both processes, which is around $2\text{-}3\text{x}10^{11}$ cm^{-2} eV^{-1}. however, nitridation process in NH_3 at 800 °C results in the highest N_{eff}, which is at the level of $1\text{x}10^{12}$ cm^{-2}.

In order to understand the effect of oxide uniformity and electronic quality distribution of oxide layers and Ta_2O_5-Si interface, MOS devices with different gate areas on the same substrate were investigated in detail. Experimental high frequency C-V curves of MOS capacitors prepared with nitridation process of 800 °C in N_2O gas with two different gate areas are shown in Figure 4.29. It is seen that normalized capacitance to the device area for two MOS devices with different areas do not overlap. The difference in the accumulation region indicate that dielectric constants ε_{ox} are not the same for these two devices even though they have the same oxide layer. For example, dielectric constant measured from bigger area is found to be 4.61, where the

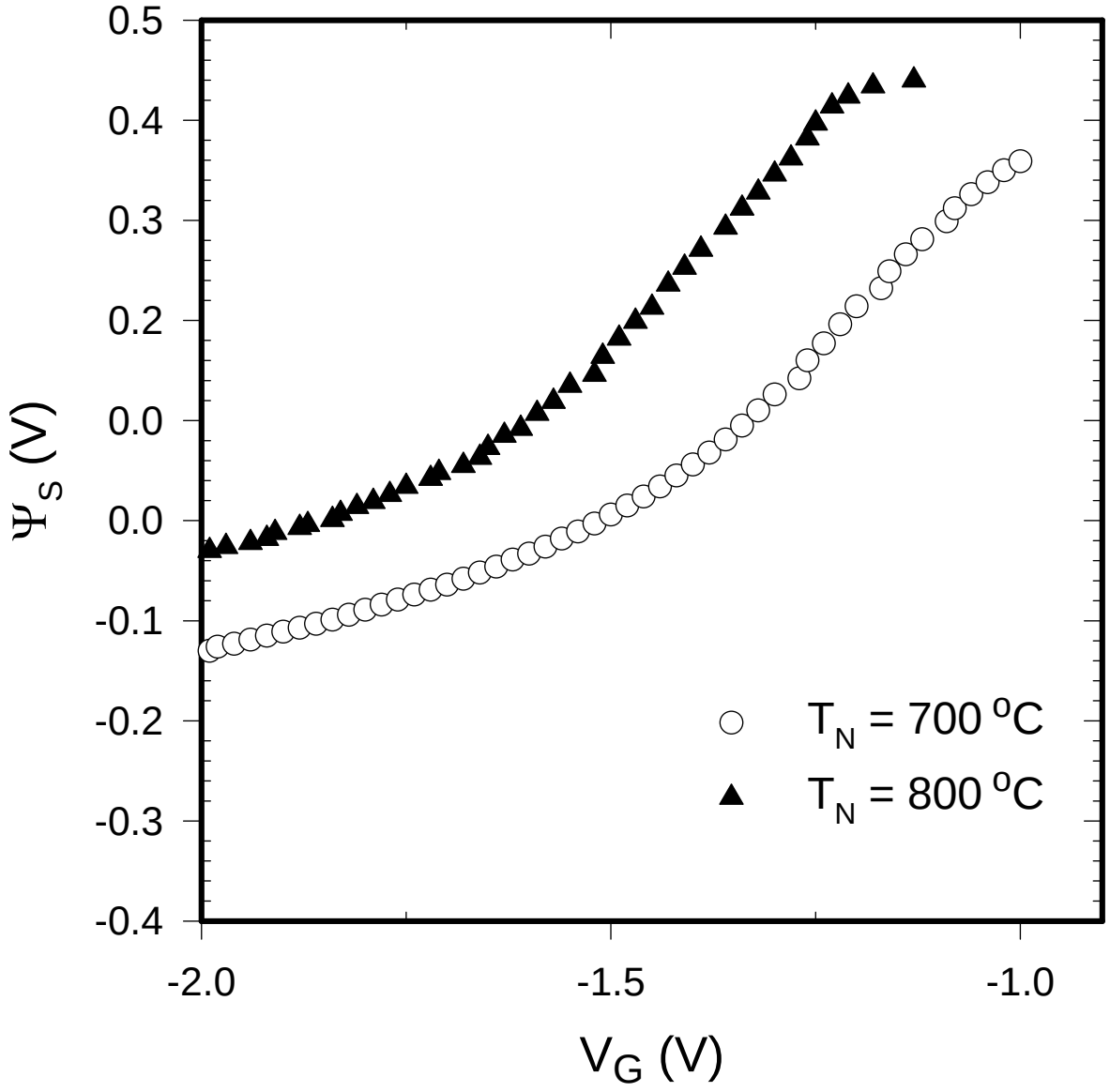

Figure 4.26 Surface potential ψ_S versus gate voltage V_G curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared after a nitridation process in NH_3 at 700°C and 800°C.

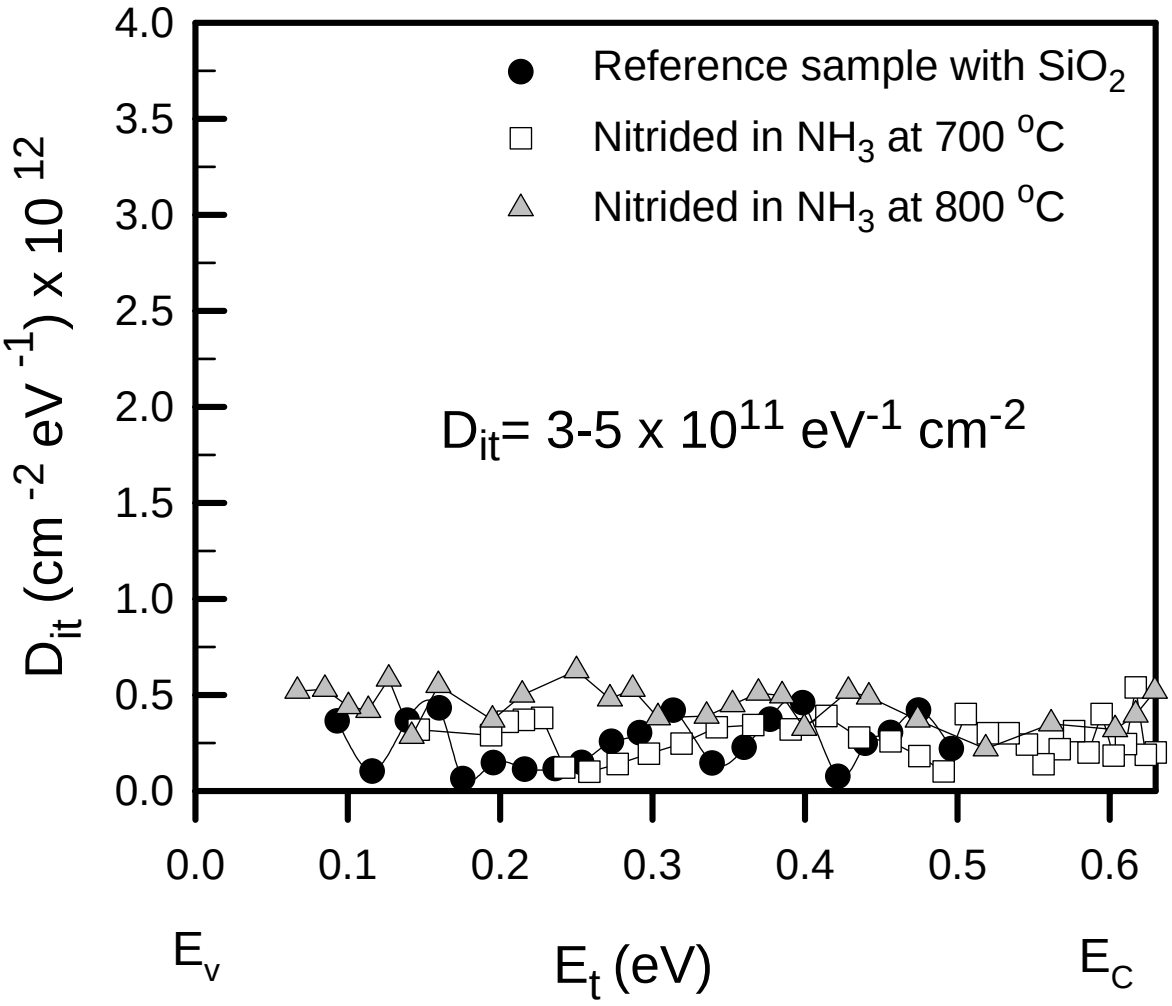

Figure 4.27 Density of interface trap states as a function of energy in the band gap of c-Si for Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared after a nitridation process in NH_3 at 700°C and 800°C and with that of reference sample with native oxide SiO_2.

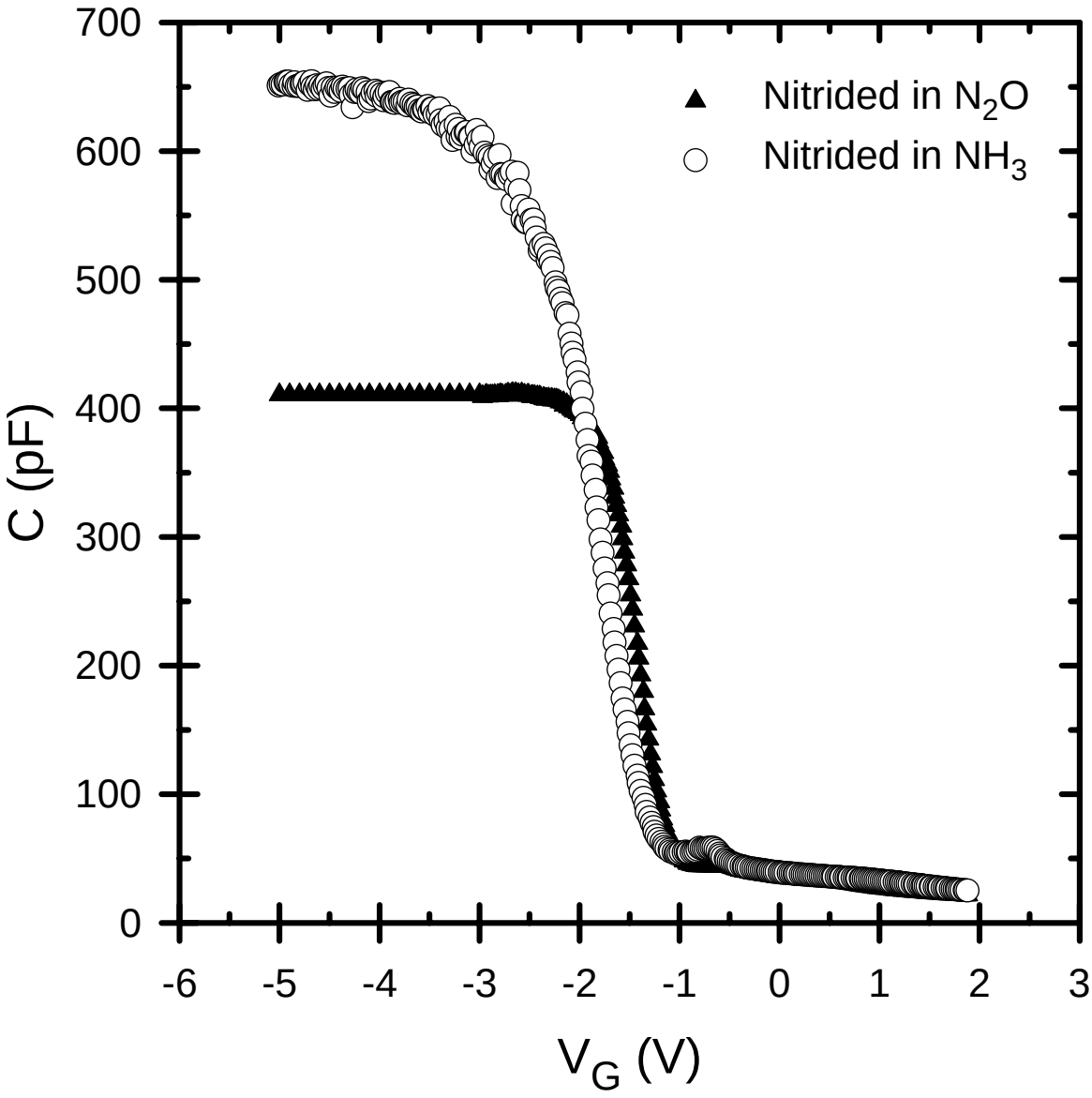

Figure 4.28 Comparison of high frequency capacitance versus gate voltage V_G curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared at nitridation temperature T_N=800°C in NH_3 and N_2O gas ambient.

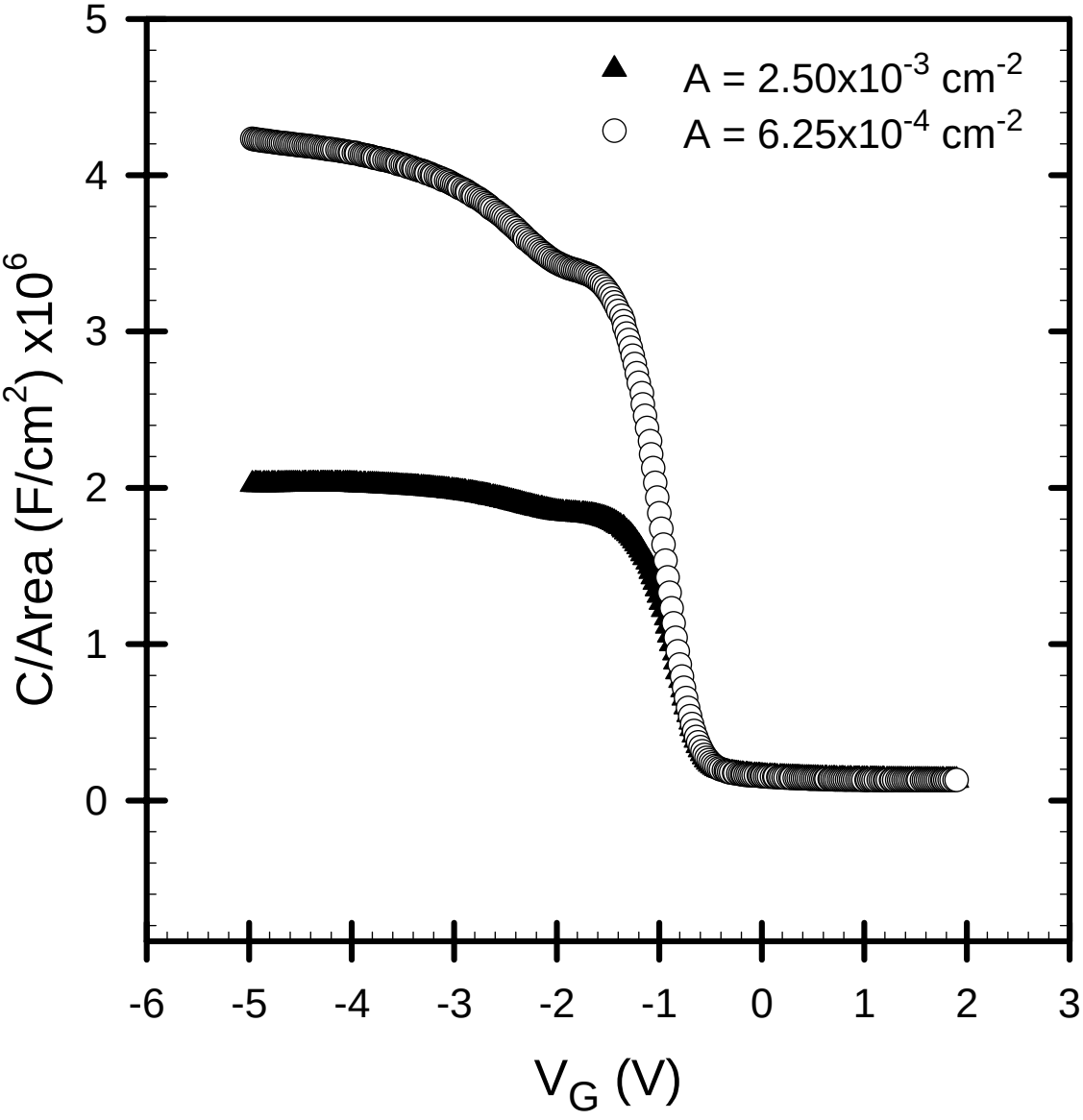

Figure 4.29 Comparison of experimental high frequency C-V curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors with two different gate area on the same substrate prepared after nitridation process in N_2O gas at 800 C.

dielectric constant measured from smaller area leads to higher values of ε_{ox} which is found to be 9.58. As a result, it can be inferred that oxide quality is not uniform throughout the substrate due to deposition type and conditions.

On the other hand, both conduction versus gate voltage and leakage current characteristics of samples are also checked. The graphs are shown in Figure 4.30 and Figure 4.31, respectively. The conduction graph again gives information about the flat band voltage, where the peak value of conductance corresponds to the flat band voltage value on the gate voltage V_G axis. In terms of leakage currents, the values obtained are above the limits of insulating layers that are used for MOS capacitors, which is a main problem of high dielectric constant insulators.

Finally, hysteresis character of high frequency capacitance-voltage curves of each MOS device studied in this thesis has been carried out by measuring the C-V from accumulation to inversion and back from inversion to the accumulation region. For most devices, no hysteresis behavior is observed indicating that both curves overlap and insignificant number of mobile ions are present in the oxide layer. However, for a few sample, a hysteresis behavior with a few mV shift in C-V curve along the voltage axis has been observed. This situation is presented in Figure 4.32 for Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor nitrided in N_2O at 850 °C.

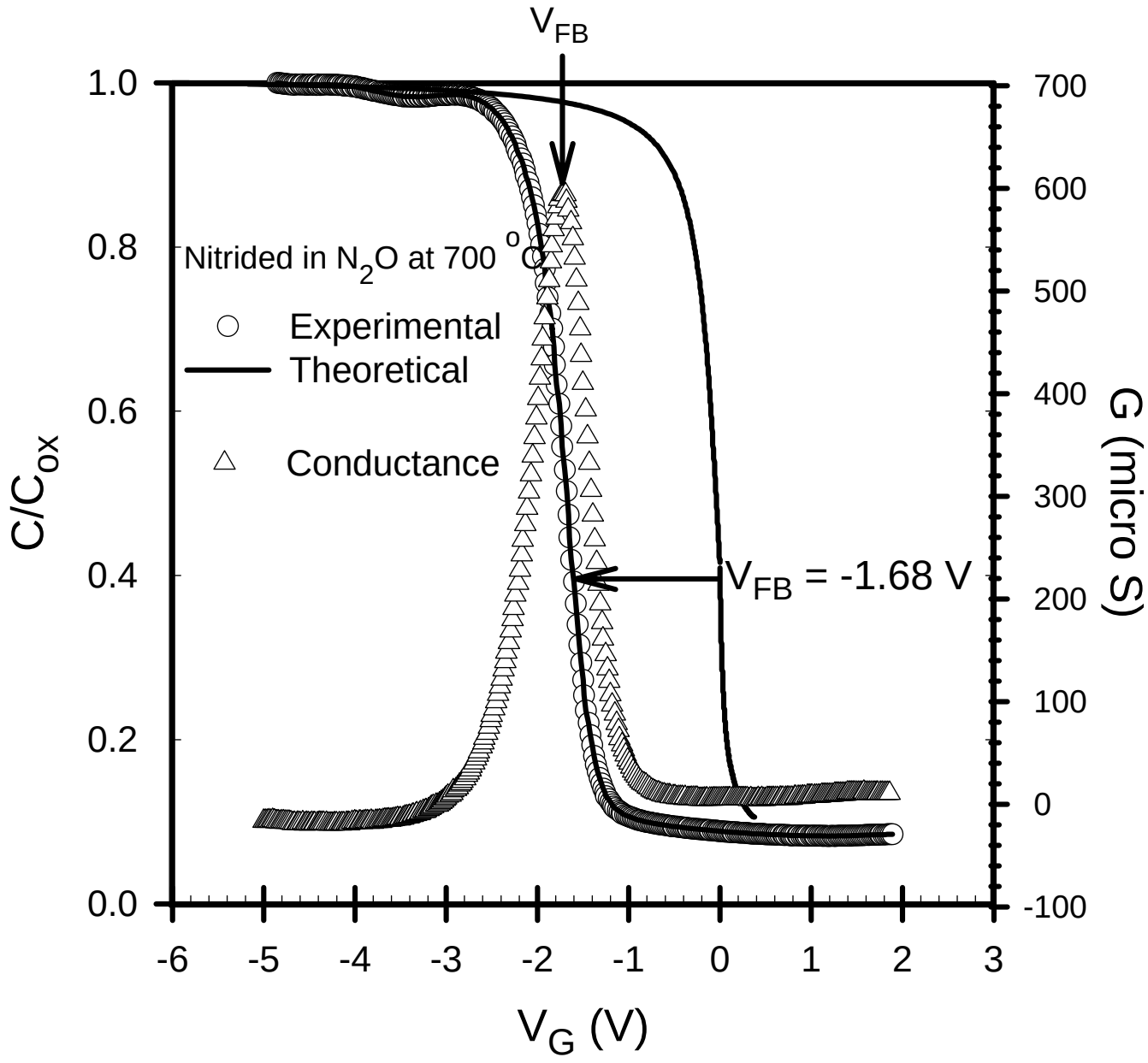

Figure 4.30 Normalized Capacitance C/C_{ox} versus gate voltage V_G and conductance versus gate voltage V_G graphs for the sample nitrided in N_2O at 700°C.

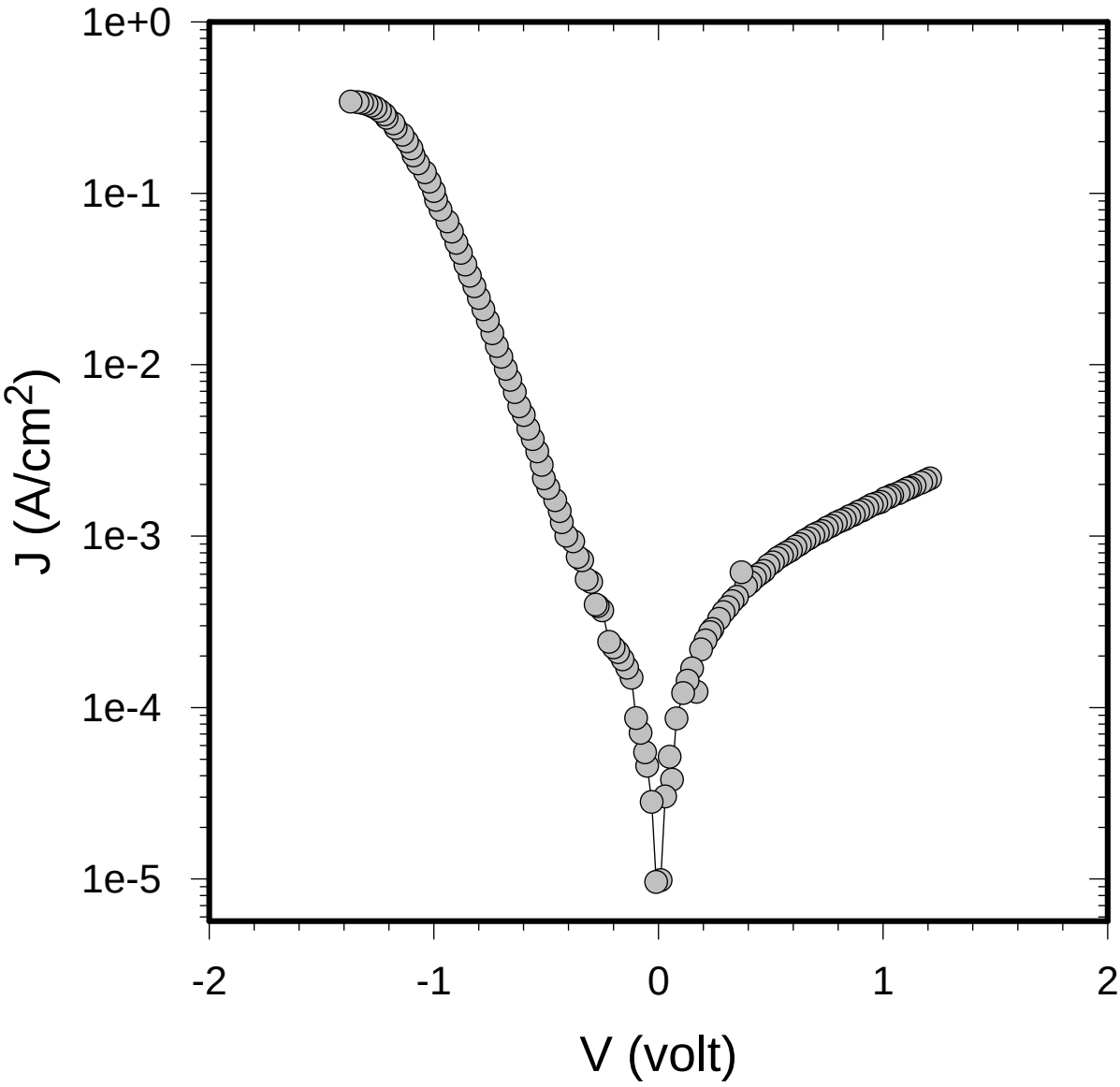

Figure 4.31 Leakage current measurements of MOS devices

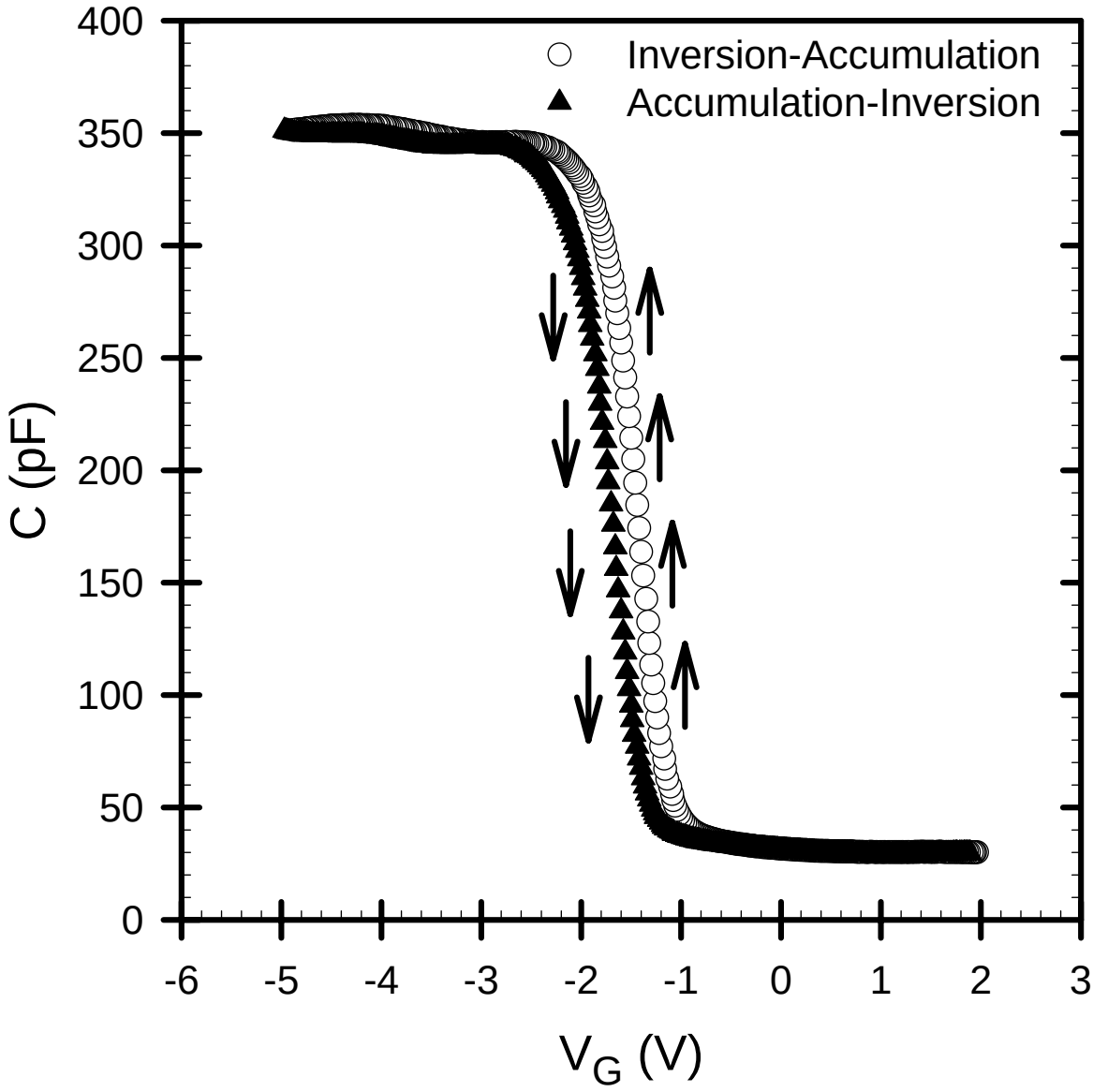

Figure 4.32 Hysteresis curve of MOS device measured from accumulation to inversion and from inversion to accumulation

4.5 Conclusions

In this thesis, capacitance voltage spectroscopy system has been established and tested by using calibration capacitors provided by the manufacturer. Then three different group of metal-oxide-semiconductor (MOS) devices have been used to investigate the capacitance-voltage characteristics of devices. First group of samples is the Al-SiO_2-Si MO>S capacitors used as a reference sample. Second group of samples is Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors with high dielectric constant Ta_2O_5 insulating layers. Third group of samples involves a prior nitridation process in N_2O and NH_3 gas environment before depositing Ta_2O_5 oxide layers. By using experimental high frequency capacitance-voltage curves and theoretical (ideal) capacitance-voltage characteristics, electronic properties of Ta_2O_5 oxide layers and that of Ta_2O_5-Si interface have been investigated in detail.

It has been found that MOS capacitors with native oxide SiO_2 has effective oxide charges in the level of $3.4x10^{11}$ cm^{-2} and interface trap density D_{it}, level is around $2.5x10^{11}$ cm^{-2} eV^{-1}. These levels are indicating the good electronic quality oxide and interface property in MOS devices. When native oxide SiO_2 is replaced by Ta_2O_5 insulating layers, the results showed that dielectric constant increased by several factors above the SiO_2 level. However, effective oxide charge and interface trap density, D_{it}, values are substantially higher than those of SiO_2. The levels of these parameters result in poor device performance in MOS operation. As an alternative procedure, a prior nitridation of p-type silicon substrate applied before growth of high dielectric constant Ta_2O_5 layers in N_2O and NH_3 gas ambient at different substrate temperatures. It was found that nitridation in both cases improved the oxide-silicon interface that D_{it} levels decreased to the level of reference sample with native oxide SiO_2. Best results were obtained for nitridation at 800 °C in both cases. However, the effective oxide charges in Ta_2O_5 layers are still higher than that of native oxide for both nitridation processes.

CHAPTER 5

DISCUSSIONS AND CONCLUSIONS

Tantalum pentoxide (Ta_2O_5) insulating layers are a potential candidate for the replacement of native oxide SiO_2, which reached to the physical limits in device miniaturization. It is a high dielectric constant material with high electrical breakdown strength. It may stay in the amorphous form after device integration, which is an important property for gate insulators. For such kind of candidates, dielectric constant value and defect levels present in the oxide or at the oxide-silicon interface are of the most important fundamental properties and they strongly depend on the deposition type and conditions. In this thesis, capacitance-voltage (C-V) spectroscopy was used in order to investigate electronic quality of Ta_2O_5 oxide layer and Ta_2O_5-Si interface of Al-Ta_2O_5-Si MOS capacitors.

One of the main goals of this thesis was to establish the capacitance-voltage spectroscopy system, which is a fundamental tool for the characterization of MOS devices. After gathering necessary instruments of Keithley 590 c-v analyzer for high frequency (1 MHz) measurements, Keithley 595 quasistatic c-v meter for low frequency measurements, Keithley 230 programmable voltage source and Keithly 5951 remote input coupler, the system setup is established by using proper BNC connections. Then, the software package is installed and modified for Ta_2O_5 insulating layers. For the measurement setup to be completed a sample box as a Faraday Cage made up of aluminium and a sample holder with a probe station by using micromanipulators and a gold tip for the gate contact are designed and manufactured in our institute. Later, the system is calibrated by using the model 5909 calibration capacitor set supplied by Keithley. C-V spectroscopy can work in three different modes, measurement of high frequency C-V, measurement of low frequency C-V or measurement of both high and low frequency C-V as simultaneous C-V technique. For most of the measurements performed in this thesis, a simultaneous C-V measurement sequence is used. The parameters that are measured during a simultaneous C-V sweep are high frequency capacitance, low frequency capacitance, conductance, leakage current and voltage. By using the capacitance value measured in strong accumulation which is the oxide capacitance C_{ox}, and by using the measured oxide thickness and gate area, it is possible to determine the dielectric constant of the oxide layer. Other device parameters

calculated as a result of simultaneous C-V sweep are, doping concentration and doping profile, flat band voltage and flat band capacitance, threshold voltage, depletion depth or thickness, density of interface trap states as a function of energy, D_{it}, effective oxide charges N_{eff}, silicon surface potential, work function difference, and series resistance. However, it should be noted that simultaneous c-v method uses both the high frequency and low frequency measurements for the analysis of these parameters as it is described in detail in chapter 3. For this reason, it is important to be careful about the low frequency measurement which is a mainly hard task for high dielectric constant insulators because of their leaky behaviour. In this thesis, simultaneous c-v analysis results are only used for native oxide SiO_2 and the analysis of Ta_2O_5 samples are performed by using Terman's method which uses the comparison of measured high frequency c-v results and theoretical ideal c-v calculations.

In this study, there are mainly three groups of samples. The first one is reference sample of Al-SiO_2-Si MOS capacitor. The second group is Al-Ta_2O_5-(SiO_2)-Si MOS capacitors prepared with different oxide thicknesses. Finally the third group is Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors prepared with a prior nitridation process applied before the deposition of oxide layer in N_2O and NH_3 gas environments an temperature ranges between 700 °C and 850 °C. The effect of replacement of native oxide SiO_2 with high dielectric constant insulator Ta_2O_5 is studied by using the c-v spectroscopy technique and the results are compared in terms of dielectric constant increase, enhancement of oxide layer and oxide-si interface due to different deposition conditions.

First of all, the system check is performed by using a reference MOS sample with native oxide SiO_2. It is clearly seen from the results presented in chapter 4 that both low and high frequency measurements for Al-SiO_2-Si MOS capacitors were successfully obtained. As a result of simultaneous C-V measurement, important device parameters such as oxide capacitance, dielectric constant, doping concentration, flat band voltage, and non-ideal effects such as effective oxide charge level and density of interface trap levels are evaluated. By using the measured value of oxide capacitance, oxide thickness and gate area, the dielectric constant of sample is found to be 3.9 which is in agreement with the value in literature. The values of N_{eff} and D_{it} obtained for native oxide SiO_2 are in the limit of good quality oxide parameters as reported in the literature (Manchanda et al. 1998). N_{eff} is around $3x10^{11}$ cm^{-2} and Dit is around $2.5x10^{11}$ cm^{-2} eV^{-1}. However, these numbers can be decreased further down when oxide layers are

prepared in an ultra high vacuum environment. For the reliability check of software analysis, these values are also calculated manually by using Terman's method. Finally, it is clearly seen that the results of density of interface trap levels for SiO_2 calculated by using Terman's method and evaluated by the software which uses simultaneous C-V method are in good agreement. This is a reliable confirmation, that the measurement system and software are working properly. Finally, the results of the reference sample with native oxide SiO_2 are used as comparison criteria when high dielectric constant Ta_2O_5 insulating layers replace the SiO_2 in MOS capacitors.

As a second group, the samples in the form of Al-Ta_2O_5-(SiO_2)-Si MOS capacitors are studied by using C-V spectroscopy technique. It is clearly seen that oxide capacitance measured in the accumulation region of high frequency C-V curve increased by several factors and scaled by the thickness resulting an effective dielectric constant of 12 ± 1 for three different oxide thicknesses. No functional dependence of dielectric constant has been obtained for the thickness ranges studied in this thesis. However, the value of effective dielectric constant is due to SiO_2-Ta_2O_5 dielectric stack. Here, dielectric constant of Ta_2O_5 is slightly reduced by low dielectric constant and very thin (1-2 nm) inevitable SiO_2 layer on p-Si. The value of effective dielectric constant at this thickness range is consistent with studies reported for Ta_2O_5 (Atanassova 1999).Even though there is an improvement in the dielectric constant , more important electronic parameters of MOS devices are the effective oxide charges present in Ta_2O_5 and interface trap levels present at Ta_2O_5-Si interface. The level of N_{eff} is around $3x10^{12}$ cm^{-2} for Ta_2O_5 layers and this is almost an order of magnitude higher than that of native oxide SiO_2. Such high N_{eff} value causes a large shift in the flat-band voltage in experimental C-V curves. Such high values of N_{eff} for Ta_2O_5 insulating layers are in agreement with the reported results in the literature (Atanassova 1999, Dimitrova and Atanassova 1998a). Furthermore, another important electronic quality criteria of MOS devices is the interface trap density, D_{it}. The level of D_{it} for Ta_2O_5-Si interface is found to be around (2-3) $x10^{12}$ cm^{-2} eV^{-1}, which is substantially, higher than that of Si-SiO_2 interface. These results indicate that Ta_2O_5-Si interface is very poor in electronic quality even though there exists an inevitable interfacial SiO_2 layer between Ta_2O_5 and silicon. Both N_{eff} and D_{it} levels are higher than minimum acceptable limit of alternative oxide layers to replace SiO_2 (Manchanda et al. 2001). Therefore, new approaches are necessary to improve both oxide and interface properties of MOS devices.

A new approach of a prior nitridation process has been recently proposed in the literature before oxidation of p-Si substrate (Novkovski et al. 2005). In this thesis, two different nitridation processes have been carried out, one is in N_2O gas and second one is in NH_3 gas at temperatures from 700 °C to 850 °C. In both processes, approximately 1.5 nm of SiO_xN_y was deposited on p-type polished silicon substrate in Class 10 clean room environment. Then, 20 nm thick Ta_2O_5 was deposited in RF magnetron sputtering system. For both group of samples, the highest dielectric constant values are obtained for samples nitrided at 800 °C for both N_2O and NH_3 gas nitridation processes. When the two samples are compared, NH_3 nitridation gives the highest dielectric constant. The level of D_{it} decreased substantially from that of unnitrided samples to that of reference sample with native oxide SiO_2. The level is around 2-3x10^{11} cm^{-2} eV^{-1}, which is in the level of acceptable limit for the replacement oxides as discussed in detail by Manchanda et al. (Manchanda et al. 2001). However, the effective oxide charges, N_{eff}, are still higher for nitrided samples. Especially, sample nitrided at 800 °C in NH_3 has N_{eff} above 1x10^{12} cm^{-2}, this high density is most probably due to the H incorporation in the oxide and formation of H-related defects, although the nitridation conditions were chosen so that less H would be incorporated in the films (i.e. lower temperature, shorter times).These results are in good agreement with the recent results given in the literature (Novkovski et al. 2005). However, for nitrided samples at 800 °C in N_2O gas, the N_{eff} values as low as 4x10^{11} cm^{-2} are obtained. This level is almost equal to that found for the reference sample with native oxide SiO_2. It can be inferred that samples nitrided in N_2O gas at 800 °C improves the dielectric constant above the level of SiO_2 and decreases both N_{eff} and D_{it} levels to that of native oxide SiO_2. These results show that a prior nitridation of p-silicon surface is a promising approach to improve both oxide and interface properties of Al-Ta_2O_5-Si MOS devices. However, further investigation is necessary to understand the nature of these oxide charges and interface properties of MOS devices with high dielectric constant oxide layers before integration into large scale fabrication.

In addition to the results discussed about Al-Ta_2O_5-Si MOS capacitors, there are also important considerations related to the deposition and structural properties of Ta_2O_5 insulating layers. It was shown that devices with different gate areas constructed on the same silicon wafer resulted in different dielectric constant values. Devices with smaller area give higher dielectric constant value than that of larger area device even though they are constructed on the same Ta_2O_5 insulator. This result indicates that Ta_2O_5

insulating layers show structural nonuniformities on the wafer. Larger area devices are affected by local micro cracks or grain boundaries which gives an average dielectric constant. However, smaller devices are less affected by the nonuniformities. These such nonuniformities also cause Ta_2O_5 insulating layer to conduct substantially that leakage current measurements are much higher than expected device limits for the MOS capacitors. Due to these high leakage currents, low frequency capacitance-voltage measurement becomes impossible to carry out for such high dielectric constant insulators. However, conductance versus voltage measurements carried out for all the samples at 1 MHz exhibits it expected characteristics that it peaks in the depletion region and at the flat band voltage of the MOS device. The values of conductance are higher for the devices studied here due to structural nonuniformities of Ta_2O_5 insulating layers. To decrease leakage current and to obtain uniform oxide growth on the polished silicon surface (nitrided or unnitrided); a prior detailed research on deposition and structural properties should be carried out before making MOS devices. Finally, these results of capacitance-voltage spectroscopy established in this thesis provide a better feedback to the deposition and structural investigation to improve both Ta_2O_5 oxide layer and Ta_2O_5-Si interface.

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