RECENT ADVANCES IN THE HARDWARE ARCHITECTURE OF FLAT DISPLAY DEVICES

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I would like to dedicate my thesis to my family who encouraged and supported me while I was taking each steps in my life.

ABSTRACT

RECENT ADVANCES IN THE HARDWARE ARCHITECTURE OF FLAT DISPLAY DEVICES

Thesis will describe processing board hardware design for flat panel displays with integrated digital reception, the design challenges in flat panel displays with integrated digital reception explained with details. Thesis also includes brief explanation of flat panel technology and processing blocks. Explanations of building blocks of TV and flat panel displays are given before design stage for better understanding of design stage. Hardware design stage of processing board is investigated in two major steps, schematic design and layout design. First step of the schematic design is system level block diagram design. Schematic diagram is the detailed application level hardware design and layout is the implementation level of the design. System level, application level and implementation level hardware design of the TV processing board is described with details in thesis. Design challenges, considerations and solutions are defined in advance for flat panel displays.

ÖZET

DÜZ EKRAN CİHAZLARIN DONANIM MİMARİSİNDEKİ SON GELİŞMELER

Tez entegre sayısal alıcıya sahip düz panel ekranlı cihazlar için ana kart tasarımını anlatmaktadır, sayısal alıcı entegre düz panel ekranların tasarım zorlukları detayları ile aktarılmaktadır. Düz panel ekran teknolojisi ve işlemci blokları hakkında genel açıklamalar tez kapsamında verilmiştir. Tasarım süreci öncesinde TV ve düz panel ekranların temel yapıları tasarım sürecinin daha net anlaşılması için verilmiştir. TV anakart donanım tasarımı iki ana süreç içerisinde incelenmiştir, bunlar şema tasarımı ve baskılı devre kartı tasarımıdır. Şema tasarımının ilk adımı sistem seviyesi blok şema tasarımıdır. Şema donanım tasarımının detaylı uygulama seviyesi tasarım kısmıdır ve baskılı devre kart tasarımı ise tasarımın gerçeklendiği seviyedir. Sistem seviyesi, uygulama seviyesi ve gerçekleme seviyesi TV işlemci anakart donanım tasarımı detayları ile tez kapsamında incelenmiştir. Tasarım zorlukları, kriterleri ve uygulanan çözümler düz panel ekranlar için detaylı olarak belirtilmiştir.

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CHAPTER 1

INTRODUCTION

The sections one to five are dedicated to brief explanations of building blocks for flat panels and display technology. Chapter six includes detailed explanation of design stage. First section is the introduction part describing basics of TV and flat panel displays, second chapter focus on flat panel display technology defining the details of the technology and driving unit circuitry of this technology. Third chapter includes common information of power regulators and includes power design for flat panel displays. Fourth chapter is dedicated to detail explanation of timer control unit which is the driving circuitry for flat panel displays. Processing board includes several audio and video interfaces and several processing building blocks, these parts are explained with details in chapter five of thesis. Addition to hardware, for system control and user interface software has an increasing act on TV system brief explanation of SW architecture on TV system is also in chapter five. The schematic and layout design stage of the processing board is in chapter six which is the back bone of the thesis. Thesis is based on two hardware design stages which are schematic and layout design of processing board. Chapter seven is the conclusion part of the thesis. The background and details on flat panel display devices hardware architectures are explained for understanding.

1.1. Flat Panel Display

Digital technology takes part in TV processing units and displays, with the development of flat panel displays screen sizes bigger than 42”, which can not be realized with CRT (Cathode Ray Tubes) become feasible. The advantages of flat panel displays over CRT can be described as larger screen size, higher resolution, smaller volume, lower weight, compatibility with digital and high resolution video interfaces. The market for flat panel displays is increasing day by day. Flat panel displays can be classified into TFT-LCD and Plasma displays. The details of these two display technologies will be described in chapter 2. Flat panel displays are based on digital

technology where the display is formed by pixels which are the smallest unit of the display. The total pixel number defines the resolution of display. The interface between the video processing board and the flat panel display is via LVDS (Low Voltage Differential Signaling) in most cases, LVDS is a digital high BW signal interface. Flat panel displays are totally digital processing based panels, input and outputs of the display are digital.

1.2. TV Building Blocks

Revolution of display technology directly affected processing board unit hardware architecture. New processing block are added and some driving units for CRT displays are removed. Digital and high BW interfaces such as HDMI (High Definition Multimedia Interface) become a standard feature of flat panel display devices. Old interfaces like as RF, SCART are also used as a standard feature because of compatibility. New interface or processing blocks are added and common interfaces or processing units are used. The processing or driving circuitries dedicated to CRT displays are removed from processing board. Our focus is on design of processing board which is used to drive flat panel displays. The detailed explanation of the processing units will be in chapter 5, but as a summary the basic building blocks for flat panel displays are as following. Tuner is the basic unit for all TV sets which provides reception of RF modulated TV signals, tuner's functionally is to convert RF band signals to IF (intermediate frequency) band. IF demodulator is the second element on RF reception path which demodulates IF band signal to base band video and audio signals. Video decoder is the third common unit used for decoding composite video to components (R, G, B and sync signals). Flat panel display devices include de-interlacer and scaler processing units. De-interlacer is the block which converts interlaced video source to progressive. This functionality is needed because flat panel displays are progressive scan type commonly, but the video source CVBS is interlaced. Resolution of the input signals are varies in wide range but the display has fixed resolution, to provide adaptation input resolution to display resolution scaler block is a must for flat panel displays. For the reception of high BW video interface as HDMI, YPbPr and VGA, units capable to receive these signals are added to processing board. YPbPr and VGA are the analog high BW video interfaces, high speed A to D converters are used

for these kinds of signals. HDMI receiver is used for the digital high BW video interface. Audio and video processing units have great role on product quality. Enhanced algorithms are used to optimize product quality. Adaptive picture enhancement algorithms are used to improve video quality and audio processing algorithms are used for sound signal quality improvement.

CHAPTER 2

FLAT PANEL DISPLAY

Current driving display technology for TV business is flat panel displays (FPD) actually FPD can be investigated in two common groups depending to their display technology. LCD displays are the first and plasma displays are the second FPD technology. Both technologies have different advantages and drawbacks. The basic difference between two types of display is, LCD displays light source at backside of the panel is continuously on and pixels which are formed by red, green and blue sub pixels act as valve which defines the output light level and color. In plasma display devices each pixel which are also formed by sub pixels RGB act as a separate lamp defining color and brightness level at that pixel point, plasma display pixels are light emitting devices separately.

Liquid Crystal is the material which is used as valve in LCD displays and plasma cells are the building block of plasma displays. Concerns of this chapter are brief explanations for FPD display basics, panel driving and backlight technologies.

2.1. TFT-LCD Displays

In most cases TFT (Thin Film Transistor) and LCD (Liquid Crystal Display) are used for the same type of display which is some times confusing. Liquid Crystal is the material used as a valve for adjusting the light level output from panel and TFT is the control circuitry of this liquid crystal material, depending to the voltage level on the crystal light intensity varies and the voltage level on crystal is controlled by transistors for each sub pixel. TFT-LCD displays are the common name used for display devices using the liquid crystal technology.

2.1.1. LCD Basics

2.1.1.1. Liquid Crystal

Crystals have perfect flat surfaces because of their molecular structures. Crystals, such as quartz, are formed when molecules form a three-dimensional matrix by attaching themselves firmly to each other in a regular pattern. They all point in exactly the same direction. Crystal are the solid materials actually, but the term "*liquid crystal*" is used to describe a substance which is in a state between a liquid and a crystal but exhibits properties similar to both (Morris 1993). Molecules in liquid crystals tend to arrange themselves until they all point to the same general direction but, at the same time the whole mass can flow like a liquid. Molecular structure of a liquid crystal is shown in Figure 2.1.

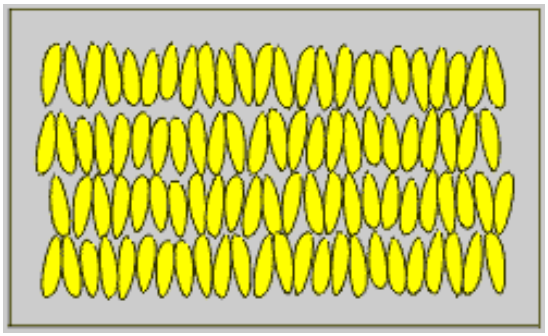


Figure 2.1. Molecular structure of a liquid crystal
(Source: Morris 1993)

Friedrich Reinitzer is the first person who observed the liquid crystal state. After heating a sample of material known as cholesteryl benzoate, it changed into a milky fluid. As the temperature increased further, the fluid changed into a transparent liquid. The milky fluid that he saw was the liquid crystal state of cholesteryl benzoate (WEB_1 2007).

Many chemical compounds exists which has the liquid crystal state, with cooling liquid or heating solid material liquid crystal state can be observed for special materials. Depending to temperature molecular structure change of liquid crystal material is shown in Figure 2.2.

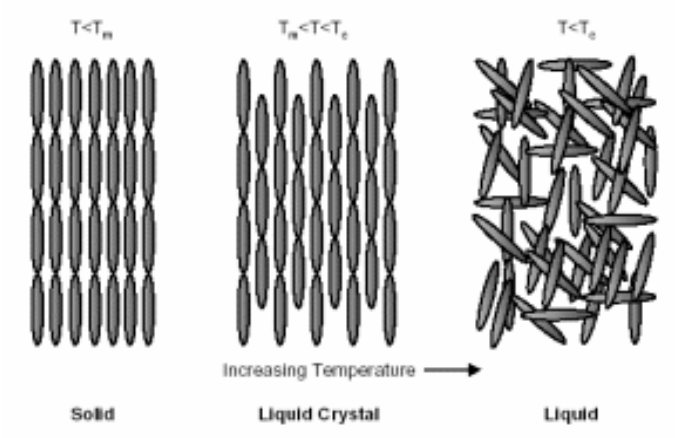


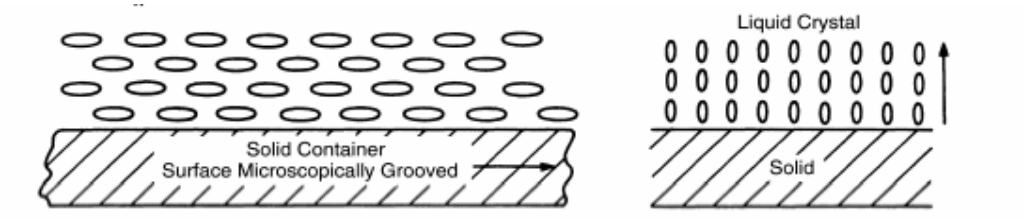
Figure 2.2. Molecular structure of LC depending to temperature

(Source: Morris 1993)

2.1.1.2. Principles of LCD Display Operation

Liquid Crystal Displays (LCD) are the most popular product in display market currently with the exception of a new technology based on light-emitting diodes which is still under development. LCD displays are used in several products ranging from small size displays used in mobile phones to large size displays used in TV sets. Although there are several types of liquid crystal material, nematic crystals are most commonly used in display devices.

Nematic material is rod physical shaped and the alignment of the crystal varies depending to electric field. The alignment of the cell without and under electric field is shown in Figure 2.3 respectively.



a) No Electric Field b) Under Electric Field

Figure 2.3. Alignment of LC depending to electric field

(Source: Morris 1993)

The alignment of rods change under electric field after a critical value but the alignment change is not abrupt, the variation has transfer curve, three stages under electric filed of rods is given in Figure 2.4 (Morris 1993).

Shapes given in Figure 2.4 are for without electric filed, under twice critical value and several times of critical electric field respectively.

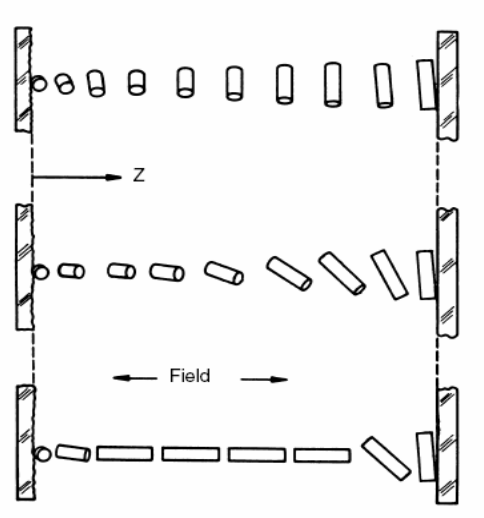


Figure 2.4. Alignment of rods under increasing electric field

(Source: Morris 1993)

Vertical alignment varies with electric field and the horizontal alignment of rods is defined by groove direction of the solid plate at the top and bottom side. Twisted nematic architecture uses this feature. The top and bottom plates are grooved orthogonally and the horizontal position of nematic is ninety degree shifted between plates. Twisted nematic structure between grooved plates is given in Figure 2.5.

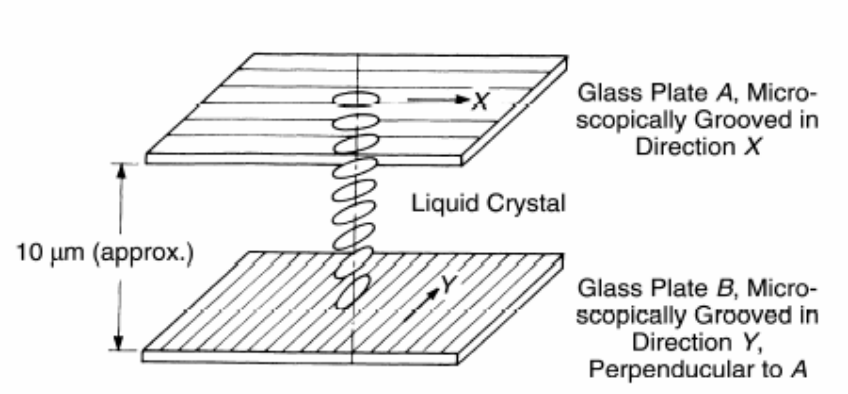


Figure 2.5. Twisted nematic architecture between grooved plates

(Source: Morris 1993)

Nematic and twisted nematic are explained before for better understanding of display operation, based on twisted nematic architecture display operation will be explained. The other LCD display architectures are the concern of the part 2.1.3 TFT-LCD Panel Technology.

Starting from the back side of the LCD panel the first element is fluorescent lamp which is always on state. The backlight technology assumed as CCFL (Cold Cathode Fluorescent Lamp) but also there are different types and architectures. Because the distribution of light can not be realized perfectly with limited numbers of lamp, diffuser is used as the second element to distribute light to whole display equally and uniformly. After diffuser light is polarized at rear part in twisted nematic architecture which is the third element, the polarization of light in one direction means passing the half of the light intensity, at this part 50% of light is absorbed by polarization filter. Absorption of light while passing through filters decrease efficiency of LCD displays. TFT arrays are the driving circuitry of the matrix structure based on rows and columns. Each pixel is addressed by applying voltage to the gate of the transistor which controls pixel and the required voltage level to control the light output level from addressed pixel is given to the drain of the transistor. Source of the transistor is connected to the metal plates which define the alignment of the liquid crystal material, the alignment of the liquid crystal is controlled by the metal plates which control electric field on liquid crystal. By alignment controlling of liquid crystal, output light level can be controlled. As explained above fourth layer of the LCD display is the TFT arrays used for addressing and as driving circuitry of LCD panels. Liquid crystal layer is the fifth element, LCD material is placed between two planes which are grooved orthogonally for twisted nematic architecture, and the electric field between plates which are controlled by TFT circuitry defines the alignment or shifting angle of the light. Liquid crystal layer defines the output light level by shifting the angle of the polarized light. For normally off panels which are in structure of ninety degree shift twisted nematic liquid crystal, the front polarizer is in the same polarization with rear polarizer. Assuming both polarizer are horizontally polarized only horizontal polarized light can pass through the both, but between each polarizer twisted nematic (TN) cell exists which shifts polarization ninety degree, under no electric field TN shifts the polarization from horizontal to vertical and vertical polarized light can not pass through front polarizer. When electric field applied to TN the shifting angle increase which means both horizontal and vertical polarization exist but only one of them in the same

polarization with the front polarizer can pass through and displayed on screen. Operation of the LCD technology is tended to be explained in Figure 2.6.

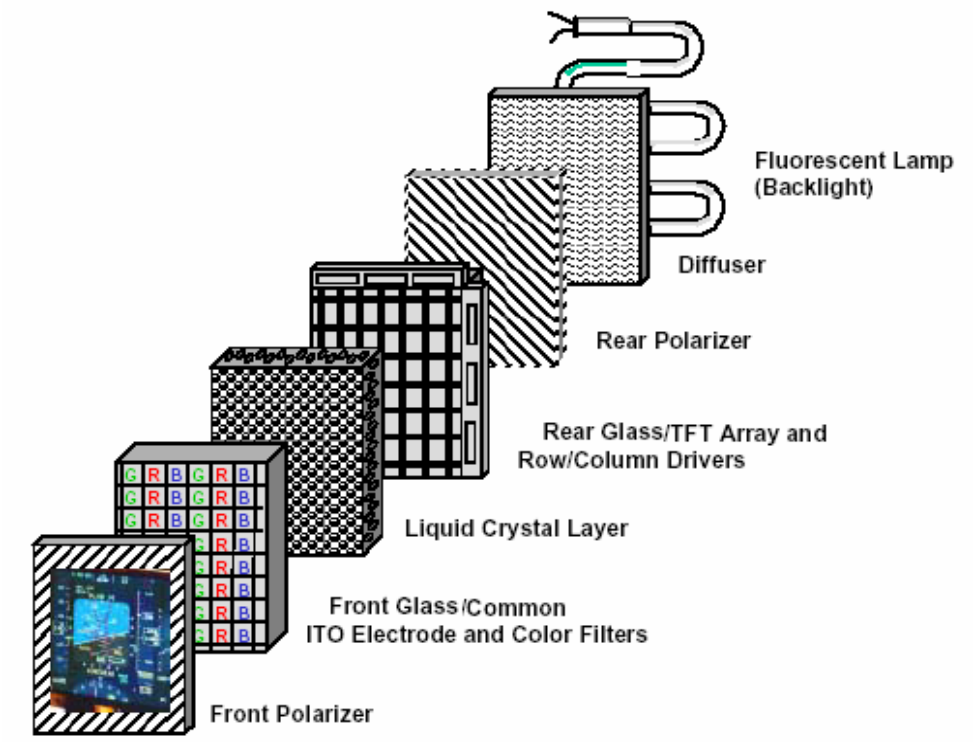


Figure 2.6. Operation of LCD display

For color display color filter in red, green and blue are used. The light coming from the first stage (fluorescent lamp) to color filters is white which includes all color tones inside. Three color filters only pass red, blue and green color range frequency individually. With the combination of these three color most of the visible color tones can be displayed on screen. But unfortunately LCD display technology has lower color range compared with CRT displays because of color filters. Color filters are the sixth layer of LCD displays which are used to display color pictures. Seventh layer and the last layer of LCD displays is front polarizer which absorbs light in the orthogonal polarization. All filters have huge losses in both density and frequency range of light. Especially color filter has the loss factor on frequency range of the color which is equal to loss of color tones, and the polarizer filters has huge factor on light intensity loss. Because of current technology level for LCD displays, efficiency and the color tone range of these types of technology panels are limited. The efficiency level is below 30% which means 70% of light is absorbed by the elements on light pass path. Accepting

CRT display color range 100%, LCD's color range is around 90%. Improvements exist in both criteria with new technology LCD displays.

2.1.2. LCD Display Drive

Addressing of the pixel is the first item in display drive. Two scheme of addressing is used, direct addressing and matrix addressing.

Direct addressing is used for low resolution displays, each pixel is directly addressed in this type of addressing scheme; for TV displays direct addressing has no usage because of resolution limitation. Matrix addressing scheme is used for TV displays, passive matrix addressing and active matrix addressing are the two types.

The first type of high information-density liquid crystal display to become commercially feasible was the passive matrix technology. It gets its name from the simple design for the way that it switches the liquid crystal cells on and off.

The individual liquid crystal cells are sandwiched between two sets of electrodes. The electrodes on the bottom layer run at right angles to the ones on the top layer. As a result, activating one row electrode and one column electrode will result in a current running through one specific cell.

The way a passive matrix creates an image is to activate each row electrode in turn, and then while a given row is selected, column electrodes are activated to turn on only those pixels in that row that are supposed to be on based on graphics display data originating from the computer or device using the passive matrix display. When the last row in the display has been scanned, the process starts over again from the top. Passive matrix addressing is the simplest and least expensive solution for medium resolution displays.

There are limitations of passive matrix design, if too great a current is run through a cell, then the adjacent cells-often those in the same column-may also be affected, resulting in ghosting. If the current is too weak, however, the cells don't switch on or off very quickly, reducing contrast and losing detail in moving images.

Drawbacks of passive matrix addressing can be summarized as following:

- Current leakage among adjacent pixels causes ghosting, or "crosstalk", and reduces sharpness, contrast;

- Because of the high twist angles of the liquid crystal, viewing angles are limited;
- Because the slow response time of this architecture, smearing of moving image elements visible.

In the late 1960's, an alternative to passive addressing was developed which uses a thin film diode in the corner of each LC pixel on the rear backplane of the two glass substrates which make up the LCD sandwich. The thin film diode was later replaced by a thin film transistor. For each pixel three transistors which are the switching active element are used in active matrix LCD (Sarma 1999).

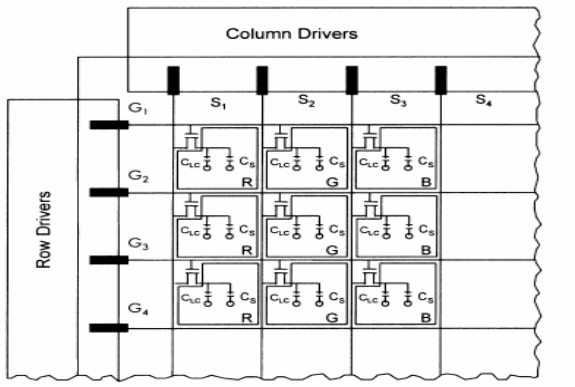


Figure 2.7. Active matrix LCD
(Source: Sarma 1999)

TFT architecture provides more efficiency, although the presence of the opaque TFT within each cell boundary means that a brighter back light is required with this addressing method, current leakage between the top and bottom substrates is reduced because of the isolation provided by the transistor. Moreover, because the transistor controls the charge on the LC material, a conventional twisted nematic alignment can be used, reducing smearing and making the display of motion video possible for the first time. The finer control also allows a number of variations in LC material and cell configuration to address the problems of ensuring wider viewing angles. This method of driving an LC matrix is called active matrix addressing and this type of LCD panels most commonly used. The structure of the active matrix addressing is given in Figure 2.7.

Transistor's gate in one row is connected to the same row select, all line is selected instantly and the data voltage is applied to the drain of the transistor, if the gate is selected the applied voltage appears at source of the transistor which drives the electrode plate. The liquid crystal material is between two plates, depending to the dielectric constant of the material capacitance between plates exists. This capacitance stores voltage level until next addressing of the row, for better storage of voltage level at one frame interval additional capacitor is used for each sub pixel.

Capacitance between two plates is given in equation 2.1 where A is the area and D is the distance between plates and Er is the dielectric factor of the material and E0 is the dielectric constant of air.

$$C = \frac{\varepsilon_r \varepsilon_0 A}{D} \tag{2.1}$$

2.1.3. TFT-LCD Panel Technology

Brief explanation of liquid crystal, operation of LCD displays, driving circuitry for addressing are described in previous parts. This part is dedicated to the structural details, operational details and different technologies developed for LCD panels.

Structural view at side cut and front cut of LCD panel are shown in Figure 2.8 and 2.9. Liquid crystal is located between two plates and spacer is used for physical space generation for LC material, the Figure 2.8 is for twisted nematic architecture, LC material locating between plates and in twisted alignment. As mentioned before each pixel is formed by R, G, B sub pixels and each sub pixel is controlled by transistor, three times panel resolution transistor exists for control circuitry and same number of sub pixels exits at color filter as shown in Figure 2.9.

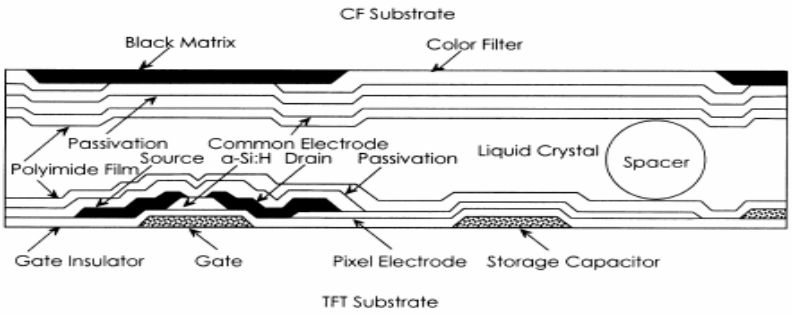


Figure 2.8. Structural view at side cut LCD panel

(Source: Morris 1993)

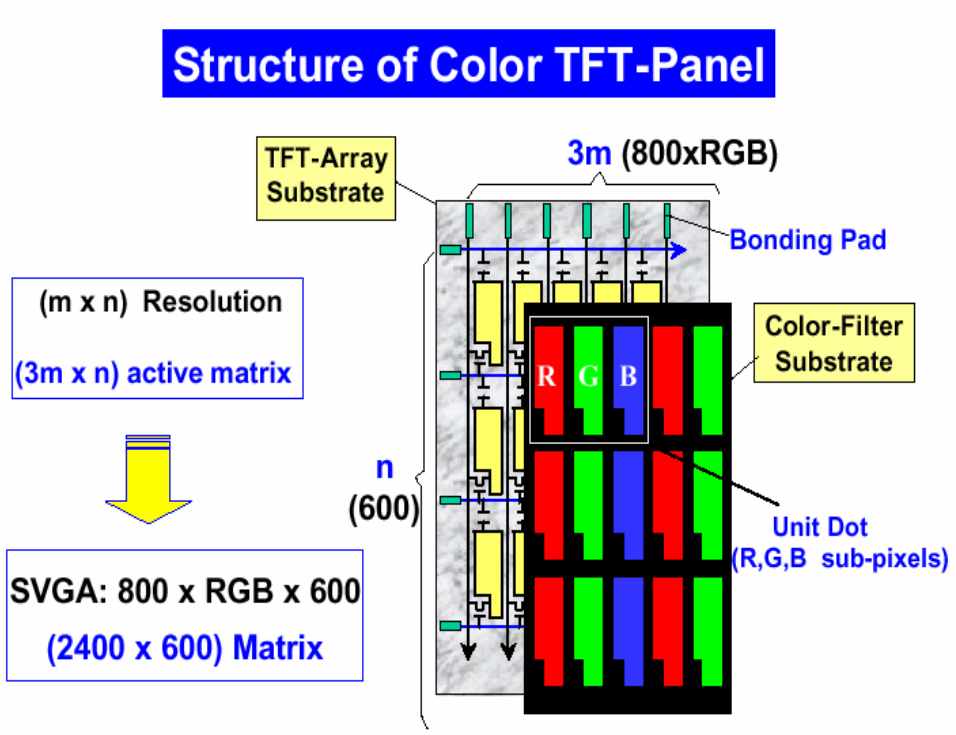


Figure 2.9. Structural view at front cut LCD panel (VGA resolution)

2.1.3.1. Twisted Nematic (TN)

The operation of LCD display explained based on TN technology in previous parts. The electrode plates at the top and bottom side are grooved orthogonally. LC material horizontal alignment at the surface of the plate is in the same direction, between each plate ninety degree phase shift of LC material is realized. For normally on panels rear polarizer and front polarizer are orthogonal. Under condition of no electric field applied to LC material, light polarization shifts ninety degree during passing through the LC, phase shifted light can pass through front polarizer and displayed on screen. For normally off panel the polarizer are the same direction, and incase of no electric field no light can pass through, black is displayed. The diagram of TN technology and operation is shown in Figure 2.10.

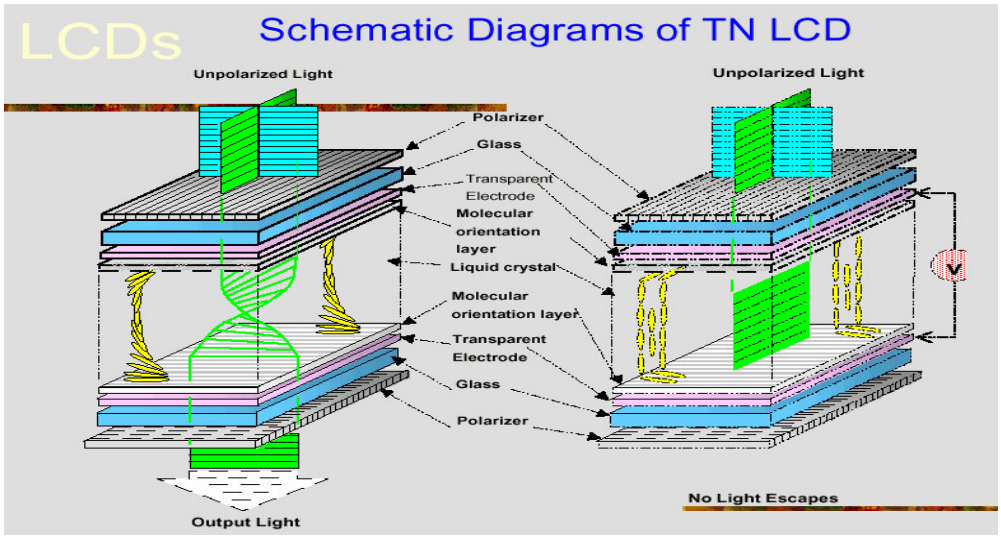


Figure 2.10. Scheme of TN technology display

2.1.3.2. Super Twisted Nematic (STN)

STN is the modified version of TN, phase shift of light while passing through STN technology is 270 degree. When the electric field applied to LC material phase shift down to 180 degree. The alignment of LC material in STN architecture is given in Figure 2.11.

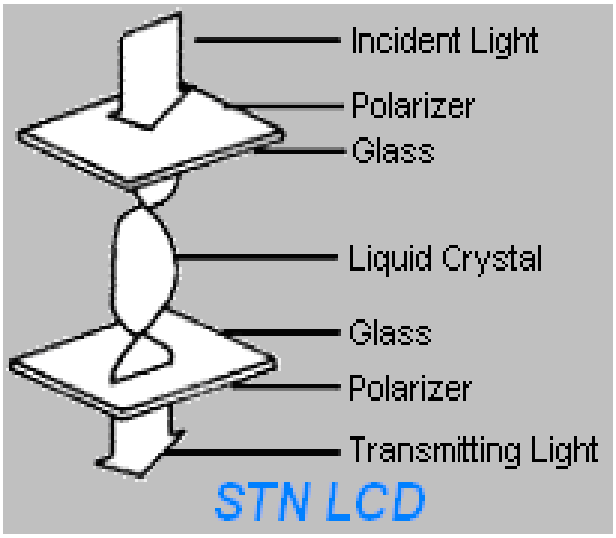


Figure 2.11. Alignment of LC material in STN structure

(Source: WEB_2 2007)

The basic advantage of this architecture is control of LC material is more sensitive to applied voltage. Considering storage capacity charge and discharge time needed in STN technology will be lower than TN because the voltage variation will be lower in STN. The relative transmission level of light due to voltage variation on LC material diagram is in Figure 2.12.

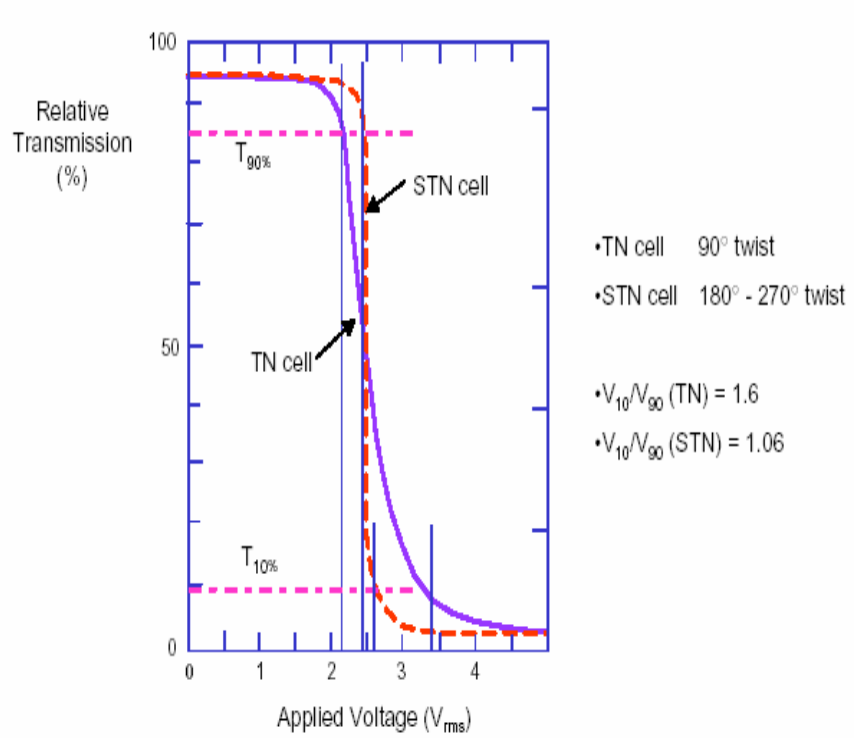


Figure 2.12. Relative light transmission level depending to voltage applied on, for TN and STN (Source: WEB_2 2007)

2.1.3.3. In-Plane Switching (IPS)

IPS technology which is developed by Hitachi display group provides wide viewing angle in LCD displays. This type of displays have the drawbacks as following, reduction of contrast ratio, less efficiency which requires stronger backlight, high power consumption, slow response time. Electrodes which control LC material is located on the same layer, alignment is controlled on horizontal direction as shown in Figure 2.13.

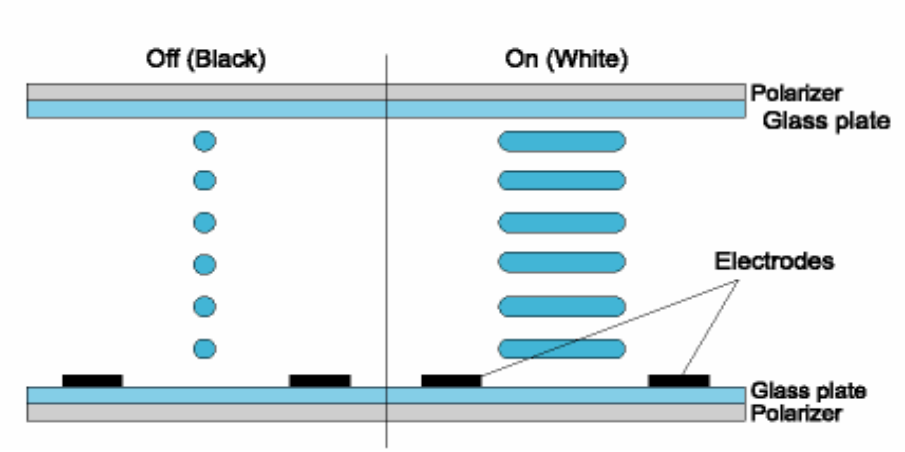


Figure 2.13. IPS architecture

(Source: WEB_3 2007)

2.1.3.4. Multi-Domain Vertical Alignment (MVA)

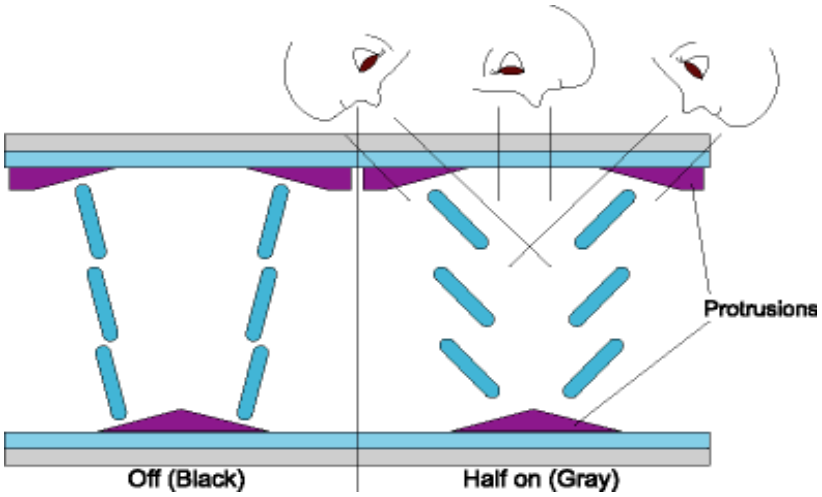


Figure 2.14. MVA architecture

Electrodes are located at top and bottom side with an angle in MVA architecture to improve viewing angle, the structured scheme is in Figure 2.14. (WEB_4 2007)

2.2. Backlight Technology

TFT-LCD panels use two types of backlight technology, Cold Cathode Fluorescent Lamp and LED backlight.

2.2.1. Cold Cathode Fluorescent Lamp (CCFL)

CCFL is the current technology used commonly for LCD panels, the locating of CCFL s and the number of lamp in one panel varies depending to panel size and manufacturer. Uniformity is the important parameter for backlight, CCFL panels use diffuser for improving uniformity of light on screen, without diffuser uniformity is limited because the number of lamp is limited physically.

Power driving circuitry of lamps is called as inverter and performance of CCFL technology backlight depended to the driving circuitry and structure. In case of lamps are located parallel in horizontal direction and if one side of the lamps are grounded, lamp is driven from the other side, light level output at the grounded side is generally lower than the other side, which decrease uniformity. The alternative driving circuitry is applying positive voltage to one and negative voltage to other side of the lamp which improves uniformity of backlight side by side.

Because of physical and electrical limitations, CCFL technology has limited performance but it is the common technology used in LCD panels currently.

2.2.2. LED Backlight

LED backlight technology will take role of CCFL technology, but current stage it is expensive and need to be validated. Several LED s are placed at the backside of the LCD panel and light is generated by these elements. The advantage of this technology the uniformity is very high because the number of lighting point is fifty times more than CCFL technology (32” CMO LCD panel use 16 CCFL (CMO 2006), for 32” LED backlight uses 500).

Special video enhancement algorithms are also used to drive LED s, most common algorithm use in LED backlight technology is for contrast enhancement. LED s are controlled individually, brightness of LED s at the dark side of the picture decreased to decrease black level. Contrast is the ratio of white level and black level, decreasing black level improves contrast ratio.

2.3. Plasma Display

Plasma displays are formed by plasma cells which control electron motion, in colored plasma display each pixel is formed by three R, G and B sub cells. Cell control electron motion less then 1uS, and 8 bit level can be realized (Morris 1993). The response time, contrast characteristic of plasma display is better than LCD displays. The operation of plasma cell is similar to lamp, depending to duty cycle cells luminance output varies. In Figure 2.15 full color plasma display cell is given.

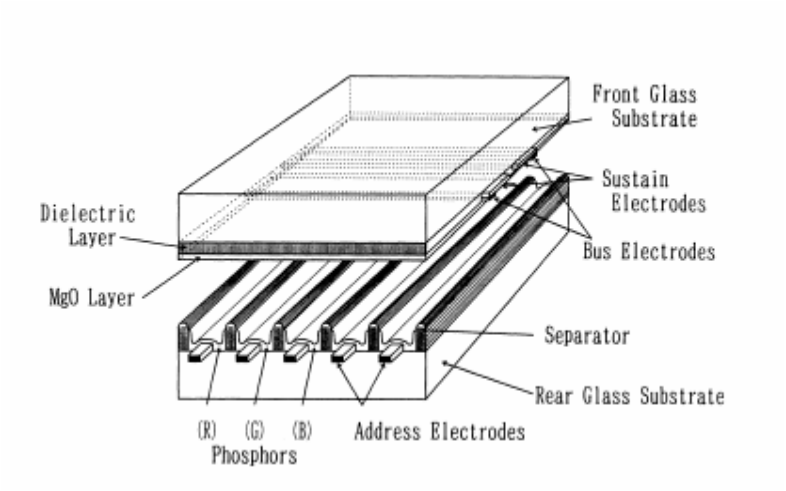


Figure 2.15. Full color plasma display cell
(Source: Weber 1993)

CHAPTER 3

POWER CIRCUITS

The aim of power design is to achieve low power dissipation. Power dissipation on regulators increase consumed power and heat in system, designs not considering power dissipation usually need heat sink which increase system cost.

3.1. Low Power Design

Low voltage supply for the circuits is the basic criteria of power consumption. Low voltage design decrease power consumption, to lower the operating voltage device geometry should be decreased, for example with 0.35u channel length technology 3.3V supply is required but in 0.18u process 1.8V and in 0.13u process technology 1.2V used as supply voltage. Threshold voltage of MOS devices decrease as the channel length minimized which provides to use lower supply voltage. High frequency operation of digital circuitries can be realized with reduction of device geometry and supply voltage. Reduction in channel length provides low voltage designs but the linearity of the circuitries affected, for digital circuitries operation this effect is not much critical but for analog circuitries linearity is an important parameter and most of the time analog circuitries use higher supply voltages. When the digital core is using 1.2V, analog circuitries such as ADC use 3.3V supply for stability and linearity.

MOS transistor system design normally has zero current flow through supply to ground at steady state but parasitic capacitors are charged and discharged during operation, MOS systems power consumption can be given in equation 3.1 (WEB_5 2007), where V is the supply voltage, C is the total parasitic capacitance and F is the operating frequency.

$$Pconsumption = \Delta V^2 xCxF \tag{3.1}$$

Power consumption of a system should be considered at system level design, power consumption increase heat. PCB layout design and placement of components

should be done considering heat dissipation. Power consumption increase by square of supply voltage, low voltage system design decrease power consumption, by this way PCB area can be decreased, components can be placed near to each other in case of power dissipation of components reduced.

3.2. DC / DC Regulators

In current technology LCD TV processing board circuitries needs several voltage levels varies between 1.2V to 24V for different uses. Voltage ranges between 1.2 ~ 1.8V supply voltage is used for core circuitry supply, 2.5V is generally used for memory interface with DDR, SDR memories and also for external devices, 3.3V is used for several I/O interface, 12V or 24V supplies are needed for audio amplifier. Different kind of voltage regulators are used to supply all needed voltage levels on processing board from the voltages coming from power board. AC line voltage is converted to DC voltages at power board, but all DC voltage levels which are used in processing board side can not be supplied from power board in many applications. Remaining voltages are generated by linear regulators and switching regulators on processing board.

3.2.1. Linear Voltage Regulator

Linear regulators generate a lower output voltage level than applied voltage level to input. The minimum voltage difference between input and output is called dropout voltage. The voltage drop across a linear regulator should be bigger than the dropout voltage for proper operation. For linear regulators the output current is equal to the input current. Voltage difference between input and output multiplied with current is dissipated power on regulator. Because of this reason linear regulator are low efficient and power dissipating regulators. Linear regulators are convenient for low current applications, depending to the internal structure drop out voltage can be minimized, the linear regulators with low drop out voltage called as LDO (Low Voltage Dropout) regulator. Linear regulators advantages compared with switching regulators are, they are noiseless devices, have stable output voltage (ripple free), do not need external passive elements like inductance and cost effective solutions can be realized for low current applications. The drawback of linear regulators is when used in high voltage

drop and high current operation, power dissipation increase which also increases heat. In this case additional precautions should be taken such as heat sink area on PCB.

The simplest architecture of linear regulator is based on zener diode and one transistor as shown in Figure 3.1. Voltage level on zener diode is fixed and independent from sink current from load resistance output voltage level is almost fixed. This kind of linear regulators output is almost fixed but depending to output current and thermal condition output voltage level can varies.

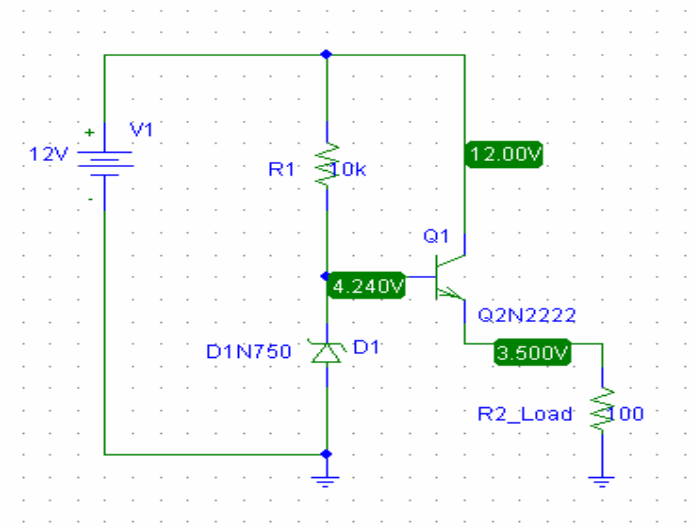


Figure 3.1. Simple linear regulator architecture (shunt regulator)

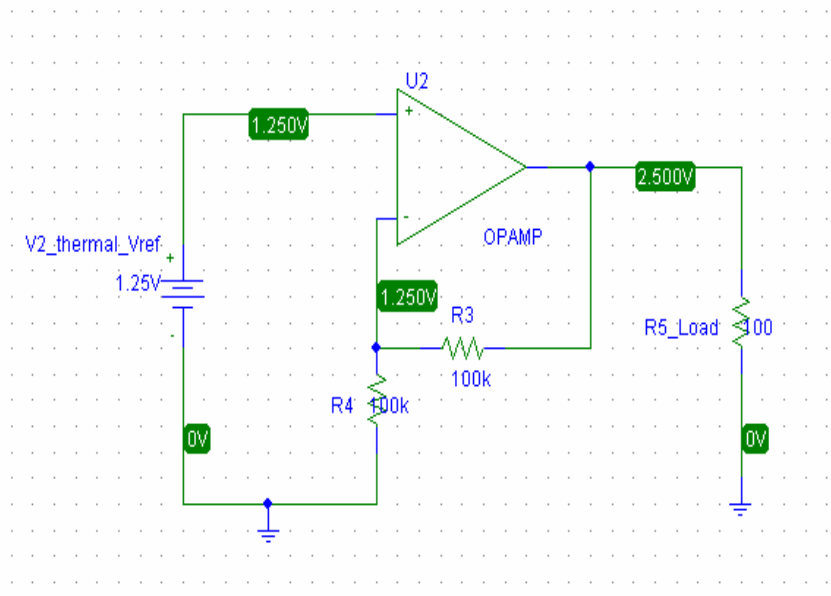


Figure 3.2. Linear regulator with feedback circuitry

With feedback circuitry and internal comparator, adjustable type of linear regulators can be realized as shown in Figure 3.2. Band gab reference circuitry used for reference voltage generation which is thermal independent. Band gap reference circuitry is given in Figure 3.3 (ONSEMI 2002). The Vref voltage is given as in equation 3.2, by choosing R1, R2, I1, I2 reference voltage can be realized independent from temperature.

$$\Delta V_{ref} = \Delta V_{BEQ3} + \Delta T_J K \left(\frac{R_2}{R_1} \right) \ln \frac{I_1}{I_2} \tag{3.2}$$

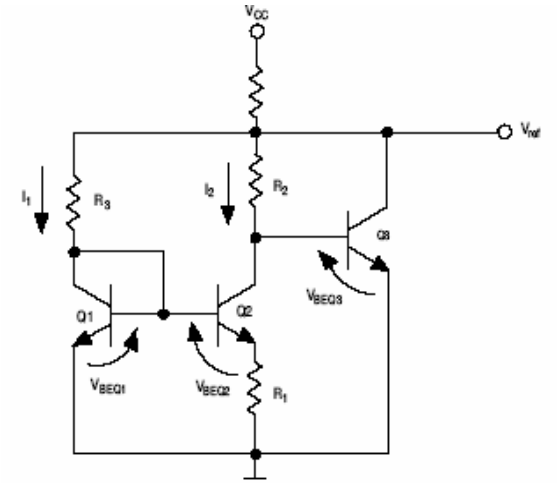


Figure 3.3. Band gab reference circuitry

(Source: ONSEMI 2002)

3.2.2. Switching Regulators

Efficiency is the most important parameter for power design, because of high efficiency of switching regulators they are convenient for efficient power design. Switching regulators use external passive elements to store energy when switched on and stored energy is used during off state. This mechanism increase efficiency of system.

Switching regulators disadvantages are, noise radiation because of switching mechanism, output ripple voltage is high which needs external passive filter and storage elements such as inductance and capacitance. Passive elements introduce cost to total switching regulator topology.

Depending to voltage in-out characteristic there are two categories of switching regulators, buck converter and boost converter.

3.2.2.1. Buck Converter

Buck converters are used to implement efficient systems with the cost of larger PCB size, complex and noisy circuitry. In step-down topology output voltage level is lower than input voltage level.

Simple buck converter circuitry is shown in Figure 3.4. At on state of transistor M1, inductance L1 charges and at off state of M1, L1 discharges.

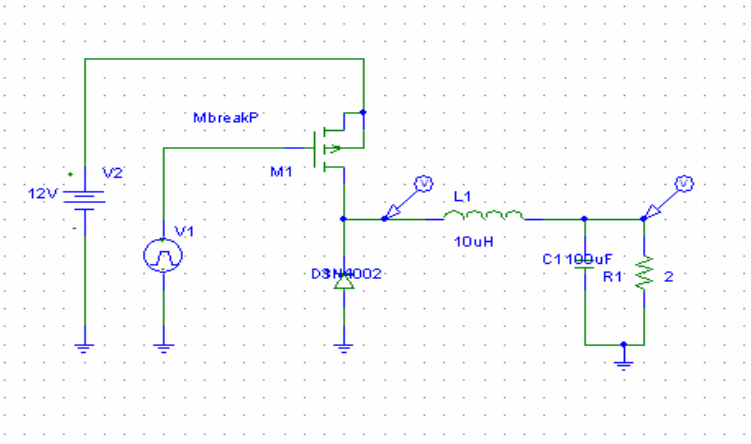


Figure 3.4. Buck converter

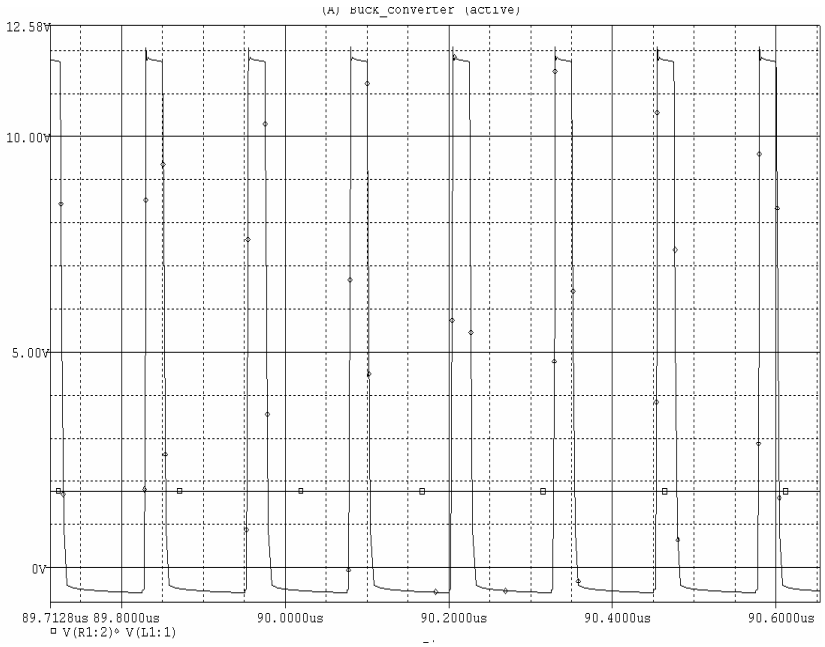


Figure 3.5. Voltage level at two nodes of L1

With the 20% duty on time and 2 ohms output load, output voltage is around 1.8V. Graph in Figure 3.5 shows voltage level at two nodes of inductance (L1). The node of L1 connected to the transistor is switching between 0V and 12V and after LC filtering DC output is provided at the other node of the L1. Diode is used to prevent negative voltages.

3.2.2.2. Boost Converter

A simple boost converter regulator schematic is given in Figure 3.6. When transistor M1 is open current flowing through L1 stores energy on L1, when M1 switches off the stored energy boost voltage level at M1 drain, by this way input voltage level is boost to upper level. Depending to load resistance (R1) pulse width is controlled for fixed output voltage. Normally there is a feedback from output to stabilize output voltage level. For fixed load with the component values given in Figure 3.6 and pulse durations 0.4us on and 1us off, output of the regulator is 9.8V. Detailed voltage characteristics are given in Figure 3.7.

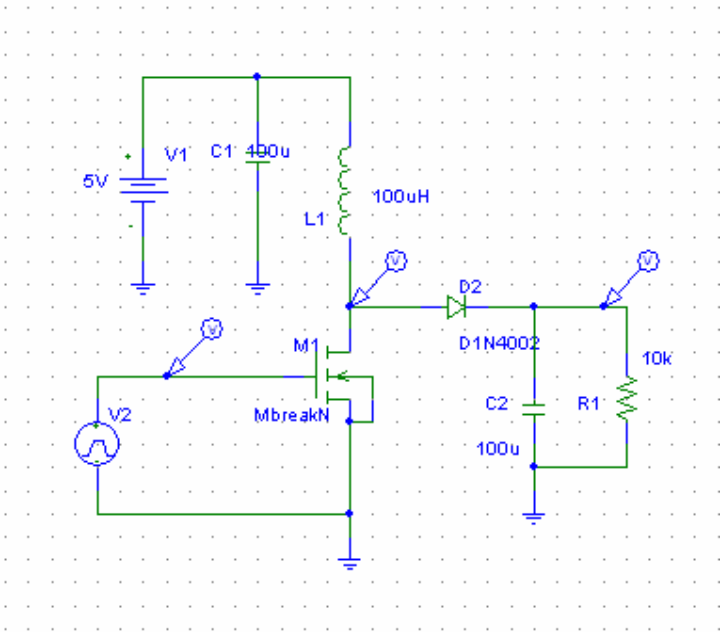


Figure 3.6. Simple boost converter

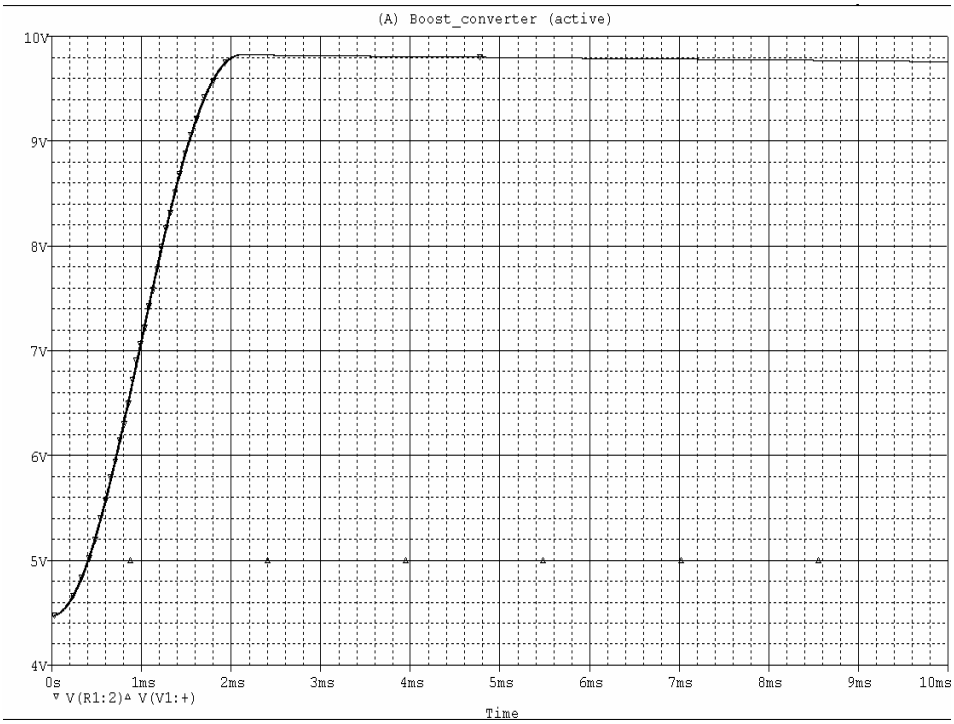


Figure 3.7. Input and output voltage for the circuitry in Figure 3.6. Red line is the input voltage and green line is the output voltage versus time

CHAPTER 4

TIMER CONTROLLER (TCON)

Each display type has specific driving timing, gamma response and response time. As the common interface between processing board and panel controller low voltage differential signaling (LVDS) is commonly used for flat panel displays. Timing controller unit is the interface between processing board and panel. TCON unit's functions are the data format conversion, timing controlling specified to panel, response time improvement and gamma correction.

4.1. LVDS RX / RSDS TX Data Conversion

Reduced swing differential signaling is the connection interface between TFT-LCD Panel module and timing controller. LVDS is the commonly used interface between processing board and timing controller module. Data conversion from LVDS to RSDS is the first property of timing controller unit (TCON). Both LVDS and RSDS interfaces are designed for high data bandwidth, reduced EMI and low power considerations. Actually RSDS is designed after LVDS and has similar properties like high speed, reduced interconnect, low power, low EMI (WEB_6 2007). Both signaling interface use differential low voltage signaling in which for LVDS 350mV and for RSDS 200mV. Low voltage differential signaling architecture provides to realize reduced EMI, low power and high data bandwidth. Unlike to LVDS which use 7:1 serialization, RSDS use 2:1 serialization scheme and also unlike LVDS RSDS do not include data control signals in RGB data. In Table 4.1 comparison between LVDS and RSDS is given (WEB_6 2007).

Table 4.1. Comparison RSDS and LVDS

Characteristic	RSDS	LVDS
Output Voltage Swing	+/- 200 mV	+/- 350 mV
Termination Resistor	100 ohms	100 ohms
Output Drive Current	2 mA	3.5 mA
Data Serialization Scheme	2:1	7:1
Data Content	RGB	RGB and Data Control
Application	Intra System Interface	System-System Interface

The block diagram of the LCD module is given in Figure 4.1. Our focus in this part is the TCON board which is the interface between processing board and TFT-LCD panel. Commonly LVDS output from video processing board is used and LVDS receiver at TCON board decodes LVDS data to row data, after specified video processing and data format conversion RSDS data from TCON board to panel drivers are sent. RSDS is in simple architecture which provides to realize simple receiver architecture at panel driver side to reduce panel system cost. Panel drivers include RSDS receivers and DAC converters, LCD cells are driven by analog voltage level. TCON unit's first functionality is the data conversion between LVDS to RSDS.

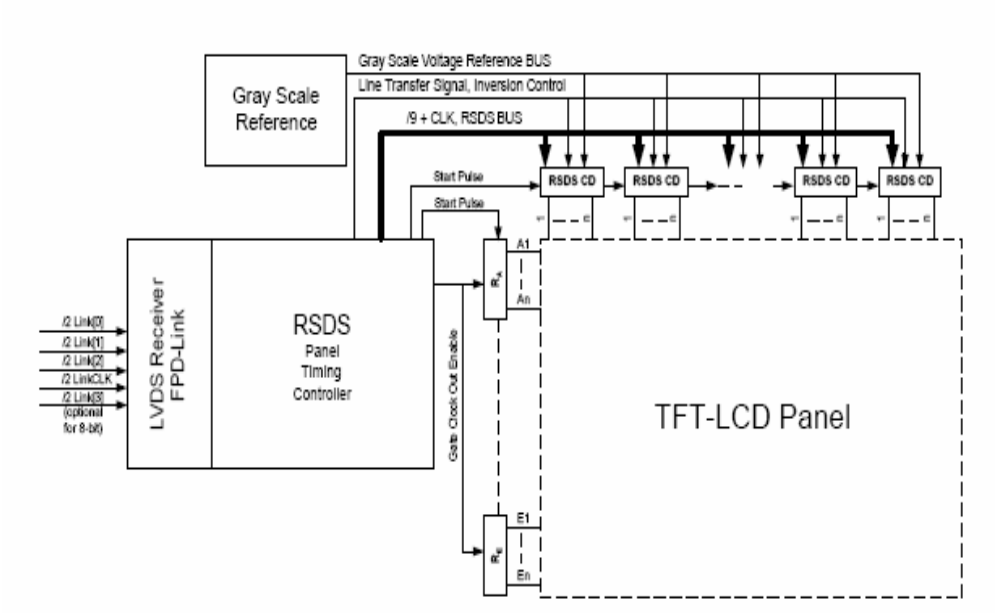


Figure 4.1. Block diagram of the LCD module

(Source: National 2003)

4.2. Timer Controller

The basic functionality of TCON board is the timing control for LCD panel drive. Each panel type depending to manufacturer, panel size, resolution has a specific rigid timing diagram. Achieving flexible interface between processing board is supplied by TCON board. LCD module has rigid timing but at data input of TCON board there is a flexible timing diagram. The timing conversion from the flexible data input via LVDS interface to rigid timing diagram via RSDS is controlled by TCON. Difficulty of TCON IC development is specifications are totally dependent to LCD panel module, details of the timing specifications at the panel side should be clearly defined for TCON development. Most panel manufacturers do not share these details related with their panel technology, that is the reason most panel manufacturers has division for TCON IC development specific to their panel technology and panel revision. TCON board is specified to panel and it is the interface buffer between LVDS data input and panel side. The block diagram of LCD module is given in Figure 4.2 the interface module between LVDS input and TFT-LCD panel is commonly called as TCON unit which includes LVDS receiver, timing controller and RSDS transmitter.

4.3. Response Time Improvement

LCD panel response time is not satisfactory due the slow response time of the LC molecules. LCD panel technology try to improve response time of LC cells by developing new LCD technology and developing panel driving algorithms to improve panel response time. Improvement in panel response time improves performance of display in moving objects, improvement means moving objects seems sharper, clear and detailed. Over drive is the commonly used algorithm for this purpose, video frames buffered in memory and depending to the transitions of pixel between each frames over voltage is applied for fast response of LCD cell. For example assume that the pixel grey level at the first frame is 100 and second frame is 150 and third frame is 200, in this transition case for the second frame of the pixel voltage level 180 is applied and because of the LCD cell response pixel actual level at the frame interval is around 150 and for the third frame 230 voltage level is applied to realize the actual level at the LCD cell at that frame interval around 200. Panel response timing is compensated and improved by

overdrive algorithm, the voltage level which should be applied is calculated depending to transition level and time interval. Different panels need different sets of overdrive parameters because panel response differs for different panels.

4.4. Gamma LUT

The response of the LCD cell is not linear with applied voltage, the transition curve which compensates the nonlinearity of LCD cell is called as gamma curve. Because the panel response is not linear for each color component, for each color component specific gamma curve is stored in look up tables (LUT) which compensates panel non linearity. With LUT panel linearity all through grey levels can be realized, color coordinate can be fixed for all grey levels.

CHAPTER 5

VIDEO & AUDIO PROCESSING

Video and audio processing is the basic functionality of the processing board which is the main concern of the thesis. In this chapter video and audio interfaces will be introduced in the first part and processing building blocks will be explained in second part, third part is dedicated to the short description of software blocks operating on TV system.

5.1. Audio & Video Interfaces

The interfaces and formats of the TV will be introduced in this part are RF, CVBS, SVHS, SCART, VGA, YPbPr and HDMI/DVI.

5.1.1. Terrestrial RF

RF input is the basic interface of TV system which is as old as the TV history, the video and audio content are RF modulated and transmitted over air. Terrestrial RF transmission will be investigated in two parts, analog and digital transmission.

5.1.1.1. Analog Transmission

Transmission and RF modulation of analog audio and video signal is called as analog RF transmission. Actually transmitted signal is always analog but depending to the content which is modulated transmission type is defined. For TV signal transmission single side band AM modulation is used for video, for audio AM or FM modulation is used depending to the audio modulation standard.

5.1.1.2. Digital Transmission

With the development of digital, video and audio content is digitized and encoded for data compression. Addition to analog content RF transmission, compressed

digital content is transmitted via air. Digital modulation techniques are used for transmitting digital coded content. COFDM modulation is used for terrestrial RF transmission and PSK is used for satellite transmission. DVB-T is the terrestrial transmission of digital signal; Integrated Digital TV (IDTV) is the name used for TVs capable of receiving digital transmissions.

5.1.2. Composite Vide Band Signaling (CVBS)

Composite Video is the based band video signal. Luminance, color and sync are the components of the CVBS signal. Horizontal and Vertical Sync are used as synchronization signals. At first video was grey scale only, after the development of colored TV color component integrated. The grey scale video includes luminance level only, in Figure 5.2 CVBS signal is shown, the grey scale video was in the form in Figure 5.2 but the color burst and color signal do not exists. When the color tubes are developed color signal integrated to the CVBS signal by adding reference color burst signal and color signal. The amplitude of the color signal defines the saturation level and the phase difference of the color signal to the reference color burst defines color coordinate. The color coordinate definition is given in Figure 5.1. (Jack 2001)

CVBS video has three kind of basic standards; NTSC, PAL and SECAM respectively. NTSC is the standard used commonly in USA, PAL and SECAM are used common in Europe, the basic difference is the vertical refresh rate, NTSC use 60 Hz and the other standards use 50 Hz vertical refresh rate. The other differences are related with color modulation.

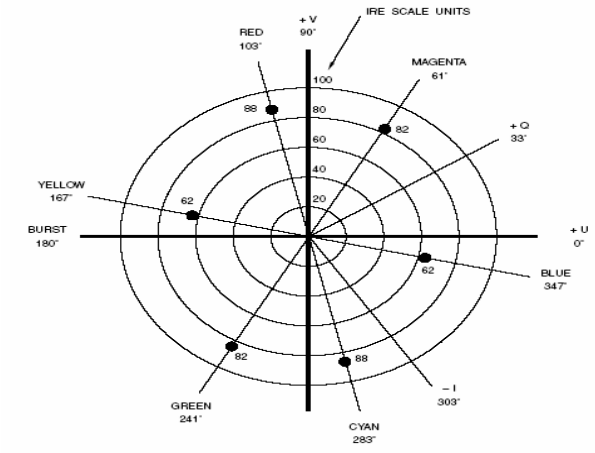


Figure 5.1. UV and IQ vector diagram

(Source: Jack 2001)

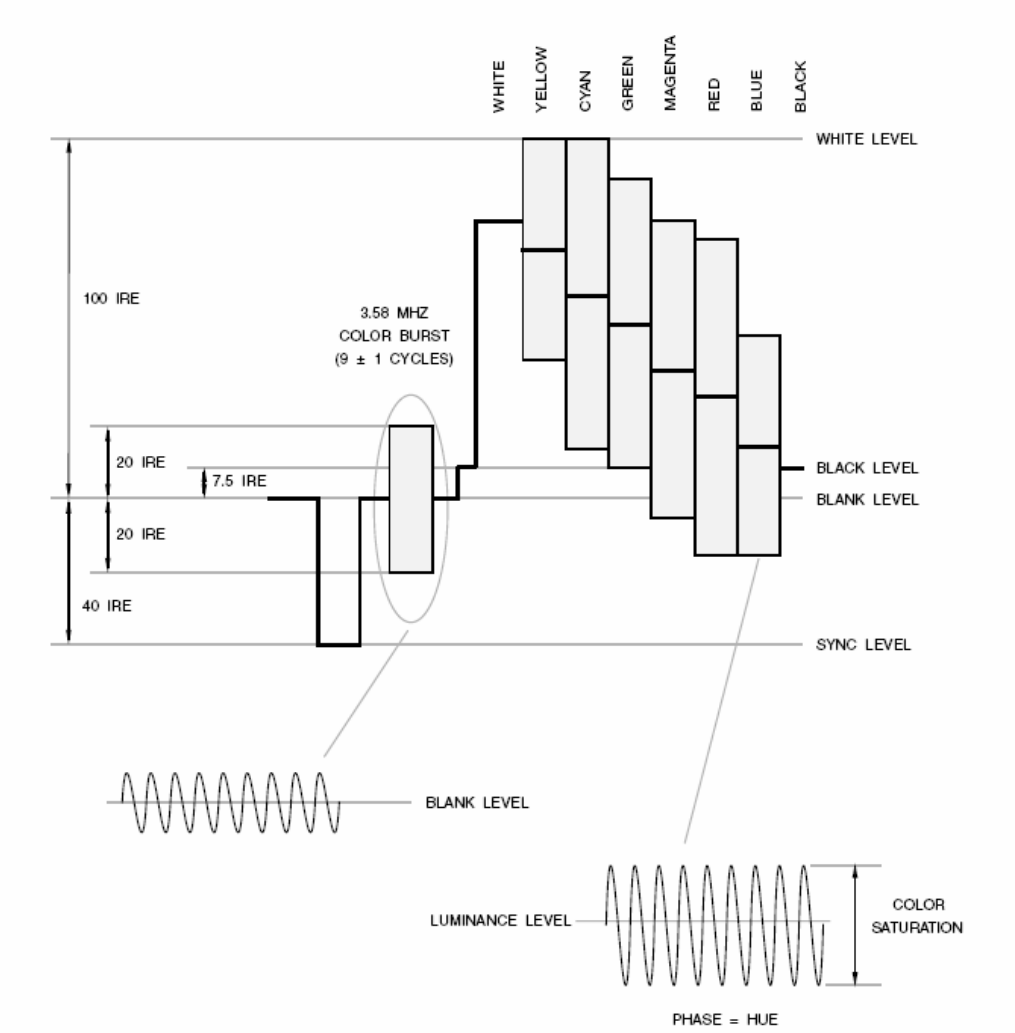


Figure 5.2. CVBS video wave diagram

(Source: Jack 2001)

5.1.3. SVHS

CVBS video is composed by luminance (Y) and color (C) signals, at the video decoder side these components are separated but this separation is never perfect. SVHS video interface includes Y and C signal separately, two signal lines are used to carry Y and C signal. The sync signals are integrated to Y signal and C is carried separately. Video quality of SVHS is better then CVBS, because CVBS lose quality during separation of Y and C component at video decoder side. Comb filter is used to separate Y and C component from CVBS signal which introduce loss and reduce signal quality.

5.1.4. SCART Interface

SCART interface is the common audio and video interface connection used in Europe. CVBS, SVHS, RGB video and base band dual channel audio can be transferred via SCART interface. Not only input but also CVBS and R/L audio output is supported in SCART interface. Pining diagram and the specification of each pin is defined in Figure 5.3 (Jack 2001).

Pin	Function	Signal Level	Impedance
1	audio right out (or audio mono out)	0.5v rms	< 1K ohm
2	audio right in (or audio mono in)	0.5v rms	> 10 K ohm
3	audio left out (or audio mono out)	0.5v rms	< 1K ohm
4	audio ground		
5	blue ground		
6	audio left in (or audio mono in)	0.5v rms	> 10K ohm
7	blue	0.7v	75 ohms
8	function select	9.5–12V = AV mode 5–8V = widescreen mode 0–2V = TV mode	> 10K ohm
9	green ground		
10	data 2		
11	green	0.7v	75 ohms
12	data 1		
13	red ground		
14	data ground		
15	red	0.7v	75 ohms
16	RGB control	1–3v = RGB, 0–0.4v = composite	75 ohms
17	video ground		
18	RGB control ground		
19	composite video out	1v	75 ohms
20	composite video in	1v	75 ohms
21	safety ground		

Figure 5.3. SCART pining and specification

(Source: Jack 2001)

5.1.5. VGA

VGA is the PC video interface, all video components red, green, blue and H, V sync signals are separate. Addition to video signals I2C communication signals clock and data exist in VGA. I2C communication is used for detecting supported formats. The pining diagram of VGA interface is given in Figure 5.4. (Jack 2001)

Pin	Function	Signal Level	Impedance
1	red	0.7v	75 ohms
2	green	0.7v	75 ohms
3	blue	0.7v	75 ohms
4	reserved		
5	ground		
6	red ground		
7	green ground		
8	blue ground		
9	+5V DC		
10	sync ground		
11	reserved		
12	DDC SDA	≥ 2.4v	
13	HSYNC (horizontal sync)	≥ 2.4v	
14	VSYNC (vertical sync)	≥ 2.4v	
15	DDC SCL	≥ 2.4v	

Figure 5.4. VGA pining and specification

(Source: Jack 2001)

5.1.6. YPbPr

Component video is the best quality video, all three video components are transferred separately. YPbPr is the one of the color space which can be given as in equation (5.1), in RGB domain. R', G', B' are the gamma corrected 8 bit RGB in 16-235 nominal range. (Jack 2001)

$$\begin{aligned} Y_{709} &= 0.213R' + 0.715G' + 0.072B' \\ Cb &= -0.117R' - 0.394G' + 0.511B' + 128 \\ Cr &= 0.511R' - 0.464G' - 0.047B' + 128 \end{aligned} \tag{5.1}$$

Human eyes are more sensitive to luminance, due to the fact that luminance is defined with Y component in YPbPr. By using this color space visual quality of image is improved.

YPbPr is High Definition (HD) video interface, video content which has more than 720 lines in one frame called as HD video by HD specification.

5.1.7. HDMI/DVI

DVI is the first digital video interface type, the digital row video data without any compression is transmitted via DVI interface. HDMI is the improved version of DVI including also digital audio data in same interface.

5.2. Processing Board Building Blocks

Processing board, power board, LCD panel are the three component of LCD TV, the thesis focus is the processing board design, details of design process will be given in chapter six, before design process the details of sub components of the processing board is the concern of this part. The building blocks of processing board are tuner, IF demodulator, COFDM Demodulator, Video Decoder, HDMI/DVI receiver, MPEG Decoder, DI, Scaler, uP, Memory, Teletext Decoder, Audio processor, Video Processor, Panel Interface, Audio Amplifier, Audio and Video Switches.

5.2.1. Tuner

Tuner is the basic front end block for RF reception, TV broad band RF signals are between 50 MHz to 850 MHz are down converted to intermediate frequency around 38 MHz (depending to the modulation system center IF frequency differs). Tuner internal structure block diagram is given in Figure 5.5 (ALPS 2006). Tuner is down converter mixer, at RF part band pass filters and pre amplifier is used to achieve improved SNR. Filtered and amplified RF signal is down converted to IF frequency by mixers. The internal block diagram given in Figure 5.5 belongs to hybrid tuner. Hybrid tuner architecture has both digital IF and analog IF output, difference between analog IF and digital IF is the intermediate carrier frequency different and for the digital IF part SAW filter and IF amplifier is integrated into tuner.

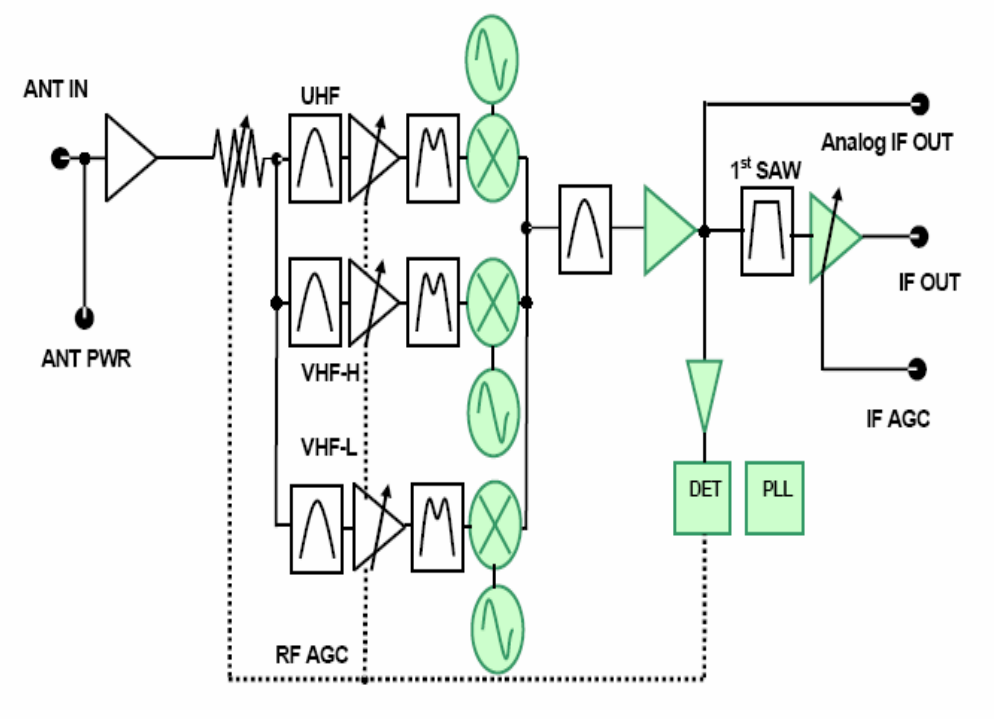


Figure 5.5. Tuner internal structure block diagram

(Source: ALPS 2006)

5.2.2. Analog IF Demodulator

Terrestrial analog RF signal is down converted to IF frequencies by tuner, IF decoder is the unit decodes RF modulated video and audio signal to base band. Down converted RF signal is the input of IF demodulator, base band video (CVBS) and QSS modulated or base band audio signal are the outputs of IF decoder. QSS is AM or FM modulated audio signal. In Figure 5.6 internal block diagram of analog IF demodulator is shown (Philips 2003). RF signal is down converted to IF by tuner, IF signal is filtered by audio and video SAW filters, SAW filters are used for better SNR and channel separation, filtered signal is the input of the IF demodulator. Modulated video and audio signal is demodulated by IF demodulator; base band video and audio signal are the outputs of IF demodulator. Because of SNR consideration and stereo audio application, QSS modulated audio signal is outputted from IF demodulator and at the audio processor side modulated audio is decoded. This architecture improves audio SNR quality.

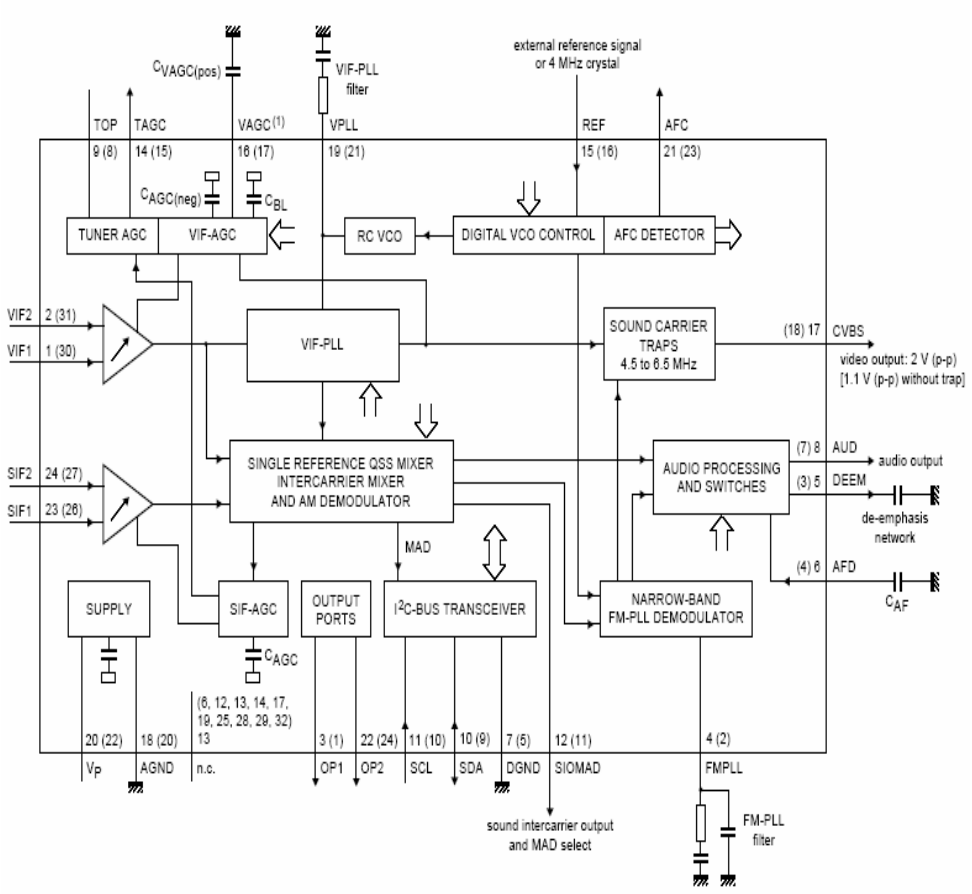


Figure 5.6. Block diagram of IF demodulator

(Source: Philips 2003)

5.2.3. COFDM Demodulator

DVB-T signal is COFDM modulated, for digital terrestrial RF reception COFDM demodulator is used at the front end side of DVB-T reception. Tuner down converts RF signal to intermediate frequency, for improved sensitivity and performance of COFDM demodulator SAW filter and IF amplifier is used on the signal path before COFDM demodulator. Depending to the HW architecture decision these parts can be inside the tuner or on board, generally using tuners which includes these parts inside is the safe way. Because the metal shield covering the tuner and weak IF signal path length between SAW filter and IF amplifier can be realized shorter in tuner which improve system noise immunity. These reasons improve system front-end performance. Internal block diagram of the COFDM demodulator is given in Figure 5.7 (NEC 2006a). IF signal is converted to digital by ADC, and COFDM coded digital signal demodulated

to transport stream. Transport stream is the base band bit stream which is MPEG coded for data compression.

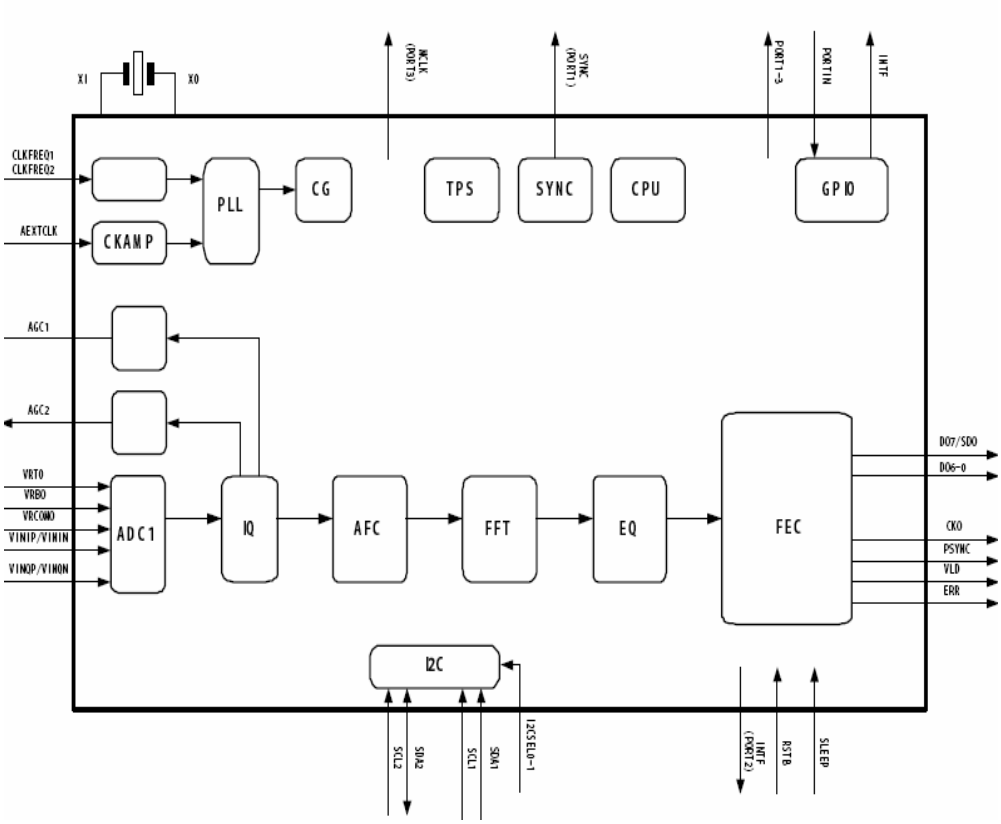


Figure 5.7. COFDM demodulator block diagram

(Source: NEC 2006a)

5.2.4. Video Decoder

CVBS video is separated to Y, U and V components by video decoder. The first part of the video decoder is the comb filter which is used for Y and C separation, the second part is the color demodulator which decodes C to U and V components. Simple video decoder architecture is given in Figure 5.8. Analog signal MUX is used to switching of two source, AGC (automatic gain control) circuitry is used for better A to D conversion, A/D block represents A to D converter, Y/C separation is the first step of video decoding and chrominance processing is the separation of C signal to U and V components (WEB_7 2007).

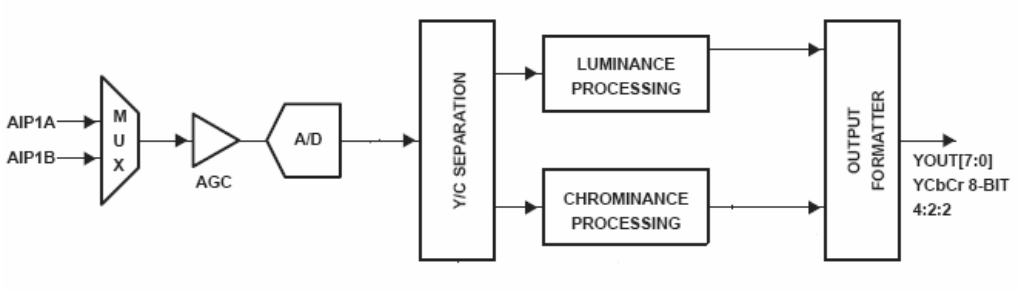


Figure 5.8. Simple video decoder architecture

(Source: WEB_7 2007)

5.2.5. HDMI/DVI Receiver

Video and audio storage devices such as DVDs are all in digital format for current situation. Because of the old audio and video interfaces are analog, digital signal is converted to analog for the compatibly to analog interface connection types. The interface between set top box and display device is mostly analog, but digital interface becomes more popular. The advantages of digital interface between display devices and video source devices are as following. Firstly original content is in digital format and also LCD displays is digital, without conversion D to A at source side and A to D at sink side digital data can be transmitted. All conversion steps analog to digital or vice versa degrease signal quality and introduce noise. Digital interface without analog conversion steps improve signal quality, secondly as the general characteristic of digital signal has better immunity to noise. Generally digital content is coded for data compression. But incase of signal is coded, at the display side decoder is needed, to provide simple interface between source and sink device row data is directly sent from source, disadvantage of transmitting row data is wide BW requirement. The first digital interface is the DVI and HDMI is the improved version of DVI. DVI includes video data only but in HDMI addition to video digital audio data is also integrated to bit stream signaling. The row data is transmitted, but firstly data is serialized and transferred via TMDS (Transition Minimized Differential Signaling) line which is optimized for wide BW applications. The cable used for this interface is also special for wide BW. At the receiver side TMDS signals are firstly converted to TTL logic voltage levels and serialized data converted to parallel data. HDMI interface is the one of the musts of display devices, and its usage areas are increasing rapidly. Currently HDMI

receiver is a default interface part of LCD TVs. HDMI is also DVI compatible, DVI source can be connected to HDMI receiver but in that case audio data will not exist in TMDS signals, via analog interface audio should be connected when DVI transmitter is connected to HDMI receiver. In some of single chip TV solutions HDMI receiver is also integrated to single TV processing chip. In Figure 5.9 internal block diagram of HDMI receiver is given (Analogix 2006). Most important part of the HDMI receiver is the TMDS Decoder. Serialized signal which is transmitted via TMDS lines are decoded to parallel data at this stage. HDCP (High Definition Content Protection) is the protection key which is used to protect content from illegal copy generation. I2C and DDC interface are the communication interfaces between sink and source devices. 24 bit digital video and I2S or S/PDIF digital audio is the output signals from HDMI receiver.

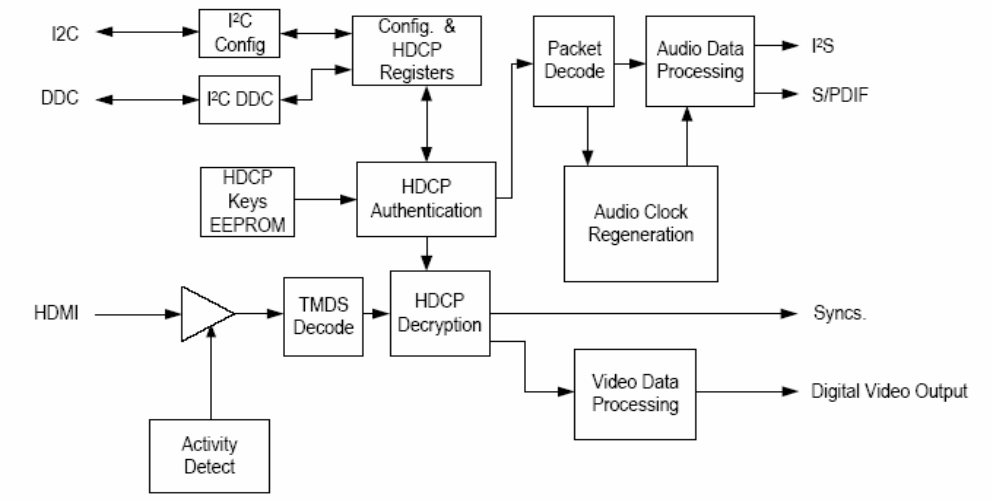


Figure 5.9. HDMI receiver block diagram

(Source: Analogix 2006)

5.2.6. MPEG Decoder

Transmission of terrestrial DVB-T signals and reception of DVB-T signals by TV is become a standard in many European countries. Broadcasting of DVB-T signals started already and soon DVB-T will be well known technology also in Turkey. Compression is a must for digital signals which should be transferred via limited BW. DVB-T Standard Definition is MPEG2 and High Definition is MPEG4 coded signals.

MPEG4 provides more compression ratio compared with MPEG2 so using MPEG4 standard provides to transmit more channels in same BW. Drawback between MPEG2 and MPEG4 is MPEG4 decoders are expensive, but MPEG4 provides to transmit same size of data in lower BW. At the receiver side MPEG decoder is used to decode coded digital signal. For the TV's with DVB-T reception feature MPEG decoder is a common part. Depending to the transmission standard MPEG2 or MPEG4 decoder used.

5.2.7. De-Interlacer

De-interlacing the basic block for digital display devices, because the video sources are mostly interlaced and display is progressive interlaced to progressive conversion is a must in digital display technology. There are several de-interlacing techniques and algorithms but the simple explanation of de-interlacing is as following for frame based DI. Two types of algorithm is used one is Spatial interpolation "Bob" and the second is Temporal interpolation "weave". Depending to the motion vectors detected these interpolation types are used adaptively.

5.2.8. Scaler

Flat panel displays are formed by pixels, panel is formed by pixels located in horizontal and vertical directions. The number of pixels defines the resolution of a display. Video sources have several kinds of resolution formats. Scaler is the one of main video processing unit for digital based display. Depending to the input and output resolution both down and up scaling is possible for each vertical and horizontal directions. Scaling function is the one of most important function which defines product picture quality for flat panel displays. Scaling is an interpolation in spatial domain, for the improved performance the interpolation coefficients are adaptive to edge, low angle and etc.

5.2.9. Controller uP

Controller is the basic unit for all kind of systems, the performance requirement of controller which is used for flat panel display TVs varies depending to the target

requirement of product. But in general processing power of controller used just only for system control in TV systems, in this case 8 or 16 bit controllers like as 8051 or M16 operating at frequency interval 20-80 MHz are used. Generally for video processing in TV system HW architectures are used, incase of using controller for video processing RTOS (real time operating systems) based systems operating at high frequencies needed. But for system efficiency HW based video processing is preferred and for system control only low specification controllers are used in TV systems. Related with micro controller decision, user interface is also a key parameter which defines system requirement, the complicated OSD (on screen display) designs need processing power. In Figure 5.10 8051 architectural block diagram is given (MacKenzie 1995).

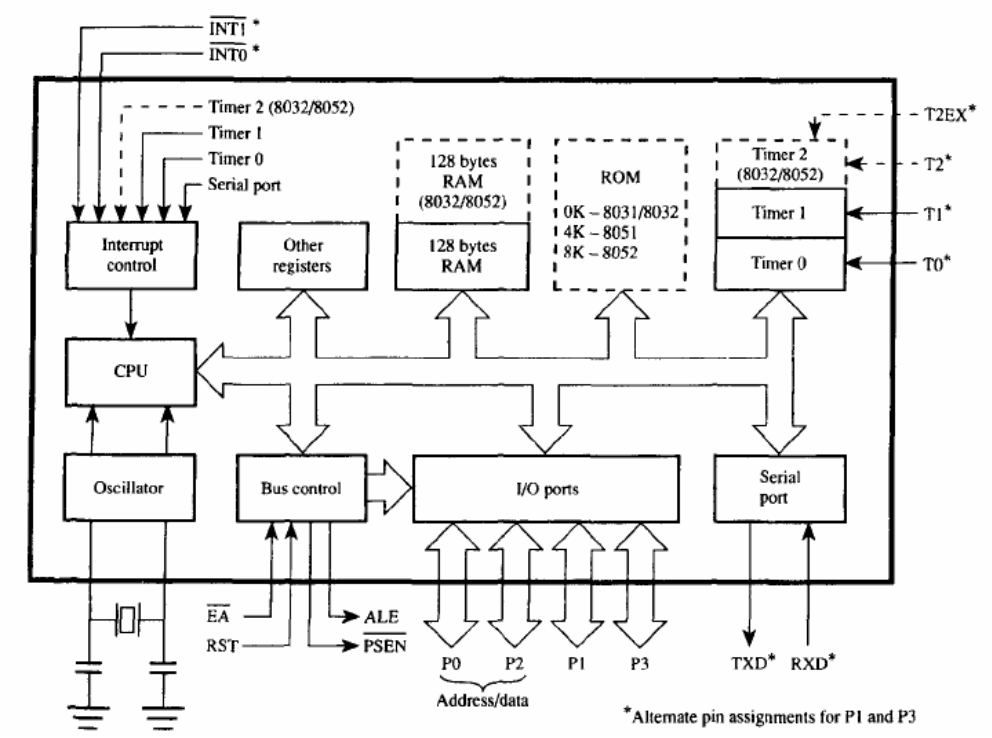


Figure 5.10. 8051 system block diagram

(Source: MacKenzie 1995)

5.2.10. Memory

Two types of memories ROM and RAM are used in flat panel displays. The system code and system data are stored in static memory units which are non volatile (MacKenzie 1995). Dynamic memories are also needed for video processing, the

memory BW is the most important parameter for video processing. The operating frequency and bus width defines memory BW, volatile memories as RAM is used for video processing. Incase of high frequency operation PCB traces have limiting effect on BW, for the high BW signals PCB layout design has an important role.

5.2.10.1. Static Memory ROM

Static memories are generally in two type of architectures NAND and NOR. NOR type memories features are, addressed mapped memory, no intrinsic bad block management and before writing or erasing special commands must be written to the first page. NAND type memories are block memory, has built in bad block management unit and memory management unit is needed for NAND type memories. Static memories are used for system code and data storage. Flash memories are non volatile memories, for non volatile memories data also stored when the power is off.

5.2.10.2. Dynamic Memory RAM

Dynamic memories are also used in TV systems actually for video processing. Dynamic memories are volatile memories, only can store data when power is on. Two types of architecture are shown in Figure 5.11. SRAM topology use six transistor for one bit storage and SDRAM based topology use single transistor. SRAM topology includes two inverter feeding each other, M1 and M3 forms the first and M2 and M4 forms the second inverter. M7 and M8 are used for writing or reading control. In SRAM based architecture when the data is written one times it is stored until the power is off. SDRAM architecture is based on single transistor and single capacitor. The transistor is the switch which controls the connection between capacitor and data bus, capacitor is the memory storage element. One bit data is stored on capacitor. Because of leakage current capacitor voltage drops down in time, refreshing is a must for this type of architecture. Memory controller is used in SDRAM topologies for this purpose. The comparison of SRAM and SDRAM topologies are as following.

- SRAM is faster and expensive
- SRAM consumes more power
- SDRAM requires memory controller for memory refreshing

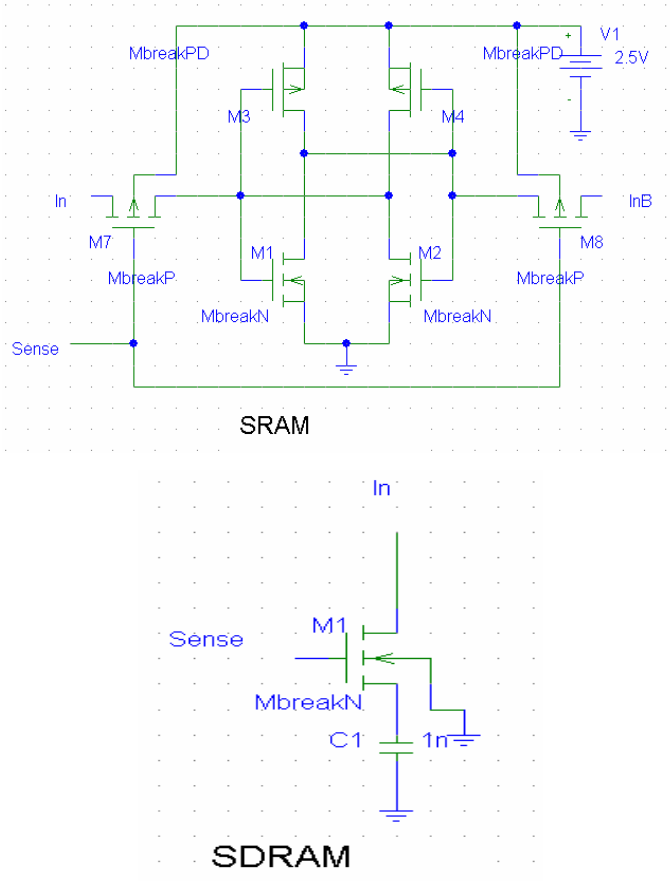


Figure 5.11. SRAM and SDRAM unit cell topologies

5.2.11. Teletext Decoder (VBI Slicer)

Addition to video data, teletext data is broadcasted. Teletext data lines are located at video blanking interval. Lines between 6 to 22 and 318 to 335 may be used to carry Teletext data packets depending to the availabilty of these lines (ETSI 2002). In Figure 5.12 blanking interval and teletext data lines are shown.

Teletext data is in digital data format, each line has a defined format and data map. The first line of teletext includes reference clock called as clock run in, system clock is locked to the clock run in and samples data bits refer to this clock. The reference timing is given in Figure 5.13.

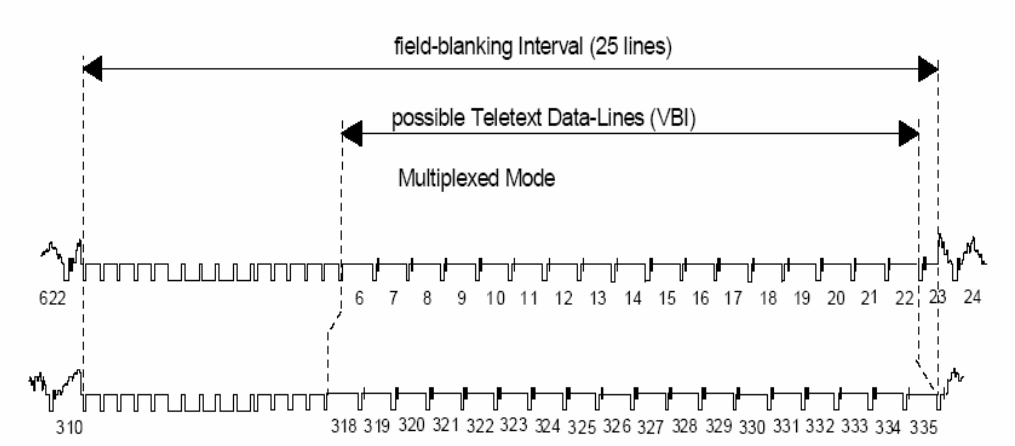


Figure 5.12. Teletext data lines at blanking interval

(Source: ETSI 2002)

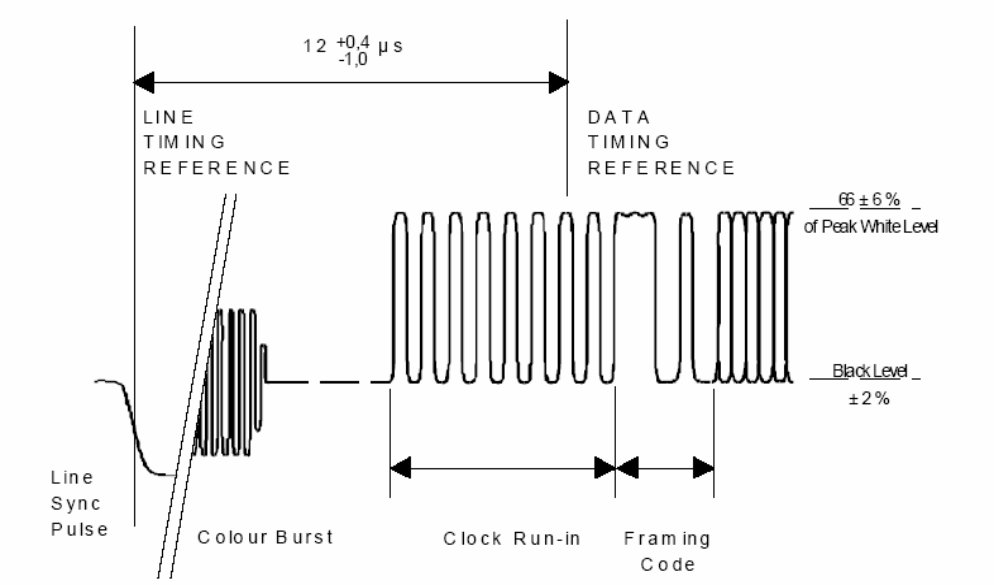


Figure 5.13. Timing reference and clock run in interval

(Source: ETSI 2002)

VBI (Vertical Blanking Interval) Slicer is the element which receives and slice teletext data, teletext decoder decodes data and displays teletext on screen. The new TV designs use additional memory for fast teletext page access. Teletext pages are stored in memory during watching TV and when the teletext page is wanted to display, stored page in memory displayed quickly. Depending to the memory size all pages can be stored in memory before for quick access to page.

5.2.12. Audio Processor

Video and audio processing are the two basic functions of TV processing board, video processing is divided to several sub items as video decoder, scaler, de-interlacer, video enhancement because of the complexity of the video processing but audio processing will be given in one item.

The audio interfaces are base band analog audio, SIF and digital audio like as SPDIF, I2S. Base band analog audio is sampled with ADC and converted to digital. SIF is the modulated analog sound signal which is demodulated and converted to base band digital. Digital audio interfaces carries serialized digital audio data, at the audio processor side these signals are received and converted to the parallel digital audio data before processing. Audio processor front end part is formed by ADC, SIF demodulator for analog and de-serialize block for digital audio interfaces. At the end of front end part all data is converted to parallel base band digital audio. DSP processor is used for audio processing, with audio processing special effects which improves audio quality can be realized. SRS, Dolby, BBE are the companies which have licensed audio processing algorithms used in TV systems. Equalizer sound effect is the one of the main functionality of audio processing.

5.2.13. Display Video Processing (Picture Enhancement)

Picture quality is the major item which defines TV system product quality. Video processor, scaler and de-interlacer have great effect on picture quality but addition to these blocks display processing block also has important effect on picture quality. Display video processing block is the last block on video processing path. After this block data is sent to panel. Display video processing includes contrast, color and sharpness enhancement functions. The display video processing blocks structure given in Figure 5.14. The video processing is done in two paths, luminance (Y) signal is on the first path and color components Cb and Cr are on the second path. First path is optimized for luminance processing and the second is optimized for color processing. Contrast enhancement is the first feature of luminance processing and sharpness on Y component is the second function. DCE (Dynamic Contrast Enhancement) block improves contrast and LTI (Luminance Transition Improvement) block improves

sharpness. SCE (selective color enhancement) is the color enhancement block including green, blue and skin tone correction. CTI (color transition improvement) block is the sharpness improvement block for color component.

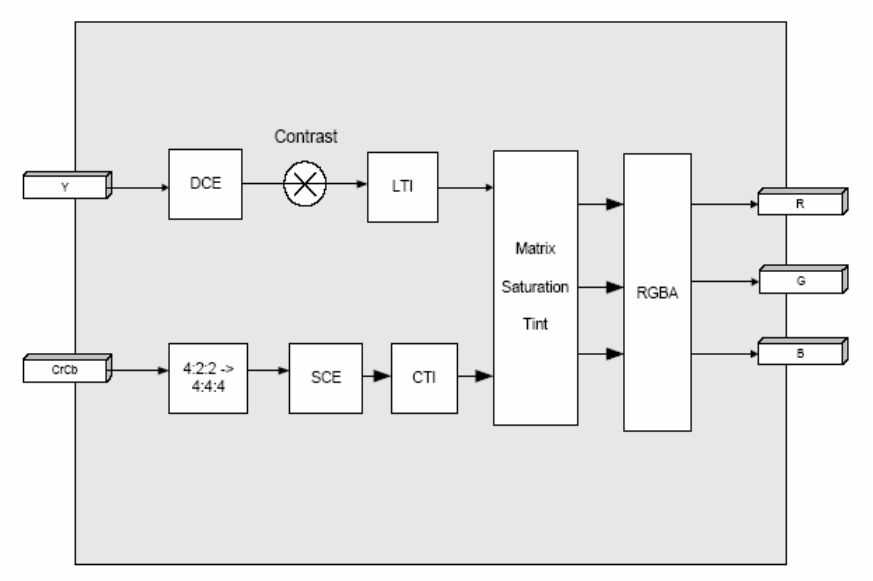


Figure 5.14. Display video processing block diagram

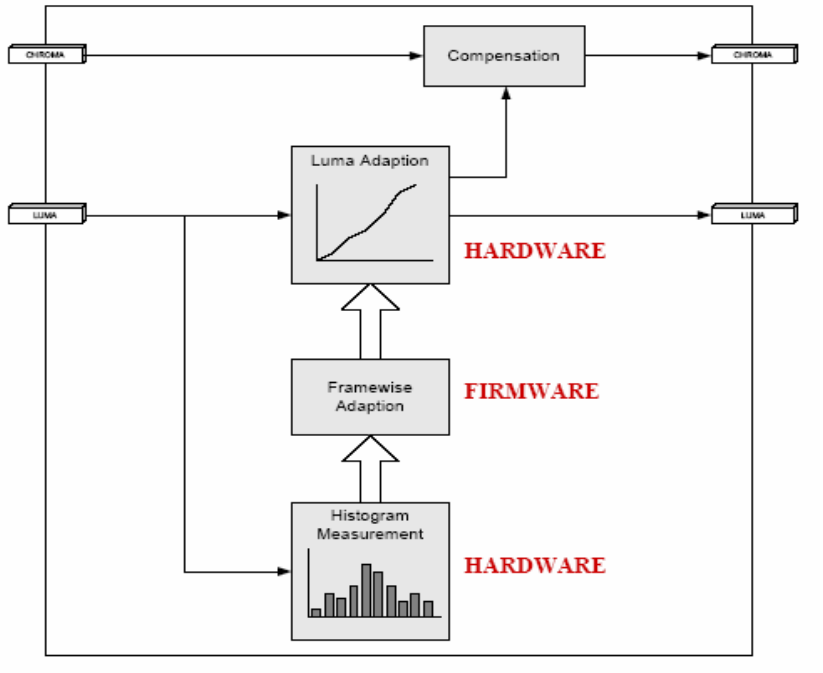


Figure 5.15. DCE block diagram

Dynamic contrast enhancement function is useful algorithm especially for LCD displays which has limited contrast ratio physically. DCE algorithm is based on histogram measurement of the frame and depending to the histogram distribution luminance transfer curve is updated frame by frame. The block diagram of DCE is given Figure 5.15 and improvement of DCE is shown in Figure 5.16.

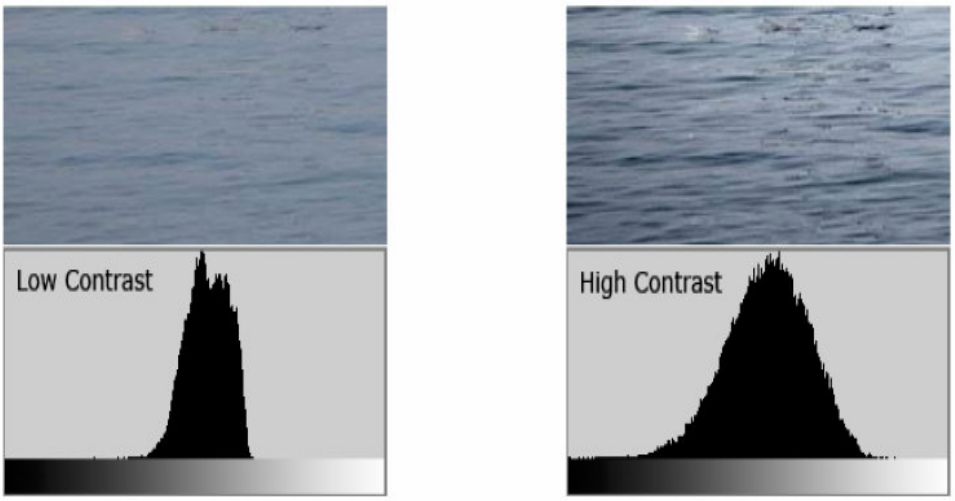


Figure 5.16. a) Original frame b) Contrast enhanced frame with DCE

Sharpening of Y component is the second processing block of luminance processing path. Two types of algorithms are used for sharpening, peaking and LTI (luminance transition improvement). The effect of peaking and LTI algorithm on black white transition is given in Figure 5.17. Top side is the original transition curve and bottom side is enhanced transition, a) is the peaking and b) is the LTI function. Peaking algorithm increase overshoot and undershoot generally if the over shoot level is too high it seems as an artifact, peaking algorithm also increase the slope of the black white transition which improves sharpness. LTI algorithm improves sharpness by increasing the transition slope.

Peaking and LTI luminance sharpness improvement is shown in Figure 5.18.

LTI and peaking algorithms operates in parallel and adaptively, the gain of LTI and peaking varies with frequency adaptively. Luminance sharpening block given in Figure 5.19 is formed with the parallel combination of LTI and peaking function.

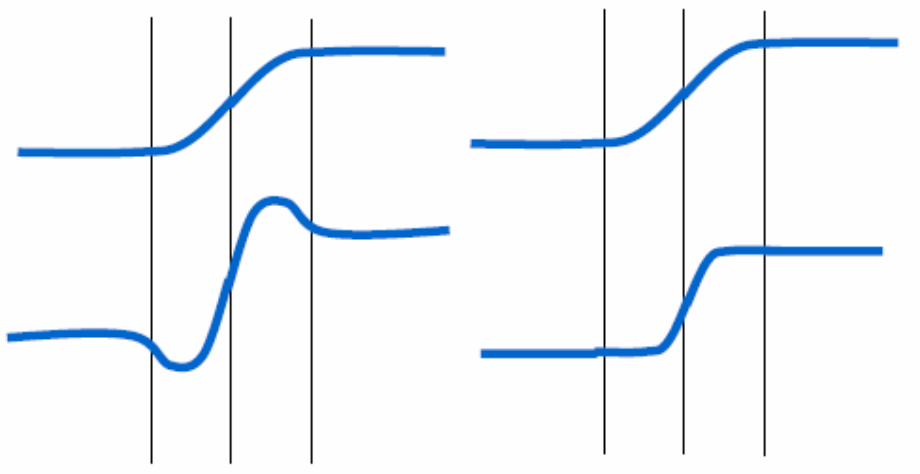


Figure 5.17. a) Peaking b) LTI (Luminance Transition Improvement)

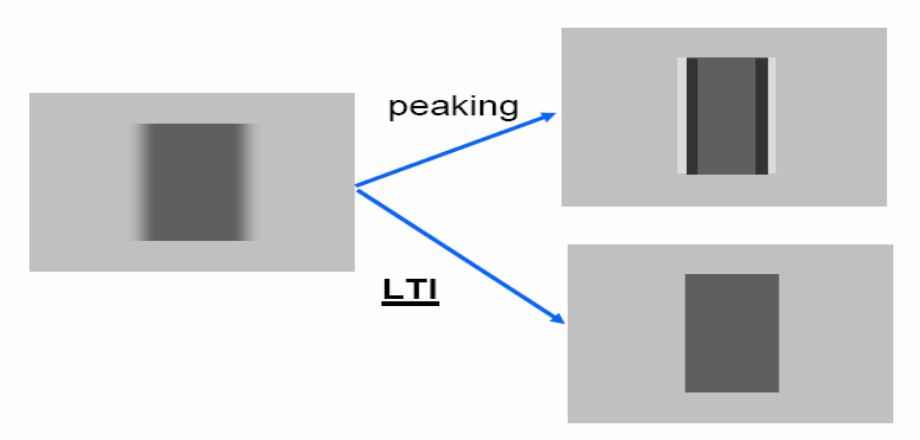


Figure 5.18. Peaking and LTI improvement

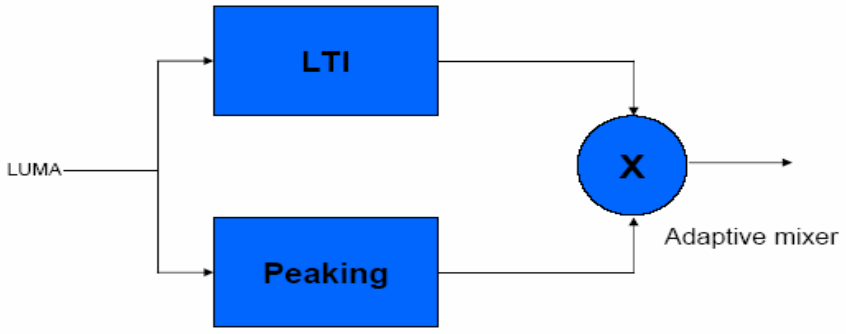


Figure 5.19. Luminance sharpening block

Peaking and LTI functions block diagrams are given in Figures 5.20 and 5.21. Peaking functions filter high frequency components of picture and adds to the original frame with amplitude adaptation.

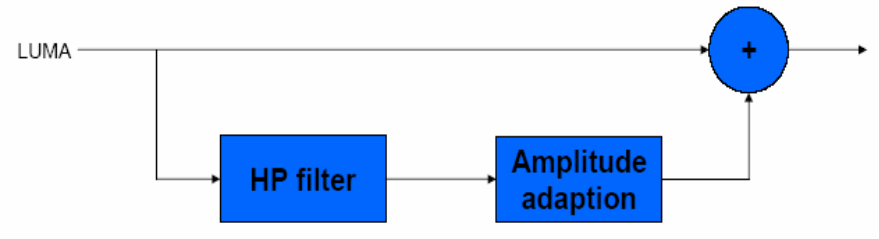


Figure 5.20. Peaking function block diagram

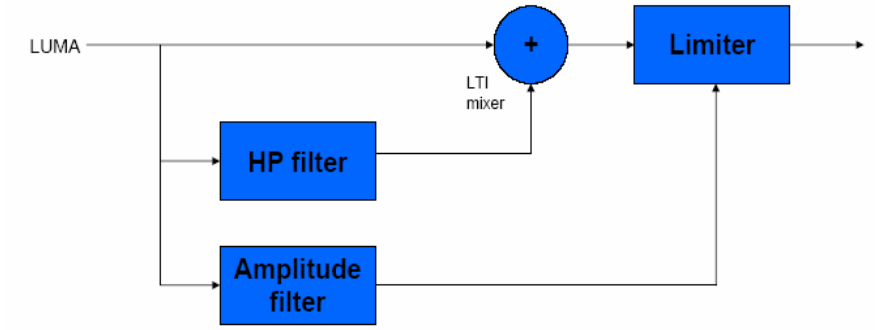


Figure 5.21. LTI function block diagram

LTI function includes limiter which is controlled by amplitude level to cancel overshoot and undershoot artifacts.

Chrominance processing path is formed by color enhancement block and CTI (chrominance transition improvement) block. Color enhancement block includes skin tone correction, blue and green improvement. Flesh tone or skin tone correction function detects color phase and maps to the defined phase which is the desired color phase for skin tone. Green and blue enhance functions increase saturation of blue and green color depending to the amplitude. In Figure 5.22 color coordinates and color enhancement functions are given.

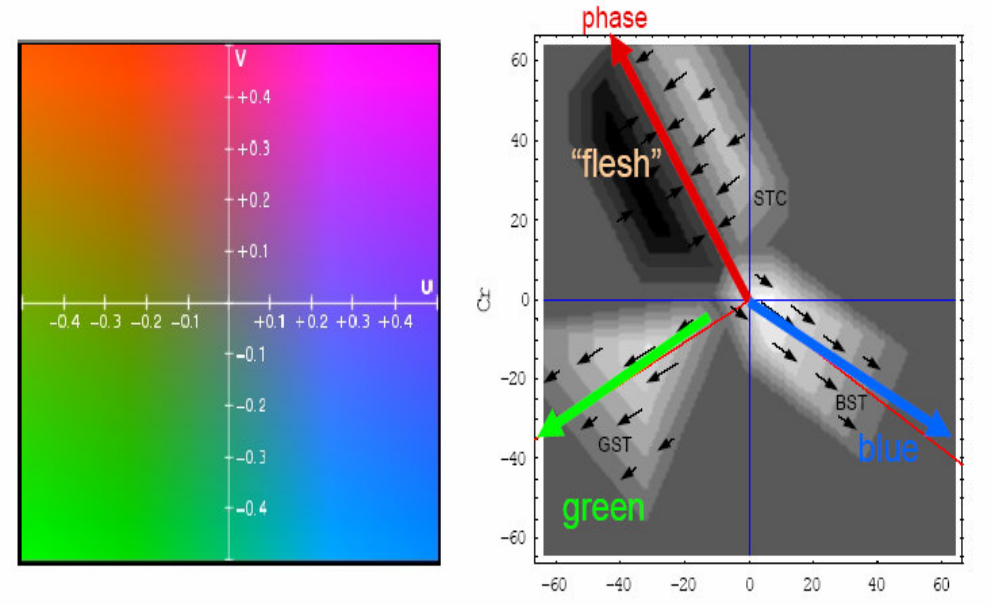


Figure 5.22. a) Color coordinates b) Color enhancement functions

Sharpening algorithm for color is CTI (color transition improvement). Transition between two colors is improved by CTI function which makes color transitions more sharp. In Figure 5.23 it is shown that, blue and red transition at the top is improved as below with CTI function.

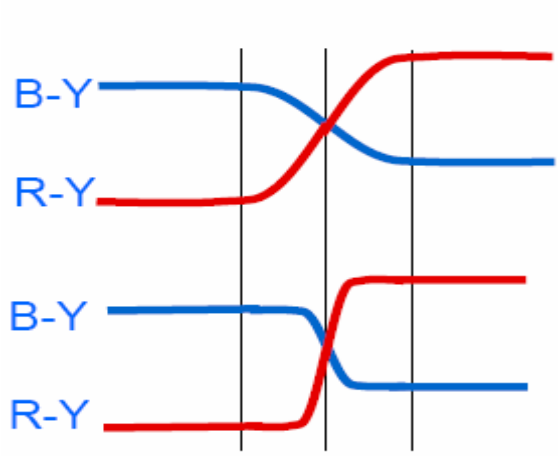


Figure 5.23. Blue and Red transition improved with CTI function

Functional block diagram of CTI is given in Figure 5.24, CTI response and functional diagram is similar to LTI with the difference of operating on Cb and Cr color components, not Y.

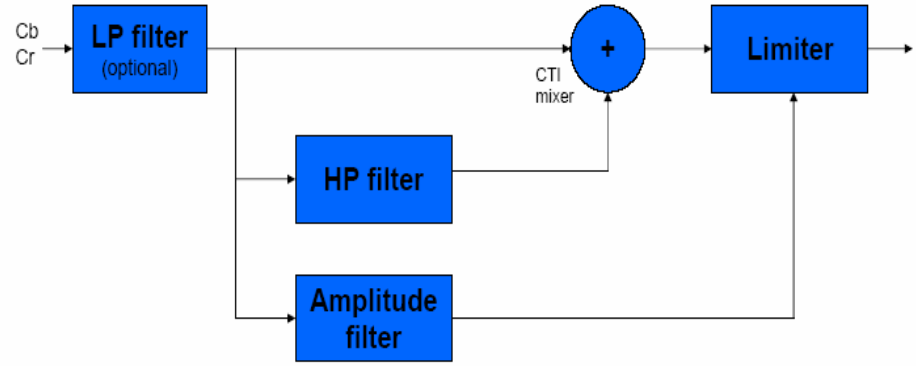


Figure 5.24. Functional block diagram of CTI

The improvement of CTI function is shown on test video pattern in Figure 5.25 a) is the original pattern and b) is the color transition enhanced pattern with CTI function.

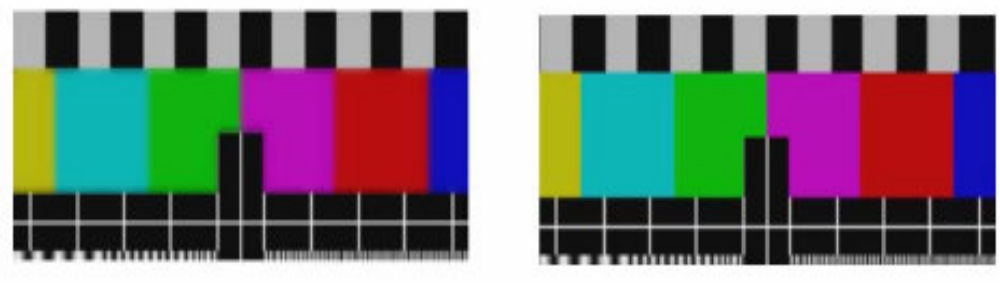


Figure 5.25. a) Original test pattern b) Test pattern with CTI function applied

Video enhancement block is the last video processing block which improves contrast, sharpness and color of the picture to provide more vivid, attractive and detailed scenes to end user.

5.2.14. Panel Interface

Processing board and flat panel interface is supplied via TTL or most commonly LVDS interface. LVDS is mostly preferred as panel interface because of low EMI and high data BW. At the processing board side processed video data is converted to LVDS format and transferred to panel by LVDS transmitter. In Figure 5.26 block diagram of LVDS transmitter is given (WEB_8 2007). The serialization ratio is 7:1 for LVDS

signal, the frequency range of data is 3.5 times clock. At the maximum transfer rate assume that the first data is low, second is high and third is low again, in this case total two data period equals to one signal period. At the receiver side data is sampled 7 times the clock frequency.

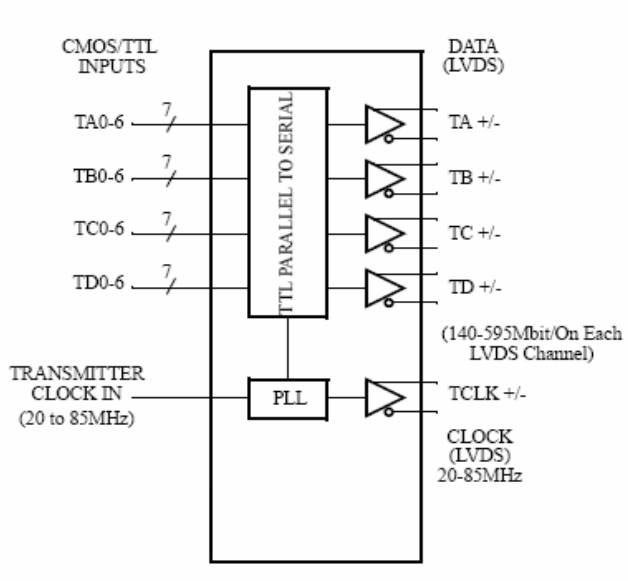


Figure 5.26. LVDS transmitter block diagram
(Source WEB_8 2007)

5.2.15. Audio Amplifier

Flat panel displays audio output power requirement varies due to panel size. Products with large screen size are used in large rooms and because of this reason required audio output power increase with display panel size. For the small size displays, which requires under 5W audio output power AB class audio amplifiers are used. Applications over 5W use Class-D audio amplifier, D type amplifiers are high efficiency amplifiers which does not require additional heat sink for heat dissipation. Class AB and Class-D type amplifiers are the audio amplifiers used in flat panel applications.

5.2.15.1. Class-AB Audio Amplifier

Class A amplifiers are linear amplifiers with low efficiency and class B amplifiers has better efficiency compared to A but has distortion, class AB amplifiers

are the hybrid amplifier type with better efficiency compared to class A and has no distortion. Simple Class AB output structure is given in Figure 5.27. Push-pull structure driver transistors are biased with voltage to be on when signal applied. Biasing network in Figure 5.27 is formed by Q3, R1, R2 and Bias current supply (Sedra and Smith 2004). Because of the efficiency of AB type is not also high enough, these type of amplifiers are used in low output audio power flat TV application.

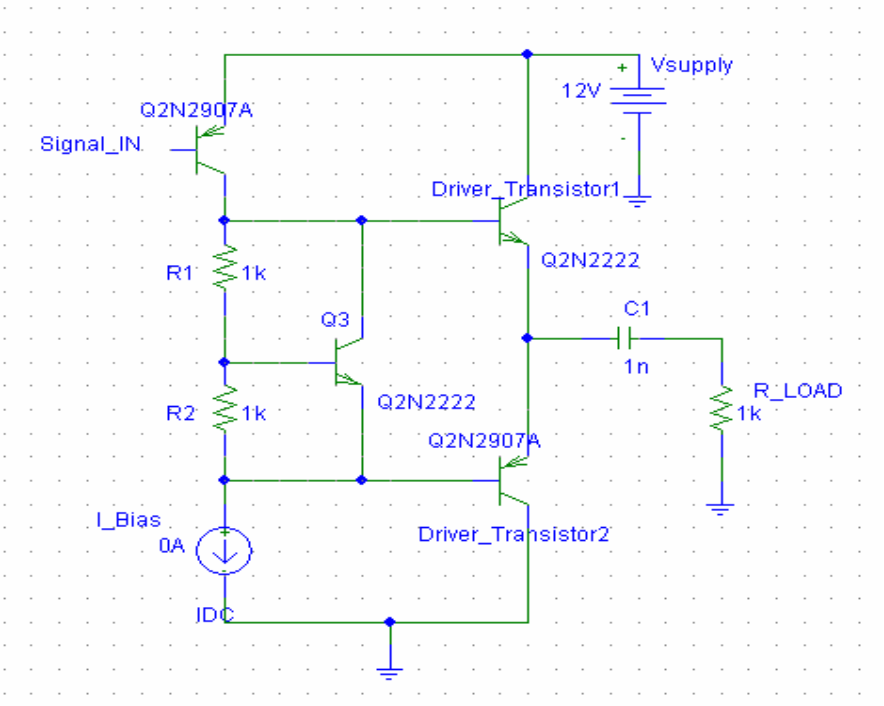


Figure 5.27. Class AB output stage

5.2.15.2. Class-D Audio Amplifier

Efficiency of an output stage is an important parameter, output stages with low efficiency requires heat sink which introduce cost and volume to the system. In flat panel applications both system volume and cost is important. Class-D type audio amplifiers have high efficiency, in most cases additional heat sink not required. Considering system cost and volume D type amplifiers are used in flat panel displays. The system architecture of a D type amplifier can be summarized in three stages. First stage is the analog front end and amplification, second stage is the most critical stage.

Second stage is the pulse width modulator which includes a comparator multiplies analog audio signal with triangle wave, the output of the second stage is pulse width modulated signal. The analog audio is pulse width modulated and low frequency component of the pulse width modulated signal carries base band signal. Third stage is the output stage, PWM modulated signal drives output transistors. Output voltage level is equal around to VDD or VSS at any time, one of output transistor is on and the other is off and the output voltage level equals to the level where on transistor is connected, voltage drop on transistor almost zero but because of internal serial resistance of the transistor current multiplied with serial resistance voltage drop appears. Efficiency level of D type amplifiers are around 90% (Philips 2006a), which is the most important advantage of D type amplifiers. The output signal is PWM modulated and after low pass filtering original signal can be obtained. Internal structure of a Class-D amplifier is given in Figure 5.28.

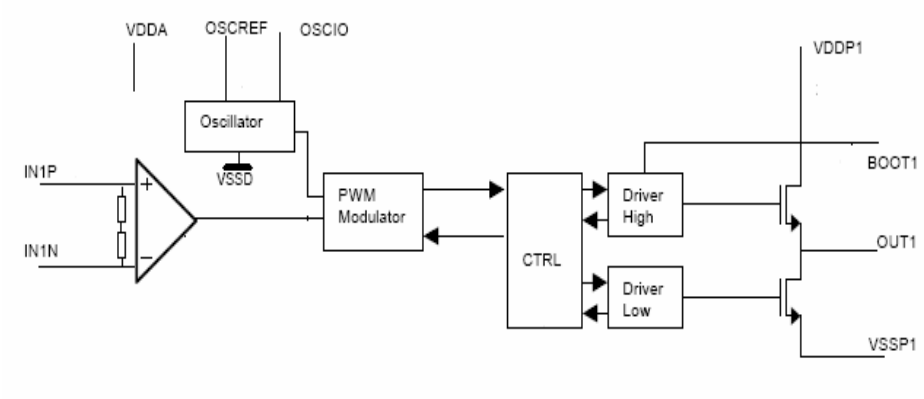


Figure 5.28. Class-D audio amplifier

(Source: Philips 2006a)

5.2.16. Audio & Video Switching

Simple TV system has several audio, video inputs and outputs. Video processor chip or audio processor chip also have many inputs and outputs pins but in most cases additional external switches are needed. For analog signals audio BW is 20kHz and video BW is 8MHz for CVBS video, HD video interfaces like as YPbPr and VGA video BW is quite high, for 1080i 50 Hz input sample rate is 74.250 MHz (Jack 2001)

and for VGA 1280x1024 75Hz commonly used PC resolution pixel rate or sampling rate is 102.250MHz (VESA 2003). Video BW can be given as in equation (5.2).

$$BW = \text{Pixel or sampling Frequency} / 2 \quad (5.2)$$

Depending to the signal characteristic which will be switched active or passive switches are used in TV processing board.

5.3. Flat Panel TV Software Building Blocks

Software development role in TV system is increasing, the functionality, efficiency and usability of a system is directly related with SW design structure. User interface and system control are the major two items controlled by SW.

5.3.1. User Interface

5.3.1.1. On Screen Display (OSD)

On screen display design is an important parameter, the functionality and usability an electronic device is defined with the user interface module. OSD is the interface module in display devices. Addition to the functionality and usability of user interface graphical design improves visual quality.

5.3.1.2. User Functionalities

Addition to standard TV functions SW development provides additional functions as sleep timer, child lock, alarm clock and several functions which are useful for user.

5.3.2. System Control

Main function of the software running on microcontroller is the system control. In a TV system microcontroller inputs are keypad, Infra Red (IR) remote controller,

inputs from audio video interfaces like as SCART pin 8, short circuit protection signal. Output control signals of microcontroller are standby control, led control, audio amplifier mute, Panel Backlight, LCD panel dimming, system reset, audio and video switching control.

Microcontroller handles system power on/off sequence, source switching, signal detection, audio and video processing chips settings. Biggest role of the system control is video and audio processing chip settings control. Processing chips has several registers which are used for signal detection, signal processing and on screen display. For simple example of chip registers control assume that signal resolution at VGA PC video signal interfaced changed from 1024x768 60Hz to 1280x768 60Hz. In video processing chip defined registers counts vertical and horizontal sync timing. Both of the resolutions have the same vertical timing but the horizontal timings are 48.4 kHz and 47.4 kHz respectively (VESA 2003). System controller will read the timing measurements and due to the read values format detection is done. After the signal detection video processing chip settings are updated. ADC sampling frequency, scaling ratio settings are the values which should be updated in case of example, because pixel clocks are 65MHz and 68.25MHz respectively ADC sampling frequency is increase by 3.85MHz in such format change. Vertical resolutions are same for both resolutions but horizontal resolution increased by factor 1.25, display resolution is fixed so horizontal scaling factor in processing chip is reduced by 1.25. The related registers which are defining ADC sampling rate, scaling ratio are updated. The register settings for supported resolutions are stored in tables which are also stored in system code.

CHAPTER 6

FLAT PANEL TV PROCESSING BOARD DESIGN

Design of the TV processing board is the main focus of the thesis, system requirements decision is the first and evaluation of building blocks is the second design stage. Schematic and layout designs are the implementation level of processing board design.

6.1. System Requirements Decision

Decision of target specifications is the first item in design process. Depending to the target market expected requirements on the mass production date, specifications of the product are defined. Flat panel TV's main requirement can be combined in four topics. First is panel related requirements such as resolution, scan type; the second is Audio & Video (AV) interface connectivity related requirements; third is the features for user and the last one is the video and audio performance which is the main item determining the product quality.

6.1.1. Panel Requirements

Display panel is the main component of flat panel TV, around 70% share of the total cost is panel price. TFT LCD and Plasma panels are two types of flat panel display technology which are used in consumer electronics now. Resolution and the panel driving technology are the two items define panel requirements for the video processor board.

The resolutions becomes most common for flat panel displays are WXGA 1366x768p which has the biggest share in market currently and 1920x1080p which's share is increasing rapidly. Real High Definition Resolution (1080p) is a driving power for consumer TV market. Real HD Resolution is an important point for display technology, because of human eye resolution limitation which is limited by the number of light receptors rods and cones, but with additional image processing by brain normal

human eye equivalent resolution is around 576M (24000x24000) pixels (WEB_9 2007). 42” size panel with 2M pixel resolution from 4 m distance which is the minimum watching distance for 42” (minimum watching distance is 4 times display axis) seems almost as natural as real. Especially for plasma displays different resolutions are possible such as 1024x1080i. Increasing resolution is difficult challenge for plasma because of their cell structure and power requirements, increasing of resolution in LCD display is easier compared with plasma displays. Panel resolution defines video processing and panel driving circuitries specifications. Depending to market demand WXGA resolution has the biggest volume in sales with 2006-2007 numbers. As the resolution specification for the aimed product WXGA resolution is decided to meet the market demand.

Second item is display timing requirements, same resolution panels can have different timing specifications, physical display resolution is called as active area and addition to active area displays need blanking areas both in vertical and horizontal directions. Total resolution which determines the panel timing is the total of active resolution and blanking interval. For example 40” Samsung panel timing requirement is specified as below in Table 6.1 (Samsung 2006).

Table 6.1. Timing requirements of LCD Panel
(Source: Samsung 2006)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit
Clock	Frequency	1/TC	60	80	85	MHz
Hsync		Fh	43	50	53	KHz
Vsync		Fv	48	60	66	Hz
Vertical Active Display Term	Display Period	Tvd	-	768	-	lines
	Vertical Total	Tv	773	838	1500	lines
Horizontal Active Display Term	Display Period	Thd	-	1366	-	clocks
	Horizontal Total	Th	1576	1600	2048	clocks

For typical values of horizontal and vertical total, pixel clock can be calculated as,

Pixel Clock = 1600 (H total) x 838 (V total) x 60 Hz (Vertical sync)

Pixel Clock = 80,448 MHz

Pixel clock is the operating frequency of the panel and the panel driving unit. Pixel clock is generated by video processor and Timer Controller board locks to the clock and operates with this reference clock.

Considering panel requirements and market demand for display resolution in midrange, WXGA panels are the main focus of the project and driving all kind and brands of these panels is the requirement specification for display panel.

6.1.2. Video & Audio Interface Requirement

TV set is a display device and connectivity of a display to external devices is an important parameter. Several kind of audio video interfaces are used in TV sets; RF, SCART, YPbPr, VGA are the analog interfaces in addition to analog, digital interfaces becomes more common, HDMI is the most popular digital interface for current technology.

RF is the oldest interface in TV sets, TV history started with transmission of TV signals via radio waves. Tuner is the building block of TV sets which down converts radio frequencies to intermediate frequencies and the signal at intermediate frequency converted to base band video and audio signal by intermediate frequency decoder (IF Decoder). There are three standards for base band standard definition (SD) TV signaling, PAL, SECAM and NTSC. PAL and SECAM which can be decoded by single front end architecture, NTSC needs different front end. After front end reception these signals are decoded by video decoder, video decoders are generally universal, can decode all of the standards but front-ends are specified to NTSC or PAL and SECAM.

In addition to analog RF, digital RF reception is a must for European countries and digital transmission is taking the role of analog transmission because of several advantages of digital transmission.

SCART interface is also SD video interface, in which base band audio and video signals are directly transmitted. Not only CVBS video but also RGB video is transmitted via this interface.

YPbPr is the High Definition (HD) video interface, up to 1920x1080p resolutions are transmitted via this interface. 1080p resolution is an important resolution which is defined as real HD resolution and supporting this resolution is an important feature for TV set.

VGA is the PC video interface, also for TV sets this interface become common. Several types of resolutions are defined for this interface but generally for TV set resolutions lower than or equals to 1280x1024 are supported.

HDMI is the most popular digital interface, row digital data is transmitted via this interface. Because the transferred resolution is high and also without any compression digital data is transmitted, the bit rate is also very high (1.6 Gbits/s for 1080p resolution). HDMI is becoming a standard digital connectivity between any kind of box such as DVD player, satellite receiver and TV sets.

Considering current technology and market demand connectivity of TV set which will be designed is defined as, hybrid tuner for both digital and analog RF reception, double full functional SCART, YPbPr interface up to 1080p resolution support, VGA interface and double HDMI interface.

6.1.3. User Requirement

User functionality of a TV set is also an important parameter, addition to technical features such as display resolution, audio video interfaces with external devices; user has demand for functional and user friendly TV sets.

On screen display (OSD) is the user interface of a TV set and the simplicity and the functionality of this interface should directly fits user's expectations. OSD design is not only a technical issue but also related with art, because viewing of icons, placement of items and interface between sub pages needs an artistic view. OSD design is the first item should be optimized for user requirements.

Functions such as sleep timer, child lock, alarm clock, auto program search improves product quality, user demand on such functions because these functions makes TV sets more functional, as an example user can use TV set as an alarm clock.

6.1.4. Video and Audio Performance Requirements

Depending to the technological improvement, expectations from a TV set become more and more high. Screen sizes at 37" and WXGA resolution become standard for current technology, both size and resolution increasing rapidly, in one or two years 42" HD resolution will become a standard product. While resolution and

screen sizes increasing video quality should also increase, otherwise picture quality will seems very low in big size and high resolution displays. To meet this demand, picture enhancement techniques aims clear, sharp, detailed, high contrast, natural pictures. Every manufacturer develops image engines to improve video quality. Not only for video but also quality expectation for audio is increasing, audio processing techniques such as Dolby, SRS and BBE also become standard for TV sets.

6.2. Evaluations of Building Blocks

System requirements are defined in previous section to support these requirements three main building blocks should be clarified, front-end block for both digital and analog terrestrial RF reception, MPEG decoder for decoding digitally compressed content, and analog block concept IC which includes audio, video processing blocks. Current technology provides audio and video processing blocks integration to meet mid-range TV sets performance requirements. Because of the integration of all processing blocks a single chip solutions are available. These three basic building blocks should be decided considering system requirements.

6.2.1. Front-End

TV signals terrestrial transmission is starting point of TV history, addition to analog transmission DVB-T (digital terrestrial transmission) become a standard now. First step was the set-top boxes for DVB-T reception, as the second step is integration of set-top boxes to TV sets. Because of integration, design of TV sets which receives both digital and analog terrestrial transmission become a must for TV designers. Tuner and the IF decoder are called as front-end which converts RF modulated signal to base band analog signal or MPEG coded digital stream. For digital reception tuners should have better performance as low phase noise and high sensitivity for low level signals. Combination of analog and digital tuners hybrid tuner formed which has two IF outputs for digital and analog. For IF demodulating of analog and digital signals, one analog IF decoder and one digital COFDM demodulator are needed. Hybrid tuner, analog IF decoder and digital COFDM decoder are the three parts of front-end which is both analog and digital terrestrial reception capable.

Operating frequency interval is the first specification for tuners and design specification covers all terrestrial band, VHF low, VHF high and UHF band.

For Hybrid Tuner decision compatibility to analog only tuners is important, whether the market situation has increasing demand on DVB-T, only analog reception front-end has 30% demand. Considering this item hybrid tuner's with compatibility to analog only tuners are searched and three alternative suppliers are found. Performance metrics of tuners are listed as in Table 6.2 below and specification of vendors are stated (ALPS 2006, Philips 2006b, Thomson 2006).

Table 6.2. Comparison of hybrid tuner performance

		ALPS	Philips	Thomson
RF Voltage Gain [dB]	Max		49	
	Min		44	
	Std		47.3	
RF AGC Range [dB]	Max		40	60
	Min		35	40
	Std		38.3	53.2
Image Rejection [dB]	Max	70	70	70
	Min	60	66	60
	Std	66.6	68.64	66.6
IF Rejection [dB]	Max	70		60
	Min	60		50
	Std	66.6		56.6
RF-input return loss [dB]	Max	8	7	6
	Min	4	5	6
	Std	6.64	6.32	6
In-channel return loss [dB]	Max		8	6
	Min		8	6
	Std		8	6
Noise Figure [dB]	Min	6	5	5
	Max	9	7	7
	Std	7.02	5.68	5.68
ESD protection of terminals		200 V	2 kV	
Surge protection at RF-input		15 kV	5 kV	

(cont. on next page)

Table 6.2. Comparison of hybrid tuner performance (cont.)

Oscillator stability [ppm]		50	80	30
Osc. Phase Noise [dBc/Hz]	Min	-100	-73	-110
	Max	-70	-73	-75
	Std	-85	-73	-90
Cross-modulation [%] at 70dBuV	Min		0.3	1
	Max		1	1
	Std		0.538	1
Amplitude Response Flatness[dB]	Max		4	3
	Min		3	3
	Std		3.66	3
Input Sensitivity [dBm] BER 2exp-4		-81.5	-82	-82

For digital reception most important parameter are sensitivity and immunity. MPEG decoder has a theoretical BER limit to operate properly, after this limit blocking effects become visible and further more nothing can be displayed. Tuner and COFDM demodulator performance directly defines sensitivity and immunity of the system. Systems have better front-end performance can receive digital transmission in wide range area which improves product quality. For digital reception DTG and NORDIG specifications defines desired performance levels for European market. Sensitivity and immunity of system are measured in several cases like as echo, side-band interference in these tests which are mandatory.

Tuners noise Figure, sensitivity and rejection of undesired bands defines tuner performance. Noise Figure is in dB, the SNR at RF input of tuner minus SNR at IF frequency, which directly effects over all system performance. Rejection of side bands defines immunity of system to undesired signals.

DVB-T signal is COFDM modulated and at tuner output COFDM demodulator is used to demodulate IF signal to transport stream (NEC 2006a). Matching of COFDM demodulator and tuner is important which defines front-end performance.

Alternatives for analog IF demodulator are in two architecture, first architecture is analog processing based IF to based band conversion (Philips 2003) and the second architecture is based on digital processing. Because analog based architecture is more consistent, for analog IF decoder this type structure is decided to be used. Considering both European transmission standards and European vendor's know how in these standards as an IF decoder TDA9886 decided to be used in system.

6.2.2. MPEG Decoder

Digital terrestrial reception becomes a must for TV sets, for digital terrestrial transmission VHF and UHF band are used, frequency interval of digital and analog TV transmission is the same but for digital transmission COFDM modulation is used. Front-end of the digital reception is formed by tuner and COFDM demodulator. Tuner is the frequency down converter RF to IF band and the COFDM demodulator demodulates digital modulated signal to transport bit stream. Because of bandwidth limitation digital signal is MPEG2 encoded for saving RF BW and depending to compression rate bit rate changes. One RF channel has 8 MHz BW, for analog TV channels each channel covers all BW but for digital transmission depending to bit rate of each channel more than one channel exist in 8 MHz RF BW. COFDM demodulator just only demodulates digital signals, channel separation and MPEG decoding are done by the channel MUX and MPEG decoder, actually channel MUX, MPEG decoder and system controller for the digital reception part are integrated into single chip for current products. Common Interface (CI) module is also a must for TV sets with DVB-T reception function. CI module supply to decode coded channels and system code upgrade. This interface is also controlled by system controller located inside MPEG decoder single chip architecture. For the digital MPEG2 decoding and digital terrestrial reception DTG test requirements are must. Depending to cost, performance, support during project development and reliability of the chip NEC EMMA2LL is used as the MPEG decoder (NEC 2006b).

6.2.3. Concept IC

Project target market is mid-range and system requirement defined fits to this range. Integration of building blocks increase step by step. First step of integration was video decoder and scaler, second step was integration of micro processor and third is integration of audio processor. For current chips video decoder, scaler, uP and audio processor are integrated for mid-range TV sets. Considering AV interfaces, video performance and system BOM cost Paulo chip set decided to be used which meets system target requirements (Mstar 2006).

6.3. Schematic Design

6.3.1. Block Diagram Design

The first stage of the schematic design is the system block diagram design, in block diagram signal flow, connectivity of external connectors to system and top level system diagram are clarified.

System audio and video connectivity are decided in system requirement decision part. External connectors are as the following, for digital and analog RF reception hybrid tuner, two full function SCART connector, one YPbPr component video with R/L audio, one VGA connector with audio in, two HDMI connector, one audio line out, one SPDIF digital audio out and one subwoofer audio out. These connectors are on the board and on the side board one SVHS and one CVBS video in with R/L audio inputs.

System can be divided into two main blocks, firstly analog part including controller, scaler, de-interlacer, audio and video processor, secondly digital part responsible of digital terrestrial reception. Front-end is the common block for both analog and digital part, both RF reception is realized with hybrid tuner solution which has analog asymmetric IF and symmetric filtered digital IF output. Analog demodulation and digital demodulation are separately done, for analog demodulation analog IF demodulator TDA9886 (Philips 2003) used and for digital demodulation COFDM demodulator UPD61540 (NEC 2006a) used. Tuner is the common component for both analog and digital RF reception and IF demodulators can be classified in analog and digital part separately.

Digital part is formed by COFDM demodulator, MPEG decoder and Common Interface (CI) module. As MPEG decoder UPD61115 (NEC 2006b) is used and this chip is not only MPEG decoder but also system controller, CI module and all digital part is controlled by UPD6115. Memory requirement of the digital part is DDR memory for MPEG decoding and Flash memory for system code storage. CI module interface needs switches between COFDM demodulator, MPEG decoder and module card, these switching is realized by buffers.

Digital part's responsibility is digital terrestrial RF reception, without this part TV set can not receive DVB-T signal, with CI module decoding of encoded channels is possible. Digital part is for additional DVB-T reception feature.

Analog part is the basic part of the TV set, all system control, audio and video processing is realized by analog part. Audio video signals coming from external connectors are processed and LVDS signal output drives flat panel directly and analog audio output drive Class-D audio amplifier.

In midrange flat panel TV sets current technology provides single chip solutions, CPU, de-interlacer, scaler, audio and video processing units are combined in one chip solution. Considering requirements MST6W82BL is decided as the single chip solution. The solution has two HDMI input, three component video input, eight analog video input four can be configured as SVHS input. One digital input port can be configured as ITU.656 or 601 digital video input.

Audio inputs are as following SPDIF input, QSS input, four analog dual channel inputs and one mono input. SPDIF and four dual channel analog audio are outputs.

Memory requirement of MST6W82BL are 16 Mbytes DDR memory and 1 Mbytes Serial Flash memory.

Single chip solution has single video decoder inside, for CVBS & CVBS PIP applications second decoder ADV7180 is used which has six analog video inputs.

Class-D amplifiers are commonly used in flat panel TV sets because of high efficiency external heat sink is not required.

Audio and video signal connectivity is shown on HW block diagram below Figure 6.1.

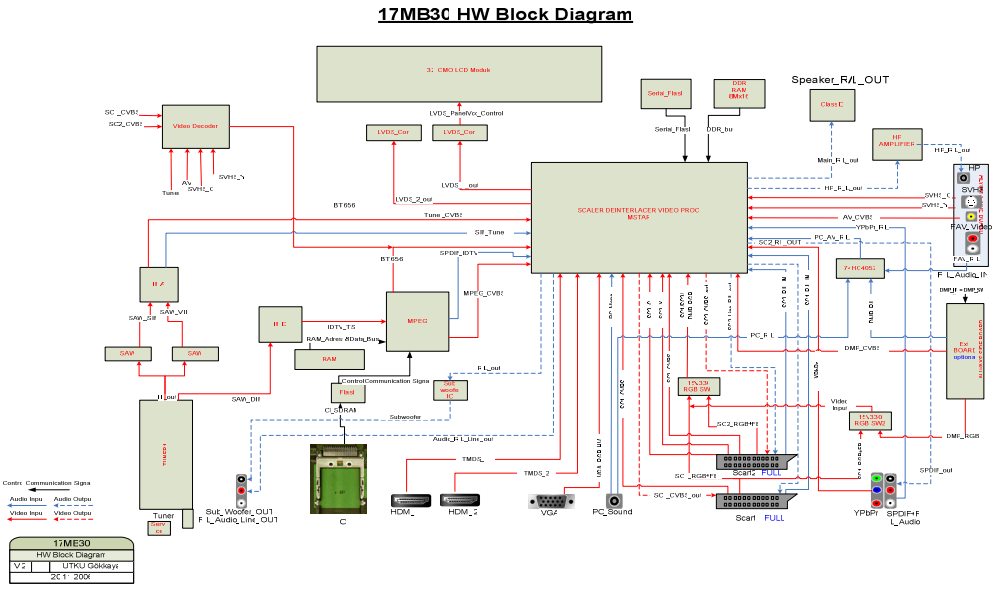


Figure 6.1. Block diagram design of MB30 project

Half NIM Hybrid tuner is used for analog and DVB-T reception, half NIM tuners include SAW filter and IF amplifier inside for digital IF output. Both analog and digital IF are separately outputted from tuner. Video carrier and audio carrier of analog IF are on different frequencies, two SAW filters are used for filtering, one for audio and one for video. Analog IF demodulator converts IF band signal to base band signal, CVBS video and QSS audio are outputs from analog demodulator. These signals are directly connected to MST6W.

Digital IF is demodulated by COFDM demodulator and converted to transport stream, digital stream is MPEG coded and MPEG decoder decodes this stream. MPEG decoder is connected via ITU.656 digital video and SPDIF digital audio interfaces to MST6W.

MST6W has two HDMI inputs, these inputs are directly connected, VGA input is connected to one of the component inputs and YPbPr is connected to the second component input. System requirement specified as double SCART connector with full function, SCART_1 RGB and SCART_2 RGB are switched before connecting to MST6W. Considering additional extension board, one more RGB switched is mentioned in block diagram.

CVBS inputs from SCART, CVBS and SVHS inputs from Side card are directly connected to MST6W.

PC audio, side board audio and optional extension board audio are switched by 4052 switch, the other audio inputs are directly connected to MST6W.

Four audio outputs are connected as, one for Class-D audio amplifier, one for SCART_1 audio output, one for both SCART_2 audio and audio lineout, fourth one for Head Phone output. Digital audio output SPDIF is also available.

ADV7180 is used as the PIP CVBS video decoder, six analog video inputs are configured as SCART one and two CVBS, Analog IF demodulator CVBS (Tuner CVBS), Side board CVBS and SVHS (SVHS input needs two analog input Y and C)

As audio Class-D amplified TDA8933 is used. Analog audio from MST6W is amplified by Class-D and drive 8 ohms speakers at max 8W output power with 24V supply voltage.

6.3.2. Front-End

Front-end is formed by Tuner, COFDM demodulator and IF decoder, for both digital and analog terrestrial reception with single tuner hybrid tuner is used. Digital IF output should be filtered and amplified before entering COFDM demodulator, for IF filtering SAW filters which are sharp passive filters are used and for amplification active circuitries such as transistor amplifiers are used with AGC function (automatic gain controlled) controlled by COFDM demodulator. For system simplicity and performance digital IF filtering and amplification is preferred to be realized in tuner. SAW filter and IF amplifier are integrated to hybrid tuner. Tuner filtered and amplified IF output for digital reception is connected via AC coupling capacitors to demodulator. Input of digital COFDM (U130) is digital IF from hybrid tuner and output is transport stream which will be decoded to row data by MPEG decoder.

Analog IF output should also be filtered with SAW filters, due to carrier frequency of video and audio is at different frequencies two SAW filter is required, one for audio (Z101) and one for video (Z102). Audio SAW filters input also should be switched for SECAM L reception by Q104. Filtered analog IF inputs are connected to TDA9886 (U148) IF decoder for analog demodulation. CVBS video and QSS modulated audio signals are the outputs of the IF demodulator.

Supply voltage and ground distribution of front-end is critical point for system performance. Great effort dedicated for front end supply design, separate LDO regulator is used to provide clean supply voltage to analog front end which is sensitive to supply noise.

Tuner has one I2C communication interface, but both analog side and digital side should communicate with tuner, U114 4053 switch is used to switch tuner I2C and AGC control signals.

Active antenna supply voltage via tuner RF input is commonly used for the IDTV application, 5V supply voltage is connected to the tuner pin 1. This power line needs current limitation and on/off control. Current limitation is provided by PTC element at position TH101 which's resistance increase with the current and after a limit element act as open circuit. On/off control of the current is provided by MOSFET at position Q169 acting as switching element. Front-end schematic is given in page1 of schematic in Figure 6.2.

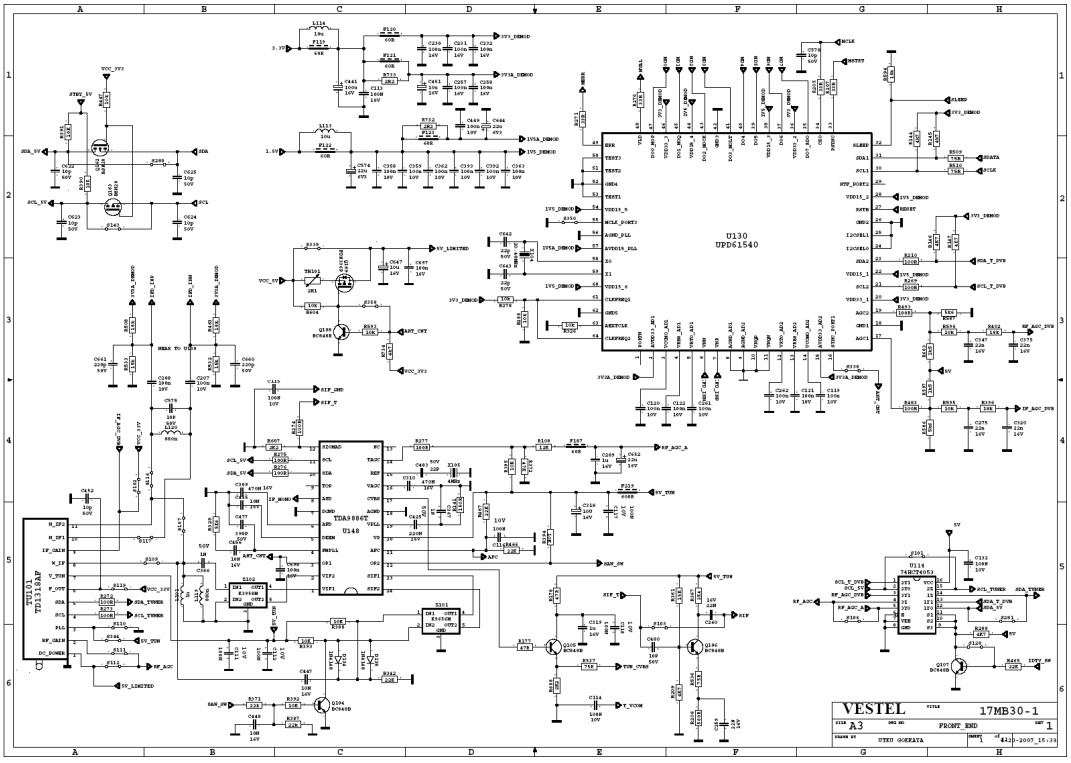


Figure 6.2. Page1 of the schematic

6.3.3. Analog Audio & Video Interfaces

Analog interfaces are double SCART, YPbPr, VGA, Side AV Board including SVHS, CVBS video, R/L audio inputs and Head Phone output.

SCART interface has CVBS and RGB video inputs, R/L audio inputs. Output signals of SCART interface are CVBS video and R/L audio outputs. Control signals are pin 8 function select and pin16 fast blanking inputs.

Specification for audio and video inputs termination and output impedance is, for video input and output 75 ohm impedance, for audio >10k ohm input and <1k output impedance (Jack 2001). Termination resistance are very important especially for video signals, with 75 ohms termination impedance reflection coefficient is zero and maximum power can be transmitted to load which improves SNR performance.

ESD protection is a must for TV sets all products have ESD protection with human body model 4kV conduct and 8kV air spikes. Zener diodes are commonly used for ESD protection. In our application for audio and video signals two zener diodes side by side are used, incase the signal is AC coupled, signal level can vary below -0.6V,

with only one zener voltages below -0.6V are clipped because zener diodes are normal diodes in forward biasing.

In our application CVBS output needs 5 voltage gain, the active feedback amplifier is used for this amplification (Q112, Q166, Q109, Q167). Feedback resistors value defines voltage gain. R507 300R and R189 75R is selected for (300+75)/75 = 5 gain. Video amplifier circuitry in Figure 6.3, transient response of the circuitry at 1 MHz input signal and frequency response of the circuitry is given in Figure 6.4 and 6.5 respectively. The high cut off frequency is computed as 41 MHz with Pspice simulation, but actual value is dependent to the parasitic effects of device and lines.

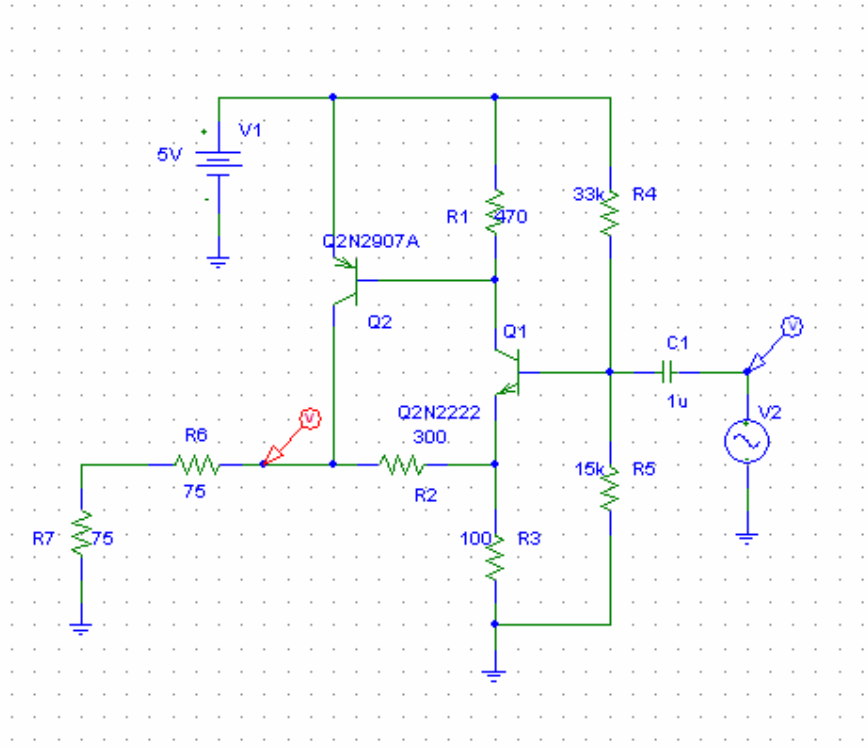


Figure 6.3. Video amplifier with 4 voltage gain

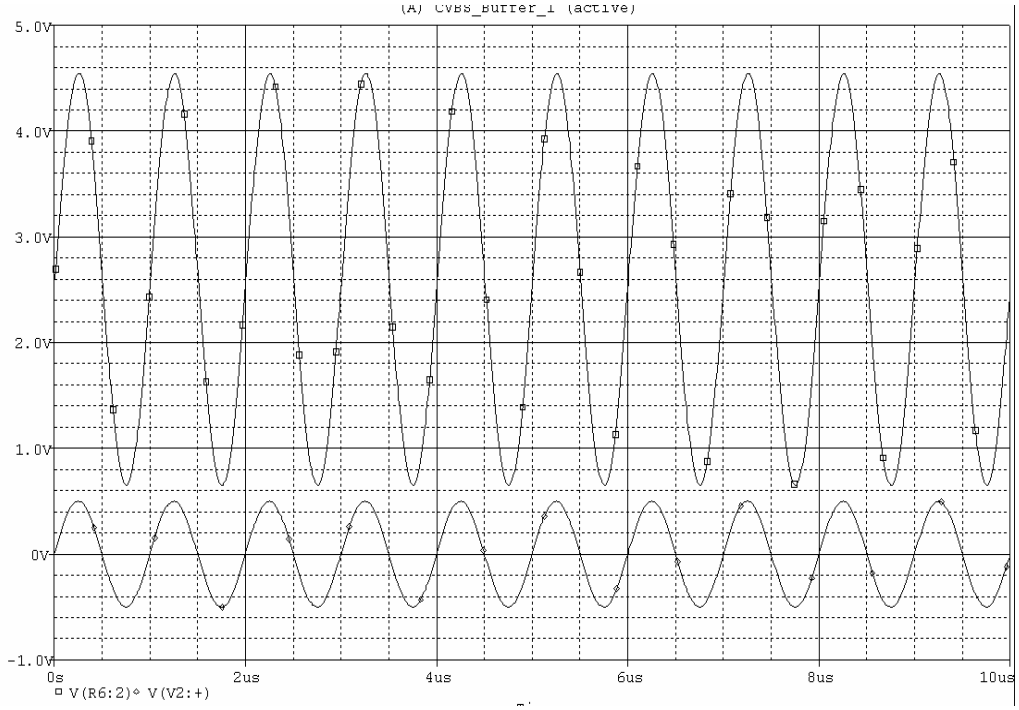


Figure 6.4. Transient response of the video amplifier with 4 Voltage gain

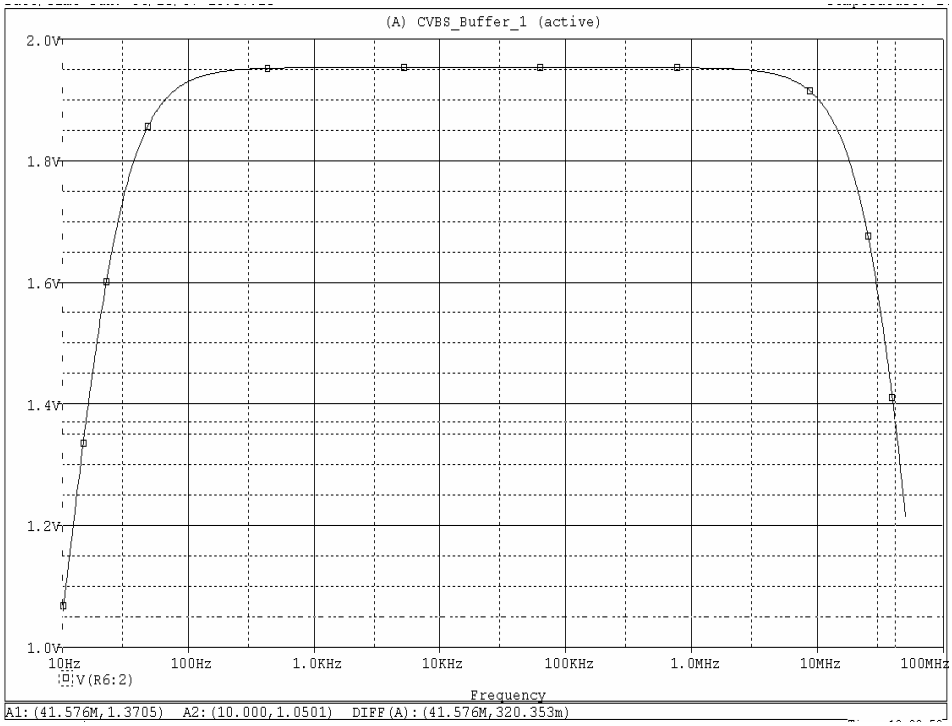


Figure 6.5. Frequency response of the video amplifier

Audio amplifier circuitries are used for audio outputs, the output signal amplitude specification is 2Vrms. The output level at audio processor output is 500mVrms to provide 2Vrms audio output OPAMP amplifier circuitries are used at positions U151 and U152. Audio amplification can also be realized with active transistor circuitries but OPAMP amplifier is used considering linearity, PSRR and SNR.

YPbPr video is high bandwidth analog video, up to 1080p resolution is defined which has around 150 MHz pixel clock and 75 MHz analog video bandwidth. Audio signal of YPbPr is standard base band analog audio. Connector which has 6 RCA input used for YPbPr input, three for Y, Pb and Pr component video, two for R / L audio and remaining one is used for SPDIF digital sound output. Similar to SCART application double sided zener diodes are used for ESD protection.

Because the signal BW is high, video signals are connected directly to the scaler chip and great effort is dedicated in layout stage, in layout high BW signal lines are directly connected without using via.

RCA connector with three outputs is used to connect audio R/L line out and subwoofer output. Incase of subwoofer is not required optional CVBS output is connected by switch jumper. Automatic switching of CVBS and sub-woofer audio signal can implemented with the circuitry given in Figure 6.6.

The operation principle of the circuitry depends to the characteristic impedance measurement of the line. By specification video signals are terminated with 75 ohms and audio signals are terminated with impedance greater than 10k. Q1 transistor in Figure 6.6 is the buffer transistor and the sink current from buffer transistor varies depending to the termination impedance. Current is mirrored by current mirror architecture (Q2 and Q3) mirrored current is converted to voltage and low pass filtered on resistor and capacitor network. Depending to the voltage level M1 and M2 transistors are switched. If impedance is lower than curtain value M2 transistor is on else M1 transistor is on. This architecture provides automatic sink device type detection and signal source switching. Output impedance of the circuit is 75 ohms which is specified for video sources and also convenient for audio source.

Audio line out signal also use the same amplifier circuit output with SCART_2 audio out, but they are DC isolated by coupling capacitor.

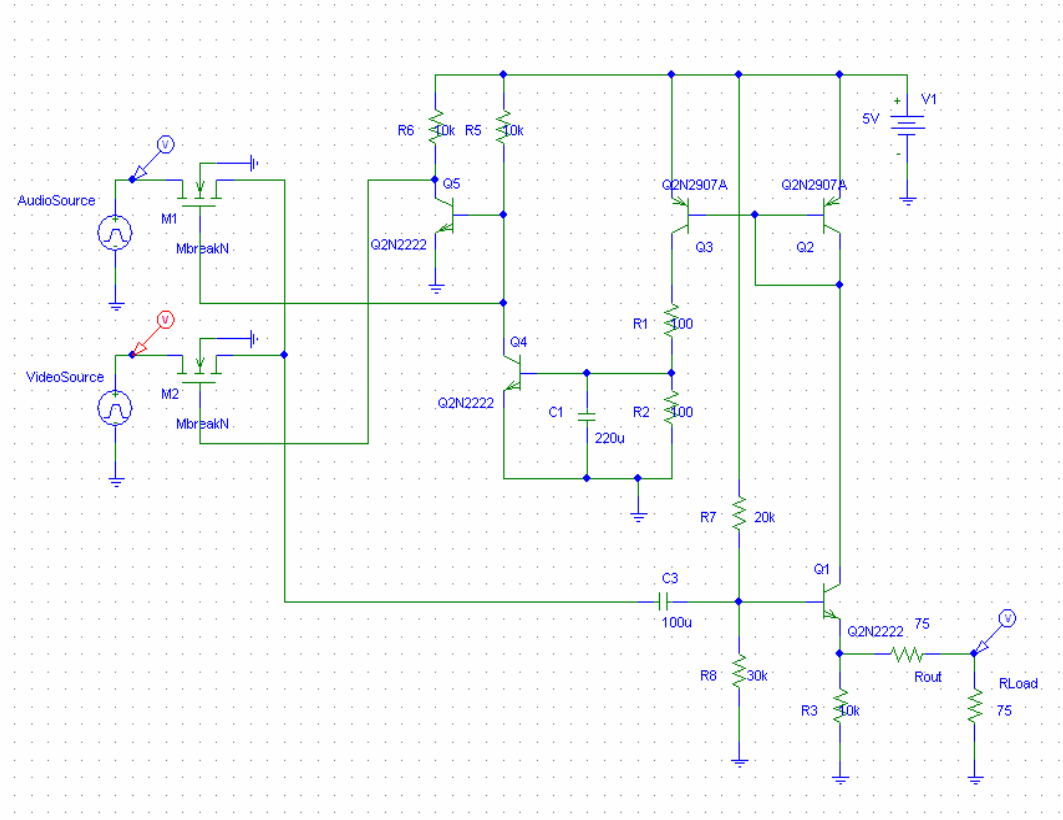


Figure 6.6. Automatic source switching circuit

SCART, YPbPr, Lineout connections circuitries and audio amplifier circuitries are in second page of schematic and given in Figure 6.7.

PC video is also high BW signal, via VGA connector PC video signal is connected to TV set. PC audio is connected via audio jack. PC video is RGB video with separated Horizontal and Vertical (H/V) synchronization signal. PC RGB video is directly connected to scaler and great effort dedicated to video lines in layout stage. Supported PC resolutions are defined and stored in U112 E2PROM. PC interface is given in third page of the schematic and given in Figure 6.8.

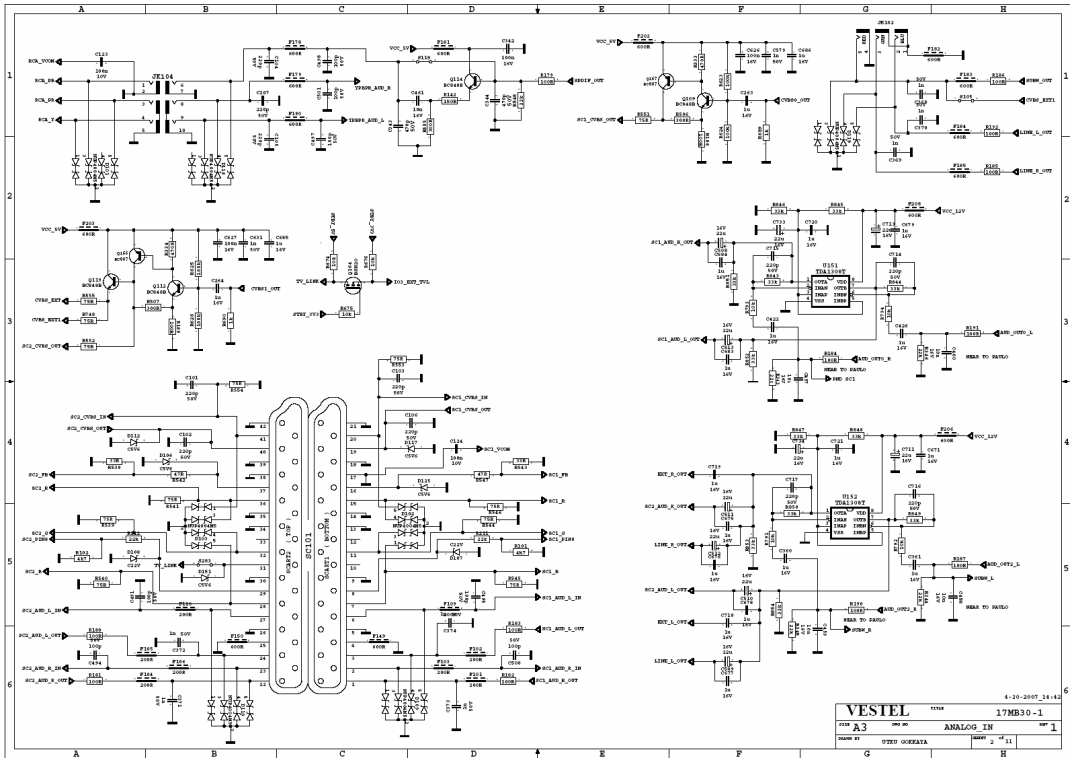


Figure 6.7. Page2 of the schematic

6.3.4. HDMI Interface

HDMI video interface become standard feature of current mid-end flat panel display TV's, in requirement specification double HDMI input is defined. There are two ways for supporting double HDMI input. First one is using TMDS switch and using single receiver and the second is using dedicated double receiver. MST6W includes double HDMI receiver inside, no external switch used, TDMS lines of both HDMI_1 and HDMI_2 are directly connected to MST6W. TMDS lines data rate is up to 1.6 Gbits/s, switching such a signal is as difficult as designing a receiver. U108 and U109 are E2PROM for storing DDC file, via I2C interface HDMI transmitter, receiver and E2PROM communicate. U101 and U102 are MOS transistors acts as buffer and used to isolate receiver's and transmitter's I2C bus. U116 and U117 are ESD protection circuitries. HDMI circuit diagram is given in third page of the schematic and given in Figure 6.8.

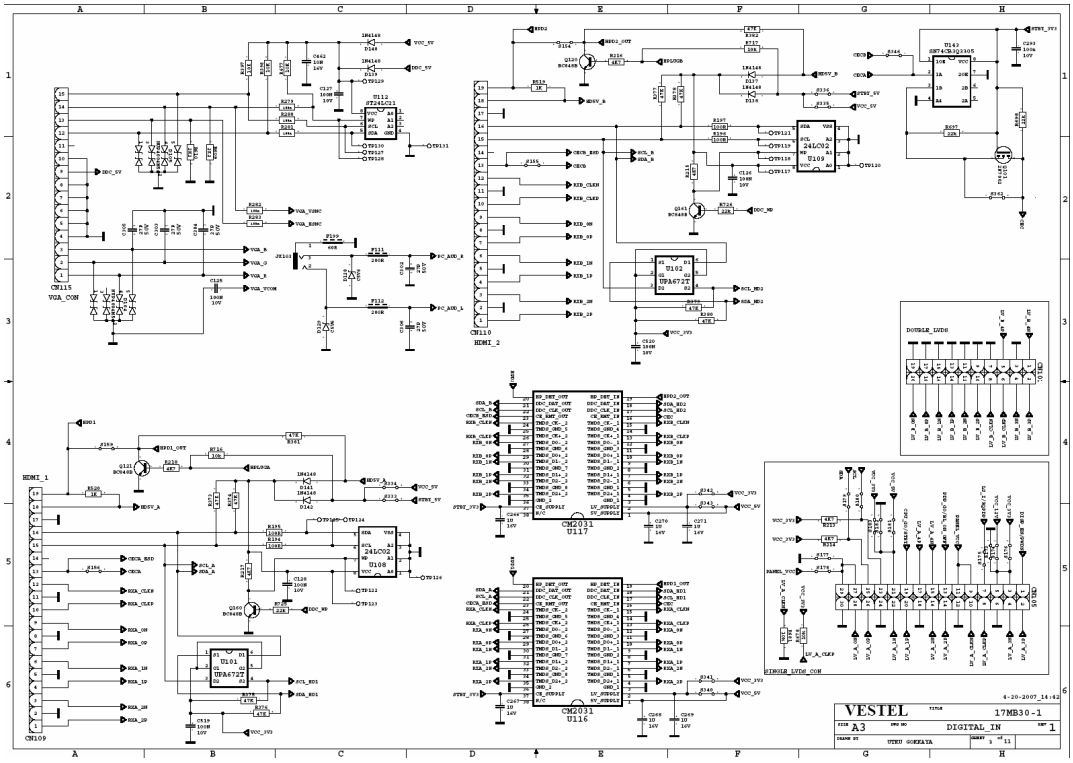


Figure 6.8. Page3 of the schematic

6.3.5 MPEG Decoder

MPEG decoding is the basic block of digital terrestrial reception, COFDM decoder converts IF band digital signal to base band transport stream. Transport stream includes MPEG encoded digital data, via transport stream signaling encoded digital data is transferred to MPEG decoder which will decode encoded signal to row data. MPEG decoder (U103) functionalities are digital terrestrial reception part system control, Common Interface module control and MPEG decoding. For program memory external flash (U115) is used. For the requirement of dynamic memory external DDR (U131) is used. DDR memory interface is 16 bit and maximum clock frequency is at 133 MHz which equals 266 bit/s for each data pin. Depending to application memory size of both flash and DDR is variable. U103 is the unified digital system controller and MPEG decoder which include processor for system controlling and decoder for MPEG audio and video decoding. MPEG encoded data stream (transport stream) output of COFDM demodulator is MPEG decoded to row data and converted to CVBS, RGB, ITU.656 video formats and SPDIF, I2S audio formats.

Connectivity of MPEG decoder to COFDM demodulator and Common Interface module (CN120) is via interface buffers, transport stream is switched by CI buffers, if there is no CI card available stream is directly send from COFDM demodulator to MPEG decoder otherwise stream is switched to CI module card and over module card stream decoded and send back to MPEG decoder. MPEG decoder is connected via buffers which have the functionality as switches to COFDM demodulator and CI module card. DDR and Flash memory interfaces are parallel memory interface. Audio and video outputs of U103 are connected to audio & video processor. MPEG decoder is given in Figure 6.9 on page 4 of the schematic, memory interface is Figure 6.10 on page 5 and CI module interface and buffers are given in Figure 6.11 on page 6 of the schematic.

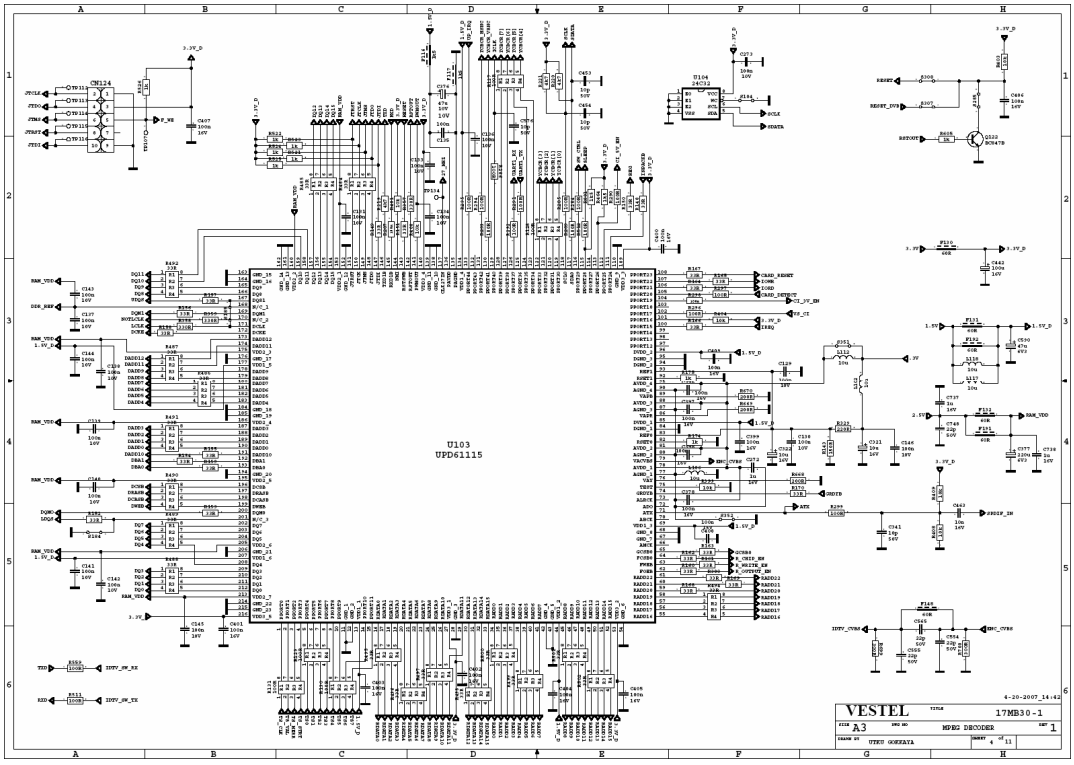


Figure 6.9. Page4 of the schematic

As explained before U103 is the system controller and MPEG decoder via serial resistor connected to flash and DDR memories. Serial resistors are used to reduce electromagnetic radiation.

CN124 is the JTAG interface which is used for system programming and debugging, via JTAG interface flash can be reprogrammed and both HW and SW

system can be debugged. JTAG interface is an important connectivity for development stage and production stage. In development stage SW emulator can be run via JTAG interface which simulates system code operation line by line and via this interface every HW connection and connectivity can be checked which provides quick HW development and fault detect.

In production stage, the feature of JTAG interface to program flash on board and HW connectivity check increase efficiency and reliability of production stage. JTAG interface is used both in development and production stage and increase efficiency in both stages.

U104 is the E2PROM which is connected via I2C interface, channel data is stored inside.

MPEG decoder, COFDM demodulator, CI module and interface forms digital part of the system. MPEG decoder U103 is also the system controller of the digital part. Communication of digital part with analog part is supplied with UART interface. The main system controller is the analog part's controller and digital part's controller operates as a slave.

U131 is the DDR memory of digital part, dynamic data is stored in this memory, for MPEG decoding memory buffer is needed and as the dynamic memory buffer U131 is used. Data bus of the DDR interface is 16 bit and the memory sizes up to 64 Mbytes are supported, depending to application memory size is defined. Memory band width is an important parameter in DDR memory interface. System clock operation is 133MHz, in DDR memories both in rising and falling edges of clock data is sampled, 16 bit data operating at 133 MHz clock provides 532Mbytes/s memory bandwidth.

System code is stored in flash memory, U115 is the flash memory depending to code size which is related with application flash size is variable. System code is once read from flash and downloaded to DDR memory at power up stage and code is operated from DDR memory, this application is used because of bandwidth limitations of flash memories. System code should operate faster to realize system requirements. U129 and X101 is used to synthesize system clock.

Common interface module is a must for digital terrestrial reception TV sets, via this interface encryption of digital data stream is supplied. Digital stream coming from COFDM demodulator should be switched.

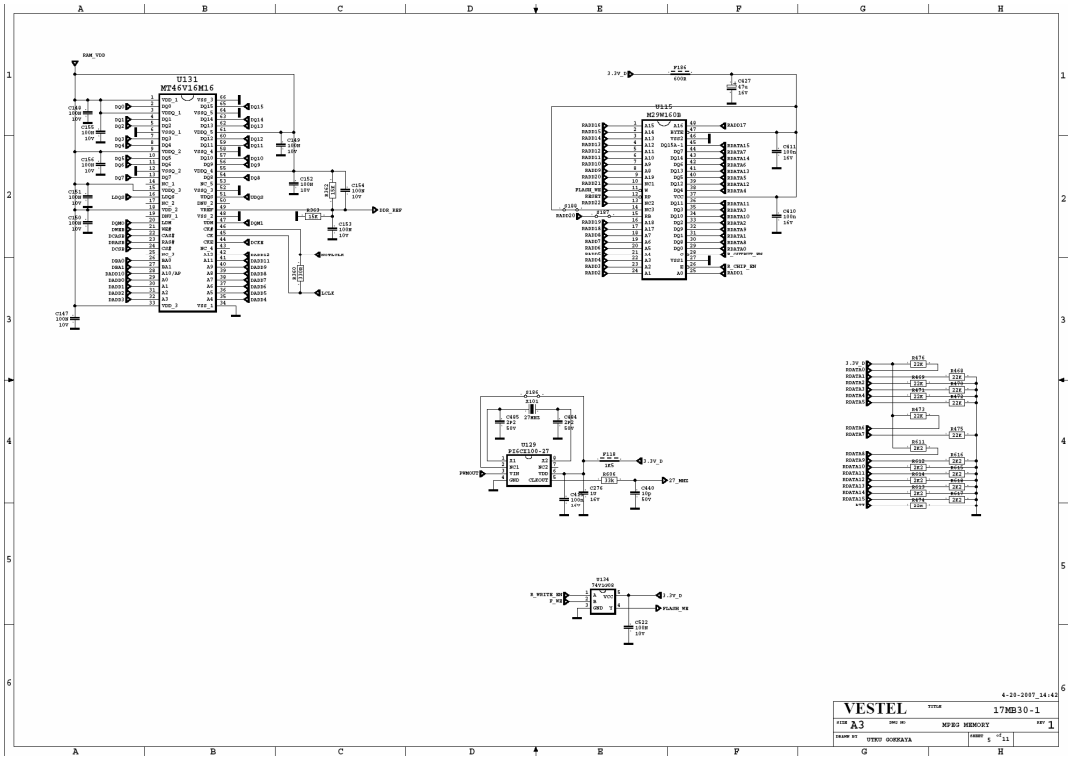


Figure 6.10. Page5 of the schematic

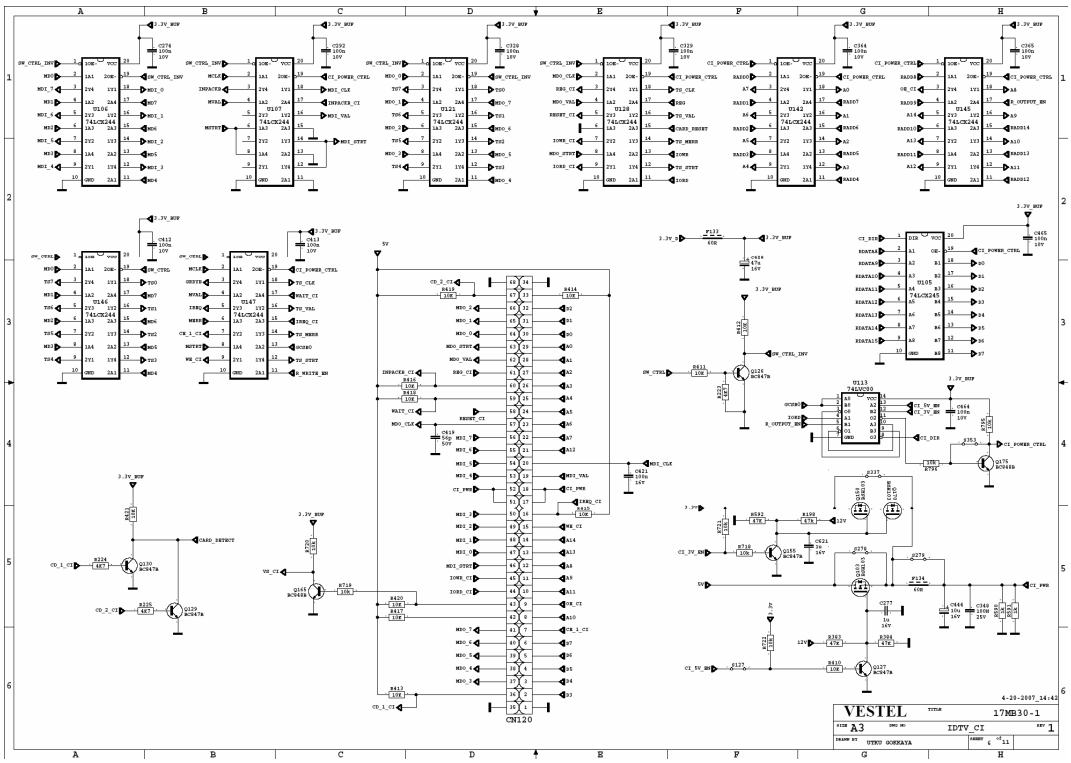


Figure 6.11. Page6 of the schematic

6.3.6. Scaler & De-interlacer

In current technology WXGA (1366x768) LCD panels are commonly used, video input resolution has wide range, starting from SD resolution up to 1920x1080 for YPbPr and UXGA resolution for PC. PAL and NTSC are the standard video signals with SD resolution and interlaced timing. Flat panels have WXGA resolution and progressive scan, de-interlacing and scaling are the basic blocks in flat panel TV sets. In first LCD TVs scaler and de-interlacer were separate chips, video decoder, CPU and Audio processor were also separate chips, but with the development of silicon technology these chip sets become single chip. Single chip including video decoder, CPU, audio processor, de-interlacer and scaler is available in current technology, remaining from the past this chip combination is called as scaler & de-interlacer but actually includes also the other building blocks.

In design as the heart of the system single chip solution MST6W is used, which including video decoder, video and audio ADCs, audio and video processor, 8051 based CPU, de-interlacer, scaler and video enhancement blocks.

Audio and video interfaces of MST6W are, two HDMI inputs, three component video for RGB or YPbPr, 8 CVBS inputs 4 can be configured as SVHS input, two port can be configured as digital video input (ITU.656 or 601) but in our application single digital port is used for video interface, the other port configured as GPIO port. MST6W has QSS audio input, 4 analog R/L audio inputs and one mono input, four analog audio outputs, digital audio SPDIF in and output, two CVBS video outputs for SCART video outputs. MST6W can drive flat panels with single and double LVDS output.

Supply voltages of MST6W are 1.2V, 2.5V and 3.3V, 1.2V is core and digital processing parts supply voltage, 2.5V is the DDR memory interface supply voltage and 3.3V is the ADCs supply voltage. MST6W is manufactured with 0.13um silicon process which requires 1.2V supply voltage. With silicon technology development channel length decreased to nm scales, which provides lower supply voltage operation and reduced silicon area (die size) for the same number of transistors. Reduction of die size provides integration of several chips into one, reduction of supply voltage level decrease power consumption and power dissipation. Power dissipation is a critical point in system operating at high frequency because power consumption is directly proportion to operating frequency. Power consumption can be given as in equation 6.1 below, V is the

supply voltage, C is the total capacitive load and F is the operating frequency. (WEB_5 2007)

$$P_{consumption} = V^2 \times C \times F \tag{6.1}$$

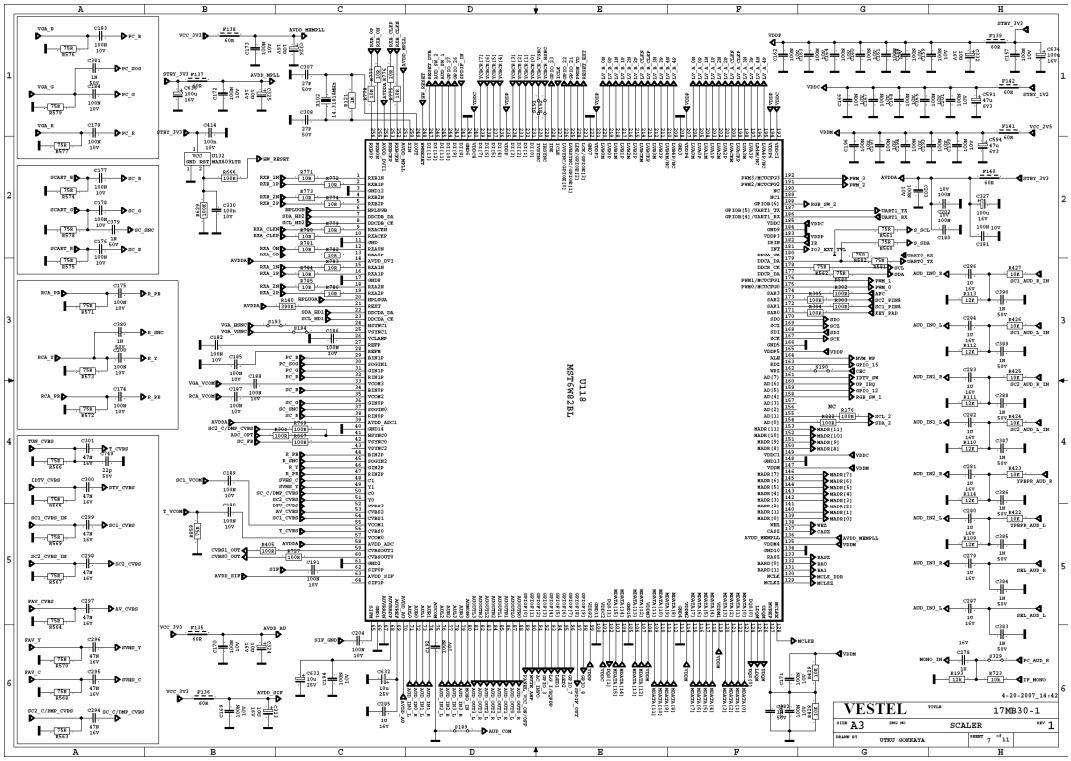


Figure 6.12. Page7 of the schematic

For each voltage supply pin 100nF SMD capacitors are used, these capacitors placed nearby to pins and high frequency current requirement is supply by these capacitors, at high frequency power lines can not supply current because of inductance effect of copper line at that point capacitors placed nearby to supply pins to supply required current. The other function of these capacitors is for EMI, digital circuitries radiate noise to supply and if it is not filtered can spread to all system, capacitors located near to supply pins are filters for noise.

Seventh page of schematic including single chip connectivity is given in Figure 6.12. Termination resistors for video signals are left hand side of the page and these resistors should be placed as close as possible to the chip for better SNR. Audio input termination resistors are at the right hand side of the page and these resistors also should be placed nearby. Audio signals are voltage divided before connected to chip, the reason is audio input signal level can exceed the maximum voltage level which can be entered

to chip. U132 is the hard reset circuitry, its supply is connected to STBY_3V3, incase of this supply level variation this circuitry resets CPU, 2.93V is the threshold voltage of the reset circuitry.

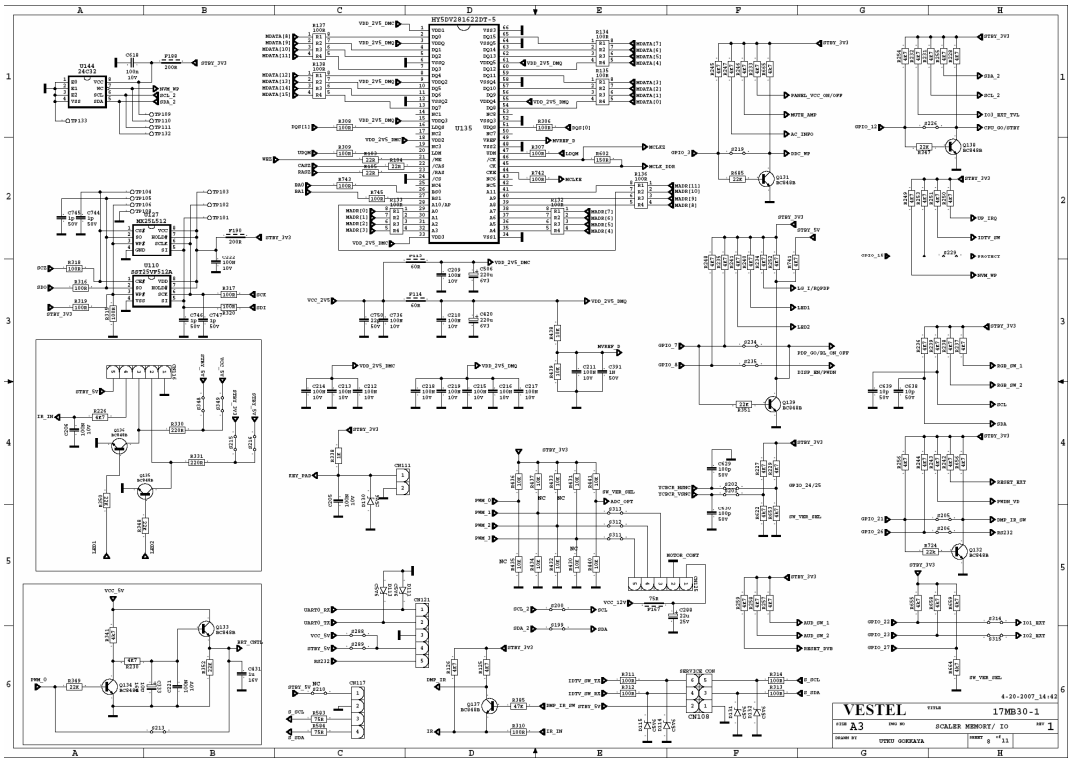


Figure 6.13. Page8 of the schematic

GPIO port number is a critical item in design, in design several combination of product aimed to be supported, this case require several I/O control. In design thirty GPIO s are used for several kind of functions. Two separate I2C communication port are assigned, one for general communication and one for E2PROM. Because of E2PROM stores critical data specific to product, E2 should be safe in any case. Communication between digital part and analog part is provided via UART interface, the second UART interface is used for RS232 communication, in system programming (ISP) and system debugging. Two GPIO are used for controlling led, for audio and video switching four GPIO are used, one PWM output is used for backlight dimming function. For power on/off sequence, short circuit protection and for the other devices or modules control the rest of the GPIO are used. GPIO connectivity is given on page eight of schematic in Figure 6.13.

Signal connectivity to scaler is; CVBS, VGA, SVHS, YPbPr video signals are directly connected from connector to scaler, for video only SCART RGB and optional RGB video are switched by two RGB switches (U122 and U123). SCART RGB s are default feature of set, in case of only two SCART RGB only U122 RGB switch is used for SCART1 and SCART2 RGB switching, also for optional RGB is desired, second switch U123 is used to switch SCART2 RGB and optional RGB. These two RGB switches are the only video switching on video processing board. RGB switches are on ninth page of schematic. Audio switching is also needed in design and 74HC4052 (U120) is used for switching PC audio, Side AV board audio and optional RGB module's audio. U120 has four dual inputs and one dual output, on page ten of schematic audio switching circuitry is given.

System memory requirement is 16 Mbytes DDR and 1 Mbytes Serial Flash, DDR memory has 16 bit data bus and operates at 200 MHz, with these values memory BW is 800 Mbytes/S. U135 is the DDR memory and U127 is the flash memory which are on page eight of schematic given in Figure 6.13.

6.3.7. Display Interface

LVDS (Low voltage Differential Signaling) is the common signal interface between video processing board and TCON (Timer controller) panel driver board. Panel resolutions are increasing definitely and also panel refresh rate will increase from 50 Hz to 100 Hz near future. In case of resolution or refresh rate increase single LVDS interface module will not be enough, second LVDS interface module is decided to use as an optional feature. LVDS interface is not the only connection between panel and processing board. GPIO ports and I2C communication are used to interface with panels.

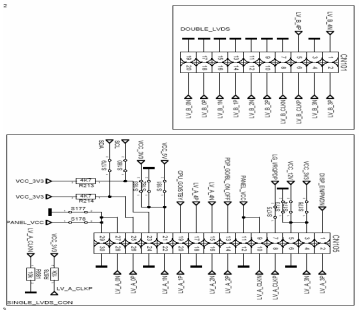


Figure 6.14. Display interface connector

Power requirement of panel is supplied by power supply and power sequence is controlled by processing board. LVDS connectivity is given in Figure 6.14.

6.3.8. PIP Video Decoder

Scaler IC (MST6W) has one video decoder inside and PIP (picture in picture, two pictures side by side) function is desired in system functions, for PIP applications of two CVBS video additional video decoder is used. ADV7180 (U133) with six analog inputs is used as second video decoder in design, number of analog input is important for system cost reduction. Side board CVBS and SVHS (Y+C), SCART 1 and 2 CVBS, Tuner CVBS are the six analog video inputs of the video decoder (Analog Devices 2006). Because the video decoder is low voltage design, maximum video level at the input is 0.5Vpp, to meet this requirement resistor divider circuit (1/2) is used to arrange the required video level. The connectivity with video decoder and scaler is via ITU.656 digital video interface. Decoded analog video is transferred via ITU.656 interface to MST6W. Supply voltages of video decoder are 3.3V and 1.8V. Schematic data of video decoder is on page nine of the schematic given in Figure 6.15.

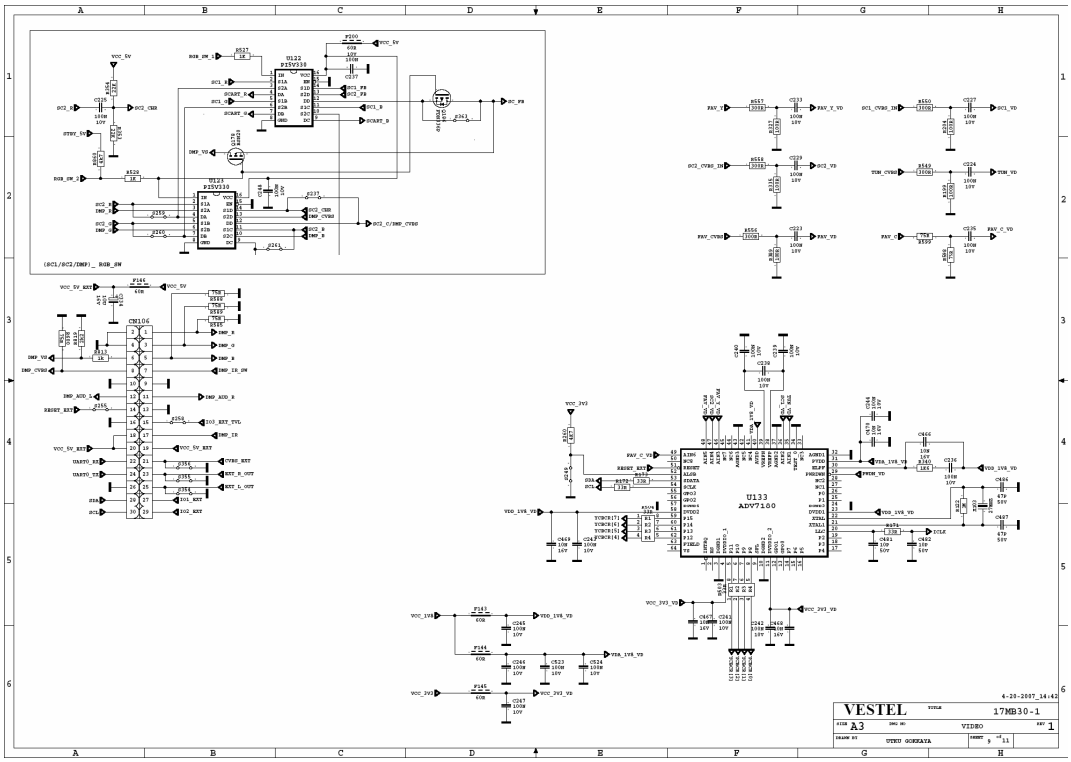


Figure 6.15. Page9 of the schematic

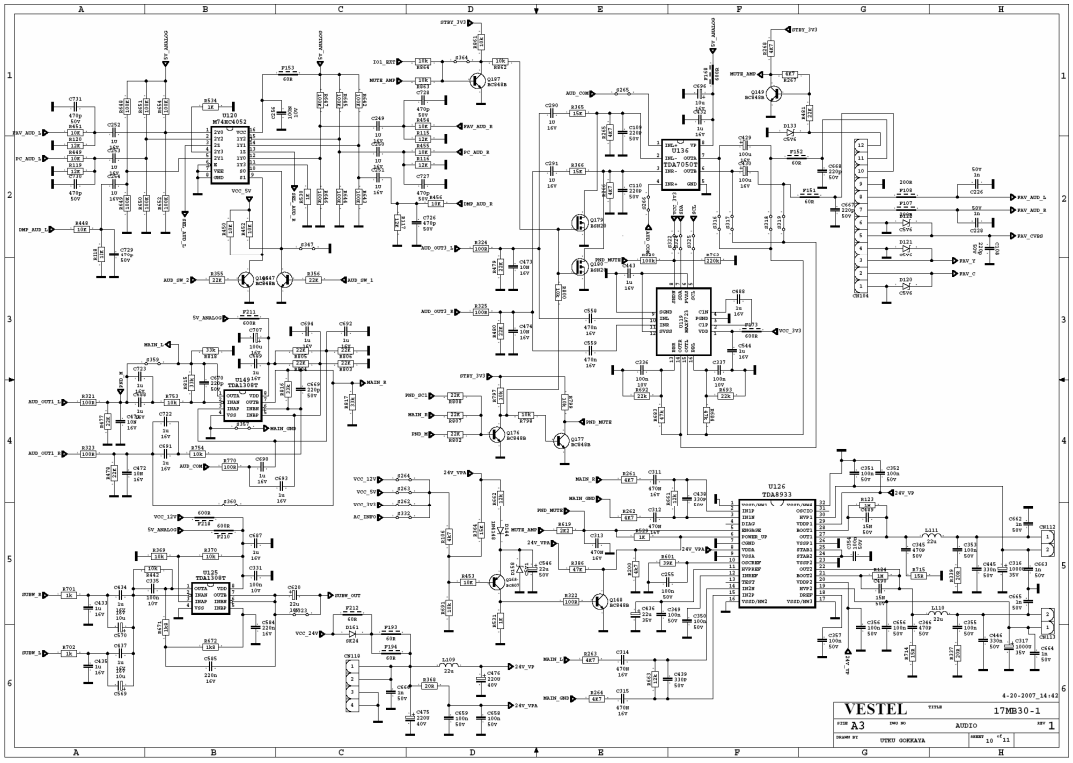


Figure 6.16. Page10 of the schematic

6.3.9. Audio Amplifier

6.3.9.1. Class-D Audio Amplifier

Flat TV designs use Class-D audio amplifiers, because of high efficiency of these amplifiers additional heat sink is not required, this advantage reduce cost by reducing system power requirement and heat sink's cost. System requirement for audio output power is 8x2 W at 10% THD. Considering system requirement TDA8933 (U126) is used as audio amplifier circuit, amplifier has differential input but the audio source (audio processor's DAC output) has single ended output, ground of the DAC is used as the negative signal line for noise cancellation, this method is used for increasing system immunity to noise and achieving better SNR at the speaker output. Ground line of the DAC output is the differential line and in layout this line should use the same way with the signal line (Mstar 2006).

Analog signal is multiplied with triangle wave and passed through comparator, by this way analog audio's data in amplitude and in time is converted to pulse width

modulated signal. Pulse widths carry amplitude and time data of audio signal. Pulse width modulated signal drives FET s. This method increase efficiency of the amplifier because drop out voltage on drain-source is minimized and power dissipation on the amplifier is also minimized which increase total efficiency. Class-D amplifier output is pulse width modulated, depending to supply voltage of amplifier switching pulses between supply voltage and ground level can be observed at amplifier output. Frequency spectrum of pulse width modulated signal includes base band analog audio spectrum and high frequency components. For filtering high frequency components and recover base band audio signal, amplifier output is filtered by inductor and capacitor network. Class-D amplifier schematic is on page ten of the schematic and given in Figure 6.16 (Philips 2006a).

Pop sound is one of the common problems for audio amplifier design, during power on and off interval because of the power supply variations pop sound observed. In audio amplifier design to solve this problem, circuitry formed Q176, Q177 is used to mute amplifier during power on and off transitions. The operation idea of the circuit is, until valid data is outputted from audio processor DAC output Q176 transistor is off and U126 is in mute state. When DAC output has valid data which has DC offset level Q176 transistor is on and U126 is in operation.

Block diagram of pop sound mute circuitry designed is given in Figure 6.17.

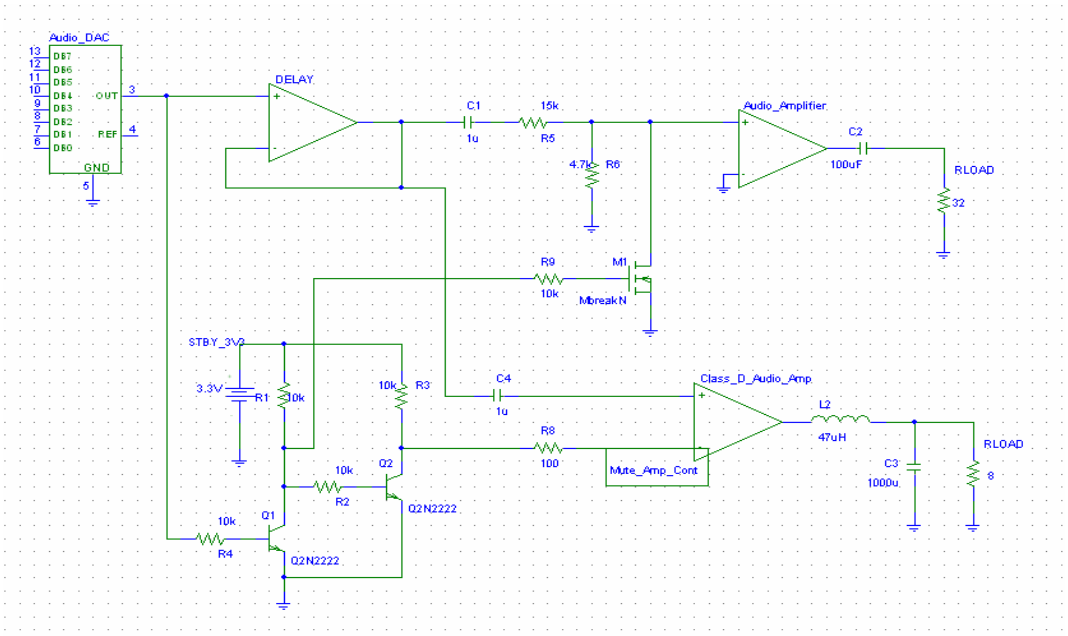


Figure 6.17. Pop sound mute circuitry

6.3.9.2. Headphone Amplifier

Head Phone output is the default feature of designed TV, and in PIP application HP output should be selected as the second displayed source. In case of PIP the volume controlled HP amplifier (MAX9723, U119) (Maxim 2005) is used because lack of audio processor to cover the requirement. TDA7050 (U136) (Philips 1994) is the fixed gain HP amplifier is used in the products which do not have the PIP feature. Products with PIP feature have U119 and the others have U136. Both amplifiers are analog amplifiers and schematic data is on page ten of the schematic which is given in Figure 6.16.

Pop sound is also problem for headphone output, same circuitry formed by Q176 and Q177 is used also for headphone pop sound problem. Because headphone amplifier has no direct mute control Q179 and Q180 is used as mute control circuit, whether transistors are on state headphone input signal is muted.

6.3.9.3. Sub-Woofer Amplifier

Sub-woofer is an optional feature of design, but audio processor has no sub-woofer output. Sub-woofer is single channel audio with 20 Hz to 200 Hz BW, TDA1308 (U125) has two OPAMP inside, first one is used for adding right and left channel, amplification and first ordered low-pass filtering and the second OPAMP is used for second ordered LP filtering. The Sub-woofer circuitry is on page ten of the schematic which is given in Figure 6.16. Circuitry and the PSpice simulation results for frequency response are given in Figure 6.18 and Figure 6.19 respectively. Critical values are, 3dB low cutoff is 10 Hz, 3dB high cutoff is 200 Hz, 18.3 dB voltage gain, 60db/decade suppression frequency response (3 poles).

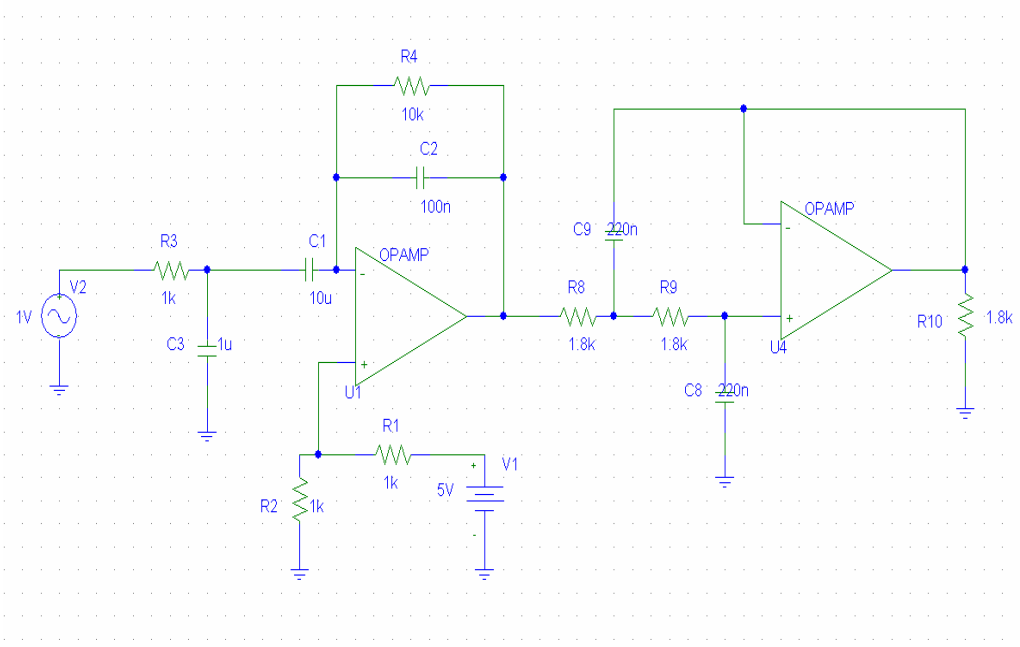


Figure 6.18. Subwoofer amplifier circuitry

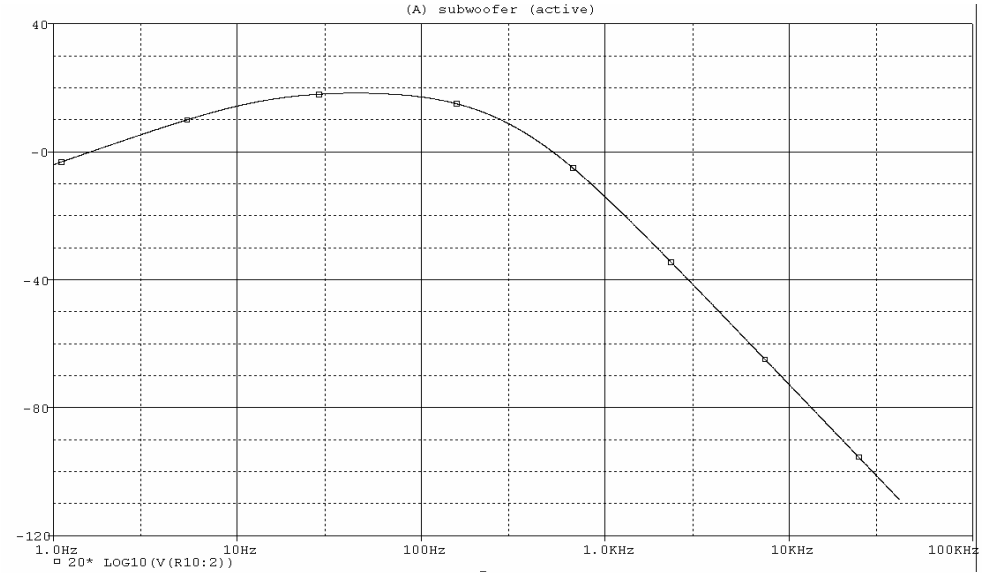


Figure 6.19. Subwoofer amplifier frequency response

6.3.10. Power Management

Power management first item is to define system power requirement, system also divided into two sub-system as power management, first one is DVB-T reception module (IDTV module) and the second one is standard analog processing part. Digital module power consumption is given in Table 6.3, analog part's maximum power

consumption is given in Table 6.4 and typical current consumption of analog part is given in Table 6.5.

Table 6.3. Current consumption of digital module

IC	1.5V	2.5V	3.3V	5V
EMMA2LL	350mA	50mA	130mA	
UPD61150	120		100mA	
DDR RAM		300mA		
FLASH			50mA	
CI BUFFERS&GATES			100mA	
CI				300mA
Max. TOTAL CURRENT	470mA	350mA	380mA	300mA
Typical Current	430mA	310mA	330mA	270mA

Table 6.4. Maximum current consumption of analog TV

IC	1.2V	1.8V	2.5V	3.3V	5V	24V
M-STAR	370mA		34mA	600mA		
Front-END					400mA	
DDR RAM			400mA			
FLASH				50mA		
ADV7180		160mA		3mA		
Class-D						1A
TOTAL CURRENT	370mA	160mA	434mA	653mA	400mA	1A

Table 6.5. Typical current consumption of analog TV

IC	1.2V	1.8V	2.5V	3.3V	5V	24V
M-STAR	330mA		30mA	500mA		
Front-END					300mA	
DDR RAM			300mA			
FLASH				50mA		
ADV7180		140mA		3mA		
Class-D						1A
TOTAL CURRENT	330mA	140mA	330mA	553mA	300mA	1A

Considering system power requirement in voltages and currents the power diagram formed. 3.3V and 5V is available from power supply for both standby and power on stages. The required missing voltages are generated on processing board. U138 FAN2012 (Fairchild 2006) is the switching step-down regulator is used to generate 2.5V which will supply current to DDR memories. As an alternative cost reduction solution for 2.5V generation BA159 (D159 and D160) are used. The core supply voltage of MST6W is 1.2V and this voltage is generated with linear regulator LM1117 (U139) (National 2006). The core supply voltage of the MPEG decoder and COFDM demodulator is 1.5V and also for this supply linear regulator LM1117 is used at position U140. External video decoder's core voltage is 1.8V and is also generated by LM1117 linear regulator (U141). Tuner supply voltage 5V can be directly used from power supply but this voltage is used for several circuitries in TV set and hybrid tuner is very sensitive to power supply noise especially digital RF reception sensitivity and immunity is affected by power supply noise. Separate linear regulators are used to supply current to tuner and front-end to improve system performance. U150 is used to generate 5V supply for tuner. The only supply voltage to generate 5V is 12V, and in this case drop out voltage is 7V, because the drop out voltage is huge power dissipation on regulator will be (current 250mA, multiplied with voltage drop 7V) 1.5W. This amount of power dissipation on one regulator will damage the regulator. Because of heat issue serial resistors are used to reduce dissipated power on regulator.

Power on sequence of panel requirement varies depending to panel vendor, to meet panel power on sequence requirement Q128 is used as power switch of the panel logic voltage.

33V is used in some kind of tuners for VCO control voltage, for some power supply models 33V is not available from power supply in this case it is generated from 12V from self oscillating circuitry (Q151, L104 and L105).

Plasma power supplies may not have 3.3V in this case to generate 3.3V standby from 5V U137 MP1593 is used and by switching this voltage VCC 3.3V is generated. Q102 is the voltage switching FET used for this issue.

In small size panels, power supply only has 12V and 5V standby voltages and the other voltages are needed to be generated from these two supplies. Power management architecture is realized considering this case. Because only standby voltages are available in case of small size display application, VCC voltages are

generated by MOSFET switch control from the standby voltages. Q102, Q181, Q182 power switching elements are used for this purpose.

The power management schematic is given below in Figure 6.20 which is the eleventh and the last page of the schematic.

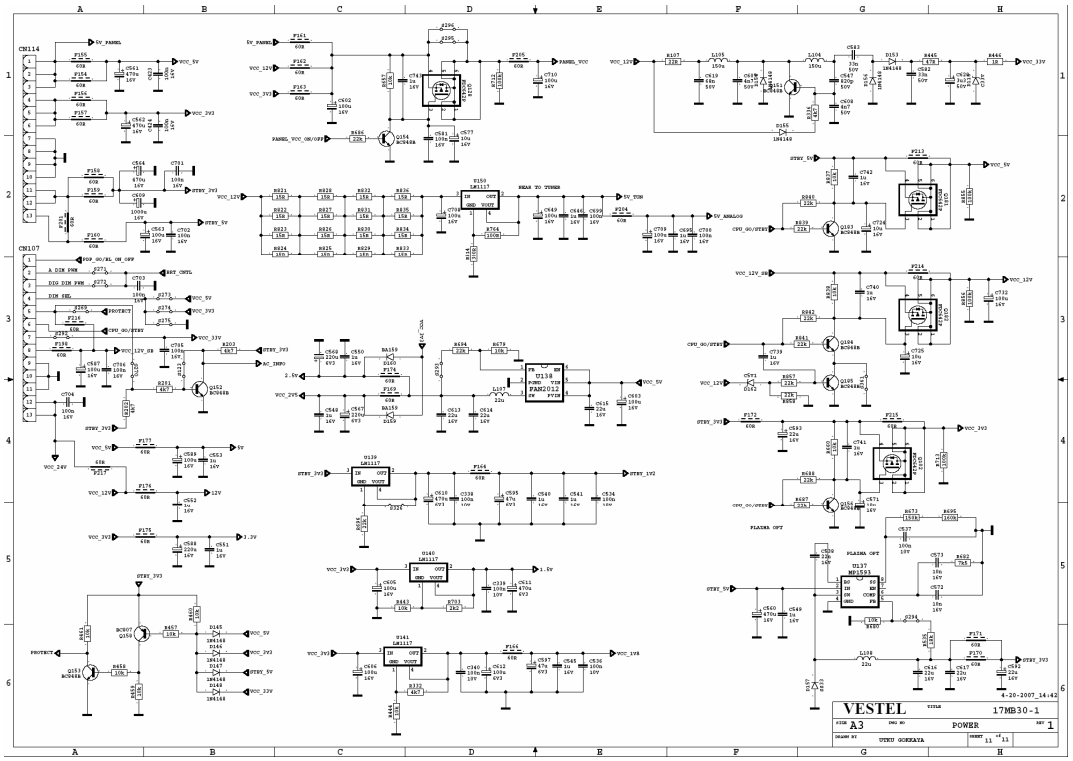


Figure 6.20. Page11 of the schematic

6.4. Layout Design

Layout design is the most important part of the system design which has great factor on system performance. Each signal type used in TV processing board and layout considerations for these will be investigated in this chapter's parts. In layout design four layer PCB is used, top and the bottom layers are the signal layers, second layer is the reference layer and the third layer is the power layer. For the signals which are impedance sensitive first layer is used because impedance controlled lines can be realized on the first layer by using the second layer as the reference layer.

6.4.1. Analog Signals

Analog signals are the most sensitive signals to noise and cross-talk, great effort should be dedicated to analog signal lines layout. Video and audio signals are the two types of analog signals used in TV board. Around the analog signal lines ground shielding method is used to protect signals from cross talk and noise.

6.4.1.1. Video Signal

Most common analog video signal is CVBS video with 8 MHz BW but addition to CVBS YPbPr and PC RGB video signals are the high BW video signals. For all video signals 75 ohm termination resistance is standard and must. The position of the termination resistance should be near to the video processing IC for better signal quality. The characteristic impedance of video signal line should be also 75 ohms which provides zero reflection coefficient. If possible all video signal lines should not use via which means discontinuity on the signal line which disturbs line impedance and BW.

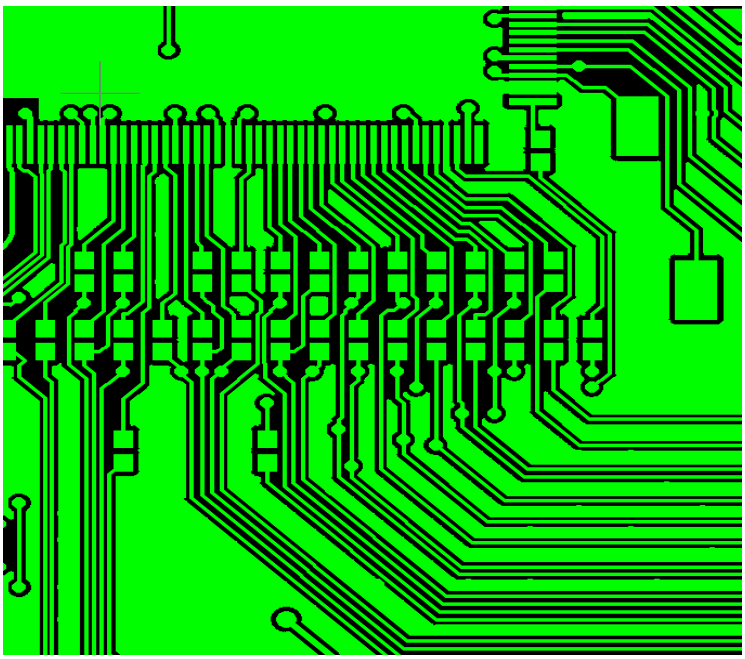


Figure 6.21. Video signals layout

Especially for the high BW signal lines, definitely via should not be used considering signal quality. In layout design of video signals line impedance and signal routings without via are considered, termination resistors are located near to IC as shown in Figure 6.21.

Analog signals are sensitive to noise and cross-talk, these signal lines should be routed away from noisy circuitries such as switching power regulators, digital lines, power lines. Shield lines surrounding analog signals are used to prevent cross-talk and noise effect. In Figure 6.21 shield lines actually ground layer can be seen, which are surrounding signal lines. If the ground of ADC input of the IC is separated internally it is better to use ground line which is connecting ground at the connector point to the IC, this ground line is also connected together with the signals. This type of connectivity provides differential signaling which improves immunity of signal to noise. In Figure 6.21 four signal lines at the left hand side are PC RGB and GND signals and beside four signal lines are YPbPr and GND lines, these signals are high BW signals and separate GND line is used to connect ADC reference ground to the ground at point of connector. First layer is used for the video lines because second layer is the reference layer this structure provides to realize impedance controlled line implementation. One another functionality of reference layer is to be used as shield at the bottom side of the signal line.

6.4.1.2. Audio Signal

Analog audio signals are low bandwidth analog signal; they are sensitive to noise and cross talk. Ground layer is used as shield around these signals to protect cross-talk and noise coupling. Most common problem in audio signal is deep noise which is sourced by power lines. Audio signals are also routed on reference plane which acts as shield between power plane and signal line. The most important audio signal line is which driving the audio amplifier, this line is routed taking care for noise and cross-talk. If the audio amplifier has differential input it is better to route ground as signal line from sound processor to the audio amplifier, as shown in Figure 6.22 GND point is routed as signal line between right and left signal channel, this structure provides both channel separation and differential signaling which improves signal immunity.

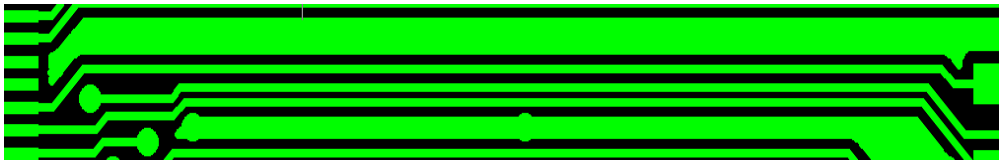


Figure 6.22. Audio signals layout

6.4.2. Digital Signals

Digital processing is used in TV system both video and audio are digitally processed. Addition to signal processing interfaces between systems are provided by digital signals. Digital signal interfaces used in TV systems are memory, display and HDMI video interfaces, in the following parts each will be investigated.

6.4.2.1. Memory Interface

In processing board design, high speed DDR memories are used. Design has two main blocks first part is the analog TV part and the second is the digital TV part which includes MPEG decoder. Both analog TV part and digital TV use DDR memories operating at 200 MHz and 133 MHz respectively. Memory BW requirement of TV processing board is increasing, memory BW is related with data bus width and operating frequency. High frequency signals routing is most difficult part of the layout design because both signal integrity and EMI should be considered together.

In design for signal integrity signal lines are routed with impedance controlled lines and length of the lines are matched. 60 ohm impedance is used for the single lines and for the differential lines 100 ohms is used. DDR signal lines can be grouped into four groups, data, address, clock and control signal lines. Data and clock operates at the maximum frequency, 200 MHz and 133 MHz in designed board, address lines operates at half of the operating frequency. Control signals maximum frequency is the half of the operating frequency. Clock and data bus is routed carefully, no via used for these signal lines and length of the data lines are matched for wider sampling interval. In Figure 6.23 signal routing of data and clock line of the DDR which operates at 200 MHz is shown. Line length matching and signal routing easily can be seen. Because of the operating frequency is quite high, maximum 45 degree turns are used considering both signal

integrity and EMI and no via is used for connection. Signal lines are directly connected without using via.

The address and control signals maximum frequency is the half of operating frequency but actually 100 MHz is still can be considered as high frequency. Similar attention is dedicated also to these lines, but incase of tradeoff between data and address line, data line has the priority.

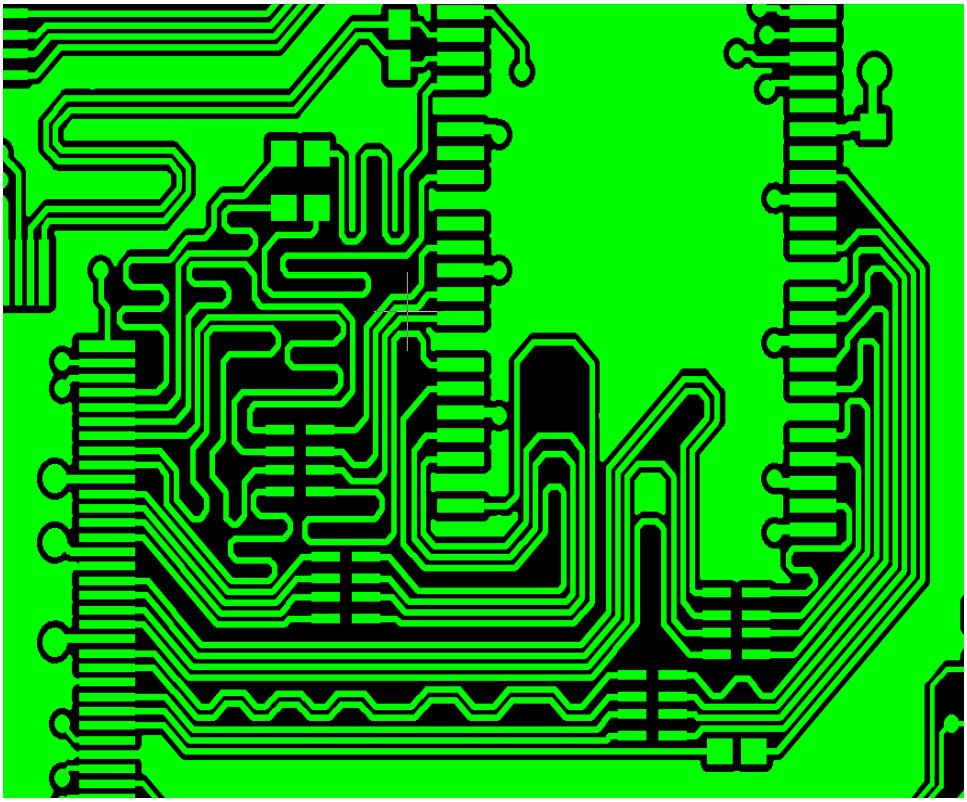


Figure 6.23. Memory interface layout

For both address and data lines 33 ohms serial resistors are used, these resistors acts as low pass filters which decrease overshoot and undershoot on signal but if the value increased over 100 ohms signal BW decrease and operation is effected. Eye diagram of the signal is the important parameter which defines signal quality. Serial resistors value has effect on eye diagram, depending to board parasitic capacitance and line impedance serial resistor value can varies for optimum result both considering signal integrity and EMI. Incase resistor values are increased electromagnetic radiation decrease, especially with the drawback of lower signal quality.

6.4.2.2. Display Interface

LVDS signaling is the common video signal interface between processing board and flat panel display. As the interface standard 3.5mA current is conducted on positive or negative path, the termination resistance at the LVDS receiver is 100 ohms, 350 mV voltage difference can be measured between positive and negative signal line. Eight bit LVDS interface has 5 channels one is used for clock and the other four is used for data. The serialization scheme of 7:1 is used for the data lines. The maximum frequency can be observed at data channel is 3.5 times clock frequency. Depending to the panel resolution pixel frequency is calculated, for WXGA (1366x768) panel around 75 MHz clock frequency is used.

LVDS lines are routed with impedance controlled lines, 100 ohm differential impedance is used for the signal line. The termination resistance is 100 ohm and for zero reflection coefficient 100 ohm differential impedance should be used. Differential lines are routed together their impedance is matched to 100 ohms and line lengths are also matched for signal integrity. In Figure 6.24 layout of LVDS lines are shown.

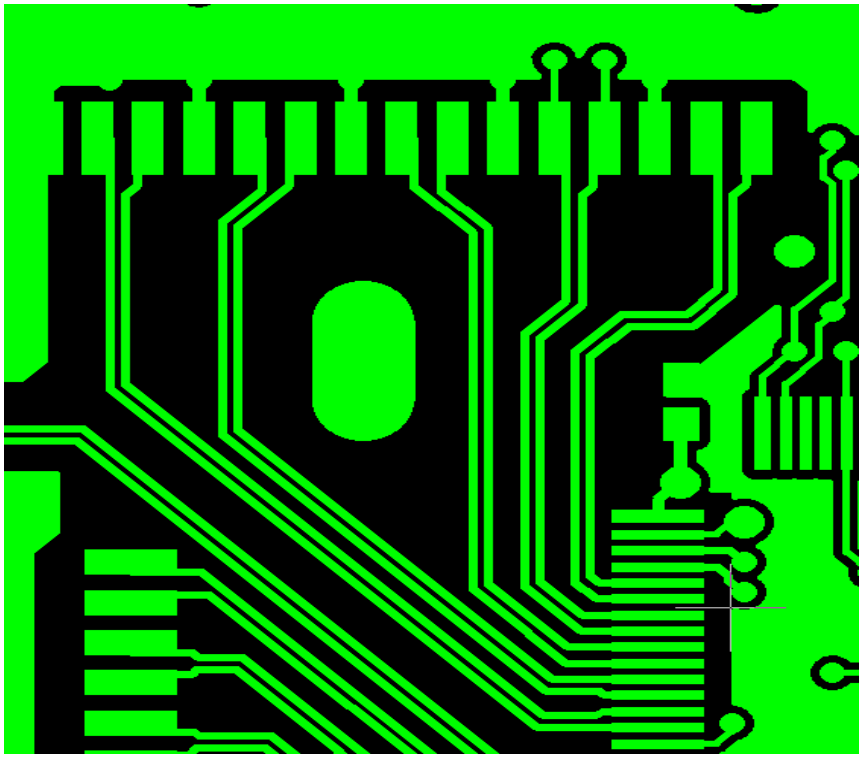


Figure 6.24. Display interface layout

6.4.2.3. HDMI Interface

High definition Multimedia Interface (HDMI) is the digital video and audio interface. High bandwidth row data is transferred via this interface. Depending to the video format interface bandwidth requirement increase, for HDMI 1.1 standard up to 1.6 G bit/S BW should be supported. The HDMI interface has to be certificated by authorized test house, test includes differential line impedance and communication lines parasitic capacitance measurement, because of this compulsory test HDMI layout is an important part in TV board layout. Differential impedance of TMDS lines are matched to 100 ohms and communication lines parasitic capacitance is minimized by minimizing line length and line width, for the lines which has to be routed long way buffers are used. HDMI interface has four differential TMDS lines, one is clock and the other three are data, the line length is an important parameter considering operating frequency, line lengths are also matched for signal integrity. The board has two HDMI input connectors for both input impedance matching and line length matching is done. In Figure 6.26 HDMI layout is shown, the differential lines are TMDS lines which are impedance matched to 100 ohms. In design the HDMI receiver is integrated to main chip and the location of the main chip is almost in the middle of the board because of total system considerations. In cases HDMI receiver is not integrated to main chip the receiver is located near to the HDMI input connector, in this case impedance matching and signal integrity considerations are more easily realized but in current design as explained before HDMI receiver is located at the middle of the board and TMDS lines are long which increase difficulty in signal integrity of these lines. While tracing HDMI lines maximum turn angle is 45 degree and the corners should be smoothed to reduce turning angle effect. To meet 100 ohms differential impedance specification 0.16mm line width and 0.34mm line spacing is used for HDMI lines. The height between first and second layer of the PCB is used as 0.12mm and Er of the fiberglass material used between two copper layers is 4.2. Differential impedance calculation is given in equation 6.2 (WEB_10 2007), where D is the spacing between two trace and H is the height between trace and reference plane. Z0 is the characteristic impedance of the micro strip line which is defined in equation 6.3 (Gupta et al. 1996). Addition to formulas Polar Si8000 simulation tool used to calculate differential impedance, simulation result with defined

values is 103.04 ohms and simulation result and program details are given in Figure 6.25.

$$Z_{diff} = 2Z_0(1-0.48e^{-0.96D/H}) \tag{6.2}$$

$$Z_{msl} = \frac{\sqrt{\mu_0/\varepsilon_0}}{\sqrt{\varepsilon_{r,eff}}}\left[\frac{w}{h}+1{,}393+0{,}667.\ln\left(\frac{w}{h}+1{,}444\right)\right]^{-1} \qquad \text{for w / h > 1}$$

where;

$$\varepsilon_{r,eff} = \frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\cdot func(w/h) \tag{6.3}$$

$$func(w/h) = \frac{1}{\sqrt{1+12h/w}} \qquad \text{for w / h > 1}$$

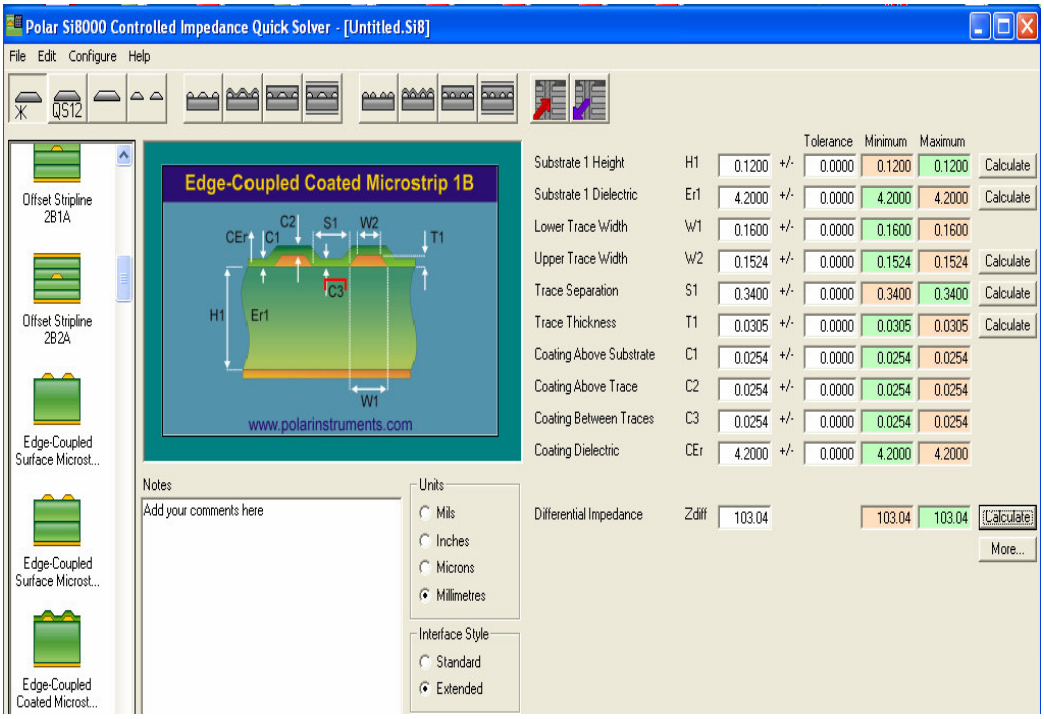


Figure 6.25. Polar Si8000 PCB impedance calculation program

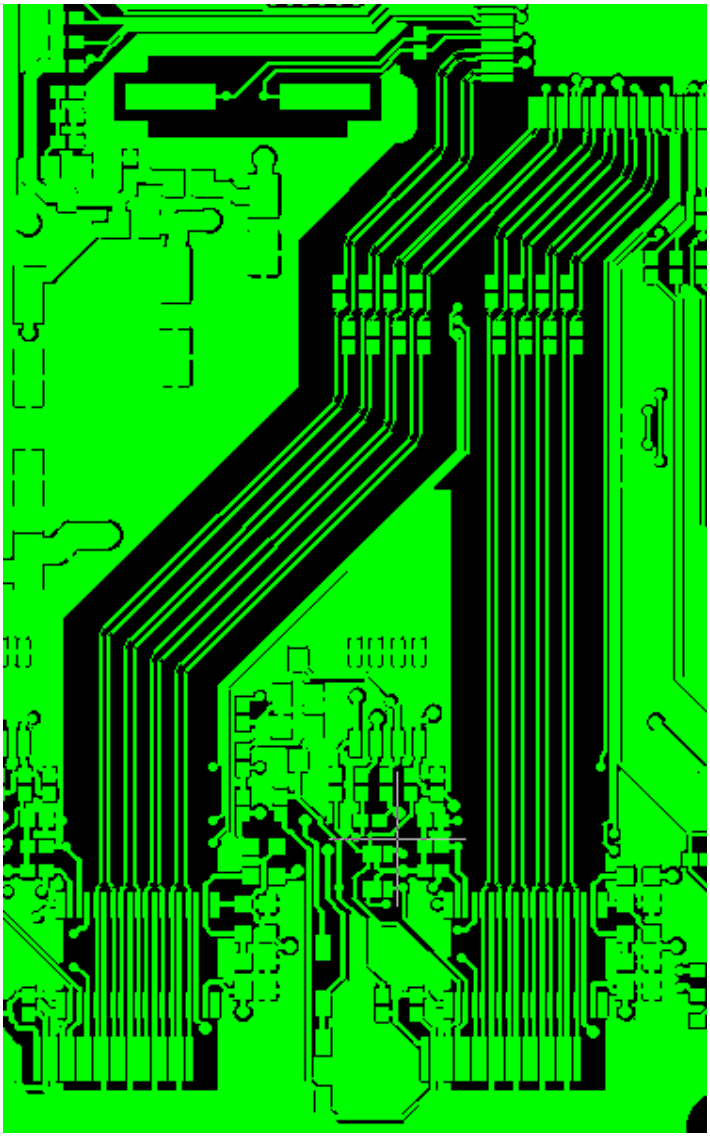


Figure 6.26. HDMI interface layout

6.4.3. Front End

High frequency layout design is the part which is challenging, front end is formed by tuner and IF demodulator. In design hybrid tuner is used for supporting digital and analog reception. Analog IF demodulator and digital COFDM demodulator are used for analog and digital reception. RF frequency is down converted to IF by tuner, the hybrid tuner used in design has differential filtered IF output signal for digital COFDM demodulator and single ended not filtered IF for analog IF demodulator. The not filtered analog IF is filtered by SAW filters before analog demodulation. Tuner IF

output signal is less sensitive to noise because of low output impedance of the tuner, but after filtered by SAW filters the IF signal is very weak and sensitive to noise because of high output impedance of SAW filter. For layout between SAW filters and IF demodulator great care is dedicated. The trace is routed as short as possible. These lines are surrounded by ground for shielding which provides to reduce effects of noise. Fourth layer is used for this line traces and third layer below fourth layer is cut and second layer is used as shield layer and reference layer for these lines. The reason of why third layer is not used as the reference layer is because third layer is near by to fourth layer and the high frequency noise on this layer can simply couple the fourth layer but by using second layer as the reference layer the capacitance between trace and reference layer is reduced which reduce high frequency noise coupling from reference layer. The ground layer between tuner and SAW filters are cut to prevent noise coupling originated at tuner ground. In Figure 6.27 layout of the IF lines after SAW filters are shown, as signal layer fourth layer used and the part of third layer under IF signal path is cut. The bottom side of the IF traces are cut at third layer and all layers between tuner and SAW filters are cut for ground isolation.

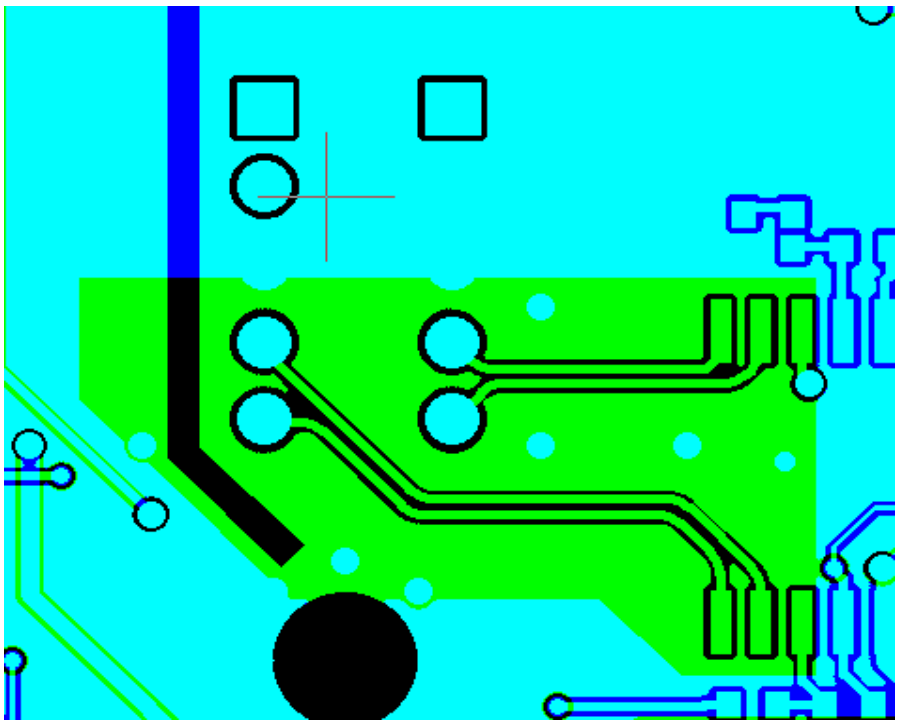


Figure 6.27. Layout of analog IF traces between SAW filters and IF demodulator

In design both hybrid type tuners and analog only tuners are considered, analog IF output in hybrid tuner case is the pin eight (fourth from top) and for the analog only case pin eleven (at top), both can be routed to the SAW filters via jumpers as shown in Figure 6.28. The trace length is as short as possible and shielded by ground layer for improving immunity. Analog IF signal is asymmetric single ended signal.

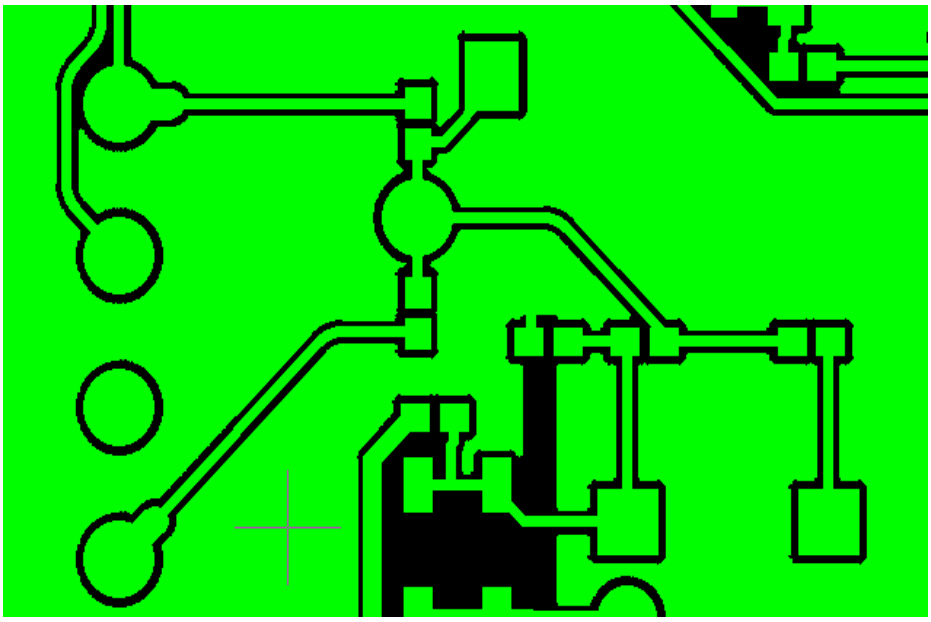


Figure 6.28. Layout of the trace between tuner and SAW filter

Tuner has differential filtered and amplified IF output for digital IF, SAW filter and IF amplifier is inside tuner. Because the tuner digital IF output is amplified signal, it is less sensitive to noise, layout considerations are easier. In Figure 6.29 layout of the part between tuner and COFDM demodulator is shown, the trace length and path also routed considering immunity of the line to noise.

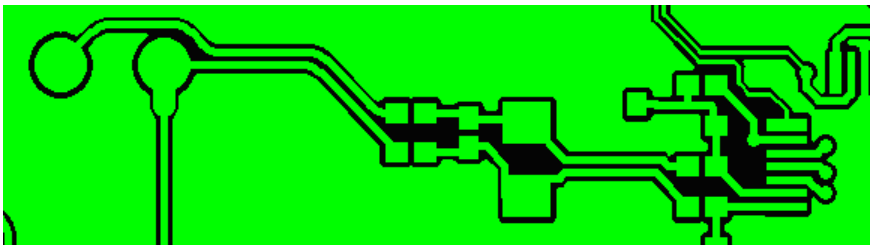


Figure 6.29. Layout between tuner and COFDM demodulator

6.4.4. MPEG Decoder

EMMA2LL is the unified chip including MPEG decoder and CPU which is responsible of digital reception. The interfaces of MPEG decoder is memory interfaces with flash memory and DDR memory, CI interface and digital audio and video interface with video and audio processing chip.

6.4.4.1. Memory Interface

Flash memory and DDR memory are the memory interfaces of the MPEG decoder. System code is stored and operated on flash memory. DDR memory is used for dynamic memory requirement of the MPEG decoder.

In Figure 6.30 the layout of the connectivity between MPEG decoder and flash memory is shown. Because of the operating frequency of these lines is below 50 MHz layout considerations are not difficult, lines are just connected simply without any considerations.

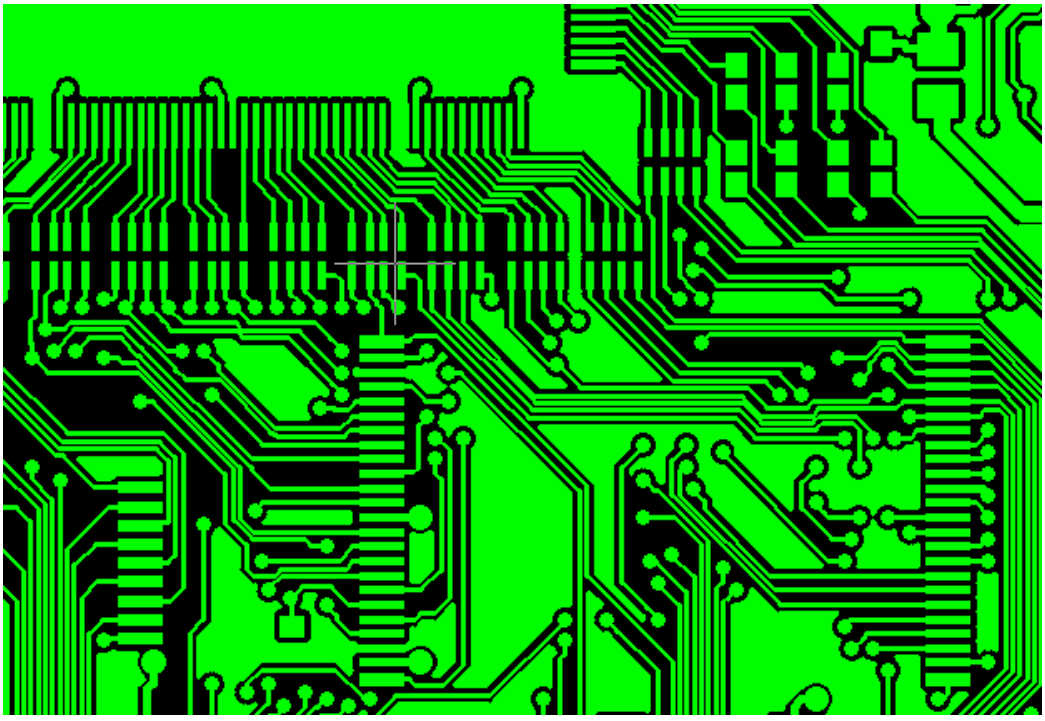


Figure 6.30. Layout of flash and MPEG decoder interface

DDR memory interface operating frequency is 133 MHz and up to 266Mbit/s data transfer over one data line is possible. Because of this high data bandwidth requirement no via used on these line traces and for signal integrity line length and impedance are matched. In Figure 6.31 DDR interface layout is shown. As seen in Figure 6.31 line lengths are carefully matched for signal integrity which provides to increase data valid time. As also seen in Figure 6.31 the ground is surrounding the data lines, this provides to reduce electromagnetic radiation of these lines because the radiation is terminated at ground. Second layer is totally reference layer which provides to realize impedance matched lines and reduce electromagnetic radiation of DDR lines.

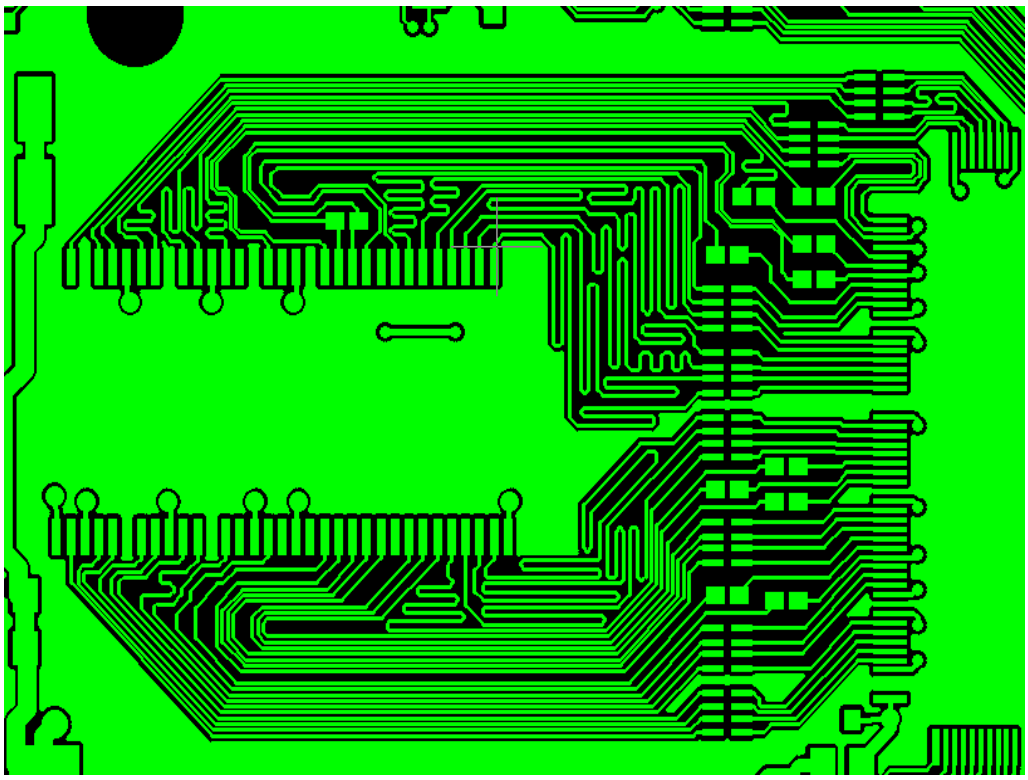


Figure 6.31. MPEG decoder and DDR interface

6.4.4.2. Common Interface

Common Interface module is an compulsory for integrated digital TVs, in case of decoder card is available coded TS (transport stream) is directed to decoder card by buffers and switches and decoded TS is directed from decoder module to MPEG decoder, otherwise TS is directed to MPEG decoder. COFDM demodulator converts

COFDM coded IF signal to TS signal which includes digital audio and video stream. TS signal is low frequency (2-3 MHz) digital signal so layout of this signal does not have considerations. In Figure 6.32 layout of the common interface is shown including interface between COFDM demodulator, CI card connector, MPEG decoder and TS buffers.

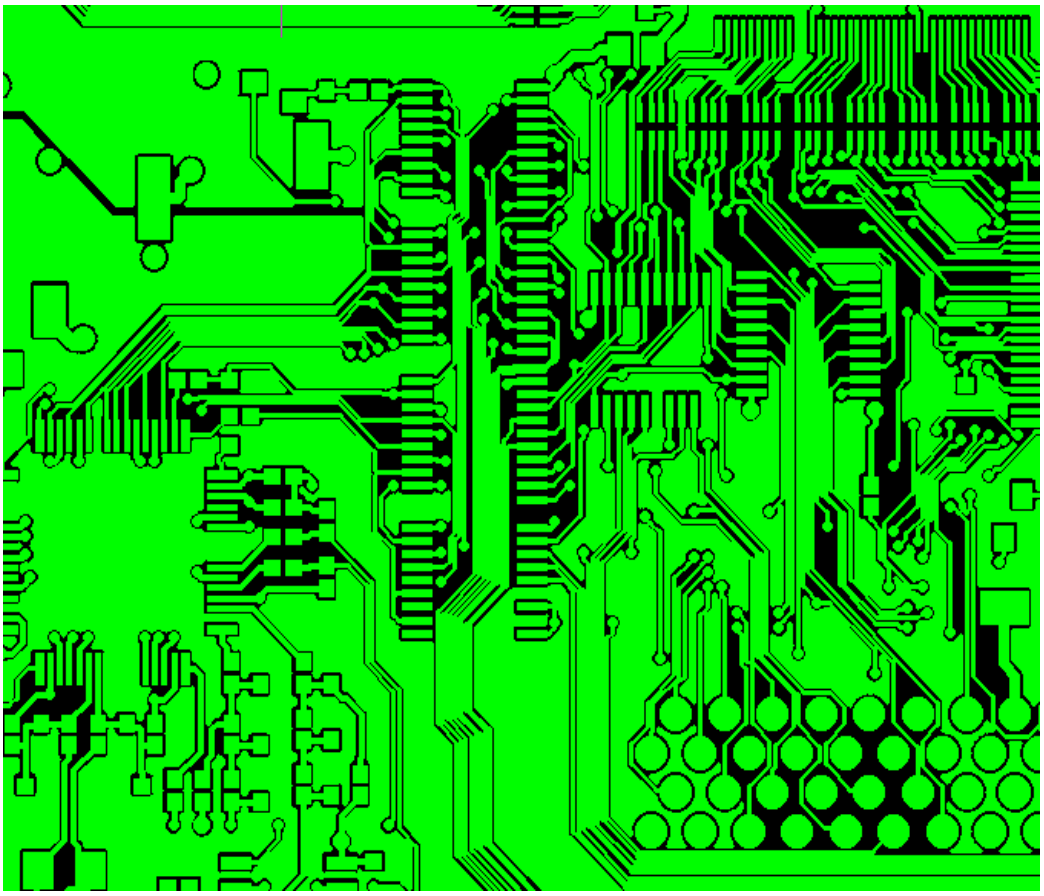


Figure 6.32. CI interface layout

6.4.4.3. Digital Audio & Video Interface

Digital audio and video output of MPEG decoder is used for the interface between MPEG decoder and audio & video processing chip. ITU 656 is the digital video interface which is formed by eight data lines and one clock line which is operating at 27 MHz. SPDIF is the digital audio interface which is used for the interface between MPEG decoder and processing chip. ITU 656 and SPDIF digital interfaces are

used for the audio and video connectivity. ITU and SPDIF lines have TTL level logic and have great radiation because of the amplitude and the frequency of the signal. Fourth layer which is the bottom layer is used for the ITU 656 lines the layers on these lines are ground layers which acts as shield and terminates the radiation of the signal.

6.4.5. Scaler & De-interlacer

Scaler and De-interlacer is the basic processing unit for flat panel displays, with the technological improvement integration of separate block became feasible and in design addition to scaler and de-interlacer video decoder, audio processor, microcontroller and HDMI receiver are integrated into same die. The single chip formed by the integration of all TV units is the major part of the processing board. DDR and flash memories are outside and the connection between DDR memory is a hard challenge considering EMI and data BW issues. Strict layout considerations should be kept for DDR layout. DDR layout is also mentioned in part Digital Signals Memory interface (6.4.2.1.) but to mention again the items which should be considered in DDR layout design are as following, impedance matching, line length matching and avoiding to use via which disturbs signal continuity, reference plane should terminate and surround the DDR lines for reducing electromagnetic radiation, these items improves signal integrity and reduce electromagnetic radiation. The placement of DDR memory which is used by scaler & de-interlacer is given in Figure 6.33.

Because of integration of sub systems into single die power dissipation and related to this item heat is a major item which should be considered carefully during layout stage. Heat sink is the solution for heat problem. In flat panel processing board metal heat sinks are not used because of space and cost considerations, the technique for heat sink implementation on processing board is to use PCB surface and copper as heat sink. TJA parameter defines thermal resistance junction to ambient, depending to case type junction to case differs but case to ambient depends to heat sink area. TJA can be given as TJA = TJC + TCA, TJA value for defined PCB size is given in datasheet or application document of the chip set. For the scaler and de-interlacer chip 2 cm2 at bottom and 1cm2 area at top is reserved for heat sink area.

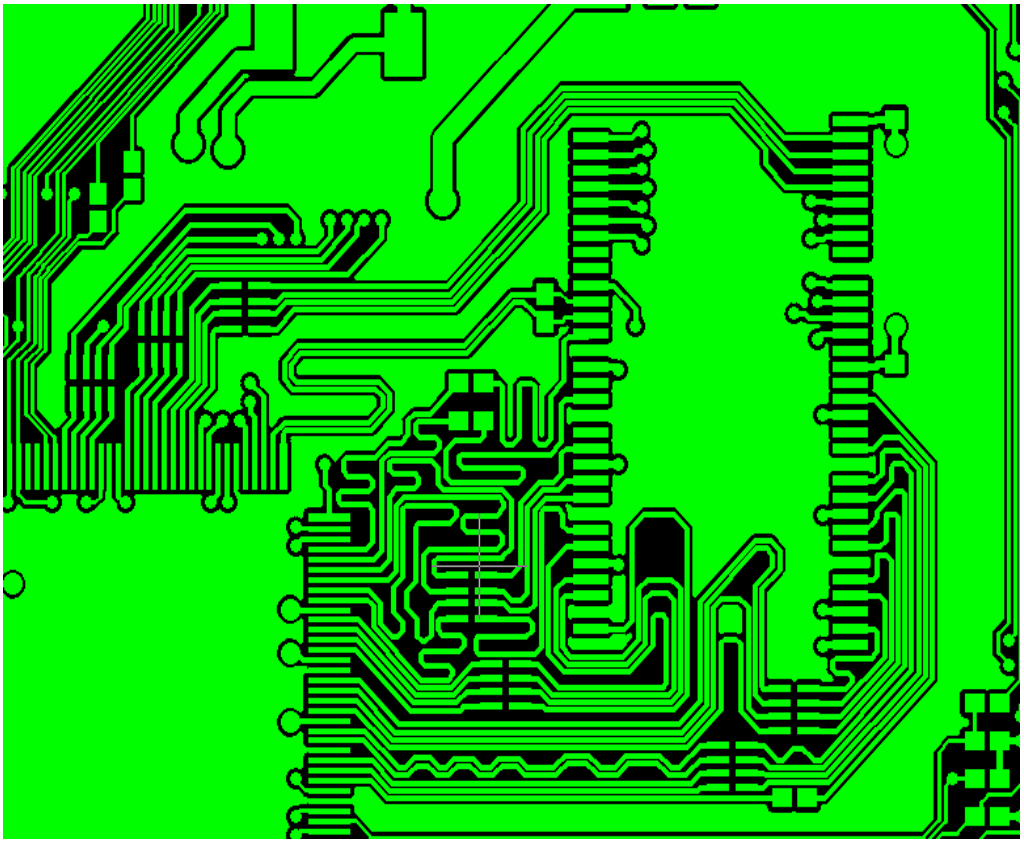


Figure 6.33. Layout of connectivity between DDR memory and scaler&de-interlacer

LVDS and HDMI digital interfaces are the most important parts in layout design which are mentioned in parts 6.4.2.2 and 6.4.2.3 respectively. LVDS lines are impedance and line length matched, pairs are totally length matched. Line length matching for differential pair reduces electromagnetic radiation; because the phase difference is 180 degree between differential pairs, radiation of pair lines cancel each other. HDMI TMDS lines are impedance matched, 100 ohms differential impedance is mandatory for HDMI compliance test and which also improves signal integrity.

The placement of the scaler and de-interlacer chip is given in Figure 6.34. The video and audio input termination resistors and coupling capacitors are placed as near as possible to chip to provide better SNR and improve signal quality. Termination resistors and coupling capacitors can be seen at right bottom side of the Figure 6.34.

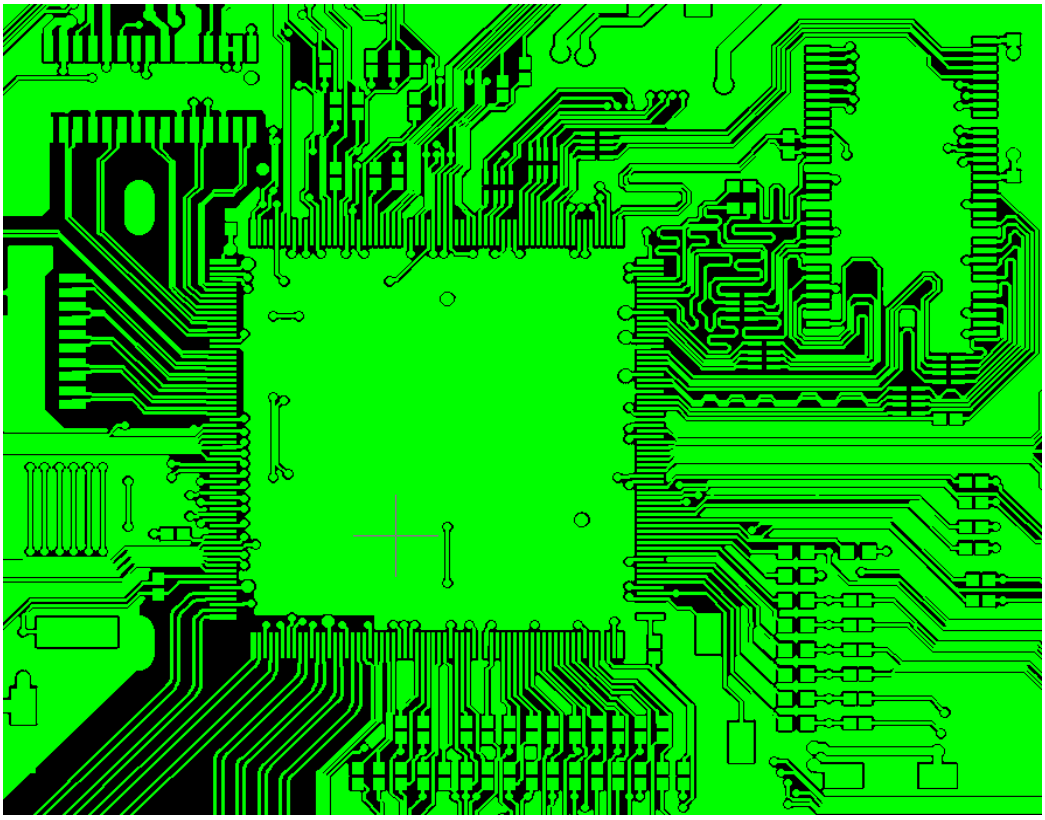


Figure 6.34. Layout of scaler and de-interlacer

6.4.6. Audio Amplifier

Audio amplifier layout is the important part because layout has great effect on audio performance. Layout related items can be divided into three groups, performance considerations, EMC considerations and thermal considerations.

Amplifier has two parts input signal part and output signal part. Input signal is the weak with high impedance signal which is sensitive to noise, cross talk and other external effects. Input signal line is isolated and shielded to prevent from noise sources. At the input stage of amplifier first item is the supply voltage which is supplying power to input stage circuitries should be clean, to provide clean supply for analog circuitries at input stage RC filtering is used. As shown in Figure 6.35 24V_VPA is the supply which is RC filtered for analog circuitries at input stage of the audio amplifier.

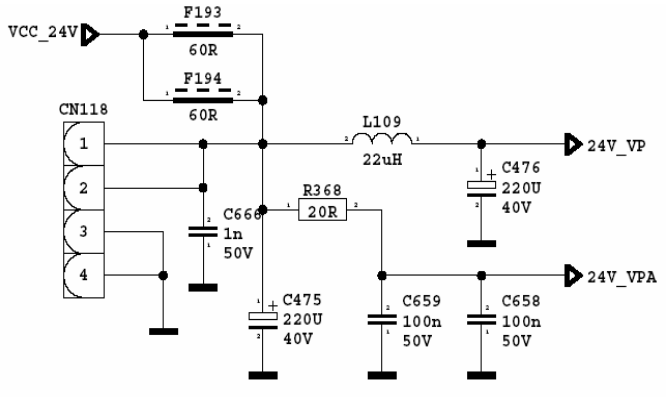


Figure 6.35. Power supply filtering

Component placement at the input stage is an important parameter in manner of performance. The coupling capacitors and terminating resistors placement should be near as possible to the amplifier, the reason of this requirement is the amplifier input impedance is 100k which is quite high value which increase sensitivity to noise, if the line between coupling capacitor and input of amplifier is long SNR will decrease. In Figure 6.36 the input stage of the amplifier is shown. (Philips 2006c)

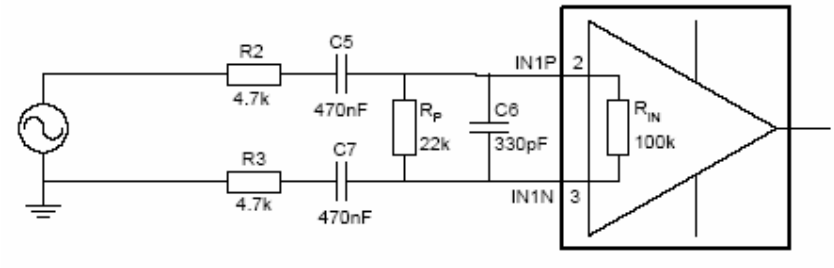


Figure 6.36. Input stage of class-D audio amplifier

Layout placement of the Class-D audio amplifier is given in Figure 6.37, as shown in Figure 6.37 placement of the components at input stage is near to the IC.

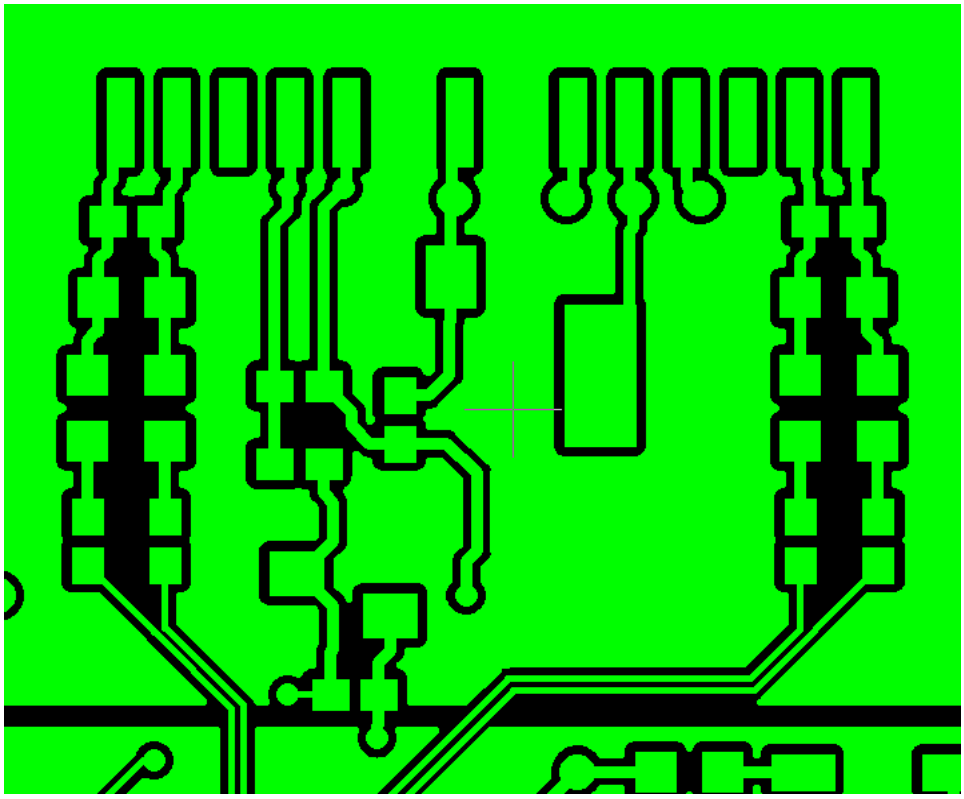


Figure 6.37. Input stage Layout of the Amplifier

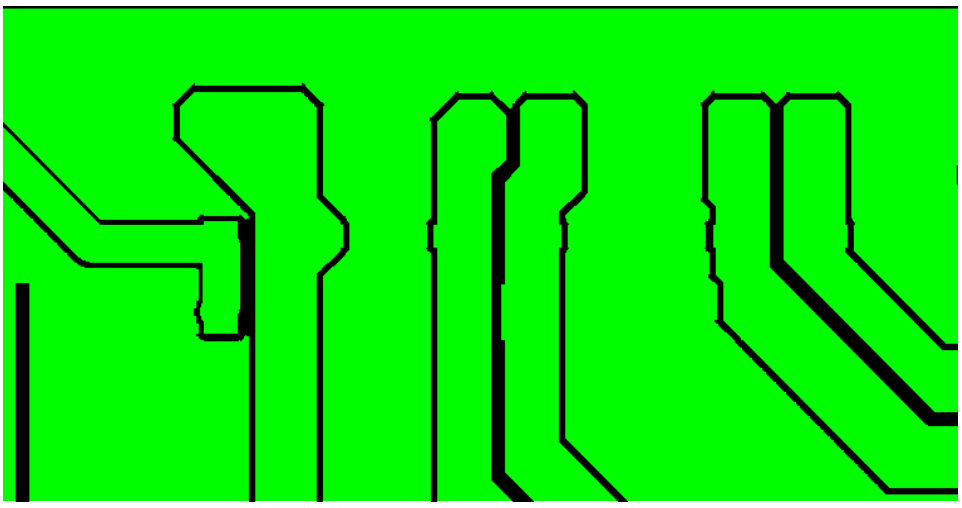


Figure 6.38. Audio amplifier power and speaker connector placement

Output stage and power connections layout also should be designed considering performance. Supply connector and audio output connectors should be near to each other as shown in implementation layout in Figure 6.38. Left side connection is the ground and power connector, the right side two connections are the right and left channel speaker outputs. As seen in Figure 6.38 power, ground and speaker connectors are closed to each other, the reason of this architecture is to provide shortest path for the current from supply to speakers and ground.

Due to the operation of D type audio amplifier EMC is a critical design challenge. Output signal at amplifier output is pulse width modulated signals changing between supply and ground level considering amplitude of the supply voltages as 24V, the radiation will be quite high. In class-D type architecture amplifier output signal is low pass filtered to provide the base band audio signal. The placement of the low pass filter effects radiation because if low pass filter is placed closed to IC high frequency components will be filtered and the path will be short, as the path length decrease the frequencies can radiate will be the higher frequencies of the spectrum. The output stage placement is given in Figure 6.39, as seen in Figure 6.39 placement of the low pass filter components are closed to amplifier. The path widths are defined as considering current level passing though the path. Supply voltage is 24V and the speaker impedance is 8 ohm, the maximum current is 3A for each path. The resistance of the path can be calculated from the equation 6.4 below. Resistivity of the copper is 1.72 E-8 (ohm/m) (WEB_11 2007). In design path length is around 4 cm and trace width is 2mm, the resistance of the trace is 0.01127 ohms using the equation, which is low enough.

$$R = \frac{\ell \rho}{\mathrm{A}} \tag{6.4}$$

Supply filtering and high frequency supply decoupling capacitors are placed near to amplifier to provide current requirement from shortest way to reduce radiation.

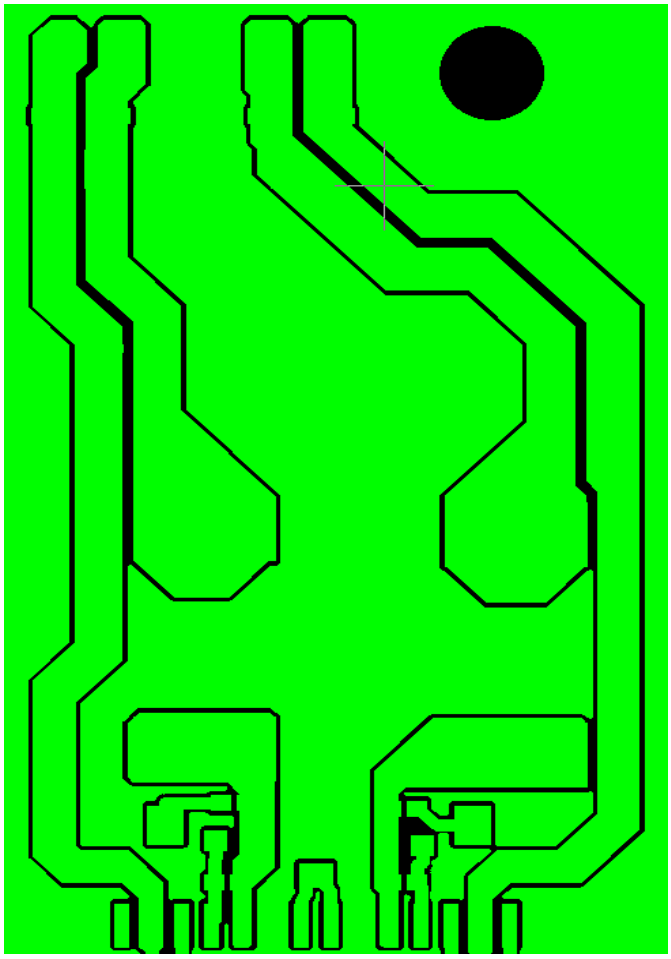
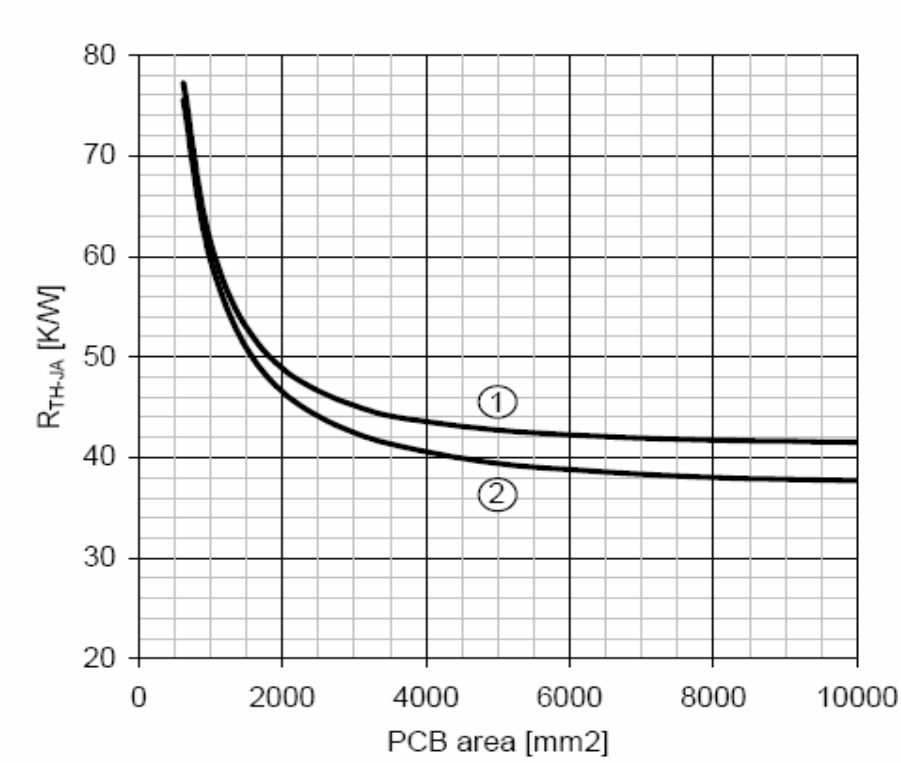


Figure 6.39. Audio amplifier speaker output trace layout

Thermal requirements of class-D type amplifiers are easy to realize because of high efficiency of operation, the power dissipated on amplifier is low. The amplifier used in design use ground pins at the corners as heat sink connection and PCB surface is used as heat sink area to reduce the thermal resistance from junction to ambient. In Figure 6.40 thermal resistance junction to ambient (TH_JA) is given due to the PCB size. In design four layers PCB is used so 2nd curve is our concern in design. The design specification of output power is max 2x10 W, the efficiency of the amplifier is around 90% at 10W output power. In worst case power dissipation on amplifier is 2W. Considering ambient temperature is 60 C in worst case and the fact of allowable maximum junction temperature is 140C, TJA should be 40 K/W. 2400 mm2 second layer ground plane and 600 mm2 soldered surface heat sink are used to achieve thermal resistance requirement in worst case.



1) FR2 PCB, single copper plane at device side (35 μm copper 100% coverage)
2) FR4 PCB, a copper plane at top and bottom side (35 μm copper 100% coverage)

Figure 6.40. Audio amplifier thermal resistance dependent to Copper PCB Area (Source: Philips 2006a)

6.4.7. Power

Power layout design can be separated into two groups, layout design for switching regulators and layout design for linear regulators. The design challenge in switching regulators is originated from operation architecture. Design challenge for the linear is originated from the power dissipation on regulator.

Switching regulators are layout sensitive devices and proper layout should be realized for operation and performance. The layout considerations for switching regulators are the current paths should be wide as much as possible, switching pin of the regulator should be directly, shortly and widely connected to the filtering passive element to reduce radiation noise and improve filtering. The layout implementation of U138 is given in Figure 6.41.

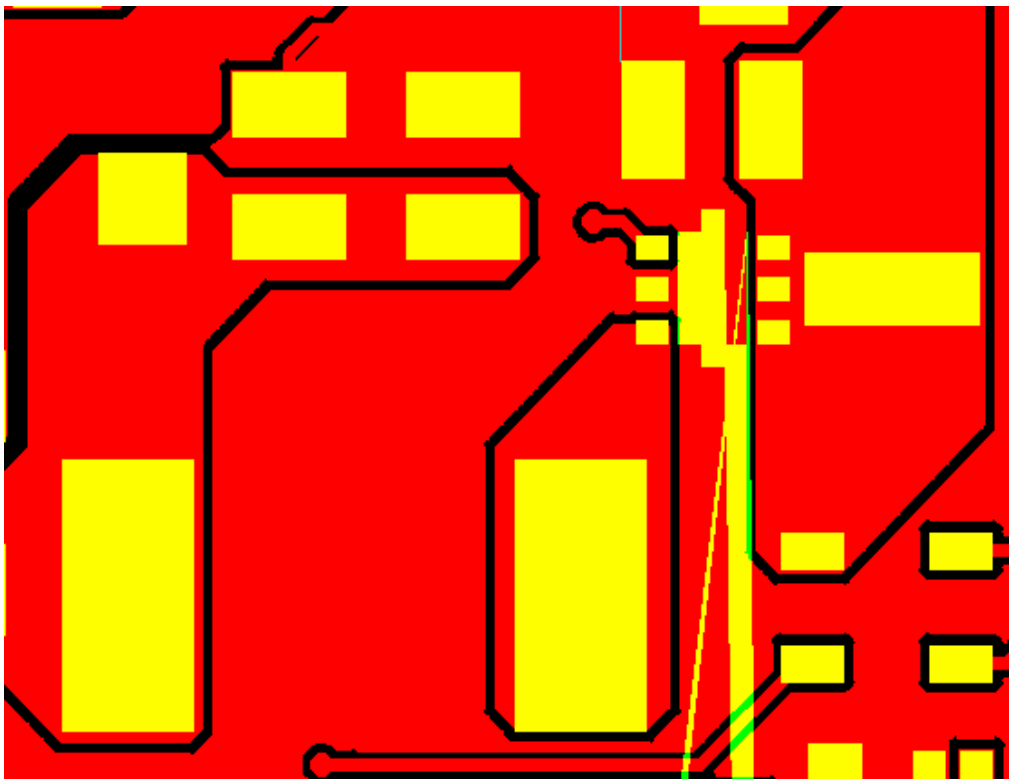


Figure 6.41. Switching regulator layout

Linear regulators are not efficient devices, but because of stable output voltage and less cost they are preferred and used. Power dissipated on linear regulator can be calculated directly by voltage drop multiplied with the output current. For the applications with low current and low drop out voltage linear regulators easily used, but in case of high power dissipation layout of the linear regulators are important because of power dissipation. In design four linear regulators are used, power dissipations are as following 0.8W, 0.8W, 0.85W and 0.2W, to provide operation at 1W heat sink area on PCB surface designed. In case of 1.5 cm2 soldered heat sink surface at top and bottom side thermal resistance ambient to junction is 70C/W (National 2006). Worst case ambient temperature is 60 C and under these conditions the junction temperature is 116 C which is below junction breakdown temperature of the device (125 C). For the regulators dissipating 0.8W 2cm2 soldered PCB surface at top and bottom side is dedicated, and for the 0.2W dissipated power 1cm2 top side soldered surface is dedicated.

CHAPTER 7

CONCLUSION

Flat panel technology and building blocks of flat panel display are investigated in thesis, details and processing structures of the building blocks are described. Hardware design stage of TV processing board is given in two stages, schematic and layout design. Design consideration and solutions for power, efficiency, cost, performance and EMI are defined both schematic and layout stages of the design. Flat panel TV processing board with the capability of driving screen sizes from 19" to 47" display is designed considering design considerations and target system specifications. Solutions for the design challenges and expected problems are defined in design stage. Addition to expected problems which are solved in first layout a second layout is needed for the unexpected problems observed in first layout, with second layout all problems are solved and design approved which is ready for mass production. In thesis two special solutions are defined, one is circuitry which can automatically detect sink device and automatically switch signal type, and the other is the pop sound circuitry which is developed to solve pop sound originated from audio processor. Building blocks and processing architectures of the flat panel displays are defined, schematic and layout design stages of processing board is described in advance and two special circuitries are designed for system performance and feature improvement.

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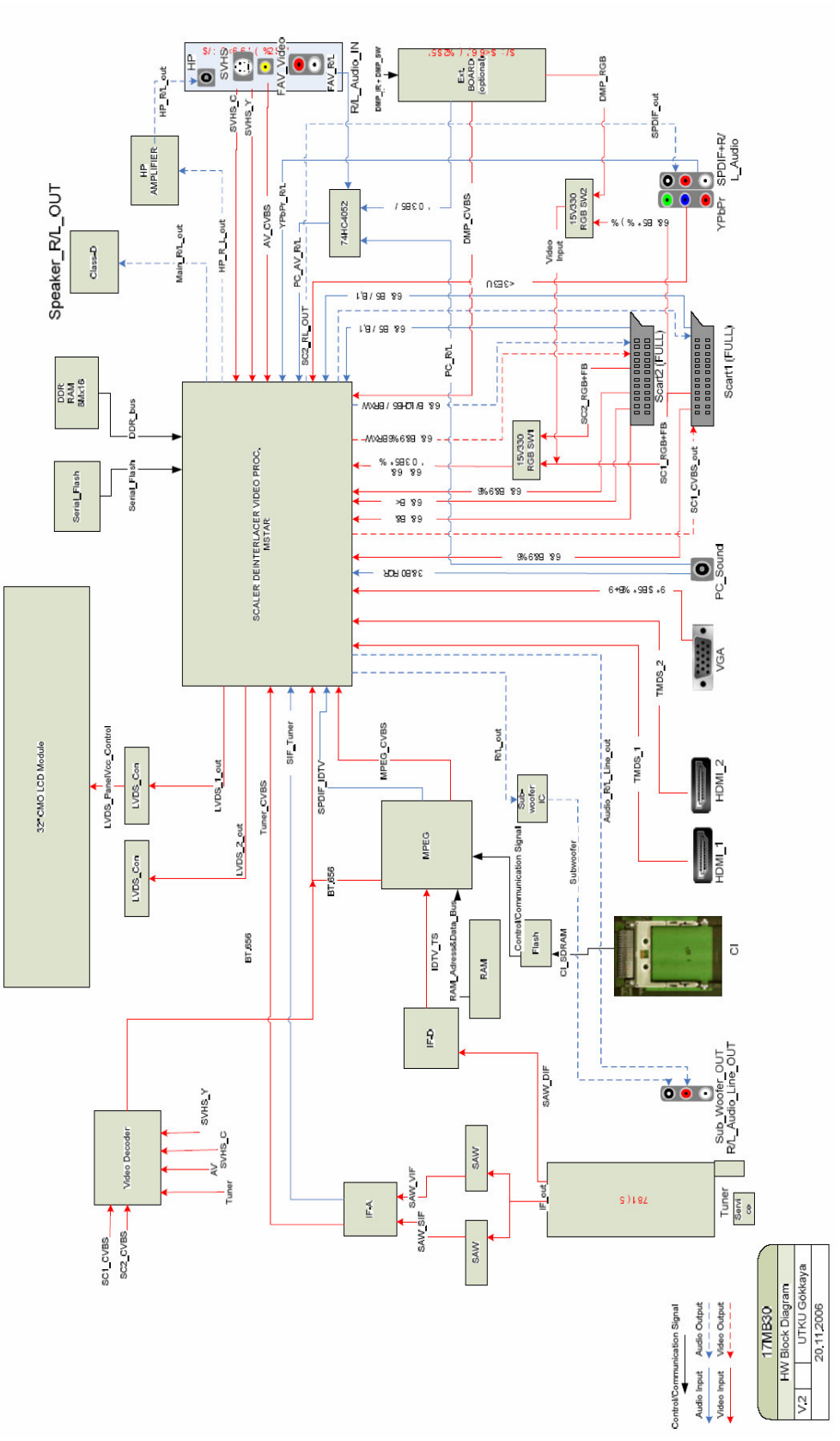
APPENDIX A

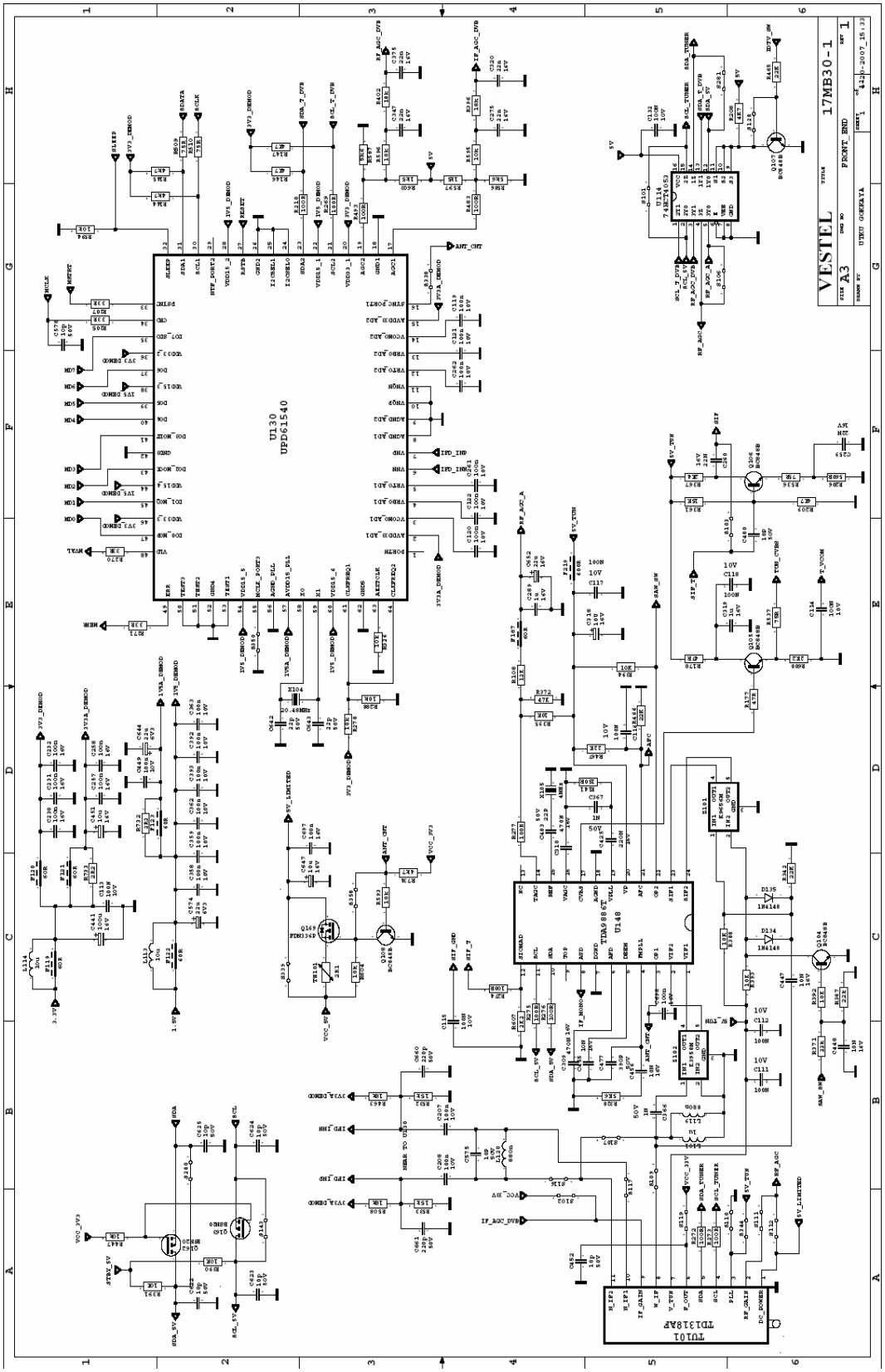
BLOCK DIAGRAM

17MB30 HW Block Diagram



APPENDIX B

SCHEMATIC DIAGRAM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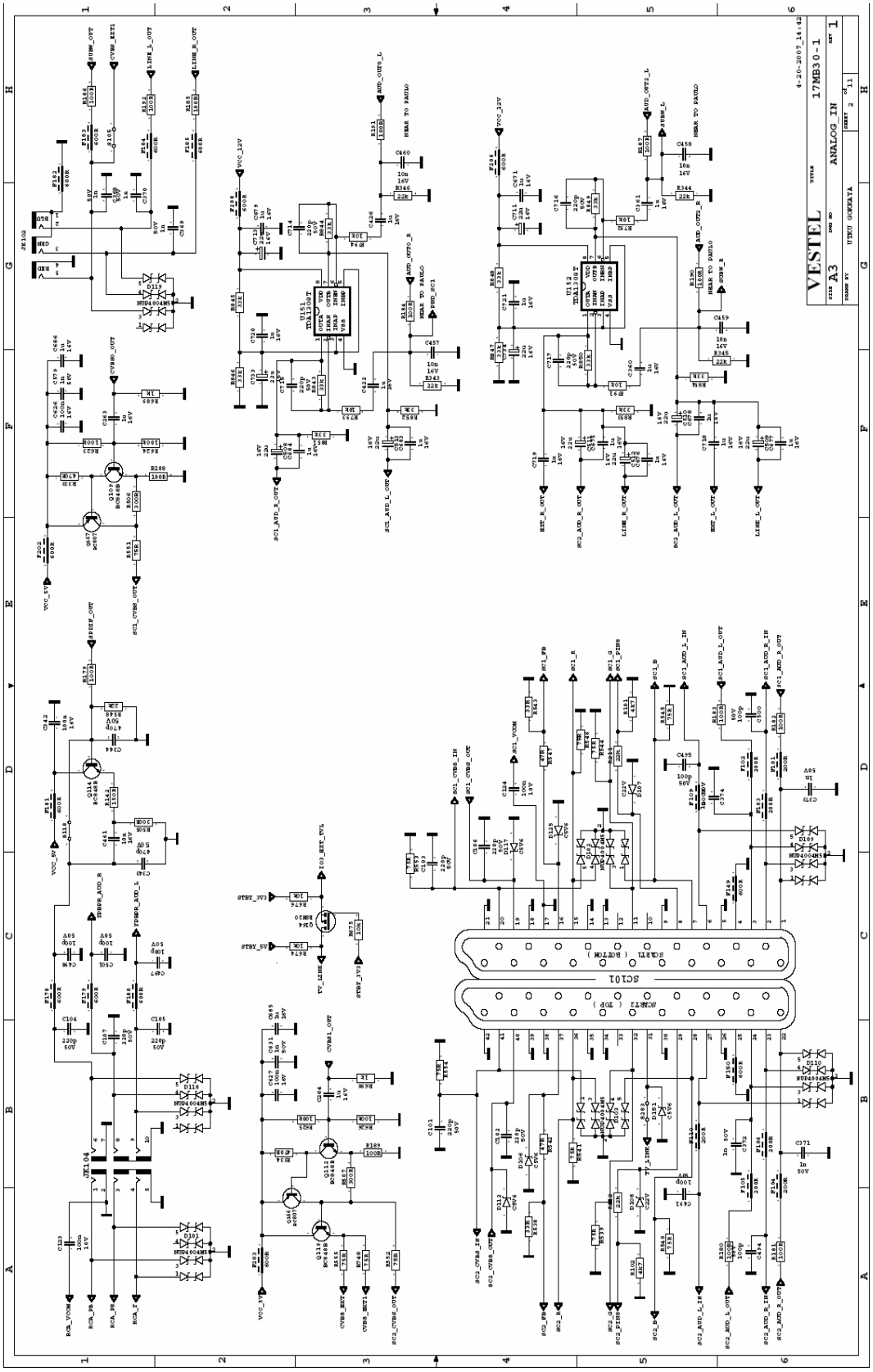
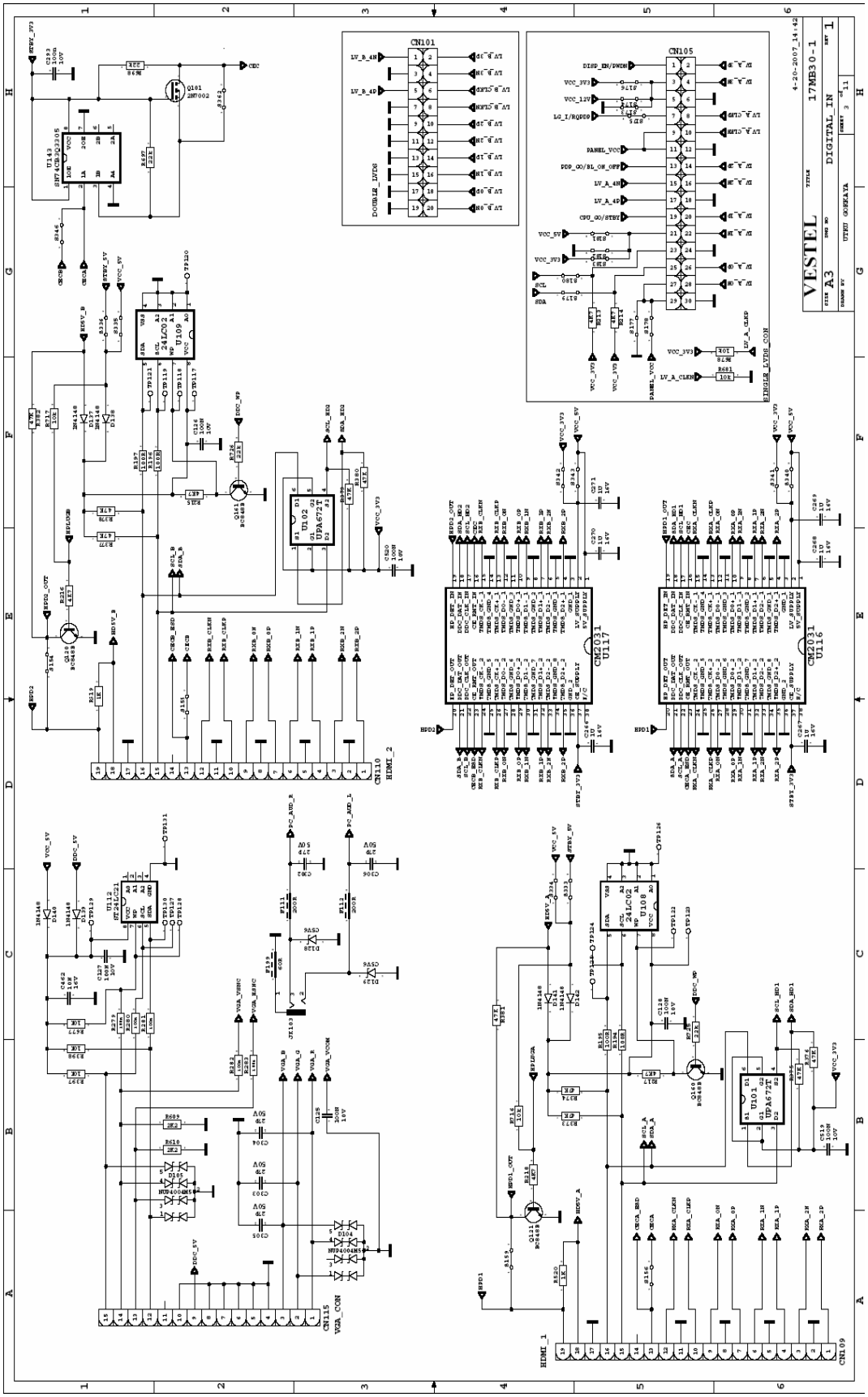
TD1318AF

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17MB30-1
DIGITAL IN
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DOUBLE_LVDS
CN105
LVDS_CON
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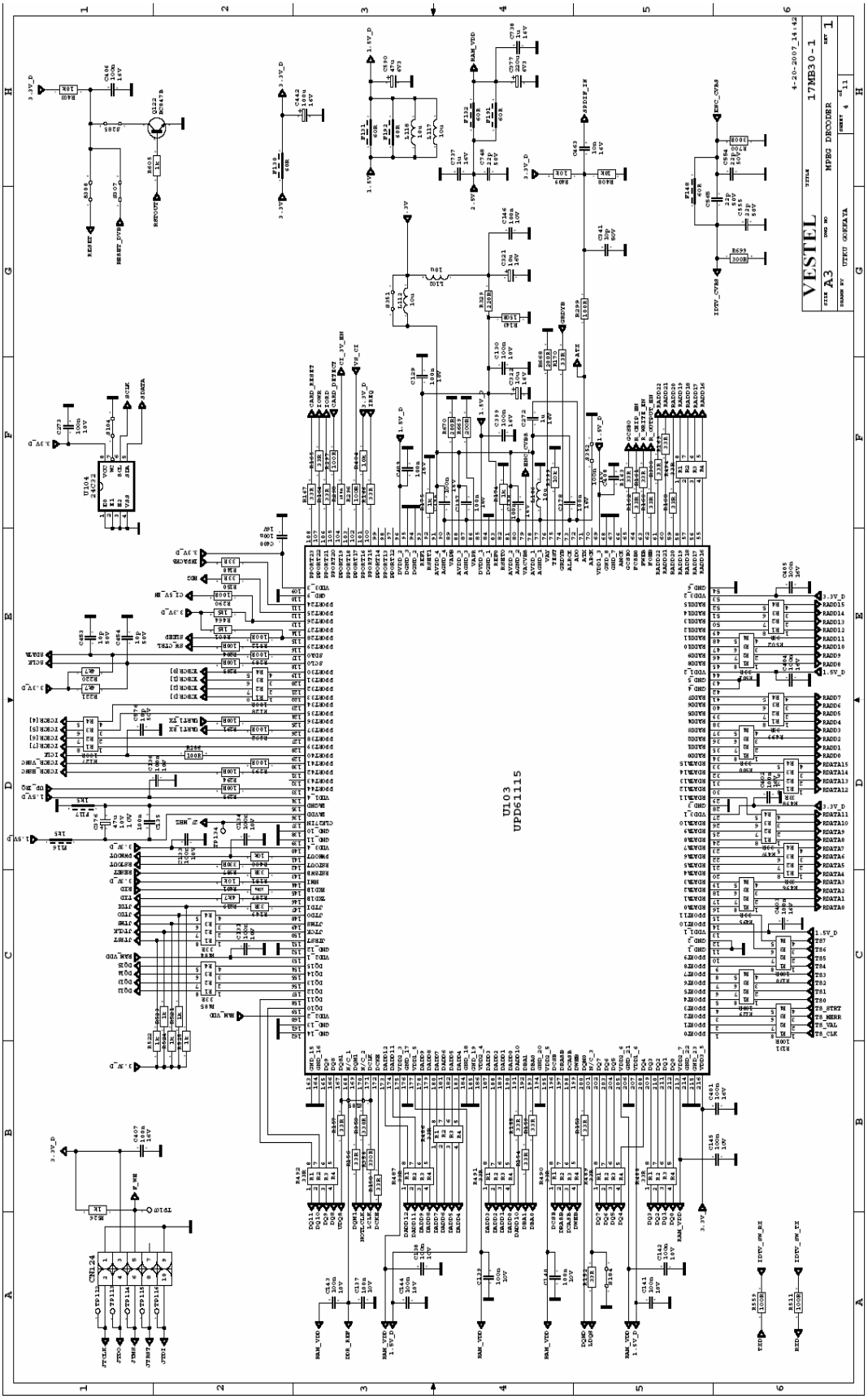
U117
U116
CM2031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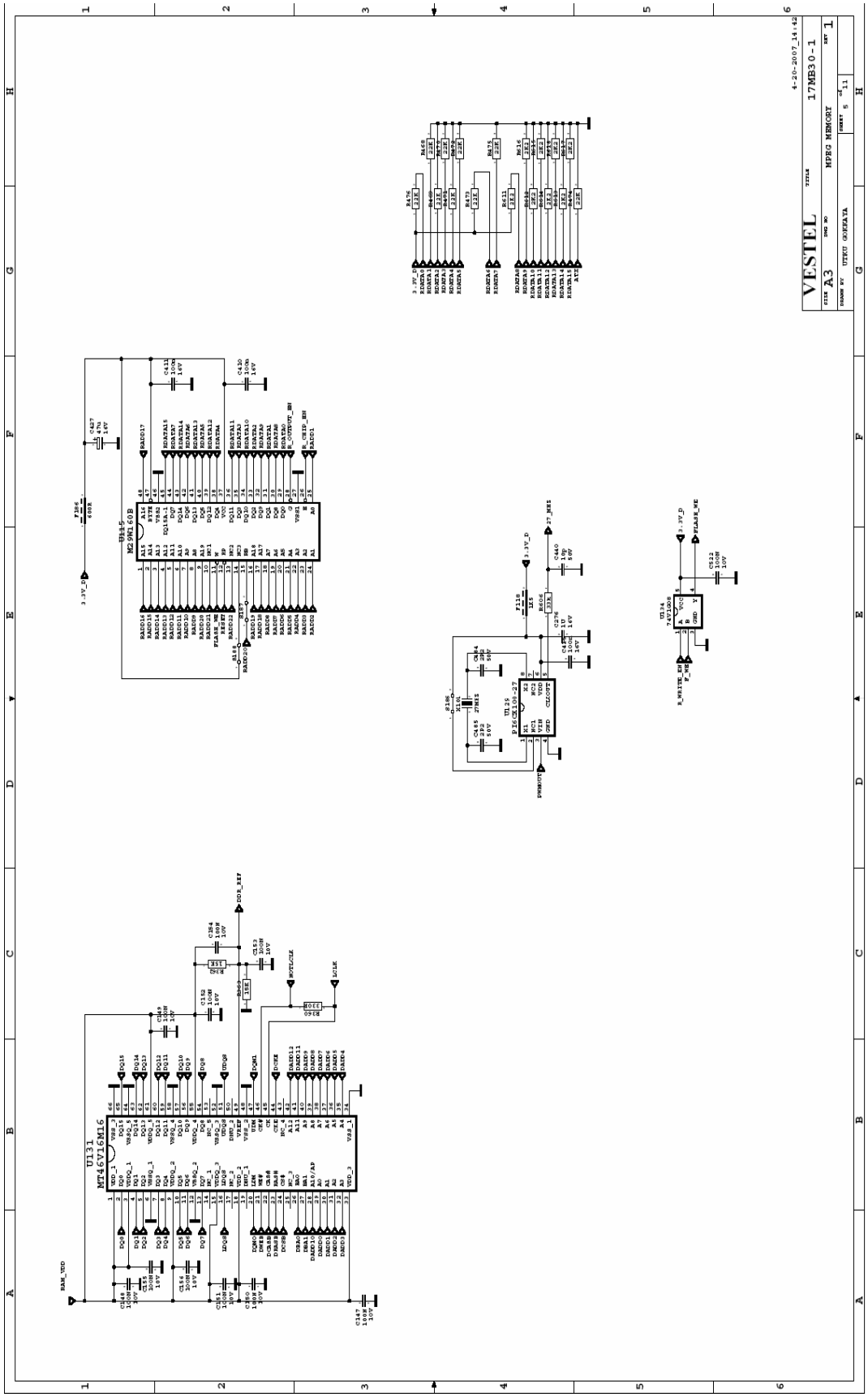

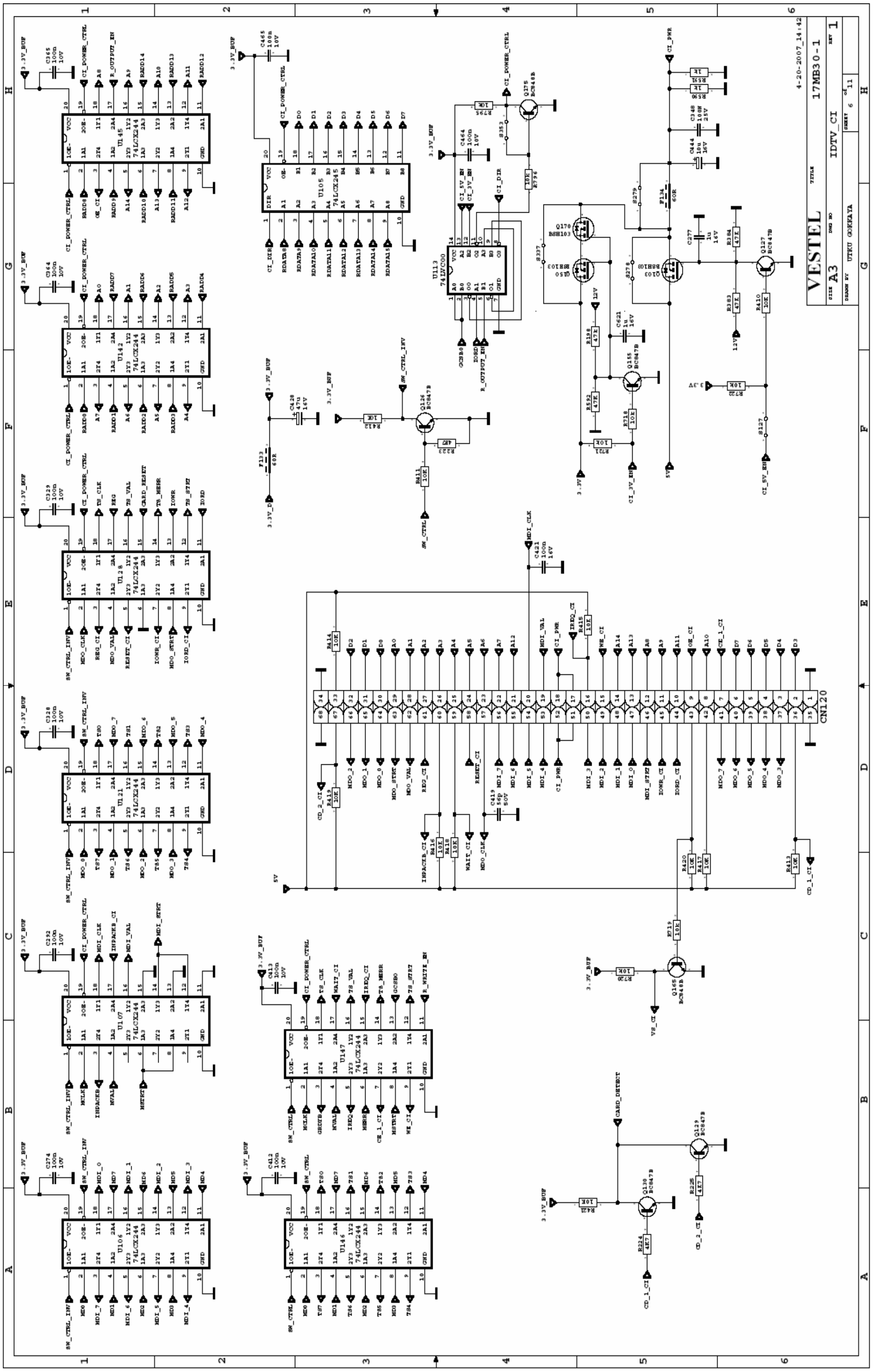
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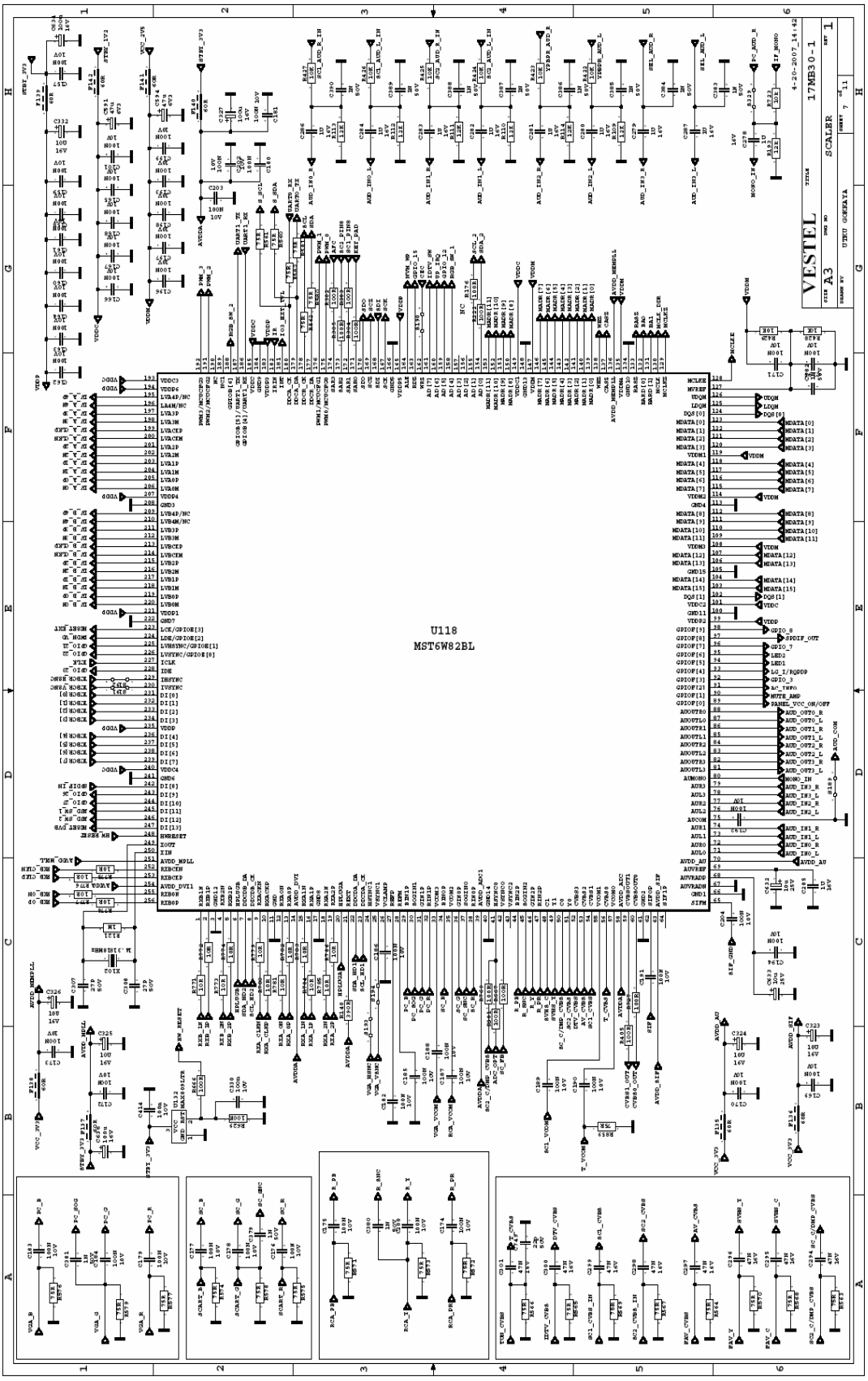
CN120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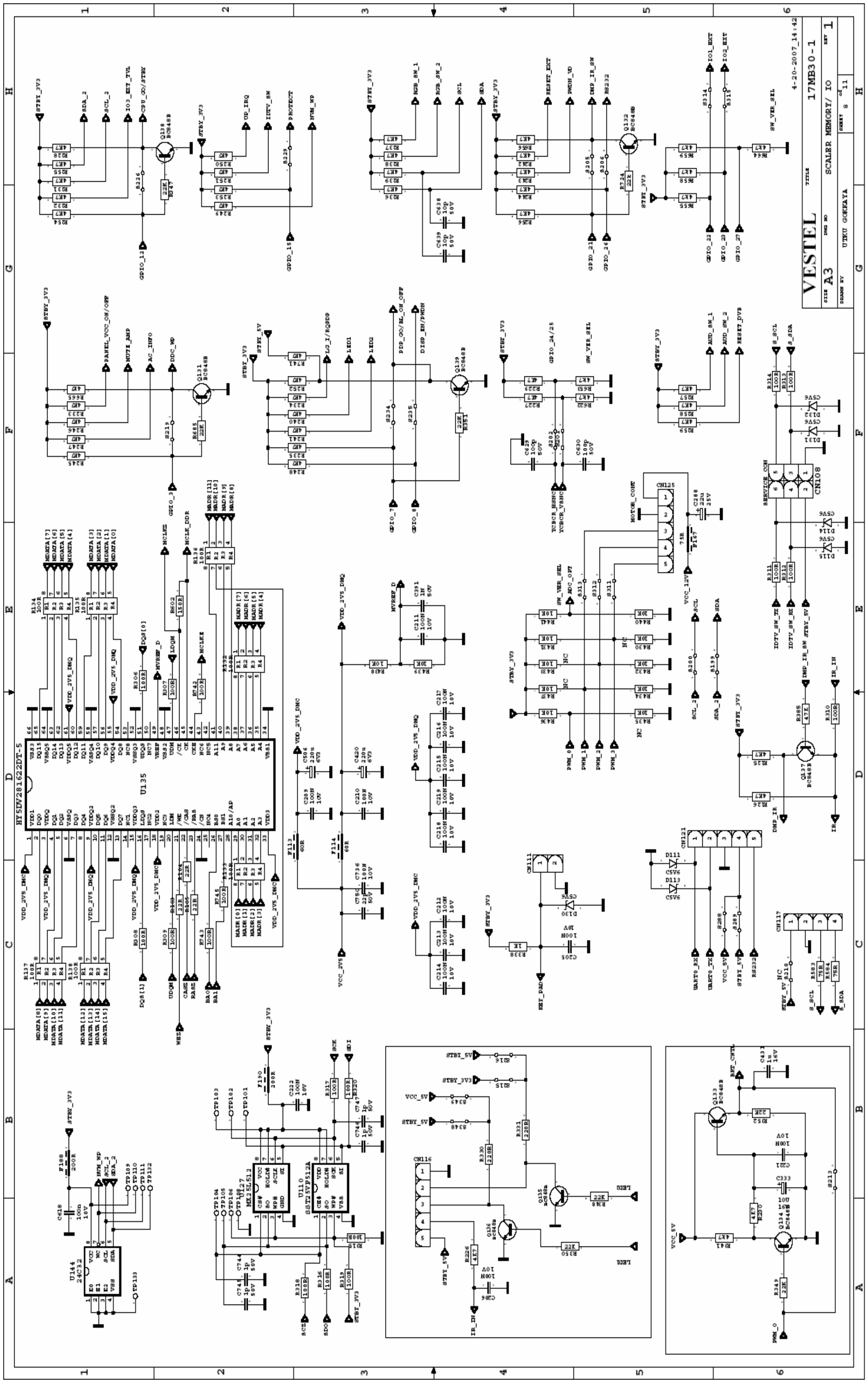
A3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U144
24C32
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U110
SST25VF512A
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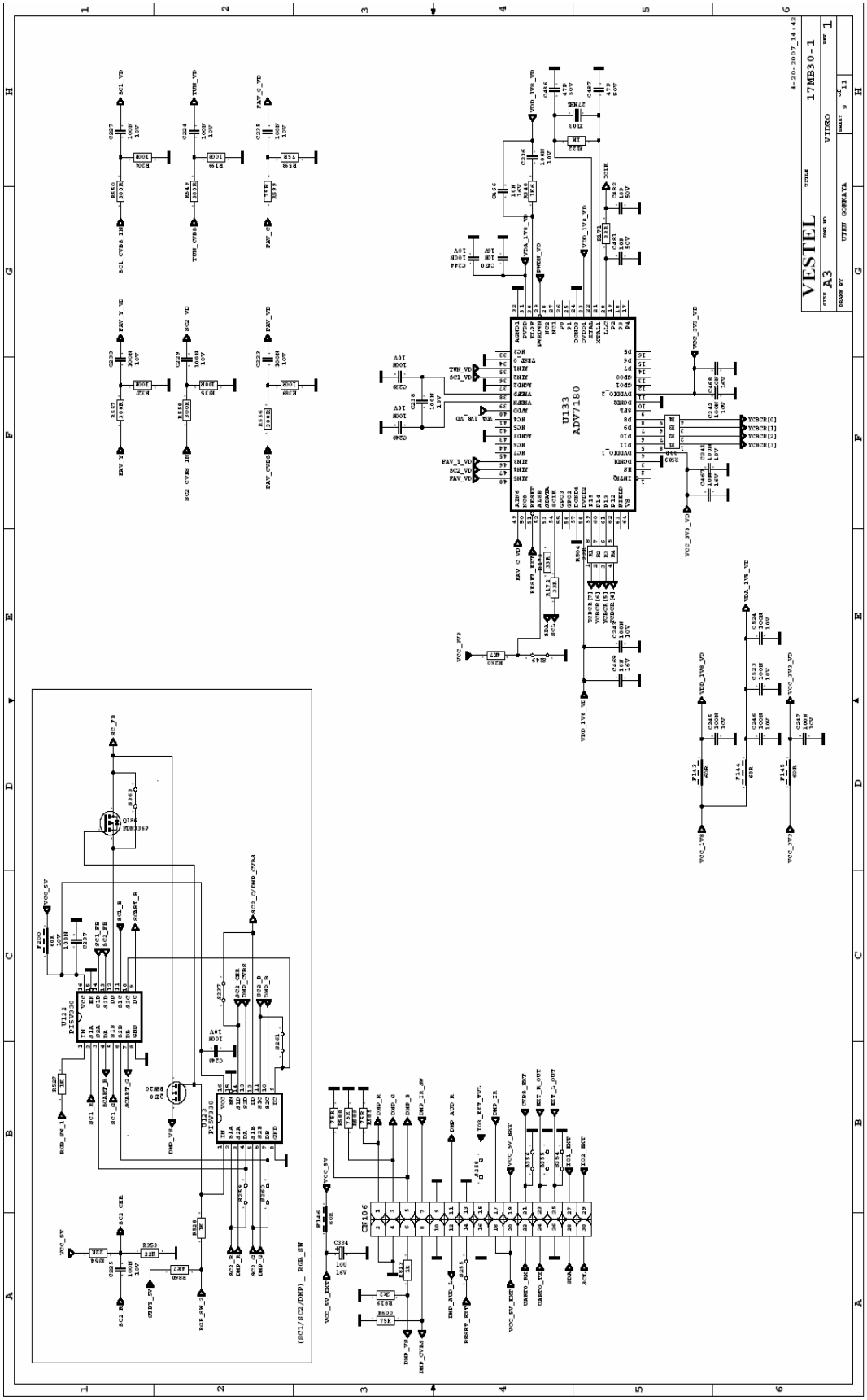
CN121
CN117
CN125
CN108
SERVICE_CON
MOTOR_CONT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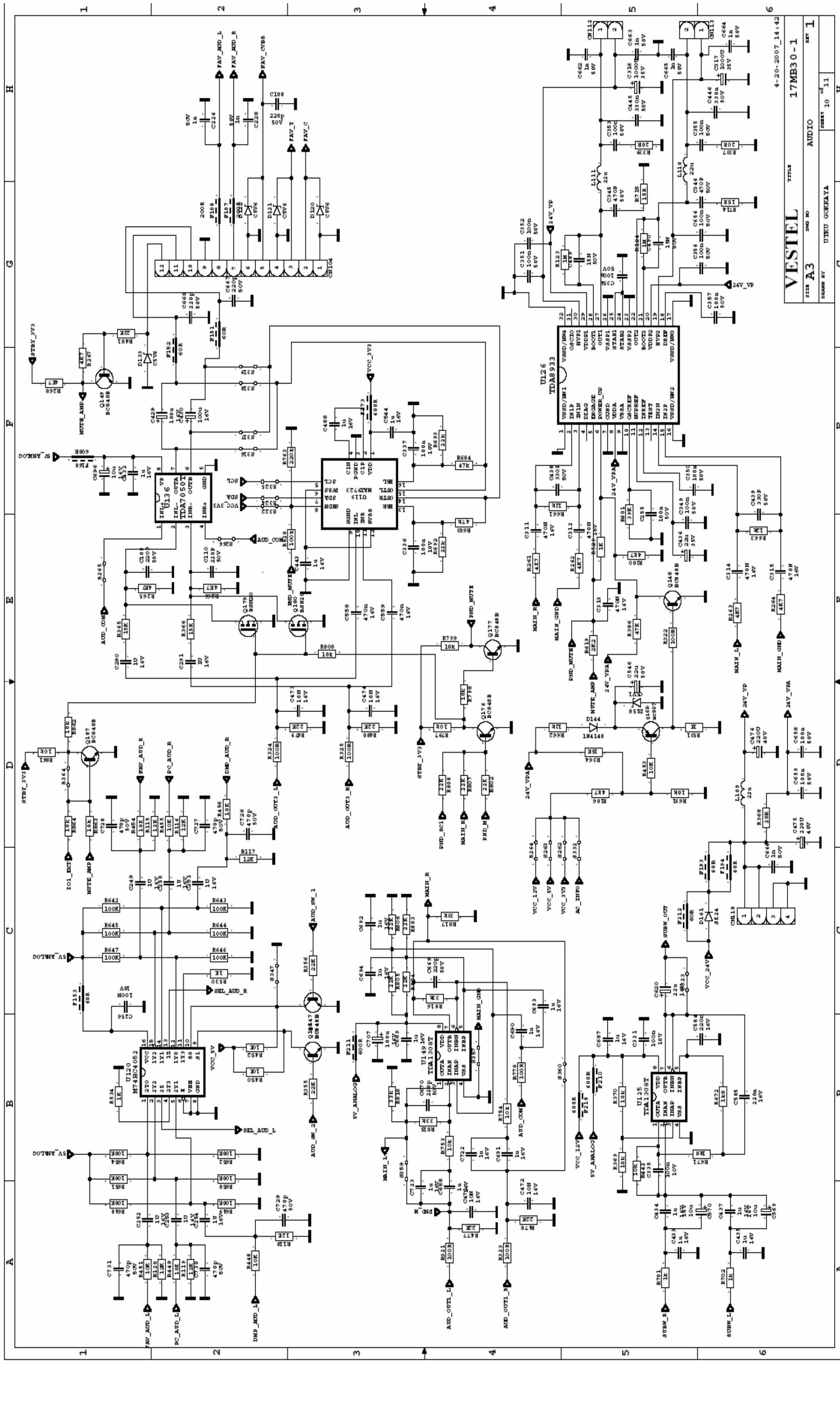
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CN113
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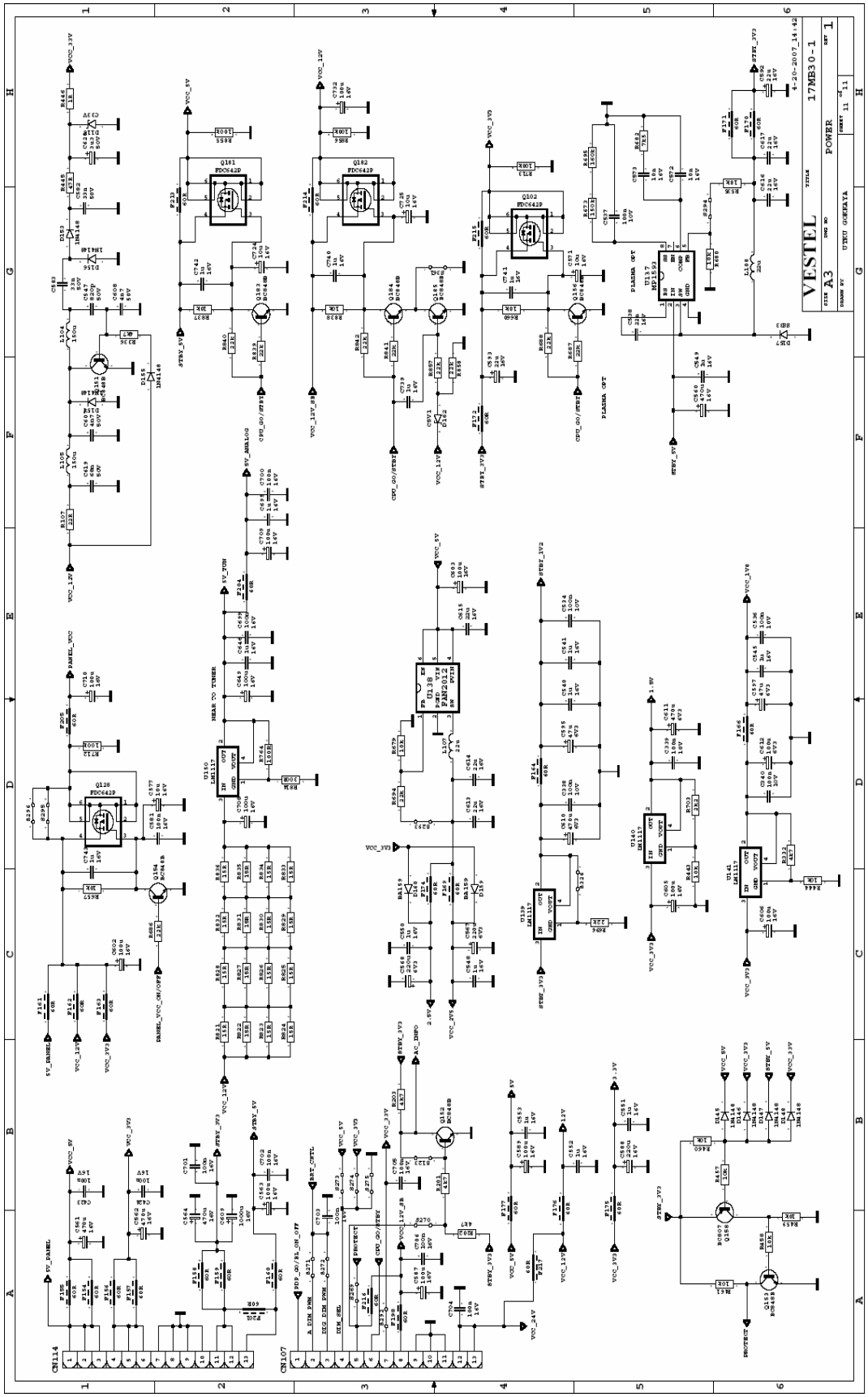
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APPENDIX C

LAYOUT