ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

A WIDE BANDWIDTH 8-BIT 20 MSPS SAR ADC

M.Sc. THESIS

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Electronics Engineering Programme

JANUARY 2015

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

YÜKSEK BAND GENİŞLİKLİ 8-BİT 20 MSPS SAR ADC

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Date of Defense : **22 January 2015**

to the dear memory of Ali,

FOREWORD

I would like to thank my thesis supervisor Assoc. Prof. Dr. Türker Küyel for his invaluable guidance, help and encouragement. I also should thank him and ITU VLSI LABs for providing me a computer and a desk at the office to work.

I thank my family and all my friends who helped me with the problems I encountered during my studies. I would never succeeded without their help and support.

And lastly, I would like to express my deep gratitude to open-source software community, especially LaTeX project and TexStudio which provided me an effective environment to create this thesis document and decreased the time I spent for formatting it.

January 2015

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ABBREVIATIONS

ADC : Analog to digital conversion
SAR : Successive approximation register
DNL : Differential non-linearity
INL : Integral non-linearity
SFDR : Spurious-free dynamic range
SINAD : Signal to noise and distortion (ratio)
SNR : Signal to noise ratio
ENOB : Effective number of bits
LTE : Long term evolution
UWB : Ultra-wide bandwidth
Msps (MS/s) : Mega-samples per second
MSB : Most significant bit
LSB : Least significant bit
DAC : Digital to analog converter
OPAMP : Operational amplifier
PVT : Process, voltage, temperature
SR : Set-reset
S/H : Sample-and-hold
VCM : Common mode voltage

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A WIDE BANDWIDTH 8-BIT 20 MSPS SAR ADC

SUMMARY

Real time oscilloscopes require very high speed analog to digital (A/D) conversion. 1 GHz bandwidth is common among mid-end oscilloscopes today, whereas up to 40 GHz bandwidth can be achieved by state of the art, high-end oscilloscopes. A/D converters in such oscilloscopes need to be 2 Gsps and 80 Gsps respectively.

Due to high bandwidth of the input signal, and difficulty of maintaining a linear, low jitter and low noise analog front-end, most oscilloscopes use no more than 8-bits of resolution in their A/D conversion stages. Other than achieving raw speed, lowering the power consumption of the A/D conversion becomes important for a certain class of battery powered, hand held oscilloscopes.

Successive approximation register (SAR) type A/D converters have recently gained popularity in high speed applications due to their inherently low power consumption. To compensate for the relatively low conversion rate of the SAR ADCs, time interleaving of multiple A/D converters can be used.

To have a smaller number of A/D converters in a time interleaved application, it becomes necessary to design a high bandwidth, fast and small SAR A/D converter. The purpose of this thesis is to demonstrate the design of such an A/D converter, using a standard 180nm CMOS process, for future work on time interleaving.

Main specifications of the A/D converter are 1 GHz analog input bandwidth, 20 Msps sampling rate, 8-bits of resolution, and more than 6 effective number of bits at Nyquist frequency across process, supply, temperature, and chip to chip variations. To help reduce mismatch effects during time interleaving, the A/D converter is offset cancelled, and voltage references will be shared. Capacitor mismatch effects will not be pronounced for 8-bits of resolution.

100-way interleaving of such an A/D converter will be needed to design an 2 Gsps oscilloscope A/D converter, which is out of the scope of this work. Optimization of the design for lowest possible power consumption and smallest area is also beyond the scope of this thesis.

In this work, a reliable and feasible 8-bit, 20 Msps SAR A/D converter with 1 GHz bandwidth is presented using 180 nm standard CMOS process. A five stage comparator with 3-stage output offset cancellation is designed, characterized using simulation and laid out. A fully differential capacitive DAC driven by the SAR logic is designed and characterized using simulation. Three reference buffers for Vref+, Vref- and Vcm are also designed and characterized via simulation. Finally, the A/D converter using an effective timing pattern is constructed and characterized for offset, differential linearity (DNL), integral linearity (INL), spurious free dynamic range (SFDR), signal to noise and distortion (SINAD), signal to noise ratio (SNR) and effective number of bits (ENOB).

Simulations indicate that at full Nyquist bandwidth, the A/D converter exceeds 6 ENOB across process, voltage, temperature and chip to chip variation, with a nominal results of 7.2 bits. At a low 1 MHz input frequency, the nominal corner shows an ENOB of 7.95. Power consumption is typically 15mW excluding reference buffers, which will be shared during interleaving.

YÜKSEK BAND GENİŞLİKLİ 8-BİT 20 MSPS SAR ADC

ÖZET

Bilgisayar ve mikrodenetleyiciler sayısal işaretlerle işlem yapmaya müsaittir, analog sinyaller üzerinde işlem yapamazlar. Dış dünya tamamen analog olduğu için, ortamdan herhangi bir işaret ile çalışmak gerektiği zaman, bu işaretin sayısal veriye çevrilmesi gerekir. Bu sayısal veri üzerinde mikroişlemci veya bilgisayarlar aracılığıyla istenen işlem gerçeklenir, alınan sonuç ise gerekiyorsa tekrar analog bir işarete çevrilir.

İşte bu iki dönüştürme işlemi için veri dönüştürücülere ihtiyaç vardır. Veri dönüştürücüler analog-sayısal dönüştürücü ve sayısal-analog dönüştürücü olarak iki gruba ayrılır. Analog-sayısal dönüştürücüler analog olduğunu bildiğimiz dış dünya ile sayısal işaretlerle çalıştığını bildiğimiz bilgisayarlar arasında bir köprü görevi görür. Adından da anlaşılabileceği gibi, analog bir işareti sayısal bir işarete dönüştürmede kullanılır.

Entegre devreler üzerinde, belirli bir işlevi gerçekleştirmek amacıyla, çok sayıda alt bloktan oluşan, karmaşık sistemler tasarlanmaktadır. Sistemdeki alt blokların sayısı arttıkça, her bir blokun tükettiği güç de önem kazanmaktadır. Bu nedenle her bir alt blokun tasarlanmasında, güç tüketimi de özellikle göz önünde bulundurulmalı, güç tüketimini azaltacak yöntemler geliştirmek ve uygulamak gerekmektedir.

Güç tüketimi dışındaki bir diğer önemli husus da tasarlanan devrenin çalışma hızıdır. Örneğin yüksek hızlı veri iletişimi sağlayacak bir entegre devre tasarlanırken alt blokların tamamının gerekli çalışma hızı kriterlerini sağladığından emin olmak gerekir. Veri dönüştürücülerin de bu kapsamda, sürekli artan çalışma hızı (çalışma frekansı) ihtiyacını karşılayabilecek düzeyde tasarlamak gerektiği göz önünde bulundurulmalıdır.

Veri dönüştürücüler tasarlanırken, yüksek olması hedeflenen bir özellik de dönüştürücünün hassasiyetidir. Veri dönüştürücülerin hassasiyetleri, giriş işaretlerinde algılayıp dönüştürebildikleri en küçük değişim ile tanımlanır. Bu değere "en az anlamlı bit" (Least Significant Bit- LSB) adı verilir. Veri dönüştürücüler genellikle dönüştürebildikleri bit sayısına göre adlandırılırlar.

Analog-sayısal dönüştürücülerde (Analog to Digital Converter - ADC) artan örnekleme frekansı ihtiyacını karşılamak ve güç tüketimini azaltmak için çeşitli metotlar kullanıma sunulmuştur. Zaman bölmeli (Time Interleaved) analog-sayısal dönüştürücü yapısı, bu alanda son derece tatmin edici sonuçlar sağlayan bir yapıdır. Zaman bölmeli ADC basitçe, bir analog giriş işaretinin belirli bir zaman gecikmesi ile, belirli sayıda alt ADC tarafından örneklenerek sayısal veriye dönüştürülmesi, ardından bu sayısal verilerin uygun şekilde birleştirilmesi esasına dayanır. Bu şekilde, her bir ADC alt blokunun tek başına örnekleyip dönüştürebileceği analog giriş işaretinden çok daha yüksek frekanslardaki analog giriş işaretleri örneklenip dönüştürülebilmektedir.

Zaman bölmeli ADC tasarımı için alt blok olarak kullanılacak bir ADC'nin sağlaması gereken özellikler, düşük güç tüketimi, orta çözünürlük, orta örnekleme frekansı, ve yüksek giriş band genişliği olarak sıralanabilir.

Gerçek zamanlı osiloskop tasarımları için, çok yüksek hızlı analog-sayısal dönüştürücülere ihtiyaç vardır. Bunun yanısıra, günümüzde orta seviye osiloskoplarda 1 GHz bant genişliği oldukça yaygınken, üst seviye, son teknoloji osiloskoplarda 40 GHz gibi bant genişliklerine ulaşılabilmektedir. Bu gibi osiloskoplarda kullanılan analog-sayısal dönüştürücülerin ise sırasıyla 2 Gsps ve 80 Gsps hızlarında çalışması gerekmektedir.

Osiloskopların analog-sayısal dönüştürücü katlarında, giriş işaretinin yüksek bant genişliğine sahip olması ve doğrusal, düşük gürültü ve düşük seğirme (jitter) hatası özelliklerine sahip analog giriş katı elde etmenin oldukça zor olmasından dolayı, çoğunlukla 8 bitten yüksek çözünürlükler kullanılmaz. Pil ile çalışan bazı belirli el tipi osiloskop çeşitleri için, temel olarak, yüksek hıza ulaşmak dışında, analog-sayısal dönüştürücünün güç tüketiminin düşürülmesi de büyük önem kazanmaktadır.

Ardışıl yaklaşımlı bellek (Successive approximation register - SAR) tipi analog-sayısal dönüştürücüler, yapıları gereği doğal olarak sahip oldukları düşük güç tüketim özelliklerinden dolayı yüksek hızlı uygulamalarda yaygınlık kazanmaya başladılar. SAR analog-sayısal dönüştürücülerin görece düşük dönüştürme oranlarını telafi etmek için birden fazla analog-sayısal dönüştürücü için zamanda dönüşümlü çalışma (time interleaving) yöntemi uygulanabilir.

Zamanda dönüşümlü çalışma uygulamalarında, kullanılacak analog-sayısal dönüştürücü sayısını düşük tutabilmek için, yüksek bant genişlikli, hızlı ve küçük boyutlu bir SAR analog-sayısal dönüştürücü tasarlamak gerekmektedir. Yapılan literatür araştırmaları sonucunda, sayılan özellikleri sağlayabilecek bir yapı olarak ardışıl yaklaşım bellekli (Successive Approximation Register - SAR) ADC yapısı kullanmak uygun görülmüştür.

Bu tezin amacı, gelecekteki, zamanda dönüşümlü çalışan analog-sayısal dönüştürücü çalışmaları için, standart 180nm CMOS prosesi kullanarak tasarlanmış olan, bu tip bir analog-sayısal dönüştürücü sunmaktır.

Tasarlanan analog-sayısal dönüştürücünün temel özellikleri şöyle sıralanabilir: 1 GHz analog giriş bant genişliği, 20 Msps örnekleme sıklığı, 8-bit çözünürlük, ve Nyquist frekans bölgesinde tüm proses, besleme gerilimi, sıcaklık ve yongadan yongaya değişimler boyunca 6'dan yüksek etkin bit sayısı. Zamanda dönüşümlü çalışma esnasında oluşabilecek uyumsuzlukları azaltmaya destek olması için, analog-sayısal dönüştürücüde offset giderme tekniği kullanılmıştır. Aynı zamanda Referans gerilimleri de ortak kullanılacaktır. 8-bit çözünürlük için kapasitör eşleşme sorunları göz ardı edilebileceği için, dile getirlilmeyecektir.

2 Gsps örnekleme sıklığına sahip bir analog-sayısal dönüştürücü tasarlamak için, bu özelliklerde bir analog-sayısal dönüştürücüden 100 tanesı zamanda dönüşümlü çalıştırılmalıdır. Bu özellikler bu tez çalışmasının konusu dışındadır.

Bu çalışmada, 180 nm standart CMOS prosesi kullanılarak, güvenilir ve uygulanabilir, 1 GHz bant genişliğine sahip bir 8-bit, 20 Msps SAR analog-sayısal dönüştürücü tasarımı sunulmaktadır. 3 aşamada offset giderme tekniği uygulanmış 5 aşamalı bir karşılaştırıcı (comparator) tasarlanmış, benzetimlerle karakteristiği çıkarılmış ve serimi çizilmiştir.

SAR mantık devresi tarafından sürülen bir tamamen farksal kapasitif sayısal-analog dönüştürücü tasarlanmış ve benzetim yoluyla karakterize edilmiştir. Vref+, Vref- ve Vcm için üç adet referans tamponu (buffer) da tasarlanmış ve benzetim yoluyla karaktesitikleri çıkarılmıştır. Son olarak, analog-sayısal dönüştürücü de olabildiğince etkin bir zamanlama şeması kullanılarak tasarlanıp ayarlanmış, ve offset, farksal doğrusallık (differential linearity - DNL), integral doğrusallık (integral linearity - INL), parazitsiz devingen aralık (spurious free dynamic range - SFDR), işaret gürültü ve saptırma oranı (signal to noise and distortion - SINAD), işaret gürültü oranı (signal to noise ratio - SNR) ve etkin bit sayısı (and effective number of bits - ENOB) karakteristikleri belirlenmiştir.

Benzetim sonuçlarına göre, analog-sayısal dönüştürücü, Nyquist frekans bölgesinin tamamında, proses, kaynak gerilimi, sıcaklık ve yongadan yongaya değişimler boyunca 6 etkin bit sayısını aşmakta, nominal durumda ise 7.2 etkin bit sayısına ulaşmaktadır. 1 MHz gibi düşük giriş frekansında, nominal durumda etkin bit sayısı 7.95'e ulaşmaktadır. Güç tüketimi, zamanda dönüşümlü çalışma esnasında ortak kullanılacak olan referans tamponları hariç olmak üzere, tipik olarak 15 mW olarak ölçülmüştür.

Bu çalışmanın devamı olabilecek, ileride yapılması düşünülen çalışmalar ise, tasarlanan ADC'nin karakteristik özelliklerinin detaylıca incelenerek daha da yükseltimesi ve güç tüketiminin düşürülmesi, bütün devrenin seriminin yapılarak şematik seviyede alınan sonuçların serim sonrasında da alınmasının sağlanması olarak sıralanabilir. Ayrıca, tasarlanan alt blok kullanılarak, zaman bölmeli bir ADC tasarımı yapılması da çalışma planları arasında bulunmaktadır.

1. INTRODUCTION

Analog to digital converters (ADC) have wide range of application areas. This areas include wired and wireless communications, data acquisition systems, signal processing applications and medical applications. Specifications of the ADC can differ based on the area of application. For example, an ADC to be used in LTE wireless receivers must satisfy at least 50 MS/s of sampling speed, and 8 bits of effective resolution [1]. An ADC to be used in ultra-wideband (UWB) radio short distance wireless communications is required to have high speeds like 500 MS/s but low resolutions like 4-5 bits [2]. An ADC to be used in a digital x-ray instrument should have both high dynamic range, typically better than 90 dB, and excellent linearity [3].

1.1 ADC Structures

ADCs are designed in many different architectures depending on specification requirements. Each architecture has strong and weak sides. So, the architecture to choose depends on the design needs.

Main ADC architectures are flash, successive approximation register (SAR), pipeline and sigma-delta ($\Sigma - \Delta$). A comparison of architectures in terms of speed, resolution, power and size can be found in Table 1.1

1.1.1 Flash ADC

Flash ADC is the has the highest speed and lowest complexity among all low resolution ADC structures. Although they are very simple for low resolutions, the design complexity increases for higher resolutions. Furthermore, the comparator count needed for the design increases exponentially with increasing number of bits. This reduced speed and increases the chip area and power requirement drastically. High power dissipation, and large chip area are mainly caused by the need of many comparators, especially for resolutions exceeding 4 bits [4].

Table 1.1: Comparison chart for ADC structures.

TYPE	*SPEED*	*RESOLUTION*	*POWER*	*SIZE*
Flash	Highest	Lowest	Highest	Highest
Pipeline	High	Medium	High	High
Sigma-Delta	Low	High	Medium	High
SAR	Medium	Medium	Low	Low

Large number of comparators occupy large chip area and dissipate high power. $(2^n - 1)$ comparators and 2^n resistors are needed for an 'n' bit flash ADC, which means number of comparator and resistors are increasing exponentially with a linearly increasing resolution.

1.1.2 Pipeline ADC

Pipeline ADC is built as cascaded stages. Each stage obtains a number of bits of the digital output word corresponding to analog input voltage. Pipeline ADCs are mainly high speed and moderate precision converters. Main drawback of pipeline ADCs is the complexity of the design. Amplifier design becomes very hard for most modern pipeline ADCs.

1.1.3 Sigma-Delta ($\Sigma - \Delta$) ADC

Sigma-delta ADC is basically based the idea of noise shaping. The fraction of noise which falls into the Nyquist band is reduced by oversampling the input signal. Then the noise falling out of the band of interest can be filtered out digitally. A $\Sigma - \Delta$ ADC is used in low bandwidth but high precision applications. But it suffers from slow settling.

1.1.4 SAR ADC

SAR ADC stands between sigma-delta and pipeline ADC architectures with precision of 8-16 bits and speeds up to several MS/s, generally with low power consumption.

SAR ADC's popularity comes from its design simplicity, its high accuracy, low latency and dissipation of low power. A more detailed analysis of SAR ADC will be provided in the next chapters.

1.2 Motivation

Successive Approximation Register type analog to digital converters (DACs) have recently gained popularity in high speed applications due to their inherently low power consumption. It is possible to use an array of SAR ADCs and time interleaving to achieve multi-gigahertz bandwidths. The purpose of this thesis is to develop the main building block of a massively parallel, time interleaved analog to digital conversion system: A WIDE BANDWIDTH 8-BIT 20 MSPS SAR ADC block.

2. LITERATURE REVIEW

SAR ADC structure and circuit implementation techniques are explanied in detail in many textbooks [5–8]. Reviewing textbooks is a good start point before doing an additional literature survey for recently published SAR ADC papers. The brief literature survey below, gives an idea about what has been done to date in the area of SAR ADCs.

A 5-bit 500 MS/s time interleaved ADC for ultra-wide bandwidth (UWB) applications consisting of 6 SAR ADC slices is presented in [2]. It makes use of bridged capacitor array in order to reduce the capacitor sizes and adjustable latch strobe instant in order to use the time for settling more effectively. It achieves SNDR levels of 27.8 and 26.1 dB for 3.3 and 239 MHz respectively with a power consumtion of 6 mW for 1.2V supply voltage.

A 10-bit 50 MS/s SAR ADC with 826 μW power consumption and 54.4 dB SNDR for an input frequency of 50 MHz which is equal to the ADC's ERBW is presented in [9]. A new scheme of monotonic switching is implemented which reduces switching energy and total capacitance.

A 10-bit 100 MS/s SAR ADC with 3 mW power consumption and 56.6 dB SNDR is presented in [10]. It uses a reference-free technique and a new switching algorithm, which removes the need of an on-chip reference generator and improves linearity, respectively. The architecture also reduces the total capacitance required by a factor of two.

A 10-bit 40 MS/s SAR ADC with power consumption of 1.21 mW using a two-stage pipelined structure is presented in [11]. A peak SNDR of 55.1 dB is reported.

A 12-bit 45 MS/s SAR ADC with 3 mW power dissipation implementing digital calibration is presented in [12]. It achieves 70.1 dB SNDR at Nyquist frequency by employing sub-radix-2 redundancy and digital calibration techniques.

A 14-bit 80 MS/s SAR ADC with 31.1 mW power dissipation implementing circuit techniques such as utilizing a flash sub-ADC to resolve the 5 MSBs quickly,and a time interleaving operation scheme for speed increasing [13]. It reports a peak SNDR of 73.6 dB.

An 8-bit 10 MS/s SAR ADC with a power dissipation of 26 μW is presented in [14]. It uses some techniques like custom designed capacitors and asynchronous dynamic logic in order to lower power consumption.

A 10-bit 1 kS/s SAR ADC for ultra low power applications like medical implant devices is presented in [15]. A power dissipation of as low as 53 nW is achieved by utilizing low leakage circuit techniques and a switching technique to take away the need for bootstrapped switches.

A 10-bit 40 MS/s SAR ADC dissipating 550 μW power is presented in [16]. It uses a custom algorithm for DAC switching, and digital error correction to improve linearity. It reports 50.6 dB SNDR for a 20 MHz input frequency.

A 12-bit 50 MS/s two stage pipeline ADC with a large first stage SAR sub-ADC resolutions proposed in [17]. A power consumption of 3.5 mW and an SNDR of 66 dB for 2 MHz input frequency is reported.

A dual 5-bit 500 MS/s 6 way time interleaved SAR ADC with a power consumption of 7.8 mW per ADC is presented in [18]. It implements full custom logic, self timed bit cycling and duty cycling of the comparator preamplifiers in order to achieve high sampling rate and low power consumption.

Our SAR ADC is meant for exploring the difficulties and error mechanisms of a standard architecture, especially in timing and offset matching.

We achieve 8-bit 30 MS/s operation at 1 GHz bandwidth with offset cancellation; however, we are far behind existing literature in terms of resolution and power. Our ADC is targeted for wide-band applications, similar to [18].

3. SAR ADC ALGORITHM

A SAR ADC consists of a sample and hold (S/H), a comparator, a digital to analog converter (DAC) and a SAR logic circuit. SAR ADC utilizes the algorithm of binary search. Operation flow of this binary search algorithm is depicted in Fig. 3.1.

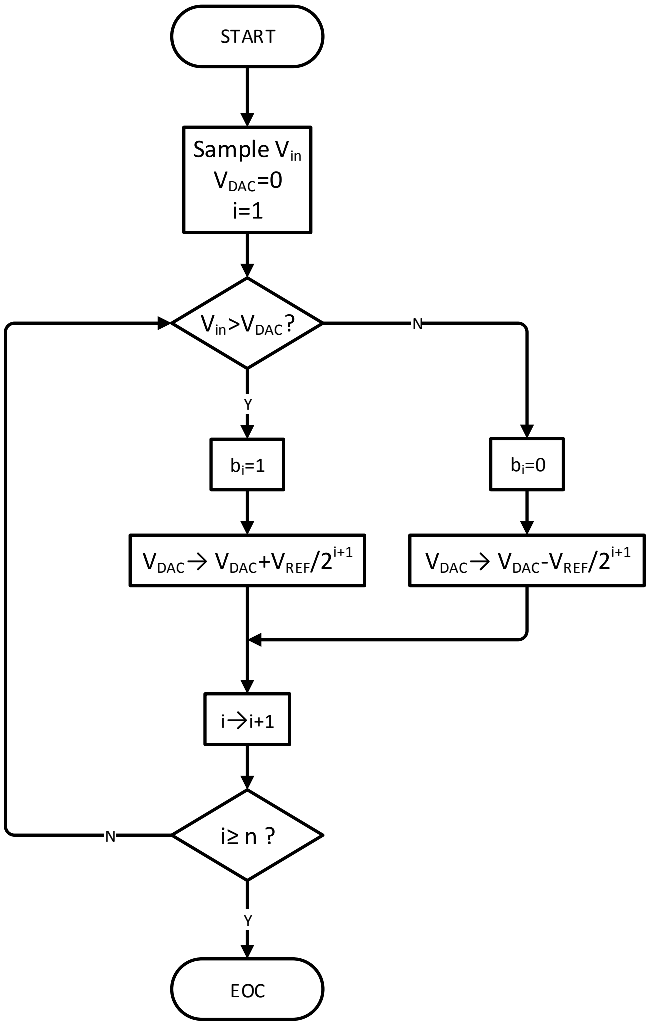
START
Sample V_{in}
V_{DAC}=0
i=1
V_{in}>V_{DAC}?
N
Y
b_i=1
b_i=0
$V_{DAC} \rightarrow V_{DAC}+V_{REF}/2^{i+1}$
$V_{DAC} \rightarrow V_{DAC}-V_{REF}/2^{i+1}$
i→i+1
i≥ n ?
N
Y
EOC

Figure 3.1: SAR ADC algorithm flow.

The ADC analog input voltage is digitized by comparing it to analog voltage counterparts of known digital words in a successive manner.

An illustration of binary search algorithm is shown in Fig. 3.2. This algorithm is very straight forward and easy to understand. Analog V_i voltage first needs to be

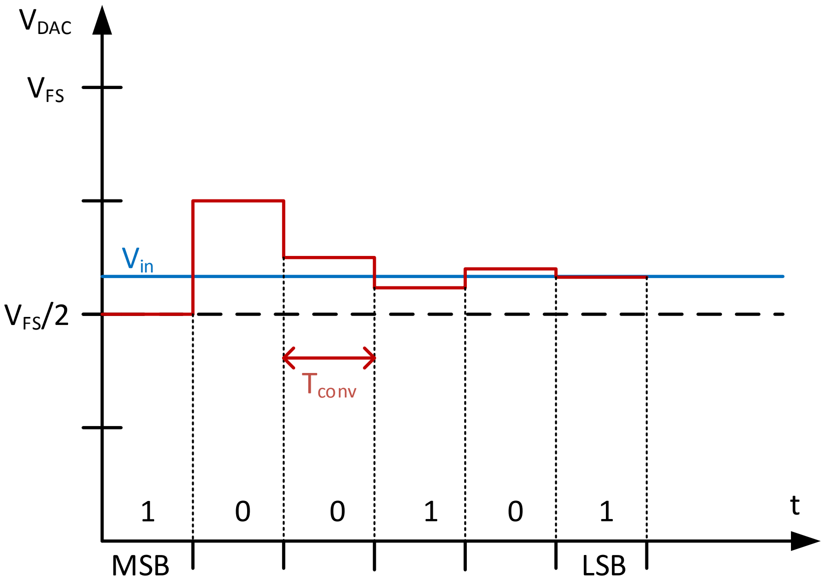

Figure 3.2: Binary search algorithm.

compared with half of the full scale voltage. To do this, SAR logic gives out digital word of '100...0' which corresponds to digital representation of half of the analog full scale voltage. This initial digital word is then converted to an analog voltage by the DAC. This analog voltage is the middle point of the full scale voltage as stated before. Then comparator compares sampled analog input voltage with the voltage converted to analog by the DAC and gives out a '1' if the analog sampled input voltage is larger than DAC output voltage, otherwise gives out a '0'.

Then, the comparator's first output is saved as the MSB of the ADC output and the first cycle is finished. Then the second cycle begins with keeping the comparator's first output as SAR logic digital output word's first MSB, and setting the second MSB to '1'. Now DAC converts this second digital word into an analog voltage again, which is either $1/4$ or $3/4$ of the full scale range depending on the first MSB came out from comparator's first result.

So the comparator's second comparison job is to find whether sampled analog input voltage is larger than DAC's second output voltage. If this is true, comparator gives a '1', if not, comparator gives a '0'. Depending on this decision, the second MSB of ADC output word is determined and the second cycle is finished.

This way, at each cycle, the sampled analog input voltage is confined into a voltage interval which is half of the previous one, beginning from half scale. That is, the search space is reduced to half, at each iteration. Continuing this process for ‘n’ cycles, the sampled analog input voltage is confined into a voltage interval of $V_{FS} \cdot 1/2^n$, and the digital representation of it is determined with a precision of $V_{FS} \cdot 1/2^n$, which is called ‘1 LSB’.

4. DESIGNED BUILDING BLOCKS

4.1 Comparator

Comparator is a circuit that compares two analog input voltages and gives digital output of either a ‘1’ or a ‘0’ depending on the result of the comparison. That is, if the analog voltage at positive input terminal is larger than the one at negative input terminal, then the comparator gives a ‘1’, otherwise gives a ‘0’. Assuming that the comparator is fully differential as in our design, the negative output terminal can be defined as the digital inverse of the positive output terminal.

4.1.1 Output offset storage

Comparators are generally designed as an amplifier to amplify the input signal difference, following by a latch to obtain output voltages at digital levels as quickly as possible. A problem of offset voltage occurs when differential input pair of amplifier do not match perfectly. When low amplitude input voltages are applied to the comparator input, amplifier offset can cause latch to do mis-decisions because of the amplifier’s offset voltage. There are several methods to minimize this offset dependency [5]. Comparator in this work is designed based on the structure of output offset storage for offset cancellation described in detail in [5, 19]. The simplest version of this architecture consists of a single fully differential amplifier, following by offset storage capacitors and a latch as seen in Fig. 4.1.

The offset cancellation process begins with shorting comparator input terminals and capacitors’ plates connected to latch input to ground. In this phase, the only voltage that amplifier will amplify is the input referred offset voltage of the amplifier (V_{off}). So, the output voltage of the amplifier is $A \cdot V_{off}$, where A is the gain, and V_{off} is the input referred offset voltage of the amplifier. Input referred offset voltage is amplified by the amplifier and stored onto the offset storing capacitors. As a second phase, the switches that connect the inputs of the amplifier (S_{osi}) and latch (S_{oso}) are OFF and the

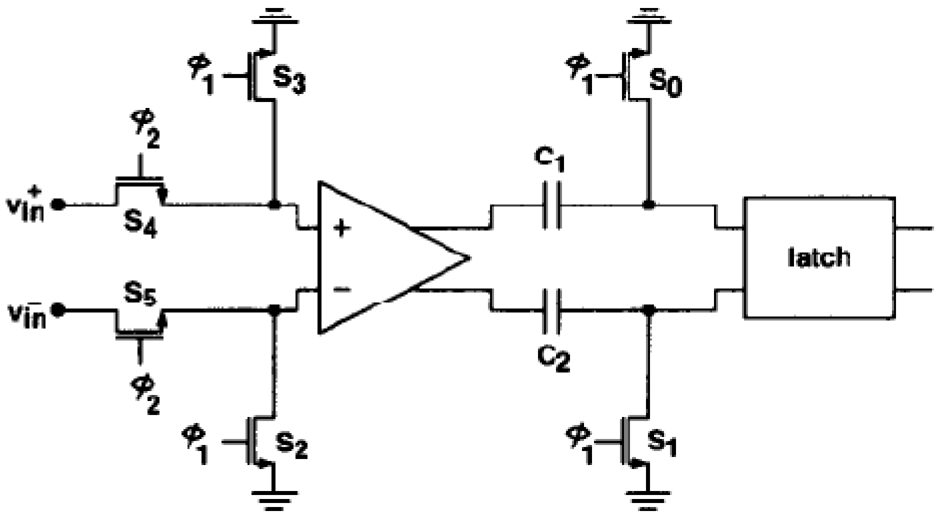

Figure 4.1: Output offset storage method.

switches between input voltages and input terminals of the comparator (S_{in}) are ON. Now, the amplifier amplifies both the input voltage and offset, so, a voltage of

$$V_{in,latch} = A \cdot (V_{in} + V_{off}) - A \cdot V_{off} = A \cdot V_{in} \quad \textbf{(4.1)}$$

at the input terminals of the latch. This way, In the first phase amplified offset voltage is stored onto the offset cancelling capacitors, and in the second phase that stored voltage is subtracted from the amplified input and offset voltage, so that only the amplified input voltage is seen from the input ports of the latch. Then the latch gives digital level output voltages by hitting either to VDD or GND depending on the amplified input voltages.

The offset voltage of amplifier can be eliminated by using output offset storig method, but the offset voltage of the latch is still remaining. A high gain amplifier is needed to overcome the offset voltage of the latch, which can be as high as 100 mV for a CMOS latch, even for the minimum comparator input voltage. But a high gain may saturate the amplifier output when amplifying the offset voltage. Furthermore, high gain amplifiers are generally slower than low gain amplifiers. In order to prevent this, multiple amplifier stages with lower gain are employed. This way, the gain required to overcome the offset voltage of the latch is obtained as a sum of lower gains, and at the same time outputs of the amplifiers are exposed to a lower risk of saturating at the offset storing phase.

A 5 gain stage followed by a latch is used in this work to fulfill both gain and speed requirement. A schematic of the designed comparator is depicted in Fig. 4.2.

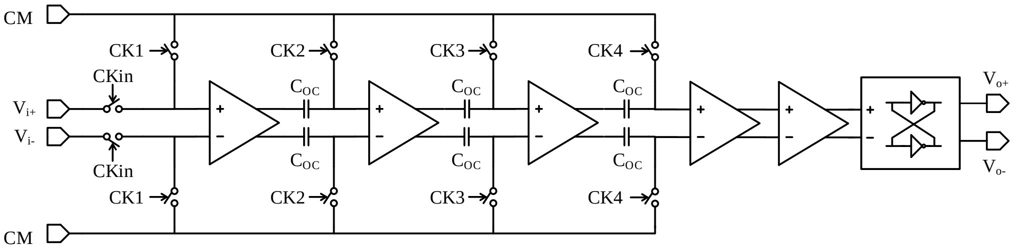

Figure 4.2: Designed comparator structure.

4.1.2 Amplifiers

Amplifiers are designed based on the CMOS common source differential pair gain stage. In order to have the highest speed, resistive loads are preferred. Trade-off here is between speed, gain and power consumption. In order to have high gain, large resistors are needed, which limits the output common mode voltage. Using small resistors increases the current flowing through branches increasing power consumption.

Gain equation for the resistive load differential pair amplifier is given by

$$A = g_m \cdot R_L \tag{4.2}$$

where

$$g_m = \frac{2 \cdot I_D}{V_{GS} - V_T} \tag{4.3}$$

as obtained from [20].

Considering the trade-off between gain and power consumption, the input transistor sizes and resistor values should be decided carefully. We used $w/l = 6\mu m/0.18\mu m$ input transistor sizes, $2.4k\Omega$ load resistors a tail current of $480\mu A$, and a $V_{ON} = V_{GD} - V_T$ voltage of $250mV$ which gives a gain around 4.6.

Using resistors as load devices brings difficulties in stabilizing the current flowing from branches of the differential pair. Mismatch in resistors and input transistors can cause the current flowing from the branches of the differential pair to differ from each other. Another drawback is that tail current should be also stabilized, since a small change in tail current changes the output common mode voltage significantly because of the load resistors. In order to stabilize tail current, a cascode transistor is added to the current source.

Another source of error is so called ‘overdrive’. If sign of small differential input voltage changes while the differential output voltage is large, amplifier may slowly flip, or even may not be able to flip the outputs. In order to minimize this effect a resetting switch is connected between output nodes of the amplifier, which shorts the outputs and sets them to the common mode voltage just before next input voltage is given. This process is named as ‘overdrive recovery’.

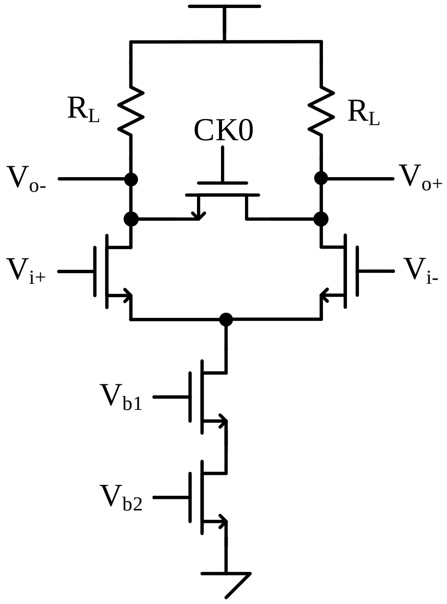

Figure 4.3: Designed amplifier architecture.

An amplifier testbench is seen in Fig 4.4, and a graph of transient waveforms of the designed amplifier is seen in Fig. 4.5. Amplifier settling time results can be seen in 4.6.

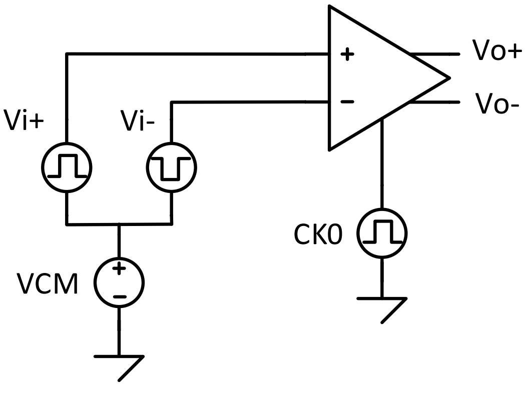

Figure 4.4: Amplifier test-bench.

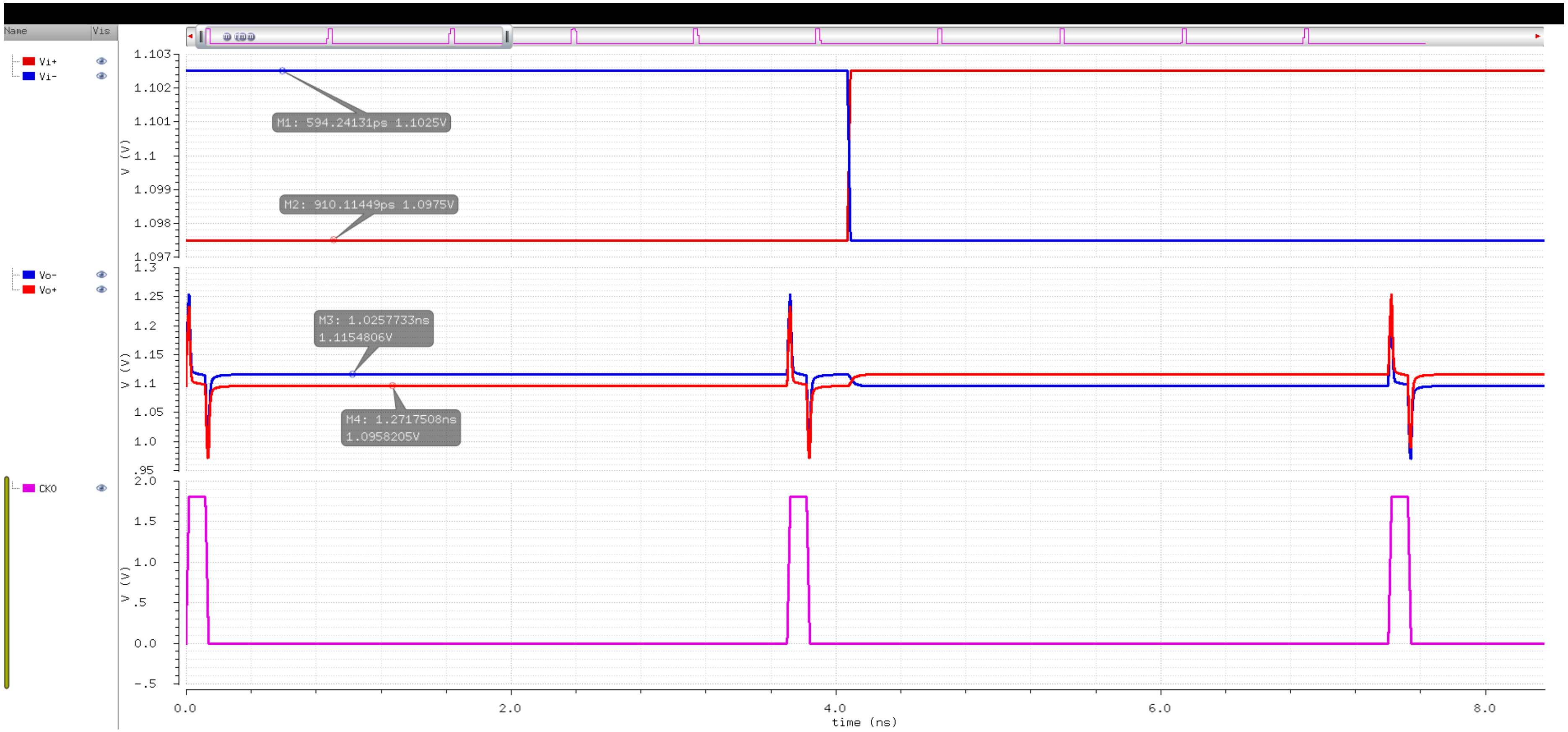

Figure 4.5: Aplifier input-output graphics.

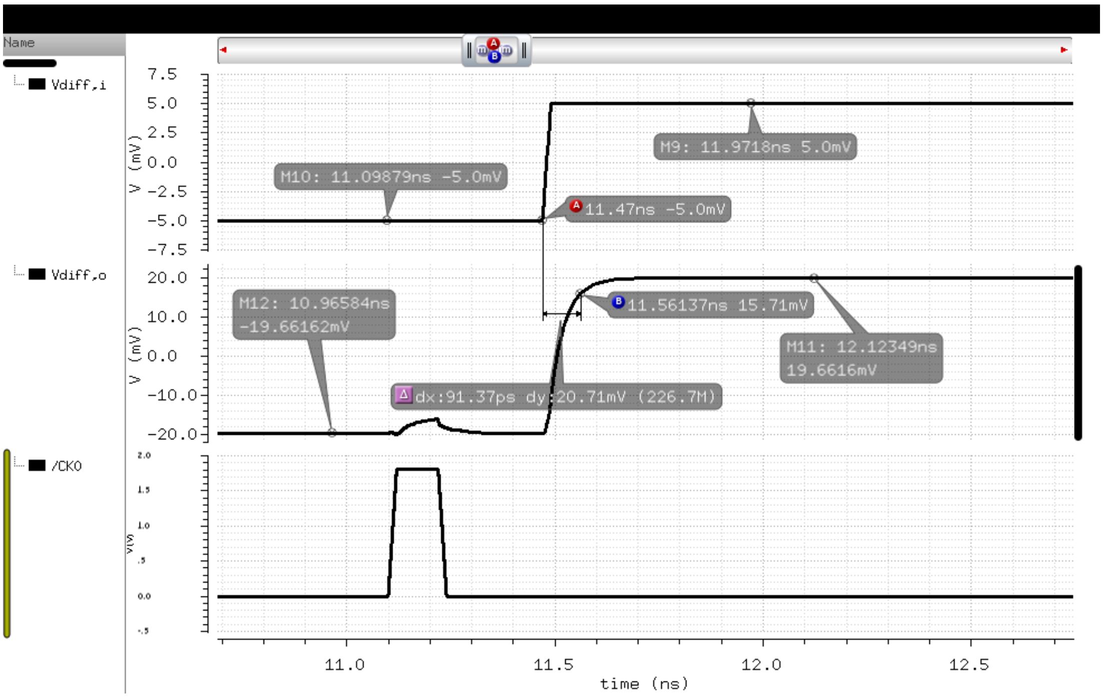

Figure 4.6: Amplifier settling time.

As seen in Fig. 4.4 and 4.5, a differential square wave of $\pm 2.5mV$ (which is actually smaller than ADC's LSB value of $7.8mV$) around a common mode voltage of $1.1V$ is given to inputs of the amplifier and the outputs are observed. Amplifier gain can be calculated as

$$\begin{aligned} A &= \frac{V_{diff,o}}{V_{diff,i}} = \frac{V_{o+} - V_{o-}}{V_{i+} - V_{i-}} \\ &= \frac{1.1155 - 1.0958}{0.005} \\ &= 3.94 \end{aligned} \tag{4.4}$$

So, ideally thinking, expected total gain from five cascaded stages can be calculated as

$$\begin{aligned} A_{tot} = 3.94^5 &= 949.47 \\ &= 59.55dB \end{aligned} \tag{4.5}$$

But the parasitic capacitors between the gate of the differential pair input transistors and the common mode voltage level form a voltage divider decreasing the gain by a factor of $C_{OS}/(C_{OS} + C_{gp})$, where C_{OS} is the offset storing capacitance and C_{gp} is the parasitic capacitances between gate and common mode voltage source.In order to keep gain reducing factor fair enough, offset storing larger capacitances should be used, considering the trade-off between gain factor and speed. Simulations showed that 100 fF offset storing capacitors are a good value to have a fair point of benefit.

Also, as [5] suggests, offsets of the last two gain stages are not canceled, since their contribution to the input referred offset voltage is not large, according to the formula of

$$V_{in,off,n} = \frac{V_{off,n}}{A^n} \tag{4.6}$$

where $V_{in,off,n}$ is the input referred offset voltage of nth amplifier, $V_{off,n}$ is the offset voltage of nth amplifier, and A is the gain of the amplifiers. This way, total gain obtained from the amplifier stages are also increased, since the gain reduction factor is not in affect at last two stages.

4.1.3 Latch

Latch is a high gain stage with logic level outputs which employs positive feedback. When using positive feedback, special attention should be paid to the inputs. Small input variations can cause the latch to hit to wrong logic level. Amplifier gain plays the key role in preventing this error. Also hitting the latch output from a logic level to the other can take longer.

A latch design of Fig. 4.7 is used in this work. The PMOS and NMOS transistor couples form two positive feedback loops which are used as a latch. The inverters at the outputs are employed in order to easily drive the next stage. When the ‘LATCH’ signal gets HIGH, the positive feedback occurs and feeds the outputs to logic levels.

4.1.4 Comparator simulations

4.1.4.1 Schematic level simulations

Comparator is simulated and its performance is analyzed. Test-bench is established as in Fig. 4.8. Input-output voltages and the clock signals of the comparator are presented in Fig. 4.9.

CK0 is the overdrive recovery switch control signal, CK(i) ($i = 1...5$) is the control signal which shorts the inputs of the ith amplifier to the common mode voltage.

CK6 is the control signal of the switch which connects the input voltage to the first amplifier. CKL is the latch control signal.

For simplicity, only some of the amplifiers input-output voltages are plotted.

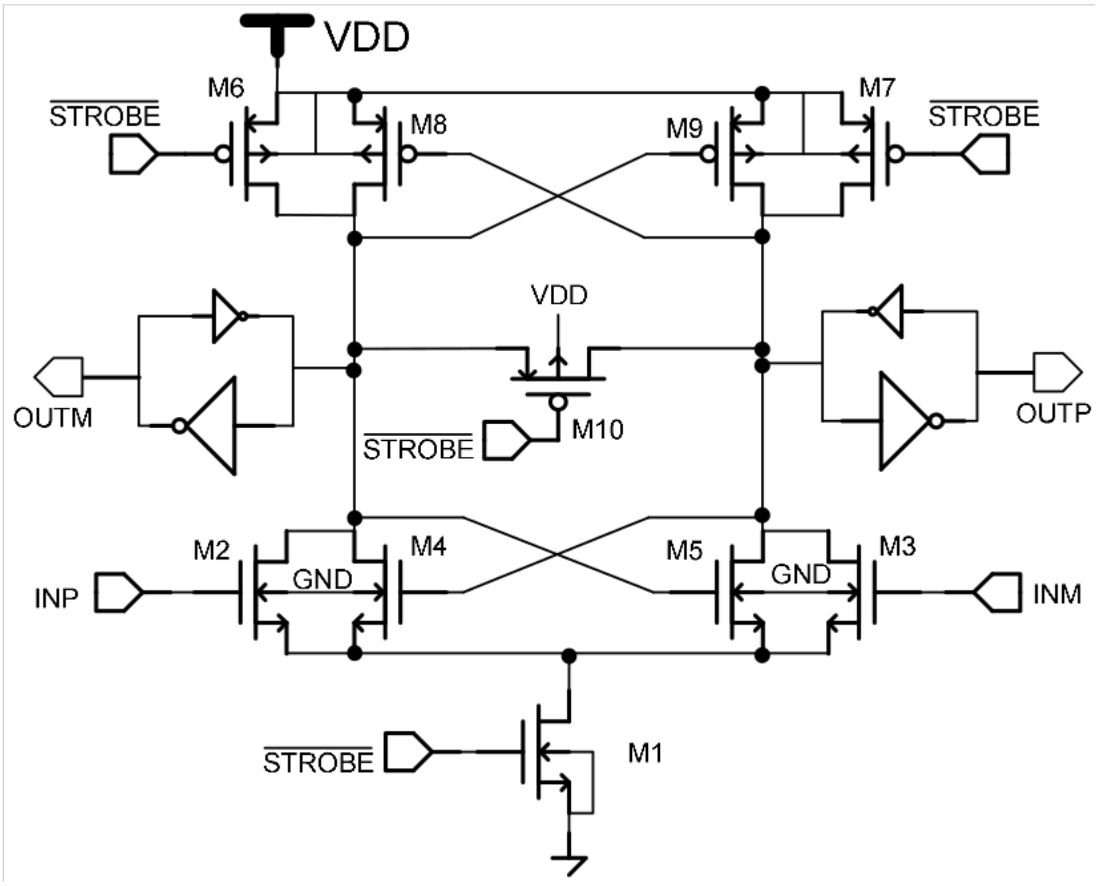
VDD
M6
M7
M8
M9
STROBE
STROBE
VDD
OUTM
OUTP
M10
STROBE
M2
M4
M5
M3
GND
GND
INP
INM
STROBE
M1

Figure 4.7: Designed latch structure.

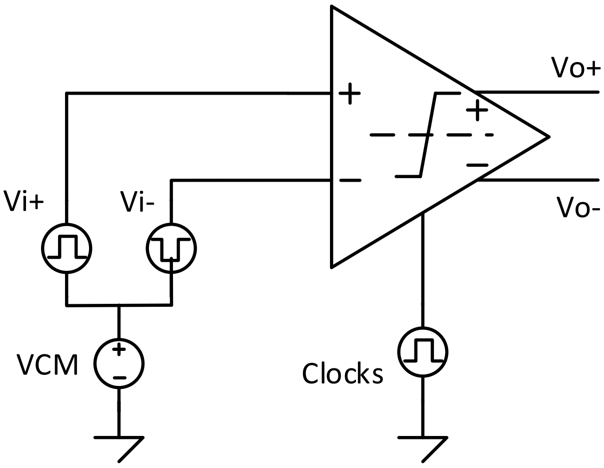
Vo+
Vo-
+
–
+
–
Vi+
Vi-
VCM
Clocks

Figure 4.8: comparator test-bench.

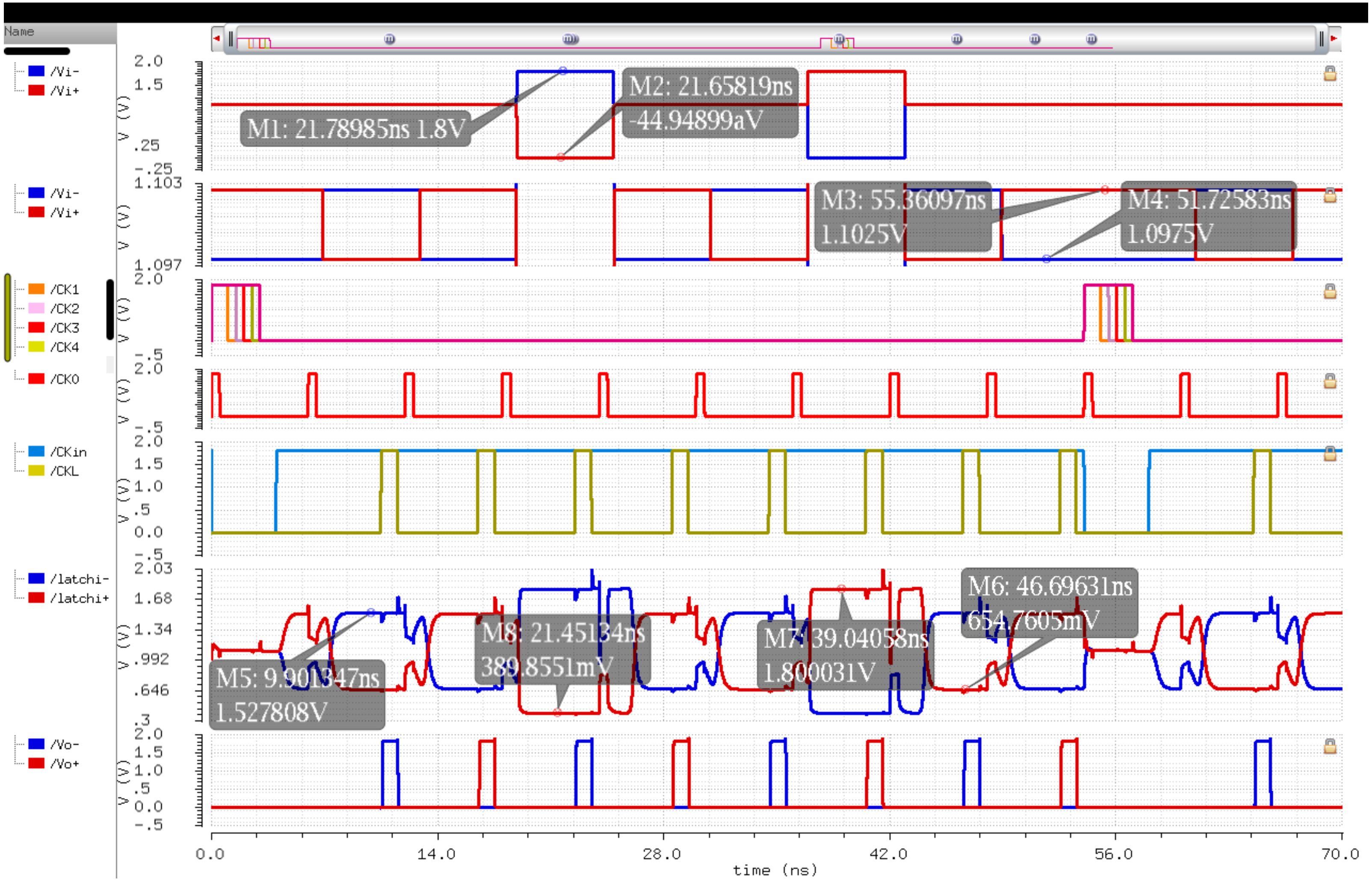

Figure 4.9: Comparator input-output graphics.

The comparator test-bench is executed as if it is operating in SAR ADC structure. That is, the comparison starts with a RESET clock, which is not directly effective in comparator operation. Since the RESET phase does not have any direct relation with the comparator, it can be used as a phase of offset cancellation. So, all the offset cancellation clock signals and the overdrive recovery clock signal are placed within the RESET phase. Following 8 clock cycles are used for 8 comparisons as seen in Fig. 4.9.

Overdrive recovery is performed at the beginning of each comparison in contrast to the offset cancellation which is performed once at each ADC conversion cycle. As the offset storing capacitors are not discharging during the ADC conversion, applying offset cancellation algorithm once in a conversion is sufficient.

The most difficult comparison for a comparator to do is when a small differential input voltage is applied after a large one. A series of small ($5mV and 10mV$) and large (V_{FS}) differential input signals is applied to the comparator input terminals in order to verify that the comparator output voltage can successfully toggle with respect to both small and large input voltages. Since it is hard to see both small and large differential input signals in a single chart, the input voltages ‘Vin+’ and ‘Vin-’ are plotted twice, the second row is a zoomed version of the first row in Y axis.

Fig. 4.9 shows that the input signals are amplified differentially through the cascaded gain stages and reaches a differential voltage of almost $1V$ at the input of the latch for a small ($5mV$) differential input voltage just after a large one (V_{FS}), which is well over the offset voltage of the latch.

Total gain obtained from the amplifier stages and seen by the latch can be calculates as

$$\begin{aligned} A_{tot} &= \frac{(Latchi+) - (Latchi-)}{(Vi+) - (Vi-)} \\ &= \frac{1.6330936 - 0.55661036}{0.005} = 215.3 \end{aligned} \tag{4.7}$$

To test the offset cancellation, a mismatch is applied to the first amplifiers input transistors since they are the most sensitive ones to the offset. Input differential pair device sizes are changed as $(w/l)_a = 5.9\mu m/0.18\mu m$ and $(w/l)_a = 6.1\mu m/0.18\mu m$ which will cause a offset voltage at the outputs. Offset voltage is loaded to the offset storing capacitors while the CK1 and CK2 switches are ON. This offset voltage can be observed as $V_{off} = 1.127818V - 1.108296V = 19.522mV$ as output voltage of first amplifier A1 at the end of CK2 where input voltage is still disconnected in Fig. 4.10. It is obvious that this offset is almost totally eliminated at the inputs of the second amplifier A2.

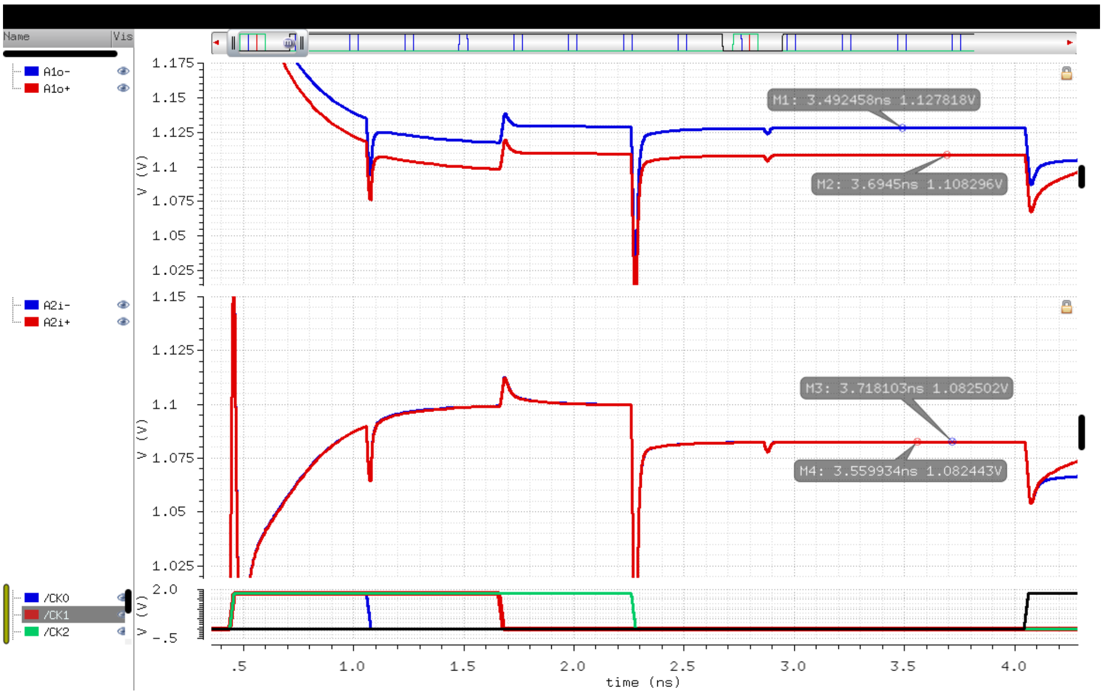
Name
Vis
A1o-
A1o+
A2i-
A2i+
/CK0
/CK1
/CK2
V (V)
1.175
1.15
1.125
1.1
1.075
1.05
1.025
M1: 3.492458ns 1.127818V
M2: 3.6945ns 1.108296V
M3: 3.718103ns 1.082502V
M4: 3.559934ns 1.082443V
2.0
-.5
.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
time (ns)

Figure 4.10: Offset cancellation process.

Comparator is also tested in PVT corners and Monte-Carlo analysis. Monte-Carlo at PVT corners of (SS, TT, FF, 1.71V, 1.8V, 1.89V, -40 °C, 0 °C, 27 °C, 85 °C, 105 °C, 125 °C) are tested and comparator passed these corners completely with zero bit error rate. A figure of comparator output voltage across corners can be seen in 4.11.

According to further Monte-Carlo analyses, the comparator found to operate properly with zero bit error rate up to 500 MHz speed at 125 °Cwith a precision of 4 mV differential input voltage.

4.1.4.2 Post-layout simulations

Drawing a layout for a high-speed comparator can be challenging. Since our design is compromises 5 stages, all the metal layers passing under and over each-other caused problems. Signal and clock paths have to be placed in a such way that the signal paths are ensured not to be effected by the high speed clock signals. Also the offset storing capacitors are very sensitive to noise both from other signals and the high speed clock

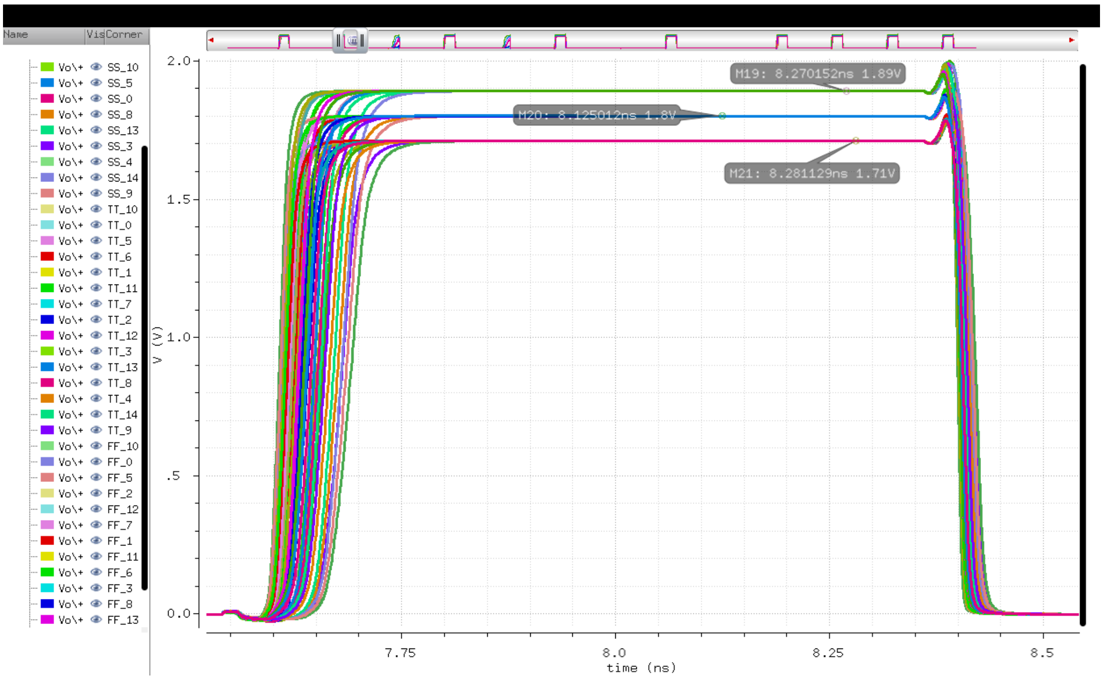

Figure 4.11: Comparator output for an input step voltage across PVT corners.

signals. They should be placed away enough from the high speed clock paths, for example.

A layout of the designed comparator is seen in Fig. 4.12. Since this is the first layout experiment, the area used is not very effective. Th whole comparator occupies an area $56\mu m \cdot 260\mu m$. It is obvious that the most of the area is reserved for the resistors. The resistors in the design should have good matching properties. In order to satisfy matching requirement, they are laid out on a larger area.

The same tests as the schematic tests are studied for the post-layout simulation. It is confirmed that the layout ensures input output characteristics of the comparator schematic design.

A graph of input-output and clock signals for the post layout simulations is depicted in Fig. 4.13.

4.2 Successive Approximation Register Logic Block

Successive Approximation Register (SAR) logic block determines each bit of the output code corresponding to analog input voltage successively, starting from the MSB. The SAR contains n bit shift register for an n-bit ADC.

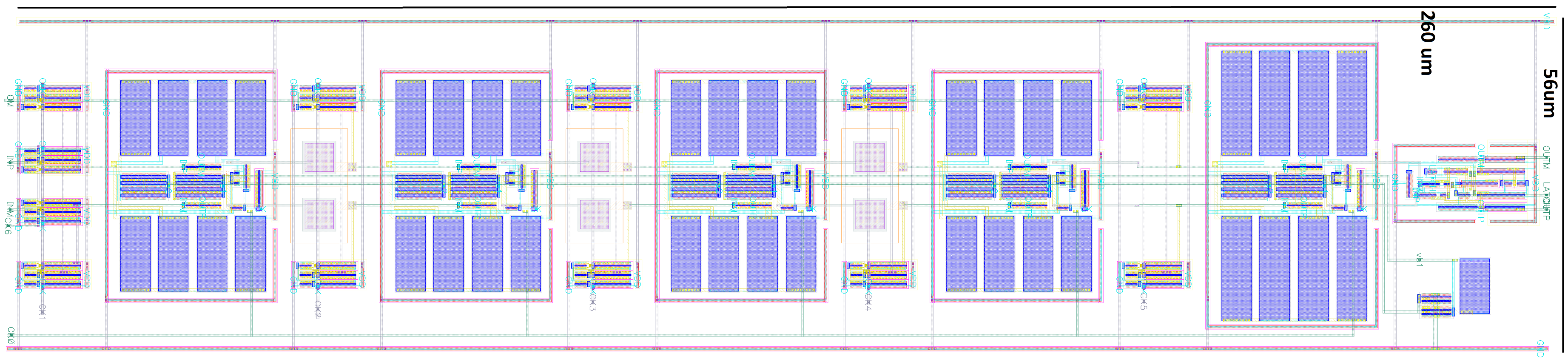
56um
260 um
VDD
GND
OUTM
OUTP
vb1
CK1
CK2
CK3
CK4
CK5
CK6
CKØ
OM
INP
INM

Figure 4.12: Comparator layout.

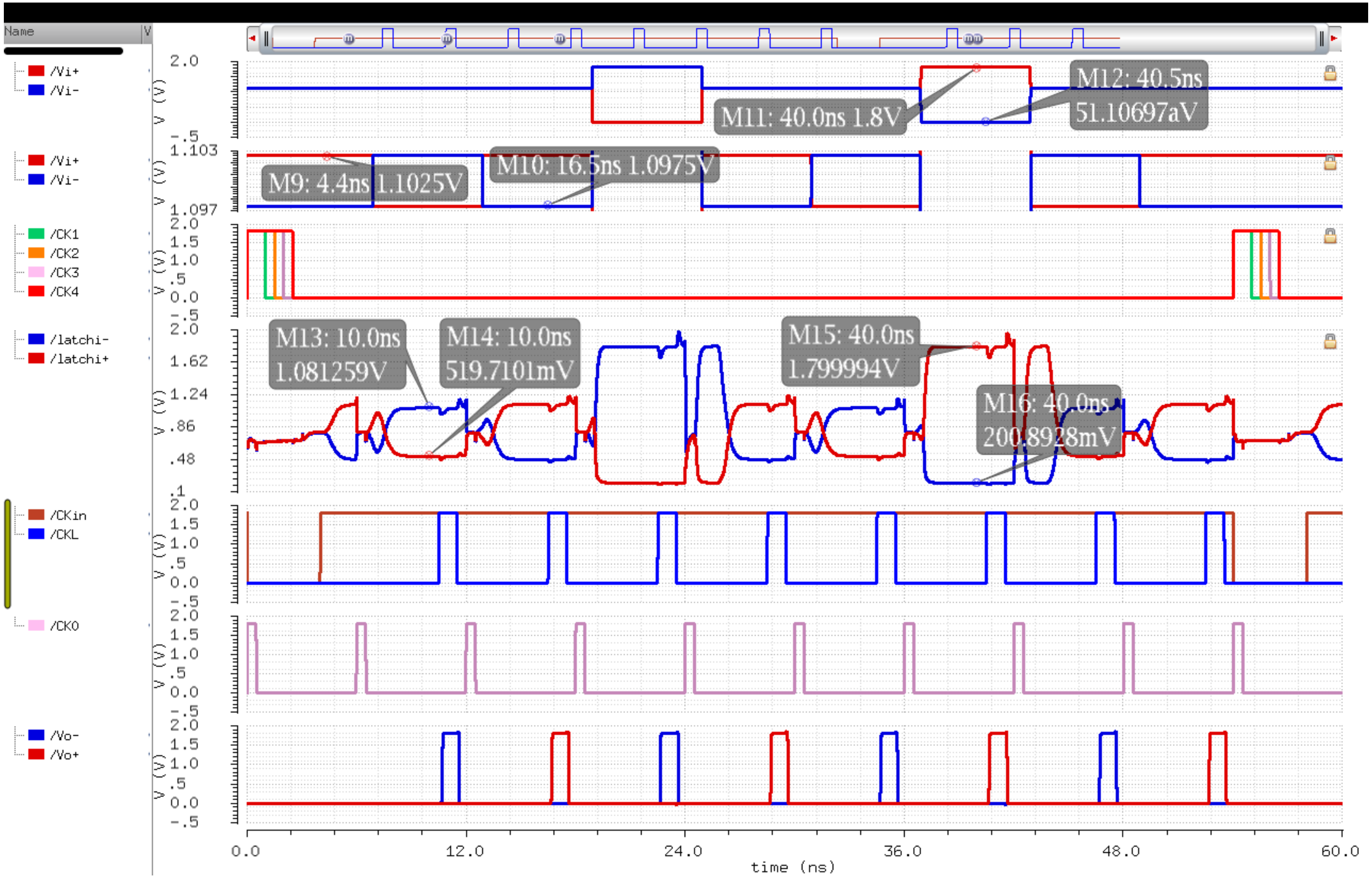

Figure 4.13: Comparator post-layout simulation input-output graph.

In the first step, MSB is set to '1' and other bits are reset to '0', the digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared to the sampled input. Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output of the DAC, the MSB remains at '1', otherwise it is reset to '0'. The rest of bits are determined in the same manner. In the last cycle, the converted digital word is stored to another shift register. Therefore, an n-bit SAR ADC takes n clock cycles and a sample time to perform a conversion.

4.2.1 SAR logic circuit design

This logic consists of a counter and a code register, in fact as a total of three 9-bit shift registers. For each conversion,in the first clock cycle, the most significant flip-flop is set to '1' which corresponds to MSB of the digital word to the DAC. Then the counter shifts '1' through the flip-flops from MSB to LSB.

In each clock cycle, one of the outputs in the counter sets a flip-flop in the code register. The output of this flip-flop which is set by the counter is used as the clock signal for the previous flip-flop. At rising edge of the clock, this flip-flop loads the result from the comparator [21]. Fig. 4.15 shows the SAR logic design.

4.2.2 Flip-flops

In this work D-type flip-flops are used as memory elements. Basically a set-reset (SR) structure containing master-slave latches is used as seen in Fig. 4.14.

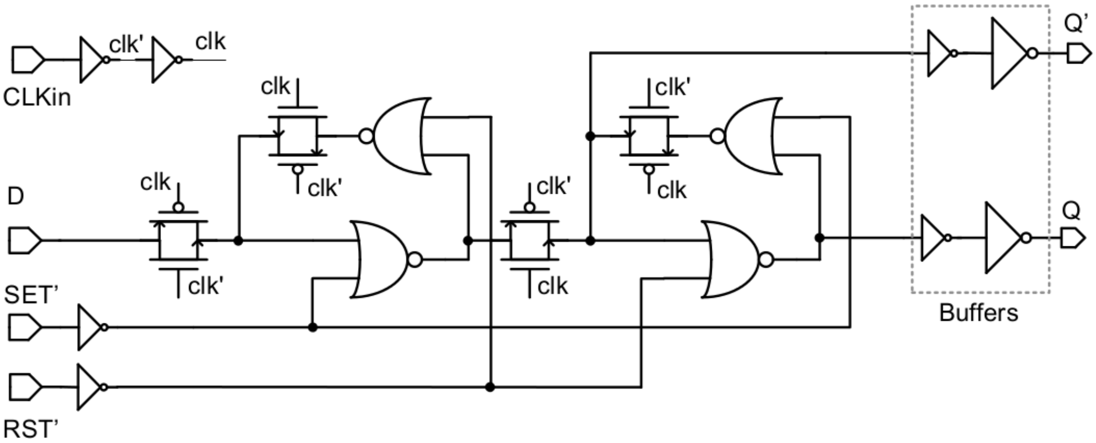

Figure 4.14: Designed flip-flop structure.

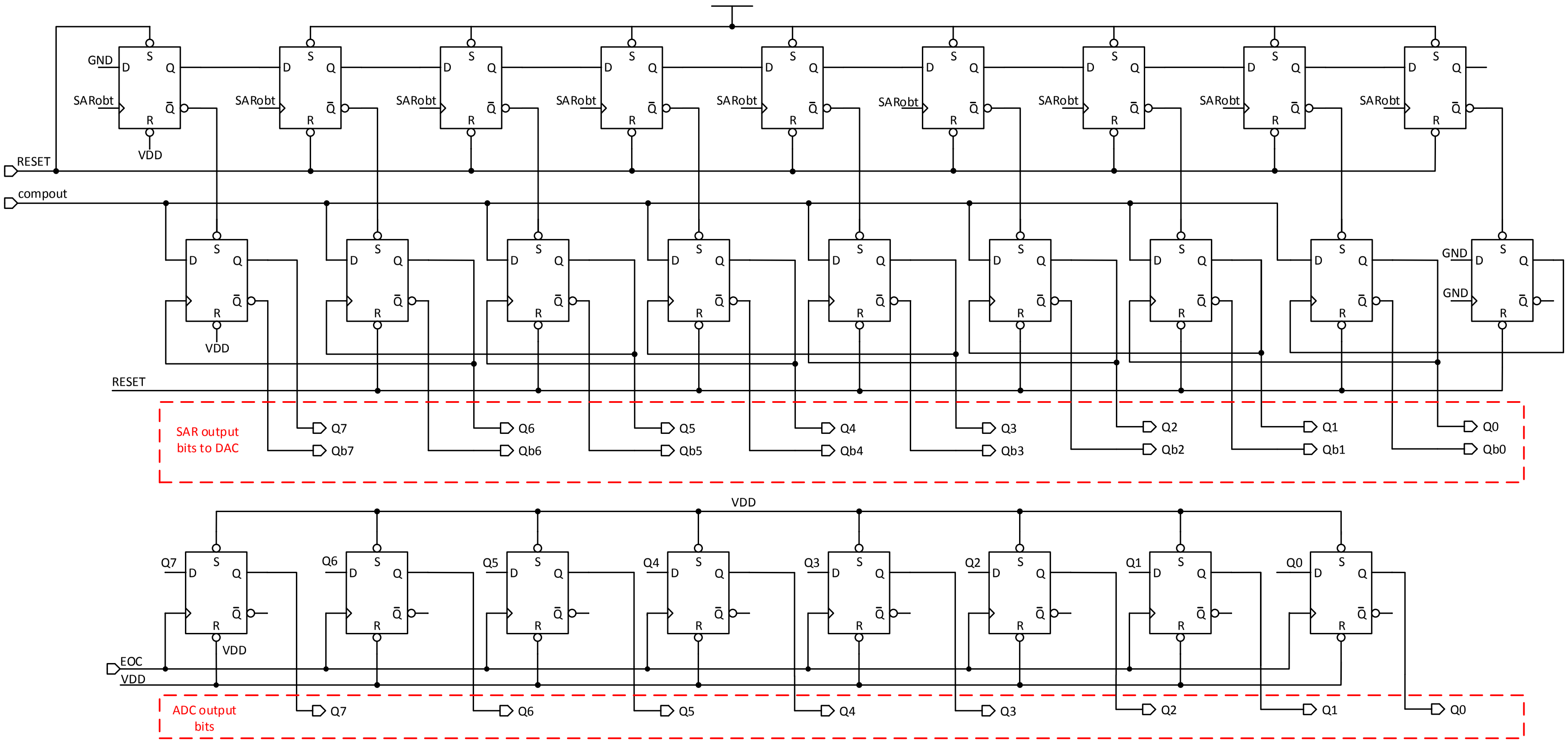
GND
SARobt
RESET
VDD
compout
RESET
SAR output
bits to DAC
Q7
Qb7
Q6
Qb6
Q5
Qb5
Q4
Qb4
Q3
Qb3
Q2
Qb2
Q1
Qb1
Q0
Qb0
VDD
EOC
ADC output
bits
D
S
Q
Q̄
R

Figure 4.15: Designed SAR logic structure.

It works as follows: While clock is low, master latch follows the input, slave latch holds its previous value. At the rising edge of clock master latch holds input's last value, the slave latch updates output to that value and holds it until next rising edge of clock. Set and reset functions are independent of the clock signal.Active low set signal sets the output to logic high, active low reset signal clears output to logic low immediately.

4.2.3 Test results

Test benches for flip-flop and SAR logic block are presented in Fig. 4.16 and Fig. 4.20 respectively.

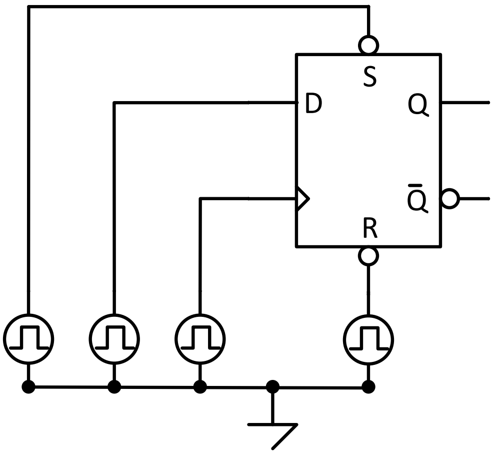

Figure 4.16: Flip flop test bench.

When testing flip-flops, data is given by a pwl source or an ideal random bit generator. Flip-flop input-output graph is presented in Fig. 4.17. It is obvious that flip flop gives expected responses to the input data, clock, set and reset signals. Q (and Qb) output changes as expected with the rising edges of the clock, according to the input data D; and get SET to '1' (RESET to '0') and/or RESET to '0' (SET to '1') with low 'Sb' and 'Rb' accordingly regardless of input data 'D'.

In order to test flip-flop's setup time a step input is applied. Clock signal is shifted in the neighborhood of transition point of the input step, The first clock which triggers the output of the flip-flop to toggle state is the clock signal to measure the setup time. As seen in Fig. 4.18, setup time of the flip-flop is measured as 140*ps*.

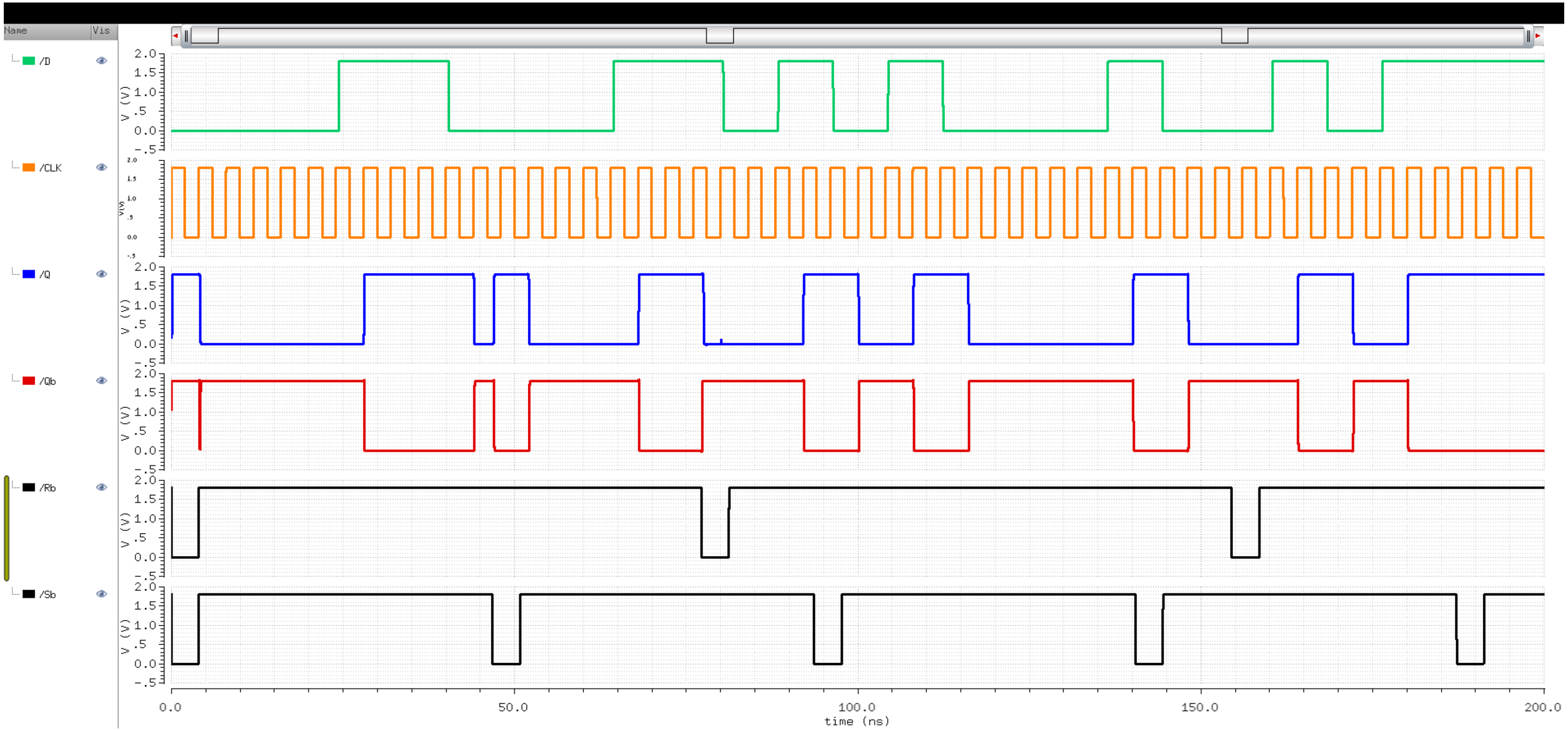

Figure 4.17: Input-output relation of the designed flip-flop.

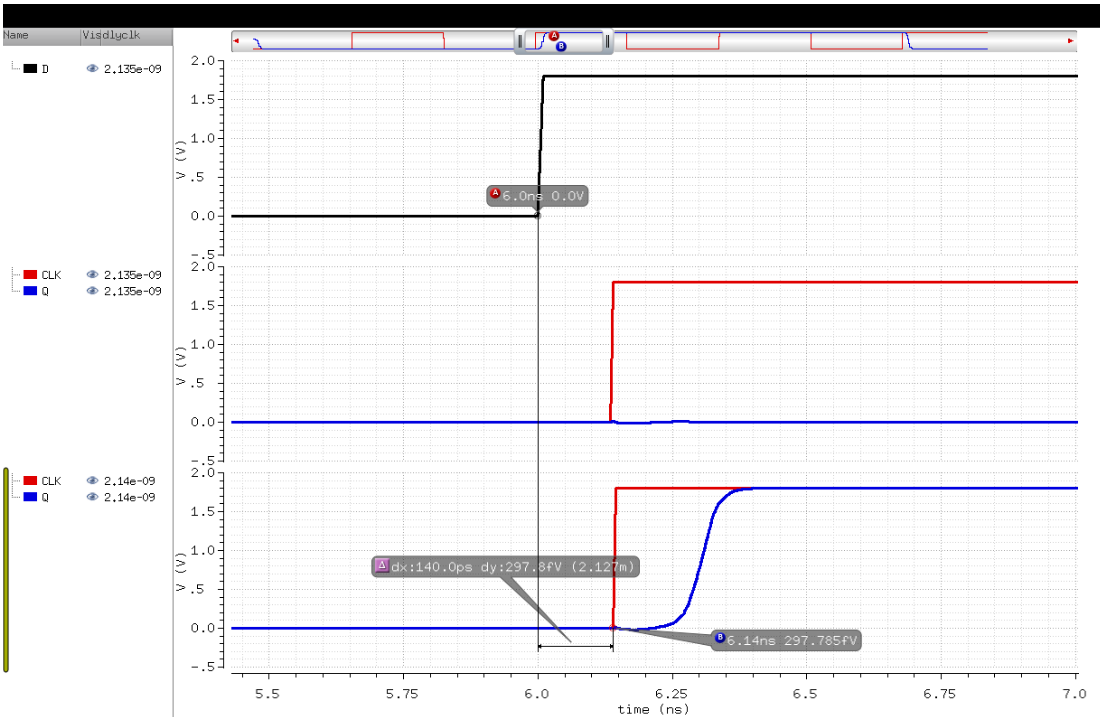
Name
Visdlyclk
D
2.135e-09
CLK
Q
2.135e-09
2.135e-09
CLK
Q
2.14e-09
2.14e-09
6.0ns 0.0V
dx:140.0ps dy:297.8fV (2.127m)
6.14ns 297.785fV
V (V)
2.0
1.5
1.0
.5
0.0
-.5
5.5
5.75
6.0
6.25
6.5
6.75
7.0
time (ns)

Figure 4.18: Flip flop setup time.

Hold time is measured similarly. Clock signal is swept around the input data transition point and now the last clock signal which keeps the output unchanged is the clock to measure the hold time. As seen in Fig. 4.19, hold time of the flip-flop is measured as 135*ps*.

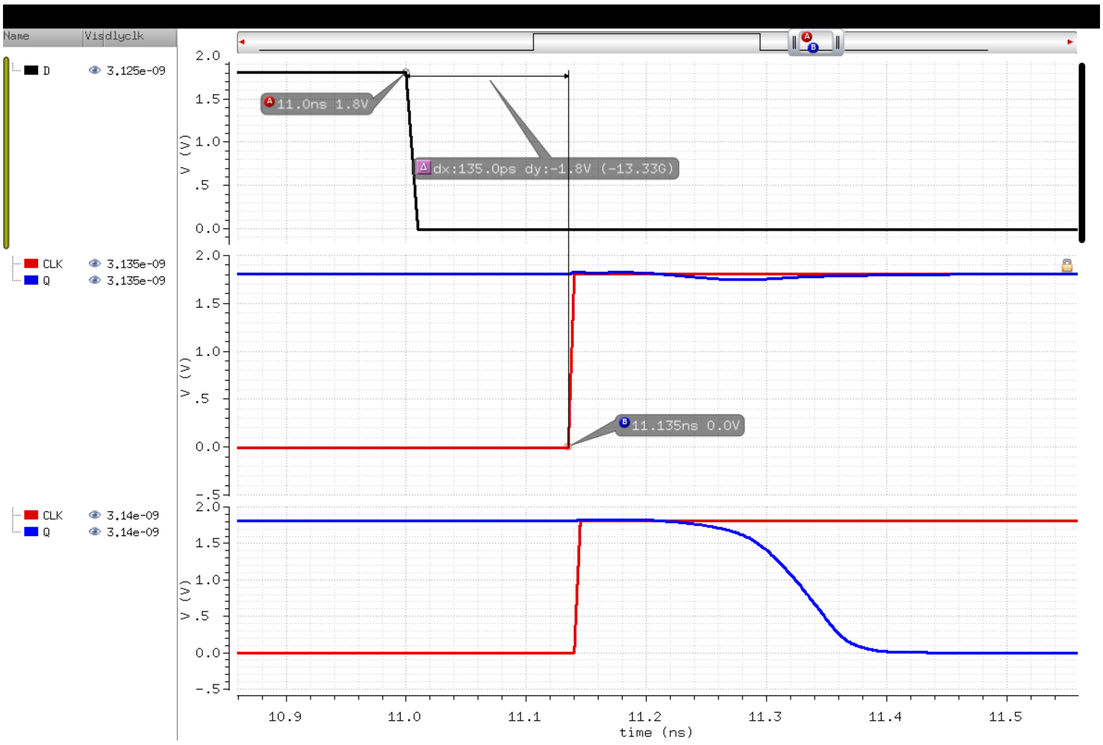
Name
Visdlyclk
D
3.125e-09
CLK
Q
3.135e-09
3.135e-09
CLK
Q
3.14e-09
3.14e-09
11.0ns 1.8V
dx:135.0ps dy:-1.8V (-13.33G)
11.135ns 0.0V
V (V)
2.0
1.5
1.0
.5
0.0
-.5
10.9
11.0
11.1
11.2
11.3
11.4
11.5
time (ns)

Figure 4.19: Flip flop hold time.

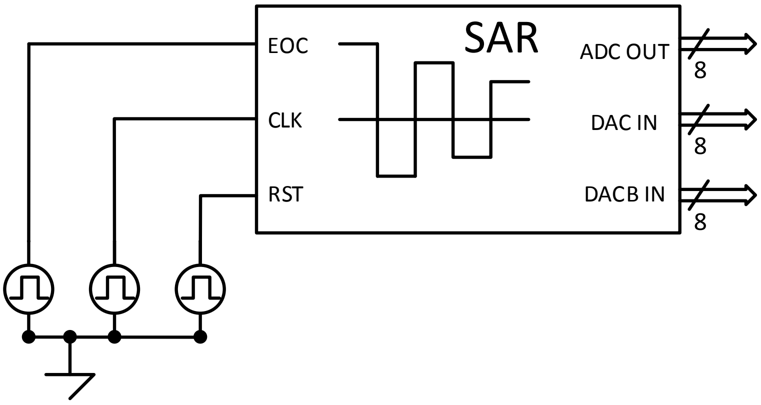

Figure 4.20: SAR test bench.

Testing SAR logic is something like testing and semi-ideal SAR ADC which the only real part is the logic. A pseudo-comparator should be included in the test bench which gives digital level voltages as an input to the SAR block as the situation in the ADC operation. This pseudo-comparator can be a simple DC voltage source, or the data input even can be shorted to VDD or GND to easily see the successive operation of the logic. In Fig. 4.21 data input is grounded to test if SAR logic gives a all zeros output as the semi-ideal ADC model. As seen in Fig. 4.21, the SAR output bits controlling DAC, get high, wait for the result of the pseudo-comparator, since this result is always a ‘0’ in this setup, get low again, starting from the MSB all the way down to the LSB. At last, with the rising edge of the ‘ADC output ready’ clock (CKO) the outputs of the semi-ideal ADC (which are all zeros in this setup) are loaded to the bottom shift register and hold until the next CKO rising edge. It is obvious that all the bits to DAC get high, and then get low back, and after CKO rises the ADC output bits (DATA<7:0>) become all zeros.

Second situation is to connect the data input of the SAR to VDD as a pseudo-comparator and the results are observed as in Fig. 4.22. Similar situation occurs here. The bits controlling DAC get high and since the pseudo-comparator continuously sends ‘1’s, they stay at high. At the end, when CKO rises, the semi-ideal ADC gives all ‘1’s as output word.

SAR logic is tested in PVT corners of (SS, TT, FF, 1.71V, 1.8V, 1.89V, -40 °C, 0 °C, 27 °C, 85 °C, 105 °C, 125 °C) and seen that it works properly up to 1 GHz frequency which is far beyond our ADC’s frequency which is $20MS/s \cdot 9 = 180MHz$.

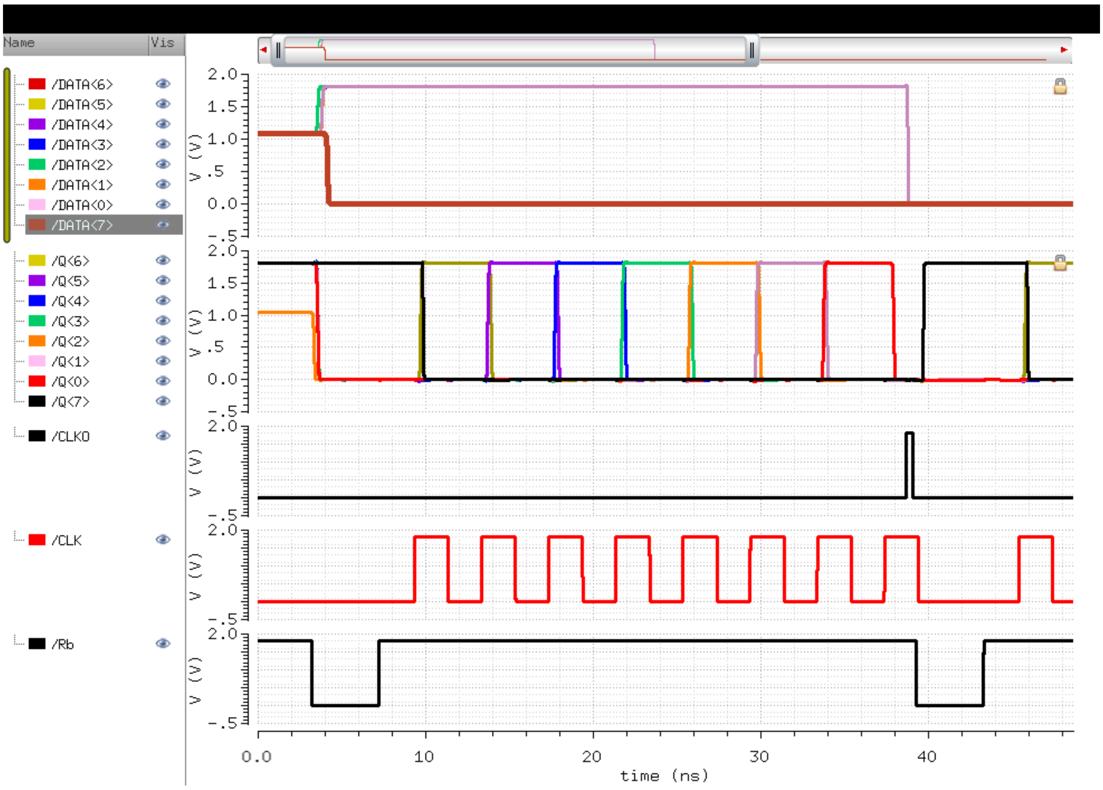

Figure 4.21: SAR out graph for all ‘0’ data input.

4.3 Digital to Analog Converter

Digital to Analog Converter (DAC), as the name implies, converts an array of digital bits into an analog voltage.

DAC plays a major role in SAR ADC. It converts the bits coming from the SAR logic block to an analog voltage, which will then be compared to the ADC analog input voltage by the comparator. Since linearity of the ADC highly depends on the linearity of the DAC, it should be designed carefully.

4.3.1 Designed DAC Architecture

Switched capacitor array DACs are well known for their low power operation. Since they are based on the charge scaling scheme, their power dissipation is very low in comparison with the counterpart architectures. The basic architecture of charge scaling DACs is the one with binary weighted capacitors reported in [22], and can be seen in Fig 4.23.

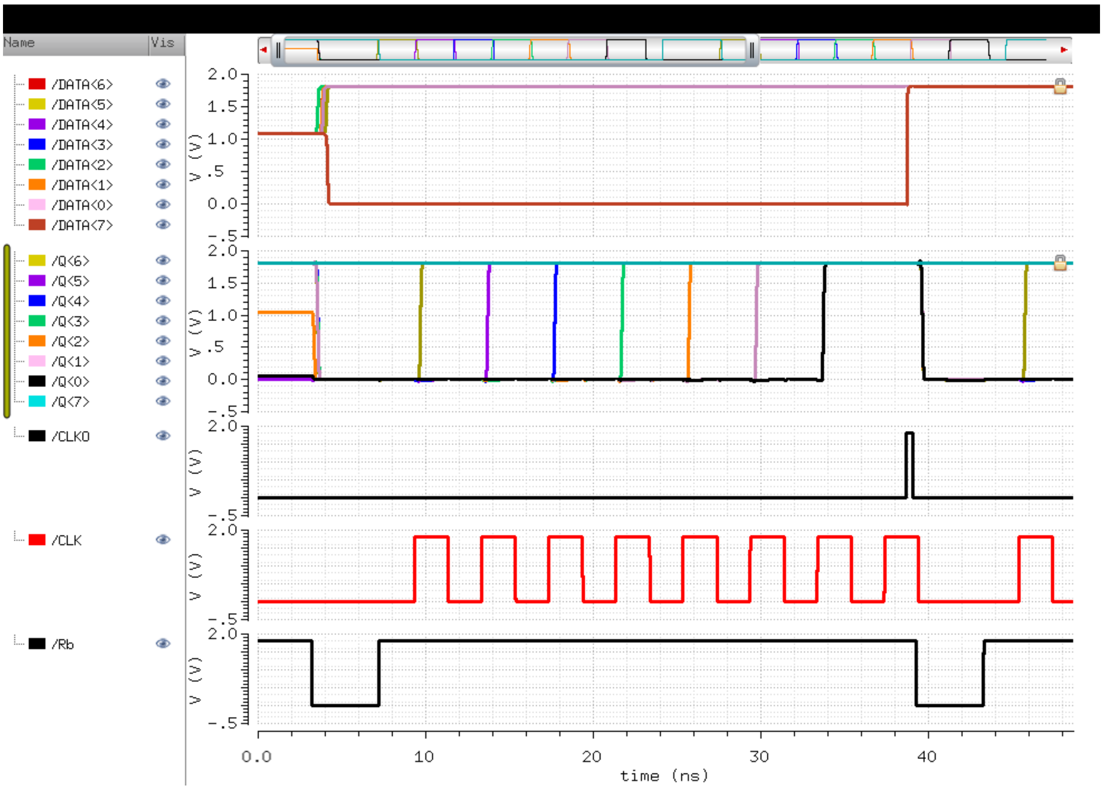
Name
Vis
/DATA<6>
/DATA<5>
/DATA<4>
/DATA<3>
/DATA<2>
/DATA<1>
/DATA<0>
/DATA<7>
/Q<6>
/Q<5>
/Q<4>
/Q<3>
/Q<2>
/Q<1>
/Q<0>
/Q<7>
/CLK0
/CLK
/Rb
V (V)
2.0
1.5
1.0
.5
0.0
-.5
0.0
10
20
30
40
time (ns)

Figure 4.22: SAR out graph for all ‘1’ data input.

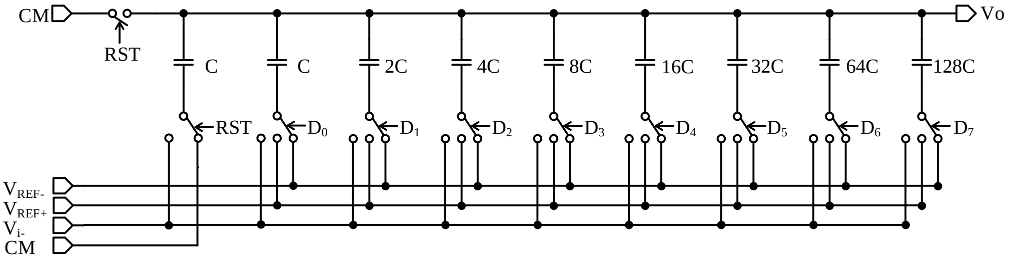
CM
RST
C
C
2C
4C
8C
16C
32C
64C
128C
Vo
RST
D0
D1
D2
D3
D4
D5
D6
D7
VREF-
VREF+
Vi-
CM

Figure 4.23: Binary weighted capacitor array DAC.

Besides the low power operation, this architecture has an important disadvantage: The more number of bits the DAC has, the larger capacitors are needed. Moreover, for each addition of bit the need for the capacitance doubles. For example, a DAC with n bits can be designed using a total capacitance of

$$\begin{aligned} C_{total} &= (1+1+2+4+\cdots+2^{n-1})\cdot C \\ &= 2^n \cdot C \end{aligned} \tag{4.8}$$

where C_{total} is the total capacitance, and C is the unit capacitance of the DAC array.

So, it is not practical to implement DACs with more than 4-5 bits as binary weighted switched capacitor array.

An elegant solution to this problem is reported in [23]. The binary weighted capacitor array is divided into two sub-sections and an attenuation capacitor is presented between these stages. This way, the need for the largest and the total capacitance values are lowered drastically.

DAC in this work is designed as two equal sections binary weighted switched capacitor array DAC in order to keep power consumption and the total capacitance low. A block diagram of de designed DAC is presented in Fig. 4.24.

The design criteria in this architecture is to decide the value of the attenuation capacitor so that the equivalent capacitance seen by the MSB bank of the DAC is equal to the unity capacitance, in order to use it as a termination capacitance. This is assured by selecting the attenuation capacitance value correctly, keeping in mind that it is connected in series with the all parallel LSB bank capacitors. So, the attenuation capacitance value can be calculated as

$$\begin{aligned} C_T = C &= (C+C+2C+4C+8C) \sim C_A \\ &= \frac{(C+C+2C+4C+8C)\cdot C_A}{C+C+2C+4C+8C+C_A} \\ \Rightarrow C_A &= \frac{16}{15}\cdot C \end{aligned} \tag{4.9}$$

where C_T is the termination capacitance for the MSB bank, C_A is the attenuation capacitance and C is the unit capacitance.

The total capacitance in the array can be calculated as

$$\begin{aligned} C_{total} &= C_T + C_{MSB} \\ &= C+C+2C+4C+\cdots+2^{(n/2-1)}C \\ \Rightarrow C_{total} &= 2^{n/2}C \end{aligned} \tag{4.10}$$

where C_{MSB} is the total capacitance in the MSB bank. As seen from Eq. (4.8) and (4.10), the total capacitance is decreased to half by using an attenuation capacitor.

4.3.1.1 Sample and hold (S/H) operation

DAC capacitor array is also used as a sample and hold circuit for the ADC operation in order to lower circuit complexity and remove the need for an extra S/H circuit which was proposed in [22].

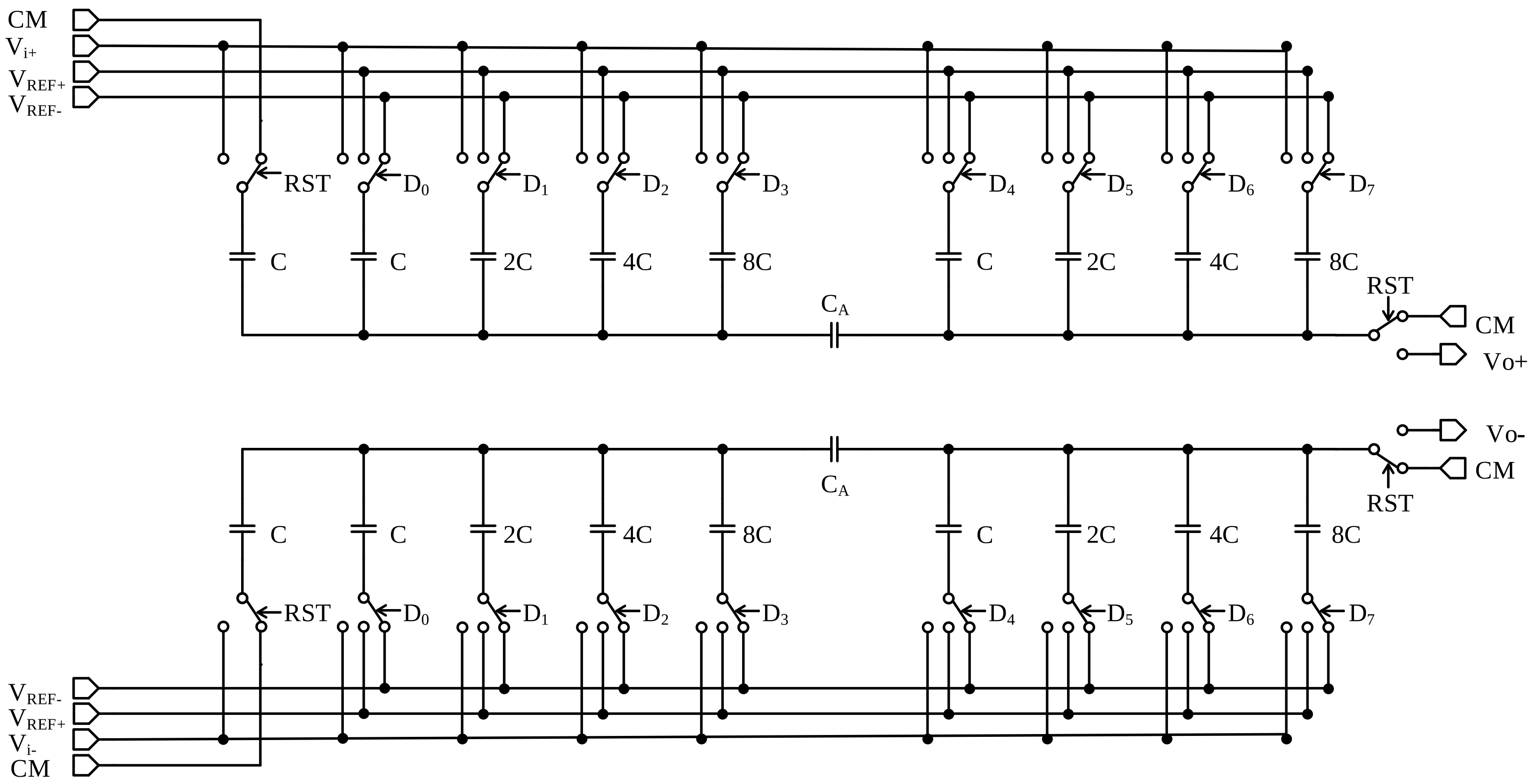
CM
V_{i+}
V_{REF+}
V_{REF-}
RST
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
C
C
2C
4C
8C
C
2C
4C
8C
C_A
RST
CM
Vo+
Vo-
CM
RST
C_A
C
C
2C
4C
8C
C
2C
4C
8C
RST
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
V_{REF-}
V_{REF+}
V_{i-}
CM

Figure 4.24: Designed DAC structure.

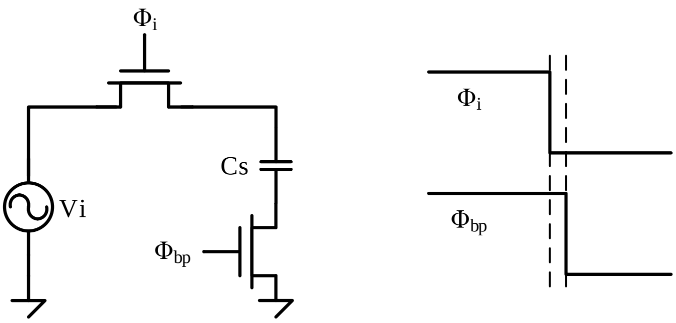

Figure 4.25: Equivalent circuit of the DAC capacitors while ADC is in input sampling (S/H) mode.

The technique provides an inherent sample and hold function and can accept both polarities of inputs. By using this technique, we combine sample and hold block with DAC block, meaning a gain in area requirement. This operation will be discussed in ADC operation chapter.

Equivalent circuit of the capacitor array in S/H operation mode is as in Fig. 4.25.

Selecting switch and capacitor sizes is based on the operation of S/H mode. Total capacitance must be large enough to tolerate the thermal noise and small enough to produce a small $\tau = RC$ time constant along with the $R_{ON} = R_{ON,in} + R_{ON,bp}$ on resistance of the ADC input sampling switches plus the bottom plate sampling switch which are in series. It is obvious that the switch R_{ON} should also be as low as possible to form a low RC time constant.

Thermal noise consideration

Thermal noise is also known as Johnson-Nyquist noise originates from the thermal excitation of electrons in a conductor at non-ideal world (non-zero temperature). Thermal noise can be expressed as in Eq. (4.11) for a sampled data system [7].

$$\overline{v_n^2} = \frac{kT}{C} \tag{4.11}$$

According to Eq. (4.11), noise power increases with increasing temperature and decreasing sampling capacitance. The capacitor value should be selected large enough so that the noise voltage at the desired temperature range stays below half LSB. Since LSB for the designed DAC is 3.9 mV for each branch,and the maximum temperature it is expected to operate is 125 °C(=398 °K), the minimum capacitor value to be used can be calculated as

$$\begin{aligned}(0.5 \cdot 3.9 \cdot 10^{-3})^2 &= \frac{1.38 \cdot 10^{-23} \cdot 398}{C} \\ \Rightarrow C &= 1.444 fF\end{aligned} \tag{4.12}$$

which is needed to overcome the thermal noise while operating. It is obvious that the thermal noise is not a big issue for 8-bit operation, since the capacitance values are most likely selected larger than the thermal noise minimum because of technological reasons as matching.

Settling time considerations

DAC forms an RC network while in ADC input sampling mode. When a capacitor is charged to an input voltage through a non-ideal switch, a certain time is needed for the capacitor to settle to that input voltage with a certain precision. This time is defined as ‘settling time’. Maximum sampling frequency of ADC is mainly limited by the settling time of the switched capacitor network (i.e. S/H circuit). Settling time can be calculated as in Eq. (4.15) going through

$$V_c = V_{in} \cdot (1 - e^{-t/\tau}) \tag{4.13}$$

where

$$\tau = R_{on} \cdot C \tag{4.14}$$

obtaining settling time t as

$$t = \ln\left(\frac{V_c}{V_{in}}\right)\tau \tag{4.15}$$

Time needed for an RC network to settle to an analog input voltage with a precision of 8-bit can be obtained as

$$\begin{aligned}t &= \ln\left(\frac{1}{1/(2^8 - 1)}\right)\tau \\ t &= 5.5\tau\end{aligned} \tag{4.16}$$

According to this result, to reduce the settling time both the switch on resistance and the sampling capacitance should be selected as low as possible. In order not to face problems with matching, especially with the attenuation capacitor which has a fractional value, a $50fF$ unit capacitance value is selected. This makes the sampling capacitance $0.8pF$ for each branch of the capacitor network. For a starting point, selecting $R_{ON} = 1k\Omega$ results with a settling time of

$$\begin{aligned} t &= 5.5\tau = 5.5 \cdot R \cdot C \\ &= 5.5 \cdot 1 \cdot 10^3 \cdot 0.8 \cdot 10^{-12} \\ \Rightarrow t &= 4.4ns \end{aligned} \tag{4.17}$$

This result seems too much, because it will limit the speed of the ADC. Lowering settling time down to $3.5ns$ which allows the input sampling phase of ADC to be fast enough, so that ADC operation can be finished in 9 clock periods, one of which is sampling (reset) phase. For that reason, a sampling switch with maximum on resistance of $R_{ON} = 800\Omega$ should be designed to satisfy settling time requirement, which results a settling time of $3.52ns$.

ADC input bandwidth considerations

This thesis work, as stated earlier, is intended to design a sub-ADC to use to design a GS/s range time interleaved ADC. For such high sampling rates, the ADC input sampler should have large bandwidth.

ADC input sampler forms a low pass filter as seen in Fig. 4.25. Bandwidth of a low-pass filter is calculated by the formula of

$$BW = \frac{1}{2\pi RC} \tag{4.18}$$

So in order to have a $1GHz$ bandwidth, on resistance of the input switch in series with the bottom plate sampling switch can be calculated as

$$\begin{aligned} 1 \cdot 10^9 &= \frac{1}{2\pi R_{ON} \cdot 0.8 \cdot 10^{-12}} \\ \Rightarrow R_{ON} &= 198.94\Omega \end{aligned} \tag{4.19}$$

Eq. (4.19) declares that the total resistance in the input sampler (R_{ON}) should have a maximum value of $\sim 200\Omega$. Since this requirement for R_{ON} is more strict that the one for the settling, switches must be designed so that $R_{ON,max} = 200\Omega$.

Sampling switches

Sampling switches are designed as 'transmission gate's in order to have a small on resistance, so, to be able to sample both the lower and higher regions of the analog input voltage swing. To improve the dynamic range, sampling switches are implemented with 3.3V transistors. A figure of designed sampling switch is presented in Fig. 4.26.

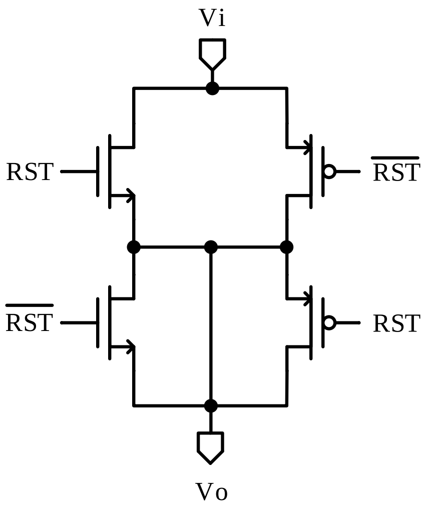

Figure 4.26: Analog input sampling switch.

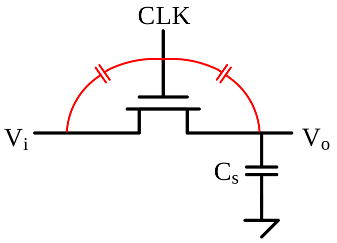

Figure 4.27: Overlap capacitors causing clock feed-through.

Error mechanisms effecting the switches are clock feed-through and charge injection. Clock feed-through is an effect caused by the overlap capacitors of gate-to-source and gate-to-drain. The switch control clock is fed through the overlap capacitors onto the sampled input voltage. Since this voltage is not input dependent, its effect is seen as an offset voltage at the end. Overlap capacitors of a sampling network is presented in Fig. 4.27.

More important effect is the charge injection. Charge injection occurs when the transistor goes to OFF state from ON state. When a transistor is in ON state, a channel is formed between source and drain, and a current flows through this channel. When the transistor goes to OFF state, that channel disappears. Charge in the channel is forced leave the channel and move through source and/or drain terminal of the transistor. This effect is too complex to be modeled adequately but it is assumed that this charge injection is shared more or less equally between source and drain terminals.

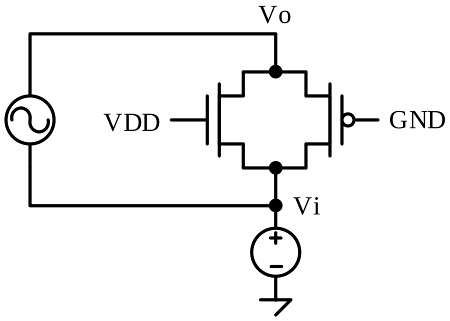

Figure 4.28: switch R_{ON} test bench.

Keeping this assumption in mind, an easy way to tolerate charge injected onto the sampled analog input voltage, a second transistor half in dimension can be connected in series with the main switch, source and drain terminals shorted, and clocked inversely. This way while the channel of the switch is disappearing channel of the serial transistor is forming, and pulling the charge injected from the switch to form its channel.

By selecting half width of the original switch for the dummy transistor, a large portion of the charge injection is canceled. Another solution to these problems is to use bottom plate sampling scheme. As seen in Fig. 4.25, an additional switch is put between sampling capacitor and ground, and that bottom plate switch is turned off and bottom plate of the sampling capacitor is left floating slightly before the sampling switch so that channel charge of sampling switch is not injected onto the sampling capacitor when sampling switch gets off.

At the end, it is obvious that total resistance of the bottom plate and top plate sampling switches, which are connected in series, should be below 200Ω as calculated in Eq. (4.19). So, the on resistance for each should be 100Ω at most.

Since the switch is input voltage dependent, a test bench of Fig. 4.28 is used to simulate maximum on resistance of the switch between $0-3.3V$ input range. Input voltage is swept from $0V$ up to $3.3V$ and the on resistance is simulated with AC analysis.

The input sampling switch is actually a combination of 16 parallel switches. So, it is sufficient if each of these parallel switches has an on resistance of $1.6k\Omega$. A figure of R_{ON} across the full scale voltage range can be found in Fig. 4.29. Switch on resistances are selected so that they have a margin to pass the corners simulations too. A result of

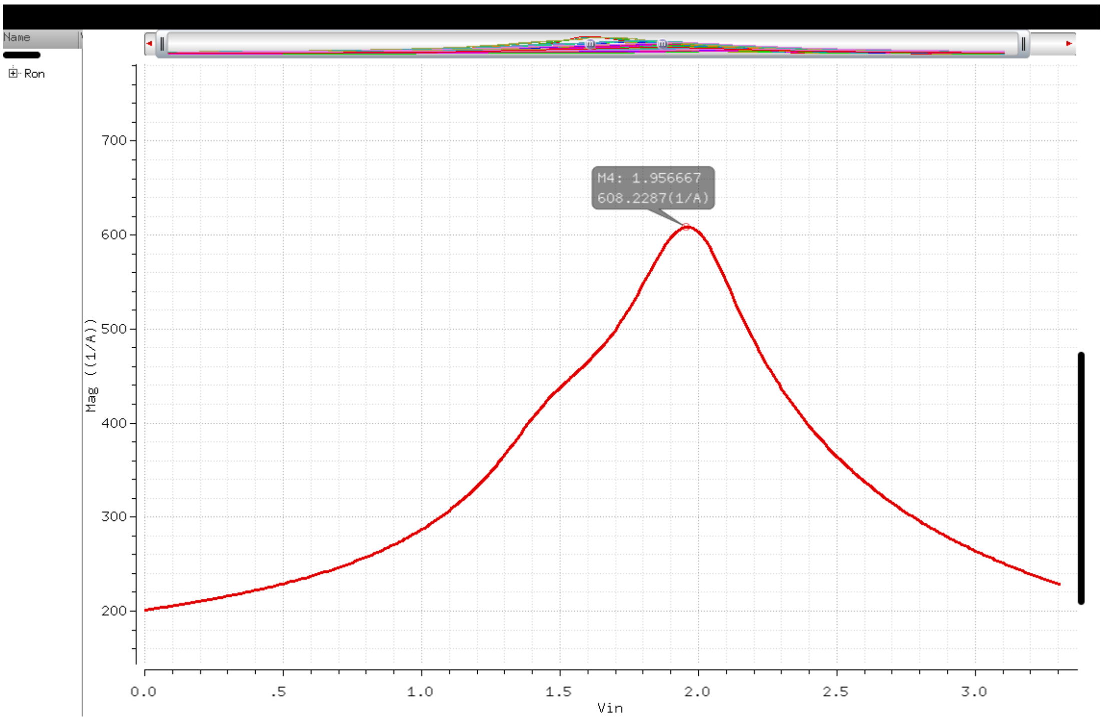

Figure 4.29: Input sampling switch R_{ON}.

PVT corners simulation is available in 4.30. Since SS corner is rare, having a slightly larger resistance is not considered as a big problem at that corner.

Reference voltage switches can be considered as the same manner as the input sampling switches. Since each switch sees a unit capacitance, reference switches are designed with the same R_{ON} as the input sampling switches.

Simulation results for the on resistance of the bottom plate sampling switch, at nominal and PVT corners are also presented in Fig. 4.31 and 4.32 respectively.

4.3.1.2 Reference voltage buffers

Reference voltages of the DAC are planned to be produced by band-gap reference voltage generators. In order that these generated voltages can be driven into massively paralleled ADCs, their driving capabilities must be enhanced. Reference voltage buffers are therefore designed.

Two kinds of buffers are designed. One for negative reference and common mode voltage and one for the positive reference voltage.

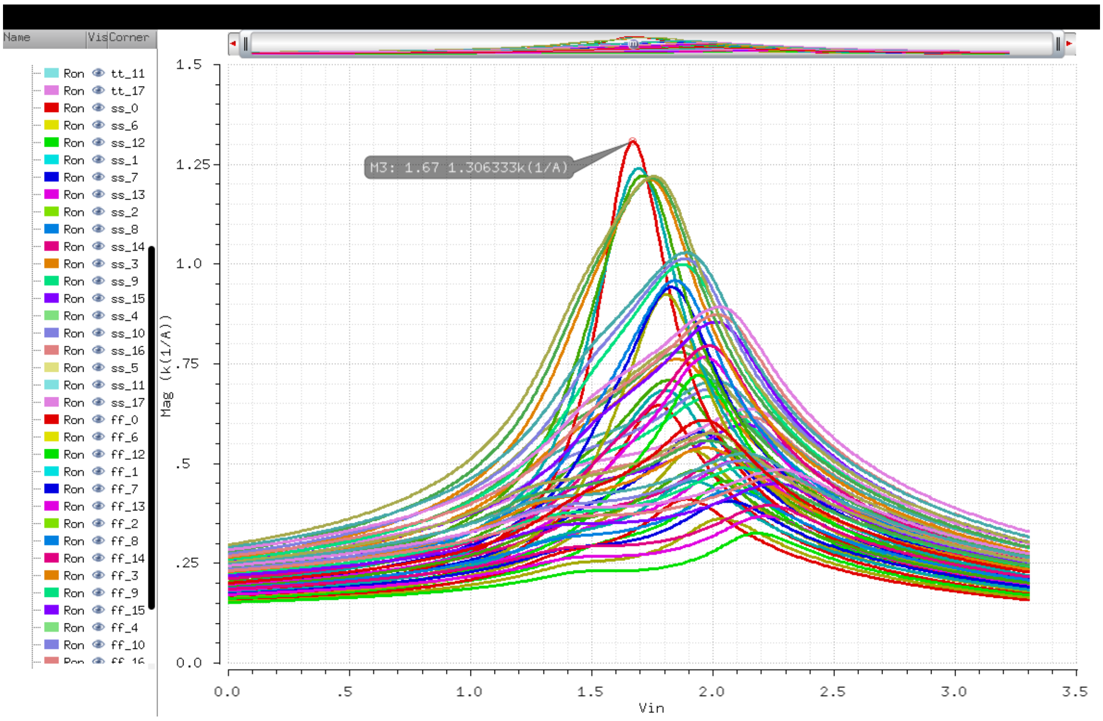

Figure 4.30: Input sampling switch R_{ON} across PVT corners.

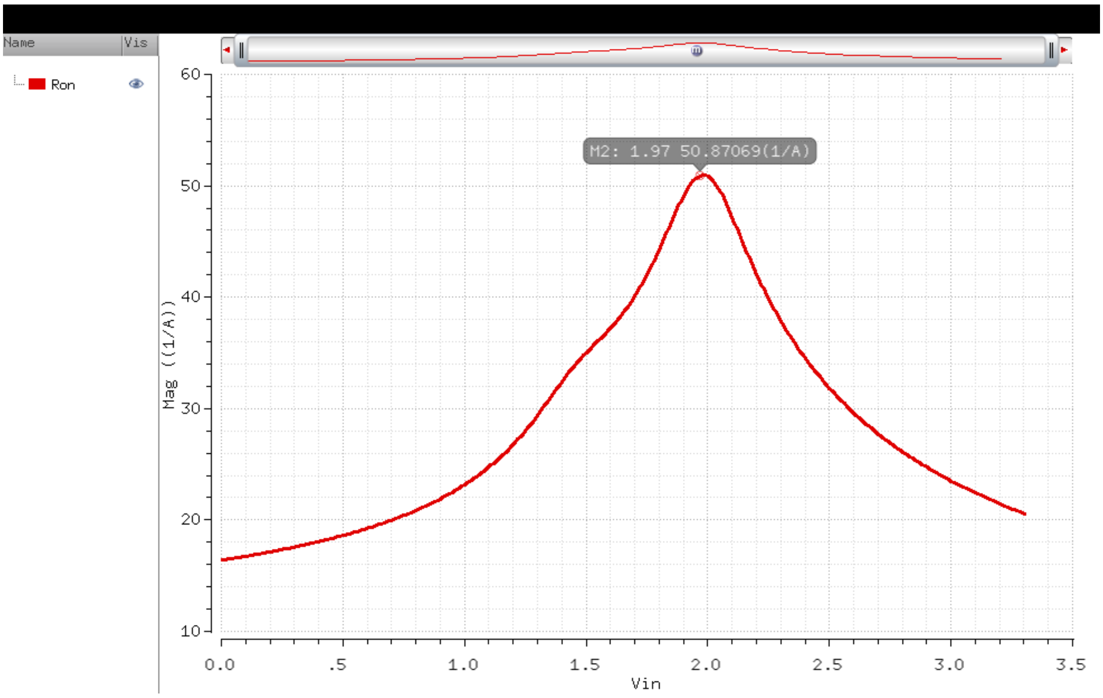

Figure 4.31: Bottom plate switch R_{ON}.

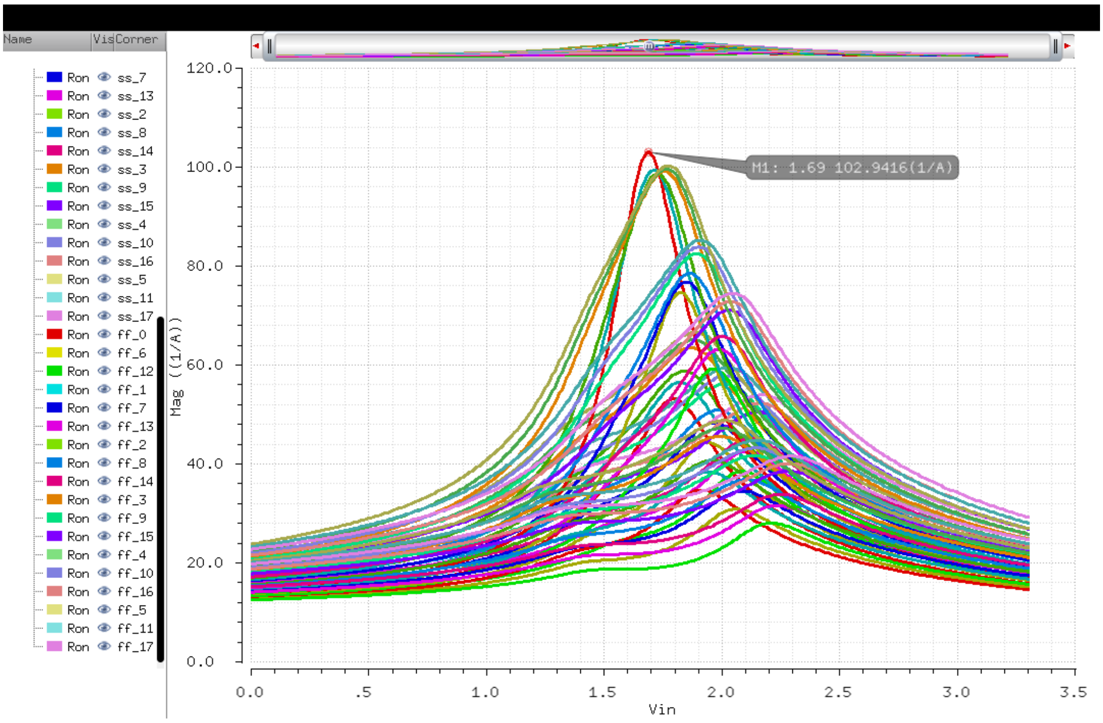

Figure 4.32: Bottom plate sampling switch R_{ON} across PVT corners.

Vref- and Vcm buffer

This buffer is designed as a high speed, moderate gain PMOS input differential pair folded cascode operational amplifier. Since the output of the opamp needs to settle quickly, tail current needs to be really high. A figure of designed PMOS input opamp is presented in Fig. 4.33.

The opamp is tested using the test-bench seen in Fig. 4.34.

PMOS input opamp settling time simulation result is presented in 4.36.

Vref+ buffer

This buffer is also designed as a high speed, moderate gain, but now, NMOS input differential pair folded cascode operational amplifier. Since the output of the opamp needs to settle quickly, tail current needs to be really high. A figure of designed NMOS input opamp is presented in Fig. 4.37.

The opamp is tested using the same test-bench as the PMOS input opamp. Only the input voltage level is changed accordingly.

NMOS input opamp settling time simulation result is presented in 4.39.

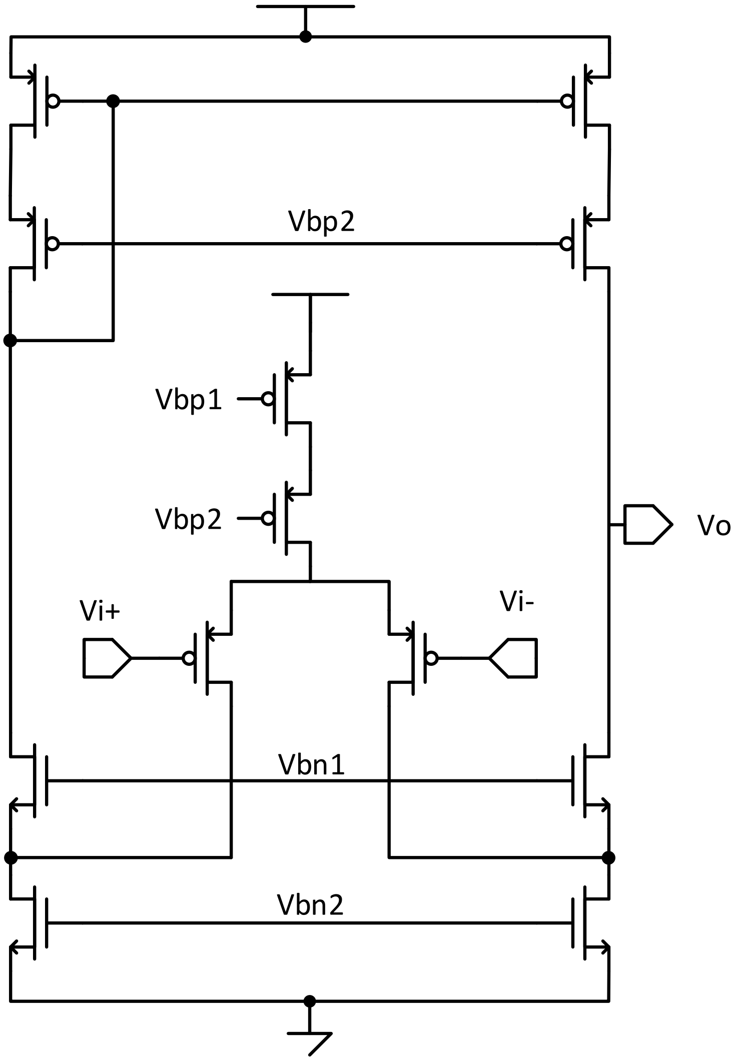
Vbp2
Vbp1
Vbp2
Vo
Vi+
Vi-
Vbn1
Vbn2

Figure 4.33: Vref- and Vcm buffer opamp schematic.

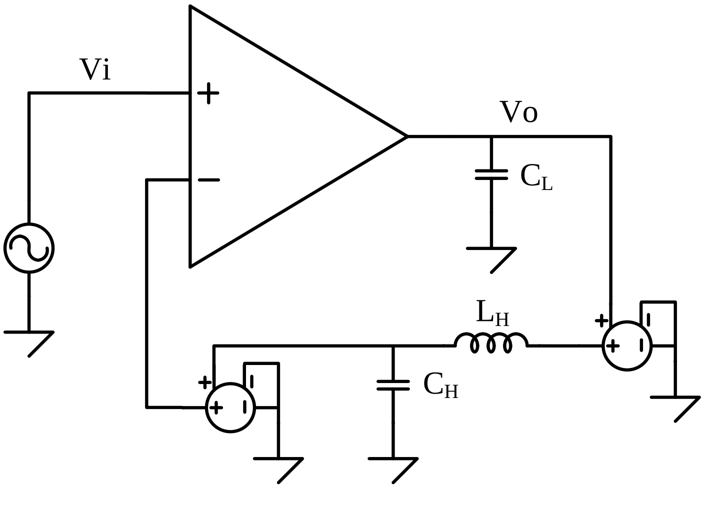
Vi
+
−
Vo
C_L
L_H
C_H

Figure 4.34: Opamp test-bench.

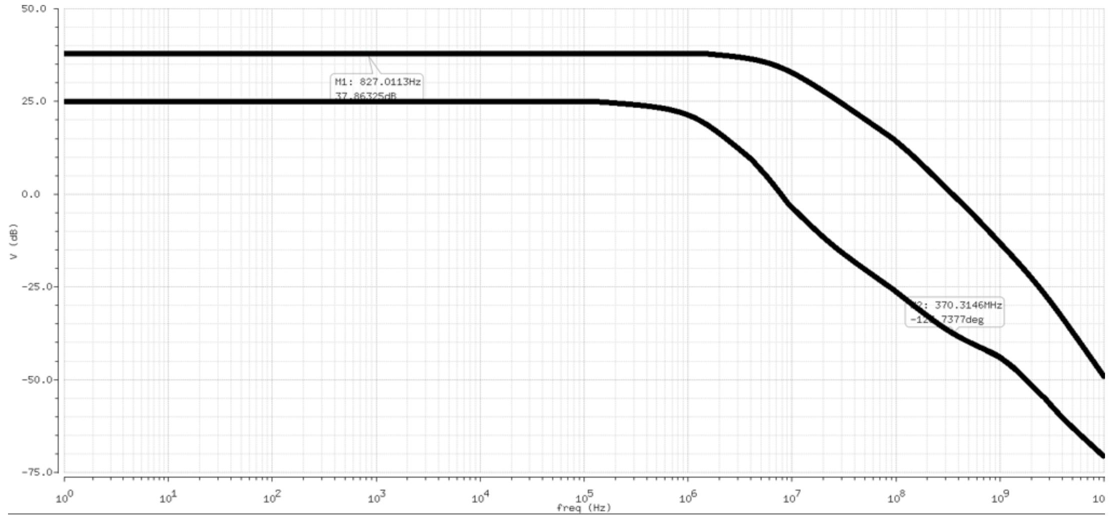

Figure 4.35: PMOS input opamp gain.

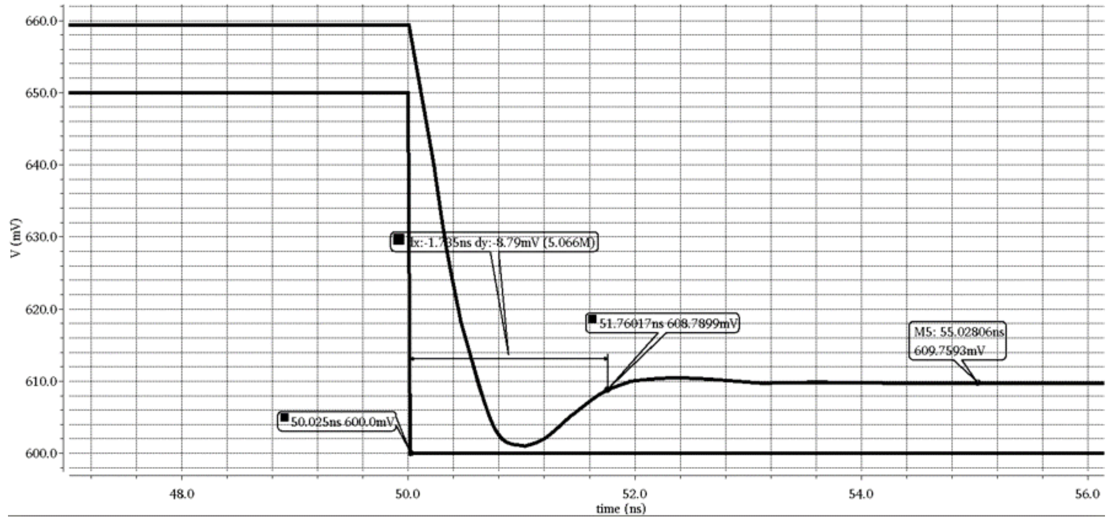

Figure 4.36: PMOS input opamp settling time.

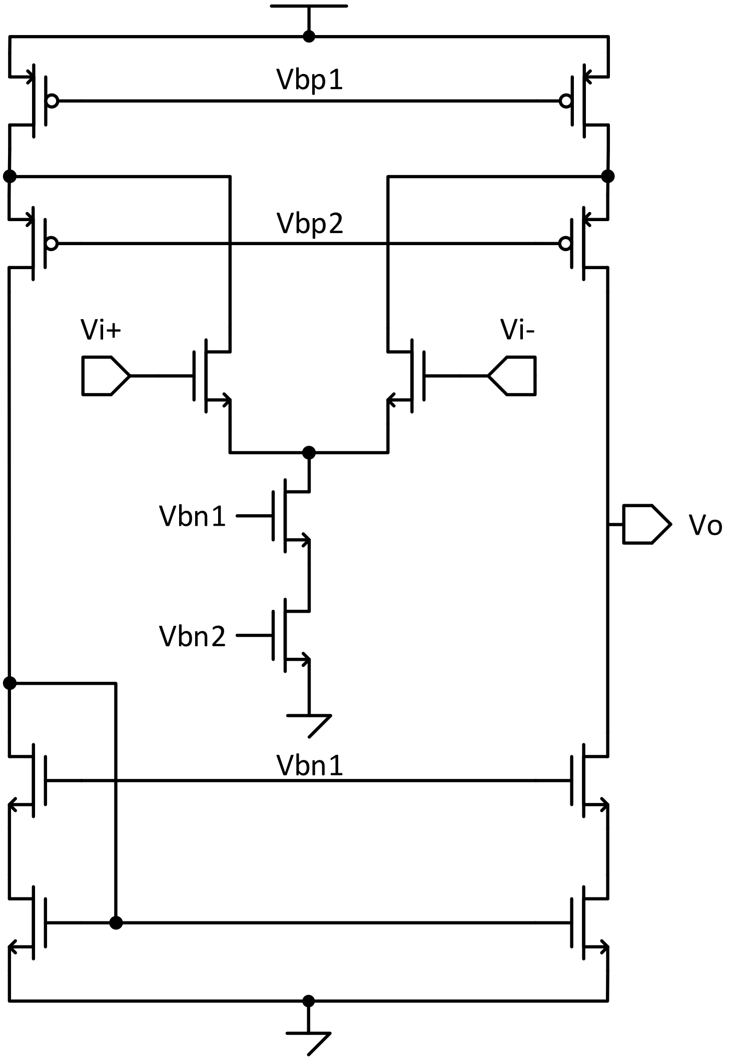
Vbp1
Vbp2
Vi+
Vi-
Vbn1
Vbn2
Vo
Vbn1

Figure 4.37: Vref+ buffer opamp schematic.

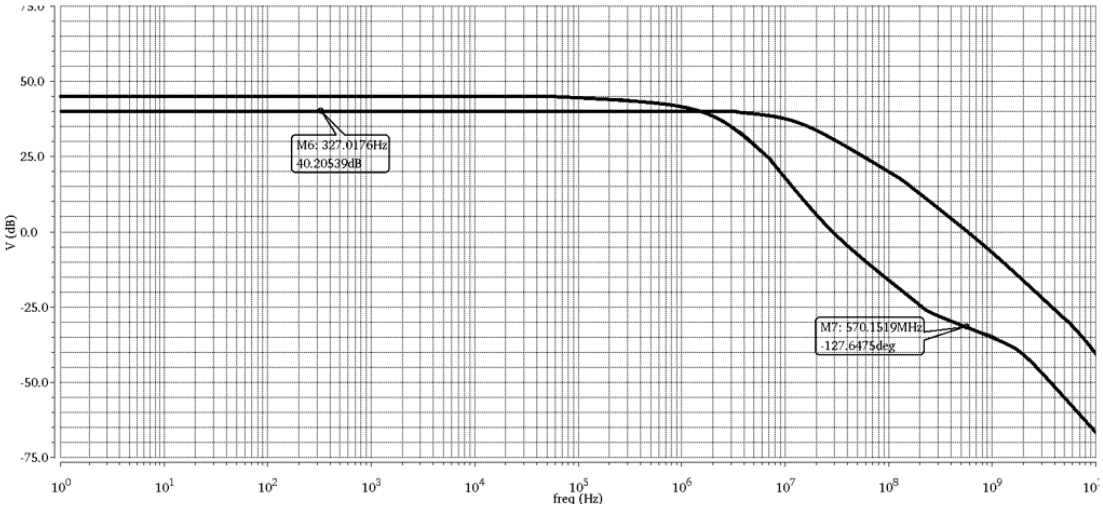

Figure 4.38: NMOS input opamp gain.

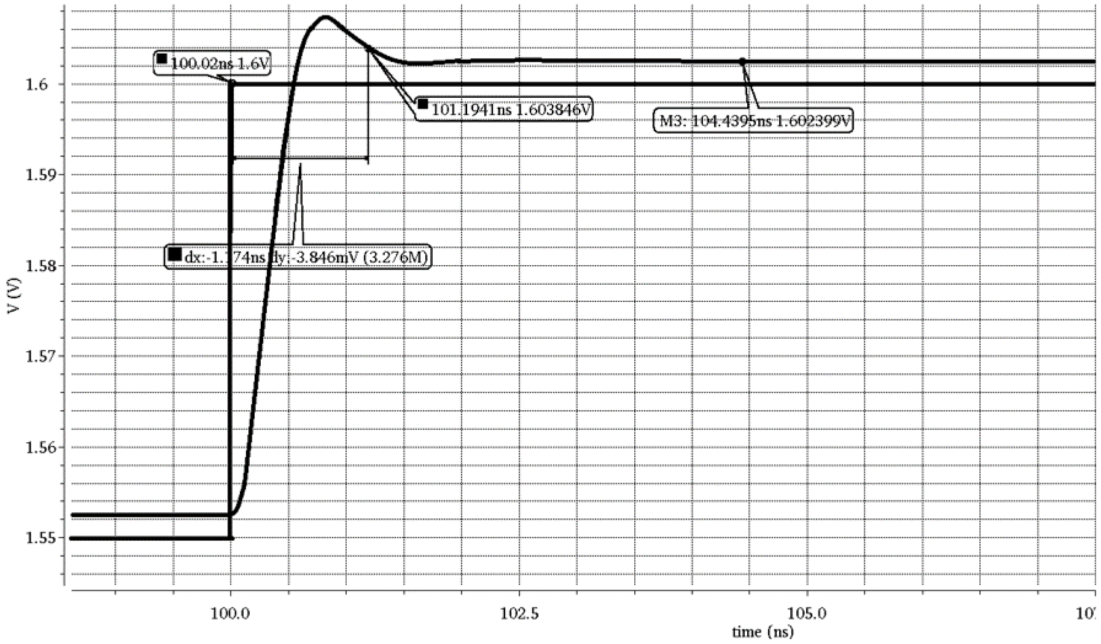

Figure 4.39: NMOS input opamp settling time.

PVT corners simulations are also performed and results are presented in Table 4.1.

4.3.2 Operation

As stated before, designed DAC has two phases of operation: Reset (i.e. sample and hold), and conversion. During reset phase, capacitor array is charged to the input voltage. During conversion mode, top plate switch is opened to establish a floating node and bottom plates are connected to either positive or negative reference voltage according to the digital input code. An output voltage appears according to the digital input code.

Positive and negative reference voltages are selected as $1.6V$ and $0.6V$ respectively, where common mode voltage is $1.1V$, the same as the comparator.

4.3.3 DAC simulations

A schematic of the DAC test is presented in Fig. 4.40. DAC input bits are produced with PWL sources in order to simulate both the DAC conversion and the ADC input sampling phase. All the input bits are ‘0’ at the beginning, one LSB is counted up at each period, upcounting is paused for one period after each 8 periods. After 256 periods of conversion and 32 periods of ADC analog input sampling periods, the full scale output is acquired. DNL and INL tests are applied to this output

Table 4.1: PMOS and NMOS input opamp PVT corners analysis results.

			NMOS INPUT		PMOS INPUT	
Prc. crnr.	*Temperature*	*VDD voltage*	*Gain (dB)*	*Settling time (ns)*	*Gain (dB)*	*Settling time (ns)*
tt	**-45 deg**	**VDD=3.135V**	65.5	1.02	40.5	1.94
		VDD=3.3V	66.4	1.26	40.1	1.94
		VDD=3.465V	66.9	1.26	39.7	1.93
	25 deg	**VDD=3.135V**	59.8	1.23	32	2.41
		VDD=3.3V	60.9	1.22	31.7	2.4
		VDD=3.465V	61.8	1.21	31.5	2.38
	105 deg	**VDD=3.135V**	59	1.53	25.8	2.86
		VDD=3.3V	50.4	1.51	25.5	2.83
		VDD=3.465V	51.6	1.49	25.2	2.82
ss	**-45 deg**	**VDD=3.135V**	63.1	1.07	37.7	2.09
		VDD=3.3V	64	1.07	37.4	2.08
		VDD=3.465V	64.6	1.06	37.1	2.07
	25 deg	**VDD=3.135V**	52.3	1.34	32	2.58
		VDD=3.3V	53.6	1.33	31.8	2.54
		VDD=3.465V	54.7	1.31	31.6	2.53
	105 deg	**VDD=3.135V**	38.7	1.92	26.8	3.14
		VDD=3.3V	39.7	1.87	26.4	3.07
		VDD=3.465V	40.6	1.83	26.1	3.03
ff	**-45 deg**	**VDD=3.135V**	65.6	0.98	42	1.86
		VDD=3.3V	66.5	0.97	41.6	1.85
		VDD=3.465V	67.1	1.29	41.2	1.84
	25 deg	**VDD=3.135V**	61.9	1.46	31.9	2.25
		VDD=3.3V	63	1.48	31.6	2.25
		VDD=3.465V	63.8	1.48	31.3	2.24
	105 deg	**VDD=3.135V**	56.2	1.4	24	2.68
		VDD=3.3V	57.6	1.39	23.7	2.67
		VDD=3.465V	58.6	1.38	23.4	2.66

voltage, excluding the sampled ADC analog input voltage. DAC output is sampled and exported to MATLAB where DNL adn INL calculations are performed.

DNL and INL plots for the DAC at TT 105 °C are presented in Fig. 4.41 and 4.42 respectively.

It is obvious that DAC have both DNL and INL properties well below 0.5 LSBs, which assures the linear operation and no missing codes.

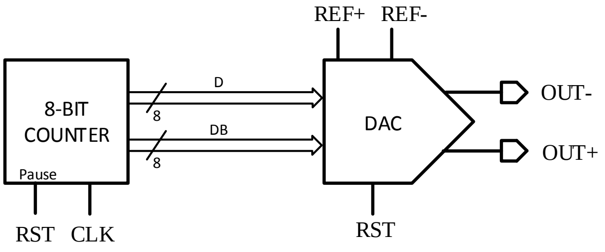

Figure 4.40: DAC test-bench.

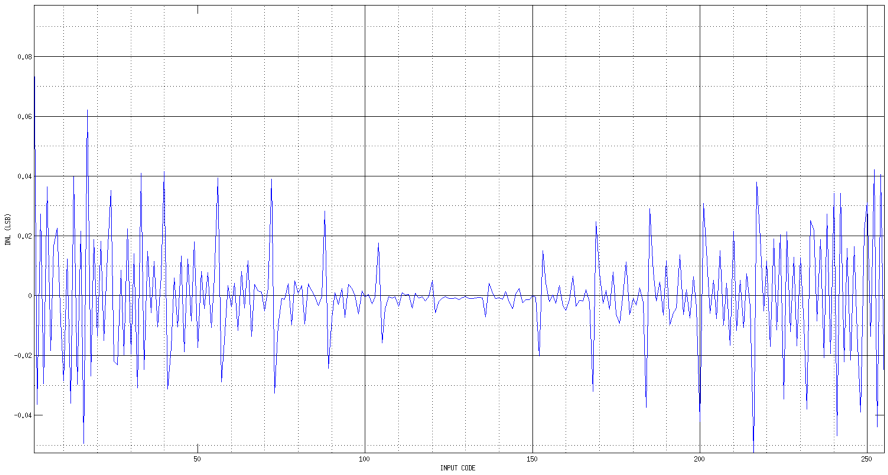

Figure 4.41: DAC DNL plot.

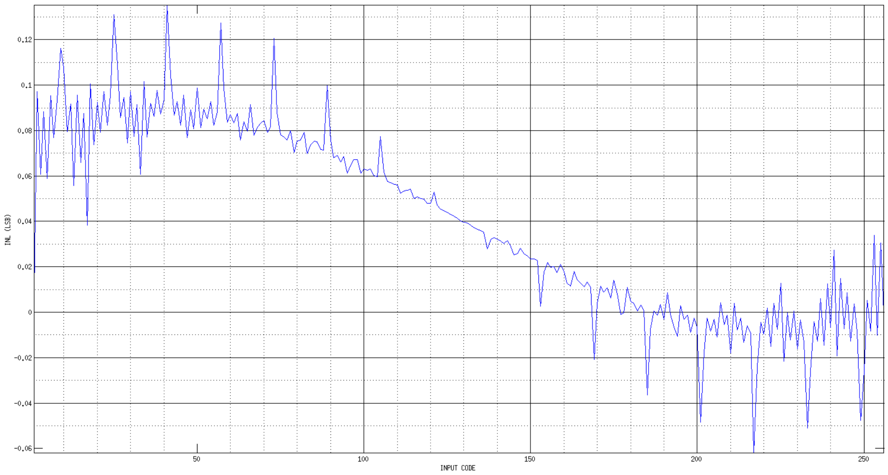

Figure 4.42: DAC INL plot.

5. ADC OPERATION

ADC in this work is designed as a fully differential 8-bit SAR ADC with the components described in the previous sections, using 0.18μ CMOS technology.

The converter has a $\pm 1V$ input voltage range and is supplied by a $1.8V$ where reference voltage buffers and input sampling switches are supplied with a $3.3V$ voltage source.

Each conversion is performed in 9 clock cycles. The minimum change in differential input voltage that ADC is able to sense and convert (Least Significant Bit - LSB) is equal to

$$\begin{aligned} LSB &= \frac{Input\ Voltage\ Range}{2^n} \\ &= \frac{2\,V}{2^8} = 7.8125mV \end{aligned} \tag{5.1}$$

A block diagram of the designed SAR ADC is seen in Fig.5.1. As seen in the block diagram, no external sample and hold circuit is used, instead, the DAC capacitors are used as sample and hold capacitors. This way, need for extra circuitry for the sample and hold is avoided, which probably would include a voltage buffer too.

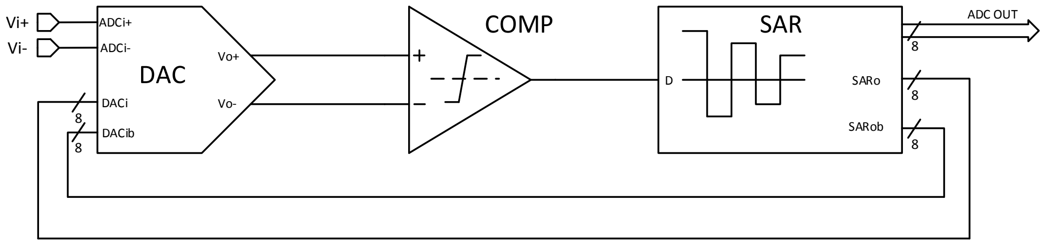

Figure 5.1: Block diagram of the designed SAR ADC.

A figure of clocks that drive the designed ADC is illustrated in Fig. 5.2.

A figure of internal node voltages together with the ADC clocks is given in Fig. 5.3. Investigating the clocks and the input-output voltage diagrams presented in Fig. 5.2 and Fig. 5.3, the working principle can be understood easily.

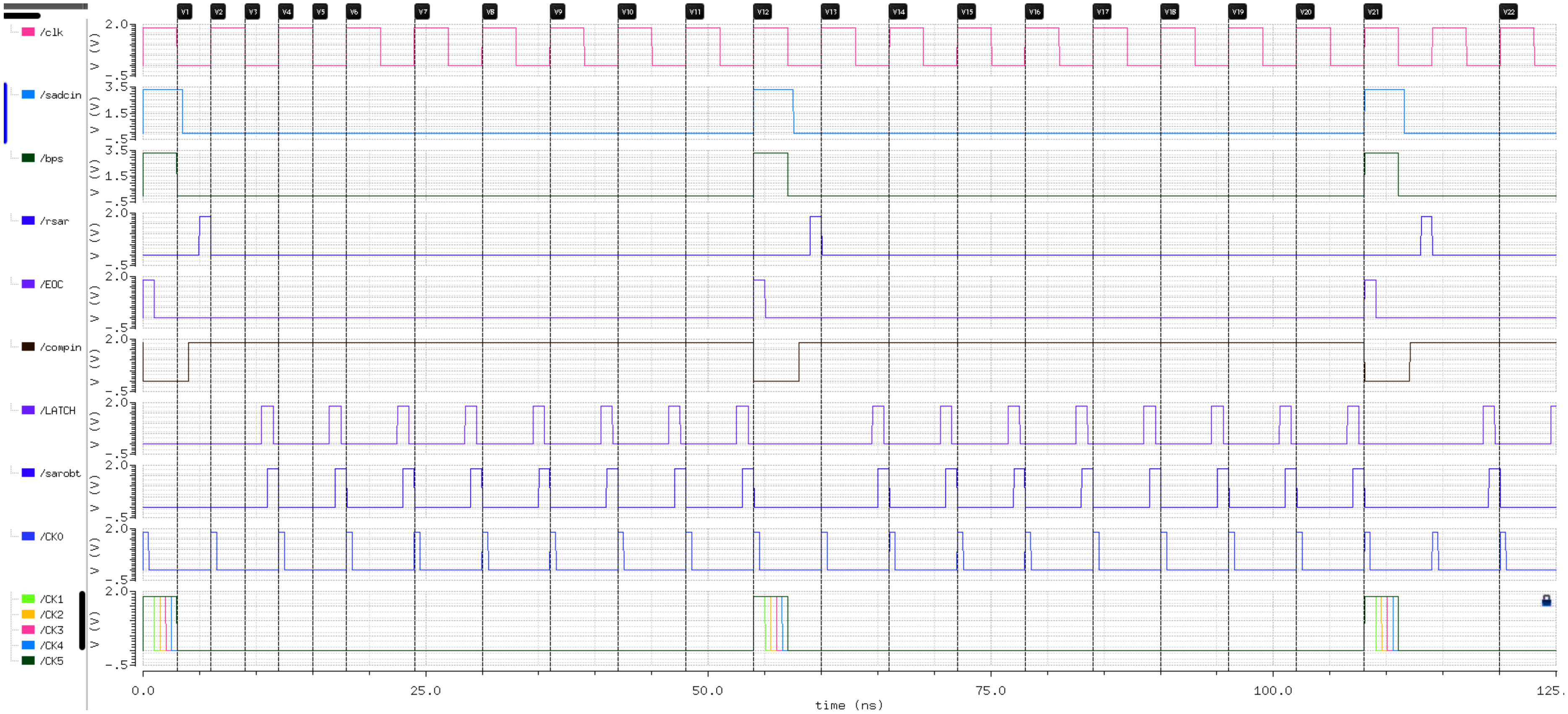

Figure 5.2: ADC clock signals.

The main clock (clk) runs 9 periods per conversion. So, there is $6 \cdot 9 = 54ns$ conversion period. First rising edge of the main clock starts everything: Comparator input is disconnected and connected to common mode voltage, bottom plate sampling switch is connected to common mode voltage, and all capacitors are connected to ADC input on the rising edge of the very first clock (clk).

First half clock period is for the analog input voltage sampling. Inside that first half clock period, there are 5 CLK[i]s, 500ps each for amplifier reset and offset cancellations. Bottom plate sampler is at the falling edge of the main clock, at 3ns. Input disconnect and common mode connect comes 500ps later, at 3.5ns. Another 500ps later, at 4ns, comes the connect to the comparator (compin). Sampling clock is now done.

In the second clock rising edge, DAC starts. SAR logic output is ready at half scale. Also on this rising edge amplifiers get reset for 500ps. 4.5ns after the rising edge, DAC and the comparator amplifiers settle. Latch gets strobed for 1ns, between 4.5ns to 5.5ns. At exactly 5ns, the latch output is clocked into a flip flop. The SAR logic has 1ns, to operate, between 5ns and 6ns. At 6ns, the SAR logic is ready so 3rd cycle starts with a clock rising edge.

Continuing these conversion steps for 8 main clock periods, the first conversion data is ready at the output of the SAR logic. End of conversion signal is synchronized with the next conversion start, that is, the rising edge of the very first clock is at the same time the clock signal for the end of conversion. Comparator input disconnect, ADC input connect, bottom plate sampling switch connect to common mode also happens at the rising edge of this very first clock.

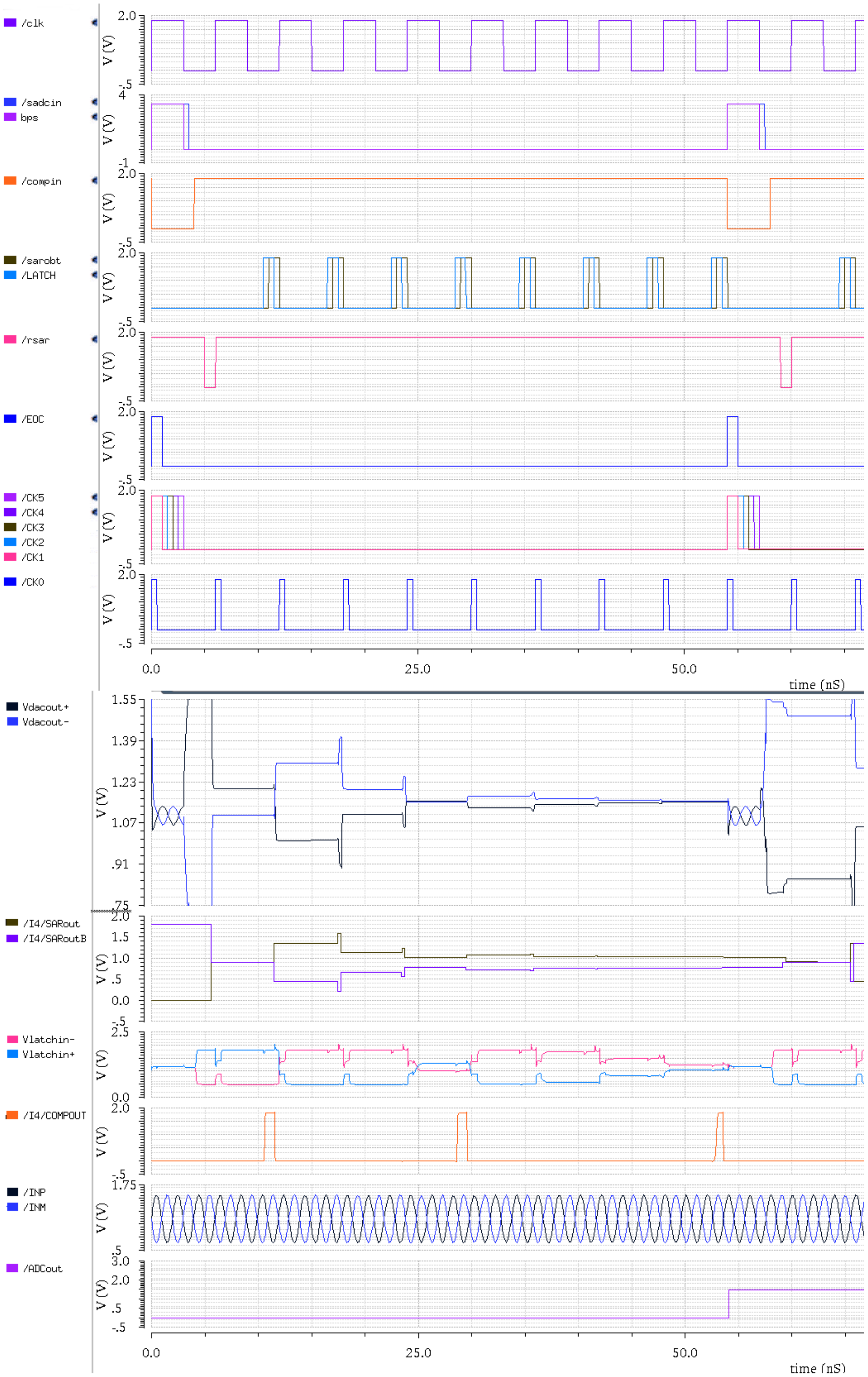

Figure 5.3: ADC clocks and the internal node voltages.

6. ADC PERFORMANCE EVALUATIONS

The designed ADC is simulated using the test-bench in Fig. 6.1. Test bench consists of the clock and input signal sources, ADC under test and an ideal DAC following the ADC under test. Ideal DAC converts the digital bits at the output of the ADC into analog voltage levels. This output is sampled at necessary points periodically and exported to a .csv file. Further processing like linearity test on the exported data is performed in MatLab environment.

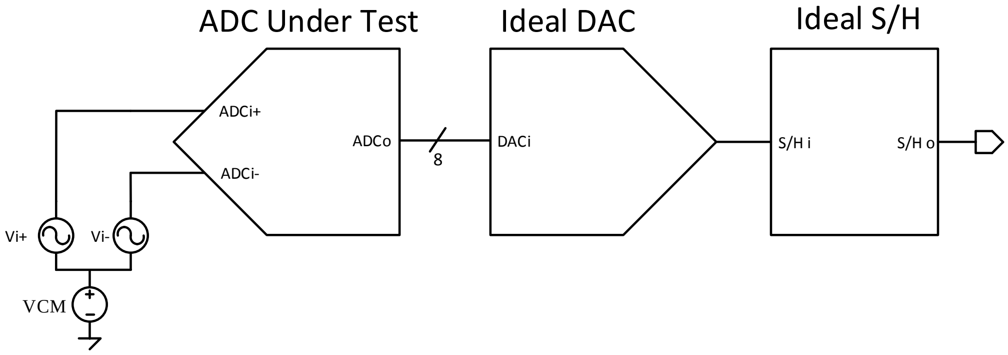

Figure 6.1: SAR ADC test-bench for performance evaluations.

6.1 Static Performance

6.1.1 Simulation setup

Static performance of the ADC is evaluated using the test bench in Fig. 6.1. Input signals are given as slow linear ramp voltages so that each code at the output should occur 8 times (8 hits per code - HPC) for an ideal ADC. Positive input voltage increases while negative input voltage decreases. ADC output words converted to analog ideally are sampled at the end of each conversion and experted to a .csv file in order to calculate static performance metrics in MatLab.

6.1.2 DNL

Differential Non-Linearity (DNL) can be defined as the difference between ideal and real number of occurrences of a code for ADC. Feeding an analog voltage corresponding to a certain output code along h conversion periods to ADC, DNL can be formulated as

$$dnl(i) = \frac{h_R - h}{h} \tag{6.1}$$

where $dnl(i)$ is DNL at ith code, h represents the ideal $hits\ per\ code$ number, h_R represents the obtained number of ith code.

Total DNL is usually reported as the absolute maximum value of the dnl array.

Eq. (6.1) is implemented in MATLAB and exported data is used for DNL calculation. MATLAB code for DNL calculation is presented in A. DNL plot of the ADC is given in Fig. 6.2.

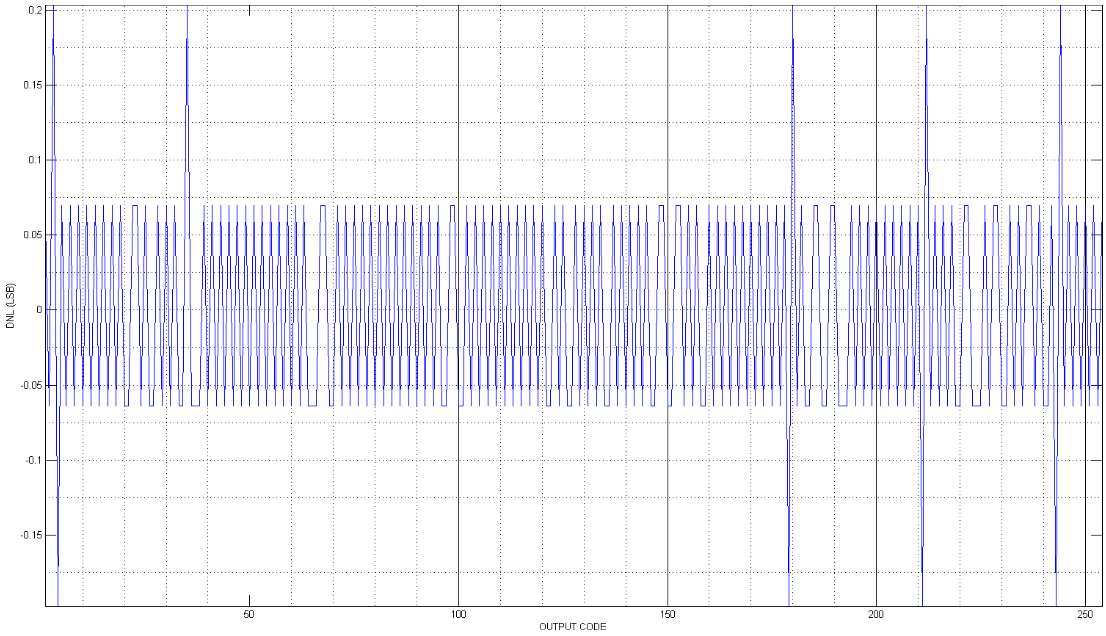

Figure 6.2: SAR ADC DNL plot.

6.1.2.1 DNL across PVT corners

DNL analysis is performed across PVT corners too. Simulation results show that the worst case DNL is just a little over 0.3 LSBs. DNL plots for the FF, TT, SS and total of corner simulations are given in Fig. 6.3, 6.4, 6.5, 6.6 respectively.

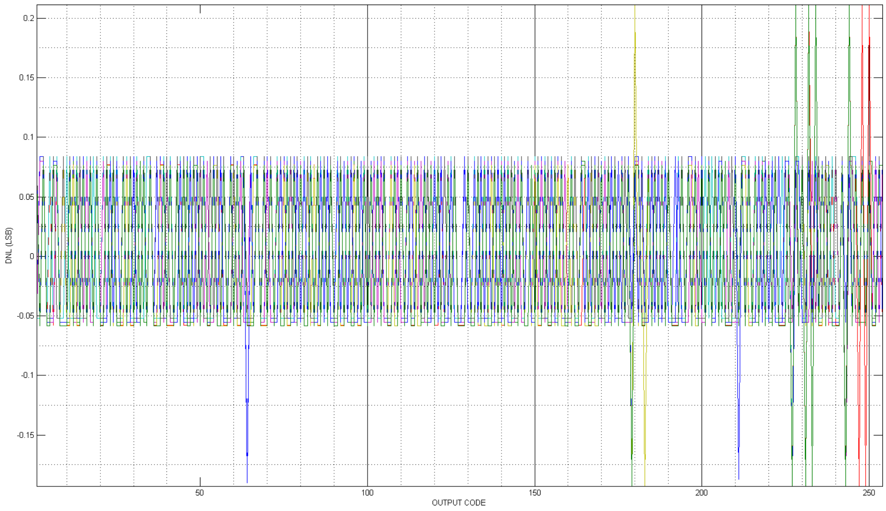

Figure 6.3: SAR ADC DNL for FF corners.

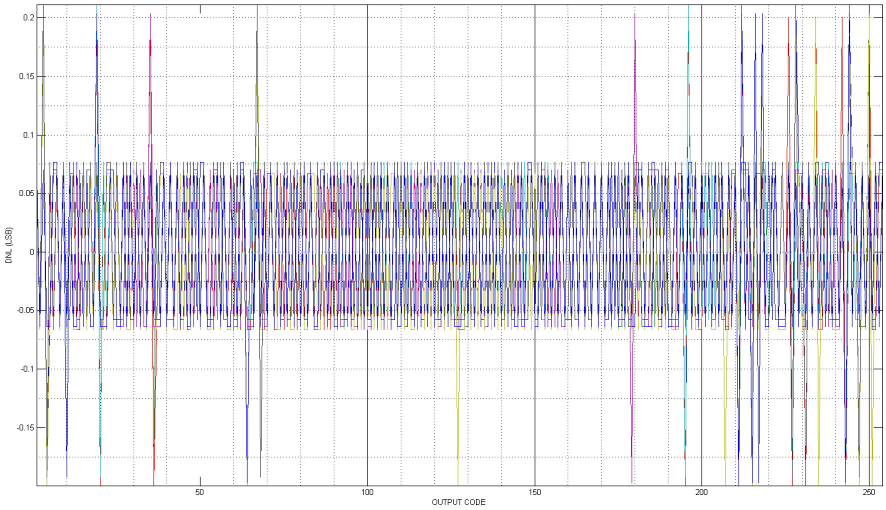

Figure 6.4: SAR ADC DNL for TT corners.

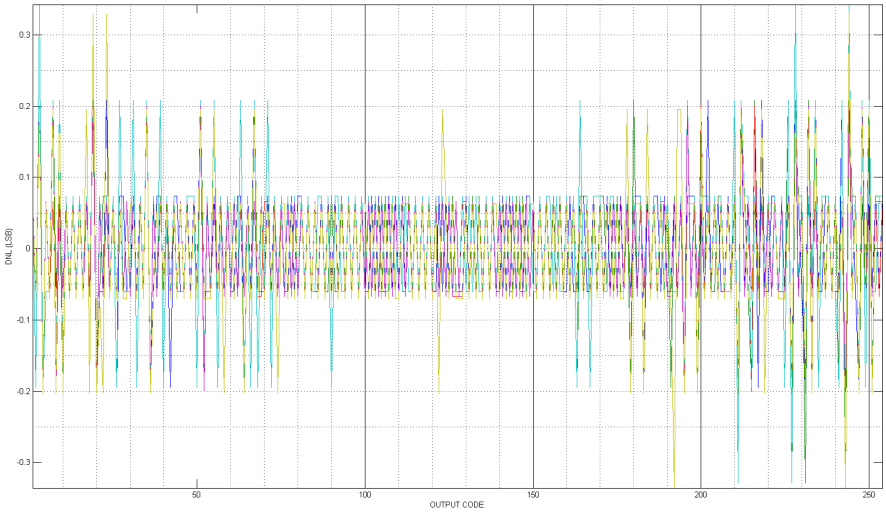

Figure 6.5: SAR ADC DNL for SS corners.

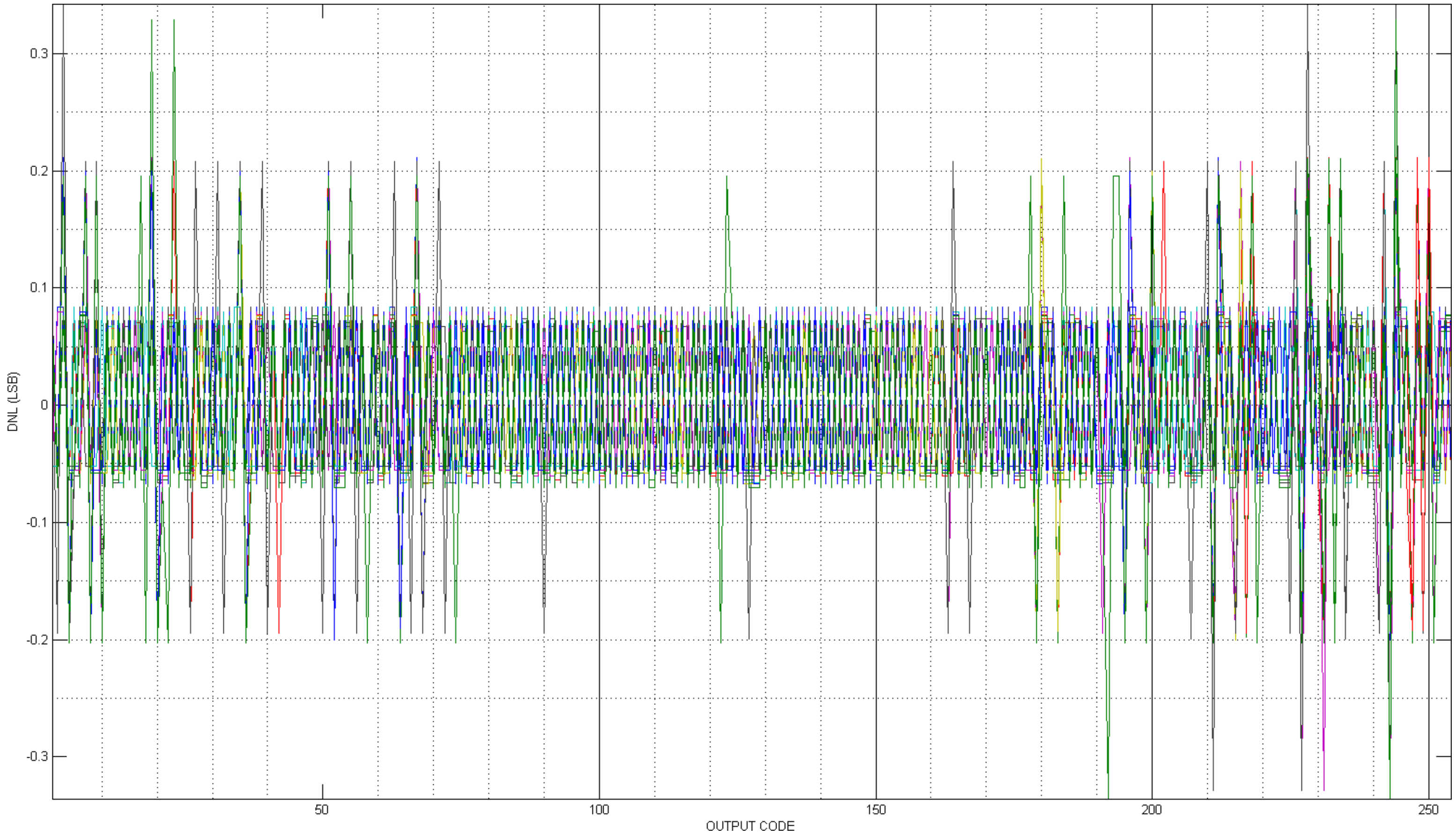

Figure 6.6: SAR ADC DNL for all PVT corners.

6.1.3 INL

INL can be simply described as the cumulative sum of the DNL array for the ADC.

$$inl(i) = \sum_{k=1}^{i} dnl(k) \tag{6.2}$$

where $inl(i)$ is the INL of ith code, $dnl(k)$ is the DNL for kth code and $1 \leq i \leq 2^n$.

Total INL is also usually reported as the absolute maximum value of the *inl* array. INL plot of the ADC is given in Fig. 6.7.

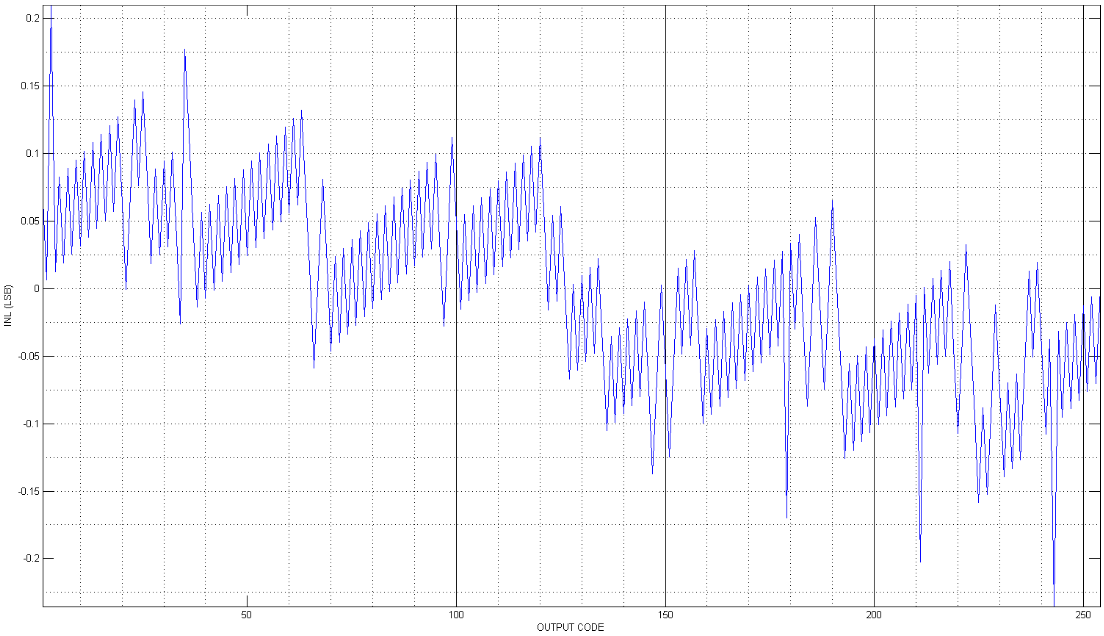

Figure 6.7: SAR ADC INL plot.

6.1.3.1 INL across PVT corners

INL analysis is performed across PVT corners too. Simulation results show that the worst case INL is just a little over 0.4 LSBs for some rare SS corners. INL plots for the FF, TT, SS and total of corner simulations are given in Fig. 6.8, 6.9, 6.10, 6.11 respectively.

6.1.4 Offset error

ADC offset error is measured at mid-code output. A very slow input ramp signal is applied and the output of the ADC is observed. The difference between common mode voltage (1.1V) and the input voltage level at which the output code turns mid-code plus

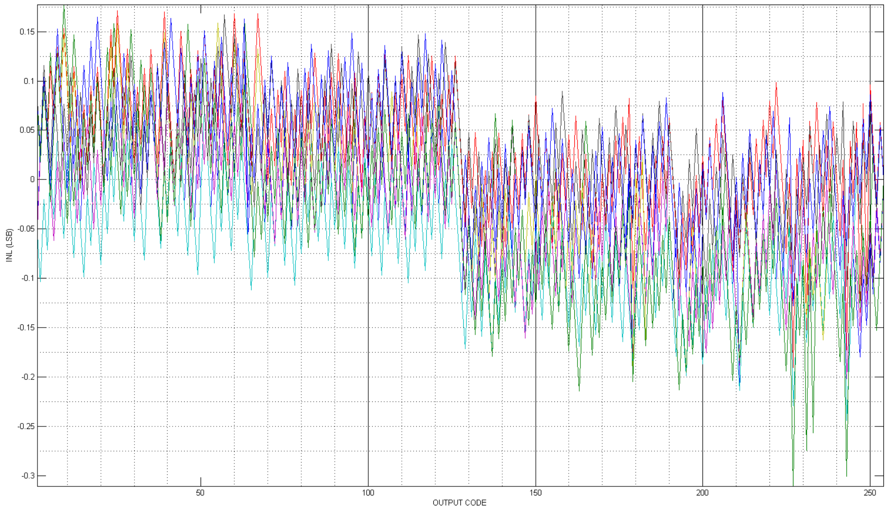

Figure 6.8: SAR ADC INL for FF corners.

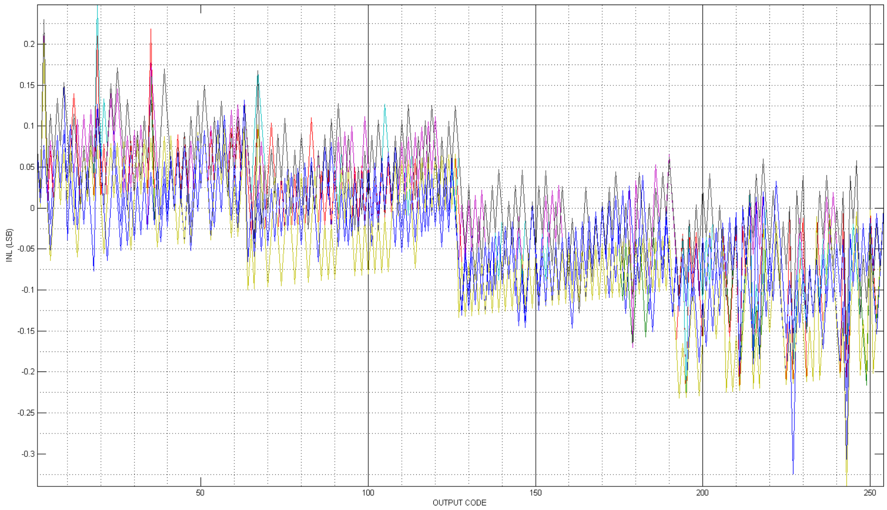

Figure 6.9: SAR ADC INL for TT corners.

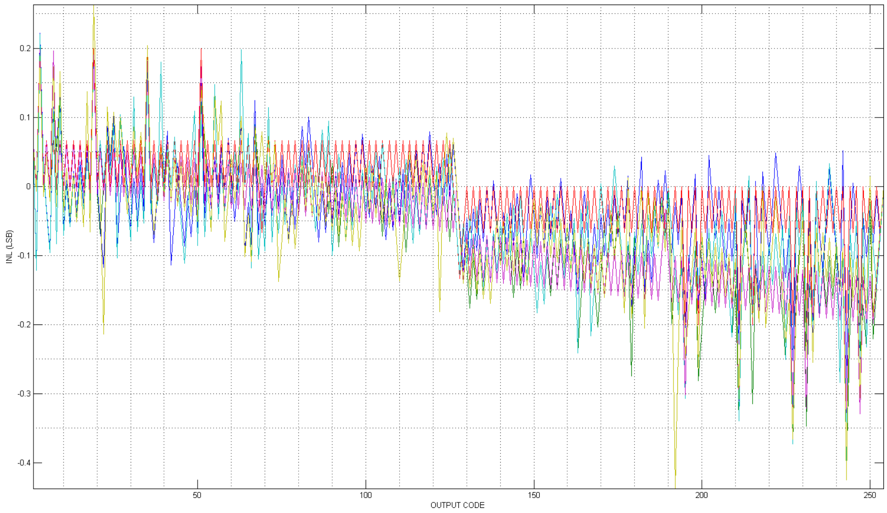

Figure 6.10: SAR ADC INL for SS corners.

one (127 to 128 in this case) is the offset error of the ADC. A 30 run Monte-Carlo simulation is performed. Offset error results are presented in Fig. 6.12.

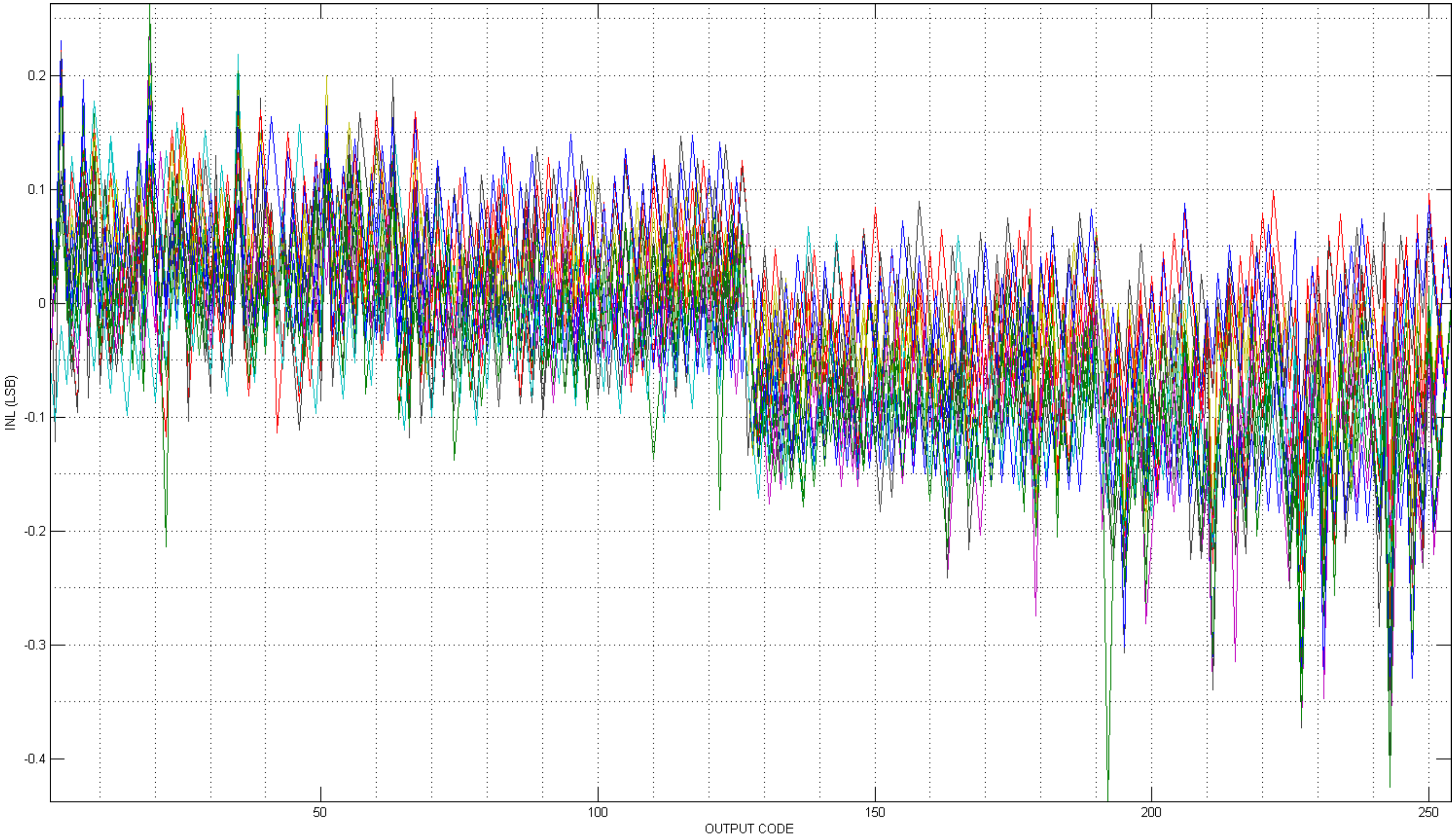

Figure 6.11: SAR ADC INL for all PVT corners.

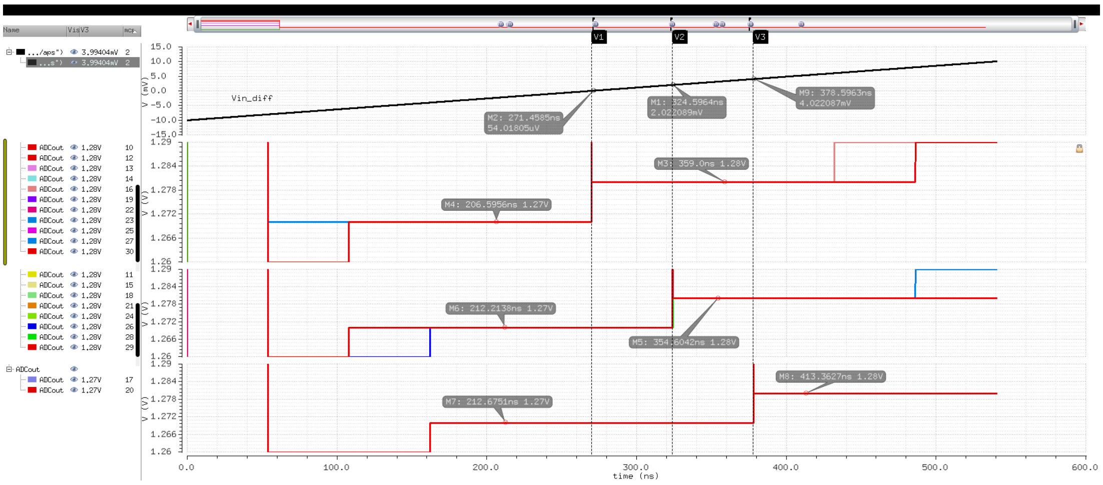

Figure 6.12: ADC offset voltage across Monte-Carlo simulation runs.

Observing offset error Monte-Carlo analysis results shows that 16 runs gives $0V$, 12 runs gives $2mV$, and 2 runs gives $4mV$ offset error. Mean offset error can be calculated as $16 \cdot 0 + 12 \cdot 2mV + 2 \cdot 4mV = 533\mu V$. Variance for the offset error is calculated as 1.53μ, standard deviation is calculated as $1.236 \cdot 10^{-3}$ and $3 - sigma$ is calculate as $3 \cdot 1.236 \cdot 10^{-3} = 3.71mV$.

6.2 Dynamic Performance

Dynamic specifications of the ADC are discussed in this section.

6.2.1 Simulation setup

Input voltages are given as sine waves with frequencies that allow coherent sampling.

Dynamic performances are obtained by running transient simulations allowing the ADC to convert 64 samples of the input. Corresponding cadence calculator functions are used in order to find dynamic performance specifications. Also FFT of the resulting data is plotted to visually observe the SFDR, harmonics and noise level.

6.2.2 SFDR

ADC SFDR is measured for 500 MHz input signal in all PVT corners. The SFDR result for the 500 MHz input shows ADC's undersampling performance. Worst corner SFDR result is seen in Fig. 6.13.

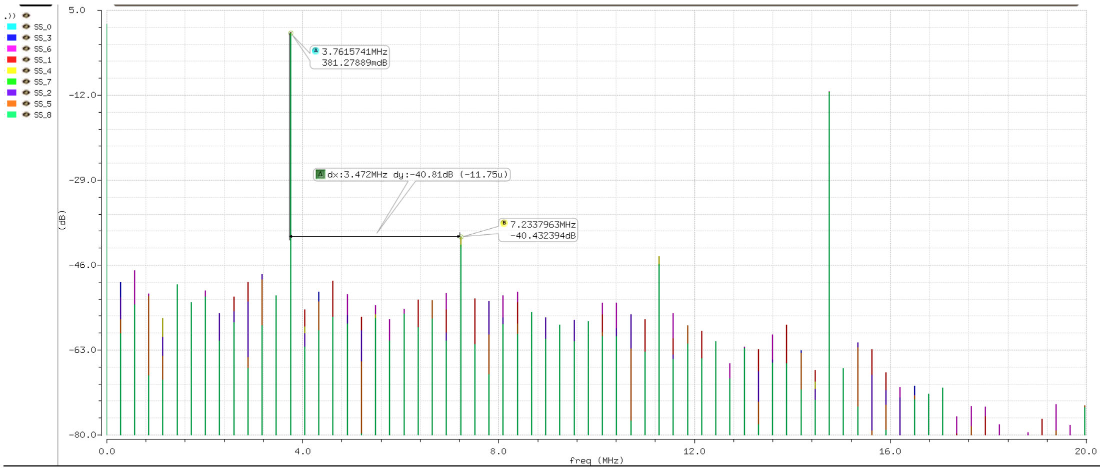

Figure 6.13: SAR ADC SFDR for a 500 MHz input signal.

6.2.3 SNR, SINAD and ENOB

Signal to noise ratio (SNR) is defined as the ratio of the signal power to the noise power and can be formulated as

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{6.3}$$

where P_{signal} is the noise power and P_{noise} is the noise power.

Signal to noise and distortion (SINAD) ratio is defined as the ratio between the signal power and the noise power plus distortion and can be formulated as

$$SNR = \frac{P_{signal}}{P_{noise} + P_{distortion}} \tag{6.4}$$

where P_{signal} is the noise power, P_{noise} is the noise power, and $P_{distortion}$ is the distortion power.

Effective number of bits (ENOB) has a relation with signal to noise and distortion ratio (SINAD) as in Eq. (6.5).

$$SINAD = 6.02 \cdot ENOB + 1.76 \tag{6.5}$$

So one can easily be calculated when the other is known.

A table of SNR, SFDR, SINAD and ENOB across PVT corners for a 500 MHz input signal is given in Table 6.1.

A table of SNR, SFDR, SINAD and ENOB versus input signal frequency at nominal corner is given in Table 6.2.

Table 6.1: ADC SNR, SFDR and ENOB results across the PVT corners

			SNR (dB)	SFDR (dB)	SINAD (dB)	ENOB
SS	1.71	-40	44.62	42.34	40.66	6.46
		25	42.87	42.76	38.72	6.14
		105	43.65	43.72	39.66	6.3
	1.8	-40	43.92	43.3	39.84	6.33
		25	43.53	40.82	39.52	6.27
		105	44.54	44.27	40.53	6.44
	1.89	-40	43.16	42.35	38.04	6.03
		25	46.73	42.36	41.42	6.59
		105	45.27	42.66	39.46	6.26
TT	1.71	-40	52.23	48.3	45.1	7.2
		25	44.21	45.48	41.16	6.54
		105	43.27	43.01	38.13	6.04
	1.8	-40	46.12	45.42	43.4	6.92
		25	45.18	42.62	39.86	6.33
		105	46.51	45.93	40.14	6.38
	1.89	-40	47.74	47.82	43.66	6.96
		25	47.27	47.35	44.35	7.07
		105	48.23	48.78	45.08	7.2
FF	1.71	-40	48.95	48.49	45.05	7.19
		25	49.98	52.71	47.26	7.56
		105	48.63	51.41	45.33	7.24
	1.8	-40	50.17	49.37	46.02	7.35
		25	50.16	51.88	46.13	7.37
		105	48.62	54.12	45.26	7.23
	1.89	-40	52.14	52.68	47.38	7.58
		25	53.01	55.19	47.52	7.6
		105	45.43	48	39.76	6.31

Table 6.2: ADC SNR, SFDR and ENOB results for different input signal frequencies at the nominal corner.

Base Frequency	Prime number	Fin(=base*prime)	SFDR (dB)	ENOB (bits)	SNR (dB)	SINAD (dB)
1/(54ns*64sample)=289.35K	3	868.0556K	55.67	7.99	51.18	49.8
	5	1.4468M	59.08	7.95	50.65	49.62
	37	10.7060M	55.79	7.55	47.11	47.22
	173	50.058M	56.41	7.74	48.29	48.4
	347	100.4051M	53.76	7.45	46.62	46.62
	1733	501.4468M	43.6	6.5	44.58	40.89
	3467	1.0031829G	45.74	6.57	41.41	41.34
	5189	1.501447G	54.04	7.41	47.38	46.34
	6917	2.001447G	44.72	6.04	39.01	38.12

A table of SNR, SFDR, SINAD and ENOB with changing sampling rate of the ADC for a 500 MHz input signal at TT 105 °C is given in Table 6.3.

Table 6.3: ADC SNR, SFDR and ENOB results for different sampling rates of the ADC for 500 MHz input signal at the PVT corners

Sampling Rate (MS/s)	SFDR (dB)	ENOB (bits)	SNR (dB)	SINAD (dB)
10	48.35	6.54	44.23	41.1
15	44.59	6.75	45.2	42.39
20	44.27	6.34	42.36	39.9
25	47.65	6.66	44.75	41.82
30	45.26	6.35	41.2	40
35	7.97	0.5	7.36	4.64
40	0	0	0	0

A 30 run Monte-Carlo simulation with 500 MHz input signal at TT 105 °C corner is performed and results are provided in Table 6.4.

Table 6.4: ADC SNR, SFDR and ENOB results for 30 Monte-Carlo runs with 500 MHz input signal at TT 105 °C corner.

MC Run Nr.	ENOB (bits)	SFDR (dB)	SINAD (dB)	SNR (dB)		MC Run Nr.	ENOB (dB)	SFDR (dB)	SINAD (dB)	SNR (dB)
1	7.11	46.38	44.59	50.13		16	6.97	44.91	43.69	50.43
2	7.15	46.69	44.80	50.02		17	7.07	45.95	44.33	50.53
3	7.23	47.06	45.27	50.87		18	7.07	45.95	44.33	50.53
4	7.07	45.95	44.33	50.53		19	7.15	46.69	44.80	50.02
5	7.11	46.39	44.56	50.31		20	7.12	46.34	44.64	50.12
6	7.11	46.38	44.59	50.13		21	7.09	46.10	44.47	50.82
7	7.09	46.07	44.47	50.05		22	7.11	46.38	44.59	50.13
8	7.24	47.27	45.36	50.90		23	7.16	46.81	44.87	49.68
9	7.02	45.45	44.04	49.95		24	7.11	46.39	44.56	50.31
10	7.11	46.38	44.59	50.13		25	7.15	46.69	44.80	50.02
11	7.14	46.49	44.74	50.88		26	7.24	47.27	45.36	50.90
12	7.11	46.39	44.56	50.31		27	7.05	45.65	44.18	50.06
13	6.99	45.31	43.84	49.83		28	7.14	46.59	44.76	50.98
14	7.10	46.06	44.53	50.05		29	7.24	47.27	45.36	50.90
15	7.07	45.95	44.33	50.53		30	7.16	46.81	44.87	49.68

6.3 Power Consumption Performance

Power consumption of the ADC is calculated for each of the sub-blocks separately and listed in Table 6.5.

Table 6.5: ADC power consumption performance.

Comparator power	DAC power	SAR power	Reference Buffers Power
9.76mW	4.94mW	1.38mW	107.83mW
ADC Total			**TOTAL SUM**
16mW			124.64mW

7. CONCLUSION

Time interleaved ADC's are based on paralleling several ADCs and clocking them accordingly so that the input signal is sampled and converted with a much higher speed. This project started as a preparation work to find and design appropriate candidate to be used a design start point for a time interleaved ADC.

Starting with this idea, probable ADC architectures have been analyzed and SAR ADC structure has been chosen because of its low power operation conditions and design simplicity comparing the other alternatives.

All sub-blocks are analyzed both theoretically and practically. Corner and temperature dependencies of properties are examined.

In this work, a reliable and feasible 8-bit, 20 Msps SAR A/D converter with 1 GHz bandwidth is presented using 180 nm standard CMOS process. A five stage comparator with 3-stage output offset cancellation is designed, characterized using simulation and laid out. A fully differential capacitive DAC driven by the SAR logic is designed and characterized using simulation. Three reference buffers for Vref+, Vref- and Vcm are also designed and characterized via simulation. Finally, the A/D converter using an effective timing pattern is constructed and characterized for offset, differential linearity (DNL), integral linearity (INL), spurious free dynamic range (SFDR), signal to noise and distortion (SINAD), signal to noise ratio (SNR) and effective number of bits (ENOB).

Simulations indicate that at full Nyquist bandwidth, the A/D converter exceeds 6 ENOB across process, voltage, temperature and chip to chip variation, with a nominal results of 7.2 bits. At a low 1 MHz input frequency, the nominal corner shows an ENOB of 7.95. Power consumption is typically 15mW excluding reference buffers, which will be shared during interleaving.

7.1 Future Work

The SAR ADC presented in this thesis can be further developed by decreasing the power consumption, increasing the sample rate, and drawing the full layout in order to see post-layout performance of the whole SAR ADC.

Since the main purpose of this thesis is to develop a building block of a massively parallel, time interleaved analog to digital conversion system, an inherent future work is to build a time interleaved A/D converter system using the designed SAR ADC as a main sub-block.

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APPENDICES

APPENDIX A.1 : MATLAB CODE FOR DAC INL&DNL CALCULATION
APPENDIX A.2 : MATLAB CODE FOR ADC INL&DNL CALCULATION
APPENDIX A.3 : ROUTE TO THE DESIGN FILES

APPENDIX A.1: MATLAB CODE FOR DAC INL&DNL CALCULATION

```matlab
dacoutfile = 'dacinldata.csv';
A = csvread(dacoutfile);
dacout=[];
for i=1:15:size(A,1)
    for j=i:i+7
        dacout=[dacout;A(j,2)];
    end
end
n=8;
bincountup=dec2bin(0:2^n-1)-'0';
%%---------------------IDEAL ...
   DAC-----------------------------------------------
for i=1:n
    index(i,1)=2^(n-i);
end
deccountup=bincountup*index;      %calculate adc decimal output
lsb=(((dacout(end)-(dacout(1))))/((size(dacout,1)-1)));
idealout=(deccountup*lsb)+dacout(1);
difference=idealout-dacout;
inl=difference/lsb;
dnl=diff(inl);
```

APPENDIX A.2: MATLAB CODE FOR ADC INL&DNL CALCULATION

```

adcoutfile = './adcinldata.csv';

adcout = csvread(adcoutfile,1,1); %read sim results from file


dnl = hist(adcout,min(adcout):max(adcout)) /... %create ...
    histogram of each value of adcout
(numel(adcout)/(max(adcout)-min(adcout)+1)) - 1; %divide ...
    quantity of values by average width of a step
% -1 calulates DNL

inl=cumsum(dnl); %calculate INL
```

APPENDIX A.3: ROUTE TO THE DESIGN FILES

Design schematics and layout files of this thesis work are located at ITU VLSI LABs' servers under the project of 'TMSMOZ' in 'components' folder.

The simulation profiles are also located in the 'TMSMOZ' project in 'sims' folder.

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