ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

CMOS CURRENT MODE EXPONENTIAL FUNCTION GENERATOR CIRCUIT USING PADE APPROXIMATION

M.Sc. THESIS

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

PADE YAKLAŞIKLIĞI KULLANAN AKIM MODLU CMOS EKSPONANSİYEL FONKSİYON ÜRETİCİ DEVRESİ

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FOREWORD

I would like to thank my advisor Prof. Dr. Ali TOKER, who always believed in me, for all his guidance, supports and encouragements to me. With his vision, he changed my life forever.

In addition, I am earnestly thankful to Prof. Dr. Serdar ÖZOĞUZ for all his efforts and spending valuable time on my thesis. Without him, I cannot do this work.

December 2015

Duygu KUTLUOĞLU
Electronics Engineer

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ABBREVIATIONS

AAC : Adaptive Atenna Combining
AGC : Automatic Gain Control
EXPFG : Exponential Function Generator
VGA : Variable Gain Amplifier
WCDMA : Wideband Code-Division Multiple Access
WPAN : Wireless Personal Area Networks
WSN : Wireless Sensor Networks

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CMOS CURRENT MODE EXPONENTIAL FUNCTION GENERATOR CIRCUIT USING PADE APPROXIMATION

SUMMARY

Over the past few years, as a result of the high demand to more powerful mobile devices, the importance of the high speed wireless communication becomes greater and greater. Automatic gain control (AGC) is necessary for controlling the signal amplitude and maximizing the dynamic range of the communication systems. The most important element of AGC loop is Variable Gain Amplifier (VGA). VGAs are widely used in biomedical applications, in imaging and signal processing circuits as well as the communication systems.

VGAs can be classified according to their control function. The control function can be an analogue (continuous) signal or a discrete signal. The VGAs that are controlled with continuous signal are either controlled with a linear signal or an exponential signal. Exponential control signals are preferred because of their higher dynamic range characteristics. To realize exponential signals, devices with exponential DC characteristics can be used. Whilst CMOS technology lacks devices that have exponential characteristics in linear or saturation regions, exponential function approximations are used as the functions that will be realized with MOSFET devices working in saturation region.

In the scope of this thesis work, first the exponential function approximations that are used for designing the control blocks of VGAs are classified. It is found out that Taylor series approximation, pseudo exponential approximation and their combinations are mostly used in literature. Recently Pade approximation is also reported in a work. Mathematical verifications are also presented for these approximations using MATLAB. Second, the Exponential Function Generator (EXPFG) circuit designs in literature are examined and a performance comparison of these circuits are provided.

Moreover, a new exponential function approximation, using Pade approximations proposed. Pade approximation is preferred because it provides a better result compared to most common approximation method, Taylor series approximation with the same order. Finally, three exponential function generator circuits are designed in CMOS 0.35μm technology using the proposed approximation methodology. Their performance is measured to verify the mathematical analysis using SPICE tool. The results verified that Pade approximation equations can be used in design of EXPFGs and a proper order of numerator and denominator can be selected according the specifications of the VGA.

PADE YAKLAŞIKLIĞI KULLANAN AKIM MODLU CMOS EKSPONANSİYEL FONKSİYON ÜRETİCİ DEVRESİ

ÖZET

Son birkaç yıl içinde, daha güçlü mobil cihazlara karşı oluşan yüksek talep, artan veri transferi ve yüksek hız ihtiyacı sonucunda, yüksek hızlı kablosuz haberleşme sistemlerinin önemi çok daha büyük hale geldi. Haberleşme sistemleri, bilginin işaret genliğinde tutulduğu sistemler ve işaret genliğinin değişkenlik gösterebildiği veri depolama sitemlerini içerdiğinden, sinyalinin genliğini kontrol etmek, gürültü eşiğinin üzerinde tutabilmek ve sistemin dinamik aralığını maksimize etmek haberleşme kalitesi için kritik rol oynamaktadır. Geniş dinamik aralığına ek olarak, modern teknolojilerde yüksek frekans karakteristiği, düşük güç tüketimi, düşük gürültü, düşük kırmık alanı, ısıl şartlara düşük duyarlılık gibi ihtiyaçlar da söz konusudur. Bu ihtiyaçları karşılamak için kullanılan farklı teknolojiler ve bloklar bulunmaktadır. Bu amaçlara hizmet eden özellikle de dinamik aralığı arttırmak için kullanılan otomatik kazanç kontrolü devreleri haberleşme sistemleri için önemli yapıtaşlarından biridir. Bu devreler giriş sinyalinin genliği ne olursa olsun, çıkış sinyalinin genliğini sabit tutarak sistemin dinamik aralığını arttırırlar. Otomatik kazanç kontrolü döngüsünde ise en önemli blok kazancı ayarlanabilir kuvvetlendiricilerdir.

Elektronik sistemlerde işaretin bloklar arasındaki geçişi sırasında bloklara uyum sağlayabilmesi, işaretin doğru algılanması ve işlenebilmesi açısından kritiktir. İşaretin uyumlandırılması ihtiyacı, giriş işareti seviyesini uygulanacak elemanın giriş seviyesine uyumlandırmak gerektiği veya sinyalin kayıplarını doldurarak giriş işareti seviyesini sabitlemek gerektiği olduğu durumlarda ortaya çıkmaktadır. Kazancı ayarlanabilir kuvvetlendirici devreleri bu ihtiyacı karşılamak amacıyla tasarlanmış devrelerdir. Bu kuvvetlendiriciler geniş bantlı haberleşme sistemlerinin yanı sıra adaptif anten birleştirici sistemleri, direk dönüşüm alıcıları, görüntü ve sinyal işleme devreleri, kablosuz sensör ağları, kablosuz kişisel alan ağları, taşınabilir haberleşme sürücüleri, disk sürücüleri, görüntüleme devreleri ve işitme cihazları gibi biyomedikal sinyallerin algılandığı ve işlendiği uygulamalarda da sıklıkla kullanılırlar.

Kazancı ayarlanabilir kuvvetlendiriciler giriş sinyalini, uygulanan kontrol sinyaline oranla kuvvetlendiren devrelerdir. Bu devrelerin temeli 1968 yılında Gilbert tarafından oluşturulmuş ve Gilbert hücresi olarak adlandırılmıştır. Bu kuvvetlendiriciler bir kazanç katı, bir ortak mod geribildirim bloğu ve bir kontrol katından oluşurlar. Kazancı ayarlanabilir kuvvetlendiriciler kontrol bloklarında kullanılan kontrol fonksiyonlarına göre sınıflandırılabilirler. Kontrol fonksiyonu analog (sürekli) bir sinyal ya da dijital (ayrık) bir sinyal olabilir ve bu şekilde analog kazancı ayarlanabilir kuvvetlendiriciler ve dijital kazancı ayarlanabilir kuvvetlendiriciler olarak ikiye ayrılabilirler. Sürekli ve tekdüze bir çıkış sinyali elde edebilmek için analog kontrol sinyalleri tercih edilmektedir. Analog olarak kontrol

edilen kuvvetlendiriciler için kontrol, doğrusal ve ya üstel bir sinyal ile sağlanır. Üstel kontrol sinyalleri, daha yüksek dinamik aralık sağladıkları için yüksek kalite ve hız gerektiren sistemlerde tercih edilmektedir.

Üstel sinyalleri gerçekleştirmek için, üstel DC özelliklere sahip elemanlar kullanılabilir. Mesela BJT'lerde gerilim doğrudan üstel fonksiyonun değişkeni olarak kullanılabilmektedir, fakat BiCMOS uygulamalar daha maliyeli olduğu için bu uygulama çok tercih edilmemektedir. CMOS teknolojisinde ise, doğrusal veya doymalı bölgelerde üstel DC özelliklere sahip eleman bulunmamaktadır. Parazitik bipolar transistorler üretilebilmektedir fakat bu elemanlar sıcaklık ve üretim şartlarına bağımlı karakteristik özellikler göstermektedir. Bu sebeple üstel fonksiyon yaklaşımları kullanılarak doymada çalışan MOSFET elemanlarla gerçekleştirilen üstel fonksiyonlar üreten devreler tasarlanmaktadır.

Taylor serisi yaklaşımı, sözde üstel yaklaşım, Pade yaklaşımı gibi matematiksel yaklaşımlar ele alınarak bu yaklaşımlarla üretilen fonksiyonlar CMOS devre yapıları kullanılarak gerçeklenmektedir. Ayrıca Taylor serisi yaklaşımı ve sözde üstel yaklaşım ile elde edilen birleştirilmiş Taylor serisi ve sözde üstel yaklaşım veya katsayıları optimize edilmiş sözde üstel yaklaşım gibi bu fonksiyonların kombinasyonları kullanılarak ve bu kombinasyonlara eklenen katsayılar düzenlenerek de yeni fonksiyonlar üretilebilmektedir. Bu fonksiyonların gerçeklendiği devrelere eksponansiyel fonksiyon üretici devreler denmektedir ve bu devreler kazancı ayarlanabilir kuvvetlendiricilerin kontrol bloğu olarak kullanılmaktadırlar. Eksponansiyel fonksiyon üretici devreler ile elde edilen fonksiyonun çıkış aralığı, kazancı ayarlanabilir kuvvetlendiricilerin dinamik aralığını doğrudan belirlemektedir.

Bu tez çalışması kapsamında, ilk olarak kazancı ayarlanabilir kuvvetlendiriciler, kontrol bloklarının tasarımında kullanılan üstel fonksiyon yaklaşımlarına göre sınıflandırılmıştır. Eksponansiyel fonksiyon üreticilerinin tasarımında kullanılan Taylor serisi yaklaşımı, sözde üstel yaklaşım ve bu yöntemlerin kombinasyonları literatürde en çok rastlanılan yöntemlerdir. Son zamanlarda yapılan bir çalışmada Pade yaklaşımı da üstel fonksiyon üretiminde önerilmiştir. Tez kapsamında tüm üstel fonksiyon yaklaşımları için matematiksel doğrulamalar MATLAB kullanarak yapılmıştır ve fonksiyonların ideal üstel fonksiyon ile arasındaki ilişkiler ve hata fonksiyonları sunulmaktadır. Daha sonra bu fonksiyonlar giriş aralıklarına göre kıyaslanmış ve performansları değerlendirilmiştir. Ayrıca, literatürdeki üstel fonksiyon üretici devrelerin tasarımları incelenmiş, ilham verici olabilecek örnekler seçilip açıklanmış ve bu devrelerin çıkış dinamik aralıkları karşılaştırılmıştır.

Bu çalışma kapsamında, Pade yaklaşımı baz alınarak yeni bir üstel fonksiyon yaklaşımı önerilmiştir. Pade yaklaşımının seçilmesindeki başlıca sebep, aynı dereceden fonksiyonları için, literatürde en çok kullanılan metot olan Taylor serisi yaklaşımına oranla daha geniş bir aralıkta doğru sonuç vermesidir. Yapılan MATLAB hesaplamalarında ikinci dereceden rasyonel Pade fonksiyonun, üçüncü dereceden Taylor serisi yaklaşımı ile elde edilen fonksiyondan daha yüksek performans gösterdiği görülmüştür. Kullanılan fonksiyonun derecesi, tasarlanacak devrenin karmaşıklığını ve kırmık boyutunu doğrudan etkilediği için, Pade yaklaşımı baz alınacak üstel yaklaşım fonksiyonu olarak seçilmiştir.

Pade yaklaşımı fonksiyonuna, literatürde sıkça rastlanan ve verilen örnek çalışmalardan birinde de önerilen, çıkış dinamiğini arttırmak için giriş işaretinin yarılanıp daha sonra çıkışın karesinin alınması yöntemi uygulanmıştır. Bu yöntem

genel olarak devrelerin performansını arttırmak için kullanılan ve bilenen bir yöntemdir. Elde edilen bu yeni fonksiyon ile hesaplamalar yapılmış ve Pade tablosundaki konjuge fonksiyonların çarpımı kullanılarak, aynı derecedeki Pade fonksiyonlarına oranla daha geniş aralıkta doğru sonuç sağlayan bir üstel fonksiyon yaklaşımı elde edildiği görülmüştür. Böylece, bu tez çalışması kapsamında Pade tablosundaki konjuge fonksiyonları kullanan ve yüksek dinamik aralık sağlayan yeni bir üstel fonksiyon yaklaşımı önerilmiştir.

Bu yeni üstel fonksiyon yaklaşımı Pade tablosundaki fonksiyonlar kullanıldığı için rasyonel özelliktir ve bu sebeple devreyi kompleks hale getireceği düşünülebilir. Fakat, literatürde kullanılan ve üstel fonksiyon üretici devrelerin yapıtaşı olan çarpma devrelerinin karakteristikleri rasyonel olduğu için, bu işlem devrenin içerisinde ek bir maliyet getirmeden yapılabilmektedir.

Önerilen üstel fonksiyon yaklaşımını kullanarak farklı derece ve karmaşıklık seviyelerinde üç fonksiyon üretici devre, CMOS 0.35µm teknolojisinde tasarlanmıştır. Literatürden seçilen bir çarpıcı/bölücü devre bu amaç için öncelikle tasarlanmış ve bu devrelerde yapıtaşı olarak kullanılmıştır. Seçilen çarpıcı/bölücü devrenin şeması, kullanılan elemanların boyutları ve analiz sonuçları bu çalışma dahilinde verilmiştir.

Tasarlanan eksponansiyel fonksiyon üretici devrelerinin performansı SPICE benzetim aracını kullanarak ölçülmüş ve matematiksel analiz ile benzerliği karşılaştırılmıştır. Sonuçlar Pade yaklaşımı denklemlerinin verdiği sonuçlarla benzerlik göstermektedir. Örnek olarak baz alınan 2,1x1,2 devresi ise literatürde benzer ikinci dereceden devrelere göre daha yüksek performans göstermektedir. Diğer örnek devreler ile, sistemin tasarımında seçilen Pade fonksiyonlarının dercesinin, sistemin kompleksitesi ve performansı ile doğru orantı sergilediği gösterilmiştir.

Sonuç olarak, Pade yaklaşımını kullanan yeni bir eksponensiyel fonksiyon yaklaşımı önerilmiştir. Önerilen bu yeni yaklaşımda kullanılacak Pade denklemlerinin dereceleri tasarlanacak sisteme uygun olarak seçilebilmekte ve dinamik çıkış aralığı istenildiği gibi ayarlanabilmektedir. Daha karmaşık devrelerle daha yüksek dinamik aralıklar yakalanabilirken, daha düşük dinamik aralıklarda çalışması yeterli olan sistemler için daha basit devre yapıları tercih edilebilmektedir.

1. INTRODUCTION

Over the past few years, the importance of high-speed wireless communication becomes greater and greater due to the high demand of more powerful mobile devices [1]. Automatic Gain Control (AGC) circuits including Variable Gain Amplifiers (VGA) are acting an important role as a building block of wireless communication systems by providing fixed output power for different levels of input signal. This characteristic increases the dynamic range of the entire system [2]. The VGAs are widely used in communication systems such as the Wideband Code-Division Multiple Access (WCDMA) wireless communication systems [3], CDMAs [4], wireless sensor networks (WSN) [5], Adaptive Antenna Combining (AAC) systems [6], Wireless Personal Area Networks (WPAN), Portable communication drivers [7], and direct-conversion receivers [8]. The VGAs also play important role in biomedical signal acquisition [9], medical equipment [10], hearing aids [11], imaging [12], disk drives [13] and audio/video analogue signal processing circuits [14].

1.1 Variable Gain Amplifiers and Their Control Functions

Variable Gain Amplifiers, amplify the input signal with a gain that canbe varied with a control signal. A VGA can be demonstrated with three blocks, which are an amplifier block, a control block and a common mode feedback block as shown in Figure 1.1.

According to the type of the control block, Variable Gain Amplifiers can be classified to two types. The digitally controlled VGAs are controlled by a switchable signal and have discrete step gain. Analogue VGAsare controlled by a continuous control signal and their output signal is also continuous. Continuous type control blocks are preferred to obtain smooth gain transitions.

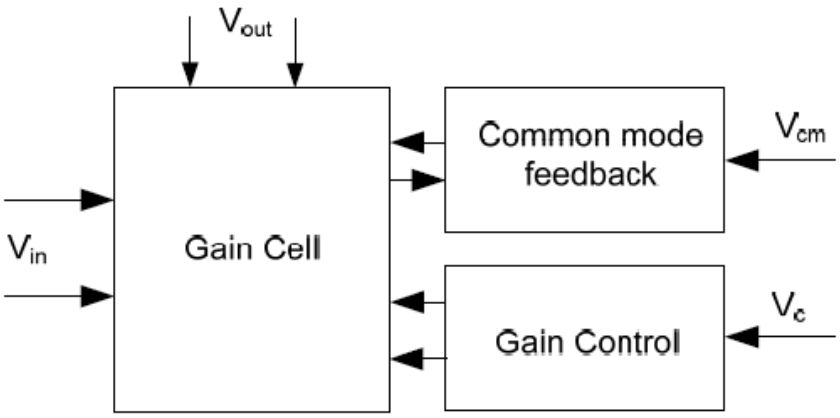

Figure 1.1 : A basic VGA Block.

Linear or exponential control functions can be used as continuoss control signals. Linear gain control can be realized by current steering technique [15, 16]or by using variable feedback resistance [17, 18].There are various ways to realize exponential gain controls and they are widely used to achieve wide dynamic range.

To realize exponential functions, devices with exponential DC characteristics can be used. DC current-voltage characteristic of bipolar transistors are very suitable for this purpose but this method is not preferred because BiCMOS technologies are not cost efficient [19]. Parasitic bipolar transistors can be created in CMOS technology but this solution strongly suffers from temperature and process variations [20]. Moreover, MOSFETs operates in subthreshold region can be used to generate exponential control signals due to their exponential current-voltage characteristic [19]. However, this kind of circuits will suffer from noise, will have low bandwidth and will operate in low frequencies. It is also possible to realize exponential functions by using differential characteristics of MOS devices [21].

Another way is to use exponential function approximations as the functions that are going to be realized with the MOSFETs,which operates in linear or in saturation region. Taylor Series Approximation function with different order of the series is widely used [22-24]. Pseudo Exponential Approximation is another common prefferedmethod [25, 26]. Extended versions of these methodscan be found as Pseudo Exponential Function with Optimized Coefficient Values [27, 28] and United Taylor Series and Pseudo Exponential Approximation [29-32]. Pade approximation is also used in a resent work [33].

The classification of the VGAs in terms of their control functions are listed below.

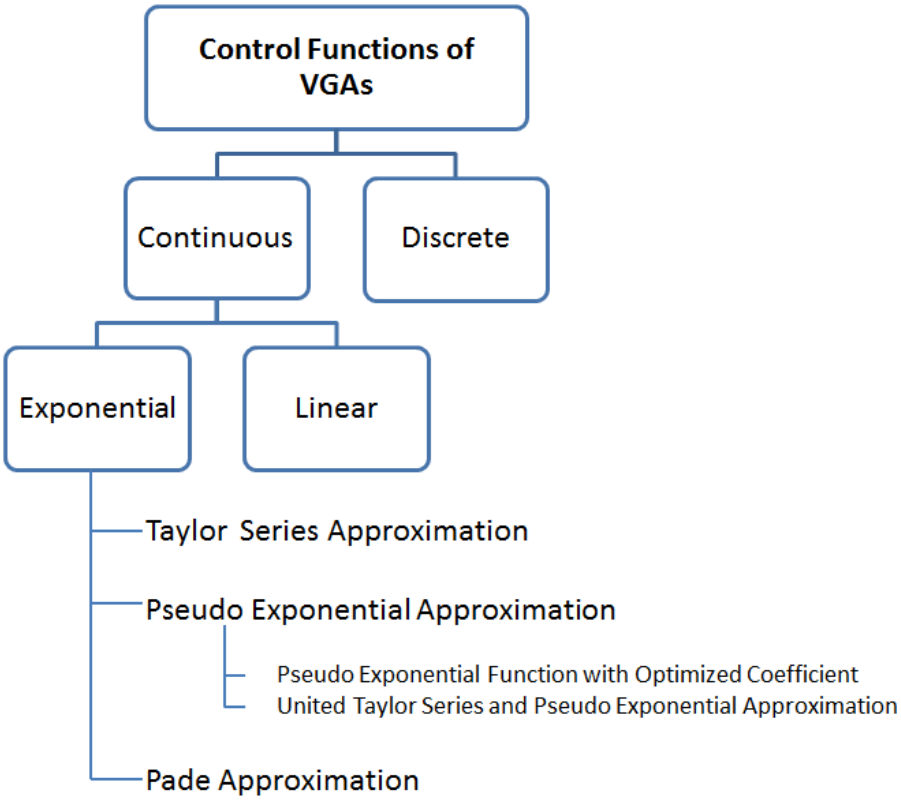

Figure 1.2 : Classification of VGAs in terms of the control functions.

1.2 Motivation

VGAs are very useful in AGC circuits as their wide dynamic range characteristic helps minimizing the settling time of the circuit, so that the output signal will be a uniform transient response.

As mentioned earlier, the exponential function generators (EXPFG) are necessary for design of wide dynamic range VGA circuits and a standard CMOS process does not have devices providing exponential characteristics in saturation region. This absence makes it difficult to design VGAs with monolithic CMOS based analog and mixed-signal circuits than bipolar technologies, where exponential functions can be easily obtained by their I-V law characteristics [34]. To be able to achieve exponential signals approximation methods are used so that the approximation function can be realized with MOSFETs working in saturation region or in linear region.

The techniques to generate exponential functions usually bring extra cost due to the need of complex circuitries [2].In this thesis work, formerly proposed exponential function generators that are used as a control block for VGA circuits are explored

and classified according to their approximation functions. The mathematical approaches are examined in detail to identify the advantages and the disadvantages. A new approach is proposed with the combination of these methodologies and is verified with PSPICE simulation.

1.3 Thesis Organization

VGA circuits, their applications and their control function approaches are introduced in Section 1. A detailed literature search is fulfilled and the control functions of VGAsare classified and listed.

In section 2, mathematical verifications are used to understand the Taylor series approximation, pseudo exponential approximation and their compositions. Mathematical verifications are also applied to Pade approximation which is recently reported as a new method for realizing exponential function generators.

Many exponential function generator circuits are examined during this thesis work. In section 3,some examples of cirduit designs are provided and performance comparison of these EXPFG circuits is listed.

In section 4, a new methodology for design of an exponential function generator by using Pade approximation is proposed. Three different circuit examples are designed in 0.35µm CMOS process and simulated by using SPICE to measure their performances.

In section 5, conclusion and recommendations are presented.

2. EXPONENTIAL FUNCTION APPROXIMATIONS

2.1 Taylor Series Approximation

Taylor series expansion of exponential function is given in Equation **(2.1)**.

$$e^{ax} = 1 + \frac{ax}{1!} + \frac{a^2x^2}{2!} + \ldots + \frac{a^n x^n}{n!} + \ldots \qquad \textbf{(2.1)}$$

For $|ax| \ll 1$, high order of Taylor series can be eliminated to obtain the exponential function with small error. The 2nd order Taylor series equation is given in Equation **(2.2)** [23].

$$e^{ax} = 1 + \frac{ax}{1!} + \frac{a^2x^2}{2!} \qquad \textbf{(2.2)}$$

For a=1, the error function of Equation (2.2) due to the ideal exponential function is given in Figure 2.1. The comparison between these functions is given in Figure 2.2. The range for x is –0.57 to 0.81 for keeping the error between positive and negative five percentages.

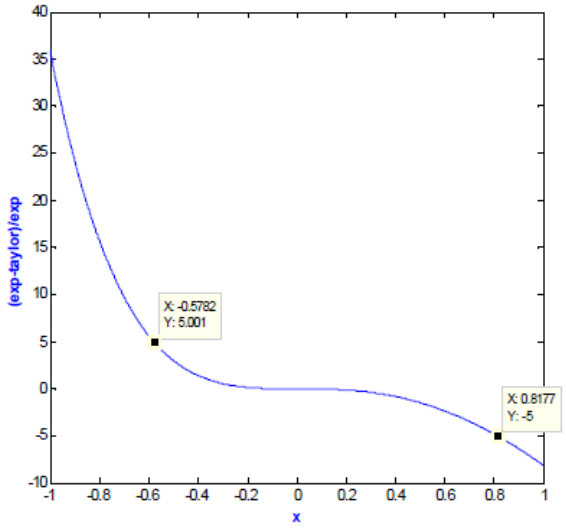

Figure 2.1 : Error function of Taylor series approximation.

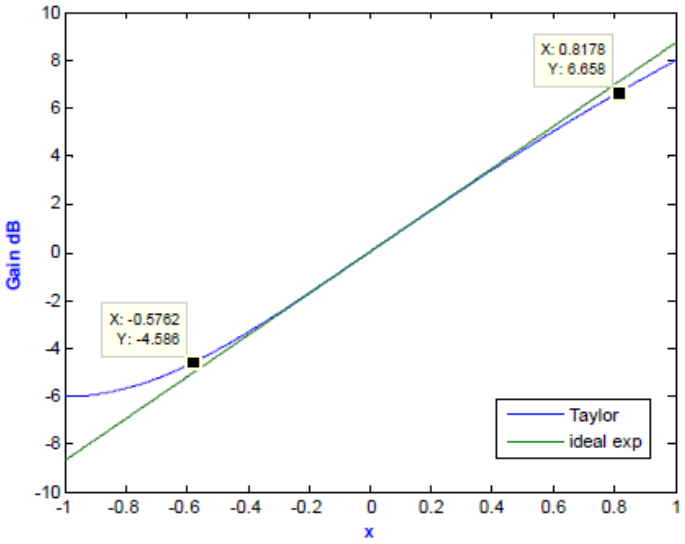

Figure 2.2 : Comparison of Taylor series function and ideal exponential function.

2.2 Pseudo Exponential Approximation

The equation of Pseudo Exponential Approximation is given below in **(2.3)** [35].

$$e^{nx} = \left(\frac{1 + x/2}{1 - x/2}\right)^{n}; \quad |x| < 1 \tag{2.3}$$

By using MATLAB, for n=1, the error function of this approximation is drawn for in Figure 2.3 and the comparison between ideal exponential function and this function is drawn in Figure 2.4 by using MATLAB.

The range for x is –0.8 to 0.8 for keeping the error between positive and negative five percentages. When x approaches to 1 or -1 this function approaches to zero or infinite.

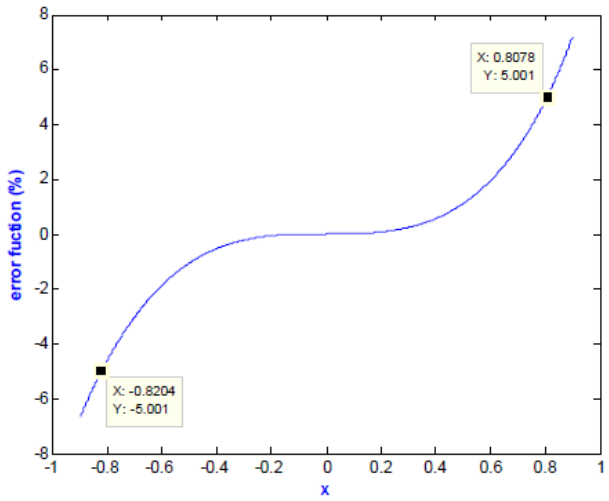

Figure 2.3 : Error function of Pseudo Exponential approximation.

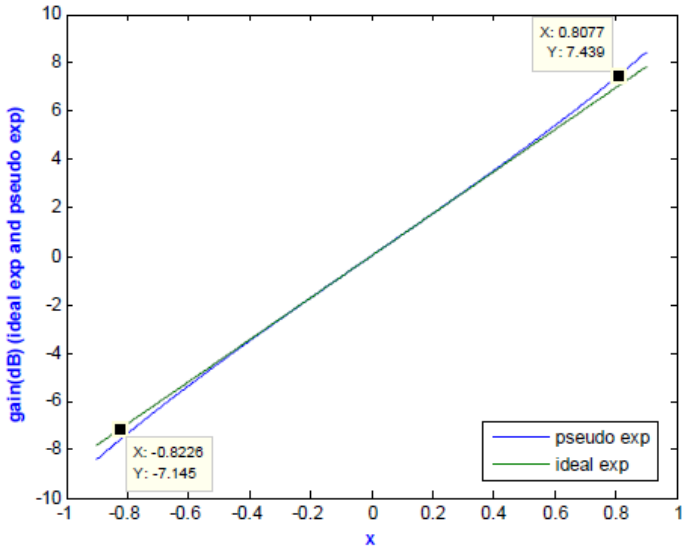

Figure 2.4 : Comparison of Taylor series function and ideal exponential function.

2.2.1 Pseudo Exponential Function with Optimizated Coefficient Values

Shortening the Taylor series to first order, an exponential function can be written as equation **(2.4)**.

$$e^{x} = e^{x+ax-ax} = \frac{1+ax}{1-(1-a)x} \tag{2.4}$$

In this equation, negative or positive range of x will increase when the value of a chosen like 0.25 or 0.75 [27]. In Figure 2.5, the error function, in Figure 2.6, the comparison between the ideal exponential function are drawn for a=0.75 and x>0.

In Figure 2.7, the error function, in Figure 2.8, the comparison between the ideal exponential function are drawn for a=0.25 and x<0.

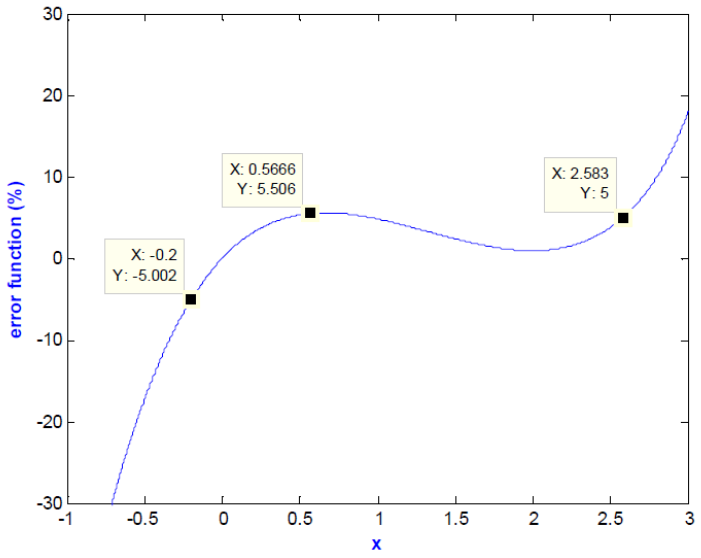

Figure 2.5: Error function of pseudo exponential approximation with optimizing coefficient (a=0.25 and x>0).

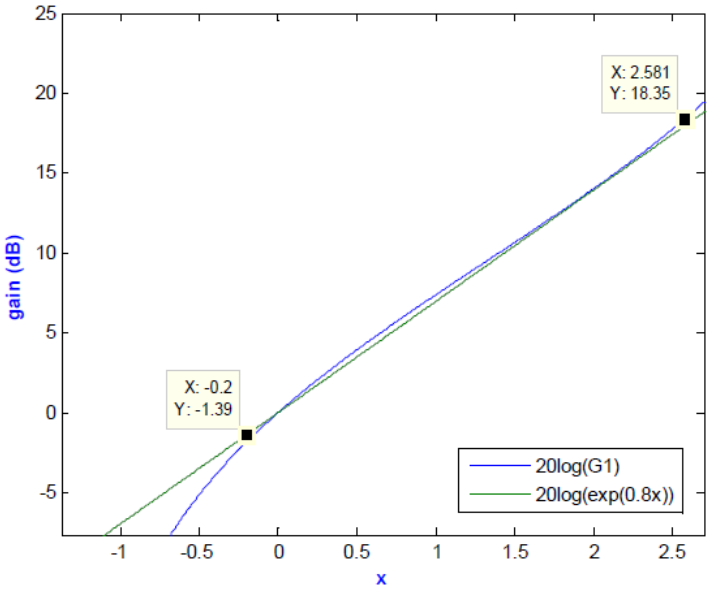

Figure 2.6 : Comparison of pseudo the function and ideal exponential function (a =0.25 and x>0).

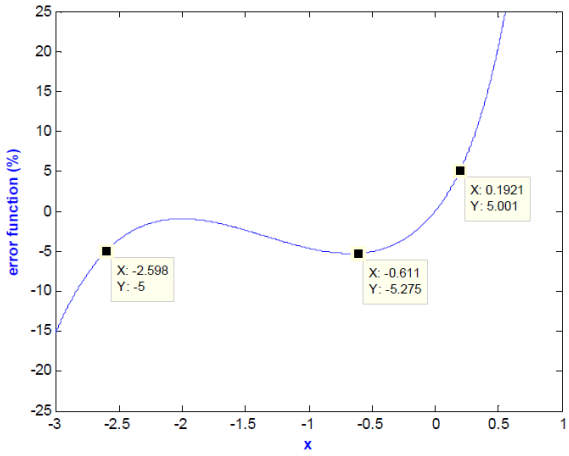

Figure 2.7 : Error function of pseudo exponential approximation with optimizing coefficient (a =0.75 and x <0).

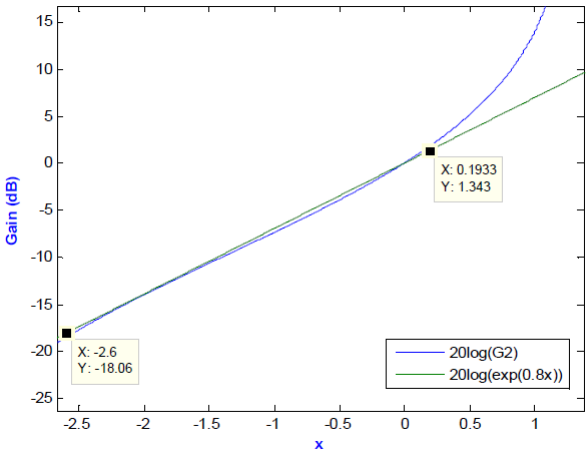

Figure 2.8 : Comparison of the function and ideal exponential function (a =0.75 and x <0).

The range for x is –2.6 to 2.58 for keeping the error between positive and negative five percentages.

2.2.2 United Taylor Series and Pseudo Exponential Approximation

In equation **(2.5)** a composition of Taylor series and pseudo exponential approximation is given [31].

$$e^{x} \approx \frac{k + (1 + ax)^2}{k + (1 - ax)^2} \qquad \textbf{(2.5)}$$

The function is drawn for different k values in Figure 2.9. The function reaches its maximum value for k =0.15 and the range for x is –10 to 10 for keeping the error

between positive and negative five percentages. The comparison of this function and the ideal exponential function is given in Figure 2.10 for k=0.15. The error function is given in Figure 2.11. It is seen that the dynamic range is 60dB.

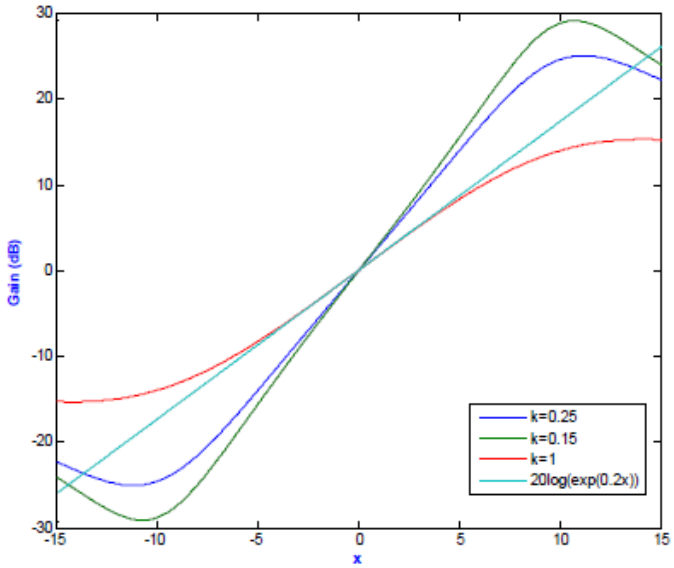

Figure 2.9: Taylor and pseudo exponential approximation values and ideal exponential function for k=0.15, k=0.25 and k=1.

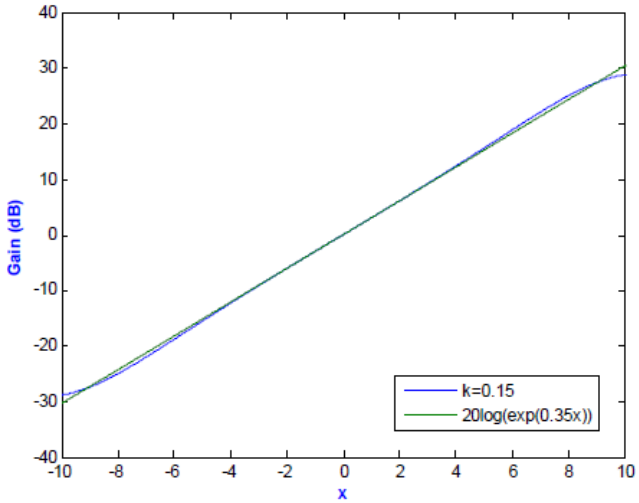

Figure 2.10 : Comparison of Taylor and pseudo exponential approximation values and ideal exponential function for k=0.15.

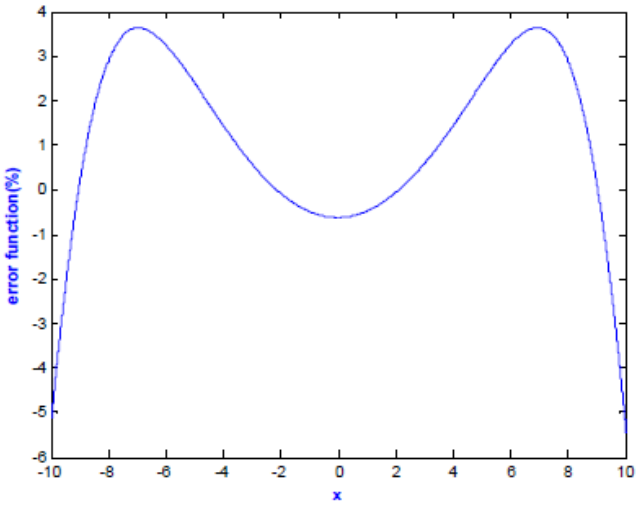

Figure 2.11 : Error function of Taylor and pseudo exponential approximation.

2.3 Pade Approximation

Recently, it is observed that there is connection between some Pade approximants and ideal exponential function [33].

When the Pade table is constructed for the exponential series given in **(2.6)**, the equations given in Table 2.1 are established to represent the function given in **(2.7)** [36].

$$e^{ax} = 1 + \frac{ax}{1!} + \frac{a^2x^2}{2!} + \ldots + \frac{a^n x^n}{n!} + \ldots \qquad \textbf{(2.6)}$$

$$P_{m,n}(x) = \frac{n_m(x)}{d_n(x)} \qquad \textbf{(2.7)}$$

Table 2.1 : A portion of the Pade table for e^x.

$m \backslash n$	0	1	2	3
0	$\frac{1}{1}$	$\frac{1}{1-x}$	$\frac{1}{1-x+\frac{1}{2}x^2}$	$\frac{1}{1-x+\frac{1}{2}x^2-\frac{1}{6}x^3}$
1	$\frac{1+x}{1}$	$\frac{1+\frac{1}{2}x}{1-\frac{1}{2}x}$	$\frac{1+\frac{1}{3}x}{1-\frac{2}{3}x+\frac{1}{6}x^2}$	$\frac{1+\frac{1}{4}x}{1-\frac{3}{4}x+\frac{1}{4}x^2-\frac{1}{24}x^3}$

Table 2.1 (cont'd): A portion of the Pade table for e^x.

m \ n	0	1	2	3
2	$\frac{1+x+\frac{1}{2}x^2}{1}$	$\frac{1+\frac{2}{3}x+\frac{1}{6}x^2}{1-\frac{1}{3}x}$	$\frac{1+\frac{1}{2}x+\frac{1}{12}x^2}{1-\frac{1}{2}x+\frac{1}{12}x^2}$	$\frac{1+\frac{2}{5}x+\frac{1}{20}x^2}{1-\frac{3}{5}x+\frac{1}{20}x^2-\frac{1}{60}x^3}$
3	$\frac{1-x+\frac{1}{2}x^2-\frac{1}{6}}{1}$	$\frac{1+\frac{3}{4}x+\frac{1}{4}x^2+\frac{1}{24}x^3}{1-\frac{1}{4}x}$	$\frac{1+\frac{3}{5}x+\frac{1}{20}x^2+\frac{1}{60}x^3}{1-\frac{2}{5}x+\frac{1}{20}x^2}$	$\frac{1+\frac{1}{2}x+\frac{1}{10}x^2+\frac{1}{120}x^3}{1-\frac{1}{2}x+\frac{1}{10}x^2-\frac{1}{120}x^3}$

By using MATLAB and for m=2 and n=2, the error function is drawn in Figure 2.12 and the comparison between ideal exponential function and pseudo exponential approximation function is drawn in Figure 2.13. Input ranges are given in Table 2.2 for different m and n values.

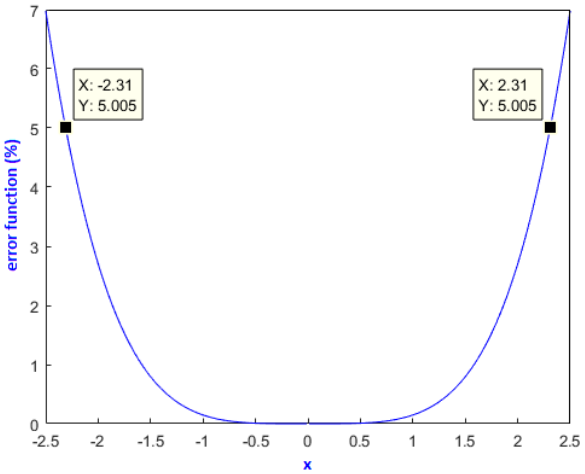

Figure 2.12 : Error function of Pade approximation.

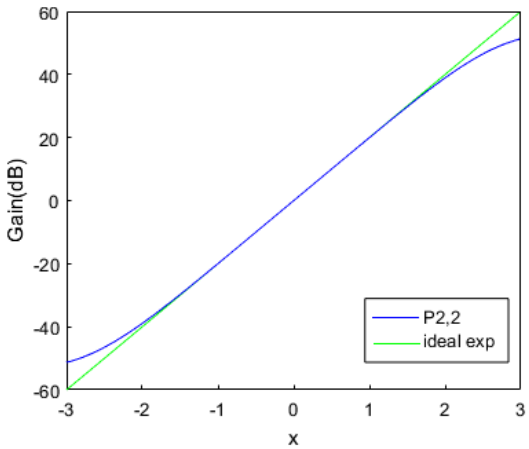

Figure 2.13 : Comparison of ideal exponential functionand Pade approximation function for m=2, n=2.

Table 2.2 : Input ranges of Pade functions for different m and n values.

m,n	Function	Input Range
0,0	1	±0.06
0,1	$\frac{1}{1-x}$	±0.3
0,2	$\frac{2}{2-2x+x^2}$	±0.6
1,0	$1+x$	±0.3
1,1	$\frac{2+x}{2-x}$	±0.85
1,2	$\frac{6+2x}{6-4x+x^2}$	±1.285
2,0	$\frac{2+2x+x^2}{2}$	±0.6
2,1	$\frac{6+4x+x^2}{6-2x}$	±1.285
2,2	$\frac{12+6x+x^2}{12-6x+x^2}$	±2.03

These Pade approximation functions are obtained by extending the Taylor polynomial approximation to rational functions. Coparison of Taylor series approximation and Pade approximation is given in Figure 2.14.

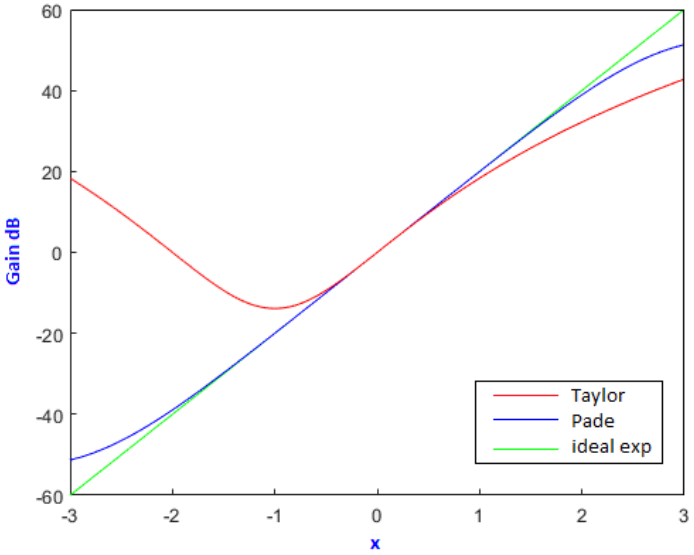

Figure 2.14 : Comparison of Taylor series approximation and Pade approximation.

In Figure 2.14 the order of the Taylor series approximation function n,equals to 2 and the order of Pade approximation's numerator, m and denominator n also equal to 2. For the same order of equations, it is obvious that Pade approximation is more accurate for a larger interval.

In order to obtain an improved performance, an immediate approach is to increase the order of the Taylor approximation. However, in case the order is set to 3 or higher, the corresponding circuit requires building blocks realizing x^3 terms whichcan be usually realized using complicated circuitry compared to x^2 or x^4 terms. This is because the voltage-current transfer characteristic of the MOSFET obeys the square-law characteristic, thus CMOS circuits have simpler circuit implementation of x^2 and x^4 terms. Hence, very effective and high-performance squarer circuits are already presentedin the literature. On the other hand, asshown in Figure 2.15, the rational Pade functions of second-orderprovides similar or better errors performance compared to third order Taylor approximation. This is the main motivation of using Pade approximations in the realization of the exponential function generator.

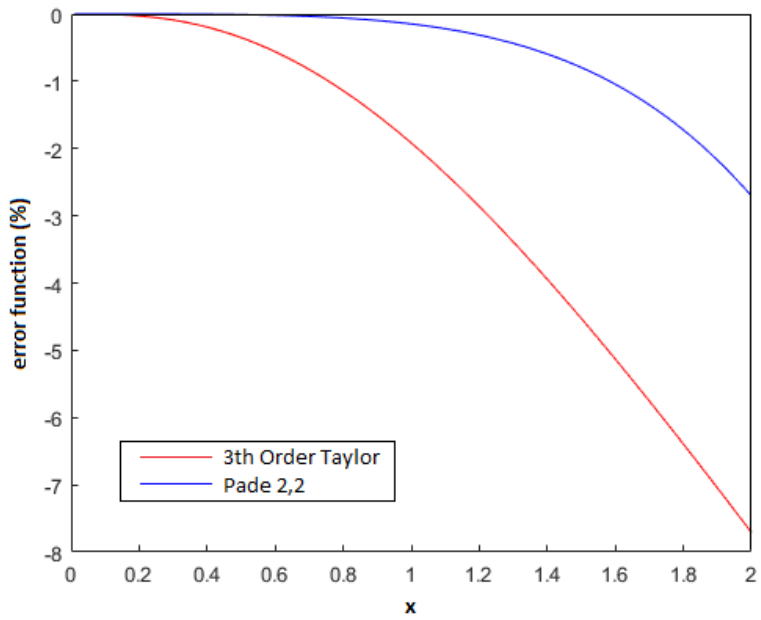

Figure 2.15 : Error function of Taylor series approximation and Pade approximation.

It can be argued that the rational form of the Pade function complicated the design, which in fact is not true. This is because in the any multiplier block, input-output characteristic is inherently of rational form, e.g. for current-mode multipliers:

$$Iout = \frac{Ix.Iy}{I0}. \qquad \textbf{(2.8)}$$

Therefore, we think that the general rational form of Pade approximation does not implies any difficulties in circuit implementation.

Considering all the above discussion, in this thesis work, instead of using a higher order Taylor series approximation, Pade approximation is preferred as the base approximation function.

3. EXPONENTIAL FUNCTION GENERATOR (EXPFG) EXAMPLES

3.1 A Pseudo-Exponential Function Generator

An exponential function generator using a composition of Taylor series and pseudo-exponential function approximation is presented in [25]. The method is based on a new approximation formula given in equation **(3.1)**.

$$e^x = ax^4 + bx^2 + cx + d \tag{3.1}$$

In this formula the coefficients "a" and "d" are to be optimized. This method is considered instead of the conventional Taylor approximation or "pseudo-exponential approximations because it is simpler and more accurate to implement x^4 or x^2 than to implement a rational function. The coefficient x^3 is very close to zero and eliminated with an acceptable approximation.

Another method used in this design is a technique that is used to improve the accuracy. The input signal range is decreased by halving the amplitude of the input signal. For a smaller input signal range the circuit approximates the exponential function with a better accuracy. The output signal is then squared to compensate decreased signal range. The equation for this technique is given in (3.2).

$$e^x = (e^{0.5x})^2 \tag{3.2}$$

The blocked diagram of the circuit is given in Figure 3.1. Here the coefficients a, b c and d are selected as 0.01214, -0.1129, 1.332 and 0.5388 respectively for the equation of $e^{0.5x}$. The simulation result of the circuit is given in Figure 3.2. It can be seen that the circuit achieves a 78dB output range.

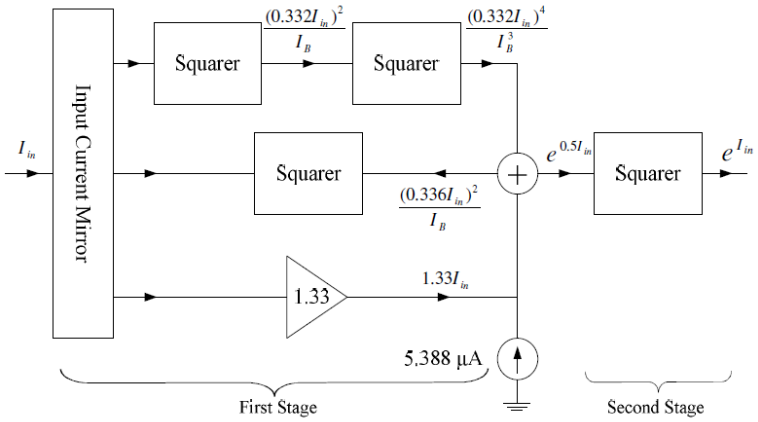

Figure 3.1 : The block diagram of EXPFG [25].

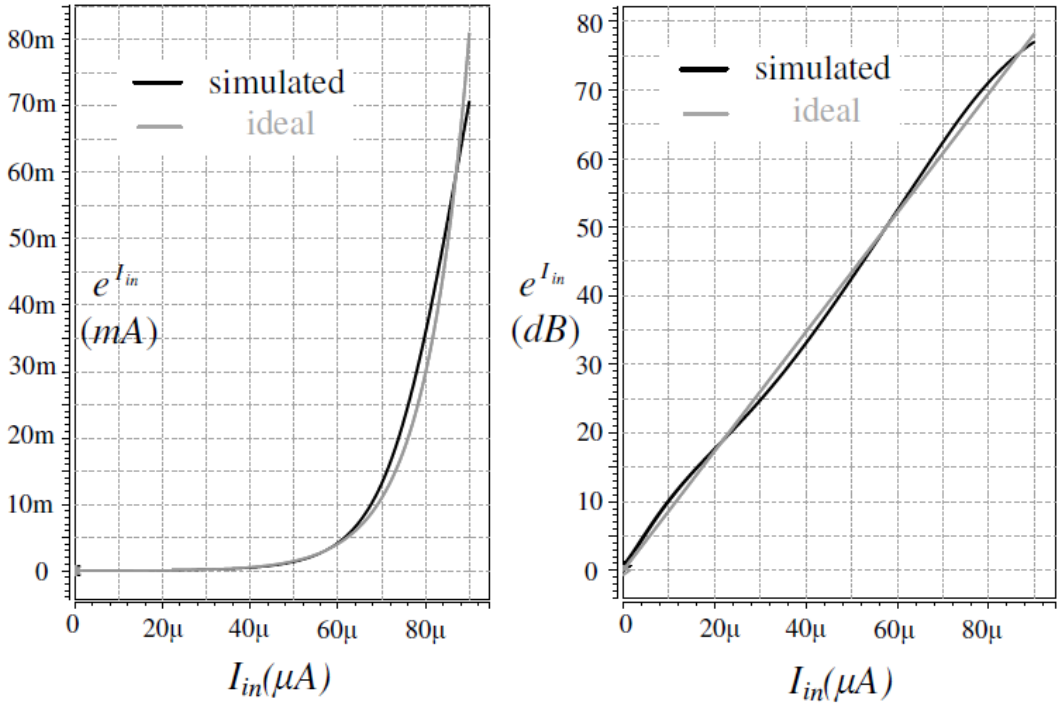

Figure 3.2 : The simulation result of the proposed circuit [25].

3.2 A Superior Order Taylor Series Approximation Exponential Function Generator

An exponential function generator using a superior order of Taylor series is presented in [24]. The method is based on the formula given in equation (3.3).

$$e^x \cong 1 + x + \frac{x^2}{2} + \frac{x^3}{6} + \ldots, \text{ for x<<1} \qquad \textbf{(3.3)}$$

The ratio of currents, input current I_{IN} and the reference current I_O is used as expansion variable and the equation (3.3) is written again as equation **(3.4)**.

$$I_O \exp\left(\frac{I_{IN}}{I_O}\right) \cong I_O\left[1+\frac{I_{IN}}{I_O}+\frac{1}{2}\left(\frac{I_{IN}}{I_O}\right)^2+\frac{1}{6}\left(\frac{I_{IN}}{I_O}\right)^3\right]+\ldots \qquad \textbf{(3.4)}$$

The circuit is designed using a squaring CMOS circuits. The block diagram of the n-thorder polynomial series expansion of exponential function is given in Figure 3.3. A block is used to compute the a_k coefficients for $k = 0,1,\ldots,n+1$. By increasing the value of n, the precision of the circuit can be increased.

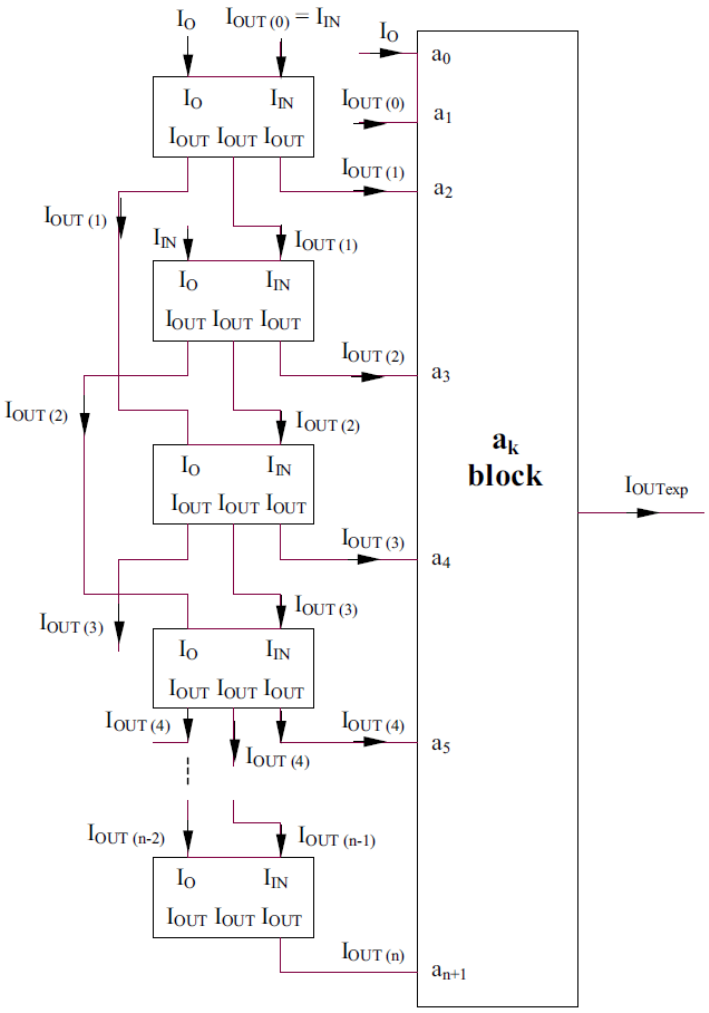

Figure 3.3 : The block diagram of EXPFG [24].

Simulationresults for n=3 confirmed that the pseudo-exponential function genetrator circuit works as expected.

3.3 A New United Taylor Series and Pseudo Exponential Approximation

A new composition of pseudo-exponential, 4th-order Taylor series and coefficient optimization is proposed in [35]. The equation is given below in (3.5).

$$e^x \approx \frac{0.025 + (1 + 0.125x)^4}{0.025 + (1 - 0.125x)^4} \tag{3.5}$$

The circuit is realized by generating the numerator and the denominator functions separately by using squaring circuits. These functions are divided by using a Single-Quadrant Divider to receive the exponential output signal. The block diagram of the designed circuit is given in Figure 3.4.

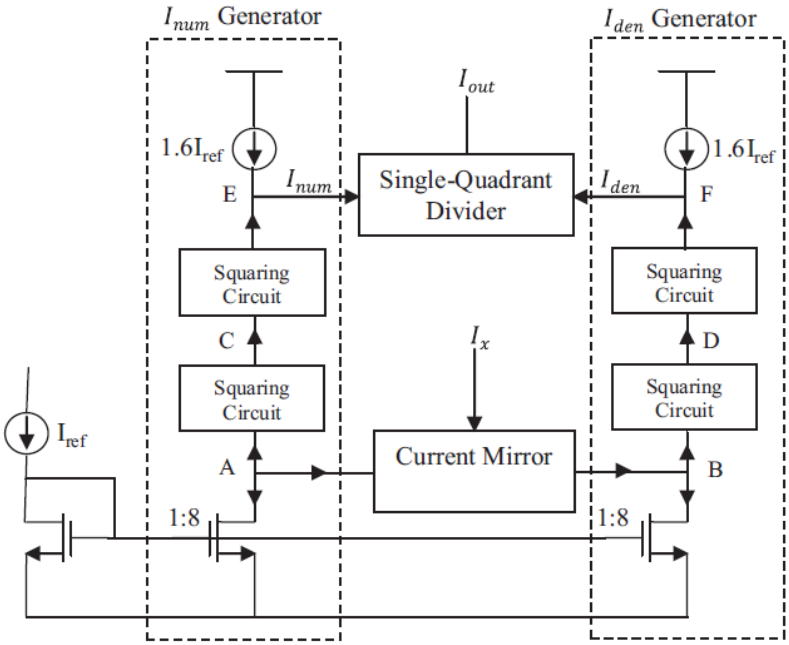

Figure 3.4 : The block diagram of the proposed EXPFG [35].

The simulation results for the proposed circuit is given in Figure 3.5. The circuit has an input range of x as -5.75 to 5.75 and the output range is measured 96dB.

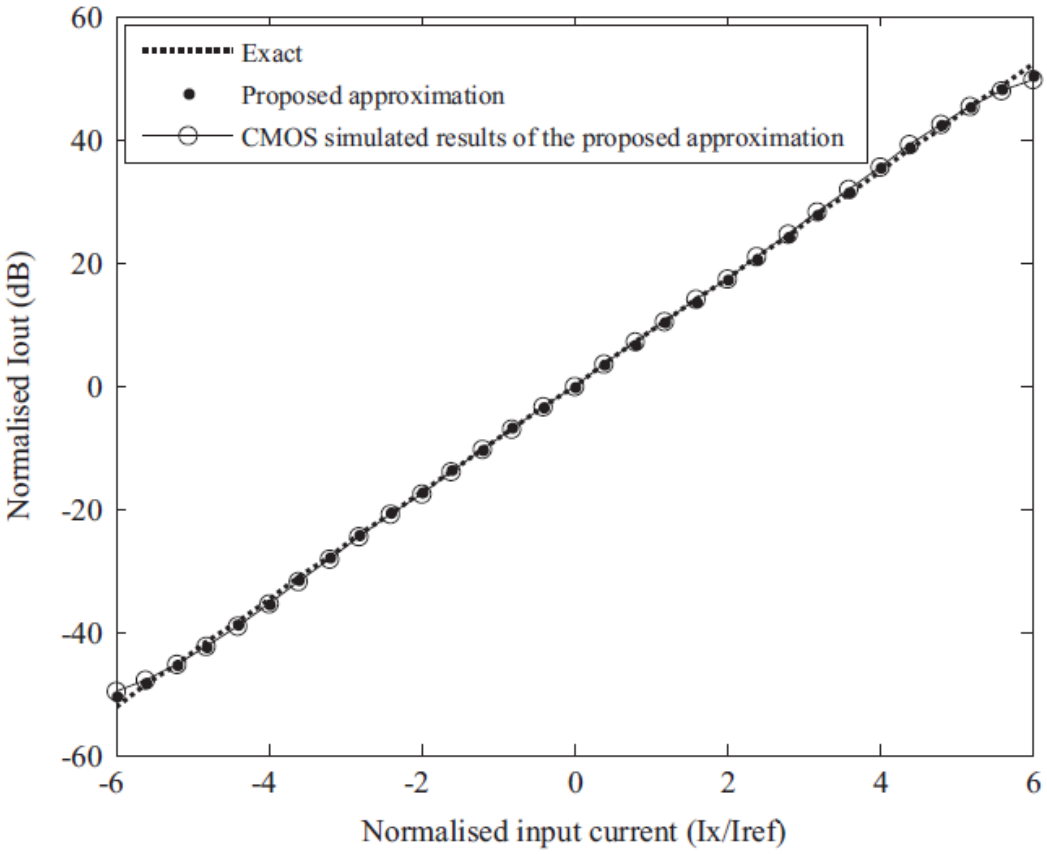

Figure 3.5 : Linear-in-dB characteristic of the proposed EXPFG [35].

3.4 Performance Comparison Between Different Exponential Approximations Approaches

Performance comparison between different exponential approximations approaches found in literature is given in Table 3.1. It is obvious that for the higher order of the equation, the output precision is also higher.

Table 3.1 : Performance comparison between different exponential approximations approaches.

Approximation	Equation	Input Range	Output Range (dB)
2nd order Taylor series [37]	$1 + x + \frac{1}{2}x^2$	-0.6≤ x ≤0.85	13
4th order Taylor series [38]	$1 + x + \frac{1}{2}x^2 + \frac{1}{3!}x^2 + \frac{1}{4!}x^4$	-1.2 ≤ x ≤ 2.0	30
Pseudo exponential [39]	$\frac{1+0.5x}{1-0.5x}$	-0.85 ≤ x ≤0.85	14.8
Pseudo-Taylor approximation (m=1) [32]	$\frac{m+(1+0.5x)^2}{m+(1-0.5x)^2}$	-1.08 ≤ x ≤ 1.08	17.8

Table 3.1 (cont'd): Performance comparison between different exponential approximations approaches.

Approximation	Equation	Input Range	Output Range (dB)
Pseudo-Taylor approximation (m=0.82) [32]	$\frac{m+(1+0.5x)^2}{m+(1-0.5x)^2}$	$-1.63 \le x \le 1.63$	27.2
Modified Pseudo-Taylor approximation [29]	$\frac{0.12+(1+0.25x)^2}{0.12+(1-0.25x)^2}$	$-3.1 \le x \le 3.1$	56
Rational function approximation [40]	$\frac{-0.026ax+(1+0.25ax)^2}{0.026ax+(1-0.25ax)^2}$	$-3.3 \le x \le 3.3$	60
Pseudo exponential [25]	ax^4+bx^2+cx+d	-	74
Pseudo-Taylor approximation [35]	$\frac{0.025+(1+0.125x)^4}{0.025+(1-0.125x)^4}$	$-5.75 \le x \le 5.75$	96

4. DESING OF A NEW EXPFG USING PADE APPROXIMATION

An exponential function generator based on Pade Approximation is proposed in this thesis work. A current-mode, simple-structured circuit is designed in this manner and high dynamic output range is achieved.

4.1 A New Exponential Function Approximation Using Pade Approximation

Pade approximation functions are obtained by extending the Taylor polynomial approximation to rational functions. Calculations showed that using the Pade approximation function with same degree of numerator and denominator gives better result than polynomial method for the same amount of computation effort [33].

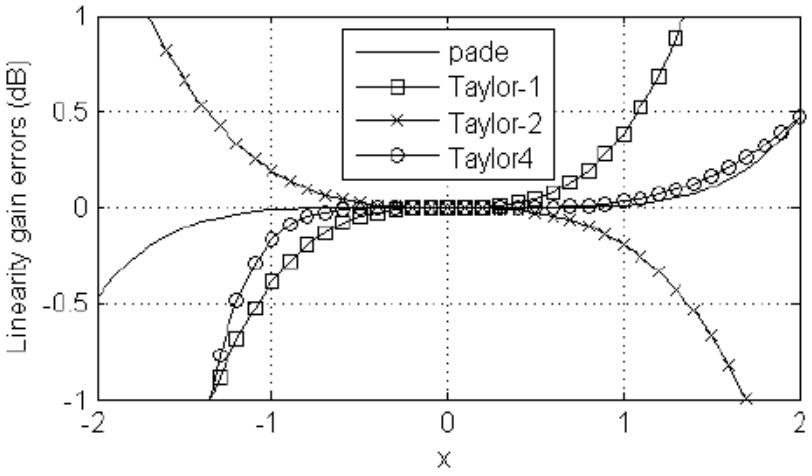

Figure 4.1 : Linearity gain errors of exponential function approximations [33].

In Figure 4.1 the linearity gain errors of different approximation functions are presented. "pade" function is the Pade approximation of e^x with 2,2 order, which is given in **(4.1)**.

$$e^x \approx \frac{1+\frac{x}{2}+\frac{x^2}{12}}{1-\frac{x}{2}+\frac{x^2}{12}} \qquad \textbf{(4.1)}$$

The function named "Taylor-1" represents the pseudo-exponential approximation given in **(4.2)**.

$$e^{x} = \frac{e^{x/2}}{e^{-x/2}} \approx \frac{1 + \frac{x}{2} + \frac{x^2}{8}}{1 - \frac{x}{2} + \frac{x^2}{8}} \tag{4.2}$$

The function named "Taylor-2" represents the pseudo-exponential approximation given in **(4.3)**.

$$e^{x} = \frac{(e^{x/4})^2}{(e^{-x/4})^2} \approx \frac{(1 + \frac{x}{4})^2}{(1 - \frac{x}{4})^2} \tag{4.3}$$

And, "Taylor4" is the 4th order Taylor series approximation given in **(4.4)** [39].

$$e^{x} \approx 1 + \frac{x}{1!} + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} \tag{4.4}$$

The input range and the output dynamic ranges varies -1.2 to 1.2, -1.3 to 1.3, -1.25 to 1.25 and -2.0 to 2.0 for Taylor-1, Taylor-2, Taylor4 and Pade respectively. It is shown in [33] that 35.4dB output range can be achieved with a simple circuitry, which is higher than the output range of Taylor-2, 23.4dB.

A combination of pseudo-Taylor approximation, where $e^{x} = e^{0.5x} / e^{-0.5x}$, and Pade approximation is proposed in this work and the equation is modified as below.

$$e^{x} = \sqrt{e^{x}}\sqrt{e^{x}} \tag{4.5}$$

Using MATLAB for calculations, it is found out that instead of using the same Pade function e.g. $Pade_{2,2}$ twice in **(4.5)**, using conjugate pairs gives better result. The approximations functions are shown in Figure 3.2.

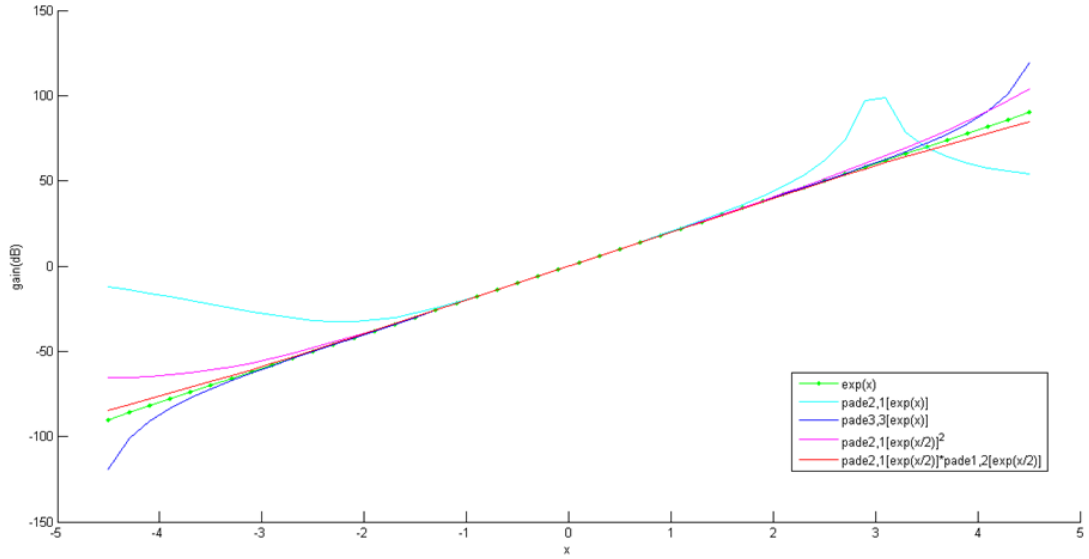

Figure 4.2 : Pade Approximations with different numerator and denominator orders.

In Figure 4.2, $Pade_{2,1}[exp(x)]$, $Pade_{3,3}[exp(x)]$, $Pade_{2,1}[exp(x/2)]^2$ and $Pade_{2,1}[exp(x/2)]$ * $Pade_{1,2}[exp(x/2)]$ represents the equations **(4.6)**, **(4.7)**, **(4.8)** and **(4.9)** respectively.

$$e^x \approx PADE_{2,1}(x) = \frac{n_2(x)}{d_2(x)} \tag{4.6}$$

$$e^x \approx PADE_{3,3}(x) = \frac{n_3(x)}{d_3(x)} \tag{4.7}$$

$$e^x \approx \sqrt{PADE_{2,1}(x)}\sqrt{PADE_{2,1}(x)} \tag{4.8}$$

$$e^x \approx \sqrt{PADE_{1,2}(x)}\sqrt{PADE_{2,1}(x)} \tag{4.9}$$

Where,

$$e^x \approx PADE_{1,2}(x) = \frac{n_1(x)}{d_1(x)} \tag{4.10}$$

It can be easily seen that Equation **(4.9)** gives a better result. Input ranges for these functions are given in Table 4.1 for dirrent m and n values.

Table 4.1 : Input ranges of different combination of exponential function approximations with Pade functions of e^x.

$P_{m,n}$ x $P_{m,n}$	Function	Input Range
$P_{0,2}$ x $P_{0,2}$	$\frac{8}{8-4x+x^2}.\frac{8}{8-4x+x^2}$	±0.99
$P_{1,1}$ x $P_{1,1}$	$\frac{4+x}{4-x}.\frac{4+x}{4-x}$	±1.36
$P_{1,2}$ x $P_{1,2}$	$\frac{24+4x}{24-8x+x^2}.\frac{24+4x}{24-8x+x^2}$	±2.2
$P_{2,0}$ x $P_{2,0}$	$\frac{8+4x+x^2}{8}.\frac{8+4x+x^2}{8}$	±0.99
$P_{2,1}$ x $P_{2,1}$	$\frac{24+8x+x^2}{24-4x}.\frac{24+8x+x^2}{24-4x}$	±2.2
.$P_{2,2}$x $P_{2,2}$	$\frac{48+12x+x^2}{48-12x+x^2}.\frac{48+12x+x^2}{48-12x+x^2}$	±3.551
$P_{0,2}$ x $P_{2,0}$	$\frac{8}{8-4x+x^2}.\frac{8+4x+x^2}{8}$	±1.1
$P_{2,1}$ x $P_{1,2}$	$\frac{24+8x+x^2}{24-4x}.\frac{24+4x}{24-8x+x^2}$	±3.05

4.2 EXPFG Generator Circuit Using $PADE_{(2,1)x(1,2)}$

4.2.1 Circuit Design

To implement Equation **(4.9)**, the ratio of input current I_x and the reference current I_{ref} is used as expansion variable in the system below. $x = \frac{I_x}{I_{ref}}$

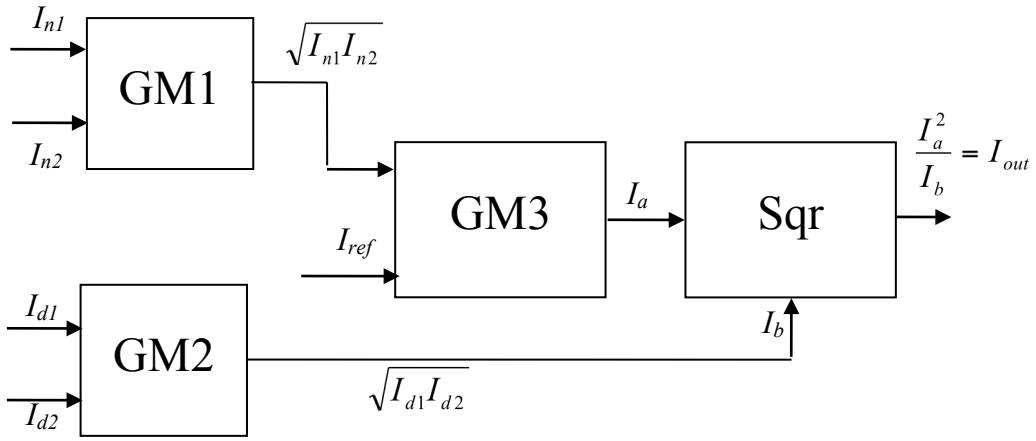

Figure 4.3 : The block diagram of the proposed exponential function generator.

"GM" blocks represent the 2-input geometric mean circuits and "Sqr" represents a squarer circuit. The output current of the circuit above is given in equation **(4.11)**, which is the circuit implementation of equation **(4.9)**.

$$I_{out} = \sqrt{\frac{I_{n1}}{I_{d1}}}\sqrt{\frac{I_{n2}}{I_{d2}}} = \frac{\sqrt{I_{n1}I_{n2}}}{\sqrt{I_{d1}I_{d2}}} \qquad \textbf{(4.11)}$$

4.2.2 Multiplier/Divider

Thecurrent-mode analogue multiplier/divider circuit in [41], which consists of a geometric mean block and a squarer block, is usedfor implementation.Figure 4.4 shows the operation principle of the multiplier/diverdir circuit.

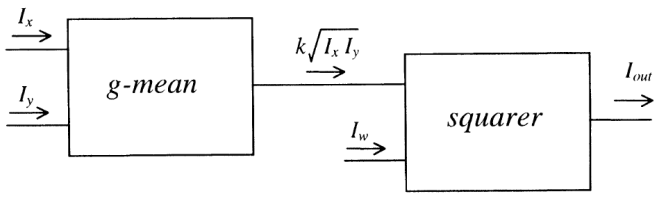

Figure 4.4 : Principle of multiplier/divider circuit [41].

The input-output characteristic of the multiplier/divider is given below.

$$I_{out} = \frac{I_x I_y}{I_w} \qquad \textbf{(4.12)}$$

This structure is very suitable for this work hence multiple g-mean circuits and a squarer can be used to form the exponential function generator circuit.

The transistor level circuit scheme of the multiplier for k=2 is shown in Figure 3.5.

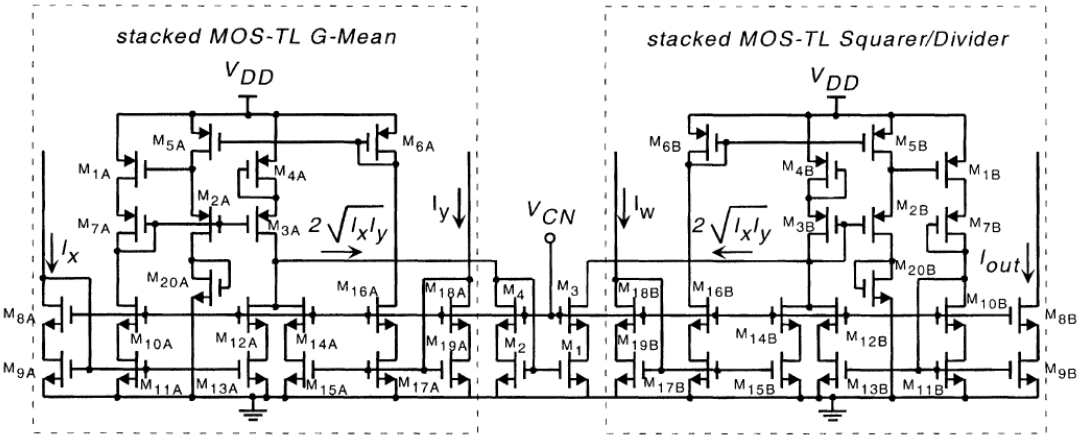

Figure 4.5 : Circuit scheme of multiplier/divider circuit [41].

In this circuit, transistors M1, M2, M3 and M4 generate the translinear stacked topology given in Figure 3.6 [41].

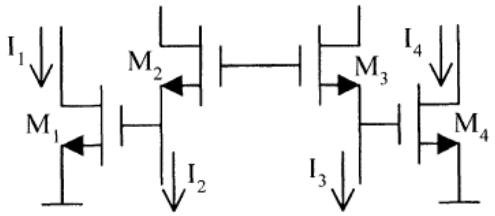

Figure 4.6 : Stacked topology [41].

Assuming all transistors are operating in saturation region and applying KVL, equation **(4.13)** can be written.

$$\sqrt{\frac{I_1}{(W_1/L_1)}}+\sqrt{\frac{I_2}{(W_2/L_2)}}=\sqrt{\frac{I_3}{(W_3/L_3)}}+\sqrt{\frac{I_4}{(W_4/L_4)}} \qquad \textbf{(4.23)}$$

The aspect ratios are chosen as below for k=2.

$$k^2\frac{W_1}{L_1}=k^2\frac{W_2}{L_2}=\frac{W_3}{L_3}=\frac{W_4}{L_4} \qquad \textbf{(4.34)}$$

Multiplier/Divider circuit is designed in 0.35µm CMOS process and simulated by using SPICE. The circuit schematic is shown in Figure 3.7.

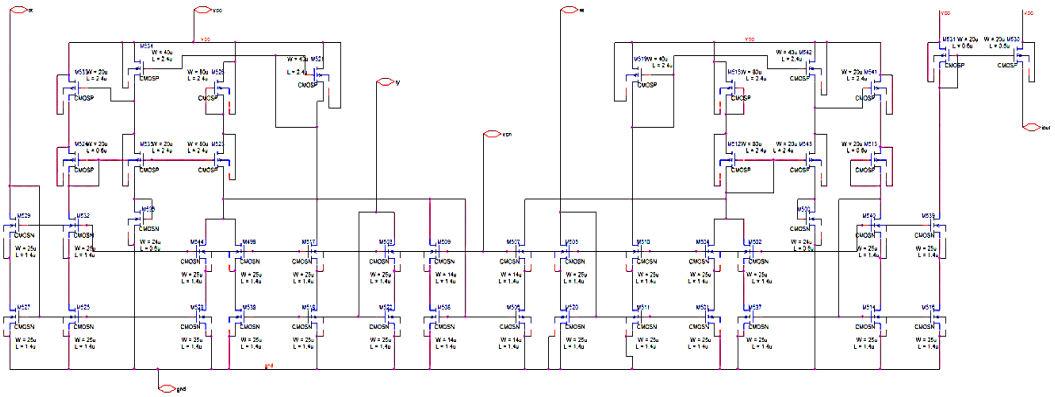

Figure 4.7 : Schematic of the Multiplier/Divider circuit.

The dimentions of the transistors in the circuit shown in Figure 4.7 are given in Table 4.2.

Table 4.2: Device dimentions of the designed multiplier/divider.

Transistor	W (µm)	L (µm)
M_{1A-2A}	20	2.4
M_{3A-4A}	80	2.4
M_{5A-6A}	40	2.4
M_{7A}	20	0.6
M_{8A-19A}	25	1.4
M_{20A}	24	0.6
M_{1-4}	14	1.4

The simulation result is given in Figure 4.8. It can be seen that the results are as expected.

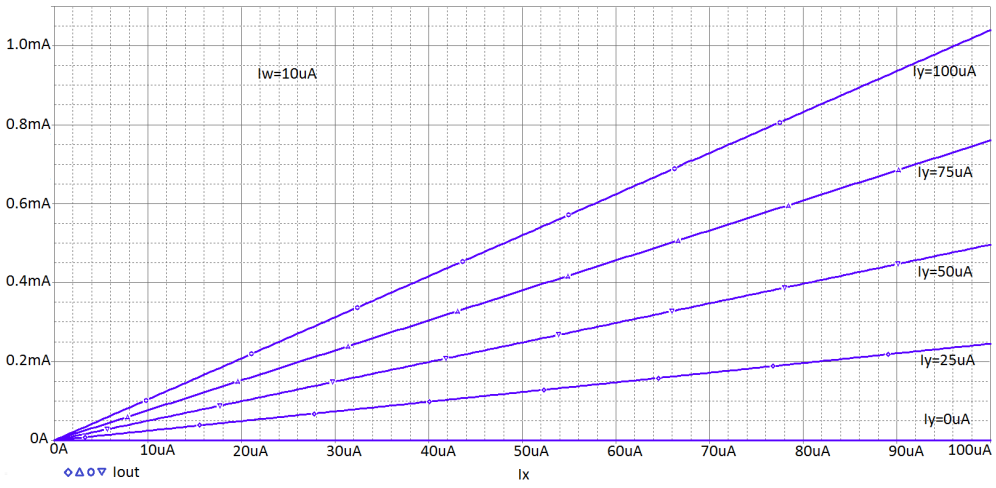

Figure 4.8 : Simulation result of the Multiplier/Divider circuit.

4.2.3 Circuit Realisation and Simulation Results

According to the Pade Table $PADE_{1,2}$ and $PADE_{2,1}$ functions are given below [42].

$$PADE_{1,2}(x) = \frac{n_1(x)}{d_1(x)} = \frac{6+2x}{6-4x+x^2} \tag{4.15}$$

$$PADE_{2,1}(x) = \frac{n_1(x)}{d_1(x)} = \frac{6+4x+x^2}{6-2x} \tag{4.16}$$

For $= \frac{I_x}{I_{ref}}$, these equatios can be written as **(4.18)** and **(4.20)**, where the coefficients are also divided to 2 for device size considerations.

$$PADE_{1,2}(x) = \frac{n_1(x)}{d_1(x)} = \frac{6+2\dfrac{I_x}{I_{ref}}}{6-4\dfrac{I_x}{I_{ref}}+(\dfrac{I_x}{I_{ref}})^2} \tag{4.17}$$

$$I_{PADE_{1,2}} = \frac{I_{n_1}}{I_{d_1}} = \frac{3I_{ref}+I_x}{3I_{ref}-2I_x+\dfrac{I_x{}^2}{2I_{ref}}} \tag{4.18}$$

$$PADE_{2,1}(x) = \frac{n_2(x)}{d_2(x)} = \frac{6+4\dfrac{I_x}{I_{ref}}+(\dfrac{I_x}{I_{ref}})^2}{6-2\dfrac{I_x}{I_{ref}}} \tag{4.19}$$

$$I_{PADE_{2,1}} = \frac{I_{n_2}}{I_{d_2}} = \frac{3I_{ref}+2I_x+\dfrac{I_x{}^2}{2I_{ref}}}{3I_{ref}-I_x} \tag{4.20}$$

The expected result for $I_{ref} = 10\mu A$ iscalculted and given in Figure 4.9.

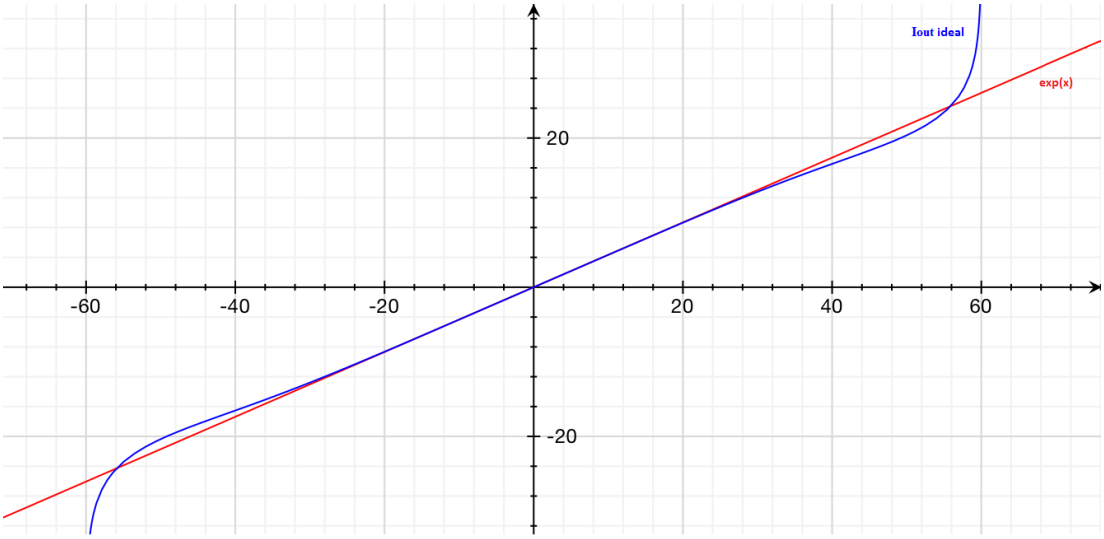

Figure 4.9 : Calculated output of proposed function.

Proposed circuit is designed and simulated by using SPICE to examine the results. n_1 , n_2 , d_1 and d_2 are realised by summation of currents which are produced by current mirrors with proper width factors. Current mode realisation of these functions are given in Figure 4.10.

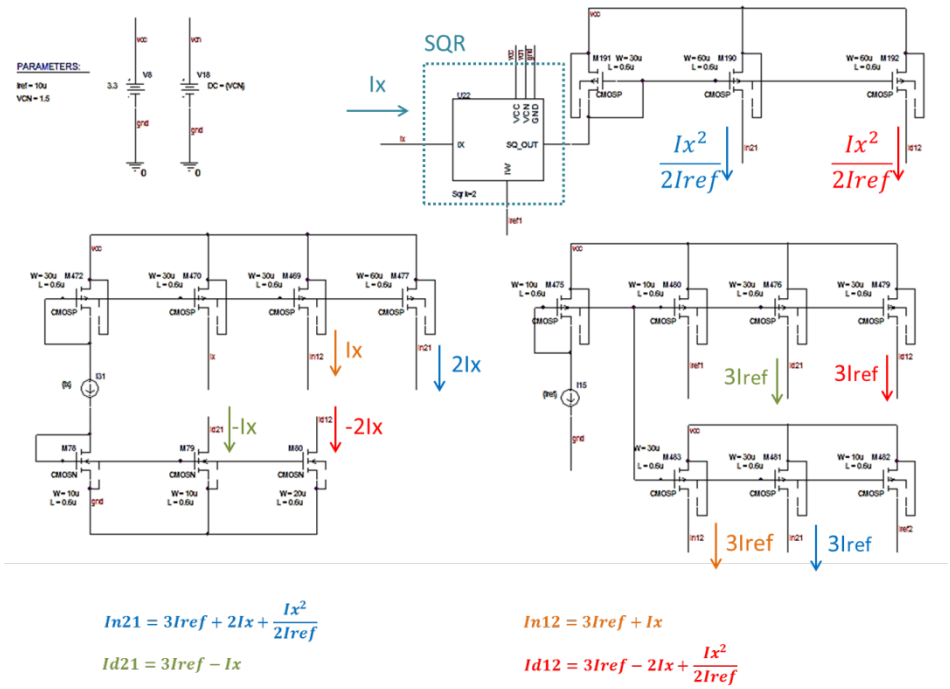

Figure 4.10 : Current mode circuit realization of n_1, n_2 , d_1 and d_2 functions.

Circuit realisation of the block diagram is given in Figure 4.11. Current mirrors are used to change the direction of the output currents of G-mean blocks.

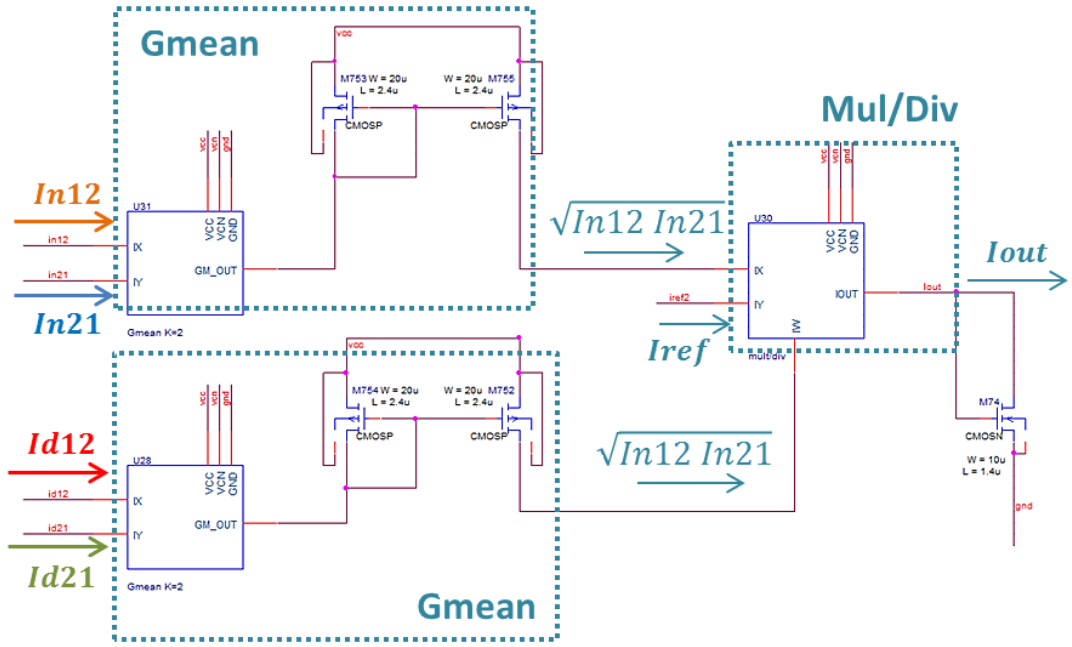

Figure 4.11 : Circuit realization of proposed EXPFG.

The comparison of the ideal exponential function and the gain function of the circuit in Figure 4.11are shown in Figure 4.12. SPICE analysis and the MATLAB results are shown to be agreeing within the gain range of -26.3dB to 26.3dB.

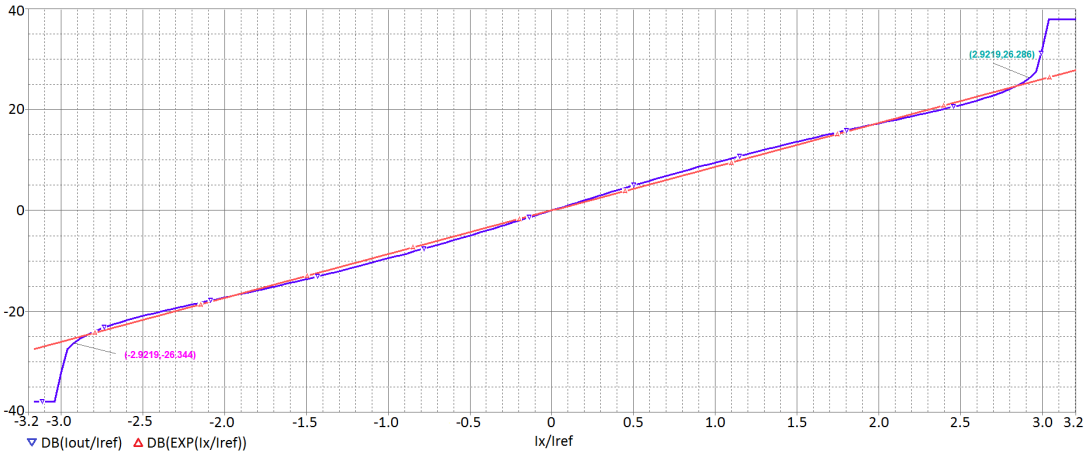

Figure 4.12 : The comparison of the ideal exponential function and the gain function of the circuit in Figure 3.8.

The error function of the output current is given in Figure 4.13. It can be seen easily that the error is always less than 1dB within the -2.9 to 2.9 input range.

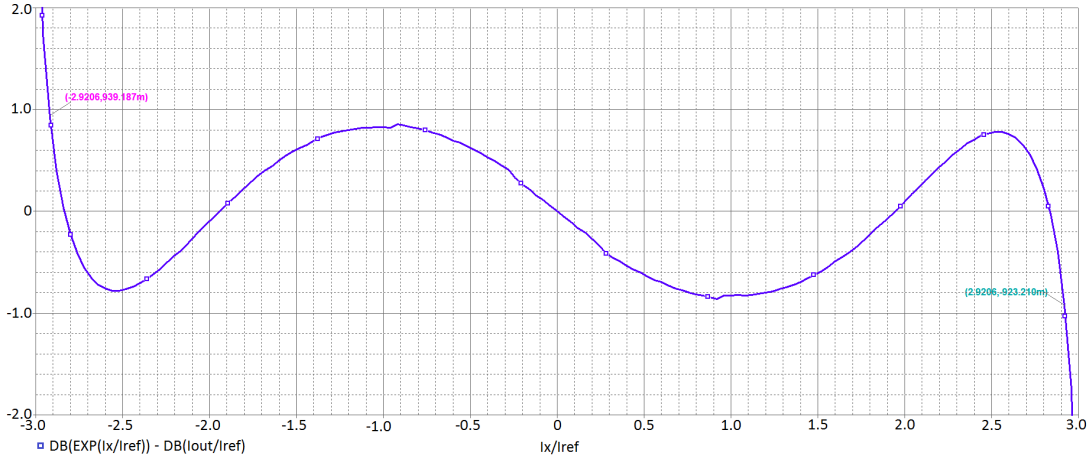

Figure 4.13 : The error function of the output current.

4.3 EXPFG Generator Circuit Using PADE$_{(2,0)x(0,2)}$

Another EXPFG is designed using the function given in **(4.19)**.

$$e^{2x} \approx \frac{4+x+x^2}{8} \cdot \frac{8}{8-4x+x^2} \tag{4.19}$$

For $= \frac{I_x}{I_{ref}}$, these equatios can be written as (4.20).The block diagram of the proposed exponential function generator is given in Figure 4.14.

$$I_{PADE_{2,0}}\left(\frac{x}{2}\right) I_{PADE_{0,2}}\left(\frac{x}{2}\right) = \frac{2I_{ref} + I_X + \frac{{I_X}^2}{4I_{ref}}}{2I_{ref} - I_X + \frac{{I_X}^2}{4I_{ref}}} \tag{4.20}$$

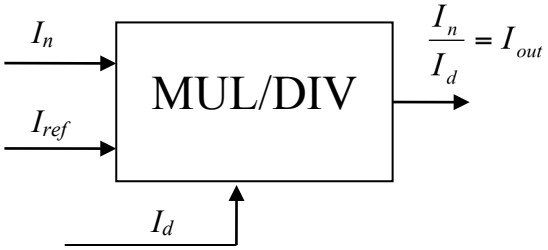

Figure 4.14 : The block diagram of the proposed exponential function generator.

Proposed circuit is designed and simulated by using SPICE to examine the results. Circuit realisation of the block diagram is given in Figure 4.15.

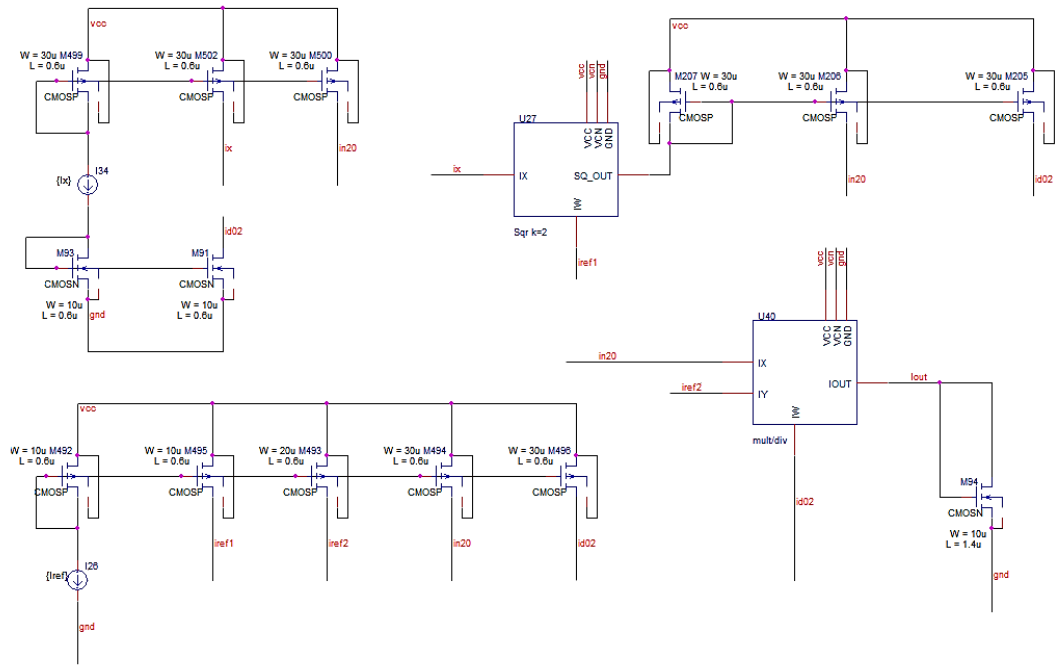

Figure 4.15 : Circuit realization of proposed EXPFG.

The comparison of the ideal exponential function and the gain function of the circuit in Figure 4.15 is shown in Figure 4.16.

SPICE analysis and the MATLAB results are shown to be agreeing within the gain range of -10.3dB to 10.3dB.

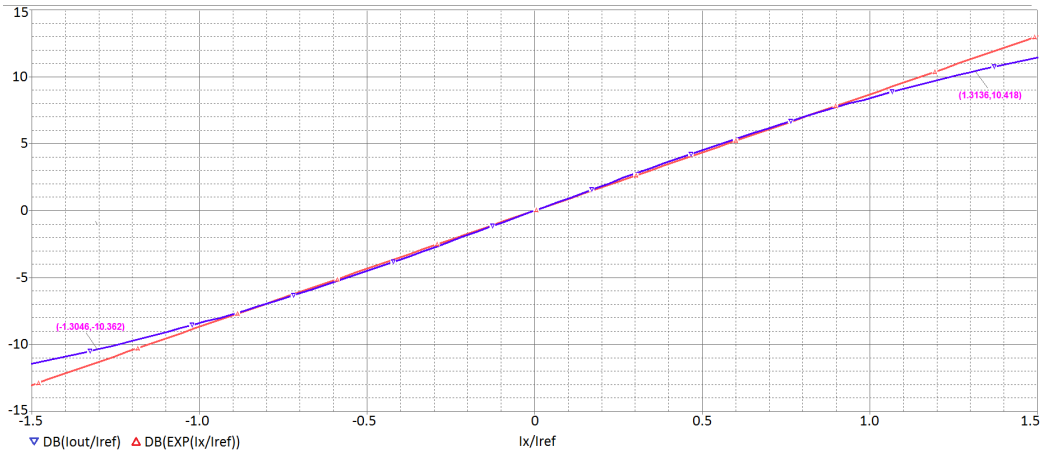

Figure 4.16 : The comparison of the ideal exponential function and the gain function of the circuit in Figure 4.15.

The error function of the output current is given in Figure 4.17. It can be seen easily that the error is always less than 1dB within the -1.3 to 1.3 inputrange.

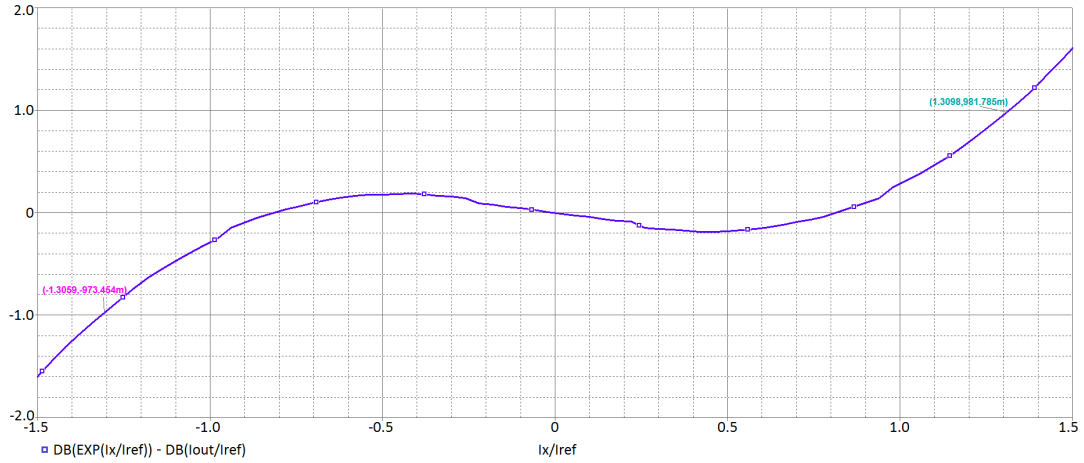

Figure 4.17 : The error function of the output current.

4.4 EXPFG Generator Circuit Using PADE$_{(1,1)}$

Another EXPFG is designed using the function given in **(4.21)**.

$$e^{2x} \approx \frac{4+x}{4-x}.\frac{4+x}{4-x} \tag{4.21}$$

For $= \frac{I_x}{I_{ref}}$, these equatios can be written as (4.22). The block diagram of the proposed exponential function generator is given in Figure 4.18.

$$I_{PADE_{1,1}\left(\frac{x}{2}\right)} I_{PADE_{1,1}\left(\frac{x}{2}\right)} = \left(\frac{4I_{ref}+I_X}{4I_{ref}-I_X}\right)^2 \tag{4.22}$$

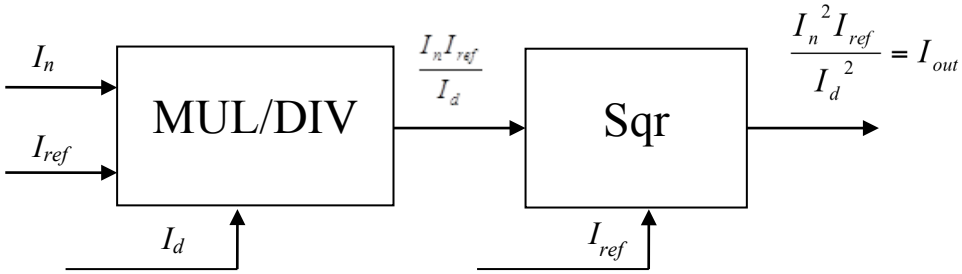

Figure 4.18 : The block diagram of the proposed exponential function generator.

Proposed circuit is designed and simulated by using SPICE to examine the results. Circuit realisation of the block diagram is given in Figure 4.19.

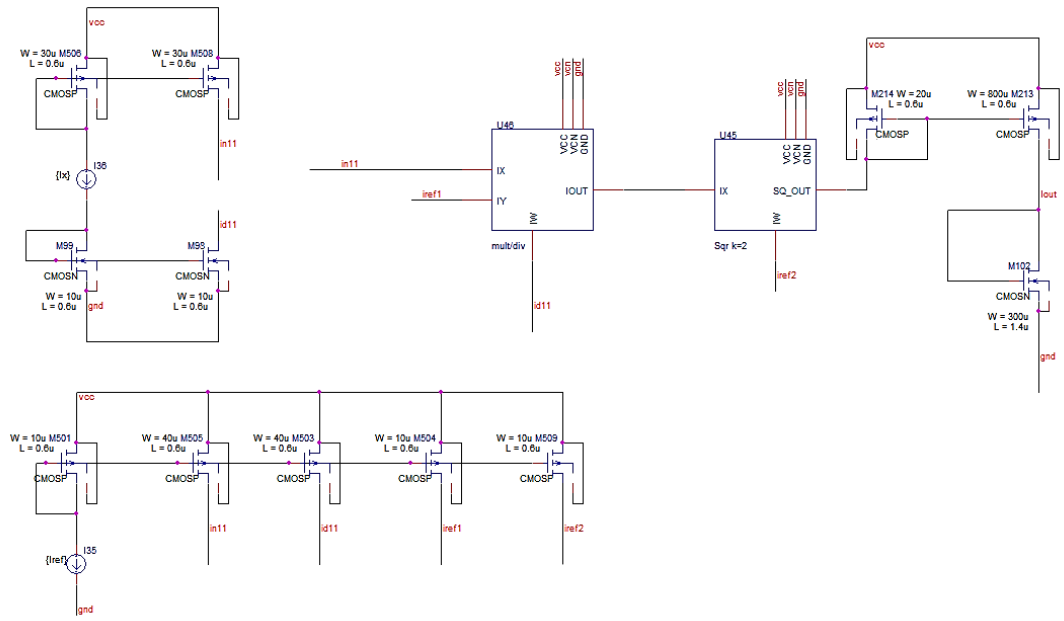

Figure 4.19 : Circuit realization of proposed EXPFG.

The comparison of the ideal exponential function and the gain function of the circuit in Figure 4.19 is shown in Figure 4.20.

SPICE analysis and the MATLAB results are shown to be agreeing within the gain range of -16dB to 16dB.

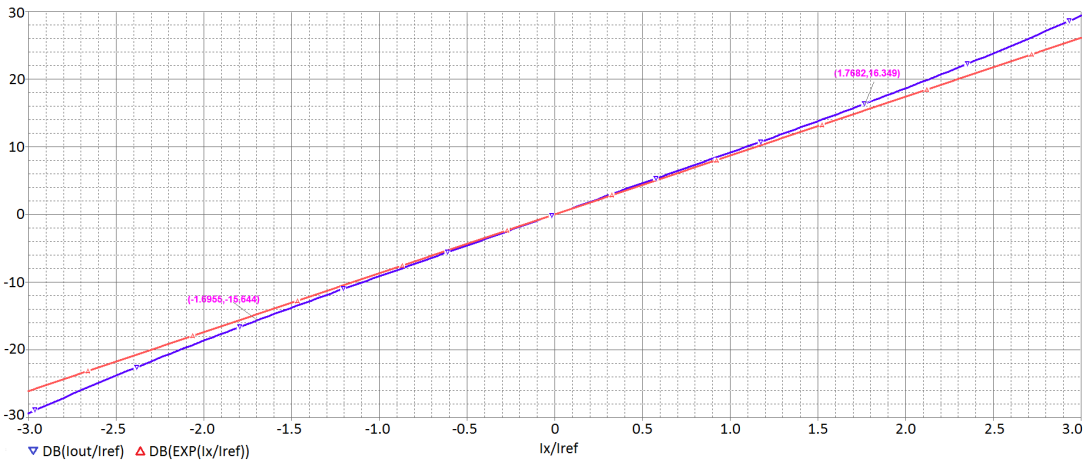

Figure 4.20 : The comparison of the ideal exponential function and the gain function of the circuit in Figure 4.19.

The error function of the output current is given in Figure 4.21. It can be seen easily that the error is always less than 1dB within the -1.7 to 1.7 inputrange.

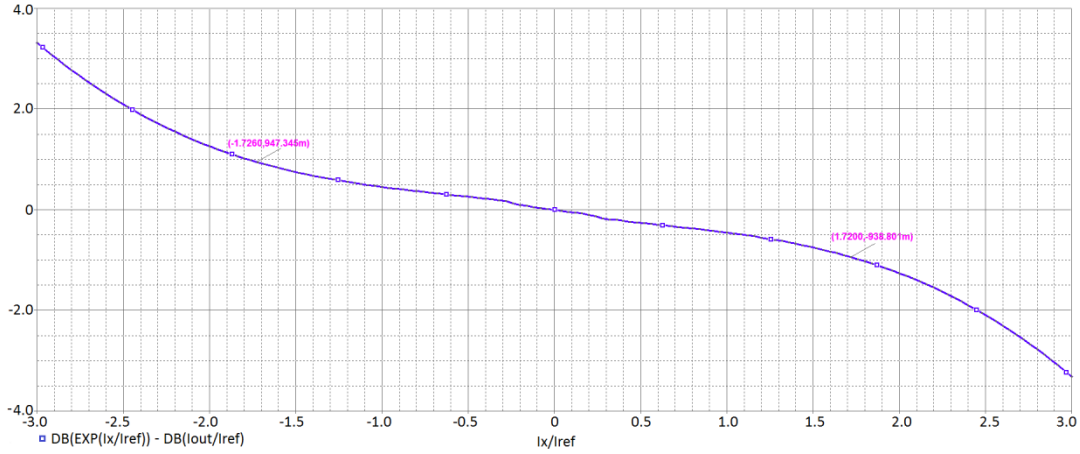

Figure 4.21 : The error function of the output current.

4.5 Chapter Summary

In this chapter, a new Pade Approximation based exponentialfunction approximationis proposed to be used as a methodology to design an exponential function generator. Afterwards, three different exponential function generators are designed using the different orders of numerators and denominators from Pade table. The comparison of the circuits output dynamic range and input range as well as the ideal input range calculated by MATLAB are given in Table 4.3.

Table 4.3: Circuit performance with different Pade functions.

Function	Output range (dB)	Input range (±)	Ideal input range (±)
$P_{2,1}$ x $P_{1,2}$	52.6	2.9	3.05
$P_{2,0}$x $P_{0,2}$	20.6	1.3	1.1
$P_{1,1}$ x $P_{1,1}$	32	1.7	1.36

5. CONCLUSIONS AND RECOMMENDATIONS

Exponential function generators are used to provide control signal to VGA circuits in communication systems where high dynamic range is required. In this thesis work, a comprehensive literature search was performed to examine and classify the exponential function generators according to their approximation functions that are used that are used to realize the exponential signal.

Pade approximation is reported as a new approach forrealizing exponential function in a recent work found in literature, where Taylor series approximation is very common. Using MATLAB for calculations, it is found out that Pade functions of second-order provides similar or better errors performance compared to third order Taylor approximation.In this thesis work, by using the accuracy improvement method mentioned in Section 3 with second order complex conjugate of the equations in Pade table, a new approach is proposed for realizing exponential function.

Three different circuits are designed with different Pade equations, simulated using SPICE. The circuit using $P_{2,1}$ x $P_{1,2}$ equation has 52.5dB output range. The output range can be increased by using Pade functions with higher order of numerator and denominator.

Future works could be to use simpler multiplier/divider architecture with higher performance to reduce the possible die size and increase the dynamic range.

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