İSTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

GaAs pHEMT CLASS-E POWER AMPLIFIER DESIGN

M.Sc. THESIS

Behnoosh MESKOOB

Department of Electronics and Telecommunication Engineering

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

GaAs pHEMT E-SINIFI GÜÇ KÜVVETLENDİRİCİ TASARIMI

YÜKSEK LİSANS TEZİ

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Behnoosh MESKOOB, a M.Sc. student of İTU Graduate School of Science Engineering and Technology student ID 504131223, successfully defended the thesis/dissertation entitled "GaAs pHEMT Class-E Power Amplifier Design", which she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To my parents whom I have my life from them

And to everyone who taught me even one word and brought me one step out from darkness of ignorance into light of knowledge

And yet there is a lot to learn and know…

FOREWORD

Before and after everything, the main thanks goes to The most compassionate, The most Merciful, for each moment of life, for each breath, for each chance of learning, for everything.

My parents are my role models and inventors of my life, so this thesis is dedicated to them. Even if I dedicate my whole life to them, it will never be enough…

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November 2016 Behnoosh Meskoob

TABLE OF CONTENTS

Page

ABBREVIATIONS

ACLR : Adjacent Channel Leakage Ratio
ADS : Advanced Design System
BB : Broad Band
BJT : Bipolar Junction Transistor
DUT : Device Under Test
EER : Envelope Elimination and Restoration
FL : Flicker Noise
GaAs : Galium Arsenide
GHz : Giga Hertz
GSM : Global System for Mobile communication
HB : Harmonic Balance
HEMT : High Electron Mobility Transistor
IMD : Inter-Modulation Distortion
InP : Indium Phosphide
LDMOS : Laterally Difused Metal Oxide Semiconductor
LNA : Low Noise Amplifier
LP : Load-Pull
LPCC : Leadless Plastic Chip Carrier
MESFET : Metal Semiconductor Field-Effect Transistor
MHz : Mega Hertz
NL : Non-Linear
NP : Noise Parameter
OIP3 : Third Order Intercept Point
OS : Orientation Selectable
PA : Power Amplifier
PCB : Printed Circuit Board
PD : Pad De-embeding
RF : Radio Frequency
SOT : Small Outline Transistor
UHF : Ultra High Frequency
W : Watts
WCDMA : Wideband Code Division Multiple Access

SYMBOLS

η_{ALL}	**:** Overal Efficiency
P_{OUT}	**:** Output Power
P_{DC}	**:** Power Taken from DC Source
P_{IN}	**:** Input Power
L_{CH}	**:** Ideal Choke Inductor
C_b	**:** DC-blocking Capacitor
R_L	**:** Load Resistor
V_{CC}	**:** Voltage taken from DC Source
P_{OUT}	**:** Output Power
V_b	**:** Input DC bias voltage
V_p	**:** Device Pinch-Off Voltage
I_q	**:** Quiescent Current
v_R	**:** Load Voltage
v_{in}	**:** Input Voltage
V	**:** Output Voltage Amplitude
I	**:** Collector/Drain Current Amplitude
f_0	**:** Fundamental Frequency
ξ	**:** Collector/Drain Voltage Peak Factor
Θ	**:** Conduction Angle
P_1	**:** Fundamental Frequency Power
C_{OUT}	**:** Total Capacitor in Shunt/ Output Capacitor of Active Device
ω	**:** Angular Switching Frequency

LIST OF TABLES

Page

LIST OF FIGURES

Page

GaAs pHEMT CLASS-E POWER AMPLIFIER DESIGN

SUMMARY

A basic single-stage power amplifier circuit includes an active device, input matching circuit to match with source impedance, and an output matching circuit to match with load impedance.

In a power apmlifier design, there are important parameters to be considered. These parameters include selection of active device, technology of active device, class of operaiton, intput and output matching network structure design, biasing, range of frequency, operation parameters such as required output power, gain, Power Added Efficiency (PAE), Input and Ouput Insertion Loss, S-parameters, etc. All these parameters shall be considered in the design and reaching design goals will end up in a successful design.

Nowadays with improvements in designing wireless communiction systems with specific applications such as hand-hold wireless devices, space telecommunication subsystems, etc. it is important to have highly reliable, efficient, small-sized systems, given the limited input power source (generally battery), attaining desirable output power level and gain.

The aim of this thesis is designing Class-E and Inverse-Class-E power amplifier with low voltge consumption in UHF band with application in small satellites. One of the main properties of this design is being supplied with only 5V which will result in elimintating a DC-DC down-converter in the next stage of a system. To reach this aim, class-E structure has been selected in order to have maximum possible PAE and high gain with the available input power, and other design specifications which will be discussed and mentioned in details in the text. Besides, Inverse-Class-E structure and a novel mix of Class-E and Inverse-Class-E has also been designed and tested to compare the function of each structure. Suitable transistor (available in market) and active device technology has been selected, different input and output matching networks have been designed and examined, biasing network has been designed carefully, and satisfying results for the given design goals has been achieved. Advanced Design System 2015.01 (ADS) is the software used for the design and circuits prepared and tested in RF Electronics Laboratory of Istanbul Technical University.

The challenges of this project was designing Class-E and Inverse-Class-E power amplifier, while having output matching circuit, maintaining design simplicity with low voltage which resulted in very limited choices in using lumped elements. Furthermore, using lumped passive elements transformation into transmission lines is not feasible in UHF band as the lines will be very long and it makes the implementations almost impossible. Therefore, transmission lines were used only between lumped passive elements to make connections. On the other hand, using lumped passive elements resulted in having a very lossy system, that for instance, a

design with PAE=59% turned to PAE=44% after implementing real passive element models and transmission lines.

The main point in designing Class-E and Inverse-Class-E power amplifier is selecting the right biasing point which is almost considered as deep class-AB biasing point and the main affecting part of system is the output matching network. Thus, different output matching networks have been designed and examined and the result is, the simpler the circuit becomes, the higher efficiency can be obtained. Simplicity and using least passive elements were key factors in this design due to using lossy passive element models and the frequency domain.

In this project, GaAs technology has been selected and ATF-511P8 is the active device, from Avago Technologies manufacturer. Process of input and output matching network designs has been presented in appendix .Three designes for Class-E, Inverse-Class-E and mixture of Class-E and Inverse-Class-E has been designed, fabricated and tested. Results indicated the importance of keeping simplicity of design, while satisfying design goals. On the other hand, superiority of functionality for Class-E power amplifier has been proved by having higher PAE than the other two designs. Novelty of this project is using a mixture of Class-E and Inverse-Class-E power amplifier which has been designed and tested for the first time.

1mm thickness standart RF4 substrate is preferred due to durable structure and low cost. According to our previous cube-satellite experiences, it is suitable for low-Earth-orbit (LEO) conditions.

Very few references was found about Inverse-Class-E which shows how implementation of this structure is hard, and not ideally practical. Thus, part of the thesis concentrates on desiging and implementation of this structure. Furthermore, a mixture of Class-E and Inverse-Class-E including series inductance, shunt capacitance and parallel-tuned circuit in the output matching network has been designed, manufactured and tested for the first time. This will give an insight to a new structure for power amplifiers and can be further improved for future works.

Simulated PAEs of Class-E, mixed strucure and Inverse-Class-E designs are 50%, 43% and 37% respectively. Measuremed gain, PAE and output power are slightly different than simulated values. In simulations, higher output power and gain but lower PAE was achieved while in measurements it was vice versa. It is impartant to mention that the mixed design was manufactured for two values of inductors 49nH and 56nH and each of them was measured separately. Measurement PAEs are 35% for Class-E, 40% for Inverse-Class-E, 57% for Mixed Design with 47nH and 37% for Mixed Design with 56nH. All results are presented in detailed at last chapter.

Desinged GaAs amplifiers are suitable for cube-satellite UHF band transmitters due to small size and low voltage stable operation. In a standard cube-satellite, they can be used without an additional DC-DC convertor.

GaAs pHEMT E-SINIFI GÜÇ KÜVVETLENDİRİCİ TASARIMI

ÖZET

Yüksek güçlü RF kuvvetlendiciler mikrodalga sistemlerde genelde verici katında antenden önce yer alır. Bu tür kuvvetlendiricilerin tasarımlarında yüksek frekans elektroniğinin tasarım ilkelerine ek doğrusal olmayan tasarım tekniklerinin de kullanılmak zorundadır.

Bir RF güç kuvvetlendiricisi aktif elemana ek olarak giriş ve çıkış katından oluşur. Giriş ve çıkış katı aynı zamanda transistörün giriş ve çıkış empedansını yük ve kaynağın empedansına uydurmak için kullanılır. Bu sayede transistörün girişe uygulanan güç yansıma kaybı olmadan transistöre aktarılır, transistörde kuvvetlendirilen işaret de yüke aktarılır. Güç kuvvetlendicileri yüksek güç tükettiği için üretilen işaretin kayıpsız olarak aktarılması verimin arttırılması açısından önemlidir.

Bir güç kuvvetlendiricisinin temel özellikleri şunlardır: Çıkış gücü seviyesi, verim, güç kazancı, bant genişliği ve doğrusallık. Çıkış gücü, bant genişliği ve çalışma frekansı sistem tasarımcıları tarafından belirlenen parametrelerdir. Güç kuvvetlendirici tasarımında bu veriler temel alınarak mümkün olduğunca yüksek verime sahip kuvvetlendirici tasarlanması gerekir. Genelde doğrusallık ile verim arasında test orantı bulunur. Güç kuvvetlendiricilerinin veriminin arttırılabilmesi için doyma bölgesinde çalıştırılması gerekir. Bu da doğrusallığı bozmaktadır. Bu nedenle tasarımcı bu iki değişken arasında en uygun olanı seçmelidir.

RF güç kuvvetlendirici tasarımında ilk olarak hangi teknolojinin kullanılacağı belirlenmelidir. Örneğin GaAs yapılı transistörler düşük gerilimle çalışması gereken sistemler için uygunken, GaN yapılı transistörler çok daha yüksek güç gerektiren yüksek gerilimle çalışabilen sistemler için uygundur. Teknolojinin belirlenmesinin ardından sistemde kullanılacak modülasyonun yapısı da dikkate alınarak uygun bir kuvvetlendirici sınıfı seçilir. Kutuplamaya bağlı A ve AB türü kuvvetlendiriciler yüksek doğrusallığa sahipken verimleri düşüktür. Yine kutuplamaya bağlı B ve C sınıfı kuvvetlendiricilerin verimleri daha yüksek olmasına rağmen doğrusallıkları ve kazançları düşüktür. Bu tür kuvvetlenlendicilere ek olarak, çıkıştaki gerilim ve akım şekillendirmesine bağlı olarak E ve F sınıfı gibi kuvvetlendiciler mevcuttur. Bu kuvvetlenlendicilerde harmonikler uygun şekilde sonlandırılarak çıkış katındaki akım ve gerilim şekillendirilerek verim arttırılır. Ancak doğrusallık da azalır.

Küp uydular düşük maliyetleri ve hızlı tasarlanabilmeleri sebebiyle ünivetsitelerde sıklıkla bilimsel çalışmalar için tercih edilmektedir. Ancak bu uydular çok küçük olduğu için üretebildikleri güç de sınırlı olmaktadır. Sınırlı bu gücün en verimli şekilde kullanılabilmesi için verimi yüksek devreler tercih edilmektedir. Küp uydularda haberleşme için düşük bant genişliğine sahip basit modülasyon yapıları tercih edilir. Bu nedenle küp uydu vericilerindeki güç kuvvetlendiricilerinin yüksek verimli olması öncelikli tasarım hedefidir.

Bu tez çalışmasında, standart küp uydu gerilimi olan 5V ile çalışabilecek, yüksek verime sahip kuvvetlendirici tasarlanması hedeflenmiştir. Aktif eleman olarak GaAs pHEMT seçilmiştir. Birçok farklı firmanın paketlenmiş yapıdaki transistörleri incelenmiştir. Avago firmasının ATF-511P8 GaAS pHEMT'i 5V ile çalışmaya uygun, yüksek kazanç sağlayabilen ve kolaylıkla temin edilebilen bir eleman olduğu için tercih edilmiştir. Verimin yüksek olması için E ve Test-E sınıfı kuvvetlendirici yapısına karar verilmiştir. Tasarımın mümkün olduğunca yüksek verime ve kazanca sahip olması gerektiği için kuvvetlendirici AB sınıfı olarak kutuplanmıştır ve bu yapı ile E sınıfı ve Ters-E sınıfı tasarım yapılmıştır. Klasik E ve Test-E sınıfına ek olarak bu tez çalışmasında iki sınıf birleştirilerek daha keskin bant seçici karakteristiğe sahip bir kuvvetlendirici de tasarlanmıştır.

Küp uydu vericileri genelde 435 MHz bandında çalışmaktadır. Bu nedenle tasarımda ayrık elemanların kullanılması gereklidir. Birçok RF pasif devre elemanı bu bantta yüksek Q değerine sahiptir ve rahatlıkla kullanılabilmektedir. Ancak tasarım gereği harmoniklerin de dikkate alınması ihtiyacından dolayı yüksek güce dayanıklı RF pasif elemanların daha yüksek frekanslardaki davranışları giderek bozulmaktadır. Bu durum tasarım ve gerçekleme aşamalarında önemli bir zorluk olarak ortaya çıkmıştır.

Tasarımın ilk aşamasında transistörün doğrusal olmayan modeli temin edilmiştir. Bu model bilgisayar destekli tasarım aracına yüklenmiş ve modelin doğrulu incelenmiştir. Bunun için temel analiz devreleri hazırlanmış ve üreticinin sağladığı ölçüm değerleri ile karşılaştırılmıştır. Modelin doğru bir şekilde yüklendiğinin belirlenmesinin ardından DC IV eğrileri incelenmiş, uygun çalışma noktası belirlenmiştir. Yükle-Çek (Load-Pull) analizleri ile istenilen çıkış gücü ve kazancı sağlayacak empedans değerleri belirlenmiştir. Bu empedans değerlerinin belirlenmesi ile E sınıfı sonlandırma için gerekli çıkış kapasitesi hesaplanmış ve E sınıfı sonlandırma sağlayacak endüktans değeri ve ek kondansatör değeri belirlenmiştir. Bu aşamada düşük gerilimle çalışıldığı için ve GaAs transistörlerin dayanma gerilimleri de düşük olduğu için RF işaretin tepe değerinin yükseldiği seviyeler dikkatli bir şekilde incelenmiştir. Transistörün zarar görmeyeceği uygun bir sonlandırma belirlenmiştir. Bu durum transistörü güvenli bir aralıkta tutsa da gerilim ve akım şekillendirmesini etkilediği için verimin düşmesine sebep olmuştur. Ancak uzay ortamında en kötü koşulların dikkate alınması gerektiği için transistörün fazla zorlanmamasına karar verilmiştir.

Gerekli empedans değerleri belirlendikten sonra ilk olarak ideal pasif devre elemanları kullanılarak E sınıfı, Ters-E sınıfı ve birleştirilmiş yapı bilgisayar destekli ortamda incelenmiştir. Gerilim ve akım şekillerinden istenilen sonlandırmanın sağlandığı görüldükten sonra gerçek devre elemanları ile tasarıma geçilmiştir. Bu aşamada bazı üreticilerin sağladığı modellerin yetersiz oluşu bu elemanların benzetimlerde kullanımını oldukça zorlaştırmıştır. Ek olarak ayrık devre elamanlarının değerlerinin belli olması da önemli bir kısıt olarak karşıma çıkmıştır. İdeal devre elemanlarının yerine mümkün olan en uygun gerçek devre elemanları yerleştirildiğinde beklendiği gibi verimin %2-4 arasında düştüğü gözlenmiştir. Bu aşamada çıkış katında farklı sonlandırma topolojileri de ele alınmıştır.

Gerçek devre elemanlarının ardından bu devre elemanlarını birbirine bağlayacak mikroşerit hatlar yerleştirilmiştir. Bu mikroşerit hatlar da tasarımı doğrudan etkilemiştir. Bilgisayar ortamında çeşitli en iyileştirme yöntemleri kullanılarak mümkün olan en yüksek verim elde edilmeye çalışılmıştır. Tasarımın son haline gelmesinin ardından 3 tip kuvvetlendiricinin üretilebilmesi için serimleri

hazırlanmıştır. Düşük maliyeti ve uzay koşullarına da uyumlu olmasından dolayı 1mm kalınlığında standart FR4 taban tercih edilmiştir. Elektronik devre kartları üniversite bünyesindeki prototip makinasında hazırlanmıştır.

Elektronik devre kartlarının hazırlanmasının ardından devre elemanları montajlanmış ve elektronik testler yapılmıştır. İlk olarak devrelerin kararlılığı incelenmiştir. Devrelerin farklı kutuplama koşulları altında da kararlı olduğu belirlendikten sonra RF karakteristiğinin belirlenmesi için ölçümlere başlanmıştır. İlk yapılan ölçümlerde devrelerin merkez frekanslarının bir miktar kaydığı ve kazançlarının da beklenilenden düşük olduğu görülmüştür. Pasif devre elemanlarının yüksek frekanstaki tepkilerinin beklenilenden farklı olmasından dolayı bu farklılık ortaya çıkmıştır. Aynı değerde farklı üreticilerin devre elemanları ve yakın değerlerdeki devre elemanları kullanılarak çeşitli denemeler yapılmıştır.

Benzetim sonuçlarına göre elde edilen güç eklenmiş verim değerleri klasik E-Sınıfı yapı için %50, karma yapı için %43 ve Ters-E-Sınıfı yapı için %37'dir. Ölçümlerin sonucunda benzetimlerle karşılaştırıldığında kazanç ve çıkış gücü daha düşük, verim ise daha yüksek ölçülmüştür. Ölçümler sırasında devre üzerinde bazı ince ayarlamalar da yapılmıştır. Ek olarak karma yapılı E-Sınıfı devrede rezonans yapısında 49 nH ve 56 nH olarak iki farklı endüktans değeri ile iki ayrı devre hazırlanmıştır ve her biri ayrı ayrı ölçülmüştür. Ölçüm sonuçlarına göre elde edilen güç eklenmiş verim sonuçları E-Sınıfı için %35, Ters-E-Sınıfı için %40, 47nH ile karma tasarım için %57 ve 56 nH ile karma tasarım için %37 olarak ölçülmüştür. Bütün ölçüm sonuçları son bölümde ayrıntılı olarak verilmiştir.

Hazırlanan devreler küp uydulardaki ihtiyacı karşılayacak şekilde 435 MHz civarında 1 W çıkış gücü sağlamaktadır. Doğrudan 5V ile çalışabildikleri için ek bir DC-DC dönüştürücü olmadan kullanılabilir.

1. INTRODUCTION- POWER AMPLIFIERS

Power amplifier design includes different considerations such as accurate active device modeling, impedance matching based on the technical requirements and operation conditions, stability and simplicity in operation and practical implementation. The assessment of the quality of a power amplifier can be done by maximum power gain with stable operation condition and minimum amplifier stages. Furthermore, if needed, the requirement of linearity or high efficienct can be assessed. In order to have stable operation, it is required to consider the frequency domains that the active device might be potentionally unstable. For many wireless communication systems and applications, linearity is considered as a key parameter for a power amplifier. Moreover, there are specific considerations for the biasing of the power amplifiers which is different for efficiency improvement and it depends on the operating class of power amplifier and the type of the active device [1].

The aim of designing power amplifier is for maximum power gain and efficiency for a given output power with required stability. As seen in figure 1.1, basic single-stage power amplifier circuit includes an active device, input matching circuit to match with source impedance, and an output matching circuit to match with load impedance. In a power amplifier design, there are important parameters to be considered. All these parameters shall be considered in the design and reaching design goals will end up in a successful design.

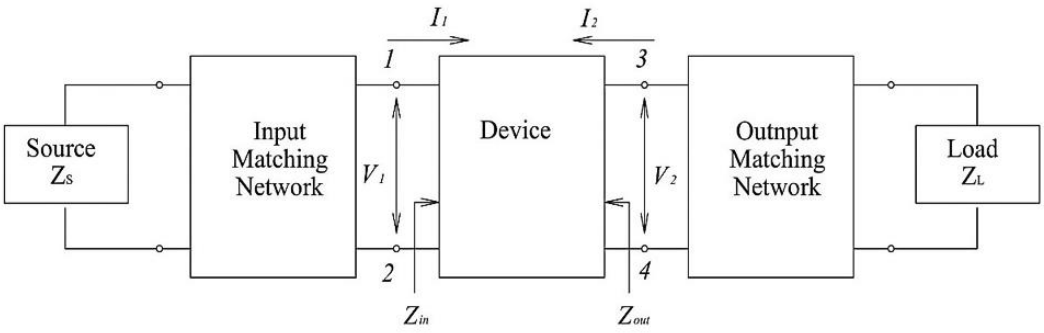


Figure 1. 1: Building blocks of a basic single stage power amplifier

Nowadays, with improvements in designing wireless communication systems with specific applications such as hand-held wireless devices, space telecommunication subsystems, etc. it is important to have highly reliable, efficient, small-sized systems, given the limit input power source (generally battery), attaining desirable output power level and gain.

1.1 Purpose of Thesis

The aim of this thesis is designing low-voltage Class-E and Inverse-Class-E power amplifier in UHF band using a GaAs pHEMT transistor. To reach this aim, Class-E and Inverse-Class-E structure has been selected in order to have maximum possible PAE with the given available input power, with high gain, and other design specifications which will be discussed and mentioned in details in following sections. Besides, Inverse-Class-E structure and novel mix of Class-E and Inverse-Class-E has also been designed and tested to compare the function of each structure. Suitable transistor (avaiable in market) and active device technology has been selected, different input and output matching networks have been designed and examined, biasing network has been designed carefully, and satisfying results for the given design goals has been achieved. Advanced Design System 2015.01 (ADS) is the software used for the design and circuits prepared and tested in RF Lab of Istanbul Technical University.

The challenges of this project was designing Class-E power amplifier, while having output matching circuit and maintaining design simplicity which resulted in very limited choices in using lumped elements. Furthermore, using transforming lumped passive elements into transmission lines is not feasible in UHF band as the lines will be very long and a make the implementations almost impossible. Therefore, transmission lines were used only between lumped passive elements to make connections. On the other hand, using lumped passive elements resulted in having a very lossy system, that for instance, a design with PAE=59% turned to PAE=44% after implementing real passive element models and transmission lines.

In this project, GaAs technology has been selected and ATF-511P8 is the active device, from Avago Technologies manufacturer. Three designes for Class-E, Inverse-Class-E and mixture of Class-E and Inverse-Class-E has been designed, fabricated and

tested. Results indicated the importance of keeping simplicity of design, while satisfying design goals. On the other hand, superiority of functionality for Class-E power amplifier has been proved by having higher PAE than the other two designs. Novelty of this project is using a mixture of Class-E and Inverse-Class-E power amplifier which has been designed and tested for the first time.

1.2 Literature Review

Class-E power amplifier which is one of highly efficient switching power amplifiers, can have theoretical efficiency of 100% and their application is common in MHz frequency domains. In case of designing class-E power amplifier in high frequencies, it shall be noted that the operation of power amplifier can be limited by the device parasitics (drain parasitics) such that transient operation is not possible, therefore, in order to have the second and third harmonic control, harmonic approximation can be applied, either by using transmission lines or benefiting from lumped element resonators [2].

For literature review, the presented references are limited to designed power amplifier in less than 1GHz in order to be comprehensive for this thesis and help to understand the function and implementation of Class-E power amplifier in low (MHz) frequencies, as the design considerations in high frequency would be vastly different.

The Switching mode tuned configuration Class-E designed and analyzed by Grebennikov et. al. with load network including a parallel capacitance, parallel inductance and series resonant circuit has been explained in [3] and design equations have been presented as well.

Kazimierczuk [4] Class-E design used BSX60 TO-39 transistor and achieved 3 W output power with collector efficiency of 95% at 1 MHz. Lie et. al. [5] obtained PAE=70% at 900MHz and PAE=60% at 2.4 GHz by designing Class-E power amplifier, IBM 7HP SiGe BiCMOS technology for wireless sensor applications. The fully differentioal CMOS Class-E amplifier designed by Mertens et. al. [6] at 700 MHz achieved PAE=62% with 1 W of output power. Lie et. al. [7] reached PAE of 68% at 900 MHz and 40% at 2.4 Ghz by analyzing the effect of operating freuqncy and transistor performance of monolithic efficient RF SiGe power amlifier using passive elements and bondwires. Achieving 73% drain efficiency with 10W output poewr at

900 MHz, Beltran et. al. [2] benefited from a technique by verifiying an experiment with a second harmonic Class-E and using lumped elements network. Ortega-Gonzalez et. al [8] could achieve PAE=79% and collector efficiency of 91% using a bipolar transistor at 900 MHz. Their design benefited from a multi-harmonic load-pull approach in frequency domain rather in time domain which proved the feasibility of using bipolar transistors in designing Class-E power amplifiers and satisfying the switching operation of transistor. Wilkinson et. al. [9] tranformed the load resistance down to a desirable level by using a simple class-E load network with suppressed harmonics in load and implementing transmission lines. Benefiting from a FET as switching active device, drain efficiency of 72% at 1 GHz was obtained. Another Class-E power amplifier design with PAE=80% and 0.55 W of output power at 0.5 GHz and PAE=73% with 0.94 W output power at 1 GHz was done by Mader et. al. [10] using Siemens CLY5 MESFET. One of the low-voltage designs were discussed in [11] by Sitch et. al. which designed Class-E PA with PAE=50% and 24 dBm output power at 835 MHz at a supply voltage of 2.5V, using a depletion mode 0.8-μm GaAs MESFET process. One of Class-E power amplifier design methods are implementing a multi-harmonic network for controlling the reactance of device at intrinsic drain. Beltran [12] implied this method for controlling harmonic up to ten harmonics which resulted in efficiency of 85%, 10W output power at 400 MHz using a GaN FET device. Brabetz et. al [13] using an OMMIC ED02A 6× 50 μm pHEMT as the active device implemented MIC which obtained maximum PAE=93%, 18dBm output power, 18 dB gain at 870 MHz. Operating across DCS1800, PCS1900, CDMA2000 and WCDMA frequency bands, Grebennikov et. al. [14] designed high efficiency two stage and three stage InGaP/GaAs HBT power amplifiers in multi-band and multi-mode structure. Results indicated PAE=50% and more, in frequency range of 1.7-2.0 GHz. The novelty of this design was paralled-circuit load netowork, with microstrip L-type matching network.

1.3 Hypothesis

Theoretically Class-E power amplifier can reach 100% of efficiency but in fact, it is impossible due to available non-idealities such as parasitic capacitance of the active device, transistor packaging, intrinsic resistance and capacitance, non-ideal harmonic suppression for second, third or higher harmonics, real model elements' tolerance,

transmission line impedance, substrate material, etc. Thus for this project, the power added efficiency of 35%-95% can be expected. It can be indicated that functionality of class-E power amplifier is better than Class-B power amplifier, reaching to semi-ideal functions. Based on calculations, available hardwares and active device packaging, PAE of higher than 35% is expected.

1.4 Power Amplifier Design Fundamentals and Figure of Merit

The objective of designing power amplifier is to reach high efficiency and maximum gain for a required output power considering all design parameters such as stability.

Considering the power amplifier as a black box as shown in figure (1.1), and based on circuit theory, having the dc supply voltage as V_{CC}, the quiescent current as I_q, the drain (or collector in case of using bipolar transistor) efficiency can be written as:

$$\eta = \frac{P}{P_{DC}} = \frac{1}{2}\frac{V}{V_{CC}} = \frac{1}{2}\frac{I}{I_q}\xi \tag{1.1}$$

Where DC output power can be defined as:

$$P_{DC} = I_q . V_{CC} \tag{1.2}$$

At fundamental frequency f_0, Delivered power to the load resistance R_L is:

$$P = \frac{VI}{2} \tag{1.3}$$

And drain (collector) voltage peak factor is:

$$\xi = \frac{V}{V_{CC}} \tag{1.4}$$

For a power amplifier the overal efficiency is defined as:

$$\eta_{ALL} = \frac{P_{OUT}}{P_{DC} + P_{IN}} \tag{1.5}$$

$$\text{PAE} = \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{1.6}$$

Where;

P_{OUT} is the delivered power to the load at the frequency of operation,

P_{DC} is the power taken from DC source,

P_{IN} is the input power,

and the dissipated power in the load at harmonics can be noted as loss.

Generally power amplifiers are mostly characterised by Power Added Efficiency (PAE). In case the power amplifier is considered as a black box (figure 1.2) overal efficiency can be used. Efficiency, overal efficiency and PAE are considered as three figures of merit for power amplifier design and characterization.

In order to have an unconditionally stable linear (small signal) amplifier, the power that enters the amplifier (P_{IN}) shall be equal to the available power (P_{Av}) from generator and that happens when the amplifier is conjugatedly matched to the source impedance.

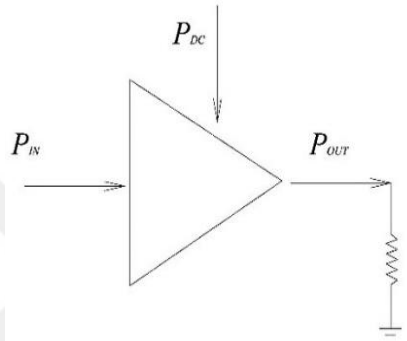


Figure 1. 2: Power amplifier shown as a black box.

In case the input power is smaller than the available power, then for PAE and η_{ALL}, refer to available power (P_{Av}) which is larger. In some cases, the input is deliberately mismatched to obtain flat gain over wider range of frequency or for the sake of better linearity. Generally throughout this thesis, P_{Av} would be considered conventionally and it is considered that power amplifier is in matched condition either with isolators or balanced configuration [15].

There are three categories for power amplifiers mode of operation: Linear mode, when the operation is attained to linear part of characteristics curve of the active device; Critical mode, when opertion continues beyond linear part up to saturation and cut-off regions while the anode current stops to flow; and nonlinear mode, when in each cycle, the anode current stops to flow during a specific part of cycle which depends on the grid biasing [1]. High efficiency amplifiers are generally considered in the third class. By using a parallel resonant circuit at the load network, harmonics of fundamental frequency can be suppressed, thus, sinusoidal signal can be tranfered from source to load. This parallel resonant structure acts as a short-cut for harmonics in a low-impedance way and its resonance recieves energy at that fundamental frequency. In

other words, in order to suppress potential harmonic components, the resonant frequency shall be equal to the operating frequency of the power amplifier. At the device, the frequency spectrum will contain second, third or higher orders of harmonics for the fundamendal frequency. But as the parallel resonant LC circuit has high quality factors, it helps only the fundamental frequency signal to pass to the load and makes the higher order harmonic components short circuit. In order to discuss the above mentioned detilas in an analytical way, equations can be written as:

$$i(\omega t) = \begin{cases} I_q + I\cos\omega t & -\Theta \le \omega t < \Theta \\ 0 & \Theta \le \omega t < 2\pi - \Theta \end{cases} \quad (1.7)$$

Conduction angle is 2Θ and can be defined as the angle of a current showing the part of the RF current cycle that the conduction happens for the device and indicates when the output current $i(\omega t)$ can have zero value. Thus,

$$i(\Theta) = I_q + I\cos\Theta = 0 \quad (1.8)$$

By calculating half of the conduction angle Θ

$$\text{Cos} = -\frac{I_q}{I} \quad (1.9)$$

This results in a fundamental explanation for non-linear operation of a power amplifier in half of the conduction angle Θ as,

- Class AB: $\Theta > 90^0$, causes $\cos\Theta < 0$ and $I_q > 0$
- Class B: $\Theta = 90^0$, causes $\cos\Theta = 0$ and $I_q = 0$
- Class C: $\Theta < 90^0$, then $\cos\Theta > 0$ and $I_q < 0$.

By writing the Fourier series expanstion of a periodic pulsed output current i(ωt),

$$i(\omega t) = I_0 + I_1 \cos\omega t + I_2 \cos 2\omega t + I_3 \cos 3\omega t + \cdots \quad (1.10)$$

In order to obtain the DC and fundamental frequency component:

$$I_0 = \frac{1}{2\pi}\int_{-\theta}^{\theta} I\,(\cos\omega t - \cos\theta)\,d\omega t \quad (1.11)$$

$$I_1 = \frac{1}{\pi}\int_{-\theta}^{\theta} I\,(\cos\omega t - \cos\theta)\,\cos\omega t\;d\omega t \quad (1.12)$$

Figure (1.3) shows the relationship between conduction angle, differenet classes of power amplifier and the efficiency percentage. As it can be seen, Class A has the greatest conduction angle, the signal has complete waveform in its cycle and this class has lowest efficiency, in ideal case, 50%. By reducing the conduction angle and moving from class B towards switching Classes, the linear amplifiers turn to non-linear mode of operation and this way the efficiency increases theoretically and ideally up to 100% in Class-E and -F.

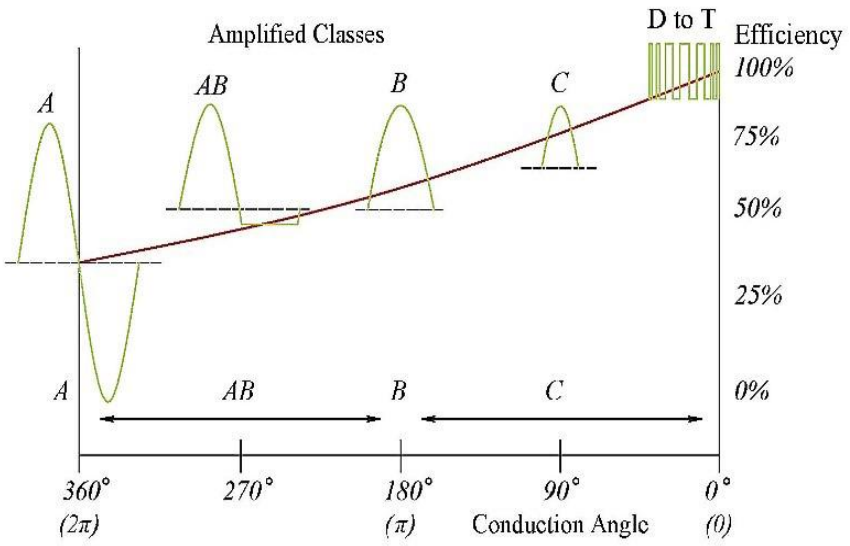


Figure 1. 3: Amplifier classes comparison in terms of conduction angle and efficiency

2. DESIGN AND IMPLEMENTATION

2.1 High Efficiency Power Amplifier

Efficiency in amplifiers mean in comparison to the RF energy which will be delivered to the load, the energy loss during the amplifying process is rather small. The reasons stated below will emphasize on the importance and necessity of RF and microwave amplification:

- DC supply in some specific applications is either limited or very hard to be recharged. For instance, in space systems, army applications, hazardous areas, changing or recharging the supply is almost impossible or not practical.
- DC supply in specific applications such as high power base station networks due to having large quantities of transmit or receive cells is highly expensive.
- Heat generation or transfer during non-efficient amplification can destructively affect the function or result in damaging the active device which means the amplifier shall be removed. Therefore, heat sinks are widely used which make the amplifier cool during amplification. But in specific applications such as small-sized hand-held devices and systems, cooling methods are not practical nor feasible.

To sum up, in order to increase the efficiency of a power amplifier, system shall have optimized power consumption function.

2.2 Concept and Mode of Class-E Operation

One of the examples of non-linear mode of operation is Class-E power amplifier where the active device works as a “switch” , that the characteristics of the active device can be modeled by a simple switch. This means the transistor is no more modeled as an ideal current source.

Figure (2.1) presents a simple structure for an ideal Class-E amplifier which includes an active device working as switch that can be turned on or off within each RF cycle and has negligible transition times.

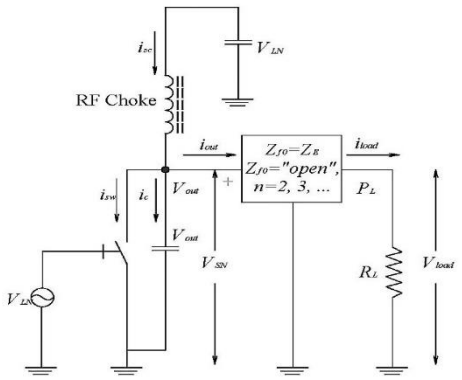
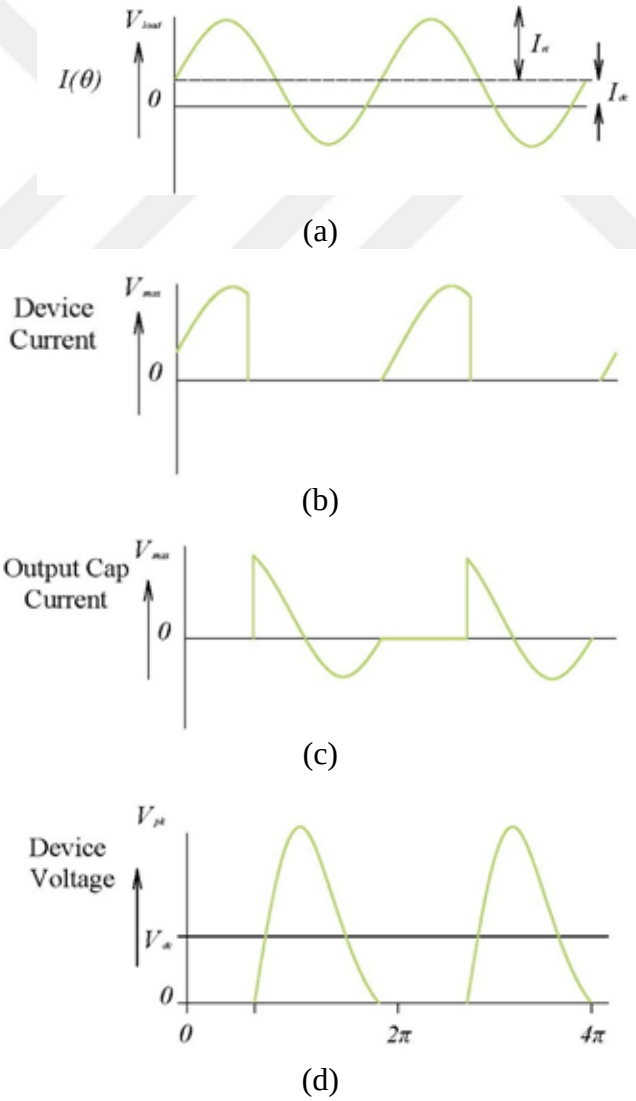


Figure 2. 1: Generic Class-E power amplifier.

This switch can be shunted by a capacitor and that is shunted by a series resonant circuit. Considering the switch is triggered at a frequency close to resonsance of the circuit, a sinusoidal current flow (figure 2.2) can be observed around the circuit loop.



(a)

(b)

(c)

(d)

Figure 2. 2: Ideal Class-E waveforms.

When the switch is “closed”, the resonant current is forced into the switch and when the switch is “opened” the resonant current is forced into the shunt capacitor. That’s why the presence of this shunt capacitor is vital for the function of Class-E power amplifier in order to complete the current loop in the circuit. This function can be clearly seen in figure (2.2) for the resultant waveforms of the device current and voltage, and the output capacitor current. Class-E operation means during the RF cycle there is no time that current and voltage of transistor’s drain exist at the same time, thus ideally there is no power dissipation, and therefore the efficiancy of DC to RF conversion can be 100%. Due to resonant feature of the circuit and containing the RF load, all energy would be restricted to the fundamental frequency.

As the voltage peak across the switch can get way larger than the DC supply voltage, this cautious situation may result in breakdown problems. Practically, the trick of this class is designing the circuit in a way that transistor acts as a switch and that includes using the threshold characteristics of the active device and the knee region. This way, there would a trafe-off between having higher efficiency and decreasing the device peak current feature and that results to less power than class-AB operation for same device with similare supply voltage. In low frequencies, the functionality of Class-E amplifiers are superior in comparison with Class-B, -C or –F. Furthermore, the efficiency can be attained in large range of output power.

By linearly changint the supply voltage, amplitude modulation can be obtained which this feature does not happen for Class-C or –F. One of the best ways to linearize Class-E PA is to cancel and restore the ampliture which leads to a signal with constant envelope and this signal is amplified in the saturation high efficiency power amplifier and at the final stages, when the envelope of the signal is going to be restored, the amplitude variations will be added to theenvelope of the signal [12].

Practically functionality of Class-E is better than Class-B because less power is dissipated in the active device which leads to higher efficiency, less junction temperature, smalled heat sink size and more reliable power amplifier. One negative point about Class-E is its sensitivity towards load variations in comparison with Class-B circuit. Though Class-E is considered as a low-impedance RF voltage source, the output current can be negatively affected by load resistance. Finally, in worst case, the transistor dissipation in Class-E is better than the best case of dissipation in class-B which is at least four times higher than dissipation in class-E [35].

Very high efficienct Class-E circuit with efficiencies around 90% has been designed in [3, 8, 13] for low frequencies but the active devices are working in highly non-linear mode [17]. An efficient design of output matching network for Class-E power amplifier, satisfies three main points:

- Minimizes switching loss by shaping voltage and current waveforms,
- In order to decrease the counterpart input capacitances due to Miller effect and speeding up the switching pace, output matching network permits the transistor's zero voltage tern on condition.
- It cancels harmonic loss in load by filtering the harmonic of output current.

Typical Class-E circuit is shown in figure 2.1 and figure 2.2(a) presents the current and voltage waveforms for an ideal switch. It can be observed that those waveforms in figure 2.2 can be obtained by following speculations:

- With a sinusoidal output current consideration, the output impedance is terminated to be open at all higher harmonics, thus it cancels the power loss due to harmonics;
- For having constant drain supply current, an idal RF chocke can be used;
- Optimally for a maximum output power, the duty cycle is considered as 50% and the active device functions as an ideal switch at ω_S;
- The switch can be terminated by a special imepdance at the fundamental frequency as:

$$Z_E = \frac{0.28}{C_{OUT} + \omega_S} e^{j49^\circ} = R_E + jX_E \quad (2.1)$$

Where ω_S is angular switching frequency and C_{OUT} as total shunt capacitance which can be considered as a main parameter for designing Class-E. This shunt capacitance is part of the output matching netowrk for lower friquencies (less than 1GHz) and can be calculated. As shown in figure 2.2 switching action causes the displacement of switching voltage and current, thus cancelling the dissipation loss.

One of unique features of Class-E can be seen in figure 2.2(b) for switching voltage that when the voltage value of C_{OUT} is zero, the switch is closed, in other words, the capacitos is shorted and that cancels the prompt discharge across the switch and avoids the switching loss. Furthermore, C_{OUT} current has zero crossing which leads to insensitivity of Class-E efficiency to output impedance variations. By applying initial conditions of voltage and current for transistor, time domain equations can be written:

$$v_{s\omega}(t)|_{t=\frac{T_S}{2}} = 0 \qquad \frac{dv_{s\omega}(t)}{dt}|_{t=\frac{T_S}{2}} = 0 \tag{2.2}$$

The ratio between fundamental components handles the optimum Class-E output impedance as obtained in equation (2.1) by applying Fourier expansions to the above waveforms. The only information transacted between input and output of a Class-E power amplifier is the input RF signal which controls the switching condition. By having this feature, Class-E power amplifiers are properly working to amplify constant envelope signals such as FM. Other methods such as EER or Chirex can be used to expand this application to variable envelope signals.

The switching function of Class-E power amplifier puts substantial stress on voltage nad current. In comparison to linear mode of operation, the peak voltage and current in this class is much higher and that indicated the maximum output power at the output of such a class. The switch voltage during the off half cycle for an active device (modeled as an ideal switch) can be determined as:

$$v_{s\omega}(t) = \frac{I_{DC}}{C_{OUT}\,.\,\omega_S}\,(\omega_S t - \text{a}\,.\,(\cos(\omega_S t + \emptyset) - \cos\emptyset)) = v_T(t) \tag{2.3}$$

During the "ON" half–period, the switch current is:

$$i_{s\omega}(t) = I_{DC}(1 - \text{a}\,.\,\sin(\omega_S t + \emptyset)) \tag{2.4}$$

where a = 1.862 and Ø = -32.48^0. Due to open harmonic termination towards output current path, the output current flowing into output network $i_{OUT}(t)$ is sinusoidal:

$$i_{OUT}(t) = a\,.\,I_{DC}\sin(\omega_S t + \emptyset) \tag{2.5}$$

while the current flowing into the switch/capacitor is:

$$i_T(t) = I_{DC} - i_{OUT}(t) = I_{DC}(1 - \text{a}\,.\,\sin(\omega_S t + \emptyset)) \tag{2.6}$$

Thus, the transistor current and peak switch voltage are:

$$v_{T-MAX} = 1.134\,.\frac{I_{DC}}{C_{OUT}\,.\,\omega_S} \tag{2.7}$$

$$I_{T-MAX} = (1 + a)I_{DC} \tag{2.8}$$

Helping from equation (2.5) the average power delivered to the matching network is:

$$P_{OUT} = \frac{1}{2}R_E(a.I_{DC})^2 \tag{2.9}$$

Where in equation (2.2), R_E is the real part of the fundamental output impedance Z_E.

From the above equation, it can be concluded that higher DC current I_{DC} results in higher output power P_L which leads to higher peak values for output voltage and current (equations 2.7 and 2.8).

Ideally, the delivered power ro the load equasl to delivered power to the network if the output matching network is lossless (P_{OUT}= P_L). In order to identify the attainable maximum output power from an active device with maximum current range of I_{MAX} voltage V_{MAX}, it is useful to recognize if the current or voltage of the transistor has a critical limit. By supposing the current limit as $I_{T-MAX} = I_{MAX}$, benefiting from equation 2.7 and 2.8, equivalent maximum voltage of transistor can be obtained by:

$$V_{T-MAX} = 1.134 \,.\, \frac{I_{DC}}{C_{OUT} \,.\, \omega_S} = \frac{1.134}{1+a} \,.\, \frac{I_{T-MAX}}{C_{OUT} \,.\, \omega_S} = 0.4 \,.\, \frac{I_{MAX}}{C_{OUT} \,.\, \omega_S} \qquad (2.10)$$

Then if:

(1) $V_{T-MAX} = V_{MAX}$. In other words, the current peak value is critical. Thus, using equation (2.8) the average transistor current I_{DC} can be obtained by replacing $I_{T-MAX} = I_{MAX}$. Output power can be reached benefiting from equation (2.9).

(2) $V_{T-MAX} > V_{MAX}$. In other words, the current peak value is not critical, and thus the voltage limit of transistor is more critical, so $V_{T-MAX} = V_{MAX}$ and the average transistor DC current can be obtained by equation (2.7) and output power can be obtained by equation (2.9).

Lastly, by speculating ideal efficiency and no loss condition (P_{DC}= P_{OUT}), the desirable DC voltage supply can be obtained as:

$$P_{OUT} = \frac{(I_{T-MAX} \,.\, V_{T-MAX})}{2} \qquad (2.11)$$

The above discussion clarifies that maximum current has more critical effect on limitations, voltage peak is rather less than the maximum voltage rating [15].

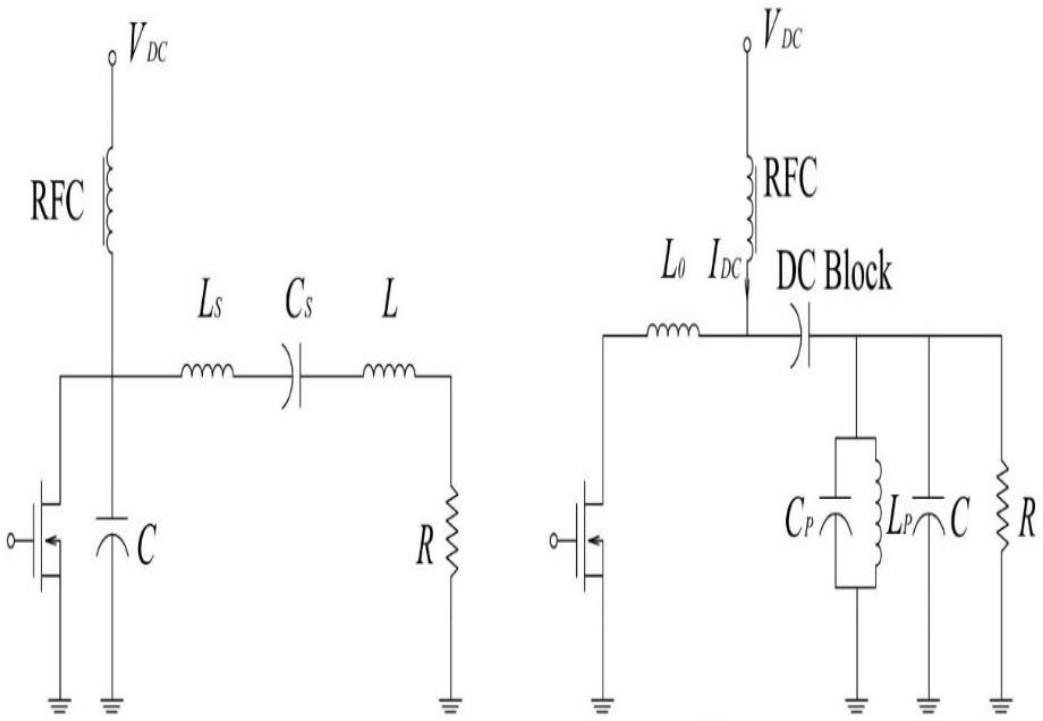
As stated in table 2.1, for 435-MHz class–E PA using an active device with the following parameters will be dimensioned:

Table. 2.1: 435MHz Class-E power amplifier parameters

Z_E	I_{T-MAX} (mA)	V_{T-MAX} (V)	P_{out} (W)	V_{DC}(V)	I_{DC} (mA)
3.59+j4.13	141	4.71	1.3694	5	100

2.3 Concept of Inverse-Class-E Operation

Classical class-E power amplifier, applying zero-voltage switching condition was first introduced by Sokal [16] and can be seen in figure 2.3(a). Inverse-Class-E applies zero current switching [17] condition to attain optimum operation. In this class, the current and voltage switching waveforms are duals of Class-E waveforms. Class-E amplifiers were considered as shunt-C/series tuned or current driven, while inverse-class-E amplifiers were known as series-L/parallel-tuned or voltage driven. The feature of Inverse-Class-E against Class-E is its 20% lower peak switching voltage. Furthermore, Inverse-Class-E has higher self-resonance frequency because it runs with lower inductance values which means reduced series resistance of inductor and leads to more chance of benefiting from lumped elements in monolithics IC designs.



(a) (b)

Figure 2. 3: Basic switching structures. (a) Class-E. (b) Inverse-Class-E[18].

Furthermore, this class permits better optimization at high output powers for high efficiency and higher peak output power. It is fairly insensitive towards value variations of design components, switching frequency and duty cycle changes.

So far, few researchers has worked on this class of PA, so for this project, lack of resources and available projects was one of the challenges.

Basic topology of Inverse-Class-E power amplifier can be seen in figure 2.3(b) which includes a transistor as an active device, series inductor L, and parallel-tuned load network (L_P-C_P-R). Fundamental frequency phase shift can be compensated by an additional capacitor C. The DC current, after passing through the RF choke, turns into fundamental frequency and higher harmonic components by the the switching performance of the transistor. The function of parallel-tuned L_P-C_P with high quality factor is to cancel out the harmonic componens of the current and lets the fundamental frequency component of current tko pass through. DC blocking capacitor stops the DC current to reach the output and short-circuit the inductor L_P to the ground. In higher frequencies, the shunt capacitance C would be substituted by two open circuit shunt stubs to facilitate the higher harmonic eliminations and distribute the function of parallel-tuned L_P-C_P network. Considering the open circuit short stubs to be lossless, with characteristic admittance (Y_0), the capacitive behavior can be modeled as [17],

$$Y=j\omega C = j\, Y_0 tan\theta \tag{2.12}$$

$$Y_0 = \frac{\omega C}{tan\,\theta_1 + tan\,\theta_2} \tag{2.13}$$

In an Inverse-Class-E power amplifier, assuming 50% duty cycle, DC supply voltage V_{DC}, desirable output power P_{OUT}, fundamental frequency f_0, and loaded quality factor Q, the design equations have been presented in [33] for optimal lumped element values. Switching voltage, current and voltage across the series inductor can be considered as $v_{s\omega}(\Theta)$, $i_{s\omega}(\Theta)$, $v_L(\Theta)$ and where $\Theta=\omega t$ and theoretically the peak switching voltage can be calculated as $v_{s\omega,peak} = 2.826\, V_{DC}$.

$$L=\frac{{V_{DC}}^2}{\pi\omega\, P_0} \tag{2.14}$$

$$C=\frac{\pi\,(\pi^2-4)}{2(\pi^2+4)}\frac{P_0}{\omega {V_{DC}}^2} \tag{2.15}$$

$$R=\frac{\pi^2+4}{8}\frac{{V_{DC}}^2}{P_0} \tag{2.16}$$

$$L_P = \frac{R}{\omega\, Q} \tag{2.17}$$

$$C_P = \frac{1}{\omega^2\, L_P} \tag{2.18}$$

$$v_{SW}(\theta) = \begin{cases} V_{DC}[1-\mathrm{a}\sin(\theta+\emptyset)] & \pi < \theta < 2\pi \\ 0 & 0 < \theta < \pi \end{cases} \tag{2.19}$$

$$v_L(\theta) = \begin{cases} V_{DC}[1 - \mathrm{a}\sin(\theta + \emptyset)] & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \quad (2.20)$$

$$v_L(\theta) = \begin{cases} \frac{V_{DC}}{\omega L}[\theta + \mathrm{a}\ \cos(\theta + \emptyset) - a\ cos\emptyset] & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \quad (2.21)$$

Where

$$a = \sqrt{\frac{\pi^2}{4} + 1} \quad (2.22)$$

$$\emptyset = tan^{-1}\left(\frac{-2}{\pi}\right) \quad (2.23)$$

Additional impedance transformation in output matching network might be needed to match the impedance to 50 Ω at input and it can be obtained by using L-type matching network.

2.4 Class-E Power Amplifier Design Challenges

In low frequencies (less than 500 MHz), it is advised to use lumped elements with high quality factor in the output matching network. These elements include shunt capacitance right after the active device output terminal (drain for FETs), as well as series resonant circuit. By detuning the resonant circuit, the fundamental frequency can be terminated. In order to filter out the harmonic components, a high impedance patch toward the output current shall be designed so that it can be considered as "open circuit" and cancel the harmonics. By knowing the design requirements such as desirable output power, features of active device and quality factor of available components, the elements of matching networks can be calculated. In order to convert the load resistance into the required load for Class-E, complementary impedance transformationg might be needed.

The design of ideal Class-E might seems simple and easy, though designing microwave power amplifiers in this class has plenty of challenges and tricks. In fact, design equations may not be practical and results may seem dissatisfactory which decreases power, gain, efficiency, frequency of operation and other design parameters. In order to make an accurate design, non-idealities shall be identified, limitations shall be considered and analyze solutions and options can be proposed.

Practically, unlike other power amplifiers, in a switching power apmlifier such as Class-E, the transistor (switch) is a time variant component which gives output voltage

and current in form of transient response by having a specifically designed output matching network and a constance DC supply. In other words, normal power amplifier rules such as load-line theory do not apply to switching mode power amplifiers.

As the output voltage and current waveform of a switching device are discontinuous, they have harmonic components. It means the efficiency can be negatively limited by the dissipated power as a result of harmonic components in the resistive load.

This way, the functionality of a Class-E might be worse than Class-B or -AB. On the other hand, the reactive components such as inductors and capacitors also have discontinuous operation, which puts high voltage and current stress on the switching deivce and that limits the maximal output power, even less than linear classes of power amplifier such as Class-A, -B or -AB.

One trick of switching mode power amplifier design is selecting proper biasing point which is triod region for FETs or a region between cut-off and saturation for bipolars. This way, the capacitance between switch terminals of the active device promptly discharges through the switch at the beginning of On-time and causes switching loss and lessens the efficiency that can be obtained in such power amplifiers [15].

2.5 Active Device Selection

The function of transistor in both Class-E and Inverse-Class-E is considered as a switch, therefore, the transitor technology selection is a critical parameters and shall provide low-loss switching capability specifically in UHF band for this project. FETs are highly prefered over bipolars due to having better switching ability and on-resistance of FETs can be decreased by increasing device size. Also, FETs can provide bidirectional switching which means there is no need to have input current [11].

Typical process of GaAs includes two gold metal layers with crossover isolation (air-bridged). This gold interconnected metals leads to five up to ten time higher current carriage in comparison with aluminum interconnects for a strip width because of thickness and higher conductivity features of gold. GaAs technologies including MESFET, HBT, HEMT, have insulating substrate, which results in less loss. GaAs technologies are more expensive in comparison with Silicon but they are becoming more useful and mature by time. GaAs High Electron Mobility Transistors (HEMTs) show better performance in comparison with MESFET and HBT but more complex

and more expensive. The features are lower noise figure, higher f_{MAX}, and ideal low voltage high efficiency performance for power amplifier applications [19]. For the above mentioned reasons, GaAs HEMT technology is prefered for the technology of active device.

2.5.1 Transistor selection

After searching for proper transistors based on the design goals, availability, desirable parameters and other parameters, the options below were selected among searching over 80 transistors and finally ATF-511P8 from Avago technologies has been selected.

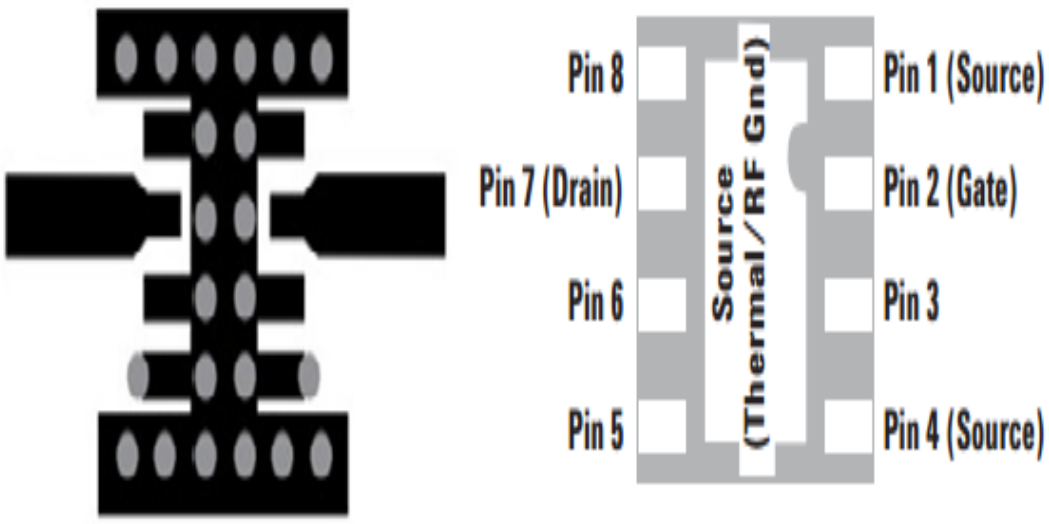
Table 2.2: Transistor Selection

Producer	Part No.	Transistor technology	Packa-ging	P1dB (dBm)	Freq. (GHz)	Specs.	Rated volta-ge	gain@ Freque ncy (dB)
Avago	ATF-511P8 [20]	pHEMT	LPCC	30	12	NL, NP, IM	7	14.8@ 2GHz
NEC	NE55 20379 A [21]	LDMOS	79A	32.3	2	NL, NP	15	16@ 915M Hz
Avago	ATF-501P8 [22]	HEMT	LPCC	29	12	NL, NP, IM	7	15@2 GHz
Avago	ATF-50189 [23]	HEMT	LPCC	30	6		7	15.5@ 2GHz

Features of this enhancement mode pHEMT transistor include high linearity, low noise, 100% RF and DC tested, operating frequency range from 50 MHz to 6 GHz which makes it a good choice for this design in UHF band and suitable for medium power applications. The mounting temperature is $+85^0$ C. Applications include based station transmit driver or first or second stage LNA in a receiver.

Operating like a normal FET, designs using ATF-511P8 needs DC basing, input and output matching networks but in contrast with depletion mode transistors, this device can act only with one positive power supply, which means turning on this transistor required giving a positive voltage on drain and gate.

Figure 2.4 represent the PCB layout for the Leadless Plastic Chip Carrier (LPCC) packages used by this transistor. As it can be seen, this package includes several number of plated through hole vias which enable this transistor for thermal and RF grounding.



(a) (b)

Figure 2. 4: (a) PCB package layout and (b) bottom view package marking[20].

Furthermore, desirable transition from microstrip to the device package has been achieved. The leadless package of this transistor has been die mounted directly to the lead frame or the belly of the package which shows its superiority against SOT packages. Thus, RF grounding has been eased by inductance reduction from source to ground [19]. Table 2.3 and 2.4 will present the ratings and device parameters.

Table 2.3: ATF-511P8 absolute maximum ratings [20].

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain-Source Voltage	V	7
V_{GS}	Gate-Source Voltage	V	-5 to 1
V_{GD}	Grate Drain Voltage	V	-5 to 1
I_{DS}	Drain Current	A	1
I_{GS}	Gate Current	mA	46
P_{diss}	Total Power Dissipation	W	3
$P_{in,max}$	RF Input Power	dBm	+30
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
Θ_{ch_b}	Thermal Resistance	°C/W	33

Table 2.4: Device parameter specifications [20].

Symbol	Parameter and Test Condition		Unit	Min.	Typ.	Max
V_{gs}	Operational Gate Voltage	$V_{ds} = 4.5V$ $I_{ds} = 200mA$	V	0.25	0.51	0.8 -
V_{th}	Threshold Voltage	$V_{ds} = 4.5V$ $I_{ds} = 32mA$	V	-	0.28	-
I_{dss}	Saturated Drain Current	$V_{ds} = 4.5V$ $V_{gs} = 0v$	μA	-	16.4	-
G_m	Transconductance	$V_{ds} = 4.5V$ $G_m = \frac{\Delta I_{dss}}{\Delta V_{gs}}$ $\Delta V_{gs} = V_{gs1}$-V_{gs2} $V_{gs1} = 0.55V$ $V_{gs2} = 0.5V$	mm ho	-	2178	-
I_{gss}	Gate Leakage Current	$V_{ds} = 0V$ $V_{gs} = -4.5V$	μA	-27	-2	-
NF	Noise Figure	F=2GHz F=900MHz	dB dB	- -	1.4 1.2	- -
G	Gain	F=2GHz F=900MHz	dB dB	13.5 -	14.8 17.8	16.5 -
OIP3	Output 3rd Order Intercept Point	F=2GHz F=900MHz	dB dB	38.5 -	41.7 43	- -
P1dB	Output 1dB Compressed	F=2GHz F=900MHz	dB dB	28.5 -	30 29.6	- -
PAE	Power Added Efficiency	F=2GHz F=900MHz	% %	52 -	68.9 68.9	- -
ACLR	Adjacent Channel Leakage Power Ratio	Offset BW=5MHz Offset BW=10MHz	dBc dBc	- -	-58.9 -62.7	- -

Pins 1 and 4 better to be grounded as they are connected to the source, while pins 3, 5, 6 and 8 are not connected, though can be used for heat dissipation from package or easier alignment of the device while soldering.

Figures 2.5 and 2.6 are the device and internal structure of ATF-511P8 in ADS.

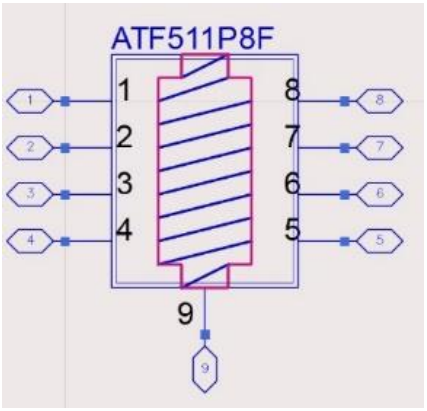


Figure 2. 5: ATF-511P8 device model in ADS.

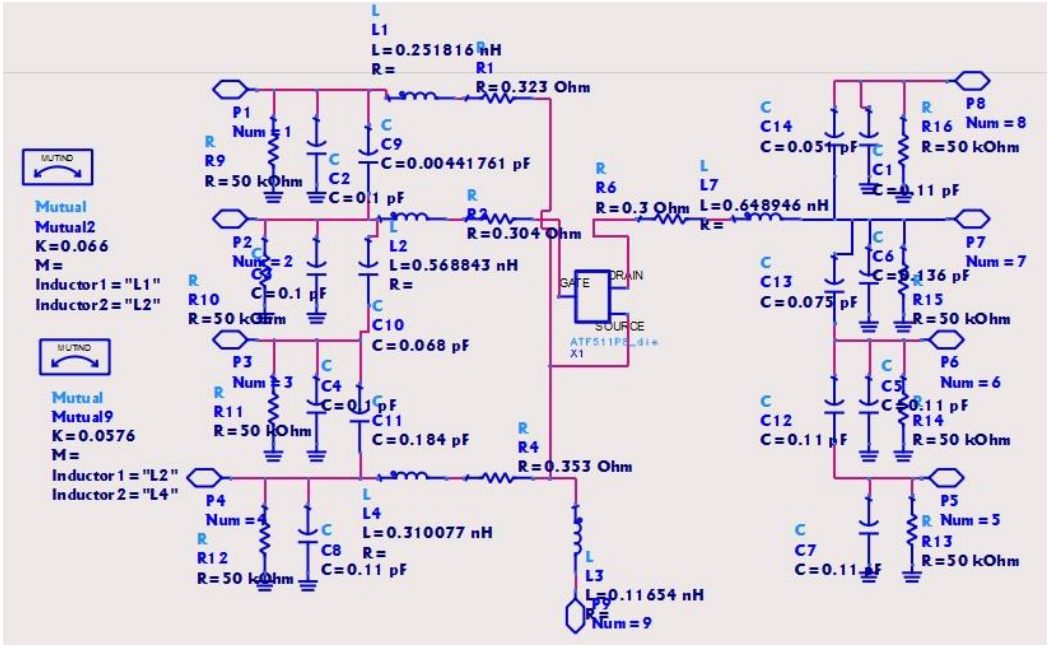


Figure 2. 6: Internal structure of ATF-511P8 device in ADS.

2.6 Design Stages

Each design needs goals that shall be met at the end of the design to be considered as a successful design. The goals of this project are listed in table 2.5 below:

Table 2.5: Design goals.

Freq. (MHz)	Output Return Loss (dB)	Input Return Loss (dB)	Gain (dB)	Output power (dBm)	Supply voltage (v)	PAE (%)	Harmonic Suppression (dBc)	Stability
430-440	<-20	<-10	>15	>33	5	>50	>30 (@1MHz)	1MHz <f<1 GHz

This narrow bandwidth has been the requirement of the design, based on the functions of the previous and next stage systems. -20dB output return loss is for the best situations. This project will be used as the power amplifier in a small satellite which means all power needs to be efficiently handled. Efficiency is the key factor for this design. Another feature of this design is using low-voltage. 5 Volt is a stardard value for small satellites and by this design, there would be no need to use an extra stage for DC-DC down-converter.

In order to meet the goals, there are steps to be taken such as finding out the DC characteristics, Load-pull and Source-pull analysis, biasing, input and output matching network design, and the results will show the level of success.

2.6.1 Transistor DC bias characteristics

One of the most important factor in a Class-E power amplifier design is biasing which indicates finding a corret voltage for gate and drain of transistor to force it to operate as a switch. This point can be selected using the polarization curve graphic (I_{DS} versus V_{DS} for different V_{GS}). In order to satisfy Class-E or Inverse-Class-E operation condition, a specific value for V_{GS} in pinch-off region shall be selected for a given V_{DS} value which has been defined by design parameters (in this case $V_{DS} = 5v$). As mentioned before, switching mode operation does not follow the classical load-line rules and theories. This V_{GS} selection shall satisfy drain voltage nad current specifications of transistor in a way that:

- V_{GS} shall give drain current to saturation mode;
- V_{DS} shall have a value that is acceptable by the transistor [24].

Figures 2.7 and 2.8 presents the circuit used to obtain the I-V curve of this transistor; the circuit and polarization curves from all the operating ranges of transistor from 0v to 7v for drain voltage can be observed. V_{GS} range goes from 0v to 0.8v.

For this design, four different I_{DS} current values have been selected and obtained the V_{GS} values, and in next level, the impedance of maximum PAE for each biasing point will be observed by doing load-pull and source-pull analysis to find out in which biasing point, highest PAE and gain can be expected. The corresponding values of four selected biasing points can be seen in the Table 2.6.

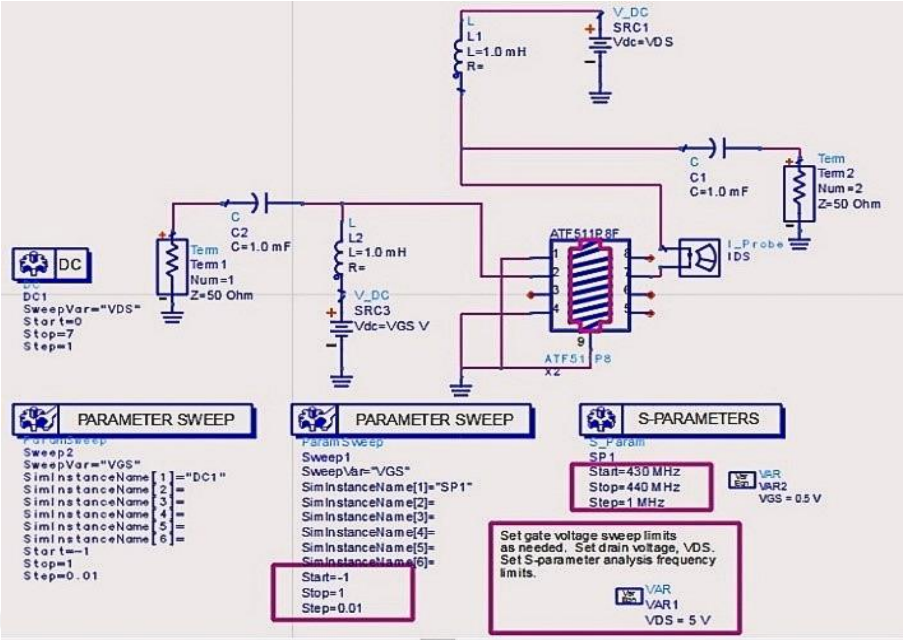


Figure 2. 7: FET bias circuit of ATF-511P8.

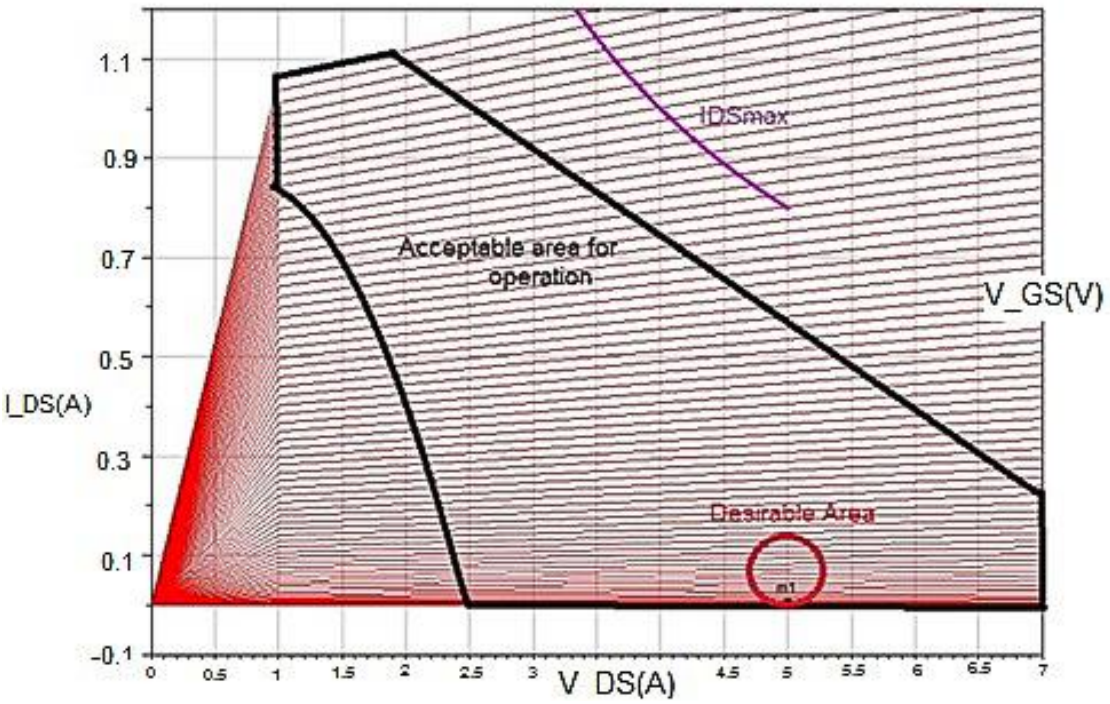


Figure 2. 8: FET bias characteristics and selection for ATF-511P8.

Table 2.6: VGS values for 4 different IDS values.

$I_{DS}(A)$	0.02503	0.04994	0.07483	0.09982
$V_{GS}\ (V)$	0.3935	0.4265	0.4525	0.475

2.6.2 Simulation for power amplifiers

Mostly linear power amplifiers act like a small signal amplifier. In order to estimate input impedance, S-parameter simulation can be helpful as a start point. But generally

power amplifiers turn nonlinear at a point, meaning that clipping, compression and distortion may happen. Thus, non-linear simulation is necessary in power amplifier design to estimate such effects. There are two options, harmonic balance (HB) as a frequency domain method, and transient analysis as a time domain method. As the power amplifier design is generally in frequency doman, HB analysis sounds more suitable and more effective, specifically in terms of saving time when convergence happens properly.

The key operation measurements benefiting from HB analysis with parameter sweeps include:

- Distortion
- Output power vs. Input power P_{IN}
- Gain vs. Input power P_{IN}
- Efficiency vs. Input power P_{IN}[25].

2.6.3 Load-Pull analysis

By performing load-pull analysis, the maximum attainable output power for a given impedance can be obtained on a Smitch chart in the form of a set of contours, as shown in figure 2.9. These contours helps to evaluate the actual impedance a transistor can have when used as an amplifier.

Furthermore, as a powerful help in design and assessment of power amplifiers, it is graphically useful to estimate the effect of any load changed from optimum load due to variations in the impedance at output. The device under test (DUT) or the amplifier operates between two impedances at input and at output, while two tuners (input and output tuner) sit between these impedances [26]. The Load pull setup provided by ADS is suitable for running load pull at a single bias point, input frequency and available source pull, as shown in figure 2.10.

For this project, load-pull and Source-pull analysis has been conducted 4 times for each voltage and current value mentioned in table 2.6 to find out in which biasing point, maximum output power and gain value can be obtained and finally the best biasing point has been selected and all results for both load and source pull analysis is presented in table 2.8.

The optimum load impedance is shown as 2.587-j*1.538Ω in figure 2.11 and if the device is matched to this load impedance, 35.53dBm of output power shall be obtained.

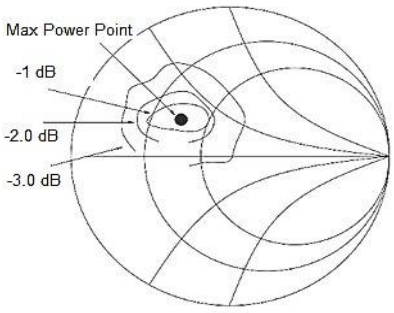


Figure 2. 9: Load-Pull contours.

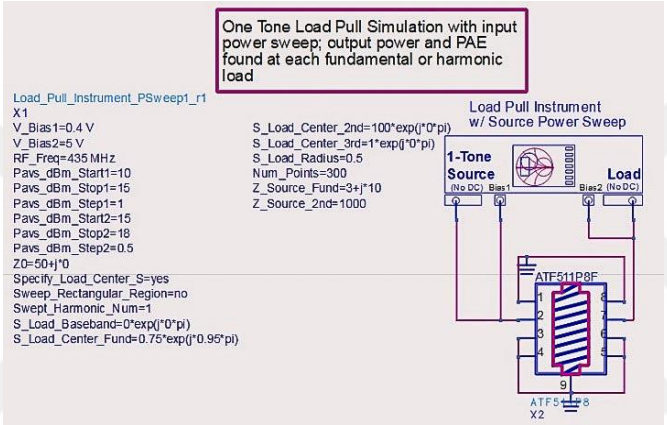


Figure 2. 10: One-tone load-pull simulation setup

By modifying the complex conjugate of source impedance as estimated by load pull simulation, the correct termination for the source can be seen. This result has been achieved by iterative simulations and observing the maximum delivered power and gain at maximum power as shown in figures below [27]. Table 2.7 shows the results of impedances, gain, PAE, delivered power and current for gain compression values.

Table2.7: Load-pull results

Zload_at_mPdel_vs_PAE	Z_In_at_mPdel_vs_PAE	PAE (%)	Bias Current (A)	Gain (dB)	Pdel (dBm)	Gain Compression vs. PAE (dB)
10.189+j*0.14	0.797-j*14.686	56.3	0.587	20.2	32.22	1.437
9.246+j*0.140	2.783-j*15.020	58.4	0.660	18.9	32.90	0.960
11.162+j*0.15	2.811-j*14.365	60.8	0.650	15.1	33.08	6.374

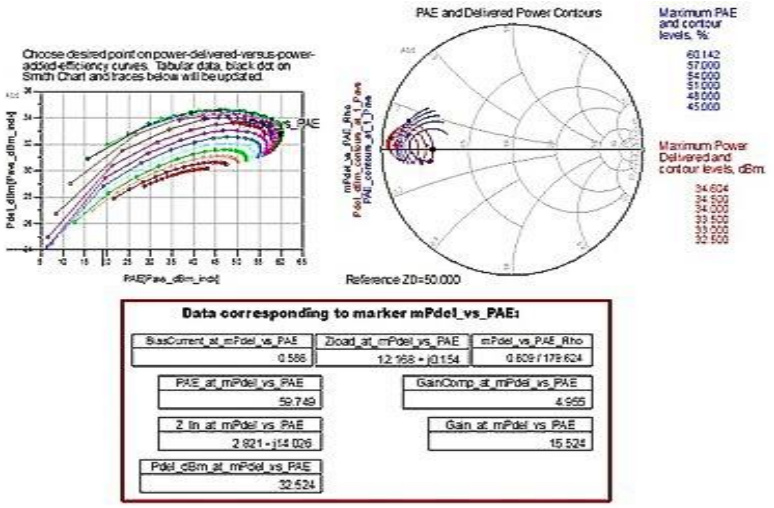


Figure 2. 11: Best PAE and delivered power contour on Smith Chart for load-pull analysis at I_DS=100mA.

From the figures and values above (figure 2.11), Z_load = 9.246+j*0.140 and Z_source = 2.783-j*15.020 for PAE=58.4% have been obtained.

2.6.4 Performance variation due to 2nd harmonic loads

When the power amplifiers have gain compression, the load impedance at harmonic frequencies affect the performance.

In order to analyze the load-pull for second harmonic, the second harmonic and phase of its reflection coefficient would be sweeping, while load imepedances at all harmonic will be kept fixed. The simulation setup in figure 2.12 and results in the figure 2.13 show as the phase of the 2nd harmonic load has changed, noticing difference in PAE and power can be observed[28].

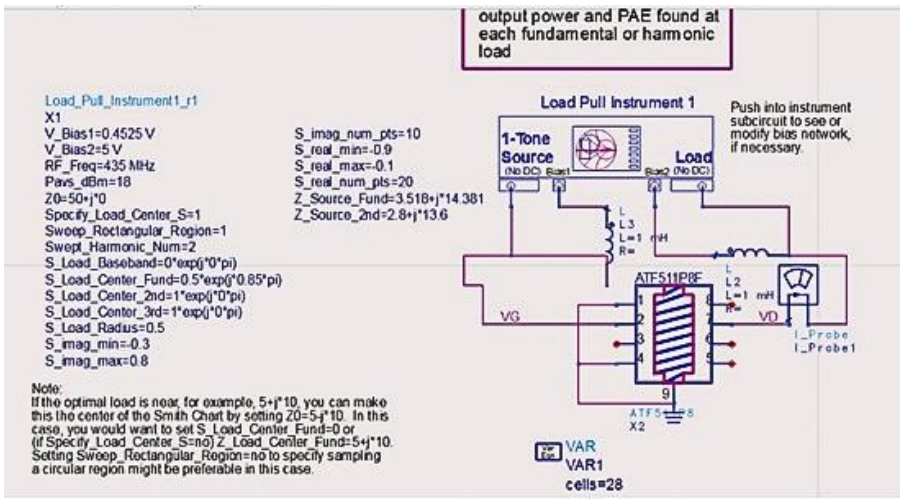


Figure 2. 12: One-tone load-pull simulation setup for 2nd harmonic analysis.

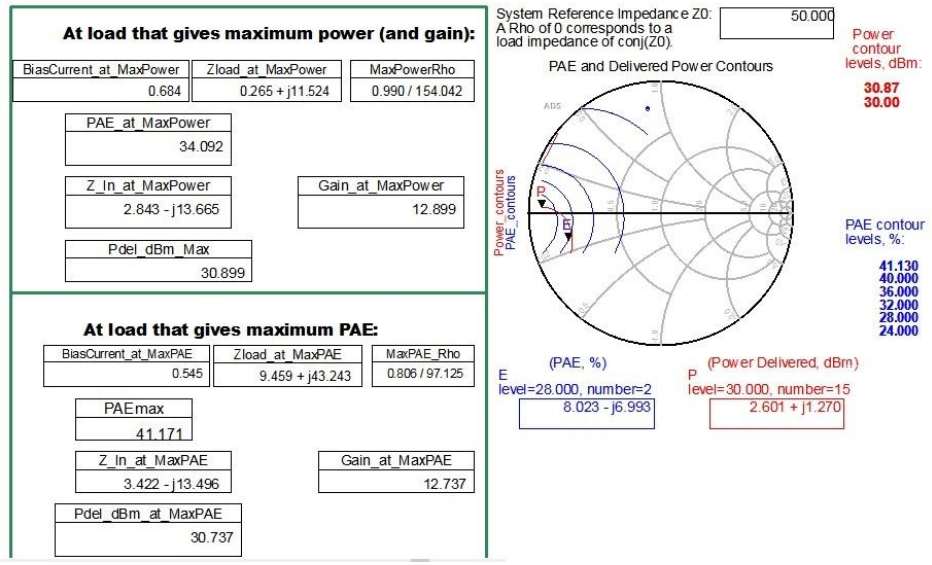


Figure 2. 13: Variation in the PAE and power delivered by sweeping the phase of the reflection coefficient at the 2nd Harmonic.

2.6.5 Source-Pull analysis

Source-pull analysis can be performed after extracting necessary information from Load-pull analysis. The aim is to achieve best source impedance and having maximum gain by reducing gain compression and have desirable level of output power. Load-pull and Source-pull analysis (figure 2.14) is conducted 4 times for each voltage and current value mentioned in table 2.6 to find out in which biasing point, max output power and gain value can be obtained and the best biasing point has been selected and all results for both load and source pull analysis is presented in table 2.8. The load has been terminated using the impedance of 2.587+j 1.538 and then iteratively change the source impedance to find out the impedance that gives the max gain.

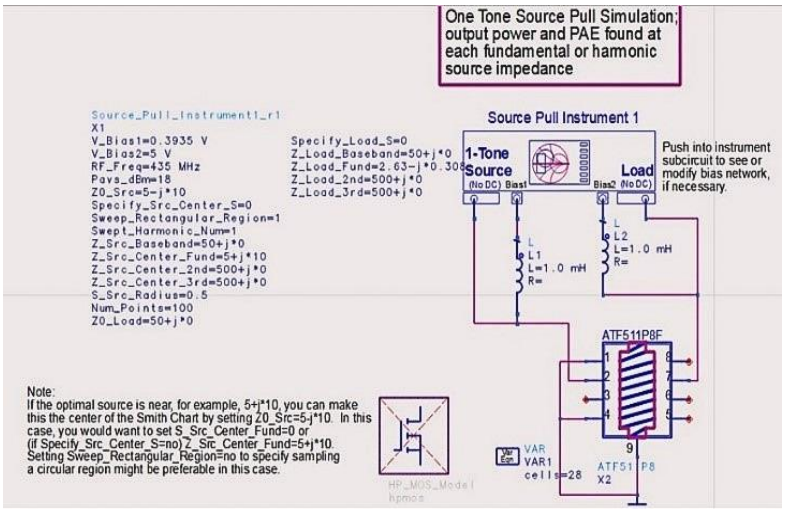


Figure 2. 14: Source-pull schematic.

Second part of Source-pull analysis would be done after designing the output matching network in order to find the right input impedance for designing the input matching network. Simulation results would be shown after designing the output matching network in the following section.

Similar process as for Load-pull has been done for Source pull as seen in figure 2.15:

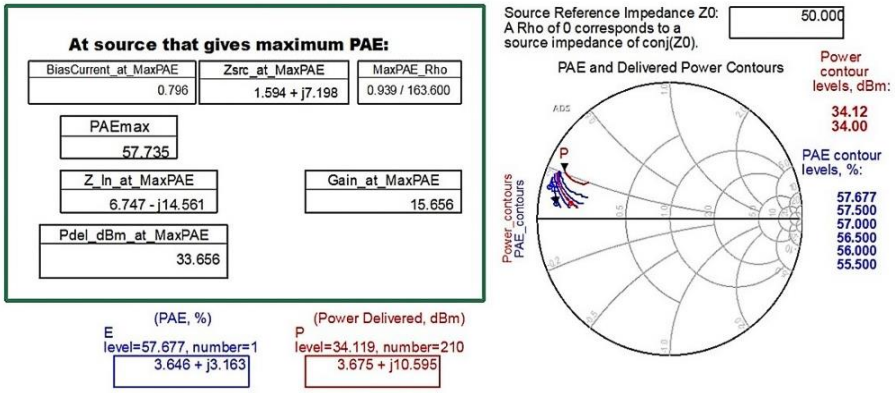


Figure 2. 15: Source-pull results for maximum PAE.

By iterative process, the value for input load has been obtained as: Zin=3.741+j*12.142.

Finally the input and the load impedance obtained from the load-pull and source pull analysis for 4 biasing points (table 2.8) can be summarized in the table below:

Table 2.8: Load-pull and Source-pull analysis results for four biasing points.

Load-Pull Analysis Results						
I_{DS} (mA)	V_{GS} (V)	Z_{Load}@Max Power	Z_{IN}@Max Power	PAE@ Max Power (%)	Gain@ Max Power (dB)	$P_{del}-Max$ (dBm)
25	0.39	2.63 -j*0.308	2.453-j*13.936	45.73	17.38	35.38
50	0.43	2.587-j*1.538	3.512-j*14.555	45.48	17.49	35.49
75	0.45	2.587-j*1.538	3.518-j*14.381	45.48	17.53	35.53
100	0.47	2.587-j*1.538	3.525-j*14.227	45.67	17.56	35.56
Source-Pull Analysis Results						
I_{DS} (mA)	V_{GS} (V)	Z_{Load}@Max Power	Z_{IN}@Max Power	PAE@ Max Power (%)	Gain@ Max Power (dB)	$P_{del}-Max$ (dBm)
25	0.39	1.392+j*11.32	2.996-j*17.006	41.48	16.18	34.18
50	0.43	3.741+j*12.14	2.808-j*14.16	42.58	16.58	34.58
75	0.45	3.741+j*12.14	2.808-j*14.158	42.58	16.58	34.58
100	0.47	3.741+j*12.14	2.789-j*13.765	42.72	16.63	34.63

Based on the results represented in table above, I_{DS}=100mA and V_{GS}=0.457V and Input_power=15dBm have been selected for the biasing of the transistor in order to obtain best Gain and output power for class-E power amplifier.

2.6.7 Input and output matching network design

Based on power amplifier design principles, in order to have maximum power transfer from source to load, the input impedance of a power amplifier shall be complex conjugate matched to the source. Figure 2.16 gives an insight on impedance matching.

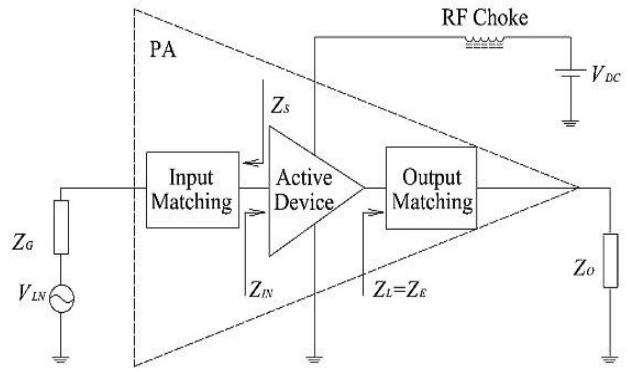


Figure 2. 16: Class-E power amplifier matching schematic.

If the condition $Z_S = Z^*_{IN}$ is satisfied, these options may happen:

• Maximum gain for the given load impedance can be obtained;

• All the available power from the source will be transfered to the input port of the active device;

The input reflection coefficient Γ_{IN} (corresponding to Z_{IN}) for a certain load reflection Γ_L, and by having active device S–parameters, can be calculated as:

$$\Gamma_{IN} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.24}$$

Class–E and Inverse-Class-E PA and such switching mode classes operate with dBs of gain compression, the linear theory can not be applied. It is impossible to roughly predict input impedance Z_{IN} without having an accurate nonlinear model or large signal measurements at the input of power amplifier. Though, benefiting from the linear approach, a proper primary predict for input matching design can be achieved[15]. L-type, π-type and T-type topology as well as load-pass and band-pass

or Chebyshev filters have been tried for both input and output matching network to obtain the maximum power at the laod and reduce dissipation at input and output. The input and output impedances can be design by having the load-pull and source-pull analysis, and these impedances will be matched with 50Ω using Smith Chart and matching tool of ADS.

In some literatures, a simple double stage amplifier [29], or a double stage amplifier consisting of class-F and class-E have been used [30].

Nathan Sokal [16], has developed clear and simple form of calculations for the network elements at any output power and loaded quality factor Q_L. These equations are:

$$R = 0.5768 \left(\frac{{V_{DD}}^2}{P_{OUT}}\right).\left(1 - \frac{0.451759}{Q_L} - \frac{0.402444}{{Q_L}^2}\right) \quad (2.25)$$

$$C = \frac{1}{5.44658\omega R}\left(1 + \frac{0.91424}{Q_L} - \frac{1.03175}{{Q_L}^2}\right) + \frac{0.6}{\omega^2.\ L_D} \quad (2.26)$$

$$C_o = \frac{1}{\omega R}\left(\frac{1}{Q_L - 0.104823}\right)\left(1 + \frac{1.01468}{Q_L - 1.7879}\right) - \frac{0.2}{\omega^2.\ L_D} \quad (2.27)$$

$$L_o = \frac{Q_L .R}{\omega} \quad (2.28)$$

where *P*out is the required output power, and ω is the angular switching frequency. For this project, following values have been calculated:
R= 6.4425 Ω C_o=12.993 pF L_o=11.78 nH C_{shunt}=18.7211 pF

2.6.8 Input matching network design

In order to design the input matching network and match the large signal input impedance of the RF device, the input impedance of transistor shall be predicted at input power, frequency, and biasing with the presence of the load and output matching networks[36].

At an input power of 15 dBm, the input impedance is approximately 9.246+j*0.140. The input matching network can thus be designed to match this value with the 50Ω source impedance. An emittance Smith chart can been used to construct either L-type, π-type or T-type matching network graphically. First the output matching network shall be designed, source-pull analysis including the output matching will be performed and the input matching network will be designed benefiting from the impedance obtained by this source pull analysis.

2.6.9 Output matching network design

In order to design the output matching network and match the large signal output impedance of the RF device, the output impedance of transistor shall be predicted at nominal output power, operating frequency, and bias voltages with the existence of the source and input matching networks[32].

The output impedance is approximately 2.783-j*15.020. The output matching network can thus be designed to match this value with the 50Ω output impedance. Smith chart has been used to construct E-class and Inverse-Class-E specific matching network. Not to forget that the Output return loss< -20 dB shall also be satisfied to give the best efficiency for highest output power.

2.6.10 Biasing

In order to have isolation between DC biasing system and the amplifier, RF chokes are frequently used at lower frequencies (lower than 1 GHz). For higher frequency applications with similar operation, λ/4 lines can be useful.

In order not to avoid losing power into the DC feed system, the rule of thumb is to have higher impedance for RF Choke than the load impedance, abstractly written as: $|Z_{choke}| \gg |Z_L|$

Potential problem is: Typically large Z_{choke} may not match with the amplitude modulation requirements because wideband digital signals may need small Z_{choke} [33].

Using finite DC feed inductance instead of an RF-choke in a Class-E PA has significant benefits, such as:

- Smaller size, less cost,
- More efficient output matching network by having a higher load resistance
- Reduction in supply voltage, which enables the implementation of the Class-E PA in low-voltage technologies and this is one of main design specificationg of this thesis,
- higher frequency of operation by having larger switch parallel capacitor C for the same supply voltage, output power and load.

Another advantage of using finite DC feed inductance can be oberved if the Class-E PA is applied in an envelope elimination and restoration (EER) system [37].

2.7 Simulation, Manufacturing, Tests and Results

In this part, the final design simulation, results, fabrican and test results would be presented for Class-E, Inverse-Class-E and the mixed structure. The software used to perform simulations is “Advanced Design System- ADS 2015.01” from Agilent. This software is specially designed to make and simulate high frequency RF circuits. It provides the possibility of making a layout of the circuit as well.

The simulation starts by designing the output impedance matching network, running Source-pull simulation, designing input matching network and adjusting structure in order to satisfy the design goals.

İn each part, first of all, design of the output matching network will be shown. In order to avoid repetition of procedure and similarity of results, the Source-pull structure will be presented only for Class-E design but not for each design. After simple structure simulation of input and output matching networks and presenting the results, transmission lines would be added and real model elements would be replaces in the circuit. Then final results before manucturing would be presented. In final section, the fabrication and test results will be investigates and presented.

2.7.1 Class-E design simulations

As mentioned in previous chapters of the thesis, Class-E design includes a shunt capacitor and parallel elemenets such as parallel L-C in order to suppress second and third harmonic. The trick in designing Class-E structure is having the switching function of the transistor, while matching the output impedance with least possible number of elements to keep the simplicity and aplicability. The Class-E output termination result can be seen in figure 2.17 for frequency range of 1MHz up to 1GHz on Smith Chart as well as S11, S22 and S21 in order to prove the matching is happening as desired. The results has been presented in figure 2.18.

Next step would be operating the Source-pull simulation to obtain the exact input impedance for designing the input matching network and implementing to the final circuit. The schematic of the source-pull as well as results have been presented in figures 2.19 and 2.20 and table 2.9 accordingly.

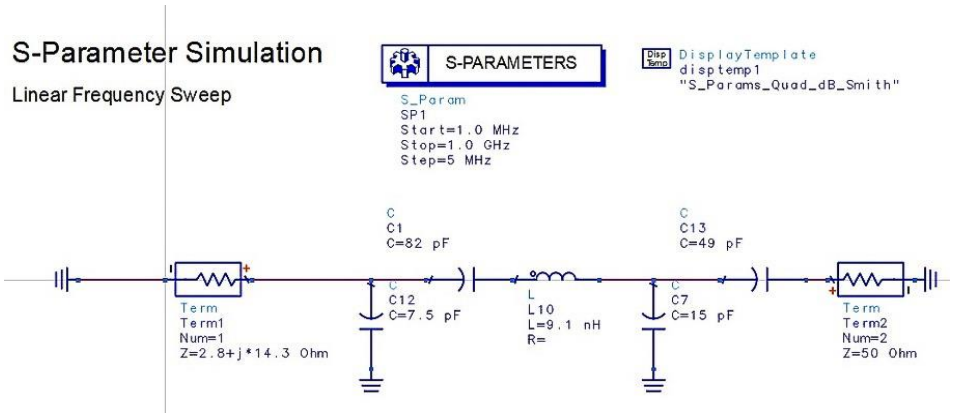


Figure 2. 17: Output termination for Class-E design.

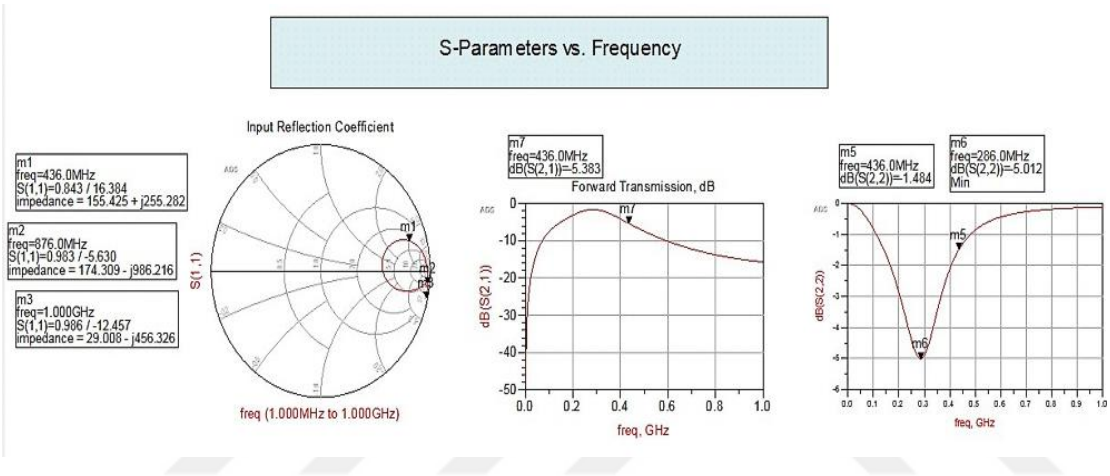


Figure 2. 18: Results of output termination for Class-E design.

Table 2.9: Results of **s**ource-pull analysis while having output matching network.

Z_Source	Z_Input	Gain (dB)	Delivered_Power (dBm)	PAE (%)	Bias_Current (A)
1.59+j*7.19	6.74-j*14.5	15.65	33.65	57.73	0.79

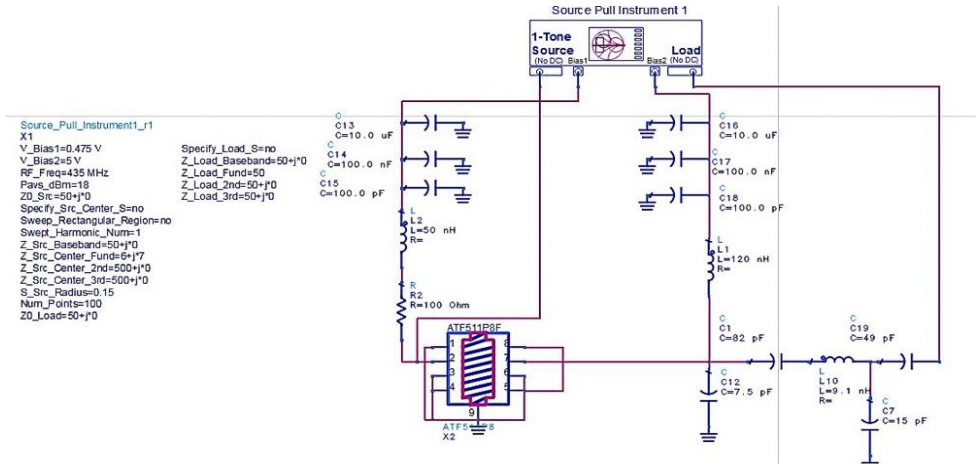


Figure 2. 19: Source-pull analysis while having output matching network.

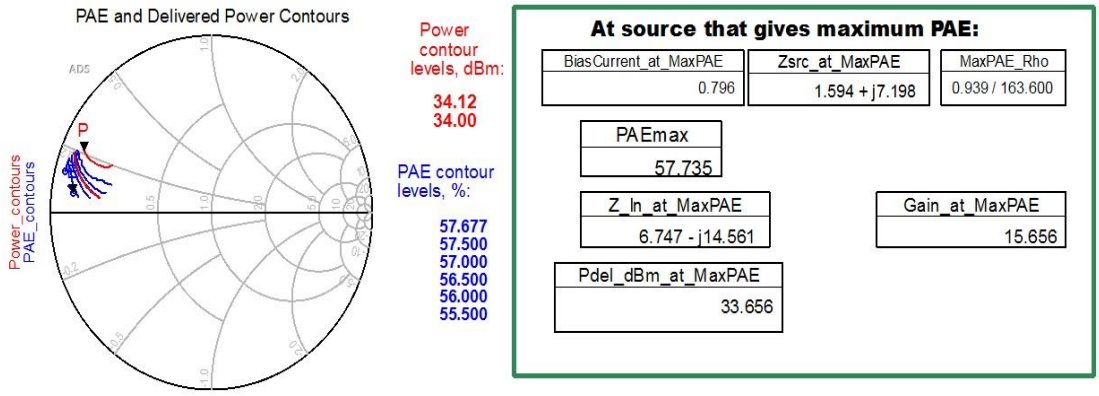


Figure 2. 20: Results of source-pull analysis while having output matching network.

After finding the input impedance, the input matching network can be designed and by integrating input and output matching network with biasing structure, the final circuit can be seen in figure 2.21.

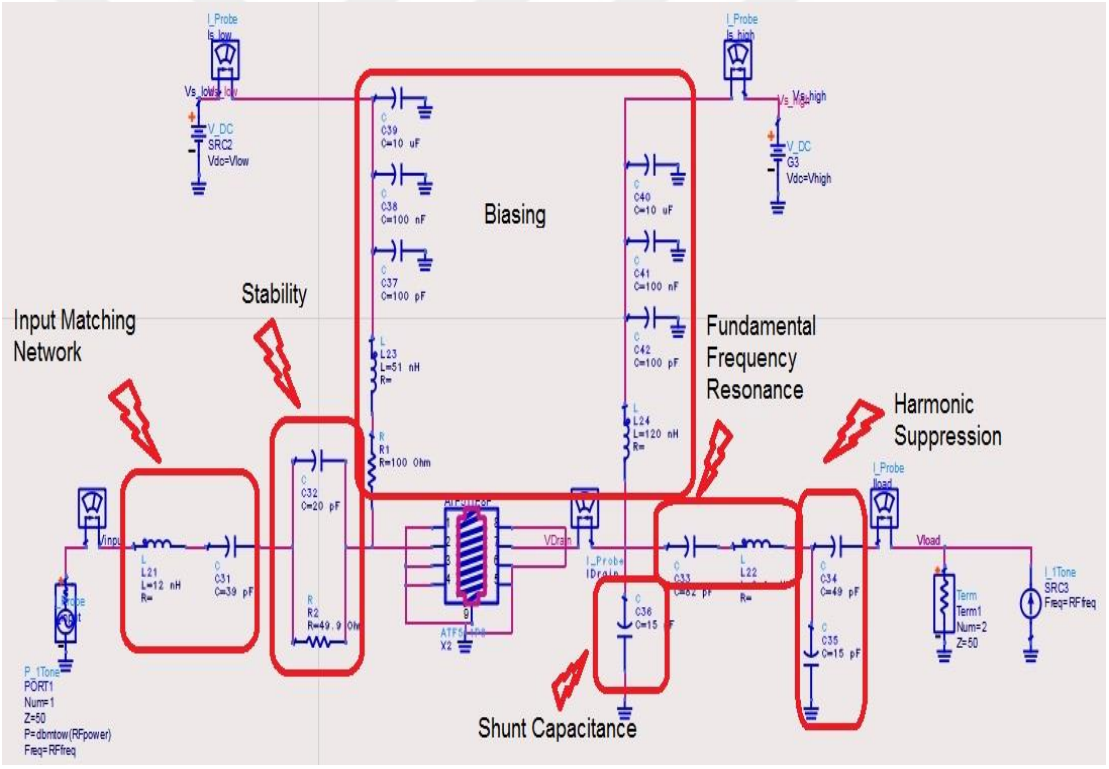


Figure 2. 21: Class-E power amplifier circuit schematic.

As it can be seen in figure 2.21, input matching network includes series LC and parallel R-C. this parallel R-C network, supports the stability of the amplifier up to 1GHz. Output matching network including shunt capacitance, series L-C as the fundamental frequency resonators, and L type structure for second and third harmonic suppression. The results can be seen in below table 2.10 and figures.

Table 2.10: Results of Class-E design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compression (dB)	PAE (%)	DC Power Consumption (W)	High Supply Current	Thermal Dissipation (W)
31.99	16.89	2.60	55.9	2.79	0.56	1.23

One of the main parameters of class-E design is seeing if the transistor is switching. The better the switching acts, the less power dissipation and more PAE can be expcted. Ideal condition is that drain current and voltage has no overlap to ideally the efficiency can be 100% but practically this is not feasible, though it can be implemented as good as possible by effective design of matching networks. Figure 2.22(right) proves the switching function of transist for this design by sweeping input power from 10 to 20 dBm. The switching function for Input_power=15dBm in figure 2.22(right).

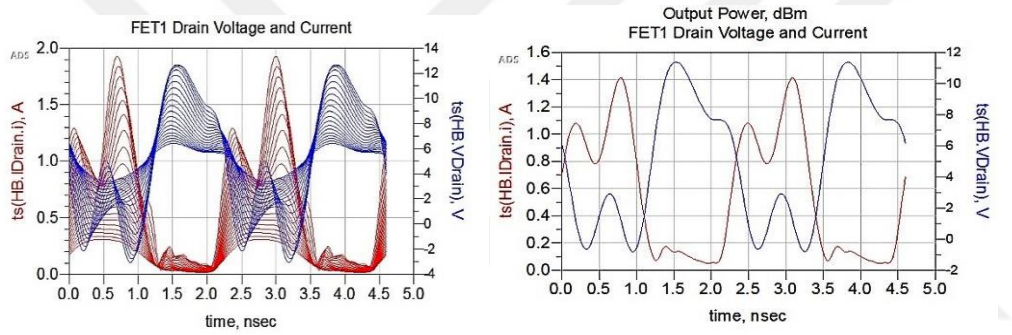


Figure 2. 22: Drain voltage and current (left) while sweeping input power and (right) for 15dBm input power.

Figrue 2.23 shows the input and output insertion loss, as well as S-parameters, including S11, S22 and S21 to show how matching networks are working effectively.

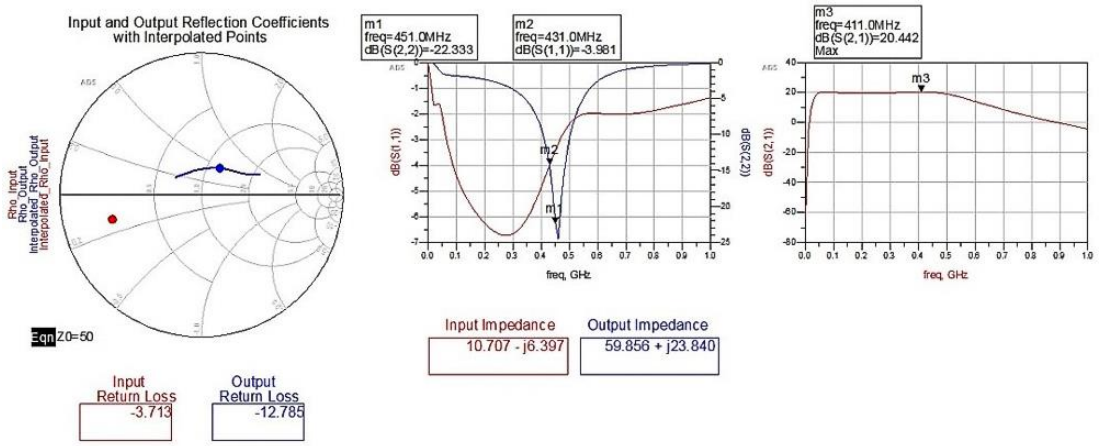


Figure 2. 23: Insertion loss and S-parameters for class-E design.

Delivered power to output, PAE and Transducer gain versus input power can be observed in figure 2.24.

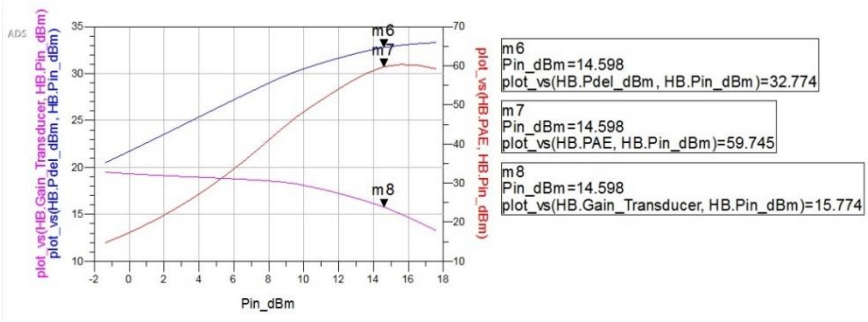


Figure 2. 24: Delivered power to output, PAE and transducer gain versus input power.

Harmonic suppression has been achieved successfully for up to fifth harmonic and results are presented in figure 2.25.

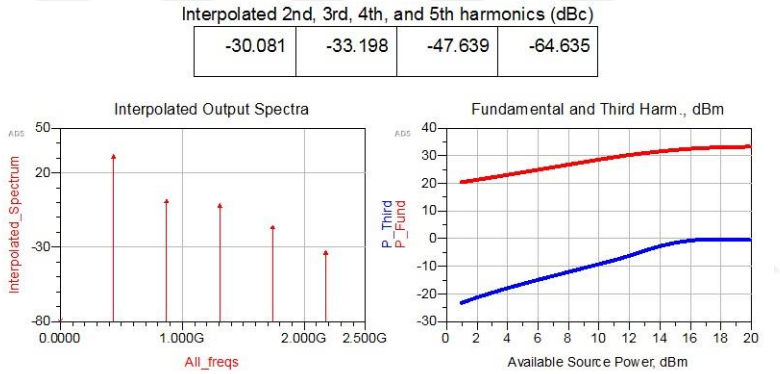


Figure 2. 25: Harmonic suppression for Class-E design.

Stability has been achieved for up to 1GHz as it can be seen in figure 2.26.

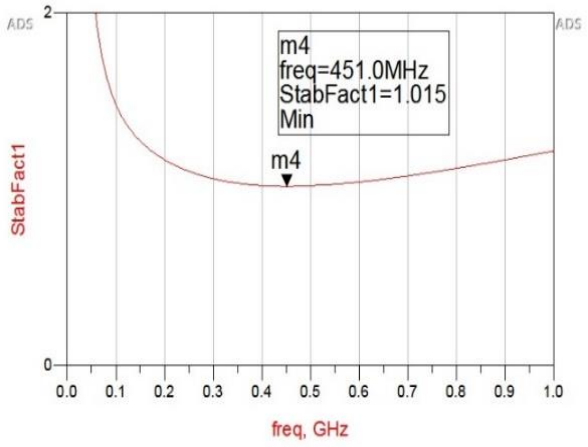


Figure 2. 26: Stability of Class-E design.

Finally figure 2.27 shows PAE versus output power and it proves that PAE of this design couldn't get higher due to limitation of gain compression which must be under 3dB and by increasing the output power, the PAE decreases after a certain extent.

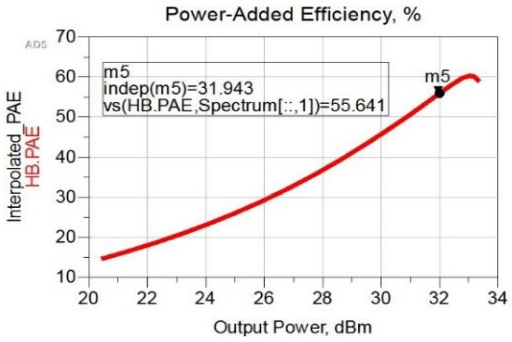


Figure 2. 27: PAE versus output power for Class-E design.

After this level, ideal elements have been replaced by real model elements from manufacturers such as TDK, Murata, Johnson, etc. Transmission lines have been added betweek elements for layout preparation. In UHF band, it is impossibe to transform elements into transmission lines as the dimension of design would be too large which is out of aim of this design and practically not feasible. On the other hand, due to impedances of tranmission lines and tolerance of real model elements, the value of some elements have been slightly changed in order to compensate the impedance variations and give the desirable class-E function. Length of transmission lines are kept as short as possible to not affect the impedance, and as long as it's needed for soldering elements. Widths of transmission lines are kept 1.8mm for 50Ω. Schematic of the circuit has been presented in figure 2.28.

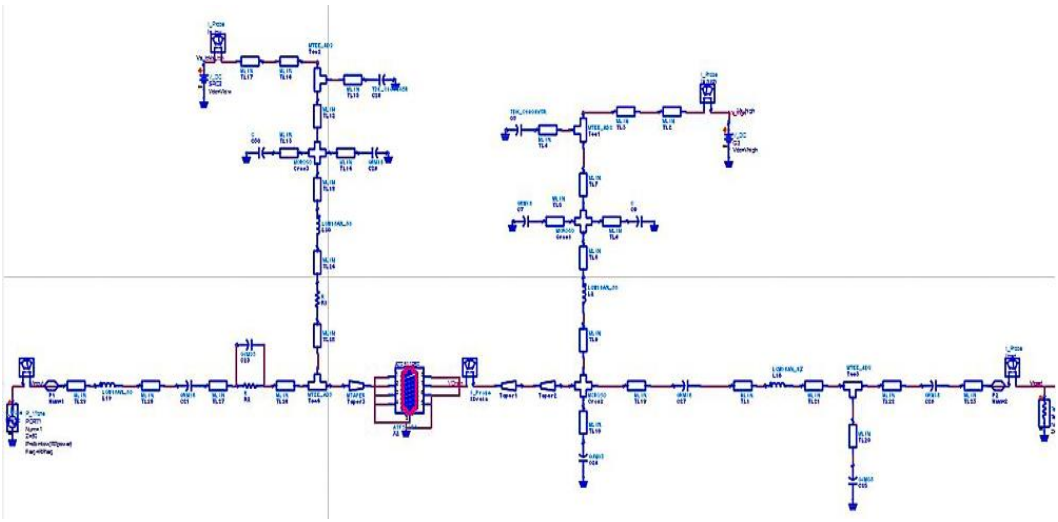


Figure 2. 28: Final schematic of Class-E design.

Results of final stage can be seen in figures below, starting with table of results (table 2.11) and figures of Class-E drain voltage and current while sweeping input power in figure 2.29 (right) and with 15dB input power in figure 2.29 (left).

Table 2.11: Results of Class-E design using real elements and transmission lines.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compression (dB)	PAE (%)	DC Power Consumption (W)	High Supply Current	Thermal Dissipation (W)
30.99	16.14	2.91	50.5	2.46	0.49	1.21

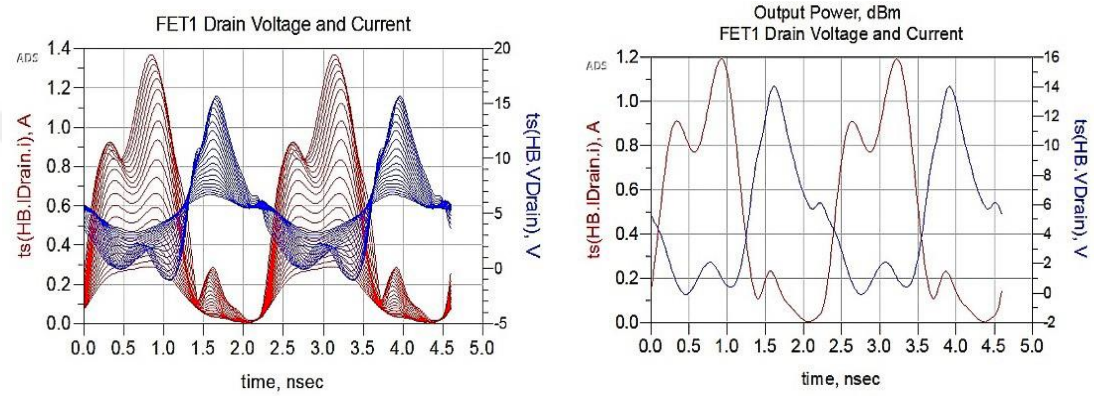


Figure 2. 29: Drain voltage and current (left) while sweeping input power and (right) for 15dBm input power for Class-E design using real model elements and transmission lines.

Figrue 2.30 shows the input and output insertion loss, as well as S-parameters, including S11, S22 and S21 to show how matching networks are working effectively.

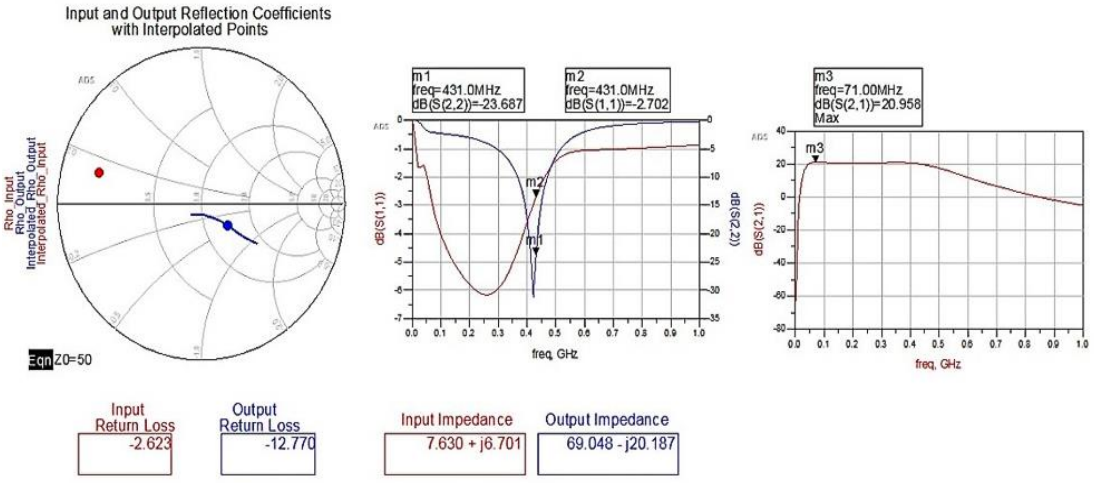


Figure 2. 30: Insertion loss and S-parameters for class-E design using real model elements and transmission lines.

Delivered power to output, PAE and Transducer gain versus input power can be observed in figure 2.31.

Harmonic suppression has been achieved successfully for up to fifth harmonic and results are presented in figure 2.32.

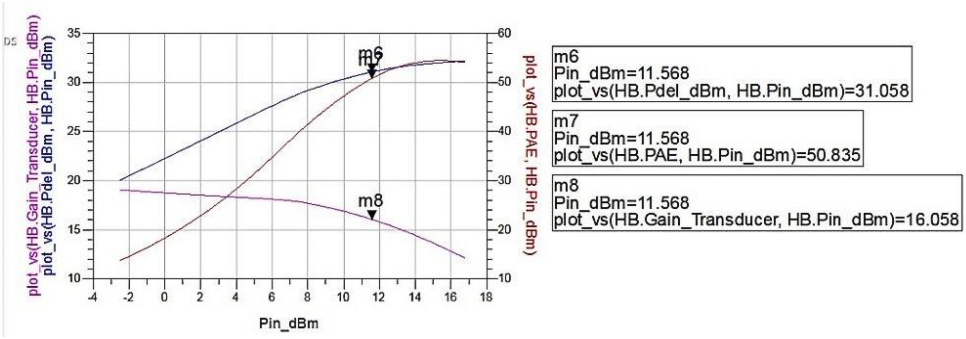


Figure 2. 31: Delivered power to output, PAE and transducer gain versus input power for Class-E design using real model elements and transmission lines.

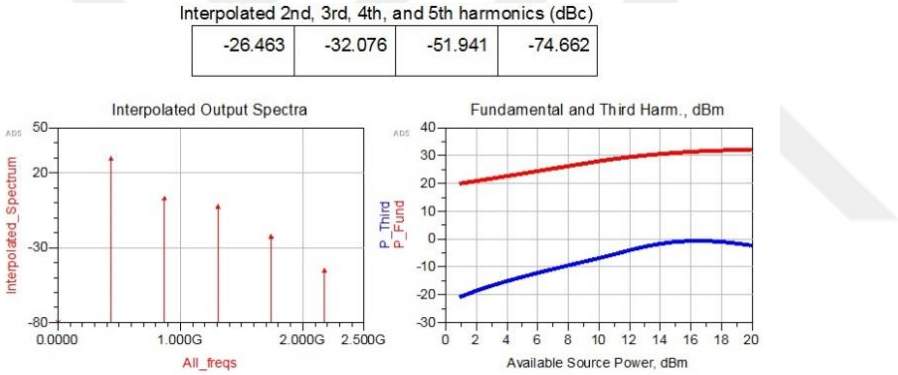


Figure 2. 32: Harmonic suppression for Class-E design using real model elements and transmission lines.

Stability has been achieved for up to 1GHz as it can be seen in figure 2.33.

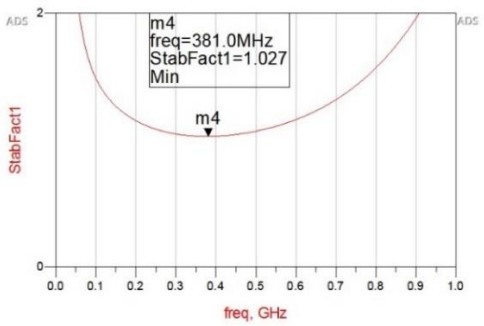


Figure 2. 33: Stability of Class-E design using real elements and transmission lines.

Finally figure 2.34 shows PAE versus output power

Figure 2. 34: PAE versus output power for Class-E design.

2.7.2 Inverse-Class-E simulation

Many of the details mentioned for Class-E design will not be repeated here again, so generally the schematic and results with less explanation would be presented. The difference of designing Class-E with Inverse-Class-E is in the output matching network. As mentioned before, class-E includes shunt capacitance but Inverse-Class-E deisgn includes series inductance right after the drain so that the switching current has a path and switching performance of transistor can be satisfies. Then series L-C has been used as fundamental frequency resonator and harmonic suppression has been realized by using a shunt inductance. Again, the simplicity is respected. Input matching network (from transistor going towards input port) includes parallel R-C for the sake of stability up to 1GHz, series capacitance for DC-blocking, and Pi-type structure for matching purpose has been used. The output termination for Inverse-Class-E can be seen in figure 2.35 and results in figure 2.36, then schematic of complete circuit is presented in figure 2.37 and results are presented in following figures.

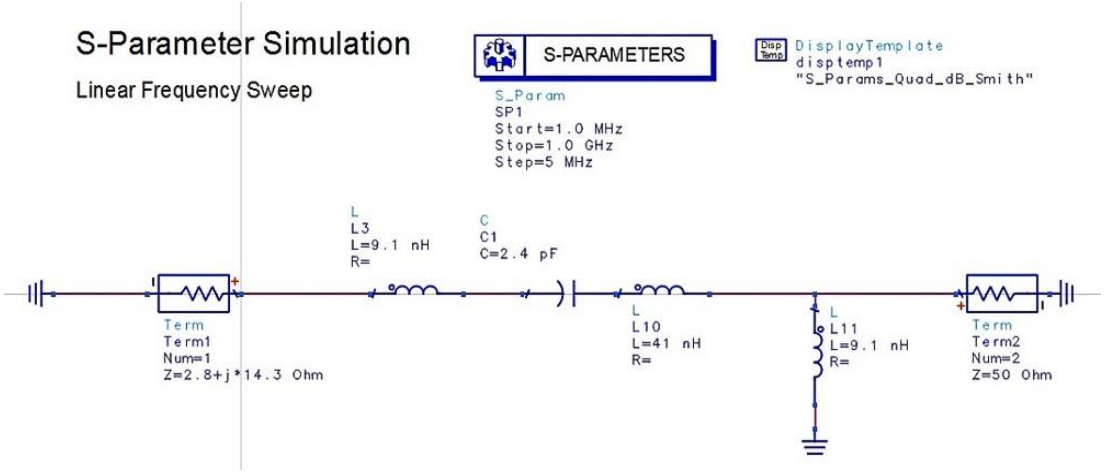


Figure 2. 35: Output termination for Class-E design.

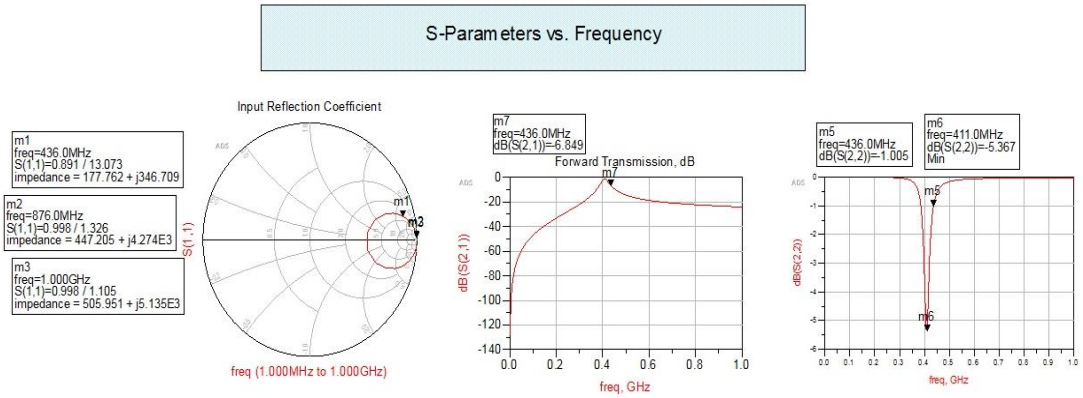


Figure 2. 36: Results of output termination for Class-E design.

By integrating input and output matching network with biasing structure, the final circuit can be seen in figure 2.37.

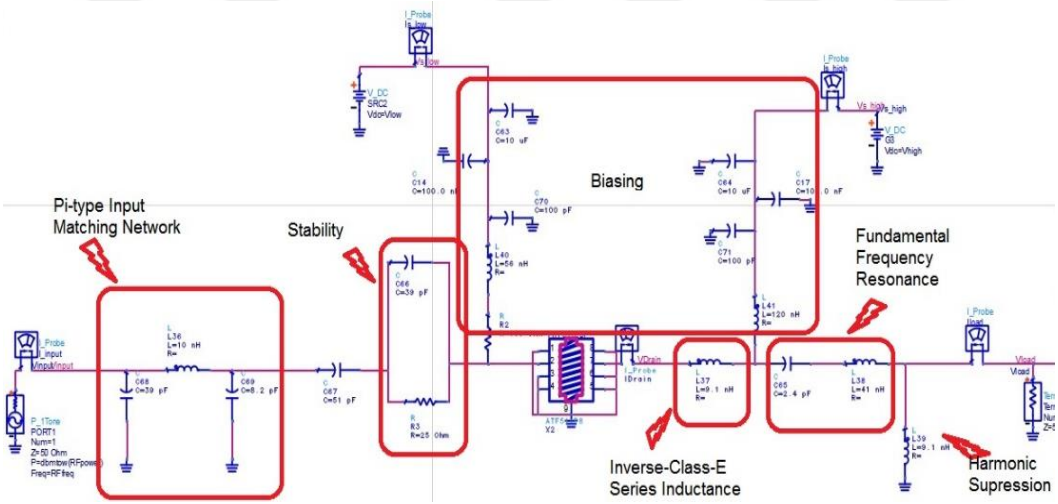


Figure 2. 37: Inverse-Class-E power amplifier circuit schematic.

As it can be seen in figure 2.37, input matching network includes parallel R-C, series DC blocking capacitance, and π-type matching network. this parallel R-C network, supports the stability of the amplifier up to 1GHz. Output matching network including series inductance, series L-C as the fundamental frequency resonators, and a shunt inductance for harmonic supression. The results can be seen in below table 2.12 and figures.

Table 2.12: Results of Inverse-Class-E design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compression (dB)	PAE (%)	DC Power Consumption (W)	High Supply Current	Thermal Dissipation (W)
29.98	20.53	2.83	47.2	2.09	0.49	1.10

One of the main parameters of class-E design is seeing if the transistor is switching. Figure 2.38(right) proves the switching function of transist for this design by sweeping input power from 10 to 20 dBm. The switching function for Input_power=9dBm in figure 2.38(right).

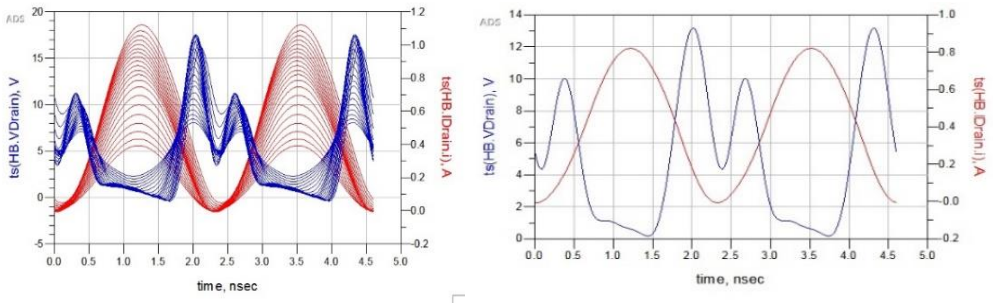


Figure 2. 38: Drain voltage and current (left) while sweeping input power and (right) for 9 dBm input power.

Figrue 2.39 shows the input and output insertion loss, as well as S-parameters, including S11, S22 and S21 to show how matching networks are working effectively.

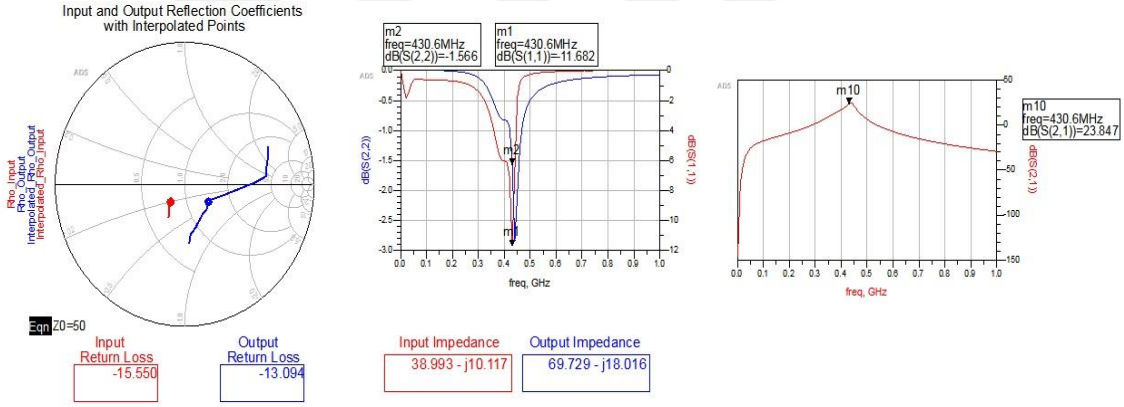


Figure 2. 39: Insertion loss and S-parameters for Inverse-class-E design.

Delivered power to output, PAE and Transducer gain versus input power can be observed in figure 2.40.

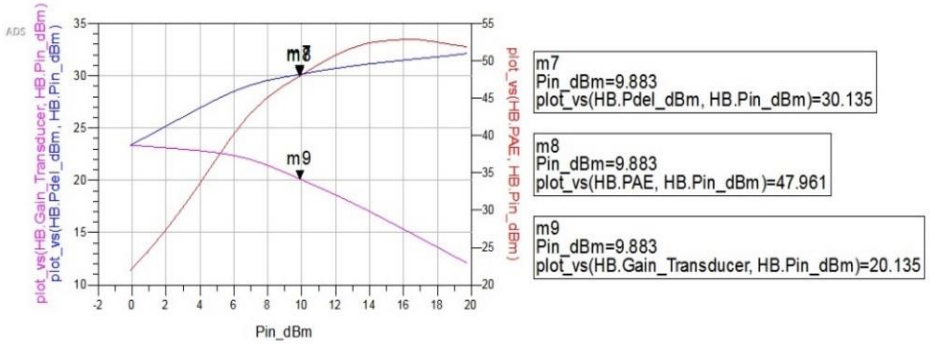


Figure 2. 40: Delivered power, PAE and transducer gain versus input power.

Harmonic suppression has been achieved successfully for up to fifth harmonic and results are presented in figure 2.41.

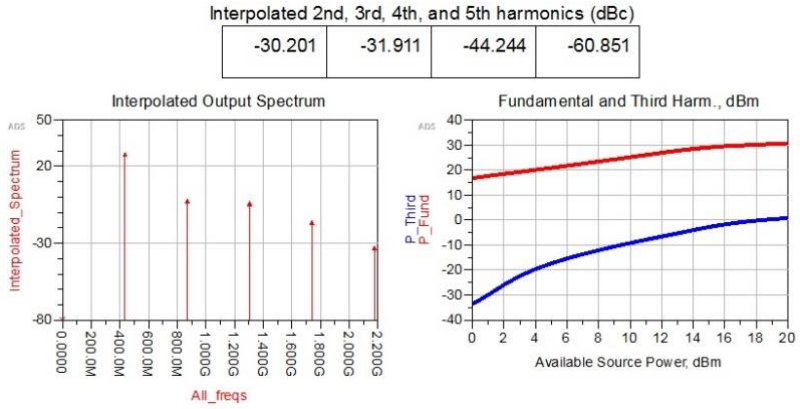


Figure 2. 41: Harmonic suppression for Inverse-Class-E design.

Stability has -been achieved for up to 1GHz as it can be seen in figure 2.42.

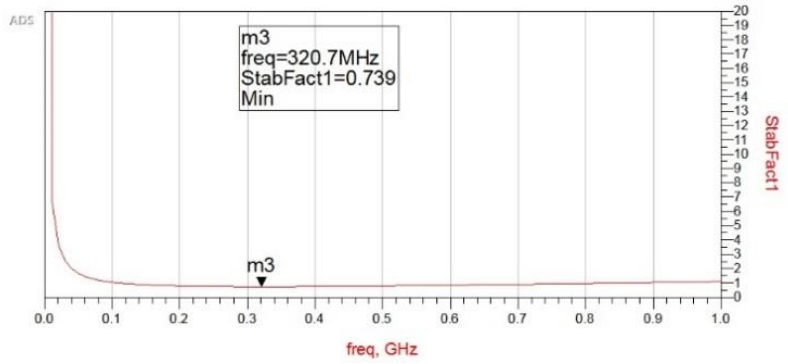


Figure 2. 42: Stability of Inverse-Class-E design.

Finally figure 2.43 shows PAE versus output power.

Figure 2. 43: PAE versus output power for Inverse-Class-E design.

After this level, ideal elements have been replaced by real model elements. Transmission lines have been added betweek elements for layout preparation. Due to impedances of tranmission lines and tolerance of real model elements, the value of

some elements have been slightly changed in order to compensate the impedance variations and give the desirable inverse-class-E function. Schematic of the circuit has been presented in figure 2.44.

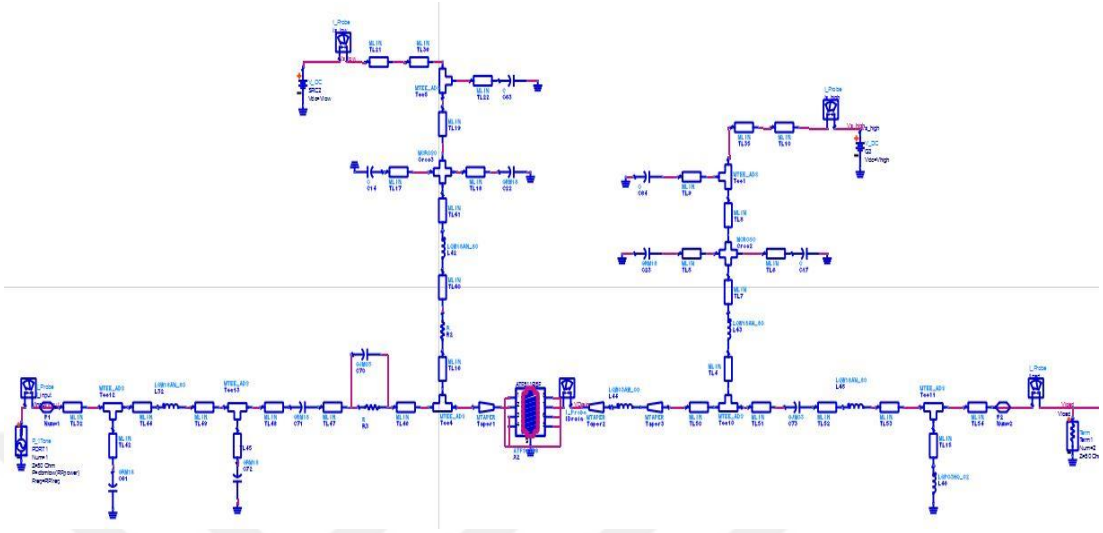


Figure 2. 44: Final schematic of Inverse-Class-E design.

Results of final stage can be seen in figures belos, starting with table of results (table 2.13) and figures of Inverse-Class-E drain voltage and current while sweeping input power in figure 2.45 (right) and with 14.5dB input power in figure 2.45 (left).

Table 2.13: Results of Inverse-Class-E using real elements and transmission lines.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compressi -on (dB)	PAE (%)	DC Power Consumpti -on (W)	High Supply Current	Thermal Dissipation (W)
29.49	15.04	2.76	37.4	2.33	0.46	1.46

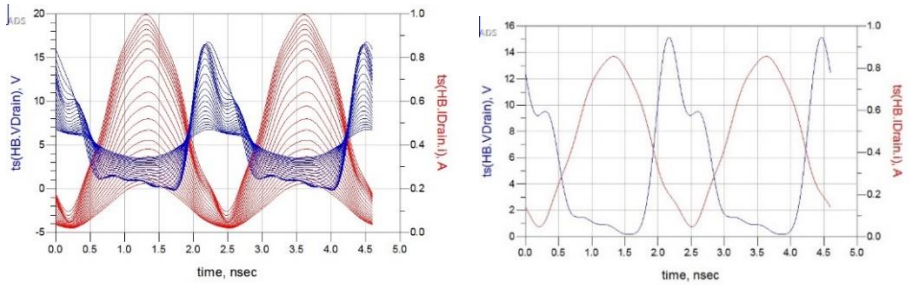


Figure 2. 45: Drain voltage and current (left) while sweeping input power and (right) for 14.5dBm input power for Inverse-Class-E design using real model elements and transmission lines.

Figrue 2.46 shows the input and output insertion loss, as well as S-parameters, including S11, S22 and S21 to show how matching networks are working effectively.

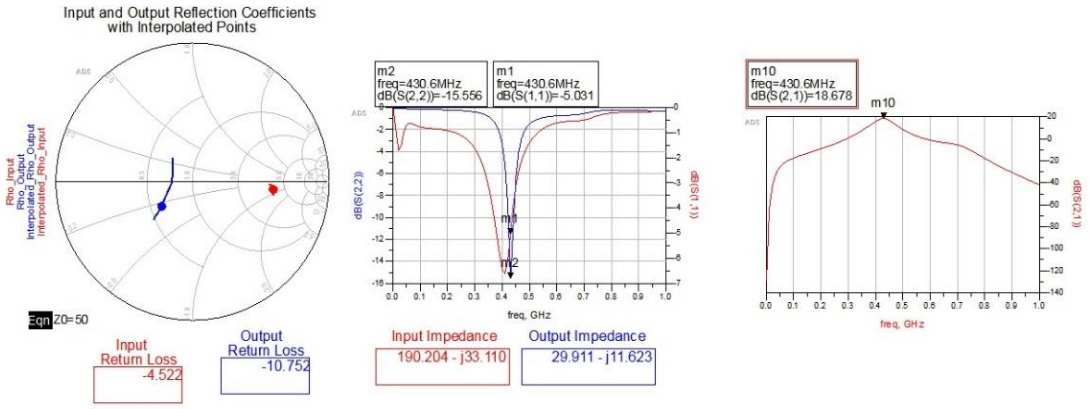


Figure 2. 46: Insertion loss and S-parameters for inverse-class-E design using real model elements and transmission lines.

Delivered power to output, PAE and Transducer gain versus input power can be observed in figure 2.47.

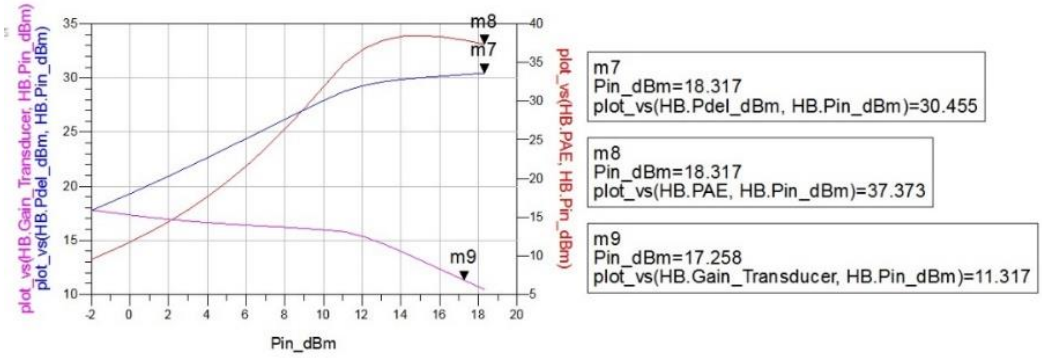


Figure 2. 47: Delivered power to output, PAE and transducer gain versus input power for Inverse-Class-E design using real model elements and transmission lines.

Harmonic suppression has been achieved successfully for up to fifth harmonic and results are presented in figure 2.48.

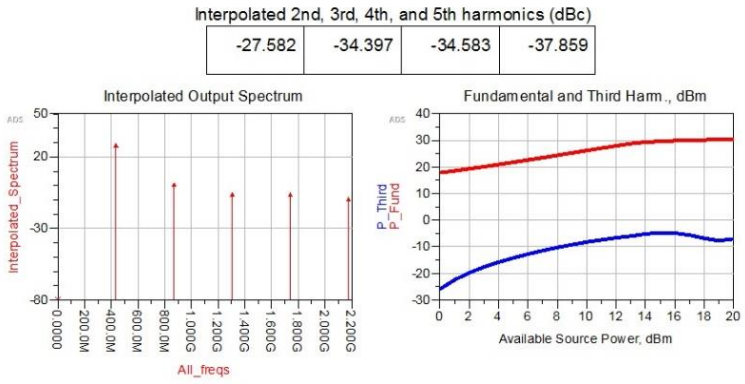


Figure 2. 48: Harmonic suppression for Inverse-Class-E design using real model elements and transmission lines.

Stability has been achieved for up to 1GHz as it can be seen in figure 2.49.

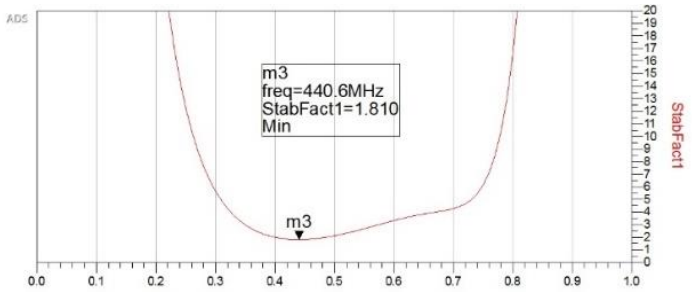


Figure 2. 49: Stability of Inverse-Class-E design using real elements and transmission lines.

Finally figure 2.50 shows PAE versus output power.

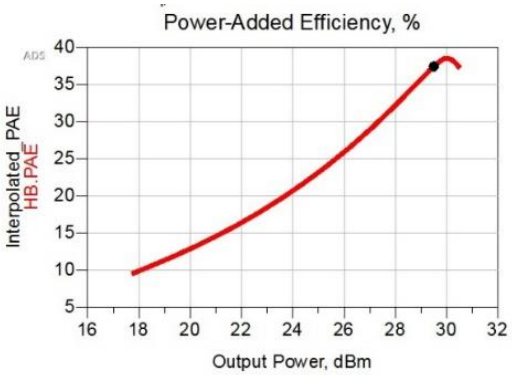


Figure 2. 50: PAE versus output power for Inverse-Class-E design.

2.7.3 Mix of Class-E and Inverse-Class-E Structure

For the first time, a mixture of class-E and inverse-class-E structure has been introduced and designed for the first time. It opens a door towards designing a new structure for switching power amplifiers and further works.

This novel design includes series inductance, shunt capacitance, fundamental frequency resonance, and parallel network for harmonic supression. In comparison to class-E, this new structure has 1 dBm higher output power, better input and output insertion loss and better harmonic supression. In comparison to Inverse-Class-E with almost similar gain compression and less elements in input matching network, it shows 10% higher PAE and 2 dBm more output power which shows the superiority of this design against Inverse-Class-E.

Then series L-C has been used as fundamental frequency resonator and harmonic suppression has been realized by using a shunt capacitance. Again, the simplicity is respected. Input matching network (from transistor going towards input port) includes

parallel R-C for the sake of stability up to 1GHz, series capacitance for DC-blocking, and L-type structure for matching purpose. The output termination for Inverse-Class-E can be seen in figure 2.51 and results in figure 2.52, then schematic of complete circuit is presented in figure 2.53 and results are presented in following figures.

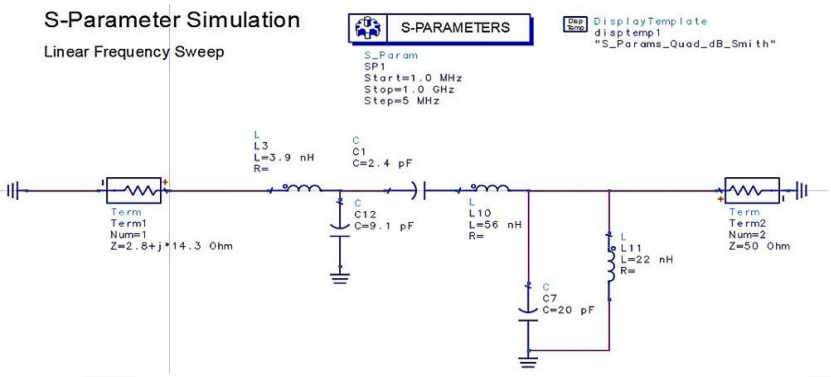


Figure 2. 51: Output termination for Mixed design.

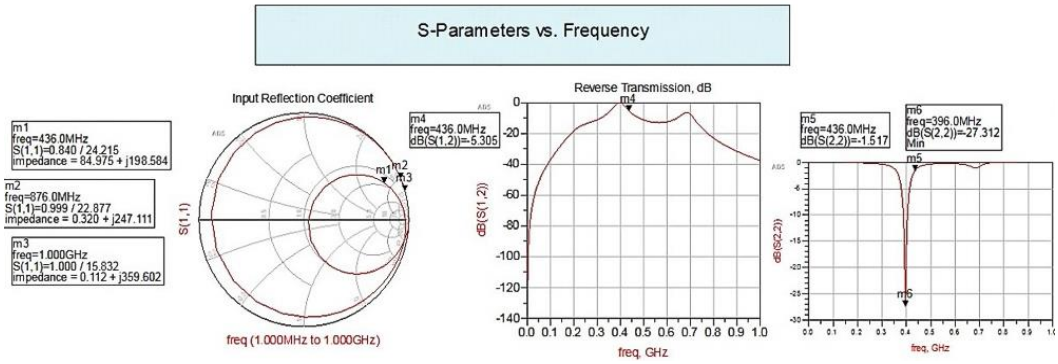


Figure 2. 52: Results of output termination for Mixed design.

By integrating input and output matching network with biasing structure, the final circuit can be seen in figure 2.53.

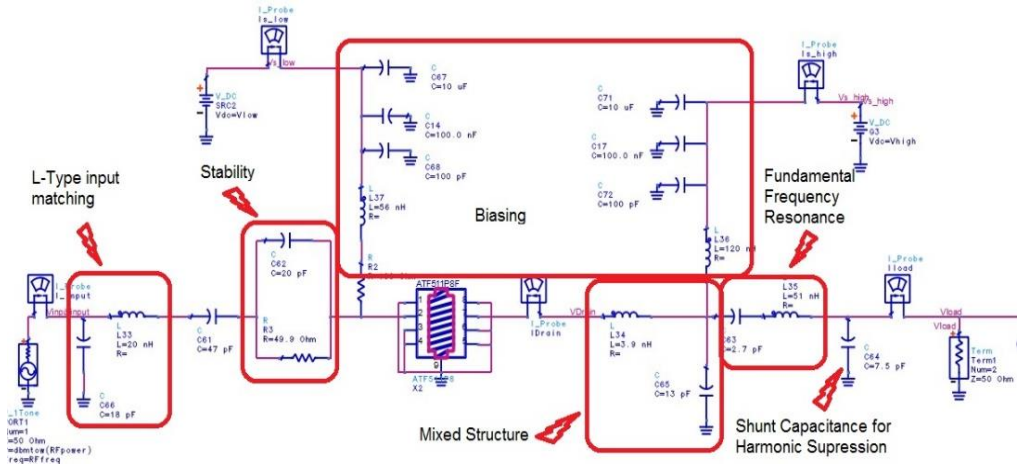


Figure 2. 53: Mixed design power amplifier circuit schematic.

As it can be seen in figure 2.53, input matching network includes parallel R-C. this parallel R-C network, supports the stability of the amplifier up to 1GHz. Output matching network including series inductance, series L-C as the fundamental frequency resonators, and a shunt inductance for harmonic supression. The results can be seen in below table 2.14 and figures.

Table 2.14: Results of Mixed design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre -ssion (dB)	PAE (%)	DC Power Consumption (W)	High Supply Current	Thermal Dissipation (W)
32.98	16.88	0.82	57	3.42	0.68	1.47

One of the main parameters of class-E design is seeing if the transistor is switching. Figure 2.54(right) proves the switching function of transist for this design by sweeping input power from 10 to 20 dBm. The switching function for Input_power=16.2dBm in figure 2.54(right).

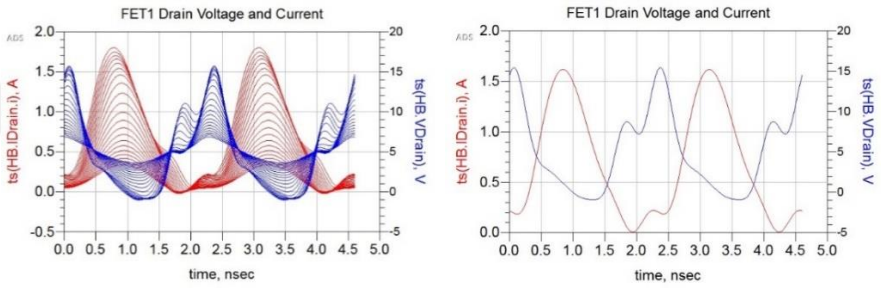


Figure 2. 54: Drain voltage and current (left) while sweeping input power and (right) for 16.2dBm input power.

Figrue 2.55 shows the input and output insertion loss, as well as S-parameters, including S11, S22 and S21 to show how matching networks are working effectively.

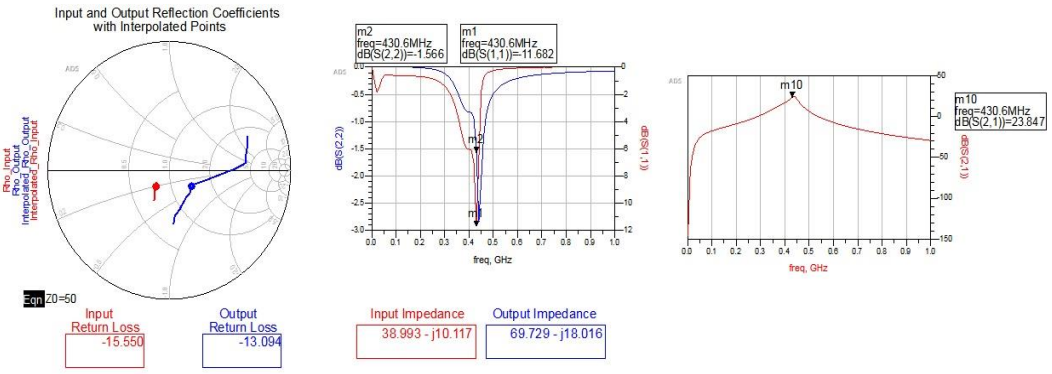


Figure 2. 55: Insertion loss and S-parameters for Mixed design.

Delivered power to output, PAE and Transducer gain versus input power can be observed in figure 2.56.

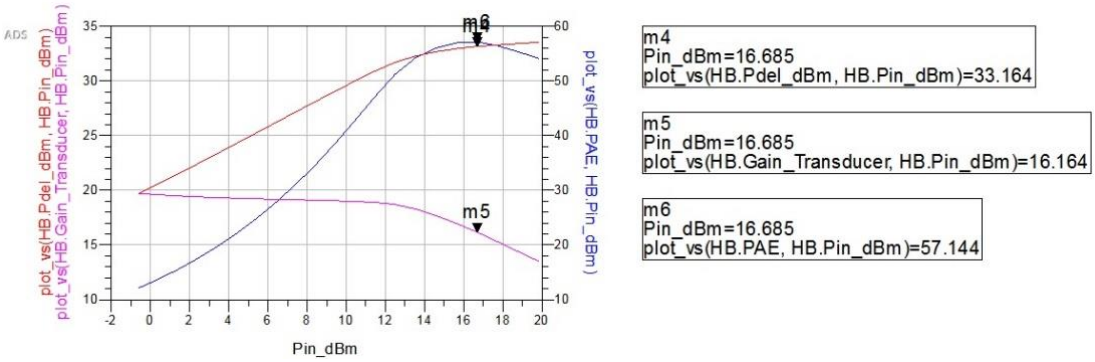


Figure 2. 56: Delivered power, PAE and transducer gain versus input power.

Harmonic suppression has been achieved successfully for up to fifth harmonic and results are presented in figure 2.57.

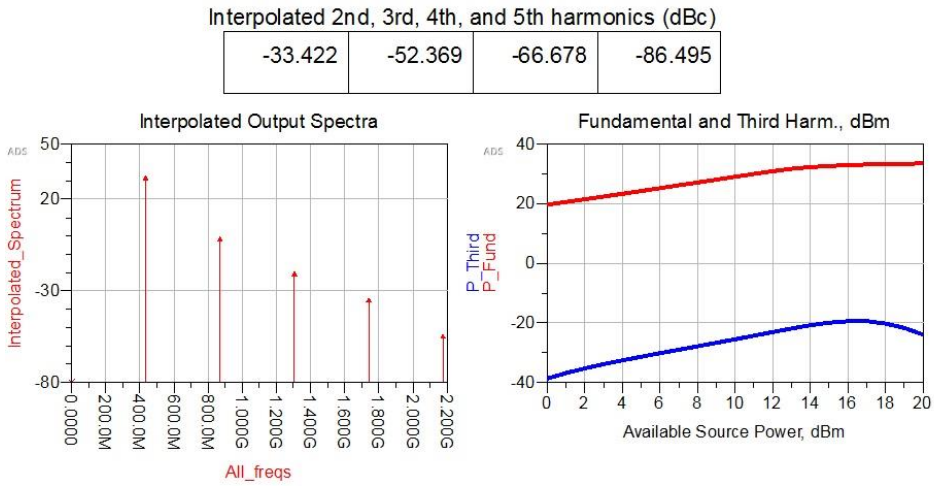


Figure 2. 57: Harmonic suppression for Mixed design.

Stability has been achieved for up to 1GHz as it can be seen in figure 2.58.

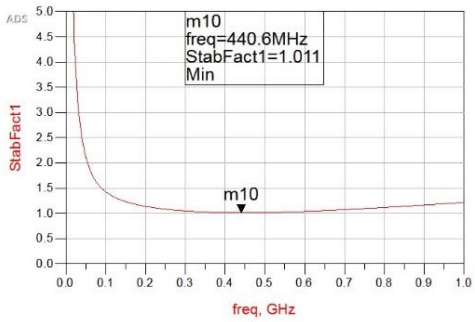


Figure 2. 58: Stability of Mixed design.

Finally figure 2.59 shows PAE versus output power.

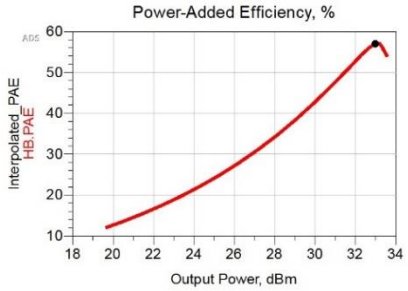


Figure 2. 59: PAE versus output power for Mixed design.

After this level, ideal elements have been replaced by real model elements. Transmission lines have been added betweek elements for layout preparation. Due to impedances of tranmission lines and tolerance of real model elements, the value of some elements have been slightly changed in order to compensate the impedance variations and give the desirable mixed design function. Due to complexity of the design, results changes more than expected. Schematic of the circuit has been presented in figure 2.60.

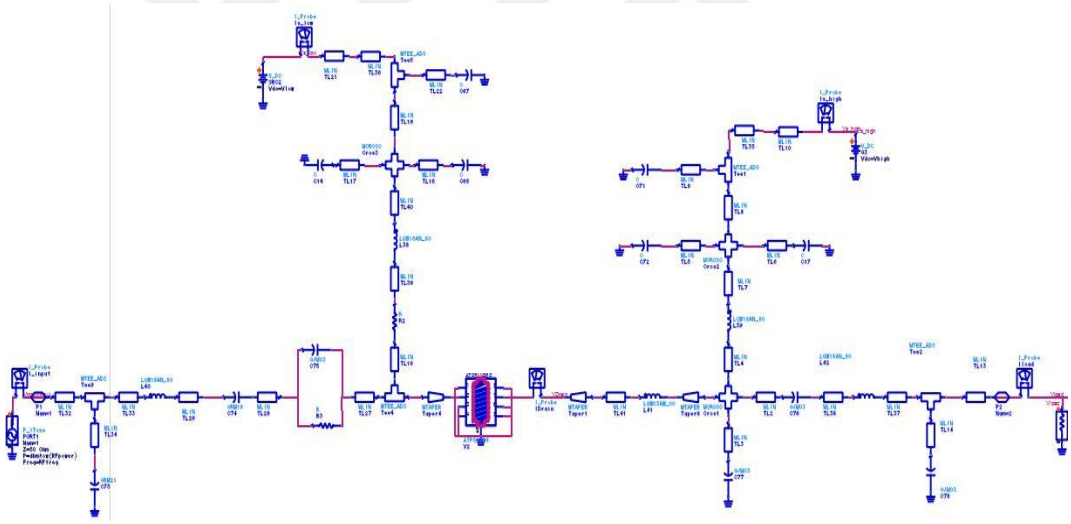


Figure 2. 60: Final schematic of Mixed design.

Results of final stage can be seen in figures belos, starting with table of results (table 2.15) and figures of mixed design drain voltage and current while sweeping input power in figure 2.61 (right) and with 18.4dB input power in figure 2.61 (left).

Table 2.15: Results of Mixed design using real elements and transmission lines.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compression (dB)	PAE (%)	DC Power Consumption (W)	High Supply Current	Thermal Dissipation (W)
31.48	13.13	2.75	43.2	3.19	0.64	1.82

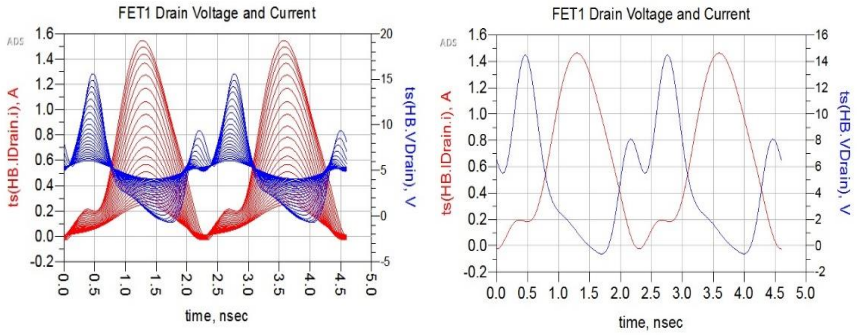


Figure 2. 61: Drain voltage and current (left) while sweeping input power and (right) for 18.4dBm input power for Mixed design using real model elements and transmission lines.

Figrue 2.62 shows the input and output insertion loss, as well as S-parameters, including S11, S22 and S21 to show how matching networks are working effectively.

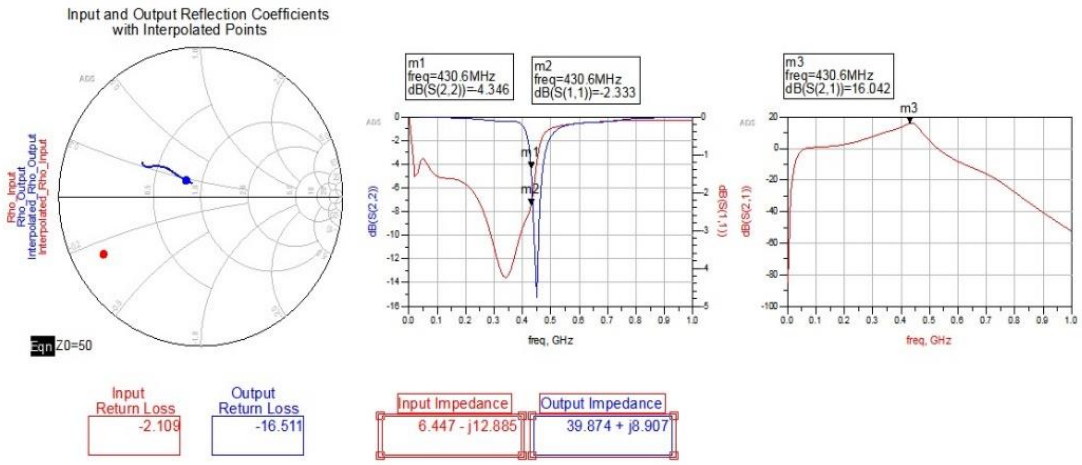


Figure 2. 62: Insertion loss and S-parameters for Mixed design using real model elements and transmission lines.

Delivered power to output, PAE and Transducer gain versus input power can be observed in figure 2.63.

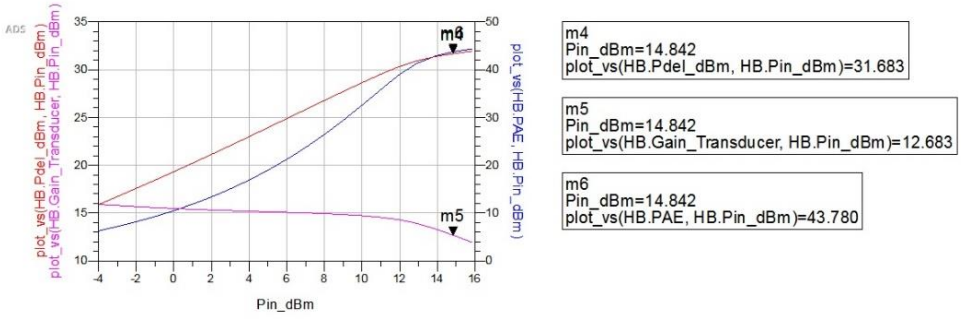


Figure 2. 63: Delivered power to output, PAE and transducer gain versus input power for mixed design using real model elements and transmission lines.

Harmonic suppression has been achieved successfully for up to fifth harmonic and results are presented in figure 2.64.

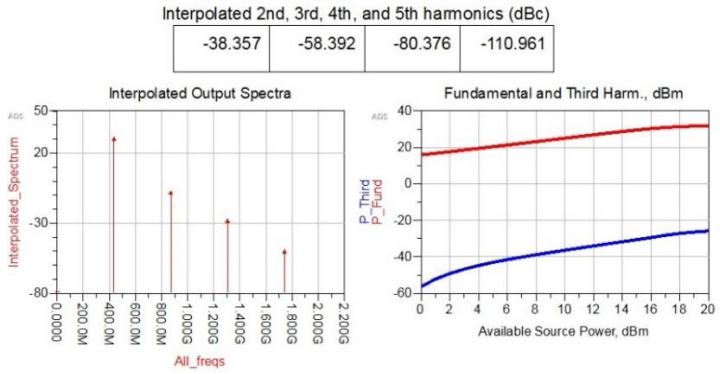


Figure 2. 64: Harmonic suppression for Mixed design using real model elements and transmission lines.

Stability has been achieved for up to 1GHz as it can be seen in figure 2.65.

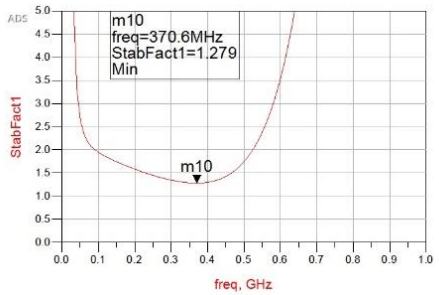


Figure 2. 65: Stability of Mixed design using real elements and transmission lines.

Finally figure 2.66 shows PAE versus output power

Figure 2. 66: PAE versus output power for Mixed design.

2.8 Layout Preparation and Fabrication

In this section, the layout preparation and fabrication would be discussed and presented for each design separately and in accordance with the previouse section.

2.8.1 Class-E design layout and fabrication

Layout of Class-E design has been prepared using ADS software and with the real models libraries. Figue 2.67 shows the layout of Class-E design ready for fabrication.

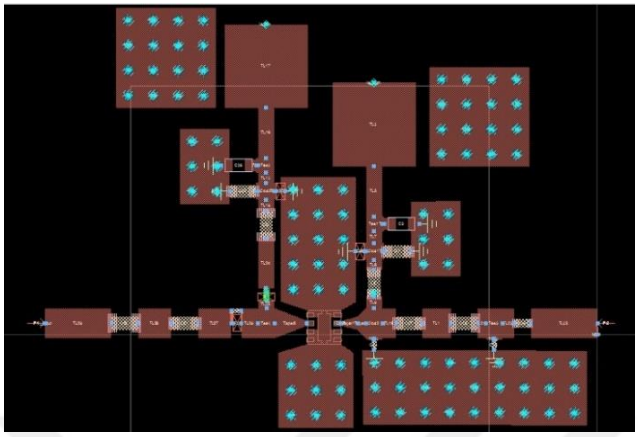


Figure 2. 67: Layout of Class-E design.

Fabrication was done in mechatronic research center of ITU and figure 2.68 shows the fabricated circuit and figure 2.69 shows the prepared and final circuit.

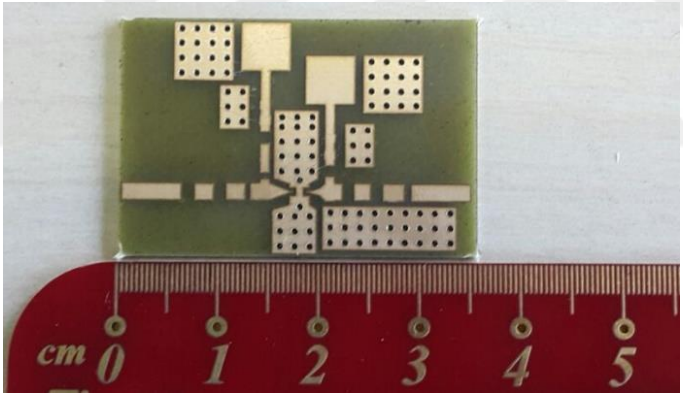


Figure 2. 68: Fabricated Class-E circuit before soldering the elements.

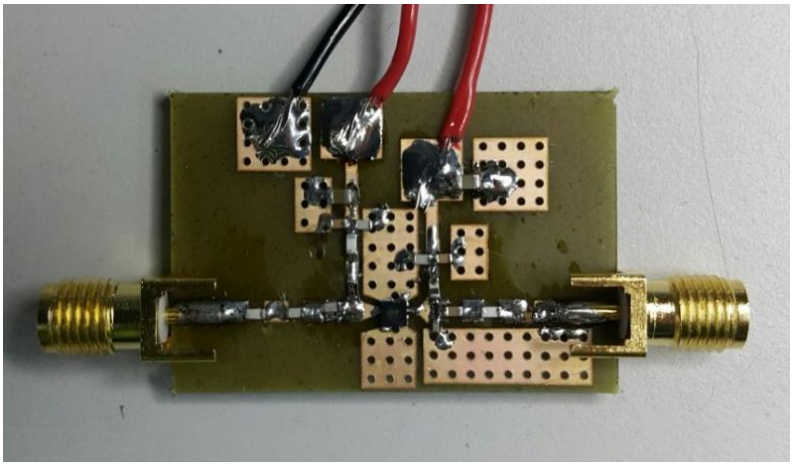


Figure 2. 69: Soldered and final circuit ready for measurement.

2.8.2 Inverse- Class-E design layout and fabrication

Layout and fabricated circuit for Inverse-Class-E power amplifier can be seen in figures 2.70 and 2.71 as follows and figure 2.72 shows the prepared and final circuit.

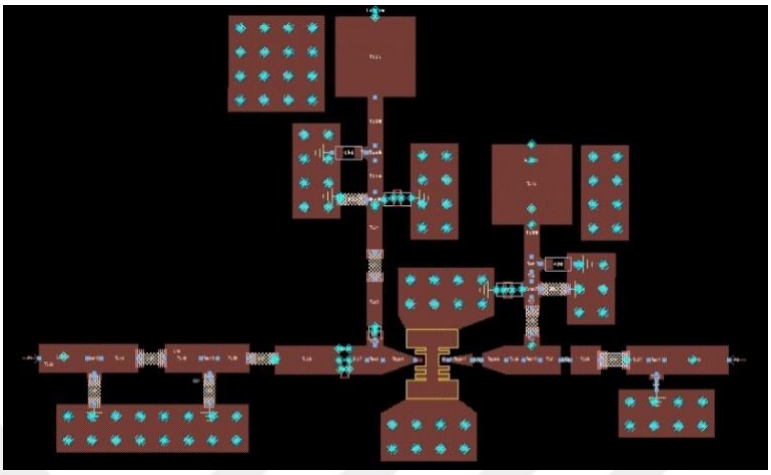


Figure 2. 70: Layout of Inverse-Class-E design.

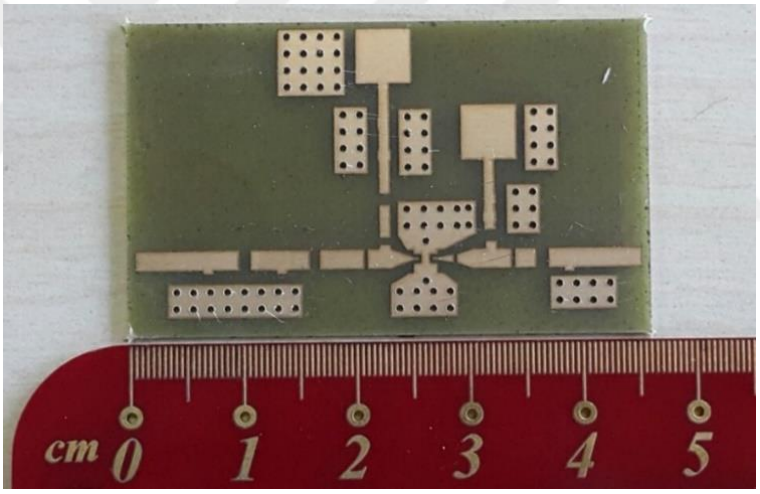


Figure 2. 71: Fabricated Inverse-Class-E circuit before soldering the elements.

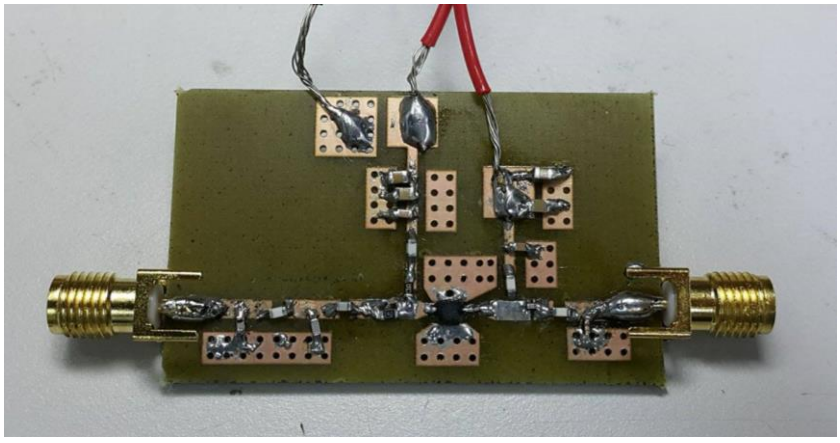


Figure 2. 72: Soldered and final Inverse-Class-E circuit ready for measurement.

2.8.3 Mixed design layout and fabrication

Layout and fabricated circuit for Mixed power amplifier can be seen in figures 2.73 and 2.74 as follows and figure 2.75 shows the prepared and final circuit.

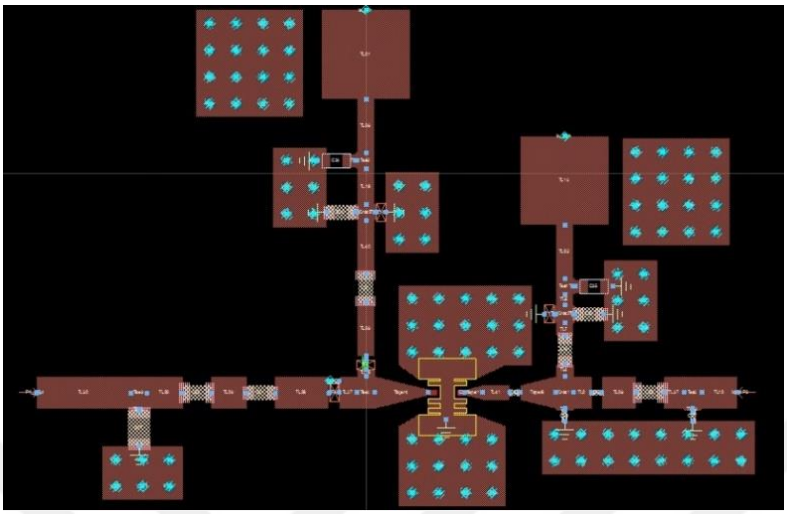


Figure 2. 73: Layout of Mixed design.

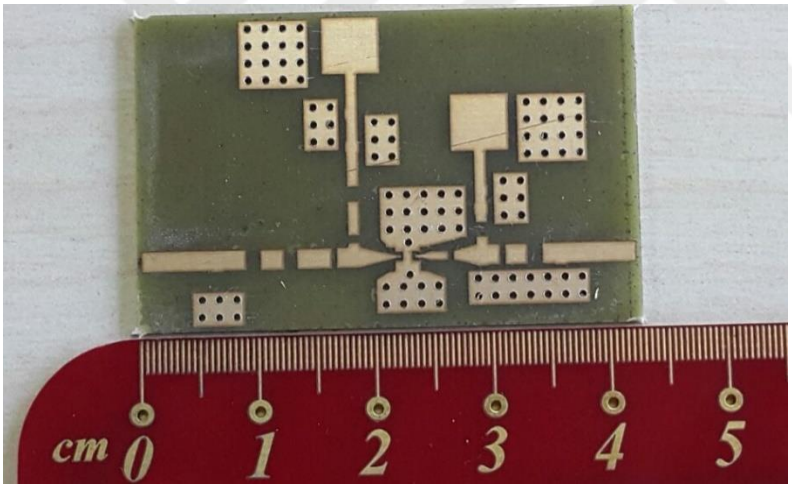


Figure 2. 72: Fabricated Mixed design circuit before soldering the elements.

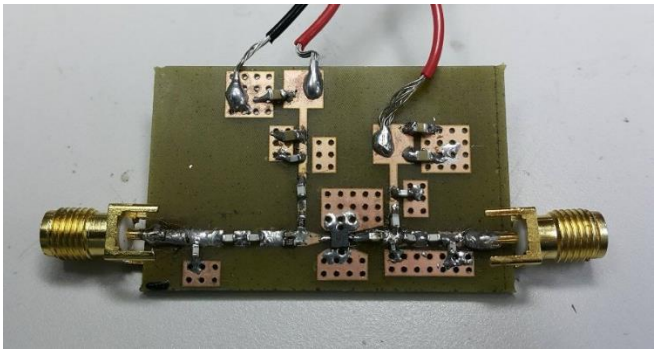


Figure 2. 75: Soldered and final Mixed design circuit ready for measurement.

For the mixed design, one of the most important element's value (51nH) was not available. So two circuits with close values of 47nH and 56nH has been selected and two separate circuits are prepared for tests and measurements. Each of their results wuld be presented.

A complete list of all elements used in this design has been presented in Appendix B.

2.9 Measurement Results

In this part, the measurements and results will be discussed. For a power amplifier, S-parameter measurements are of vital importance. Class-E, Inverse-Class-E and Mixed design's S-parameter measurements will be presented accordingly. For mixed design, two circuits have been prepared, both were measured, and results would be presented. Due to technical problem of the measurement device, only S11 and S21 parameters have been measured by Network Analyzer (Rhode and Schwartz, FSH8, 100 KHz-8GHz).

Next step of measurements was done by giving input power by Mini-Circuits synthesized signal generator (SSG-6000RC, 25-6000MHz) and measuring the output power by R&S spectrum analyser and by calculations, gain, DC power, drain efficiency and power added efficiency was calculated and results will be presented in following section for each circuit. Mini-circuits signal generator could provide up to +10 dBm input power and in order to increase it to +20 dBm, another power amplifier has been used as a driving amplifier to amplify the input power up to desired value. Attenuators have been used for the protection of measuring tool.

2.9.1 Class-E design S-parameters measurement

S11 nad S21 parameters have been measured for each circuit. The measurement setup can be seen in figure 2.76. +3dB attenuator in input and +10dB attenuator have been used in output. DC values have been given based on design parameters, drain voltag of +5v and 0.4v for gate, giving 100mA of current in drain to have the switching function of the power amplifier. The setup has been kep similar for measurements of four circuits.

S11 nad S21 parameters have been measured for Class-E circuit in figures 2.77 and 2.78.

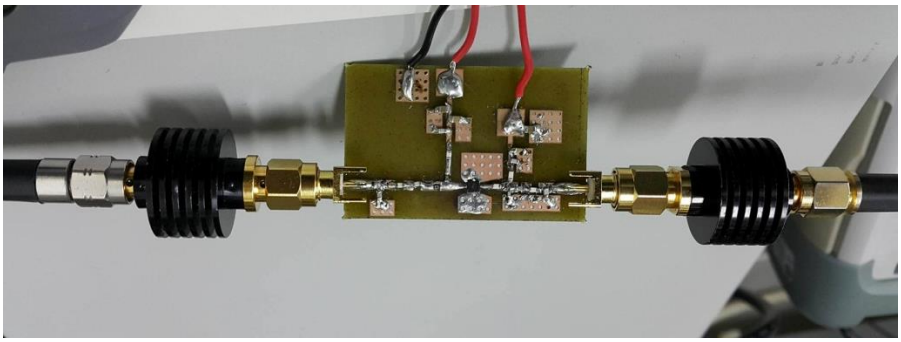


Figure 2. 76: Measurement setup for S-parameters measurement.

Figure 2. 77: Measurement S11 for Class-E circuit.

Figure 2. 78: Measurement S21 for Class-E circuit.

Measured and simulated S-parameters for Class-E has been presented in table 2.16.

Table 2.16: S11 and S21 result for simulation and measurement for Class-E.

Result	S11	S21
Simulation	-2.7	20.57
Measurement	-4.2	18.17

2.9.2 Inverse- Class-E design S-parameters measurement

S11 nad S21 parameters have been measured for Inverse-Class-E circuit in figures 2.79 and 2.80.

Figure 2. 79: Measurement S11 for Inverse-Class-E circuit.

Figure 2. 80: Measurement S21 for Inverse-Class-E circuit.

Measured and simulated S-parameters for Inverse-Class-E has been presented in table 2.17.

Table 2.17: S11 and S21 result for simulation and measurement for Inverse-Class-E.

Result	S11	S21
Simulation	-15.5	18.68
Measurement	-2.8	14.13

2.9.3 Mixed design S-parameters measurement

S11 nad S21 parameters have been measured for Mixed circuit in figures 2.81 and 2.82 for 47nH and figures 2.83 and 2.84 for 56nH.

Figure 2. 81: Measurement S11 for Mixed circuit- 47nH.

Figure 2. 82: Measurement S21 for Mixed circuit- 47nH.

Figure 2. 83: Measurement S11 for Mixed circuit- 56nH.

Figure 2. 84: Measurement S21 for Mixed circuit- 56nH.

Measured and simulated S-parameters for both 47nH and 56nH values are presented in table 2.18.

Table 2.18: S11 and S21 result for simulation and measurement for Mixed design.

Result	S11 (47nH)	S21 (47nH)	S11 (56nH)	S21 (56nH)
Simulation	-15.0	19.14	-11.27	20.71
Measurement	-11.54	16.93	-9.72	18.75

2.9.4 Output power measurement and other results for all circuits

In order to measure output power, input power has been given by mini-circuit signal generator and output power measured by R&S spectrum analysor. The measurement setup can be seen in figure 2.85, using signal generator, driver power amplifier, attenuators, and spectrum analysor, having DC supply, sweeping the input power from -10dBm up to +20dBm and up to 6dB of gain compression. By having the output power and DC values (current and voltage) other parameters such as DC power, gain, drain efficiency and power added efficiency could be calculated and results are present in figures 2.86-2.89.

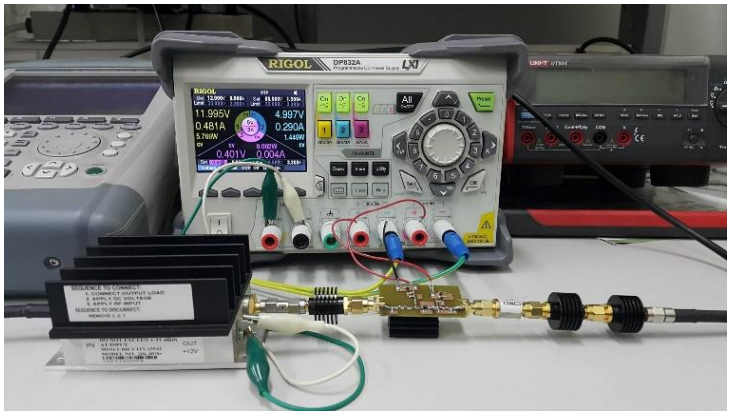


Figure 2. 85: Measurement setup to measure output power.

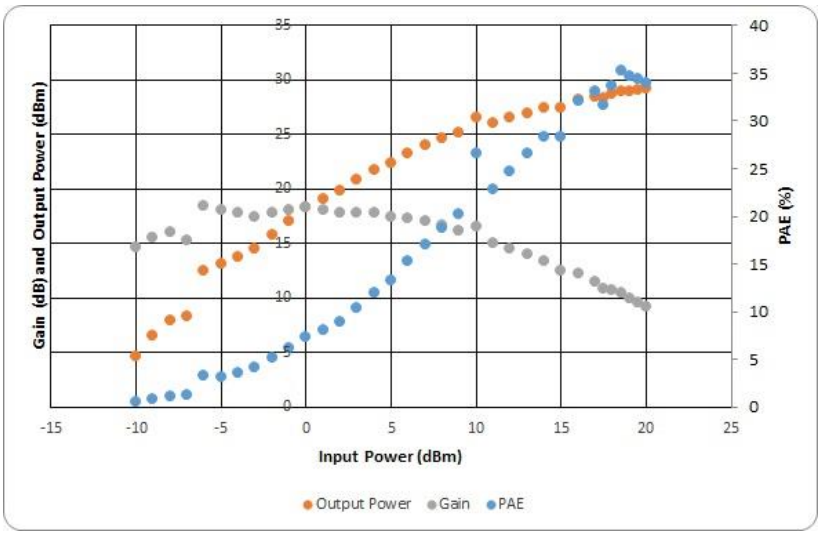


Figure 2. 86: Gain, output power and PAE results for Class-E design.

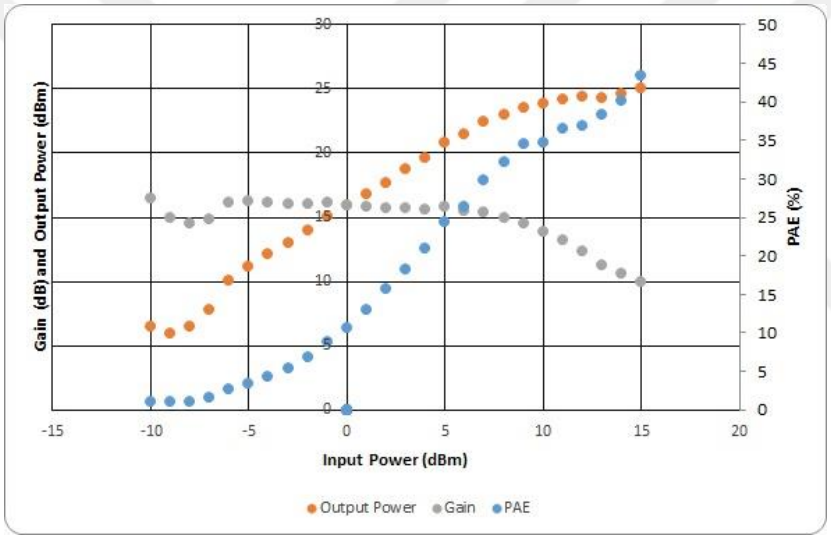


Figure 2. 87: Gain, output power and PAE results for Inverse-Class-E design.

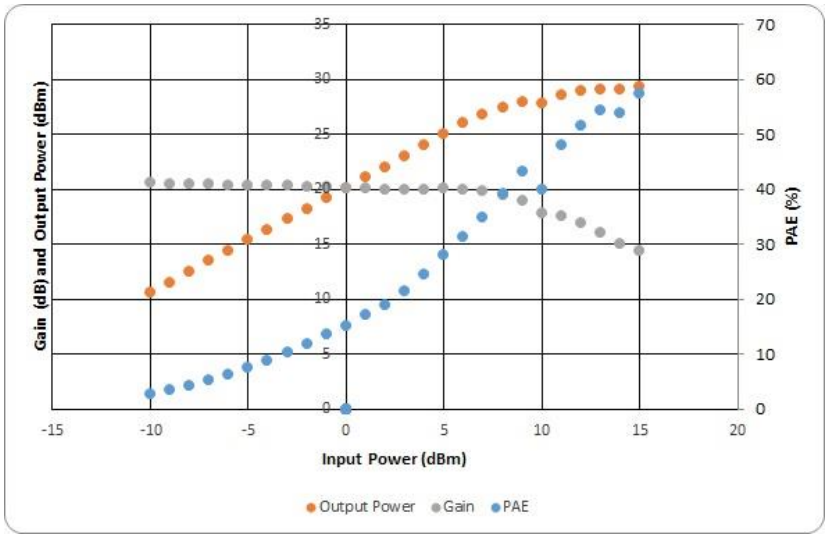


Figure 2. 88: Gain, output power and PAE results for Mixed design (47nH).

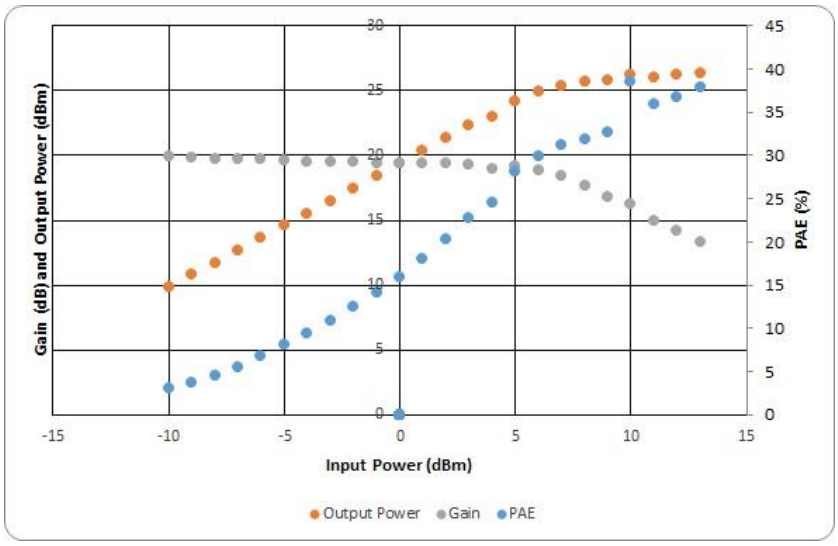


Figure 2. 89: Gain, output power and PAE results for Mixed design (56nH).

3. CONCLUSION

All results have been compiled in table 2.19 to make a comparison between simulated and measured results and present the success of this project.

Table 3.1: Design parameters for simulation and measurement results of all circuits.

	Output Power (dBm)	Gain (dB)	PAE (%)	S11	S22
Class-E					
Simulation	30.99	16.14	50.5	2.7-	20.57
Measurement	29	10.5	35.29	4.2-	18.17
Inverse-Class-E					
Simulation	24.49	15.04	37.4	15.5-	18.68
Measurement	29	10.5	40.19	2.8-	14.13
Mixed Design (47nH)					
Simulation	30.48	16.73	46.93	15.0-	19.14-
Measurement	29.4	14.4	57.29	11.54-	16.93
Mixed Design (56nH)					
Simulation	27.47	17.7	39.36	11.27-	20.71
Measurement	26.3	13.3	37.82	9.72-	18.75

In this thesis, three diferrent structurs of Class-E, Inverse-Class-E and a novel Mixed design has been simulated and fabricated.

These power amplifiers work with 5V DC supply which reduces the need for another extra DC-DC downconverter and makes it a great choice for small satellite applications. Simulation results are 50%, 43% and 37% for Class-E, mixed strucure and Inverse-Class-E designs and also results of hardware measurements have been presented. The trade-off between having higher output power and gain against PAE has been observed after measurements. In simulations, higher output power and gain but lower PAE was achieved while in measurements it was vice versa. It is imoprtant to mention that the mixed design was manufactured for two values of inductor and each were measured separate, once with 49nH and 56nH values. Hardware measurement PAE results are 35% for Class-E, 40% for Inverse-Class-E, 57% for Mixed design with 47nH and 37% for Mixed design with 56nH. Finally, satisfactory results have been obtained for each design.

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APPENDICES

APPENDIX A: 12 Different designs for Class-E, Inverse-Class-E or mixed

APPENDIX B: Bill of Material (BoM)

APPENDIX A

In this appendix, design structures have been presented, including schematics and results shown for this project. The software used to perform simulations is “Advanced Design System- ADS 2015.01” from Agilent.

In a class-E amplifier it is interesting to see the amplifier switching performance, and the performed simulations shall prove this concept in the output and load of the transistr.

The figures below show the whole circuit with components and designed in a way to perform the switching action. Also, other simulations to show the efficiency, PAE, gain, harmonics and other specifications have been performed. The results of 12 different structures, results and comments are presented in table A.13 to make a comparison and final successful structure has also been presented in following figures.

Here are also the formulae used for the simulations and obtaining desirable parameters of the design:

Pdel_W=0.5*real(Vload[1]*conj(Iload.i[1]))

Pdc=real(Vs_high[0]*Is_high.i[0]+Vs_low[0]*Is_low.i[0])

P_In_Watts=0.5*real(Vinput[1]*conj(I_input.i[1]))

PAE=max2(100*(Pdel_W-P_In_Watts)/Pdc,0)

Gain_Transducer=Pdel_dBm-RFpower

Pin_dBm=10*log(1000*P_In_Watt)

Design 1: No Impedance Matching Network

In this design, no impedance matching network, neither in input nor in output has been used to observe the contribution of biasing in the whole design and results. In the circuit, only ampere-meters, volt-meters and ports are visible as can be seen in figure A.1. The results are also presented in table A.1. As it can be comprehended from the results, Transducer Power Gain (TPG), PAE and output power is very low, harmonic suppression has not been accomplished, thus the design doesn't satisfy the design goals.

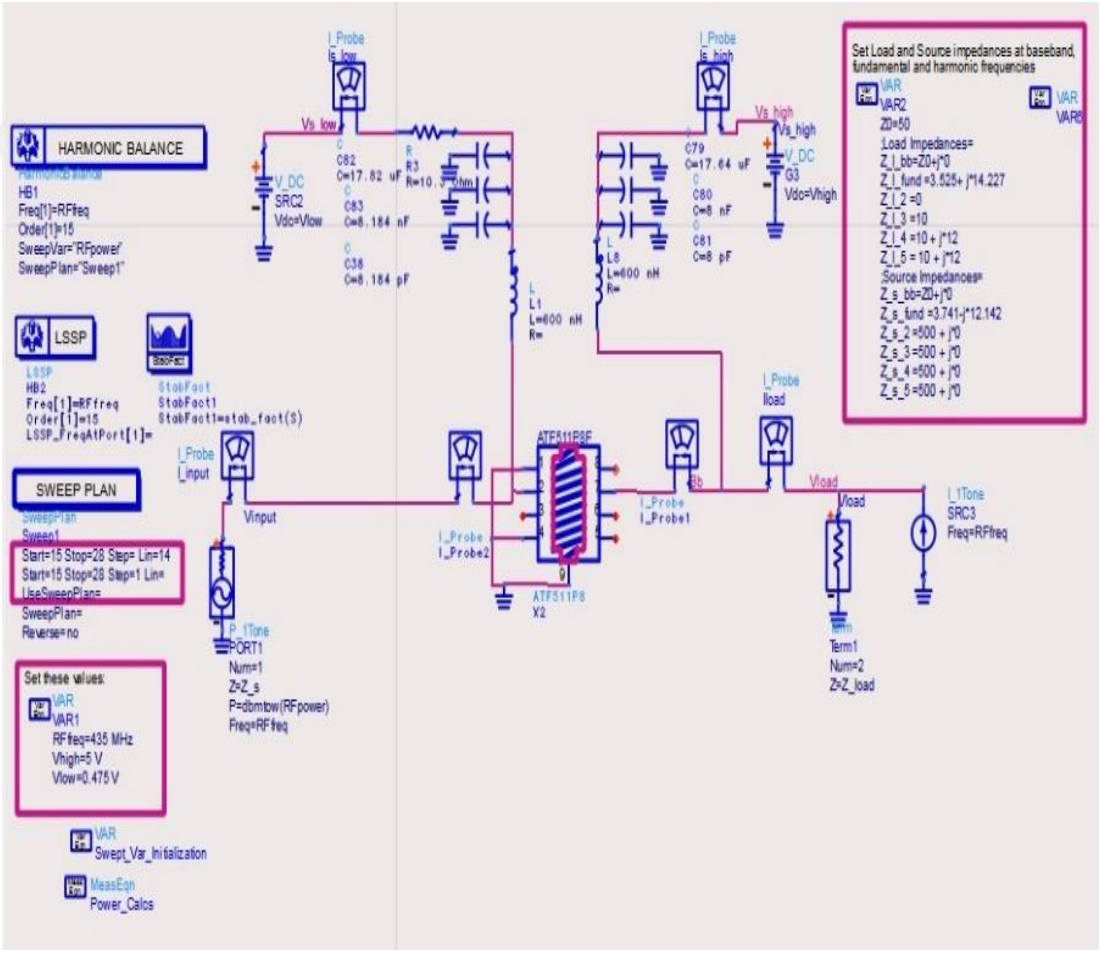

Figure A.1: Simple circuit without matching network and only with biasing.

Table A.1: Results of **s**imple circuit without matching network and only with biasing.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre -ssion (dB)	PAE (%)	DC Power Consumpt -ion (W)	High Supply Current	Thermal Dissipati -on (W)
23.98	5.38	2.55	12.6	1.97	0.39	1.34

Design 2: Simple 2-element Input and Output Matching Network Design

In this design, simple 2-element input and output matching network has been applied, figure A.2. As it can be seen in figure A.4, switching act has not been shaped correctly to satisfy the requirements for class-E design. Values of TGP, PAE and output power is low, although the harmonic suppression has been accomplished due to the semi-low-pass filter structure of the input and output. The results are also presented in table A.2.

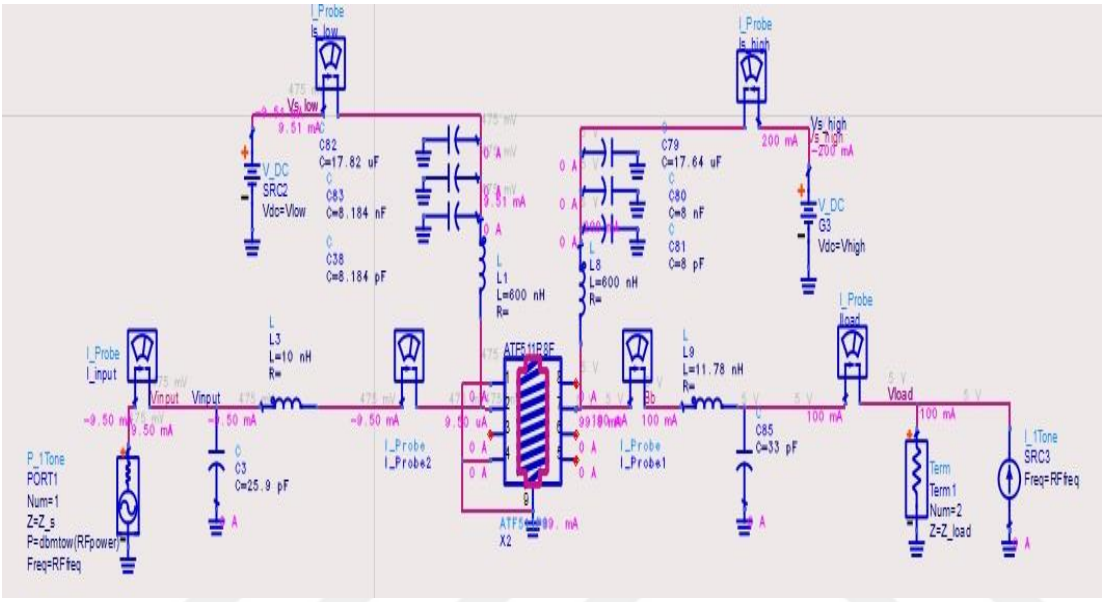

Figure A.2: simple 2-element input and output matching network.

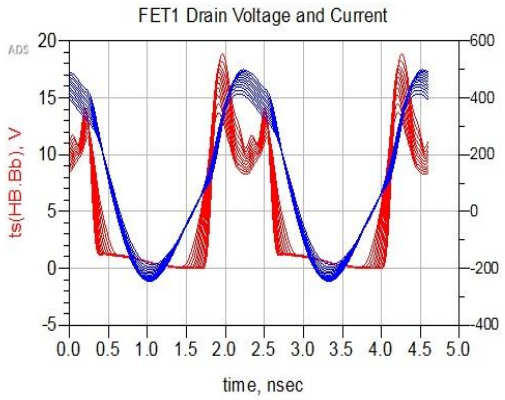

Figure A.3: Simple 2-element circuit's drain voltage and current.

Table A.2: Results of simple 2-element input and output matching network.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumption (W)	High Supply Current	Thermal Dissipati-on (W)
31.12	6.12	8.33	40.9	3.05	0.61	1.54

Design 3: L-Type Input matching, Class-E Output Matching Design

In figure A.5, L-type low-pass input matching network, and simple class-E structure at output matching network can be seen. DC annotation shows the accordance of this design with class-E assumptions. Figure A.5. shows that switching effect of Class-E is happening as predicted, harmonic suppression goal is satisfied, PAE, TGP and output power is desirable but due to high gain compression, TPG value is very low. Also, output return loss is not satisfactory. The results are also presented in table A.3.

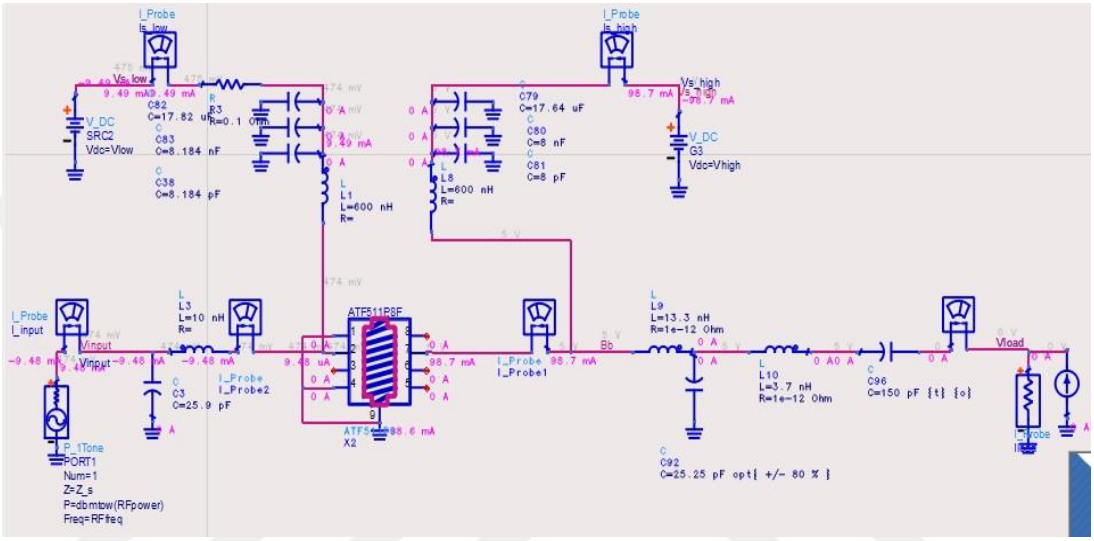

Figure A.4: L-Type input matching, Class-E output matching design.

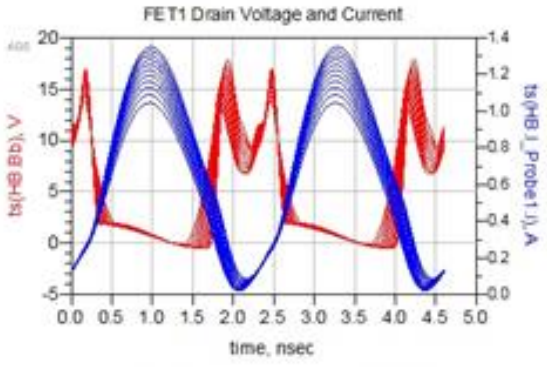

Figure A.5: L-Type input matching, Class-E output matching design's drain voltage and current.

Table A.3. Results of L-Type input matching, Class-E output matching design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumpt-ion (W)	High Supply Current	Thermal Dissipation (W)
33.27	8.27	8.2	56.5	3.66	0.73	1.59

Design 4: T-Type Low-pass filter input matching, Class-E output matching with different biasing application

T-type low-pass filter has been used for the input matching network, and in the output, there is Class-E structure but the difference is in the plan of biasing application (figure A.6). All parameters are good for this design, the only problem is the phase shifting in the load current and voltage which is not desirable. DC consumption is high. Figure A.7 shows the non-ideal switching effect and table A.4 presents the results.

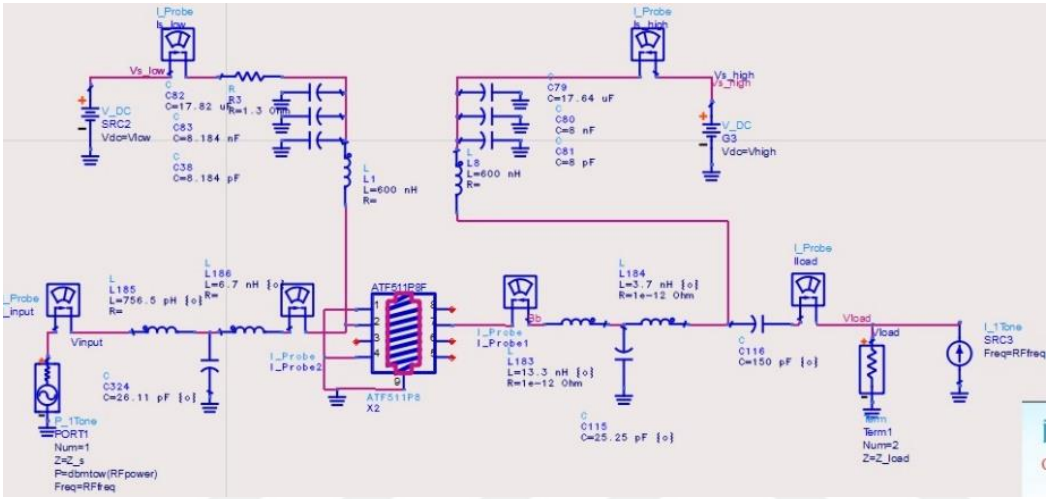

Figure A.6: T-Type Low-pass filter input matching, Class-E output matching with different biasing application.

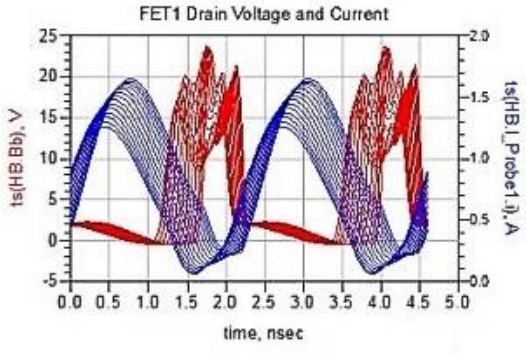

Figure A.7: Drain-source current and voltage to show the switching effect.

Table A.4: Results of T-Type Low-pass filter input matching, Class-E output matching design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumpti-on (W)	High Supply Current	Thermal Dissipation (W)
32.97	17.22	0.59	56.5	3.46	0.69	1.5

Design 5: Class-E Structure in both Input and Output Matching Network

As it can be seen in figure A.8, class-E structure has been used both in input and output matching network to see how it will affect the overall results. Figure A.9 shows the switching effect. The positive point about this design is lower DC consumption but in the expense of lower PAE, TPG and output power. There is also phase shifting in both input and output voltages, and load voltage and current, but it is obvious that switching is functional very well. Also a second shunt capacitance has been used in output which results in good harmonic suppression. The results are also presented in table A.5.

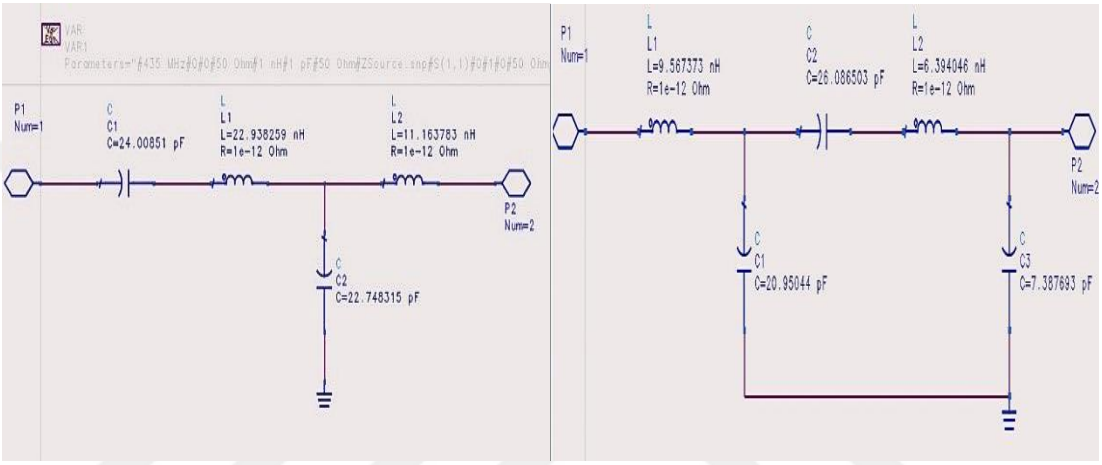

Figure A.8: Class-E Input (left) and output (right) matching networks (separately).

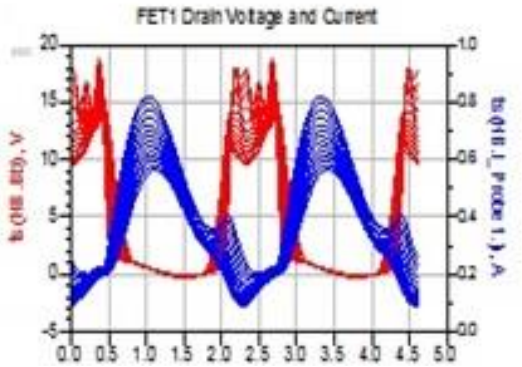

Figure A.9: Drain-source current and voltage to show the switching effect.

Table A.5: Results of Class-E input and output matching design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumpt-ion (W)	High Supply Current	Thermal Dissipation (W)
28.48	11.88	1.33	42.9	1.62	0.32	0.92

Design 6: Class-E input matching, Class-E plus Chebyshev Band-pass filter in output matching

For this design, class-E structure for the input matching network has been used, and in the output, Class-E structure plus Chebyshev bandpass filter has been applied for further harmonic suppression and desirable switching function as shown in figure A.10. PAE, TPG, output power, harmonic suppression results are acceptable. Phase shift between the input and output voltage and between the load current and voltage is visible which is not desirable. Input and output matching impedances need modification. Switching function can be observed in figure A.11 from the Drain-Source current and voltage. From this design and from table A.6, it can be realized that using Chebyshev band-pass structure at output matching network can have positive effects on overall function of the system.

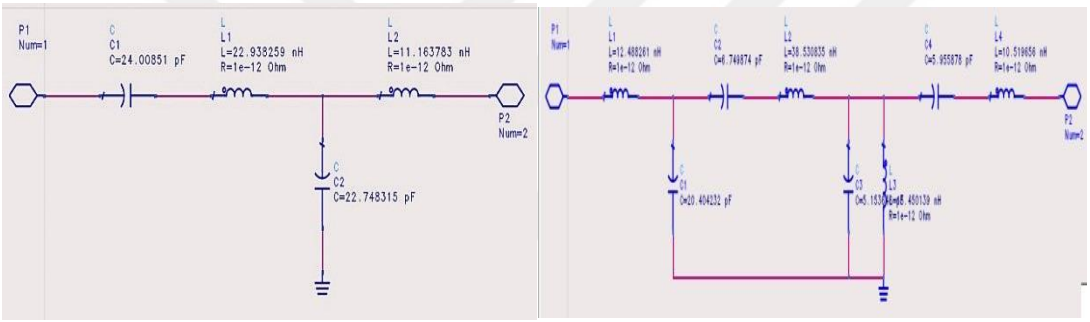

Figure A.10: Class-E input matching (left) and Class-E plus Chebyshev bandpass filter output matching (right) network.

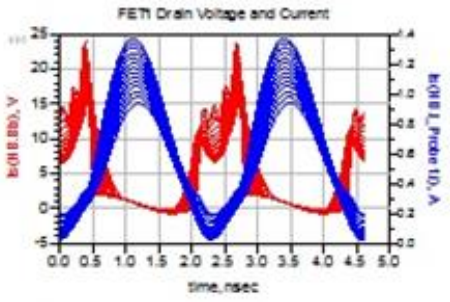

Figure A.11: Drain-source current and voltage to show the switching effect.

Table A.6: Results of Class-E input matching and Class-E plus Chebyshev bandpass filter output matching network design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumption (W)	High Supply Current	Thermal Dissipation (W)
31.48	12.58	2.83	50.4	2.75	0.55	1.36

Design 7: T-type Input Matching, Class-E plus Chebyshev Band-pass Filter at Output Matching

Here, the number of elements have been reduced by having a T-type input matching network, and output stays the same, including class-E structure with a band-pass Chebyshev filter (figure A.12) for switching function (figure A.13) and harmonic suppression. Higher PAE, TGP, output power, less DC consumption, better harmonic suppression, better matching and no phase shifting in the input and output voltage proves the superiority of this design over the previous one and presented in Table A.7.

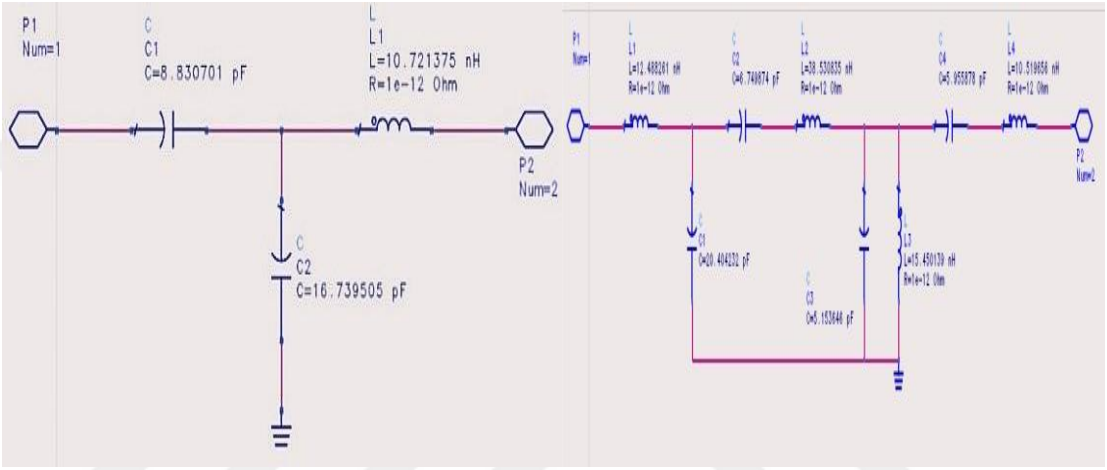

Figure A.12: T-type input matching (right) and class-E feat. Chebyshev bandpass filter for output matching (left) network.

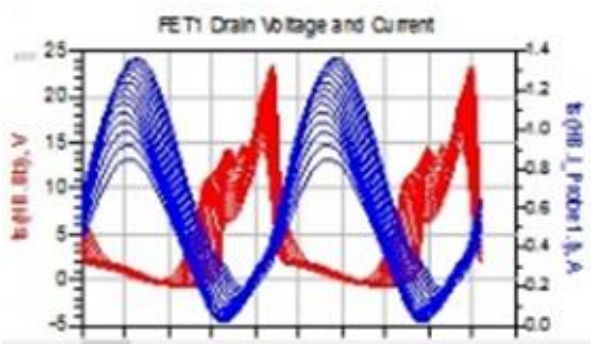

Figure A.13: Drain-source current and voltage to show the switching effect.

Table A.7: Results of T-type input matching and class-E feat. Chebyshev bandpass filter for output matching network design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumpti-on (W)	High Supply Current	Thermal Dissipation (W)
31.48	12.73	1.89	50.4	2.75	0.55	1.36

Design 8: Class-E Structure plus Chebyshev Band-pass Filter both in Input and Output Matching, Different place of Biasing Application

This time, the effect of using both class-E plus Chebyshev Band-pass filter in input and output matching network can be observed in figure A.14. higher PAE has been achieved, but there is a disturbing gain compression that results in a low TPG (table A.8). Switching function works well (figure A.15) but there is phase shift in input and output voltage.

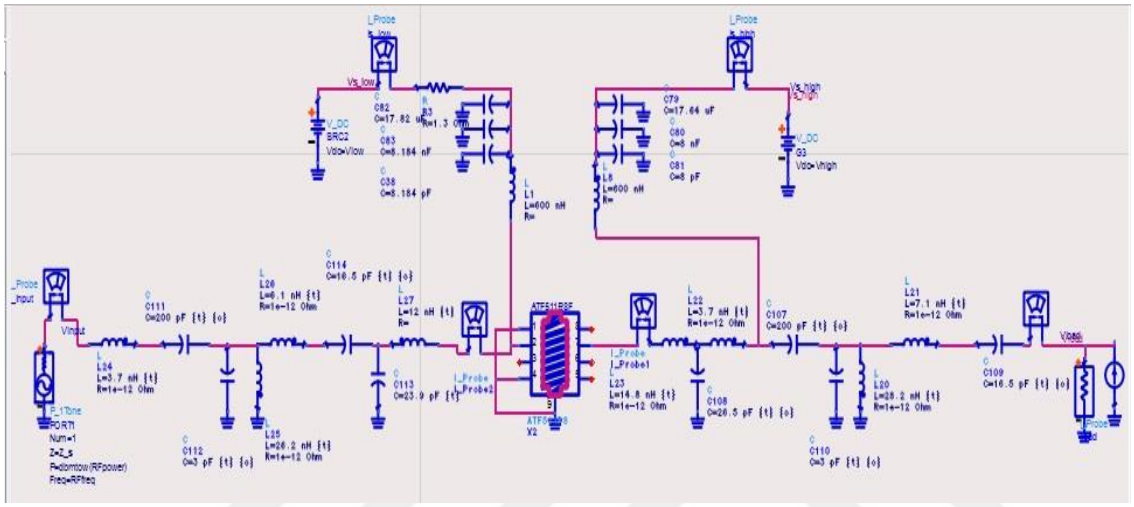

Figure A.14: Class-E Structure plus Chebyshev Band-pass Filter both in Input and Output Matching with different biasing application.

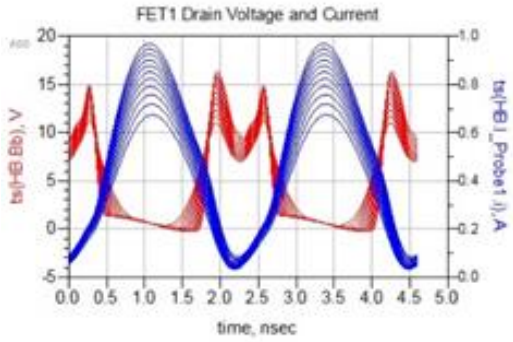

Figure A.15: Drain-source current and voltage to show the switching effect.

Table A.8: Results of Class-E Structure plus Chebyshev Band-pass Filter both in Input and Output Matching with different biasing application design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumpti-on (W)	High Supply Curren t	Thermal Dissipation (W)
31.71	6.71	7.23	54.2	2.68	0.53	1.23

Design 9: Class-E Structure plus Chebyshev Band-pass Filter both in Input and Output Matching

This design is the same as the above design with different biasing application place (figure A.16). It didn't much have significant effect on harmonic suppression, though the aim is reached. Higher TPG, output power has been achieved with the cost of higher DC consumption. Overall function is good, input matching network needs modification, output matching works well, and there is a phase shift between the input and output voltage which need modification. Figure A.17 shows the switching effect and table A.9 presents the results.

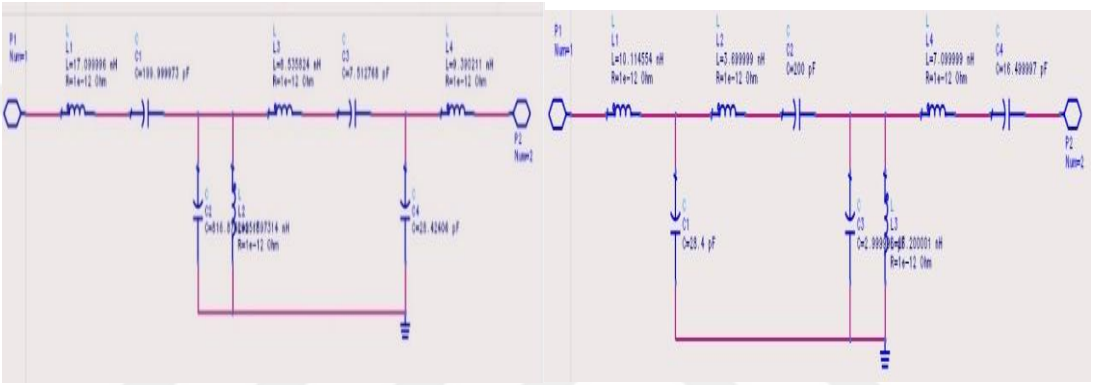

Figure A.16: Class-E Structure plus Chebyshev Band-pass Filter both in Input and Output Matching

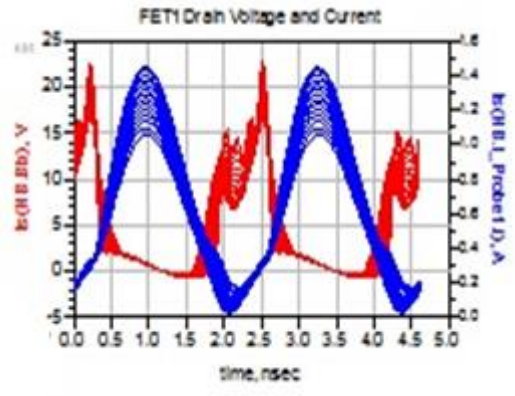

Figure A.17: Drain-source current and voltage to show the switching effect.

Table A.9: Results of Class-E Structure plus Chebyshev Band-pass Filter both in Input and Output Matching design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumpt-ion (W)	High Supply Current	Thermal Dissipation (W)
31.98	13.93	2.27	52.4	2.97	0.59	1.41

Design 10: Multi-harmonic output matching network

For this design, Low pass filter has been used in input matching network (figure A.18), with multi-harmonic structure in output matching network (figure A.19). All results are satisfactory (table A.10) but the design is complicated and practically not feasible to be realized. So in next design, simplification will be tried.

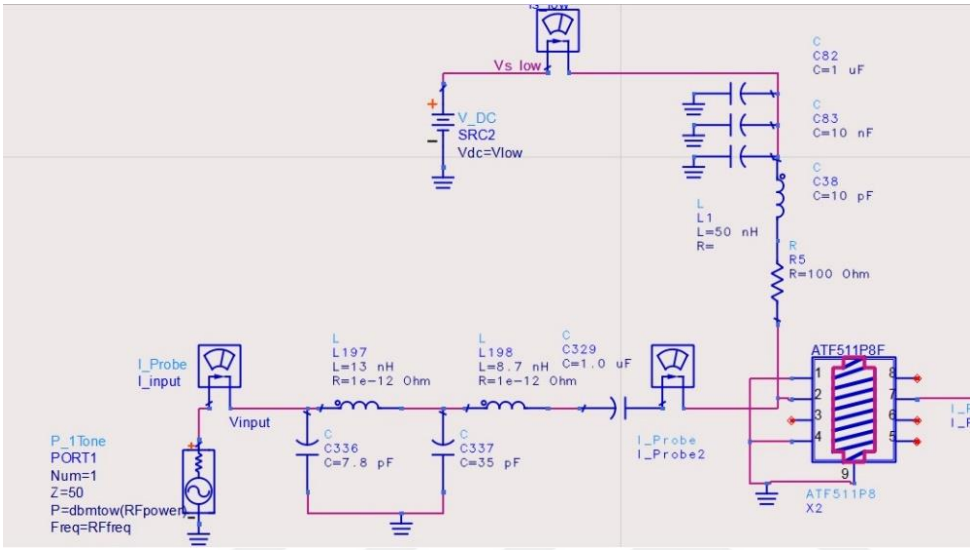

Figure A.18: Input biasing and matching network.

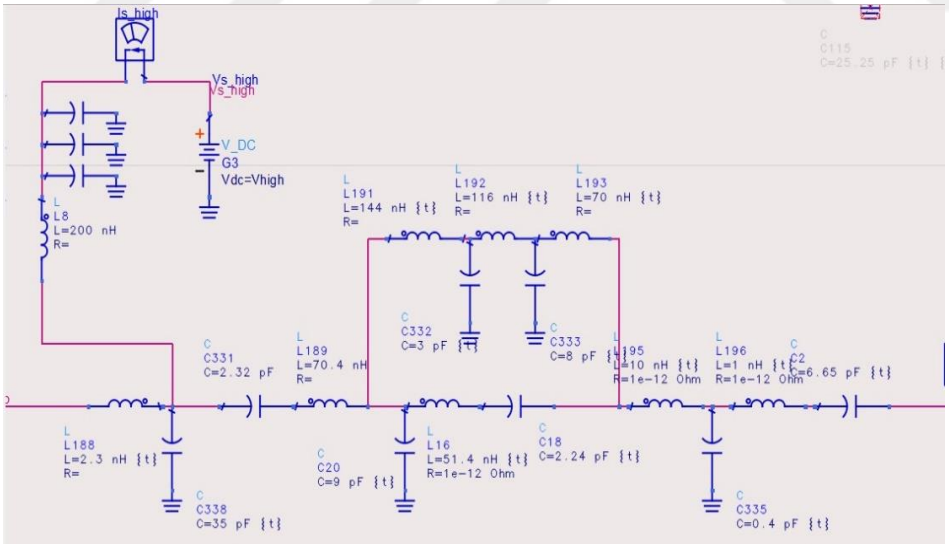

Figure A.19: Output biasing and matching network.

Table A.10: Results of Multi-harmonic output matching network design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumpti-on (W)	High Supply Current	Thermal Dissipation (W)
33.48	19.98	2.93	55.7	3.96	0.79	1.75

Design 11: Similar input design, with adding a dipole network to multi-harmonic output matching network

Similar as previous one, low pass filter has been used in input matching network and in output matching network, before the multi-harmonic structure, a dipole network has been applied for further impedance matching and improving output parameters (figure A.20). This design shows better results (table A.11) than the previous one and good switching capability (figure A.21), but complexity has been increased and still the production of this design is not feasible.

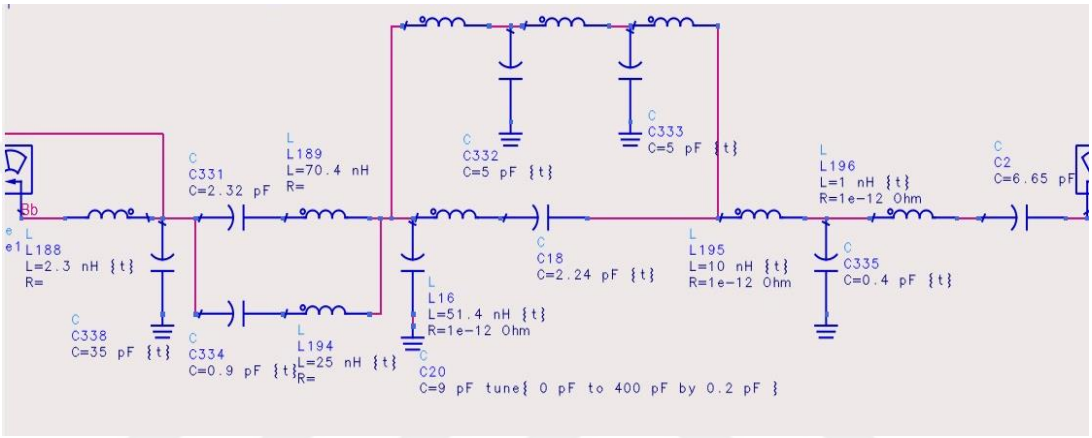

Figure A.20: Output matching network including multi-harmonic structure and dipole network.

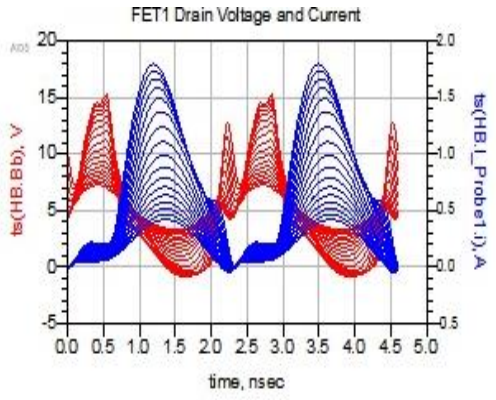

Figure A.21: Drain-source current and voltage to show the switching effect.

Table A.11: Results of Multi-harmonic output matching network including multi-harmonic structure and dipole network design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consum-ption (W)	High Supply Current	Thermal Dissipation (W)
33.48	19.03	2.79	58.2	3.78	0.75	1.58

Design 12: Mixed-Class-E and Inverse-Class-E output matching network and similar input matching network

Finally, new mixed structure has been proposed in this design (figure A.22) to offer a new design structure for switching power amplifiers (figure A.23). All design results are satisfactory (table A.12) and also this design is feasible for production.

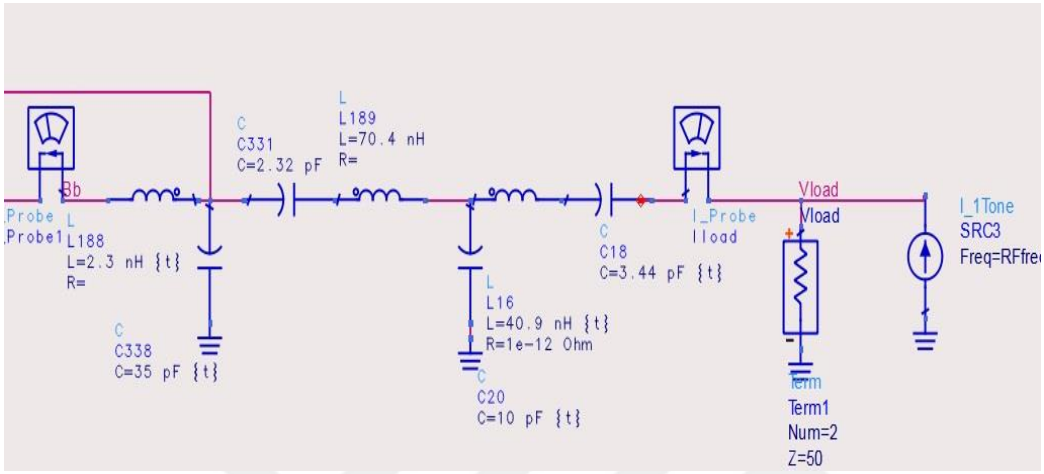

Figure A.22: Mixed Class-E and Inverse-Class-E structure.

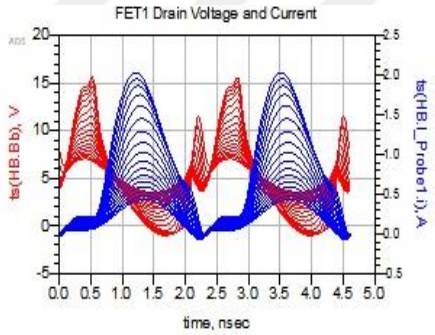

Figure A.23: Drain-source current and voltage to show the switching effect.

Table A.12: Results of Mixed Class-E and Inverse-Class-E structure design.

Fundamental Output Power (dBm)	Transducer Power Gain	Gain Compre-ssion (dB)	PAE (%)	DC Power Consumpti-on (W)	High Supply Current	Thermal Dissipation (W)
33.97	19.12	2.17	57.4	4.29	0.86	1.83

All the results of the 12 above designs have been presented in table A-13. Finally, the last design has been presented in details in the following section which proves simplicity has positive effect on the function of this design and proposes a new structure for switching mode power amplifiers for the first time.

Table A.13: Results of different designs for comparison

utput power (dBm)	Gain	Gain Compression (dB)	PAE (%)	DC power consumption (W)	Comment about this design	Structure type
23.98	5.38	2.55	12.7	1.97	-	Without matching- only biasing
31.12	6.12	8.33	41	4.41	Too much gain compression- non switching- two element	Two element input and output
32.97	17.2	0.589	56.5	3.46	Not good input matching- high DC consumption	T input- Class-E output
28.48	11.9	1.33	42.9	1.62	Bad stability- bad output return loss	almost simple input and output network
33.27	8.27	820	56.5	3.66	High gain compression- low return loss	2 element input matching- class E output
31.48	12.6	2.83	50.4	2.75	Bad input impedance matching- low output return loss- high dc consumption	Simple input- Chebyshev at output network
31.48	12.7	1.89	50.4	2.75	Complicated output network	T input, Chebyshev and class-E output network
31.71	6.71	7.23	56.2	2.68	Too much gain compression- low input and output return loss	Using Chebyshev bandpass filter in both input and output- different biasing place in output
31.98	13.9	2.27	52.4	2.97	Not good matching- low output return loss- unstable	similar with Chebyshev filter in input and output network
33.48	19.9	2.93	55.6	3.96	Complex structure- not physically applicable and implementable	Low pass filter input- multiharmonic output matching
33.48	19.0	0.79	58.2	3.78	Complex structure- not implementable	Lowpass filter input- dipole network and multiharmonic output matching
33.97	1912	2.17	57.4	4.29	Simple structure- implementable	Lowpass input, mix of Class-E and Inverse-Class-E output network

APPENDIX B

Table B.1: Bill of Material (BoM)

Element	Value	Tolerance	Packaging	Manufacturer	Amount
ATF-511P8	-	-	LPCC	Avago	3
GRM21A5C2D270JW01	27PF	5%	0805	Murata	1
LQW18AN18NG80	18NH	2%	0603	Murata	1
GRM1885C1H390JA01	39PF	5%	0603	Murata	2
GJM0335C1E220GB01	22PF	2%	0201	Murata	2
LQW18AN56NG80	56NH	2%	0603	Murata	2
LQW03AW3N3C00	3.3NH	0.2NH	0201	Murata	1
GJM0335C1E9R1WB01	9.1PF	0.05PF	0201	Murata	1
LQW18ANR12G80	120nH	2%	0603	Murata	3
GJM0335C1E2R4WB01	2.4PF	0.05PF	0201	Murata	2
LQW18AN51NG80	51NH	2%	0603	Murata	2
GJM0335C1E120GB01	12PF	2%	0201	Murata	1
GRM1885C1H180JA01	18PF	5%	0603	Murata	1
LQW18AN8N2G80	8.2NH	2%	0603	Murata	1
GRM1885C1H270JA01	27PF	5%	0603	Murata	1
GRM1885C1H470JA01	47PF	5%	0603	Murata	1
GJM0335C1E300GB01	30PF	2%	0201	Murata	1
LQW03AW4N7J00	4.7NH	5%	0201	Murata	1
LQW18AN39NG80	39NH	2%	0603	Murata	1
LQP03HQ9N1H02	9.1NH	3%	0201	Murata	1
LQW18AN12NG80	12NH	2%	0603	Murata	1
LQW18AN8N2G8Z	8.2NH	2%	0603	Murata	1
GJM0335C1E7R5WB01	7.5PF	0.05PF	0201	Murata	1
GRM1885C1H820JA01	82PF	5%	0603	Murata	1
GJM0336C1E150GB01	15PF	2%	0201	Murata	1
GRM1555C2A560GA01	56PF	2%	0402	Murata	1
GRM1885C1H101JA01D	100PF	5%	0603	Murata	6
C1608X5R1A106K080AC	10UF	10%	0603	TDK	6
	25 Ω				1
	49.9 Ω				2
	100 Ω				3
	100nF				6

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