ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

A 0.18 μm CMOS X-BAND LOW NOISE AMPLIFIER FOR SPACE APPLICATIONS

M.Sc. THESIS

Nergiz ŞAHİN

Department of Electronics and Communications Engineering

Electronics Engineering Programme

Thesis Advisor: Asist. Prof. Dr. Mustafa Berke YELTEN

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ISTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

UZAY UYGULAMALARI İÇİN 0.18 µm CMOS X-BANT DÜŞÜK GÜRÜLTÜLÜ KUVVETLENDİRİCİ

YÜKSEK LİSANS TEZİ

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HAZİRAN 2017

Nergiz ŞAHİN, a M.Sc. student of ITU Graduate School of Science Engineering and Technology student ID 504141218, successfully defended the thesis entitled "A 0.18 μm CMOS X-BAND LOW NOISE AMPLIFIER FOR SPACE APPLICATIONS", which she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To my father,

FOREWORD

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ABBREVIATIONS

CMOS	**:** Complementary Metal Oxide Semiconductor
EM	**:** Electromagnetic
ELT	**:** Enclosed Layout Transistor
GaAs	**:** Gallium Arsenide
HCE	**:** Hot Carrier Effect
HEMT	**:** High Electron Mobility Transistor
HFET	**:** Heterostructure Field Effect Transistor
IIP3	**:** Input Third Order Intercept Point
LNA	**:** Low Noise Amplifier
MOS	**:** Metal Oxide Semiconductor
MMIC	**:** Monolithic Microwave Integrated Circuit
NBTI	**:** Negative Bias Temperature Instability
NF	**:** Noise Figure
NFmin	**:** Minimum Noise Figure
NMOS	**:** N-channel Metal Oxide Semiconductor
PMOS	**:** P-channel Metal Oxide Semiconductor
PBTI	**:** Positive Bias Temperature Instability
RF	**:** Radio Frequency
RadHard	**:** Radiation Hardened
SEE	**:** Single Event Effect
SNR	**:** Signal to Noise Ratio
TID	**:** Total Ionization Dose
VCO	**:** Voltage Controlled Oscillator

SYMBOLS

C	**:** Capacitance
K	**:** Kelvin
L	**:** Inductance
P	**:** Power
R	**:** Resistance
Rad	**:** Unit of Radiation Dose
W	**:** Watt
Ω	**:** Ohm
β	**:** Current Gain
S_{21}	**:** Transmission Coefficient
S_{11}	**:** Input Reflection Coefficient
S_{22}	**:** Output Reflection Coefficient
S_{12}	**:** Reverse Transmission Coefficient

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A 0.18 μm CMOS X-BAND LOW NOISE AMPLIFIER FOR SPACE APPLICATIONS

SUMMARY

Low noise amplifiers are the first and one of the most important stages of receiver systems. They are RF circuits which are widely used in many applications such as wireless systems, radio astronomy, space communications etc. Their main purpose is to amplify the weak signal at the input of the receiver by adding as little noise as possible. Since, LNAs constitute the first stage of receivers, they dominate the overall noise performance of the system.

Low noise amplifier designs are mostly done using SiGe and HEMT technologies. However, low cost and better process integration of CMOS technology along with its rapidly increasing performance metrics has made it a significant contender.

Mankind is exploring the space by satellites, telescopes and space crafts. These expeditions need strong support of electronics technology. Space electronics has evolved considerably over the years, however designs accomplished mostly depend on discrete elements and expensive technologies such as High Electronic Mobility Transistor (HEMT). As the space technology should get more important and prevalent in the foreseeable future, related applications require cheap, wide-spread and easily (re)producible technologies.

Temperature in the outer world can get as low as 77 K and objects in space are under high radiation doses emitted by the stars and planets. Low temperature and high radiation affect the circuit performance drastically. Thus, developing designs for these extreme environments with cheap technologies is an important research problem.

The main goal of this thesis is to design a 7 GHz X-band low noise amplifier for space applications using 0.18 μm UMC CMOS Mixed-Mode/RF technology. This LNA is designed for being tested at temperatures below 100 K (also called cryogenic temperatures) and radiation. Designed LNA is still at the production stage and has not been measured yet. All the results in this thesis are post-layout simulation results from Cadence and ADS tools.

The classical cascode topology with inductive degeneration is used in this design. An additional bias inductance is employed to help in input impedance matching. Bias of the LNA is designated to be directly applied to the pads so that they can be changed during measurements to comply with cryogenic temperatures and radiation. Designed CMOS LNA achieves a voltage gain higher than 15 dB, 2.6 dB noise figure, –2.24 dBm IIP3 while consuming 25 mW of power.

UZAY UYGULAMALARI İÇİN 0.18 µm CMOS X-BANT DÜŞÜK GÜRÜLTÜLÜ KUVVETLENDİRİCİ

ÖZET

Düşük gürültülü kuvvetlendiriciler alıcı sistemlerinin ilk ve en önemli bloklarından biridir. Kablosuz sistemler, haberleşme, radio astronomi ve uzay haberleşmesi gibi bir çok uygulama için tasarlanan, geniş kullanım alanına sahip RF devrelerdir. En temel amaçları alıcı girişindeki zayıf işareti olabildiğince az gürültü ekleyerek kuvvetlendirmektir. Düşük gürültülü kuvvetlendiriciler alıcı sistemlerinin ilk katı oldukları için, bütün sistemin gürültü performansını belirlemektedir.

Düşük gürültülü kuvvetlendiricilerin tasarımı çoğunlukla SiGe ve yüksek electron mobiliteli transistor (HEMT) teknolojileri ile yapılmaktadır. Ancak bu teknolojilerin pahalılığı, CMOS teknolojisinin daha iyi üretim tümleştirmesi ve CMOS teknolojisinin hızla küçülmesiyle performansının iyileşmesi tasarımları CMOS teknolojisine doğru yöneltmiştir.

İnsanoğlu uydular, teleskoplar ve uzay araçları yardımıyla uzayı keşfetmektedir. Bu keşifler elektronik teknolojisinin güçlü desteğine ihtiyaç duymaktadır. Uzay elektroniği büyük bir geçmişe sahip olmasına rağmen, genel olarak kullanılan elektronik tasarımlar ayrık elemanlı devreler veya HEMT gibi pahalı teknolojiler ile gerçekleştirilmektedir. Uzay konusunun önemi gittikçe artmakta ve hayatımızda yaygınlaşmaktadır. Dolayısıyla uzay teknolojisinde kullanılabilecek ucuz, yaygın ve kolay üretilebilir teknolojilere ihtiyaç duyulmaktadır.

Dünyanın dışı 77 K seviyelerinde sıcaklıklara düşmekte ve uzaydaki cihazlar yıldız ve gezegenlerden gelen ışınıma (radyasyon) maruz kalmaktadır. Dahası bu düşük sıcaklık ve yüksek ışınım devre performansını kuvvetli bir şekilde etkilemektedir. Bu nedenle olağanüstü ortam koşullarında çalışabilen ucuz teknolojilerin varlığı önemli bir araştırma konusudur.

Bu tezin temel amacı 0.18 µm UMC CMOS Mixed-Mode/RF teknolojisini kullanarak, uzay uygulamaları için 7 GHz X bandında çalışacak bir düşük gürültülü kuvvetlendiricinin tasarlanmasıdır. Bu düşük gürültülü kuvvetlendirici kriyojenik sıcaklıklarda ve ışınım altında test edilmek için tasarlanmıştır ve halen üretim aşamasındadır. Tez kapsamında verilen tüm sonuçlar Cadence ve ADS programlarının serim sonrası benzetim sonuçlarına dayanmaktadır.

Tez kapsamında öncelikle tasarım elemanlarının düşük sıcaklıkta ve ışınım altında performansı literatür araştırması yapılarak incelenmiştir. Bunun için yüksek frekanslı devre tasarımında geniş kullanım alanları bulunan heterojonksiyon bipolar transistör (heterojunction bipolar transistor, HBT), yüksek electron mobiliteli transistör (high electron mobility transistor, HEMT) ve metal oksit yarıiletken (metal oxide semiconductor, MOS) transistörlerin düşük sıcaklıklarda ve yüksek ışınım altındaki davranışları incelenmiştir. Daha sonra literatürde bu elemanlar kullanılarak tasarlanan düşük gürültülü kuvvetlendiricilerin yine aynı koşullarda (düşük sıcaklık ve yüksek ışınım) performans farklılıklarına bakılmıştır. Tez kapsamında MOS teknolojisi

kullanılmasına karar verilmiş, ayrıca tezin dahil olduğu proje kapsamında yapılan bir üretim sonucunda oda sıcaklığında ve kriyojenik sıcaklıklarda n-kanallı metal oksit yarıiletken (NMOS) transistor ölçümü yapılmıştır.

Literatür araştırması MOS transistörlerin eşik geriliminin (V_{TH}) sıcaklık düştükçe yükseldiğini ancak taşıyıcıların hareket yeteneğinin arttığını, sonuç olarak savak akımının arttığını göstermektedir. Ayrıca tez kapsamında yapılan ölçümlerle NMOS transistor eşik gerilimi ve savak akımı artışı literatür araştırmasını doğrulayacak şekilde elde edilmiştir. Tasarlanan düşük gürültülü kuvvetlendiricilerin ise besleme gerilim ve akımlarının düşük sıcaklıklara göre ayarlanması sonucunda gerilim kazancının (S_{21}) arttığını, gürültü faktörünün (NF) ise düştüğü bir çok makale ile gösterilmiştir. Ancak düşük gürültülü kuvvetlendirici tasarımları genellikle HBT ve HEMT elemanlarla yapılmış olup, henüz literatürde MOS elemanlarla tasarlanmış bir düşük gürültülü kuvvetlendiricinin gürültü faktörü ölçümü yapılmadığı görülmüştür.

Işınım testleri için toplam iyonlaştırma dozu (total ionization dose, TID), tekil olay etkisi (single event effect, SEE) gibi farklı testler yapılmaktadır. Düşük gürültülü kuvvetlendiriciler için asıl etkili olan ve uzay şartlarında dayanıklı olunması gerekli olan ışınım çeşidi toplam iyonlaştırma dozudur. Işınım altında ölçümler tez kapsamında yapılmamış olup, toplam iyonlaştırma dozu altında eleman ve düşük gürültülü kuvvetlendirici performansı ile alakalı literatür araştırması yapılmıştır. Çeşitli elemanların ve düşük gürültülü kuvvetlendiricilerin çeşitli ışınım düzeylerine dayanıklılıkları gözlenmiştir. Sonuç olarak tez kapsamında tasarlanan 7 GHz bütünleyici metal oksit yarıiletken (complementary metal oxide semiconductor, CMOS) düşük gürültülü kuvvetlendiricinin bir düzeye kadar ışınıma dayanıklı olması beklenmektedir. Düşük gürültülü kuvvetlendiricinin ışınıma dayanabildiği doz düzeyinin yükseltilmesi ise gelecek çalışmalar için hedeflenmektedir.

Anlatılan uygulama için endüktif dejenerasyonlu klasik kaskod topolojisi kullanılmıştır. Kararlılık ve salınım (osilasyon) sorunları ile karşılaşmamak için tek katlı yapı ile teknik isterlerin sağlanması amaçlanmıştır. Çıkıştan girişe yansımaların en düşük düzeye indirilmesi için kaskod topoloji en yaygın kullanılan düşük gürültülü kuvvetlendirici yapısıdır. Endüktif dejenerasyon ise hem gürültü hem giriş empedansı eşleştirmesinin aynı anda yapılması için en uygun topolojidir. Emetördeki endüktör ile giriş empedansı ayarlanırken, baza seri olarak gelen endüktör hem giriş empedansının imajiner kısmının hem de gürültü eşleştirmesinin ayarlanmasında kullanılmaktadır. Ek olarak giriş empedans eşleştirmesi ve kazancın iyileştirilmesi için kutuplama endüktörü kullanılmıştır. Bu endüktör küçük işaret eşdeğerinde girişe parallel gelip, girişten görülen empedans değerinin arttırılmasında kullanılmış böylece dejenerasyon endüktansının daha küçük seçilebilmesine imkan tanımıştır. Dejenerasyon endüktansının değeri küçüldükçe gerilim kazancı artmaktadır. Böylelikle tek katta daha yüksek kazanç elde edilmiştir. Aynı zamanda girişe parallel gelen bu kutuplama endüktörü sayesinde girişe seri gelen baz endüktörünün değeri de küçültülmüştür. Girişe seri gelen baz endüktörünün seri direnci de gürültüye sebep olduğundan bu endüktörün değerinin küçültülmesi gürültü faktörünün azalmasını sağlamıştır.

Çıkış empedansı eşleştirmesi bir direnç, bir endüktör ve bir kapasite elemanı ile yapılmıştır. Endüktör ve kapasitenin rezonans frekansı devrenin çalışma frekansı olarak seçilmiştir. Teknoloji sarmal (spiral) endüktörlere izin vermediğinden ve sarmala en yakın endüktörlerin kalite faktörünün daha iyi olduğu bilindiğinden, sekizgen endüktörlerin tasarımı yapılmıştır. Kalite faktörünün yüksek olması düşük gürültüye ulaşmakta kritik bir faktördür.

Literatür araştırması özellikle düşük sıcaklıklarda düşük gürültülü kuvvetlendiricilerin kutuplama gerilim ve akımlarının değiştirilmesi ihtiyacını göstermektedir. Düşük gürültülü kuvvetlendiricinin kriyojenik ortamlara ve ışınıma uyum sağlayabilmesi için, kutuplama gerilimleri direkt olarak bağlantı ayaklarından (padlerden) alınmaktadır. Tasarlanan CMOS düşük gürültülü kuvvetlendirici 25 mW güç tüketirken, 15 dB'den yüksek gerilim kazancı ve 2.6 dB gürültü faktörü sağlamaktadır. Giriş ve çıkış empedansları, giriş ve çıkış yansıma katsayıları (sırasıyla S_{11} ve S_{22}) –10 dB'den küçük olacak şekilde eşleştirilmiştir. Düşük gürültülü kuvvetlendiricinin kararlılık benzetimi yapılmış ve tüm frekanslarda K kararlılık kriterinin birden büyük olması sağlanmıştır. Düşük gürültülü kuvvetlendiricinin doğrusallığı (lineerlik) üçüncü dereceden kesişim noktası (third-order intercept point, IP3) benzetimi ile gözlenmiştir. Girişte üçüncü dereceden kesişim noktası (input third-order intercept point, IIP3) –2.24 dBm olarak ölçülmüştür.

1. INTRODUCTION

Low noise amplifier (LNA) is first stage of receiver circuits. A superheterodyne receiver circuit, shown in Figure 1.1, consists of an antenna, a RF filter, a low noise amplifier, a mixer and a voltage controlled oscillator (VCO). Ideally, the signal received by the antenna is filtered and amplified by causing minimum degradation in signal to noise ratio (SNR). Thereafter, the signal frequency is converted to baseband through the demodulation by mixer where the center frequency is generated by the voltage controlled oscillator. Finally, the signal passed to digital signal processor unit. LNA is responsible here for amplifying the signal while adding as little noise as possible. Also, because the signal comes to LNA from the antenna, input power matching is very critical to avoid reflections at the input.

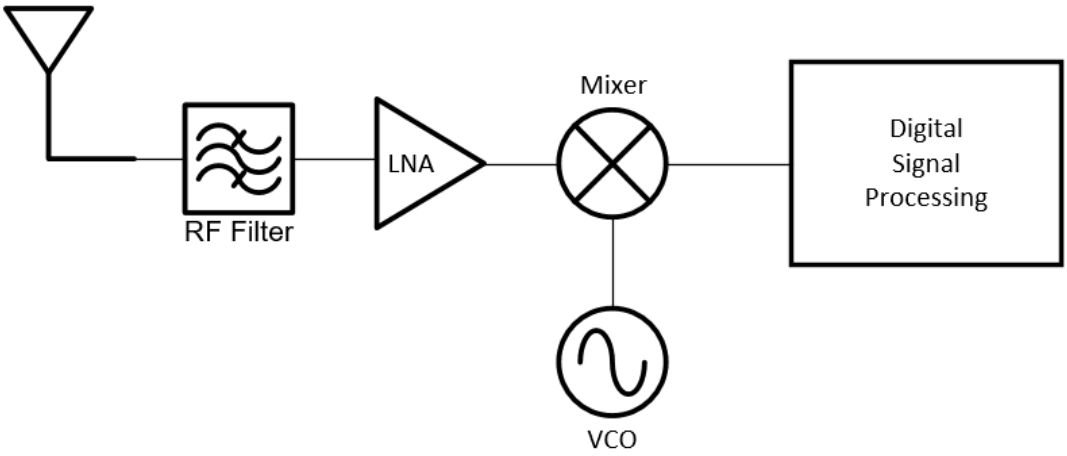


Figure 1.1 : Block diagram of a superheterodyne receiver

Low noise amplifiers receive signals with low signal-to-noise ratio (SNR) values. Consequently, it is essential to amplify these signals by adding little noise before transmitting to the next stage. Moreover, as shown in Figure 1.1, the receiver system is composed of building blocks that are cascaded. Friis formulated [1] the noise contribution of each cascaded stage to the total noise of the receiver system as (1.1)

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \quad (1.1)$$

(1.1) depicts that, the noise contribution of the stages after first are reduced by the gain value of previous stages. As the first stage of the receiver chain, noise figure of the LNA dominates the noise figure of the whole receiver system.

Low noise amplifiers are also used in space communications and radio astronomy [16]. Space electronics conditions can be listed as cryogenic temperatures and radiation. Performance improvement of transistors at cryogenic temperatures makes the design of LNAs at cryogenic temperatures more interesting [14]. There are studies in this area using SiGe and HEMT transistors indicating that LNAs designed at room temperature can also provide satisfactory performance at cryogenic temperatures [15]. Cryogenic performance of CMOS is investigated for a long periode. However, CMOS LNAs are interestingly rarely investigated at cryogenic temperatures.

There are also further studies on radiation robustness of RF circuits based on SiGe and HEMT devices [29]. Radiation effects on electronics circuits are divided into two sections such as single event effect (SEE) and total ionization dose (TID) [58, 59]. Since low noise amplifiers are mostly affected by TID, TID effects of radiation are studied in the scope of this thesis. Radiation robustness of CMOS circuits is an ongoing research area [54, 60]. These researches mostly focus on digital and mixed-mode performance, leaving an RF circuits area intact. SiGe and HEMT devices are claimed to be more radiation tolerant by the nature, however there are different types of CMOS design that improve the performance of the circuit under radiation [14, 61-63].

LNAs can be employed in discrete circuits, monolithic microwave integrated circuits (MMIC) and integrated circuits. Their main performance metrics can be listed as noise figure, gain, input and output reflection coefficients, stability and linearity. Even though the output impedance matching may not be necessary, if the LNA is going to be measured separately, it is still very critical for stability, since strong reflection waves at the output can sneak through the LNA input causing stability problems.

LNA performance mainly depends on the device technology and the design strategy. Even though the design strategy can improve the performance, mostly the device technology defines the borders of the results. Thus, technology selection and design optimization according to that technology is very important.

1.1 Purpose of Thesis

Space applications such as space communications require radiation hardened circuits that can work at cryogenic temperatures. The purpose of this thesis is to design an LNA for space applications to be tested at room temperature, cryogenic temperatures and under radiation. Designed LNA has been taped out and it is at the production stage. Thus the literature, design target and the LNA performance based on the post layout simulations with the available models are included in this thesis. After generic introduction to cryogenics and radiation the thesis focuses on the CMOS LNA design, including the methodology followed and the resulting performance. UMC 0.18 μm Mixed-Mode/RF technology is used in the LNA design.

Frequency bands of space communications are reported in Deep Space Network of California Institute of Technology document [66]. 7145–7190 MHz is designated to the uplink frequency band (from earth to space) in the X-band. Since LNAs are located in receiver systems, this LNA should receive the signal at space in 7145–7190 MHz band. Frequency band is enlarged 500 MHz at both limit considering process variations and modelling errors. Therefore, frequency band of this LNA is specified as 6670–7670 MHz.

This thesis is a part of the TUBITAK project "Analog and Radio Frequency Metal–Oxide–Semiconductor–Field–Effect–Transistor (MOSFET) Modeling and Integrated Circuit Design for Space Research". The main goal of this project is to model of transistors at cryogenic temperatures and under radiation and improve the performance of RF circuits operating in such extreme environment. Specifications of the LNA is designated as the voltage gain of 15 dB, noise figure of 1 dB at 80 K. Input and output reflection coefficients are targeted to be lower than −10 dB. The output IP3 is desired to be −10 dBm while the amplifier consumes a total power of 40 mW. Since below 1 dB noise figure is unattainable at room temperatures with the available technology, it is aimed to reach the lowest possible noise figure in this study. The noise figure is estimated to drop below 1 dB at cryogenic temperatures.

Firstly, a test chip is designed to extract the transistor models. Currently, this test chip is being measured to extract transistor characteristics. Afterwards, a LNA design will be done with the available models. This LNA is in the production process and is going to be measured both at room and cryogenic temperatures and under radiation. These

measurements will represent the LNA performance under space conditions and provide the designer with experimental insight for a better design. Finally, a new LNA will be designed with the new models, and its performance will be compared with the LNA designed in this thesis. As stated before, this thesis includes the design of 7 GHz LNA by adopting a classical design approach with existing models from UMC to be able to make a fair assessment on the performance of a classical LNA.

1.2 Literature Review

CMOS low noise amplifiers exhibit good performance of gain and noise under normal circumstances. General design methodologies have been extensively studied in many great books such as [10,27,57] and good papers such as [11,17-25]. Cryogenic and radiation performances of different LNAs also indicate that this area is open to further research [42-45, 48-54, 67-69].

1.3 Hypothesis

CMOS device performance is proven to improve at cryogenic temperatures for various design properties [28,30,31,37,38]. Moreover, CMOS devices that have an oxide thickness lower than 10 nm is claimed to be radiation tolerant to a total ionization dose (TID) of 300 kRad [55]. However, these findings are based on results of limited studies whose implementation is not executed prevalently. For example, there are other studies claiming that CMOS is vulnerable to radiation [56]. This study accredits the modelling of transistors under space conditions will improve the designed LNA performances. Thus, as a part of this thesis, the design of an LNA with classical models and methods are performed, showing good performance in the outcomes of post-layout simulations. The design of this LNA will present the reader a perspective on the CMOS LNA design with a 0.18 μm technology. A 7 GHz, 15 dB gain, 2.6 dB noise figure, 13.6 dBm OIP3 low noise amplifier is designed with a power budget of 25 mW. The designed LNA yields good performance compared to its counterparts in 0.18 μm device technology.

1.4 Thesis Organization

The first chapter introduces the project that the thesis is a part of and the work done in this thesis. While presenting LNAs, it discusses the role of LNAs in receiver systems

and its design requirements. Low noise amplifiers in extreme environments is investigated in the second chapter. The analysis starts with the device performance at cryogenic temperatures and under radiation, then it continues with LNAs in the same extreme environment conditions. This chapter summarizes previous work on LNAs at cryogenic temperatures and under radiation. Third chapter starts with the traditional CMOS LNA design methodology including as well as the noise theory, gain and matching theories. Subsequently, the design steps of 7 GHz LNA is presented. Lastly, the conclusion of the thesis is presented with what has been accomplished in the design and what the future encompasses.

2. LOW NOISE AMPLIFIERS IN EXTREME ENVIRONMENTS

Extreme environment definition span for where ambient temperatures ranging from the very low to very high, and for the environments in which radiation doses are high. Those environment conditions eventually effect electronic devices. Robust design of electronic devices tolerant to these extreme environment conditions is an extensively studied topic. However, these studies mostly focus on technologies such as Silicon-Germanium (SiGe) heterojunction transistors (HBT), Gallium-Arsenide (GaAs) and Indium-Phosphide (InP) high electron mobility transistors (HEMT). These devices perform well at cryogenic temperatures and they are relatively robust to radiation. Investigation of CMOS devices in extreme environments scarcely inquired topic, however low cost and high integration capability of CMOS provides a substantial motivation for research. In this chapter, RF design case studies for extreme environments will be briefly reviewed. Firstly, electronic devices that are used in RF designs and their performance in extreme environments will be discussed. Then, previous research on low noise amplifiers in extreme environment will be comparatively examined.

2.1 Devices and LNAs at Cryogenic Temperatures

This section includes the general research of LNAs and transistors at cryogenic temperatures for the purpose of LNA design. Investigation of transistor performance at cryogenic temperatures dates back early in the electronics history. Historically, performance of CMOS transistors was investigated first. However, as technology becomes diverse, SiGe and HEMT devices have been discovered to present better RF performance than their CMOS counterparts.

2.1.1 Devices at cryogenic temperatures

Research on performance changes of electronic devices is an important topic for many applications such as radio astronomy, space electronics and high speed electronics. Cryogenic response of CMOS devices was a hot topic back in the 80s and 90s. However, with the rapid

improvement of other technologies such as SiGe HBT and HEMT devices, these devices have taken over the place of CMOS especially in RF circuits.

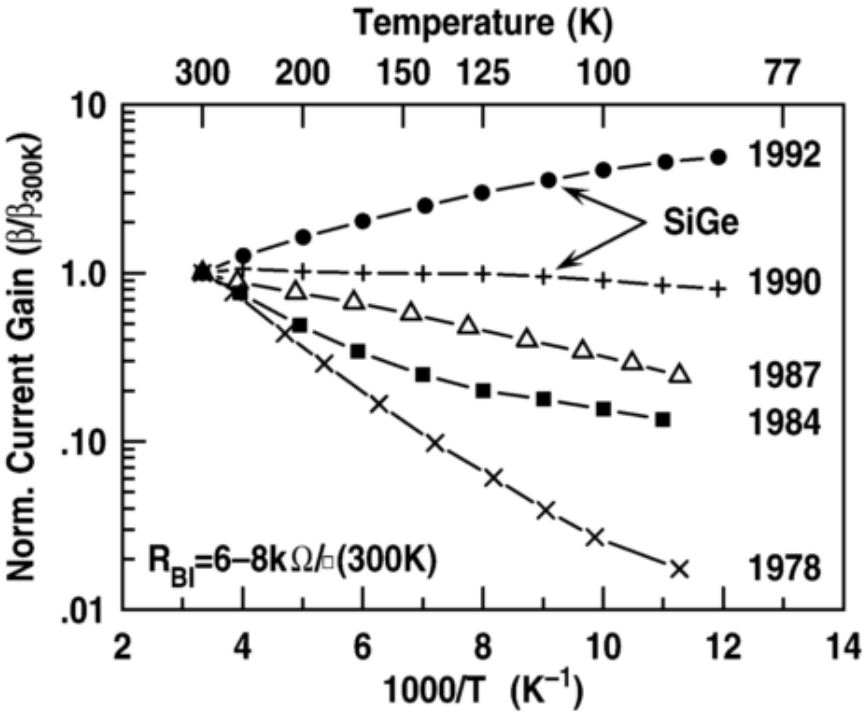


Figure 2.1 : Current gain improvement of SiGe devices in history [29]

The potential of SiGe HBTs have been extensively studied by Cressler [29], showing that SiGe HBT devices are promising for cryogenic circuit design. Moreover, this study is supported with more studies [15, 42-45] on the design of LNAs. As stated in [29], cooling these devices improves the critical properties such as current gain (β) and cut-off frequency(f_T). As seen in Figure 2.1, current gain increases with the Ge implantation to Si devices. It is stated that with proper bandgap engineering of SiGe compositions, performance of HBT devices at cryogenic temperatures can be significantly improved. Furthermore, a special SiGe HBT named "emitter-cap" optimized at 77 K has been tested to yield much better performance at cryogenic temperatures. Figure 2.2 depicts the improvement of current gain of this device.

In addition to the development of SiGe HBT technology, HEMT technology also improved in cryogenics. There are many studies on the performance of circuits and systems designed with HEMT devices in the literature. [46-49]. As stated in [46], HEMT drain current and transconductance increases as temperature decreases. Figure 2.3 shows the drain current and transconductance graphs of a $Ga_{0.51}In_{0.49}P$/GaAs HEMT device whose size is 1 um x 150 um.

Measurements of this device is done by varying gate-to-source voltages at 300K and 77 K when a fixed drain-to-source voltage of 3 V bias applied. Further studies have taken place in the literature on the cryogenic performance of HEMT devices such as [47-49]. For example, a comparison of HEMT and GaAs FET devices is done in [47], showing that HEMTs have relatively better noise figure performance compared to GaAs FETs.

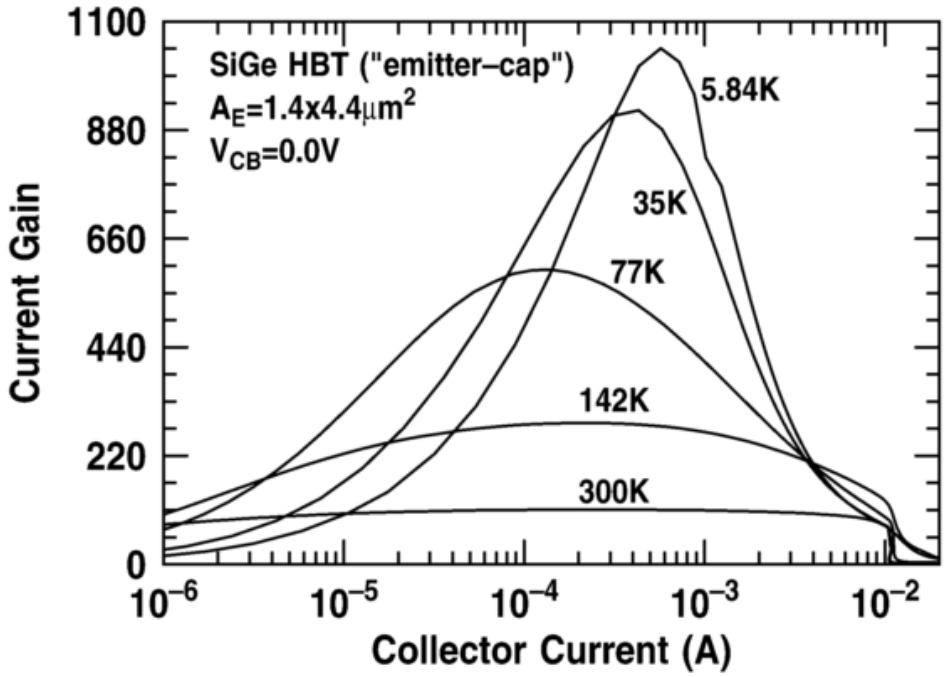


Figure 2.2 : Current gain improvement of a SiGe HBT which is optimized for operation at 77 K [29]

As discussed above, cryogenic performance of SiGe, GaAs FET and HEMT devices were conducted extensively in the literature, concluding their superior performance at cryogenic temperatures. However, these technologies are more sophisticated and expensive compared to CMOS technology. Performance improvement of CMOS devices at cryogenic temperatures can reduce the cost and enable the cryogenic circuit design in a wide range of applications. Thus, investigation of CMOS performance at cryogenic temperatures can be leveraged in RF circuits which stands out as a source of motivation for this work.

Performance of CMOS devices at cryogenic temperatures is an extensively investigated topic since 1970s [28-41]. Different transistor quantities such as the drain current, transconductance, cut-off frequency, mobility, threshold voltage, subthreshold swing, aging effects and etch have been considered. Mostly, analog and mixed-signal designs are aimed in these studies, and

research on RF characteristics of CMOS devices at cryogenic temperatures is still ongoing. In particularly, design of CMOS LNAs for cryogenic applications deserves further attention.

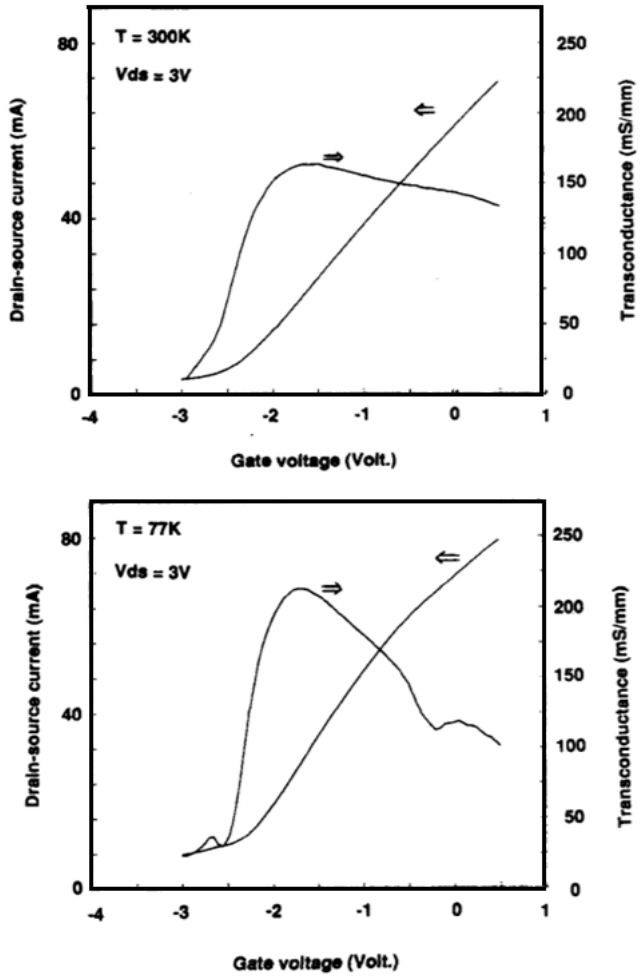
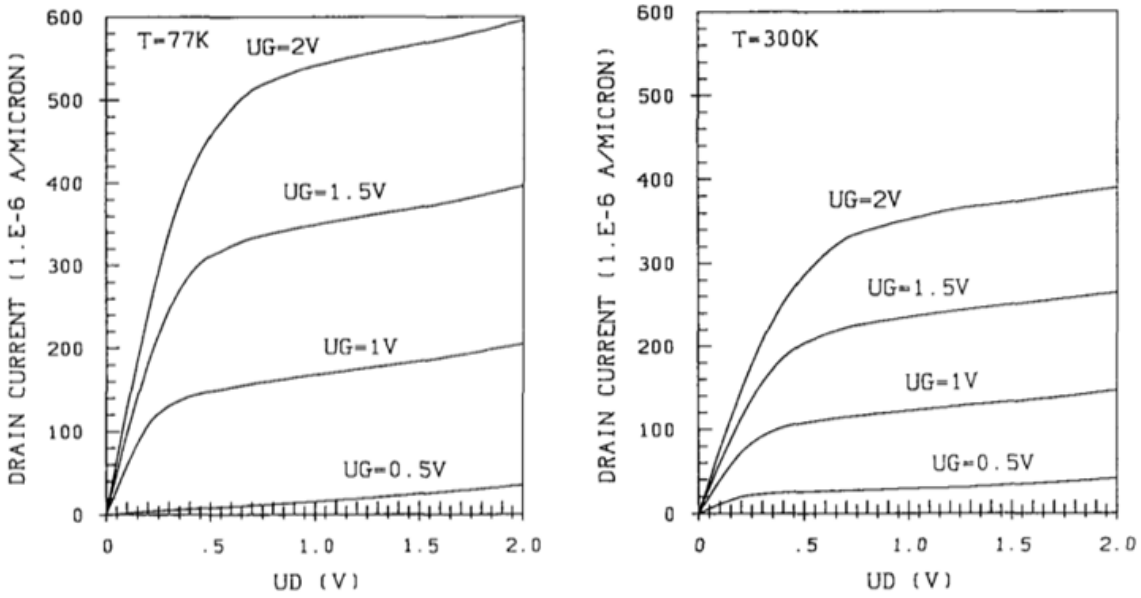


Figure 2.3 : Drain current and transconductance characteristics of a HEMT device at 300 K (above), at 77 K (below) [46]

One of the fundamental outcome of this research states that, as temperature decreases, the drain current of MOS increases [28-30, 36-38]. Figure 2.4 demonstrates this observation by presenting the drain current increase from 300 K to 77 K from the simulated data of based on an extensive modelling approach. However, author states that more measurement verification is needed for this research [38]. Figure 2.5 shows the drain current measurements of Si CMOS devices from the 0.5 um SiGe BiCMOS process. This figure shows that as temperature decreases from 300 K to 43 K, the drain current increases for the same bias conditions. This observation has been attributed to the increase of the carrier mobility [14]. The most recent

study compares the drain currents of 0.16 um and 40 nm technologies for both NMOS and PMOS devices at 300 K and 4K in Figure 2.6 respectively [35].



(a) (b)

Figure 2.4 : Model simulation results for the drain current of an NMOS device vs. its drain voltage at (a) 77 K and (b) 300 K [38]

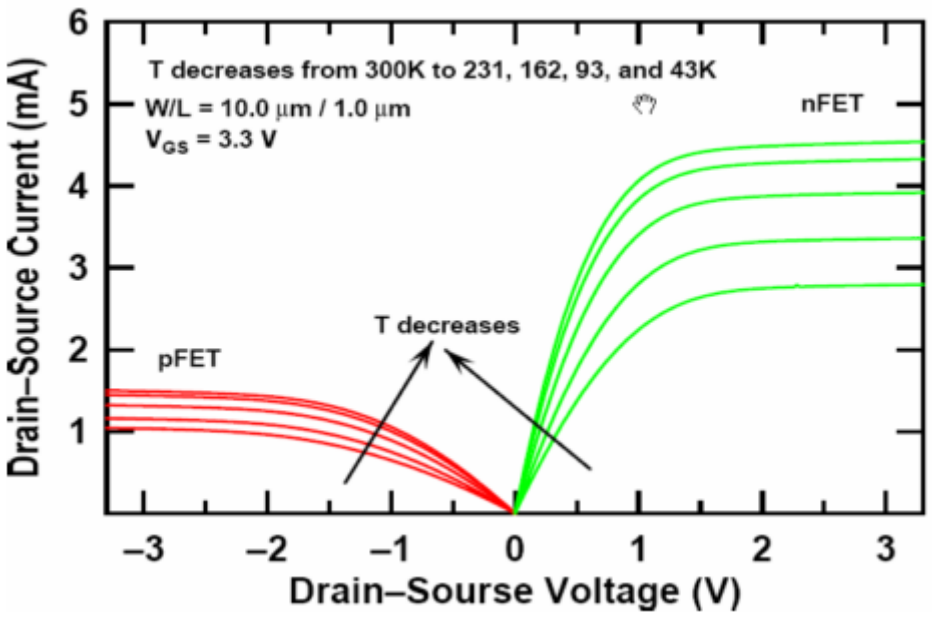
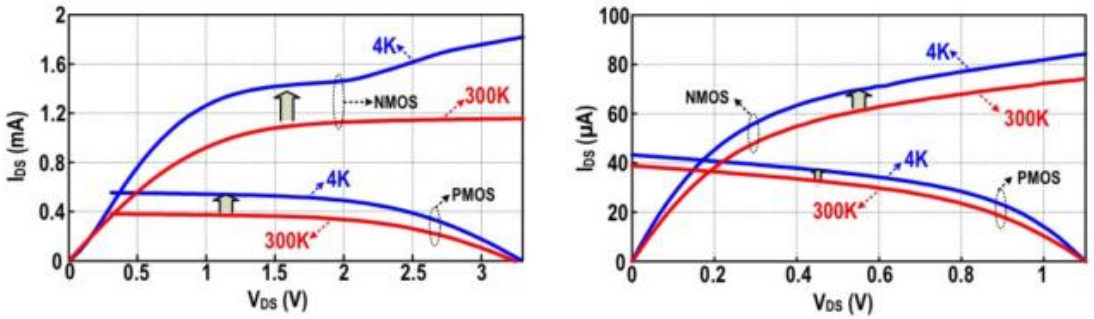


Figure 2.5 : Measurement results for the drain current of an n-channel and p-channel MOS device vs. their drain voltages for different temperatures in Kelvin [14]



(a) (b)

Figure 2.6 : Measurement results for the drain current of NMOS and PMOS devices vs. their drain voltages for different temperatures in Kelvin by measurements for (a) 0.16 um technology and (b) 40 nm technology [35]

Similar to drain current, transconductance (g_m) of MOSFETs are shown to increase with the decreasing temperature. It is stated in [30] that as the temperature decreases, transconductance and effective oxide thickness (EOT) multiplication increases with diminishing temperatures until 100 K as in Figure 2.7. However, further reduction of temperature, decreases the transconductance due to carrier freeze-out. In Figure 2.7, SiO_2 and HfO_2 devices are compared, but they have different effective oxide thickness. Thus, transconductance is multiplied with the EOT to have a fair comparison of the transistors that have different EOT.

Similarly Figure 2.8 depicts that, the cut-off frequency increases as temperature decreases, until 100 K, after which it drops due to the carrier freeze-out [30]. As temperature decreases dopants cannot be fully ionized and density of ionized carriers gets smaller leading to increased resistivity. For example, for a device that the majority carriers are electrons, below certain temperature electron density falls below the acceptor density. This reduction in carriers is shown in Figure 2.9 and called as carrier freeze out [38-41]. Although these comparisons show that high dielectric oxide transistors show better performance compared to the SiO_2 devices, improvement of SiO_2 devices is also inevitable. Figure 2.9 also indicates to the performance differences between HfO_2 and SiO_2 devices, with HfO_2 based transistors having larger f_T but smaller g_mxEOT product for all temperatures.

Carrier mobility of MOS devices is critical at cryogenic temperatures and has been studied since 1970s [38-41]. These studies indicate that as the temperature decreases, carrier mobility increases. Nonetheless, for very low temperatures below 100 K, carrier mobility starts to drop. This effect is also associated with the carrier freeze out problem. It is stated that in highly doped

devices carrier freeze out happens at lower temperatures compared to lightly doped devices [28,37]. Carrier freeze-out problem is also dependent on the device technology and a recent study [36] suggests that carrier freeze-out is not a problem for new technology devices.

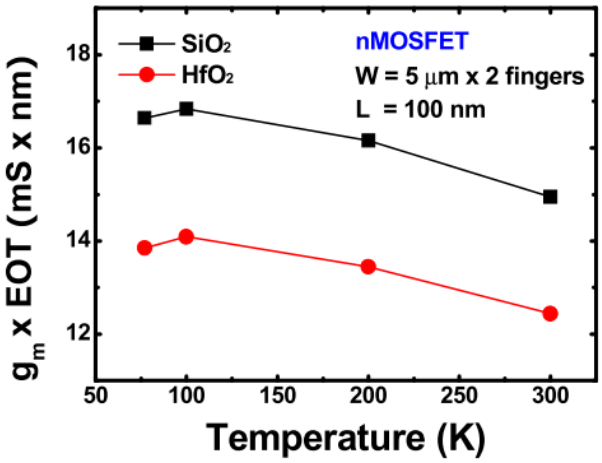


Figure 2.7 : Transconductance and EOT product change of an NMOS with respect to temperature [30]

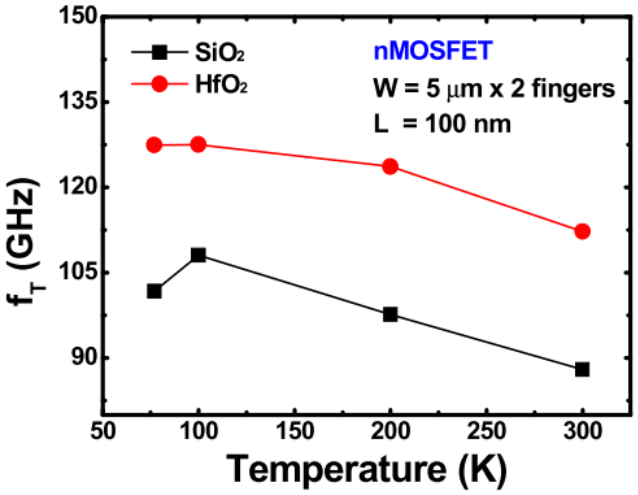


Figure 2.8 : Cut-off frequency change of an NMOS with respect to temperature [30]

Change of the threshold voltage with temperature is investigated in various papers. Figure 2.10 shows that threshold voltage increases with different channel lengths as temperature decreases [37]. In another study [38], for two different drain bias (UD=0.1 V & UD=2 V) and two different temperature values (T=77 K & 300 K), change of the threshold voltage with respect to changing channel length values are drawn in Figure 2.11. For long channel devices, threshold voltage is 580 mV at 77 K, while it is 340 mV at 300K.

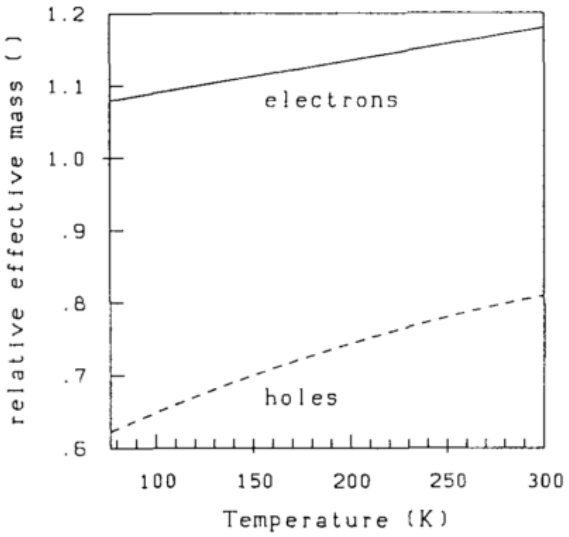


Figure 2.9 : Change of relative mass of carriers in silicon according to temperature [38]

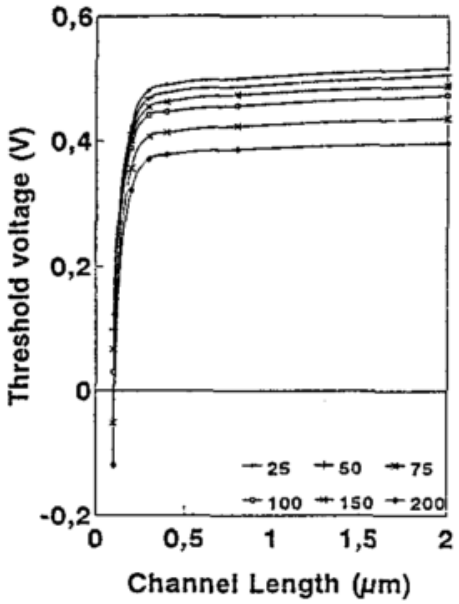


Figure 2.10 : Threshold voltage of an NMOS device vs. channel length for different temperatures in Kelvin [37]

As stated before, a test chip is designed to measure the differences of the transistors at room and cryogenic temperatures in the scope of this thesis. RF NMOS transistors are measured at 293 K and 80 K and results are shown in Figure 2.12 and 2.13. Channel width of the transistor is 35 µm while the channel length is 0.18 µm. Figure 2.13 implies that the threshold voltage increases as the temperature decreases. Eventhough the threshold voltage increases, because of

an effective increase in the carrier mobility, the drain current of the RF NMOS transistor increased at cryogenic temperatures as given in Figure 2.12. Thus, measurement results verify the reported trends in previous studies.

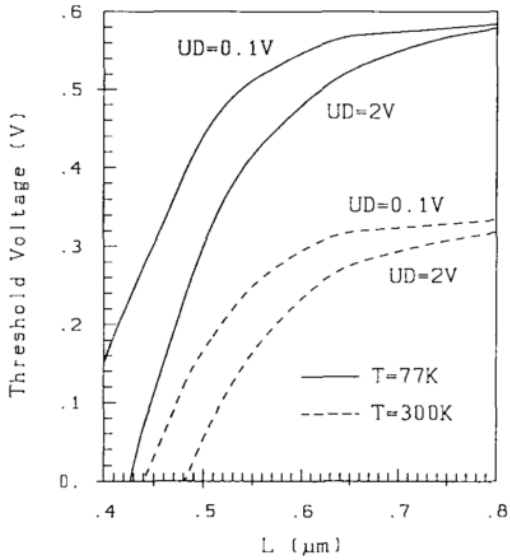


Figure 2.11 : Threshold voltage of an NMOS device vs. channel length for 77 K & 300 K [38]

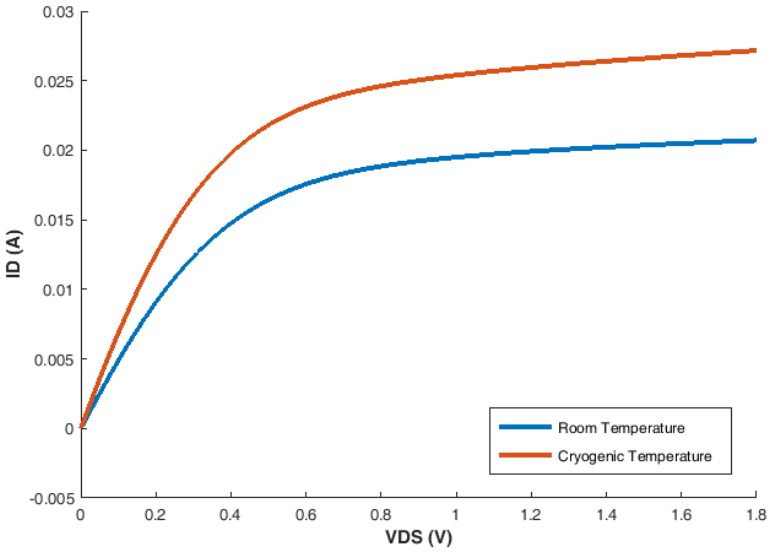


Figure 2.12 : I_D vs. V_{DS} graph of RF NMOS at 293 K and 80 K (V_{GS} *=1.8 V*)

Since research is mostly interested in digital performance, most of the topics of research on CMOS are subthreshold swing, hot carrier injection, and etc. For RF designs the current density and transistor capacitances are of paramount importance. MOS capacitances at cryogenic

temperatures have not been analyzed in depth. To the author's knowledge only one study states that the MOSFET gate capacitance is somewhat higher in the inversion region at 50 K, than it was at 300 K. Moreover, MOSFET gate capacitance changes drastically in the accumulation region especially for higher frequencies. The graph of the gate capacitance is given in Figure 2.14 [32]. This indicates a special care for RF design at cryogenic temperatures must be taken into consideration.

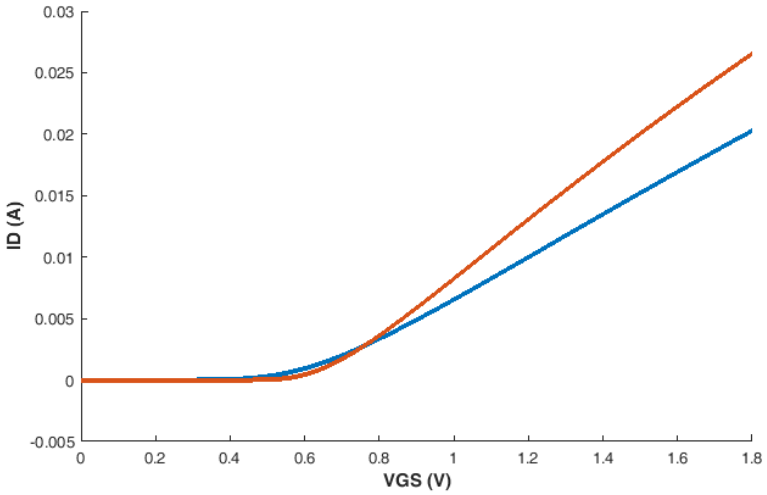
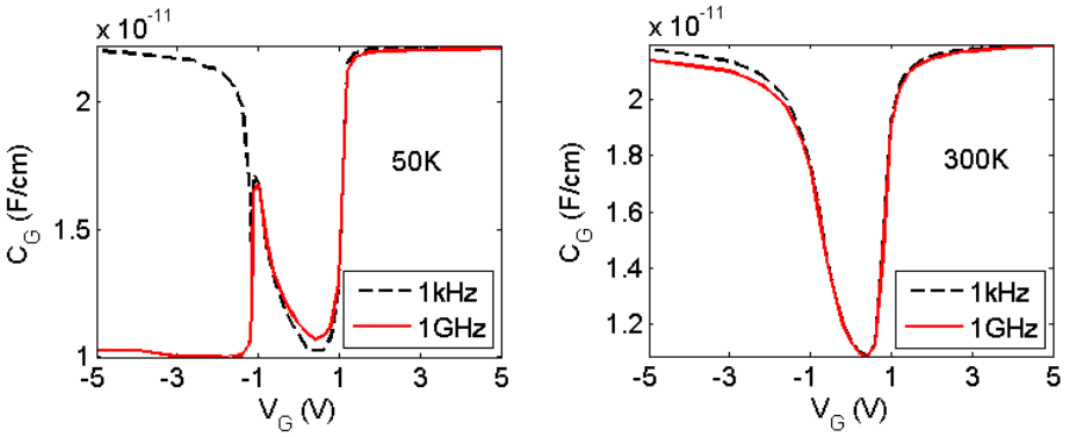


Figure 2.13 : I_D vs. V_{GS} graph of RF NMOS at 293 K and 80 K (V_{DS}=*1.8 V*)



(a) (b)

Figure 2.14 : Unit gate capacitance (C_G) vs. gate voltage (V_G) at temperatures (a) 50 K and (b) 300 K [32]

Aging effects such as hot carrier injection (HCI), negative-bias temperature instability (NBTI) and positive bias temperature instability (PBTI) are getting worse in CMOS devices as temperature decreases. However, these topics are not in the scope of this thesis.

To summarize for the same biasing conditions, following observations can be made in a SiGe HBT device at cryogenic temperatures:

- Its collector current increases (improvement)
- Its current gain increases (improvement)
- Noise contribution of the device decreases (improvement)

Similarly, for the same bias conditions HEMT devices undergo the following changes:

- Its drain current increases (improvement)
- Its transconductance increases (improvement)
- Noise contribution of the device decreases (improvement)

Finally, for the same biases underlies CMOS device exhibits the following characteristics at cryogenic temperatures:

- Its drain current increases (improvement)
- Its transconductance increases (improvement)
- Its cut-off frequency increases (improvement)
- Its threshold voltage increases (degradation)
- Its thermal noise decreases (improvement)
- Aging effects such as HCI, NBTI and PBTI aggravate (degradation)

2.1.2 LNAs at cryogenic temperatures

Nearly all of the research on cryogenic LNAs have been conducted using SiGe and HEMT device technology. While their superior performance is the main reason for this choice in general, their expensiveness remains as an obstacle in the widespread adoptions in cryogenics. Conversely, CMOS technology is dominating the electronics industry and is a more economical

technology that can be utilized more easily to promote scientific researches and commercial products. Thus, there is a growing potential of CMOS devices cryogenic applications.

Before an in-depth discussion of cryogenic LNAs, definition of the noise temperature should be explained. Noise temperature is another way of expressing the available noise power introduced by a component or a system. It is used to define the noise measure when generally low noises exist. Since the noise in the electronic circuits are not determined, they can be represented as a Johnson-Nyquist noise source. Thus, defining the noise source in terms of the noise temperature that would generate the same amount of noise power spectral density is valid. Noise temperature and noise figure relation is given in (2.1). Ambient temperature usage is very common, when noise temperature measure is also used to inhibit the confusion. Ambient temperature can be defined as the temperature of the environment that the circuit is located. In addition, noise temperature is strongly depended on ambient temperature.

$$NF = 10\log(\frac{T_{noise}}{T_{ref}} + 1) \tag{2.1}$$

2.1.2.1 SiGe based LNAs

Due to superior transistor properties of SiGe technology at cryogenic temperatures as explained in section 2.1.1, SiGe LNAs have yielded promising outcomes [29, 42-45]. The SiGe LNA in [51] shows 4 dB average gain increase and nearly 100 K drop in noise temperature at cryogenic temperatures as shown in Figure 2.15. The comparison of noise temperatures of SiGe LNAs at cryogenic temperatures is given in Figure 2.16 shows that very low noise temperatures as 5 K are achieved at cryogenic temperatures as low as 15 K.

A SiGe LNA is measured at different ambient temperatures 293 K, 200 K, 80 K, 40 K and 15 K in [43], demonstrating nearly linear noise temperature decrease as the ambient temperature decreases. (Figure 2.17) This result is compatible with the expectations since the dominant noise source in LNAs are temperature dependent. However, the outcome of this study is important in another aspect such that whether noise match condition of this LNA is not deteriorated by the temperature decrease hence the DC operating point change, or temperature decrease is more effective on noise even noise match is no longer ensured. Moreover, Figure

2.17 depicts that when the collector current is increased, noise temperature decreases, showing a better noise match.

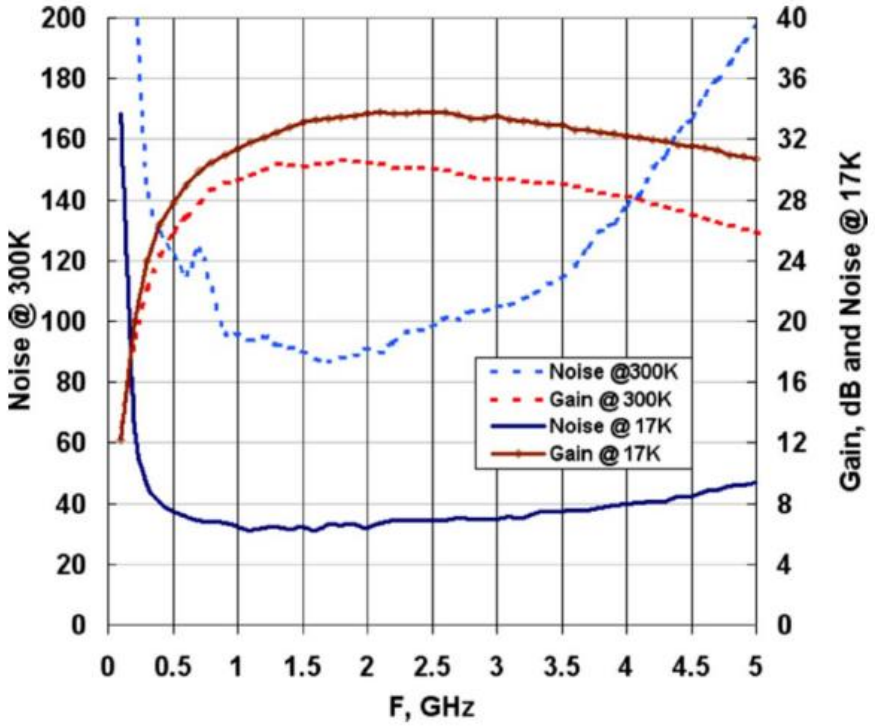


Figure 2.15 : Gain increase and noise temperature drop of a SiGe LNA at cryogenic temperatures [51]

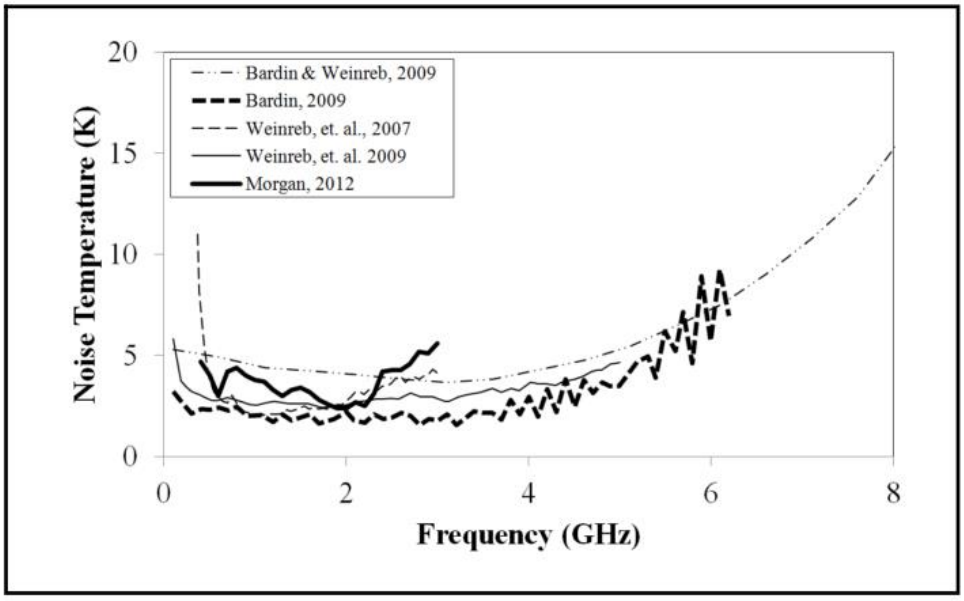


Figure 2.16 : Summary of SiGe LNA noise temperatures [49] of the SiGe LNAs reported in [42], [50], [43], [51] and [52]

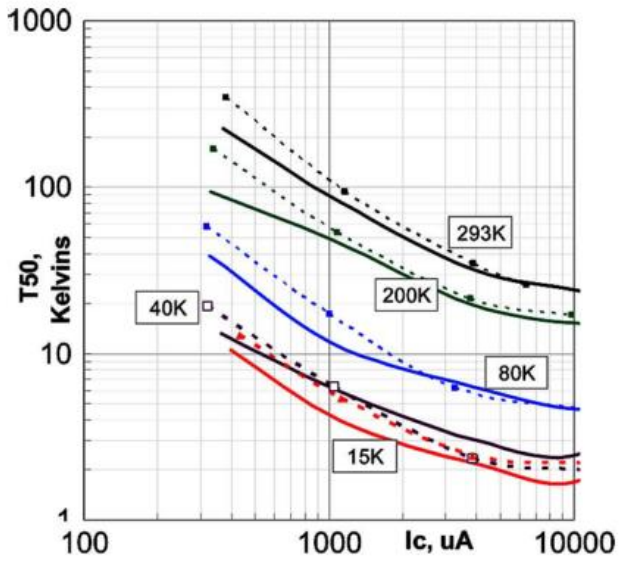
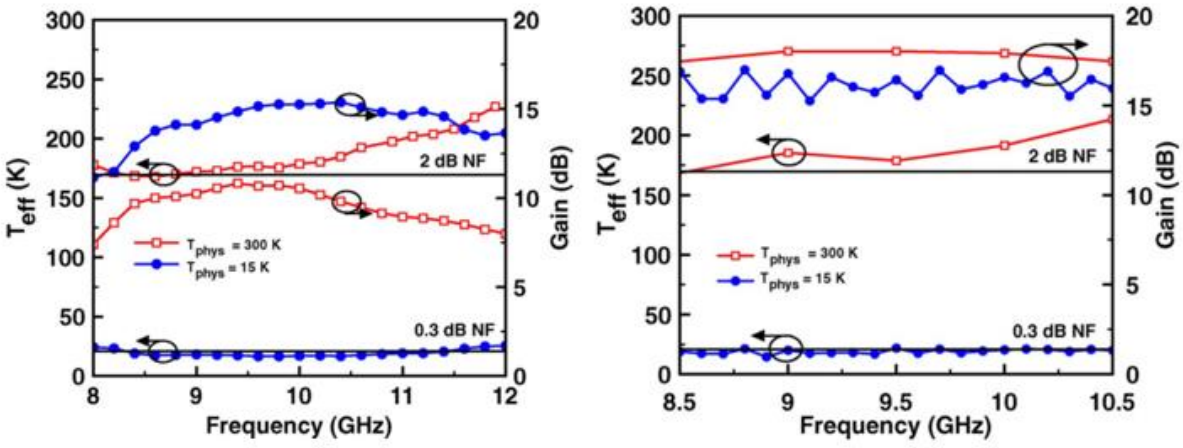


Figure 2.17 : Noise temperatures of an SiGe LNA at various ambient temperatures [43]

Two SiGe LNAs have been compared in [15] is shown in Figure 2.18. First LNA (a) is optimized for low power consumption, and the second LNA (b) is designed for less than 1.5 dB noise figure. The LNA in 2.18 (a) has lower noise figure and nearly 5 dB higher gain at 15 K ambient temperature, with respect to its performance at 300 K. However, the second LNA exhibits a decrease in gain with a reduced noise figure. This is interpreted by the authors that power constrained design performs better, since currents increase when the temperature is lowered [15].



(a) (b)

Figure 2.18 : Comparison of gain and noise temperatures of two SiGe LNAs at 300 K and 15 K [15]

2.1.2.2 HEMT based LNAs

HEMT devices are widely used in monolithic microwave integrated circuit (MMIC) LNA design. Performance of an HEMT LNA in cryogenic temperatures is given in [52]. Figure 2.19 depicts that the gain of this low noise amplifier is increases at lower temperature.

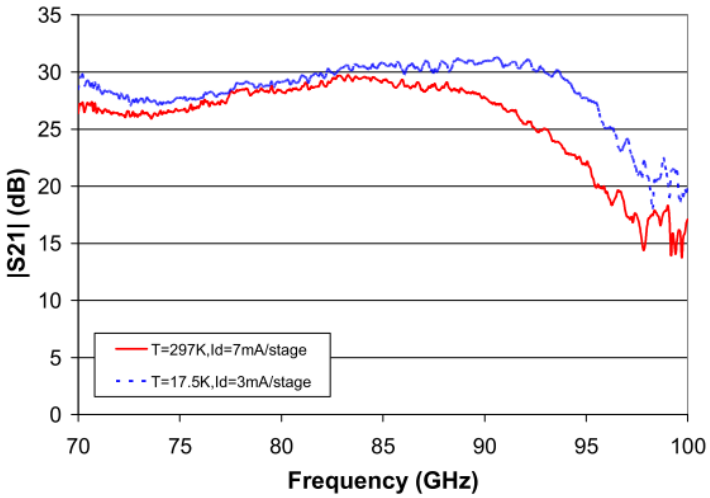


Figure 2.19 : Gain improvement with the temperature decrease in an LNA designed with HEMT devices [52]

Noise figure and gain improvement of another HEMT LNA is given in Figure 2.20 [53]. This result also indicates that HEMT LNAs have improved performance metrics at cryogenic conditions.

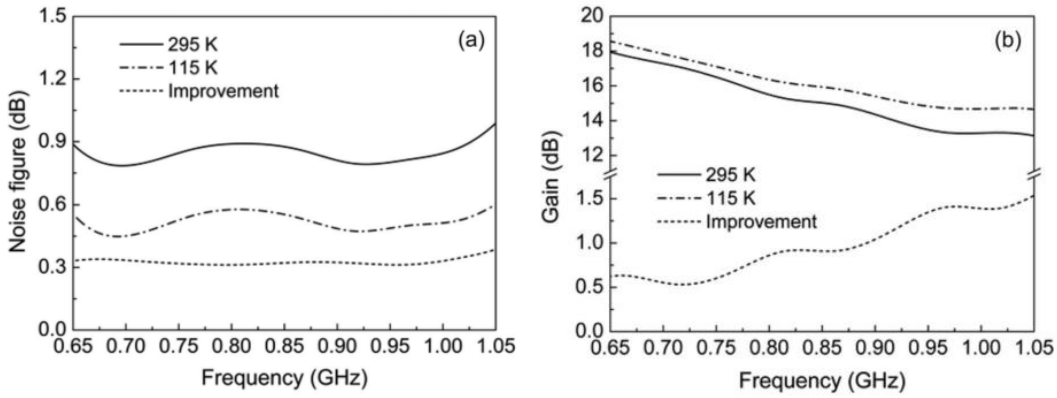
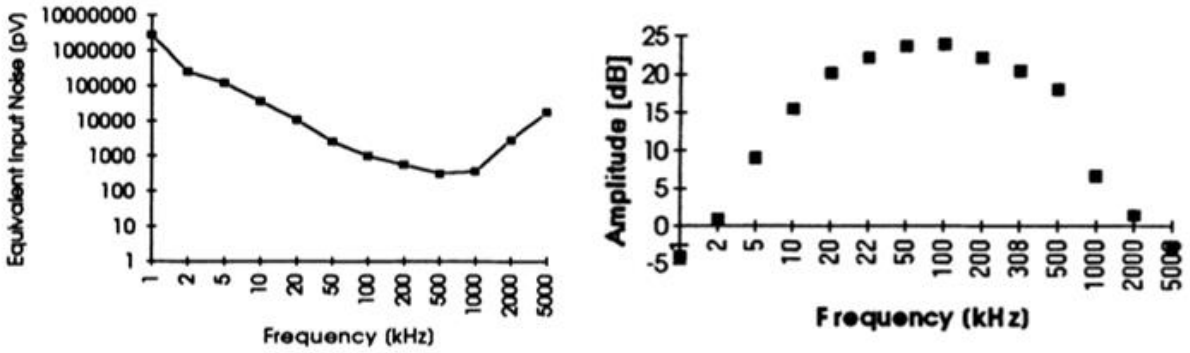


Figure 2.20 : Noise figure and gain improvement with the temperature decrease in an LNA designed with HEMT devices [53]

As explained before and shown in the Figures 2.15-2.20, SiGe and HEMT devices yield better performances at cryogenic temperatures than at room temperatures due to the improved device properties as seen in Figures 2.1-2.4.

2.1.2.3 CMOS based LNAs

Research of CMOS LNAs at cryogenic temperatures is much scarce compared to HBT and HEMT based LNAs. To the best of author's knowledge, the only LNA designs that are tested at cryogenic temperatures were provided in [34] and [35]. The first one is a low noise CMOS readout preamplifier designed for cryogenic temperatures cited in [34]. Measurement results of this preamplifier is shown in Figure 2.21. It is stated that the equivalent noise is lower than $0.5nV/\sqrt{Hz}$ at 20 kHz and the flicker noise (*1/f*) is dominant in these frequencies at cryogenic temperatures. Gain of the amplifier is also shown in Figure 2.21 (b), however the comparison of these metrics to room temperature measurements are not presented in the study.



(a) (b)

Figure 2.21 : Equivalent input noise (a) and gain (b) of the pre-amplifier at 4 K [34]

The second one is a very recent study that has reported measurements of a CMOS LNA at cryogenic temperatures, with no noise figure measurement being included [35]. The paper reports only the gain measurement (Figure 2.22) of the LNA at liquid helium temperature and that states noise figure is expected to be 0.009 dB which cannot be measured due to the experimental deficiencies. They attribute this very low noise figure to noise cancellation and 4 K ambient temperature. Finally, it has been mentioned that the designed LNA operates until 1.2 GHz and does not include any inductors.

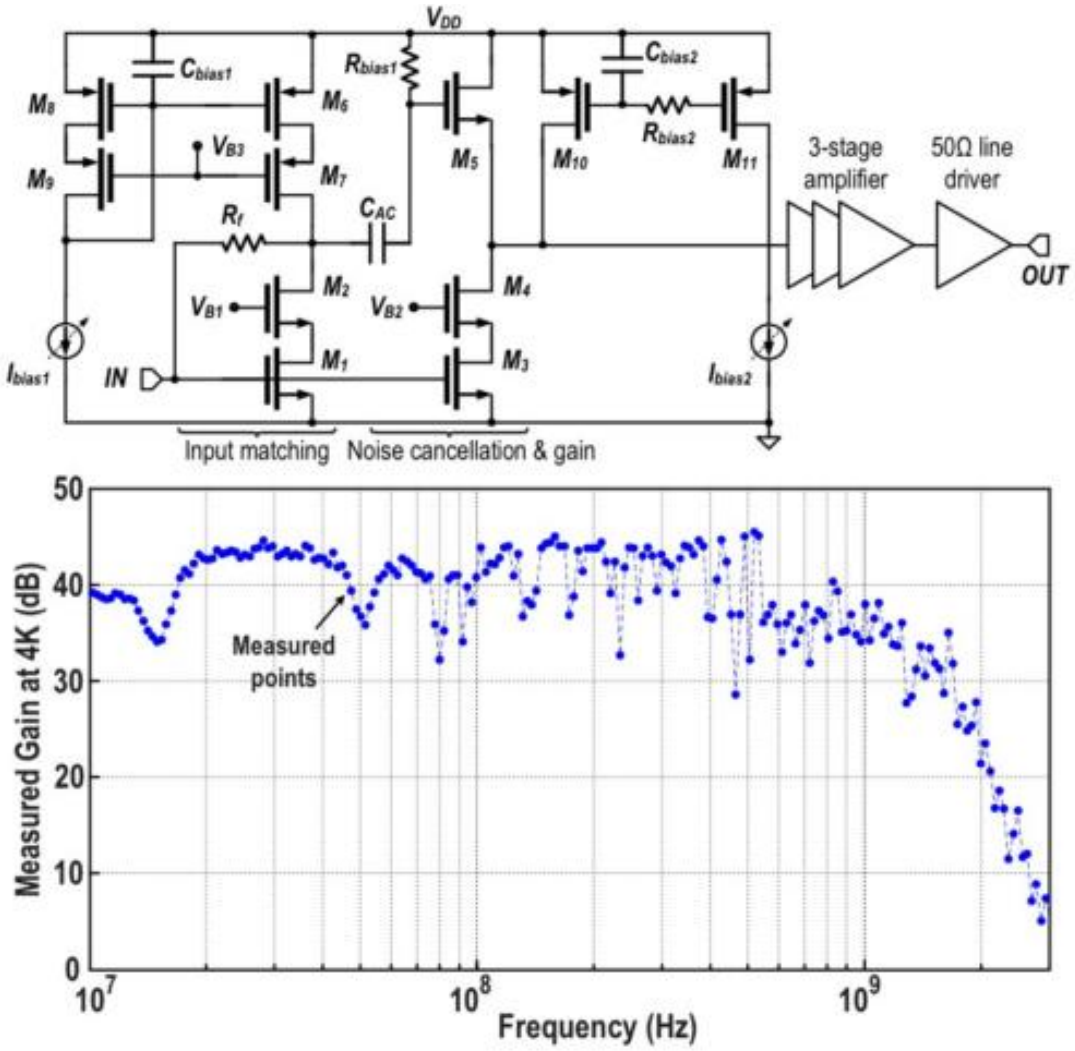


Figure 2.22 : Schematic of CMOS LNA with noise cancelling and measured gain at 4 K [35]

2.2 Devices and LNAs under radiation

Electronic circuits need to be robust against radiation damage to be able to work in space. For LNAs, the foremost radiation impact comes from total ionization dose (TID). Ionising radiation (ionizing radiation) is radiation that carries enough energy to free electrons from atoms or molecules, thereby ionizing them [64]. Total ionization dose should be applied with Co-60 sources homogenously according to European Space Agency (ESA) [58]. There are also different irradiation types that are used to test radiation robustness of RF circuits such as X-ray and proton radiations.

2.2.1 Devices under radiation

Research on radiation damage to electronic devices has been mostly done considering SiGe and HEMT circuits. Research with CMOS circuits focus concentrated on the digital or mixed mode designs mostly. There are many gaps in the research of RF circuits designed with CMOS technology under radiation. Transistor performance affects the design of the circuits preeminently. Thus, investigation of transistor performance under radiation is an important step in the design of radiation-hardened circuits.

Research of SiGe HBTs under radiation shows that SiGe technology is very robust to radiation as given in [29]. Figure 2.23 indicates that the cut-off frequency performance of different generations of SiGe HBTs at pre-radiation and post-radiation, and it can be seen that the cut-off frequency is only slightly degraded by radiation.

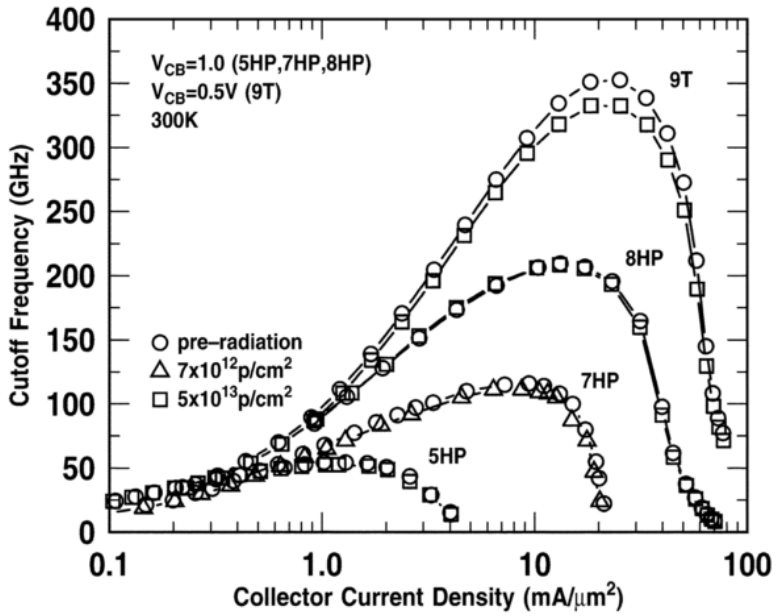


Figure 2.23 : Cut off frequencies of SiGe HBT devices with different technologies given pre and post-radiation [29]

HEMT devices are also investigated under radiation, and exhibit good performance under total ionizing doses. As shown in Figure 2.24, drain current of PHEMT device does not change until total dose exceeds 100 Mrads. In this figure, applied drain voltage is 2 V and initial drain current is 8 mA for DC operation. In standby operation drain voltage is not changed, however gate voltage is adjusted to -2 V.

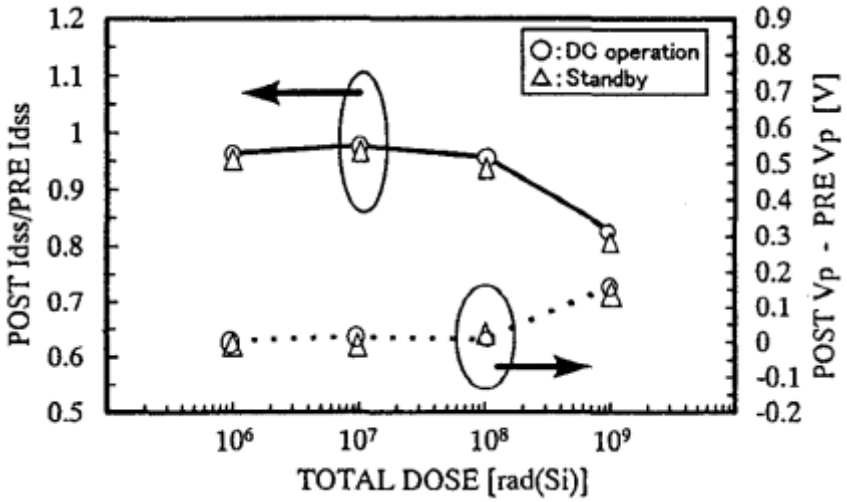


Figure 2.24 : Post and pre-radiation drain current ratio and pinch-off voltage (V_P) of a PHEMT according to total dose [65]

CMOS devices are examined under radiation extensively in the literature. Main subject of these studies, which begin in late 70s, are DC characteristics of MOS transistors such as drain current and threshold voltage. Figure 2.25 shows the drain current graph of a MOSFET whose channel length is 0.7 μm. It is stated that as the radiation dose increases drain current at a constant gate voltage increases. This also illustrate that the threshold voltage is decreasing as the radiation dose increases. This effect is also shown in Figure 2.26 clearly for different channel lengths [67]. Radiation effects on MOS devices are summarized in [60] as below:

- Decrease of transconductance
- Threshold voltage shift
- Increase of leakage currents
- Reduction of drain-source breakdown voltage
- Deterioration of noise parameters
- Reduction in surface mobility
- Increase of the surface recombination velocity

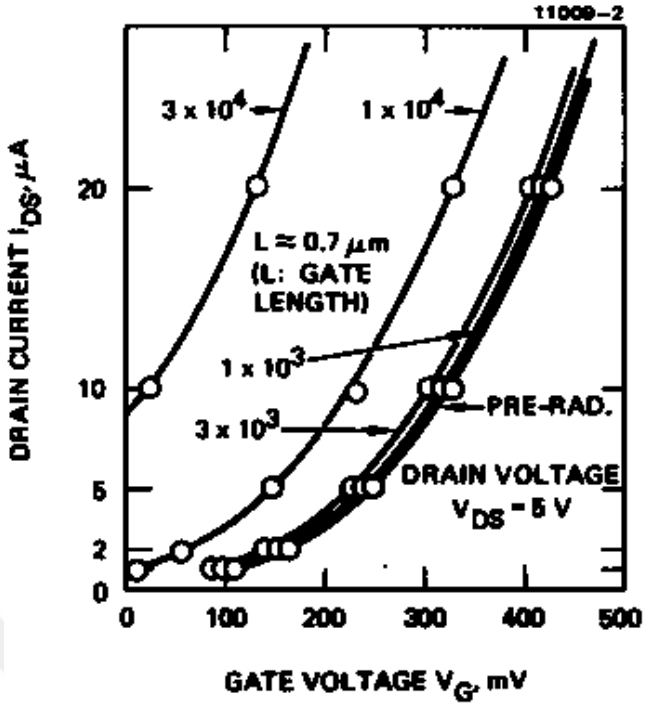


Figure 2.25 : Drain current vs. gate voltage for a MOSFET at various radiation doses [67]

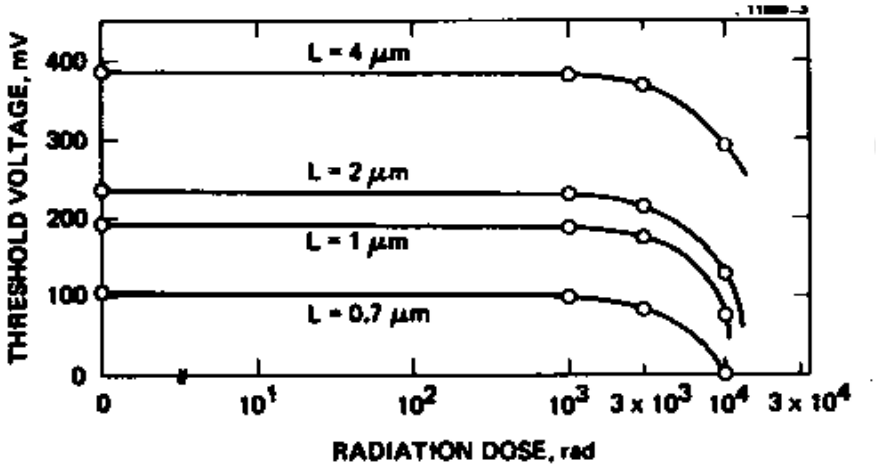
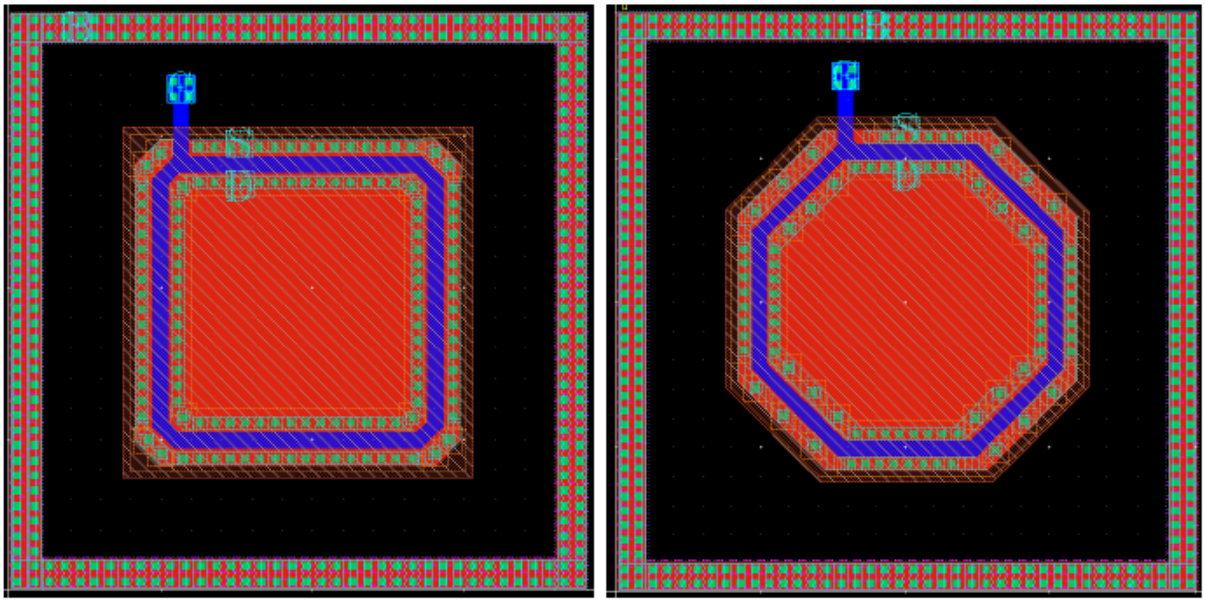


Figure 2.26: Dependence of threshold voltage on radiation dose for devices with various gate lengths [67]

There are methods to compensate radiation effects such as double guardring, enclosed layout transistors (ELT) and thinner gate oxides. Thinner gate oxides are achieved with today's technology and CMOS devices are more robust to total ionization dose irradiation. Enclosed layout transistors and double guardring structures mostly focus on minimizing the leakage current increments caused by radiation. Enclosed layout transistor is constructed as in Figure

2.27 so that field oxide traps cannot occur at drain side, also parasitic devices, which cause latch up, are precluded [64].



(a) (b)

Figure 2.27 : Enclosed layout transistors (a) square and (b) octagonal shaped

2.2.2 LNAs under radiation

Radiation robustness of low noise amplifiers is an underinvestigated topic. Few study lay emphasis on durability of RF circuits to gamma radiations. Some studies adopt X-ray and some use electron and proton radiations. Since investigation of LNAs is divided under three categorizations as HEMT, SiGe HBT and CMOS, radiation performance can also be examined for these blocks.

An LNA which is designed with pHEMT device shows a stable performance to total ionization dose generated by a Co-60 gamma ray source. Figure 2.28 indicates that gain of this LNA does not change till 10 Mrad, and starts to degrade after that dose. At 1 Grad irradiation, reduction of the gain reaches to 2 dB. This figure also includes the noise figure performance, showing that nearly no change in noise figure at all radiation doses.

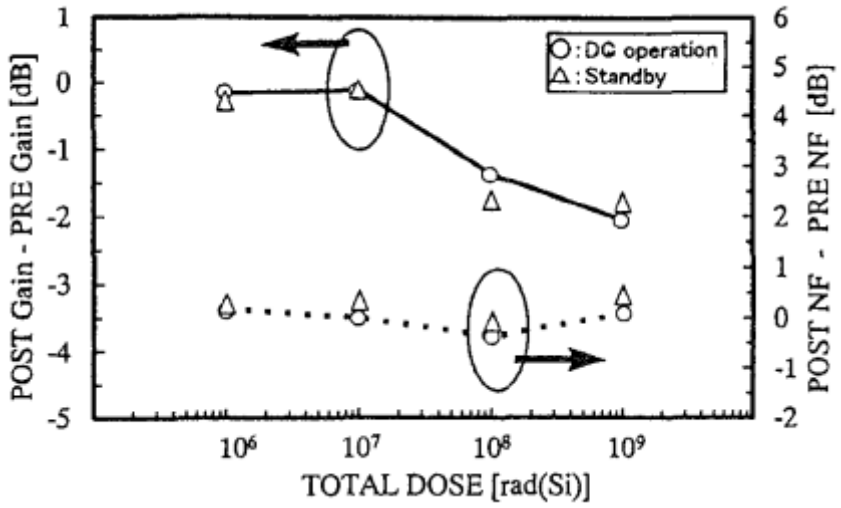


Figure 2.268: Post and pre-radiation gain and NF of a PHEMT LNA under total dose radiation [65]

As stated before, SiGe devices are naturally invulnerable to radiation. An SiGe LNA performance under 6.7 Mrad proton radiation is shown in Figure 2.29. It is observed that this LNA is nearly not affected by radiation. However, there is another study that state gain of SiGe LNA degrades with radiation of 1 Mrad X-ray. (Figure 2.30)

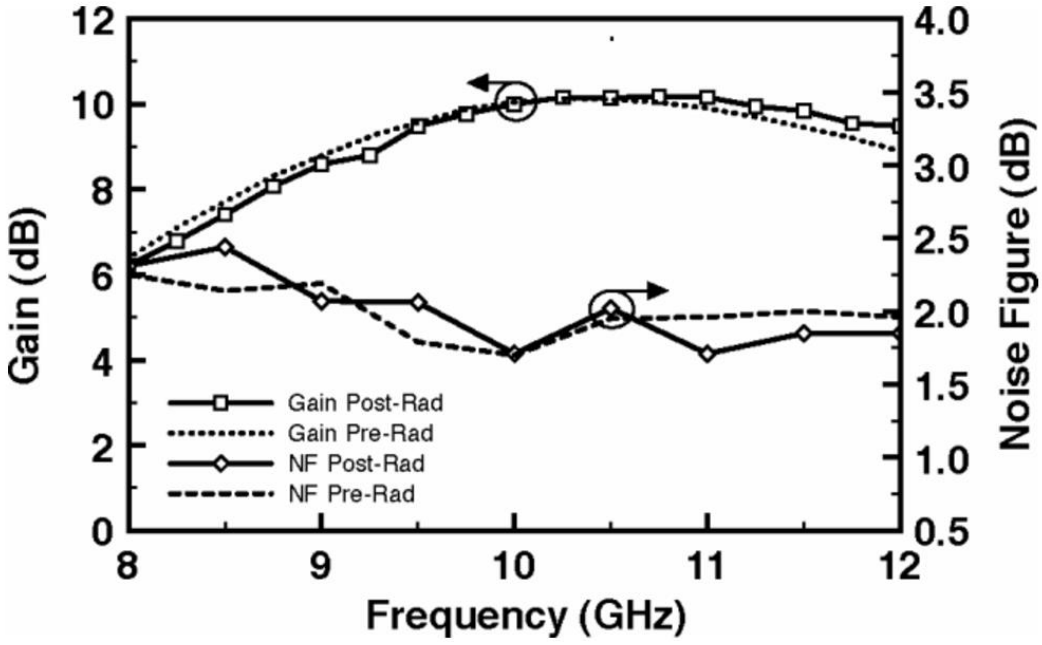


Figure 2.29 : Post and pre-radiation gain and NF of a SiGe LNA under total dose radiation [68]

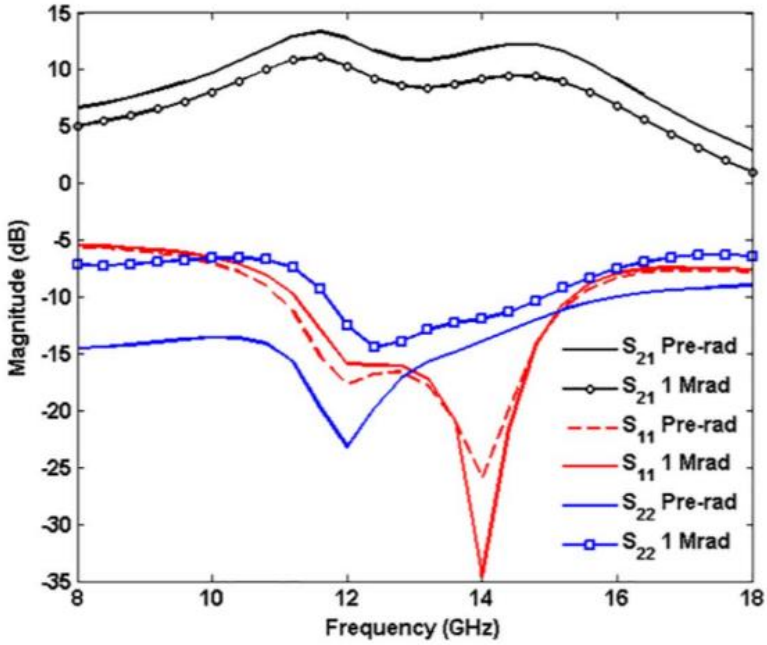


Figure 2.30 : Post and pre-radiation gain and NF of a PHEMT according to total dose [69]

Examination of CMOS LNAs under radiation is not performed to the author's knowledge. Nonetheless a study states that CMOS LNAs that are designed with NMOS devices of annular layout (a different name of ELT or octagonal shaped ELT) are naturally durable to 500 Krad [54]. Figure 2.31 indicates that the noise figure and gain of an annular NMOS LNA at pre-radiation and post-radiation is nearly the same.

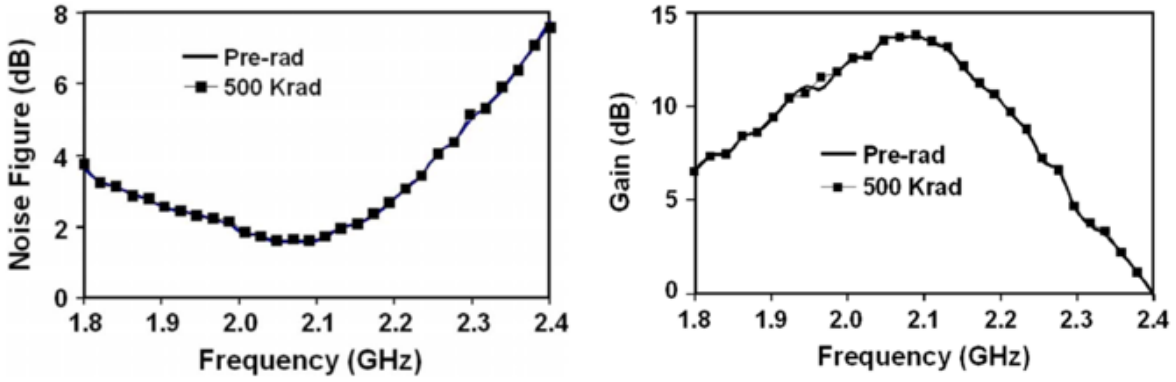


Figure 2.31 : Gain and noise figure of a 0.13 um CMOS LNA using annular devices at pre and post-radiation [54]

3. LOW NOISE AMPLIFIER DESIGN

3.1 Introduction to LNA Concept

Low noise amplifier (LNA) is first critical stage of the receiver circuits. A superheterodyne receiver circuit, as explained in the first chapter and seen in Figure 1.1., consists of an antenna, an RF filter, a low noise amplifier, a mixer and by a voltage controlled oscillator (VCO). The role of the LNA in this system is to amplify the signal by adding minimum noise. As (1.1) illustrates, the overall noise figure of the system is dominated by the noise figure of the LNA. While presenting the minimum noise figure possible, low noise amplifiers should also have a high gain to amplify the weak signals received, to reduce the noise contiributions of the following stages. Moreover, because they are located in the system right after the antenna, their input impedance should be matched to the antenna impedance to avoid reflections at the input. Powerful reflection waves at the input of the LNA can cause LNA and system to be unstable.

Low noise amplifiers are used nearly in every communication system, and space communications is one of them. LNAs that are going to be used for space communications and radio astronomy should have specific features in addition to the explained properties earlier such as radiation robustness. They also should be able to work at cryogenic temperatures.

In this thesis, UMC 180 nm technology is used to design a 7 GHz Low Noise Amplifier (LNA). This LNA is designed for test purposes at room temperature and cryogenic temperature of 80 K as well as under radiation. Firstly, transistors of the available technology are examined, and cut-off frequency and noise figure performances are reviewed through simulations. Since LNAs are one of the most critical building blocks of receiver systems, their optimization is a thoroughly deliberated topic. In light of the previous studies, optimization steps are shown through simulations, and their comparison is done with the theoretical foundations which demontrates how far theory works in the design.

After investigation of transistors, a classical cascode topology is assembled and optimum noise match is achieved. Subsequently, input power match is sought out while achieving the least degradation in noise figure. At this point in design, gain of the LNA is also protected by the designer not to move away from the desired value.

After achieving the desired design parameters with ideal elements, the next step is the realization of inductors. Simulations are conducted to improve the design. Layout issues are briefly discussed and the design is finalized with post layout simulations. Literature survey shows that the design is comparable with the most recent research body.

Low noise amplifier design is studied extensively in the literature. In this chapter, it is aimed to clarify the formulas and underlying theory with simple simulations and finalize the design with a step-by-step LNA design methodology. As stated before, noise is the most important design parameter that leads the name to the circuit LNA, so firstly a brief explanation of noise will be provided. Design methodology will be based on this theory.

3.2 Theory of LNA Design

Low noise amplifiers are used to amplify the signal with minimum noise degradation. However, to amplify a signal with minimum noise degradation, there are more important contraints that should be satisfied such as the input reflection and stability. For the LNA in this thesis output reflection is also important because if there are strong reflection waves at the input and output of the LNA, those can cause instability. If there were a mixer following the LNA, output reflection were not going to be the issue of this design [27]. Hence, we will investigate the noise, gain, input and output reflections, reverse isolation and the stability of the designed LNA.

3.2.1 Noise of LNA

It is important to define the terminology that is common in LNA design. Noise factor (F) is a measure of a system's noise degradation in terms of signal-to-noise ratio [27]. Signal-to-noise ratio (SNR) is defined as the ratio of average signal power to average noise power in a particular bandwidth.

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{3.1}$$

Noise factor is ratio of the input SNR to output SNR [9].

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{3.2}$$

Noise figure is equal to the noise factor given in decibels.

$$NF = 10\log(F) \tag{3.3}$$

Classical two port noise theory gives us a good understanding of the noise contribution of any two port linear system, which is the case for our amplifier. Extensive analysis of noise in linear two ports are done in [3] by Haus et al yielding (3.9).

A noisy two port can be modeled by a noiseless two port and two noise sources in the input which are $\overline{e^2}$ and $\overline{i^2}$ as in Figure 3.1. Noise is modeled with two sources in the form of a noise voltage and a noise current, and they are in correlation with each other. This expression helps for any situation, for example, if the input of the amplifier is shorted the noise current is also shorted out but noise is represented with the voltage source, and similarly if the input is open circuited, the noise voltage is canceled out, but noise is represented by the noise current [27].

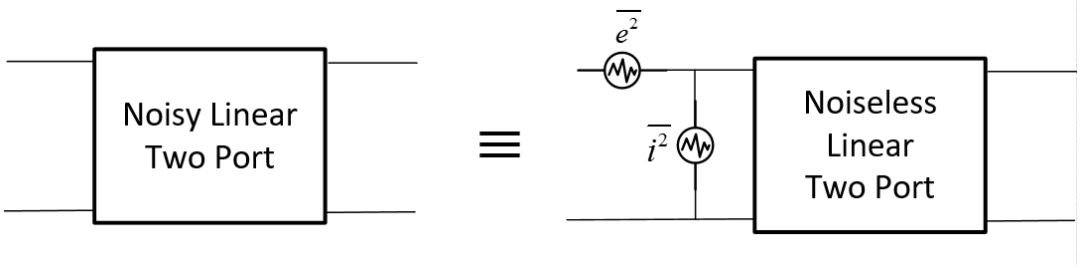


Figure 3.1 : Noisy two port modelling

Another definition is noise figure is the ratio of total output noise to output noise due to the source as in (3.4). i_s is source noise, Y_s is source admittance and i and e are the noise current and noise voltage of the noisy linear two port respectively. Calculation is done with currents, thus noise voltage multiplied with Ys translates to a current quantity.

$$F = \frac{i_s^{\,2} + \left|i + Y_s.e\right|^2}{i_s^{\,2}} = 1 + \frac{\left|i + Y_s.e\right|^2}{i_s^{\,2}} \tag{3.4}$$

Assuming internal noise and source noise is uncorrelated and separating uncorrelated and correlated parts of noise current as i_u and $i\text{-}i_u = Y_\gamma.e$ respectively, equation is derived to (3.5) where Y_γ is the correlation admittance.

$$F = \frac{i_u^{\,2} + \left|Y_s + Y_\gamma\right|^2 \cdot e^2}{i_s^{\,2}} \tag{3.5}$$

Since $\overline{i_u^{\,2}} = 4kT_0G_u\Delta f$, $\overline{i_s^{\,2}} = 4kT_0G_s\Delta f$, $\overline{e^2} = 4kT_0R_n\Delta f$, $Y_s = G_s + jB_s$ and $Y_\gamma = G_\gamma + jB_\gamma$ noise figure further calculated as (3.6) where G_u is uncorrelated noise conductance and R_n is the equivalent noise resistance of the two-port network.

$$F = \frac{G_u + R_n.\left[(G_s + G_\gamma)^2 + (B_s + B_\gamma)^2\right]}{G_s} \tag{3.6}$$

The purpose of this calculation is the extraction of optimum source admittance which is $Y_{opt} = G_{opt} + jB_{opt}$. Optimum source admittance is the source admittance value that makes noise figure minimum which is F_{min}. Source conductance G_s and source susceptance B_s that achieves minimum noise figure, gets the derivation of noise figure to zero.

$$\frac{\delta F}{\delta B_s} = 0 \xrightarrow{gives} B_{opt} = B_s = -B_\gamma \tag{3.7}$$

$$\frac{\delta F}{\delta G_s} = 0 \xrightarrow{gives} G_{opt} = G_s = \sqrt{\frac{G_u + R_n G_\gamma^2}{R_n}} \tag{3.8}$$

Consequently, noise figure of linear two port network is obtained as

$$F = F_{\min} + \frac{R_n}{G_s}[(G_s - G_{opt})^2 + (B_s - B_{opt})^2] \tag{3.9}$$

where minimum achievable noise factor F_{min} is

$$F_{\min} = 1 + 2R_n \left[G_{opt} + G_c \right] \tag{3.10}$$

As seen in (3.9), for optimum source admittance (Y_{opt}) second term cancels out, bringing down noise factor (F) equal to minimum achievable noise factor (F_{min}) as in (3.10).

Since the design will be done using MOS transistors, a brief examination of MOS noise parameters is helpful. Noise can be defined as any interfering signal other than the desired signal. To be more specific, noise is the manifestation of random motion of particles due to their thermal energy. Electronic circuits generate noise through the random motion of charge carriers during conduction. As indicated before, LNAs are designed to amplify the signal with minimum noise contribution. Thus, MOSFETs in LNA design must be carefully examined for their noise performance. The MOSFET noise sources are generally considered in two parts as channel thermal noise and induced gate noise [2]. MOSFET noise model is given in Figure 3.2.

1. Channel thermal noise, $\overline{i_d^{\,2}}$ stems from the charge carriers in the channel constituting the device current. Hot electrons within those charge carriers causes channel thermal noise.

$$\overline{i_d^{\,2}} = 4kT\gamma g_{do} \tag{3.11}$$

In (3.11), k is the Boltzmann constant ($1,38\times10^{-23}$ J/K), T is the absolute temperature in Kelvin, g_{do} is the zero-bias drain conductance and γ is the coefficient of the channel thermal noise whose value varies for long channel devices between 2/3 and 1. However, for short channel devices in saturation γ is greater than 2/3 [5-8].

2. Induced gate current noise, $\overline{i_g^{\,2}}$ which is caused by the fluctuations in the channel ending up as a physical noise current in the gate.

$$\overline{i_g^{\,2}} = 4kT\delta g_g \tag{3.12}$$

where,

$$g_g = \frac{\omega^2 C_{gs}{}^2}{5 g_{do}} \tag{3.13}$$

δ being the coefficient of gate noise. For long channel devices it is equal to 4/3. g_g is the high frequency non-capacitive value of gate impedance. These noise currents are correlated with each other through the correlation coefficient *c*.

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g{}^2}\,\overline{i_d{}^2}}} \tag{3.14}$$

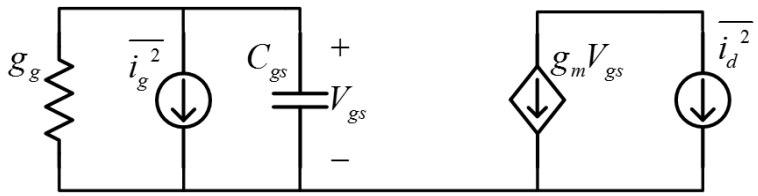


Figure 3.2 : MOS noise model

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta\left(1 - |c|^2\right)} \tag{3.15}$$

In the analysis of the two port network, the minimum achievable noise factor, its expression and the optimum source admittance are investigated. If these expressions are represented with the MOS transistor parameters and circuit parameters, a design methodology for the optimum noise factor can be defined. The detailed analysis of the noise parameters for MOS transistors are done in [11] yielding expressions in (3.4) for F_{min}, G_{opt}, B_{opt} and R_n in (3.15), (3.16), (3.17) and (3.18) respectively.[1]

[1] In these calculations, input impedance of the MOS transistor is assumed to be completely capacitive which is very acceptable for frequencies well below ω_T. Additionally, distributed gate noise is neglegted. Consequently, these approximations and expressional results describe the noise performance of MOS transistors and aid the designers.

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}\left(1-|c|^2\right)} \tag{3.16}$$

$$B_{opt} = -\omega C_{gs}\left(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{3.17}$$

$$R_n = \frac{\gamma g_{do}}{g_m{}^2} = \frac{\gamma}{\alpha}.\frac{1}{g_m} \tag{3.18}$$

with α being

$$\alpha = \frac{g_m}{g_{d0}} \tag{3.19}$$

These equations above show that the noise factor of a MOS transistor depends on the device size which sets C_{gs} as in (3.20),

$$C_{gs} = \frac{2}{3}WLC_{ox} \tag{3.20}$$

and the bias point which determines g_m as in (3.21) and ω_T as in (3.22).

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)I_D} = \frac{2I_D}{V_{GS}-V_T} \tag{3.21}$$

$$w_T = \frac{g_m}{C_{gs}} \tag{3.22}$$

The classical cascode topology with inductive emitter degeneration gives the optimum noise figure performance in accordance with the input matching [2]. Thus, we continue our minimum noise figure design approach by assembling the inductive degenerated MOS as given in Figure 3.3.

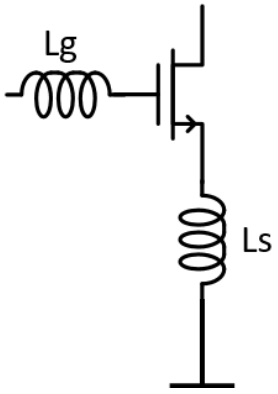


Figure 3.3 : Inductively degenerated MOS transistor

As explained above and understood from the formulas (3.15) through (3.22), noise factor (*F*) as well as noise figure (*NF*) are functions of the drain current density. Hence, minimum achievable NF_{min} value depends on the drain current density and the size of the transistor. NF_{min} is the noise figure of the transistor when the optimum source impedance is presented at the input. Since the source impedance is standard, in the design of LNAs, we try to generate the optimum source admittance to 50 Ω so that the noise match is accomplished. In the design methodology, firstly the drain current density and the width of the transistor is chosen to get the minimum NF_{min} value. Secondly, inductances should be choosen such that *NF* converges NF_{min}.

In general, inductive degeneration is used to simultaneously achieve the input power match and the optimum noise match [2]. It is emphasized in [12] that the noise figure of an LNA depends on the design of the amplifying MOS transistor and the losses of the input network. However, the value of degeneration inductance changes the noise figure, because inductive degeneration also effects the transconductance of the amplifier as in (3.23). Previous research studies show that as L_s increases, F_{min} increases as well [26].

$$G_m = \frac{g_m}{1 + g_m R_S} \tag{3.23}$$

As stated in [2], *"A minimum F exists for a particular* Q_L*"* meaning that *F* can be optimized with gate and source inductors which can be found using the equations (3.24), (3.25) and (3.26).

$$F = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right) \tag{3.24}$$

$$\chi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L{}^2) \tag{3.25}$$

$$Q_L = \frac{\omega_0\left(L_s + L_g\right)}{R_s} = \frac{1}{\omega_0 R_s C_{gs}} \tag{3.26}$$

In conclusion, noise figure of an LNA is optimized through the steps below:

Step 1: Determine the drain current density and the size of the amplifying transistor according for minimum NF_{min}.

Step 2: Determine L_s and L_g to equalize NF and NF_{min}. L_g is used to bring optimum source susceptance to zero.

While optimizing the noise figure, one must consider the input matching and the gain. Input network of an LNA should be optimized both for its noise figure and its input matching.

3.2.2 Input power matching of LNA

Today most used LNA topology is the cascode topology. To suppress leakage from output to the input of the LNA, a high reverse isolation is necessary [27]. Common gate transistor, which is cascaded to the common source transistor, reduces the feedback from output due to smaller parasitic drain-to-source capacitance compared to the gate-to-drain capacitance [57]. Thus, a basic LNA is provided in Figure 3.4. The next goal is to achieve input match without degrading the noise figure. The input impedance of a classical cascode LNA can be given as in (3.27).

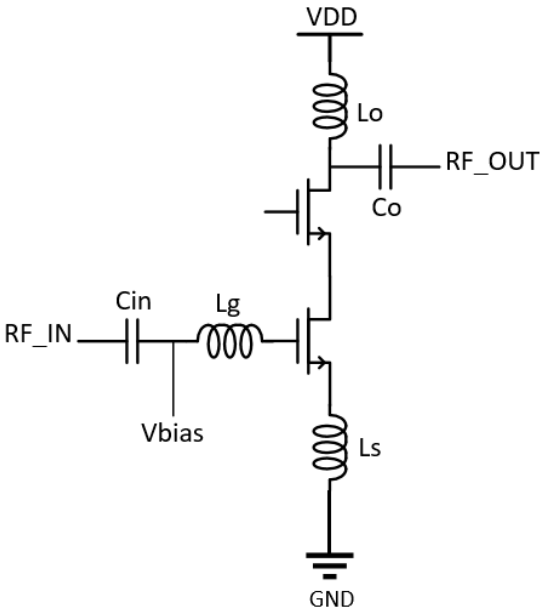


Figure 3.4 : Classical cascode topology with inductive degeneration

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \tag{3.27}$$

At the resonance frequency $\omega_0 = \sqrt{\frac{1}{(L_g + L_s)C_{gs}}}$ the input impedance depends only on the cut-off frequency and L_s as in (3.27). Thus, it is observed the input power match is achieved with L_s and L_g at the desired frequency.

$$\mathrm{Re}\{Z_{in}\} = \omega_T L_s \tag{3.28}$$

Nevertheless, the value of L_s that gives the optimum input resistance could be large and decrease the gain. Therefore, if we use an additional inductance at the input which is put between the bias node and the input node as in Figure 3.5, a better input match and a higher gain can be obtained. Shunt inductance L_b in Figure 3.6 increases the impedance Z'_{in}, thus

resulting in higher Z_{in} with lower $\omega_T L_s$. Now we can choose a lower L_s to yield a lower noise figure and higher gain, with better input match simultaneously.

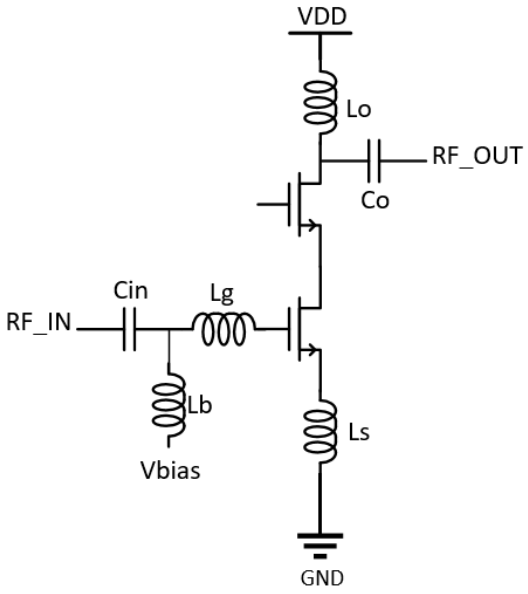


Figure 3.5 : Classical cascode topology with inductive degeneration and inductive bias

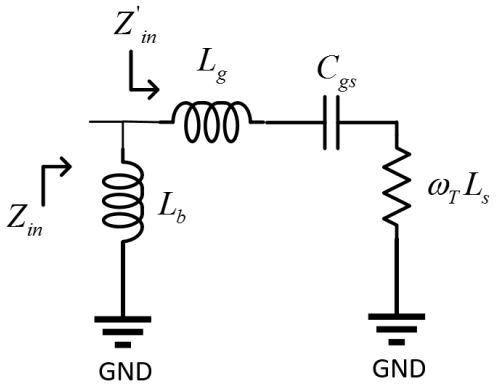


Figure 3.6 : Input matching circuit with L_b

Z_{in} was given in (3.26) before. We rename it as Z'_{in} with Z_{in} being calculated as in (3.30)

$$Z'_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \qquad (3.29)$$

$$Z_{in} = \frac{Z'_{in} s L_b}{Z'_{in} + s L_b} \tag{3.30}$$

Calculation of Z_{in} ends up with complex equations (3.31) and (3.32) that indicates that real and imaginary parts of Z_{in} impedance depends directly on L_b inductance but does not demonstrates the effect of L_b clearly. Thus, using the formulas given in (3.29) and (3.30), impact of L_b, L_s and L_g has been separately investigated by sweeping these values in MATLAB. Real and imaginary parts of input impedance are drawn for different values of L_b, L_s and L_g in Figure 3.7 and Figure 3.8 respectively. Since equations include many assumptions, MATLAB calculations do not yield inductance values that exactly match real component values. However, they indicate that L_b can be used to increase the input impedance. These figures are drawn for the L_b values of interest. As L_b increases it acts as a very large impedance at 7 GHz and the curves settle to the values when input node, that L_b is connected, is open circuit. When L_b is not connected, it is assumed that an infinite impedance is shunted to that node. When there is L_b in that node as seen in Figure 3.22, this shunt impedance is lowered. As seen from Figure 3.7, lowering the impedance of L_b firstly increases the real part of the input impedance, but then starts to lower it down. Hence one can choose an appropriate value for L_b through simulations.

Also we see that lower L_s values along with lower L_b values yield higher increase in impedance. This characteristic enables us to get higher gain, lower noise and input power match simultaneously.

$$\mathrm{Re}\{Z_{in}\} = \omega^2 g_m L_b \frac{(L_b - L_s)\left(1 - \omega^2 C_{gs} L_g\right) + \omega^2 C_{gs} L_s}{1 + \omega^2\left[g_m{}^2 L_b{}^2 - 2C_{gs}\left(L_g + L_s + L_b\right)\right] + \omega^4 C_{gs}{}^2\left(L_g + L_s + L_b\right)^2} \tag{3.31}$$

$$\mathrm{Im}\{Z_{in}\} = \omega L_b \frac{1 + \omega^2\left[g_m{}^2 L_b L_s - C_{gs}\left(L_g + 2L_s\right)\right] + \omega^4 C_{gs}{}^2\left(L_g + L_s\right)\left(L_g + L_s + L_b\right)}{1 + \omega^2\left[g_m{}^2 L_b{}^2 - 2C_{gs}\left(L_g + L_s + L_b\right)\right] + \omega^4 C_{gs}{}^2\left(L_g + L_s + L_b\right)^2} \tag{3.32}$$

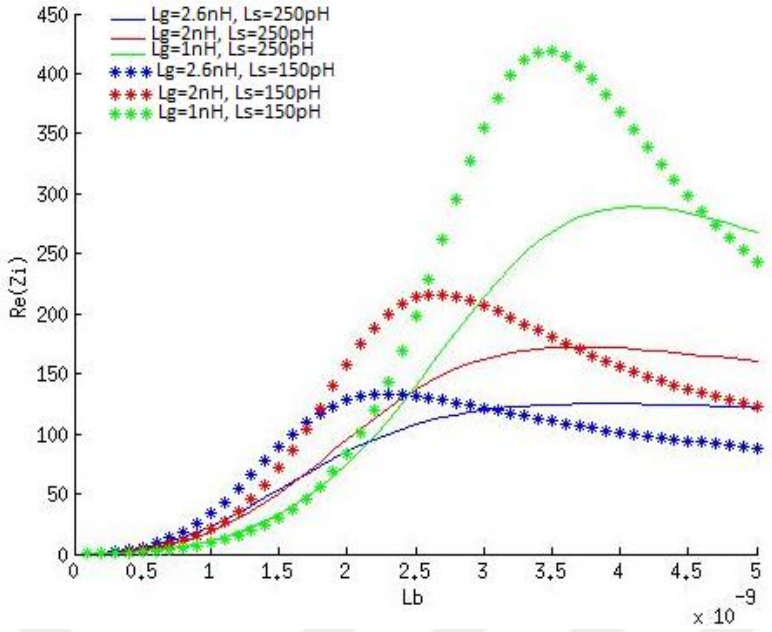


Figure 3.7 : Real part of Z_{in} with different L_b , L_s and L_g values.

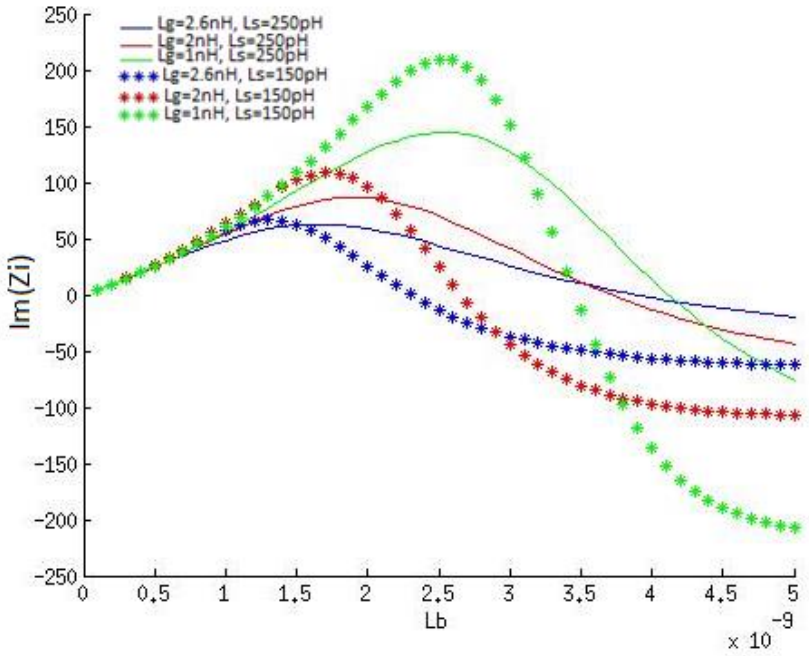


Figure 3.8 : Imaginary part of Z_{in} with different L_b , L_s and L_g values.

3.2.3 Power gain and output power matching of LNA

Voltage gain of an LNA is the multiplication of equivalent transconductance and output resistance as in (3.33). Equivalent transconductance can be derived from simplified schematic of an inductively degenerated common source stage as in Figure 3.9 [27].

$$A = G_m R_L \tag{3.33}$$

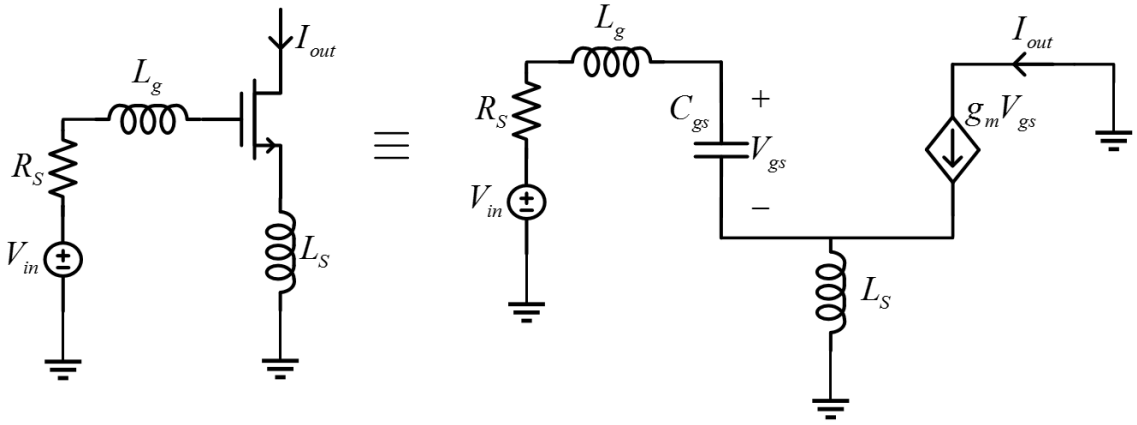


Figure 3.9 : Input network of inductively degenerated cascode LNA topology

Equivalent transconductance (G_m) is the division of output current I_{out} to input voltage V_{in}. Hence, V_{in} and I_{out} should be extracted in terms of the components of the circuit in Figure 3.9. Output current is equal to the multiplication of transconductance and gate-to-source voltage of the transistor as in (3.34). Voltage drop over source inductance (3.35), source resistance and gate resistance summed with gate-to-source voltage is equal to input voltage V_{in}. Derivation is simplified with the aid of the resonance at ω_0 which cancels out $\left[1+sC_{gs}\left(sL_g+sL_S\right)\right]$ term. Resonance frequency is determined by gate-to-source capacitance and source and gate inductances as in (3.37). Definition of V_{in} further simplified with the help of the equations given in 3.35, concluding the equivalent transconductance value as in (3.40).

$$I_{out} = g_m V_{gs} \tag{3.34}$$

$$V_{Ls} = s(g_m V_{gs} + sC_{gs} V_{gs}) L_S \tag{3.35}$$

$$
\begin{aligned}
V_{in} &= (R_S + sL_g)sC_{gs}V_{gs} + sL_S(I_{out} + sC_{gs}V_{gs}) + V_{gs} \\
&= V_{gs}\left[1 + sC_{gs}\left(R_S + sL_g + sL_S\right)\right] + sL_S I_{out} \\
&= \frac{I_{out}}{g_m}\left[1 + sC_{gs}\left(R_S + sL_g + sL_S\right)\right] + sL_S I_{out} \\
&= \frac{I_{out}}{g_m}\left[sC_{gs}R_S\right] + sL_S I_{out} \;@\; \omega_0 \\
&= \frac{I_{out}}{g_m}\left[j\omega_0 C_{gs}R_S\right] + j\omega_0 L_S I_{out} \\
&= I_{out} j\omega_0\left[\frac{C_{gs}R_S}{g_m} + L_S\right]
\end{aligned}
\tag{3.36}
$$

$$
\omega_0^{\,2} = \frac{1}{C_{gs}(L_g + L_S)} \tag{3.37}
$$

$$
\frac{g_m L_S}{C_{gs}} = R_S \;\&\; \frac{g_m}{C_{gs}} = \omega_T \tag{3.38}
$$

$$
\begin{aligned}
\frac{I_{out}}{V_{in}} &= \frac{g_m}{j\omega_0\left[C_{gs}R_S + g_m L_S\right]} \\
&= \frac{g_m / C_{gs}}{j\omega_0\left[R_S + g_m L_S / C_{gs}\right]} \\
&= \frac{\omega_T}{j\omega_0 2R_S}
\end{aligned}
\tag{3.39}
$$

$$
G_m = \left|\frac{I_{out}}{V_{in}}\right| = \frac{\omega_T}{2\omega_0 R_S} \tag{3.40}
$$

After the derivation of equivalent transconductance voltage gain can be redefined as in equation (3.41) which indicates that the gain is dependent on the output impedance, operating frequency and the source inductance. If this LNA was going to be a part of a receiver system which is followed by a mixer, output matching to 50 Ω was not necessary and meaningful [27]. Since we are going to measure this LNA using a probe station, we require power match at the output

as we did in input, thus output impedance is 50 Ω. Cut-off frequency ω_T and operating frequency ω_0 cannot be changed since the former is strongly technology dependent and the latter is chosen for space applications. Consequently, the designer is left with an only choise of reducing the the source inductance to increase the gain.

$$A = \frac{\omega_T R_L}{2\omega_0 L_S} \tag{3.41}$$

Output matching of the cascode is managed with the output inductor L_O and output capacitor C_O. Output circuit can be simplified as in Figure 3.10 and Z_{out} is calculated as in (3.42). Real and imaginary parts of output impedance are derived as (3.43) and (3.44). These equations indicate that C_O is used to cancel out imaginary part at the operating frequency ω_0 and R_O and L_O adjust the real part to 50 Ω. This derivation shows that Z_{out} can be arranged to be purely resistive and equal to 50 Ω, with the aid of L_O and C_O.

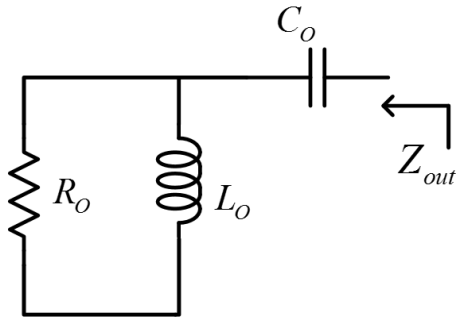


Figure 3.10 : Simplified schematic of output tank

$$Z_{out} = \frac{j\omega L_O + R_O - \omega^2 R_O L_O C_O}{j\omega R_O C_O - \omega^2 L_O C_O} \tag{3.42}$$

$$\mathrm{Im}\{Z_{out}\} = j\left(\frac{\omega^2 {R_O}^2 L_O C_O - {R_O}^2 - \omega^2 {L_O}^2}{\omega C_O\left({R_O}^2 + \omega^2 {L_O}^2\right)}\right) \tag{3.43}$$

$$\mathrm{Re}\{Z_{out}\} = \frac{R_O {L_O}^2}{\frac{{R_O}^2}{\omega^2} + {L_O}^2} \tag{3.44}$$

3.3 LNA Design and Simulation Results

Theory of the LNA design has been examined in the previous section. This section provides the details of the design of an LNA operating at 7 GHz. Methodology of this design can be organized as below and shown graphically in Figure 3.10.

- Examination of available transistors
    - f_T simulations: choosing the channel length of cascode transistor
    - NF_{min} simulations: choosing the optimum current density and number of fingers to get minimum NF_{min}
- Noise matching of the amplifying MOS transistor: choosing L_s and L_g appropriately
- Input matching for the cascode topology with little degradation in noise: optimizing L_s, L_g along with L_b
- Design and characterization of inductors to be used in the design
- Further simulations using the designed inductor models and optimization of inductance values more accurately
- Layout floorplanning
- Characterization of inductors and RF paths in the layout floorplan and further optimization of inductance values, RF paths and floorplan by considering post-layout simulations
- Finalizing the layout

3.3.1 Examinations of transistor characteristics

The design of LNA begins with the feasibility of available MOS transistors. As seen in (3.24), noise factor directly depends on ω_T of the device. Henceforth, we will start with ω_T examination of available transistors.

UMC 180 nm mixed-mode and RF technology is used for the LNA design. UMC 180 nm technology has four different RF NMOS devices and four different RF PMOS devices. We are interested in NMOS devices so we examined two of these RF NMOS devices which are 1.8 V

devices. Other RF NMOS transistors were 3.3 V devices which will not be used. First RF NMOS device is named as N_L18W500_18_RF and has a constant channel length of 180 nm and a constant finger width of 500 nm. Its only reconfigurable parameter is the finger which can vary from 5 to 21. The other RF NMOS device is named as N_PO7W500_18_RF and has a constant finger width and number. Its length can be changed from 200 nm to 500 nm.

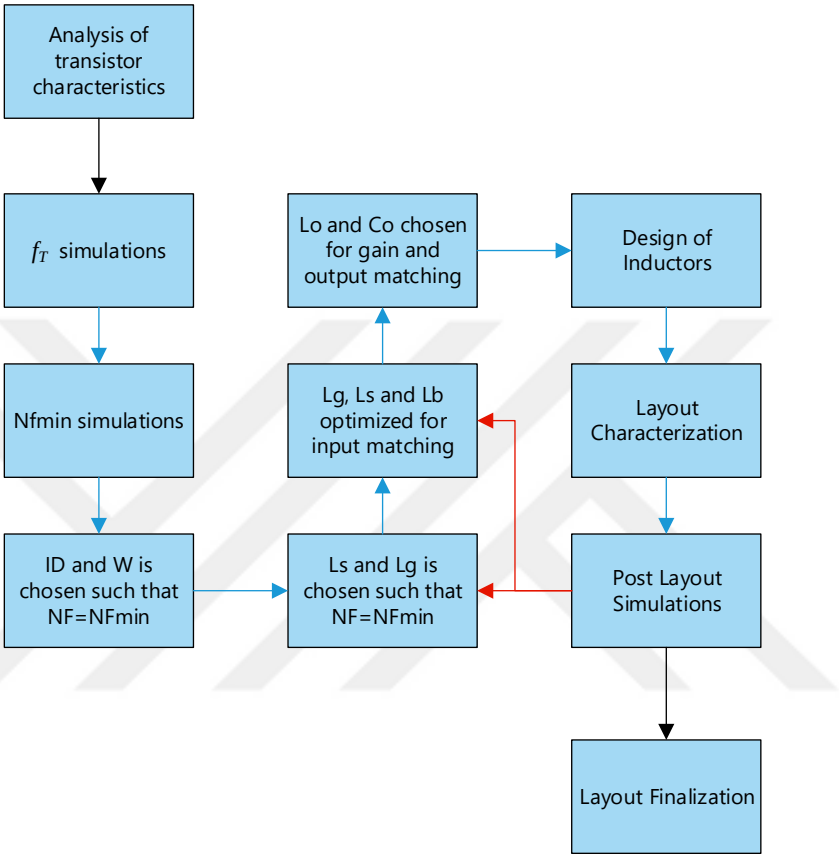


Figure 3.10 : LNA design methodology flow chart

3.3.1.1 Cut-off frequency (f_T) calculation and simulations

Cut-off frequency (f_T) is the frequency at which the current gain of the transistor falls to 1. Extensive analysis of the LNA noise figure for the cascode topology shows that the noise figure of the LNA strictly depends on the cut-off frequency of the transistor as defined in (3.45) [2],

$$F = 1 + \frac{R_g}{R_s} + \gamma g_{do} R_s \left(\frac{f_0}{f_T}\right)^2 \qquad (3.45)$$

where R_g is gate resistance of the NMOS.

Cut-off frequency of a MOS transistor is simply formulated as in (3.22). As transistor channel lengths are scaled down and smaller transistor gate lengths are possible, transconductance (g_m) of transistors increase as gate-to-source capacitances become smaller. Thus the cut-off frequency of the transistor increases, resulting in reduced noise figure.

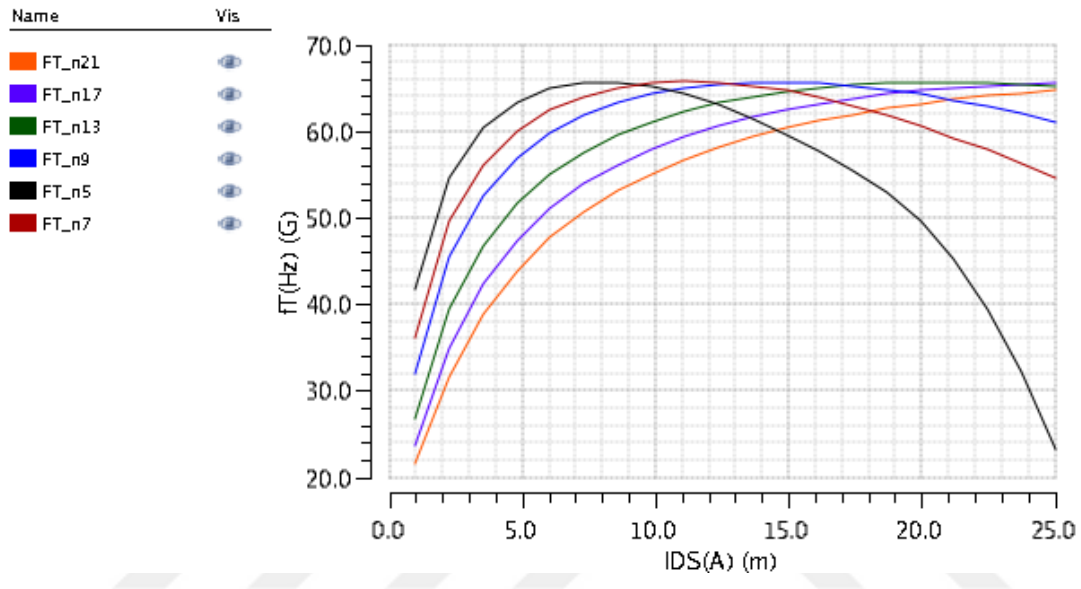


Figure 3.11 : f_T vs. I_{DS} graph of N_L18W500_18_RF with different finger number values

In the light of information above, cut-off frequency of available transistors is simulated for 180 nm UMC technology as in Figure 3.11. Finger number values were changed from 5 to 21 and the drain current of transistors were changed from 1 mA to 25 mA. As the finger number increases, cut-off frequency of the transistor decreases with the current being kept constant. Cut-off frequency of transistors with few number of fingers decreases as the drain current rises. However, with more number of fingers, cut-off frequency of transistor tends to increase with increasing drain current.

Higher gain and lower noise figure is achievable with higher cut-off frequency but other problems arise as the current increases and the number of finger decreases. Further simulations will impose a tight limit on the selection of these parameters.

Table 3.1 : Cut-off frequency and drain current relations of NMOS Transistor at 7 GHz

Number of Finger	I_{DS}@ f_{Tmax} (mA)	f_{Tmax} (GHz)	f_T@7mA (GHz)
5	8	65.6	65
7	11	65.6	63
9	14.6	65.6	61
13	21	65.6	57
17	26	65.6	53
21	32	65.5	50

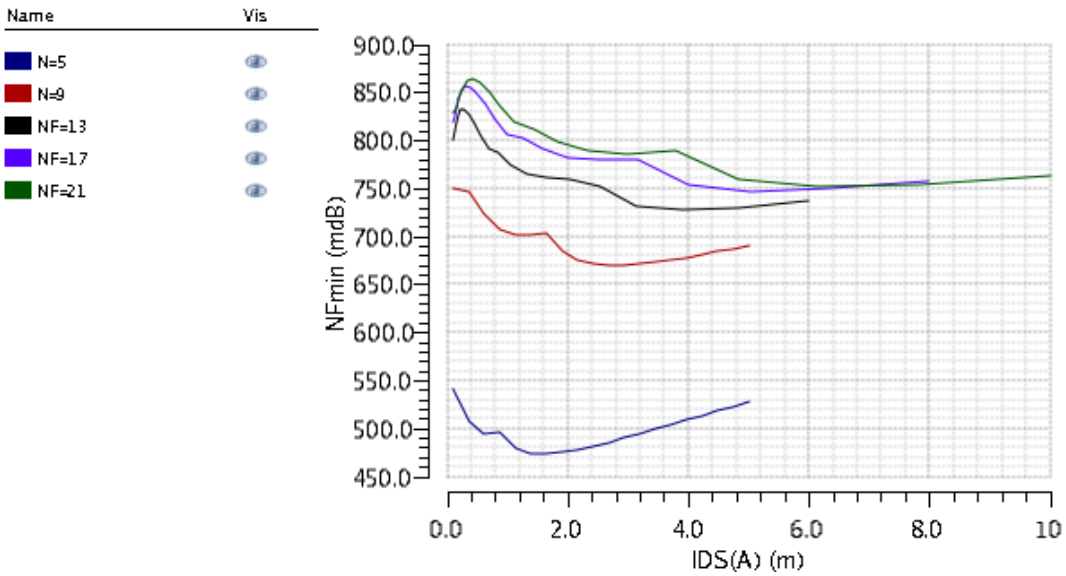


Figure 3.12 : *NF_{min}* vs. *I_{DS}* graph of N_L18W500_18_RF with different finger number values at 7 GHz

Table 3.2 : Noise Parameters and Bias Points of NMOS Transistor at 7 GHz

Number of Fingers	Multiplicity	I_{DS} (mA)	NF_{min} (dB)	R_{opt} (Ω)	NF (dB)	V_{ov} (V)
5	1	1.6	0.475	2400	5.7	0.28
21	1	7	0.75	370	2.48	0.28
21	2	13	0.75	183	1.9	0.27
21	3	20	0.75	122	1.9	0.28
21	4	26	0.75	91	2	0.27

Table 3.2 indicates that the first row yields the best NF_{min} value. That is to say, if the source impedance is matched to the noise impedance, noise figure as low as 0.475 dB can be achieved. However, the R_{opt} is 2400 Ω for this row and bringing this value down to 50 Ω is very difficult. Moreover, if the second row is investigated, increasing the number of finger reduces R_{opt} to 370 Ω, which is much more achievable despite the cost of increasing NF_{min} to 0.75 dB. It should be noted that, *NF* values in Table 3.2 is in accordance with R_{opt} because the source impedance is 50 Ω in these simulations and *NF* decreases as R_{opt} converges to 50 Ω. Based on these observations, device current and the number of fingers have been chosen 7 mA and 21 respectively to get minimum noise figure possible and appropriate power consumption. Overdrive voltage (V_{ov}), the difference of the gate voltage and threshold voltage of the transistor, is given in the Table 3.2 for NF_{min} simulations.

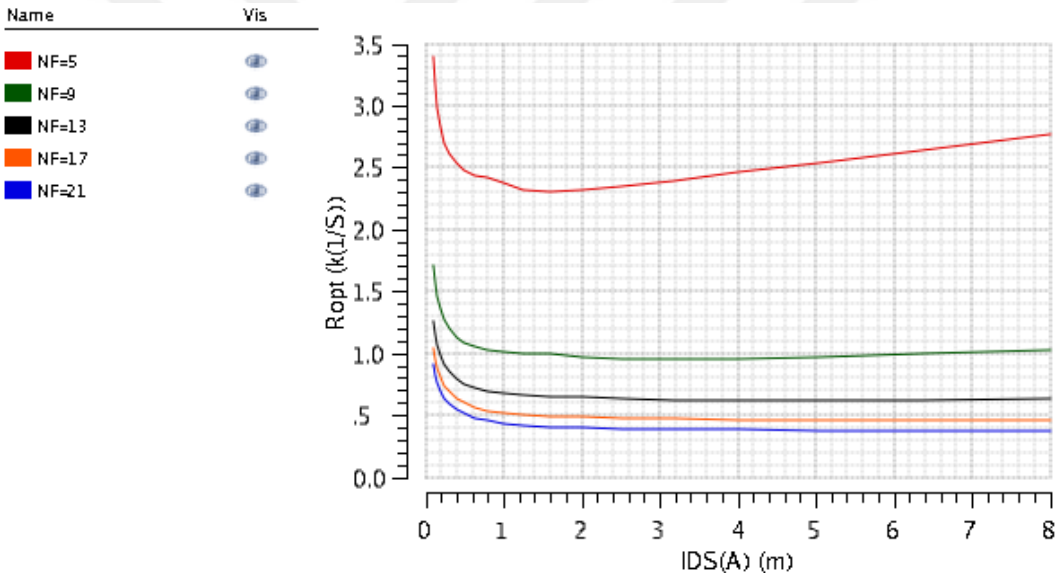


Figure 3.13 : Ropt vs. I_{DS} graph of N_L18W500_18_RF with different finger number values

3.3.2 Design for minimum noise figure and input match

Design for minimum noise figure has been discussed in Section 3.2.1. This section includes the simulations that were done to determine the component values. As explained before the classical cascode topology with inductive emitter degeneration yields the optimum noise figure performance in accordance with its input matching [2]. As shown in Figure 3.4 Lg and Ls are used to obtain the optimum source impedance as 50 Ω.

3.3.2.1 L_s optimization

For the optimum noise match, source degeneration inductance can be used. In the following simulations gate series inductance Lg is neglected. Ls value for the optimum noise match can be selected in a process depicted in Figures 3.14 through 3.17. Figure 3.14 shows that to get to NF_{min}, Ls should be chosen as 100 pH; however, in order to make R_{opt} 50 Ω, Ls should be chosen bigger than 1 nH as shown in Figure 3.15. Thus, NF_{min} and R_{opt} depend oppositely on L_S. These relationships yield the optimum *NF* at L_S*=450 pH* as illustrated in Figure 3.16 and 3.17.

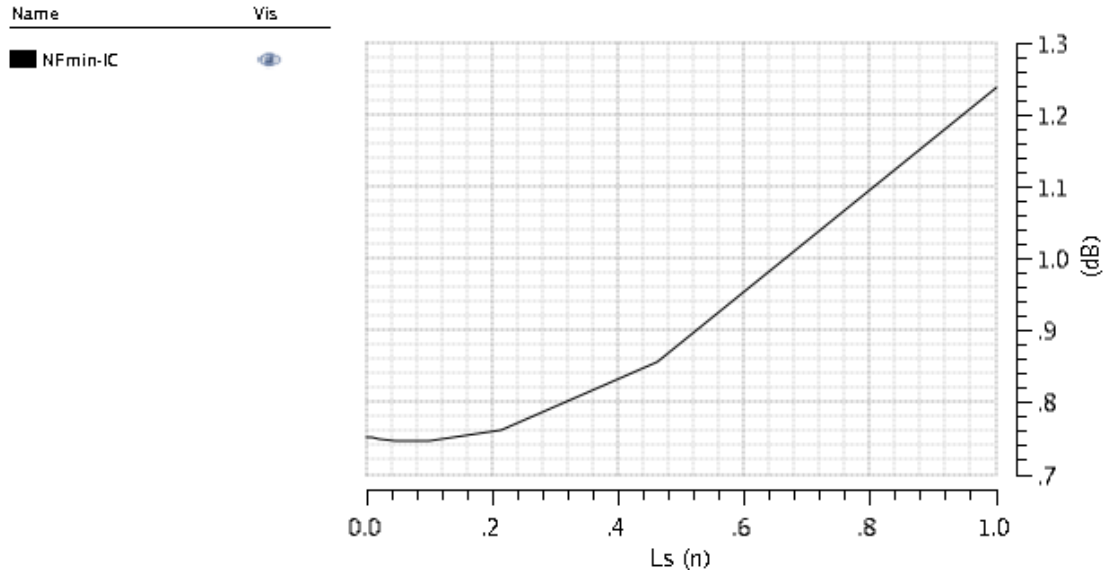


Figure 3.14 : NF_{min} values with regards to Ls

If we look in a closer projection, we see that *NF* value does not change much. If *Ls=0, NF=2.4 8dB, Ls=100 pH, NF=2.42 dB,* for *Ls=200 pH, NF=2.36 dB,* for *Ls=300 pH, NF=2.32 dB, Ls=400 pH, NF=2.31 dB*. Its effect on the *NF* get weaker for the higher values. Thus, choosing *Ls* nearly *200 pH* seems enough. However, this will reduce the gain. So there must be some optimization for these values in the final S-parameters of the full LNA.

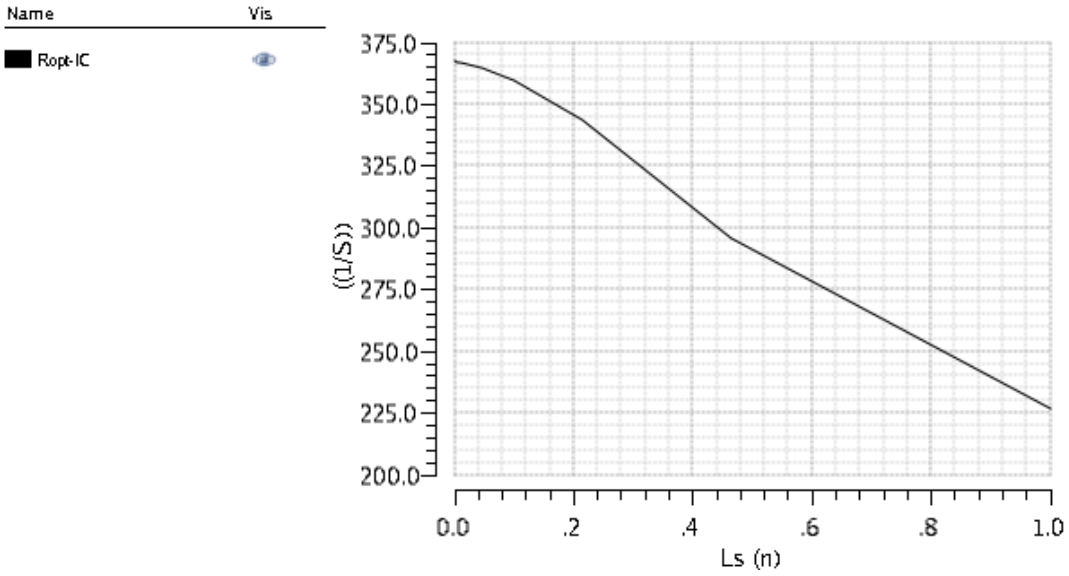


Figure 3.15 : R_{opt} values with regards to L_S

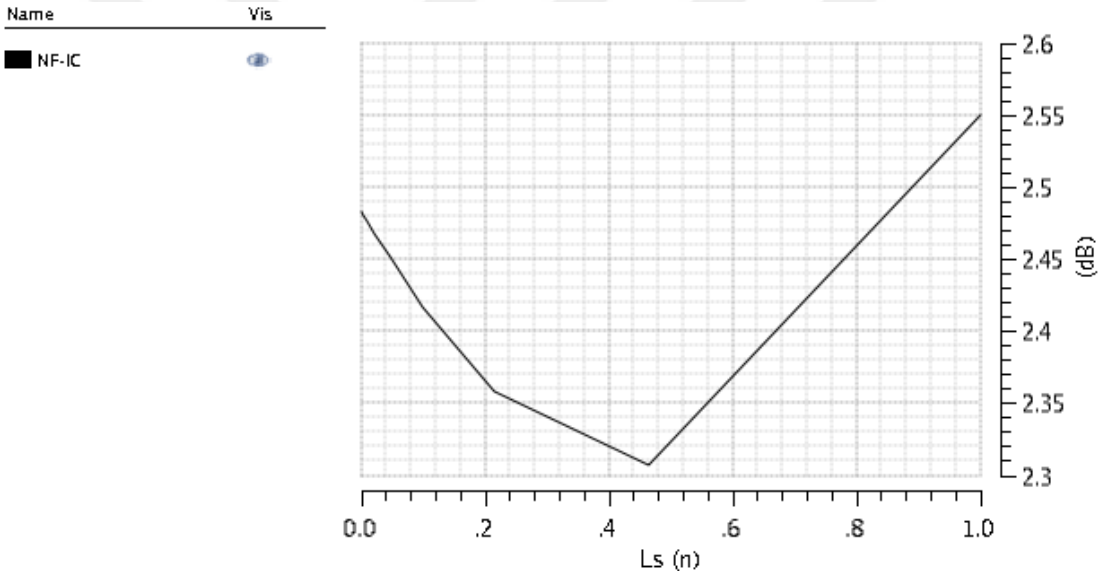


Figure 3.16 : *NF* values with regards to L_S

3.3.2.2 L_g optimization

After the optimization of L_S separately, we investigate the effect of L_g to noise figure also separately. L_S is cancelled out for these simulations. Gate series inductance L_g in the Figure 3.4, does not affect the NF_{min} of the topology as seen in Figure 3.18. However, R_{opt} value strongly depends on Lg and becomes 50 Ω for *Lg=2.6 nH* making *NF=0.8 dB*. Note that, these simulations are done with ideal inductors, so real optimum noise values will end up being much

higher because of the inductor losses. However, the trend of *NF* with changing Lg values will be the same.

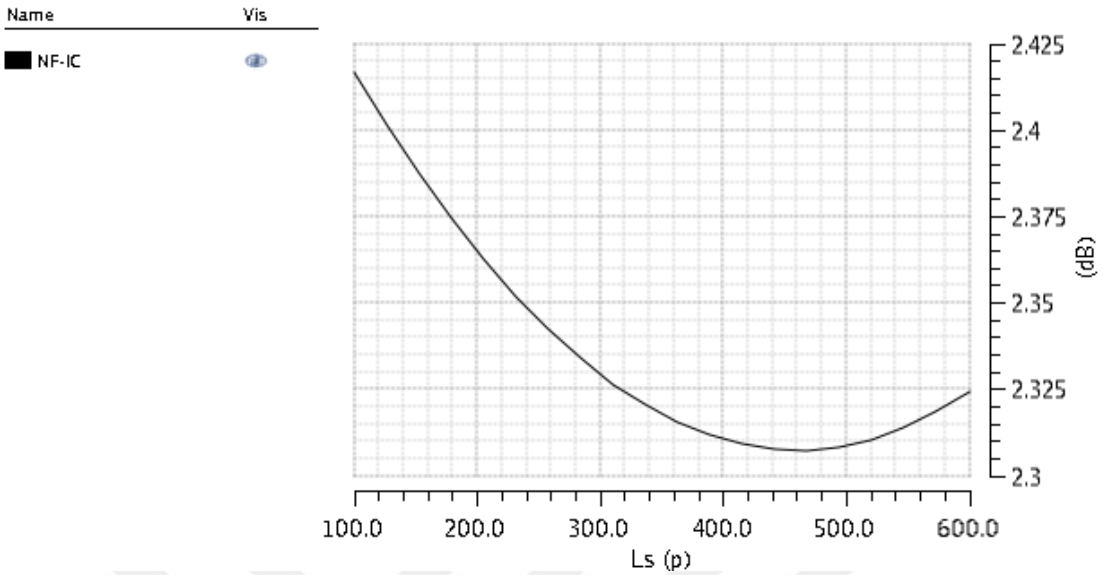


Figure 3.17 : *NF* values with regards to L_S in 100 – 600 pH gap

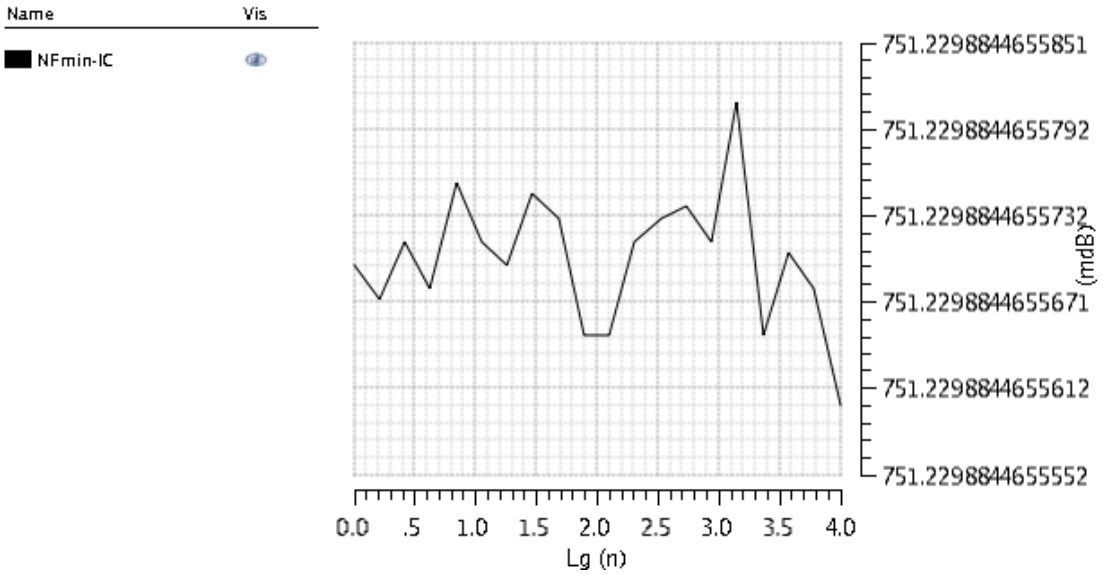


Figure 3.18 : NF_{min} values with regard to L_g

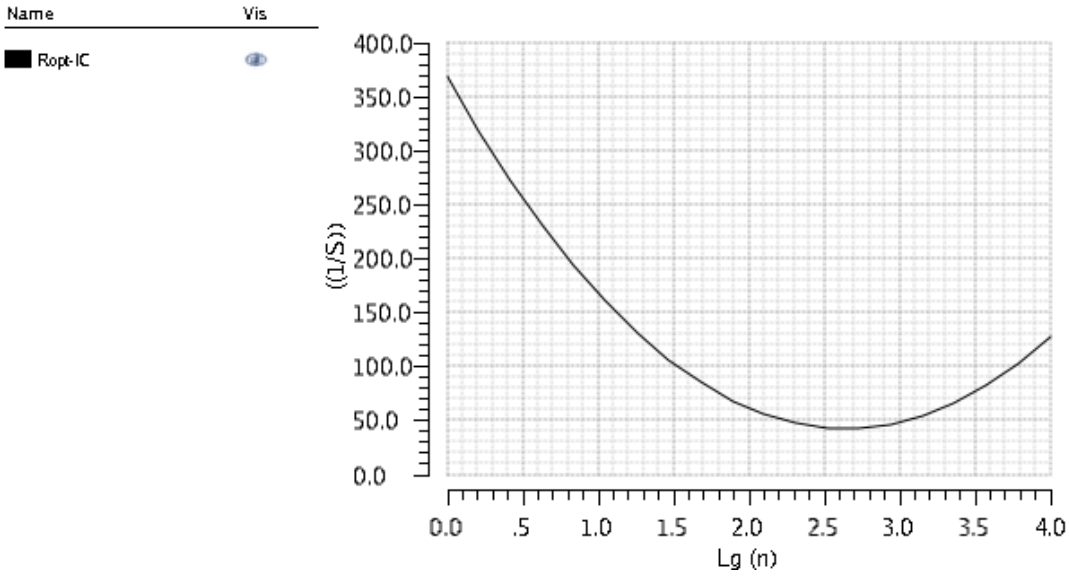


Figure 3.19 : R_{opt} values with regard to L_g

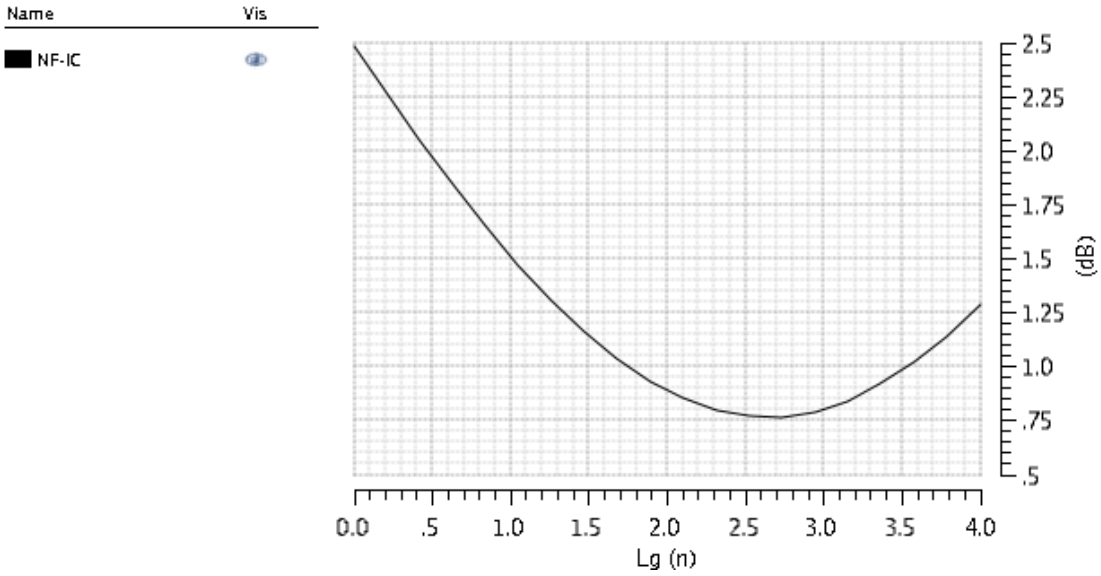


Figure 3.20 : *NF* values with regard to L_g

3.3.2.3 L_g and L_s optimization

As seen from the analyses above, L_g and L_S both have an effect on L_g and L_S. Thus investigation of both will give the designer a better result. L_S does not depend on L_g but depends on L_S since L_S changes g_m by degeneration. (Figure 3.22)

Optimum value of R_{opt} seems to be 42 Ω, because the optimum value of *NF* is obtained when R_{opt} *=42* Ω (Figure 3.23). When Lg=2.6 nH, R_{opt} is 42 Ω. Finally, at L_S*=50 pH, NF* is achieved as the minimum which is 750 mdB (Figure 3.24).

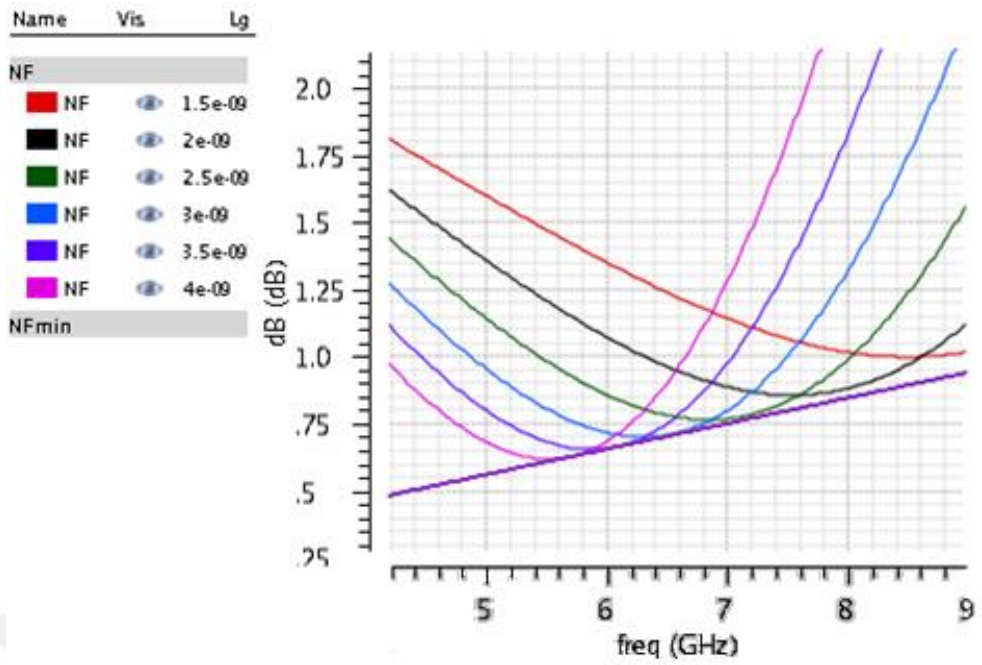


Figure 3.21 : Bringing *NF* values to NF_{min} in the desired frequency with L_g

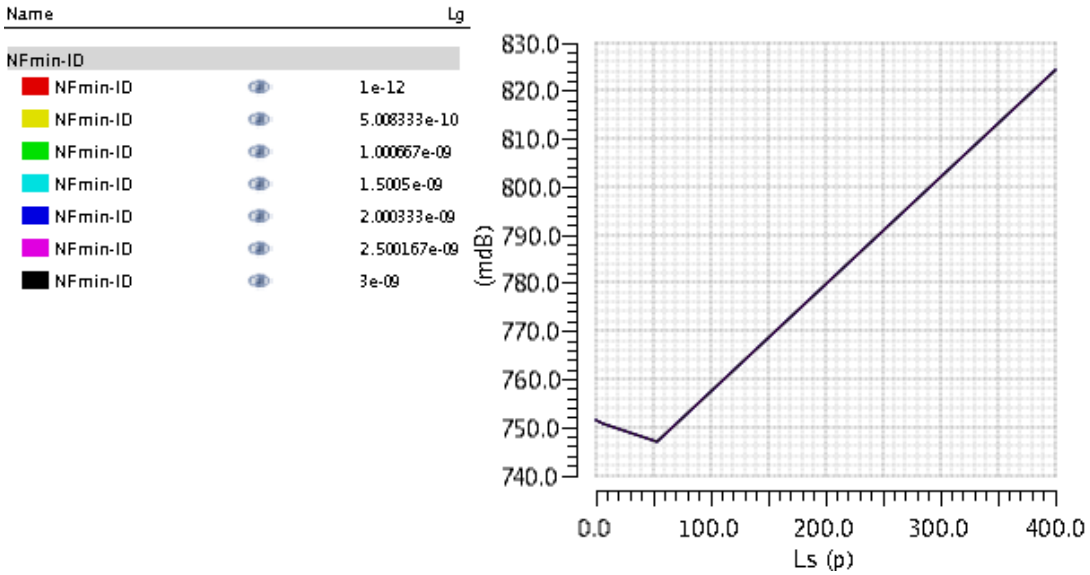


Figure 3.22 : NF_{min} with regard to L_g and L_S

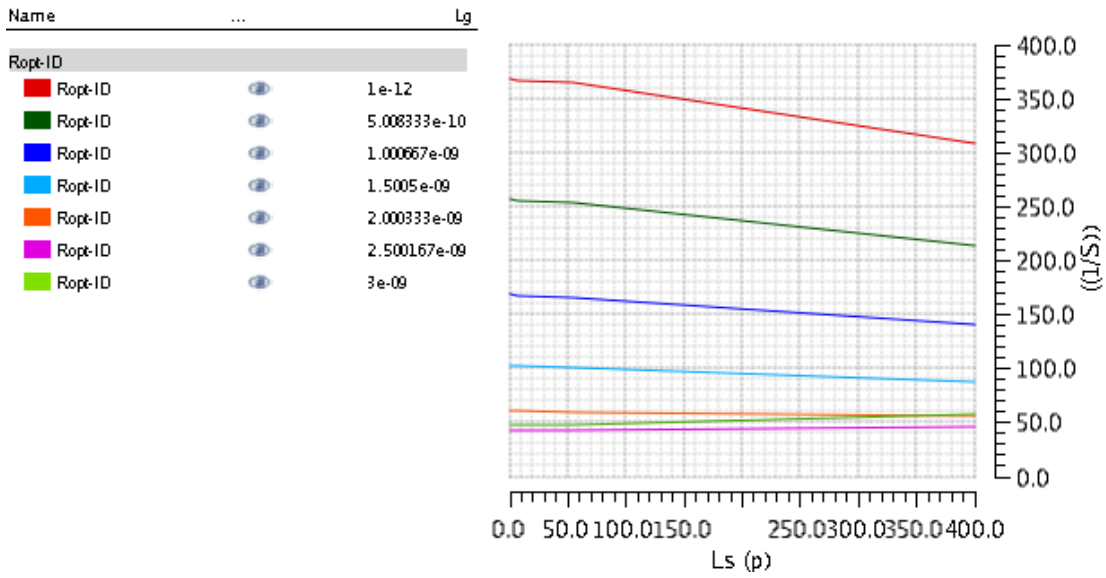


Figure 3.23 : R_{opt} with regard to L_g and L_S

As explained in Section 3.2.1, NF_{min} can be achieved for a particular Q_L which depends on the frequency of interest, L_g and L_s. It can be seen from Figure 3.9 that $L_s = 100\,pH$ gives the minimum NFmin, and from Figure 3.15 and Figure 3.18 $L_g = 2.6nH$ brings NF to NFmin.

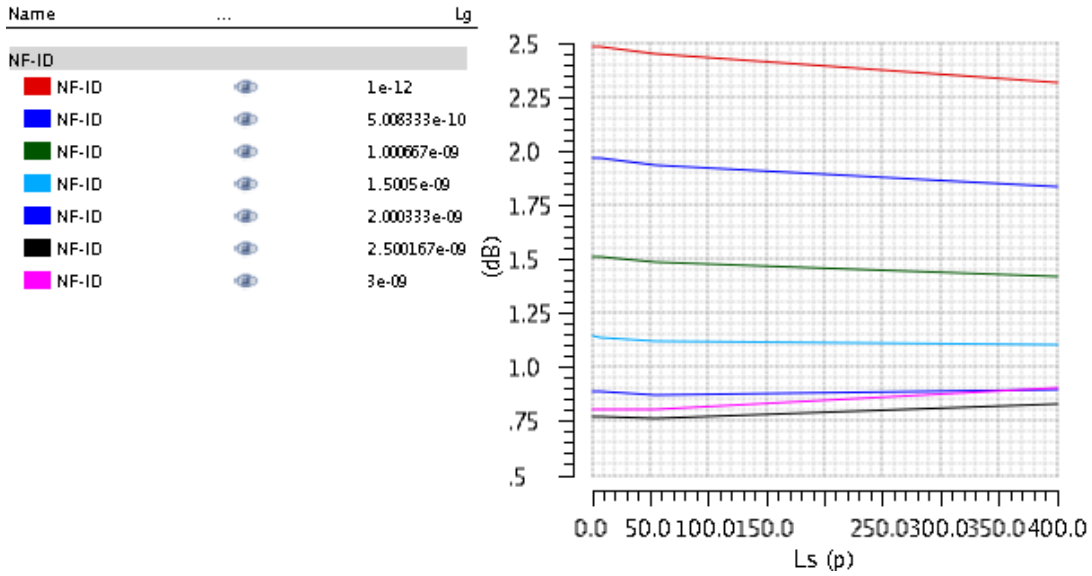


Figure 3.24 : *NF* values with regard to L_g and L_S

When L_s is changed from 1pH to 400pH, optimum value of L_g is constant and is equal to 2.6 nH. However, when L_g is changed from 1 pH to 3 pH, optimum value of L_s changes

dramatically. When $L_g = 2.6nH$ which is optimum for NF, $L_s = 50pH$ gives the optimum NF. As L_g drops below its optimum value, L_s increases and even exceeds 400pH. As L_s increases the gain will decrease, hence L_s optimized for a smaller value.

These considerations were only for the noise figure of the LNA. However, input reflection coefficient is a crucial parameter of the LNA that must be set below -10 dB. In the next section, input reflection coefficient (S_{11}) of the circuit will be optimized with respect to L_s and L_g.

3.3.3 Design for input power match and gain

Input matching should be accomplished without degrading the noise figure. Input impedance of a typical cascode LNA is given in (3.27) and is equal to (3.28) at resonance. Therefore, L_s is chosen to make Z_{in} 50Ω, and L_g is chosen to have a resonance frequency at 7 GHz. Since, the current density and the number of finger respectively have been already determined to yield the minimum NFmin, one can get the cut-off frequency, gate-to-source capacitance and transconductance of the amplifying transistor for further calculation. Circuit simulations reveal these values as $C_{gs} = 120fF$ and $g_m = 0.04S$. For a 50Ω input impedance at 7 GHz, L_g and L_s can be calculated as in (3.46) and (3.47).

$$L_s = \frac{C_{gs}}{g_m} \times 50 = \frac{120f}{0.04} \times 50 = 150pH \tag{3.46}$$

$$L_g = \frac{1}{\omega^2 C_{gs}} - L_s = \frac{1}{(2\pi \times 7 \times 10^9)^2 \times 120 \times 10^{-15}} - 150p = 4.3nH \tag{3.47}$$

Detailed simulations give more precise values of L_s and L_g by sweeping their values in a range around the values that are calculated. Input reflection coefficient S_{11} is obtained as in Figure 3.25 for various L_s values. But, L_g is found to be nearly half of the calculated value. For $L_g = 2.6nH$ and $L_s = 250pH$, S_{11} is below -11 dB for wide band with a good match at the center frequency. However, NF is 2.35 dB for this L_s value. Moreover, larger L_s values causes gain to be lower as will be explained in the next section.

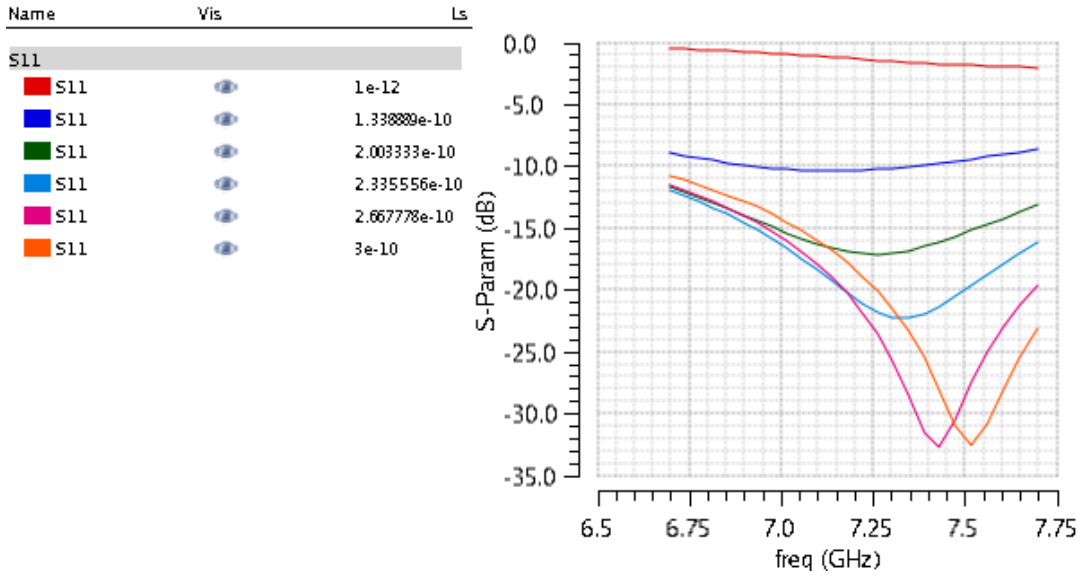


Figure 3.25 : Input reflection S_{11} for different L_s values

In section 3.2.2, the biasing inductor was proposed for better noise matching with higher gain as in Figure 3.5. Though the input impedance equation turns out to be complicated, MATLAB simulations showed that L_b could be used to increase the impedance seen looking into to amplifier input. L_b, L_g and L_s values are obtained more precisely with circuit simulations. Figure 3.26 shows that $L_g = 1.7\ nH$ and $L_b = 1.2\ nH$ (drawn with the black line), yields best S_{11} of the LNA. If we check the noise figure of the LNA with these values, it is seen in Figure 3.27 that these inductor values also provide a reasonable noise figure. $L_g = 1.7\ nH$ and $L_b = 1.2\ nH$ enable S_{11} to be lower than $-11.4\ dB$ and realize $NF = 2.13\ dB$.

Simulations above are done using ideal inductors. Modelling ideal inductors with series resistances yields more realistic noise figures. Hence resistances of these inductors are calculated with the formula below, assuming a constant Q factor for different inductor values, in order to have a fair comparison.

$$R_{series} = \frac{\omega L}{Q} \tag{3.48}$$

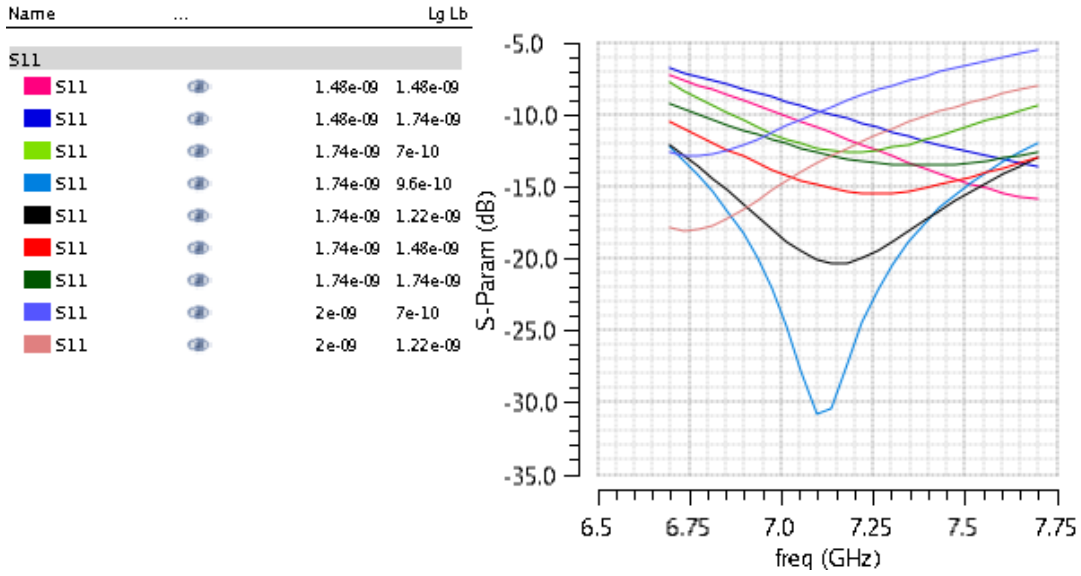


Figure 3.26 : S_{11} vs. frequency for different L_g and L_b values

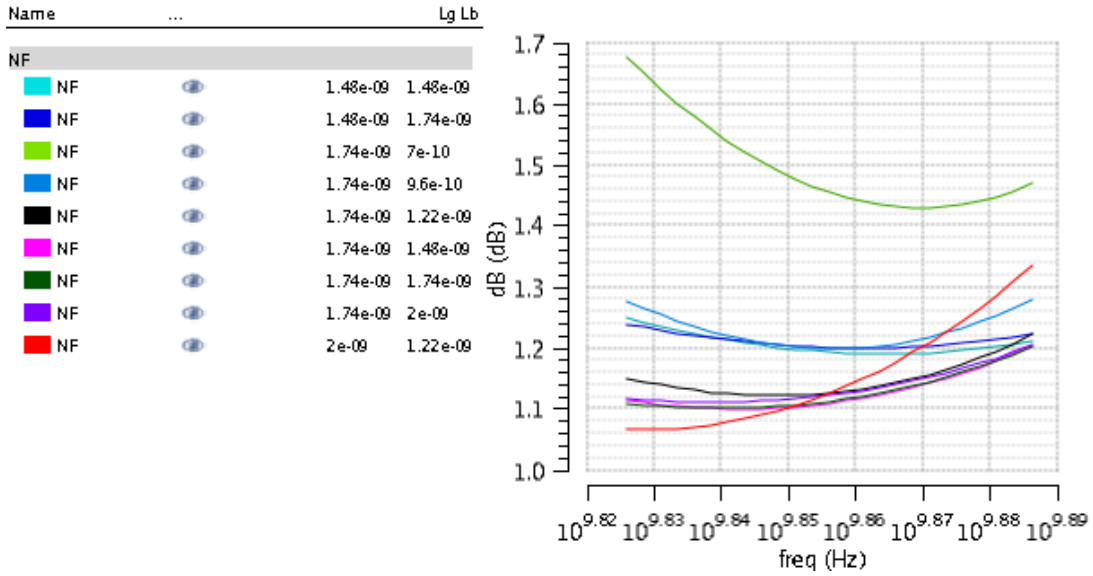


Figure 3.27 : Noise figure vs. frequency for different L_g and L_b values

Simulation results for the classical cascode inductive degenerated LNA is given in Figure 3.28. Power gain S_{21} is *14.85 dB*, *NF=1.97 dB* and S_{11} is below *-11 dB*. Simulation results for the LNA which is cascode inductively degenerated as well as having an additional L_b is given in Figure 3.29 and S_{21} is *17.75 dB*, *NF=2.13 dB* and S_{11} is below *-11 dB*. This result shows that the gain increases by 3 dB with *0.16 dB* compromise from the noise figure.

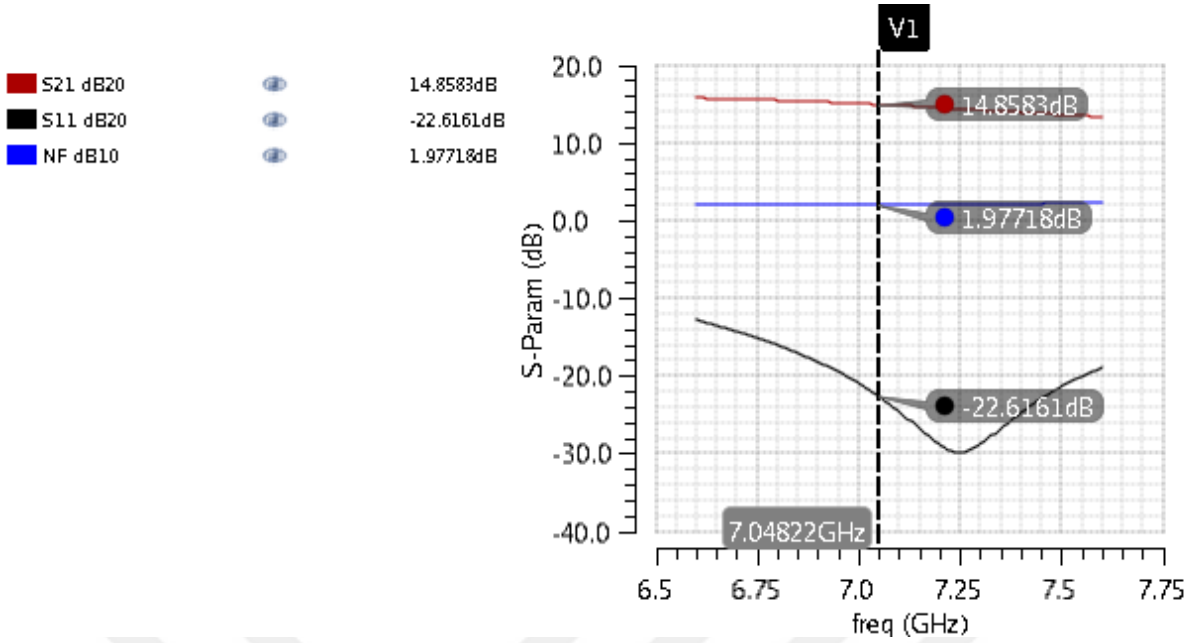


Figure 3.28 : S_{21}, S_{11} and NF of the classical cascode degenerated LNA (L_g and L_s)

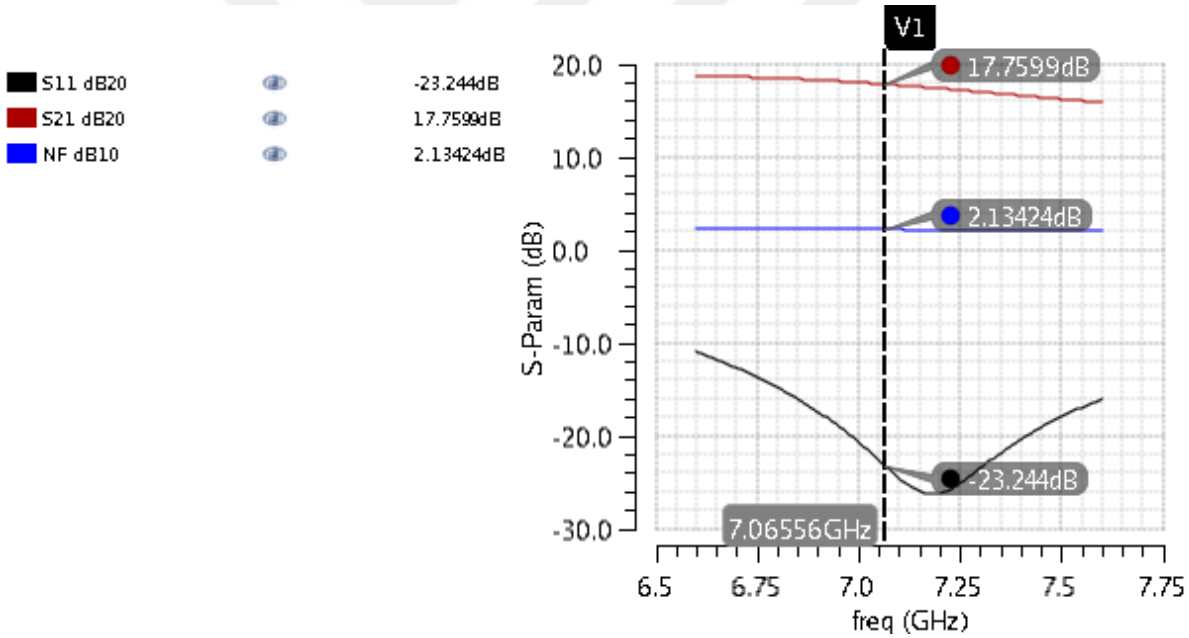


Figure 3.29 : S21, S11 and NF with additional L_b inductor LNA

This optimized noise figure is degraded by the Q factor of the inductances and the layout parasitics.

3.3.4 Design of inductances

UMC technology has inductances with a corresponding model, but since they are drawn in a general manner, they do not satisfy all the preferred parameters such as the area. Custom designed inductors are used because UMC inductors cover a large layout area. In the design of inductors; firstly, sizes of inductors should be determined with respect to the desired inductor value. For this purpose, a website of a study group from Stanford has been utilized. Here calculation of the inductor sizes is done based on the formulas given in [13]. After finding the sizes of inductors such as the number of turns (N), turn spacing (S), turn width (W) and the outer diameter (D_{out}), inductors are drawn using the top metal of the technology with the calculated length and widths in (3.49), (3.50 and (3.51). D_{in} is the inner diameter, and f is the length of first rectangle, and lengths of following rectangles are 2f+k, 2f+2k, 2f+3k… After drawing the inductor layout, its gds is exported from Cadence and imported to ADS. With ADS electromagnetic (EM) characterization, S-parameters file of this inductor is generated. This S-parameters file contains the inductance, parasitic capacitances and resistances of the inductor. Design of the inductor is finalized with further simulations in Cadence and ADS for characterizastion purposes.

In the design of inductances there are several important points. Firstly, larger width decreases the inductance but increases the quality factor by decreasing the series resistance of inductor. Nevertheless, due to the skin effect, increasing the width of the inductor does not help the quality factor after some point [27]. Moreover, increasing the width increases the parasitic capacitances resulting in self resonance at a lower frequency. If the frequency of operation is close to the self-resonance, inductance value of the inductor will change dramatically in that frequency regime. This kind of inductances are very hard to use in RF designs. The outer diameter and eventually the inner diameter, and the number of turns are the most effective parameters on inductance rather than the turn width or spacing. Schematic simulations of the LNA regarding S_{11}, S_{21}, S_{22}, S_{12} and NF are done with inductor models given in Figure 3.31, 3.32, 3.33, 3.34, and 3.35.

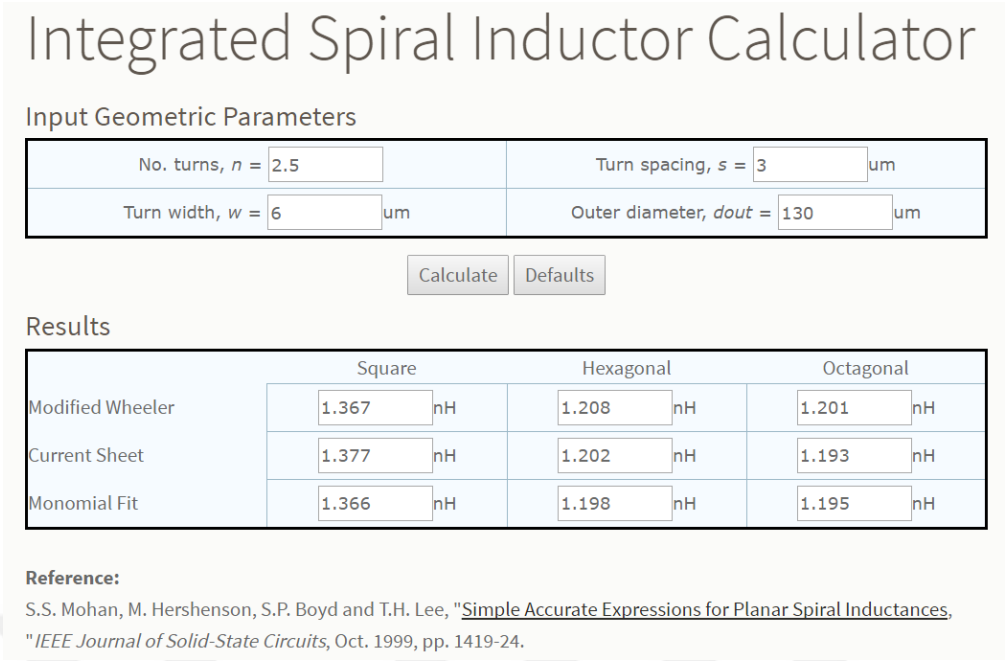


Figure 3.30 : Integrated spiral inductor calculator interface [12]

$$k = \frac{(s+w)}{4+4\sqrt{2}} \tag{3.49}$$

$$D_{in} = D_{out} - 2\left[\ n \bullet s + \left(\ n\ +1\right) \bullet w\right] \tag{3.50}$$

$$f = \left(\frac{D_{in}}{1+\sqrt{2}} - 2k\right) \Big/ 2 \tag{3.51}$$

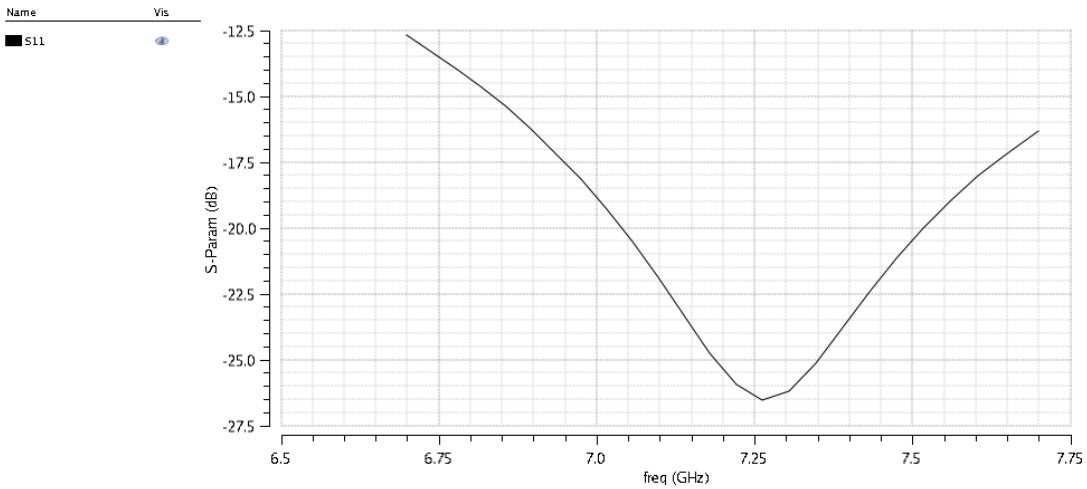


Figure 3.31 : S_{11} graph of the LNA with inductor models

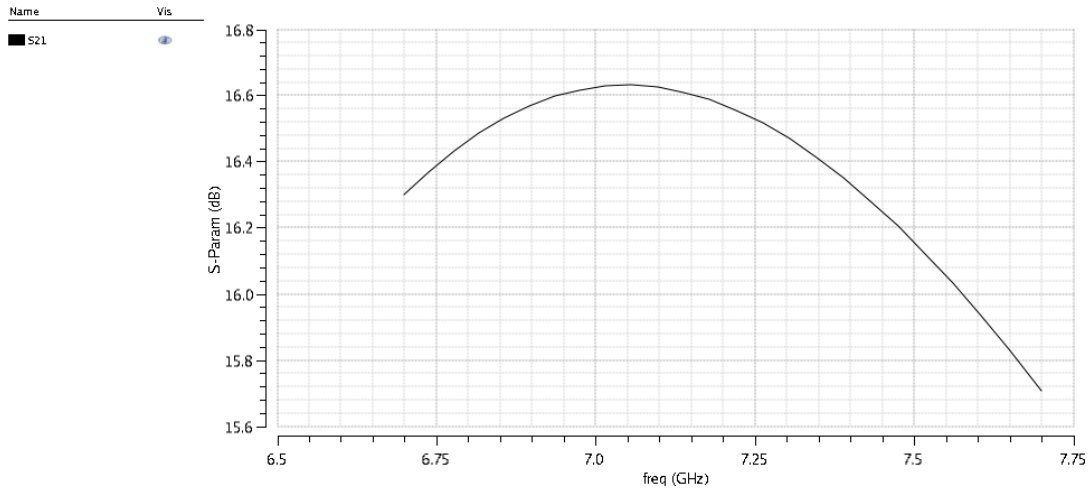


Figure 3.32 : S_{21} graph of the LNA with inductor models

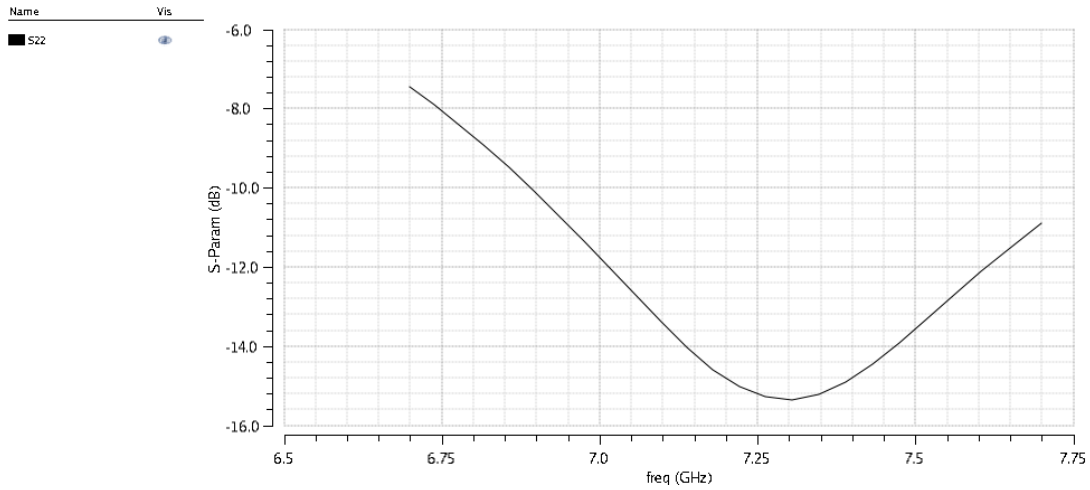


Figure 3.33 : S_{22} graph of the LNA with inductor models

Figure 3.35 shows that inductors add an extra *1.2 dB* noise figure such that the noise figure becomes *2.4 dB*. In these simulations mutual inductance effects are not included because inductors are characterized separately. Next step is the ADS characterization of the inductances and RF lines together. After characterization, further simulations and optimization, post layout simulation results are given as below.

Layout floorplan is critical to determine the impact of the mutual inductances which can ruin the performance of the LNA. Distance between inductors are chosen as at least the size of an inductor in the floorplan to minimize this effect. Also RF paths are critical in the LNA layout. Instances must be placed such that minimum number of lines should cross RF paths. In this design only RF path that goes to the RF output path is crossed with VDD line due to the need

for more decoupling capacitances. In circuit simulations it is observed that, DC lines that cross the input RF path are more critical in the LNA performance.

Steps of the complete design methodology and the outputs of each step is given in Figure 3.36.

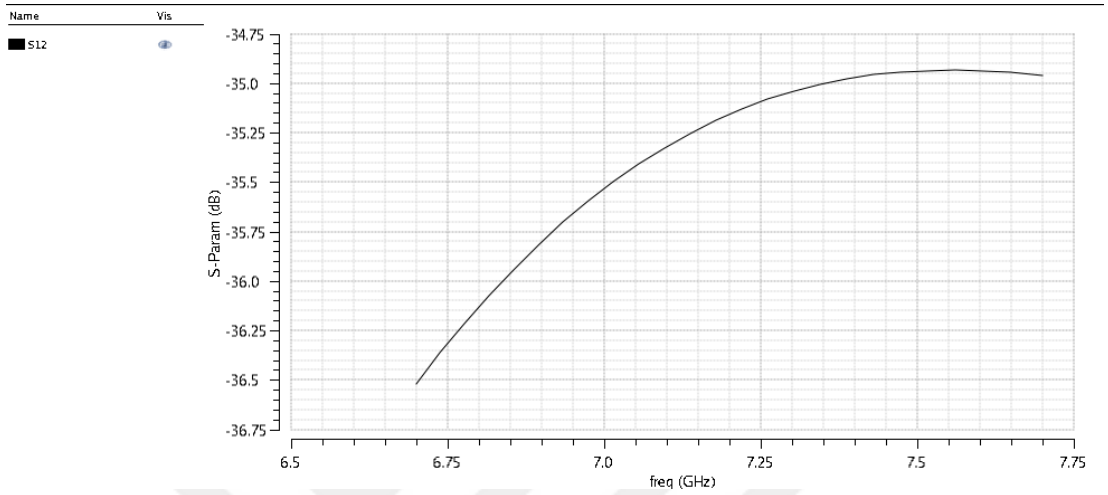


Figure 3.34 : S_{12} graph of the LNA with inductor models

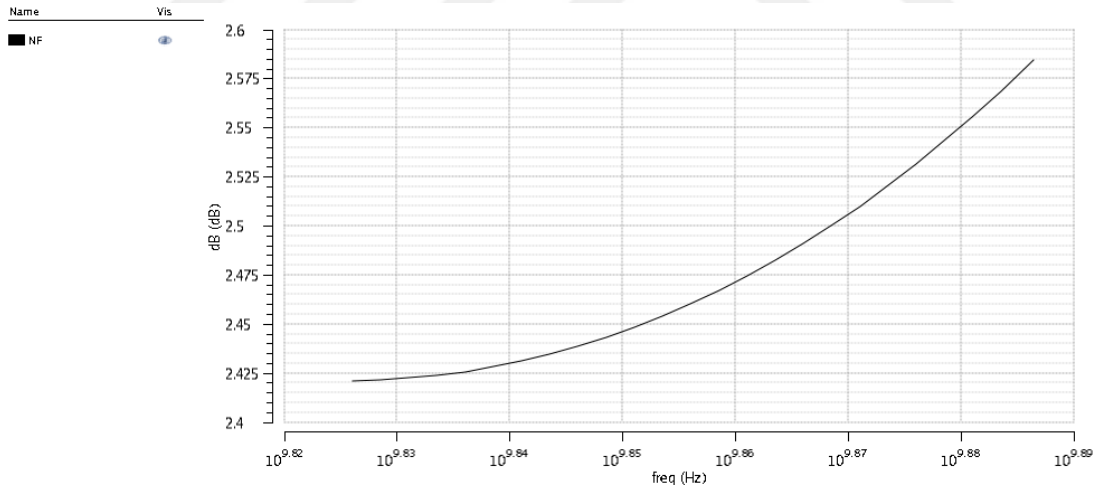


Figure 3.35 : NF graph of the LNA vs. frequency with inductor models

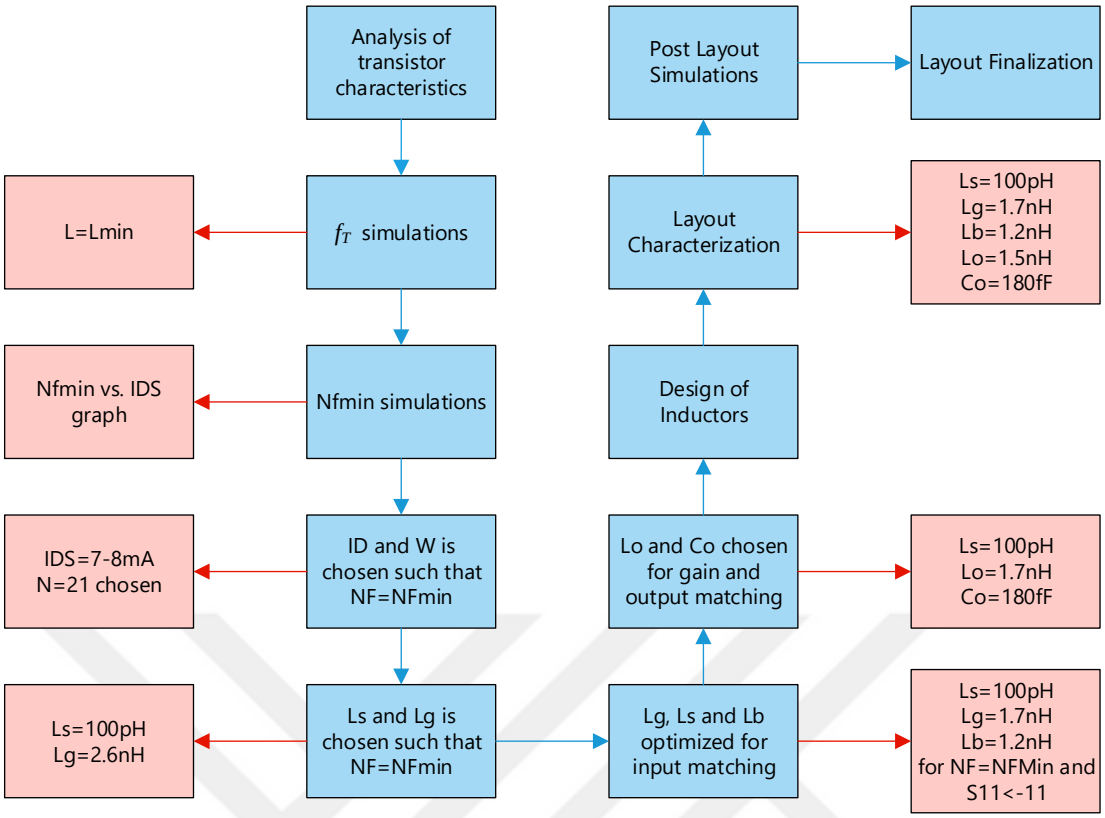


Figure 3.36 : LNA design steps and determination of critical values

3.3.5 Post layout simulations and final results

Final layout of the designed LNA is drawn as in Figure 3.37. Post layout simulations are run to finalize the design before production of the circuit and given in APPENDIX A. Figure A.1 and Figure A.2 shows S_{11} and S_{22} are obtained below *-11 dB* in post layout simulations. *NF* is *2.6 dB* and S_{21} is higher than *15 dB* as shown in Figure A.3 and A.5. As in Figure A.7 stability factor *K* is larger than 1 at all frequencies confirming unconditionally stability. Also, the third order input intercept point (IIP3) is $-2.24\ dBm$. (Figure A.6) Results highlight that a highly linear LNA is designed at room temperature (27°C), verified with post layout simulations.

Table 3.3 gives a comparison of CMOS LNAs from the literature designed near the frequency of interest. Table shows that the designed LNA has very low noise and high linearity at the same time. Thus it can be concluded that this LNA is comparable with other LNAs from the literature and can be tested under space conditions such as cryogenic temperatures and radiation for various applications.

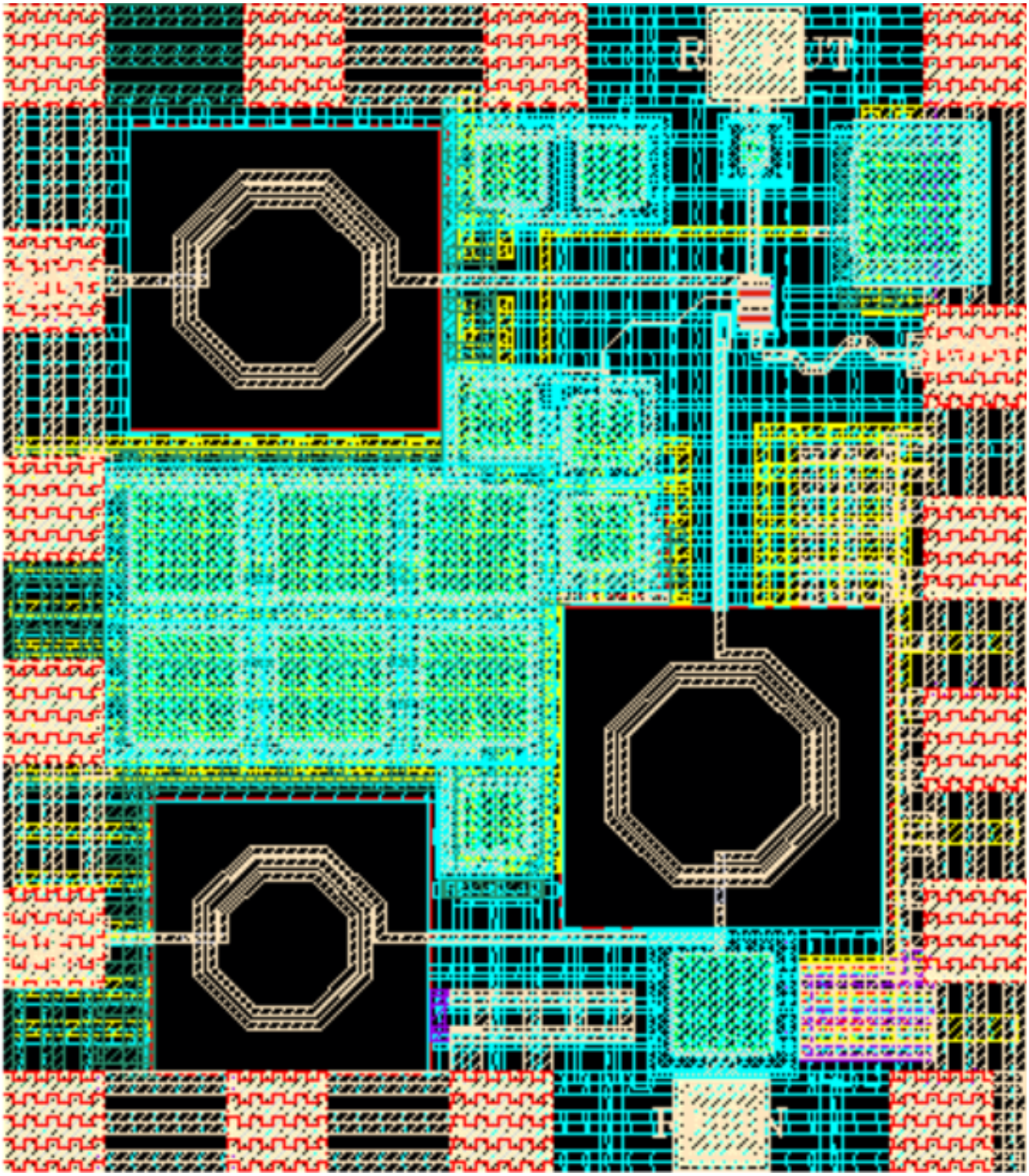


Figure 3.37 : Final layout of the designed LNA

The simulation model files of Mixed Mode/RF technology of UMC are verified to be valid until −40°C. Even though model files are not valid at the aimed temperatures, simulations at −40°C can represent the trend of the LNA parameters with the temperature decrease. Post layout simulation results at −40°C are given in APPENDIX B. Figure B.1 depicts that input reflection improves by 1 dB and it is seen in Figure B.2 that output reflection curve shifts slightly to the right. Since the LNA is designed for a wider band centering the desired space communication band, 7145-7190 MHz, this shift does not cause any trouble. Figures B.3 and B.5 show the voltage gain increase of 1 dB and noise figure decrease of 0.5 dB, respectively. These improvements of the LNA parameters are coherent with the expectations as stated before. Further progress is expected as the temperature decreases to cryogenic temperatures. Additionally, linearity of the LNA improves as can be visualized in Figure B.6 and input IP3 becomes −1.164 dBm.

Table 3.3 : Comparison of LNAs in the literature with the designed LNA in this thesis (* Post Layout Simulation)

	Specialty	Technology	Bandwidth (GHz)	S21 (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Chip Area (mm^2)
This Work*		0.18um CMOS	6-8	15.6	2.6	-2.4	25	0.56
[11]	UWB	0.18um CMOS	2.3-9.2	9.3 (max)	8 – 4(NF_{min})	-6.7	9	-
[17]	UWB	0.18um CMOS	3.1-10.6	9.7	5.1	-6.2	20	0.59
[18]		0.25um CMOS	7	6.2(max)	3.3	8.4	13.8	-
[19]	WB	0.13um CMOS	0.1-6.5	19	4.2	1	12	-
[20]	WB	0.18um CMOS	2.45-5.5	12.2	5.1	-4.7	75	-
[21]	UWB	0.13um CMOS	3.1-10.6	15.1	2.5	-8.5	9	0.87
[22]	UWB	0.18um CMOS	0.4-10	12.4	6.5	-6	12	0.42
[23]	ESD protection	0.13um CMOS	4.5-6	14.8(max)	2.6	-9	6.6	0.14
[24]		0.18um CMOS	3-6	13.5	6.7	-5	5.94	1.1
[25]		0.18um CMOS	8-10	10(from graph)– 18(max)	5 – 4(min)	-11.3	18	-

4. CONCLUSIONS AND RECOMMENDATIONS

Receiver systems generally consist of an antenna, an LNA, a Mixer and a VCO. LNAs being the first stage of the receiver system, determine the noise figure of the system. Receiver systems and LNAs are excessively investigated and designed using different technologies such as SiGe, HEMT and CMOS. LNAs that are used for space applications such as space communications and radio astronomy need more ability such as radiation robustness, very high sensitivity, very low noise temperature and high linearity etc. Although LNA research has been widely engineered, performance under space conditions still needs more exploration.

Most of the research on cryogenic and radiation LNAs were done using SiGe and HEMT devices. However, SiGe and HEMT technologies are very expensive and sophisticated compared to CMOS technology. Thus, moving the space electronics research towards CMOS technology will expand the alternatives and capabilities for a lower cost.

Literature search shows that only one paper reports cryogenic CMOS LNA and that study does not include any noise figure measurement. Generally cryogenic CMOS research studies were done about digital or precision analog circuits. Therefore, performance of CMOS LNA at cryogenic temperatures and under radiation should be investigated and improved.

The main goal of this thesis is to design a 7 GHz CMOS LNA to be tested under space conditions as cryogenics and radiation. Firstly, a general research on cryogenics and radiation basics are done. Then, the design of the LNA is analyzed and completed using 0.18 um UMC Mixed-Mode/RF CMOS technology.

4.1 Practical Application of This Study

As a result of this thesis a 7 GHz CMOS low noise amplifier has been designed. This LNA is built using 0.18 μm UMC Mixed-Mode/RF technology RF NMOS transistors.

Computer aided design tools Cadence and ADS have been employed. ADS is used to characterize the inductors and full layout without active devices via electromagnetic (EM) simulations. All other simulations were conducted with Cadence. Completed LNA achieves *2.6 dB* noise figure while having a voltage gain higher than *15.6 dB* in 6.7 and 7.7 GHz frequency band. Input and output reflections are below -11 dB all over the band. IIP3 of the LNA which characterizes the linearity of the circuit is found to be -2.24 dBm while the LNA consumes a total power of 25 mW.

4.2 Future Work

The design of the LNA is concluded with post layout simulations. Measurements of this LNA is very important to understand the factors on cryogenic and under radiation operation of LNAs. Measurement steps can be listed as below:

- Measurements at room temperature.
- Measurements at cryogenic temperatures.
- Measurement under radiation (TID).
- Measurements after radiation at cryogenic temperatures.

Room temperature and cryogenic temperature measurements will be done in ITU VLSI measurement laboratories. Measurements after radiation are also going to be conducted in ITU VLSI measurement laboratories, though under radiation tests will be performed in other laboratories. Co^{60} source is going to be used to realize the total ionization dose tests.

After measurements and modelling of transistors, as well as measurements of the designed LNA, a new radiation-robust cryogenic LNA is going to be designed for space conditions. With lower power consumption, a higher linearity, a better gain and a lower noise figure will be targeted in the design of this second LNA.

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APPENDICES

APPENDIX A: Post layout simulations at 27°C
APPENDIX B: Post layout simulations at -40°C

APPENDIX A

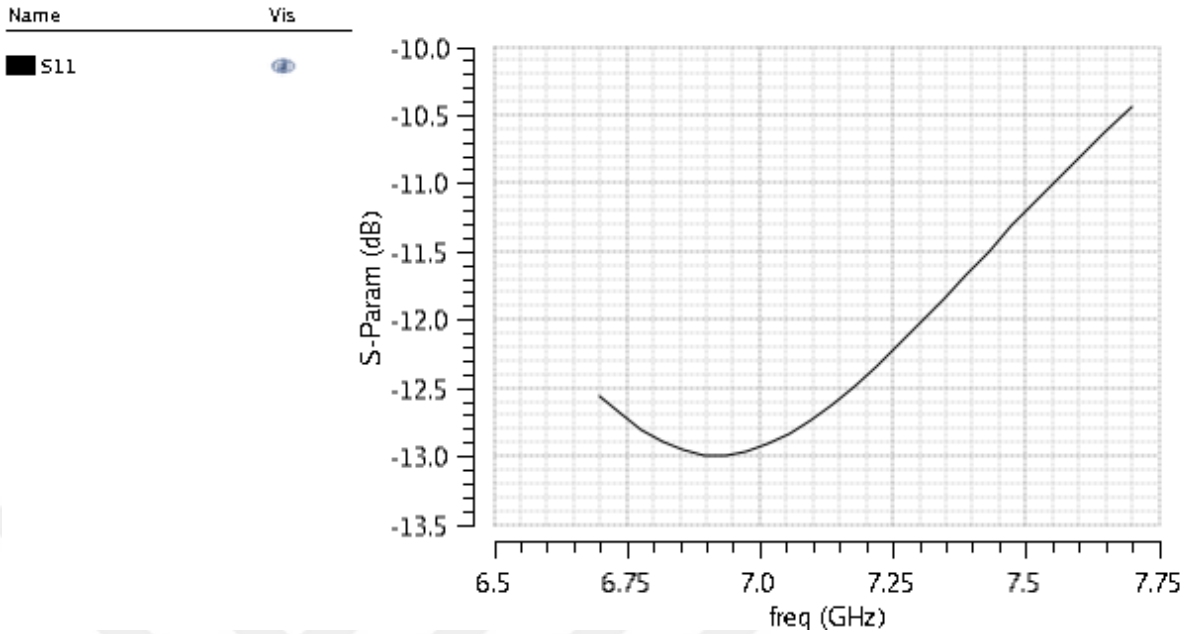

Figure A.1 : S_{11} vs. frequency of the designed LNA based on post layout simulations at 27°C

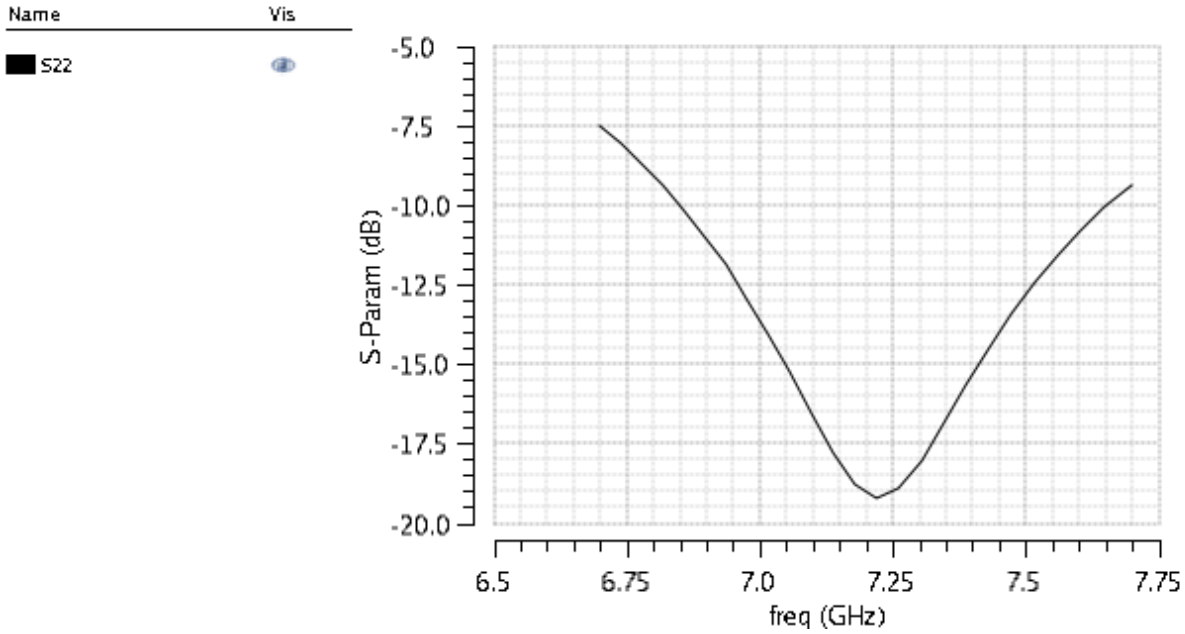

Figure A.2 : S_{22} vs. frequency of the designed LNA based on post layout simulations at 27°C

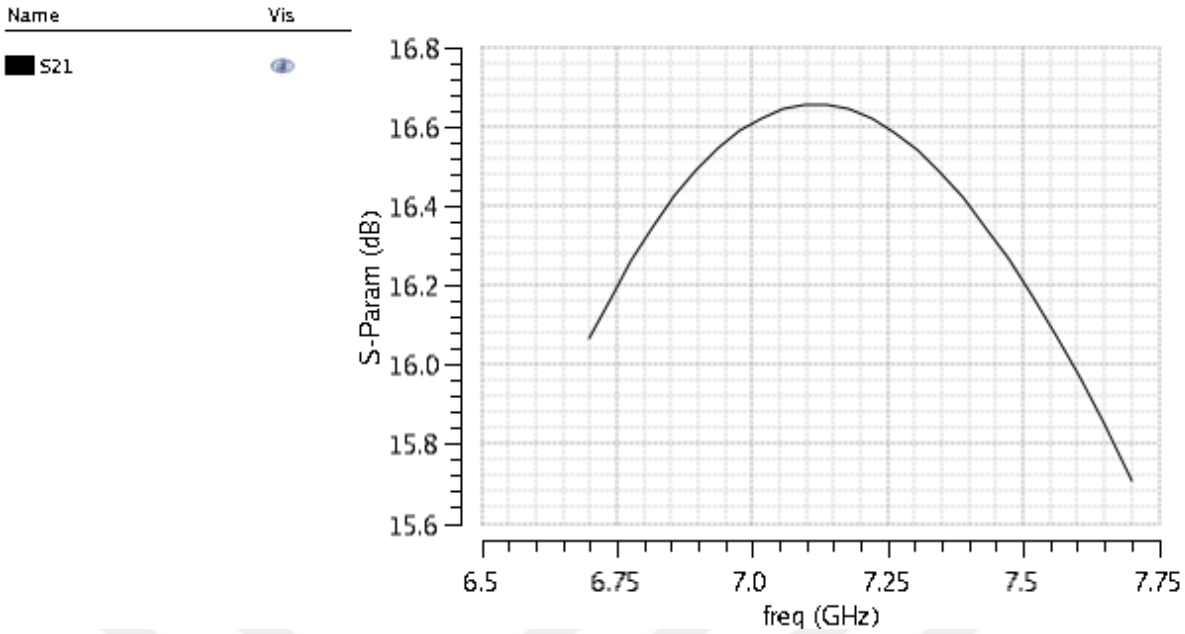

Figure A.3 : S_{21} vs. frequency of the designed LNA based on post layout simulations at 27°C

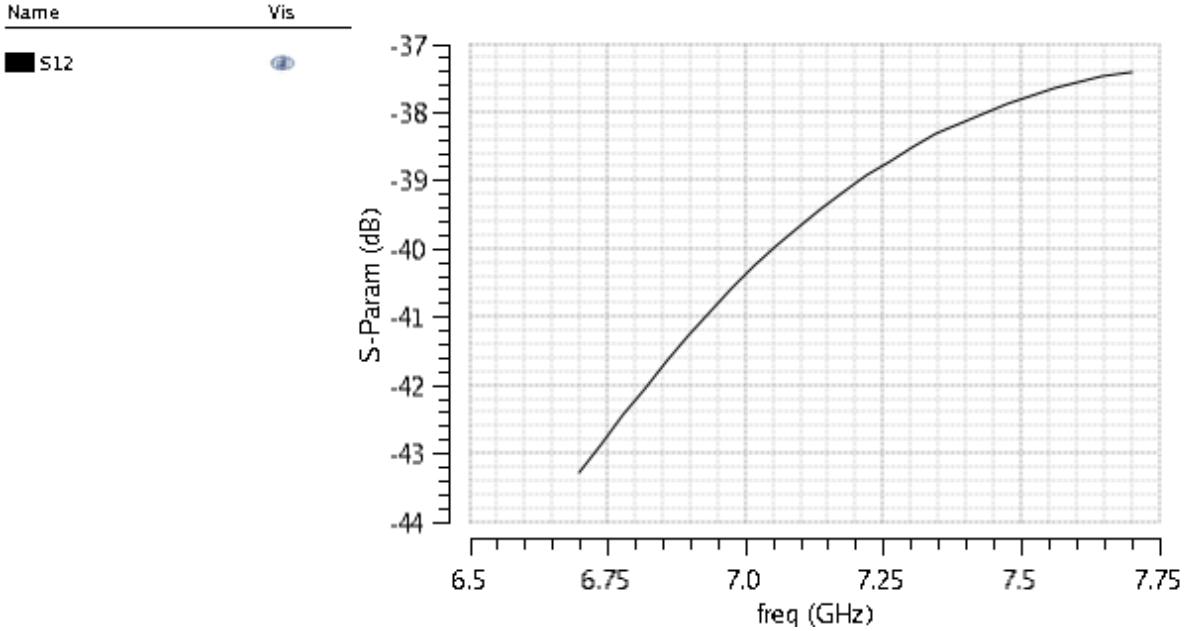

Figure A.4 : S_{12} vs. frequency of the designed LNA based on post layout simulations at 27°C

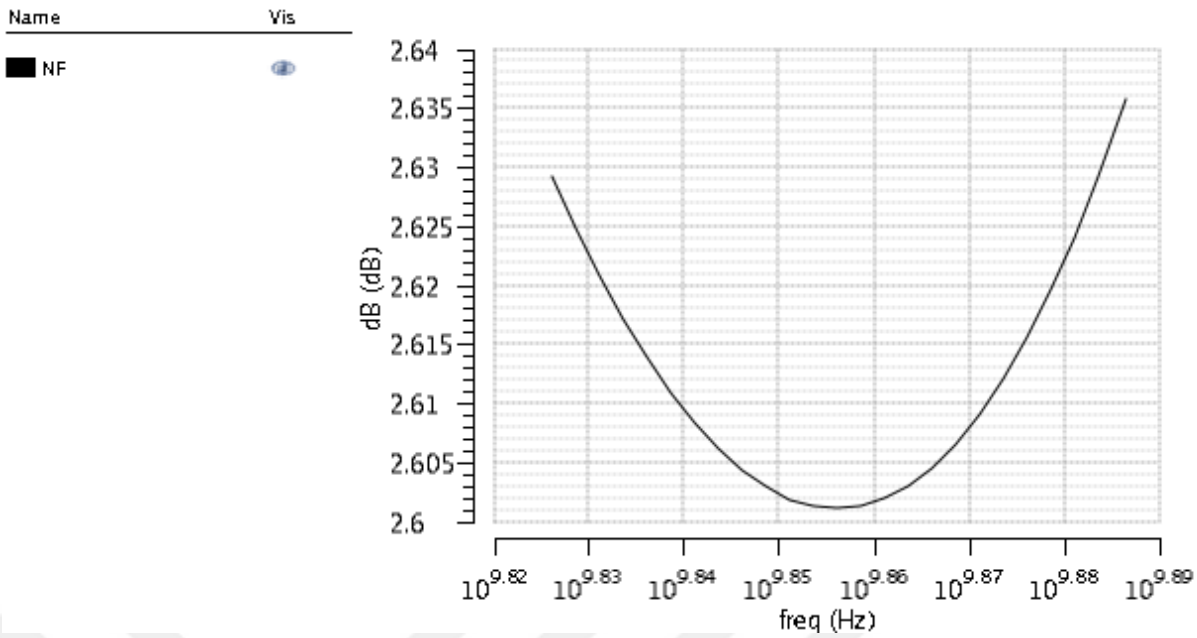

Figure A.5 : *NF* vs. frequency of the designed LNA based on post layout simulations at 27°C

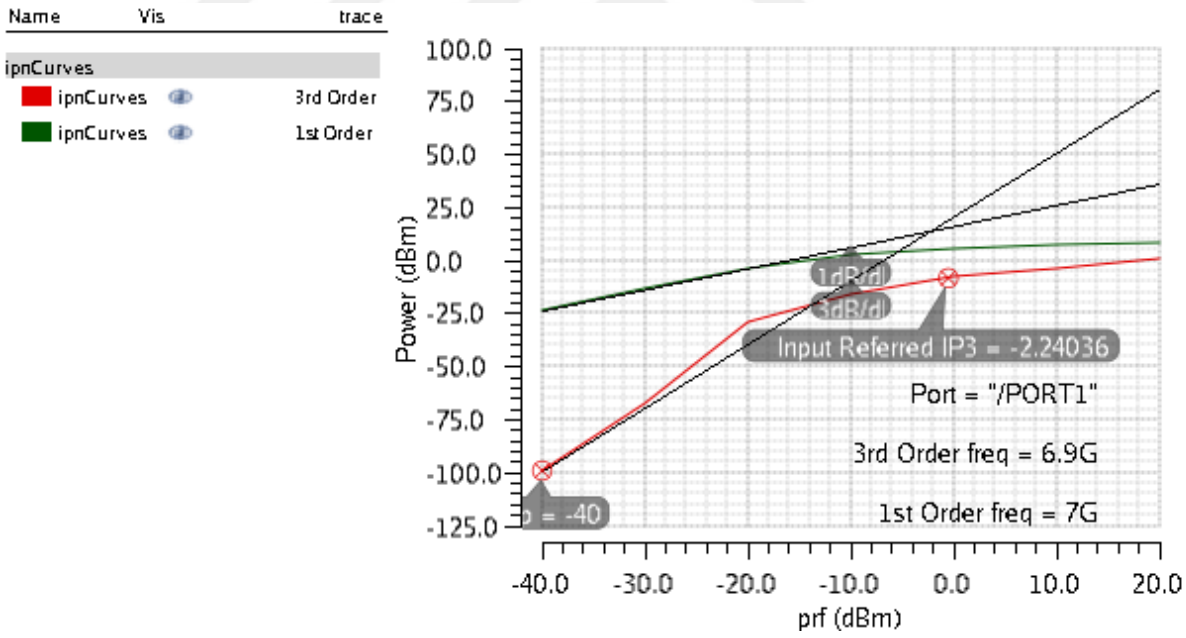

Figure A.6 : Post layout linearity simulation of the designed LNA at 27°C

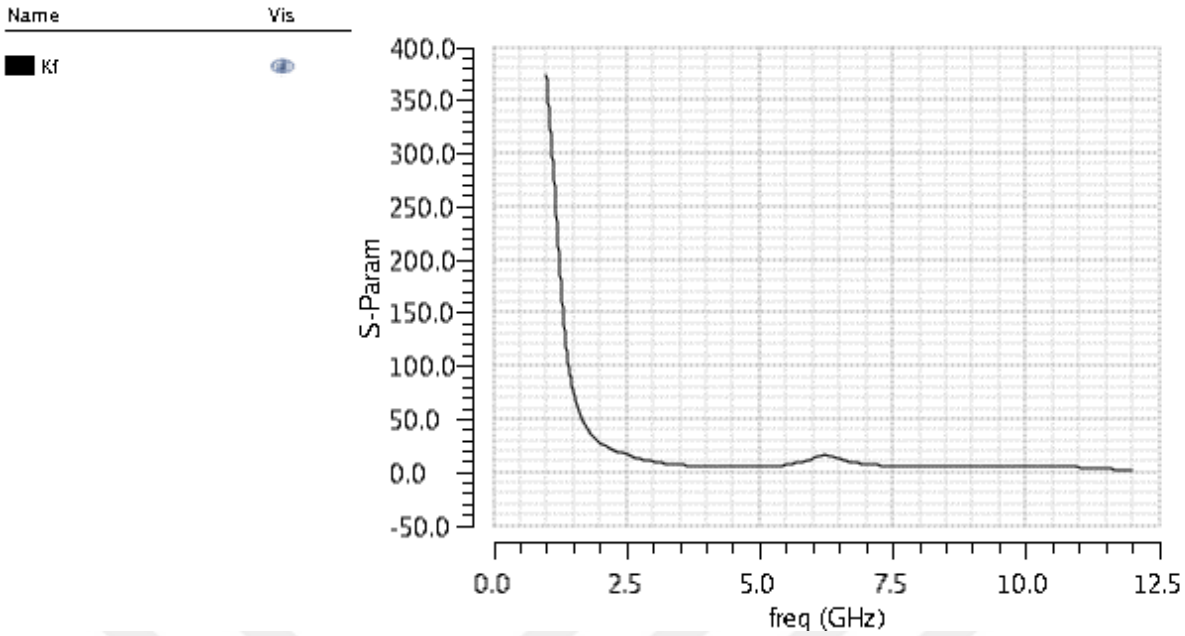

Figure A.7 : Post layout stability simulation of the designed LNA at 27°C

APPENDIX B

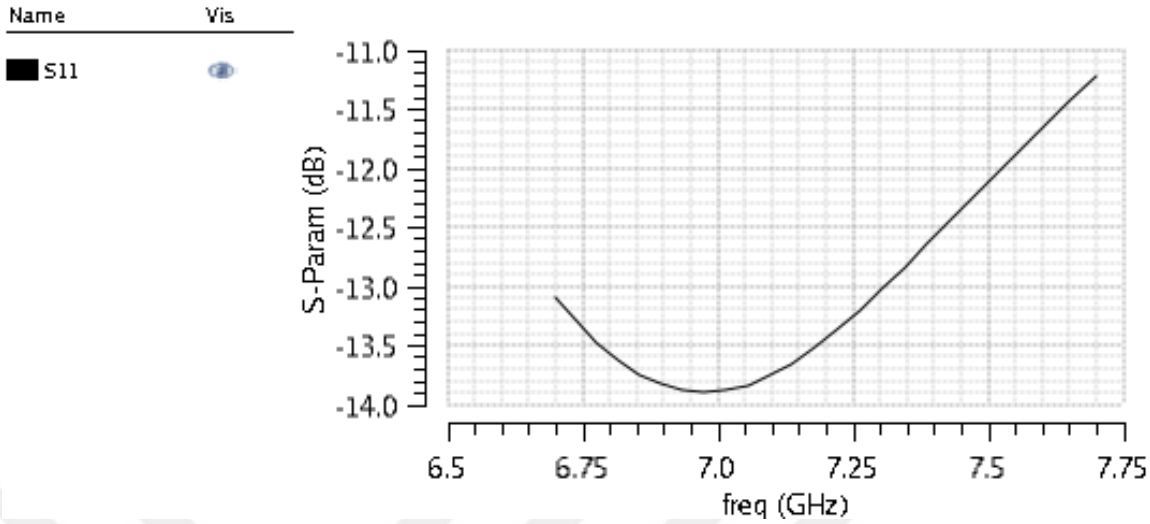

Figure B.1 : S_{11} vs. frequency of the designed LNA based on post layout simulations at −40°C

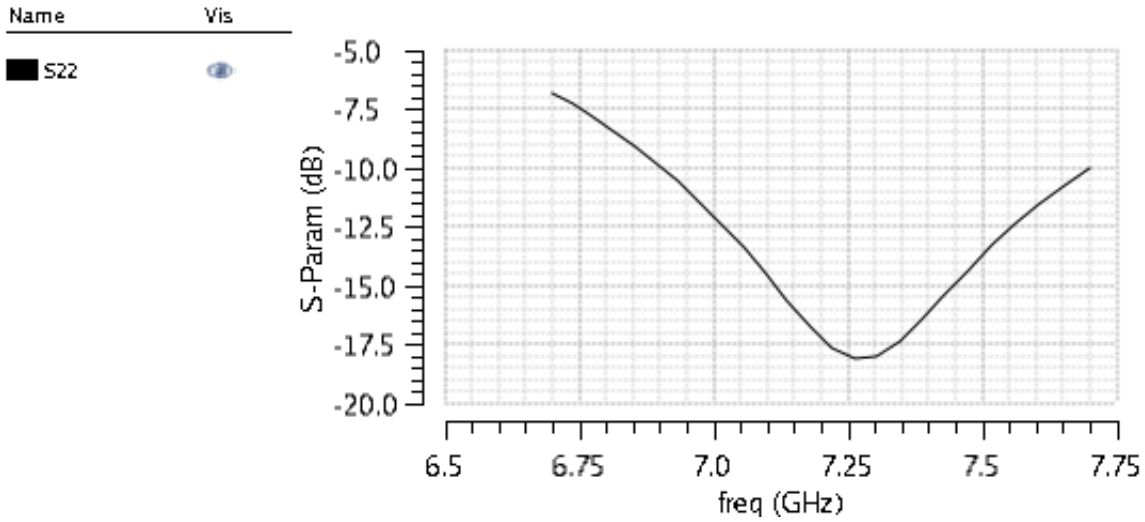

Figure B.2 : S_{22} vs. frequency of the designed LNA based on post layout simulations at −40°C

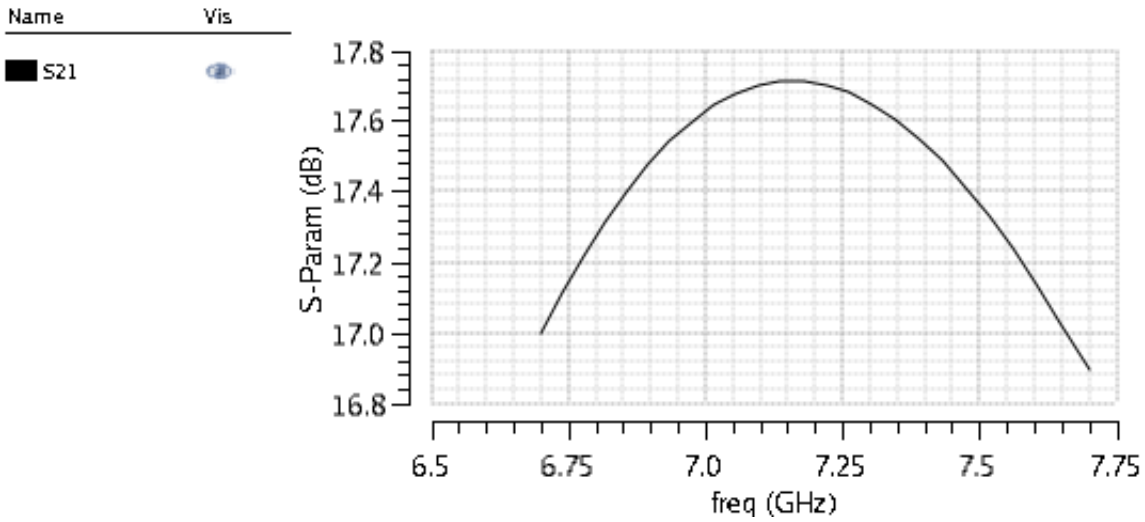

Figure B.3 : S_{21} vs. frequency of the designed LNA based on post layout simulations at −40°C

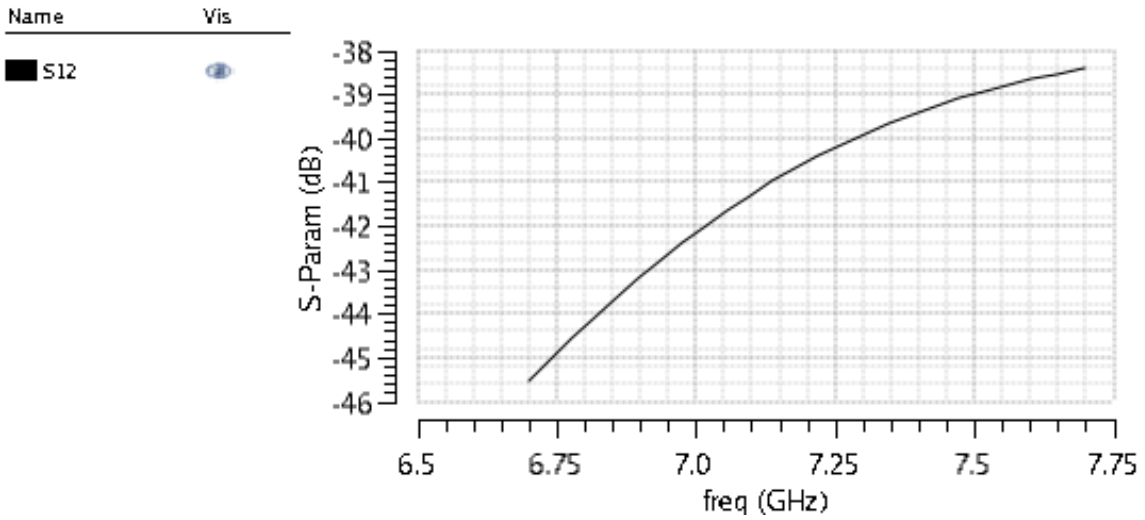

Figure B.4 : S_{12} vs. frequency of the designed LNA based on post layout simulations at −40°C

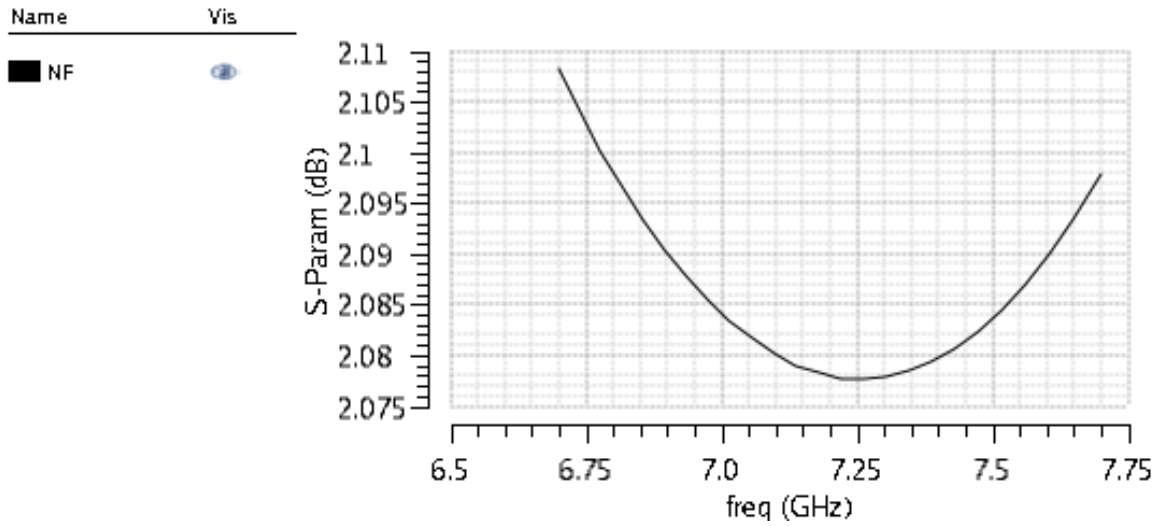

Figure B.5 : *NF* vs. frequency of the designed LNA based on post layout simulations at −40°C

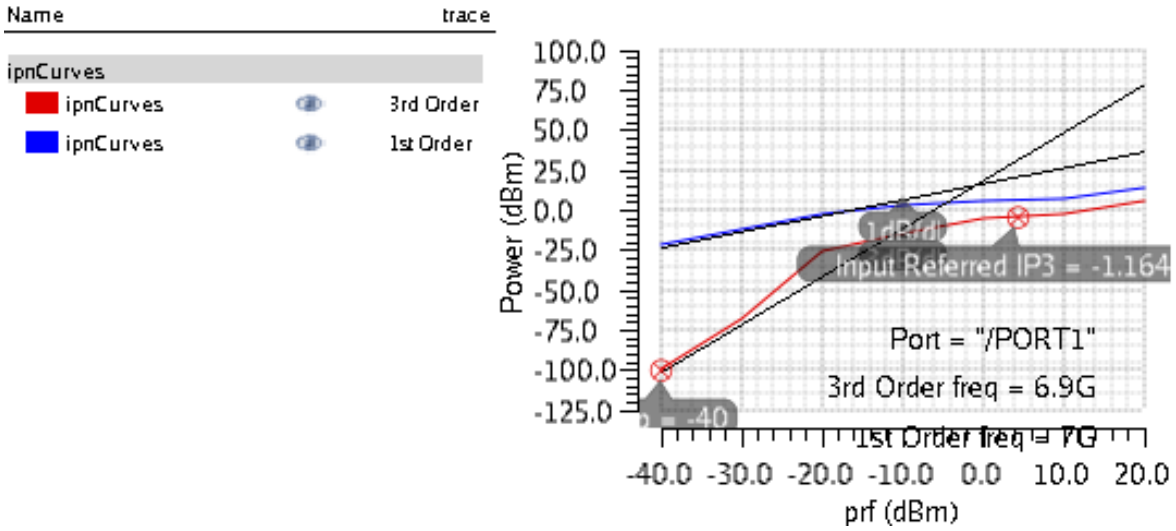

Figure B.6 : Post layout linearity simulation of the designed LNA at −40°C

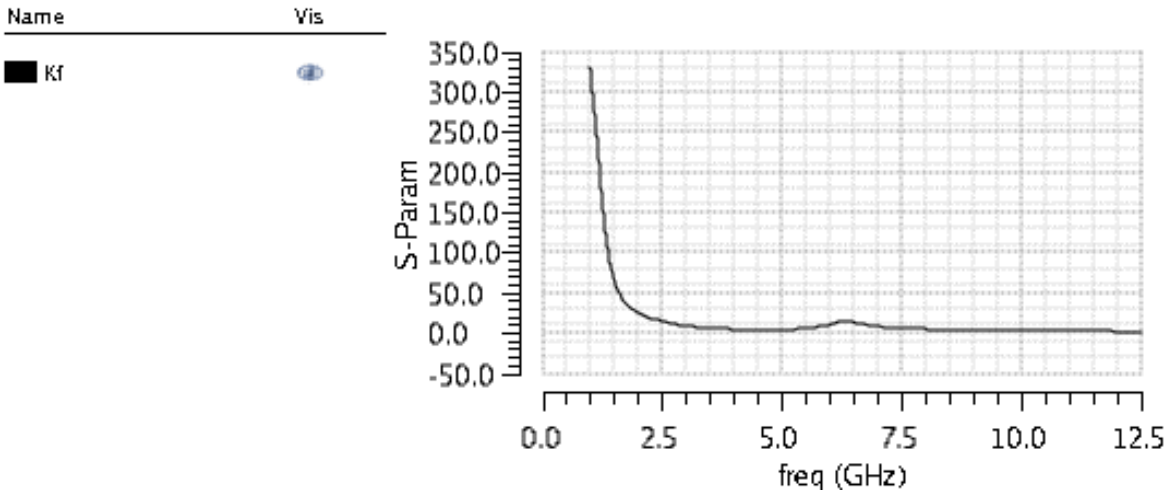

Figure B.7 : Post layout stability simulation of the designed LNA at −40°C

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- 2009 Outstanding success scholarship from Türk Eğitim Vakfı and success scholarship from Istanbul Technical University
- 2009 3rd to enter Istanbul Technical University
- 2009 300th place in the nation wide university entrance exam

PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

OTHER PUBLICATIONS, PRESENTATIONS AND PATENTS: