ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE
ENGINEERING AND TECHNOLOGY

STATISTICAL CRYOGENIC MODELING METHODOLOGY OF MOSFET DC CHARACTERISTICS IN BSIM3

M.Sc. THESIS

Aykut KABAOĞLU

Department of Electronics and Communication Engineering

Electronics Engineering Programme

JUNE 2019

ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE
ENGINEERING AND TECHNOLOGY

STATISTICAL CRYOGENIC MODELING METHODOLOGY OF MOSFET DC CHARACTERISTICS IN BSIM3

M.Sc. THESIS

Aykut KABAOĞLU
(504161205)

Department of Electronics and Communication Engineering

Electronics Engineering Programme

Thesis Advisor: Asst. Prof. Dr. Mustafa Berke YELTEN

JUNE 2019

İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

MOSFET DC KARAKTERİSTİĞİNİN KRİYOJENİK KOŞULLARDA BSIM3 İLE İSTATİSTİKSEL OLARAK MODELLENMESİ

YÜKSEK LİSANS TEZİ

Aykut KABAOĞLU
(504161205)

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Programı

Tez Danışmanı: Asst. Prof. Dr. Mustafa Berke YELTEN

HAZİRAN 2019

Aykut KABAOĞLU, a M.Sc. student of ITU Graduate School of Science Engineering and Technology 504161205 successfully defended the thesis entitled “STATISTICAL CRYOGENIC MODELING METHODOLOGY OF MOSFET DC CHARACTERISTICS IN BSIM3”, which he/she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor : **Asst. Prof. Dr. Mustafa Berke YELTEN** ....
Istanbul Technical University

Jury Members : **Asst. Prof. Dr. Onur FERHANOĞLU** ....
Istanbul Technical University

Prof. Dr. Günhan DÜNDAR ....
Boğaziçi University

....

Date of Submission : **3 May 2019**
Date of Defense : **14 June 2019**

FOREWORD

Foremost, I would like to thank to my supervisor Asst. Prof. Dr. Mustafa Berke Yelten for all of his support and guidance during my academic life and M.Sc. thesis.

I appreciate ITU Duran Leblebici VLSI Laboratory members, specially, Sadık İlik for his efforts in measurements of this work.

I would also like to express my gratitude to my family for their continuous support through all my life.

This work was sponsored by the Technological Research Council of Turkey under the project TÜBİTAK 1001 215E080 and thanks for their contribution.

June 2019 Aykut KABAOĞLU

TABLE OF CONTENTS

Page

ABBREVIATIONS

CAD	**:** Computer Aided Design
MOSFET	**:** Metal Oxide Semiconductor Field Effect Transistor
UMC	**:** United Microelectronics Corporation
BSIM	**:** Berkeley Short-channel Insulated-Gate-Field-Effect-Transistor Model
CAD	**:** Computer Aided Design
EKV	**:** Transistor Model Developed by C. C. Enz, F. Krummenacher and E. A. Vittoz
PSP	**:** Penn State Philips Transistor Model
VDSAT	**:** Drain Saturation Voltage
VSAT	**:** Velocity Saturation
NMOS	**:** n-type MOSFET
PMOS	**:** p-type MOSFET
VDS	**:** Drain-Source Voltage
VGS	**:** Gate-Source Voltage
VTH	**:** Threshold Voltage
RF	**:** Radio Frequency
LN2	**:** Liquid Nitrogen
GHZ	**:** Gigahertz

SYMBOLS

^oC : Temperature in Celcius
I : Current
V : Voltage
A : Ampere
σ : Standard Deviation
ρ : Fixing coefficient for current equations
μ : Micro
V_{th0} : Threshold voltage at $V_{BS} = 0$ for Large length
V_{fb} : Flat-band voltage
$K1$: First order body effect coefficient
$K2$: Second order body effect coefficient
U_0 : Mobility at Temp. = 27^oC
U_a : First-order mobility degradation coefficient
U_b : Second-order mobility degradation coefficient
U_c : Body-effect of mobility degradation coefficient
UTE : Mobility temperature exponent
KT_1 : Temperature coefficient for threshold voltage
KT_{1L} : Channel length dependence of temperature coefficient for threshold voltage
KT_2 : Body-bias coefficient of Vth temperature effect
U_{a1} : Temperature coefficient for U_a
U_{b1} : Temperature coefficient for U_b
U_{c1} : Temperature coefficient for U_c
AT : Temperature coefficient for saturation velocity

LIST OF TABLES

LIST OF FIGURES

Page

STATISTICAL CRYOGENIC MODELING METHODOLOGY OF MOSFET DC CHARACTERISTICS IN BSIM3

SUMMARY

Electronic design automation tools (EDA) and electronic computer-aided design softwares (ECAD) use industrial standard models to converge the simulation results to realistic attitudes of devices. These models can satisfy meaningful simulation results only for a specific temperature range and they are generally extracted under room temperature circumstances. BSIM3 is one of the most commonly used model standard in the industry and supports only between -55^{o}C and 125^{o}C. There is a need to model cryogenic conditions to be able to produce trustworthy designs for extreme environment electronics such as military and space applications. A methodology has developed to produce a new model file with only modifying temperature dependency parameters analytically; therefore, there is no need to use iterative model extraction methods also, more robust model files can be obtained with this methodology. In the proposed automation system, mobility, threshold voltage and velocity saturation changes are taken into account and BSIM3 equations are used to compute the temperature dependency parameters of these phenomenas.

The methodology has been developed in MATLAB to calibrate temperature dependency parameters of BSIM3. Rather than modifying BSIM3 equations, the algorithm only changes the values of relevant parameters through analytical operations. Resulting cryogenic models have been extensively verified through device measurements performed on a cryogenic probe station cooled by liquid nitrogen ($-196^{o}C$). The model can estimate with an error of less than 5% the $I_D - V_{GS}$ and $I_D - V_{DS}$ curves of transistors having different channel lengths and widths. Statistical analysis of cryogenic measurements is used to introduce variation levels on top of regular cryogenic operations to identify the impact of process variations of cryogenic conditions. Models adjusted to various temperatures between $-196^{o}C$ and $-40^{o}C$ are have been accomplished for applications requiring a broader range of cryogenic operating temperature. Experimental data collected from a ring oscillator is used to visualize the model performance in estimating the cryogenic characteristics of a circuit. Distortions on the I-V curves of simulation results have been suppressed and average errors of various sizes NMOS and PMOS transistors for 0.18 μm technology has been reduced significantly by using this methodology.

MOSFET DC KARAKTERİSTİĞİNİN KRİYOJENİK KOŞULLARDA BSIM3 İLE İSTATİSTİKSEL OLARAK MODELLENMESİ

ÖZET

Elektronik devre tasarımları bilgisayar destekli benzetim programları aracılığıyla test edilirken endüstriyel model standartları kullanılır ve bu standartlar transistör seviyesinde hesaplamalar yaparak istenilen çıktıları gösterir. Simülasyon programlarında kullanılan model standartları elle çözülemeyecek kadar karmaşık seviyede akım-gerilim denklemlerinden oluşur ve bu denklemlerin içerisinde sıcaklığa bağımlı birçok parametre yer alır. Kullanılan transistör teknoloisine göre üreticiler model parametrelerini tasarımcılara verirler ve bu parametreler yalnızca belli bir sıcaklık aralığında anlamlı sonuçlar üretirler. Bu aralık dışında gerçekleştirilen benzetimler; sıcaklık aralığından uzaklaşıldıkça gerçeğe daha uzak sonuçlar vermektedirler.

Sağlanan model parametreleri oda sıcaklığı referans alınarak oluşturulurlar. Endüstride en çok kullanılan modellerden bir tanesi BSIM3 standartlarıdır. BSIM3, -55^oC ile 125^oC derece sıcaklık aralığında düzgün sonuç verebileceğini garanti eder ve yapılan benzetimlerde oda sıcaklığından uzaklaştıkça hata miktarı bu aralıkta kalınsa bile artmaktadır. Çünkü sıcaklığa bağlı parametreler, benzetim sıcaklığının oda sıcaklığından farkı ile çarpan durumundadırlar ve oda sıcaklığından uzaklaşıldıkça parametrenin sonuca etkisi artmaktadır. Düşük sıcaklıklarda çalışılması gereken ortamlarda bu etki dikkate alınmalıdır, standart modeller kullanıldığında devre performansı tamamen değişmektedir. Oda sıcaklığından çok daha düşük sıcaklıklarda çalışılan alanların başında uzay elektroniği, kuantum elektroniği ve savunma sanayii gelmektedir. Çalışmada hedef olarak uzay koşulları seçilmiştir. Ay yüzeyi veya Uluslararası Uzay İstasyonu dikkate alındığında -150^oC derece sıcaklıklar görülmekte, uzay boşluğunda ise bu değer -270^oC derecelere ulaşabilmektedir. Üreticilerin yayınladığı standart modeller bu sıcaklıklar için kullanılamazlar aksi halde devre performansı beklenenden çok farklı olur veya devre tamamıyla çalışmaz hale gelebilir. Üretim sonrası bu tip sorunlarla karşılaşmamak için benzetim sonuçlarının düşük sıcaklıklar için de gerçek performans değerlerine yakınsanması gerekmektedir.

Yaklaşık olarak -150^oC derecenin altında sıcaklığa sahip ortamlar kriyojenik olarak adlandırılır. Kriyojenik koşullar gibi uç noktalarda çalışacak devreler için yeni transistör modelleri oluşturulması gerekmektedir aksi durumda benzetim sonuçları üretilecek devre ile çok farklı olacaktır. Bu çalışmada kriyojenik ortamlarda transistörlerin DC karakteristiğindeki değişimler incelenmiş ve endüstriyel seviyede kullanılan benzetim programlarının anlamlı sonuç üretebilmesi için BSIM3 standardı bozulmadan MOSFET modellerinin; sıcaklık katsayılarının otomatik olarak değiştirilebileceği bir yöntem bilim önerilmiş ve gerçeklenmiştir. Model oluşturmak için üreticilerin de kullandığı çeşitli programlar mevcuttur ancak bu programlar iteratif yöntemlerle ölçüm sonuçlarını, model sonuçlarına yakınsayarak model parametreleri üzerinde rastlantısal değişiklikler gerçekleştirerek en uygun değerleri

elde etmeye çalışırlar. Önerilen yöntemde ise geliştirilen algoritma iteratif yöntemleri değil, BSIM denklemlerini ele alarak ölçüm sonuçlarında gözlemlenen değişimlerin fiziksel etkilerini ayrı ayrı inceler ve gerekli denklemleri bağımsız olarak ele alır. Fiziksel etkiyi modelleyen parametreyi, denklemlerin ölçüm sonuçlarına eşitlenerek çözdürülmesiyle elde eder. Bu sayede yeni parametre setinin fiziksel olarak anlamlı şekilde oluşturulmasıyla daha geniş sıcaklık aralığında da sonuçların benzer kalması ve hata oranlarının doğrusal olarak değişmesi beklenmektedir.

Sıcaklık düştükçe transistör karakteristiğinde en dikkat çekici iki fiziksel etki; mobilite ve eşik gerilimindeki değişimlerdir. Mobilite, yük taşıyıcılarının elektrik alan içerisindeki hareket kabiliyetlerini temsil eder ve sıcaklık düştükçe taşıyıcıların saçılma miktarlarında düşüş yaşandığı için mobilitede artış yaşanır. Mobilitedeki artış aynı gerilim altında bir MOSFET'in üzerinden geçen akım miktarının artması demektir ve akım değerleri transistör boyutuna bağlı olarak oda sıcaklığı referans alındığında 3 katın üzerine çıkabilmektedir. Kanal boyu daraldıkça akım artış miktarı uzun kanallara göre daha azdır. Yine sıcaklık düşüşü ile birlikte MOSFET içerisinde yüzey gerilimindeki artıştan kaynaklı olarak fakirleşmiş bölgenin genişlediği gözlemlenir bu sebeple MOSFET'in aktif hale geçtiği bir başka deyişle eşik gerilimine ulaştığı anda kanalda yer alması gereken taşıyıcı yoğunluğuna erişmek için daha çok enerjiye ihtiyaç duyulur; yani eşik gerilimi sıcaklığın düşmesiyle birlikte artar.

Çalışma içerisinde önerilen yöntem ile fiziksel etkileri temsil eden eşitlikler içerisindeki sıcaklığa bağımlı parametreler MATLAB üzerinde gerçeklenen algoritma aracılığı ile sırayla hesaplanır. Algoritma Cadence Analog Design Environment benzetim programı ile paralel olarak çalışır. BSIM3 standardının, MOSFET'lerin DC karakteristiğini simgeleyen yayınlanmış tüm eşitlikleri algoritma içerisine eklenmiştir. Ancak yayınlanan BSIM3 eşitlikleri tüm denklemleri içermez ve benzetim programları yayınlanmış denklemler dışında hesaplamaları da sisteme dahil ederler. Simülatörlerin kullandığı eşitlikler ile algoritmaya dahil edilmiş BSIM eşitliklerini örtüştürmek için MATLAB'de hesaplanan akım değeri ile simülatörden elde edilen akım değeri arasındaki fark bir katsayı yardımı ile giderilir ve bu hesaplanan katsayı algoritma içerisinde daha sonra tekrar kullanılacak olan BSIM3 eşitlikleri içerisine dahil edilir. Hesaplamanın gerçekleştirilmesi için kullanılacak olan teknolojideki bir MOSFET'in istenen sıcaklıkta ölçümü alınmalı ve bu ölçüm sonucu algoritmaya dahil edilmelidir. Sistem önce soğuktaki ölçüm sonuçlarını alıp BSIM eşitliklerini kullanarak ölçümü yapılan sıcaklıkta hesaplama yapar ve hesaplanan ile ölçüm arasındaki farkı sıcaklık ile çarpan olarak gelen parametreleri değiştirerek giderir. Parametrelerin değiştirilmesi önce eşik geriliminin hesaplanması ile başlar. Yeni eşik gerimi oluşturulduktan sonra tekrar benzetim yapılır ve elde edilen sonuçlar sisteme dahil edilerek sırasıyla mobilite ve doyma hızı parametreleri hesap edilir. Bu fiziksel etkileri gövde gerilimi sıfır olmayan durumlar için modelleyen ayrı parametreler vardır. Her bir eşitlik tekrardan farklı gövde gerilimi ölçümü dikkate alınarak hesap edilir. Tüm işlemlerin sonunda algoritma kriyojenik ölçüm sonuçlarını yakınsayacak yeni bir parametre dosyası oluşturur ve bu dosya BSIM3 standardını destekleyen herhangi bir benzetim programı üzerinde çalıştırılarak karmaşık devrelerin kriyojenik ortamlar için davranışı incelenebilir.

Çalışmada, algoritmanın doğrulanması için 0.18 μm teknolojisinde farklı kanal boyu ve genişliklere sahip MOSFET'ler sıvı azot altında ölçülmüştür. Sıvı azot -196^{o}C derece kaynama sıcaklığına sahiptir ve uzay boşluğu hariç uzay koşullarına benzer koşulları elde edebilmek için doğada bulunan en uygun ve en çok kullanılan malzemedir. İTÜ VLSI Duran Leblebici Laboratuvarı'nda bulunan kriyojenik ölçüm istasyonu vasıtasıyla ölçümler alınmıştır. Ölçümler paketsiz olarak üretilmiş olan kırmıklar üzerinde yapılmış ve farklı boyutta transistörler kullanılmıştır. Her boyuttaki transistör için 10'ar adet ölçüm yapılarak istatistiksel analizler elde edilmiştir. Daha sonra ölçüm sonuçları algoritma üzerinde çalıştırılarak yeni model dosyaları oluşturulmuş ve bu model dosyaları Cadence Analog Design Environment benzetim programı üzerinde çalıştırılarak, ham BSIM3 model sonuçları ile karşılaştırılmıştır. Değiştirilmemiş model parametreleri ile yapılan benzetim sonuçlarıyla ölçüm sonuçları arasında %100'e kadar varabilen hatalar gözlemlenirken, algoritma vasıtasıyla oluşturulan yeni modellerin hata oranları farklı boyutlara sahip tüm MOSFET'ler için %5'in altına indirilmiştir. Farklı boyutlara sahip MOSFET'ler üzerinde sıcaklık değişiminin etkisi incelenmiş ve sonuçlar aktarılmıştır. MOSFET seviyesinde gösterilen sonuçların ardından modeller ring osilatör devresi üzerinde de kullanılmış ve ölçüm sonuçları ile doğrulanmıştır. Böylelikle kriojenik koşulların MOSFET'ler üzerindeki fiziksel etkileri incelenmiş, bu koşullar için model üreten algoritma oluşturulmuş, farklı boyutlardaki MOSFET'lerden, -196^oC derecede sonuçlar alınmış ve bu sonuçlar ile modeller üretilip benzetim sonuçları, ölçüm sonuçları ile kıyaslanmıştır. Hem ölçüm sonuçlarının hem de yeni oluşturulan modellerin istatistiksel analizleri paylaşılarak modelleme için tüm kriterler çalışma içerisinde incelenmiş ve sonuçlarla sergilenmiştir.

1. INTRODUCTION

Semiconductor device characteristics strongly depend on operation temperature thus the circuit performance alters in response to a temperature change. This performance variation should be carefully captured to model and design electronic circuits for extreme environments (such as space applications). Traditional models are not sufficient to account for these changes as they only focus on a limited temperature range considered as nominal. Most of the designs which have been realized using a CAD (computer aided design) tool at typical conditions may not work properly in low temperature environments. Hence, the equations have been derived to model the low temperature characteristics of MOSFETs. These equations are mostly semi-empirical and new parameters have been introduced to fit the measurement data by using polynomial equations without considering common model standards in the industry [2]. The situation gets even more complicated when these equations are translated into simulations because, a new module should be designed and implemented into the simulation tool. Therefore, there is a need to optimize the current model files used in simulations for low temperature (also called cryogenic) applications. Circuits in space or other extreme environment applications must be accurate and reliable. When developing models for such applications, a more mature technology is preferred as it contains the least number of manufacturing variations. In this work, UMC 180 nm technology along with its BSIM 3v3 model are used to improve the current transistor model at cryogenic conditions. In BSIM3, thermal changes are modeled by inserting binning parameters into equations of mobility, threshold voltage, drain-source parasitic resistance and saturation velocity [3]. Because temperature binning parameters are fit in a limited temperature range, they cannot describe the correct *I-V* characteristics of a MOSFET in cryogenic conditions. Thus, an automated tool is developed to find revised binning parameters that will hold in cryogenic conditions without creating new equations and substantially changing the transistor model. After parameters have been extracted by the algorithm, resulting model file can be employed within any simulation tool that supports BSIM3.

1.1 Literature Review

Cryogenic operation of MOSFETs has been a focus of research for the last few decades [4]. The main effect in all studies concentrated on an accurate modeling strategy to capture the DC characteristics of MOSFETs at cryogenic temperatures [2,5–15]. These modeling approaches have been implemented in different MOSFET model standards including BSIM, EKV and PSP.

The contribution of this thesis mainly lies in extending the capabilities of a cryogenic transistor model to include the impact of device variability as well as to investigate the device characteristics over a broader range of low temperatures. These aspects are especially crucial for circuits that will be used in an application when the operation temperature is not fixed and can vary significantly as in the case of space electronics. Besides, device variability can also alter the cryogenic circuit behavior and should properly be accounted for the transistor model so that designers become sufficiently informed in advance how the cryogenic characteristics are changed with process variations. The major points of our approach can be summarized as follows: 1) BSIM3 equations are kept in fact and an algorithm to calibrate the temperature dependency parameters has been developed thereby avoiding iterative solutions. 2) The impact of device sizes on the cryogenic operation has been investigated. It is shown that the channel length has a decisive role in the device characteristics changes observed and transistor model should be crafted such that this role is correctly reflected in them. 3) Different intermediate low temperatures between the liquid nitrogen temperature ($-196^{o}C$) and the room temperature have been considered for model extraction.Various measurements have been performed to analyze device variability; additionally, $\pm 3\sigma$ (of the measurement variation) values have been introduced to the model to represent the "corners" of the measurement data. Resulting models have been validated experimentally on a 7 stage ring oscillator.

The thesis organization can be given as follows: Section I describes the temperature dependent BSIM parameters and the coefficients that control the level of this temperature dependency. Section II explains in detail the modeling methodology.

Experimental results as well as the performance of the proposed modeling approach are discussed in Section III. Finally, conclusions are provided in Section IV.

1.2 The Temperature Dependency Parameters

1.2.1 Mobility (μ)

The mobility of charge carriers describes the relationship of the velocity of charge carriers with the electric field acting on them [16]. The major scattering mechanisms that limit the carrier mobility are phonon scatterings and surface roughness [17] [18]. The decrease in lattice vibration due to temperature drop causes scattering mechanisms to reduce in magnitude; moreover, the mobility increases because of this reduction. At high temperatures, the carrier density is proportional to the intrinsic carrier concentration and when the temperature is close to the room temperature, the carrier density is assumed to be equal to the doping concentration. However, the carrier density decreases at lower temperatures and the freeze-out effect can take place [19]. While the temperature is decreasing, the mobility does not increase anymore and it starts to fall below a certain temperature depending on the technology due to lack of kinetic energy of charge carriers. The freeze-out impact becomes evident at much lower temperatures as the device technology scales down since the doping concentration increases with every technology node [20]. In addition to device sizes, lateral non-uniform doping techniques change the freeze-out effect onset temperature depending on the doping concentration.

Generally, the vertical electric field of MOSFETs degrades mobility. When the gate voltage increases, mobility degradation effect rises due to scattering becomes enhanced [21]. The mobility degradation is also affected by device scaling, as it increases when the channel length is scaled down [22].

In BSIM3, three distinct mobility models are used and each mobility model has four different parameters which are U_0, U_a, U_b and U_c as shown in (1.1-1.5) [23].

$$\mu_{eff} = {}^{U_0}\!\Big/\!{}_{(1+(U_a+U_cV_{bseff})\frac{(V_{gsteff}+2V_{th})}{Tox}+U_b\frac{(V_{gsteff}+2V_{th})^2}{Tox})} \tag{1.1}$$

The zero field mobility U_0 has a temperature dependency parameter UTE which changes U_0 exponentially in response to a temperature change (1.2). U_a (first order mobility degradation), U_b (parabolic mobility degradation) and U_c (body effect coefficient of mobility degradation) are binning parameters to model the effective gate voltage impact [24]. U_{a1}, U_{b1} and U_{c1} are sub-parameters of U_a, U_b and U_c to indicate their temperature dependence, respectively (1.3-1.5). UTE has the dominant impact on the mobility change among all.

$$U_0(T) = \mu_0 \cdot ({}^{T}/{}_{T_{nom}})^{UTE} \tag{1.2}$$

$$U_a(T) = UA + UA1 \cdot ({}^{T}/{}_{T_{nom}} - 1) \tag{1.3}$$

$$U_b(T) = UB + UB1 \cdot ({}^{T}/{}_{T_{nom}} - 1) \tag{1.4}$$

$$U_c(T) = UC + UC1 \cdot ({}^{T}/{}_{T_{nom}} - 1) \tag{1.5}$$

1.2.2 Threshold voltage (V_{th})

The intrinsic doping concentration has an exponential dependence of temperature and more gate voltage is needed to obtain the same channel charge concentration at lower temperatures [25]. Temperature changes affect the work function. Increase in surface potential leads to a larger depletion charge; additionally, the decrease in thermal energy causes slower ionization of channel dopants. [5]. In short, the increase in Fermi potential causes a rise in V_{th} [20]. In BSIM3, V_{th} is described in a tedious equation (1.6) and temperature dependency of the threshold voltage is included within the parameter V_{th0} [23]. $V_{th0}(T_{nom})$ specifies the threshold voltage of a device without short channel effects at zero body bias. Three further parameters, $KT1$, $KT1L$, $KT2$, characterize $V_{th0}(T)$ at an arbitrary temperature T as shown in (1.7) [23].

$$\begin{aligned} V_{th} = {} & V_{th0}(T) + K_1\sqrt{\phi_s - V_{bseff}} - K_2 V_{bseff} + K_1(\sqrt{1 + \frac{N_{lx}}{L_{eff}}} \\ & - 1)\sqrt{\phi_s} + (K_3 + K_{3b}V_{bseff})(\frac{T_{ox}}{(W_{eff} + W_0)})\phi_s \\ & - D_{vt0w}(e^{-\frac{D_{vt1w}W_{eff}L_{eff}}{2ltw}} + 2e^{-\frac{D_{vt1w}W_{eff}L_{eff}}{ltw}})(V_{bi} - \phi_s) \\ & - D_{vt0}(e^{-\frac{D_{vt1}L_{eff}}{2lt}} + 2e^{-\frac{D_{vt1}L_{eff}}{lt}})(V_t ln[\frac{N_{ch}N_{DS}}{n_i^2}] - \phi_s) \\ & - (e^{-\frac{D_{sub}L_{eff}}{2lto}} + 2e^{-\frac{D_{sub}L_{eff}}{lto}})(E_{tao} + E_{tab}V_{bseff})V_{DS} \end{aligned} \tag{1.6}$$

$$\begin{aligned} V_{th0}(T) = {} & V_{th0}(T_{nom}) + (KT1 + KT1L/L_{eff} \\ & + KT2 \cdot V_{bseff}) \cdot ({}^{T}/{}_{T_{nom}} - 1) \end{aligned} \tag{1.7}$$

While $KT1$ is the dominant parameter to describe the temperature dependency of V_{th}, $KT1L$ improves the fitting for various channel length sizes and $KT2$ models the temperature dependency of the body effect on V_{th0} [24].

1.2.3 Saturation velocity (v_{sat})

In short channel devices, drain saturation voltage (V_{dsat}) is used to mark the onset of velocity saturation rather than the conventional pinch-off assumption [2]. When a certain lateral electric field is attained, MOSFETs get into saturation region since carriers cannot move faster than v_{sat} [3]. The temperature dependence of v_{sat} is given in (1.8) [23].

$$v_{sat(T)} = v_{sat(Tnom)} - AT \cdot (T/Tnom - 1) \tag{1.8}$$

With temperature change, v_{sat} has a less evident impact compared to other parameters [26].

1.2.4 Drain-source parasitic resistance (R_{ds})

R_{ds} is called the parasitic drain-source resistance which includes different resistances such as the contact resistance, the diffusion resistance between the contact and the gate edge and the crowding resistance near the gate [2]. In BSIM3, R_{ds} has a fitting parameter R_{dsw} in (1.9); additionally, (1.10) is used to characterize the temperature dependence where PRT is the temperature coefficient [23]. Even though some methods have been developed to extract the drain-source parasitic resistance, R_{ds} change resembles mobility degradation and they can be treated similarly [27].

$$\begin{aligned} R_{ds} = (&R_{dsw}[1 + P_{rwg} \cdot V_{gsteff} + P_{rwb} \\ &\times (\sqrt{\varphi_s - V_{bseff}}) - \sqrt{\varphi_s})])/(10^6 \cdot W_{eff'})^{(W_r)} \end{aligned} \tag{1.9}$$

$$R_{dsw(T)} = R_{dsw(Tnom)} + PRT \cdot (T/T_{nom} - 1) \tag{1.10}$$

2. PROPOSED MODEL

2.1 Temperature Model Parameter Calibration Methodology

An algorithm is developed to change the temperature dependency model parameters in BSIM3(3v3) to make the models accurate for cryogenic applications. In this methodology, there is no need to adjust all coefficients of relevant equations as most model optimizers typically do. The algorithm modifies only the coefficients of temperature analytically. BSIM3 equations are used directly to calculate these parameters analytically. Because no equation of BSIM3 was manipulated, the extracted model can be used with any simulation tool supporting BSIM model file.

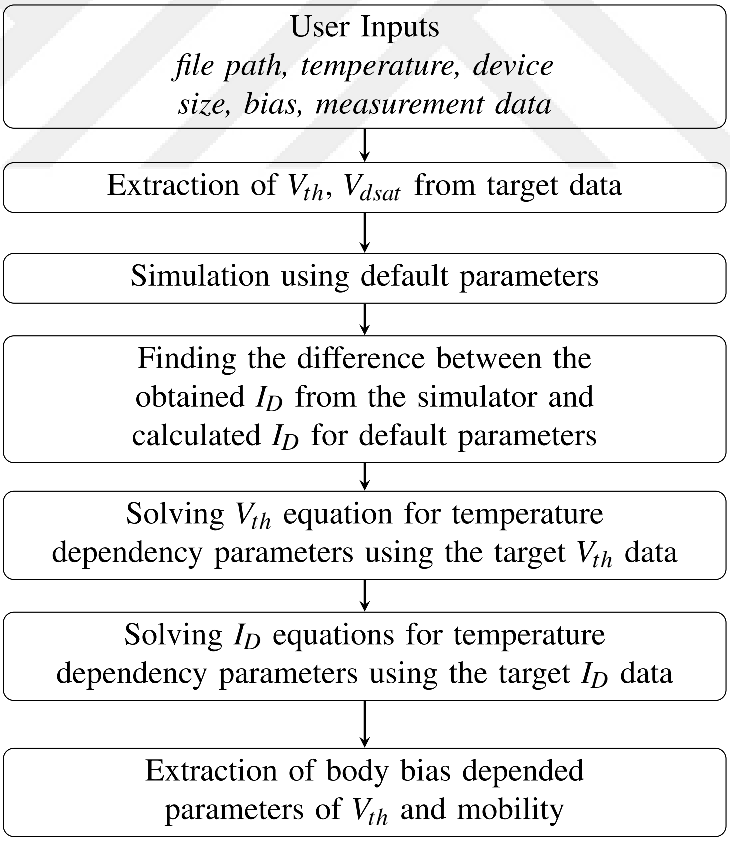


Figure 2.1 : The flowchart of the proposed methodology [1]

The algorithm was developed on MATLAB and the MATLAB runs circuit simulations on CADENCE Design Systems Spectre by using Ocean scripts. When MATLAB got the necessary input data, it calls the Ocean scripts and imports simulation results which were written to a file after completion of simulations. Inputs required are the temperature of the experiment, $I-V$ curves of measurements, biasing information, device sizes and the model file path. Subsequently, MATLAB starts to compute the temperature dependency parameters step by step through backward solving of BSIM3 equations. All steps to extract a new model file from measurement data are shown in Fig. 2.1

2.1.1 Processing the target data

When the temperature of interest is not within the range of BSIM (i.e. below -55^oC), device measurements should be collected to optimize relevant BSIM parameters for the desired temperature. Firstly, the algorithm extracts the maximum device current at $V_{DS}=V_{GS}=1.8V$, as well as corresponding V_{th} and V_{dsat}. There are numerous methods in the literature to extract V_{th} from the $I-V$ curve of a transistor. In this work, two of these methods were considered; the first one is finding the intersection point of the voltage axis and the line extrapolated at the maximum value of the first derivative of the I_D-V_{GS} curve as shown in Fig. 2.2. The second one is taking the voltage that points the maximum value of second derivative of the normalized I_D-V_{GS} curve (Fig. 2.3). In order to remove the computational noise, a smoothing filter should be applied so that a meaningful threshold voltage value can be obtained [28]. This method sometimes results in an error because of the floating measurement data and insufficient filtering. Nevertheless, the second derivative method has been tested using the room temperature data and it yields a more accurate V_{th} value with respect to simulation results. Therefore, both the $I-V$ curve extrapolation and second derivative methods are used concurrently for a reliable and accurate V_{th} extraction. Both procedures were applied at low V_{DS} as traditional V_{th} extraction methodology requires.

Another necessary step to mark the velocity saturation is V_{dsat} extraction from the I_D-V_{DS} curve. Both room temperature and cryogenic measurements were taken into account and the difference in V_{dsat} values of both curves are extracted because there is no exact method to determine V_{dsat} value alone using the $I-V$ curve of the device. Fig. 2.4 shows the extraction method where two lines are drawn by extrapolating $I-V$ curve at the minimum and maximum value points of the first derivative. Intersection

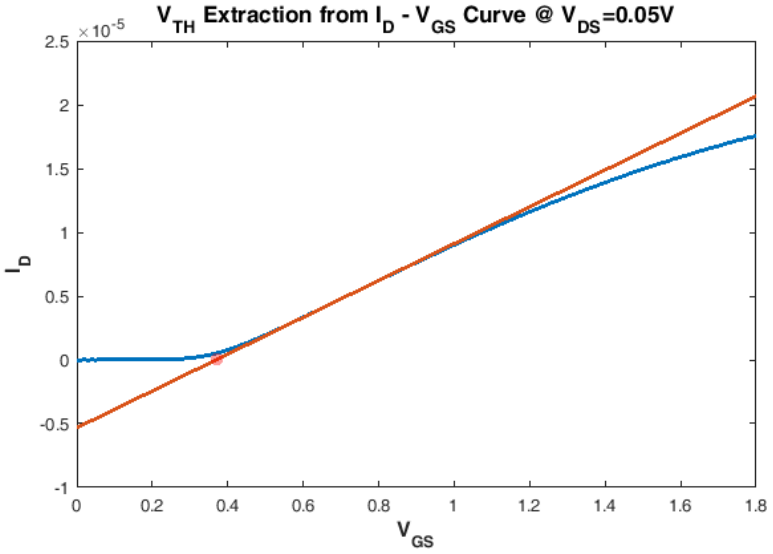


Figure 2.2 : Demonstration of the extrapolation method for V_{TH} extraction

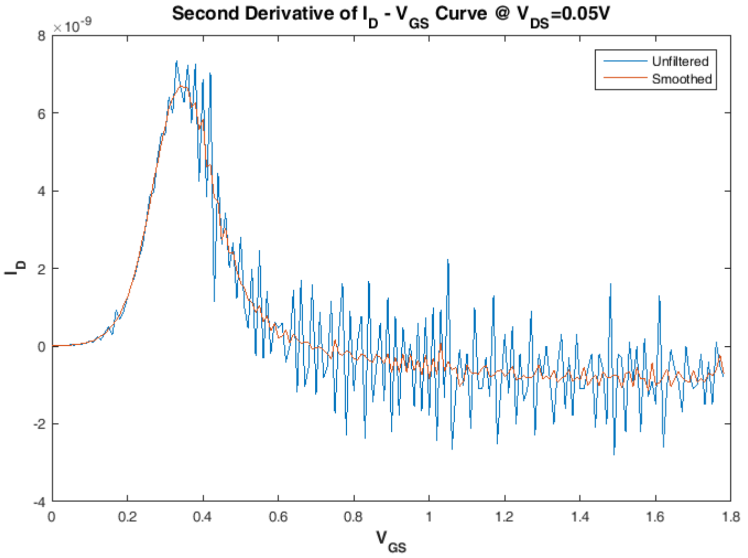


Figure 2.3 : Demonstration of the second derivative method for V_{TH} extraction

points of these lines are taken as V_{dsat}. The difference of the V_{dsat} values are then used by the proposed modeling algorithm to calculate the temperature dependency parameter of v_{sat}.

2.1.2 Fixing BSIM equations

Published BSIM equations do not exactly correspond to the equations used in the simulator [23]. Since the simulator has a modified version of published BSIM equations, results of the equations calculated in MATLAB should be adjusted. A correction coefficient (ρ) has been introduced to the I_D equation to eliminate this difference. ρ is extracted by subtracting the current value calculated with the

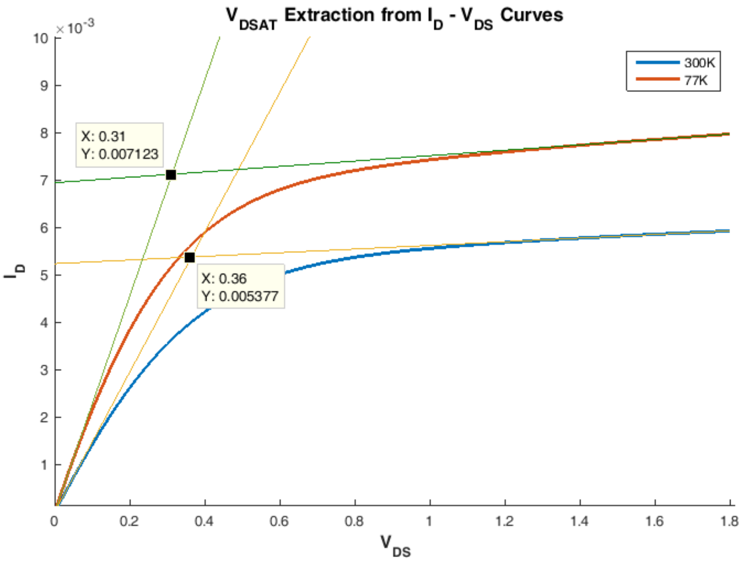


Figure 2.4 : Demonstration of the extraction of V_{DSAT} change between the room and cryogenic temperature

BSIM equations in MATLAB, from the current value simulated with initial model parameters at the highest bias used in measurements, i.e. $V_{DS} = V_{GS} = 1.8\ V$. This choice of the bias will result in the maximum error to be observed. Based on this coefficient, MATLAB can produce the current values closest to the simulator result so that equations can be used to solve the revised values of temperature dependency parameters in cryogenic conditions.

2.1.3 Parameter extraction algorithm

The algorithm employs target measurement data to extract the temperature dependency parameters vector in (2.1) that minimizes the modeling error.

$$\vec{v}=[KT1,\ KT1L,\ KT2,\ UTE,\ UB1,\ UC1,\ AT,\ DELTA] \tag{2.1}$$

The extraction methodology is composed of eight steps and they can be grouped 3 stages as shown in Fig. 2.5 which are 1) parameter extraction without body effect, 2) parameter extraction at a specified body bias, 3) V_{dsat} difference elimination. In the first stage $KT1$,UTE and $UB1$ will be evaluated without including the body effect. Then, $KT2$ and $UC1$ will be obtained at a specified body bias. V_{dsat} difference elimination consists of AT and $DELTA$ extraction. If the modeling of the channel length scaling for the threshold voltage is desired, finding $KT1L$ constitutes the sub-stage of the first stage and it is calculated after $KT1$ parameter has been obtained. A long channel

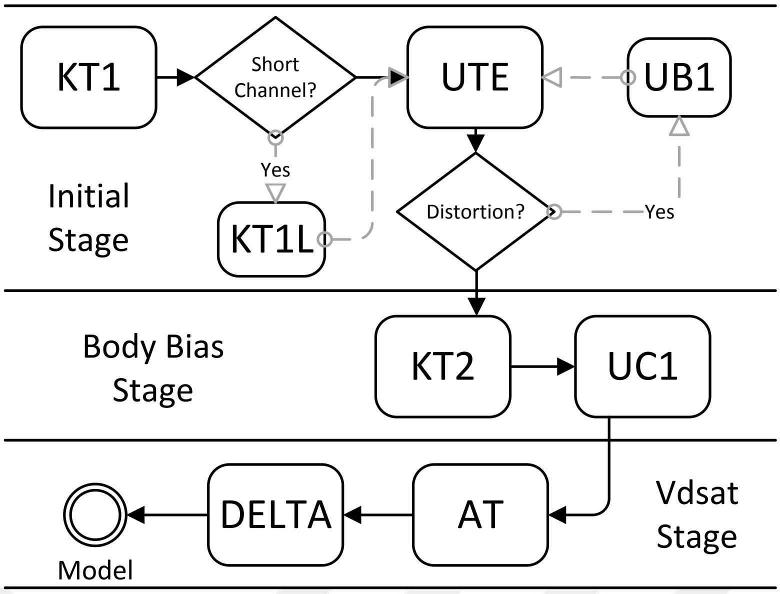


Figure 2.5 : Parameter Extraction Algorithm

and a short channel device are necessary for this sub-stage. All other steps can be implemented considering a long channel device. If a designer wants to use just short channel devices in his/her own design, there is no need to use $KT1L$ parameter, other stages will suffice to produce an accurate model for cryogenic conditions. R_{DS} was not included to the model extraction procedure due to the similarity between R_{DS} effect and mobility degradation.

Temperature change is modeled using $KT1, KT2, KT1L$ for the threshold voltage; $UTE, UB1, UC1$ for the mobility and AT for the V_{dsat}. Additionally, $DELTA$ specifies the smoothness of the discontinuity between the linear and saturation region of a transistor in the I_D-V_{DS} curve.

2.1.4 Computation cost of the methodology

The computation cost of the methodology consists of mostly circuit simulations done by the simulator, which means that the parameter extraction procedure takes much smaller time to complete. Extracted parameters are imported into the model file to perform simulations. Outcomes of these simulations are then used to validate new model parameters. Since the model generated should operate at different bias voltages for various device sizes, multiple simulations should run successively during model generation. Despite this simulation cost, the algorithm achieves its goal of providing a new model file suitable for the input cryogenic conditions in around 6 to 15 minutes depending on device properties. It should be mentioned that the model generation is done only once for a given device type to be operated at cryogenic temperatures. Furthermore, the algorithm is made robust toward handling numerical problems that might occur during analytic operations to extract the new device model parameters.

3. EXPERIMENTAL RESULTS

A tape-out using the commercially available 180 nm technology has been accomplished to experimentally verify the algorithm, with regular n-type and p-type MOSFETs that were measured at cryogenic conditions. NMOS and PMOS devices of 5 different sizes are used to investigate the size dependency of MOSFETs' operational behavior at low temperatures. Additionally, an RF NMOS and low threshold voltage NMOS are included in measurement chip to investigate the effects of different MOSFET designs; also, RF MOSFETs will be used for fundamental applications of space electronics. All measured transistor types and their sizes are itemized in Table 3.1 and these items numbers will be referred throughout the rest of this thesis to specify each transistor.

Table 3.1 : Device names and sizes

No	Type	Width	Length	No	Type	Width	Length
1	NMOS	0.24 μm	0.18 μm	7	PMOS	0.24 μm	0.18 μm
2	NMOS	10 μm	0.18 μm	8	PMOS	10 μm	0.18 μm
3	NMOS	0.24 μm	10 μm	9	PMOS	0.24 μm	10 μm
4	NMOS	10 μm	10 μm	10	PMOS	10 μm	10 μm
5	NMOS	35 μm	0.5 μm	11	PMOS	35 μm	0.5 μm
6	Low V_{TH} NMOS	35 μm	0.5 μm	12	RF NMOS	35 μm	0.18 μm

A large size transistor 4 was chosen to analyze physical changes in MOSFETs at low temperatures without considering short channel and narrow width effects. Transistors 2 and 3 are employed to check these effects individually at cryogenic conditions. Additionally, the smallest size transistor is used to observe both effects together. Transistor 5 is a control device and it has a moderately long channel with regard to transistor 1 and 4. Transistors like 5 are typically used in analog circuits. Besides, the cryogenic behavior of 5 acts as a bridge between the cryogenic characteristics of the long channel and short channel devices. The transistor numbers between 7-11 are same size PMOS transistor of 1-5 transistors. Therefore, the effects of cryogenic conditions on n-type and p-type transistors can be investigated separately and change of

Figure 3.1 : The measurement bench and probe station

model parameters can be considered individually. Aside from these, an RF transistor is considered to extract a model for RF circuit designs operating at very low temperatures. Because of the threshold voltage increase with temperature decrease, a low threshold voltage device 6 is considered of interest for digital applications. At least 10 chips from 3 wafers were put under test. Hence, the process variation and measurement errors can be considered in the research.

3.1 Measurement Setup

Unpackaged dies from 3 different wafers have been measured using the MDC 441 cryogenic probe station. Agilent Technology B1500A semiconductor device analyzer is used to extract *I-V* curves at different bias voltages. The temperature of the probe station chuck is monitored by a Keithley 2000 multimeter. The probe station is cooled by liquid nitrogen hence the chuck temperature decreased down to $-196°C$. In the probe station, the chips are vacuumed by a compressor for avoiding undesirable slide. The typical supply voltage for this technology is 1.8 V and the devices under test were biased at V_{GS} values between 0.6 V and 1.8 V to extract $I_D - V_{DS}$ curves. Also, the body effect was taken into account by changing V_{BS} from 0 down to -0.4 V. $I_D - V_{GS}$ curves were extracted in the same V_{BS} range by using two different V_{DS} values which

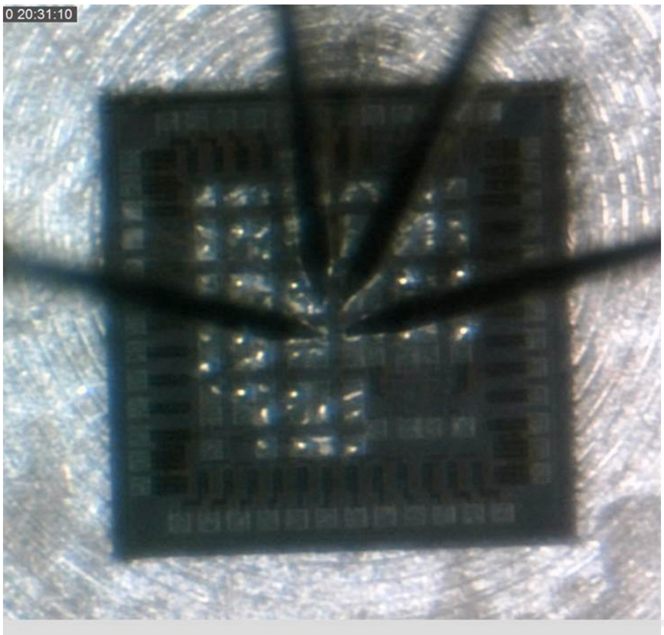


Figure 3.2 : The device under test

are 0.05 V and 1.8 V. Low V_{DS} is needed to capture the device threshold voltage. The measurement setup and the chip under test on the probe station are shown in Figs. 3.1 and 3.2. The measured dies are observed by microscope and DC probes of cryogenic measurement station are contacted with pads of each MOSFETs that are gate, drain, source, body contacts. The probes are moved manually and due to the sensitivity of measurement setup, these contacts are sometimes shorted as a result of touching probes to wrong areas. Therefore, some chips got lost and measurements were repeated again. This situation also creates measurement variation due to probe-pad contact. Before creating new model files, this case was taken into account and mean current values of measurements were used in the algorithm to suppress this measurement variation. The contacts of MOSFETs can be seen in the Fig. 3.3. The size of the die is $1.5m^2$ and each group of 4 pad represents one MOSFET.

3.2 Comparison of the Measurements between Cryogenic Temperature and Room Temperature

At both room temperature and cryogenic conditions, 10 different dies were measured for each size of NMOS and PMOS devices to extract the correct model parameters. The Figs. 3.4, 3.5 and 3.6 show $I_D - V_{GS}$ measurements at $V_{DS} = 0.05V$ to indicate V_{TH} increase as temperatures drop down. In Figs. 3.4a-3.4e, comparison of $I - V$

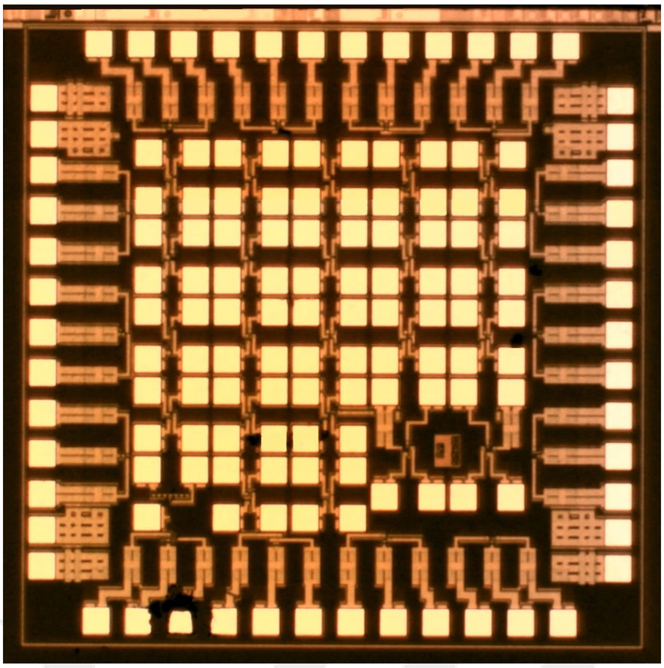
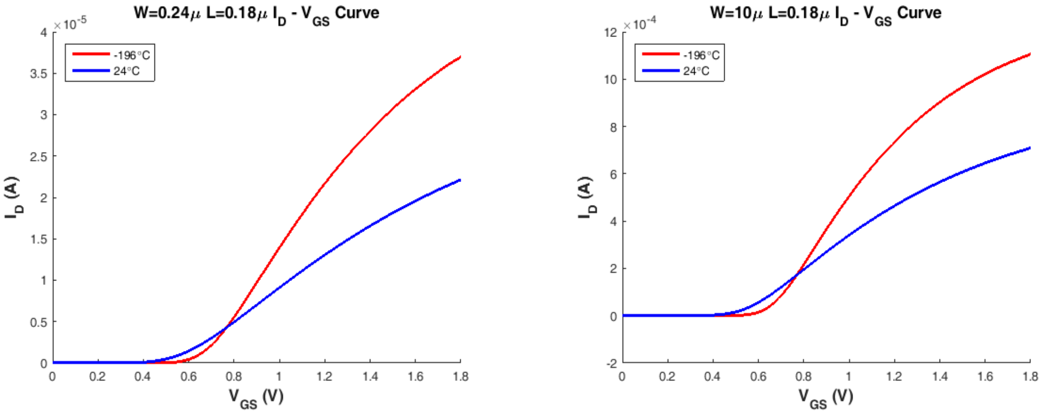


Figure 3.3 : The die layout observed with a microscope

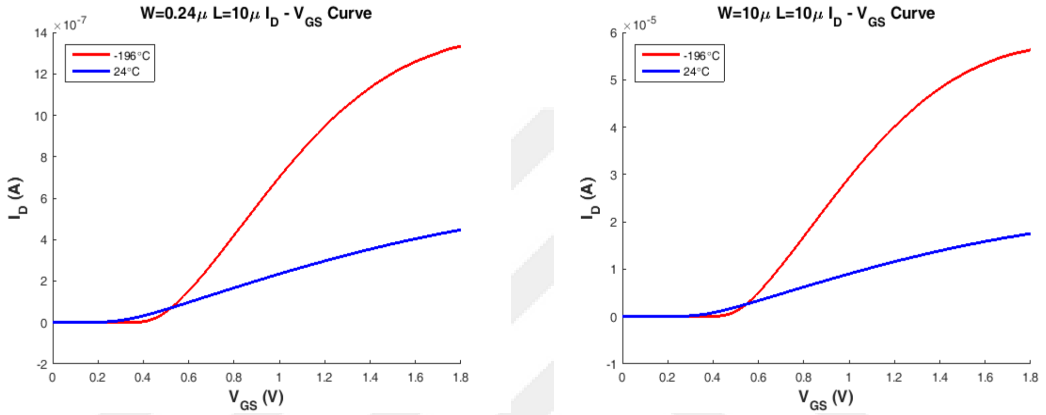
for NMOS devices of various sizes and in Figs. 3.5a-3.5e, comparison of $I-V$ for PMOS devices of various sizes are shown both at room and cryogenic temperatures. Additionally an RF-NMOS transistor with size of 35 $\mu m x 0.18$ μm and a low threshold voltage NMOS device with the same reference size transistor's measurement result are shown in Fig. 3.6a,3.6b.

The Figs. 3.7, 3.8 and 3.9 represent mean $I_D - V_{DS}$ curves of 10 measurements for each kind of transistor at $V_{GS} = 1.8V$ and $\pm 3\sigma$ values are found using the experimental data to show the statistical variance of transistors. All size of NMOS and PMOS device measurements are shown in Figs. 3.7a-3.7e and Figs. 3.8a-3.8e respectively. The RF-NMOS transistor and the low threshold NMOS device measurement results are also shown in Fig. 3.9a,3.9b.

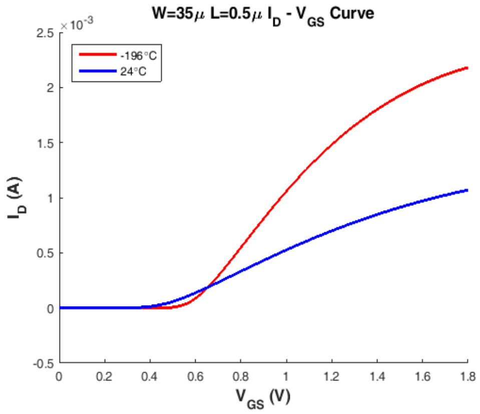
The mean curve of NMOS devices has variations between %0.9 and %6.6, in comparison to the simulation results at the typical (TT) corner found by simulating the default model parameter set provided by the manufacturing company. Current increase rates of devices with temperature decrease are not equal, they depend on device sizes. It is clear from Table 3.3, that the current increase ratios are strongly correlated with device lengths. Transistors 1 and 2 have the same length, different width and the increase rates are almost the same. When the device length is raised to



(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



(c) $W = 0.24\ \mu m, L = 10\ \mu m$ (d) $W = 10\ \mu m, L = 10\ \mu m$



(e) $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.4 : NMOS $I_D - V_{GS}$ Curve @ $V_{DS} = 0.05V$ demonstrating V_{TH} increase as temperatures drop down

10 μm from 0.18 μm, current increase ratios became around 6 times higher for NMOS devices and 5 times higher for PMOS devices. As the increase ratio became higher, larger device widths have a slight impact on the ratio. If process variations are taken into account, the ratio change due to width difference can be practically ignored. The situation can be explained as the basis of the difference between the short channel and

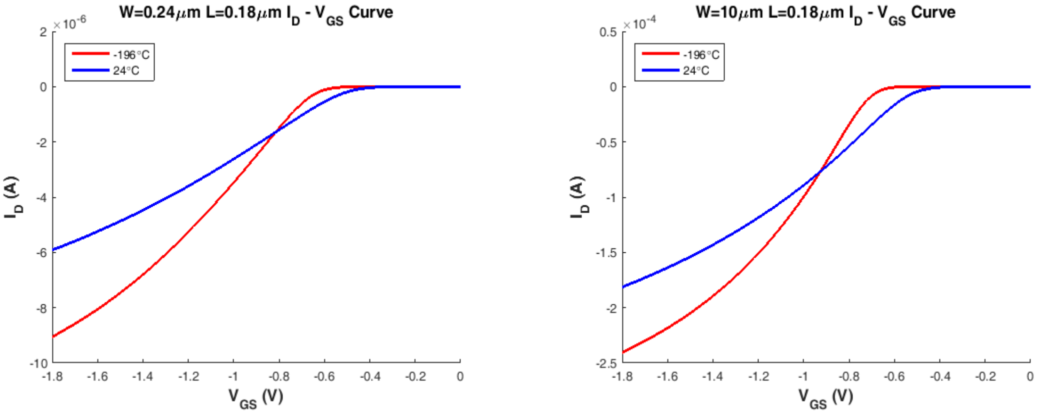
long channel transistors: In short channel transistors, charge carriers already operate at a large longitudinal electric field thus they are close to the velocity saturation regime, in which, the increase of the mobility at cryogenic temperatures does not increase the drain current. Conversely, in long channel transistors, charge carriers are far from velocity saturation, thus the low field mobility increase makes a greater impact on the drain current of the long channel transistor [25]. Because holes have less mobility, PMOS current increase amounts are not as remarkable as those of NMOS devices (Fig. 3.8a-3.8b).

Threshold voltage increase amounts for various transistors are shown in Table 3.2. These V_{TH} values are extracted from graphs with the method mentioned in section PROPOSED MODEL. Because of the threshold voltage extraction procedure sensitivity, it is hard to comment on the relationship between transistor sizes and threshold voltage increase. Thus, the size dependence of the threshold voltage increase can be practically ignored. All of the transistors have similar threshold voltage increase amounts because the bulk Fermi potential increase is independent of device size and the transistors get into the strong inversion regime when surface potential equals twice the bulk potential [29]. Therefore, it is assumed that the necessary gate voltage does not change with different device sizes to create the same surface potential.

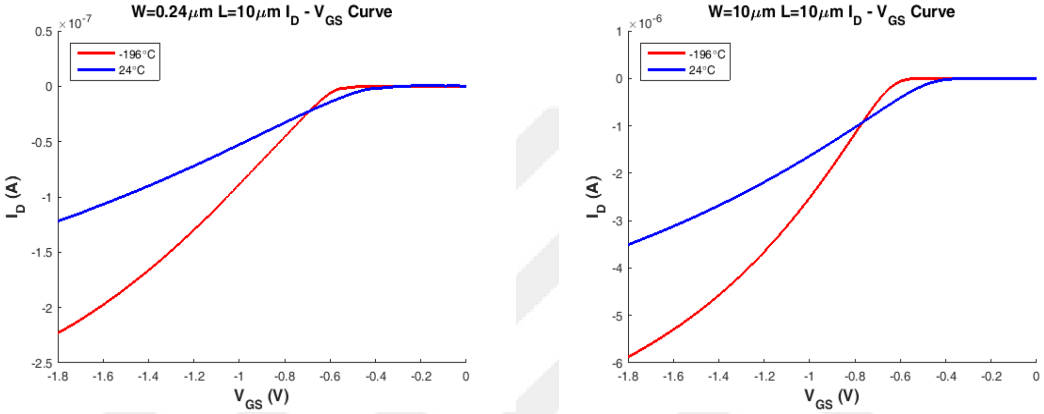
Table 3.2 : Threshold Voltage increase amounts

Type	Size($W \times L$)	Room Temp.	Cryogenic	Difference
NMOS	$0.24\ \mu m \times 0.18\ \mu m$	$0.54\ V$	$0.69\ V$	$0.15\ V$
NMOS	$10\ \mu m \times 0.18\ \mu m$	$0.53\ V$	$0.64\ V$	$0.11\ V$
NMOS	$0.24\ \mu m \times 10\ \mu m$	$0.30\ V$	$0.46\ V$	$0.16\ V$
NMOS	$10\ \mu m \times 10\ \mu m$	$0.34\ V$	$0.5\ V$	$0.16\ V$
NMOS	$35\ \mu m \times 0.5\ \mu m$	$0.44\ V$	$0.56\ V$	$0.12\ V$
PMOS	$0.24\ \mu m \times 0.18\ \mu m$	$-0.49\ V$	$-0.64\ V$	$-0.15\ V$
PMOS	$10\ \mu m \times 0.18\ \mu m$	$-0.52\ V$	$-0.69\ V$	$-0.17\ V$
PMOS	$0.24\ \mu m \times 10\ \mu m$	$-0.42\ V$	$-0.55\ V$	$-0.13\ V$
PMOS	$10\ \mu m \times 10\ \mu m$	$-0.46\ V$	$-0.62\ V$	$-0.16\ V$
PMOS	$35\ \mu m \times 0.5\ \mu m$	$-0.49\ V$	$-0.66\ V$	$-0.17\ V$
RF NMOS	$35\ \mu m \times 0.18\ \mu m$	$0.51\ V$	$0.63\ V$	$0.12\ V$
Low V_{TH} NMOS	$35\ \mu m \times 0.5\ \mu m$	$0.16\ V$	$0.29\ V$	$0.13\ V$

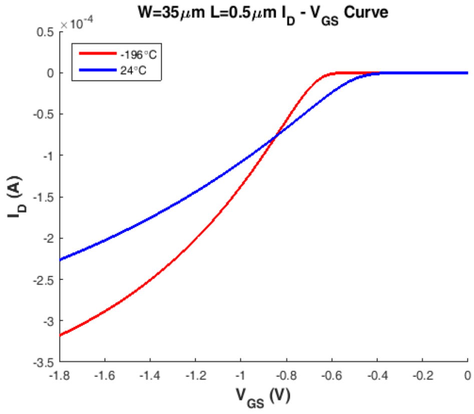
The drift current is related to the lateral electric field and the drain current saturates after a specific electric field E_{SAT}. The voltage that generates E_{SAT} is called V_{dsat}. If the electric field magnitude is below E_{SAT}, the carrier velocity is determined by



(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



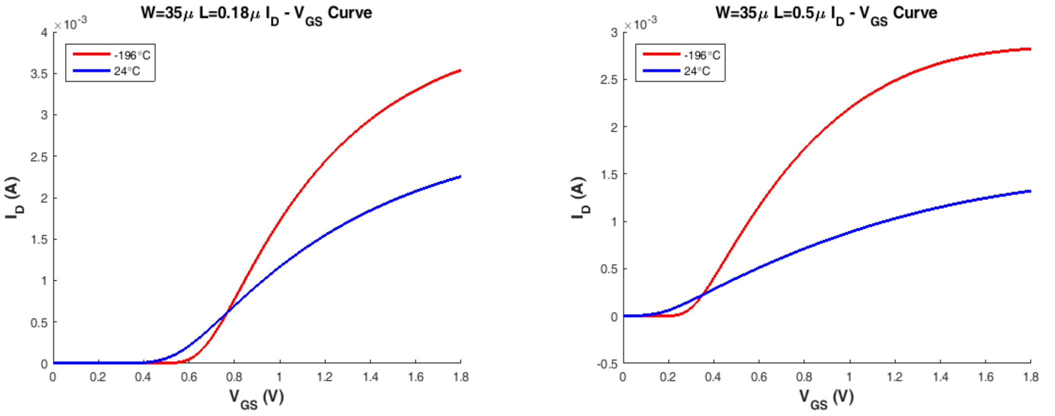
(c) $W = 0.24\ \mu m, L = 10\ \mu m$ (d) $W = 10\ \mu m, L = 10\ \mu m$



(e) $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.5 : PMOS $I_D - V_{GS}$ Curve @ $V_{DS} = 0.05V$ demonstrating V_{TH} increase as temperatures drop down

the low-field mobility. After V_{DS} reaches the V_{dsat} value the average carrier velocity becomes equal to the saturation velocity. Mobility has a much higher increase compared to v_{sat}; hence, carriers reach v_{sat} value faster at lower temperatures and V_{dsat} becomes smaller. Even though the saturation velocity increases with temperature decrease, V_{dsat} cannot increase along with the saturation velocity because of the



(a) RF-NMOS $W = 35\ \mu m, L = 0.18\ \mu m$ (b) Low V_{TH} NMOS $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.6 : $I_D - V_{GS}$ Curve @ $V_{DS} = 0.05V$ demonstrating V_{TH} increase as temperatures drop down

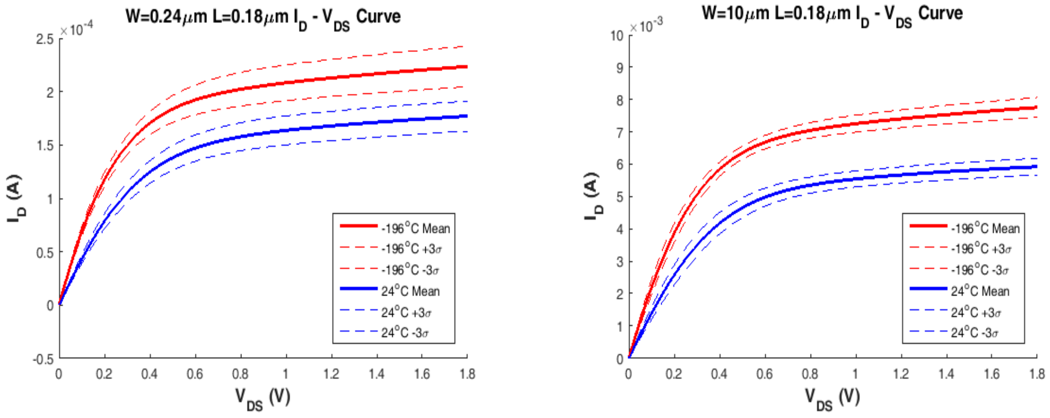
Table 3.3 : The maximum current value comparison of transistors both at the room temperature and cryogenic temperature

Type	Size(WxL)	Room Temp.	Cryogenic	Difference	Increase
NMOS	0.24 μmx0.18 μm	0.177 mA	0.223 mA	0.057 mA	%32
NMOS	10 μmx0.18 μm	5.92 mA	7.75 mA	1.83 mA	%31
NMOS	0.24 μmx10 μm	6.39 μA	18.0 μA	11.6 μA	%181
NMOS	10 μmx10 μm	0.241 mA	0.719 mA	0.478 mA	%198
NMOS	35 μmx0.5 μm	11.2 mA	16.92 mA	5.72 mA	%51
PMOS	0.24 μmx0.18 μm	-70.7 μA	-81.5 μA	-10.8 μA	%15
PMOS	10 μmx0.18 μm	-2.29mA	-2.65mA	-0.36mA	%15
PMOS	0.24 μmx10 μm	-1.41 μA	-2.44 μA	-1.03 μA	%73
PMOS	10 μmx10 μm	-40.5 μA	-62.9 μA	-22.4 μA	%55
PMOS	35 μmx0.5 μm	-2.78 mA	-3.63 mA	-0.85 mA	%30
RF NMOS	35 μmx0.18 μm	20.28 mA	26.92 mA	6.64 mA	%33
Low V_{TH} NMOS	35 μmx0.5 μm	16.92 mA	25.31 mA	8.39 mA	%50

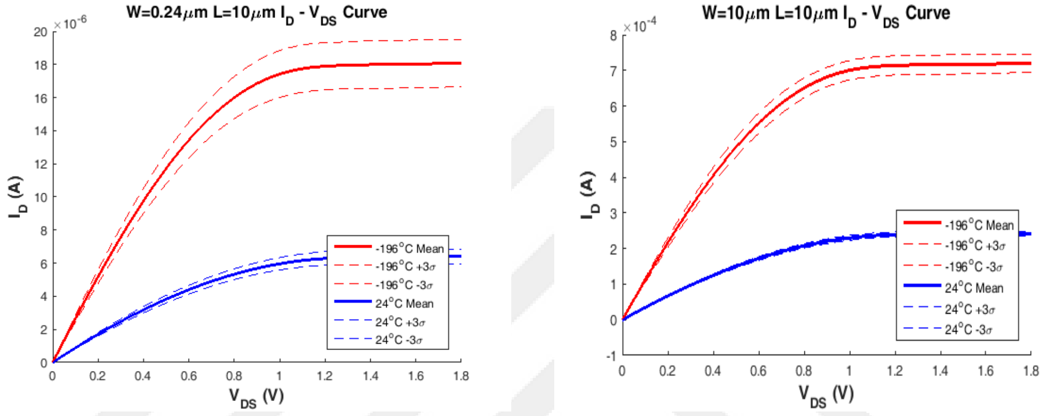
mobility increase. In the measurement results, V_{dsat} decreased by 0.05 V to 0.15 V when the maximum gate-source bias is applied.

3.2.1 Measurements at various intermediate temperatures

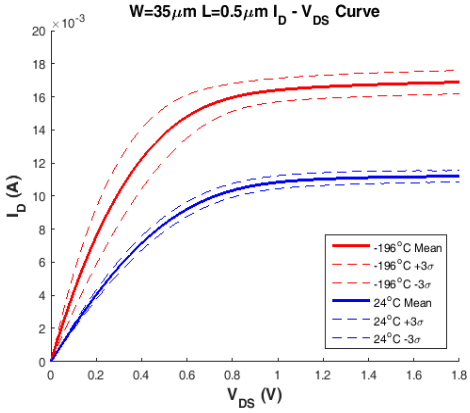
In addition to transistor measurements at $-196°C$, *I*-*V* curves were extracted at various intermediate temperatures between $-196°C$ and $-40°C$. Extraction temperatures of these curves can vary by $\pm 2^o C$ around the reported extraction temperature. It is observed that the drain current of each transistor increases monotonically as temperatures go down. For the 180 nm device technology and the corresponding



(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



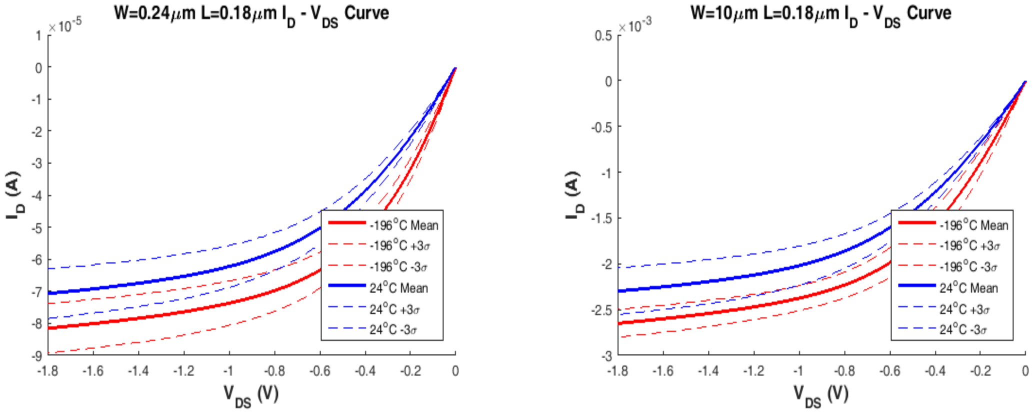
(c) $W = 0.24\ \mu m, L = 10\ \mu m$ (d) $W = 10\ \mu m, L = 10\ \mu m$



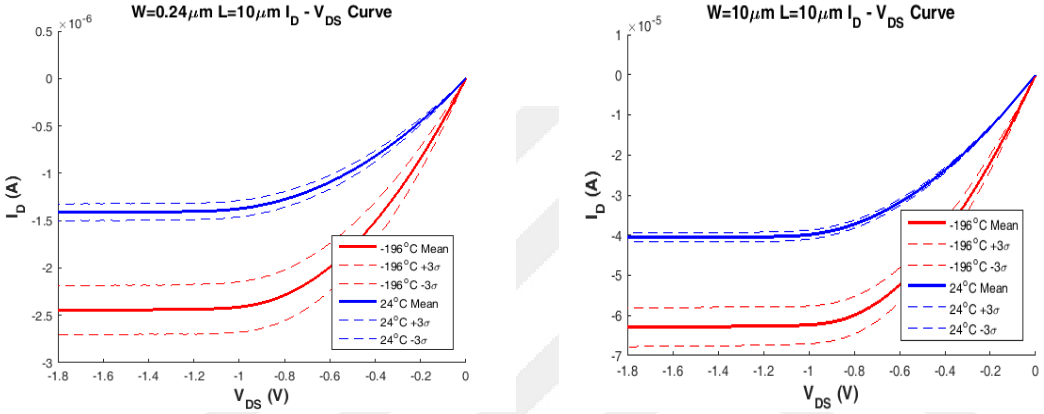
(e) $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.7 : The mean result and variations of NMOS measurements at $24^{o}C$ and $-196^{o}C$

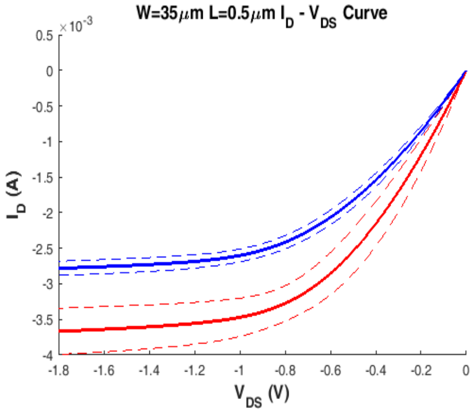
doping concentration amounts, freeze-out effects have not been come across within this temperature range. In Figs.3.10a to 3.11c, it can be seen that the mobility increases steadily from $-40°C$ to $-196°C$ for various sizes of NMOS and PMOS devices respectively.



(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



(c) $W = 0.24\ \mu m, L = 10\ \mu m$ (d) $W = 10\ \mu m, L = 10\ \mu m$



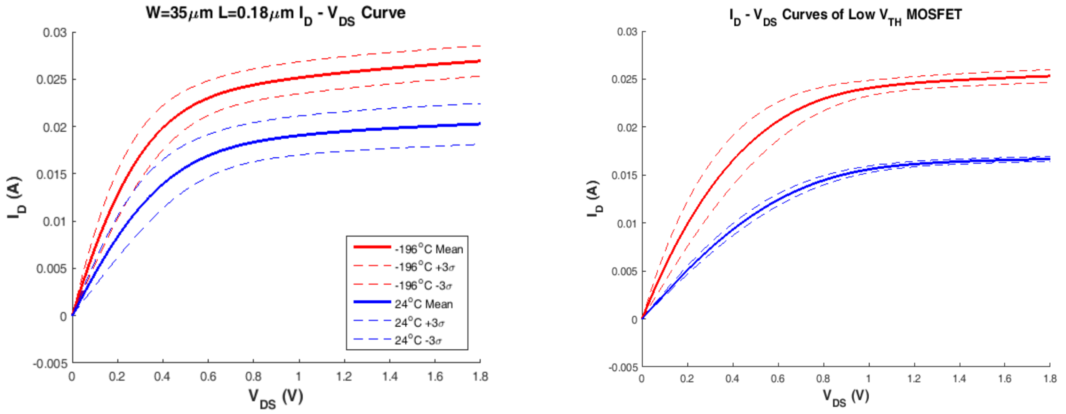
(e) $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.8 : The mean result and variations of PMOS measurements at 24^oC and -196^oC

3.2.2 Extracted model parameters

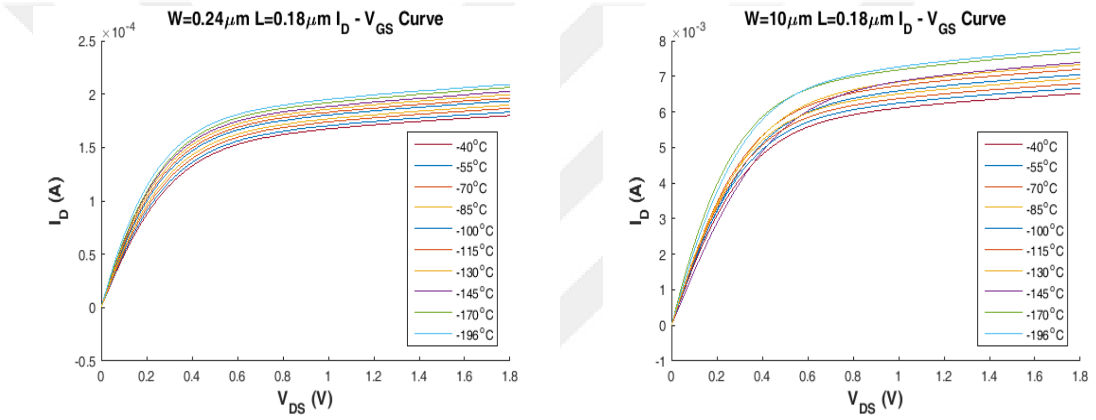
3.2.2.1 Model usage in simulation

BSIM3 is one the most commonly used model standard in the industry, it is developed by University of California, Berkeley. However, BSIM models provided

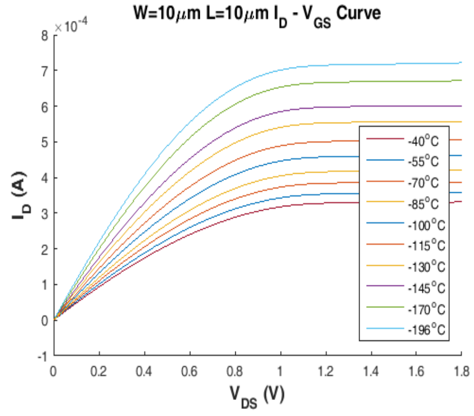


(a) RF-NMOS $W = 35\ \mu m, L = 0.18\ \mu m$ (b) Low V_{TH} NMOS $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.9 : The mean result and variations of RF and Low V_{TH} NMOS measurements at 24^oC and -196^oC



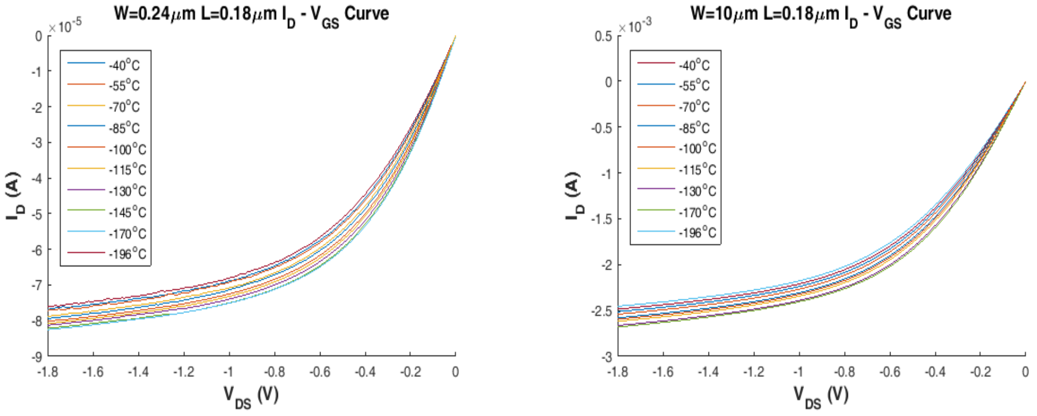
(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



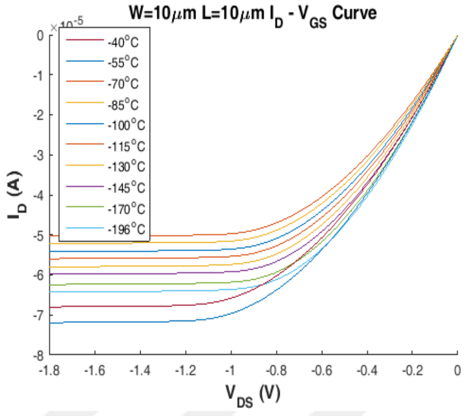
(c) $W = 10\ \mu m, L = 10\ \mu m$

Figure 3.10 : $I_D - V_{DS}$ measurements of NMOS devices from -40^oC to -196^oC

by manufacturers can not fit the experimental results at cryogenic conditions, because the model standard uses different equations for sub-threshold, linear and saturation regimes and it has fitting parameters extracted from measurements to fit simulation results to measured curves and these fitting parameters are products of temperature as



(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



(c) $W = 10\ \mu m, L = 10\ \mu m$

Figure 3.11 : $I_D - V_{DS}$ measurements of PMOS device from -40^oC to -196^oC

shown in 1.2 and gives the best result only in room temperature. When the working conditions are far away from room temperature, the model cannot converge to real values with default parameters. Furthermore, BSIM3 has a deficiency in modeling the channel length dependency of mobility. Different size transistors have distinct mobility increase amounts at low temperatures. Therefore, if a designer wants to obtain less error between simulations and measurements, different parameter sets for short and long channel devices should be used to adjust the model at low temperatures. Simulation programs allow designers to use multiple model files in the same design so different parameter sets can be used for different size transistors if lower errors are desired.

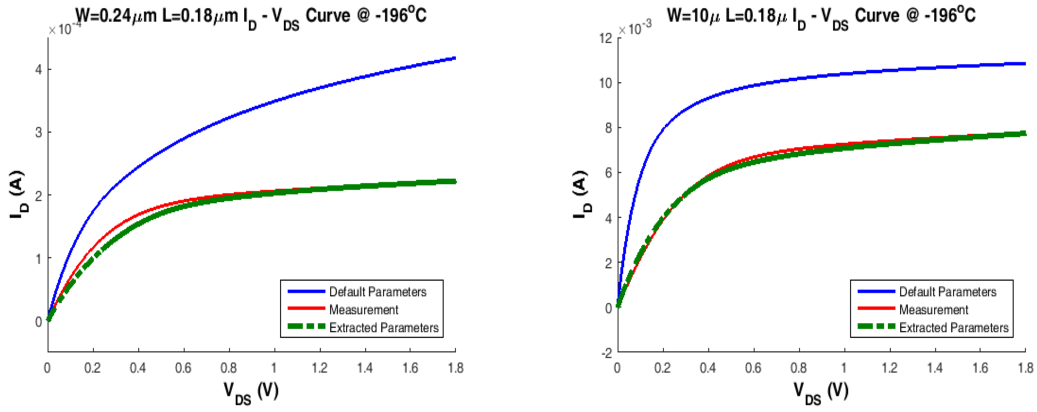
In the algorithm, mobility phenomena does not have length and temperature dependency together but threshold voltage has a parameter for model this dependency. The KT1L parameter specifies threshold voltage length dependency and KT1L extraction step in the proposed methodology can be used to get a single parameter set to model the threshold voltage for various size transistors at cryogenic temperatures; otherwise, this step can be disabled and the user can create new model files considering different measurements of various size transistors. The extracted new model files should be included within the simulation model file directory; after that, the designer can make simulations on any simulator that supports BSIM.

3.2.2.2 Comparison of default and extracted model

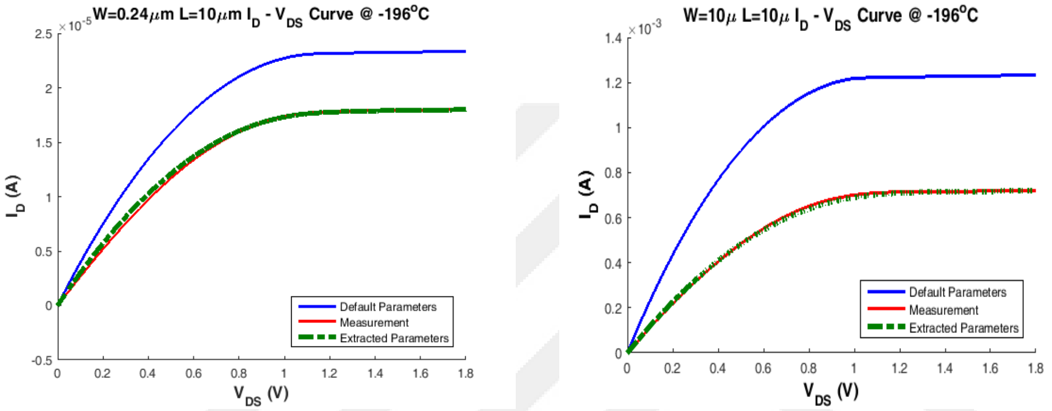
Without generating any new model card, designers can only use the default model file provided by the manufacturer. This model file cannot be used below -55^oC and the error margin of the model increases dramatically in cryogenic conditions as shown in Figs. 3.12-3.14. The algorithm can produce a new model parameter set for specific temperatures so the error rate can be minimized at that temperature as default parameters give the best result only at room temperature and error rates of parameter sets increase when moving away from the extraction temperature.

The comparison of measurements with simulation results using the extracted parameters are shown in Figs.3.12a$-$3.17b. Here, the error rate is scaled below $\%5$ for different parameter sets extracted per each transistor type. The error rates for different gate bias and temperature conditions are given in Table 3.4 and 3.5 and these error rates have similar values with body effect presence because the temperature dependency parameter of the body bias is also modified at cryogenic conditions as discussed previously. The model accuracy reduces for very long channel devices but the model performs with high accuracy in 180 nm and 500 nm devices which are commonly used in analog applications. Furthermore, these transistors produce accurate simulation results with the revised model file in a larger temperature range in comparison to long channel devices. Although default parameters are valid at -55^oC, the new parameter set has a smaller error at this specific temperature for the above mentioned devices.

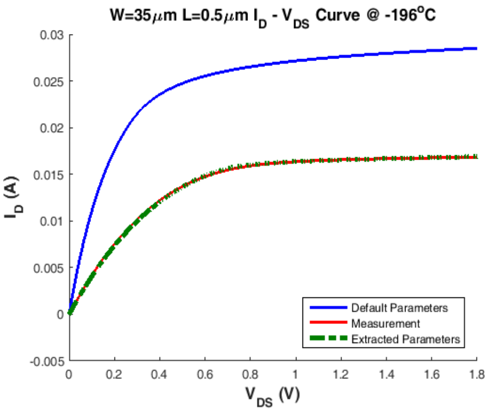
The extracted models performance in cryogenic conditions are not related with default model success. As shown in Table 3.4 the number 1 NMOS that has the smallest device size has %74.1 error with default model and it is decreased to %4.0 with extracted model. Although the device 4 has similar error rates with default model, it can be



(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



(c) $W = 0.24\ \mu m, L = 10\ \mu m$ (d) $W = 10\ \mu m, L = 10\ \mu m$

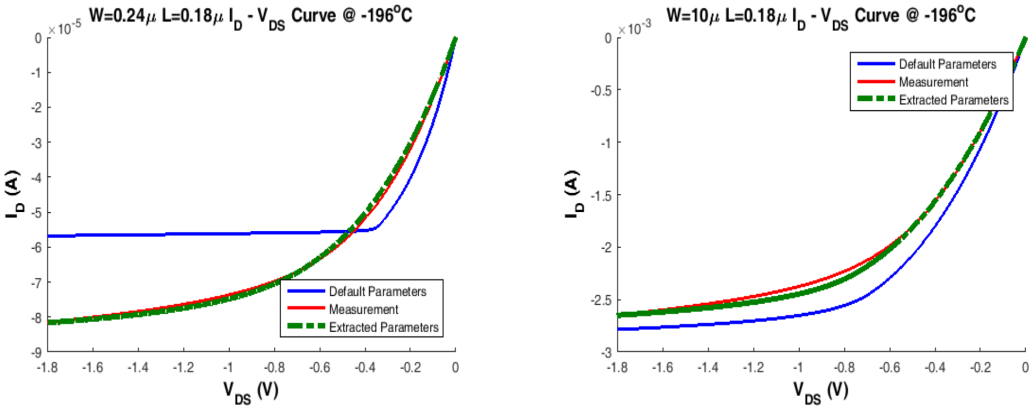


(e) $W = 35\ \mu m, L = 0.5\ \mu m$

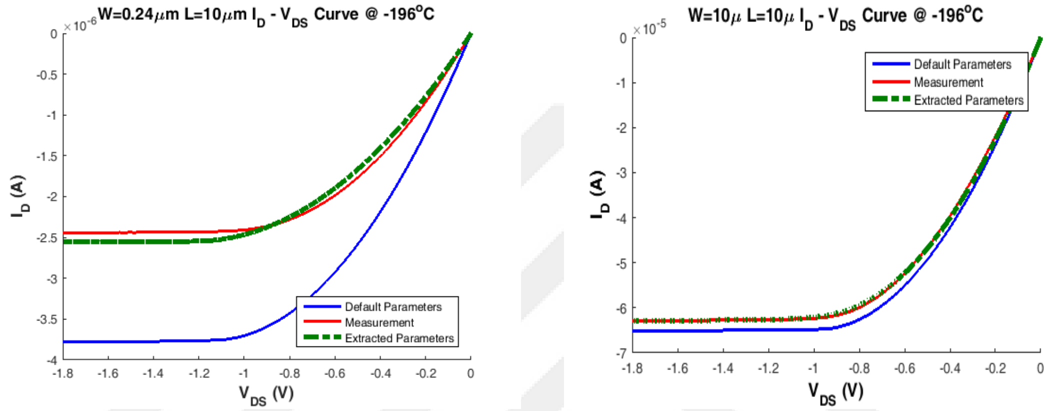
Figure 3.12 : Comparison of the default model and extracted models of NMOS with measurement results at -196^oC

decreased to %1.1. The device 3 has similar error rates with device 1 when extracted model used but its initial error is smaller than the half of the error of device 1.

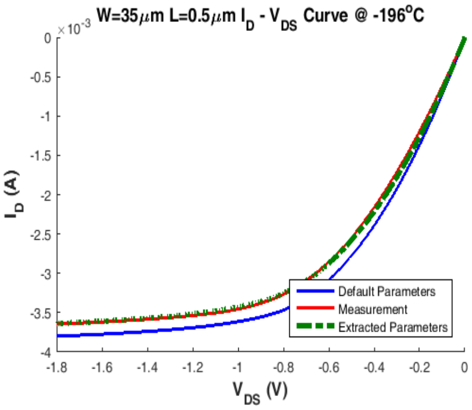
Although current increase by temperature lowering depends on length size, we cannot observe any relation between length size and default model mismatch to measurements when Figs. 3.12 and 3.13 are considered. However, the default model shows better



(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



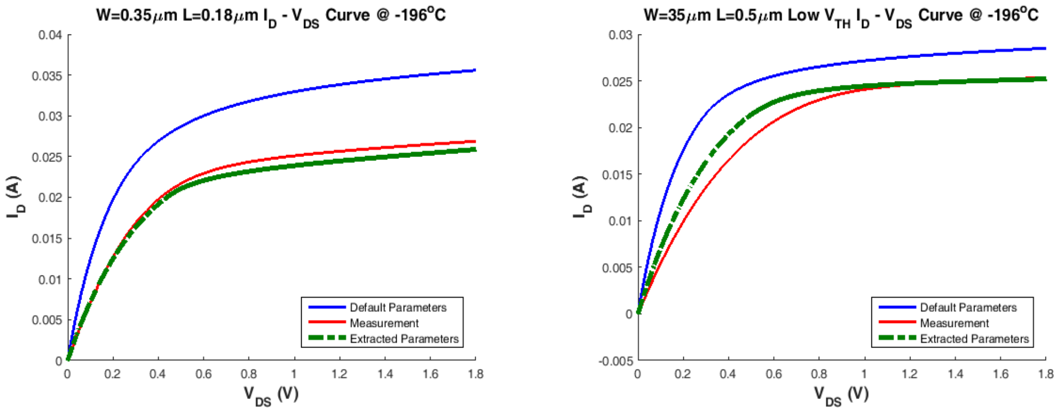
(c) $W = 0.24\ \mu m, L = 10\ \mu m$ (d) $W = 10\ \mu m, L = 10\ \mu m$



(e) $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.13 : Comparison of the default model and extracted models of PMOS with measurement results at $-196^{o}C$

performance on PMOS devices comparing the performance on NMOS device because holes have less mobility that involves less current increase; therefore, default model errors do not increase as much as NMOS devices. Hence, the proposed model is independent of the initial error rates of the default model and the size of devices because the methodology uses BSIM equations with measurements and it solves



(a) RF NMOS $W = 35\ \mu m, L = 0.18\ \mu m$ (b) Low V_{TH} NMOS $W = 35\ \mu m, L = 0.5\ \mu m$

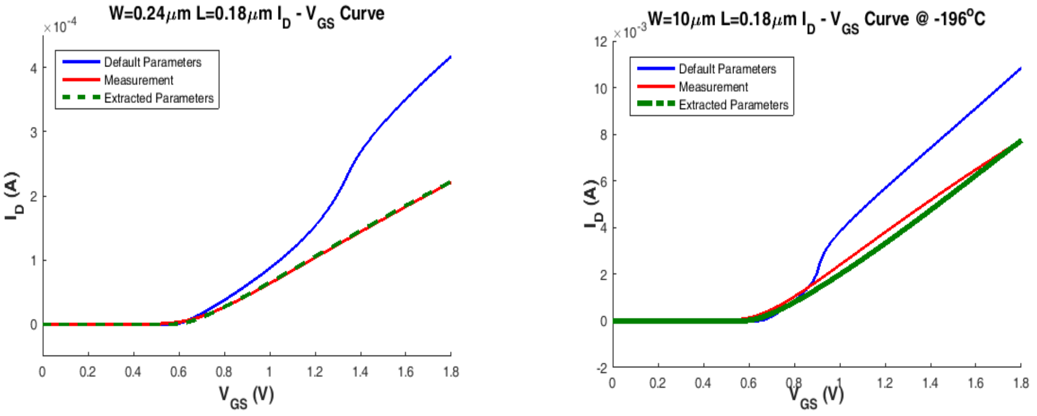
Figure 3.14 : Comparison of the default model and extracted models of PMOS with measurement results at -196^oC

equations considering device size and the simulation software results that works in parallel with the model algorithm.

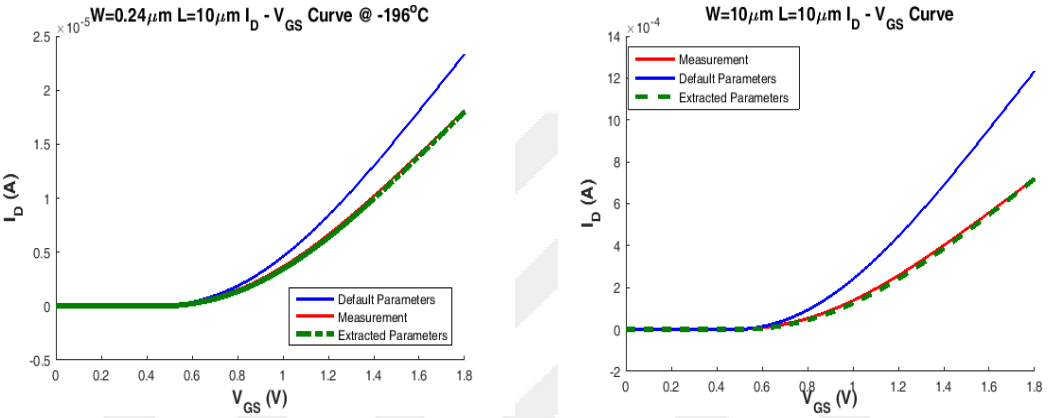
The curves obtained from simulations with default parameters in cryogenic conditions have insufficiency on both $I_D - V_{DS}$ and $I_D - V_{GS}$. In addition to current mismatch, the shapes of the curves are also incompatible with reality. The shape of the $I_D - V_{DS}$ curves vary on V_{DSAT}. Especially in the $I_D - V_{GS}$ simulations, curves can become distorted in active region when default parameters are used at low temperatures. The Figs. 3.15a and 3.15b have such cases and their shapes are not related with device physics. These distortions are treated separately in the algorithm and the UB1 parameter that specify second order mobility degradation is optimized to restore proper $I_D - V_{GS}$ curve shape as discussed in section PROPOSED MODEL.

Table 3.4 : Error rates of $I_D - V_{DS}$ curves $@|V_{GS}| = 1.8V$ with extracted model files at -196^oC for transistors of every size and the model performance at different temperatures

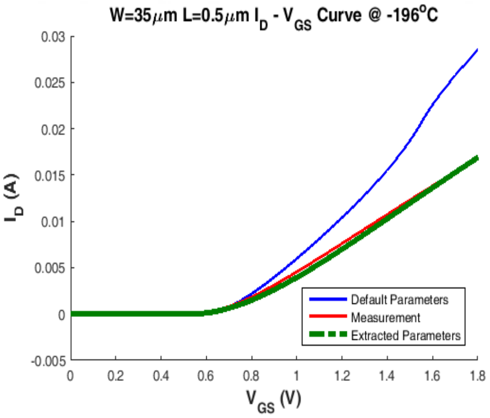
Type	Size(WxL)	-196^oC		-170^oC		-145^oC	
		Def.(%)	Model(%)	Def.(%)	Model(%)	Def.(%)	Model(%)
NMOS	0.24 μm x 0.18 μm	71.1	4.0	42.0	5.7	26.3	8.4
NMOS	10 μm x 0.18 μm	48.7	1.8	49.8	5.6	57.0	5.7
NMOS	0.24 μm x 10 μm	31.4	3.9	-	-	-	-
NMOS	10 μm x 10 μm	75.0	1.1	34.5	15.2	16.4	19.9
NMOS	35 μm x 0.5 μm	99.7	0.6	-	-	-	-
PMOS	0.24 μm x 0.18 μm	39.5	1.6	25.4	8.9	24.8	13.2
PMOS	10 μm x 0.18 μm	11.0	2.0	12.1	4.7	11.4	5.3
PMOS	0.24 μm x 10 μm	13.6	4.3	-	-	-	-
PMOS	10 μm x 10 μm	4.3	0.6	7.1	10.2	11.4	13.8
PMOS	35 μm x 0.5 μm	5.9	1.1	-	-	-	-
RF_N	35 μm x 0.18 μm	33.2	1.3	31.3	5.3	32.3	3.4



(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



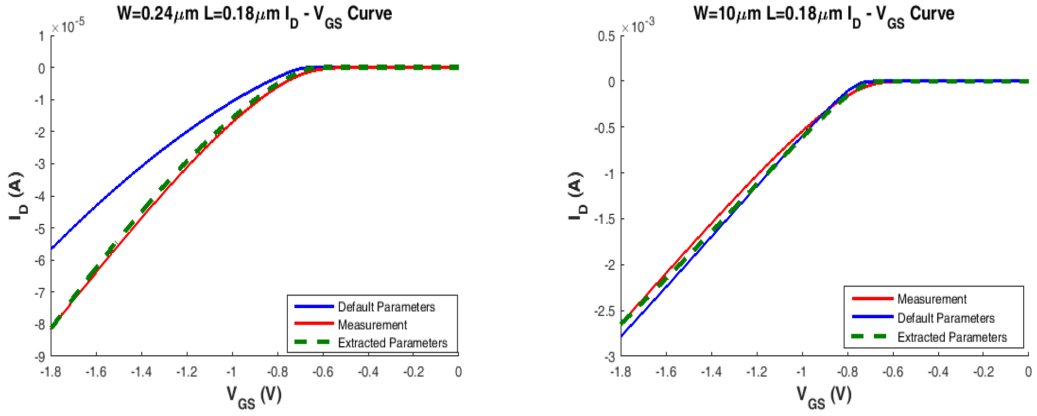
(c) $W = 0.24\ \mu m, L = 10\ \mu m$ (d) $W = 10\ \mu m, L = 10\ \mu m$



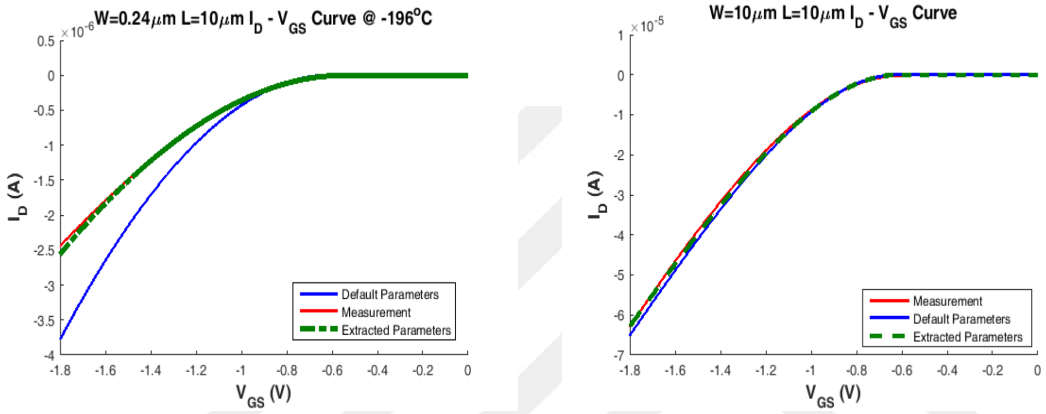
(e) $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.15 : Comparison of the default model and extracted model of NMOS with measurement results at -196^oC

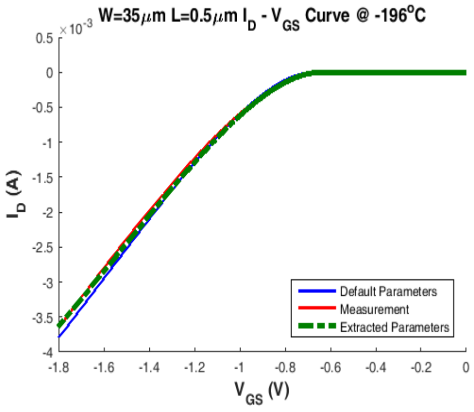
In addition to the extraction of different parameter sets for each transistor, a single parameter set can be obtained by only considering transistors 1, 2 and 5. This is especially useful and critical for analog and mixed-signal circuits where transistors of multiple channel lengths used together in a circuit topology. Transistors 1,2 and 5 can be counted as the most common devices observed in typical analog circuit blocks.



(a) $W = 0.24\ \mu m, L = 0.18\ \mu m$ (b) $W = 10\ \mu m, L = 0.18\ \mu m$



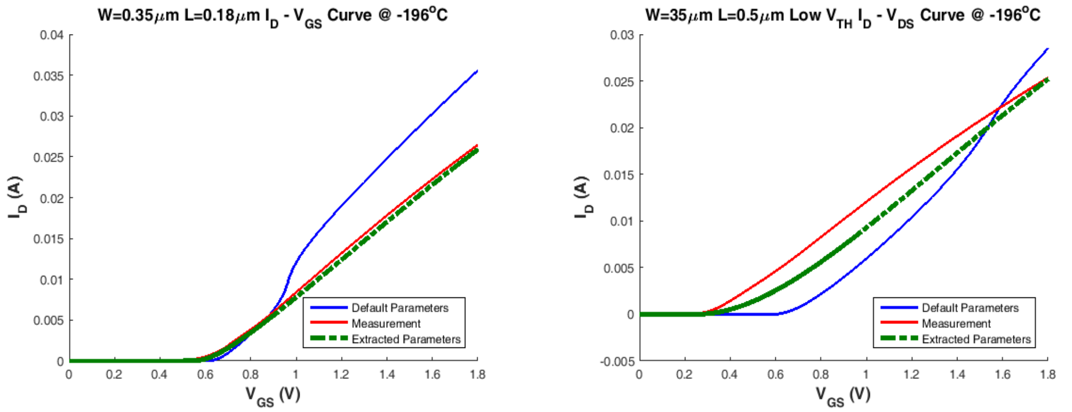
(c) $W = 0.24\ \mu m, L = 10\ \mu m$ (d) $W = 10\ \mu m, L = 10\ \mu m$



(e) $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.16 : Comparison of the default model and extracted model of PMOS with measurement results at -196^oC

Even though the error rates rise when only one parameter set is extracted, they are still significantly lower in regard to the default model. When $I_D - V_{DS}$ measurements are compared with simulations using the extracted model file, for transistors 1, 2 and 5, error rates of %14.21, %12.34 and %1.25 are acquired, respectively. Conversely, the default model can only yield error rates of %71.1, %48.7 and %99.7 which clearly



(a) RF NMOS $W = 35\ \mu m, L = 0.18\ \mu m$ (b) Low V_{TH} NMOS $W = 35\ \mu m, L = 0.5\ \mu m$

Figure 3.17 : Comparison of the default model and extracted model of RF NMOS and Low V_{TH} NMOS with measurement results at -196^oC

Table 3.5 : Error rates of $I_D - V_{DS}$ curves of different parameter sets for each transistor with lower gate biasing at -196^oC

Type	Size(WxL)	$-196^oC@\lvert V_{GS}\rvert = 1.2V$	
		Def.(%)	Model(%)
NMOS	0.24 μm x 0.18 μm	44.2	1.1
NMOS	10 μm x 0.18 μm	53.8	11.6
NMOS	0.24 μm x 10 μm	29.0	3.2
NMOS	10 μm x 10 μm	74.7	5.9
NMOS	35 μm x 0.5 μm	43.5	8.3
PMOS	0.24 μm x 0.18 μm	30.5	6.5
PMOS	10 μm x 0.18 μm	17.2	12.2
PMOS	0.24 μm x 10 μm	33.3	2.3
PMOS	10 μm x 10 μm	7.4	3.9
PMOS	35 μm x 0.5 μm	8.0	6.2
RF_N	35 μm x 0.5 μm	42.4	1.5

identifies the improvement achieved by the extracted model. Various temperatures, body and gate biases are taken into account and the algorithm with its outputs are proved for its accuracy measurements under LN2(liquid nitrogen).

3.2.2.3 Circuit measurements

A ring oscillator is considered to demonstrate the model in a typical circuit example and Rohde&Schwarz FSU $20\text{Hz} - 26.5\text{GHz}$ spectrum analyzer is used. Measurements have been performed on four different dies at both room temperature and cryogenic conditions. The measured oscillation spectrum of acquired from one of the ring oscillators at -196^oC is shown in Fig.3.18. The mean of measured oscillation

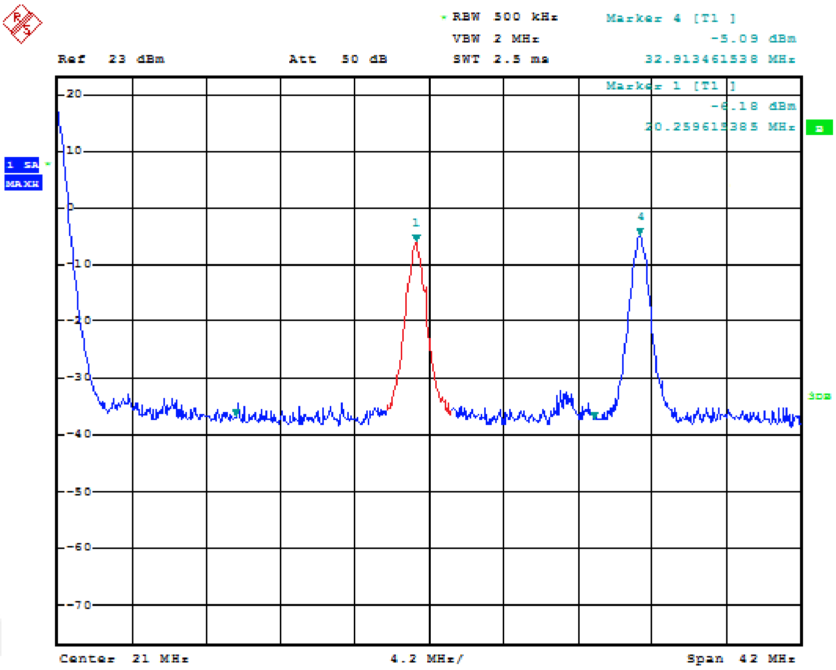


Figure 3.18 : Measured spectrum of the ring oscillator at -196^oC (blue) and 24^oC (red)

frequencies are 20.67 MHz and 32.65 MHz for 25^oC and -196^oC respectively. Simulation and measurement results of 4 different dies are compared in Table 3.6. While the default model results in 38.43% error in simulation-measurement comparison, a single model extracted for all sizes by the proposed methodology can accurately match the measurement results and the error is decreased down to 1.53% as shown in Table 3.6.

Additionally, a single ring oscillator was measured at various temperature from 24^oC to -196^oC. All measured oscillation frequencies with temperature sweep are given in Fig. 3.19. The oscillation frequency shows similar result with current change and it is increased linearly with temperature decrease as expected. The standard deviation values at -196^oC, -170^oC and -145^oC are also given that is calculated considering the measurement variation. The extracted model is verified with a circuit application and the validation of the model is proved at different temperatures and the statistical analysis are given for cryogenic conditions.

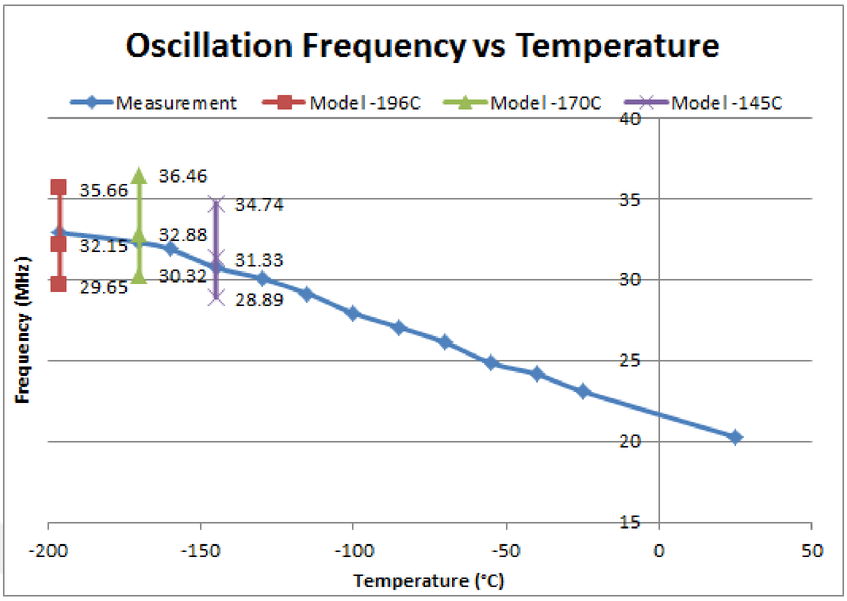


Figure 3.19 : Measured oscillation frequencies of the ring oscillator from -196^oC to 24^oC and proposed model results at -196^oC, -170^oC and -145^oC with $\pm 3\sigma$ values

Table 3.6 : Comparison of oscillation frequency for the ring oscillator at nominal and liquid nitrogen temperatures

Results	25^oC	-196^oC
Post Layout Sim. (Default)	19.1 MHz	45.2 MHz
Post Layout Sim. (Modeled)	19.1 MHz	32.15 MHz
Measurement (Chip 1)	20.73 MHz	31.9 MHz
Measurement (Chip 2)	21.26 MHz	33.31 MHz
Measurement (Chip 3)	20.46 MHz	32.51 MHz
Measurement (Chip 4)	20.26 MHz	32.91 MHz

4. CONCLUSION

In this thesis, a method has been presented to calibrate the BSIM3 temperature dependency parameters for cryogenic temperatures at which BSIM parameters cannot match the measurement outcomes. Although the algorithm was demonstrated for using 180 nm technology with measurements under liquid nitrogen, it can also be implemented in different device technologies because the method is independent of process parameters. The algorithm developed in this project is based on BSIM3 model and it only needs the target data with the default model file to yield the experimental results using BSIM equations and analytical solution methods. The extracted model parameter set can be called for simulations from any CAD program which supports BSIM3. This methodology can be used in BSIM4 as well because it has same modeling approach. The only need is adapting new equations and parameters to the developed methodology flow. This experimentally verified model on analog circuit design in the sense that it correctly reflects the device characteristics changes in transistors of various sizes. The model has a statistical approach and it includes the impact of process variation at cryogenic conditions. Finally, intermediate temperatures between the -196^oC and room temperature has also been considered and a specific model, calibrated at these temperatures are developed. The accuracy of the model derived from single-transistor experiments has been verified using a ring oscillator as well, which confirms its suitability for use in more complex circuit design.

REFERENCES

[1] **Kabaoğlu, A. and Yelten, M.B.** (2017). A cryogenic modeling methodology of MOSFET IV characteristics in BSIM3, *Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2017 14th International Conference on*, IEEE, pp.1–4.

[2] **Zhao, H. and Liu, X.** (2014). Modeling of a standard 0.35 μm CMOS technology operating from 77K to 300K, *Cryogenics*, *59*, 49–59.

[3] **Hu, C., Liu, W.** *et al.* (1999). BSIM3v3. 2.2 MOSFET Model. Users' manual, *UC Berkeley*.

[4] **Mauriello, R.**, **Sundaram, K. and Chow, L.** (1999). Simulation of Si power MOSFET under cryogenic conditions, *Solid-State Electronics*, *43*(4), 771–777.

[5] **Akturk, A.**, **Holloway, M.**, **Potbhare, S.**, **Gundlach, D.**, **Li, B.**, **Goldsman, N.**, **Peckerar, M. and Cheung, K.** (2010). Compact and distributed modeling of cryogenic bulk MOSFET operation, *IEEE Transactions on Electron Devices*, *57*(6), 1334–1342.

[6] **Varizat, L.**, **Sou, G.**, **Mansour, M.**, **Alison, D. and Rhouni, A.** (2017). A low temperature 0.35 μm CMOS technology BSIM3. 3 model for space instrumentation: Application to a voltage reference design, *Metrology for AeroSpace (MetroAeroSpace), 2017 IEEE International Workshop on*, IEEE, pp.74–78.

[7] **Dao, N.C.**, **El Kass, A.**, **Azghadi, M.R.**, **Jin, C.T.**, **Scott, J. and Leong, P.H.** (2017). An enhanced MOSFET threshold voltage model for the 6–300K temperature range, *Microelectronics Reliability*, *69*, 36–39.

[8] **Venkataraman, S.**, **Banerjee, B.**, **Lee, C.h.**, **Laskar, J. and Cressler, J.D.** (2007). Cryogenic small signal operation of 0.18 μm MOSFETs, *Silicon Monolithic Integrated Circuits in RF Systems, 2007 Topical Meeting on*, IEEE, pp.52–55.

[9] **Goryachev, M.**, **Galliou, S. and Abbé, P.** (2010). Cryogenic transistor measurement and modeling for engineering applications, *Cryogenics*, *50*(6), 381–389.

[10] **Baek, R.H.**, **Kang, H.S.**, **Lee, J.s. and Jeong, Y.H.** (2006). IV modeling for nanoscale n-MOSFET from liquid-nitrogen temperature to room temperature, *Nanotechnology Materials and Devices Conference, 2006. NMDC 2006. IEEE*, volume 1, IEEE, pp.316–317.

[11] **Martin, P.**, **Cavelier, M.**, **Fascio, R.**, **Ghibaudo, G. and Bucher, M.** (2009). EKV3 compact modeling of MOS transistors from a 0.18 μm CMOS technology for mixed analog–digital circuit design at low temperature, *Cryogenics*, *49*(11), 595–598.

[12] **Incandela, R.**, **Song, L.**, **Homulle, H.**, **Sebastiano, F.**, **Charbon, E. and Vladimirescu, A.** (2017). Nanometer CMOS characterization and compact modeling at deep-cryogenic temperatures, *Solid-State Device Research Conference (ESSDERC), 2017 47th European*, IEEE, pp.58–61.

[13] **Beckers, A.**, **Jazaeri, F.**, **Ruffino, A.**, **Bruschini, C.**, **Baschirotto, A. and Enz, C.** (2017). Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing, *Solid-State Device Research Conference (ESSDERC), 2017 47th European*, IEEE, pp.62–65.

[14] **Liu, S.**, **Li, X.**, **Liu, C. and Sun, W.** (2017). Improved Metal Oxide Semiconductor Field Effect Transistor models with wide temperature range including cryogenic temperature, *Superlattices and Microstructures*, *109*, 31 – 40.

[15] **Chen, F.**, **Zhao, Y.**, **Zou, H.**, **Kraft, M. and Li, X.** (2017). A front-side non-soi fabricated tri-axis capacitive accelerometer with electromechanical sigma-delta modulators interface, *2017 19th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, pp.930–933.

[16] **Wolpert, D. and Ampadu, P.**, (2012). Temperature effects in semiconductors, Managing temperature effects in nanoscale adaptive systems, Springer, pp.15–33.

[17] **Balestra, F. and Ghibaudo, G.** (2013). *Device and circuit cryogenic operation for low temperature electronics*, Springer Science & Business Media.

[18] **Gutierrez-D, E.A.**, **Deen, J. and Claeys, C.** (2000). *Low temperature electronics: physics, devices, circuits, and applications*, Academic Press.

[19] **Van Zeghbroeck, B.** (2004). Principles of semiconductor devices, *Colarado University*.

[20] **Hong, S.H.**, **Choi, G.B.**, **Baek, R.H.**, **Kang, H.S.**, **Jung, S.W. and Jeong, Y.H.** (2008). Low-temperature performance of nanoscale MOSFET for deep-space RF applications, *IEEE Electron Device Letters*, *29*(7), 775–777.

[21] **Arora, N.D. and Gildenblat, G.S.** (1987). A semi-empirical model of the MOSFET inversion layer mobility for low-temperature operation, *IEEE Transactions on Electron Devices*, *34*(1), 89–93.

[22] **Sakuna, N.**, **Muanghlua, R.**, **Niemcharoen, S.**, **Ruangphanit, A. and Poyai, A.** (2013). Temperature and devices dimension dependence on threshold voltage, the low field mobilty and the series parasitic resistance of PMOSFET, *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2013 10th International Conference on*, IEEE, pp.1–6.

[23] Cadence Design System Inc., (2001). Affirma Spectre Circuit Simulator Device Model Equations.

[24] **Liu, W.**, (2001). MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4.

[25] **Cressler, J.D. and Mantooth, H.A.** (2012). *Extreme environment electronics*, CRC Press.

[26] **Cheng, Y.**, **Imai, K.**, **Jeng, M.c.**, **Liu, Z.**, **Chen, K. and Hu, C.** (1997). Modelling temperature effects of quarter micrometre MOSFETs in BSIM3v3 for circuit simulation, *Semiconductor science and technology*, *12*(11), 1349.

[27] **Sucre-González, A.**, **Zárate-Rincón, F.**, **Ortiz-Conde, A.**, **Torres-Torres, R.**, **García-Sánchez, F.J.**, **Muci, J. and Murphy-Arteaga, R.S.** (2016). A DC method to extract mobility degradation and series resistance of multifinger microwave MOSFETs, *IEEE Transactions on Electron Devices*, *63*(5), 1821–1826.

[28] **Ortiz-Conde, A.**, **Sánchez, F.G.**, **Liou, J.J.**, **Cerdeira, A.**, **Estrada, M. and Yue, Y.** (2002). A review of recent MOSFET threshold voltage extraction methods, *Microelectronics Reliability*, *42*(4), 583–596.

[29] **Streetman, B.G. and Banerjee, S.K.** (2005). *Solid state electronic devices*, Prentice-Hall.

APPENDICES

APPENDIX A.1 : Source Code of Main Function

APPENDIX A.1 - Source Code of Main Function

```
%%%%%%%%%%%%%%%%%%%%%%% INPUTS %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
      transistor_no = 2;
     % No - W(um), L(um) , type
     %  1 - 0.24 , 0.18  , n
     %  2 - 10   , 0.18  , n
     %  3 - 0.24 , 10    , n
     %  4 - 10   , 10    , n
     %  5 - 35   , 0.5   , n
     %  9 - 0.24 , 0.18  , p
     % 10 - 10   , 0.18  , p
     % 11 - 0.24 , 10    , p
     % 12 - 10   , 10    , p
     % 13 - 35   , 0.5   , p
     % 15 - 35   , 0.18  , rf-n
temp = -196; % measurement temperature

Wdrawn=10e-06; % transistor width
Ldrawn=0.18e-06; % transistor length

short_ch = 0; % KTIL activation
Ldrawn_s = 0.18e-06; % short channel transistor length

transistor_name = 'n_18'; % name in the model file
type = 'n'; % n / p type

vds_second_bias = 8; % Id-Vds, VGS 8 9 10 11 12 (VGS = 1.8 1.5...
% 1.2 0.9 0.6)

step = 10; % delta iteration
maksimum_simulasyon_sayisi = 10; % simulation_limit
target_min_error = 0.5;

% maximum biases
if type == 'n'
     vd = 1.8;
     vg = 1.8;
     vs = 0;
     vb = 0;
elseif type == 'p'
     vd = 0;
     vg = 0;
     vs = 1.8;
     vb = 1.8;
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% ocean file path for each sweep
[~,transistor_size] = size(transistor_name);
if transistor_size == 4 & (transistor_name =='n_18' |...
          transistor_name =='p_18')
     %--------- N_18, P_18 ---------%
     ocean_address_n_vds = './ocean_files/ocean_n_vds.ocn';
     ocean_address_n_vgs = './ocean_files/ocean_n_vgs.ocn';
     ocean_address_n_vgs_low_vds = ...
          './ocean_files/ocean_n_...vgs_low_vds.ocn';
     ocean_address_p_vds = './ocean_files/ocean_p_vds.ocn';
     ocean_address_p_vgs = './ocean_files/ocean_p_vgs.ocn';
     ocean_address_p_vgs_low_vds = ...
          './ocean_files/ocean_p_vgs_low_vds.ocn';
     model_address = '/vlsi/projects/mm180_reg18_v124.mdl.scs';

     file = fopen(model_address);
     formatSpec = '%s';
     C = textscan(file, formatSpec);
     [boyut, ~] = size(C{:});
```

```

    % model parameter location in model file
    for i=1:boyut
        k=strfind(C{1}{i},’type=’);
        if k==1
            model_mosfet_type = textscan(C{1}{i},’type=%s’);
            model_mosfet_type = model_mosfet_type{1}{1};
            if type == ’n’
                if model_mosfet_type==’n’
                    baslangic = i; %nmos
                elseif model_mosfet_type==’p’
                    son = i; %pmos
                end
            end

            if type == ’p’
                if model_mosfet_type==’p’
                    baslangic = i; %pmos
                    son = boyut;
                end
            end
        end
    end
    fclose(file);

else % for rf transistor
    %———— RF ————%
    ocean_address_n_vds = ’./ocean_files/ocean_n_vds_rf.ocn’;
    ocean_address_n_vgs = ’./ocean_files/ocean_n_vgs_rf.ocn’;
    ocean_address_n_vgs_low_vds = ...
        ’./ocean_files/ocean_n_vgs_low_vds_rf.ocn’;
    ocean_address_p_vds = ’./ocean_files/ocean_p_vds_rf.ocn’;
    ocean_address_p_vgs = ’./ocean_files/ocean_p_vgs_rf.ocn’;
    ocean_address_p_vgs_low_vds = ...
        ’./ocean_files/ocean_p_vgs_low_vds_rf.ocn’;
    model_address = ’/vlsi/projects/mm180_reg18_v124.mdl.scs’;

    file = fopen(model_address);
    formatSpec = ’%s’;
    C = textscan(file, formatSpec);
    [boyut, ~] = size(C{:});

    % RF Transistor model dosyasi
    n = 1;
    for i=1:boyut
        k = strfind(C{1}{i}, transistor_name);
        if k==1
            if n==1
                baslangic = i;
                n = 2;
            elseif n == 2
                son = i;
            end
        end
    end
end

% simulation results of cadence
result_address_vgs = ’./sonuclar/n_vgs.dat’;
result_address_vgs_low_vds = ’./sonuclar/n_vgs_low_vds.dat’;
result_address_vds = ’./sonuclar/n_vds.dat’;

% iteration parameters
ub1_n_max=−10.6730e−18;
delta_n_max = 0.2;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

command = ’sed −i −e ’’s/’’"%s"’’/’’"%s"’’/g’’ %s’;
if type ==’n’
    ocean_address_vds = ocean_address_n_vds;
```

```
    ocean_address_vgs = ocean_address_n_vgs;
    ocean_address_low_vds = ocean_address_n_vgs_low_vds;

elseif type =='p'
    ocean_address_vds = ocean_address_p_vds;
    ocean_address_vgs = ocean_address_p_vgs;
    ocean_address_low_vds = ocean_address_p_vgs_low_vds;
end

%%%%%%%% Algorithm starts here %%%%%%%%%
simulasyon_sayisi=1;
level = 1;
% level 1 - vbs=0
% level 2 - bulk effect
% level 3 - vdsat, delta
while level <= 3
    if level == 2
        if type == 'n'
            vb = -0.4; % bulk effect (vbs = -0.4)
        elseif type == 'p'
            vb = 2.2; % bulk effect(vbs = 0.4)
        end
    elseif level == 3
        if type == 'n'
            vb = 0;
        elseif type == 'p'
            vb = 1.8;
        end
    end

    %%%%%% Measurement Data Import %%%%%%
    if type == 'n'
        V = 0:0.01:1.8;
        if (level == 1 || level == 3)
            [ Id_mean_ln2,  Id_3sigma, Id_e3sigma] =...
                target_meas_data( transistor_no, 'VGS',  2, 8 );
            V_aim_low_vds = V;
            I_aim_low_vds = Id_mean_ln2;

            [ Id_mean_ln2,  Id_3sigma, Id_e3sigma] =...
                target_meas_data( transistor_no, 'VGS',  1, 8 );
            V_aim = V;
            I_aim = Id_mean_ln2;

            [ Id_mean_ln2,  Id_3sigma, Id_e3sigma] =...
        target_meas_data( transistor_no, 'VDS',  0, vds_second_bias );
            Vds_aim = V;
            Ids_aim = Id_mean_ln2;
        elseif level == 2
            [Id_mean_ln2,  Id_3sigma, Id_e3sigma] =...
                target_meas_data( transistor_no, 'VGS',  2, 12 );
            V_aim_low_vds = V;
            I_aim_low_vds = Id_mean_ln2;
            I_aim_low_vds_vbs = I_aim_low_vds;
            %          FF = importdata(Id_Vg_Vdmax1_path);
            %          V_aim = FF(:,1);
            %          I_aim = FF(:,2);
            [ Id_mean_ln2,  Id_3sigma, Id_e3sigma] =...
        target_meas_data( transistor_no, 'VDS',  4, vds_second_bias );
            Vds_aim = V;
            Ids_aim = Id_mean_ln2;
            Ids_aim_vbs = Ids_aim;
        end
    elseif type=='p'
        V = 1.8:-0.01:0;
        if (level == 1 || level == 3)
            [Id_mean_ln2,  Id_3sigma, Id_e3sigma] =...
                target_meas_data( transistor_no, 'VGS',  2, 8 );
            V_aim_low_vds = V;
            I_aim_low_vds = Id_mean_ln2*-1;

```

```
        [ Id_mean_ln2, Id_3sigma, Id_e3sigma] =...
            target_meas_data( transistor_no, 'VGS', 1, 8 );
        V_aim = V;
        I_aim = Id_mean_ln2*-1;

        [ Id_mean_ln2, Id_3sigma, Id_e3sigma] =...
    target_meas_data( transistor_no, 'VDS', 0, vds_second_bias );
        Vds_aim = V;
        Ids_aim = Id_mean_ln2*-1;
    elseif level == 2
        [Id_mean_ln2, Id_3sigma, Id_e3sigma] =...
            target_meas_data( transistor_no, 'VGS', 2, 12 );
        V_aim_low_vds = V;
        I_aim_low_vds = Id_mean_ln2*-1;
        I_aim_low_vds_vbs = I_aim_low_vds;
        %           FF = importdata(Id_Vg_Vdmax1_path);
        %           V_aim = FF(:,1)+1.8;
        %           I_aim = FF(:,2)*-1;
        [ Id_mean_ln2, Id_3sigma, Id_e3sigma] =...
    target_meas_data( transistor_no, 'VDS', 4, vds_second_bias );
        Vds_aim = V;
        Ids_aim = Id_mean_ln2*-1;
        Ids_aim_vbs = Ids_aim;
    end
end

if level == 1 %% measurement graphs
    subplot(2,2,1)
    ax1_I_aim = plot(V_aim,I_aim,'linewidth',2,'color','r');

    subplot(2,2,3)
    ax2_I_aim = plot(V_aim_low_vds,I_aim_low_vds, ...
        'linewidth',2,'color','r');

    subplot(2,2,2)
    ax3_I_aim = plot(Vds_aim,Ids_aim,'linewidth',2, ...
        'color','r');

elseif level == 2
    subplot(2,2,4)
    ax4_I_aim = plot(Vds_aim,Ids_aim_vbs,'linewidth',2,...
        'color','r');
end
drawnow
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%



%%%%%%%%%%% Input Import / Ocean File %%%%%%%%%%%
ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
    ocean_address_vds);
ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
    ocean_address_vgs);
if type == 'n'
    vd = 0.05;
    ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
        ocean_address_low_vds);
    vd = 1.8;
elseif type == 'p'
    vd = 1.75;
    ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
        ocean_address_low_vds);
    vd = 0;
end
%%%%%%%%%% default degerlerde analiz %%%%%%%%%%%

drawnow

[ Vds, Ids ] = simulation( ocean_address_vds, result_address_vds );
[ V, I ] = simulation( ocean_address_vgs, result_address_vgs );
[ V_low_vds, I_low_vds ] = simulation( ocean_address_low_vds,...
    result_address_vgs_low_vds ); % (ID-VGS @ low VDS)
```

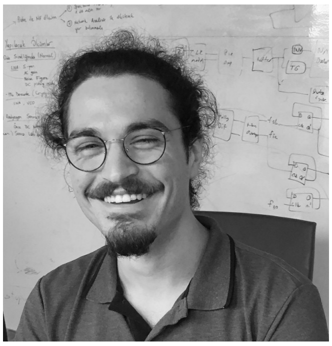
```
vth = importdata('./sonuclar/vth.dat');
vdsat = importdata('./sonuclar/vdsat.dat');
if level ==1
    Ids_cad_ln2 = Ids;
    I_cad_ln2 = I;

    plot(V,Ids)
    plot(V,Ids_aim)

    subplot(2,2,1)
    ax1_I_cad_ln2 = plot(V,I_cad_ln2,'-');

    subplot(2,2,2)
    ax3_I_cad_ln2 = plot(Vds,Ids_cad_ln2,'-');

    drawnow
end


%%%%%%%%%%%%%%%%%%%%%%%%% VTH Extraction %%%%%%%%%%%%%%%%%%%%%%%%%%%
I_aim_low_vds = smooth(I_aim_low_vds);

if type =='n'
    [~,loc]=max(diff(I_aim_low_vds));
elseif type == 'p'
    [~,loc]=max(abs(diff(I_aim_low_vds)));
end

if loc>=3
    m= (I_aim_low_vds(loc)-I_aim_low_vds(loc-2))/...
        (V_aim_low_vds(loc)-V_aim_low_vds(loc-2));
else
    m= (I_aim_low_vds(loc)-I_aim_low_vds(loc+2))/...
        (V_aim_low_vds(loc)-V_aim_low_vds(loc+2));
end
b = I_aim_low_vds(loc) - m*V_aim_low_vds(loc);

vth_graph = -b/m; % linear method

if ~manual_input
    [~,loc]=max(smooth(transpose(V_aim_low_vds(1,...
        1:size(V_aim_low_vds,2)-2)),diff(I_aim_low_vds,2)));
else
    [~,loc]=max(smooth(transpose(V_aim_low_vds(1:...
        size(V_aim_low_vds,1)-2)),diff(I_aim_low_vds,2)));
end

vth_sd = V_aim_low_vds(loc); %  second derivative method
if type == 'p'
    vth_sd = 1.8-vth_sd;
    vth_graph = 1.8-vth_graph;
end

vth_app = vth_sd;
if abs(abs(vth_graph)-abs(vth_sd))>0.2
    vth_app = vth_graph;
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
error_vds=100;
[Ids_boyut,~] = size(Ids);

while error_vds>target_min_error || (Ids_aim(Ids_boyut,1)...
        -Ids(Ids_boyut,1))/Ids(Ids_boyut,1)>0.01
    %%%%%%%%%%%%%%%%%%%%%%%% VDSAT %%%%%%%%%%%%%%%%%%%%%%%%%

    [ vdsat_difference ] = vdsat_finding( Vds, Ids, Vds,...
        Ids_aim );

    %%%%%%%%%%%%%%%%%% Calculations %%%%%%%%%%%%%%%%%%%%%%%%
```

```
        % Parameters are extracted at this stage
        if type =='n'
            [level, hata, Ids_app] = parametric_calculations_n(...
temp, vg, vd, vs, vb, vth, vth_app, Wdrawn, Ldrawn, model_address,...
command, Ids_aim, Ids, I, I_aim, vdsat, vdsat_difference,...
ocean_address_vgs, ocean_address_low_vds, ocean_address_vds,...
result_address_vgs, result_address_vgs_low_vds, result_address_vds,...
ub1_n_max, step, level, baslangic, son, short_ch, type );

        elseif type =='p'
            [level, hata, Ids_app] = parametric_calculations_p(...
temp, vg, vd, vs, vb, vth, vth_app, Wdrawn, Ldrawn, model_address,...
command, Ids_aim, Ids, I, I_aim, vdsat, vdsat_difference,...
ocean_address_vgs, ocean_address_low_vds, ocean_address_vds,...
result_address_vgs, result_address_vgs_low_vds, result_address_vds,...
ub1_n_max, step, level, baslangic, son, short_ch, type );
        end

        if hata == 1
            if level == 1
                hata_ute = 1;
            end
        end

        if short_ch == 1 && level == 1 && simulasyon_sayisi > 2
            level = 4;

            if type =='n'
                FF = importdata(Id_Vg_Vdmin_s_path);
                V_aim_low_vds_s = FF(:,1);
                I_aim_low_vds_s = FF(:,2);

            elseif type == 'p'
                FF = importdata(Id_Vg_Vdmin_s_path);
                V_aim_low_vds_s = FF(:,1)+1.8;
                I_aim_low_vds_s = FF(:,2)*-1;
            end

            %%%%%%%%%%%%%%%%%%%%%% VTH %%%%%%%%%%%%%%%%%%%%%%%%
            I_aim_low_vds_s = smooth(I_aim_low_vds_s);

            if type =='n'
                [~,loc]=max(diff(I_aim_low_vds_s));
            elseif type == 'p'
                [~,loc]=max(abs(diff(I_aim_low_vds_s)));
            end

            if loc>=3
                m= (I_aim_low_vds_s(loc)-I_aim_low_vds_s(loc-2))/...
                    (V_aim_low_vds_s(loc)-V_aim_low_vds_s(loc-2));
            else
                m= (I_aim_low_vds_s(loc)-I_aim_low_vds_s(loc+2))/...
                    (V_aim_low_vds_s(loc)-V_aim_low_vds_s(loc+2));
            end
            b = I_aim_low_vds_s(loc) - m*V_aim_low_vds_s(loc);

            vth_graph = -b/m;

            [~,loc]=max(smooth(V_aim_low_vds_s(1:...
                size(V_aim_low_vds_s)-2,1),diff(I_aim_low_vds_s,2)));
            vth_sd = V_aim_low_vds_s(loc);
            if type == 'p'
                vth_sd = 1.8-vth_sd;
                vth_graph = 1.8-vth_graph;
            end

            vth_app = vth_sd;
            if abs(abs(vth_graph)-abs(vth_sd))>0.2
                vth_app = vth_graph;
            end

```

```
            Ldrawn_old = Ldrawn;
            Ldrawn = Ldrawn_s;

            %%%%%%%%%%% Input Import / Ocean File %%%%%%%%%
            ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
                ocean_address_vgs);
            if type == 'n'
                vd = 0.05;
                ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
                    ocean_address_low_vds);
                vd = 1.8;
            elseif type == 'p'
                vd = 1.75;
                ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
                    ocean_address_low_vds);
                vd = 0;
            end

            %%%%%%% Simulations %%%%%%
            [ V_low_vds, I_low_vds ] = simulation( ...
                ocean_address_low_vds, result_address_vgs_low_vds );
            [ V, I ] = simulation( ocean_address_vgs, ...
                result_address_vgs );
            A = importdata('./sonuclar/vth.dat');
            vth = A;


            %%%%%%%%%%%%% Calculations %%%%%%%%%%%%%%%%%%%
            if type =='n'
                [level, hata, Ids_app] = parametric_calculations_n(...
temp, vg, vd, vs, vb, vth, vth_app, Wdrawn, Ldrawn, model_address,...
command, Ids_aim, Ids, I, I_aim, vdsat, vdsat_difference,...
ocean_address_vgs, ocean_address_low_vds, ocean_address_vds,...
result_address_vgs, result_address_vgs_low_vds, result_address_vds,...
ub1_n_max, step, level, baslangic, son, short_ch, type );

            elseif type =='p'
                [level, hata, Ids_app] = parametric_calculations_p(...
temp, vg, vd, vs, vb, vth, vth_app, Wdrawn, Ldrawn, model_address,...
command, Ids_aim, Ids, I, I_aim, vdsat, vdsat_difference,...
ocean_address_vgs, ocean_address_low_vds, ocean_address_vds,...
result_address_vgs, result_address_vgs_low_vds, result_address_vds,...
ub1_n_max, step, level, baslangic, son, short_ch, type );
            end

            Ldrawn = Ldrawn_old;
            level = 1;
        end


        %%%%%%% Simulations with new parameters %%%%%%%%
        [ Vds, Ids ] = simulation( ocean_address_vds, ...
            result_address_vds );
        [ V_low_vds, I_low_vds ] = simulation( ...
            ocean_address_low_vds, result_address_vgs_low_vds );
        [ V, I] = simulation(ocean_address_vgs,result_address_vgs);
        A = importdata('./sonuclar/vth.dat');
        vth = A;
        A = importdata('./sonuclar/vdsat.dat');
        vdsat = A;
        if level == 2
            Ids_vbs = Ids;
            I_low_vds_vbs = I_low_vds;
            I_vbs = I;
        end
        %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
        %%%%%% ERROR %%%%%%
                error=0;
            for i=1:size(I)
        error = abs(I_aim_low_vds(i)-I_low_vds(i))+error;
            end
```

```
                toplam=0;
            for i=1:size(I)
        toplam = abs(I_aim_low_vds(i))+toplam;
            end
        error_vgs = error/toplam*100 % maksimum error

        error=0;
        for i=1:size(Ids)
            error = abs(Ids_aim(i)-Ids(i))+error;
        end
        toplam=0;
        for i=1:size(Ids)
            toplam = abs(Ids_aim(i))+toplam;
        end
        error_vds_new = error/toplam*100 % maksimum error

        if abs(error_vds_new-error_vds) < 0.1
            break
        else
            error_vds = error_vds_new
        end
        %%%%%%%%%%%%%%%%%%%%%%%%%%

        simulasyon_sayisi=simulasyon_sayisi+1
        if level == 1 && simulasyon_sayisi==...
                maksimum_simulasyon_sayisi
            break
        end

        if level == 2 && simulasyon_sayisi==2*...
                maksimum_simulasyon_sayisi
            break
        end

        if level == 3 && simulasyon_sayisi==2*...
                maksimum_simulasyon_sayisi + 2
            break
        end
        if hata == 3
            break
        end
    end

    %%%%%%%%%%%%%%% Iterations for DELTA %%%%%%%%%%%%%%%%%%%%%%%%
    if level == 3
        [ delta_n, Vds, Ids ] = delta_iteration(...
model_address, baslangic, son, command, step, Ids, Vds, Ids_aim,...
Vds_aim, ocean_address_vds, result_address_vds, delta_n_max, ...
error_vds, vdsat_difference );
    end

    level = level + 1
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Algorithm ends here

%%%%%%%%%%%%%%% Input Import / Ocean File %%%%%%%%%%%%%%
ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
    ocean_address_vds);
ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
    ocean_address_vgs);
if type == 'n'
    vd = 0.05;
    ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
        ocean_address_low_vds);
    vd = 1.8;
elseif type == 'p'
    vd = 1.75;
    ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
        ocean_address_low_vds);
    vd = 0;
end
```

```matlab

%%%%%%% Last Simulations %%%%%
[ Vds, Ids ] = simulation( ocean_address_vds, result_address_vds );
[ V_low_vds, I_low_vds ] = simulation( ocean_address_low_vds,...
    result_address_vgs_low_vds );
[ V, I ] = simulation( ocean_address_vgs, result_address_vgs );
A = importdata('./sonuclar/vth.dat');
vth = A;

if type =='n'
    vb = −0.4;
elseif type =='p'
    vb = 2.2;
end
ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
    ocean_address_vds);
ocean_file_edit(temp, vg, vd, vs, vb, Wdrawn, Ldrawn,...
    ocean_address_vgs);
[ Vds, Ids_vbs ] = simulation( ocean_address_vds,...
    result_address_vds );
[ V, I_vbs ] = simulation( ocean_address_vgs,...
    result_address_vgs );
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```



CURRICULUM VITAE

Name Surname: Aykut Kabaoğlu

Place and Date of Birth: 13.08.1993

E-Mail: kabaoglua@itu.edu.tr

EDUCATION:

- **B.Sc.:** 2016, Istanbul Technical University, Electrical and Electronics Faculty, Electronics and Communication Engineering
- **M.Sc.:** 2019, Istanbul Technical University, Graduate School of Science Engineering and Technology, Electronics Engineering

PROFESSIONAL EXPERIENCE AND REWARDS:

- 2018- Co-Founder of Ravinspect Technology.
- 2016-2019 Research Student in VLSI Duran Leblebici Laboratory, Istanbul Technical University
- 2014-2016 Intern in RF Laboratory, Istanbul Technical University

PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

- Kabaoğlu, A., & Yelten, M. B. (2017, June). A cryogenic modeling methodology of MOSFET IV characteristics in BSIM3. *In 2017 14th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)* (pp. 1-4). IEEE.
- Kabaoğlu, A., Solmaz, N. Ş., İlik, S., Uzun, Y., & Yelten, M. B. (2019). Statistical MOSFET Modeling Methodology for Cryogenic Conditions. *IEEE Transactions on Electron Devices*, 66(1), 66-72.