ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

RADIATION-INDUCED EFFECTS ON N-TYPE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICES: MODELING, SIMULATION AND OPTIMIZATION

M.Sc. THESIS

Sadık İLİK

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

N-TİPİ METAL OKSİT YARI İLETKEN ALAN ETKİLİ TRANZİSTORLAR ÜZERİNDE RADYASYON KAYNAKLI ETKİLER: MODELLEME, SİMÜLASYON VE OPTİMİZASYON

YÜKSEK LİSANS TEZİ

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Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

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HAZİRAN 2019

Sadık İLİK, a M.Sc. student of ITU Graduate School of Science Engineering and Technology 504161218 successfully defended the thesis entitled “RADIATION-INDUCED EFFECTS ON N-TYPE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICES: MODELING, SIMULATION AND OPTIMIZATION”, which he/she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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Date of Submission : 3 May 2019
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To my family,

FOREWORD

This master thesis aims better understanding radiation effects on devices and creating an easy to use model. Also aims to give designers best suitable design perspective with possible healing mechanisms and radiation tolerant devices shapes. The thesis is the result of 3 years of hard work from 2016 to 2019.

The project was under management of Asst. Prof. Dr. Mustafa Berke YELTEN and financed by the TÜBİTAK. In the scope of the project with modeling of cryogenic and radiation effects on devices and analog circuit design for this environments, I have done the radiation modeling section. Despite of experimental and other difficulties, I have learned lots of valuable knowledge about both my field and my personal evolution.

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I hope you enjoy your reading.

June 2019

Sadık İLİK
(Electronics and Communication Engineer)

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ABBREVIATIONS

ESA : European Space Agency
MOS : Metal Oxide Semiconductor
ELT : Enclosed Layout Transistor
TAEK : Turkish Atomic Energy Authority
SANAEM : Sarayköy Nuclear Research and Training Center
TID : Total Ionizing Dose
PCB : Printed Circuit Breadboard
SEE : Single Event Effects
EHP : Electron Hole Pair
STI : Shallow Trench Isolation
FET : Field Effect Transistor
MOSFET : Metal Oxide Semiconductor Field Effect Transistor
FinFET : Fin Field Effect Transistor
RINCE : Radiation Induced Narrow Channel Effects
RISCE : Radiation Induced Short Channel Effects
LDD : Lightly Doped Drain
CMOS : Complementary Metal Oxide Semiconductor
RHPD : Radiation Hardening by Process
RHBD : Radiation Hardening by Design
BSIM : Berkeley Short-Channel IGFET Model
TCAD : Technology Computer Aided Design

SYMBOLS

I_D : Drain current
W : Transistor channel width
L : Transistor channel length
V_{TH} : Threshold voltage
V_{DS} : Drain to source voltage
V_{GS} : Gate to source voltage
V_{BS} : Body to source voltage
N_{OT} : Inner oxide trapped charge
N_{IT} : Oxide-semiconductor interface trapped charge

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RADIATION-INDUCED EFFECTS ON N-TYPE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICES: MODELING, SIMULATION AND OPTIMIZATION

SUMMARY

In this work, radiation-induced effects on NMOS devices are investigated for different transistor sizes. Three different dose rates were applied with two different biasing configurations. In first configuration, NMOS devices were irradiated with the gates biased to 1.8 V and with the drain, source and body biased to 0 V. In the second configuration, NMOS devices were irradiated with the gates and drains biased to 1.8 V and with the source and body biased to 0 V. In total, 7 different doses were obtained. Before and after irradiation, the $\mathrm{I_D}$-$\mathrm{V_{DS}}$ and $\mathrm{I_D}$-$\mathrm{V_{GS}}$ graphs were extracted for different gate, drain and body voltages.

It is observed that the device size and number of fingers both have effects on the radiation tolerance of transistors, and the relative contribution of each changes. Sub-threshold leakage current increase which also depends on V_{DS} and V_{BS} voltage, threshold voltage shift, linear and saturation region currents changings among the radiation induced effects. Furthermore, time dependent healing effects and body-biasing effects were investigated. A parameter modification modeling approach was used to model irradiated transistors. Only an extra current source placed between drain and source to model the sub-threshold leakage current at $V_{GS} = 0$ V. After that, with “VTH0”, threshold voltage change, with “UA” linear region, with “VSAT” and “A2” saturation region, with “DELTA” transition region between linear and saturation regions and with “NFACTOR” sub-threshold slope are modeled. “K1” and “KETA” are used to include body-bias effects. This modeling approach suitable for all transistor sizes. But to obtain single model for all sizes, this modelling approach is applied to a long and wide channel transistor. Using an short and wide channel transistor and with “PVAG”, short channel effects were modeled. Finally, using an short and narrow channel transistor, with “DWG”,“WINT” and “K3” narrow channel effects were modeled. Created single model shows good agreement with experiments for different sized transistors. Lastly, extracted model were applied to simple circuit, ring oscillators with 5 inverters. Their frequency shift and power consumptions were compared with standard pre-rad model.

In the second section, NMOS transistors were irradiated with the configuration gates biased to 1.8 V and other three terminals drain, source and body biased to 0 V. Before and after irradiation, measurements were done with proper device configurations called straight configuration. Subsequently, the drain and source were swapped, and the same measurements were repeated. This second configuration is call reverse configuration. Given the symmetrical structure of the MOSFET transistors, pre-irradiation measurements were in strong agreement for the two measurement configurations. But after irradiation, sub-threshold leakage currents of straight configuration were much higher than those of the reverse configuration. Furthermore, all these effects were investigated using different transistors with different channel

lengths, widths and finger numbers. As a result, the most significant difference was observed with the smallest device. These differences between straight and reverse configurations can be attributed to different charge trapping concentrations in insulators near the drain and source regions of the device because of the different electrical fields at these regions. To test this idea, Sentaurus TCAD was used and traps were included in the insulator regions. A good agreement is observed between the result of these simulations and the experiments.

Finally, same sized one regular layout transistor and two ELTs with different shapes (octagonal and square) have been investigated according to their process variations, their radiation induced sub-threshold current shifts and its dependence on reverse body bias. It has been demonstrated that even if the layout symmetry of ELTs slightly increase the area consumption, it makes them less vulnerable to process variations. Finally, measurements have demonstrated that the even up to 1 Mrad dose, radiation tolerance and the electrical behaviour of ELTs is not depend on the shape of ELT.

N-TİPİ METAL OKSİT YARI İLETKEN ALAN ETKİLİ TRANZİSTORLAR ÜZERİNDE RADYASYON KAYNAKLI ETKİLER: MODELLEME, SİMÜLASYON VE OPTİMİZASYON

ÖZET

Bu tezde, radyasyonun n-tipi alan etkili tranzistor cihazlar üzerindeki etkileri incelenmiş, radyasyona bağlı etkiler için literatür araştırması yapılmıştır. Bir cihaz üzerindeki radyasyon etkilerinin oluşum mekanizmaları incelenmiştir. Bu kapsamda adım adım radyasyon kaynaklı etkilerin nedenleri araştırılmıştır. Bunun sonucunda cihazlar üzerindeki radyasyon etkilerinin, yalıtkan malzemelerde oluşan tuzak yüklerden kaynaklandığına ulaşılmıştır. Oluşum mekanizması araştırıldığında daha önce araştırmacılar tarafından ortaya konulan teoriye ulaşılmıştır. Bu teoride öncelikle gelen radyasyondan alınan enerji ile elektron ve delik çifti oluşmaktadır. Bu oluşan yeni çiftlerden bir çoğu hızla tekrar birleşip yok olurken, bir kısmı ise birbirinden ayrılmakta ve yalıtkan içerisinde hareket etmektedirler. Yalıtkan kristal örgüsü içerisinde ve/veya yalıtkan-silisyum arayüzünde, değişik mekanizmalar ve kusurlar ile yükler sabit kalmakta ve tuzaklanmaktadır.

Radyasyon etkilerinin oluşmasında yalıtkanlar etkili olduğundan, farklı yalıtkan kalınlıklarına bağlı olarak cihazların radyasyondan etkilenme miktarları da farklı olmaktadır. Eski teknolojilerde geçit yalıtkanının kalınlığı yüksek iken, gelişen teknoloji ile bu kalınlık azalmış olup, radyasyonun bu bölge üzerinde oluşturduğu etki de azalmıştır. Diğer yandan, sığ çukur ayrıştırma bölgelerinin kalınlığı yüzlerce nanometre boyutlarında kalmış ve bu etkilere hala açık bulunmaktadır.

Kullanılan cihazları radyasyona daha dayanıklı hale getirmek için tarih boyunca farklı yöntemler uygulanmıştır. Bunlardan ilkinde, ışınıma maruz kalacak bölgelerin bir koruma kalkanı ile korunması ve ışınımın bu bölgelere ulaşamadan gücünü yitirmesi amaçlanmıştır. Ancak bu uygulamadan haberleşme sistemlerinde uygulama zorluğu gibi birçok nedenden ötürü uzaklaşılmıştır. Günümüzde, sistemlerin ışınıma dayanıklılıkları iki temel yaklaşım ile sağlanmaya çalışılmaktadır. Bunlardan ilki doğal olarak ışınıma dayanıklı malzemelerden yapılmış cihazların ve yine dayanıklı yapıların kulanılması ile oluşturulan süreç ile ışınım dayanıklılığı olmaktadır. Buradaki dezavantajlardan bazıları da bu tür işlemlerin yüksek maliyeti ve tranzistorların tümleşik devre üzerinde geniş yer kaplaması olarak gösterilebilir.

İkinci yaklaşımda ise ışınımın tranzistorlar üzerindeki etkilerinin önceden bilinmesi ve tasarım aşamasında bunlar da dikkate alınarak ışınım sonrasında da istenilen aralıkta çalışabilecek yapıların kurulabilmesi sağlanmaktadır. Bu noktada ışınım etkilerinin modellenmesi büyük bir öneme sahip olmakta, etkilerin benzetimlerde gözlenebilmesi uygun bir model oluşturulması ile sağlanabilmektedir. Bu tezde de bu yöntem tercih edilmiş ve ışınım etkileri modellenmiştir.

Tezde kullanılan tranzistorlar, 180 nm tamamlayıcı-metal-oksit-yarıiletken teknolojisi ile üretilmiş olup, farklı özelliklere sahiptirler. Bu özelliklerin başında kanal

uzunlukları ve kanal genişlikleri, serim sırasında seçilen parmak sayıları gelmektedir. Ayrıca, ışınım dayanıklılıkları olduğu bilinen ve kapalı-serim-tranzistor adlı yapılar da yongaya eklenmiş ve bu yapılar karşılaştırılarak incelenmiştir.

Işınım testleri TAEK (Türkiye Atom Enerjisi Kurumu) bünyesinde SANAEM'deki (Sarayköy Nükleer Araştırma ve Eğitim Merkezi) Gama Işınlama Tesisleri'nde yapılmıştır. Bu testler sırasında Kobalt atomunun radyoaktif bir izotopu olan Kobalt-60 kullanılmıştır. Işınım sırasında yongalara gerilim uygulayabilmek için baskı devreler tasarlanmış ve üretilmiştir. Sonrasında bu baskı devreler aracılığıyla yongalara ışınıma dayanıklı kablolar ve güç kaynakları yardımıyla ışınım odası dışından gerilim uygulanmıştır.

İki ayrı baskı devre tasarımı ile iki ayrı kutuplama şekli uygulanarak deneyler gerçekleştirilmiştir. İlk deney grubunda tranzistorların geçitleri, 1.8 V'a; savakları, kaynakları ve gövdeleri de 0 V'a bağlanmıştır. Bu testler, Avrupa Uzay Ajansı'nın (ESA) belirttiği şekilde yapılmış, doz hızı belirtilmiş pencerelere uygun seçilmiş ve tranzistorlar en kötü durum olarak isimlendirilen en fazla değişime uğradıkları yukarıda belirtilen koşullarda kutuplanmıştır. Ayrıca yine aynı yönergede belirtilen üzere ölçümler; yongalar ışınım bitiminden itibaren iki saat içinde tamamlanmıştır. Bu gruba üç adet yonga yerleştirilmiş ve ışınım ortamından 50 krad, 100 krad ve 300 krad dozlarında çıkarılmışlardır.

İkinci grupta aynı kutuplama şeması kullanılmış fakat tranzistorlar daha yüksek doz hızına maruz bırakılarak daha yüksek dozlar hedeflenmiştir. Bu grupta iki yonga kullanılmış ve 500 krad ile 1 Mrad dozlarına erişmeleri sağlanmıştır.

Üçüncü grup için tasarlanan baskı devrelerle ışınım sırasında tranzistorların geçit ve savaklarına 1.8 V, kaynak ve gövdelerine ise 0 V uygulanmıştır. Bu grupta iki yonga kullanılmış ve 355 krad ile 651 krad dozları elde edilmiştir.

Işınım öncesi ve sonrası ölçümlerde 50 mV, 200 mV, 400 mV ve 1.8 V olmak üzere dört farklı savak gerilimi için savak gerilimi sabit tutularak geçit gerilimi 0 V'tan 1.8 V'a sabit gerilim adımlarıyla arttırılarak geçit gerilimine bağlı savak akımı (I_D-V_{GS}) grafikleri elde edilmiştir. Yine aynı tranzistor için geçit gerilimi 0 V'tan başlayarak 1.8 V'a kadar 300 mV adımlarla arttırılarak ve her geçit gerilimi için savak gerilimi 0 V'tan 1.8 V'a arttırılarak savak gerilimine bağlı savak akımı (I_D-V_{GS}) grafikleri elde edilmiştir. Bahsedilen ölçümler, sırasında gövde ve kaynak 0 V'a bağlanmış, daha sonrasında aynı ölçümler gövde -300 mV'a bağlanarak tekrarlanmıştır.

Öncelikle, tranzistorlar üzerindeki ışınım etkilerinin tranzistorların boyutlarına, parmak sayılarına ve gövde gerilimine göre davranışları incelenmiş, bunlar arasında karşılaştırmalı analiz yapılmıştır. Ardından bu etkilerin BSIM 3v3 modeli baz alınarak modellemesi yapılmıştır.

Modelleme yapılırken, yeni eşitlikler ekleme ya da matematiksel bir model yerine elde bulunan tranzistor modeli uygun hale getirilmiştir. Bu yöntemin seçilmesindeki birincil amaç modeli kullanacak tasarımcıya fazladan benzetim yapmadan, kolaylıkla kullanabileceği bir model sağlamaktır.

Modelleme aşamasında ilk olarak, ışınım sonrasında tranzistor karakteristiklerinde oluşan değişiklikler araştırılmış ve ölçümler ile de kontrol edilmiştir. Bu kapsamda elde edilen bulgularda tranzistorların geçit gerilimi verilmeksizin oluşan kaçak savak akımlarında artış, eşik gerilimlerinde değişim, lineer ve doyma bölgesi akımlarında değişim gözlenmiştir. Ayrıca bu değişimlerin tranzistorların boyutlarına, parmak sayılarına, gövde gerilimlerine, geçit gerilimi uygulanmazken dahi uygulanan savak gerilimlerine bağlı olduğu gözlenmiştir. Ayrıca tranzistorların zamana bağlı iyileşme özellikleri de incelenmiştir.

Bahsedilen ışınım etkileri modellenirken öncelikle geniş ve uzun kanala sahip bir tranzistor kullanılarak savak kaçak akımının modellenmesi ile başlanmış ve harici bir akım kaynağı savak ile kaynak arasına paralel olarak yerleştirilmiştir. Akım kaynağının değeri olarak her tranzistor için 0 V geçit gerilimi altında çıkarılmış savak gerilimine bağlı savak akımı ölçümü kullanılmış ve böylece kaçak akımının bağlı olduğu boyut etkileri, parmak sayısı etkileri, gövde gerilimi etkileri ve savak gerilimi etkileri dahil edilmiştir. İkinci aşamada benzetim ile ölçüm arasında eşik gerilimi farkı kullanılarak eşik gerilimi modellenmiştir ve bunun için “VTH0” parametresi kullanılmıştır. Ardından lineer bölge modellemesi için “UA” ve doyma bölgesi modellemesi için “VSAT” ve “A2” parametreleri kullanılmıştır. Lineer bölge ile doyma bölgesi arasındaki geçiş için de “DELTA” parametresi kullanılmıştır. Eşik gerilimi altındaki eğimin modellenmesi için “NFACTOR” kullanılarak tek bir tranzistor için gövde gerilimleri eklenmeden model tamamlanmıştır. Bir sonraki aşamada, eşik geriliminin gövde gerilimine bağlı etkisi “K1” ile, doyma akımının gövde gerilimine bağlı etkisi “KETA” parametreleri ile modele dahil edilmiştir.

Sonraki aşamada öncelikle kısa ve geniş kanala sahip bir tranzistor kullanılarak kısa kanal etkileri “PVAG” parametresi ile ve daha sonrasında kısa ve dar kanala sahip bir tranzistorun ölçümleri kullanılarak dar kanal etkileri “DWG”,“WINT” ve “K3” ile modellenmiştir. Sonuç olarak, farklı boyutlarda kullanılabilen gövde gerilimi etkilerini de içeren tek bir model elde edilmiştir.

Daha sonraki kısımda savak ve geçitlerine 1.8 V, gövde ve kaynaklarına 0 V uygulanarak ışınıma maruz bırakılmış yongalar kullanılmıştır. Öncelikle metal-oksit-yarıiletken-alan-etkili-tranzistorların savak ve kaynak simetrileri literatürden ve deneylerle de tekrar kontrol edilmiş ve bu yapılarda savak ile kaynağın yer değiştirerek birbirleri yerine kullanılabilecekleri görülmüştür. Daha sonra bu tranzistorlar belirtildiği gibi ışınıma maruz bırakılmış, ardından aynı savak ve kaynak simetrisi kontrol edilmiştir. Burada gözlendiği üzere, simetrik olmayan kutuplama koşullarında yapılan ışınım testlerinden sonra ölçümler yapıldığında normal durum olarak isimlendirilen savağın pozitif gerilime, kaynağın ise 0 V’a bağlanarak yapıldığı ölçümlerdeki kaçak akımı değerlerinin ters olarak isimlendirilen ve savağın kaynak; kaynağın da savak olarak kullanıldığı ölçümlere göre daha yüksek olduğu gözlenmiştir. Bu etkinin sebepleri incelenirken bilgisayar destekli benzetim programlarından yararlanılmış ve bu kutuplama koşullarında cihazdaki yalıtkanlarda oluşan elektrik alanlar gözlenmiştir. Beklendiği gibi, aradaki potansiyel farkın fazla olmasından kaynaklı kaynak bölgesine yakın yalıtkanlarda elektrik alan daha yüksek olurken, geçit ve savak aynı gerilimde olduğu için savak bölgesine yakın yalıtkanlarda elektrik alan daha düşük olmaktadır. Bu durum, kaynak bölgesinde daha fazla pozitif yüklü tuzağın oluşmasına neden olmaktadır. Kaynak çevresinde savak çevresine göre daha fazla tuzak bulunan durum, benzetim uygulaması aracılığıyla test edilmiş; deney sonuçlarına benzer sonuçlarla karşılaşılmıştır. Böylece içerisinde kaynak-savak simetrisine sahip iletim kapısı gibi devrelerde kaçak akımların etkilerinin, kaynağın artı ve eksi uçlarının değiştirilmesi ile azaltılabileceği ve ışınım dayanıklılığının bu şekilde arttırılabileceği gösterilmiştir.

Son olarak, aynı boyuta sahip kare ve sekizgen şeklinde geçide sahip olarak oluşturulan kapalı-serim-tranzistorlar ve aynı boyutta normal bir tranzistor arasında karşılaştırmalar yapılmıştır. Bu çerçevede öncelikle üç cihazın ışınım dayanıklılıkları incelenmiş ve beklenildiği gibi kapalı-serim-tranzistorlar 1 Mrad dozda dahi ilk özelliklerini korurken, normal tranzistorda bariz değişiklikler gözlenmiştir. Daha sonrasında bu üç yapı, üretim çeşitliliği, gövde gerilimi etkilerine bağlı savak akımları değişimi ve kapladıkları alan açılarından incelenmiş ve özellikle iki kapalı-serim-tranzistorlar karşılaştırılmıştır. Sonuçta, sekizgen yapının üretim çeşitliliğine daha dayanıklı olduğu gözlenmiş ancak yine sekizgen yapının alan tüketiminin kare yapıya göre %2.78 daha fazla olduğu belirlenmiştir. Üretim çeşitliliğine daha dayanıklı olmasının nedeni olarak üretimin serimde dik açılara izin vermemesi dolayısıyla kare yapıda köşelerde küçük uzunlukların bulunması ve bu uzunlukların cihazı üretim çeşitliliğine karşı daha savunmasız bir duruma getirmesi olduğu şeklinde açıklanmıştır. Bu kısımda amaç, bir tasarımcının bu yapıda bir cihaz çizimi sırasında üretim çeşitliliğinden mümkün olduğunca kaçınabilmesi için en uygun yapının belirlenmesidir.

1. INTRODUCTION

1.1 Literature Review

Robustness to radiation, which can cause ionizing damage in materials, for example, gamma radiation, is an important property for electronic circuits and devices which will be used in particle accelerators, space research, and nuclear facilities. To work safely under harsh conditions, these systems should be radiation hard enough. In order to achieve this qualification, various methods used by practicing engineers and researchers have been applied over the years. As the first prevention, all components were shielded against the ionizing radiation. It is provided to attenuate exponentially the energy of the ionizing radiation depending on the type of the shielding material and its depth [6]. Large overhead requirements and excessive costs are some important disadvantages of this method. Nowadays, two different approaches have been proposed to acquire radiation hardness. The first one, radiation hardening by the process, (RHBP), is proposing to make changes in the fabrication steps. However, the second one, radiation hardening by design (RHBD), is aiming to employ various design and layout techniques through leaving the manufacturing stages intact.

The effects of radiation on MOSFETs can be grouped under two main categories, Single Event Effects (SEE) and TID. Over the past two decades, many studies have investigated different aspects of these two categories and the radiation-induced effects [7–11]. Some examples include reverse body bias effects [12], bias condition effects during irradiation [13], and the effects of voltages on device characteristics.

To assess the level of radiation hardness, it is proper to record the total dose of radiation taken by an electronic device throughout irradiation, which is called TID. Ionizing radiation induces electron-hole pairs (EHPs) both in insulator and semiconductor parts of an electronic device. Most of the EHPs in the semiconductor and insulator portions recombine in a short time and leave no damage. However, some EHPs in insulators result in relatively high densities of charge trapping centers, that can retain their spots for the long term [1]. These traps can reduce the mobility of charge carriers. They can also act as hopping centers in the field oxide, which is located between two adjacent transistors, and lead to an increased sub-threshold leakage current. With sizes of transistors scaling down in recent technologies, gate insulator thickness becomes shorter, so diminishing the number of traps being formed in the gate insulator. Because of its large thickness, most of the damage comes from the traps occurring in the shallow trench isolation (STI), which replaces the field oxide in modern transistors [1, 14]. Increased leakage current through STI leads to increased sub-threshold current and reduces threshold voltage for the impacted transistor [3,3,15–22]. With an introduction here, a more detailed radiation induced effects on transistors are done in the next section and explained.

TID induced effects have been modeled previously with different approaches [5, 23–27]. In [5], they have modeled for different sized technologies. However, body-bias effects and VDS effects on leakage current are not covered. Also, modified parameters are not mentioned clearly, so it is not easily applicable by different researches. In [23], they model TID effects with a different approach that compensate for TID effects with electrical stress. In [24] it is modeled with a parasitic transistor approach at the edges of STI with settling parasitic transistors widths and lengths. On the other hand, it is not include full parameters of a transistor, length and width dependence, and body effects. In spite of circuit applications in [27], still, size effects are not included.TID Effects also modeled using macro models [26]. It is done for double-gate FinFETs with using standard parameter extraction tools instead of the new one.

One popular technique to implement RHBD is the building enclosed layout transistors (ELT). ELTs are designed to avoid the leakage current through STI by having a ring shaped gate, where either the drain or the source is located inside of the ring, and the other terminal is situated outside of the ring. In this configuration, there is no STI structure at the edge of the gate, so it becomes radiation tolerant up to doses above hundred of krad doses [28–31]. ELTs can be of different shapes, including square, hexagonal, octagonal, and circular (annular). Even though many research studies focusing on ELTs, none of them have focused on the similarities and differences of the ELTs having different enclosure forms.

1.2 Radiation Effect Mechanism and Irradiation Effects on MOSFET

The total ionizing dose is the total amount of energy deposited by a particle that results in EHP production. The transferred energy determine the density of EHPs generated [17].In this case, rad which is a typical unit of TID used in electronic devices defined as one hundred ergs absorbed per gram [3].

The physical processes after the initial deposition of ionizing energy until the creation of defects begin with the generation of ehp, which is formulated in Equation (1.1). κ_g is the EHP density, E_p is the mean ionization energy, and ρ is the material density [3]. After that creation, a fraction of the generated EHPs recombine. Next, remaining free carriers after recombination transport in the oxide. After this transportation, there are two probabilities for free carriers. First one is the formation of net positive trapped charge via hole trapping in defect precursor sites.

$$\kappa_g\left[\frac{\#ehp}{cm^3 rad}\right] = 100\left[\frac{erg}{g}\right]\left[\frac{1}{rad}\right]\bullet\frac{1}{1.6\times10^{-12}}\left[\frac{eV}{erg}\right]\bullet\frac{1}{E_p}\left[\frac{\#ehp}{eV}\right]\bullet\rho\left[\frac{g}{cm^3}\right] \tag{1.1}$$

The second one is the formation of interface traps via reactions involving hydrogen with a simple reaction shown in Equation (1.2) [5, 15, 17, 32, 33]. D^+ refers to the resulting interface trap.

$$SiH + H^+ \rightarrow D^+ + H_2 \tag{1.2}$$

Allover trap creation processes are summarized in Figure 1.1 [1].

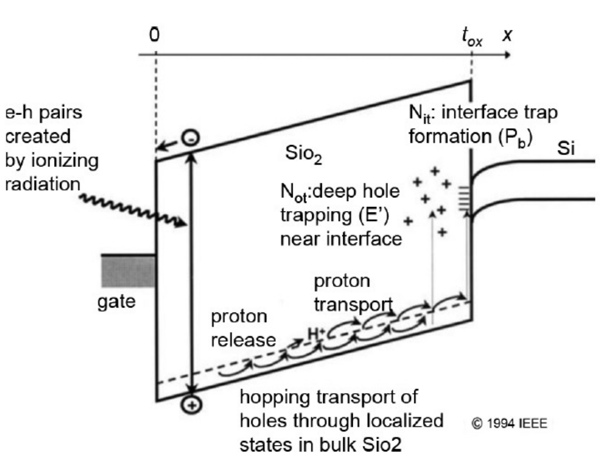


Figure 1.1 : Radiation effect and trap creation mechanism on insulators [1].

Radiation-induced effects in literature can be grouped under four main categories.

1.2.1 Threshold voltage and mobility shift

Trapping of positive charges is a more probable inner oxide (N_{OT}). Trapped charges in the insulator layer shift V_{TH} to lower values for both NMOS and PMOS. Namely, for NMOS V_{TH} decreases and for PMOS absolute value of V_{TH} increases. With this phenomena and some others, for many applications, radiation tolerance of NMOS is the main problem [34].

On the other hand, interface traps have the opposite effect on the threshold voltage. Increasing N_{IT} concentration has the effect of decreasing mobility of the carriers and thereby increasing the threshold voltage in NMOS [34]. According to the changing the density of oxide trapped charges and density of interface traps, V_{TH} changes have been modeled using a surface potential approach by Esqueda and Barnaby [2]. They have used a standard FET model and a controlled voltage source as shown in Figure 1.2. According to N_{OT} and N_{IT} values, they have modeled the threshold voltage change and applied to the gate this voltage with the Verilog-A model.

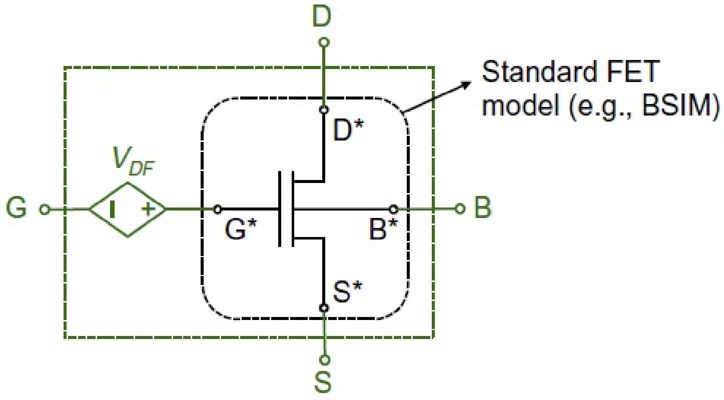
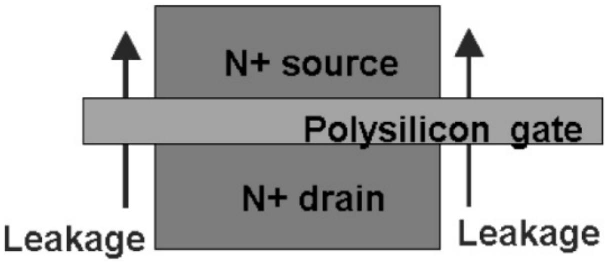


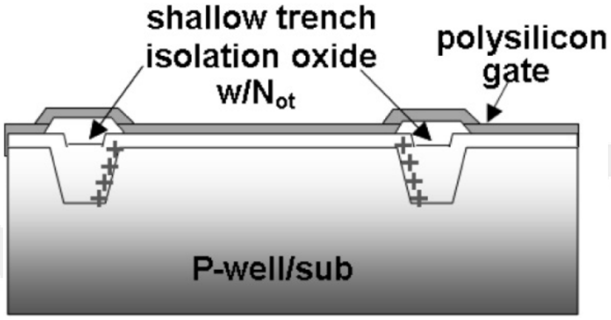
Figure 1.2 : Modeling of radiation-induced threshold shift with an external voltage source [2].

1.2.2 Inter-device leakage

Inter-device leakage is because of the inversion channels between the n^+ drains and sources of two adjacent NFETs, the n^+ drain/source of one NFET and an n-type well, or between two n-type wells. Radiation induced positive charge trap buildup along the isolation oxide layer causes the inter-device leakage [3, 32]. Inter-device leakage currents and responsible charges with top view and its cross section are shown in Figure 1.3.



(a)



(b)

Figure 1.3 : Inter-device leakage current in a transistor with a) top view b) cross section [3].

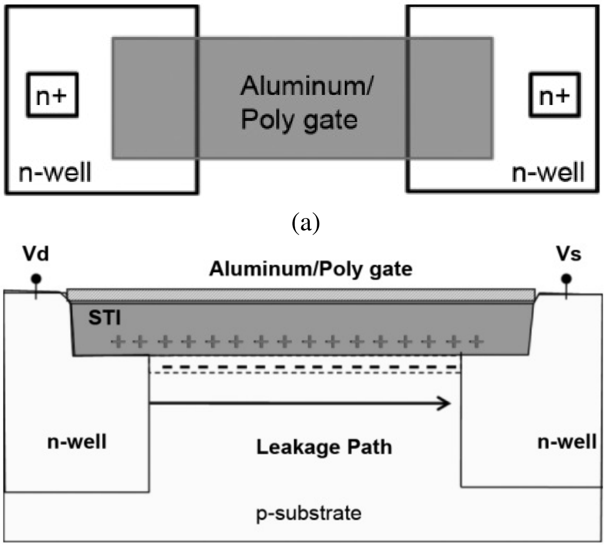
1.2.3 Intra-device leakage

Charge trapped in the isolation dielectric along the sidewalls creates a leakage path that allows to current flow between n-wells. With the top view and cross-section view, this effect is illustrated in Figure 1.4 [4].

Radiation-induced intra-device leakage is modeled before by different researchers [5, 32]. The main problem is the edge Shallow Trench Isolation (STI) corner edge modeling in intra-device leakage and they have used the assumption of [32] parallel devices with changing the width. In [5], they have created a Verilog-A model which includes a controlled current source between the drain and source as shown in Figure 1.5.

1.2.4 Radiation-induced narrow channel effects (RINCE) and radiation-induced short channel effects (RISCE)

It is shown that before the device length and width effects under high radiation dose. It is stated that because of the charge trapping in the lateral isolation oxide, they



(a)

(b)

Figure 1.4 : Intra-device leakage current between transistors with a) top view b) cross section [4].

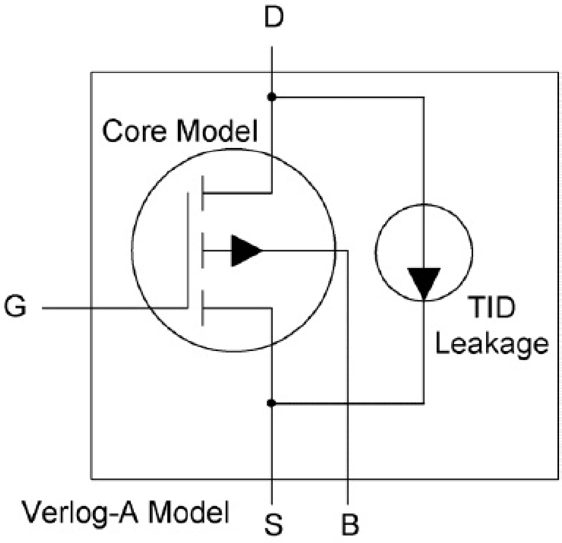


Figure 1.5 : Modeling of lekage current with an external current source [5].

can modify the electric field in the main transistor. So, performance degradation is observed at narrow channel transistors when compared with wide channel transistors. This phenomenon is called radiation-induced narrow channel effects (RINCE) [35].

The underlying mechanism of this effect is explained as the electric field at the transistor decreases the available channel width because it changes channel inversion properties. Also, this phenomena reveals itself as a degradation in the maximum drain current [35].

Especially on PMOS transistors, RINCE has dramatic consequences. But for NMOS devices, the interface and oxide trapped charges partially compensate their effects, and results are less remarkable. Results in [35] are compared for 130 nm and 60 nm technologies.

Origin of radiation-induced short channel effect (RISCE) is explained with positive charge trapping in the spacer oxide or at its interface with lightly doped drain (LDD) region, beneath it which charge cause the RISCE. This phenomena leads to modifying the effective doping and affecting the overall channel resistance [35].

1.3 Purpose of Thesis

In this thesis, radiation-induced effects on different transistors, and naturally radiation tolerant transistor structures called ELTs are investigated. Firstly, Total Ionizing Dose (TID) effects on transistors are investigated depend on transistor dimensions, the number of fingers,V_{DS} and V_{BS} effects, and total absorbed dose are investigated and shown. After that, a radiation aware BSIM3v3 transistor model is developed. With an approach to creating an easy to use for designers, TID effects on transistors are proposed. In this model, a single model of a dose for different sized transistors, V_{DS} and V_{BS} bias awareness is provided.

Secondly, TID effects depend on biasing conditions during irradiation is investigated. Drain and source symmetry of a MOSFET is shown, and the effects of biasing during irradiation results on this symmetry are investigated. A deeper understanding of biasing effects during irradiation on charge trapping symmetry is aimed. Measurement results are compared with simulations using TCAD tools. Also, a possible recovery for proper circuits with drain and source symmetry is proposed.

Finally, radiation tolerances of two different layouts with the same dimensions of ELTs, process variations, and area consumptions of them are investigated and compared together with a standard layout transistor. Finding the best layout shape depend on the desired features for ELT structures is aimed.

In Section 2, tests and used test chips are shown. In Section 3, radiation induced effects and modeling of them is investigated. After model extraction, the model is applicated to simple ring oscillator circuits. Biasing effects during irradiation and a new effect is discussed in Section 4. Two differently shaped ELT structures are compared in Section 5 and finally Section 6 concludes all the thesis.

2. TEST CHIP AND EXPERIMENTS

2.1 Test Chip

A model that will cover analog, digital, and radio frequency circuit applications are aimed in researches. So, this model has to include body bias effects, all short channel, and narrow width effects. Moreover, Two types of ELTs which have different shapes have been included to investigate its effects on other effects such as process variations and radiation tolerances. ELTs, regular layout transistors with different properties and other devices not related to this work have been fabricated with a commercial 180 nm CMOS technology whose micrograph can be visualized in Figure 2.1.

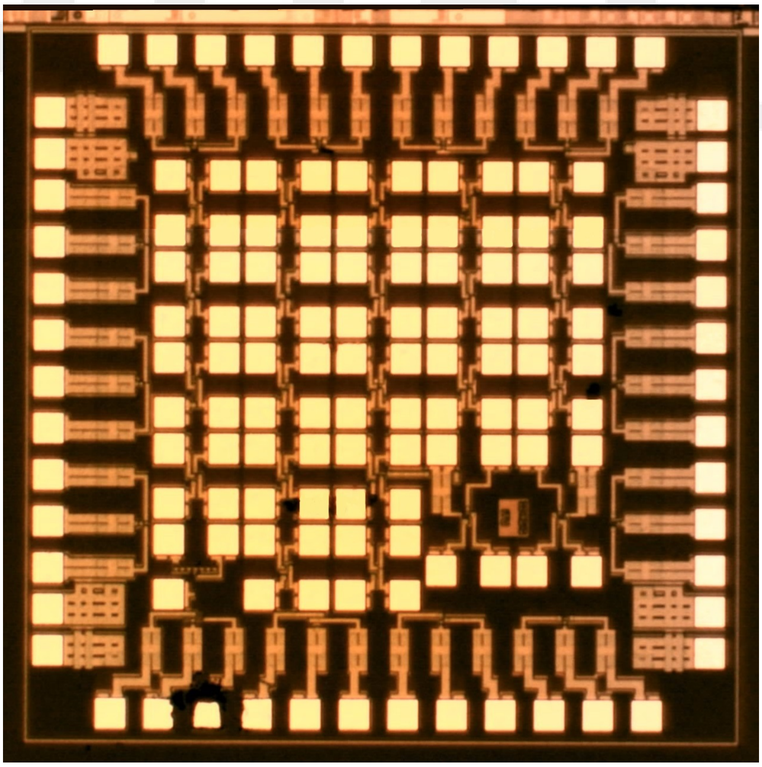


Figure 2.1 : Micrograph of the fabricated test chip.

For radiation tests, transistors which drain, source and gate terminals have been connected to the independent pads. An electro-static-discharge (ESD) protection the mechanism has been constructed, and biases have been applied for this protection mechanism with pads called V_{DD} pads which have been applied 1.8 V and ground pins which have been applied 0 V. Bulk terminals of all NMOS transistors have been connected to each other. Finally, they have been connected to these ground pins.

All these transistor pins have been located at the edges of the chip. Thus, these pins have been connected to packages. Pads at the inside of the chips have been used for probe station measurements, and they have been used for non-irradiation measurements. Names and features of transistors which are used in these work are shown in Table 2.1. Marked transistors T7 and T8 are both ELTs and their shapes are declared.

Table 2.1 : Sizes and specifications of transistors.

Transistor	Width	Length	Finger Number/ELT Shape*
T1	0.24 μm	0.18 μm	1
T2	10.0 μm	0.18 μm	4
T3	0.24 μm	10 μm	1
T4	10 μm	10 μm	4
T5	35 μm	0.5 μm	1
T6	35 μm	0.5 μm	7
T7*	35 μm	0.5 μm	Square*
T8*	35 μm	0.5 μm	Octagonal*

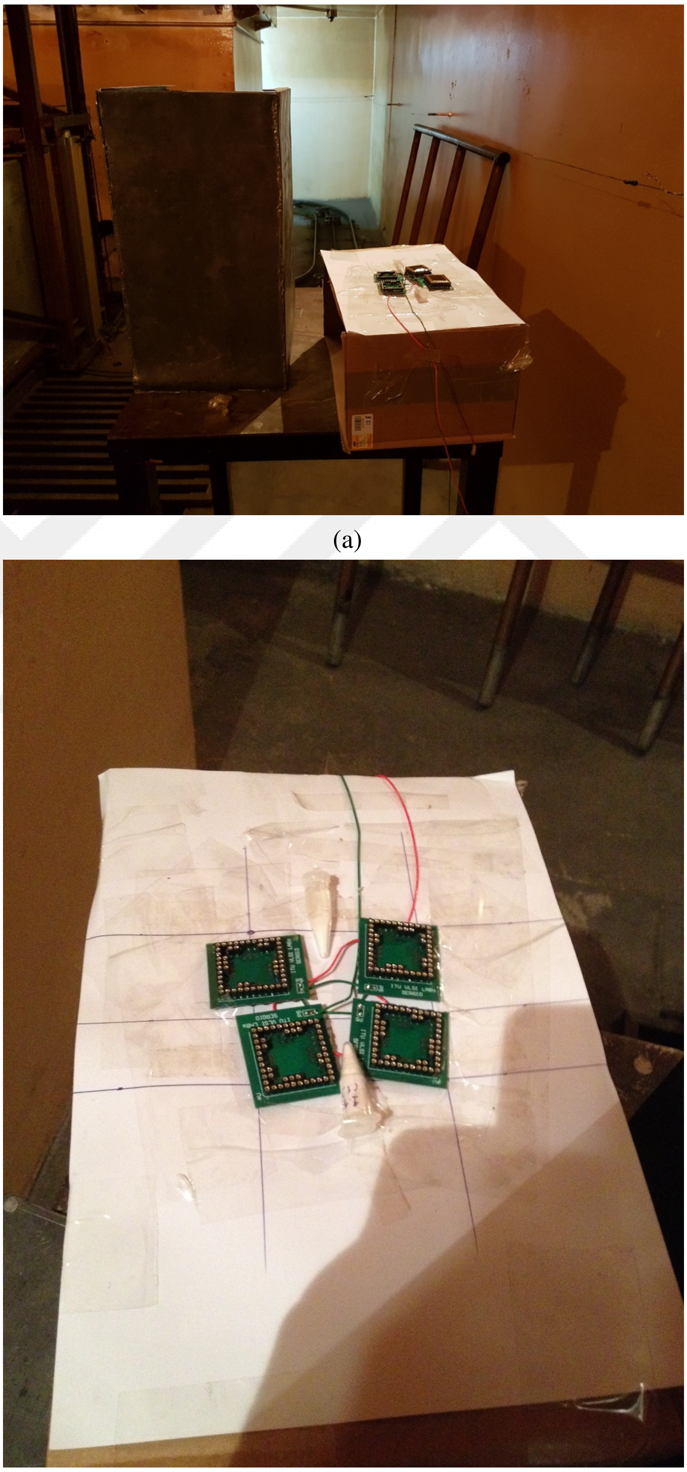
2.2 Tests

2.2.1 Radiation tests

Radiation tests were conducted in the Turkish Atomic Energy Authority (TAEK) Sarayköy Gamma Radiation Department, in Ankara, Turkey. A Cobalt-60 gamma ray source was used for experiments.

Cobalt-60 is useful in the industry because of its some advantages. Firstly, it has 5.27 year half-life, so that it has much less radioactive waste. Moreover, it decays two photons with 1.17 Mev and 1.33 Mev energies. These energies low enough to do not cause any core reaction, so it is safe to use in different areas. Sterilization, cross-linking in polymers are some other examples of usage areas of Cobalt-60.

Some photos from radiation environments are shown in Figure 2.2. The designed PCBs were fixed on a box, and chips were plugged on PCBs. Dosimeters were also attached near to chips to confirm that desired doses were taken correctly by the devices. After that, this box was placed in the boxes of lead (Pb).



(a)

(b)

Figure 2.2 : Photos of radiation test environment and irradiated chips and PCBs.

In Figure 2.3, final view before the irradiation of the radiation environment is shown. Two groups of chips are located in the boxes which are marked with red rectangles. Radiation source raised near group 2, so it had a higher dose than group 1.

Figure 2.3 : Photos of radiation environment with where two groups of.

In the experiments, three different dose rates were chosen for three groups of chips.The first group was irradiated with a 34.87 krad/h dose rate, which is in the permitted dose rate window of the European Space Agency (ESA). To obtain receiving doses of 50 krad, 100 krad, and 300 krad, three chips were irradiated at different times.

The second group consists of two chips, which were placed close to the source to obtain higher dose rates in less time. The chips were irradiated with 500 krad and 1 Mrad doses and a 252.8 krad/h (Si) dose rate was used.

In these two groups, transistors were biased with the worst case bias conditions, in which the gate terminal was connected to 1.8 V and the source, drain, and body terminals were connected to the ground potential.

In the third group, 355 krad and 641 krad doses were applied to the two chips. In contrast to the other two groups, these devices were irradiated while the drain and gate terminals were at 1.8 V and the other two terminals were at ground potential.

Shield boxes of Pb were used in all experiments to provide uniformity. Pb boxes allow only directly released photons to pass from the Cobalt-60 radiation source; thus, all other reflected and low energy photons were blocked. Therefore, the desired 5%

maximum nonuniformity, as declared in the ESA rules, was obtained [36]. Radiation tolerant cables (up to 10 Mrad) were used for biasing devices with a power supply outside of the radiation environment.

Before and after irradiation, I_D-V_{GS} curves with 50 mV, 200 mV, 400 mV and 1.8 V drain biases were extracted. Moreover, I_D-V_{DS} curves from 0 V to 1.8 V gate biases with 300 mV steps were extracted. All measurements were repeated with -300 mV V_{BS} voltage and completed in two hours after the chips were removed from the radiation environments.

2.2.2 Variability tests

To assess the process variability characteristics of the ELTs along with the regular layout transistor, statistics of the measurements should be generated. For this purpose, 25 regular transistors, 29 square shaped ELTs, and 29 octagonal shaped gate ELTs have been measured. Four transistors for all types are chosen from packaged chips, each taken from a different wafer. A printed circuit board is used to measure these packaged chips using a semiconductor test fixture box. Remaining chips were bare, and their measurements were done on a probe station. Keysight B1500A Semiconductor Device Analyser was used for all measurements, and they have been performed at 23°C. To clarify the differences between the packaged chip and the probe station measurements, which may arise due to packaging parasitics, results from each group were separately examined. It has been observed that these parasitics have a negligible contribution. Therefore, results from packaged and bare dies are merged, and they have been analyzed together.

3. RADIATION EFFECTS AND MODELING

3.1 Radiation Experiment Results

First, radiation-induced effects on a transistor that had a 0.35 μm width and 0.5 μm length were investigated. This transistor was chosen because it has nearly no short channel and narrow width effects. The sub-threshold leakage current, which was at 0 V gate bias, increased as expected after radiation test measurements depending on the radiation dose level, as shown in Figure 3.1. Up to 50 krad, there was no significant change. With the 100 krad dose, there was a slight but observable change. On the other hand, the sub-threshold leakage current increased to nearly 1.5 μA, 2.5 μA, and 4.5 μA levels with the 300 krad, 500 krad and 1 Mrad doses, respectively. These sub-threshold currents were almost 10^3 times larger than at initial conditions.

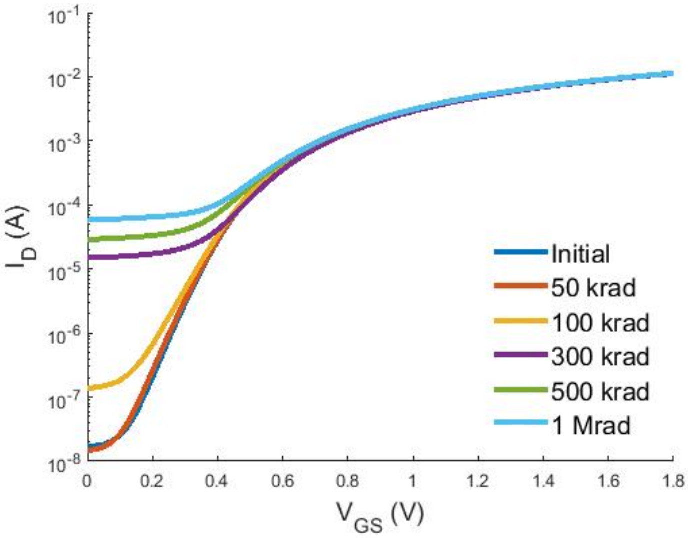
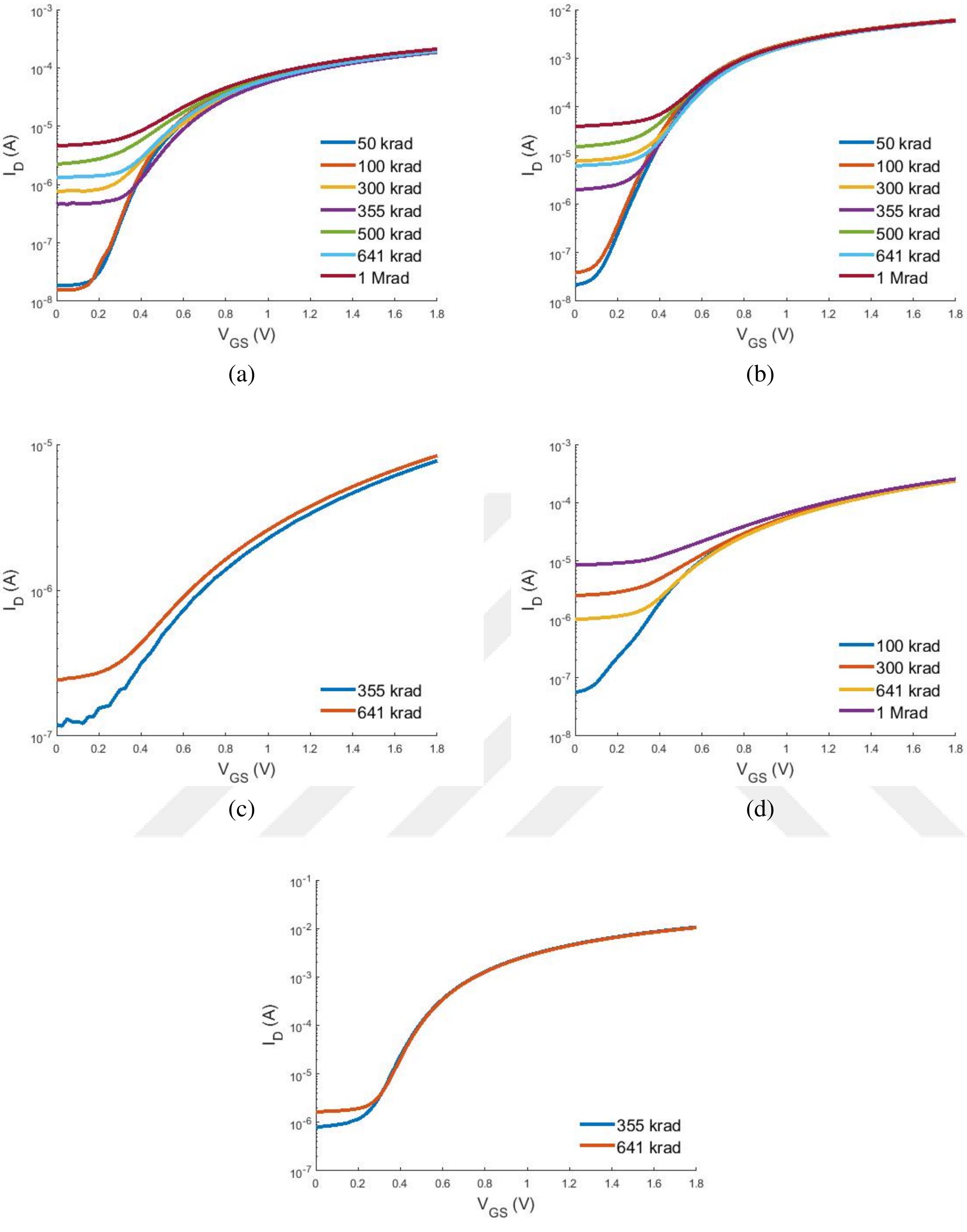


Figure 3.1 : Sub-threshold current depend on the radiation dose for T6.

For all transistors, radiation-induced changes depend on dose is shown in Figure 3.2. All doses are not shown for all transistors since some doses were not applied all transistors and some of the transistors were broke out because of other effects such as ESD.



(a) (b)

(c) (d)

(e)

Figure 3.2 : I_d - V_{gs} graphs while $V_{ds} = 1.8$ V for different doses of a) T1, b) T2, c) T3, d) T4 e) T5

Moreover, time-dependent radiation-induced effects were investigated. Time dependent healing was recorded for all of the transistors that had doses above 50 krad; at 50 krad, no change occurred, even immediately after radiation exposure. For the 100 krad dose, a small change was observed right after exposure, and then time dependent healing was observed. Finally, after 100 °C annealings, the device fully returned to its initial condition.

Time-dependent healing and annealing effects were clearly seen, especially for the devices that received the 300 krad dose. For example, for the $W/L = 0.24\ \mu m/0.18\ \mu m$ device, the sub-threshold leakage current was 0.76 μA right after radiation exposure. It was 0.29 μA after 48 hours and 0.13 μA after 168 hours of room temperature annealing. Finally, it is fully healed and returned to its initial condition after 336 hours of annealing as in Figure 3.3. The sub-threshold leakage current change time dependence for different transistors was investigated, and the results are presented in Table 3.1. Because the transistors returned to their initial conditions after 100 °C annealing, these results are not shown in the table.

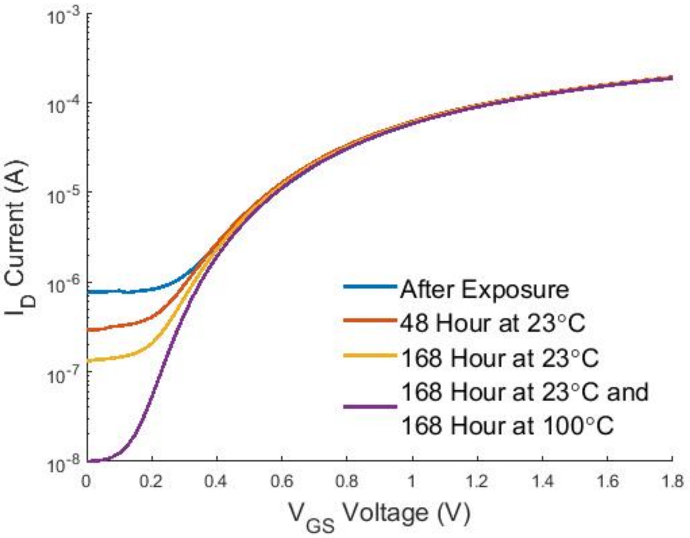


Figure 3.3 : Time dependent healing for the transistor with $W/L = 0.24\ \mu m/0.18\ \mu m$ at 300 krad TID. In addition to the measurements right after exposure, post-annealing results after 48 and 168 hours, at room temperature and 100 °C are shown.

Radiation-induced effects and size dependence have been previously investigated for 180 nm CMOS technology [13]. The drain currents of 0 V gate bias are dependent upon the W/L ratios of the transistors and can be modeled with the drain current equation. Here, we combined it with the dependence of radiation-induced effects on the device finger number. In Figure 3.4, even though T5 and T6 were the same size, leakage currents at $V_{GS} = 0V$ are different, and T2 has larger leakage current than T5 because it has more fingers.

Table 3.1 : Sub-threshold leakage change percentages according to without irradiation conditions at $V_{DS} = 1.8\ V$ and $V_{BS} = 0\ V$. All results are for 300 krad dose.

Transistor Dimensions (W/L)	After irradiation	48 hour 23 °C annealing	168 hour 23 °C annealing
0.24 μm/0.18 μm	3.7146×10^3	1.3499×10^3	5.5646×10^2
10 μm/0.18 μm	1.9857×10^4	1.0941×10^4	6.1949×10^3
10 μm/10 μm	7.4503×10^3	4.4026×10^3	2.4474×10^3
35 μm/0.5 μm	8.7003×10^4	5.5925×10^4	3.2271×10^4

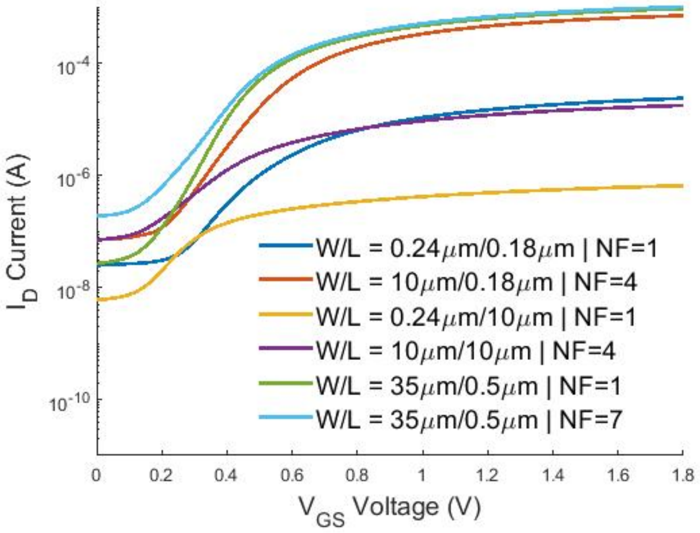


Figure 3.4 : I_D-V_{GS} measurements at 641 krad.

The dependence of radiation effects on device dimensions and biasing conditions during irradiation were also investigated through T1 and T4. W/L ratios for these two transistors were 1.33 and 1, respectively. Nevertheless, T4 had four fingers and T1 had one finger. Therefore, the leakage current of T1 for 0 V gate bias is smaller than that of T4 as in Figure 3.5. Moreover, for the 341 krad and 655 krad doses, the sub-threshold leakage currents were smaller than those of the previous radiation dose levels because the transistors that had these doses were irradiated while V_{DS} and V_{GS} were both at 1.8 V, and this caused them to be affected less under irradiation.

Reverse body-bias effects on leakage currents have already been applied to radiation tests [37, 38]. In addition to confirming previous research outcomes, as a further contribution, we investigated the reverse body-bias effect in conjunction with radiation dose effects and transistor dimensions.

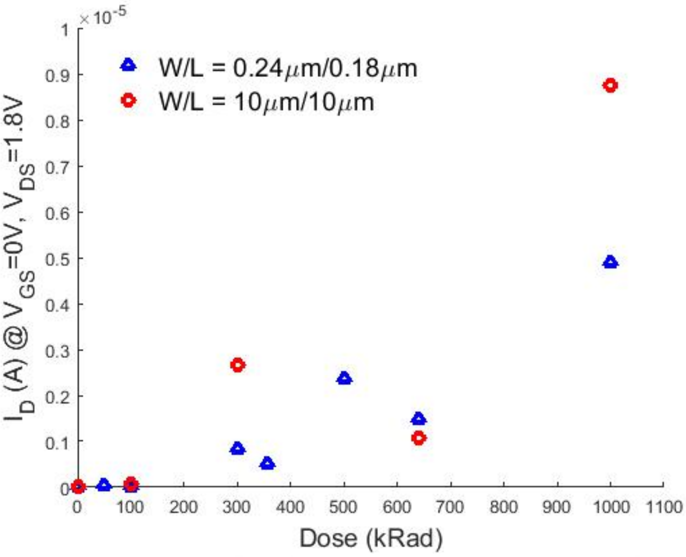


Figure 3.5 : Sub-threshold leakage current depends on the radiation dose and bias condition during irradiation.

The difference between two conditions that were body-biased to 0 V and -0.3 V were tested with different radiation doses for a regular transistor. First, initial measurements before radiation showed that the leakage current difference between the two body-bias voltages in the sub-threshold region was in the *nA* range. Second, after exposure tests, more significant differences were observed. For all radiation doses, the sub-threshold current was the largest for $V_{BS} = 0$ V. Change percentage according to the no body-biased condition of sub-threshold currents for 0 V and -0.3 V V_{BS} voltages are listed in Table 3.2 for various transistors and radiation doses.

In Table 3.2, V_{BS} effects changed with total dose and transistor dimensions. With increasing doses from 300 krad to 1 Mrad, difference percentage decreases, but still, it is observable. Moreover, the biggest change is observed for the smallest device.

Table 3.2 : Change percentage of sub-threshold leakage currents at $V_{BS} = -0.3\ V$ according to $V_{BS} = 0\ V$ measurements.

Transistor Dimensions (W/L)	300 krad	500 krad	1 Mrad
0.24 $\mu m/0.18\ \mu m$	458.20	222.55	199.57
10 $\mu m/0.18\ \mu m$	144.76	117.26	51.33
35 $\mu m/0.5\ \mu m$	133.34	86.13	67.86

3.2 Modeling of Radiation Effects

After irradiation, changes in transistor characteristics were analyzed and grouped into four main categories: sub-threshold leakage current increase, V_{TH} shift, saturation current shift, and linear region current differences. Our approach is to come up with a modified device model (in this context BSIM3v3) that can capture TID degradation effects. This is practical from the viewpoint of a circuit designer as it does not require additional simulation steps or tools. In fact, the modified BSIM card can be perceived as further process corner, which corresponds to the transistor characteristics after a certain TID radiation degradation. All of the parameters that are employed in the proposed modeling methodology are listed in Table 3.3 and the flowchart of the model development is shown in Figure 3.6.

The used simulation structure is shown in Figure 3.7. As mentioned before, a current source was placed between drain and source, and it was called idc. Four voltage sources were used to control four terminals of transistor independently. They were called according to their connected terminal as vd, vg, vb and vs for drain, gate, body, and source, respectively. The same schematic was used for different sizes so that sizes were attributed to parameters called width and length. All these parameters were controlled with created ocean script files. Also, ocean script files and transistor model files were controlled with Matlab. Simulation results were saved to a file, and they were read with Matlab.

Table 3.3 : Description of the model parameters

Parameter Name	Modeled Effect
UA	First-order mobility degradation coefficient
VTH0	Threshold voltage $@V_{BS} = 0$ for Large L
VSAT	Saturation velocity at Temp = Tnom
A2	Second non-saturation factor
DELTA	Effective Vds parameter
K1	First order body effect coefficient
KETA	Body-bias coefficient of bulk charge effect
PVAG	Gate dependence of Early voltage
DWG	Coefficient of Weff's gate dependence
WINT	Width offset fitting parameter from I-V without bias
K3	Narrow width coefficient

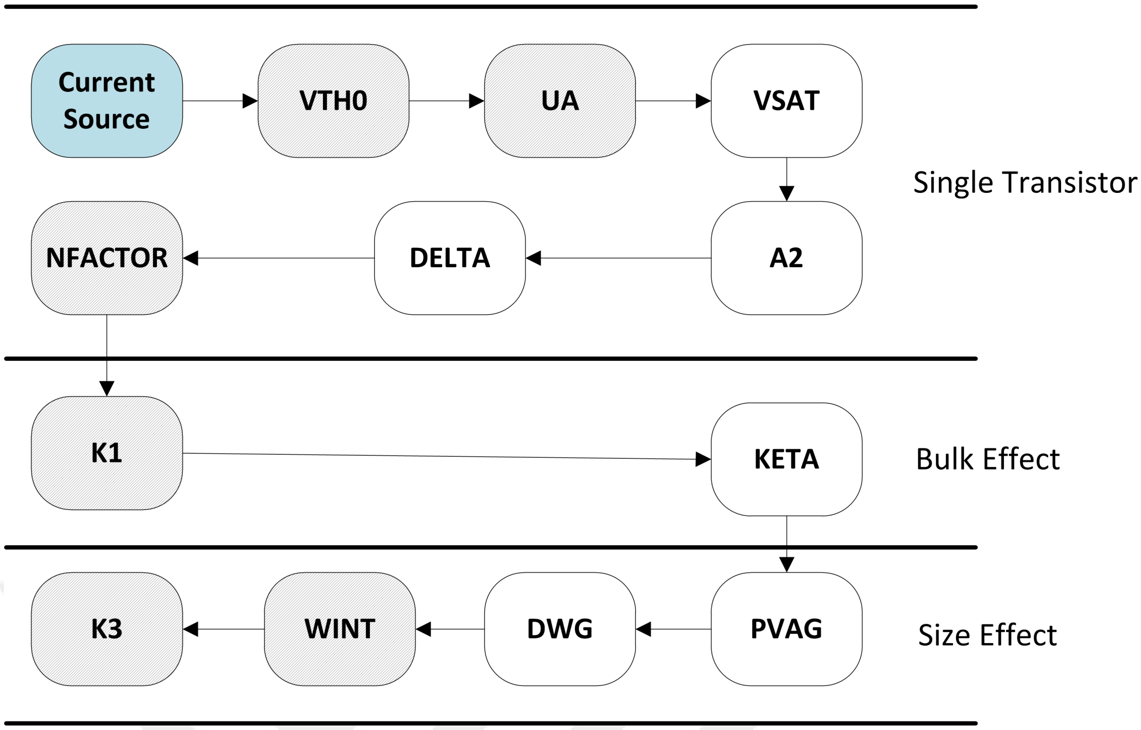


Figure 3.6 : Flowchart of modeling approach. Blocks with stripes use I_D-V_{GS}, solid blocks use I_D-V_{DS} curves. Only blue block modifies current source value instead of a model parameter.

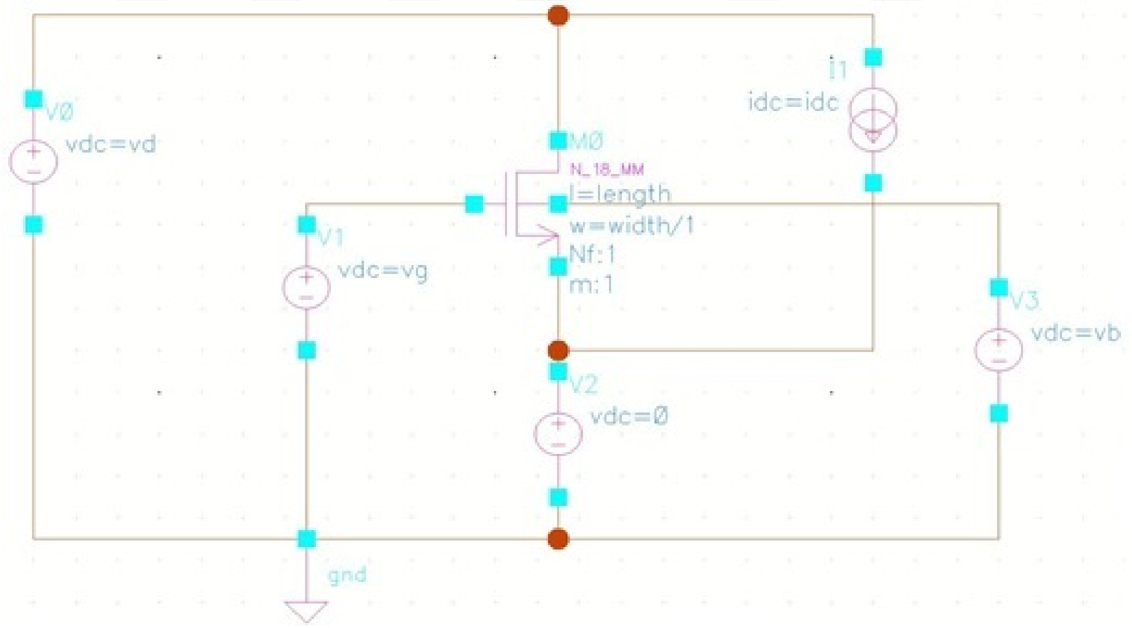


Figure 3.7 : Schematic of circuit which is used for modeling.

3.2.1 Sub-threshold current

An external current source in the direction of I_D, which is connected to the drain and source of the transistor has been used to model the sub-threshold current increase because BSIM3v3 lacks a parameter to adequately model the current component at around $V_{GS} = 0$ V. The investigation of MOSFET characteristics before and after irradiation revealed that the value of this current depends on several parameters. It changes with the dimensions of the device, absorbed dose, drain voltage, and body-bias. So, the I_D-V_{DS} measurement, which was extracted at $V_{GS} = 0$ V, was used to calculate the value of the current source. For each dose and transistor type, I_D-V_{DS} measurement outcome corresponding to the present V_{DS} was set to this current source, and other modeling steps are done using this value.

3.2.2 Linear region

The linear region behavior of devices without body-bias was modeled using I_D-V_{GS} curves, which were extracted at 50 mV drain bias. There were differences between the simulation results based on standard BSIM model and experimental result, especially at large V_{GS} voltages. This effect can be correctly taken into account by modifying the mobility parameters of transistors. Saturation region differences can be mitigated subsequently without affecting this region. So, parameter "UA" has been used to model the mobility changes at $V_{BS} = 0\ V$.

A common impact of irradiation on MOSFETs is the change in the V_{TH}. This change has been observed in our measurements at amounts varying with TID. In order to correctly model the new V_{TH}, the BSIM parameter "VTH0" is used. This parameter can directly modify V_{TH} without a dependence on any other voltage or process variable. Also, it enables modeling the change in V_{TH} caused by only TID degradation, without including channel and layout effects.

The procedure to find the new value of "VTH0" starts by choosing a current data point in I_D-V_{GS} measurements after TID radiation at $V_{DS} = 50\ mV$ and $V_{BS} = 0\ V$. The same data point is picked in the simulation graph of I_D-V_{GS} of that particular transistor. Here, it is important to identify that depending on the pre-radiation I_D-V_{GS} measurements; the transistor can be closer to one of the process corners. Consequently, the closest process corner model will be used in the simulations. This makes the proposed modeling approach more process-variation-aware. Flow chart of "VTH0" extraction flow is described in Figure 3.8.

In both the simulation and post-radiation measurement I_D-V_{GS} graphs, the slope drawn at the selected data point is extended to intersect the V_{GS} axis. The difference between the crossing values in each graph will yield the change in "VTH0" value.

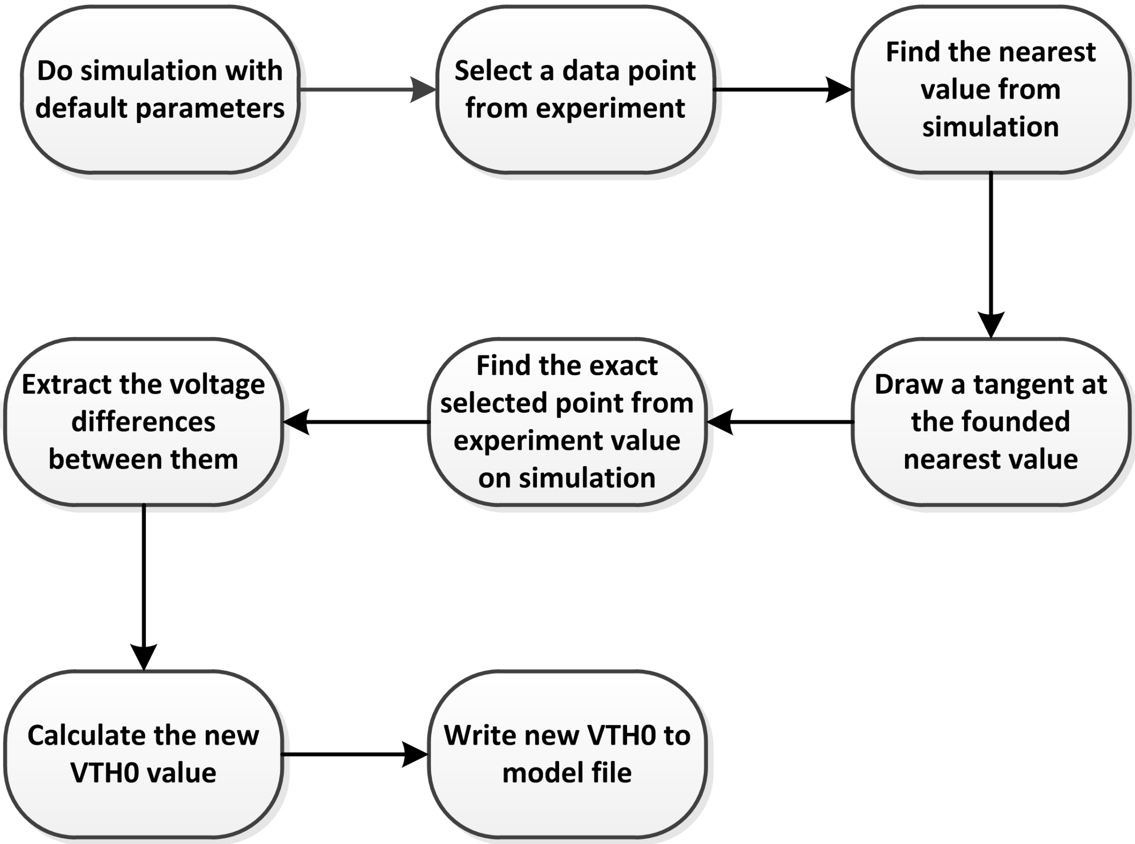


Figure 3.8 : VTH0 extraction flow.

3.2.3 Saturation region

Subsequent to irradiation, characteristics of the saturation region alter, as well. In order to capture these effects, I_D-V_{DS} curve for any dose extracted at $V_{GS} = 1.8$ V is utilized. Parameters that modify the saturation region, "VSAT" and "A2", are varied iteratively based on BSIM equations until the difference observed between the measurement and the simulation outcomes based on the modified model is minimized as much as possible [39]. Flow chart of iteration steps are shown in Figure 3.9.

While changing the saturation region characteristics, the smoothness of the transition from linear to saturation region may be impaired. To mitigate the discrepancy,

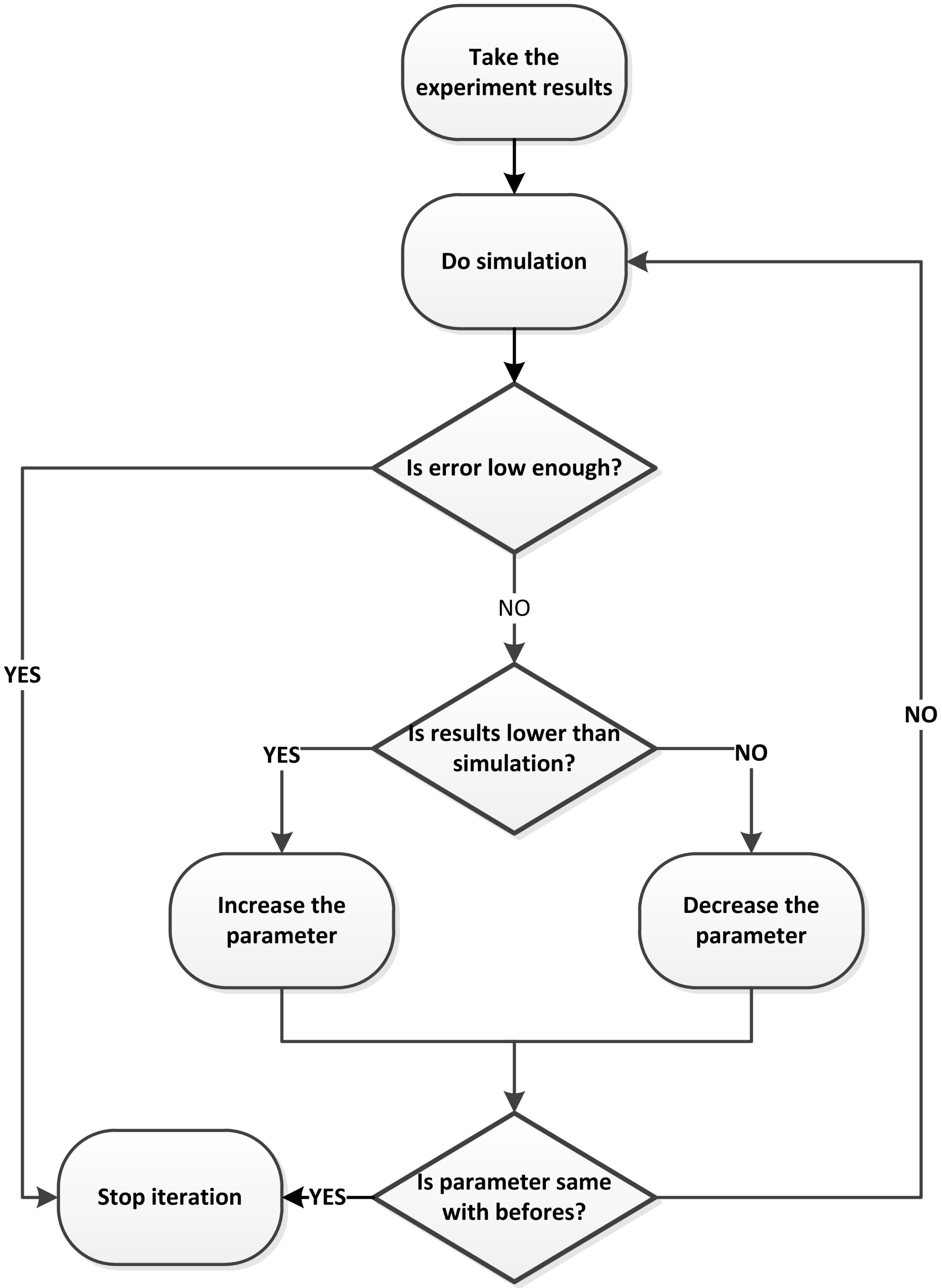


Figure 3.9 : Iteration flow.

the parameter "DELTA" is altered so that the measurement characteristics can be accurately obtained.

3.2.4 Body-bias effect

The “K1” parameter, which models the threshold voltage depend on the body-bias, was used to model the body-bias induced threshold voltage shift after irradiation. A method similar to that used when calculating the “VTH0” parameter was used. Two asymptotes were drawn and the difference between two threshold values, the new “K1” parameter was calculated using the appropriate part of the V_{TH} equation in [39].

Next, the “KETA” parameter was used for the saturation current changes caused by the body-bias. Simulation results were fitted to the measurements using an iterative method.

Up to this point, extracted parameters are suitable for only one transistor. These parameter can be used for single transistor sized circuits and can be extracted for any transistor at specified dose and bias conditions.

3.2.5 Device dimension effects

Size awareness was done using size dependence parameters. A $W/L = 10\mu m/0.18\mu m$ sized device was used to model only short channel effects without narrow width effects. By changing “PVAG”, the length dependence was modeled.

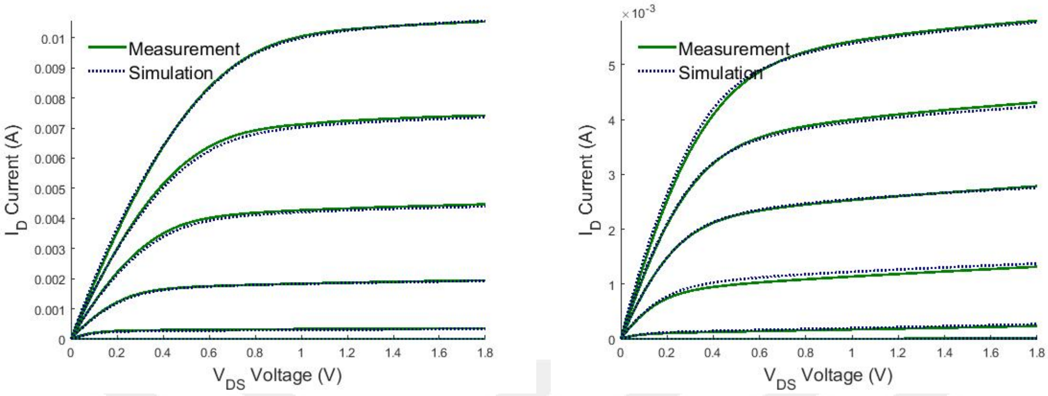
A $W/L = 0.24\mu m/0.18\mu m$ sized device was used to model especially narrow width effects, which have an important effect after irradiation. The “DWG”, “WINT” and “K3” parameters were used for this purpose.

In analog circuits of 180 nm CMOS technology, most of the time the length of the transistors does not exceed 0.54 μm, which is three times larger than the minimum size for the technology. The proposed model can work at these dimensions. The comparison between the model and measurement results is shown in next section.

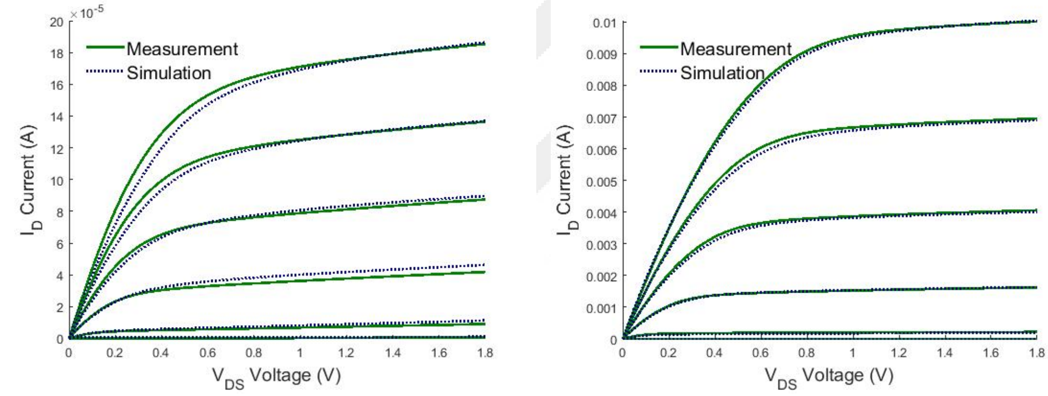
3.3 Modeling Results

Using one model for all three transistors, the simulation and measurement results were compared, and the results are shown in Figure 3.10 and Figure 3.11. $I_D - V_{DS}$ graphs with 0.3 V V_{GS} steps from 0 V to 1.8 V are shown for three transistors with two different V_{BS} biases, 0 V and -300 mV. $I_D - V_{GS}$ graphs are shown again for 50 mV and 1.8 V V_{DS} voltages and for 0 V and -300 mV V_{BS} voltages.

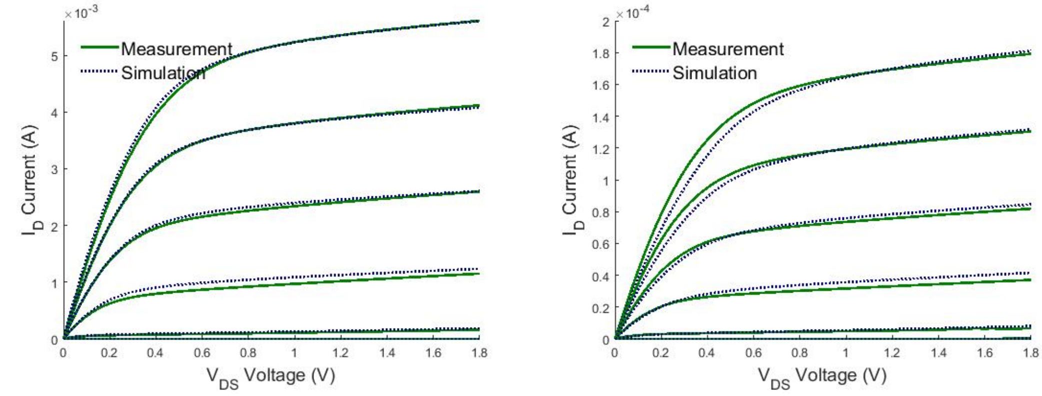
In these graphs, measurement results are not seen at some points, especially for lower drain voltages, because the drain currents may be negative due to noise and cannot be seen in the semi-logarithmic scale.



(a) $W = 35\ \mu$m, $L = 0.5\ \mu$m, $V_{BS} = 0\ V$ (b) $W = 10\ \mu$m, $L = 0.18\ \mu$m, $V_{BS} = 0\ V$



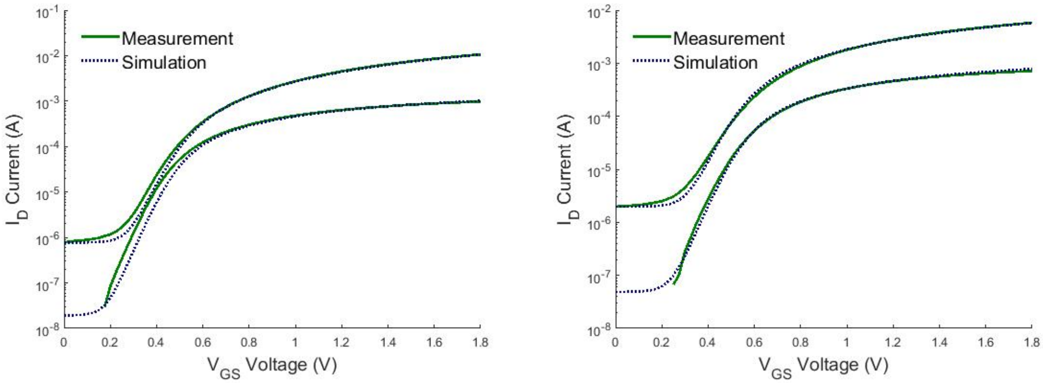
(c) $W = 0.24\ \mu$m, $L = 0.18\ \mu$m, $V_{BS} = 0\ V$ (d) $W = 35\ \mu$m, $L = 0.5\ \mu$m, $V_{BS} = -0.3\ V$



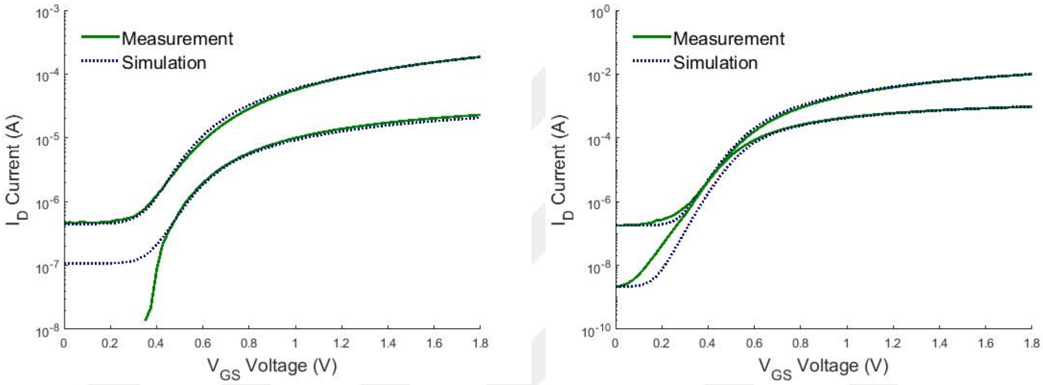
(e) $W = 10\ \mu$m, $L = 0.18\ \mu$m, $V_{BS} = -0.3\ V$ (f) $W = 0.24\ \mu$m, $L = 0.18\ \mu$m, $V_{BS} = -0.3\ V$

Figure 3.10 : Performance of the developed model over measurements with $I_D - V_{DS}$ graphs.

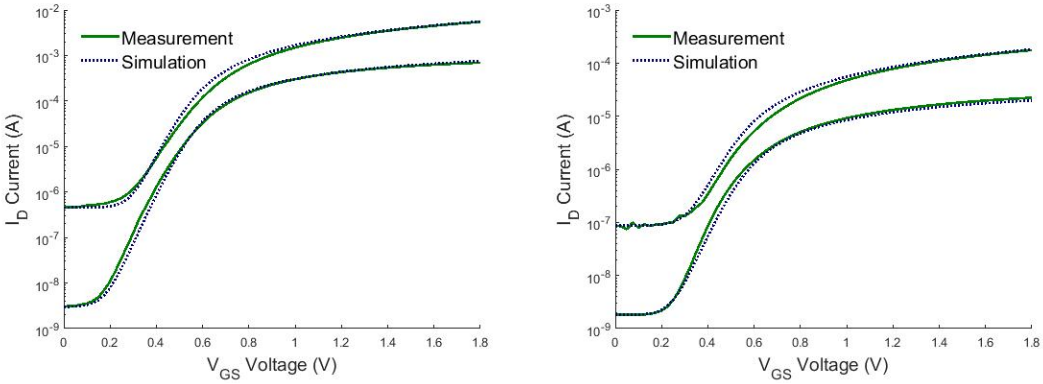
Mean errors for $I_D - V_{DS}$ curves bigger than 0.3 V gate voltage for all three transistors were extracted from the model and are shown in Table 3.4.



(a) $W = 35$ μm, $L = 0.5$ μm, $V_{BS} = 0\ V$ (b) $W = 10$ μm, $L = 0.18$ μm, $V_{BS} = 0\ V$



(c) $W = 0.24$ μm, $L = 0.18$ μm, $V_{BS} = 0\ V$ (d) $W = 35$ μm, $L = 0.5$ μm, $V_{BS} = -0.3V$



(e) $W = 10$ μm, $L = 0.18$ μm, $V_{BS} = -0.3V$ (f) $W = 0.24$ μm, $L = 0.18$ μm, $V_{BS} = -0.3V$

Figure 3.11 : Performance of the developed model over measurements with $I_D - V_{GS}$ graphs. I_D measurement values above the noise level shown only.

Table 3.4 : Error rates of transistors for single model.

Transistor Dimensions	V_{BS}= 0 V	V_{BS}= -0.3 V
W/L = 0.24 μm/0.18 μm	7.7998	7.7144
W/L = 10 μm/0.18 μm	4.4110	5.1101
W/L = 35 μm/0.5 μm	1.8349	1.8675

Main function of the code is attached to Appendix.

3.4 Model Application to Circuit

A model for one size and dose was applied to a sample circuit. For this purpose, a ring oscillator with 5 inverters was designed and simulated with default parameters and extracted parameters. Minimal transistor dimensions were selected, 0.24 μm width and 0.18 μm length, for both PMOS and NMOS. For PMOS devices, the standard model was used because PMOS devices are more radiation hardened than NMOS devices. So, only NMOS devices were modeled with our model. The difference between our model and the standard model was investigated for 1 Mrad.

Schematic of the designed first ring oscillator is shown in Figure 3.12. As can be seen and mentioned earlier, five inverter stages were used. In all stages, to model the leakage current, a current source was placed between drain and source of NMOS.

At this dose level, sub-threshold leakage current, threshold voltage and saturation currents change. So that, characteristics of a ring oscillator change. As expected, its power consumption increases 9.42% because of both leakage current increase at 0 V V_{GS} voltage and in the saturation region. Also its frequency changes 30 MHz again because of the different transistor characteristics. Power consumption and output frequencies are shown in Table 3.5 for both standard model and model extracted for 1 Mrad.

Table 3.5 : Simulation results of ring oscillator with standard model and our proposed model.

Used Model	Power Consumption	Frequency
Standard Model	1.0957×10^{-4} W	2.790 GHz
1 Mrad Model	1.1989×10^{-4} W	2.820 GHz

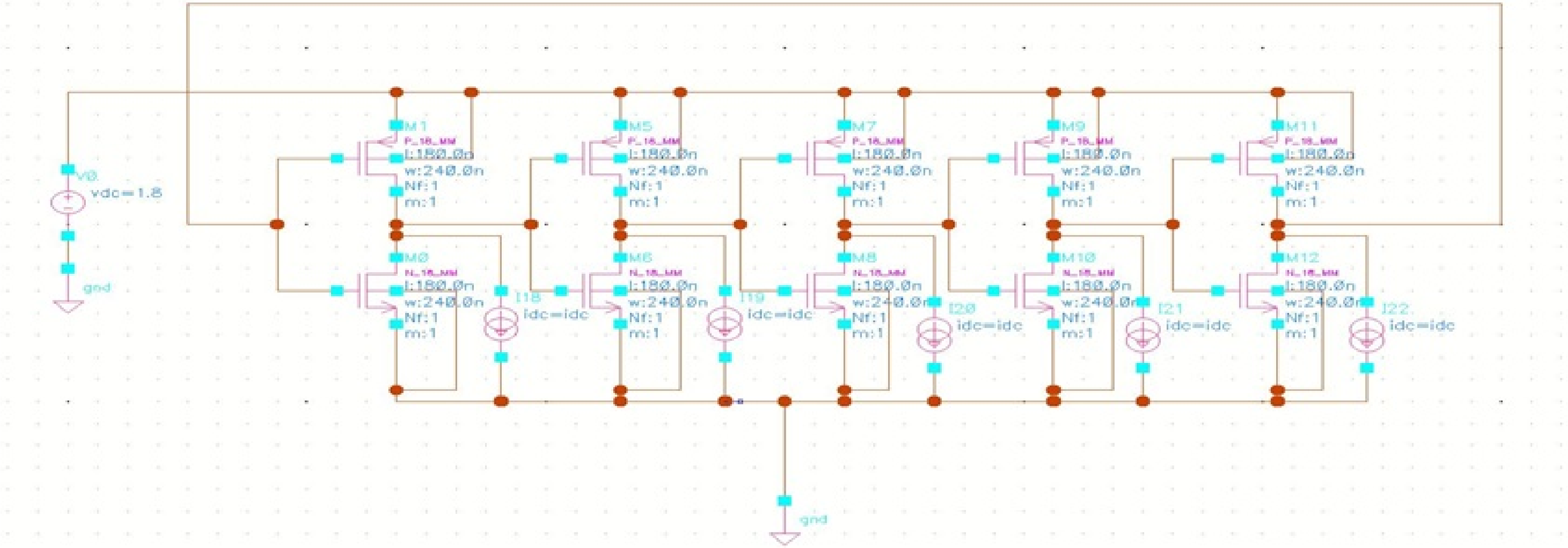


Figure 3.12 : Schematic of designed ring oscillator with PMOS.

Another application of model is done with another topology of ring oscillator. Circuit is shown in Figure 3.13. These ring oscillators are designed as a chain of 5 resistively-loaded NMOS amplifiers, where the load resistance for each stage is 10 $k\Omega$. Two different types of transistors, T2 and T6, have been separately employed as amplifying devices in each circuit, and two distinct models extracted for the TID amounts 355 krad and 1 Mrad have been utilized to evaluate the TID impact on both oscillators. Both the oscillation frequency and the total power consumption have been recorded for all designs. Results for all case-studies are provided in Table 3.6.

Table 3.6 : Comparison of ring oscillator performance with the standard and proposed model

Used Model	Transistor Type	Power Consumption	Frequency
Standard Model	T2	1.1364 mW	1116 MHz
355 krad Model	T2	1.145 mW	1136 MHz
1 Mrad Model	T2	1.1588 mW	956 MHz
Standard Model	T6	1.163 mW	235 MHz
355 krad Model	T6	1.170 mW	239 MHz
1 Mrad Model	T6	1.204 mW	201 MHz

Given that the sub-threshold leakage current rises after radiation exposure, the power consumption of the ring oscillator increased by as much as 3.5% after TID degradation. In terms of frequency, at a lower TID (355 krad), both ring oscillators built with T2 and T6 retained their oscillation frequency with a subtle increase below 2%. As the TID increases to 1 Mrad, however, for both oscillators, the oscillation frequency decreased by as much as 14%. This observation provided by the model-based simulation is very much in line with the experimental results of a ring oscillator designed with 65 nm CMOS technology [40]. As the leakage currents increase, the apparent gate impedance comes down leading to a larger gate capacitance. Thus, the delay per stage increases and the frequency of oscillation drops.

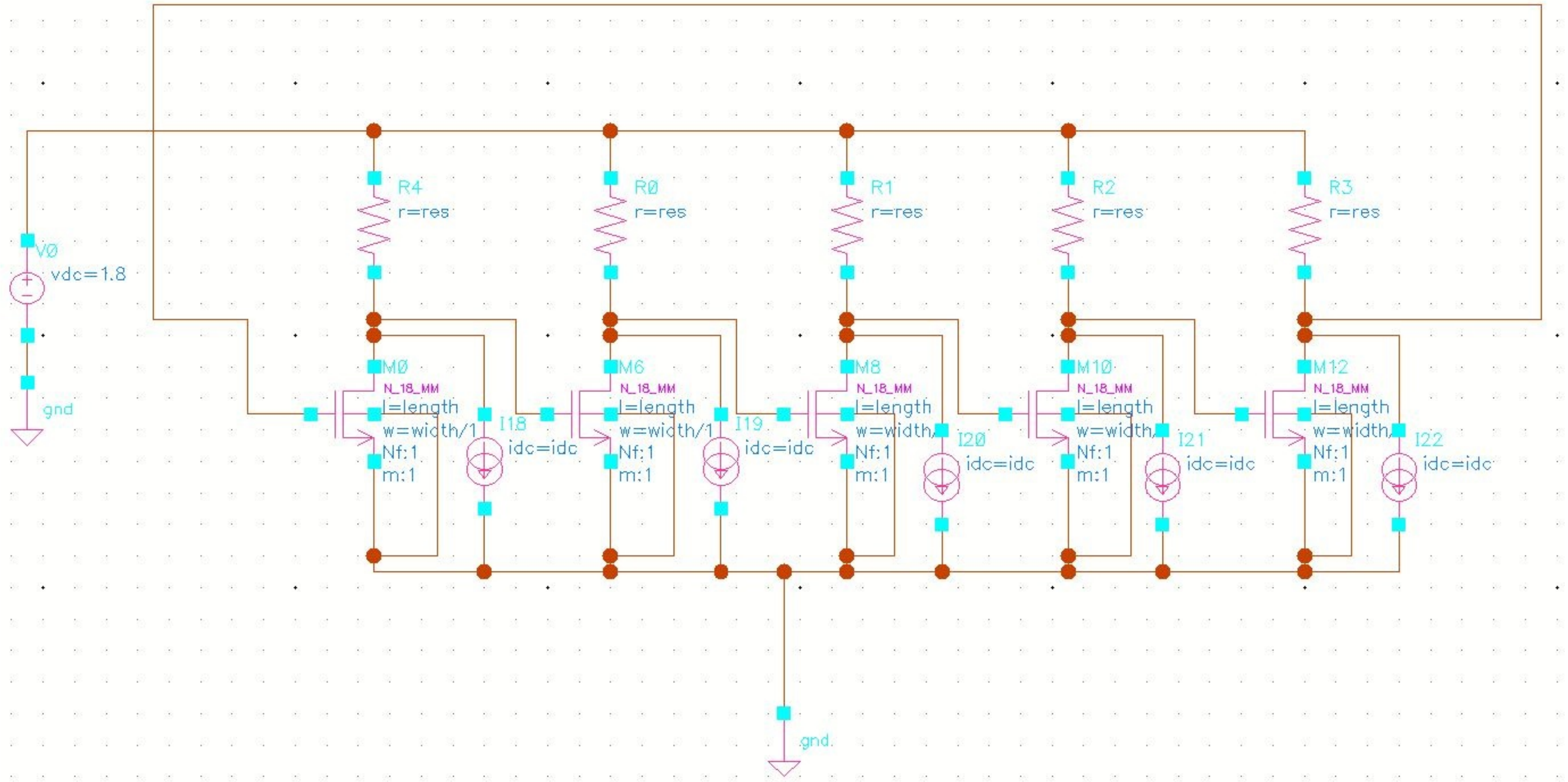


Figure 3.13 : Schematic of designed ring oscillator with resistor.

4. EFFECTS OF BIASING DURING IRRADIATION ON MOSFET SYMMETRY

In this section, the effects of biasing condition during irradiation while drain and gate were biased to 1.8 V and body and source were connected to 0 V is investigated. It is shown that this configuration changes transistor symmetry, and this asymmetry lets to use a possible improvement for proper circuits. All measurement results referenced in this section is biased with the condition mentioned above.

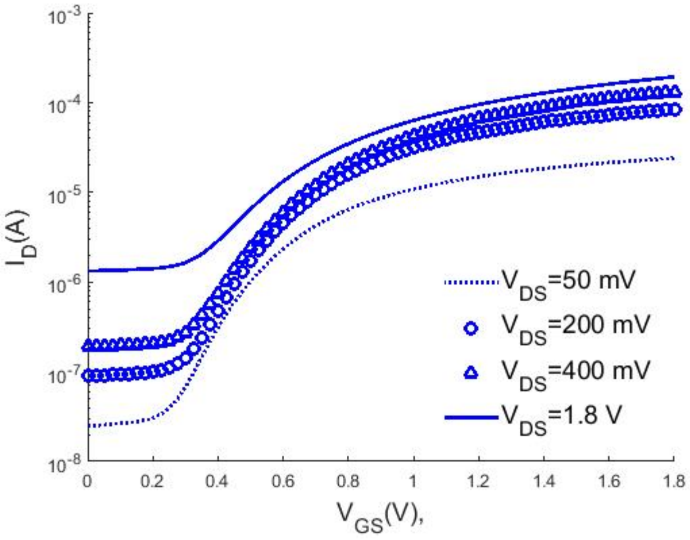
4.1 Experimental Results

Using I_D-V_{GS} graphs which y-axis is plotted on a logarithmic scale and the x-axis on a linear scale, sub-threshold currents of transistors were investigated. Moreover, "straight" and "reverse" words refer to measurements which drain and source terminals used as original and when drain and source terminals were exchanged, respectively.

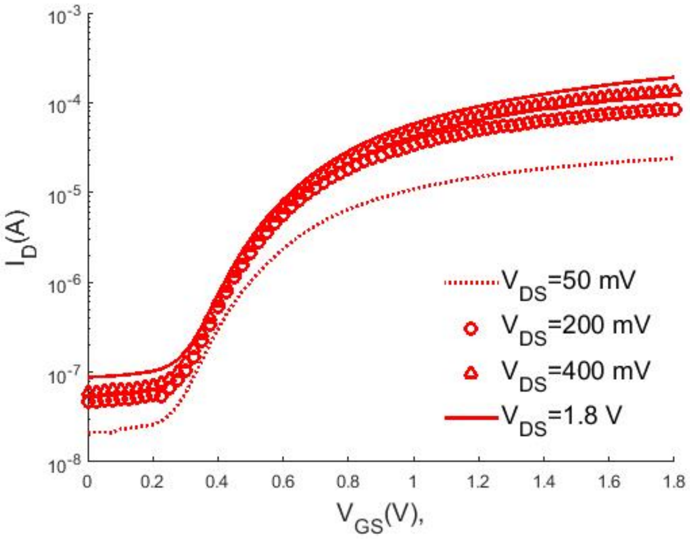
According to experimental results, it is clear that leakage current in straight measurement was much higher than reverse configuration. Also, this difference between two measurements is increased with increasing drain voltage and as the expected maximum value was at 1.8 V (Figure 4.1).

Difference between different straight and reverse measurements changed for different sized transistors. Furthermore, maximum differences were reported as the ratio of them. With smaller sizes, ratio tended to increase, and the biggest ratio was observed for the smallest transistor called T1. For this transistor, the ratio between straight and reverse measurements was 15.3 which means straight leakage current was 15.3 higher than reverse leakage current. As mentioned, the smallest ratio was observed in the biggest transistor called T4, and it was 0.4. Also, for T2 and T3, ratios are 14.4 and 13.6, respectively. All measurement results are shown in Figure 4.2.

Moreover, the slope of I_D - V_{GS} curves are different for reverse and straight measurements and it is larger in reverse measurements. This phenomenon originates from trapped charges in the oxide, as other radiation-induced effects. Also, an



(a)



(b)

Figure 4.1 : I_D - V_{GS} graphs for 50 mV, 200 mV, 400 mV and 1.8 V V_{DS} values for a) Straight and b) Reverse configurations of T1.

interesting behaviour is observed in T3 and T4 curves. The currents in reverse configuration is bigger than the values in the straight configuration for a given V_{GS} range.

Due to the radiation-induced effects which are occurred with a mechanism declared before, in Chapter 1, sub-threshold slopes of transistors become degraded. Because of the trapped charges, leakage currents with the hopping mechanism became important especially in long channel devices. The reason behind these effects attributed to this hopping mechanism because two transistors which show this behavior both have

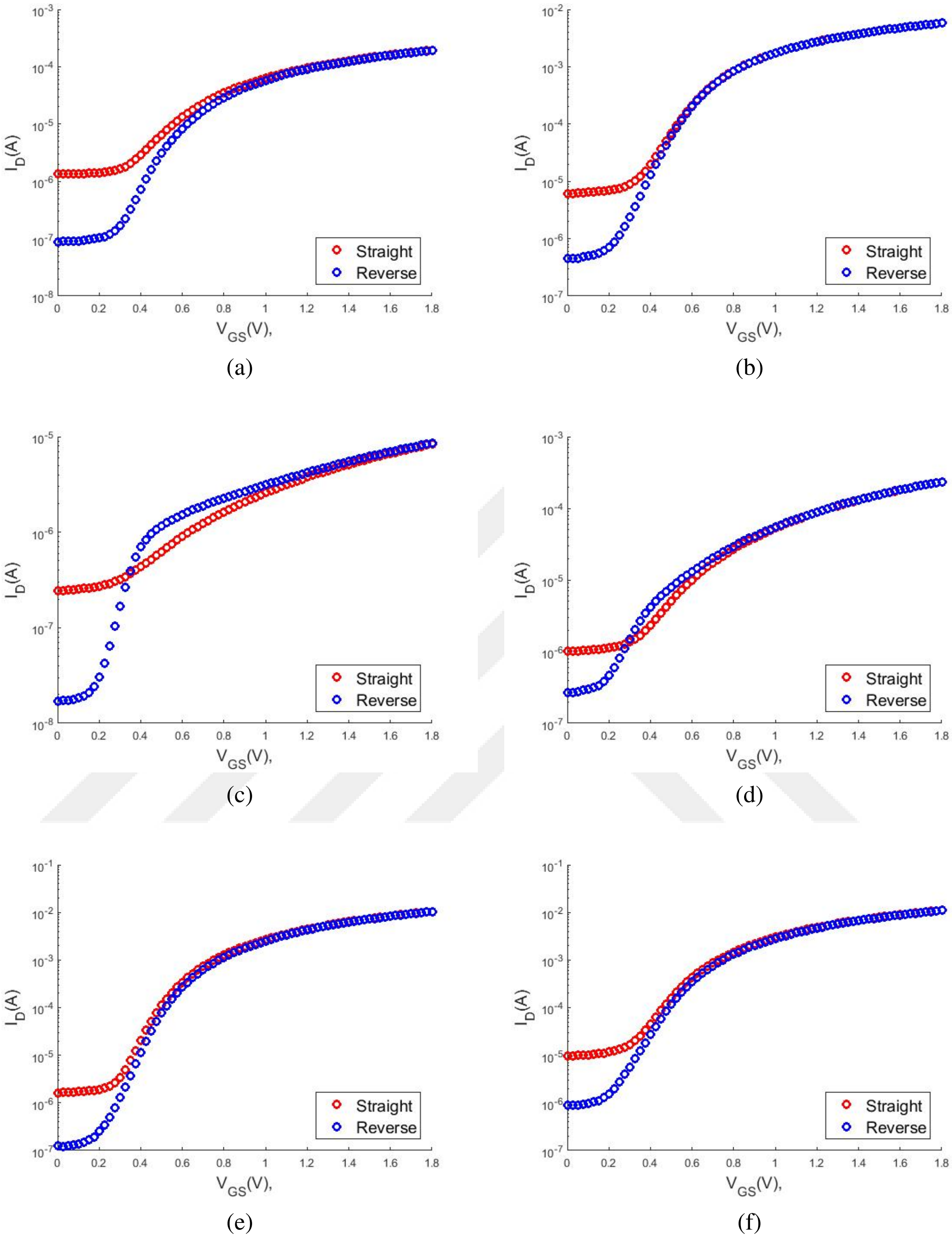


Figure 4.2 : I_D - V_{GS} graphs while $V_{DS} = 1.8$ V for the straight and reverse configurations of a) T1, b) T2, c) T3, d) T4 e) T5 f) T6.

10 μm channels. As a result, for the gate voltage range of 0.4 V to 1 V, straight configuration current stay under reverse configuration current for T3 and T4.

The T5 and T6 share the same dimensions with only one difference. While T6 has 7 fingers, T5 has one finger. It is a known consequence of finger number, with increasing finger number, radiation tolerance of transistor decreases. So, more number of fingers lead to larger leakage current [41]. This phenomenon is confirmed by our results too. Consequently, T6 has a larger leakage current than T5, and they share similar leakage current ratios 12.9 for T5 and 10.8 for T6.

Also, reverse body bias effects are investigated. For the reverse and straight configurations, similar results were observed. For both configuration, sub-threshold current decreased and threshold voltage increased, as expected.

As demonstrated in Figure 4.3 for T1, sub-threshold leakage currents increased with increasing radiation level for all transistors. With the aim of simple design, only measurements results of T1 is demonstrated instead of all transistor measurements.

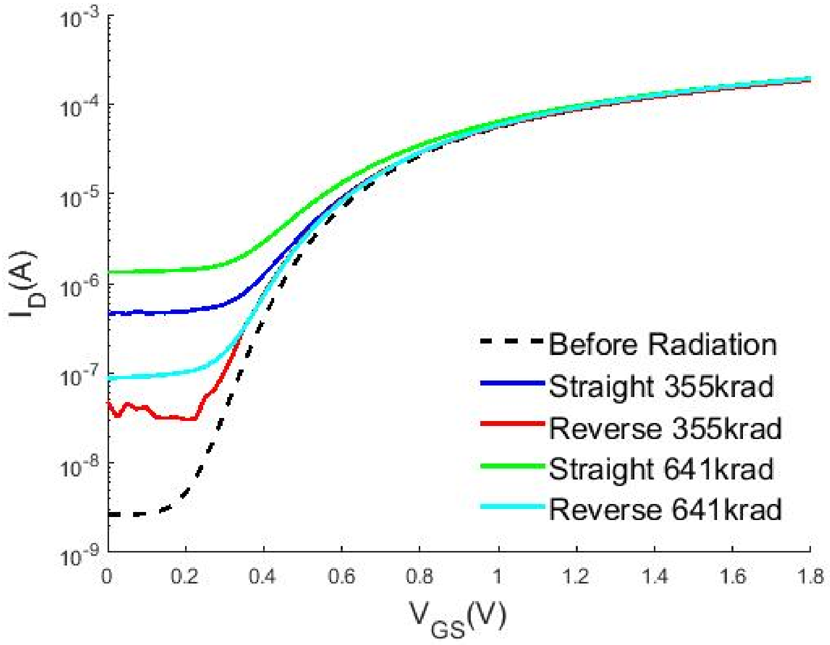
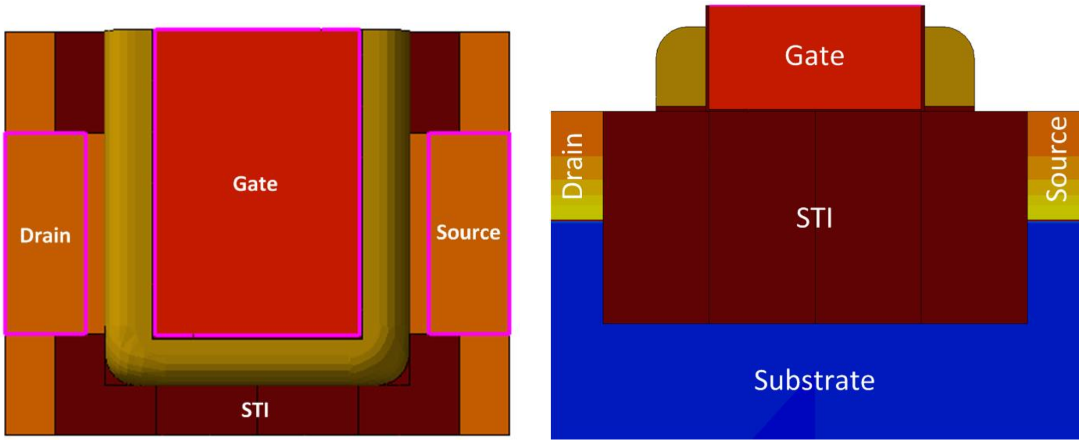


Figure 4.3 : TID effects on the sub-threshold leakage current of T1 for the reverse and straight configurations. V_{DS}= 1.8 V for all measurements.

4.2 Discussion and Explanation

Asymmetric charge trapping in the insulator regions is suggested as an explanation for this behavior. Worst case bias configuration is known as the gate terminal connected to 1.8 V while other three terminals connected to 0 V. In this configuration voltage difference between both drain and source becomes maximum, and electric field maximizes. Due to this is the worst bias configuration, maximum trap occupation occurs with the maximum electric field. Also, this phenomenon was reported before by other researches [3]. On the other hand, when both drain and gate terminals were connected to 1.8 V while source and body terminals were connected to 0 V, the voltage difference between gate to drain and source will be different. It is higher on the source side. So that, several traps in insulators near the source side will be much more when compared with the drain side insulators.

A Technology Computer Aided Design (TCAD) tool Sentaurus TCAD is used to test the proposed argument about asymmetric charge trapping effects. Using Sentaurus Device Editor, A 3D NMOS device is created, which shares the same sizes with T1 [42]. To control overall insulator regions effectively and easily, they were separated into four parts. So, traps were placed in insulator parts while uniform in each part and increases towards to source side. Minimum concentration was at drain side, and it was 10^{15} cm^{-3} and maximum at source side with 10^{18} cm^{-3} concentration. Number of traps chosen arbitrarily to simulate only charge concentration effects. After that, I_D-V_{GS} graphs were simulated for both straight and reverse configurations with same specs in the experiments. The designed device is shown in Figure 4.4. In Figure, brown regions represent the four separate oxide STI regions. Drain, source and gate contacts are shown in pink frames b) Cross sectional view. Length of the substrate is 500 nm, height of the STI regions and gate regions are 200 nm and 100 nm, respectively.



(a) (b)

Figure 4.4 : Simulated device used to estimate the different trap concentration effects on the drain and source sides. a) Front view b) Cross sectional view.

Electric fields in insulator regions of the device is visualized in Figure 4.5 when both drain and gate terminals at 1.8 V while the source and body terminals at 0 V like irradiation experiments. Drain is on the left side of the figure and source is on the right. As the color changes from blue to red, magnitude of the electric field increases. The vertical electric field points from gate to substrate, and the lateral electric field points from drain to source. It is confirmed that our hypothesis about electric field differences in insulator regions for such a biasing scheme.

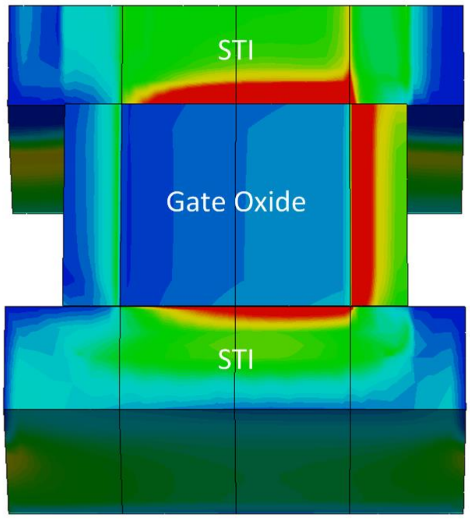


Figure 4.5 : Magnitude of electric fields in STI regions is reflected when the drain and the gate are biased with 1.8 V.

According to I_D-V_{GS} curves in Figure 4.6, compatible results can be seen with experimental results. Sub-threshold leakage current for reverse configuration is lower than straight configuration. Unlike experimental results, TCAD simulations do not show the low, flat values of leakage currents [43]. It can be said that, in the light of this information, hypothesis about charge trapping asymmetry is confirmed.

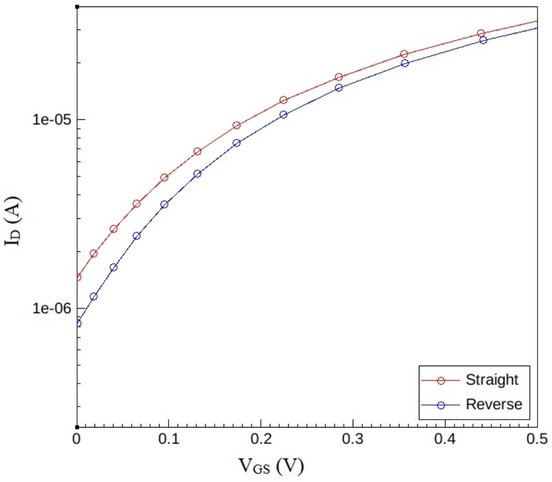


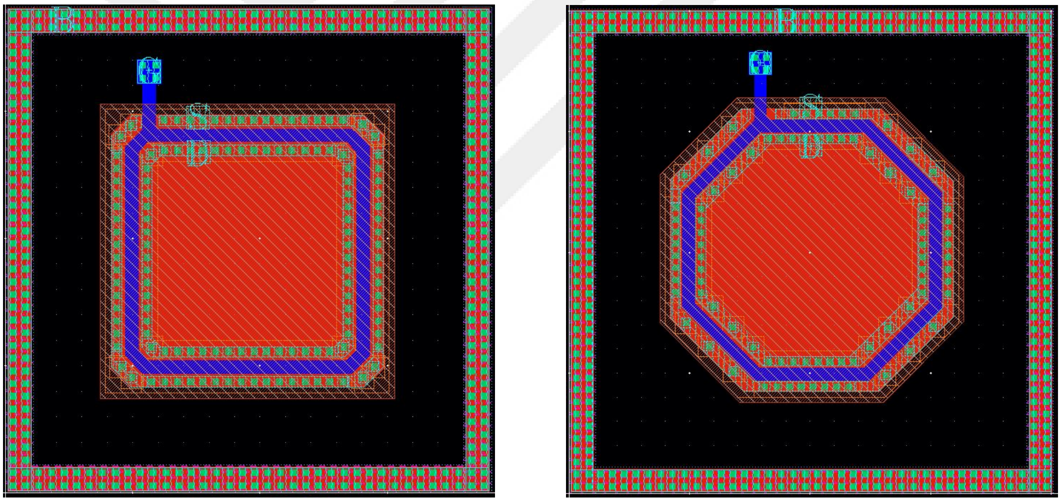
Figure 4.6 : TCAD Simulation results for reverse and straight measurements with asymmetric trap concentrations.

Consequently, TID effects increase sub-threshold leakage currents, thus they increase power consumption of a circuit. It is presented that, with the proposed and tested idea, power consumption can be decreased with changing ground and high potential. Proper circuits can be designed according to this source-drain symmetry, or this phenomena can be used proper structures like transmission gates.

5. COMPARISION OF DIFFERENT SHAPED ENCLOSED LAYOUT TRANSISTORS (ELT) AND REGULAR LAYOUT TRANSISTOR

5.1 Extra Information About Test Chip

In addition to test chip specifications specified before, it is proper to describe ELT layout structures. The layouts of the ELTs have been manually drawn, and their channel length has been chosen to be 500 nm. The channel width is set to 35 μm (see Figure 5.1). Moreover, for the regular layout transistor, the parametrized cell (pcell) layout is also employed with the same sizes as the ELTs.



(a)

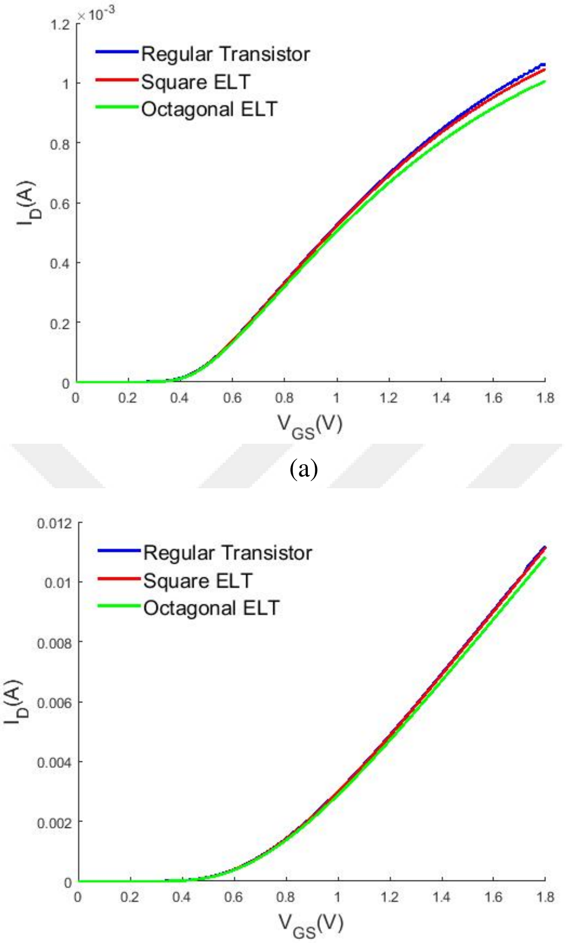
(b)

Figure 5.1 : Layout of the a) square ELT and b) octagonal ELT.

5.2 Experiment Results

5.2.1 Process variability tests

All I_D-V_{GS} measurement waveforms captured at $V_{DS} = 50$ mV have been collected together. Also, their statistical mean is found for the octagonal ELT, square ELT and regular layout transistor. All of the graphs are shown in Figure 5.2. They can be used to extract the threshold voltages of the transistors since these waveforms are taken at a low V_{DS} potential. As expected, no appreciable difference has been observed between the threshold voltages of the transistors because they physically refer to the same structure. Moreover, in general the characteristics of $V_{DS} = 1.8$ V, $V_{DS} = 50$ mV measurements match well for all three transistors.



(a)

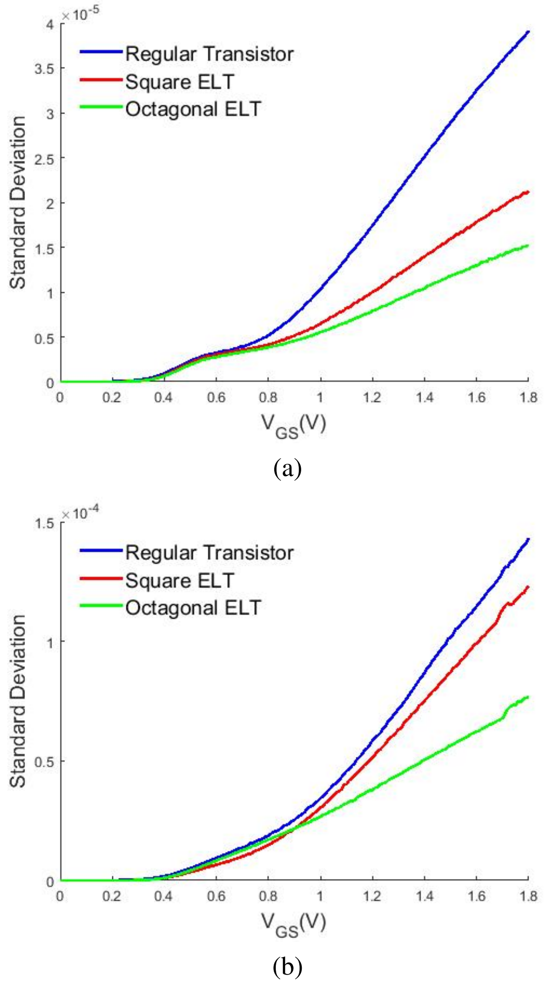
(b)

Figure 5.2 : Mean of I_D - V_{GS} graphs for a) $V_{DS} = 50\ mV$ and b) $V_{DS} = 1.8\ V$.

Peak values of the standard deviation for each measured graph are listed in Table 5.1. Furthermore, the ratio of the standard deviation of the waveforms to the mean waveform (σ/μ) is reported as a measure of spread in measured curves. Given that the mean of waveforms are pretty close to each other; this figure can be interpreted as a direct measure of process variability. According to that metric, it can be seen that the square ELT has the largest spread for all three measurement curves and its standard deviation is bigger than the one of the octagonal ELT by 47.8% Standard deviation for I_D-V_{GS} measurements are shown in Figure 5.3.

Table 5.1 : Peak values of the standard deviation (σ) and the standard deviation over the mean (μ) values for all measured curves.

Transistor	Measurement type	σ (A)	$\sigma/\mu(\times 10^{-2})$
Regular transistor	I_D-V_{DS}, $V_{GS} = 1.8\ V$	1.38×10^{-4}	1.23
	I_D-V_{GS}, $V_{DS} = 50\ mV$	3.94×10^{-5}	3.75
	I_D-V_{GS}, $V_{DS} = 1.8\ V$	1.40×10^{-4}	1.25
Square ELT	I_D-V_{DS}, $V_{GS} = 1.8\ V$	2.74×10^{-4}	2.48
	I_D-V_{GS}, $V_{DS} = 50\ mV$	6.63×10^{-5}	6.51
	I_D-V_{GS}, $V_{DS} = 1.8\ V$	1.55×10^{-4}	1.40
Octagonal ELT	I_D-V_{DS}, $V_{GS} = 1.8\ V$	1.43×10^{-4}	1.32
	I_D-V_{GS}, $V_{DS} = 50\ mV$	4.39×10^{-5}	4.40
	I_D-V_{GS}, $V_{DS} = 1.8\ V$	1.33×10^{-4}	1.22



(a)

(b)

Figure 5.3 : Standard deviation of regular transistor, square ELT and octagonal ELT for I_D - V_{GS} curves with a) $V_{DS} = 50\ mV$ and b) $V_{DS} = 1.8\ V$.

5.2.2 Radiation tolerance tests

Two types of ELTs are found to be radiation hard even for doses up to 1 Mrad. There has been no significant change between the measurements at the initial condition and after radiation exposure. As observed in Figure 5.4, drawn for 1 Mrad dose level, both the square ELT and the octagonal ELT preserve their initial characteristics. A single measurement is used here since all other measurements at different doses of both types of ELTs confirm the same conclusions. These results are also in line with the generic knowledge on ELTs that they can withstand radiation doses up to several Mrads [30].

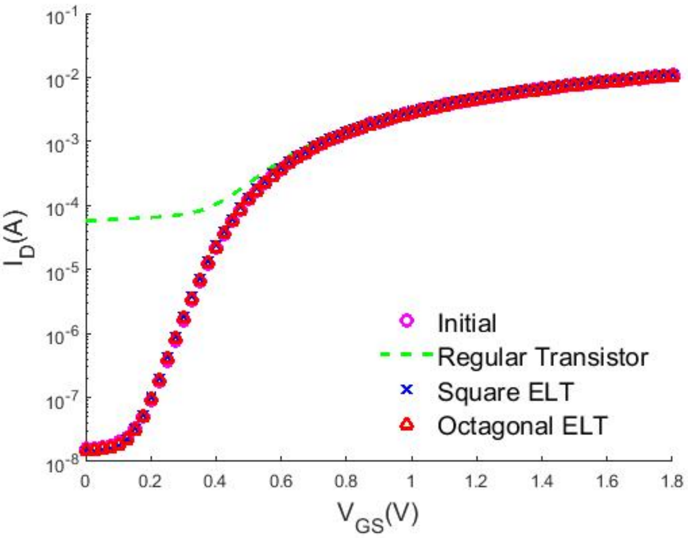


Figure 5.4 : Comparison of radiation exposure effects for the regular layout transistor, square ELT and the octagonal ELT. All measurements belong to the 1 Mrad dose except the initial condition graph.

5.3 Discussion and Suggestion

Process variability tests show that the octagonal ELT is more robust to process variations than the square ELT. This stems from the symmetry of the layout. While drawing the layouts for these ELTs, the user is only allowed to draw 45°. So, it is impossible to draw a perfect 90° at the corners of the square. This impairs the layout symmetry of the square ELT, which makes it more vulnerable to process variations. As a result, one should keep the layout symmetry as a priority in designing the ELTs. Even so, area overhead of the octagonal ELT is 2.78% larger than the square ELT. This suggests that there is a trade-off between the robustness to process variability and the area overhead.

Other measurements show that there is no appreciable difference between the square and octagonal ELTs in terms of their radiation tolerance up to the dose of 1 Mrad. Besides, their characteristics under body bias are very similar.

6. CONCLUSION

This thesis focuses on the characterization, optimization, and modeling of radiation-induced effects on metal-oxide-semiconductor-field-effect-transistors (MOSFETs) and it is composed of three main parts. In the first part, total ionization dose degradation on n-MOSFETs from a commercial 180 nm device technology library is investigated and modeled. During the tests, chips were irradiated using a Cobalt-60 gamma-ray source at three different dose rates up to 50 krad, 100 krad, 300 krad, 355 krad, 500 krad, 641 krad, and 1 Mrad doses. In addition, two different bias configurations were applied. The first configuration is called the worst case condition, where the gate terminal is connected to 1.8 V and the drain, source, and bulk terminals are at 0 V consequently. In the second configuration, in comparison to the first approach the gate and drain terminals are biased with 1.8 V; whereas, the source and body terminals are at 0 V. After the radiation exposure, first, irradiated transistors are annealed for 168 hours at 23°C, and then for another 168 hours at 100°C. In that regard, time-dependent healing effects have been characterized for different types of transistors.

A user-friendly modeling approach, which takes different channel geometries and various biasing conditions into account, has been developed. The approach leverages the experimental characterization of radiation-induced effects on six transistors with different channel lengths and widths. Subsequently, the current-voltage characteristics of these transistors have been analyzed after irradiation. In this vein, the amount of degradation due to irradiation is noted for different levels of TID, channel geometries (various sizes of channel length and width, as well as number of fingers) and terminal voltages (including body-biasing), for all devices under test. Moreover, time-dependence of these effects have been considered, as well.

Radiation-induced effects on the current-voltage characteristics of a transistor manifest themselves in four main symptoms. These four symptoms are as follows, the sub-threshold leakage current increase, the threshold voltage shift, linear and saturation current changes. These symptoms have been categorized based on the observations of device characteristics before and after the irradiation experiments.

A parameter modification methodology is used to model the radiation-induced effects. In that respect, only one external current source has been employed to model the high leakage current caused by irradiation, since there is no parameter in BSIM3 to model that kind of a high leakage current. The value of this current source has been evaluated by leveraging the I_D-V_{DS} measurement curve at $V_{GS} = 0$ V for each transistor. After this adjustment, the threshold voltage as well as the current–voltage relationship in the linear and saturation regimes are modeled separately. Also, body bias effects have been included to our proposed model, so that with this methodology, a TID degradation model for all kind of transistors at any bias condition has been developed.

To obtain a single model for transistors of various sizes, short channel and narrow width effects are included in our suggested single model. At the end, with this approach, a single model, which is validated for different dimensions up to three times of minimum channel length and all possible channel widths has been extracted. Subsequently, the developed model is compared with experimental results and corresponding error rates are calculated for three selected transistor types at two different body bias voltages. Overall, it is shown that the error rates are in all cases under 8

The extracted radiation model for two kinds of five-stage ring oscillator circuits is applied and results have been compared. In the first topology, our proposed model is applied to a ring oscillator, which is designed with an NMOS and a PMOS type inverter circuit topology. In this topology, minimum sized transistors are used.

For the second topology of the ring oscillator, another type of inverter that includes a resistor and an NMOS, has been simulated using two kinds of transistor models at two distinct dose levels. Furthermore, the power consumption and oscillation frequency values have been compared and it is observed that our obtained results are compatible with the results reported in the literature.

In the second part, bias effects during irradiation on NMOS symmetry is investigated. Firstly, the drain-source symmetry of NMOS devices is tested and as a result it has been observed that swapping drain and source terminals turns out to be beneficial in terms improving the radiation tolerance of the device under test. To verify, devices are irradiated while drain and gate terminals are tied to 1.8 V, whereas source and body terminals are biased at 0 V. It has been recognized that swapping drain and source terminals after irradiation has reduced the sub-threshold leakage current. The cause of this effect has been explained on the basis of different trap concentrations in insulator regions near the drain and the source.

Electric field in the insulators during irradiation are claimed as the reason of different charge trapping concentrations. This idea has been assessed using TCAD simulation. An NMOS device is designed, and electric fields on it are shown for the aforementioned case near the terminals. Due to the voltage difference between the gate and the source, the higher electric field is observed near to the source region of the gate oxide compared to the drain region. These higher electric fields lead to a higher trap concentration in the insulator close to the source region.

Finally, charge trap concentration effects have been considered. In the simulation, traps are populated in the insulator with a greater concentration on the source side in comparison to the drain side. After simulation of this device, similar results with our experiments are observed. With this phenomenon, a novel potential healing methodology for circuits is accomplished.

In the third part, the same sized square and octagonal shaped ELT structures have been compared according to radiation tolerance, process variations, and area consumption. Overall, it is noticed that, there is appreciable difference between their radiation tolerances, and both of them are radiation hard up to 1 Mrad dose.

I_D-V_{GS} measurements for both 50 mV and 1.8 V drain biases are used for our comparison. Moreover, process variations of two ELTs have been compared with two metrics. These two metrics are composed of the standard deviation and the standard deviation over the mean value. In both of them, the variation of octagonal ELT is much less than that of the square ELT that can be attributed to the small dimensions at the edges of the square ELT. The manufacturing process does not allow creating perfect 90° at the corners so that only 45° is allowed. This causes the devices to be more sensitive more to process variations. On the other hand, the area consumption of the octagonal ELT is larger than that of the square ELT. Consequently, it is suggested that the designers should choose the shape of ELTs according to their own priority about variation tolerance and area consumption.

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APPENDICES

APPENDIX A : Main Function of Codes

APPENDIX A

In the main function of the modeling codes, different sub-functions are used. First of the functions is called "choose_data" is used for to choosing experiment result from the builded working cell. This function takes name of the cell, number of transistor, before or after irradiation result, dose value, body bias value and measurement type as inputs and gives current result of the measurement as output.

"basic_model" function takes working cell, simulation ocean file and model file locations, type of the transistor, aimed experimental results, drain, gate, body and source voltages, transistor number, dose and level number as inputs and gives error between simulation and experimental results as an output. All different level numbers refer to a different model parameter extraction and they are given in the specified order in the modeling section.

Function "body_effect" takes same inputs with "basic_model" function but it models different parameters and takes body biased measurement results as inputs. Moreover, "width_and_length" function takes inputs from two different transistors.

Finally, for an visual output, using "sweep" function takes simulation type, transistor number, body bias, dose level and working cell as inputs. After that plots simulation results with measurement results together.

```
%% Loading experiment results, choosing radiation dose and transistor which is modeled for single transistor model.
% For size dependent model, long and wide transistor is choosen.

load(’ID_cell_with_641_and_355_krads.mat’)
modelloc = ’/vlsi/projects/SERGIO/UMC_180nm_02_16/Cadence_IC6_RF/UMC_18_CMOS/../Models/Spectre/mm180_reg18_v124.mdl.scs’;
idvgsim = ’/home/sadikilik/projects/modeling/with_current_source/idvg.ocn’;
idvdsim = ’/home/sadikilik/projects/modeling/with_current_source/idvd.ocn’;
idvgsimbe =  ’/home/sadikilik/projects/modeling/with_current_source/idvg_body.ocn’;
idvdsimbe =  ’/home/sadikilik/projects/modeling/with_current_source/idvd_body.ocn’;

transistor = 5;
dose = "355 krad";

%% Choosing desired experiment results for linear and saturation region modelings.

Id = choose_data(ID_cell, transistor, 1, dose, 1, "VG", 0, "VDS = 0.05");
Id2 = choose_data(ID_cell, transistor, 1, dose, 1, "VD", 0, "VGS = 1.8");

[error1] = basic_model(ID_cell, modelloc, idvgsim,idvdsim ,’n’, Id, Id2, 0.05, 0.05, 0, 0, transistor, dose, 1);

[error2] = basic_model(ID_cell, modelloc, idvgsim, idvdsim, ’n’, Id, Id2, 0.05, 0.05, 0, 0, transistor, dose,4);

[error3] = basic_model(ID_cell, modelloc, idvgsim, idvdsim, ’n’, Id, Id2, 1.8, 1.8, 0, 0, transistor, dose,2);

[error4] = basic_model(ID_cell, modelloc, idvgsim, idvdsim, ’n’, Id, Id2, 1.8, 1.8, 0, 0, transistor, dose,5);

[error5] = basic_model(ID_cell, modelloc, idvgsim, idvdsim, ’n’, Id, Id2, 1.8, 1.8, 0, 0, transistor, dose,6);

[error6] = basic_model(ID_cell, modelloc, idvgsim,idvdsim ,’n’, Id, Id2, 0.25, 0.25, 0, 0, transistor, dose,0.5);


%% Using VBS = -0.3 V experimental results, reverse body bias effects are adding.

Id3 = choose_data(ID_cell, transistor, 1, dose, 1, "VG", -0.3, "VDS = 0.05");

Id4 = choose_data(ID_cell, transistor, 1, dose, 1, "VD", -0.3, "VGS = 1.8");

```

```
[error7] = body_effect(ID_cell, modelloc, idvgsimbodyeffect, idvdsimbe, ’n’, Id3, Id4, 0.05, 0.05, -0.3, 0, transistor, dose, 2);

[error8] = body_effect(ID_cell, modelloc, idvgsimbodyeffect, idvdsimbe, ’n’, Id3, Id4, 1.8, 1.8, -0.3, 0, transistor, dose, 3);

%% With long and narrow channel and short and narrow channel transistor measurements, dimension effects are adding.

Id5 = choose_data(ID_cell, 2, 1, dose, 1, "VD", 0, "VGS = 1.8");

Id6 = choose_data(ID_cell, 1, 1, dose, 1, "VD", 0, "VGS = 1.8");

Id7 = choose_data(ID_cell, 1, 1, dose, 1, "VG", 0, "VDS = 0.05");

Id8 = choose_data(ID_cell, 1, 1, dose, 1, "VG", 0, "VDS = 1.8");


[error9]= width_and_length(ID_cell, modelloc, idvgsim, idvdsim, ’n’, Id5, Id5, Id7, 1.8, 1.8, 0, 0, 2, dose, 1);

[error10] = width_and_length(ID_cell, modelloc, idvgsim, idvdsim, ’n’, Id6, Id6, Id7, 1.8, 1.8, 0, 0, 1, dose, 2);

[error11] = width_and_length(ID_cell, modelloc, idvgsim, idvdsim, ’n’, Id6, Id6, Id7, 0.05, 0.05, 0, 0, 1, dose, 3);

[error12] = width_and_length(ID_cell, modelloc, idvgsim, idvdsim, ’n’, Id6, Id6, Id7, 0.05, 0.05, 0, 0, 1, dose, 4);
%% To see a clear result, new modeled simulation results and experimental results are shown on the same graph.

[result] = sweep(’IDVD’, 1, 0, "1 Mrad", ID_cell);
```

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