ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

X-BAND HYBRID FRONT-END RECEIVER MODULE DESIGN FOR SPACEBORNE SYNTHETIC APERTURE RADAR APPLICATIONS

M.Sc. THESIS

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SENTETİK ARALIKLI RADAR UZAY PLATFORMLARINA UYGUN X-BANT HİBRİD ÖN UÇ RF MODÜLÜ TASARIMI

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Arif Ekin UZUN, a M.Sc. student of ITU Graduate School of Science Engineering and Technology 514101011 successfully defended the thesis entitled "X-BAND HYBRID FRONT-END RECEIVER MODULE DESIGN FOR SPACEBORNE SYNTHETIC APERTURE RADAR APPLICATIONS", which he/she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To every scientist and engineer who paved the way for current technological achievements...

FOREWORD

I would like to express my gratitude to my supervisor, Professor Sedef Kent Pınar, for her guidance and support during development of the thesis project.

June 2019

Arif Ekin UZUN
(Design Engineer)

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ABBREVIATIONS

RF	**:** Radio Frequency
MW	**:** Microwave
SAR	**:** Synthetic Aperture Radar
BW	**:** Bandwidth
SNR	**:** Signal-to-Noise Ratio
DC	**:** Direct Current
PRI	**:** Pulse Repetation Interval
PRF	**:** Pulse Repetation Frequency
SWaP	**:** Size-Weight and Power
MDS	**:** Minimum Detectable Signal Level
FET	**:** Field Effect Transistor
BJT	**:** Bipolar Junction Transistor
HBT	**:** Heterojunction Bipolar Transistor
GaAs	**:** Gallium Arsenide
SiGe	**:** Silicon Germanium
SOI	**:** Silicon-on-Insulator
InGaP	**:** Indium-Gallium-Phosphate
BiCMOS	**:** Bipolar-Complementary Metal Oxide Semiconductor
LTCC	**:** Low Temperature Co-Fired Ceramic
dBFS	**:** Full Scale in Decibel
MMIC	**:** Monolithic Microwave Integrated Circuit
MIC	**:** Microwave Integrated Circuit
pHEMT	**:** Pseudomorphic High Electron Mobility Transistor
CAD	**:** Computer Aided Software
MoM	**:** Method of Moments
PCB	**:** Printed Circuit Board
PTFE	**:** Polytetrafluoroethylene
SPICE	**:** Simulation Program with Integrated Circuit Emphasis

SYMBOLS

C	**:** Capacitance
L	**:** Inductance
Δt	**:** Time Delay
Δr	**:** Spatial Distance
τ	**:** Pulse Width
$\mathbf{V_n}$	**:** Velocity of Object N
$\mathbf{f_d}$	**:** Doppler Frequency Shift
Δx	**:** Range Resolution
Δy	**:** Cross-Range Resolution
$\Omega_{\mathbf{3dB}}$	**:** 3dB Antenna Beamwidth
$\mathbf{V_{pp}}$	**:** Peak-to-Peak Voltage
$\mathbf{V_{peak}}$	**:** Peak Voltage
$\mathbf{f_c}$	**:** Center Frequency
W	**:** Microstrip Width
h	**:** Substrate Height
$\varepsilon_\mathbf{r}$	**:** Dielectric Constant
$\varepsilon_\mathbf{e}$	**:** Effective Dielectric Constant
$Z_\mathbf{0}$	**:** Characteristic Impedance
$R_\mathbf{x}$	**:** Resistance of x
$X_\mathbf{x}$	**:** Reactance of x
$\lambda_\mathbf{g}$	**:** Guided Wavelength

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SUMMARY

Synthetic Aperture Radars (SARs) are widely investigated active microwave imaging systems which generate their own source of radiation. Due to their active sensing nature, electrical performance and specification of microwave equipments such as SAR Receivers and Transmitters directly effects the imaging performance. On the other hand, synthetic aperture radars can be integrated into various airborne and spaceborne platforms. Design methodology for microwave equipments greatly differs with utilized platforms owing to unique environmental conditions and reliability requirements.

In the scope of this thesis, Spaceborne SAR Receiver Front-End Hybrid Module design methodology is presented in detail. Firstly, Synthetic Aperture Radar theory of operation has been briefly disclosed to reveal crucial radar parameters that determine the quality of constructed radar images. Subsequently, SAR receiver related design parameters are introduced which will be used as design constraints on following chapters. Platform related design challanges and their sources such as radiation tolerance and low probability of failure due to long mission lifetimes are elaborated in detail. Because of the fact that SAR receiver front-end modules are part of a complete receiver equipment, their electrical specifications and design constraints are correlated to receiver system architecture that they are integrated. Therefore most commonly used receiver design architectures are examined and a unique SAR receiver architecture has been proposed. System level RF simulation approach has been chosen to validate electrical performance of the proposed receiver. Prior to system level simulations, part selection process which is severely constrained by space environment, electrical performance and reliability concerns are presented in detail. Consequently, receiver front-end module has been isolated from proposed SAR receiver architecture based on frequency of operation, interconnection methods of circuit elements and manufacturing technology preferences.

Finally, detailed design process of each individual RF/Microwave sub-blocks which reside in SAR Receiver Hybrid Front-End Module is presented in depth. Designed microwave integrated circuits (MICs), namely; LNA, Image Reject Filter, Downconversion Mixer, Frequency Doubler, Harmonic Rejection Filter and LO Buffer Amplifier are integrated into single enclosure to construct hybrid front-end structure. Designed SAR Receiver Hybrid Front-End module can operate within 7500-8500 MHz input frequency with 250 MHz signal bandwidth, provide more than 35 dB conversion gain and 50dB Image Rejection while requiring power consumption less than 1.1W.

SENTETİK ARALIKLI RADAR UZAY PLATFORMLARINA UYGUN X-BANT HİBRİD ÖN UÇ RF MODÜLÜ TASARIMI

ÖZET

Sentetik Açıklıklı Radarlar (SAR) kendi oluşturdukları radyo frekans dalgalarını kullanarak hedef görüntüsü oluşturabilen ve oldukça fazla araştırmaya konu olan aktif mikrodalga görüntüleme sistemleridir. Birçok farklı hava ve uzay platformuna yerleştirilebilen Sentetik Açıklıklı Radarların sistem gereksinimleri, bulundukları platformun kendine özel çevresel koşulları ve görev süresi ile ilintili güvenilirlik isterlerine bağlı olarak farklılık gösterebilmektedir. Aktif sensör yapılarından dolayı, sinyal alıcı ve verici ekipmanlar gibi üzerlerinde taşıdıkları mikrodalga ekipmanların elektriksel özellikleri ve performansları görüntüleme kabiliyetlerine doğrudan etki etmektedir. SAR altsisteminin parçaları olan mikrodalga ekipmanlarının tasarım yöntemleri de platform ve görev gereksinimlerine göre oluşturulmaktadır. Mikrodalga ekipmanların tasarım mimarileri; çevresel sıcaklık koşulları, görev süresi boyunca ekipman üzerine düşebilecek radyasyon dozu oranı, ekipmanların görev süresi içinde izin verilen en yüksek arıza yapabilme ihtimali, elektriksel performans gereksinimleri ve üretim teknolojileri gibi tasarım girdileri birlikte değerlendirilerek ortaya konulmaktadır.

Bu tez kapsamında, Uzay Platformlarına Uygun Sentetik Açıklı Hibrit Ön-Uç RF Modülü tasarım metodolojisi detaylıca sunulmuştur. RF Modül yapılarının SAR alıcı/verici ekipmanların bir parçası olması, SAR alıcı/verici ekipmanların ise bütün Sentetik Açıklıklı Radar sistemlerinin bir parçası olması göz önünde bulundurularak yukarıdan-aşağıya tasarım yöntemi benimsenmiştir. Yukarıdan aşağıya tasarım yöntemi ile sistem mimarisinden ekipman mimarisine, ekipman mimarisinden RF alt-modül ayrımına geçiş yapılmıştır. Gereksinimleri belirlenen RF hibrid modülün detaylı tasarımı ise uzay koşullarında yüksek güvenilirliğe sahip malzeme, yarı-iletken ve üretim teknolojileri göz önünde bulundurularak belirlenmiştir.

İlk bölümde; Sentetik Açıklıklı Radar sistemlerinin çalışma yöntemlerinin, geleneksel radar sistemleri ile birçok benzerlik barındırması nedeniyle öncelikle geleneksel radar sistemlerinin çalışma prensipleri ele alınmıştır. Bir radar sisteminin hedef ayırt edebilme yeteneğini belirleyen mesafe çözünürlüğü ve çapraz açıklık çözünürlüğü özelliklerini etkileyen sistem parametreleri değerlendirilmiştir. Daha sonra Sentetik Açıklıklı Radar çalışma prensipleri ve kuramları incelenmiş, çalışma prensipleri doğrultusunda oluşturulacak radar görüntülerinin kalitesini belirleyen sistem değişkenleri elde edilmiştir. Sentetik Açıklıklı Radar sistemlerinin yerleştirildikleri platformun hareketinden yararlanarak; geleneksel radar sistemlerinin aksine, fiziksel boyutları küçük bir anten kullanarak çok daha büyük radar antenleri ile sağlanabilecek çapraz açıklık çözünürlüklerine ulaşabilecekleri doğrulanmıştır. Sentetik Açıklıklı Radar sistem parametrelerini kullanarak; hedeften yansıyan radar sinyallerinin güç

seviyesinin, gürültü seviyesine oranını belirlemek amacı ile SAR Radar denklemi türetilmiştir.

Uzay platformlarında kullanılan RF/mikrodalga ekipmanlarının olası bir arıza durumunda tamir ve bakım imkanı olmaması nedeniyle yüksek güvenilirliğe sahip olması gerekmektedir. Tasarımda kullanılan elektronik bileşenlerin ve materyallerin beş ile yirmi yıl arasında değişen uydu operasyon süresince maruz kalacağı sıcaklık değişimleri, iyonize doz etkileri, yüksek enerjili parçaçık etkileşimleri ve vakum ortamı altında performans kaybı olmadan çalışmayı sürdürebilmelidir. Diğer taraftan, fırlatma sırasında fırlatıcı kaynaklı yüksek ivme değerlerine sahip mekanik titreşim ve şok etkilerine karşı zarar görmemelidir. İkinci bölümde; SAR sistemlerinde kullanılan radyo frekans alıcı ekipmanlar ile ilgili taşıyıcı frekans bandı, radar sinyali bant genişliği, dinamik bölge, gürültü faktörü elektriksel tasarım parametreleri ve kullanılan platforma bağlı radyasyon etkisi, yüksek güvenilirlik ihtiyacı, malzeme ve teknoloji limitasyonları değerlendirilmiştir. Uydu platformlarında kullanılan örnek SAR sistemlerinin kabiliyetleri karşılaştırılmış ve ekipman mimari tasarımı aşamalarında kullanılmak üzere hedef gereksinimler üretilmiştir.

Kablosuz haberleşme sistemlerinde kullanılan tasarım mimarileri, sistem isterlerine göre büyük farklılıklar gösterebilmektedir. Uzay şartlarına uygun kalifikasyona sahip elektronik bileşenlerin yüksek maliyetleri ve limitli çeşitliliği, mimari tasarımda seçilebilecek yöntemleri sınırlandırmaktadır. Üçüncü bölümde; en sık kullanılan alıcı tasarım mimarileri incelenmiş, uzay platformu SAR sistemlerinde kullanılmak üzere zayıf ve güçlü yönleri değerlendirilmiştir. İncelenen mimarilerin avantaj sağladıkları alanlar bir araya getirilerek, özgün Sentetik Açıklıklı Radar Alıcı Ekipmanı mimarisi sunulmuştur.

Bilgisayar destekli tasarım ortamları, detaylı tasarım aşamasına geçilmeden önce mimari tasarımı doğrulamak amacı ile kullanılabilmekte böylece öngörülemeyen tasarım eksikliklerinin hızlıca giderilmesi için pratik bir yöntem sağlamaktadır. RF/mikrodalga alıcı ekipmanları için kritik olan kazanç bütçesi, gürültü figürü, lineer operasyon güç seviyesi aralığı, üretilen istenmeyen sinyal seviyeleri gibi performans parametreleri yüksek doğruluk ile gözlemlenebilmektedir. Dördüncü bölümde; sunulan ekipman mimarisinin elektriksel performansını doğrulamak amacı ile sistem seviyesi radyo frekans benzetimleri yürütülmüştür. Sistem seviyesi benzetimleri gerçekçi kılmak amacıyla, uzay platformlarına uygun limitli elektronik bileşenler ve/veya ayrık tasarım yöntemleri belirlenerek benzetimlere girdi sağlanmıştır. Benzetim sonuçları ile doğrulanan SAR alıcı ekipman mimarisinden; çalışılan frekans bandı, elektriksel bileşenlerin bağlantı yöntemleri ve üretim teknolojileri değerlendirilerek Hibrid RF Ön-Uç Modülü kapsamı belirlenmiştir.

Beşinci bölümde ise; kapsamı belirlenen Hibrid RF Ön-Uç Modülü'nün içinde bulunan RF/Mikrodalga alt-blokların detaylı tasarım süreçleri ayrıntıları ile sunulmuştur. RF Ön-Uç Modülü; Düşük Gürültülü Yükseltici, Görüntü Bastıran Filtre, Frekans İndirgeme Karıştırıcı, Frekans Çarpıcı, Harmonik Bastıran Filtre ve Lokal Osilatör Yükseltici mikrodalga entegre devrelerini içerisinde barındırmaktadır. Mikrodalga entegre devreler; düşük iletim kaybına, ortam sıcaklığından ve çalışma frekansından etkilenmeyen dielektrik sabitine, yüksek eğilme mukavemetine sahip aluminyum oksit alt katmanları üzerinde gerçeklenmiştir. GaAs yongalar ile yakın termal genleşme

katsayısına sahip olan aluminyum oksit malzemesi aynı zamanda sıcaklık değişimleri sırasında genleşmeden kaynaklı kesme gerilmesi etkisini en aza indirgemektedir. İnce film üretim teknolojisi seçilerek yüksek frekanslarda devre performansını etkileyen üretim toleranslarının etkisi zayıflatılmıştır.

Düşük Gürültülü Yükseltici devresi; GaAs teknolojisi ile üretilen monolitik mikrodalga tümleşik devre yongası kullanılarak tasarlanmıştır. Geniş bantta yüksek kazanç ve düşük gürültü figürü sağlayabilen yonganın kullanılan bant içi performansı, harici empedans uyumlama teknikleri ile arttırılmıştır. Yonganın ihtiyaç duyduğu besleme gerilimi, altın tel-bağlama üretim yöntemlerine uygun tek katlı kapasitörler ile aktarılarak besleme hattı üzerinde oluşabilecek salınımlar engellenmiştir.

Görüntü Bastıran Filtre devresi; mikroşerit dağıtılmış eleman filtre yöntemi ile tasarlanmıştır. Bant-geçiren mikroşerit filtre mimarileri incelenmiş, düzlemsel yapısı ve daha az fiziksel alan kullanımı nedeniyle Firkete Filtre yapısı tercih edilmiştir. Analitik simülasyon yöntemleri ile başlangıç parametreleri belirlendikten sonra, tasarım elektromanyetik Memont Metodu kullanılarak optimize edilmiştir.

Frekans İndirgeme Karıştırıcı devresi; çift dengeli mimariye sahip monolitik mikrodalga tümleşik devre yongası kullanılarak tasarlanmıştır. RF giriş portu, lokal osilatör giriş portu ve ara frekans çıkış portuna sahip karıştırıcı devresi; X-Bant'ta aldığı işareti C-Bant'ta üretilen lokal osilatör işaretini kullanarak S-Bant'a indirgemektedir. Karıştırıcı bileşenlerin port empedansları, doğrusal olmayan yapılarından kaynaklı çalışma frekanslarına ve sürülme gücüne göre değişiklik gösterebildiği için giriş/çıkış portlarına ayarlama dolguları yerleştirilmiştir.

Frekans Çarpıcı devreleri pasif ve aktif olarak iki grupta incelenmektedir. Pasif frekans çarpıcı devreleri varaktör ve Schottky diyotların doğrusal olmayan karakteristikleri kullanılarak, aktif frekans çarpıcı devreleri ise transistörlerin doğrusal olmayan çalışma aralığında sürülmesi ile gerçeklenebilmektedir. Pasif frekans çarpıcı devrelerin yüksek giriş gücü ihtiyacı ve yüksek dönüşüm kaybına sahip olması nedeniyle, aktif frekans çarpıcı mimarisi seçilmiştir. Transistör seçiminde S-Bant ve C-Bant arasında geniş bantlı empedans uyumlaması imkanı sağlayan ve yüksek kazanç verebilen SiGe HBT teknolojisi seçilmiştir.

Harmonik Bastıran Filtre devresi; mikroşerit dağıtılmış eleman filtre yöntemi ile tasarlanmıştır. Mikroşerit filtreler arasında en az fiziksel alan kullanımına ve en yüksek harmonik sinyal bastırma oranına sahip olması nedeni ile Parmakarası Filtre yapısı tercih edilmiştir. Analitik benzetim yöntemleri ile başlangıç parametreleri belirlendikten sonra, tasarım elektromanyetik Memont Metodu kullanılarak optimize edilmiştir.

Aluminyum oksit alt-katmanları üzerinde tasarlanan mikrodalga entegre devreleri kovar taban plakası üzerine yerleştirilerek bir araya getirilmiş ve Hibrid Ön-Uç Modülü oluşturulmuştur. Modül içinde yüksek güçlü lokal osilatör sinyalinin RF giriş sinyaline kuplajını zayıflatmak amacı ile devreler iki ayrı kavite içine yerleştirilmiştir. Tasarlanan SAR Alıcı Hibrid Ön-Uç Modülü 7500-8500 MHz giriş frekans aralığında 250 MHz'lik radar sinyal bant genişliği, 35 dB dönüşüm kazancı sağlayabilmekte ve 1.1W'tan daha az güç tüketmektedir.

1. INTRODUCTION

Synthetic Aperture Radar Systems provide a method to generate high-resolution images where image quality does not depend on weather conditions or solar illumination of the target surface unlike optical imaging systems. Primary application areas of SAR systems are military reconnaisance and survaillance, terrain imaging, tracking of environmental conditions and climate change, agricultural planning and planetary surface mapping [1].

Principle of SAR operation relies on collecting radar echo signals reflected from target surface where radar signals are generated and transmitted by SAR platform. Amplitude and phase information carried on reflected radar signals depends on physical and material characteristics of the target surface. Combination of multiple echo signals while SAR platform is on the move simulates the effect of much longer antenna aperture size with smaller physical antenna aperture. Signal and image processing algorithms applied on collected echo signals provides high-resolution images.

LEO Satellite platforms are found to be excellent carriers for imaging SAR systems due to complete coverage of the Earth Surface, low maintanence cost of satellite and uninterrupted operation advantage. However designing electronics equipments for spaceborne applications presents significant challanges due to radiation effects and long mission life-times. Therefore spaceborne electronics are built upon radiation hardened/tolerant, high-reliability parts and technologies which are very limited in type and quantity. Reducing the risk of the failure for spaceborne systems are crucially important since there are no ways to repair the hardware and schedule a maintanance once the satellites has been launched into their operational orbit.

1.1 Purpose of the Thesis

This thesis present a methodology for designing a Synthetic Aperture Radar Hybrid Front-End Module for Spaceborne Applications. Considering a RF receiver module design requirements and boundaries depends on the receiver architecture that module is placed into, complete receiver design architecture is presented at first in parallel with system level mission requirements that are derived from current spaceborne SAR programs. Therefore, three main stages of a spaceborne RF/Microwave front-end design is covered in thesis, namely; derivation of system requirements, architectural design of SAR receiver equipment and detailed design steps of Receiver Hybrid Front-End module.

1.2 Literature Review

Synthetic Aperture Radar systems theory of operation, critical radar parameters and signal processing methods has been published in detail by Curlander *et al.* [2], Mahafza [3], Elachi [4], Lusch [5] and Lacomme *et al.* [6]. However aforementioned publications are intended for solely academic purposes therefore does not possess adequate information on SAR instrument design or spaceborne environment related design constraints. On the other hand; several papers that presents in-depth knowledge regarding SAR instruments have been issued by companies and agencies involved in space industry such as Thales Alenia Space [7] [8] [9] [10], Airbus Defence and Space [11] [12] [13] [14] [15] and European Space Agency [16] [17]. Although these papers presented in various proceedings explain the system level architecture of the different SAR RF instruments, design methodologies are not elaborated.

2. SYNTHETIC APERTURE RADAR

In this chapter, basic operation principles of Synthetic Aperture Radar (SAR) will be examined. Design parameters which will be derived from theory shall be presented and will be used for consecutive chapters. Since SAR systems can be deployed to various platforms such as land, airborne and spaceborne platforms; several spaceborne SAR applications shall be given in detailed as reference design platforms.

2.1 Introduction

Synthetic Aperture Radar (SAR) remote sensing technology has been proposed as an alternative/complementary solution to Optical and Infrared Remote Sensing Technologies by Carl A. Wiley in June 1951 [18]. Since its time of invention, SAR systems has been used in wide range of applications such as environmental monitoring, landscape mapping and military reconnaissance [5].

SAR systems are categorized as active remote sensing systems which uses their own source of microwave radiation to collect data from reflected waves. Since passive remote sensing technologies uses reflection of waves generated by solar radiation, their performance depends on several visibility factors such as day/night conditions, cloud formations and weather conditions. Due to their active nature, SAR systems does not require an external radiation source therefore eliminates dependency on solar illumination.

Theory of operation of the Synthetic Aperture Radar is very similar to conventional radar. Since all radar systems operate on the same principle which is determining the distinction between transmitted and received electromagnetic waves, main difference between synthetic aperture and conventional radar systems comes from antenna aperture size [3].

2.2 Radar Principles

First of all, it is essential to understand fundamental radar operations before investigating SAR systems. Let us consider a radar signal pulse transmitted from a fixed platform and its interaction with two stationary points in space as given in Figure 2.1. When we observe the reflected waves, there will be a time difference between them due to spatial distance between the scatterers. Resulting time delay can be found by dividing two times the distance between scattering points to wave propagation speed

$$\Delta t = \frac{2\Delta r}{c} \tag{2.1}$$

where Δt represents time delay, Δr is the spatial distance and c is the speed of an electromagnetic wave. Multiplication by two arises from two-way propagation of transmitted waves. In order to distinguish the points from each other, pulse width (τ)

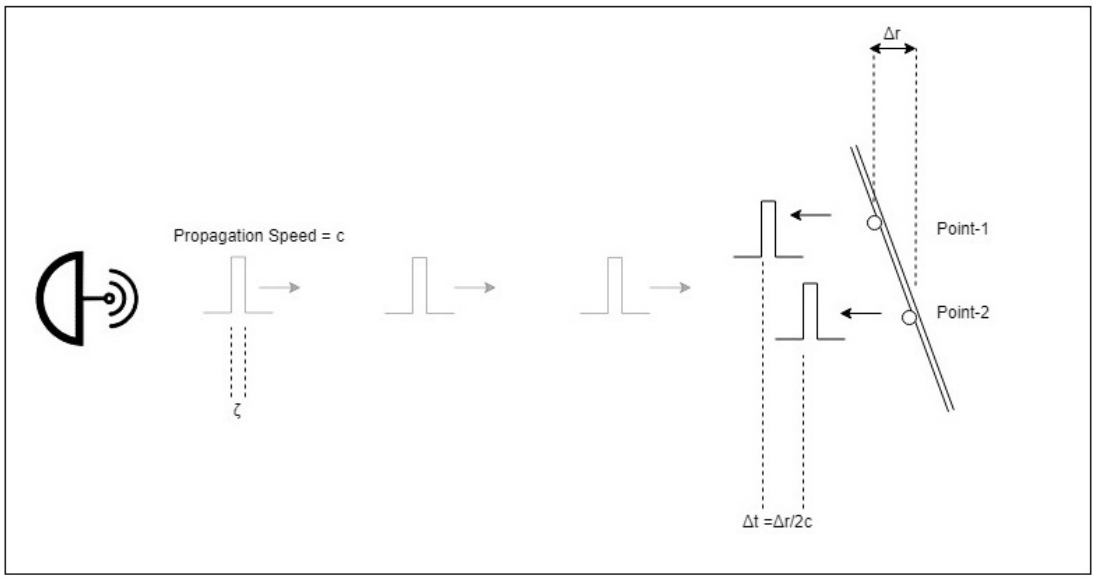


Figure 2.1 : Radar reflection of two points in space.

of the transmitted signal should be smaller than $2\Delta r/c$. Otherwise echo signals will overlap in time and will be interpreted as single point in the receiver side. Therefore the minimum distance that can be discriminated between to points can be calculated by

$$\Delta r = \frac{c\tau}{2}. \tag{2.2}$$

Since pulse width is related to radar signal bandwidth as $\tau = 1/BW$;

$$\Delta r = \frac{c}{2BW} \tag{2.3}$$

Δr is defined as *Range Resolution*. Smaller Δr results in better discrimination of the targets which in return results in better radar performance. As it can be seen from Equation 2.2 in order to improve the range resolution, pulse width should be decreased. However there are hardware constraints which limits the minimum pulse width that can be used in a radar system. Due to hardware limitations, pulse compression techniques has been proposed as an alternative way to increase the bandwidth of the radar pulse without decreasing the pulse width [3].

Using solely range discrimination methods, radar systems can generate 1-D mapping of targets. If there is a relative radial velocity difference between targets and radar platform, it is possible to differentiate the targets on a second mapping plane (cross-range plane) utilizing doppler effect. Sample case of a system with stationary radar platform and moving object with constant speed of V_t is given in Figure 2.2. Although moving object has a constant speed, radial velocity of two scatterer points will differ with respect to stationary radar platform.

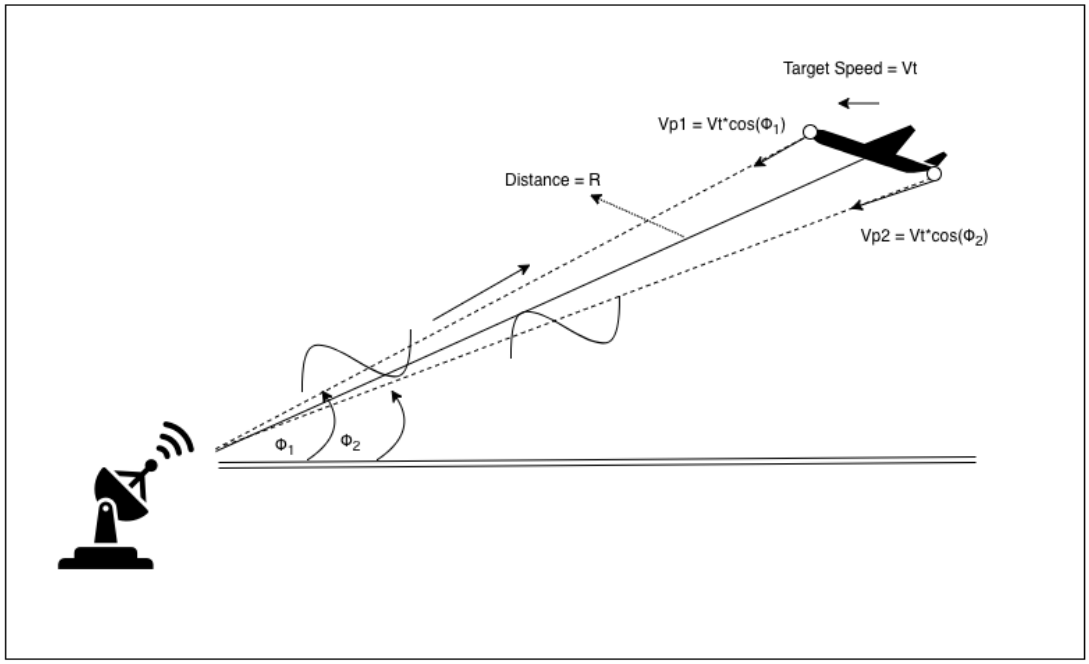


Figure 2.2 : Radar reflection from moving target.

$$V_{p1} = V_t cos\theta_1 \tag{2.4}$$

and

$$V_{p2} = V_t cos\theta_2 \tag{2.5}$$

represents radial velocity of scatterer points p_1 and p_2 with respect to radar platform. Due to doppler effect, carrier frequency of the reflected radar waves will be shifted depending on relative radial velocity of the scatterer points. Frequency shift of the reflected waves can be calculated by

$$fd_1 = \frac{2Vp_1}{\lambda} \tag{2.6}$$

and

$$fd_2 = \frac{2Vp_2}{\lambda} \tag{2.7}$$

where λ is the wavelength of the radar wave. Doppler frequency difference of the scatterers can be discovered using

$$fd_1 - fd_2 = \frac{2Vp_1}{\lambda} - \frac{2Vp_2}{\lambda} \tag{2.8}$$

inserting Equation 2.4 and 2.5 into 2.8:

$$fd_1 - fd_2 = \frac{2V_t(cos\theta_1 - cos\theta_2)}{\lambda}. \tag{2.9}$$

Cosine term in 2.9 can be expanded to multiplication of sine terms using $cos(a) - cos(b) = -2sin(\frac{a+b}{2})sin(\frac{a-b}{2})$ which results in

$$fd_1 - fd_2 = \frac{2V_t}{\lambda}(-2sin(\frac{\theta_1 + \theta_2}{2})sin(\frac{\theta_1 - \theta_2}{2})). \tag{2.10}$$

It can be assumed that $\theta_1 - \theta_2$ is close to zero. Using small-angle approximation $sin(x) \approx x$ on Equation 2.10 and taking angle difference to left-hand side of the equation:

$$fd_1 - fd_2 = \frac{-4V_t}{\lambda} sin\theta_1(\theta_1 - \theta_2) \tag{2.11}$$

$$(\theta_1 - \theta_2) = \frac{(fd_1 - fd_2)\lambda}{-4V_t sin(\theta_1)}. \tag{2.12}$$

As it can be seen from Equation 2.12, azimuth angle difference between scatterers can be found utilizing doppler frequency difference of the reflected radar echos.

However in order to discriminate the scatterers from each other, projection of antenna beam-width to the target should be smaller than the distance between scatterer points;

$$\Delta y = 2Rsin(\Theta_{3dB}/2) \tag{2.13}$$

where R is the target distance, Θ_{3dB} is the 3dB beamwidth of the antenna and Δy is the smallest distance between scatterer points that can be discriminated from each other. Antenna beamwidth projection on a aerial target has been given as an example in Figure 2.3. Using small-angle approximation $sin(x) \approx x$ on Equation 2.13 follows

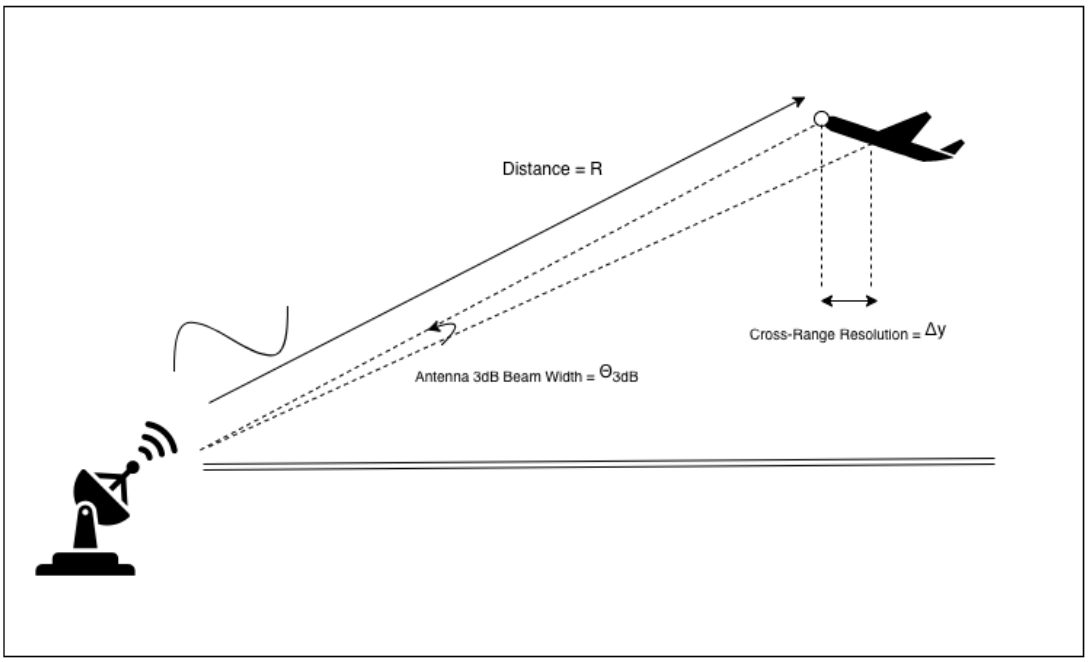


Figure 2.3 : Antenna beamwidth projection to aerial target.

that

$$\Delta y = R\Theta_{3dB}. \tag{2.14}$$

Since 3dB beamwidth of an antenna with aperture length of L_{ANT} and operating wavelength λ is equal to

$$\Theta_{3dB} = \lambda / L_{ANT} \tag{2.15}$$

Equation 2.14 can be represented in terms of antenna aperture length and operating wavelength as following formula

$$\Delta y = \frac{R\lambda}{L_{ANT}}. \tag{2.16}$$

Δy is known as $Cross-Range$ or $Azimuth\,Resolution$. Smaller Δy results in better discrimination of the targets which in return provides better radar performance. Equation 2.16 shows the fact that; antenna aperture length should be increased in order to improve the cross-range resolution. However physically length the antennas are limited by platform installations which may not be feasable in practical applications.

2.3 Theory of Operation

Synthetic Aperture Radar is a special type of radar technology that can construct high-resolution two-dimensional images of terrestrial surface while utilizing the movement of the airborne or spaceborne platform. SAR overcomes the cross-range resolution dependency on target distance by means of synthetically emulating much bigger antenna in comparison to actual aperture length [2]. Spaceborne SAR platform representation of operation is illustrated in Figure 2.4 . As satellite platform moves with speed of $Vsat$ in reference to earth surface, illumination area of the surface is swept alongside satellite flight trajectory. Distance traveled by satellite during illumination time of the target will result in collection of return signals with different reflection angles therefore produce the same effect of a single physical antenna with the aperture size of D_{SA}. Returned radar waves are collected by satellite for further data processing in order to reconstruct image of the surface. Size of illumination area depends on antenna 3dB beamwidth (θ), distance of satellite to earth surface (R_d) and wave incidence angle (γ). Ground swathe width can be approximated to

$$W_g \approx \frac{R_d \theta}{cos(\gamma)}. \tag{2.17}$$

Reconstructed two-dimensional radar image consists of small cells that defines the resolution of image. In order to achieve a high quality image, resolution should be increased by decreasing the size of the cells that compose the image. Therefore enhancement of the image quality directly depends on range and azimuth resolution of the SAR system. These resolution cells can be visualized as given in Figure 2.5 and they will be referenced as azimuth and range cells throughout the chapter. Range resolution of the satellite SAR platform represented in Figure 2.4 can be calculated

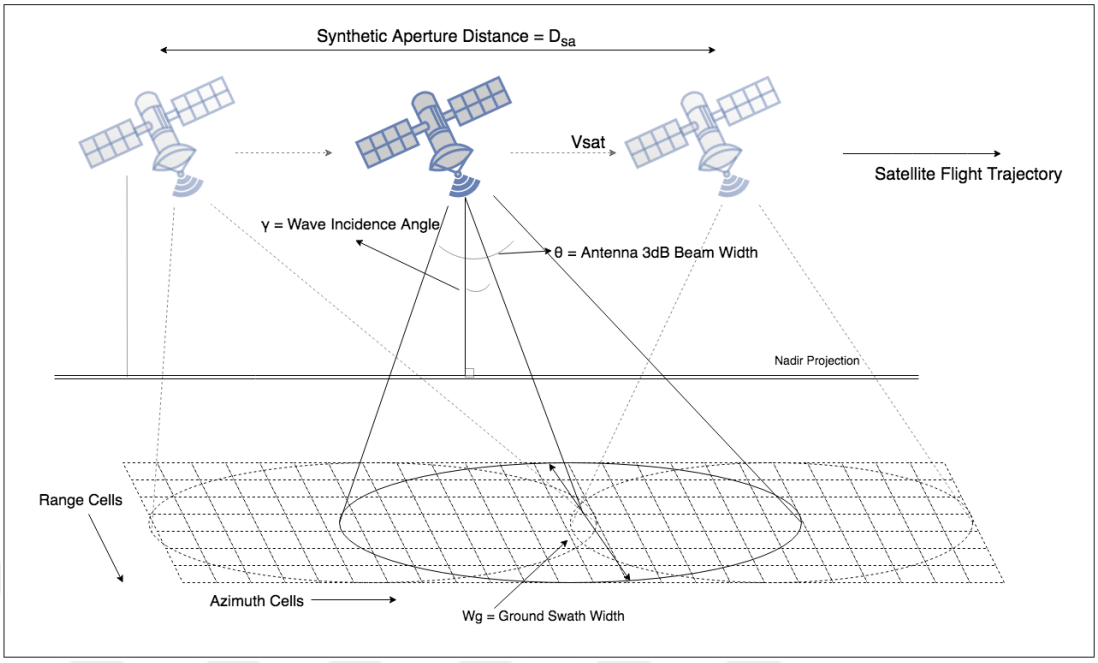


Figure 2.4 : Spaceborne SAR platform operation.

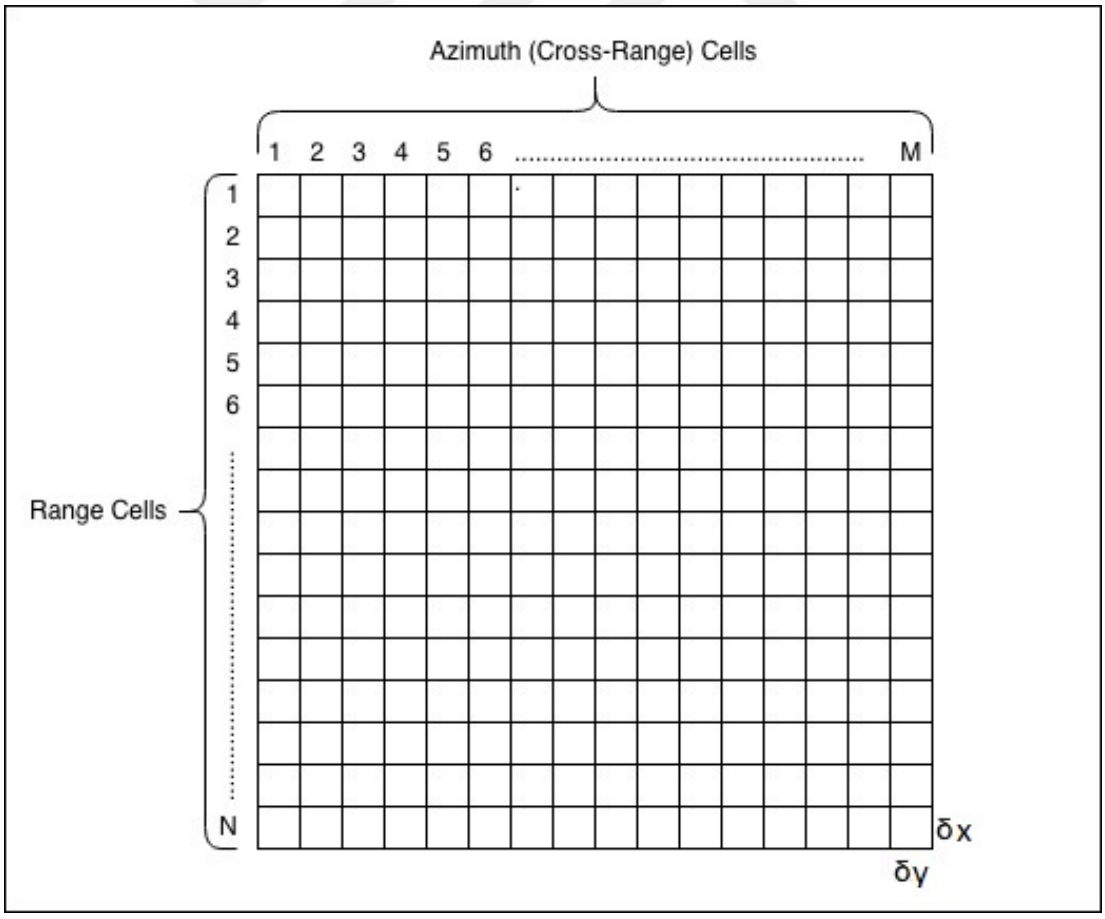


Figure 2.5 : 2-D radar image representation using resolution cells.

with

$$\delta r = \frac{c}{2BW\sin(\gamma)} \tag{2.18}$$

where BW is the frequency bandwidth of the radar signal, c is the speed of light and γ is the wave incidence angle. Cross-range resolution of the satellite SAR platform represented in 2.4 can be calculated with

$$\delta y = \frac{\lambda R}{L_{eff}} \tag{2.19}$$

where λ is the wavelength of transmission frequency of the radar signal, R is the slant range and L_{eff} is the effective antenna aperture length. Evidently, range and cross-range resolution equations of a SAR systems given in Equation 2.18 and Equation 2.19 is similar to ones that are used on conventional radar systems given in Equation 2.18 and Equation 2.16 except the fact that L_{ANT} is now replaced with L_{eff}. L_{eff} of a satellite SAR system can be found by

$$L_{eff} = T_{Illumination} V_{SAT} \tag{2.20}$$

where $T_{Illumination}$ represents the illumination time of the target and V_{SAT} represents the velocity of the satellite with respect to earth surface. Illumination time of the target $T_{Illumination}$ depends on antenna beamwidth Θ_{3dB}, slant range R and satellite velocity V_{SAT} with following formula

$$T_{Illumination} = \frac{Rsin\Theta_{3dB}}{V_{SAT}} \tag{2.21}$$

Assuming satellite is far away from the surface and antenna beamwidth is very narrow, small angle approximation $sin(x) \approx x$ can be applied to 2.21

$$T_{Illumination} \approx \frac{R\Theta_{3dB}}{V_{SAT}} \tag{2.22}$$

Inserting Equation 2.15 into Equation 2.22 and combining with Equation 2.20, cross-range resolution of SAR system can be simplified to

$$\delta y = L_{ANT} \tag{2.23}$$

Interestingly, cross-range resolution found in Equation 2.23 no longer has any dependancy on slant range in contrast to conventional radars. This attribute of SAR

Table 2.1 : Spaceborne SAR systems parameters.

System Parameters	SENTINEL-1A	PAZ	KOMPSAT-5
Satellite Altitude	693 km	514 km	550 km
Incidence Angle	20-45deg	15-60deg	20-45deg
Range Resolution	5m	3m	1m
Cross-Range Resolution	5m	3m	1m
Operating Frequency	5.405 GHz	9.65 GHz	9.66 GHz
Maximum Bandwidth	87.6 MHz	300 MHz	120 MHz
Antenna Length	12.3m	4.8m	4m

makes constructing high resolution 2-D images with small antennas from distant platform possible. In order to better understand effect of synthetic aperture, several spaceborne SAR satellite systems specifications has been listed in Table 2.1 [19]. In case of using a conventional radar for terrestrial imaging on SENTINEL-1A, PAZ and KOMPSAT-5 platforms, antenna aperture length should have been 7693m, 5326m and 17080m respectively in order to achieve required cross-range resolution. As it can be understood, several km antenna sizes are not practical in real world applications.

2.4 SAR Radar Equation

As described in Section 2.3, image reconstruction is accomplished by collecting and processing echo signals reflected by the target area. Although range and cross-range resolution determines the quality of the image; primarily, radar receiver should be able to distinguish the received signals from noise level for further processing. Noise level that is present in the SAR receiver could be originated from external or internal sources in practical applications however only internally generated noise will be used throughout the section for simplicity. Every electronic circuit intrinsically generates white random noise due to thermal agitation of the electrons which is called Thermal Noise. Owing to its white-noise characteristic, total thermal noise power of the radar receiver within interested signal bandwidth can be calculated using

$$ThermalNoisePower = kTB \tag{2.24}$$

where k is the Boltzman Constant, T is the temperature in Kelvin and B is the bandwidth of interest. Successful detection and discrimination of the received echo signals depends on the ratio of the received power level to noise generated by receiver

electronics which is called Signal-to-Noise (SNR) ratio. SNR level of the single radar pulse can be calculated using

$$SNR_{Single} = \frac{P_r}{kTB} \tag{2.25}$$

where P_r represents the received radar signal power. Since SAR systems transmit number of radar pulses and collect the return signals during the time it takes to travel synthetic aperture length, collected data is integrated to improve processed SNR. Time interval between two consecutive radar pulse is defined as *Pulse Repetation Interval* (PRI). Assuming a SAR radar satellite platform with synthetic aperture length of L_{eff} and platform velocity of V_{SAT}, number of pulses N generated during timeframe of synthetic aperture synthesis can be calculated using

$$N = \frac{L_{eff}}{V_{SAT} PRI}. \tag{2.26}$$

Therefore overall SNR value after integration of the pulses is

$$SNR_{Overall} = \frac{P_r N}{kTB} = \frac{L_{eff} P_r}{V_{SAT} PRI kTB}. \tag{2.27}$$

Due to free space path loss and atmospheric effects, transmitted radar signals are greatly attenuated while propagating in the air. Assuming SAR system uses same antanna for transmit and receive operation on a target with radar cross section σ, received power level P_r at the antenna can be calculated by

$$P_r = \frac{Pt G_{ANT}^2 \lambda^2 \sigma}{(4\pi)^3 R^4} \tag{2.28}$$

where P_t is transmitted radar signal power, G_{ANT} is the antenna gain, λ is the wavelength of the operating frequency and R is the target range. Inserting Equation 2.28 to Equation 2.27 reveals the final form of the $SNR_{Overall}$

$$SNR_{Overall} = \frac{L_{eff} Pt G_{ANT}^2 \lambda^2 \sigma}{(4\pi)^3 R^4 V_{SAT} PRI kTB} \tag{2.29}$$

$$T = (F-1)T_0 \tag{2.30}$$

Examining equation 2.29 reveals the fact that overall SNR of the SAR system directly proportional to Synthetic Aperture Length (L_{eff}), Transmitted Signal Power (Pt), Antenna Gain (G_{ANT}), Wavelength of the Operating Frequency (λ) and radar cross section (σ). On the other hand inversely proportional to Radar Range (R), Pulse Repetation Interval (PRI) and thermal noise power of the receiver (kTB) where T represents the receiver noise temperature [6].

3. SPACEBORNE SAR RECEIVER DESIGN CONSIDERATIONS

3.1 Introduction

SAR Receivers play a crucial role in Spaceborne Synthetic Aperture Radar Systems. Receiver electronics has to satisfy related equipment level requirements such as signal bandwidth, noise figure and interference immunity while maintaining the performance throughout mission lifetime. Even though lifetime varies between different missions, satellite platforms are generally designed to operate five to fifteen years in space environment owing to extremely high cost of satellite launch operation. Additionaly, every electronic and mechanical part/equipment used on the satellite should have very small probability of failure due to impossibility of maintanance and repairability on the equipments once the satellite has been sent to its mission orbit. These inherent challanges of a space missions impose stringent requirements to spaceborne electronics design. In this chapter, receiver related design parameters will be identified and isolated from SAR System Parameters discussed in Section 2.2 and Section 2.3. Practical design implementation constraints will be discussed and elaborated. Several receiver design architectures will be examined and proposed receiver design architecture will be presented.

3.2 Design Parameters

Main purpose of all SAR system is the construct a high quality image of target area. As it is described in Section 2.2, range resolution and cross-range resolution are the two substantial parameters that requires utmost attention while designing the system. Equation 2.18 indicates the fact that only way to enhance range resolution is the increase signal bandwidth of the radar signal. On the other hand, cross-range resolution is directly proportional to real antenna aperture length used on satellite platform. Hence higher frequency of operation is preferred in order to reduce the real

antenna aperture length therefore enhancing the cross-range resolution. Eventually, increasing the resolution of the image provides higher number of cells that represents the image of the target. With higher number of cells, details of the reconstructed image can be increased. As latter mentioned in section 2.4, increasing the number of range and cross-range cells that represents the target area are not solely enough to construct high quality SAR image. Radar receiver should be able to identify and discriminate the incoming radar echo signals from noise levels. Higher received signal power with respect to noise power will result in higher quality representation of each range/cross-range cell. Equation 2.29 given in Section 2.4 represents the overall received SNR of the radar signal. As is evident from the equation, lower receiver noise temperature will increase the overall received SNR value. Therefore keeping noise figure of the receiver low, directly improves the SAR System performance.

3.2.1 Carrier frequency band

In the last ten years, various SAR satellite mission has been launched into space by agencies and ministries. SAR Satellites currently being flown has been given in Table 3.1 with their main characteristics and application areas. As it can be seen from list

Table 3.1 : Currently operational SAR satellites and main characteristics [19].

Mission	Agency,Country	Frequency Band	Application
ALOS-2	JAXA, Japan	L-Band	Land Monitoring
COSMO-Skymed	ASI/MoD, Italy	X-Band	Land Surface Topography
GF-3	Cresda, China	C-Band	Land Surface Topography
PAZ	CDTI, Spain	X-Band	High Res. Imagery
RADARSAT-2	CSA, Canada	C-Band	Enviromental Monitoring
Tandem-X	DLR, Germany	X-Band	High Res. Surface Imaging
TerraSAR-X	DLR, Germany	X-Band	High Res. Surface Imaging

of SAR Satellites, frequency band of operations are focused on L-Band, C-Band and X-Band. Due to enchanced cross-range resolution on higher frequency bands, X-Band is the preferred frequency spectrum for high resolution surface imaging applications. Therefore in the scope of this thesis, frequency band is selected between 7.6-8.4 GHz.

3.2.2 Bandwidth

Theoratically; there is no limitation for maximum bandwidth that can be used in a SAR System. However in practice, every electronic circuit has a limited frequency band of operation due to their physical structures, limitations of utilized semiconductor technology and size-weight-power(SWaP) requirements. Therefore minimum radar signal bandwidth design parameter is derived from range resolution requirement. In order to comply with a SAR system with 1m range resolution and 50° worst case wave incidence angle, minimum receiver signal bandwidth can be calculated using Equation 2.18:

$$BW = \frac{c}{2\delta r \sin(\gamma)} = \frac{3 * 10^8}{2\sin(50°)} \approx 196MHz. \tag{3.1}$$

Considering wave incidence angle of the SAR radar signal will be subjected to variations due to earth surface roughness and constant movement of the satellite, required minimum bandwidth should be expected to change accordingly. For this reason, %25 bandwidth tolerance has been added to minimum calculated receiver bandwidth of $196MHz$ to achieve final design parameter of $250MHz$.

3.2.3 Noise figure

The effect of noise is crucial to the performance of SAR receivers since the ratio of signal power to noise power ultimately determines the quality of the received signal. Noise power in a receiver could be introduced from the external environment through the receiving antenna or internally generated by the receiver circuitry however only internally generated noise powers will be taken into account throughout the thesis [20]. As received signal propagates through RF component chain, every active or passive electronic part increase the in-band noise power therefore reduces the SNR . It is important to design the receiver such a way that internally additive noise will be kept at minimum level. Noise figure of a cascade RF chain with number of N serial component can be generalized with following well-known formula [21] :

$$NF_{Cascade} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_N - 1}{\prod_{n=1}^{N} G_n} \tag{3.2}$$

where F_1 represents the losses before the first active element with gain, G_1 is the gain of the first amplifier in the RF chain. An example simplified block diagram has been given in Figure 3.1. RF input signals propagate through an amplifier, filter and a downconversion mixer respectively. Cascaded noise figure calculation of the front-end

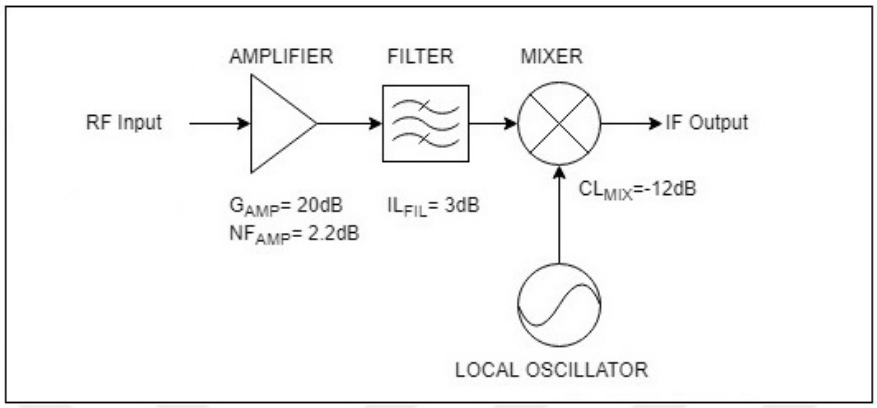


Figure 3.1 : Simplified block diagram of receiver front-end.

given in the Figure 3.1 can be calculated using Equation 3.2. Care must be taken to convert decibel values to linear representation for correct result.

$$NF_1 = 10^{(NF_{AMP}/10)} + \frac{10^{(IL_{FIL}/10)} - 1}{10^{(G_{AMP}/10)}} + \frac{10^{(CL_{MIX}/10)} - 1}{10^{(G_{AMP}/10)} 10^{(IL_{FIL}/10)}} \tag{3.3}$$

Inserting relevant gain and loss values to the equation will result in

$$NF_1 = 10^{(2.2/10)} + \frac{10^{(3/10)} - 1}{10^{(20/10)}} + \frac{10^{(12/10)} - 1}{10^{(20/10)} 10^{(3/10)}} \tag{3.4}$$

$$NF_1 \approx 1.66 + 0.01 + 0.2962 \approx 1.9662 = 2.936dB. \tag{3.5}$$

As it can be seen from the noise contribution of each stage given in the Equation 3.5, losses after amplification stage has very small effect on total noise figure. Furthermore, every lossy component before the amplification and noise figure of the amplifier directly accumulate which in turn greatly increase the noise figure of the receiver front end. If selected amplifier would provide 10db gain instead of 20dB, same calculation would yield a total cascaded noise figure of 6.741 dB which increase the former noise figure value by 3.805dB.

$$NF_2 \approx 1.66 + 0.1 + 2.962 \approx 4.722 = 6.741dB. \tag{3.6}$$

In conclusion, noise figure of a receiver front-end can be kept low by following two important design rules:

- Pre-amplification losses should be minimized.
- An amplifier with low noise figure and high gain should be utilized.

3.2.4 Dynamic range

As it is derived in Equation 2.28, received SAR echo signal power is directly proportional to radar cross section (σ) of the target area. However surface characteristics such as roughness, radar signal incidence angle and surface composition greatly alter the backscattering coefficient therefore received power level. SAR receiver should be able to differentiate and detect the signals with different power levels. Margin between maximum and minimum detectable signal levels is called *Dynamic Range* of the receiver [6]. Example spectrum representation of received radar echo signal is given in the Figure 3.2. Dynamic Range of SAR Receiver equipments

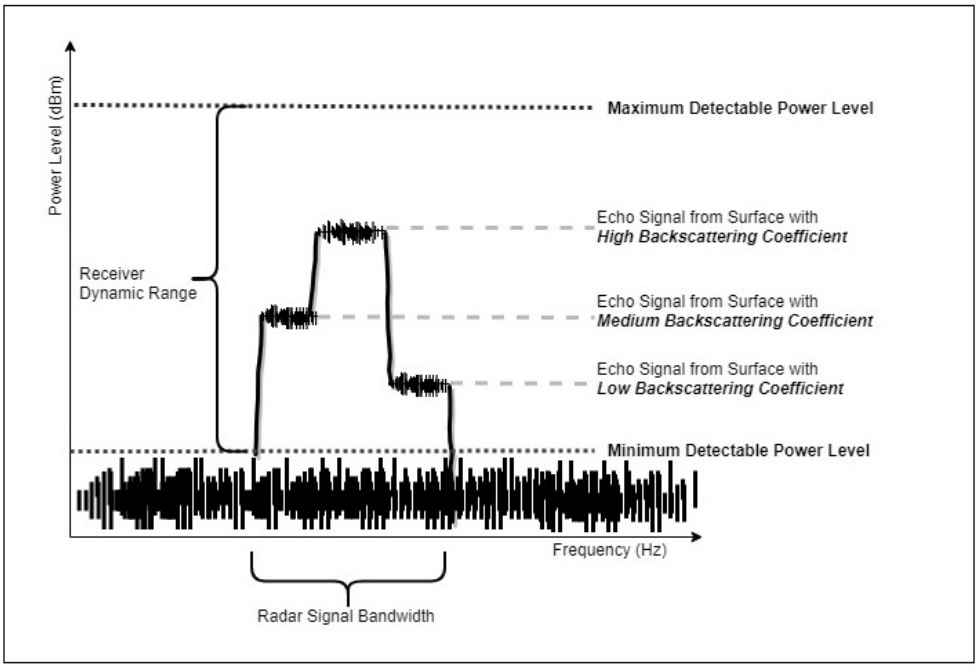


Figure 3.2 : Example backscattered radar signal spectrum.

are usually defined by performance of the digitizer section. RF/Microwave blocks of the receiver equipments aim to amplify and convert received signal to the proper level for digitization process which is accomplished by Analog-to-Digital Converters (ADC). RF or Analog signals are converted to sequence of bits according to the voltage level of the signal at the sampling instants. However there are limitations on the

minimum meaningful signal level for ADCs to distinguish signal from noise level. Minimum detectable signal level (MDS) at the input of an ADC is in fact the voltage required to assert least significant bit (LSB) of the ADC which can be calculated by

$$MDS(V) = \frac{ADC\ Full\ Scale(V_{pp})}{2^{Number\ of\ Bits}}. \tag{3.7}$$

Assuming 12-Bit ADC with $2V_{pp}$ full scale voltage, minimum detectable signal level is

$$MDS(V) = \frac{2}{2^{12}} = 0.000488V \tag{3.8}$$

which is equal to $-56.23\ dBm$ input power in a system with 50 ohm characteristic impedance. In this case, received echo signals should be amplified by RF/Microwave sections to higher level than $-56.23\ dBm$ otherwise signal discrimination from noise will not be possible. One possible method to reduce the minimum detectable power level by the digitization process is to utilize a analog-to-digital converter with higher number of bits. Higher number of bits provided by the ADC increases the resolution of the digital representation of the signal therefore results in lower minimum detectable power levels. ADC conversion visual representation in time domain with full-scale signal amplitude has been given in the Figure 3.3. In the event of signal reception

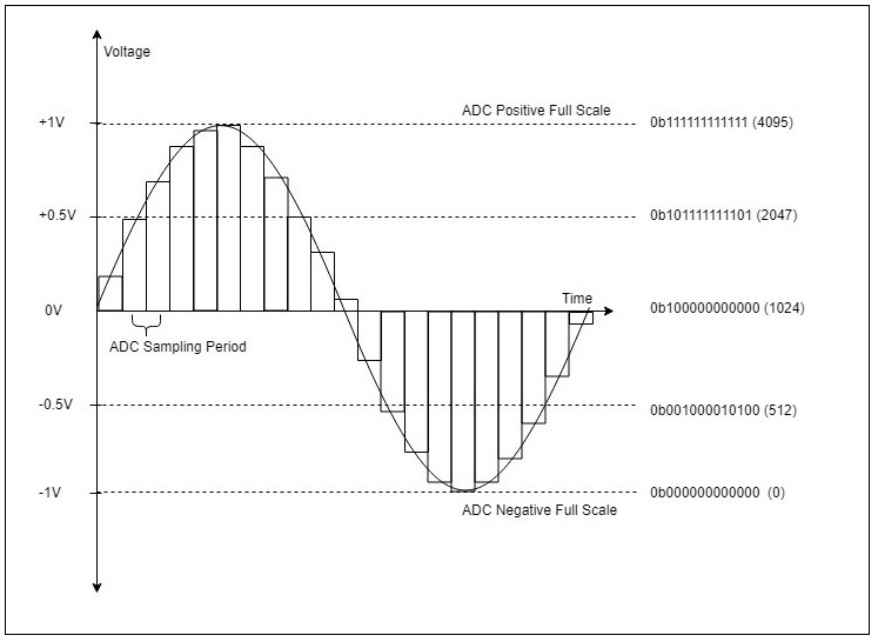


Figure 3.3 : Analog to digital domain conversion - Time domain representation.

with higher voltage level than ADC full scale limit, clipping of the signal occurs and

integrity of the received signal will be lost in the digitization process. Furthermore, signal saturation drives the ADC to non-linear operation region where it introduces harmonics and intermodulation products at the output. In order to avoid non-linearity related products, ADC should be driven in linear region where the voltage level of the received signal is lower than full-scale voltage range.Time domain representation of over-range scenario is shown in the Figure 3.4.

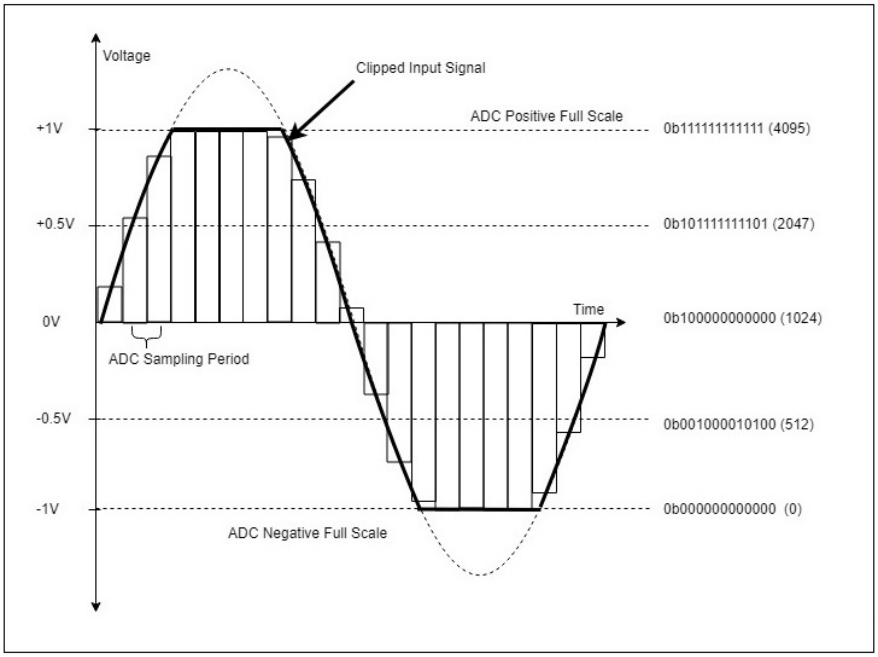


Figure 3.4 : ADC over-range scenario - Time domain representation.

3.2.5 Radiation effects

Electronics in space environment are constantly bombarded by radiated particles originated from cosmic rays, nuclear reactions on the surface of the Sun and entrapped electrons reside in Earth's magnetosphere [22]. These radiated particles possess different energy levels therefore effects caused by collision of the particles with semiconductor layers reside in electronics also depends on the characteristics and energy level of the interacted particles. Among every particle present in space environment; impact of electrons, photons, neutrons, protons and heavy ions on electronics are well documented and studied over the course of many years [23] [24]. Radiation effects on semiconductors are generally divided into three main categories:

- Total Ionizing Dose (TID)
- Single Event Effects (SEE)
- Displacement Damage (DD).

3.2.5.1 Total Ionizing Dose (TID)

Total ionizing dose (TID) is defined as the total amount of energy accumulated on semiconductors over time due to interaction of ionized particles with the substrates. Accumulated energy is highly dependent on the material, composition and geometrical structure of the semiconductor process. Most commonly used unit for the TID representation is 1 *rad* which is equal to 100 joule energy accumulation per kilogram on the effected semiconductor [22]. Energy transferred to the semiconductor by the impact of ionized particles generates new electron-hole pairs throughout the oxide substrate layer. As generated p-type or n-type carriers propogate along the semiconductor, positive or negative charge accumulates on oxide layer. In time, amount of accumulated trapped particles increases and deteriorates the performance of the semiconductor device [23]. How TID influences the device is depents on the physical structure and construction. MOSFETs generally exhibits reduction on gate threshold voltage (Vgs) and increase on the drain-source leakage current as total ionizing dose increases. As a result N-type of MOSFETs' becomes conductive even at zero gate bias voltage while P-types would require much larger turn-on voltage bias to switch from off state to on state. In silicon BJTs, TID increases the noise generated by the device and diminishes the current gain (β) of the transistors. Since current gain variations directly effect the operation of many integrated circuit, performance degradation becomes inevitable. On the other hand gallium-arsenide(GaAs) and silicon-germanium(SiGe) semiconductor technologies can withstand TID levels up to >1Mrad without any performance degradations.

3.2.5.2 Single event effects (SEE)

Single event phenomenas are instantenous disruptions on the semiconductor that could induce permanent(destructive) or temporary (non-destructive) damage to electronics. Highly energetic particles with large mass such as heavy ions, protons and neutrons

can transfer enough energy to circuit nodes to impair their operation conditions. Single event effects are categorized into Single Event Upset (SEU), Single Event Latch-Up (SEL), Single Event Transients (SET), Single Event Burn-Out (SEB) and Single Event Gate Rupture (SEGR). In case of Single Event Upset (SEU); particles collide with the memory section of the circuits and change the status of the stored bits. If induced charge by the particle impact generates a low impedance path on the semiconductor, current flow through the effected node rises which is called Single Event Latch-Up(SEL). Increased current consumption by particle strike may result in device failure due to elevation of the temperature along high current path. If particles hit to input-output circuitry of the device, abrupt voltage spikes and transients (SET) can occur on the voltage lines to temporarily disturb the data integrity. Single Event Burn-Out (SEB) and Gate Rupture (SEGR) effects are usually observed on high current devices. If perchance transfered energy by the particle impact shifts the bias condition of the high current device, resulting current induced avalanche effect could destroy the device [23].

3.2.5.3 Displacement Damage(DD)

In rare instances, high energy protons could knock-out an atom in semiconductor lattice from its original location. If displaced atom has absorbed enough energy from particle impact, it could also push other atoms back. Because of this chain reaction, lattice composition could be severely damaged. Empty locations left behind by displaced atoms generates new electron-hole pairs which in turn alters the minority and majority carrier distribution in the semiconductor [24].

3.2.5.4 Radiation hardness and assurance

As the physics behind radiation effects on electronics are examined and understood, various methods has been proposed to design and manufacture electronics parts with resistance to radiation. Radiation hardening endeavours can be summarized into three categories [23]:

- Radiation Hardness by Design (RHBD)
- Radiation Hardness by Process (RHBP)

- Radiation Hardness by Technology (RHBT)

Semiconductor technology and related material engineering is ever-evolving area of research and development. Technologies or parts nominated as a candidate for space applications should gone through related total dose and single event radiation tests to ensure proper operation in radiation environment [25].

4. RECEIVER DESIGN ARCHITECTURES

In Chapter 3, RF Front End related design parameters and space environment associated application considerations has been presented. Since every module and part used in system are closely interrelated, equipment level receiver design and architecture will be established prior to RF Front End design phase. Designed architecture should provide a solution for all electrical requirements such as input carrier frequency, signal bandwidth, dynamic range, interference rejection while maintaining robust and reliable implementation considering radiation hardness, reliability assurance, process and technology limitations. Taking account of their wide range of usage and adaptability to various design requirements, three different design architecture will be investigated in this chapter. Advantages and disadvantages of these receiver architectures will be discussed in following sections and proposed receiver design architecture will be presented.

- Super-Heterodyne Architecture
- Homodyne Architecture
- Direct RF Sampling Architecture [26].

4.1 Heterodyne Architecture

Invention of the Super-Heterodyne receiver can be traced back to the early 20th century [27]. Although electronics parts that have been used for implementation evolved drastically through time, main idea of operation is still same as of today. High frequency carrier signal is downconverted to lower intermediate frequency(IF) signal by mixing operation where it can be amplified, sampled and demodulated more easily. Number of frequency downconversion stages can be increased to improve spurious filtering of the receiver, enchance interference immunity characteristic and

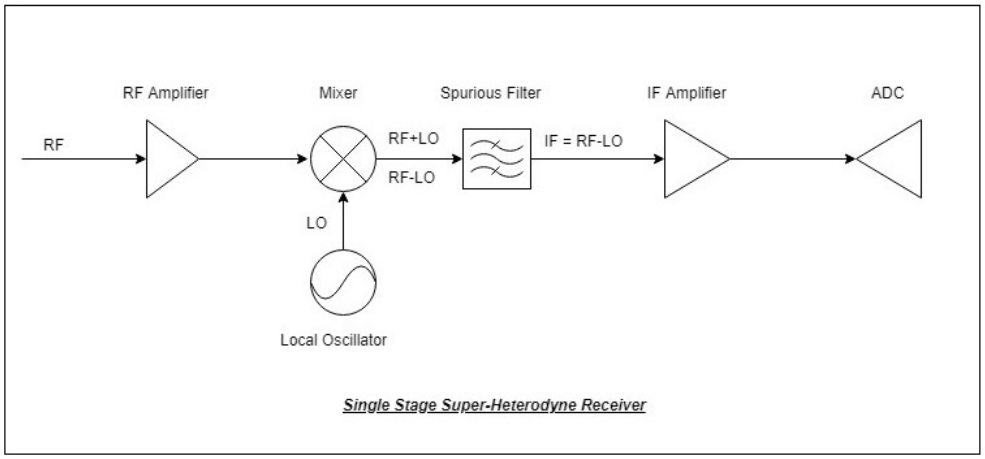


Figure 4.1 : Single stage Super-Heterodyne receiver block diagram.

provide wide-band coverage of RF input frequency. Generalized single stage and dual stage super-heterodyne receiver block diagram has been illustrated in Figure 4.1 and Figure 4.2 respectively. Super-Heterodyne architecture provides distinctive

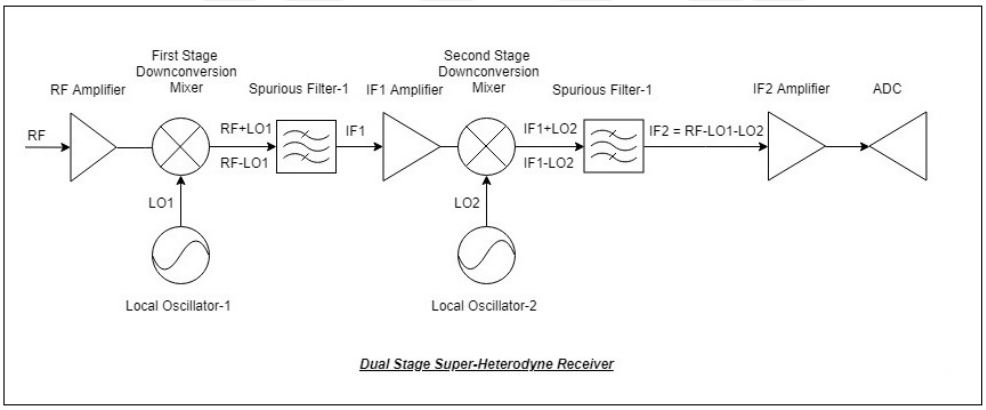


Figure 4.2 : Dual stage Super-Heterodyne receiver block diagram.

advantages on receiver implementation. Using fixed intermediate frequency (IF) allow the designed to use narrow-band filters compatible with signal bandwidth to reject unwanted signals efficiently. While keeping IF fixed, first stage local oscillator signal (LO1) can be designed to be tunable in certain frequency range to allow different RF input carrier frequency utilization with the same hardware. Higher number of stages allow designer to distribute signal amplification gain to different frequency bands which in turn prevents possible unwanted oscillation in the gain stages. Lowering the carrier frequency from microwave bands (X,Ku,Ka) to low frequency bands makes it possible to use lower cost analog-to-digital converters. Main disadvantage of the

super-heterodyne receiver is high component cost, implementation area and power consumption due to number of electronic parts used in implementation. On the other hand, care must be taken to filter out image frequency and image noise in each downconversion stage to prevent signal to noise degredation [28].

4.2 Homodyne (Zero-IF) Architecture

Homodyne receiver architecture downconverters the signal directly into baseband instead of lower intermediate frequency bands by choosing local oscillator (LO) frequency same as RF input carrier frequency. Utilization of quadrature mixer provides image rejection without any external filtering component. Resulting baseband signals are forwarded to digital conversion blocks using low-pass filters with cut-off frequency that is equal to half of the signal bandwidth since each in-phase and quadrature baseband components carries the half of the information. As an alternative to super-heterodyne architecture, homodyne receivers can remove high frequency image reject and spurious filters from the design consequently reduce the size, cost and power consumption of the receiver. Example simplified homodyne receiver block diagram has been illustrated in Figure 4.3. There are several drawbacks associated with

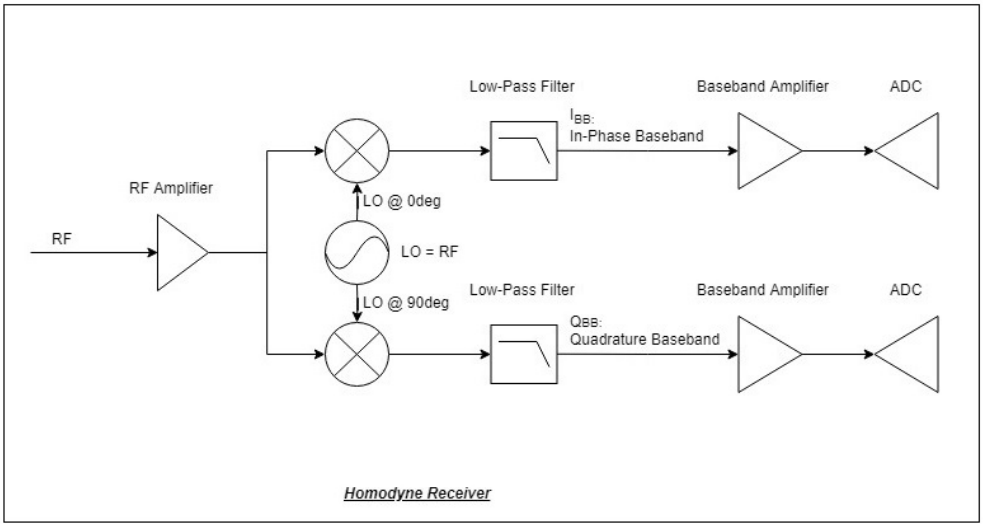


Figure 4.3 : Homodyne (Zero-IF) receiver block diagram.

homodyne architecture. Due to imperfection of downconversion mixers and reverse isolation limits of the amplifiers, small amount of synthesized LO signal leaks through input section of the receiver circuitry. Since LO frequency is at the same frequency of

RF input signal, leaked LO signal is amplified and feed back to downconversion stage therefore producing DC voltage product by self-mixing operation. On the other side, LO leakage could cause problems for surrounding equipments and systems if enough power can reach to receving antenna.

Image-rejection performance of the homodyne receivers are also highly dependent on phase and amplitude precision of the generated LO signals. As RF input signal frequency therefore LO frequency increases, phase and amplitude imbalance also increase on account of circuit parasitics and manufacturing variance of the electronic parts. Thus, homodyne architecture becomes impractical to use in high frequency applications.

4.3 Direct RF Sampling Architecture

Sampling speed and input signal bandwidth of the analog-to-digital converters (ADCs) has been constantly improving with the advancements in the semiconductor technologies. As of today, various part manufacturers can offer ADCs that can directly digitize RF signals up to C-Band. As it has been discussed in previous sections; main purpose of the downconversion stages shown in superheterodyne and homodyne architectures is to lower the carrier frequency to the appropriate range where ADCs can digitize the signal with high efficiencies. Utilization of RF ADCs into the system can eliminate the downconversion stages in receiver chain with direct digitization of signal in high frequency bands. As a result of this, number of components used in design can be reduced which in turn reduce the size, complexity and cost of the receiver. Simplified comparison of Direct RF Sampling Architecture with single stage super-heterodyne architecture has been illustrated in Figure 4.4. Although reduced part count brings enormous advantages to receiver design, there are several drawbacks associated with RF ADCs performance limitations while using Direct RF Sampling architecture. Investigation on electrical characteristics of RF ADCs offered in market shows the fact that dynamic range and minimum detectable input power level greatly diminishes as input RF frequency approaches the limit specifications. In order to meet with the receiver dynamic range requirements derived from system level demands, care

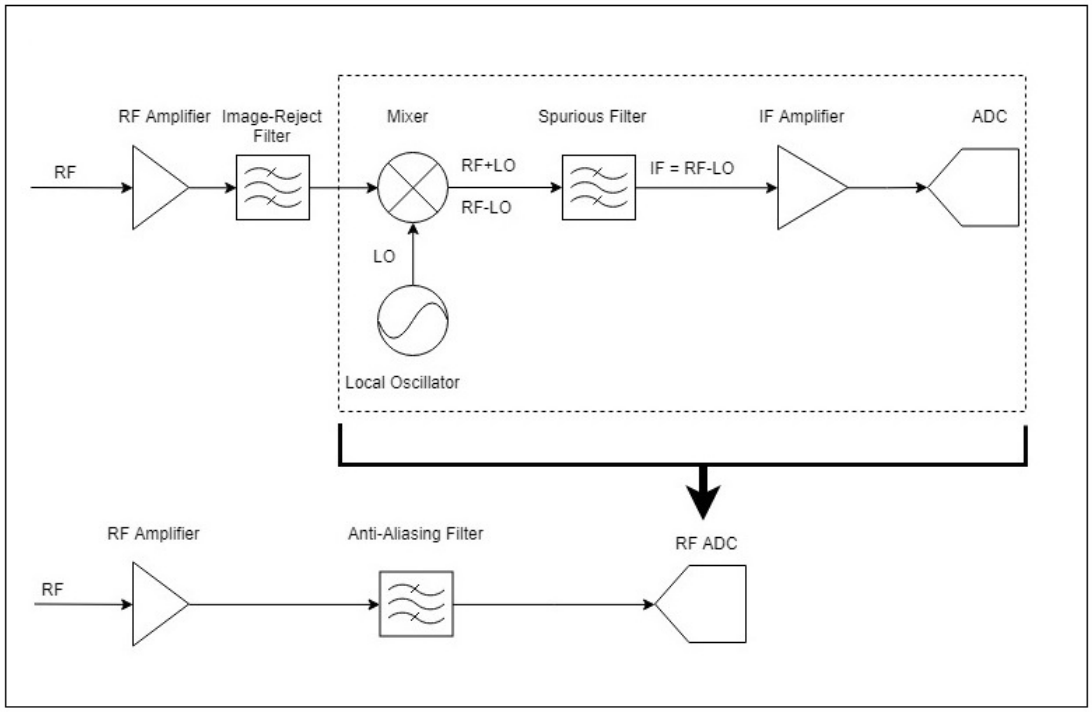


Figure 4.4 : Comparison of Direct RF Sampling and Super-Heterodyne receiver architectures.

must be taken to ensure utilized RF ADC can support necessery input power range at given RF input frequency.

Phase noise or jitter performance of local oscillator signal that is used on downconversion stage and sampling clock signal which is driven to analog to digital converter greatly effects the digitized signal quality. Integrated noise power caused by phase noise of the RF input signal and ADC sampling clock greatly escalates as their frequencies increase thus reducing SNR of the digitized signal. Therefore RF sampling ADCs generally offer better quantization and SNR performance with lower input carrier frequencies.

In conclusion; designing a X-Band SAR Receiver solely with Direct RF Sampling Architecture is not considered as the optimum solution due to aforementioned drawbacks summarized below:

- Maximum RF input frequency range of the currently offered space qualified ADCs on the market can not reach to X-Band frequencies.

- Dynamic range limitations of the ADCs while operating at high input frequencies directly dominates the receiver dynamic range performance and can not be improved by external design blocks.
- Reducing phase noise influence on received signal SNR impose significant challanges in implementation.

4.4 Proposed Receiver Design Architecture

Examination of most widely used receiver architectures clearly shows that each architecture has their strengths and weaknesses in different aspects. Apart from electrical performance considerations such as input frequency band, receiver dynamic range, signal bandwidth and phase noise; restrictions imposed by space environment should also be taken into account while designing spaceborne electronics. Radiation hardness and reliability assurance requirements limits the number of parts and technologies that can be used in spaceborne applications. Evaluating all of these factors; a mixed approach of combining superheterodyne and RF sampling architecture deemed suitable for SAR Spaceborne Receiver with electrical and product assurance requirements given in Table 4.1. X-Band input frequency range of the receiver

Table 4.1 : X-Band SAR receiver electrical and product assurance requirements.

Parameter	Value	Unit
Input Frequency Range	7500-8500	MHz
Signal Bandwidth	250	MHz
RF Input Power	-120 to -80	dBm
Noise Figure	< 4	dB
Dynamic Range	> 40	dB
Spurious Leakage	< -60	dBm
Image Rejection	> 40	dB
Interference Rejection	> 20 @ $f_c \pm 250$MHz	dBc
Operating Temperature	-20 deg to 60 deg	C
Radiation Hardness	> 50	krad
Lifetime	10	years

prohibits direct RF sampling due to RF ADC performance limitations on the space qualified RF analog-to-digital converters currently offered by parts manufacturers [29] [30] [31]. On the other hand; local oscillator leakage, image rejection performance

and minimum RF input power requirements impose significant design challanges with direct conversion due to inherent drawbacks of the architecture. Although downconversion of the input signal to lower frequency range may improve leakage suppresion and image rejection of the receiver, frequency spacing between the RF and local oscillator (LO) signals should be chosen adequately distant to each other where practical image-reject filters will be able to satisfy required suppresion performance. Downconversion to lower S-Band provides several significant advantages. Distance between RF and LO signal ease the image-reject filter design. Narrow-band surface acoustic wave (SAW) filters with low insertion losses can be utilized in IF section for superior signal selectivity which provide sharp filtering of mixing products, unwanted interferences and anti-alias frequencies [32] [33] [34] [35].. On the other hand; reducing the carrier frequency to lower S-Band makes employing a RF ADC possible where signal can be directly digitized without any SNR degradation therefore eliminating second downconversion section entirely. Proposed SAR receiver design architecture has been presented in Figure 4.5. As stated in Section 3.2.3, placement

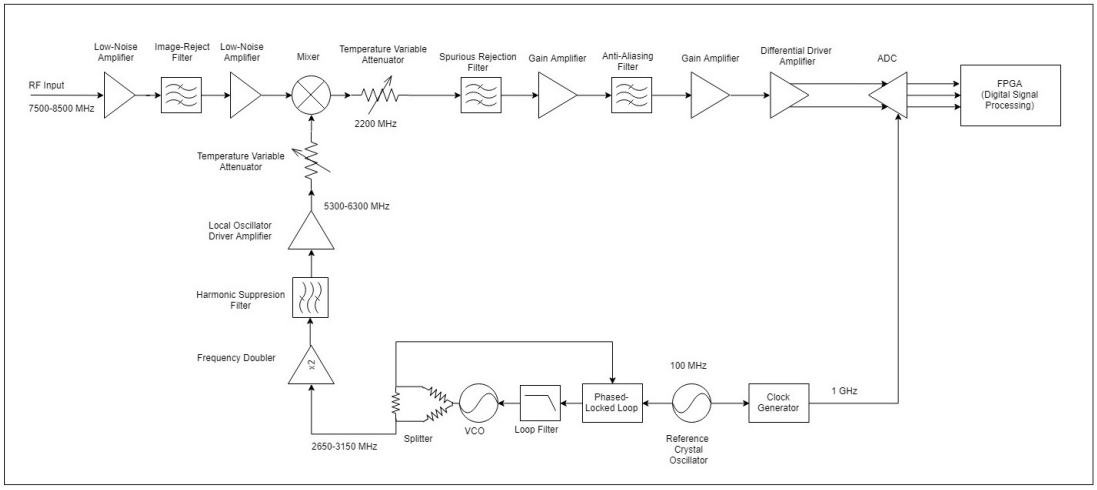


Figure 4.5 : Proposed SAR receiver design architecture.

of low-noise amplifier (LNA) with high gain and noise factor as a first component in RF chain ensures low cascaded noise figure performance. Image-reject filter utilization before downconversion mixer provides supression of image noise and improve selectivity of the RF front-end. Temperature variable attenuator (TVA) is placed at the output of mixer to eliminate temperature related gain variance of RF Front-End

chain [32]. C-Band local oscillator (LO) carrier required for downconversion operation is synthesized by multiplication of the S-Band signal produced by phased locked-loop (PLL) and VCO configuration. Harmonic suppresion filter is employed to suppress unwanted fundamental and harmonic signal produced by frequency multiplication operation. Multiplied LO signal is amplified to required power level where mixer can downconvert the RF signal with low conversion loss. LO output power variation due to temperature changes is reduced by utilizing second TVA at the end of LO synthesis chain. Surface acoustic wave (SAW) filters with pass-band of 250MHz provides spurious and anti-aliasing filtering functions. Gain and differential driver amplifiers provides signal amplification and single ended to differential conversion respectively in order to reach full-scale input power level of the ADC to benefit from maximum attainable SNR from analog-to-digital conversion. Due to the fact that signal bandwidth of 250 MHz requires minimum 500Mpbs sampling rate for data sampling in order to avoid loss of information, sampling rate of 1 GHz is selected to benefit from oversampling gain [36].

5. SAR RECEIVER RF CHAIN ANALYSIS

System level analyses and simulations provide an effective way to observe electrical parameters and performance of the designed architecture before detailed design stage. Crucial performance metrics such as gain budget, noise figure, linear operation range and spurious response can be easily examined to see if they indeed satisfy the target performance specifications. Embedding real electrical characteristics of selected parts to analysis environment produces realistic analysis results which could prevent multiple design iterations in advance. In this chapter; system level RF chain analysis of SAR receiver architecture proposed in Section 4.4 will be investigated in detail. Part selection methodology and performed design iterations will be presented with their justifications in accordance to results gathered by simulation steps.

5.1 Part Selection

5.1.1 Low noise amplifier (LNA)

Low noise amplifier plays an important role on receiver chain due to its dominant effect on cascaded noise figure. Design or implementation of LNA should provide high gain with low noise factor in order to reduce the cascaded noise figure of the receiver. Due to its excellent noise figure, small signal gain and gain flatness performance, GaAs (Gallium-Arsenide) MMIC (Monolithic Microwave Integrated Circuit) technology is chosen for LNA block implementation. Although GaAs technology provides inherent radiation tolerance, reliability concerns restrict the number of suitable parts and foundaries for space applications. Therefore, required LNA part is chosen from European Space Agency (ESA) approved UMS *PH*25 *Low Noise pHEMT* process [37]. Schematic diagram and electrical characteristics of selected low noise amplifier within 7500-8500 MHz input frequency range are given in Figure 5.1 and Table 5.1 respectively. As it can be seen from electrical characteristics, chosen LNA can provide

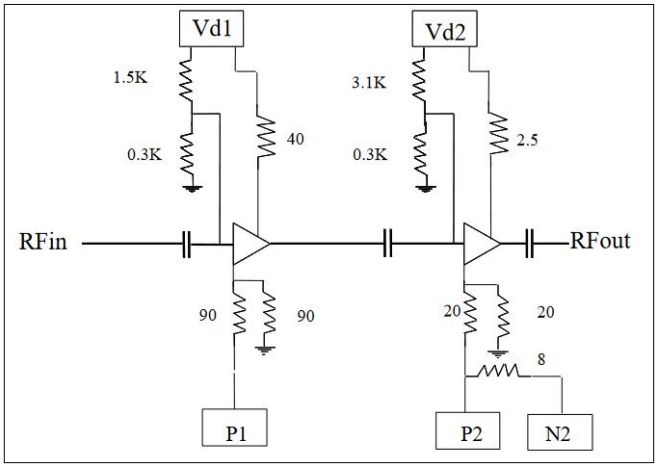


Figure 5.1 : X-Band LNA schematic diagram.

higher than 20 dB gain with less than 1.5 dB noise figure due to GaAs pHEMT process with more than 90 GHz transition frequency.

Table 5.1 : X-Band LNA electrical characteristics.

Symbol	Parameter	Value	Unit
G	Gain	22.2	dB
G	Gain Flatness	$\pm$ 0.05	dB
NF	Noise Figure	<1.5	dB
S11	Input Return Loss	<-8	dB
S22	Output Return Loss	<-12	dB
P1dB	Output Power @ 1dB Compression	>17,5	dBm
Vdd	Drain Bias Voltage	4	V
Id	Drain Bias Current	80	mA

5.1.2 Downconversion mixer (MIX)

Converting X-Band RF input signal to S-Band IF signal can be accomplished with frequency mixers. However due to their non-linear and non-ideal characteristics, frequency mixers generate various unwanted harmonics apart from target IF frequency. Output spectrum of a generic RF mixer consists of sum and difference of input frequencies and their harmonics which can be shown as;

$$f_{output} = \pm N \cdot RF \pm M \cdot LO \; where \; N : M \in \mathbb{Z} \tag{5.1}$$

where N and M are integer multipliers that represent harmonic order of RF and LO frequencies. Example representation of downconversion mixer output spectrum is

illustrated in Figure 5.2 where RF and LO frequencies are 8000 and 5800 MHz respectively. Lower levels of intermodulation products generated by mixing operation

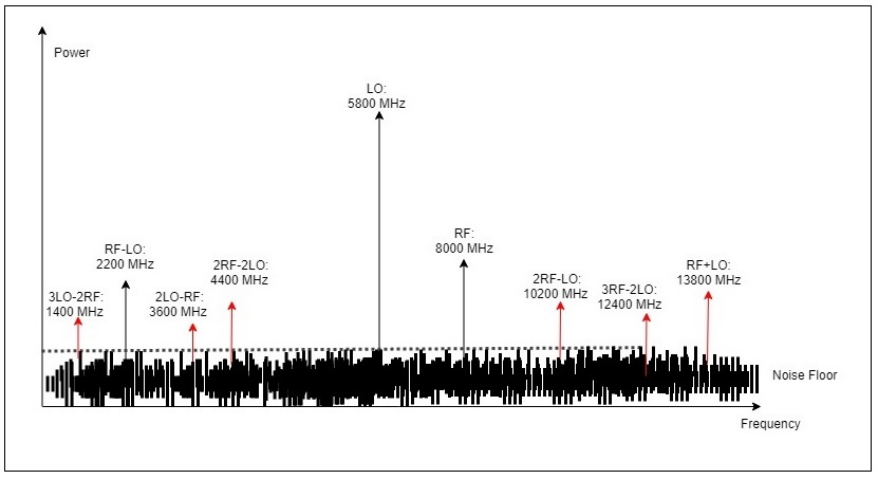


Figure 5.2 : Mixer output spectrum example.

results in lower filtering requirements on consequtive RF stages to filter out unwanted frequencies. However, power level of the unwanted intermodulation products highly depends on design topology of the mixer. Several commonly used RF/Microwave mixer architectures are;

- Single Ended Mixer
- Balanced Mixer
- Double Balanced Mixer

Each mixer type has their advantages and disadvantages in comparison with each other. In order to select most suitable mixer for design, their strengths and weaknesses should be taken into consideration depending on the desired application requirements.

5.1.2.1 Single ended mixer

Single ended mixers are considered as simpliest mixer type that consist of a diplexer circuit, single non-linear RF element such as diode or field effect transistor(FET) and low-pass filter [38]. Diplexer circuit is used to combine RF and LO signal inputs and provide isolation between RF and LO ports. If the power level of the combined signal is high enough to drive diode/FET to their non-linear operating region, desired mixing

outputs can be observed at the output of the non-linear element. Low-pass filter is used to suppress unwanted higher order spurious output signals at IF output. Required LO signal power depends on forward voltage for the diodes and turn-on voltage for FETs. However this dependency could be eliminated by DC biasing method which also reduces the required LO signal power. In case of diode mixers, biasing the diode close to their forward voltage results in on/off action with smaller LO swings. Same approach can be used for FET mixers with biasing gate voltage of the mixer FET close to turn-on voltage. Simplified single ended diode and FET mixer circuit schematics are illustrated in Figure 5.3 and Figure 5.4 respectively. Main advantage of single ended

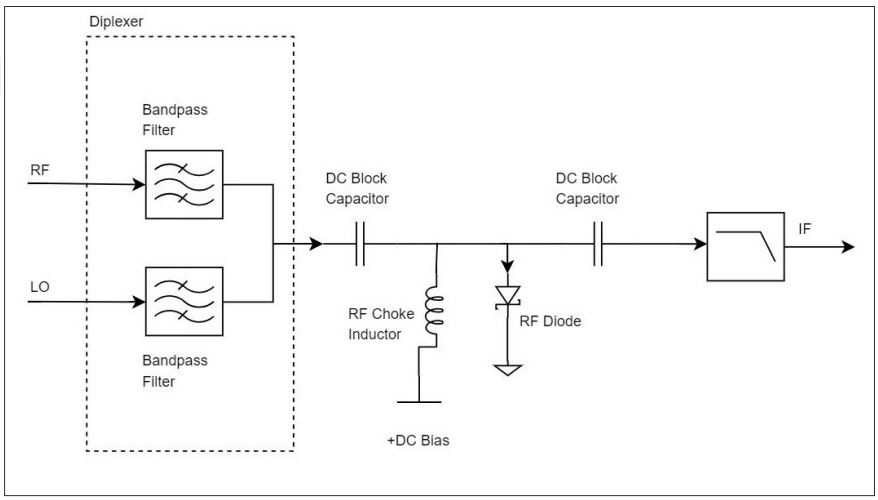


Figure 5.3 : Single-ended diode mixer circuit.

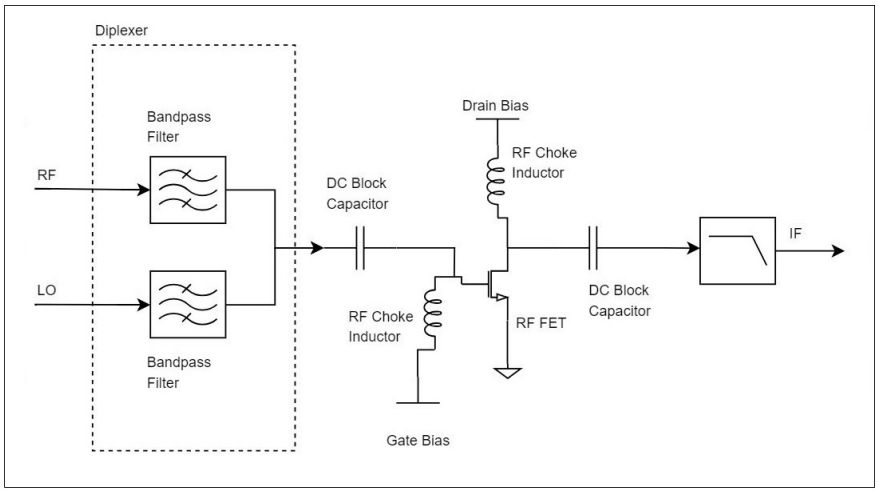


Figure 5.4 : Single-ended FET mixer circuit.

mixers that they can provide low cost solutions due to small number of parts used in

the design. However signal isolation between RF and LO port is directly dependent on performance of the diplexer which innately becomes smaller as RF and LO frequencies get closer to each other in spectrum. Another crucial drawback of single ended mixers is their input and output matching becomes troublesome for wideband applications due to large impedance variations of non-linear diodes and FETs with changing RF/LO frequencies.

5.1.2.2 Balanced mixer

Balanced mixer architecture consists of a 90° or 180° hybrid coupler, two RF diodes and IF filter [38]. Replacement of diplexer with a hybrid coupler inherently isolates the RF and LO ports thus improves the isolation between the ports while eliminating bandpass filters at the RF and LO inputs. Input signals divided by hybrid coupler drives anti-paralel diodes to generate mixing products. Simplified balanced diode mixer circuit schematic is illustrated in Figure 5.5. Hybrid coupler also provides

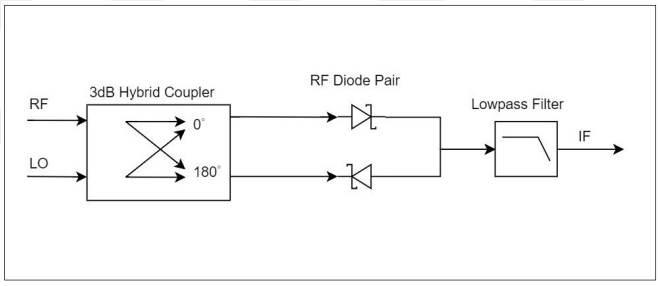


Figure 5.5 : Balanced diode mixer schematic.

even-order RF or LO intermodulation suppression at the IF output based on selected port configuration. Considering 180° hybrid coupler symbol representation given in Figure 5.6, signal fed to Port 1 will be equally divided in-phase between Port 2 and Port 3. However; if signal is fed to Port 4, outputs will still have equal powers but 180° phase difference. Single ended to balanced conversion provides suppression of even-order mixer intermodulation products of balanced input signal. Recalling Equation 5.1, two possible set of spurious frequencies can be eliminated. In case of RF signal is used to drive port 1, intermodulation products with even harmonics of LO signal which is given in Equation 5.2 ($RF \pm 2LO, RF \pm 4LO, ...$) will be suppressed.

$$f_{supressed} = \pm N \cdot RF \pm M \cdot LO \; where \; M = 2k \; \& \; k \in \mathbb{Z} \tag{5.2}$$

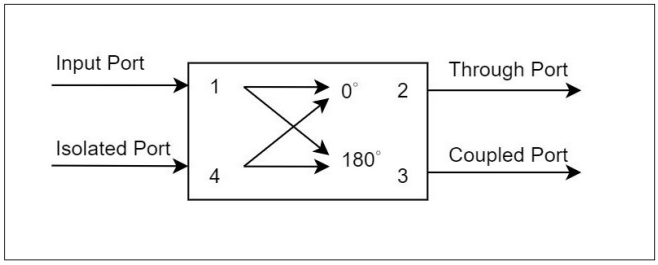


Figure 5.6 : 180° Hybrid coupler symbol.

On the other hand; if LO signal is fed to port 1, intermodulation products with even harmonics of RF signal which is given in Equation 5.3 ($LO \pm 2RF, LO \pm 4RF, ...$) will be seen suppressed at the output of the mixer.

$$f_{supressed} = \pm N \cdot RF \pm M \cdot LO \; where \; N = 2k \; \& \; k \in \mathbb{Z} \tag{5.3}$$

5.1.2.3 Double balanced mixer

Double balanced mixer architecture consist of two baluns, four non-linear element (Diode,FET) and IF filter. Baluns used in the design provides single ended to balanced signal conversion for RF and LO signals which results in even order intermodulation products suppresion of both RF and LO signals at the mixer output. Since RF and LO paths are blocked by non-linear elements, double balanced mixers provide inherent RF-LO isolation. Furthermore, baluns placed at RF and LO ports ensure broadband matching for wide-band applications [38]. Simplified double balanced diode mixer circuit schematic is illustrated in Figure 5.7. There are several drawbacks associated

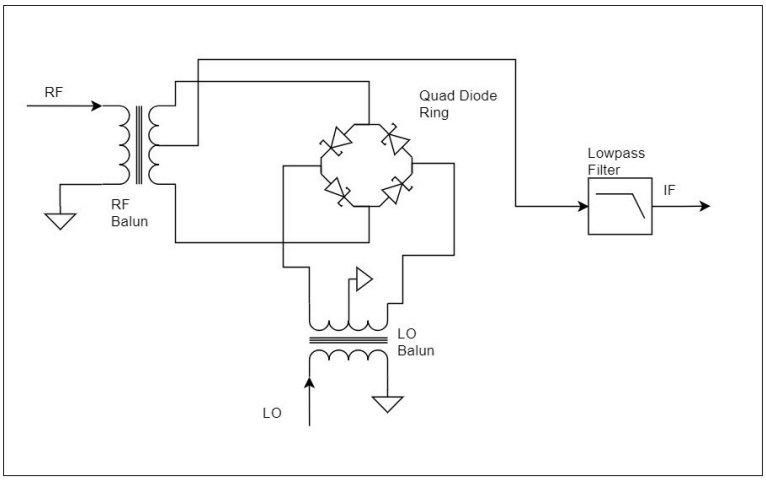


Figure 5.7 : Double balanced diode mixer schematic.

with double balanced mixer topology. Any parameter difference of non-linear elements used in ring configuration diminishs the intermodulation suppresion and RF-LO isolation performance of the mixer. Although it produce significant challenge in discrete designs where diodes are seperately packaged and placed on the circuit, utilization of monolithic processes used in MMICs drastically reduce the parameter variations of the non-linear elements therefore eliminate performance reduction. Secondly, double balanced mixer circuits requires 3dB more local oscillator signal power in comparison with single or balanced mixer circuits with identical non-linear diodes/FET since LO drives two sequential non-linear element instead of one. Examination of three different mixer architecture reveals the fact that double-balanced GaAs MMIC mixers exhibit superior intermodulation suppression and port isolation while providing inherent radiation hardness with only 3dB more LO signal power requirement. Therefore decided as optimum solution for spaceborn SAR front-end applications. Electrical parameters of selected space qualifiable mixer part within 7500-8500 MHz RF frequency range and 5500-6500 MHz LO frequency range are listed in Table 5.2 [39].

Table 5.2 : Mixer electrical characteristics.

Symbol	Parameter	Value	Unit
LO_{Power}	LO Drive Level	+13	dBm
CL	Conversion Loss	7	dB
NF	Noise Figure	<7	dB
LO-RF	LO-RF Isolation	<45	dB
LO-IF	LO-IF Isolation	<32	dB
RF-IF	RF-IF Isolation	<18	dB
IRL (RF)	RF Input Return Loss	<-8	dB
ORL (IF)	IF Output Return Loss	<-14	dB

5.1.3 Image reject filter (IRF)

As it can be derived from Equation 5.1, there are two frequency band which could fall into desired IF frequency; $LO+IF$ and $LO-IF$. Based on frequency planning scheme, one of the two frequencies becomes *Image Frequency* that will degrade signal quality in case of interference or increase the noise floor in the IF band at the output of mixer. Therefore filtering image frequency improves the total noise figure

and improves interference immunity of the receiver front-end. Distributed element filter with microstrip implementation is chosen as the optimum design solution for required image reject filter due to their convenience on circuit integration and flexible customization. Target electrical specification of the image reject filter that can satisfy receiver requirements is given in Table 5.3.

Table 5.3 : Image reject filter electrical characteristics.

Symbol	Parameter	Value	Unit
f_c	Center Frequency	8000	MHz
BW_{1dB}	1dB Bandwidth	>1000	MHz
IL	Insertion Loss	<2	dB
IRL	Input Return Loss	<-10	dB
ORL	Output Return Loss	<-10	dB
IR	Image Rejection	>50 @ LO-IF	dBc

5.1.4 Local oscillator (LO)

Local oscillator synthesis block generates the LO signal required for downconversion of received RF signal to lower intermediate frequency. Frequency stability and phase noise performance of the LO signal have considerable impact on receiver performance. Frequency offset carried by local oscillator signal directly shifts the downconverted intermediate frequency with the same amount. Moreover, phase noise of the LO signal and RF signal accumulate with each other while producing IF frequency at the mixing stage which ultimately degrades the signal-to-noise ratio of the received signal. Power level of the LO signal also should be considered and amplified to optimum level defined by electrical characteristics of downconversion mixer. Inadequate output power of local oscillator chain will increase the conversion loss of the mixer therefore reduce overall gain of the RF signal path of the receiver. In case of superheterodyne receiver architecture with wide input frequency range, local oscillator synthesis should provide tunable output frequency to keep intermediate frequency fixed. Otherwise received signal will be shifted out of passband range of IF filter and suppressed at the IF signal chain. There are several methods to synthesize tunable local oscillator frequency with low phase noise and high frequency stability. Dielectric resonator oscillators (DROs) are one of the mostly used type of microwave oscillators which

consists of a negative resistance microwave device and a dielectric puck with very high dielectric constant. Coupling between microstrip line and dielectric material creates resonance frequency and generates oscillation when combined with negative resistance circuit. Schematic representation of dielectric resonator oscillator is illustriated in Figure 5.8. DROs provides best phase noise performance and lowest cost among

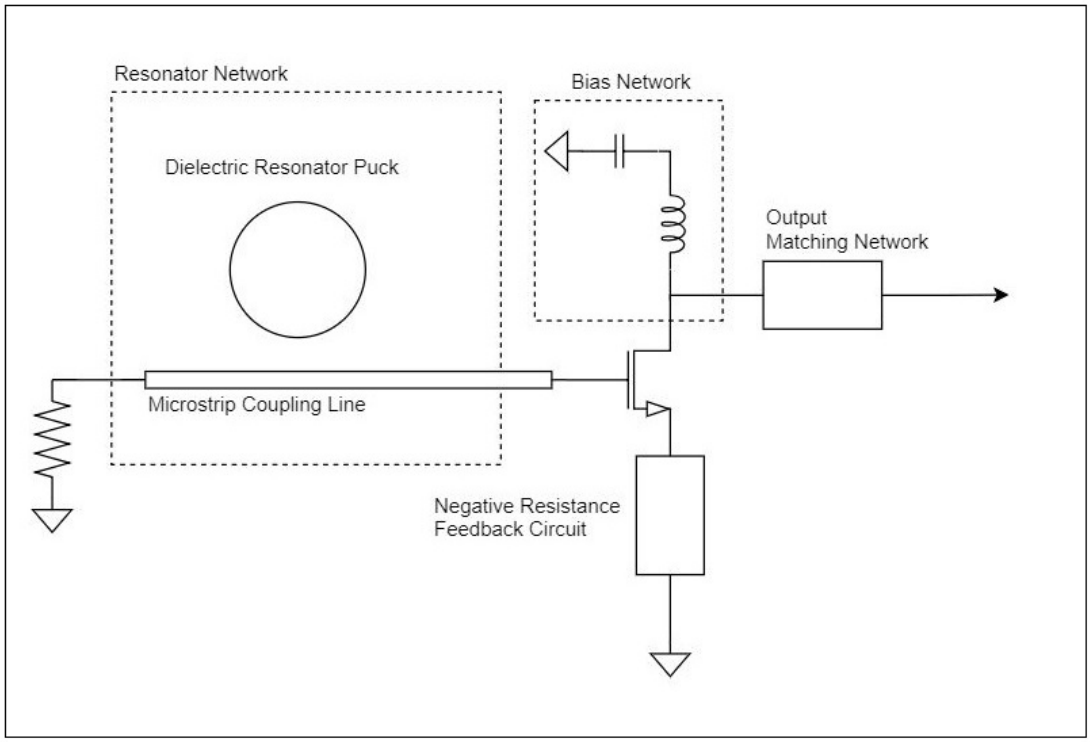


Figure 5.8 : Dielectric resonator oscillator schematic.

other LO synthesis methods however their frequency tuning range is usually limited within %1 of local oscillator frequency which inhibits their usage on receivers with wide RF input frequency range. Voltage controlled microwave oscillators (VCOs) on the other hand which consist of microwave negative resistance device, varactor diode, resonator and bias network can reach up to %85 tuning range. Even though discrete VCO design methodologies has limitations on achievable maximum output frequency due to intrinsic parasitics associated with packages and interconnection of utilized parts, monolithic designs are able to reach up to 80 GHz. Main disadvantage of the voltage controlled oscillators are their poor phase noise performance if they are left in free-running oscillation condition. However phased-locked-loops (PLLs) with very low noise reference oscillators can be used to improve frequency stability and

phase noise performance of the voltage controlled microwave oscillators. Schematic representation of colpitts type voltage controlled oscillator is illustriated in Figure 5.9. In order to generate local oscillator frequency in the range of 5500-6500 MHz

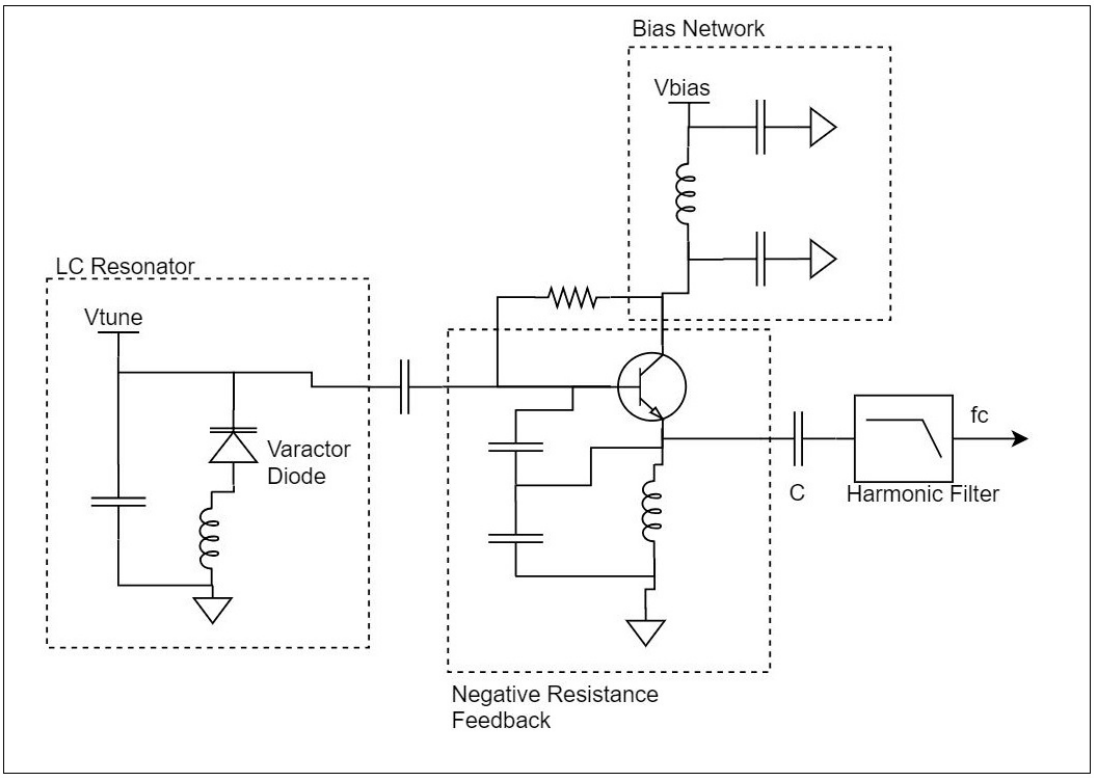


Figure 5.9 : Colpitts voltage controlled oscillator schematic.

with low phase noise, high frequency stability; employing tunable VCO phased locked to reference oscillator via PLL circuitry has been found as optimum solution for proposed SAR receiver application. Fractional-N type frequency synthesizer designed on radiation tolerant silicon-on-insulator (SOI) process has been selected due to the fact that it allows frequency tuning with small frequency increments due to fractional division operation and provides immunity to TID and SEE effects [40] [41] [42]. Functional block diagram and electrical parameters of selected SOI frequency synthesizer part are given in Figure 5.10 and Table 5.4 respectively.

As it can be seen in Table 5.4, maximum RF frequency range of the synthesizer limits the local oscillator frequency directly synthesizable by VCO+PLL pair to 5 GHz. Therefore, frequency multiplication approach has been deemed suitable to reach targeted 5500-6500 MHz LO frequency range which is required for downconversion of

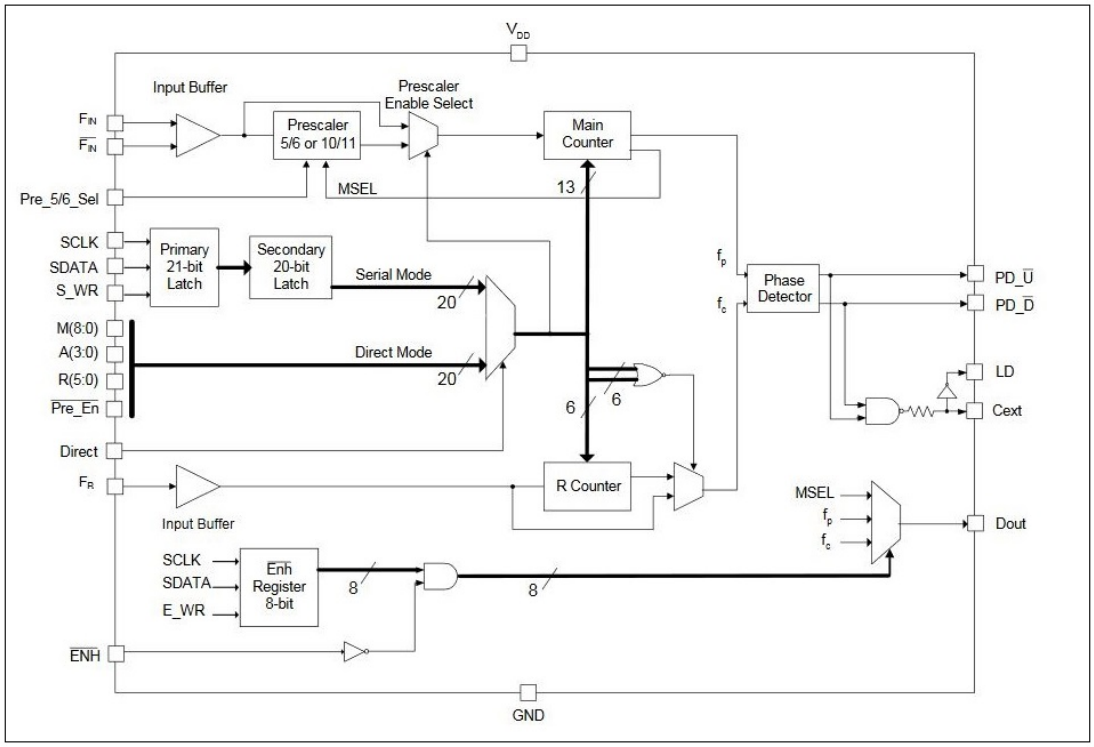


Figure 5.10 : Fractional-N PLL functional block diagram.

X-Band input RF signal to S-Band intermediate frequency. VCO in phase locked loop is used to generate LO signal between 2750-3250 MHz which is multiplied by two with frequency multiplier. Unwanted fundamental and harmonic products are filtered out with bandpass filter placed at the output of frequency doubler. Multiplied local oscillator signal is amplified to power level required for downconversion mixer for optimum conversion loss performance.

Table 5.4 : Radiation hardened PLL electrical characteristics.

Symbol	Parameter	Value	Unit
F_{IN}	Maximum RF Frequency	5	GHz
F_{REF}	Maximum Reference Frequency	100	MHz
PN	SSB Phase Noise	<-110 @ 1 kHz	dBc/Hz
FOM	Figure of Merit	<-227	dBc/Hz
TID	Total Ionizing Dose Tolerance	<100	kRad
Vdd	Supply Voltage	<2.8	V
Idd	Supply Voltage	<80	mA

Due to lack of suitable space qualified frequency doubler parts offered by the manufacturers, frequency multiplier is decided to be designed by discrete hybrid

process. On the other hand, distributed element filter with microstrip implementation is chosen as the optimum design solution for required harmonic suppresion filter due to their convenience on circuit integration and flexible customization. Target frequency multiplier and harmonic suppresion filter specifications are listed in Table 5.5 and Table 5.6 respectively.

Table 5.5 : Target electrical characteristics of frequency doubler.

Symbol	Parameter	Value	Unit
Pin	Input RF Drive Level	<4	dBm
CG	Conversion Gain	>0	dB
CGF	Conversion Gain Flatness	$<\pm$ 1	dB
S11	Input Return Loss	<-10	dB
S22	Output Return Loss	<-10	dB
P_{F0}	Fundamental Suppresion	>20	dBc
P_{F3}	Third Order Suppresion	>20	dBc
Vdd	Drain Bias Voltage	4	V
Id	Drain Bias Current	<30	mA

Table 5.6 : Target electrical specification of harmonic supression filter.

Symbol	Parameter	Value	Unit
f_c	Center Frequency	6000	MHz
BW_{3dB}	3dB Bandwidth	>1200	MHz
IL	Insertion Loss	<3	dB
IRL	Input Return Loss	<-10	dB
ORL	Output Return Loss	<-10	dB
-	Fundamental Suppresion	>30	dBc
-	3rd Order Harmonic Suppresion	>20	dBc

5.1.5 Intermediate frequency filter (IFF)

Intermediate frequency filter is placed after downconversion stage to remove unwanted spurious products originated from mixing operation and filter out interference signals which possibly coupled to receiver input from external sources and propagate through RF chain. Since the frequency is much smaller in comparison with RF and LO frequencies, distributed element microstrip filter size increases proportional to increased wavelength of the passband signal. On the other hand, S-band range allows selection of ceramic and SAW filters for intermediate frequency filtering that offer very high close band rejection ratios and narrow bandwidths with small form

factors. Although SAW filters exhibit smaller size and weight due to their monolithic construction, procurement of a space qualified SAW filter with $\approx$ %15 passband becomes challanging. Therefore ceramic filter with electric characteristics listed in Table 5.7 is chosen as IF filter.

Table 5.7 : Electrical specification of intermediate frequency filter.

Symbol	Parameter	Value	Unit
f_c	Center Frequency	2200	MHz
BW_{3dB}	3dB Bandwidth	>275	MHz
IL	Insertion Loss	<1.4	dB
IRL	Input Return Loss	<-10	dB
ORL	Output Return Loss	<-10	dB
-	Stopband Attenuation @ 1800MHz	>35	dBc
-	Stopband Attenuation @ 2600MHz	>35	dBc

5.1.6 Intermediate frequency amplifier (IF-AMP)

Intermediate frequency amplifiers provide necessary gain to increase power level of received signal in order to reach dynamic range of analog-to-digital converter. Due to high reliability and intrinsic radiation hardness, hermetically sealed LTCC amplifier manufactured with monolithic InGaP HBT process has been selected as intermediate frequency amplifier. Since selected IF-AMP provides near perfect input and output matching at S-Band frequency range, no external matching circuits is required for proper operation. Electrical characteristics of selected IF-AMP at 2200 MHz input frequency are given in Table 5.8.

Table 5.8 : Intermediate frequency amplifier electrical characteristics.

Symbol	Parameter	Value	Unit
G	Gain	20.2	dB
GF	Gain Flatness	$\pm$ 0.2	dB
NF	Noise Figure	<4	dB
S11	Input Return Loss	<-20	dB
S22	Output Return Loss	<-20	dB
P1dB	Output Power @ 1dB Gain Compression	>18	dBm
IP3	Third-Order Intercept Point	>32	dBm
Vdd	Drain Bias Voltage	5	V
Id	Drain Bias Current	71	mA

5.1.7 RF analog-to-digital converter (RF-ADC)

Analog-to-Digital converter concludes the receiver chain by converting amplified and downconverted input signal to digital domain for further processing of received data. As semiconductor process technologies advanced through time, sampling speed and input frequency range of the ADCs increased dramatically. Taking advantage of 28nm CMOS and SiGe BiCMOS technologies, current ADCs can support sampling speed up to 10 GSPS and input bandwidths that can cover up to C-Band. Space grade RF analog-to-digital converter from Teledyne E2V is chosen for direct sampling of S-Band IF signal. Functional block diagram and electrical characteristics of selected RF-ADC are given in Figure 5.11 and Table 5.9 respectively. 12-Bit conversion resolution

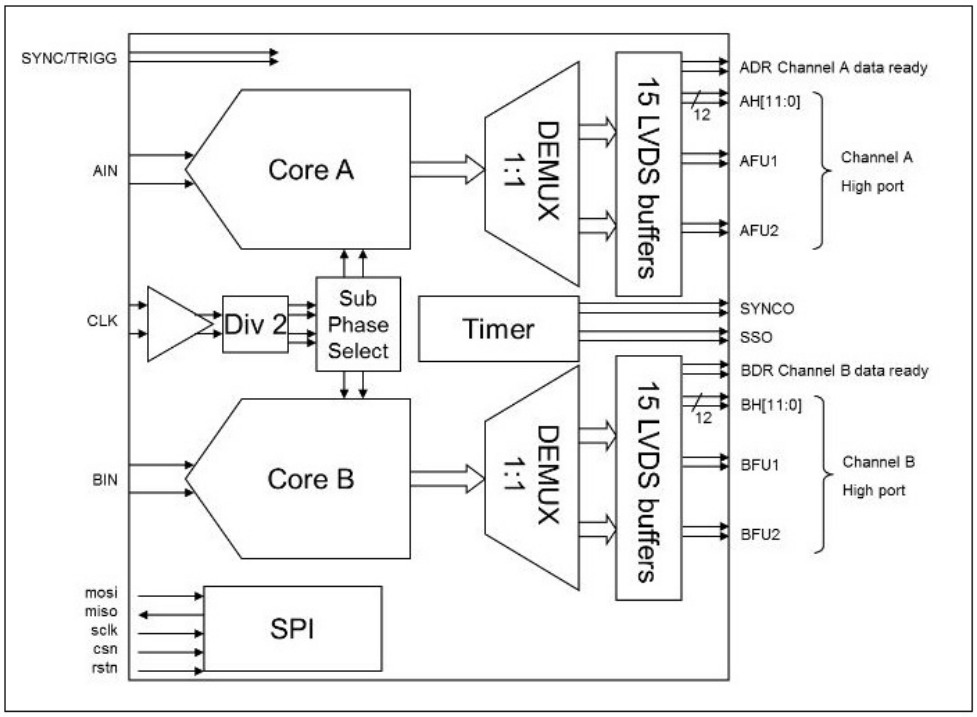


Figure 5.11 : RF-ADC functional block diagram.

and input bandwidth up to 4.3 GHz allows for direct digitization from S-Band without SNR degradation. As a result of direct sampling from S-Band, second downconversion stage usually required for further frequency downconversion which is needed to lower input frequency suitable for convential ADC input bandwidth is removed from receiver RF chain.

Table 5.9 : RF-ADC electrical characteristics.

Parameter	Value	Unit
Resolution	12	Bits
3dB Input Bandwidth	4.3	GHz
Sampling Rate	1.6	GSPS
Analog Input Full Scale Swing	1.0	Vpp
Signal to Noise Ratio @ 2200MHz	57	dBFS
Signal to Noise and Distortion Ratio @2200 MHz	56.5	dBFS
Effective Number of Bits	9.1	Bits
Power Consumption	2.3	W

5.2 RF Chain Analyses

Traditionally, RF Chain Analyses are performed on spreadsheet utilities to understand cascaded system behaviour, gain budget, noise figure or spurious products. However spreadsheet methods become inadequate for understanding impact of crucial parameters such as RF mismatches between components, phase noise and intermodulation effects due to part non-linearities and image noise related SNR reduction. Computer Aided Software (CAD) tools allow designers to include aforementioned non-idealities and produce closer results to real performance of the manufactured equipment. Therefore, AWR Design Environment's Visual System Simulator (VSS) has been chosen as the simulation platform for RF chain analyses of the proposed SAR Receiver. Electrical performance specification of selected parts and targeted designs are imported on simulation platform to increase the accuracy of the simulations. Designed block diagram for system level simulations is given in Figure 5.12.

5.2.1 Cascaded noise figure

As it is decribed in Section 3.2.3, cascaded noise figure of the receiver is predominantly defined by the noise factor and gain of first element placed in the RF Chain. Selection of a amplifier with low noise figure and high gain reduces the effect of subsequent components to total cascaded noise figure performance of the receiver. On the other hand, the noise figure and gain specifications of active RF components varies with enviromental temperature therefore temperature effects has been taken into account for operational temperature range of $-20°C$ to $-60°C$. SAR receiver cascaded

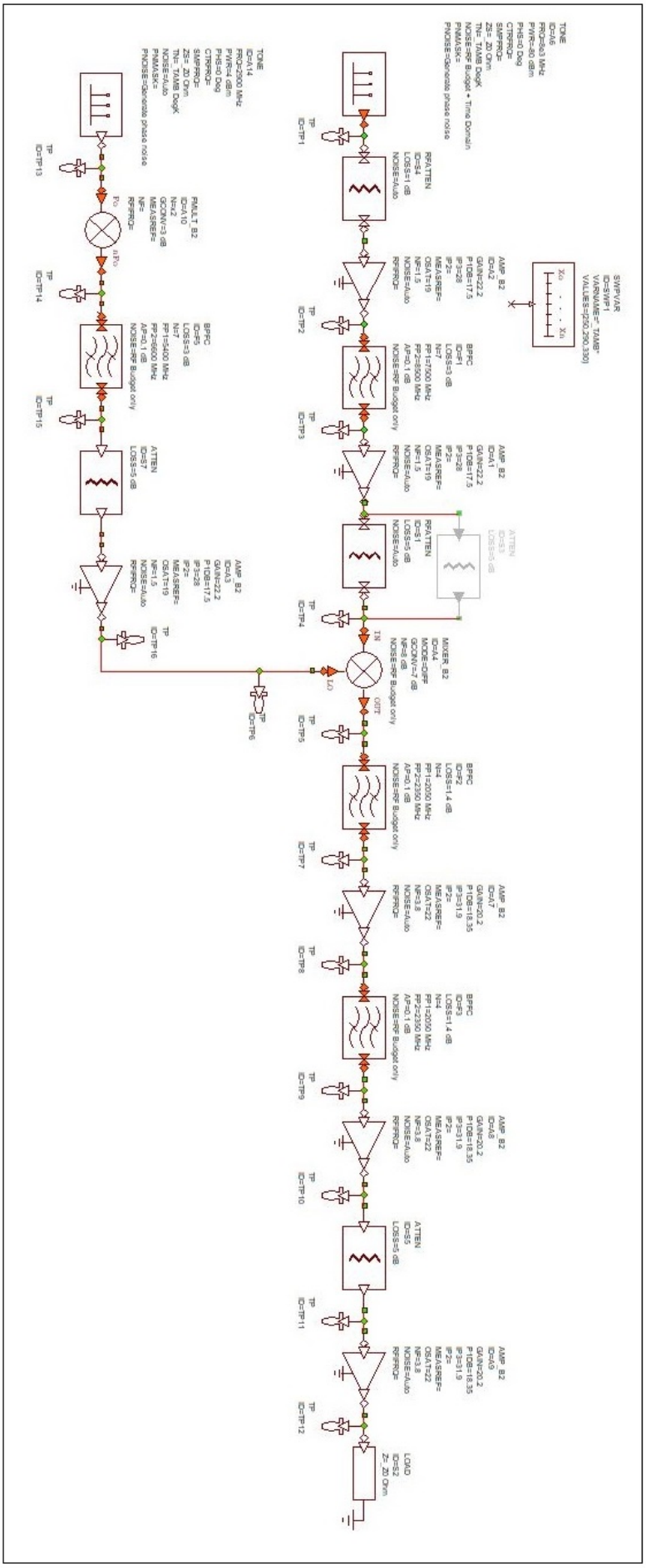


Figure 5.12 : SAR receiver system level simulations block diagram.

noise figure simulation results given in Figure 5.13 are consistent with theory and lower than <2.8dB in worst case high temperature scenario.

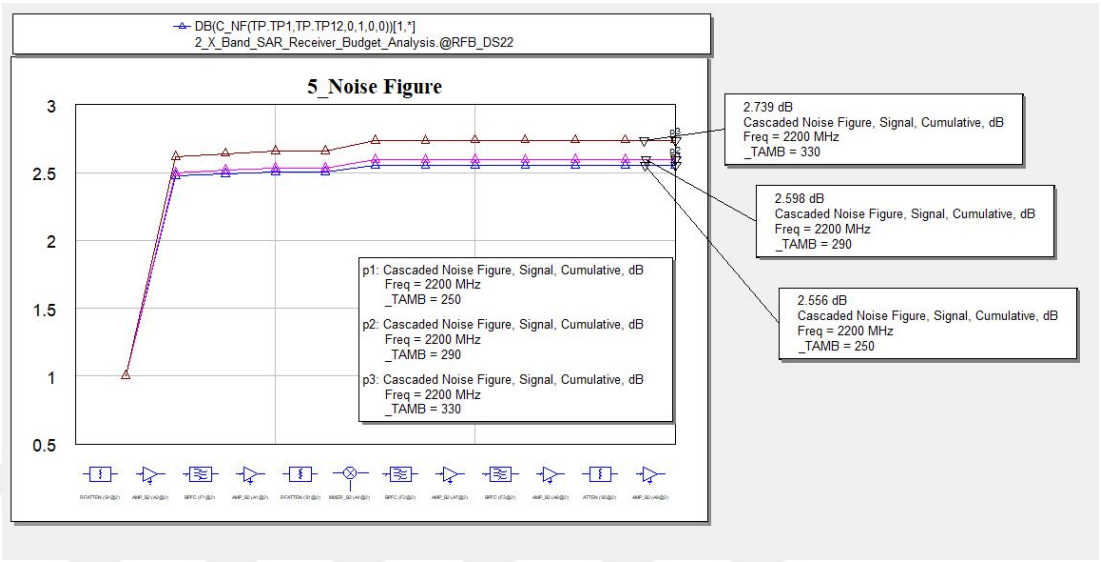


Figure 5.13 : Receiver cascaded noise figure results- System simulation.

5.2.2 Gain budget

RF signal power available at the input of the receiver needs to be amplified throughout RF chain to place the signal into analog-to-digital converter dynamic range. Considering proposed RF input power range of -120 to -80 dBm stated in Table 4.1 and ADC maximum input signal level of 1Vpp given in Table 5.9, required signal amplification value can be calculated by

$$G_{Cascade} = Maximum\ ADC\ Input\ Power\ - Maximum\ Receiver\ Input\ Power \quad (5.4)$$

$$G_{Cascade} = 10log(\frac{(V_{peak})^2}{2R}(10^3)) - (-80)dB \quad (5.5)$$

where R represents the characteristic impedance of 50 ohm and V_{peak} represents the peak voltage of ADC maximum input signal. Embedding related values to Equation 5.5 results in optimum system gain to reach full dynamic range of the ADC;

$$G_{Cascade} = 10log(\frac{(0.5)^2}{100}(10^3)) - (-80)dB = 84dB. \quad (5.6)$$

Number of gain amplifiers and attenuators are placed on the chain to adjust required 84 dB cascaded signal amplification. Gain budget analysis of the proposed receiver is given in Figure 5.14.

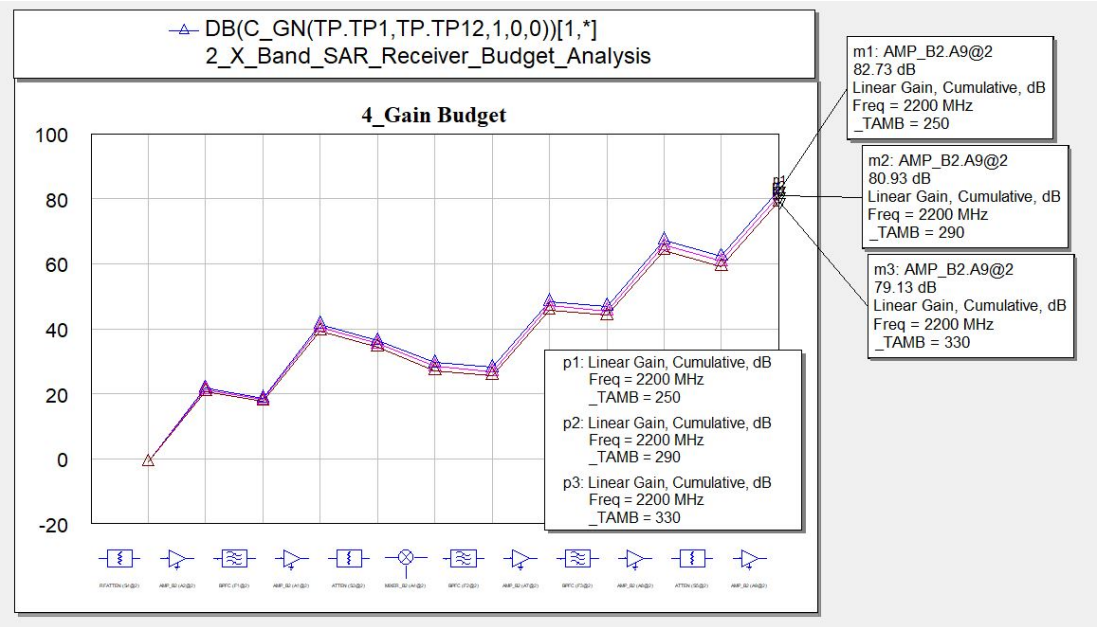


Figure 5.14 : Receiver gain budget analysis results.

As it can be seen from analysis results, there is approximately 3.6dB gain variation between maximum and minimum temperature limits associated with temperature dependency of the RF parts in the signal chain. In order to compansate gain variation, temperature variable attenuator is placed on IF section. Temperature coefficient of attenuation (TCA) of the TVA part can be calculated by following equation;

$$TCA = \frac{G_{T_{Low}} - G_{T_{High}}}{(T_{Low} - T_{High})(Att_{Fixed})}\ dB/dB/^{\circ}C \tag{5.7}$$

where $G_{T_{Low}}$ and $G_{T_{High}}$ represents system gain at minimum and maximum operating temperature in dB whereas T_{Low} and T_{High} represents the temperature limits in Celcius. Inserting related parameters to Equation 5.8 with fixed attenuation value of 5dB;

$$TCA = \frac{(82.73) - (79.13)}{((-20) - (60))(5)} = 0.009\ dB/dB/^{\circ}C \tag{5.8}$$

Temperature versus attenuation graph of the temperature variable attenuator selected according to calculated TCA value is displayed in Figure 5.15. Gain budget analysis of the SAR receiver after placement of TVA shows that gain variation within operating temperature range is reduced down to $\pm 0.4dB$. Cascaded gain graph with TVA is displayed in Figure 5.16.

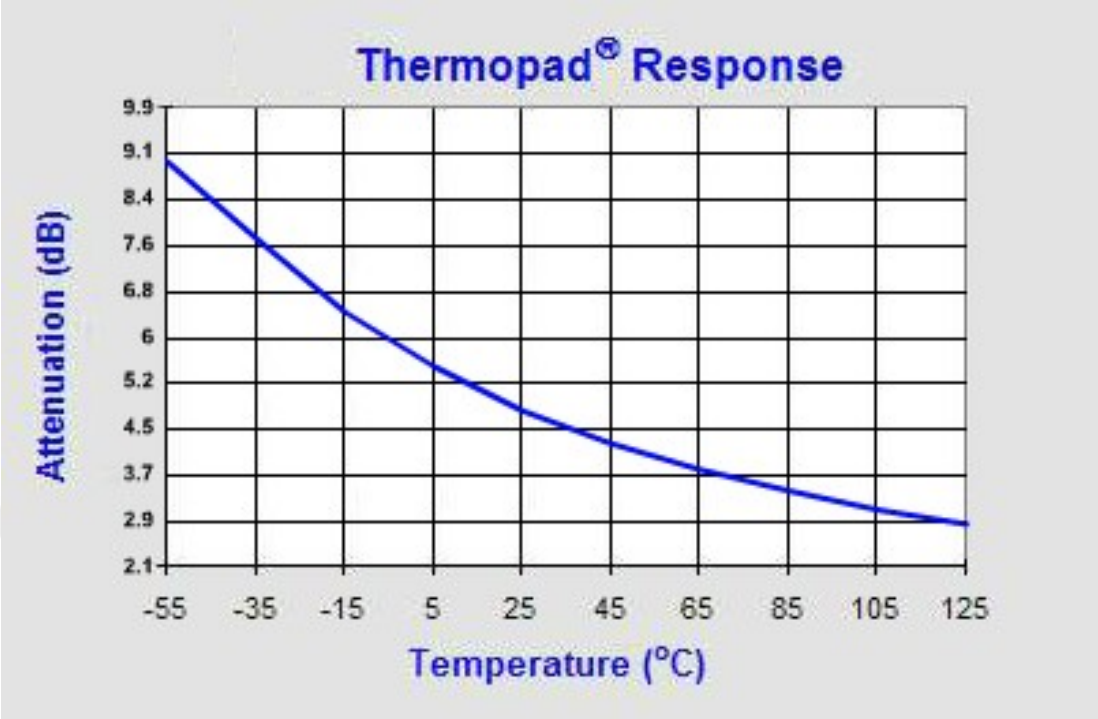


Figure 5.15 : Temperature variable attenuator with TCA:0.007 dB/dB°*C*

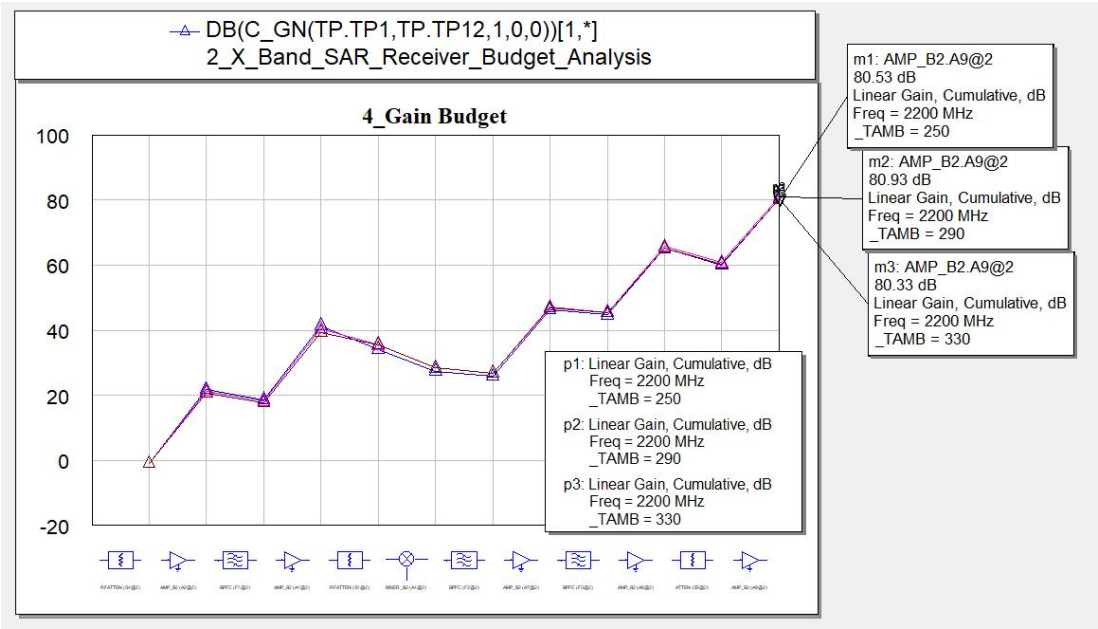


Figure 5.16 : Gain budget analysis result with TVA

5.2.3 Linearity analysis

Transistors and diodes used in microwave/RF components have non-linear system responses to input signals. Output function of generalized non-linear component can be expressed with Taylor series of expansion in terms of input signal voltage V_{IN};

$$V_{OUT} = c_0 + c_1 V_{IN} + c_2 V_{IN}^2 + c_3 V_{IN}^3 + ... \tag{5.9}$$

where coefficient of c_0, c_1, c_2, c_3 represents DC voltage output, linear conversion factor and higher order harmonic generation of input signal respectively. Non-linear output function can be turned into an advantage in frequency multiplication, frequency mixing and power detection applications. On the other hand, non-linearity becomes an issue in signal amplification due to unwanted output saturation, intermodulation distortion and spectral regrowth which results in SNR degradation of received signal. Linearity of an amplifier is generally expressed by their $1dB\ Compression\ Point\ (P_{1dB})$ and $Third-Order\ Intercept\ Point\ (IP_3)$. Input-Output function of an amplifier is illustriated in Figure 5.17. Investigating Figure 5.17 shows the fact that gain of the

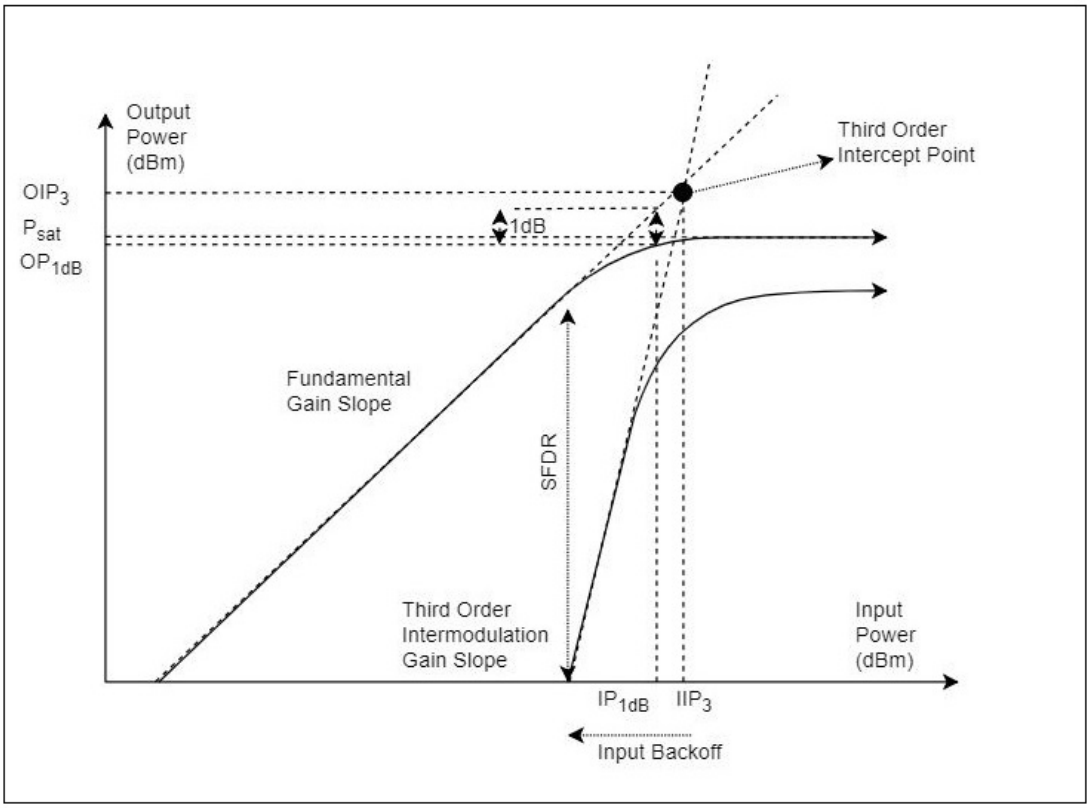


Figure 5.17 : Input-output function of an amplifier.

amplifier decreases as input signal power increases. Input signal power level where amplifier gain is reduced by 1dB in comparison with ideal linear gain slope is defined as $Input\ 1dB\ Compression\ Point\ (P_{1dB})$. Moreover, harmonic products starts to appear at the output spectrum with increasing input signal power. Interpolated virtual point where output third order intermodulation signal power is equal to fundamental output power is defined as $Output\ Third-Order\ Intercept\ Point\ (OIP_3)$. Third-order products such as $2f_0 - f_1$ and $2f_1 - f_0$ could potential fall in signal bandwidth where filtering will not be possible. In order to avoid signal degradation by third-order products, maximum output power produced by amplifiers can limited. Generated third-order intermodulation product power $Pout_{IM3}$ can be expressed in relation with output power ($Pout_{Fund.}$) and output third-order intercept point ($OIP3$) of an amplifier;

$$Pout_{IM3} = \frac{(Pout_{Fund.})^3}{(OIP3)^2}. \tag{5.10}$$

Taking logarithm on both sides results in:

$$log(Pout_{IM3}) = 3log(Pout_{Fund.}) - 2log(OIP3). \tag{5.11}$$

Maximum attainable SNR in proposed SAR receiver is limited by analog-to-digital converter performance given in Table 5.9 which is 57 dBFS. Third-order intermodulation products generated by the amplifiers lower than 57dB in comparison with fundamental signal power will reside in noise floor therefore will not further degrade the SNR performance. In order to limit the $Pout_{IM3}$ to -60dBc with respect to $Pout_{Fund.}$, maximum output power of an amplifier can be calculated by

$$log(Pout_{Fund.}) - 60dB = 3log(Pout_{Fund.}) - 2log(OIP3). \tag{5.12}$$

Rearrenging Equation 5.12 results required output backoff from $Pout_{IM3}$ of the amplifier:

$$30dB = log(OIP3) - log(Pout_{Fund.}). \tag{5.13}$$

In order to keep third-order intermodulation products lower than 60 dBc, signal power at the amplifier output should be 30dB lower than output IP3 level of the amplifier. Signal power distribution on RF chain has been represented in Figure 5.18.

Figure 5.18 shows the fact that signal is amplified up to $\approx 1dBm$ where the IF amplifier has IP3 level of 32 dBm therefore output power back-off is sufficient to keep IM3

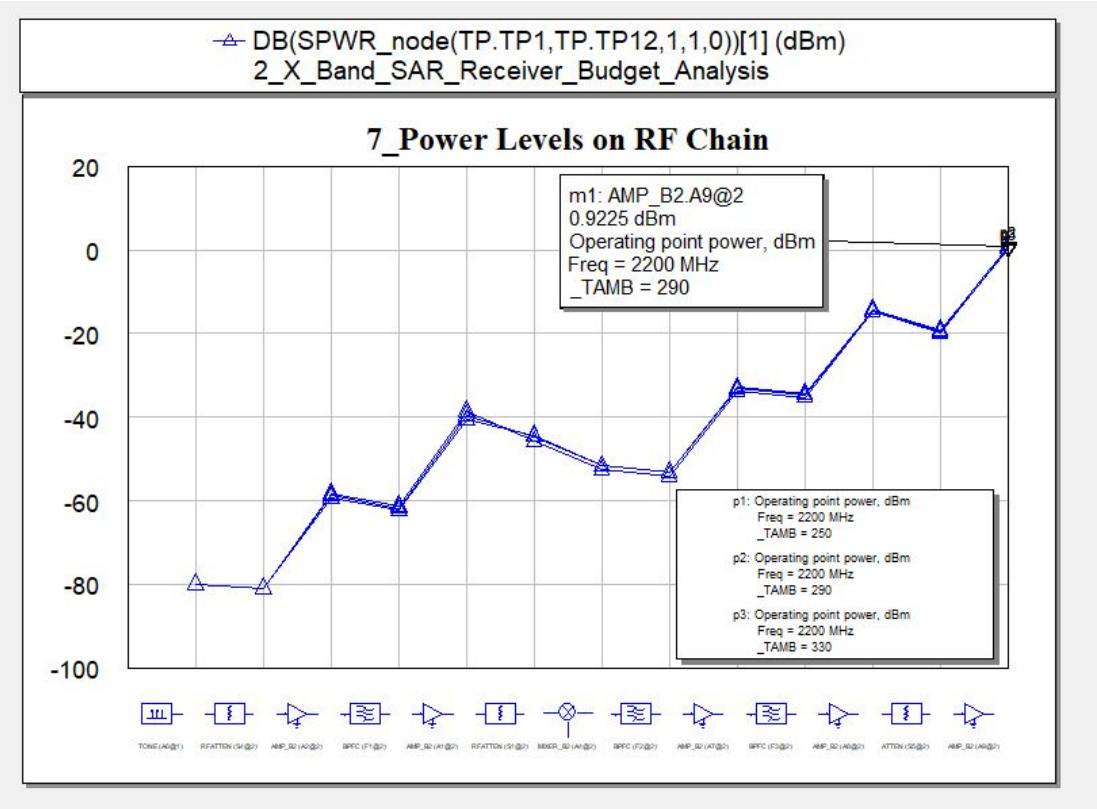


Figure 5.18 : Received signal power distribution on RF chain.

products lower than 60dBc. Linearity analysis graph of the proposed SAR receiver architecture has been shown in Figure 5.19 to validate theoretical calculations.

As it can be seen from Equation 5.11 and Figure 5.19 , power level of generated third-order intermodulation (IM3) product increases with increasing signal output power. Maximum power level in respect to fundamental signal is below 67 dBc where the amplified signal reachs its maximum power on RF chain which is compatible with theoretical calculations.

5.2.4 Spurious analysis

Downconversion of the received signal produce various unwanted spurious products due to non-linearity of mixer. Although utilization of double-balanced mixer eases the filtering due to suppressed even-order LO and RF intermodulation products, LO leakage and odd-order intermodulation products will be present at output spectrum of the mixer. On the other hand, keeping clean LO signal to drive downconverter mixer also reduces the number of unwanted spurious products. Therefore it is crucial

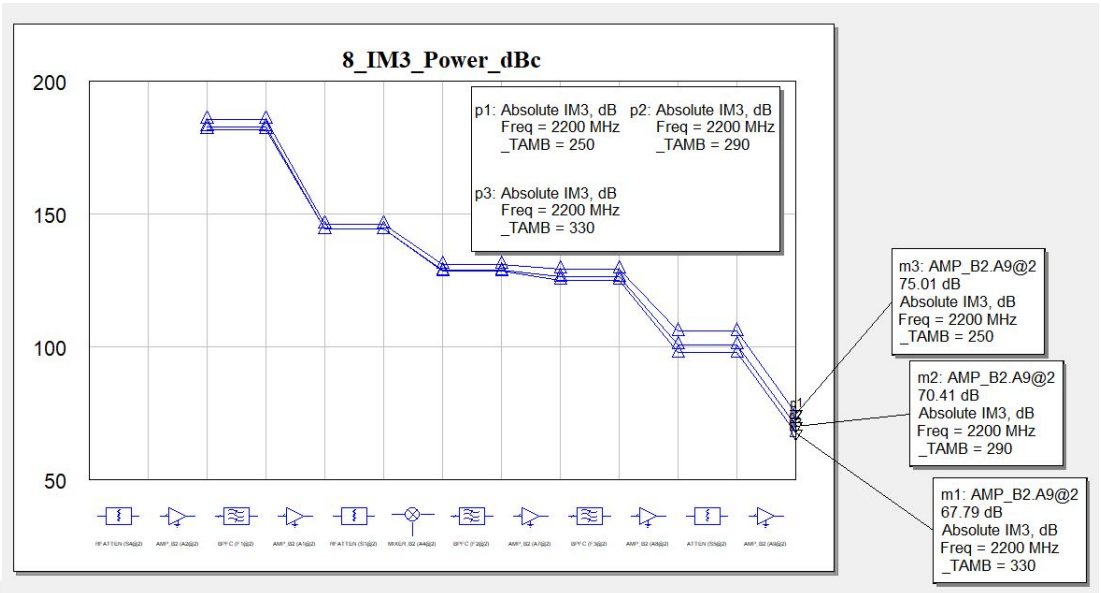


Figure 5.19 : Third-order intermodulation distortion analysis.

to analyze local oscillator spectrum and downconverted signal spectrum to adjust filtering requirements if deemed necessary. Spurious analysis graph of the local oscillator output has been shown in Figure 5.20. Due to frequency multiplication

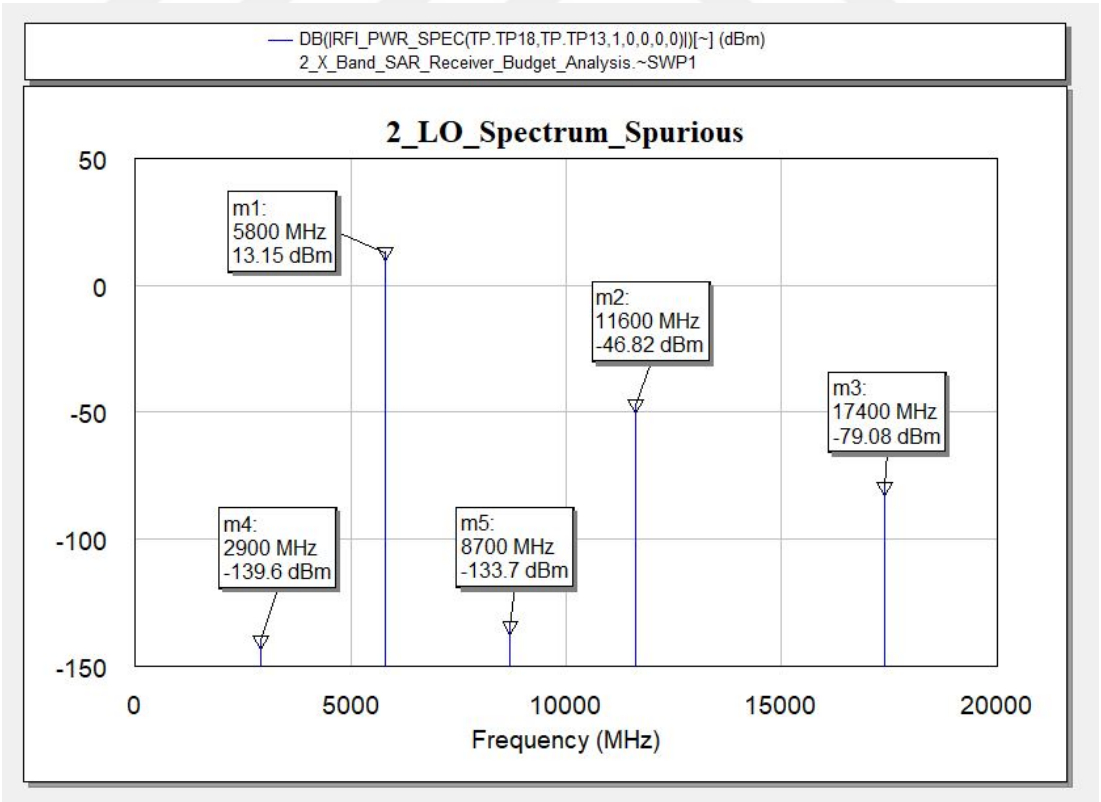


Figure 5.20 : Local oscillator output spectrum spurious signal analysis.

scheme chosen for local oscillator signal generation, fundamental (2900 MHz) and third-harmonic (8700 MHz) of the reference signal are present in the spectrum however highly suppressed because of the band-pass filtering after multiplication. Since downconverter mixer requires minimum +13dBm LO power to satisfy stated electrical specification, buffer amplifier is used to amplify the multiplied local oscillator carrier . However non-linearity of the buffer amplifier causes second (11600 MHz) and third harmonic (17400 MHz) signal generation at the local oscillator spectrum. Spurious analysis graph of the downconverter mixer output where RF frequency is 8000 MHz and local oscillator frequency is 5800 MHz has been shown in Figure 5.21. Source of spurious signals presented in the spectrum has been given in detailed in Table 5.10.

Unwanted spurious signals which could propagate through RF chain and reduce

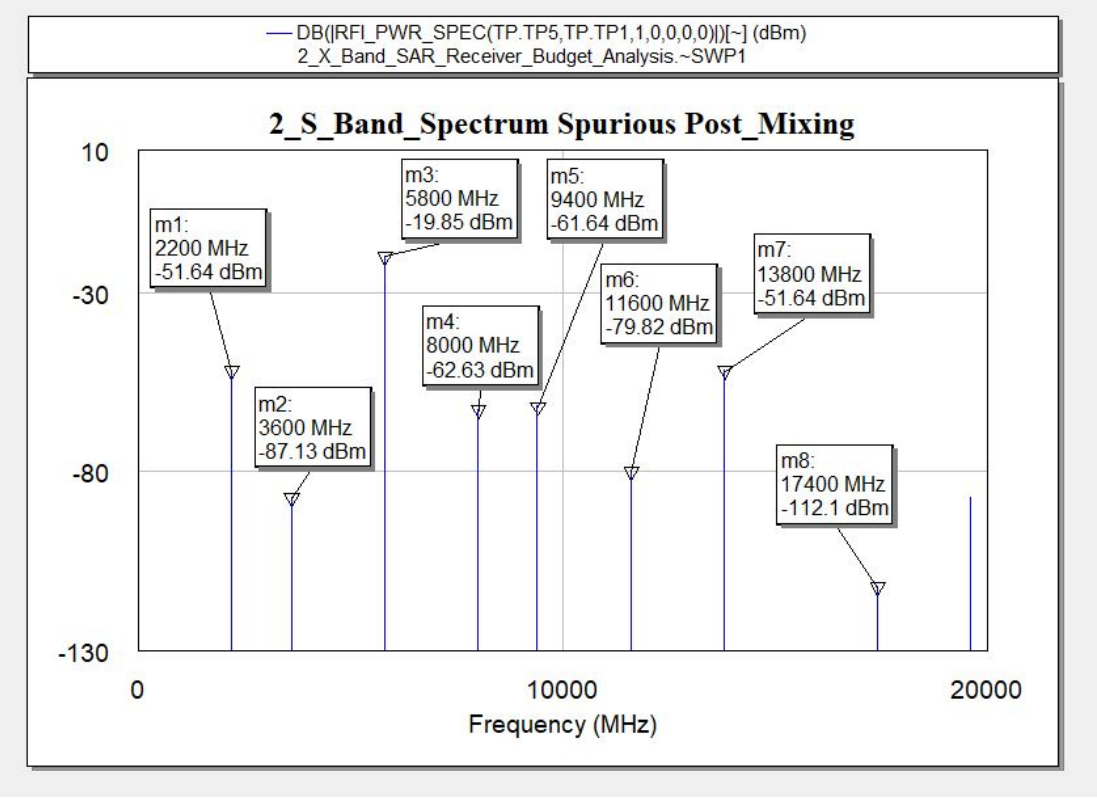


Figure 5.21 : Mixer output spectrum spurious signal analysis.

the signal integrity are filtered at IF section with narrow band pass filters. Desired intermediate frequency of 2200 MHz is further amplified to reach ADC full scale. Spurious analysis graph at the end of RF receiver chain has been shown in Figure 5.22. Examination of Figure 5.22 shows that mixer spurs generated by downconversion

Table 5.10 : Spurious signals source of generation.

Frequency (MHz)	Power (dBm)	Source of Generation (mLO±nRF)
2200	***-51.64***	***RF-LO***
3600	-87.13	2LO-RF
5800	-19.85	LO
8000	-62.63	RF
9400	-61.64	3LO-RF
11600	-79.82	2LO
13800	-51.64	RF+LO
17400	-112.1	3LO

step has been suppressed by the intermediate frequency filters. On the other hand, non-linearity of the IF amplifiers results in generation of second and third harmonic of the IF signal which is ≈80 dBc lower than fundemental signal. Since maximum SNR achievable by the proposed receiver architecture is limited by ADC SNR performance of 57dBFS, generated harmonics are considered negligible and does not require further filtering stages.

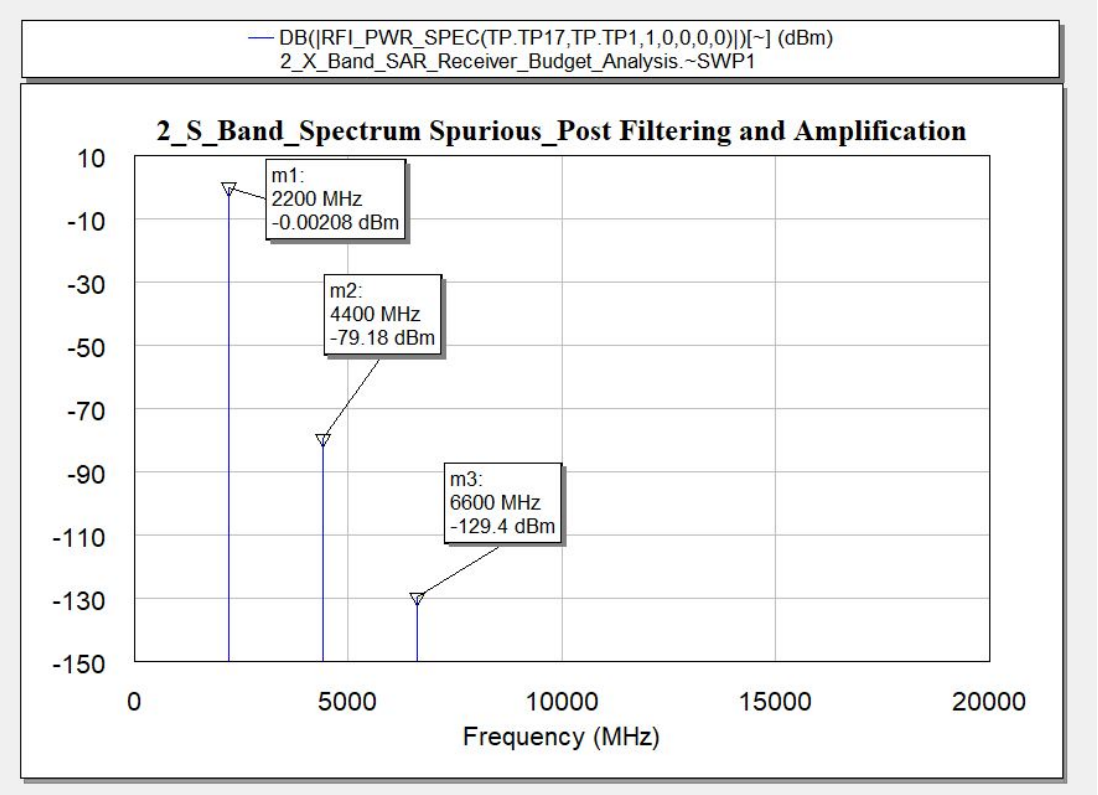


Figure 5.22 : IF spectrum spurious signal analysis post-filtering and amplification.

6. X-BAND HYBRID FRONT END DESIGN

Proposed X-Band SAR Receiver architecture has been divided into two physical platform based on operating frequency, compexity of interconnection between circuit elements, packaging types of selected parts and manufacturing tolerances. Since RF MMIC parts used on high frequency blocks are unpackaged die parts, coefficient of thermal expansion (CTE) difference between parts and microwave substrates becomes critical for long term reliability [43]. On the other hand, manufacturing tolerances on microstrip lines results in undesired performance variation which eventually decrease the yield of the manufactured microstrip boards. Most particularly, distributed element filters and matching circuits are highly susceptible to conductor manufacturing tolerances where design performance greatly relies on line widths and spacings. Moreover, dielectric and conductor losses of the selected substrates are directly proportional to operating frequency therefore selection of a low loss conductor on high frequency section reduces the unwanted path losses between signal paths. Microwave Integrated Circuit (MIC) alumina substrates manufactured with thin-film technology offers significantly low dielectric and conductor losses, precise etching of conductor patterns and CTE of $\approx 7ppm/^{\circ}C$ which is closely matched to GaAs CTE of $\approx 6ppm/^{\circ}C$ [44]. However thin-film MIC process is limited with single layer construction and does not allow multi-layer high density designs. Due to utilization of packaged parts and large number of interconnect required for mixed-signal and digital circuits, multi-layer PTFE based printed circuit board (PCB) technology is found as the best approach for IF and digital sections of the receiver. As a result, RF and LO sections are separated from IF and digital sections to be designed and manufactured with Thin-Film MIC technology. Physical separation of the proposed SAR receiver is illustriated in Figure 6.1.

6.1 Substrate Material and Stack-Up Construction

Alumina substrates with %99.9 purity provides excellent medium as a microwave/RF circuit carriers due to their low dielectric losses at high frequencies, high flexural strengths and thermal conductivity. Moreover, dielectric constant variation of high purity alumina is negligeble with changing frequency, temperature and process due to single material composition. Secondly, high dielectric constant results in reduction on RF circuit sizes and dimensions where effective wavelength on microstrip line is inversely proportional to dielectric constant of the substrate material. Electrical and mechanical properties of %99.9 alumina substrate is listed in Table 6.1 [44]. Dielectric thickness can be used in thin-film %99.9 alumina substrates are standardized

Table 6.1 : %99.9 Alumina (Al2O3) substrate electrical and mechanical properties.

Properties	***Value***	***Unit***
Flexural Strength	660	MPa
Bulk Density	3.97	g/cm^3
Coefficient of Thermal Expansion	8	ppm/K
Thermal Conductivity	33	W/mk
Volume Resistivity	1e-15	ω.cm
Dielectric Constant @ 10 GHz	9.9	-
Dielectric Loss Tangent	1e-4	-

within range of 0.1, 0.15, 0.2, 0.25 and 0.38 um. Metallization on top of the substrate selected as gold in order to avoid oxidation of the conductor patterns which could result degradation on electrical performance. However direct contact with gold and alumina results in weak adhesion therefore requires thin intermediate metallic layers to improve adhesion between substrate and conductor materials. Most widely used metals placed between alumina and gold are titanium (Ti), palladium (Pd) and platinum (Pt). Characteristic impedance of a microstrip line with thin metallisation layer can be approximately calculated using following set of equation given in [20];

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\varepsilon_e}} ln(\frac{8h}{W} + \frac{W}{4h}) & W/h \leq 1 \\ \frac{120\pi}{\sqrt{\varepsilon_e}[W/h+1.393+0.667ln(W/h+1.444)]} & W/h \geq 1 \end{cases} \tag{6.1}$$

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12h/W}} \tag{6.2}$$

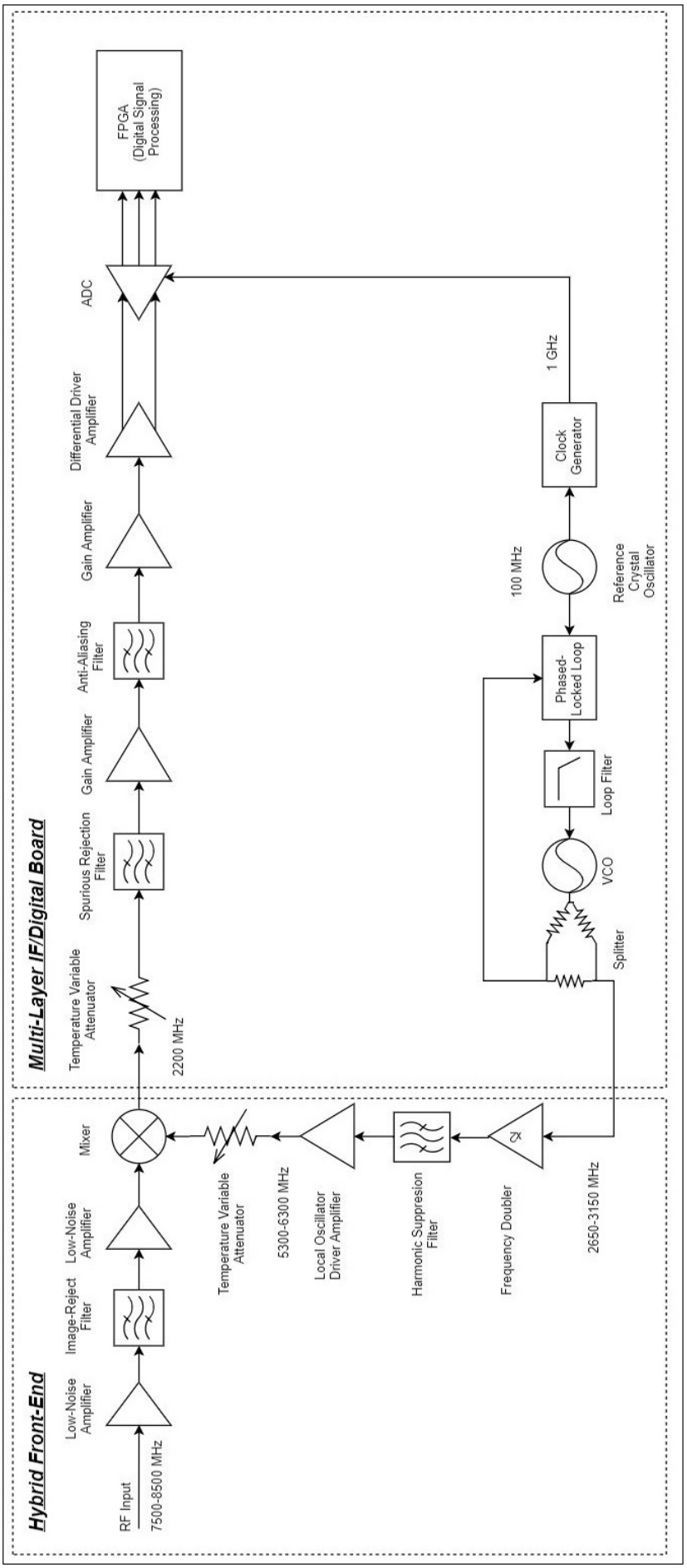


Figure 6.1 : Proposed SAR receiver design architecture physical separation.

where h represents the substrate height, W represents the conductor width and ε_e represents the effective dielectric constant. Microstrip line width to substrate height calculation for 50Ω characteristic impedance can be calculated by modifiying Equation 6.1 and Equation 6.2 as

$$W/h = \begin{cases} \frac{8e^A}{e^{2A}-2} & W/h \leq 2 \\ \frac{2}{\pi}[B-1-ln(2B-1)+\frac{\varepsilon_r-1}{2\varepsilon_r}\{ln(B-1)+0.39-\frac{0.61}{\varepsilon_r}\}] & W/h \geq 2 \end{cases} \quad (6.3)$$

where

$$A = \frac{Z_0}{60}\sqrt{\frac{\varepsilon_r+1}{2}} + \frac{\varepsilon_r-1}{\varepsilon_r+1}\left(0.23+\frac{0.11}{\varepsilon_r}\right) \quad (6.4)$$

$$B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_r}}. \quad (6.5)$$

Solving Equation 6.3 and 6.4 for microstrip line with characteristic impedance of a 50Ω on alumina substrate with 9.9 ε_r results in width to height ratio (W/h) of 0.958. Assuming industry standart thin flim circuit tolerance of $\pm 5um$, calculated widths and impedance variations for 50 Ω microstrip lines are listed in accordance with possible substrate thickness values in Table 6.2. Resulting table indicates the

Table 6.2 : Conductor width & dielectric height vs manufacturing tolerance.

Dielectric Height (um)	Conductor Width (um)	Impedance Variation (Ohm)
100	96	± 1.23
150	144	± 0.73
200	192	± 0.64
250	240	± 0.51
380	***364***	± ***0.42***

fact that as dielectric height increases, impedance variation due to manufacturing tolerance decreases. Furthermore, thicker dielectric substrates simplifies handling of the designed boards in manufacturing and integration phase. Therefore dielectric thickness of 380um is selected for substrate thickness for X-Band Hybrid Front-End design. Verification of calculated microstrip line widths has been done on AWR Design Environment Computer Aided Software (CAD) tool. Output of AWR software microstrip line calculator is shown in Figure 6.2. Because of the fact that CAD calculator includes the conductor thickness on microstrip line calculation, ≈4um line width difference arises between theoretically derived and software aided results.

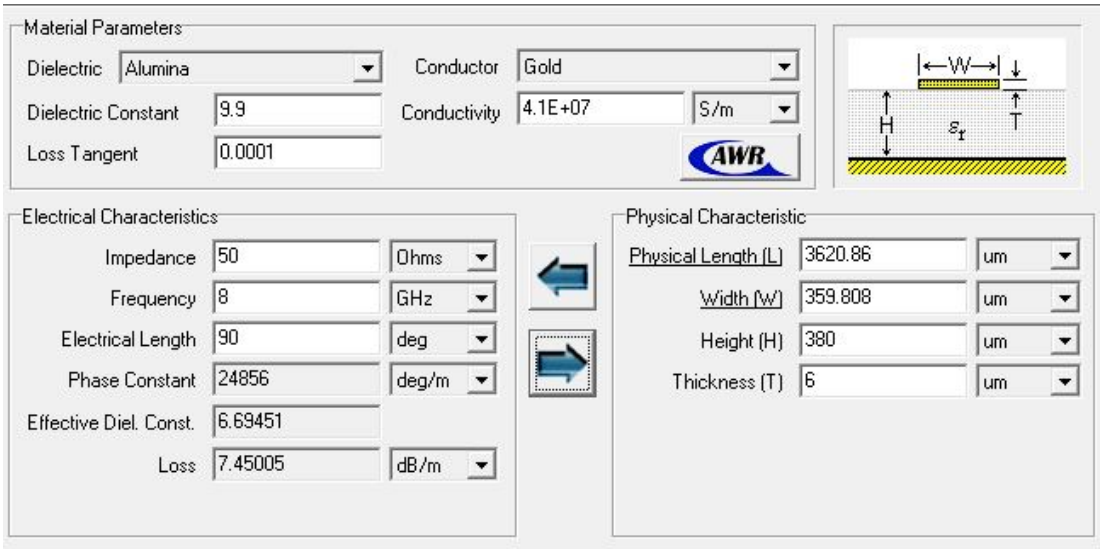


Figure 6.2 : AWR Design Environment microstrip line calculator result.

6.2 LNA MIC Design

LNA MIC designed for hybrid front end consists of MMIC LNA die, wire-bondable decoupling capacitors and a bias resistor. Electrical parts are placed on top of a % 99,9 alumina substrate with 381um dielectric thickness. Decoupling capacitors are used to provide low impedance path for supply power required by low noise amplifier. Bias resistor is placed for adjustment and fine tuning of LNA MMIC gain if required after assembly. Wideband gain (S21), input reflection (S11) and output reflection (S22) parameters of selected LNA part has been given in rectangular format in Figure 6.3. Input matching specification of the LNA within interested operation bandwidth of 7750-8250 MHz is higher than -10dB which could be considered as poorly matched. Microstrip line impedance matching techniques is used to improve input matching of the LNA part within operation bandwidth. Due to ease of manufacturing, tunability and low cost, open stub transmission lines are utilized on matching circuit. In order to achieve lossless power transfer and reflection due to impedance mismatch, source impedance of the circuit should be equal to complex conjugate of the input impedance.

$$Z_S = R_S \pm jX_S = Z_{IN} = R_{IN} \pm jX_{IN} \tag{6.6}$$

Source impedance is taken as $50\Omega + j0$ which is the industry standart for microwave and RF systems. Normalization with respect to 50Ω characteristic impedance results

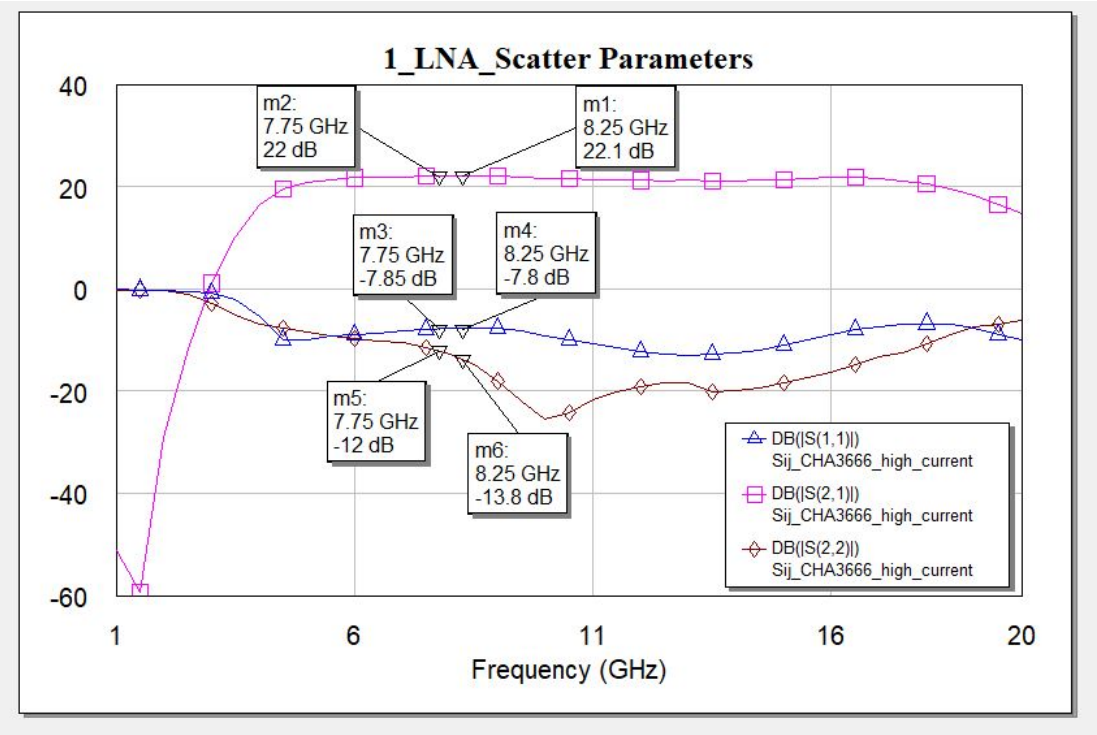


Figure 6.3 : LNA wideband scatter parameters.

in

$$Z_s = 1 \pm j0 = Z_{in} = R_{in} \pm jX_{in}. \tag{6.7}$$

In most cases, load impedance of the transmission lines consists of real and imaginary part in their impedance representation due to reactive parasitic elements. Impedance matching between purely resistive source to reactive load can be accomplished with utilization of *Microstrip L Section* which consists of two reactive elements constructed by microstrip lines. Visual representation of L section matching network has been shown in Figure 6.4. Input impedance Z_{IN} of the network given in Figure 6.4 can be calculated by

$$Z_{IN} = \frac{1}{jB + \frac{1}{jX+Z_L}} = \frac{1}{jB + \frac{1}{jX+R_L+jX_L}}. \tag{6.8}$$

Embedding Equation 6.6 into Equation 6.8 results in equation which relates input impedance to load impedance for perfect matching condition:

$$\frac{1}{R_S + jX_S} = jB + \frac{1}{R_L + j(X + X_L)}. \tag{6.9}$$

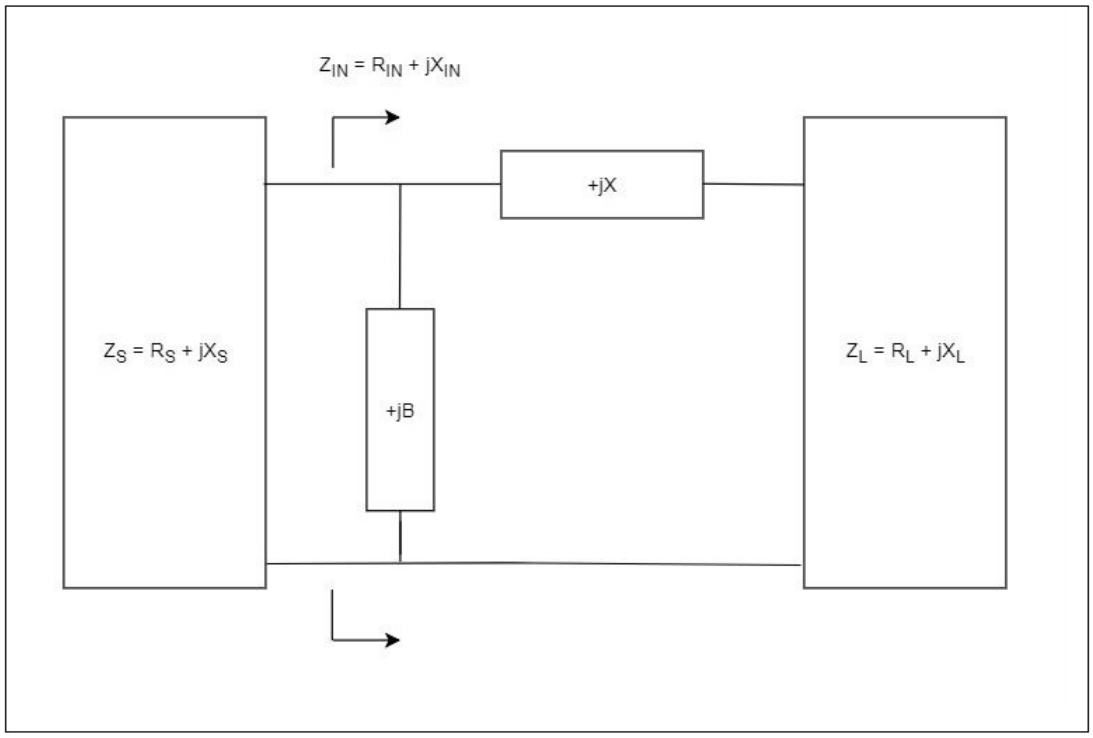


Figure 6.4 : L-Section impedance matching network.

Rearranging and separation of real and imaginary part of the Equation 6.9 produces two equation with unknown X and B values;

$$R_L - R_S = -B(XR_S + X_L + R_S + R_L X_S) \tag{6.10}$$

$$X + X_L = BR_L R_S - X_S(B(X + X_L) - 1). \tag{6.11}$$

Since source impedance of the system is purely real ($Z_S = R_S + j0$), Equation 6.10 and Equation 6.11 can be simplified into following forms by replacing X_S with 0;

$$R_L - R_S = -B(XR_S + X_L + R_S) \tag{6.12}$$

$$X + X_L = BR_L R_S. \tag{6.13}$$

Solving for B and X produce two set of equation that provide elegant way to find B and X values in terms of load impedance and source impedance;

$$X = \pm\sqrt{R_L(R_S - R_L)} - X_L \tag{6.14}$$

$$B = \pm\frac{\sqrt{(R_S - R_L)/R_L}}{R_S}. \tag{6.15}$$

In order to calculate required reactance and susceptance values of X and B, input impedance of the LNA is acquired from scatter parameters which is represented in Figure 6.5 smith chart. As it can be read from Figure 6.5, normalized input impedance

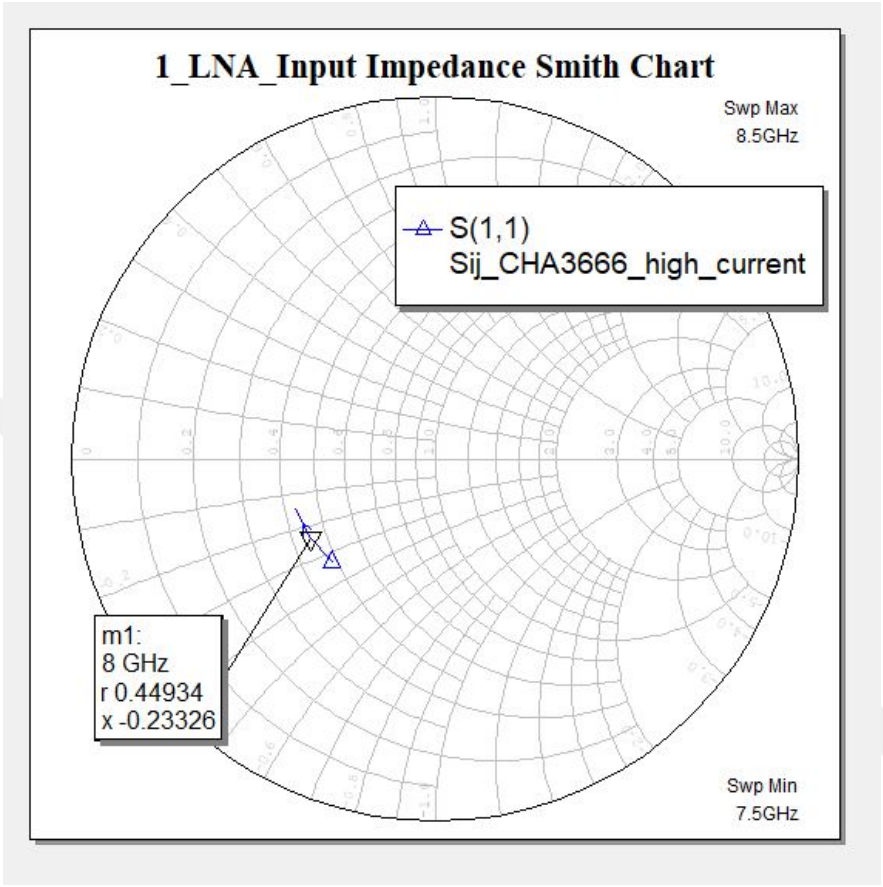


Figure 6.5 : LNA input impedance @ 8 GHz.

of the LNA is equal to $Z_L = R_L + jX_L = 0.45 - j0.23$. Inserting related values to Equation 6.14 and 6.15 results in required reactance and susceptance value for matching L network:

$$X = \pm\sqrt{0.45(1-0.45)} + 0.23 \tag{6.16}$$

$$B = \pm\frac{\sqrt{(1-0.45)/0.45}}{1}. \tag{6.17}$$

There are two sets of values that will result in exact match condition. Series reactance value of X and parallel susceptance value of B has two possible solution; {+0.73: -0.22} and {+1.1: -1.1} respectively. First set of solution which is $X = +0.73, B = +1.1$ is chosen for further calculations. Validation of calculated results and determining initial values of microstrip line lengths to achieve needed reactance

and susceptance values are performed on smith chart tool due to its convenience and simplicity. Starting from input impedance of the LNA at 8 GHz operating frequency

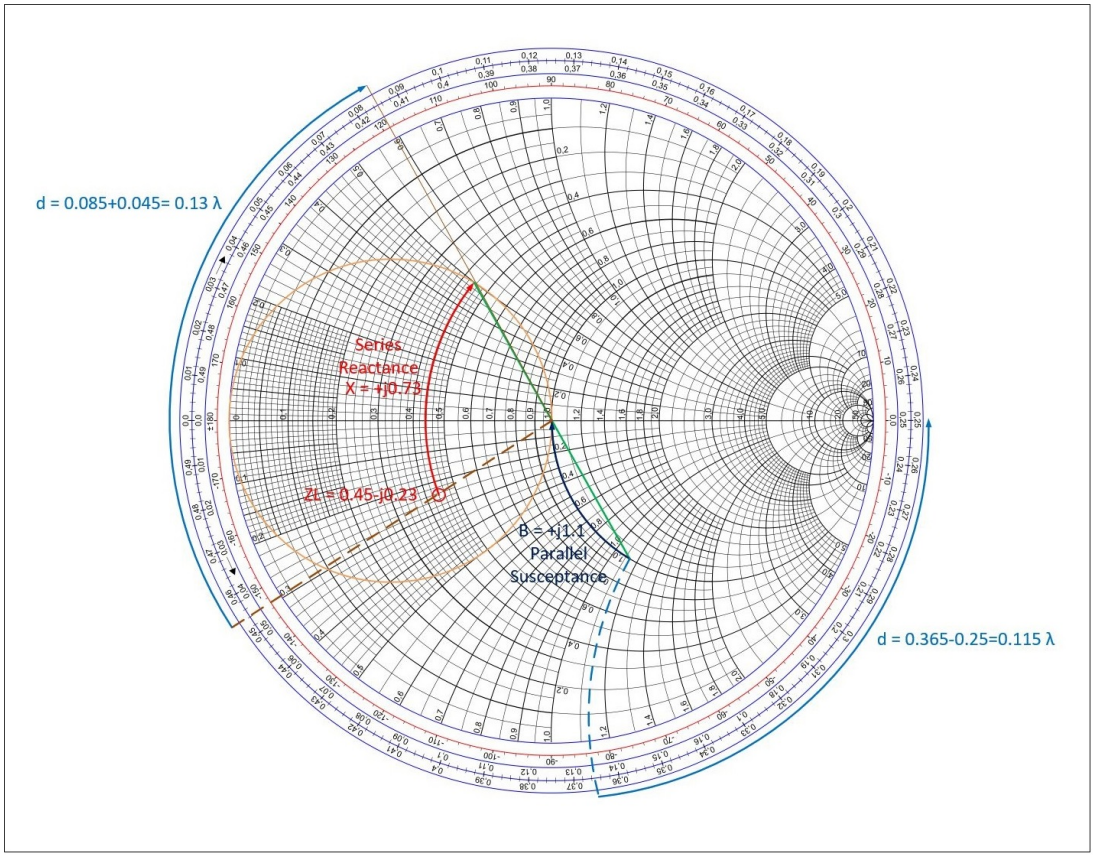


Figure 6.6 : LNA input matching on Smith Chart.

which is the load impedance of input matching network, series reactance value of $X = +j0.73$ has been added to reach constant admittance $Y = 1$ circle. Electrical length required to create aforementioned reactance is found to be approximately 0.13λ. In order to add parallel susceptance of $B = +1.1$, impedance value achieved by addition of series reactance has been projected into constant impedance $R = 1$ circle. Addition of paralel susceptance results in input impedance of $1 + j0$ which provides the perfect matching condition for frequency of 8 GHz. In case of utilizing open circuit stub to generate paralel susceptance value of $B = +1.1$, required electrical length is equal to approximately 0.115λ. Physical microstrip line lengths of stub distance and stub length which generates series reactance and parallel susceptance respectively are found as;

$$L_X = 0.13\lambda = 0.13 * 14.48mm \approx 1882mm \tag{6.18}$$

$$L_B = 0.115\lambda = 0.115 * 14.48mm \approx 1665mm \tag{6.19}$$

where guided wavelength of 8 GHz (λ) on alumina substrate defined in 6.1 is equal to 14.48mm. Post-matching wideband gain (S21), input reflection (S11) and output reflection (S22) parameters of LNA MIC board are presented in rectangular format in Figure 6.7. Input reflection of the LNA within operating bandwidth of interest is improved to S11<-18 dB which verifies that theoratical calculations are compatible with CAD simulation results. 2-D and 3-D layout illustration of designed

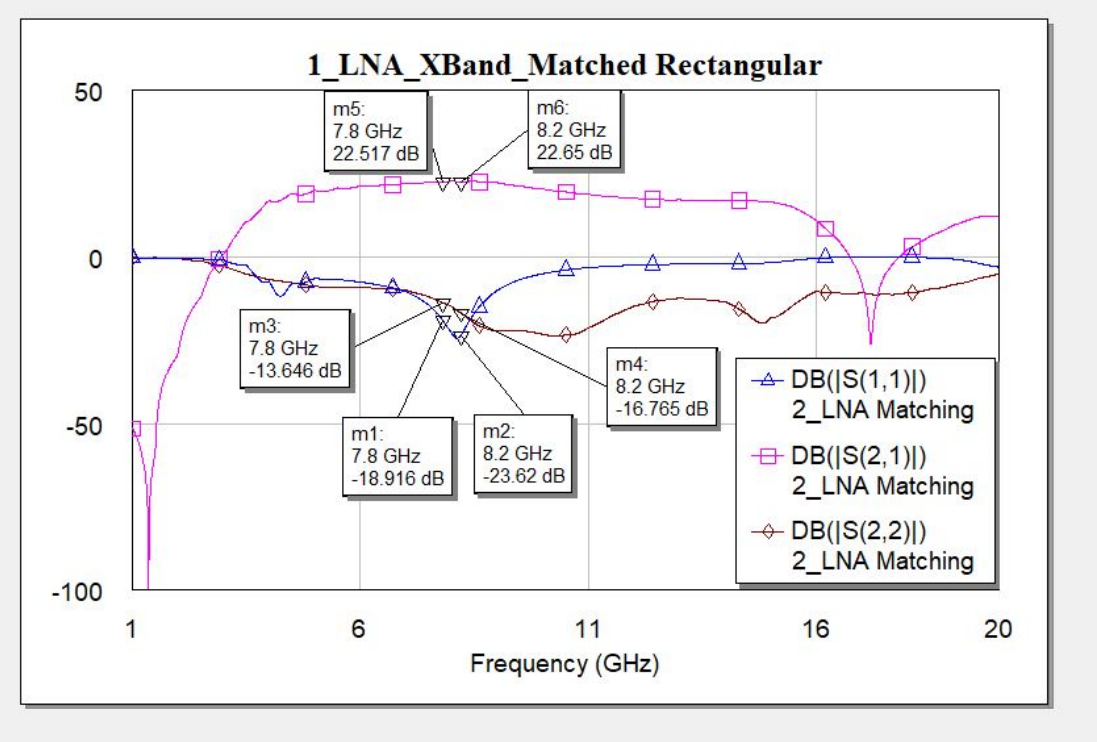


Figure 6.7 : LNA post matching wideband scatter parameters.

MIC board is shown in Figure 6.8 and Figure 6.9 respectively. Interconnection between microstrip lines, LNA MMIC die and decoupling capacitors are implemented by 25um gold wires. Input matching open stub is divided into two sections to decrease the length of the single stub. Additional bonding pads are placed alongside input and output transmission lines to provide post-manufacturing tuning to compansate unwanted impedance variations that could originate from manufacturing tolerances, MMIC performance variations and additive bonding wire impedance uncertainities. End points of RF transmission line are enlarged to compansate inductive effect of bonding wires. Total area of the circuit is confined within $80mm^2$.

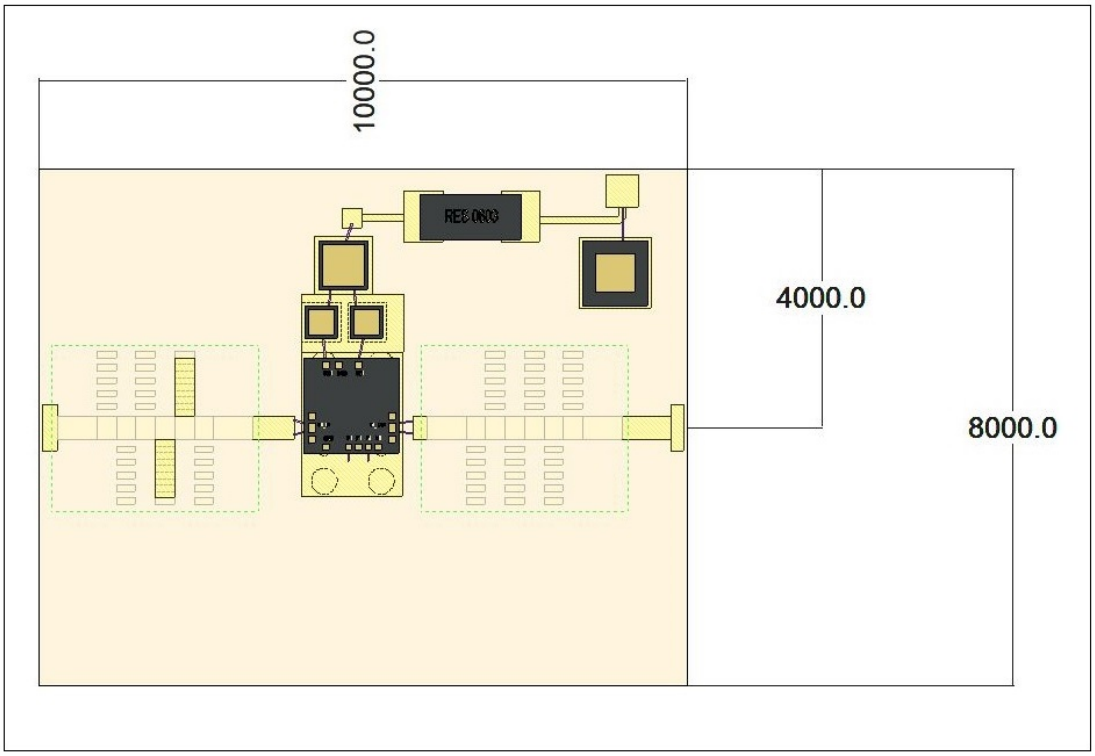


Figure 6.8 : LNA MIC 2-D visual.

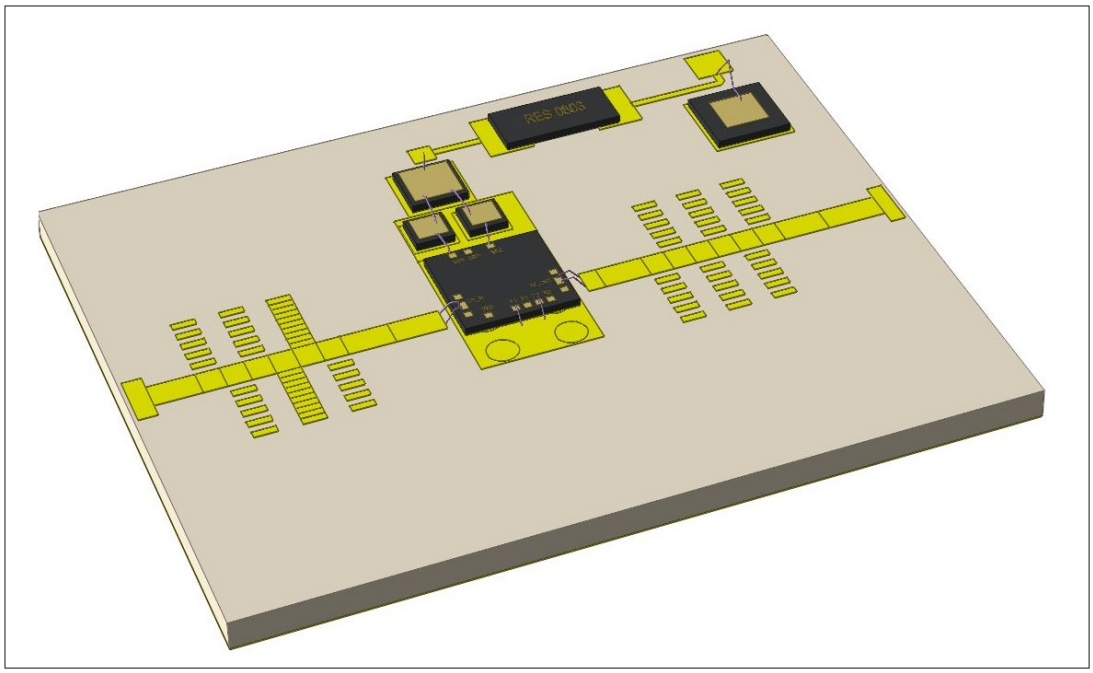


Figure 6.9 : LNA MIC 3-D visual.

6.3 Image-Reject Filter Design

Image Reject Filter placed after first low noise amplification stage provides two distinctive advantage to front end design. Firstly, IRF is designed to suppress image noise which would increase the noise figure of the receiver if not filtered. Moreover, bandpass response of the filter improves the selectivity of the receiver by filtering any unwanted out-of-band interference signals.

6.3.1 Mathematical model

Theoratical parameter derivation of bandpass filter is initialized with low-pass filter prototype design. Among Butterworth, Gaussian, Chebyshev and Elliptic filter responses, Chebyschev function filter is taken into consideration due to superior rejection and low passband ripple performance [45]. Generalized filter transfer function can be defined as

$$|S_{21}(j\Omega)|^2 = \frac{1}{1+\varepsilon^2 F_n^2(\Omega)} \tag{6.20}$$

where Ω represents frequency, ε is passband ripple constant and $F_n^2(\Omega)$ is the frequency dependent transfer response of the filter. Insertion loss and return loss performance of the generalized filter can be calculated by

$$L_A(\Omega) = 10log\frac{1}{|S_{21}(j\Omega)|^2}dB \tag{6.21}$$

$$L_R(\Omega) = 10log[1-|S_{21}(j\Omega)|^2]dB \tag{6.22}$$

where $L_A(\Omega)$ represents insertion loss and $L_R(\Omega)$ represents return loss performance of the filter [45]. Lowpass filter prototypes are base starting points to analytical calculations of filter synthesis. They can be used to determine the minimum order of the filters for required attenuation on specific frequency and derive the initial values for filter component values prior to detailed design phase. Lumped element representation of nth order Chebyshev lowpass filter prototype and Elliptic Function lowpass filter prototype has been illustriated in Figure 6.10 and in Figure 6.11 respectively.

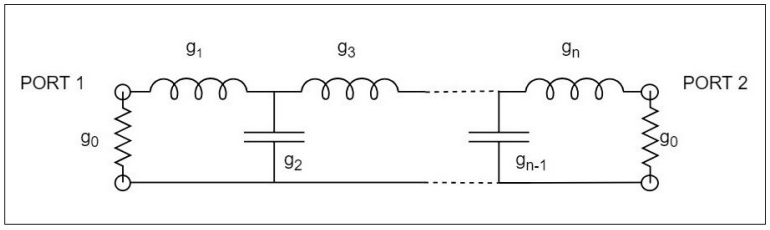


Figure 6.10 : nth order lowpass filter prototype.

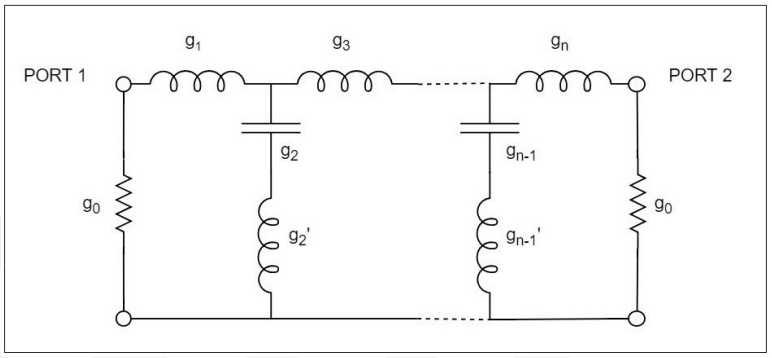


Figure 6.11 : nth order elliptic function lowpass filter prototype.

6.3.1.1 Chebyshev type lowpass filter prototype

Chebyshev filter response varies with predefined passband ripple requirement. Frequency dependent transfer response of the Chebyshev type filter is

$$|S_{21}(j\Omega)|^2 = \frac{1}{1+\varepsilon^2 T_n^2(\Omega)} \tag{6.23}$$

where T_n represents the Chebyschev function of the first kind of order n with following equations;

$$T_n = \begin{cases} cos(n\ cos^{-1}\Omega) & |\Omega| \leq 1 \\ cosh(n\ cosh^{-1}\Omega) & |\Omega| \geq 1 \end{cases} . \tag{6.24}$$

Transfer function coefficients of Chebyshev type lowpass filter prototype can be calculated using following formulas

$$\begin{aligned} g_0 &= 1 \\ g_1 &= \frac{2}{\gamma} sin(\frac{\pi}{2n}) \\ g_i &= \frac{1}{g_{i-1}} \frac{4sin[\frac{(2i-1)\pi}{2n}]sin[\frac{(2i-3)\pi}{2n}]}{\gamma^2 + sin^2[\frac{(i-1)\pi}{n}]} \qquad for\ i = 2,3,4,...n \end{aligned} \tag{6.25}$$

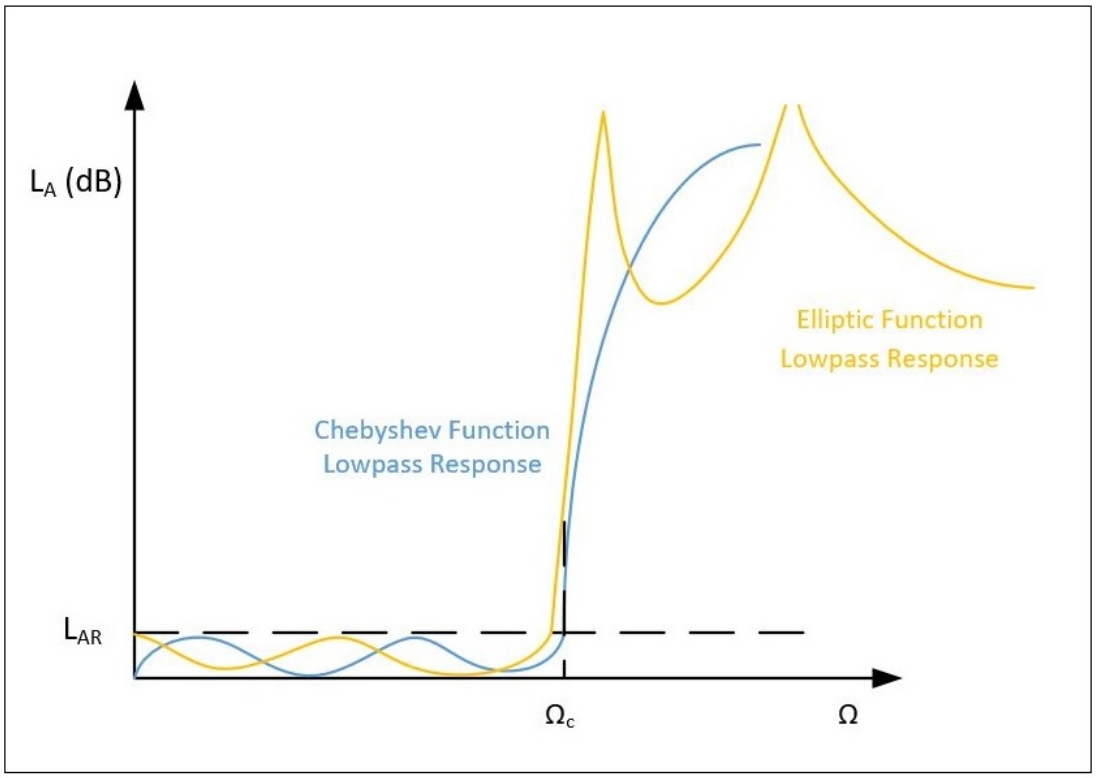


Figure 6.12 : Chebyshev lowpass response.

where β and γ can be calculated using

$$\beta = ln[coth(\frac{L_{AR}}{17.37})] \tag{6.26}$$

and

$$\gamma = sinh(\frac{\beta}{2n}). \tag{6.27}$$

Minimum number of filter order to satisfy target image rejection which is stated in Table 5.3 can be calculated by

$$n \geq \frac{cosh^{-1}\sqrt{\frac{10^{(IR/10)}-1}{10^{(0.1PB_{Ripple})}-1}}}{cosh^{-1}\Omega_s} \tag{6.28}$$

where IR represents image reject value in dB, PB_{Ripple} represents passband ripple in dB and Ω_s is the image frequency normalized to center frequency of image reject filter [45]. As it can be seen from Equation 6.28, order of the filter needed to achieve required image rejection value increases as passband ripple parameter decreases. Since received input signals with 250 MHz bandwidth propagates through image reject filter, low passband ripple is prefered to prevent any amplitude variation within input

signal bandwidth. However smaller passband ripple parameter will result in higher number of filter order thus increases the physical size and complexity of the realizable fillter. Therefore, a trade-off between filter size/complexity and passband ripple is investigated to decide filter order for implementation. Normalized value of Ω_s which represents bandpass filter centered on 8GHz with 1 GHz bandwidth is calculated with

$$\Omega_s = \frac{|(f_{Center} - f_{Image})| + (\frac{BW}{2})}{BW}) = \frac{|8GHz - 4GHz| + (1/2)}{1} = 4.5. \quad (6.29)$$

$IR = 50dB$ image rejection requirement and $\Omega_s = 4.5$ normalized image frequency is inserted into Equation 6.28. Minimum number of stages versus passband ripple PB_{Ripple} values are calculated using Equation 6.48 and given in Table 6.3.

$$n \geq \frac{cosh^{-1}\sqrt{\frac{10^5-1}{10^{0.1PB_{Ripple}}-1}}}{cosh^{-1}(4.5)} \quad (6.30)$$

In order to have symmetrical filter structure, odd number of filter stage is prefered in

Table 6.3 : Chebyshev type filter order calculation vs passband ripple.

PB_{Ripple} (dB)	Calculated "n"	Minimum Required Filter Order
0.01	4.342	5
0.05	3.972	4
0.1	3.812	4
0.2	3.651	4

implementation phase. Therefore fifth order filter is chosen as an optimum solution which can provide 0.01 dB passband ripple while maintaining 50dB image rejection. g_n coefficients of Chebyshev lowpass prototype filters can be obtain from precalculated coefficient tables. Coefficient values of prototype filter with orders up to seven and several passband ripple values are given in Table 6.4, Table 6.5 and Table 6.6 [45].

6.3.1.2 Chebyshev type lowpass filter prototype to bandpass filter transformation

Coefficient tables are used to determine inductive and capacitive elements which constitute microwave filters. Constructed lowpass prototypes can be converted to lumped element bandpass filters using frequency and element transformation equations. Frequency transformation from lowpass prototype to bandpass filter implementation is performed with

$$\Omega = \frac{\Omega_c}{FBW}(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}) \quad (6.31)$$

Table 6.4 : Coefficient values of Chebyshev lowpass prototype filters for 0.01 dB passband ripple.

PB_{Ripple} 0.01 dB								
n	g1	g2	g3	g4	g5	g6	g7	g8
1	0.0960	1.0	-	-	-	-	-	-
2	0.4489	0.4078	1.1008	-	-	-	-	-
3	0.6292	0.9703	0.6292	1.0	-	-	-	-
4	0.7129	1.2004	1.3213	0.6476	1.1008	-	-	-
5	0.7563	1.3049	1.5773	1.3049	0.7563	1.0	-	-
6	0.7814	1.3600	1.6897	1.5350	1.4970	0.7098	1.1008	-
7	0.7970	1.3924	1.7481	1.6331	1.7481	1.3924	0.7970	1.0

Table 6.5 : Coefficient values of Chebyshev lowpass prototype filters for 0.043 dB passband ripple.

PB_{Ripple} 0.04321 dB								
n	g1	g2	g3	g4	g5	g6	g7	g8
1	0.2000	1.0	-	-	-	-	-	-
2	0.6648	0.5445	1.2210	-	-	-	-	-
3	0.8516	1.1032	0.8516	1.0	-	-	-	-
4	0.9314	1.2920	1.5775	0.7628	1.2210	-	-	-
5	0.9714	1.3721	1.8014	1.3721	0.9714	1.0	-	-
6	0.9940	1.4131	1.8933	1.5506	1.7253	0.8141	1.2210	-
7	1.0080	1.4368	1.9398	1.6220	1.9398	1.4368	1.0080	1.0

Table 6.6 : Coefficient values of Chebyshev lowpass prototype filters for 0.1 dB passband ripple.

PB_{Ripple} 0.1 dB								
n	g1	g2	g3	g4	g5	g6	g7	g8
1	0.3052	1.0	-	-	-	-	-	-
2	0.8431	0.6220	1.3554	-	-	-	-	-
3	1.0316	1.1474	1.0316	1.0	-	-	-	-
4	1.1088	1.3062	1.7704	0.8181	1.3554	-	-	-
5	1.1468	1.3712	1.9750	1.3712	1.1468	1.0	-	-
6	1.1681	1.4040	2.0562	1.5171	1.9029	0.8618	1.3554	-
7	1.1812	1.4228	2.0967	1.5734	2.0967	1.4228	1.1812	1.0

where ω_1 and ω_2 represents passband corner angular frequencies, ω_0 is center angular frequency and FBW is $fractional\ bandwidth$ of the filter [45]. Center angular frequency ω_0 and fractional bandwidth of the filter are defined as

$$FBW = \frac{\omega_2 - \omega_2}{\omega_0} \tag{6.32}$$

and

$$\omega_0 = \sqrt{\omega_2 \omega_1}. \tag{6.33}$$

Applying frequency transformation in Equation 6.31 into reactive elements g_n shown in Figure 6.10 shows the fact that inductive and capacitive elements included in lowpass filter prototypes are converted to series and parallel inductor/capacitor resonant pairs [45]:

$$j\Omega g -> j\omega \frac{\Omega_c g}{FBW\,\omega_0} + \frac{1}{j\omega}\frac{\Omega_c \omega_0 g}{FBW}. \tag{6.34}$$

Element transformation from lowpass prototype to bandpass filter is illustrated in Figure 6.13. Derivation of real inductor and capacitor values are calculated by

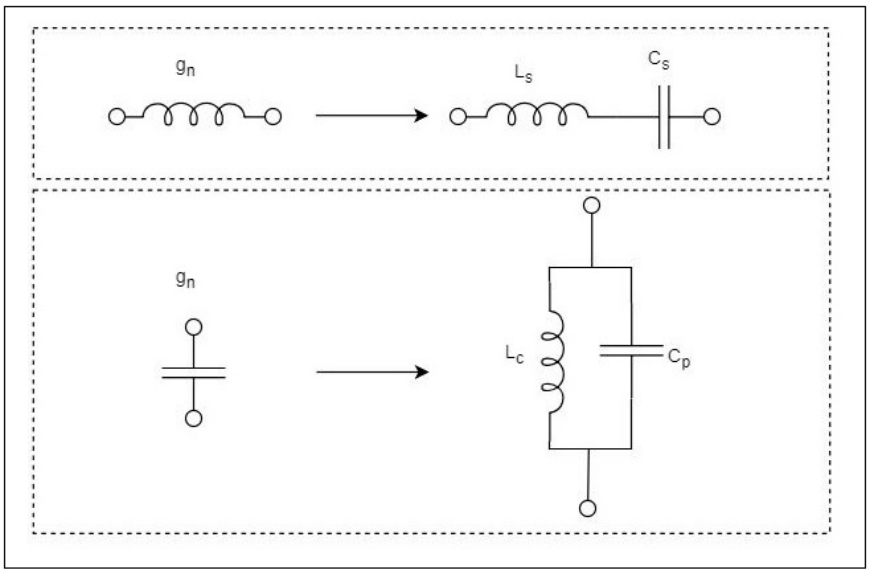


Figure 6.13 : Generalized lowpass to bandpass element transformation.

following set of equations where lowpass prototype filter coefficients are taken from coefficient tables

$$\begin{aligned} L_s &= (\frac{\Omega_c}{FBW\,\omega_0})Z_0 g \qquad C_s = \frac{1}{\omega_0^2 L_s} \\ C_p &= (\frac{\Omega_c}{FBW\,\omega_0})\frac{g}{Z_0} \quad L_p = \frac{1}{(\omega_0^2 C_p)} \end{aligned} \tag{6.35}$$

where Z_0 is the chosen characteristic impedance of the system. Lumped element representation of image reject filter with 8 GHz center frequency and 1 GHz bandwidth with calculated inductor/capacitor values is shown in Figure 6.14. Simulation

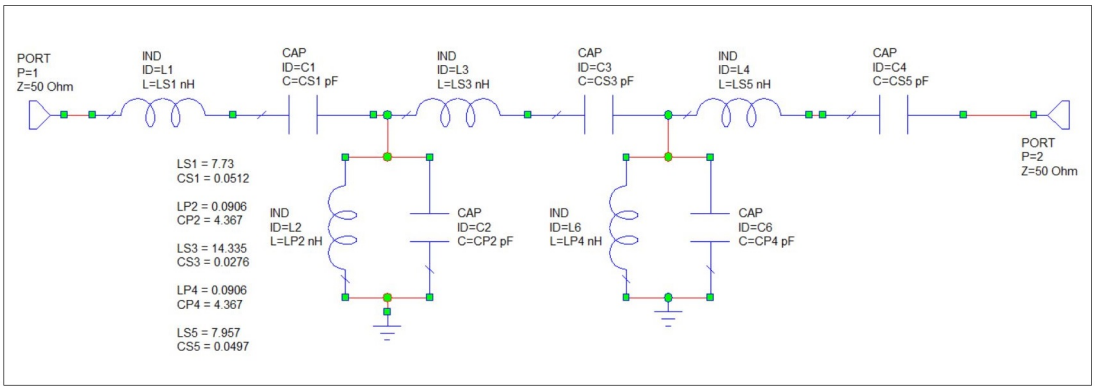


Figure 6.14 : Lumped element representation of fifth order Chebyshev type image reject filter.

results on AWR CAD software given in Figure 6.15 shows the fact that filter performance are perfectly aligned with design specifications. However calculated inductor and capacitor values can not be realized with real lumped elements due to limited inductance and capacitance ranges provided by manufacturers. Therefore distributed element realization is chosen for implementation phase. Although there

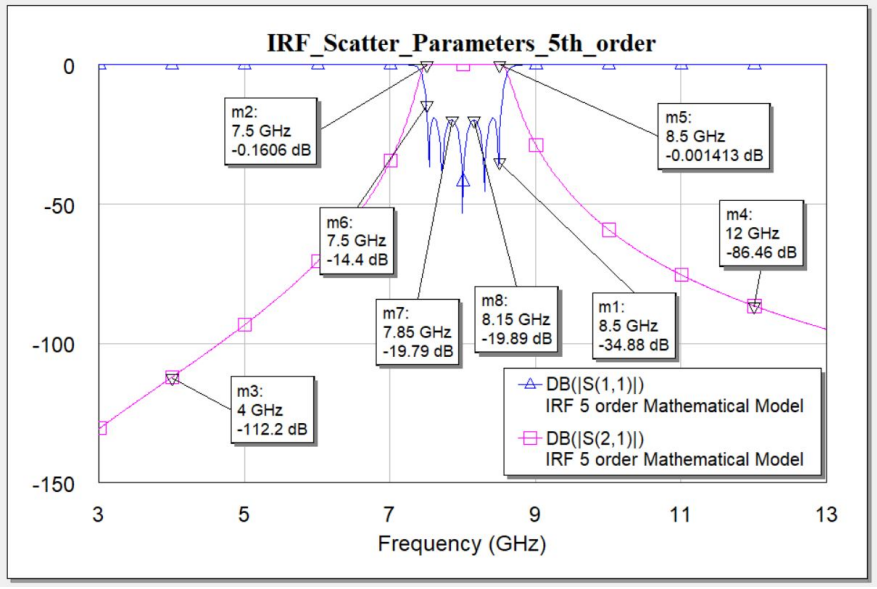


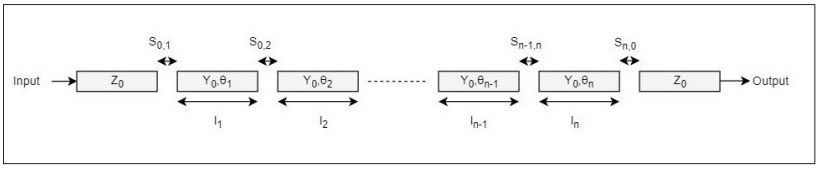
Figure 6.15 : Simulation results of lumped element fifth order image reject filter.

are several well-known theoratical methods such as Richard's Transformations and

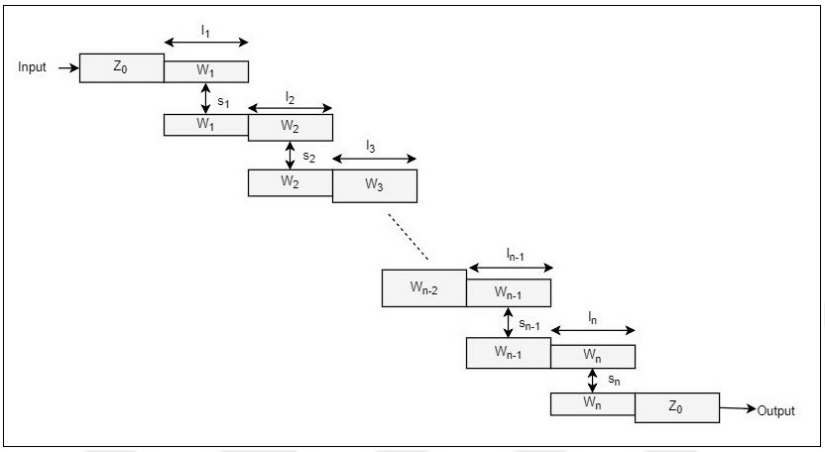
Kuroda Identities to convert filters with lumped element components to distrubuted element filters [46], calculation complexity exponentially increases with inclusion of parasitic effects, unintended couplings between distributed elements and fringing fields at the end of open microstrip lines. Computer aided microwave design softwares with 2-D electromagnetic simulation (EM) capabilities provides convenient approach for high-frequency distributed element type filter designs. 2-D EM analyzers utilizes Method of Moment (MoM) solver technique to achieve highly accurate simulation results. Therefore distrubuted element filter design has been performed on AXIEM 2-D EM simulation tool provided by AWR Design environment.

6.3.2 Distributed element image reject filter design

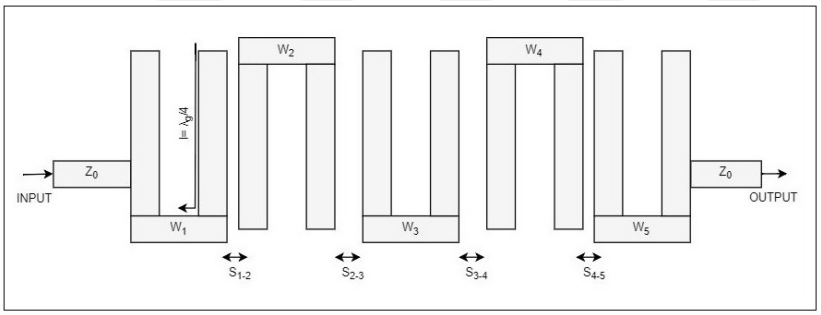
Instead of using lumped inductor and capacitors, microstrip lines with lengths lower than guided electrical length of operating frequency can be utilized to construct reactive elements associated with filter design. Most commonly used distributed element bandpass filter constructions which consist of microstrip lines are end-coupled filters, parallel-coupled line filters, interdigital filters and combline filters. Although interdigital and combline filters can be realized in smaller sizes, their implementation consists of short stubs that requires ground vias. Since manufacturing tolerances on shorting vias are harder to control in printed circuit technologies due to their vertical construction, performance variation between designed and manufactured filters proliferate with increasing operating frequency. On the other hand, parallel-coupled line filters exhibit several advantages in comparison with end-coupled filters. Parallel-coupled line filter lengths consume approximately half the space that is needed by end-coupled filters with same electrical characteristics. The gaps parallel-coupled line filters are wider therefore less effected by manufacturing tolerances where coupling spacing between resonators in end-coupled configuration are very narrow and critical to design performance [47]. Simplified planar models for microstrip end-coupled, paralel-coupled, hairpin and interdigital filters are illustriated in Figure 6.16. Hairpin bandpass filter type is chosen for image reject filter implementation on account of the fact that planar structure without grounding vias can be manufacturing with thin-film technology while preserving tight dimension



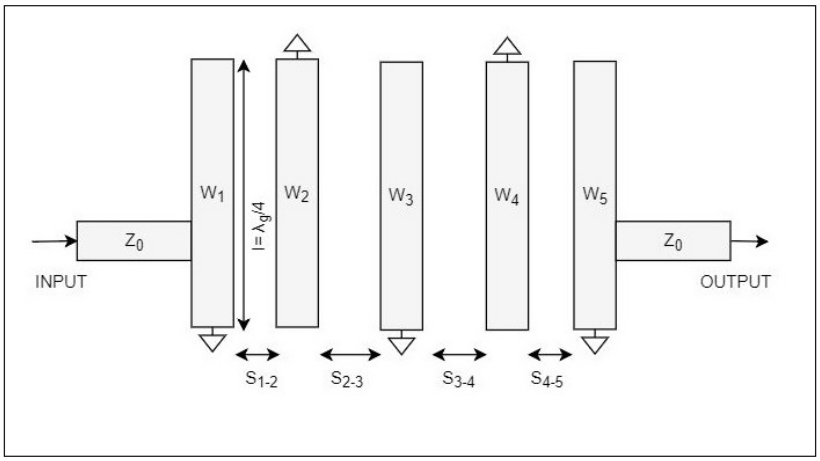
(a) End-Coupled bandpass filter.



(b) Parallel-Coupled bandpass filter.



(c) Hairpin bandpass filter.



(d) Interdigital bandpass filter.

Figure 6.16 : Microstrip bandpass filters simplified planar models.

tolerances. On the other hand, hairpin type bandpass filters occupy approximately half the area in comparison with parallel coupled type bandpass filters. Filter design has been performed on AWR Design Environment microwave analysis software. Dielectric substrate is defined as alumina with dielectric constant of 9.9 and 381um thickness. Simulations and optimisations steps are run through AXIEM 2D Planar simulator package. Initial design parameters for the filter taken as

$$\begin{aligned} W_1 = W_2 = W_3 = W_4 = W_5 = 360um \\ S_{1,2} = S_{2,3} = S_{3,4} = S_{4,5} = 150um \\ \lambda_g = 3620um \end{aligned} \tag{6.36}$$

where W_n dimensions represent coupled line widths that are equal to characteristic impedance of 50Ω and $S_{n,n+1}$ dimensions are the coupling spacing between U shaped resonators. Initial design and its simulation results are shown in Figure 6.17 and Figure 6.18 respectively. Due to fringing field capacitances associated with open-ended microstrip lines and unintended coupling between non-adjacent resonators, center frequency of the filter is shifted to higher frequencies and bandwidth of the filter is widened. Although initial design performance satisfy the image rejection requirement, insertion loss within passband shows high variation because of the poor return loss performance. Filter dimensions and consequently performance has been optimized

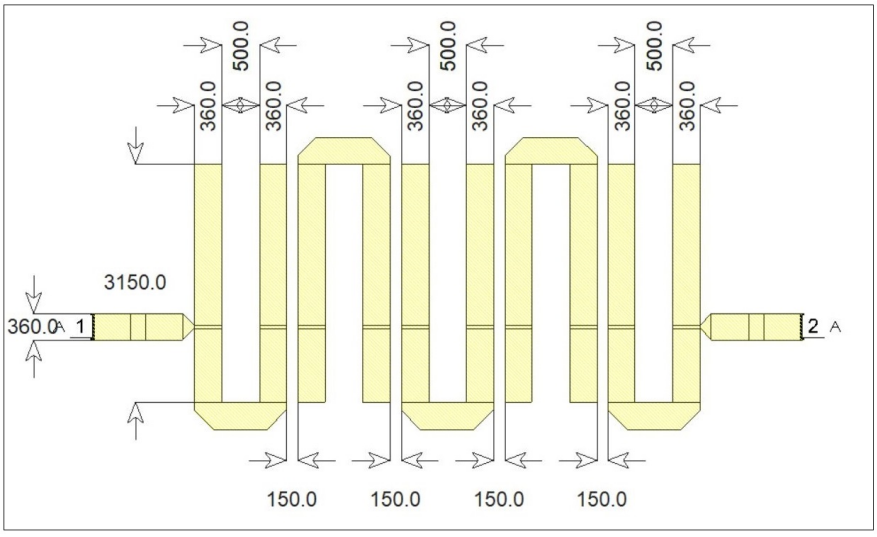


Figure 6.17 : Hairpin image reject filter initial dimensions.

by utilizing *Particle Swarm* optimization method on AXIEM planar electromagnetic

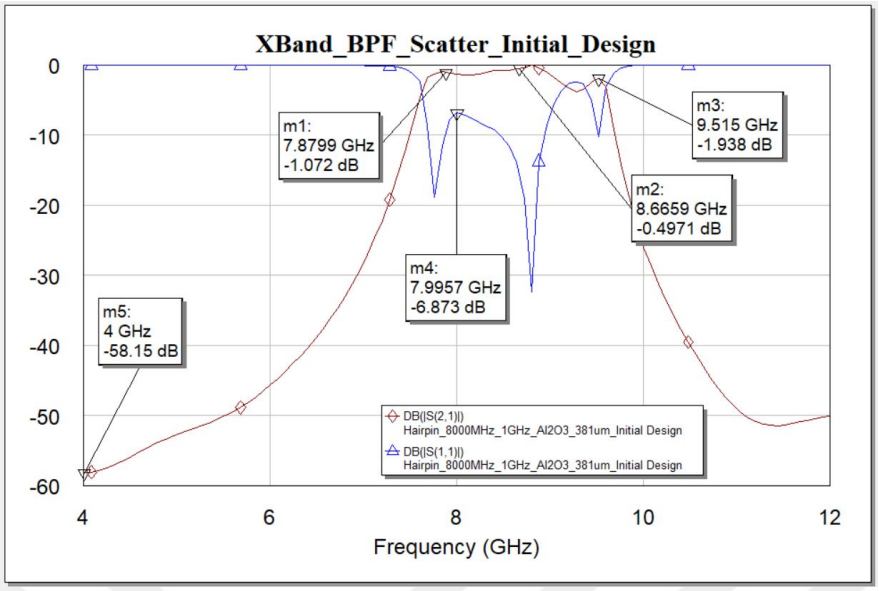


Figure 6.18 : Hairpin image reject filter initial design simulation results.

simulator. Optimization constraints are given as:

$$\begin{aligned} S21 &< -50dB \;\; within \; 4000-5000 \; MHz \\ S11 &< -20dB \;\; within \; 7500-8500 \; MHz. \end{aligned} \tag{6.37}$$

Obtained filter dimensions and simulation results are shown in Figure 6.19 and Figure 6.20 respectively. Achieved filter performance versus target electrical specifications are listed in Table 6.7. 2-D and 3-D layout illustration of designed Image Reject

Table 6.7 : Achieved vs target electrical specification of microstrip image reject filter.

Symbol	***Parameter***	***Target Specification***	***Simulation Result***	***Unit***
f_c	Center Frequency	8000	8100	MHz
BW_{1dB}	1dB Bandwidth	>1000	>1600	MHz
IL	Insertion Loss	<2dB	<0.5	dB
IRL	Input Return Loss	<-10	<-20	dB
ORL	Output Return Loss	<-10	<-20	dB
IR	Image Rejection	>50 @ LO-2IF	54 @ LO-2IF	dB

Bandpass Filter MIC board is shown in Figure 6.21 and Figure 6.22 respectively. Image Reject Filter MIC design consist of alumina substrate, microstrip 50 ohm interconnection and coupled microstrip transmission lines. Microstrip transmission lines are centered on the alumina carrier for convenient assembly with other designed MIC boards. End points of RF transmission line are enlarged to add capacitive

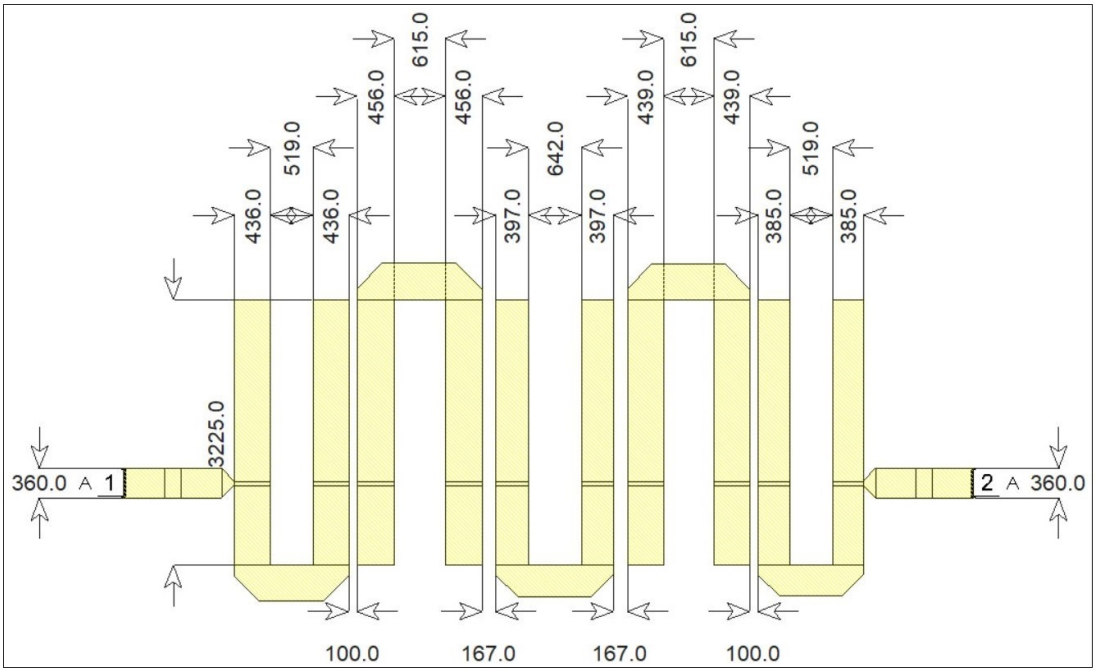


Figure 6.19 : Hairpin image reject optimized filter dimensions.

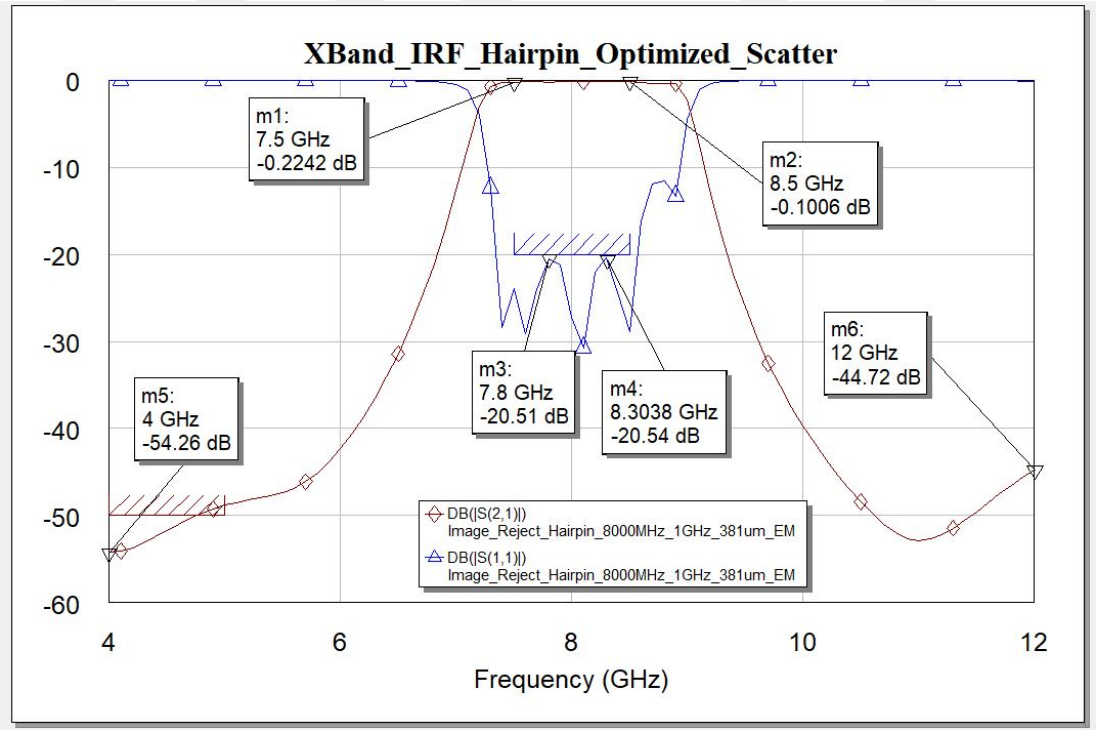


Figure 6.20 : Hairpin image reject optimized filter simulation results.

reactance to compansate inductive effect of bonding wires. Total area of the Image Reject Filter MIC board is confined within $128mm^2$.

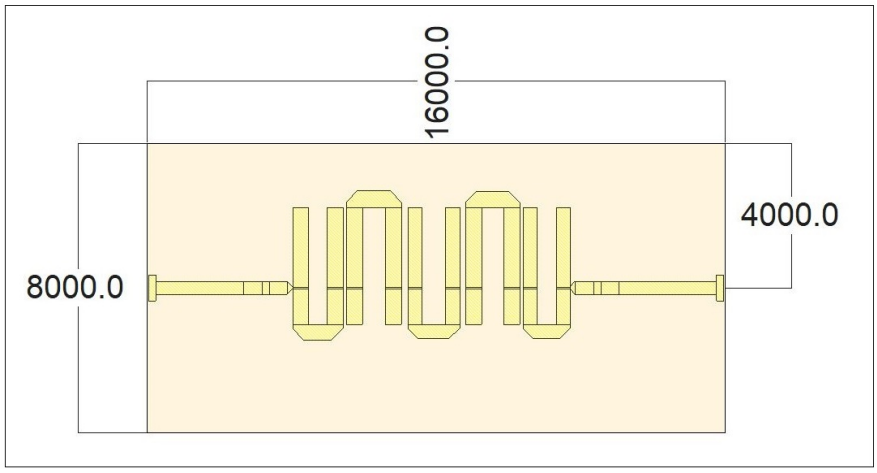


Figure 6.21 : Hairpin image reject filter 2-D visual.

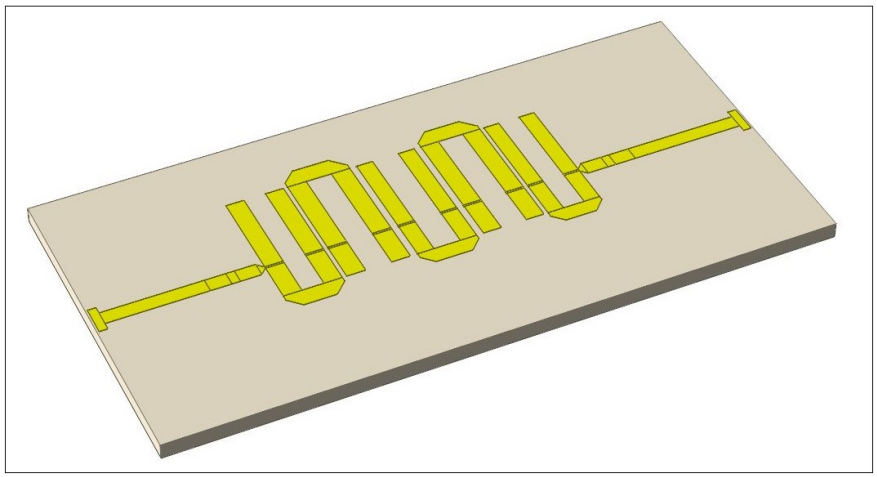


Figure 6.22 : Hairpin image reject filter 3-D visual.

6.4 Mixer MIC Design

Mixer microwave integrated circuit (MIC) is designed to accomplish frequency downconversion operation. Electrical parameters of the selected part has been given in Table 5.2. Double balanced design architecture allows rejection of even order intermodulation products of both RF and LO signals at the mixer output. MxN spurious output table is given in Figure 6.23.

	nLO				
mRF	0	1	2	3	4
0	xx	6.5	33.5	30.5	29.5
1	17.5	0	37.5	38.5	57.5
2	>75	69.5	66.5	66.5	> 75
3	> 75	> 75	> 75	62.5	> 75
4	> 75	> 75	> 75	> 75	> 75
RF = 10.1 GHz @ -10 dBm LO = 10.0 GHz @ +13 dBm All values in dBc below the IF output power level (1RF - 1LO)					

Figure 6.23 : Spurious output table of double balanced mixer die.

Conversion gain of the mixer varies between -7 to -6 dB within temperature range of $-40°C\ to\ +85°C$ while driving the mixer with +13dBm local oscillator signal. As local oscillator drivel level decreases, conversion gain performance of the mixer diminished due to inadequate switching of internal microwave diodes utilized inside mixer die. Conversion gain versus temperature and LO drive level is given in Figure 6.24 and Figure 6.25 respectively. Return loss performance of the chosen mixer

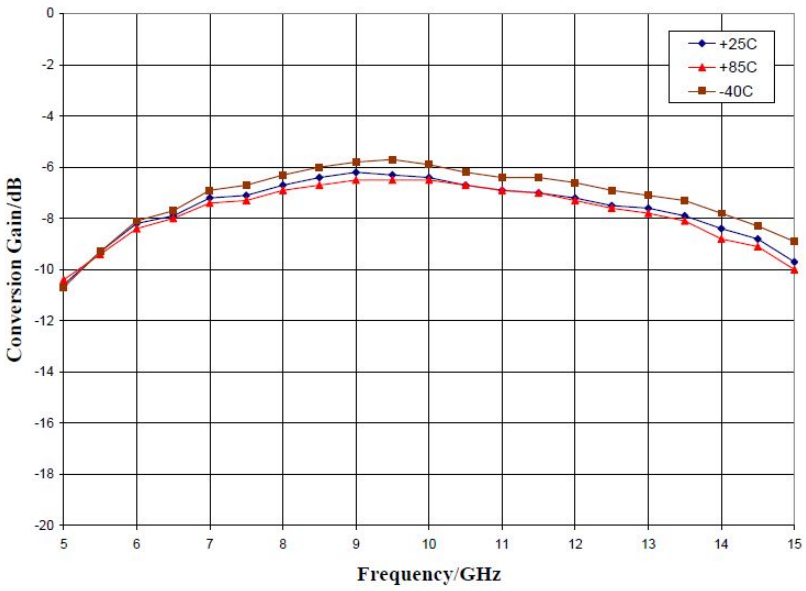


Figure 6.24 : Mixer conversion gain vs temperature graph.

die presents broadband RF and LO input match within 8-14 GHz frequency range which is shown in Figure 6.26. Although RF and LO return loss performance of the mixer part can be improved by implementing external microstrip matching circuit

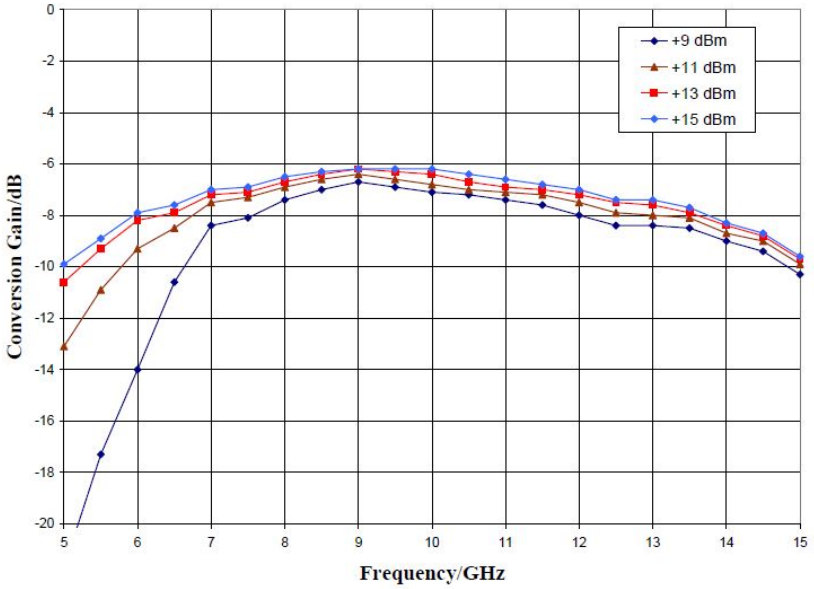


Figure 6.25 : Mixer conversion gain vs LO drive level graph.

within frequency band of interest, design of impedance matching circuit requires scatter parameters of the mixer part. However; non-linear operation of mixers result in variation of scatter parameters with different LO drive power levels. Therefore, scatter parameters of the mixer part should be obtained by characterisation based on application parameters. In order to provide a opportunity to improve return loss performance of the manufactured Mixer MIC, impedance tuning pads has been placed on the carrier. 2-D and 3-D layout illustration of designed Mixer MIC board is shown in Figure 6.27 and Figure 6.28 respectively. Mixer MIC design consist of mixer die part, alumina substrate, microstrip 50 ohm interconnection and RF grounding vias. Since double balanced mixer is a passive microwave circuit, no biasing and decoupling scheme is required in design. Interconnection between microstrip lines and Mixer MMIC die are implemented by 25um gold wires. Several tuning pads are placed adjacent to RF and LO input lines to provide external matching option in testing phase. Microstrip transmission lines are centered on the alumina carrier for convenient assembly with other designed MIC boards. End points of RF transmission line are enlarged to add capacitive reactance to compansate inductive effect of bonding wires. Total area of the Mixer MIC board is confined within $96mm^2$.

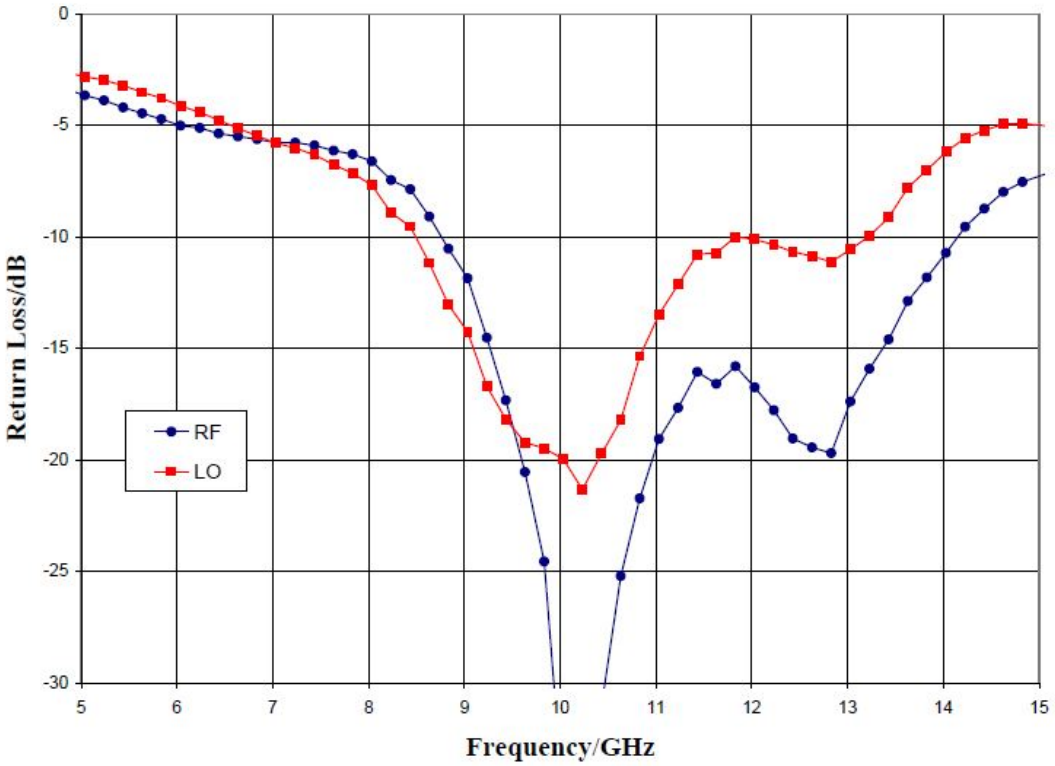


Figure 6.26 : Mixer RF and LO input return loss graph.

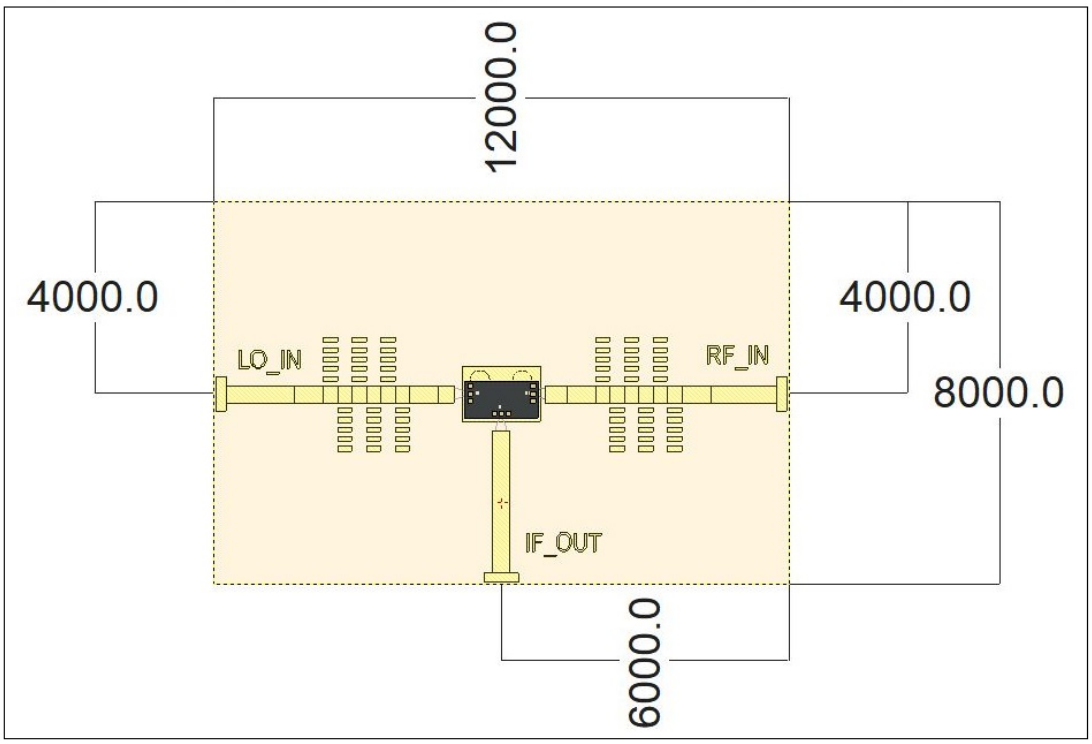


Figure 6.27 : Mixer MIC 2-D visual.

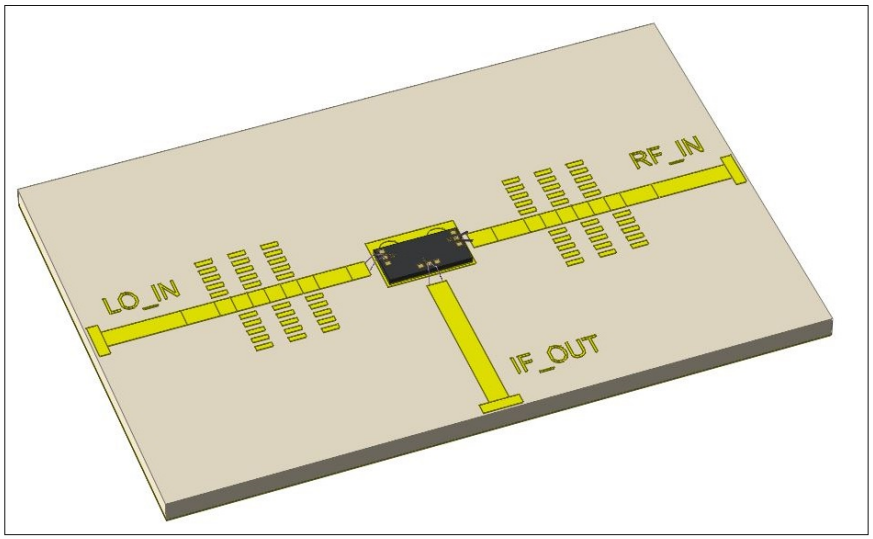


Figure 6.28 : Mixer MIC 3-D visual.

6.5 Local Oscillator Frequency Multiplier MIC Design

Direct synthesis of high frequency local oscillator signal presents various challanges to designers. One of these challanges arise from limitations of input frequency range of locking circuits such as PLLs. On the other hand, phase noise performance of the oscillator source degrades as oscillation frequency increases. Direct synthesis of frequencies than are higher than S-Band, prevents to use packaged lumped elements at oscillator design since parasitics associated with packages limits the highest achivable frequency range of LC resonators. Frequency multiplication method enables the use stable local oscillator source with much lower frequency which will be multiplied to achieve required frequency range at the end of LO signal chain. SAR Receiver frontend LO signal that will be driven to downconversion mixer stage is located in C-Band spectrum. Frequency multiplication method is chosen to enable lumped element VCO design to generate S-Band signal that can be fed back to phased-locked-loop circuit. Stable oscillator source is multiplied by order of two to achieve required C-Band LO signal.

6.5.1 Frequency multiplier topologies

Frequency multipliers are non-linear microwave circuits that generate multiples of input frequency at the output spectrum. In case of applying a continous sine wave

of $V_{IN}(t)$ to frequency multiplier

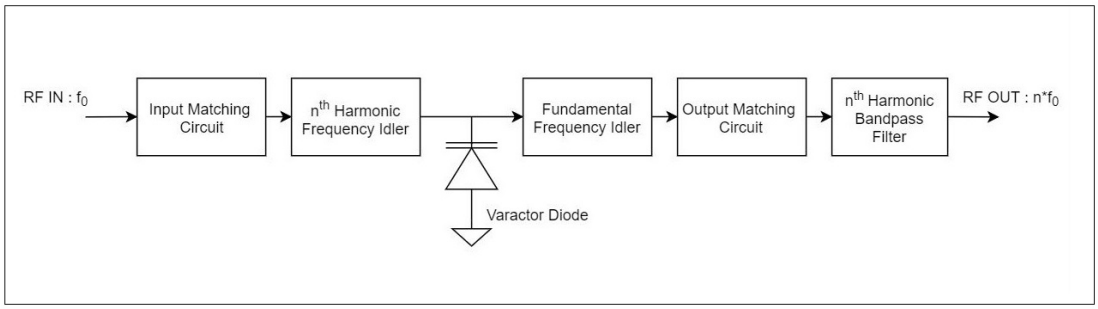
$$V_{IN}(t) = V_i cos[\omega_{IN} t + \phi_{IN}] \tag{6.38}$$

where V_i represents amplitude constant, ω_{IN} is frequency in radian and ϕ_{IN} is the phase of the input signal, resulting output signal can be expressed as:

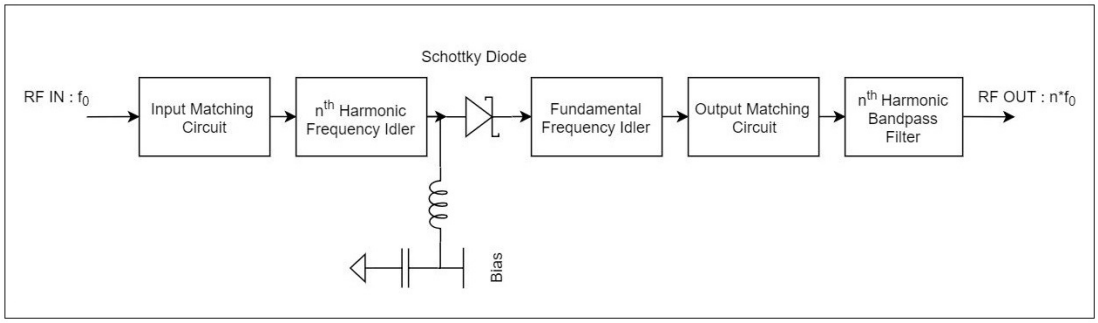
$$V_{OUT}(t) = AV_i cos[n(\omega_{IN} t + \phi_{IN}) + \Phi_{Mult.}] \tag{6.39}$$

where n is the multiplication factor, $\Phi_{Mult.}$ is the phase of the multiplier itself and A represents the gain of the frequency multiplier circuit. Frequency multipliers can be divided into two subcategories as passive and active multipliers depending on biasing required for the circuits. Most commonly used non-linear elements for passive frequency multipliers are schottky diodes, varactor diodes and step-recovery diodes. Each diode type presents different conversion response function due to their distinct junction voltage-current characteristics. Frequency multiplier designs that consists of varactor or step-recovery diodes have highly reactive input and output impedances because of the fact that varactor and step-recovery diode based designs take advantage of diodes' non-linear capacitance characteristics. Since broadband impedance matching to purely reactive devices results in impractical matching solutions, they are usually used for narrowband applications. On the other hand, schottky diodes can be used to achieve relatively broadband frequency response due to their resistive part in their impedance. However, schottky diode frequency multipliers exhibit reduced conversion efficiency in comparison with varactor or step-recovery diode frequency multipliers due to aforementioned resistive impedance characteristics. Varactor and schottky diode based simplified frequency multiplier circuits have been illustrated in Figure 6.29. Harmonic idler circuits are resonant LC or microstrip structure that are used to suppress generated harmonic signal in order to reduce the leakage to input port and prevent any unwanted further multiplication. Purpose of the fundamental idler circuits are similar to harmonic idlers which is to suppress fundamental signal presented at the multiplier output. Input and output matching circuits provide optimum power transfer to non-linear device for efficient frequency conversion. Bandpass filter centered at the desired harmonic frequency

ensure high fundamental signal and unwanted harmonic signal rejection performance [20] [48] [21]. Active frequency multipliers exploit the non-linear characteristic of the



(a) Varactor diode multiplier.



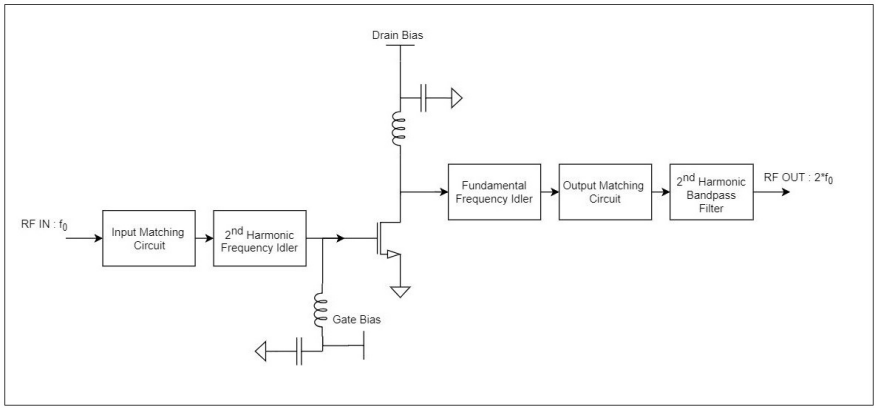
(b) Schottky diode multiplier.

Figure 6.29 : Simplified diode based frequency multipliers.

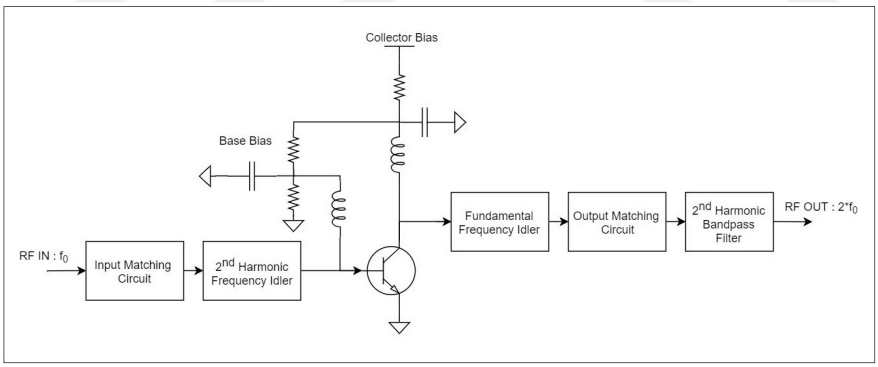
microwave devices that are operated in cut-off and saturation region. Main advantages and disadvantages of the active multiplier design topology in comparison with passive diode multipliers can be listed as;

- Advantages:
  - Lower input signal drive level requirement
  - Conversion gain instead of conversion loss
  - Suitable for wideband operation due to practical broadband matching.
- Disadvantages:
  - Consumes power even though its small
  - Requires DC biasing circuit
  - Very hard to achieve multiplication factor more than two (n>2).

Microwave field effect transistors and bipolar junction transistors can be used to implement frequency multipliers with very low noise and conversion gain over wide input bandwidths. Due to their inherent signal amplification characteristics, input signal drive level can be kept low which in turn removes the driver amplification stage from the design that is required for passive diode based multipliers. Therefore active frequency multiplier topology is chosen for local oscillator frequency multiplier circuit design. Simplified representation of active frequency multiplier circuits in doubler configuration are shown in Figure 6.30.



(a) FET frequency doubler.



(b) BJT frequency doubler.

Figure 6.30 : Simplified active frequency multipliers in doubler configuration.

6.5.2 S-Band to C-Band frequency doubler design

Small number of manufacturers provide space qualified discrete microwave FETs and BJTs due to very limited number of applications they are required. On the other hand; beside reliability issues, electrical characteristic of the selected non-linear element should be compatible for the application such as input and output impedance, bias

voltages, maximum attainable gain and noise figure. Among the limited number of parts, SiGe Heterojunction Bipolar Transistors (HBT) manufactured by Infineon provide high gain, low noise figure, medium output power and single bias supply operation with transition frequency of 40 GHz . Furthermore, SiGe HBTs' input and output impedance characteristics are well suited for practical matching to frequency of operation up to C-Band. Electrical characteristics of chosen SiGe HBT are listed in Table 6.8.

Table 6.8 : SiGe HBT electrical characteristics.

RF Electrical Characteristics					
Parameter	**Symbol**	**min.**	**typ.**	**max.**	**unit**
Transition Frequency I_C = 30mA, V_{CE} = 3V, f=2.0 GHz	F_t	20	22	-	GHz
Collector-Base Capacitance V_{CB}= 2V, V_{BE} =0, f=1 MHz	C_{CB}	-	0.14	0.9	pF
Collector-Emitter Capacitance V_{EB}= 0.5V, V_{CB} = 0, f=1 MHz	C_{CE}	-	0.46	0.85	pF
Emitter-Base Capacitance V_{EB} = 0.5V, V_{CB} = 0, f=1 MHz	C_{EB}	-	0.67	3	pF
Noise Figure I_C = 5mA, V_{CE} = 2V, f= 1.8GHz	NF	-	1.1	1.7	dB
Power Gain I_C=20mA, V_{CE}=2V, f=1.8 GHz, Zs=Zl=50 Ohm	Gms	-	21	-	dB
1dB Compression Point I_C=20mA, V_{CE}=2V, f=1.8 GHz	P_{1dB}	-	12	-	dBm

6.5.3 Theory of operation

Bipolar transistors can be considered as voltage controlled current sources. Voltage applied between base-emitter junction of the transistor V_{BE} induce current flow through base of the transistor. Base current I_B is multiplied by the gain of the transistor and generates amplified collector current I_C. Simplified π model of a microwave bipolar junction transistor with common emitter configuration is shown in Figure 6.31 [49]. Small-signal relationship between base-emitter voltage and collector current can be expressed as

$$I_C = I_S(e^{V_{BE}/V_T} - 1) \tag{6.40}$$

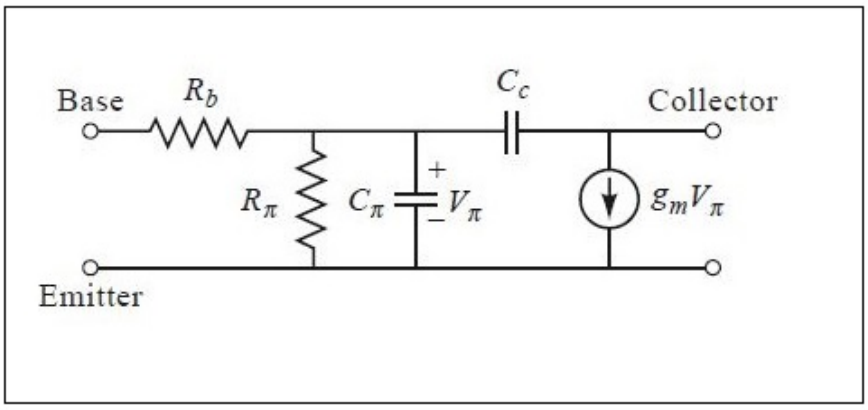


Figure 6.31 : Bipolar junction transistor.

where I_S is saturation current of the transistor and V_T represents thermal voltage. Expanding exponential term with Taylor series result in

$$I_C \approx I_S[1 + (V_{BE}/V_T) + \frac{(V_{BE}/V_T)^2}{2!} + \frac{(V_{BE}/V_T)^3}{3!} + ...]. \tag{6.41}$$

Considering applying a sinusoidal waveform to base-emitter junction of the transistor with DC bias of V_{DC}, V_{BE} becomes

$$V_{BE}(t) = V_{DC} + Acos(\omega t + \phi). \tag{6.42}$$

Inserting equation 6.42 into 6.41 and neglecting higher order terms reveals the non-linear function between base-emitter voltage and collector current;

$$I_C(t) \approx I_S[1 + (V_{BE}/V_T) + \frac{1}{2V_T^2}(V_{DC} + Acos(\omega t + \phi))^2] \tag{6.43}$$

$$I_C(t) \approx I_S[1 + (V_{BE}/V_T) + \frac{1}{2V_T^2}(V_{DC}^2 + 2V_{DC}Acos(\omega t + \phi)) + \frac{A^2}{2}cos(2\omega t + 2\phi))]. \tag{6.44}$$

Equation 6.44 shows the fact that collector current carries DC, fundamental and second harmonic component at the output spectrum where second harmonic power level is related to squared function of the input power level. Strong non-linear components can be generated by abrupt limitation on collector current flow. RF signal driven to base of the BJT with adequate power level results in continous switching action which in turn generates harmonically rich output spectrum. Simplified base-emitter voltage, collector current and collector-emitter voltage waveforms of an microwave BJT frequency multiplier are illustriated in Figure 6.32.

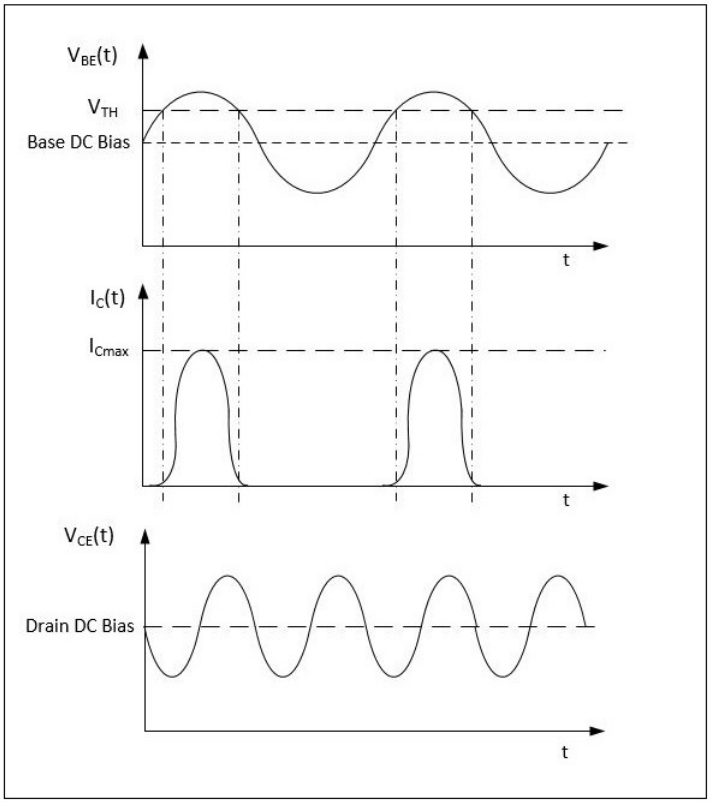


Figure 6.32 : Microwave BJT frequency multiplier signal waveforms.

6.5.4 HBT modeling

Design of a non-linear microwave circuit requires detailed large-signal model for the non-linear elements used in the design. Large-signal model enable to see circuit response in all operation regions that is active, saturated and cut-off operations throughout computer aided simulations. Detail and complexity of the model directly effects the accuracy of the simulations results in comparison with actual performance of the manufactured samples. Consequently, several device models has been developed for HBTs in order to achieve accurate CAD simulation results. First practical large signal BJT model was introduced by Ebers and Moll [50]. Fifteen years later, Gummel and Poon improved the model by involving Early Effect, Sah-Noyce-Shockley Effect, Webster Effect and Kirk Effect that are identified after studies of Ebers and Moll [51]. Even though various enhanced HBT models published by the researchers based on Ebers-Moll and Gummel-Poon models, Gummel-Poon model is still most widely used large-signal model for non-linear simulation environments. Although Heterojunction Bipolar Transistors (HBTs) present significant differences with respect

to Bipolar Junction Transistors (BJTs) due to different semiconductor materials and physical structure used in construction and manufacturing, Gummel-Poon model elegantly covers the HBTs as well as BJTs. Schematical representation and SPICE parameters of the HBT Gummel-Poon model has been given in Figure 6.33 and Table 6.9 respectively. Large-signal spice model also includes parasitic capacitances and inductances owing to packaging of the device.

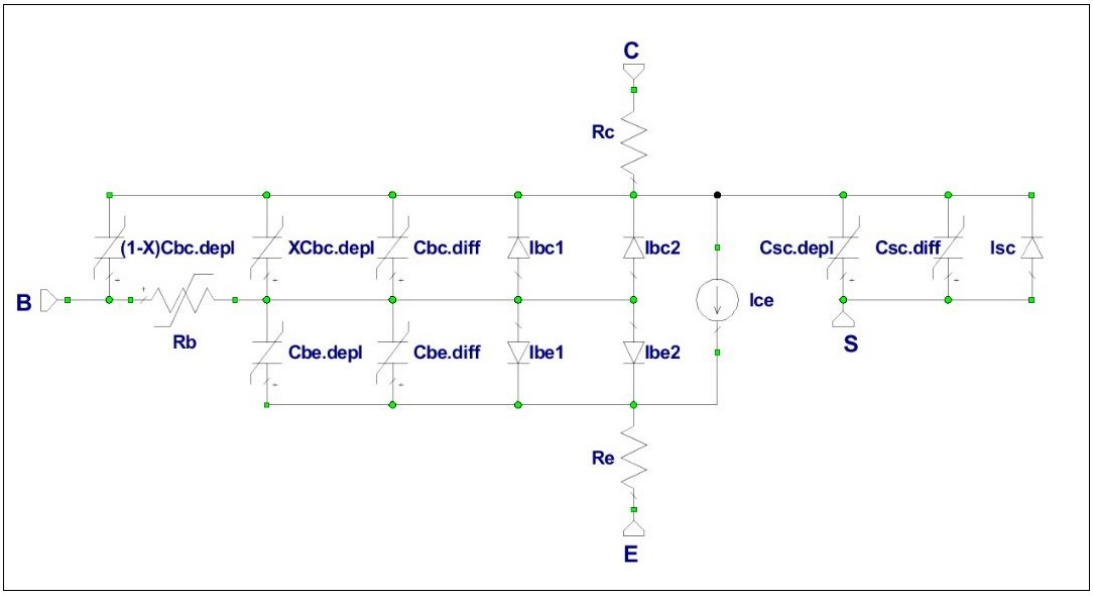


Figure 6.33 : Gummel-Poon bipolar junction transistor model.

6.5.5 SiGe HBT characterisation

AC and DC analyses has been performed on constructed HBT SPICE model with parameters listed in Table 6.9. Firstly, current-voltage relationships of the transistor with DC voltage excition is derived to choose proper operating bias point. This characteristics are shown in well known current-voltage (IV Curve) curves. Secondly, AC analysis with several biasing condition has been run to understand impedance behaviour of the transistor based on different bias voltage and currents. However linear AC analysis on the transistor is not sufficient to properly characterize input and output impedances of the element since frequency multiplication with high conversion gain can be achieved with highly non-linear operating conditions. Therefore non-linear AC

Table 6.9 : SiGe HBT Gummel-Poon model SPICE parameters.

Parameter	Abbreviation	Value	Unit
Base-Emitter Parasitic Capacitance	CBEPAR	5.592E-014	F
Base-Collector Parasitic Capacitance	CBCPAR	1.143E-013	F
Collector-Emitter Parasitic Capacitance	CCEPAR	1.596E-013	F
Base Parasitic Inductance	LB	7.42E-010	H
Emitter Parasitic Inductance	LE	1.656E-010	H
Collector Parasitic Inductance	LC	7.7E-010	H
Base-Emitter Package Capacitance	CBEPCK	4.741E-014	F
Base-Collector Package Capacitance	CBCPCK	1.135E-015	F
Collector-Emitter Package Capacitance	CCEPCK	4.48E-014	F
Base Package Inductance	LBX	2.339E-010	H
Emitter Package Inductance	LEX	4.189E-011	H
Collector Package Inductance	LCX	2.243E-010	H
Substrate Resistance	RSub	176.4	Ohm
Saturation Current	IS	3.753E-017	A
Forward Current Gain	BF	140.8	-
Forward Ideality Factor	NF	0.9996	-
Forward Early Voltage	VAF	59.18	V
Forward Current Knee	IKF	0.6604	mA
Base-Emitter Leakage Current	ISE	1E-014	A
Base-Emitter Leakage Ideality Factor	NE	2	-
Reverse Current Gain	BR	13.61	-
Reverse Ideality Factor	NR	0.9938	-
Reverse Early Voltage	VAR	2.685	V
Reverse Current Knee	IKR	0.007013	mA
Base-Collector Leakage Current	ISC	3.49E-016	mA
Base-Collector Leakage Ideality Factor	NC	1.5	-
Base Resistance	RB	11.99	Ohm
Minimum High-Current Base Resistance	RBM	1.521	Ohm
Emitter Resistance	RE	0.3062	Ohm
Collector Resistance	RC	2.152	Ohm
Temperature Scaling Term for Current Gain	XTB	0.1187	-
Energy Gap	EG	1.11	
Temperature Scaling Term	XTI	4.162	-
Base-Emitter Junction Intrinsic Capacitance	CJE	5.621E-013	F
Base-Emitter Built-In Potential	VJE	0.4892	V
Base-Emitter Grading Coefficient	MJE	0.2565	-
Forward Transit Time	TF	4.83855E-012	ns
Coefficient for Bias Dependance of TF	XTF	6.245	-
Coefficient for VBC Dependance of TF	VTF	10.66	-
High Current Parameter for TF	ITF	0.5436	-
Base-Collector Junction Intrinsic Capacitance	CJC	1.227E-013	F
Base-Collector Built-In Potential	VJC	0.8453	V
Base-Collector Grading Coefficient	MJC	0.6803	-
Reverse Transit Time	TR	4.7E-009	ns
Coefficient of Forward-Bias Depletion	FC	0.4148	-

analysis applied to transistor model with different power levels. Obtained nonlinear scatter parameters are used for impedance matching circuitry in following subsections.

6.5.5.1 DC-IV curve

Main purpose of DC-IV curves is the obtain insight on behaviour of the non-linear devices. Sweeping collector voltage and base current simultaneously and plotting the correlated collector current-voltage values in the graph produce representation of the device behaviour in static biasing conditions, which is DC-IV curves. Collector voltage and base current are limited to 4.0 VDC and 0.3 mA respectively due to maximum electrical specification of the chosen HBT. Base current is swept between 0 to 0.3mA with 0.05mA resolution. Obtained DC-IV curve of the SiGe HBT is shown in Figure 6.34.

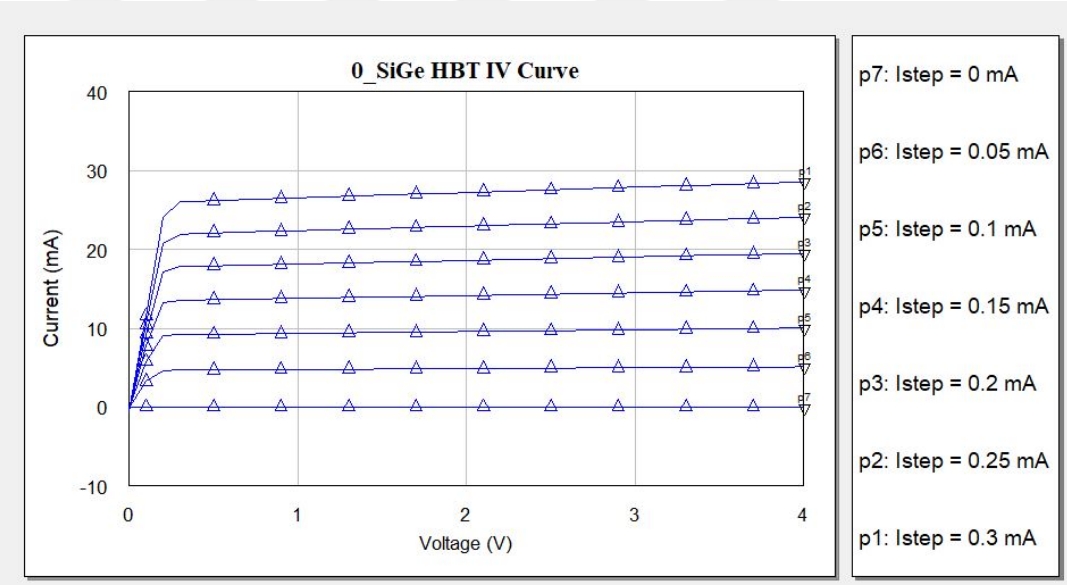


Figure 6.34 : SiGe HBT DC-IV curve.

6.5.5.2 Linear scatter parameters

HBT port impedances varies with different biasing points. Understanding and avoiding the bias conditions which causes large impedance changes on the transistor ports simplify the impedance matching stage that will take place in further design process. Linear input and output normalized impedances of the HBT within frequency range of 1-8GHz are casted on smith chart and shown in Figure 6.35. Base current has been

swept between 0.05mA to 0.3mA with 0.05mA resolution. As it can be seen from

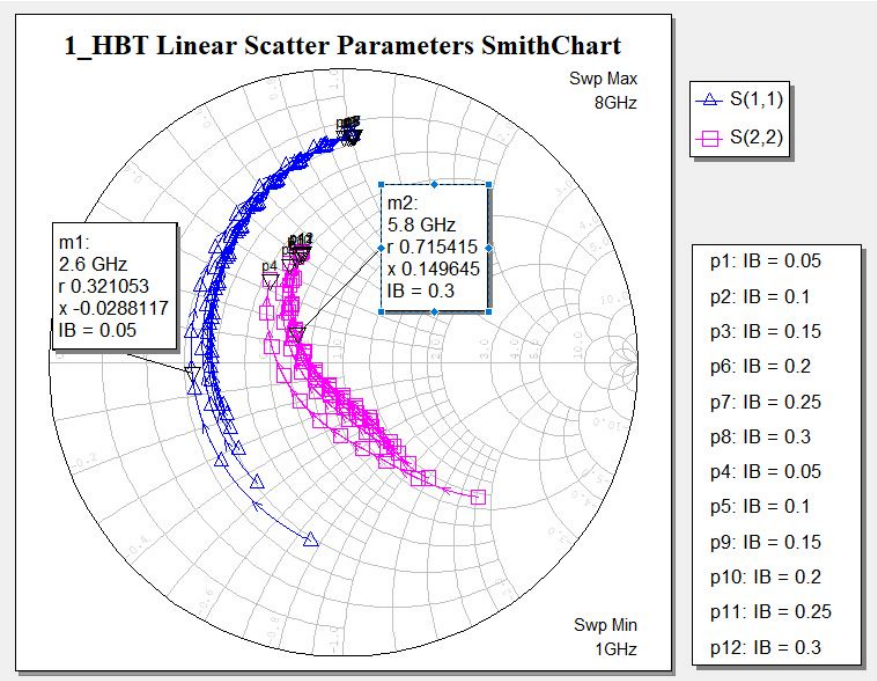


Figure 6.35 : SiGe HBT linear scatter parameters - Smith Chart.

Figure 6.35, base current value of 50uA slightly lowers the resistive part of the port impedances. Therefore HBT bias circuit will be adjusted to allow higher base current than 50uA to prevent bias related impedance changes on the transistor ports.

6.5.5.3 Non-Linear scatter parameters

Aside from biasing point dependency, port impedances of the HBT are also effected by AC signal power level presented on base and collector ports due to intrinsic P-N junctions residing in physical structure of HBT which acts like forward biased diodes in high drive levels. Nonlinear input and output normalized impedances of the HBT within frequency range of 1-8 GHz are casted on smith chart and shown in Figure 6.36. Base current and collector-emitter voltage has been taken as 0.1mA and 4.0 VDC respectively. Input power drive level is swept between -5 to +5 dBm. Figure 6.36 shows the fact that input impedance of the HBT with common emitter configuration exhibit susceptability to drive levels. As power level of the AC input signal increases, port impedances present negative reactances. Consequently, impedance matching will

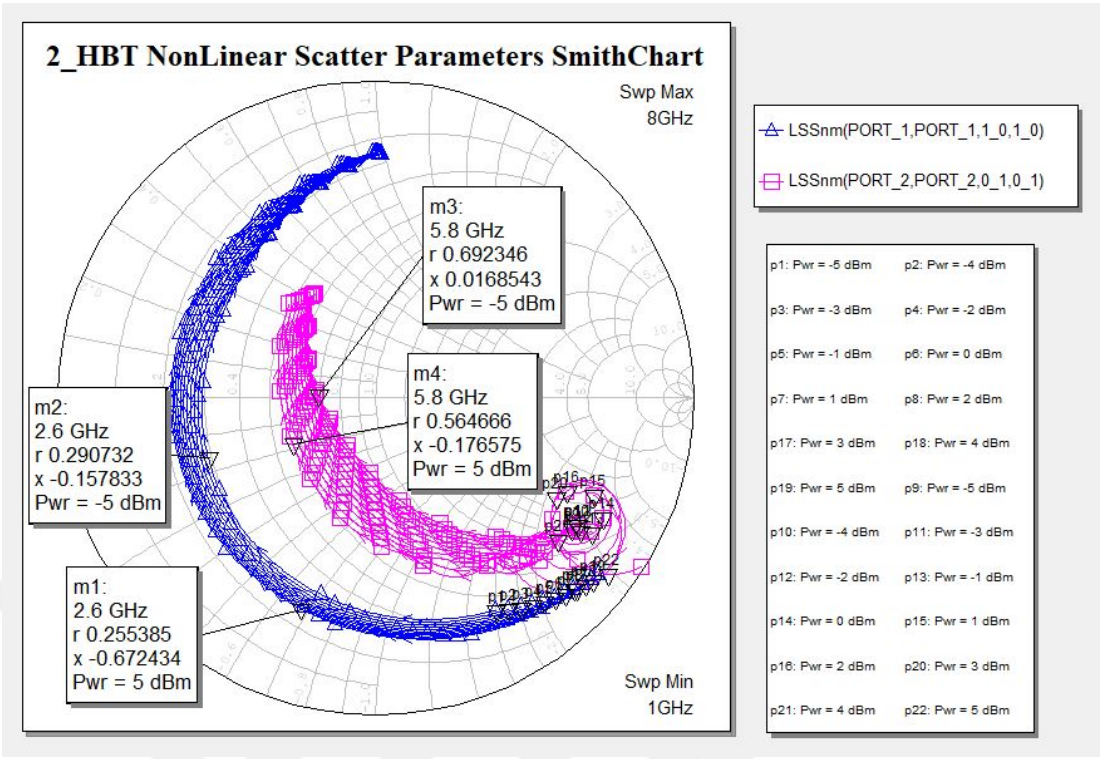


Figure 6.36 : SiGe HBT non-linear scatter parameters - Smith Chart.

be performed after defining DC bias points and fundamental signal drive level in the process of HBT based frequency multiplier design.

6.5.5.4 Conversion gain

Conversion gain in frequency doublers is defined as ratio of 2nd harmonic output signal power to fundamental input signal power:

$$G_{CONV} = S21[f_0 * 2][f_0] = \frac{P_{OUT}[2^{nd} Harmonic]}{P_{IN}[Fundamental]}. \tag{6.45}$$

Since conversion gain is one of the most important electrical parameters that defines performance of the active multipliers, choosing optimum biasing point and drive level is considered as a crucial design step. In order to investigate the conversion gain of the HBT with various bias and input drive level condition, non-linear swept analysis has been performed on the unmatched HBT. Input frequency and output frequency is fixed to 2600 and 5800 MHz respectively. Swept parameters are listed below with limit conditions:

- V_{CE} : 1.0V-4.0V with 1V steps

- I_B : 0.1mA-0.3mA with 0.1mA steps
- PWR_{IN} : -5 to +5 dBm with 1dB steps.

Conversion gain graph with aforementioned swept parameters has been given in Figure 6.37. Blue lines, pink lines and brown lines represents base current bias with 0.1mA,

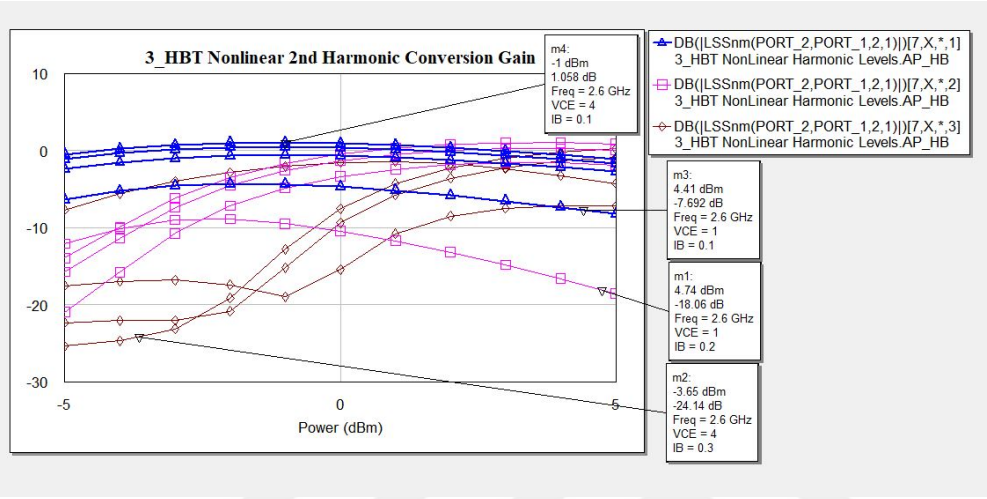


Figure 6.37 : SiGe HBT non-linear conversion gain graph.

0.2mA and 0.3mA respectively. Conversion gain graph indicates the fact that highest conversion gain can be achieved by fundamental signal drive level and bias conditions listed in Table 6.10.

Table 6.10 : Frequency doubler bias and fundamental drive conditions.

Parameter	Abbreviation	Value	Unit
Collector-Emitter Bias Voltage	V_{CE}	4.0	V
Base Current	I_B	0.1	mA
Fundamental Input Drive Level	$PIN_{Fund.}$	-1	dBm

6.5.5.5 Dynamic load line

Defined DC collector bias voltage and base current are applied to microwave transistor through voltage divider and current limiter resistors. Schematic diagram of bias circuit has been given in Figure 6.38. Dynamic load line analysis is performed to understand if circuit is operating within non-linear region with chosen bias points and input drive level. Dynamic load line of the frequency multiplier is cast onto DC-IV curve of

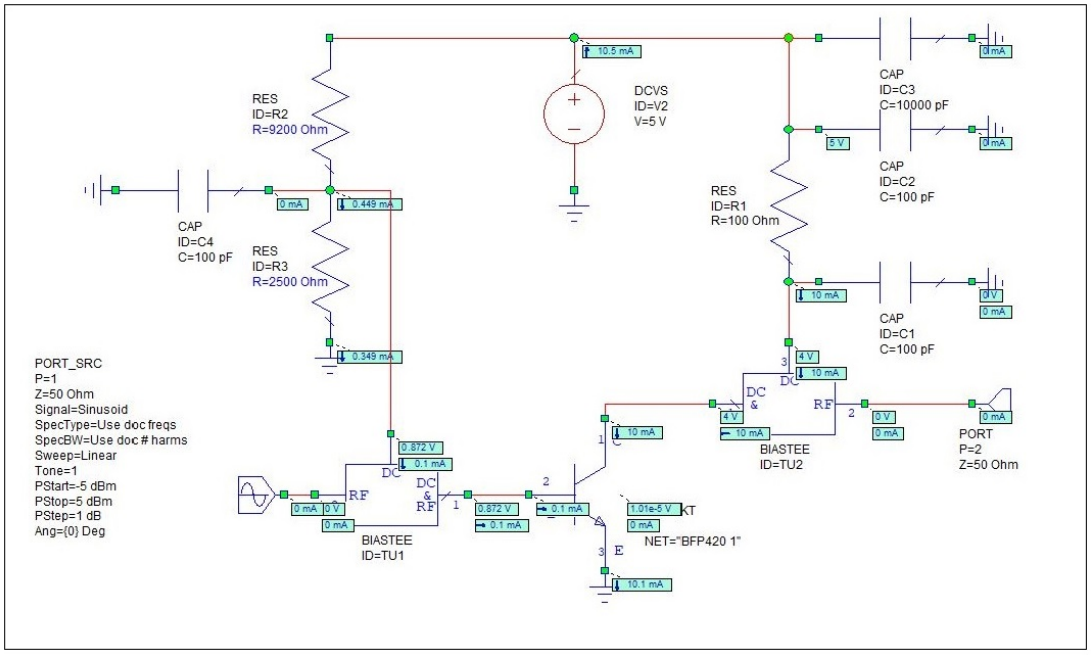


Figure 6.38 : SiGe HBT frequency doubler bias circuit schematic.

the HBT. Dynamic load line versus DC-IV curves has been given in Figure 6.38. Dynamic load line of the operating circuits proves the non-linear operating conditions

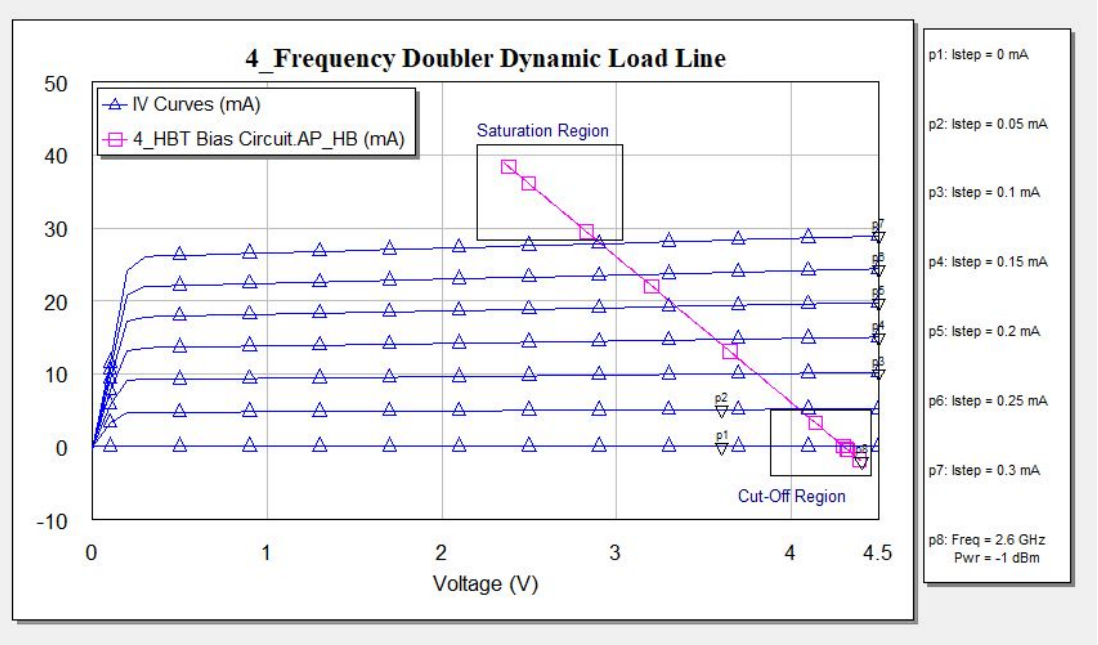


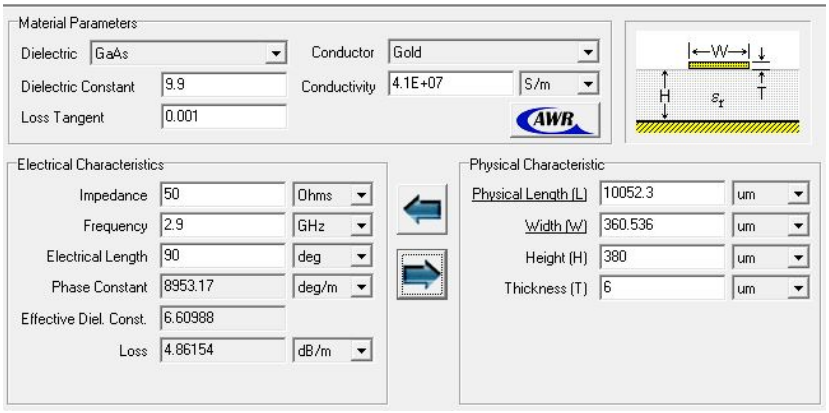
Figure 6.39 : SiGe HBT frequency doubler dynamic load line.

where pink line reachs above linear operating region of the HBT and goes down to cut-off region. Driving the transistor up to saturation region and down to cut-off

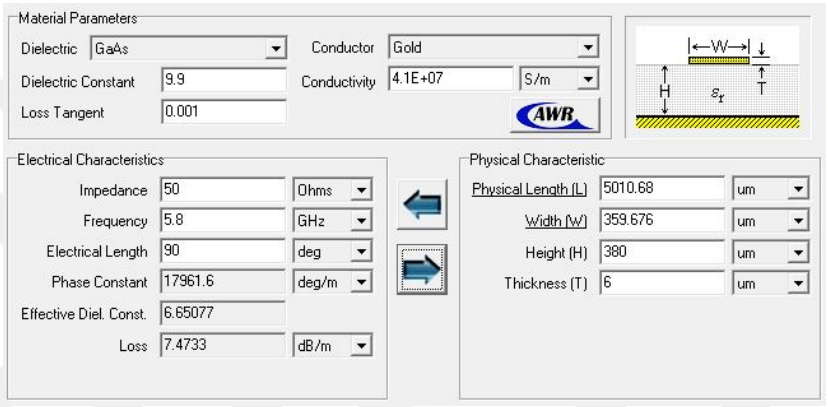
region provides abrupt signal clipping in time domain which results in harmonically rich output spectrum as explained in Subsection 6.5.3.

6.5.5.6 Idler circuits

Ideal frequency doublers receive the input signal with fundamental frequency and produce the output frequency that has twice the fundamental signal frequency while rejecting fundamental and higher order harmonics at the output spectrum. In reality, generating a spectrum with pure second harmonic is not possible due to higher order and fundamental frequency terms residing in the response function of the non-linear circuits. However these unwanted products can be reduced with method known as idler circuits. Idler circuits are microstrip lines that are placed at the input and output ports with the purpose of providing short circuit path to second harmonic signal at the input port and short circuit path to fundamental signal at the output port. In case of open circuit stub utilisation, two cascaded quarter wavelength lines of 2nd harmonic frequency effectively short circuit the leaked output signal at the input port. Identical approach is followed to place two cascaded quarter wavelength lines of fundamental frequency on the HBT output to supress fundamental signal at the output spectrum. Electrical line lengths of 2.9GHz fundamental and 5.8GHz 2nd harmonic signal is calculated with AWR Design Environment TX-Line tool. Calculated results are used to define idler microstrip line lenghts. Additional tuning is applied to compansate open-end effect of open stub. Therefore idler line lengths are increased by 200um more than calculated values. Calcution parameter and results are given in Figure 6.40. Schematic diagram and layout drawing of the frequency doubler with bias and idler circuits is given in Figure 6.41 and Figure 6.42 respectively. Fundamental signal rejection response at output port has been simulated by driving the circuit with bias conditions given in Table 6.10. Frequency versus output power graph demonstrates more than 30dB rejection is achieved at fundamental frequency of 2.9 GHz. Identical analysis has been performed for 2nd harmonic rejection response at the input port. Frequency versus input leakage graph demonstrates more than 80dB rejection is achieved at 2nd harmonic frequency of 5.8 GHz leaked back to input port.



(a) Fundamental quarter wavelength calculation.



(b) 2nd harmonic quarter wavelength calculation.

Figure 6.40 : Quarter wavelength calculation using AWRDE TXline tool.

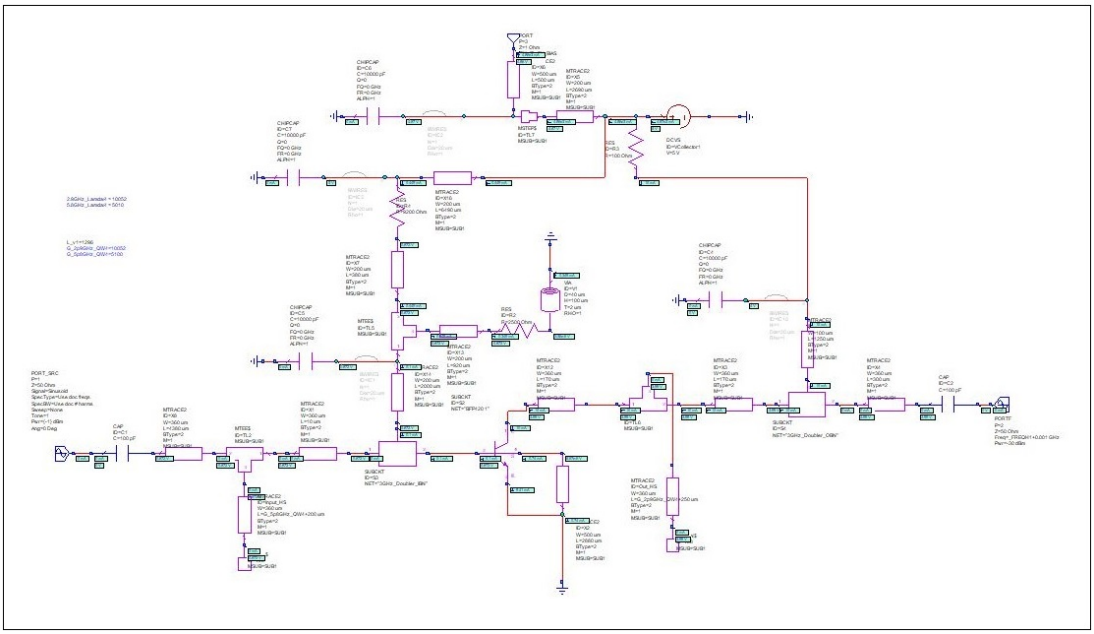


Figure 6.41 : SiGe HBT frequency doubler schematic with bias and idler lines.

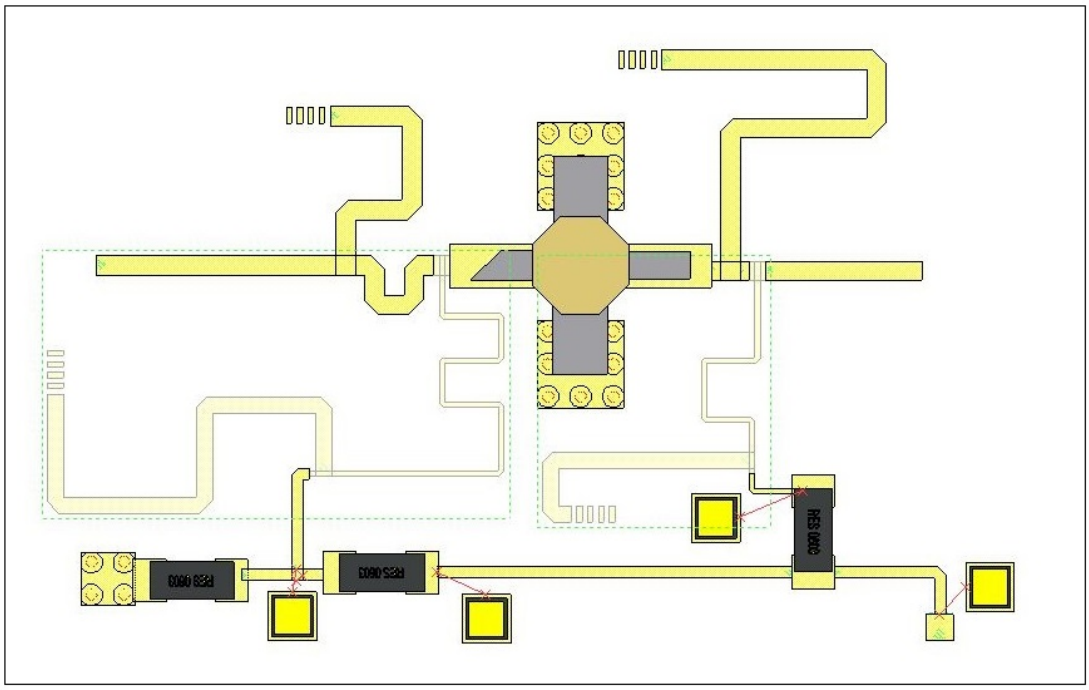


Figure 6.42 : SiGe HBT frequency doubler layout with bias and idler lines.

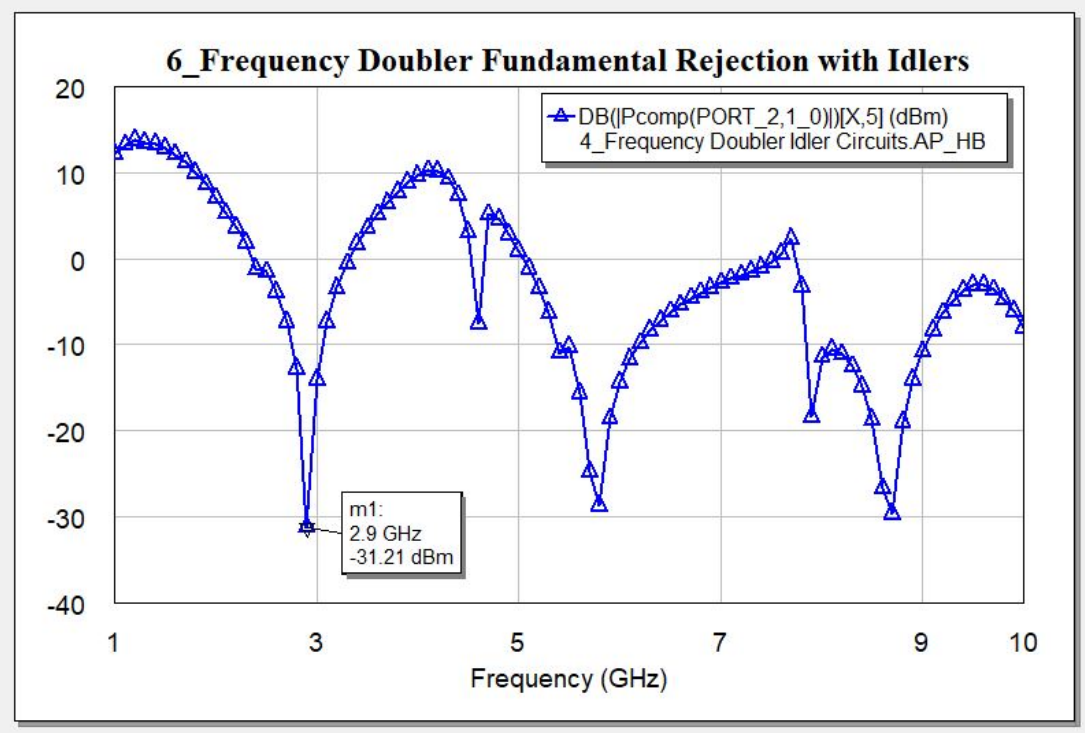


Figure 6.43 : Frequency doubler fundamental rejection graph with idlers.

Reverse isolation of the transistor is the other main contributer of the high rejection value besides idler circuit.

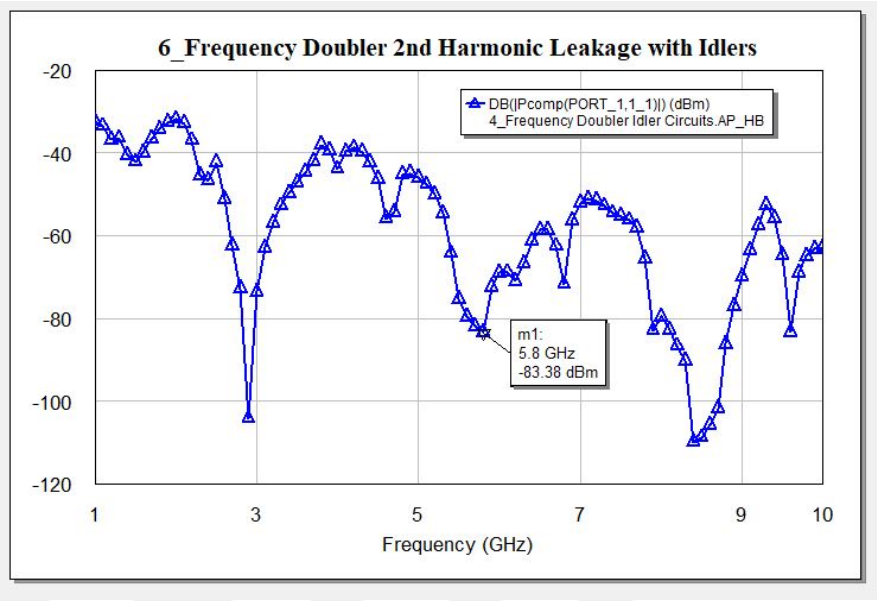
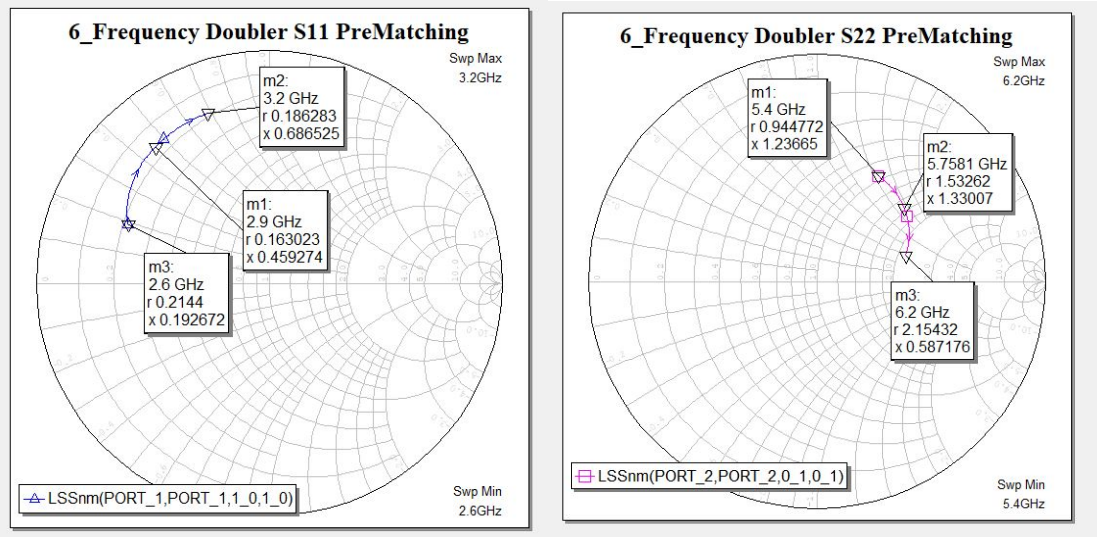


Figure 6.44 : Frequency doubler 2nd harmonic leakage graph with idlers.

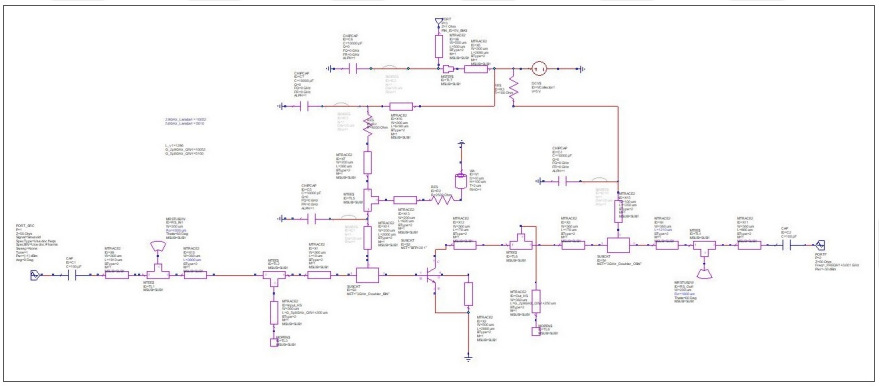
6.5.5.7 Impedance matching

In order to improve the conversion efficiency of the designed frequency doubler, reactive impedance matching circuits have been designed on input and output ports. Impedance matching for the frequency doublers slightly differs from linear circuits because of the fact that frequencies of interest are not equal to each other at input and output ports. Therefore reactive matching circuit for the input port of the HBT is centered to fundamental signal while output port is matched to 2nd harmonic of the input signal. Impedance matching methods described in Section 6.2 are followed for matching circuit design. Input and output nonlinear scatter parameter of the circuit prior to impedance matching have been given in Figure 6.45a and Figure 6.45b respectively. Microstrip open stubs has been placed on the input and output transmission lines to produce required reactances. Radial stubs are preferred to achieve wider bandwidth. Completed frequency doubler circuit schematic and layout has been shown in Figure 6.46. Input and output return loss after impedance matching has been given in Figure 6.47 on rectangular format. Input return loss performance of the frequency doubler circuits performs better than -10dB within 250MHz input

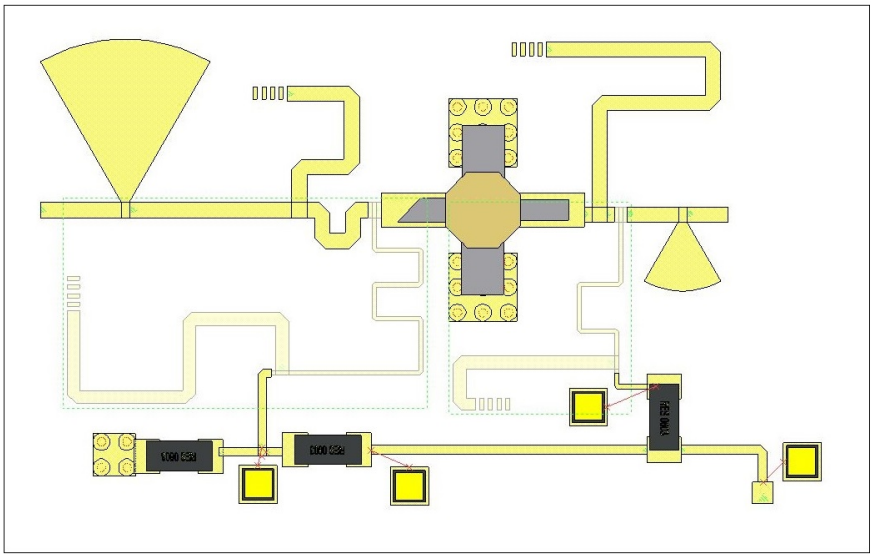


(a) Pre-matching S11 graph. (b) Pre-matching S22 graph.

Figure 6.45 : Frequency doubler pre-matching non-linear scatter parameters.



(a) Frequency doubler schematic.



(b) Frequency doubler layout.

Figure 6.46 : Frequency doubler final schematic and layout.

bandwidth. On the other hand, output return loss is lower than -10dB within more than 1 GHz bandwidth.

6.5.5.8 MIC design layout

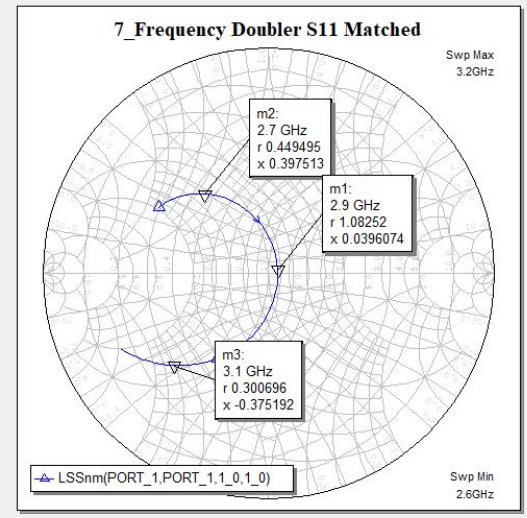
S-Band Frequency multiplier has been designed on alumina substrate with 381um thickness. DC blocking series capacitors are placed on input and output ports to block current leakage to subsequent design blocks. Decoupling capacitors placed parallel to bias lines provide RF ground path to high frequency signals and reduce the voltage ripple on the bias lines. 25um gold wires are used for Interconnections between wirebondable parts and microstrip lines. Additional tuning pads are placed adjacent to input transmission line, output transmission line, fundamental idler open stub and 2nd harmonic idler open stub. Total area of the circuit is confined within $240mm^2$. 2-D and 3-D layout illustration of designed MIC board is shown in Figure 6.48. Total DC power consumption of the design is 50.5mW.

6.5.5.9 S-Band frequency doubler MIC performance results

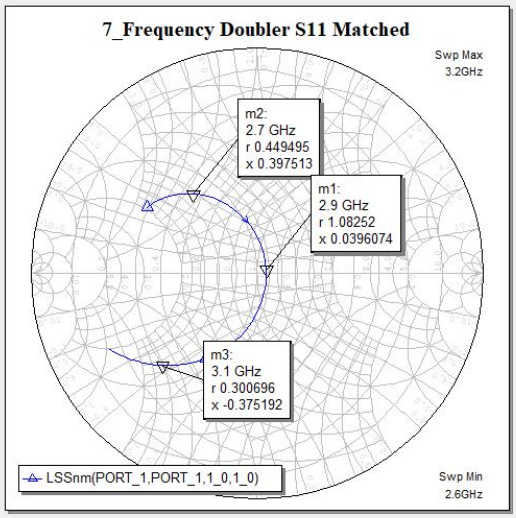
Designed doubler circuit exhibits higher than 0 dB conversion gain within 600 MHz bandwidth centered at 3GHz input frequency. Highest conversion gain of $\approx$ 3.7dB is achieved at target fundamental frequency of 2.9GHz. On the other hand, output spectrum graph indicates the fact that more than 25dB fundamental and 3rd harmonic rejection are obtained due to idler microstrip lines. Conversion gain and output spectrum results has been demonstrated in Figure 6.49 and Figure 6.50 respectively. Electrical specifications of the SiGe HBT based S-Band Doubler MIC design are listed in Table 6.11.

6.6 Harmonic Supression Filter Design

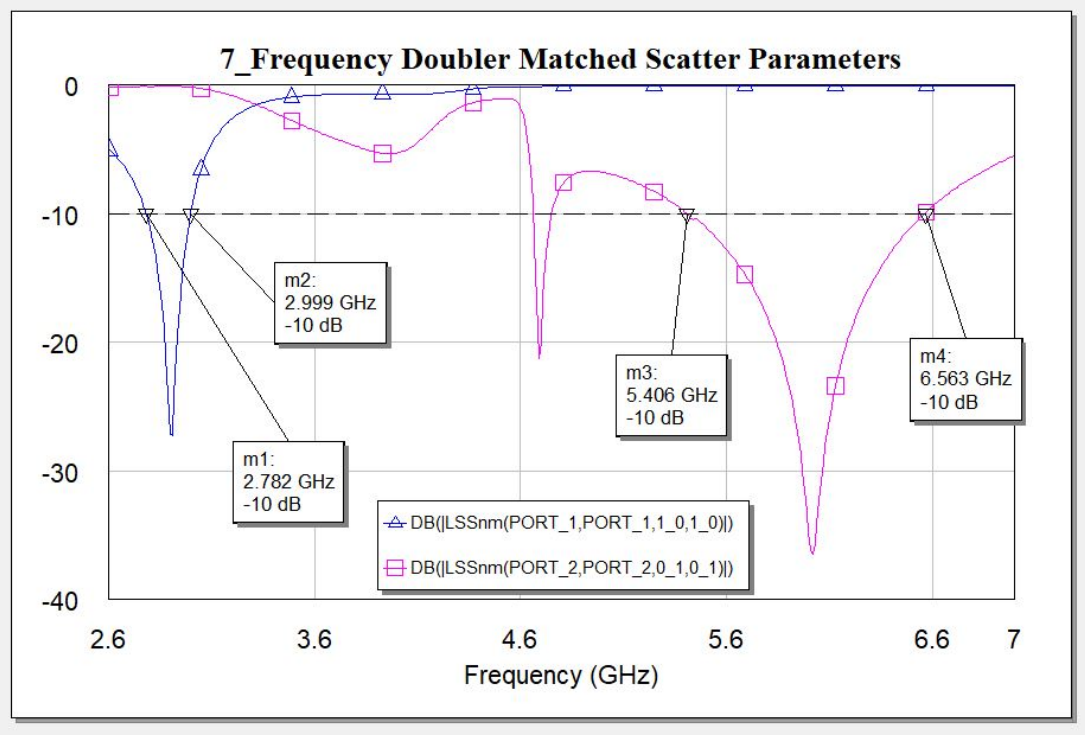
Frequency multiplication operation through S-Band frequency doubler produce residual fundamental signal and higher order harmonics at the output spectrum even though they are highly attenuated. Further unwanted signal rejection is accomplished by Harmonic Suppresion Filter that is placed after frequency multiplication stage. Main purpose of the Harmonic Supression Filter is to further filter out fundamental and



(a) Post-matching input return loss - Smith Chart.

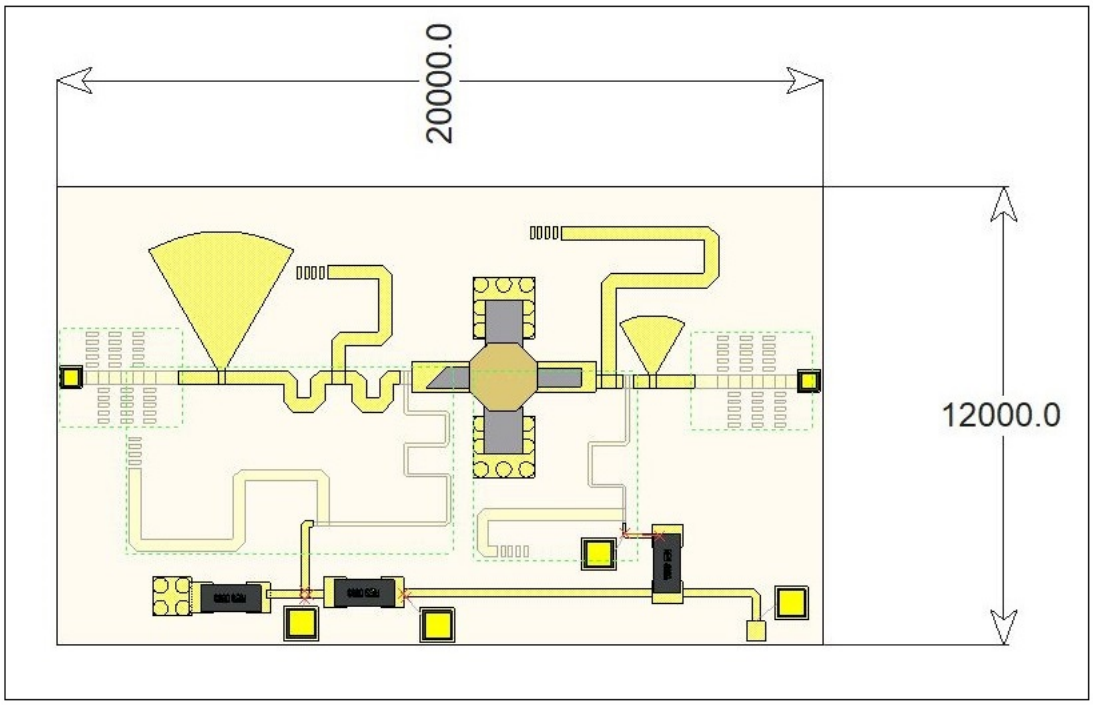


(b) Post-matching output return loss - Smith Chart.

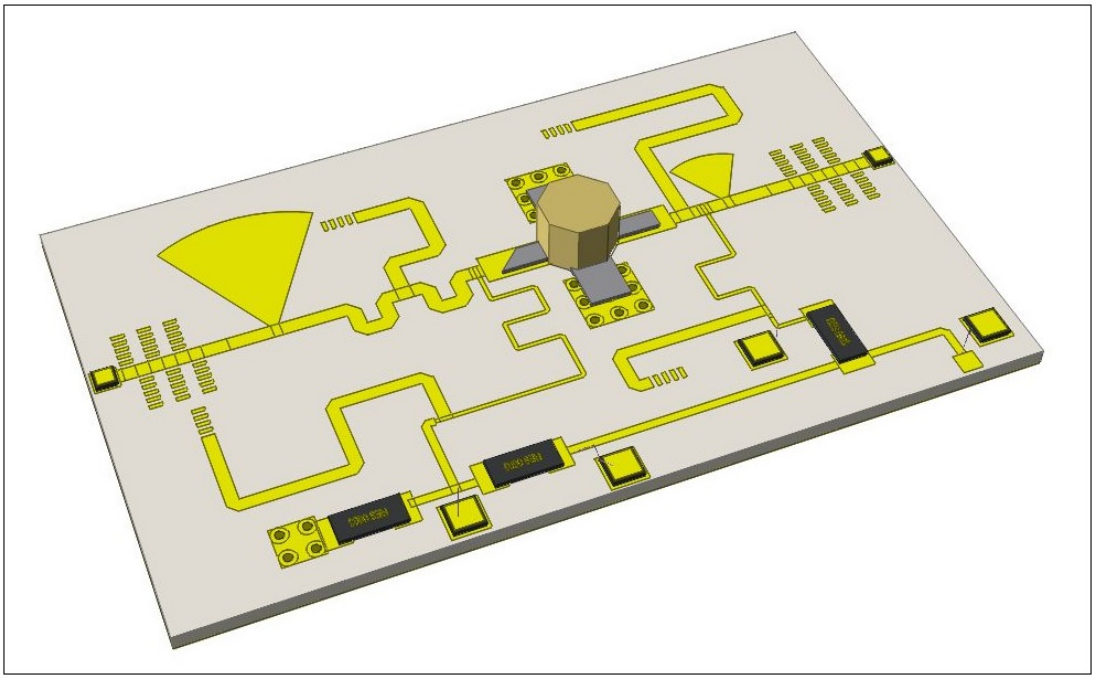


(c) Post-matching return loss performance - Rectangular Form.

Figure 6.47 : Frequency doubler post-matching return loss performance.



(a) 2-D



(b) 3-D

Figure 6.48 : S-Band frequency doubler MIC visual representation.

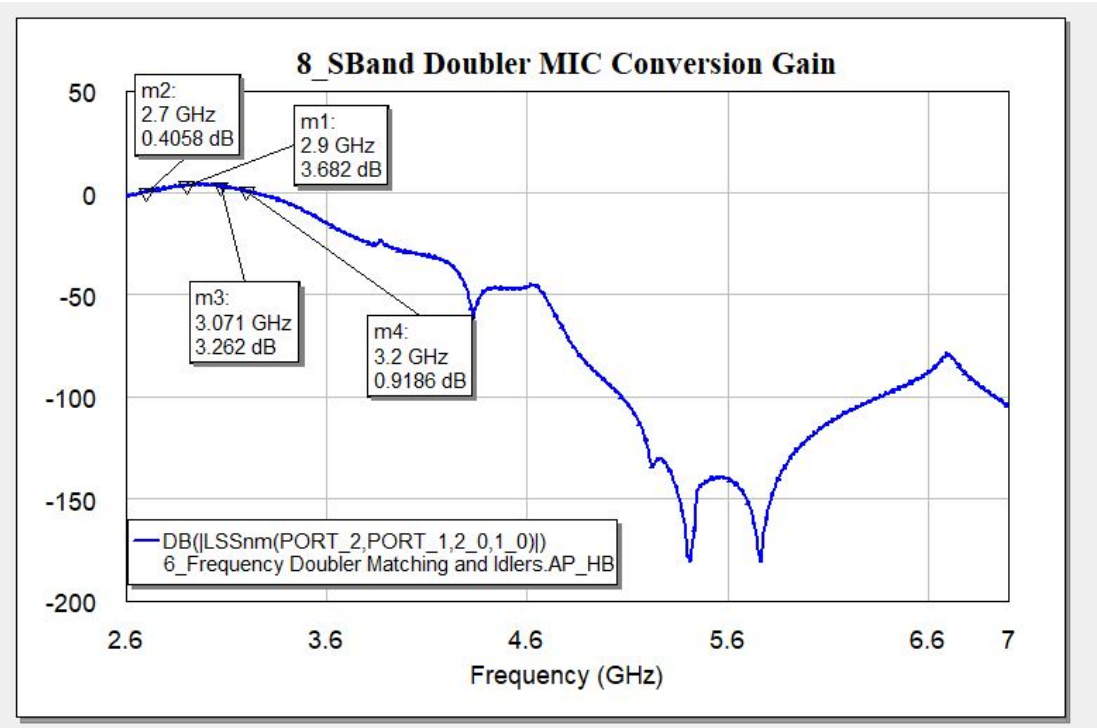


Figure 6.49 : S-Band frequency doubler MIC conversion gain.

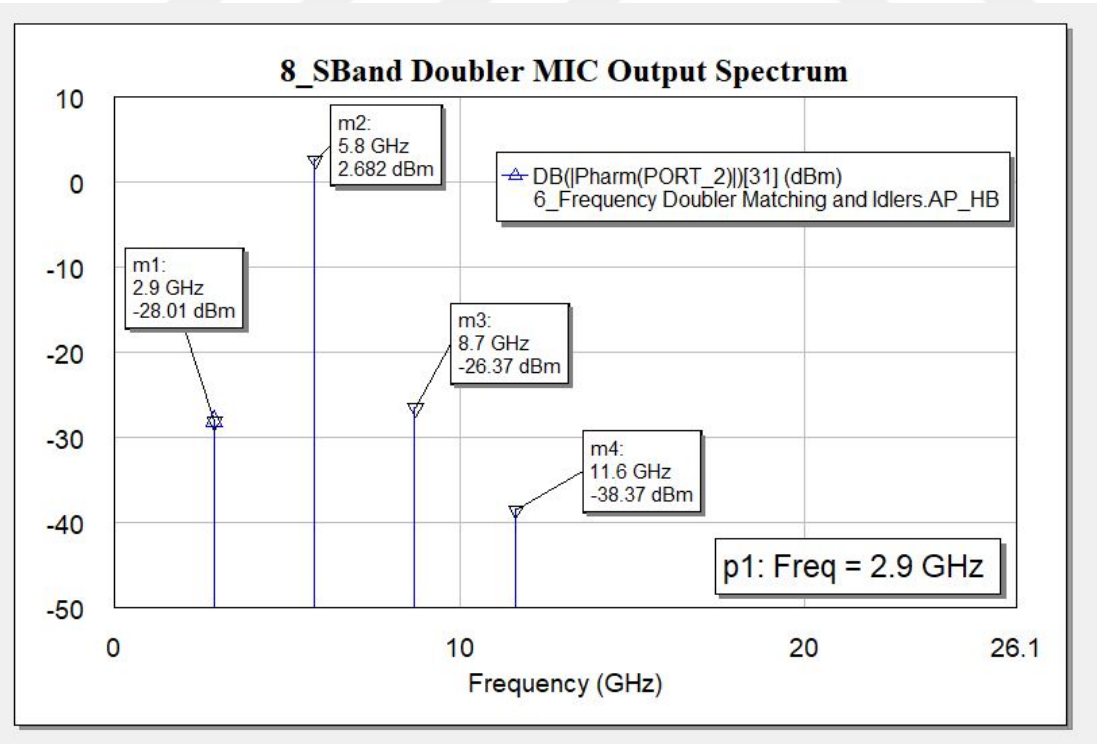


Figure 6.50 : S-Band frequency doubler MIC output spectrum.

Table 6.11 : Electrical specifications of SiGe HBT based S-Band doubler MIC.

Symbol	Parameter	Value	Unit
Pin	Input RF Drive Level	-1	dBm
CG	Conversion Gain	>0	dB
CGF	Conversion Gain Flatness	$\pm$ 1.5	dB
S11	Input Return Loss	<-10	dB
S22	Output Return Loss	<-10	dB
P_{f0}	Fundamental Suppresion	>27	dBc
P_{f3}	Third Order Suppresion	>25	dBc
V_{Supply}	Bias Voltage	5	V
I_{Supply}	Bias Current	10.1	mA

higher order harmonic components while passing through required second harmonic signal with small insertion losses. Thus bandpass filter frequency response is chosen as the most suitable filter behaviour.

6.6.1 Mathematical model

As elaborated in detail in Section 6.3, theoratical parameter derivation of a bandpass filter is initialized with low-pass filter prototype design. Chebyschev function filter is taken into consideration due to superior rejection and low passband ripple performance. Minimum number of filter order required to achieve target frejection performances listed in Table 5.6 is derived by using Equation 6.28. Subsequently, low-pass prototype coefficients are extracted from Chebyshev Lowpass Filter Prototype Coefficients given in Table 6.6.

6.6.1.1 Chebyshev type lowpass filter prototype

Minimum number of filter order to satisfy target harmonic supression values which is stated in Table 5.6 can be calculated by

$$n \geq \frac{cosh^{-1}\sqrt{\frac{10^{(SS/10)}-1}{10^{(0.1PB_{Ripple})}-1}}}{cosh^{-1}\Omega_s} \tag{6.46}$$

where SS represents highest signal suppression value among fundamental and higher order harmonics in dB, PB_{Ripple} represents passband ripple in dB and Ω_s is the unwanted fundamental or higher harmonic frequency normalized to center frequency of harmonic supression filter. As it can be seen from Equation 6.46, order of the filter

needed to achieve required supression value increases as passband ripple parameter decreases. Since received input signals is the stable local oscillator frequency that will have single frequency component with 1 Hz bandwidth, passband ripple parameter is not taken into consideration and taken as 0.1dB. On the other hand, filter implementation with higher supression values would increase the number of filter order. Due to the fact that higher number of filter order increases the physical size and complexity of the realizable fillter, a trade-off between filter size/complexity and unwanted signal supression is investigated to decide filter order for implementation. Normalized value of Ω_s is taken as the same value for the fundamental and third harmonic frequencies since spacing between them to 2nd harmonic signal is equal to each other.

$$\Omega_s = \frac{|(f_{Center} - f_{Unwanted})| + (\frac{BW}{2})}{BW}) = \frac{|5.8GHz - 2.9GHz| + (0.25GHz)}{0.5GHz} = 6.3. \tag{6.47}$$

$SS = 80dB$ unwanted signal suppression requirement and $\Omega_s = 6.3$ normalized harmonic frequency are inserted into Equation 6.46. Minimum number of stages versus passband ripple PB_{Ripple} values are calculated using Equation 6.48 and given in Table 6.3.

$$n \geq \frac{cosh^{-1}\sqrt{\frac{10^8-1}{10^{0.01}} - 1}}{cosh^{-1}(6.3)} = 4.66 \tag{6.48}$$

In order to have symmetrical filter structure, odd number of filter stage is prefered in implementation phase. Therefore fifth order filter is chosen as an optimum solution which can provide 0.1 dB passband ripple while maintaining 80dB harmonic and fundamental signal rejection. g_n coefficients of Chebyshev lowpass prototype filters are obtained from precalculated coefficient tables. Coefficient values of prototype filter that represent fifth order and 0.1dB passband ripple are taken from parameter Table 6.6.

6.6.1.2 Chebyshev type lowpass filter prototype to bandpass filter transformation

Coefficient tables are used to determine inductive and capacitive elements which constitute microwave filters. Constructed lowpass prototypes can be converted to lumped element bandpass filters using frequency and element transformation

equations. Frequency transformation from lowpass prototype to bandpass filter implementation is performed by calculation steps through Equation 6.31 to Equation 6.31 which are explained in detail in Subsection 6.3.1.2. Calculated lumped element representation of harmonic supression filter that has 5.8 GHz center frequency and 500 MHz bandwidth is shown in Figure 6.51. Simulation results on AWR CAD software

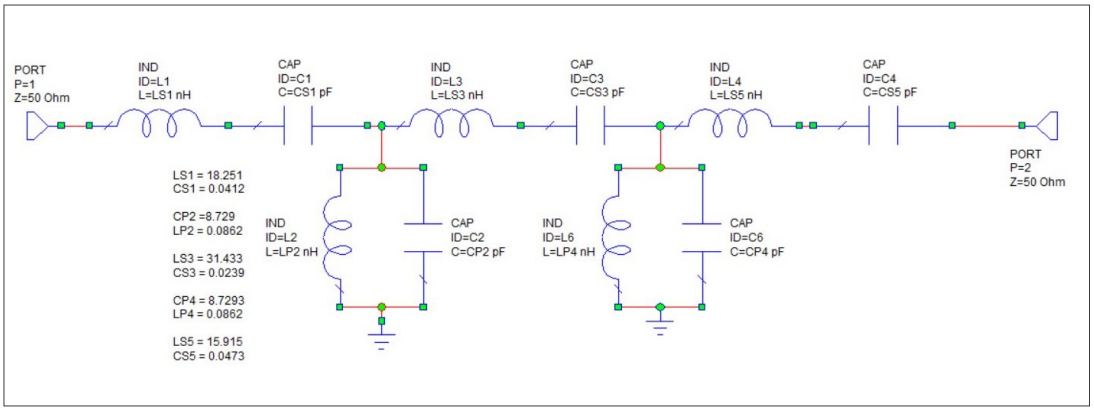


Figure 6.51 : Lumped element representation of fifth order Chebyshev type harmonic supression filter.

given in Figure 6.51 shows the fact that filter performance are perfectly aligned with design specifications. However calculated inductor and capacitor values can not be realized with real lumped elements due to limited inductance and capacitance ranges provided by manufacturers. Therefore distributed element realization is chosen for implementation phase. Although there are several well-known theoratical methods such as Richard's Transformations and Kuroda Identities to convert filters with lumped element components to distrubuted element filters, calculation complexity exponentially increases with inclusion of parasitic effects, unintended couplings between distributed elements and fringing fields at the end of open microstrip lines. Computer aided microwave design softwares with 2-D electromagnetic simulation (EM) capabilities provides convenient approach for high-frequency distributed element type filter designs. 2-D EM analyzers utilizes Method of Moment (MoM) solver technique to achieve highly accurate simulation results. Therefore distrubuted element filter design has been performed on AXIEM 2-D EM simulation tool provided by AWR Design environment.

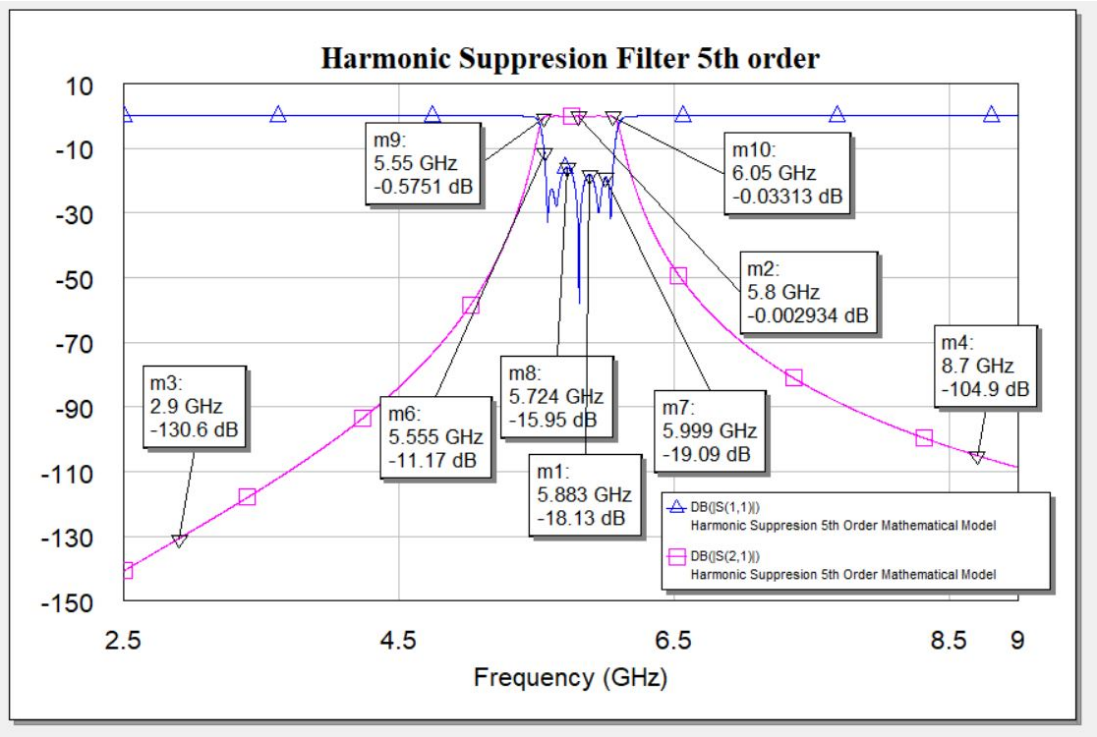


Figure 6.52 : Simulation results of lumped element fifth order harmonic suppression filter.

6.6.2 Distributed element harmonic suppression filter design

Instead of using lumped inductor and capacitors, microstrip lines with lengths lower than guided electrical length of operating frequency can be utilized to construct reactive elements associated with filter design. One of the most commonly used distributed element bandpass filter, Interdigital Type is chosen for Harmonic Suppression Filter Design due to its smaller size and superiour higher harmonic rejection. Since operating frequency of the filter is on C-Band, manufacturing tolerances on shorting vias are considered negligeble. Filter design has been performed on AWR Design Environment microwave analysis software. Dielectric substrate is defined as alumina with dielectric constant of 9.9 and 381um thickness. Shorting via diameter is chosen as 200um with 400um capture pad due to thin film manufacturing constraints. Simulations and optimisation steps are run through AXIEM 2D Planar

simulator package. Initial design parameters for the filter taken as

$$W_1 = W_2 = W_3 = W_4 = W_5 = 360um$$
$$S_{1,2} = S_{4,5} = 650um \tag{6.49}$$
$$S_{2,3} = S_{3,4} = 800um \qquad \lambda_g = 5000um$$

where W_n dimensions represent quarterwave coupled line widths that are equal to characteristic impedance of 50Ω and $S_{n,n+1}$ dimensions are the coupling spacing between quarter wavelength coupled line resonators. Initial design and its analytical simulation results are shown in Figure 6.53 and Figure 6.54 respectively.

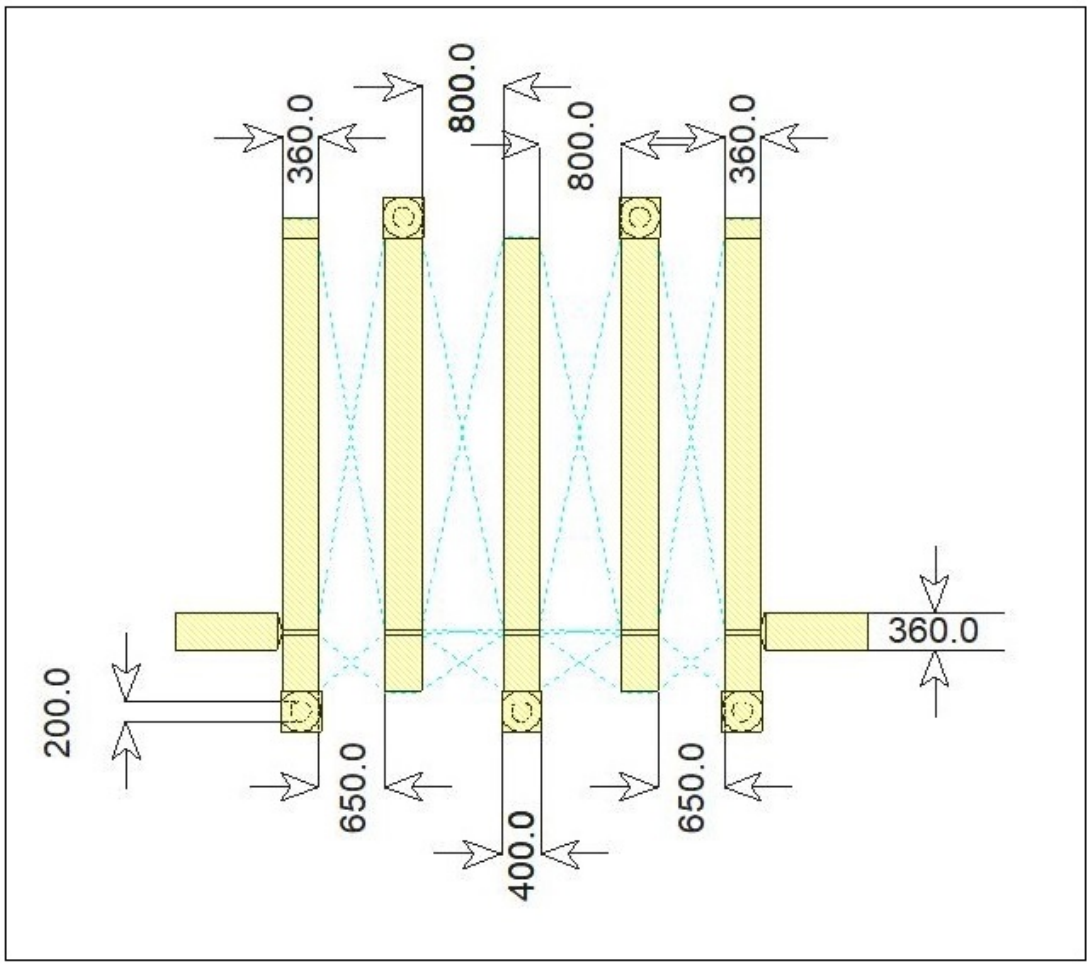


Figure 6.53 : Interdigital harmonic suppression filter initial dimensions.

In order to achieve more accurate simulation results, AWRDE Axiem planar EM simulation has been run on designed interdigital filter. Mesh view of the designed filter is illustriated at Figure 6.55. EM simulation results shows slight frequency

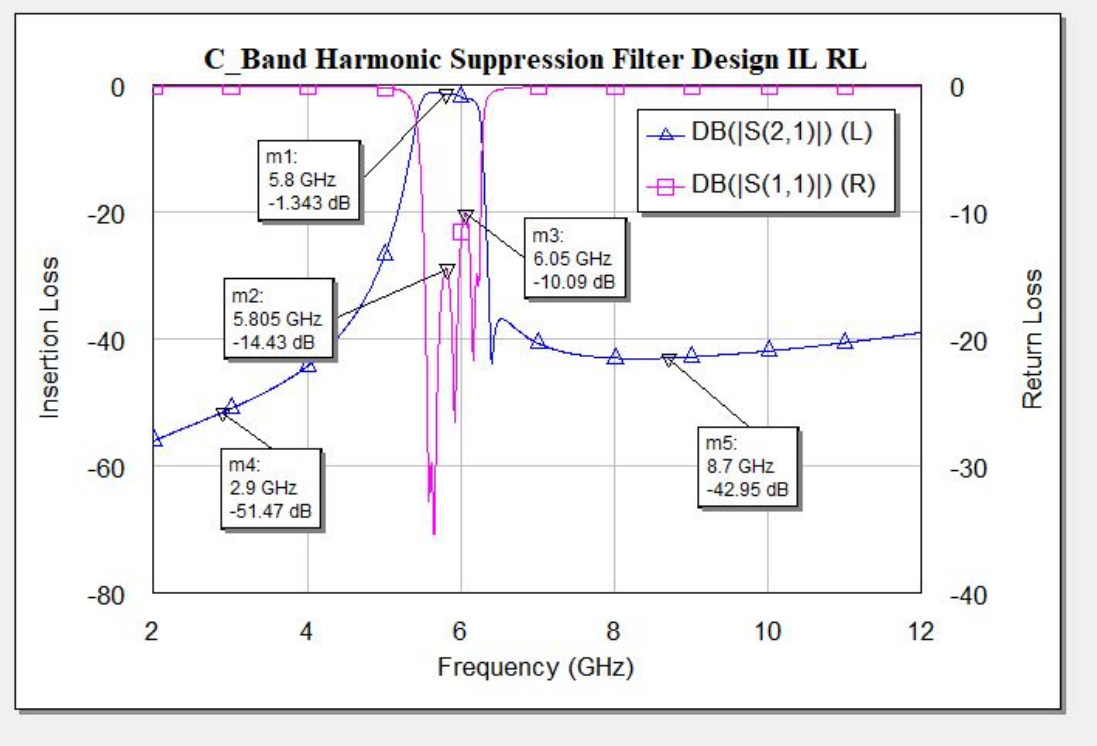


Figure 6.54 : Interdigital harmonic suppression filter analytical simulation results.

shift to higher frequency band and degraded return loss performance. However since filter is designed for 500MHz bandwidth, 5.8GHz local oscillator frequency still fall into passband.On the other hand, return loss better than -10dB is considered acceptable for microstrip filter implementations. Both analytical and electromagnetic simulation results indicates the fact that higher order harmonic rejection performance at high frequencies can not be lowered down to -80dB levels. Unwanted coupling between resonators results lower suppresion values than expected by theory. Achieved filter performance versus target electrical specifications are listed in Table 6.12.

2-D and 3-D layout illustration of designed Interdigital Harmonic Suppression

Table 6.12 : Achieved vs target electrical specification of microstrip harmonic suppression filter.

Symbol	Parameter	Target Spec.	Simulation Result	Unit
f_c	Center Frequency	5800	5900	MHz
BW_{1dB}	1dB Bandwidth	>500	>600	MHz
IL	Insertion Loss	<2dB	<1	dB
IRL	Input Return Loss	<-20	<-10	dB
-	Fundamental Suppression	<80	> 62	dB
-	3rd Harmonic Suppression	>80	>56	dB

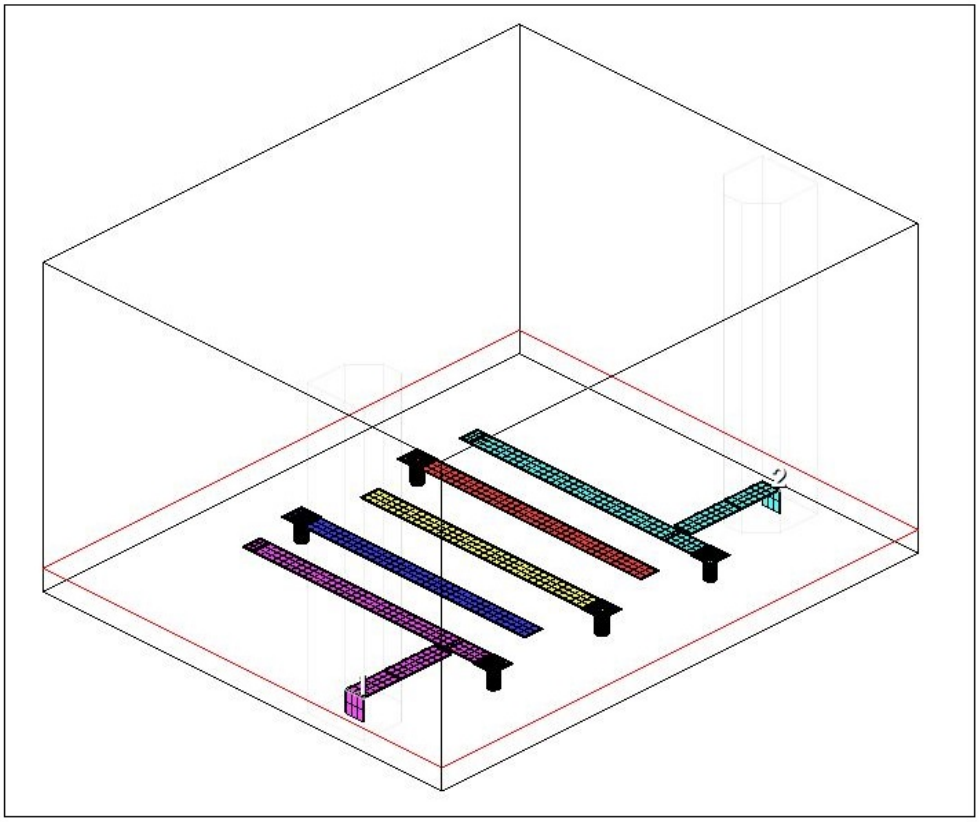


Figure 6.55 : Interdigital harmonic suppression filter Axiem-EM simulator 3-D mesh view.

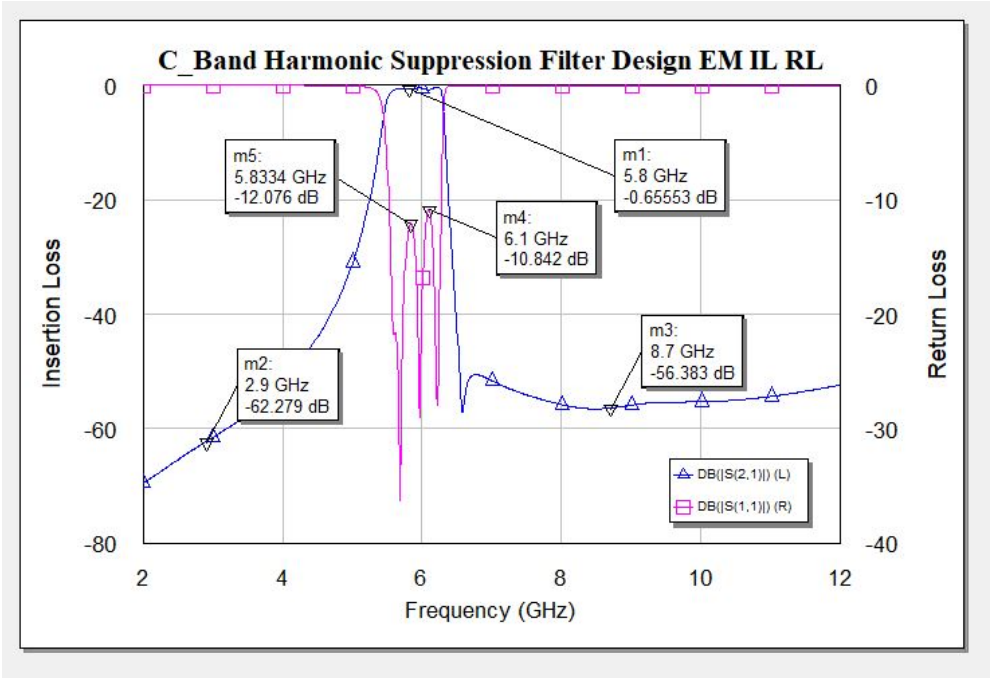


Figure 6.56 : Interdigital harmonic suppression filter EM simulation results.

Filter MIC board is shown in Figure 6.57 and Figure 6.58 respectively.Interdigital Harmonic Suppression Filter MIC design consist of alumina substrate, microstrip 50 ohm interconnection and coupled microstrip transmission lines. End points of RF transmission line are enlarged to add capacitive reactance to compansate inductive effect of bonding wires. Additional tuning pads have been placed on each side of input and output transmission lines for future impedance tuning. Total area of the filter board is confined within $112mm^2$.

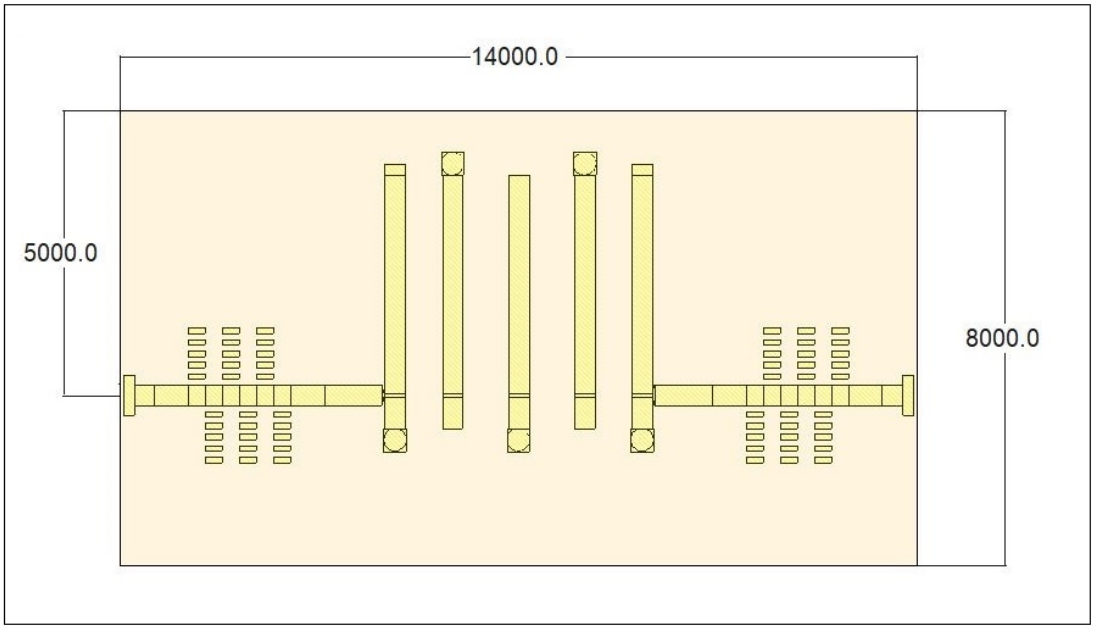


Figure 6.57 : Interdigital harmonic suppression filter MIC 2-D visual.

6.7 Hybrid Integration

X-Band SAR Receiver Front-End physical placement is divided into two section, namely; Low Noise Amplification and LO Generation sections. Low Noise Amplification section consists of X-Band LNA, Image Reject Filter and Downconversion Mixer MICs. On the other hand, LO Generation section combines S-Band Frequency Doubler, C-Band Harmonic Suppression Filter and Buffer Amplifier MICs. Considering high linearity of chosen LNA die, LNA MIC has been used instead of designing separate buffer amplifier. Physical separation of the section helps to reduce unintended coupling between high power LO signals to low power RF input and DC bias lines. Several consideration has been taken into account for baseplate

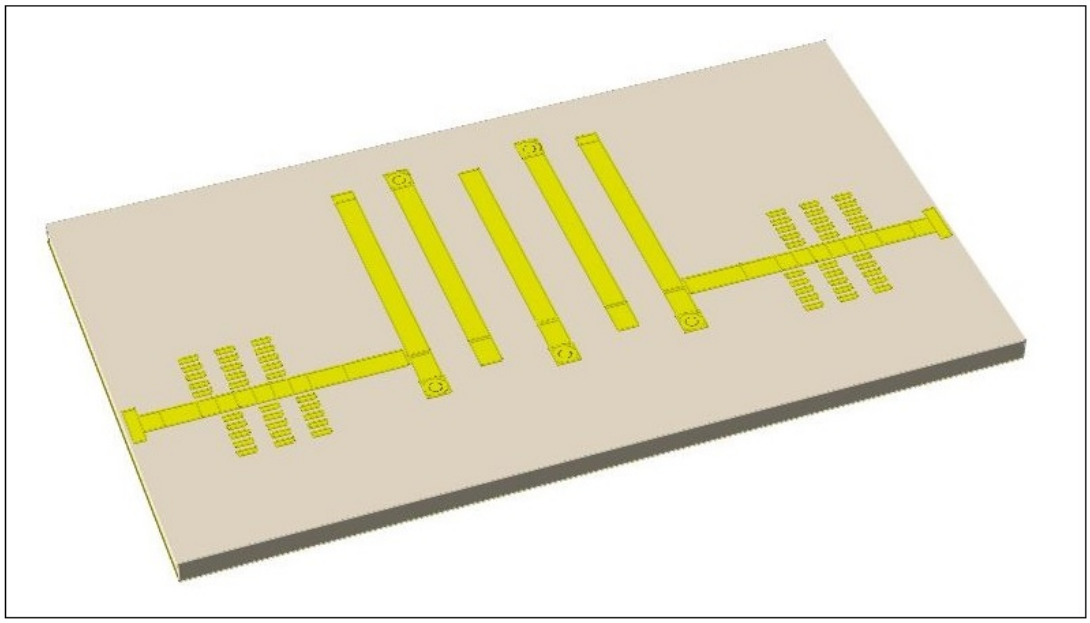


Figure 6.58 : Interdigital harmonic suppression filter MIC 3-D visual.

material selection. Most commonly used low weight-high strength metal alloys such as aluminum or brass alloys exhibit high coefficient of thermal expansion (CTE). Material interfaces with different CTE characteristics cause thermal stress on connection surface when materials encounter temperature variations. Generated thermal stress dimishes the long-term reliability of the hybrid assembly [44]. Moreover, materials with higher thermal conductivity present lower temperatures on electronic parts due to better heat distribution and conduction. Thermal conductiivity and thermal expansion characteristics of several metal alloys which are frequenctly used in electronics industry are compared to %99.9 alumina material in Table 6.13 [44]. Although

Table 6.13 : Thermal conductivity and CTE characteristics of most commonly used metals and metal alloys vs Alumina (Al2O3).

Material	**Thermal Conductivity (W/mK)**	**Coefficient of Thermal Expansion (ppm/K)**
Alumina	33	8
Aluminum	237	24
Brass	109	19
Copper	385	17
Steel	50	13
Platinum	71.6	9
Kovar	17	5.5

copper and aluminum exhibits highest thermal conductivity, their CTE characteristics makes them unsuitable for high reliability application that will encounter continous variation on environmental temperature. Therefore Kovar is chosen as the baseplate material due to its 5.5 ppm/K CTE value which has the closest thermal expansion match to alumina substrates. Designed alumina substrates are integrated on top of kovar baseplate and placed in enclosure. RF and DC interconnections between alumina boards are conducted with 25um gold bonding wires. In order to distribute RF and DC signals throughout the hybrid assembly, several through lines are included in the design. 2-D and 3-D views of X-Band SAR Receiver Hybrid Front-End Assembly is given in Figure 6.59 and Figure 6.60 respectively. Total surface area of the hybrid design is measured as 61x43mm.

Electrical specifications of designed hybrid front-end is listed in Table 6.14

Table 6.14 : X-Band SAR receiver hybrid front-end assembly electrical specifications.

Parameter	Value	Unit
Input Frequency	7500-8500	MHz
Input Bandwidth	250	MHz
Image Rejection	>-50	dB
LO Input Frequency	2900	MHz
LO Input Power	-1	dBm
Conversion Gain	>35	dB
Power Consumption	<1100	mW

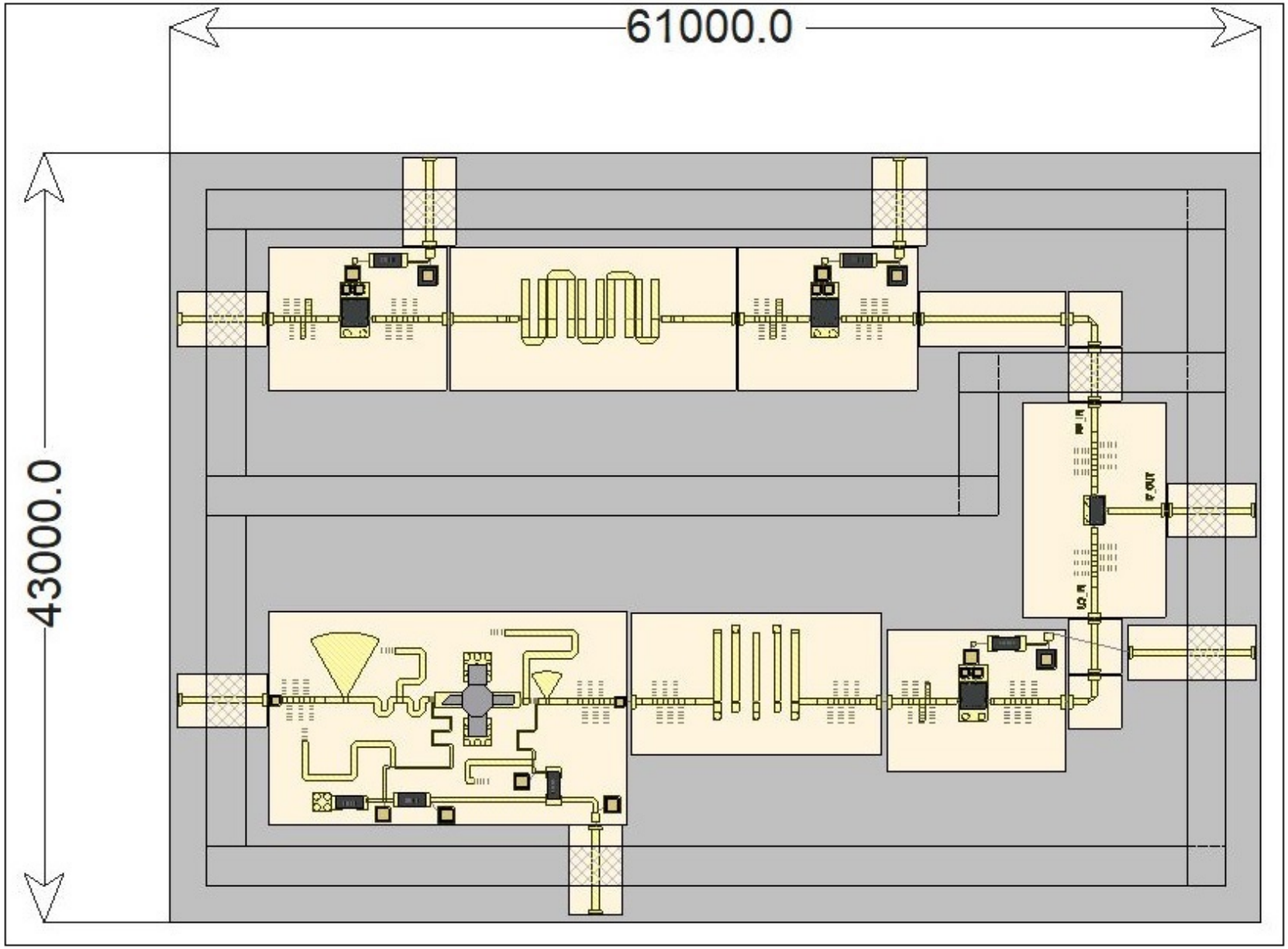


Figure 6.59 : X-Band SAR receiver hybrid front-end assembly 2-D visual.

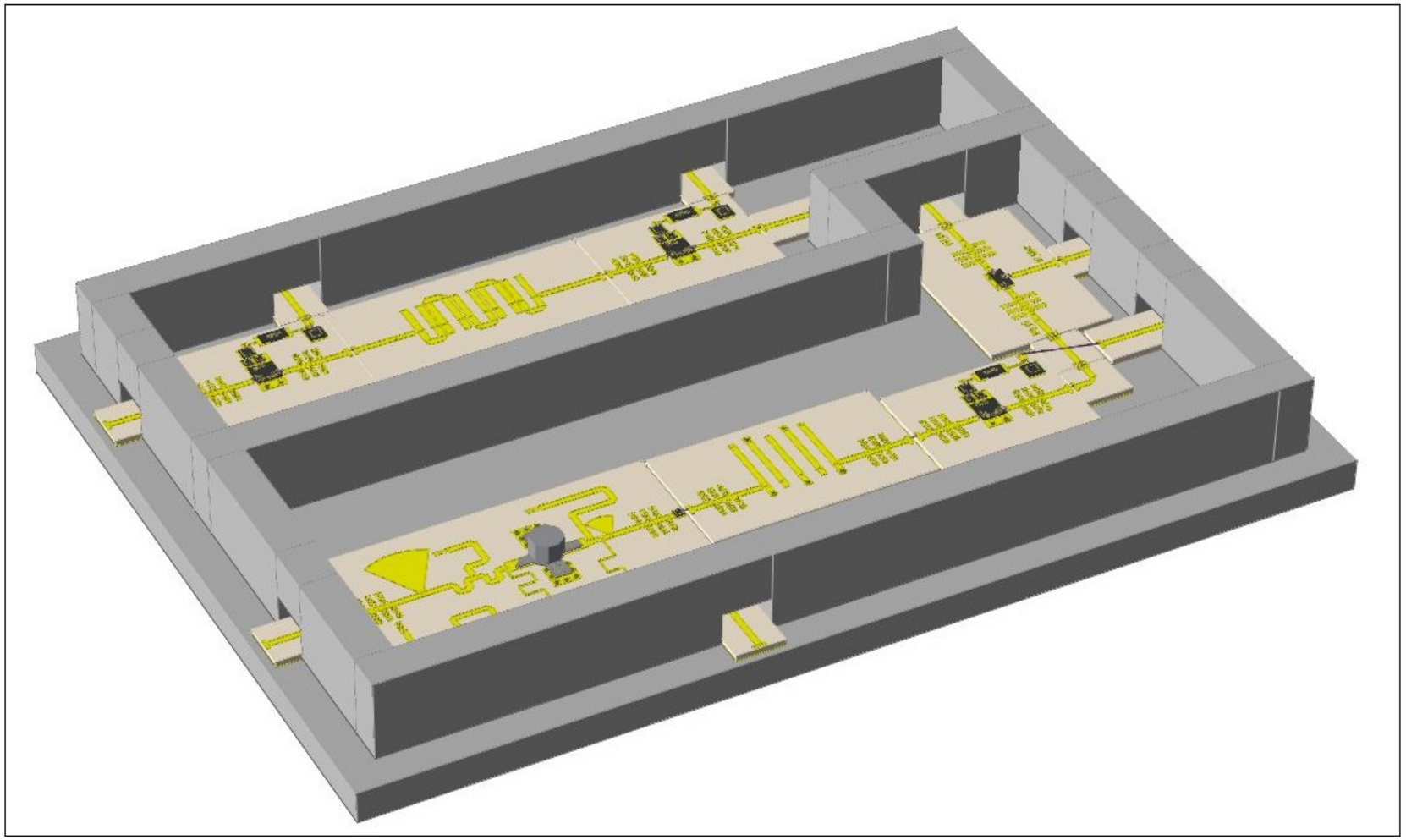


Figure 6.60 : X-Band SAR receiver hybrid front-end assembly 3-D visual.

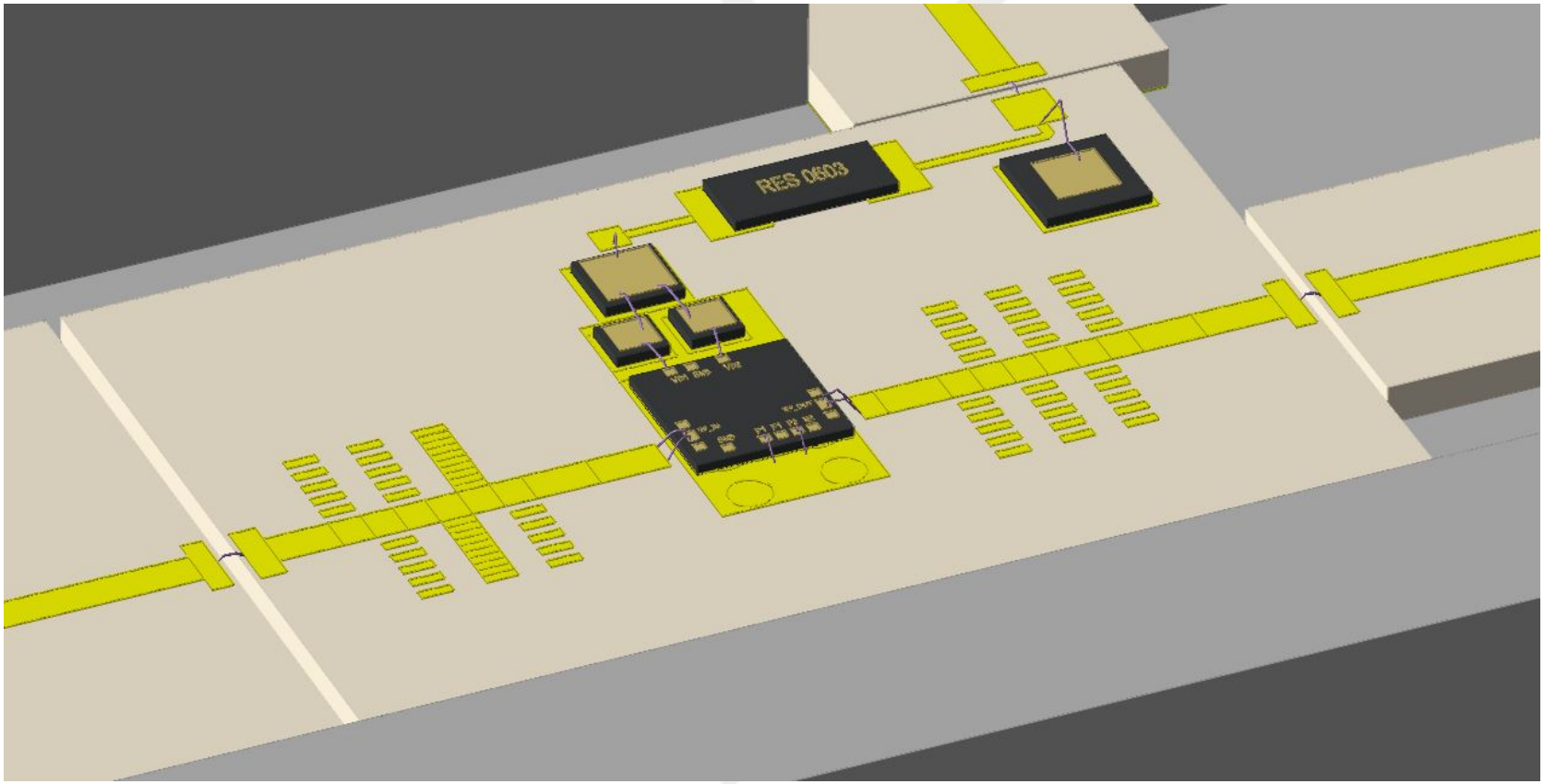


Figure 6.61 : X-Band SAR receiver LNA MIC wire-bond interconnections - Zoomed view.

7. CONCLUSION

Design procedure of spaceborne instruments/modules has distinct differences in comparison with terrestrial applications due to challenging radiation tolerance and reliability requirements. In the scope of this thesis; derived SAR receiver electrical performance parameters such as signal bandwidth, noise figure, interference immunity and dynamic range are used to design a unique receiver architecture which is build upon space qualified state-of-art high reliability parts, materials and technologies. Every item involved in designed subsections has been investigated for total ionizing dose tolerance, single event effect vulnerability and operational life. On the other hand, physical structure of the Receiver Front-End Module is designed to withstand long-term temperature cycling by utilizing materials with close thermal expansion coeffecients. Thin-film technology on alumina substrates are chosen to design MIC boards that enables tight manufacturing tolerances to achieve minimum performance variation between produced parts.

In conclusion; complete Spaceborne SAR Receiver RF Module design methodology is presented while following top-down design approach that starts from system requirements, followed by instrument level design and ends with detailed microwave circuit design.

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