A Wide-Current Range Switched Capacitor DC-DC Converter Utilizing Frequency, Interleaving and Switch-Size Scaling Techniques

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in

Electronics and Computer Engineering

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Electronics and Computer Engineering.

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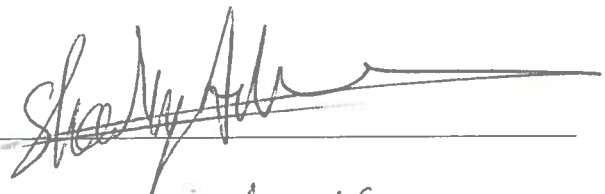
Signed: 

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A Wide-Current Range Switched Capacitor DC-DC Converter Utilizing Frequency, Interleaving and Switch-Size Scaling Techniques

Shady A.Mohammed

Abstract

DC-DC converters are one of the main components of any system. Since analog and digital sub-modules in SoC require different supply voltages, large number of DC-DC converter are used to provide supply voltages for each module from the global input voltage source.

DC-DC converters are divided into two main types; linear and switching regulators. As the drop between the global input source and required voltage increases, linear regulators suffer from high losses and consequently achieve low efficiency compared to switching regulators. Since integration is one of the main objectives, switched capacitor DC-DC converters are more preferable compared inductor based regulators. SC DC-DC regulators eliminate the bulky and costly inductor and can be integrated fully on-chip to be used in sensor networks, energy harvesters and bio-sensors.

In this dissertation, a switched capacitor DC-DC converter, which can directly convert input voltage of 3.3V to five different output voltages, is presented. Different design techniques are used in the design to improve efficiency over a large output current range, reduce output ripple, increase response time and reduce the overall cost.

To improve efficiency, the converter uses a combination of frequency, interleaving and switch width scaling techniques in a feedback loop that respond to the output load and current conditions. The loop consists of a four-phase clock generator, a clock divider, high speed dynamic comparators and a decision making unit. In order to reduce the output ripple, the converter uses four interleavers and frequency scaling. A decision making circuit is included to switch the converter into high response speed mode. Off-chip components were eliminated to minimize the cost of the design.

Frekansı, Serpiştirmeyi ve Anahtar Boyutunu Ayarlama Tekniklerini Kullanan Geniş Akım Aralığına Sahip Anahtarlamalı Kapasitör DA-DA Çeviricisi

Shady A.Mohammed

Öz

DA/DA çeviriciler bir sistemin ana bileşenlerinden biridir. Çip üzerindeki sistemlerdeki analog ve dijital alt modüller farklı besleme gerilimleri gerektirdiğinden, bir çok DA/DA çeviricileri ana giriş gerilim kaynağından her bir modüle besleme gerilimi sağlamak için kullanıldı. DA/DA çeviricileri iki ana çeşide ayrılır; doğrusal ve anahtarlama regülatörü. Ana giriş gerilim kaynağı ve gerekli gerilim arasındaki fark arttıkça, doğrusal regülatörler yüksek kayıptan zarar görür ve anahtarlama regülatörleriyle kıyaslandığında sonuç olarak düşük verim elde edilir. Entegrasyon ana hedeflerden biri olduğu için; anahtar kapasitör DA/DA çeviricileri, regülatör temelli indüktör ile kıyaslandığında tercih edilir. Anahtar kapasitör DA/DA regülatörleri hacimli ve masraflı indüktörü tasfiye eder ve sensör ağlarında, enerji üreticilerde ve biyosensörlerde kullanılmak kullanılmak üzere çip üzerine tamamen entegre edilebilir. Bu tezde, 3.3V giriş gerilimini direkt olarak beş farklı çıkış gerilimine çevirebilen anahtar kapasitör DA/DA regülatörleri tanıtıldı. Çıkış akımının aralık değerini arttırmak, çıkış dalgalanmalarını azaltmak, tepki süresini arttırmak ve toplam maliyeti azaltmak için tasarım kısmında değişik tasarım teknikleri kullanıldı. Verimi arttırmak için, dönüştürücü frekansın, serpiştirmenin ve çıkış yükü ce akım durumlarına yanıt veren geribesleme döngüsündeki anahtar boyutu ölçekleme tekniklerinin kombinasyonunu kullanır. Devrede dört fazlı saat üreteci, saat pergeli, yüksek hızlı dinamik komparatör ve karar verme birimi vardır. Çıkış dalgalanmalarını azaltmak için, komparatör 4 serpiştiriciyi ve frekans ölçeklendirmeyi kullanır. Dönüştürücüyü yüksek tepki hızı moduna çevirmek için bir karar verme devresi dahil edilmiştir. Çip üzerinde olmayan bileşenler tasarımın maliyetini azaltmak için çıkartılmıştır.

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This thesis could not be completed without the guidance, support and encouragement of my professor Hakan Doğan. I would like to thank him for giving me an opportunity of working under supervision and develop this design.

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Thank you from the bottom of my heart.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Power management for modern Soc

Since portable electronic devices are getting smaller and smaller, electronics industry have led to the development of more compact and higher performance electronic systems. These devices are powered through portable batteries. These portable devices consist of a variety of different circuits and blocks [1]. Each block requires a different voltage and current supply as shown in Figure 1.1. Local power supply for these blocks can be generated and distributed by DC-DC converters. The main role of these converters are to provide constant and clean output voltages to the electronic circuit. DC-DC converters are divided into two main categories; linear regulators and switching converters. Moreover, switched converters are divided to inductor based converters and switched capacitor converters [2].

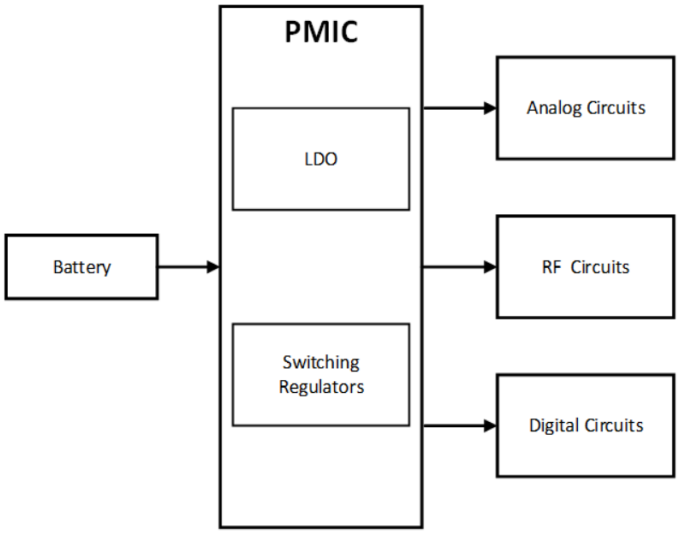


FIGURE 1.1: Typical circuit blocks in Soc and they are powered.

Inductor-based DC-DC converters are used to supply high power consumption blocks such as power amplifiers in order to get high power efficiency. Since these efficient converters have large area and are expensive, it is not convenient to have these bulky-converters for each block and circuit. Linear regulators are used for most of the blocks due to its small size and ease of integration. Linear regulators are efficient when the dropout voltage is small. If a large number of linear regulators are used as on-chip regulators and since the efficiency of linear regulators decrease linearly with the increase of dropout voltage, the collective power loss in them may be significant [1]. For this reason, switched capacitor DC-DC converters are the more power efficient all integrated alternative which eliminates the need to use bulky inductor, consume a reasonable amount of area and have high efficiency in a broad range of output voltages. Moreover SC converters can generate higher, equal and lower output voltages compared to the input source [2].

1.2 Thesis Organization

The thesis is organized as follows. Basic background theory of the DC-DC converters focusing on switched capacitor converters and its loss mechanisms are explained in Chapter 2. Explanation of the proposed design and its implementation is described in Chapter 3. Layout issues faced and solutions are described in Chapter 4. Measurement results are given in Chapter 5. Finally, conclusions are given in Chapter 6.

Chapter 2

Background Theories

2.1 Classification of DC-DC converters

2.1.1 Linear Regulators

Linear regulators are used to provide voltage levels to sub- blocks by regulating the output voltage using a feedback loop. These regulators are used due to advantages of low area and cost, and they enable the PMIC to be integrated on the same chip [2]. However, linear regulators, as shown in Figure 2.1, suffer from efficiency limitations when the dropout voltage is quite large. The use of these linear regulators is only efficient for lower dropout voltages.

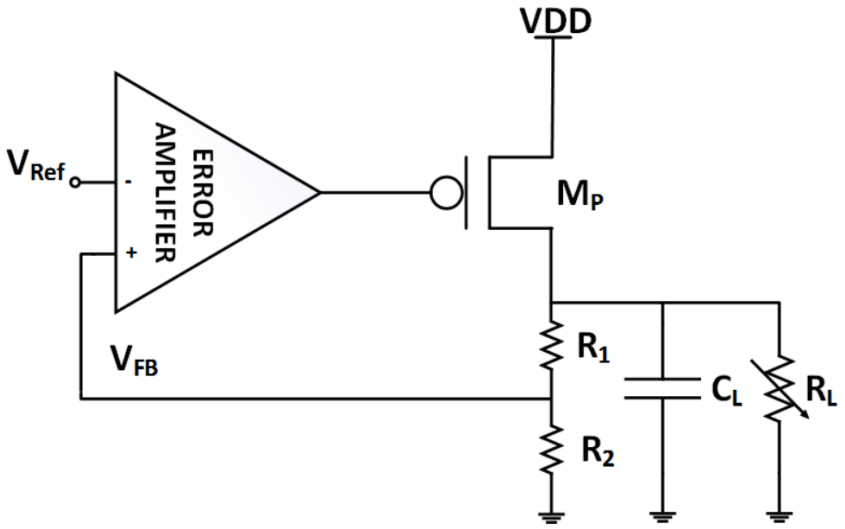


FIGURE 2.1: Typical circuit diagram of low-dropout regulators

2.1.2 Inductor-Based Switching DC-DC converters.

Off-chip inductor-based converters, shown in Figure 2.2, are mainly used to provide high output current with high efficiency. This kind of converters can generate different levels of DC voltages. This can be done by filtering a pulse-width modulated signal by an LC filter [1]. As explained earlier, Although Inductor-based switching DC-DC converters are energy efficient, they are expensive and consume large area. Hence, most of the low cost applications use linear regulators as DC-DC converters due to minimum area and cost.

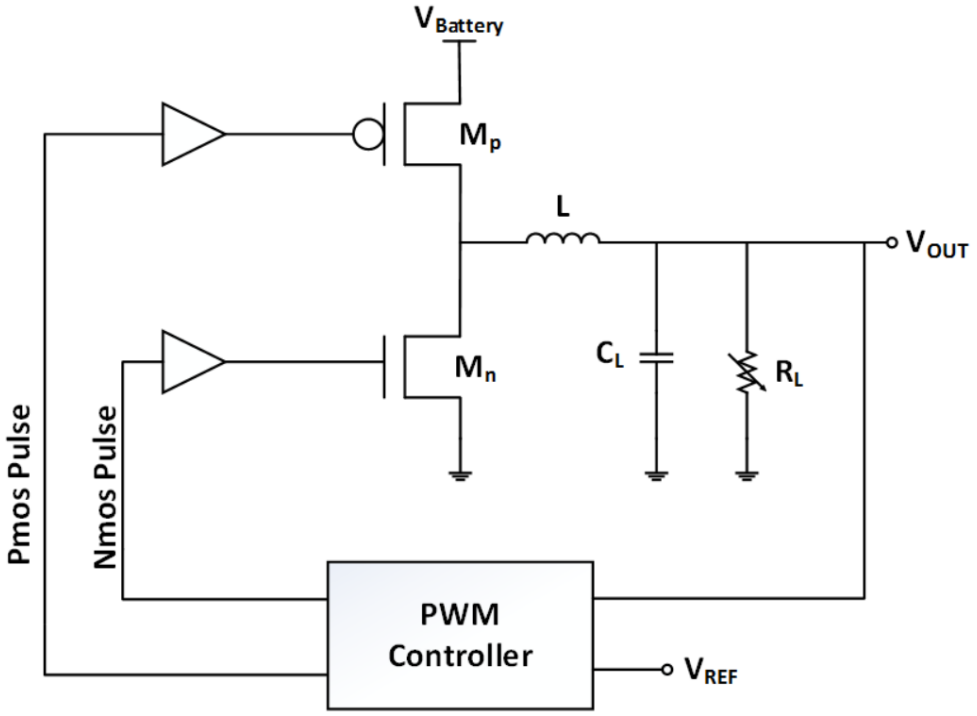


FIGURE 2.2: Typical circuit diagram of Inductor-Based Converters.

2.1.3 Switched capacitor DC-DC converters

Switched capacitor (SC) DC-DC converters, as shown in Figure 2.3, consist only of capacitors and switches. This enables the SC converter to be easily integrated on-chip. This kind of converters are like Inductor-based converters, they can provide different DC voltage levels. These levels can be generated according to the configuration of switches and capacitors. Output voltage can be equal, higher, lower or opposite in polarity compared to the voltage source as in Figure 2.3a, b, c and Figure 2.3d respectively [1].

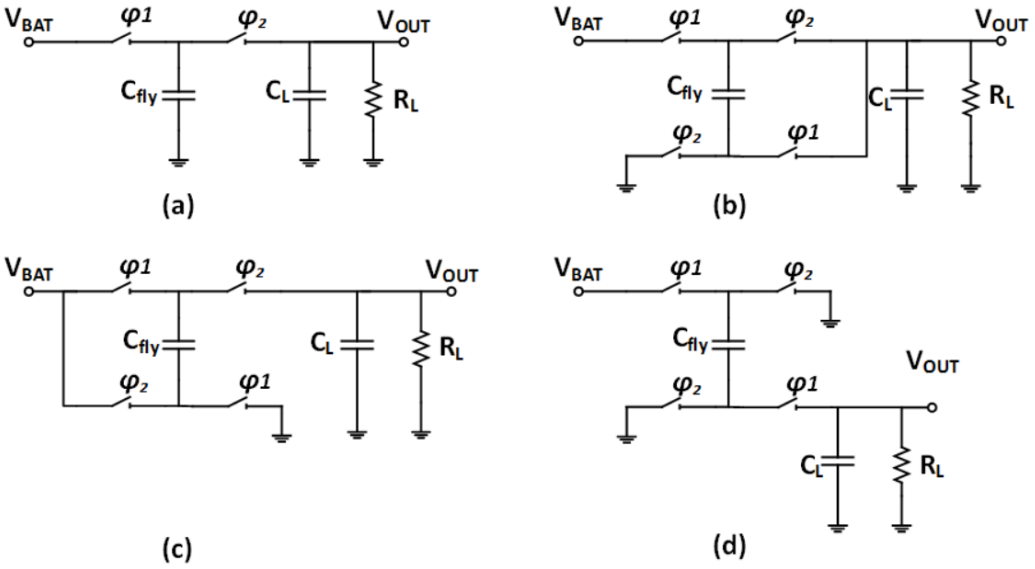


FIGURE 2.3: Switched Capacitor converters (a) 1-to-1 Topology (b) 2-to-1 Topology (c) 1-to-2 Topology (d) 1-to-(-1) Topology

With continuous CMOS technology scaling, SC DC-DC converters gain more attention since the switching frequency can be increased to reduce the total area of SC converters without degrading efficiency. This can be achieved because due to CMOS scaling, capacitance per unit area increases and the on-resistance per unit area decreases [1].

Table 2.1 summarizes the advantages and disadvantages of different DC-DC converter types [2].

Table 2.1: Summary for different types of DC-DC converters

Converter Types	**Advantages**	**Disadvantages**
Linear converters	• High efficiency for low dropout voltages. • No output ripples. • Smaller size and easy to be integrated. • Simple design.	• Poor efficiency for high dropout. • Can provide output for only lower than the input voltage.
Inductor-Based converter	• Very high efficiency.	• Complex design. • Not easily integrated • Bigger size.
SC converters	• Easy to be integrated. • Higher Efficiency than linear regulators for high dropout. • Can provide higher and opposite voltages.	• Only discrete number of output are possible at the peak Efficiency. • Slightly Less Efficient than inductor based converters. • Low output current compared to Inductor based converter.

2.2 Basic operation of switched capacitor Converters

The switches in the circuit shown in Figure 2.4, are operated by two non-overlapping clock signals, Φ_1 and Φ_2. By turning them on and off consecutively, the configuration of the flying capacitors changes.

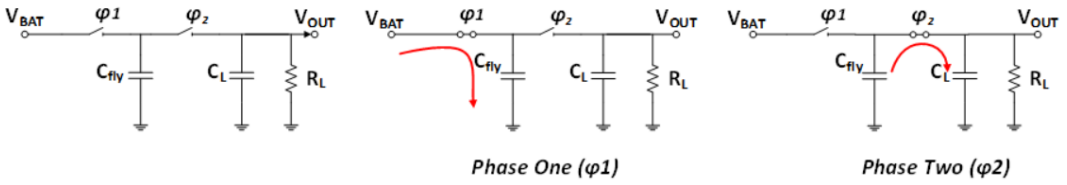


FIGURE 2.4: A 1:1 SC converter toplogy

During the first half period Φ_1, the battery charges the flying capacitor C_{fly} through the first switch. Similarly, during the next half period Φ_2 the second switch turns on and C_{fly} discharges into the load capacitor C_L. The charging and discharging time depends on the on-resistance of the switch, a small amount of voltage is dropped across the switch-on resistance. If it is assumed that the switch on-resistance is negligible, then the output voltage at no-load condition V_{NL} will be equal to the input battery voltage and the SC converter topology shown in Figure 2.4 is called 1-1 SC topology. For the real implementation, SC converters have some current load and switch on-resistance (R_{on}) is not negligible. Due to these load and switch on-resistances, output voltage V_L of the SC converter drops below the no-load output voltage V_{NL}. The difference between the V_{NL} and V_L is known as dropout voltage and is given by $\Delta V = V_{NL} - V_L$ [1]. The linear efficiency related with the SC converter is given by:

$$\eta_{LIN} = \left(\frac{V_L}{V_{NL}}\right) \tag{2.1}$$

Equation 2.1 shows that the efficiency degrades as V_L gets smaller compared to V_{NL}. Consequently, the converter has increased losses due to higher switch on-resistance Ron and parasitic capacitances. In order to have good efficiency, different SC topologies need to be implemented that can achieve small dropout voltage ΔV for different voltage ratios and current loads. In this dissertation, 1/2, 1/3, 2/3, 2/5 and 2/7 topologies are designed in order to have a wide range of voltages with maximum efficiency values achieved.

2.3 Loss mechanism in switched capacitor Converters

2.3.1 Conduction loss [charge transfer loss]

As was described before, the maximum attainable efficiency is limited by the value of V_L given in Equation 2.1. As the output voltage V_L drops below the no-load voltage V_{NL}, the maximum attainable efficiency decreases linearly in the same manner as a linear regulator. This loss is due to the charging and discharging of the capacitors through the on-resistance of the switch, Equation 2.2.

$$R_{ON} = \frac{L}{Kw(V_{GS} - V_t)} \tag{2.2}$$

When charge flows from battery to the load, some of it is dissipated on the switch resistance. The amount of the dissipated energy is given in Equation 2.3. Due to this loss, a lower value of VL will be generated and the efficiency will drop. This is one of the major drawbacks of SC converters and need to be addressed carefully.

$$P_{RSW} = I_{load}^2 . R_{ON} \tag{2.3}$$

2.3.2 Bottom plate and parasitic capacitor loss.

The second contributor of efficiency loss is the bottom-plate capacitors. The effect of the bottom-plate capacitors appear because they are being charged and discharged every clock cycle. It especially appears when MOS capacitors are used as transfer fly capacitors. For N-well capacitors, this parasitic capacitor is formed between the N-well and P-substrate due to the reverse biases diode junction capacitors. It scales with the capacitor dimensions, technology and the layout. If C_{BP} represent the bottom plate capacitance of the flying transfer capacitance C_{fly}, then

$$C_{BP} = \alpha . C_{fly} \tag{2.4}$$

where α is a technology depended constant and the power loss associated with bottom plate capacitance is given as [1]:

$$P_{BP} = f_{sw} . \sum_i C_{BP,i} . V_{bp,i}^2 \tag{2.5}$$

where f_{sw} is switching frequency, C_{bp} is bottom plate capacitance and V_{bp} is the maximum voltage swing across bottom plate capacitance.

Consider the SC 1/2 topology in Figure 2.5. During phase 1, all switches connected to Φ_1 are shorted and the two capacitors are charged to half of the battery voltage. In the next phase, the switches connected to Φ_2 are closed and the fly capacitors transfer charge to the output capacitor C_L. Bottom-plate capacitor of the upper fly capacitor is also charged to half the battery voltage in Φ_1 and the charges in it is wasted in Φ_2 as it is connected to ground from both terminals. Consequently, this energy loss can result in notable efficiency degradation [2].

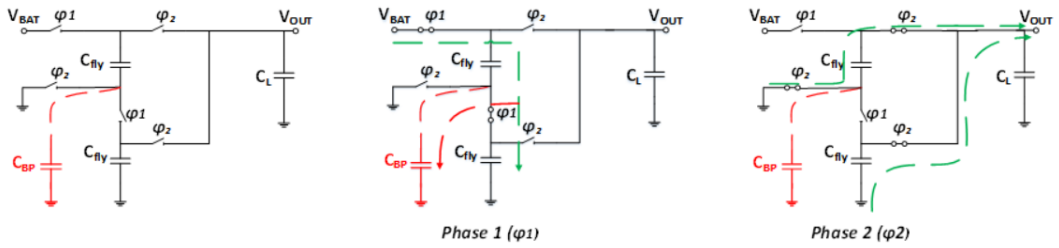


FIGURE 2.5: A 1:2 SC Topology with bottom plate capacitance

2.3.3 Gate-drive loss

When transistors are used as switches, the gate and parasitic capacitors associated with them are charged and discharged to clock levels every cycle. Power consumed in this process is known as switching power and it is given by

$$P_{CW} = f_{sw} . \sum_{i} C_{MOS} . V_i^2 \tag{2.6}$$

Where CMOS represents the MOSFET parasitic capacitances given in Equation 2.7 and shown in Figure 2.6 . Vi is the maximum voltage swing across the transistor.

$$R_{ON} = \frac{\epsilon . w . L}{t_{ox}} \tag{2.7}$$

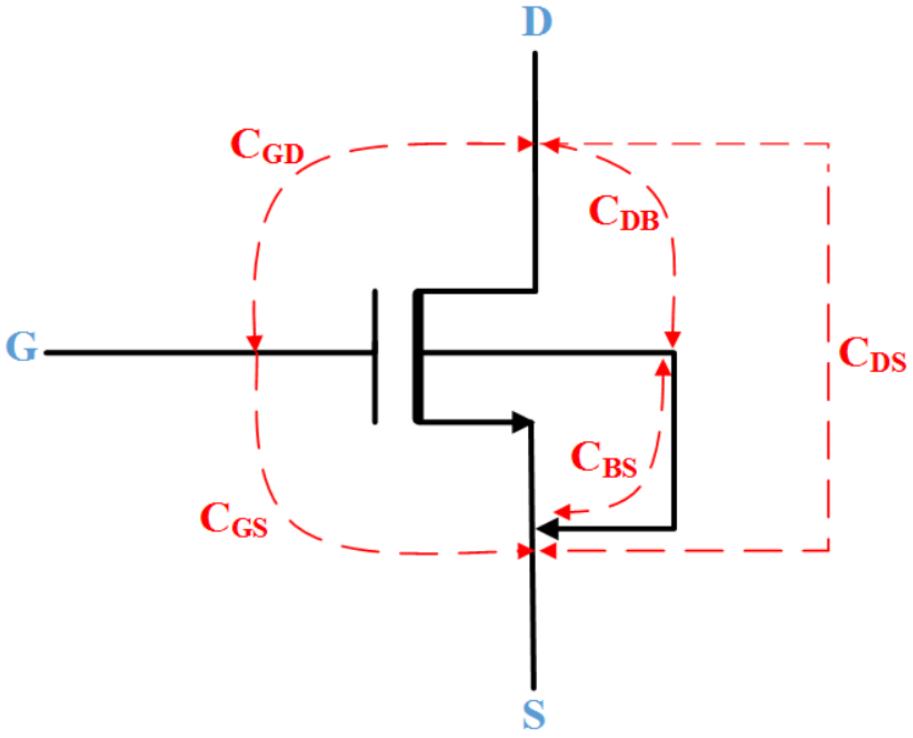


FIGURE 2.6: MOS transistor parasitics capacitances [2]

Increasing transistor width will increase the parasitic capacitances associated with the transistor. On the other hand, increasing the transistor width will decrease on-resistance of the transistor (RON). Hence, there is an optimum sizing for each switch that can achieve the minimum possible parasitic capacitance and minimum on-resistance [2].

2.3.4 Control circuit loss

The SC core topologies will be surrounded with control circuitry in order to achieve constant voltage regulation. These control circuitry such as comparators, digital blocks and reference voltage generators must be insensitive to process, supply voltage and temperature variations. These circuits usually require constant energy for their operations. The power lost in the control circuitry is especially a concern when delivering ultra-low load power levels [1]. The power lost in every switching cycle can be broken into switching and leakage power losses and is given by Equation 2.8

$$P_{CNTRL} = C_{CONT}.V_{BAT}^2.f_{sw} + I_{leak}.V_{BAT} \tag{2.8}$$

where C_{CONT} is the equivalent capacitance switched in the control circuitry per cycle, I_{leak} is the total leakage current in the control circuitry.

The overall efficiency, given by equation 2.9 and taking into account all the above mentioned losses, can be expressed as the ratio of the power delivered to the load to the sum of all the power losses and the power delivered to the load.

$$\eta = \frac{P_L}{P_L + P_{Csw} + P_{Rsw} + P_{bp} + P_{cntrl}} \tag{2.9}$$

Here, P_L is the total output power, P_{Csw} is the switching power loss due to gate capacitance, P_{Rsw} is the switching power loss due to on-resistance, P_{bp} is the bottom plate capacitance power loss and P_{cntrl} is the control circuitry power loss.

2.3.5 Output Ripple

SC DC-DC converters suffer from output ripple. Since many electronic circuits are voltage sensitive, they need a clean and stable voltage supply [2]. Therefore, it is important to reduce the output ripple as much as possible. Additionally, output ripple causes additional power loss due to charging and discharging of the capacitors with the ripple amount. Ripple can be reduced by increasing the switching frequency, increasing the fly capacitor amount, increasing the output capacitance or decreasing the parasitic resistance R_{ESR}.

Interleaving is another approach that can be used to decrease the output ripple. Since the flying capacitors are charged/discharged through a resistance, R_{ESR}, the charge/discharge glitches may be significant. These glitches and the abrupt charge transfer to the load capacitor are the main causes of the output ripple. The main idea of interleaving is to have more than one working core connected in parallel with shifted clocks feeding into them. For example, a 4-way interleaving uses four different phases (0o, 90o, 180o and 270o) of the input clock. With interleaving, fly capacitor can be divided into smaller components and charge is transferred to the output in small portions at each phase. This causes a smaller but increased frequency ripple at the output.

In normal operation of SC converter, during phase-One, flying capacitors are charged by the battery. During phase-Two, flying capacitors are discharged into output capacitance C_L. If high current is drained at the output, the DC-DC converter cannot provide enough charge to the output to keep the output voltage constant. In order to address this issue, either bigger flying capacitance need to be used or the switching frequency need to be increased. For lower output ripple, interleaving technique can be implemented or the load capacitor can be increased. This way, output capacitance C_L discharge slowly as a result of higher capacity, which give the flying capacitance time to charge it back and keep the output voltage nearly constant with low ripple [2] [3].

2.3.6 Summary of losses

As mentioned in the previous sections, SC DC-DC converters suffer from many kinds of losses. If we substitute the MOSFET parasitic capacitance (Equation 2.7) and on-resistance of the switch (Equation 2.2) in Equation 2.6 and Equation 2.3 respectively, we see that the transistor width (w) and the switching frequency(fSW) are the main factors in determining the power loss and ripple in the SC DC-DC converters as shown in Table 2.2 .

Increasing switch width will increase the gate parasitic capacitance but will decrease the on-resistance of the switch. Likewise, increasing the switching frequency will decrease the output ripple, but at the same time increase the bottom plate losses. Consequently, there is an optimum width and switching frequency that give minimum losses and optimal ripple amplitude.

TABLE 2.2: Summary for different types voltage control techniques

Conduction Loss $P_{Rsw} = I_{load}^2 \cdot \frac{L}{Kw(V_{GS}-V_t)}$	**Bottom Plate Loss** $P_{bp} = f_{sw} . \sum_i C_{BP,i} . V_{bp,i}^2$
Gate Drive Loss $P_{Csw} = f_{sw} . \sum_i \frac{\epsilon . w_i . L}{t_{ox}} . V_i^2$	**Output Ripples(OR)** $O.R. \ \alpha \ \frac{1}{f_{SW}}$

2.4 Control Techniques

Various techniques are used to control the operation of SC DC-DC converters. These techniques include changing parameters such as switching frequency, pulse width, charge transfer capacitor size [2] and switch sizes according to the output current requirements using a lookup table [4]. Some of the important controlling schemes are explained below.

2.4.1 Pulse frequency modulation (PFM) technique

Pulse frequency modulation (PFM) technique is one of the most popular techniques used to control high performance SC DC-DC converters to output a desired voltage level. High efficiency can be achieved over a wide load current range since the bottom-plate and control losses scale with the switching frequency (f_{sw}) as shown in Equation 2.5, 2.6 and 2.8.

The PFM consists of dynamic latched comparators and a resistance divider at the output to provide a feedback voltage as shown in Figure 2.7. The basic operation principle of the PFM technique is as follows. At the rising Edge clock, the dynamic latched comparator compares the feedback voltage (V_{FB}), which is a scaled version of the output voltage, with the given reference (V_{REF}) as shown in Figure 2.8. When the output voltage (V_L) falls below the defined reference voltage (V_{REF}), the dynamic latched comparator permits the clock to be connected to the SC converter to charge its capacitors. When the output voltage (V_L) goes above the reference voltage (V_{REF}), the comparator blocks the clock connection to maintain the desired output voltage. In this manner, the feedback voltage can be regulated at a voltage near the reference voltage [5] [6].

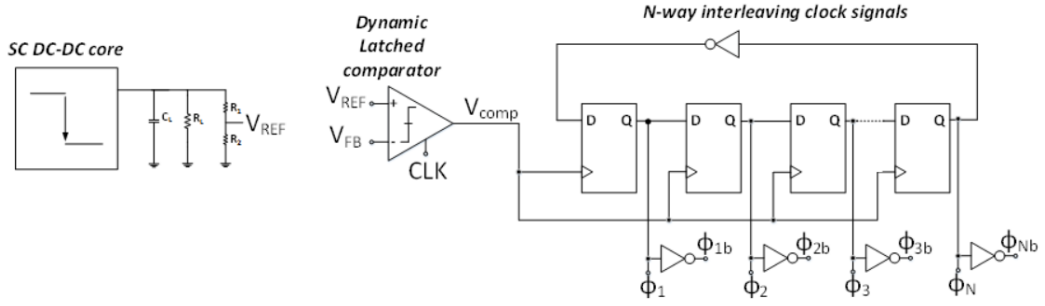


FIGURE 2.7: Voltage regulation using frequency pulse modulation

The drawback of this method is the large output ripple voltage especially at light output load condition. Since the flying capacitor is relatively large compared to the amount of charge needed to supply the required output load current, the output current ends up

being large. This large flying capacitor delivers large amounts of charge to the output every cycle, which makes the output voltage overshoot as shown in Figure 2.9 [1].

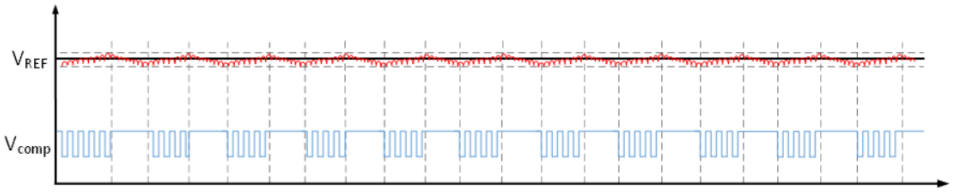


FIGURE 2.8: Basic Operation of frequency pulse modulation

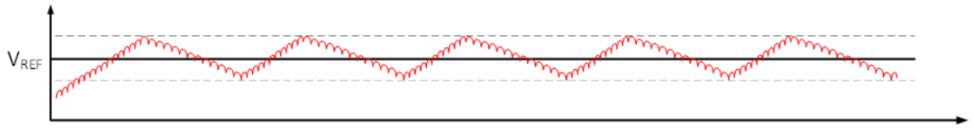


FIGURE 2.9: Overshoot due to small load and relatively large flying capacitor

2.4.2 Switch width modulation technique

If the switching frequency is fixed, the amount of charge delivered to the load can be controlled by either the capacitor or switch size [1]. In slow switching regime, switches have enough time to charge the flying capacitors so the limitation of charge transferring from the input to the output comes from the flying capacitor sizes and the amount of charge that can be stored in them. In fast switching regime, there is not enough time to deliver the charge to the load. This limitation is due to the switch conductance. Increasing or decreasing the width of the transistor can help controlling the amount of charges that can be delivered to the load [7, 8].

The switch width modulation technique consists of multiple switches connected in parallel as shown in Figure 2.10 and controlled by a decision making unit which is usually a look up table [4]. The main disadvantage of switch width modulation is that, even though the sizes of switches are scaled with the load amount, the bottom plate parasitic capacitor does not scale with change in load current, therefore the losses stay the same. In addition, it is difficult to have an acceptable efficiency over a large load current range by only controlling the switch widths [1].

2.4.3 Switch width modulation technique

As mentioned in section 2.4.2, capacitor size dominates the losses in the slow switching regime. Flying capacitor modulation is similar to switch width modulation. With this

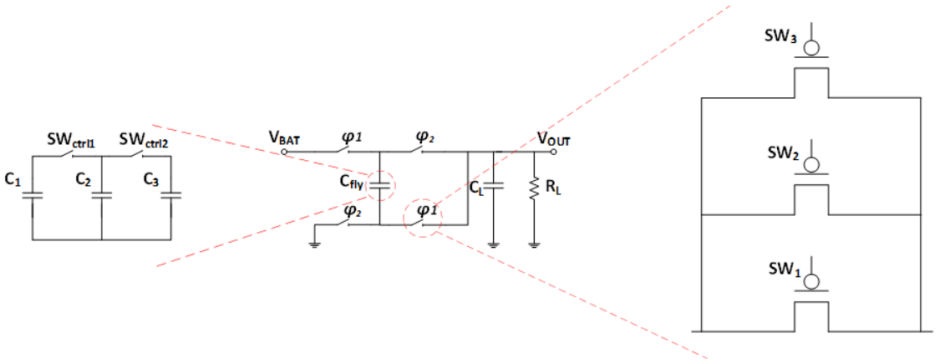


FIGURE 2.10: Voltage regulation using switch and capacitor modulation

technique, the amount of capacitance that takes part in the charging process is changed according to the output load current as shown in Figure 2.10. The advantage of this technique is that by scaling the capacitor size, the bottom plate capacitor is also scaled. This in return decreases the losses of the switched capacitor core. However, as in the switch width modulation case, it is difficult to have acceptable efficiency over a wide load current range only by controlling the capacitor size [1].

Table 2.3 summarizes the advantages and disadvantages of different control techniques [2].

TABLE 2.3: Summary for different types voltage control techniques.

Control Technique	**Advantages**	**Disadvantages**
Frequency pulse modulation	• Ease of implementation.	• large peak-to-peak output ripple voltage especially at the light load condition. • High power consumption of the comparator as it works at fast clock.
Switch width modulation	• Ease of implementation.	• Switching losses is higher at smaller loads due to constant frequency. • Optimum efficiency is not achieved due to changing pulse width.
Capacitor modulation	• Bottom plate parasitic capacitance losses reduce at smaller load currents.	• Requires more complicated structure of charge transfer capacitors.

Chapter 3

Implementation of Switched Capacitor DC-DC Converter

Chapter two provided the advantages and disadvantages of switched capacitor regulators and their basic operation. Moreover, it showed the aspects of losses that the SC regulator suffers and how to minimize them. Finally, it showed various kinds of control techniques that were commonly used recently in the literature to achieve maximum possible efficiency. This chapter focuses on the design of a fully integrated all-CMOS SC DC-DC regulator to provide a wide range of output voltages from 0.94 V to 2.2V using a 3.3 V input supply. This converter has five different gain configurations and can provide output load current in the range of 20uA - 4.3mA with high efficiency, therefore it is suitable for integration with ultra-low voltage (UVL) and ultra-low power (UVP) applications such as bio-sensors and sensor networks. The proposed design uses a feedback control loop to control and improve the overall power efficiency. This loop uses frequency scaling, switch width scaling techniques and reduces the number of interleaver stages as needed.

3.1 Architecture of the converter

The proposed architecture is shown in Figure 3.1. The design consists of multi-gain all-CMOS core converter and a feedback control loop. The loop comprises of 2-dymanic latched comparators, a frequency divider, a 4-phase non overlapping clock generator, a decision making unit and a reference voltage generator. The converter reaches its steady state when Equation 3.1 is achieved.

$$V_{th1} < V_L < V_{th2} \tag{3.1}$$

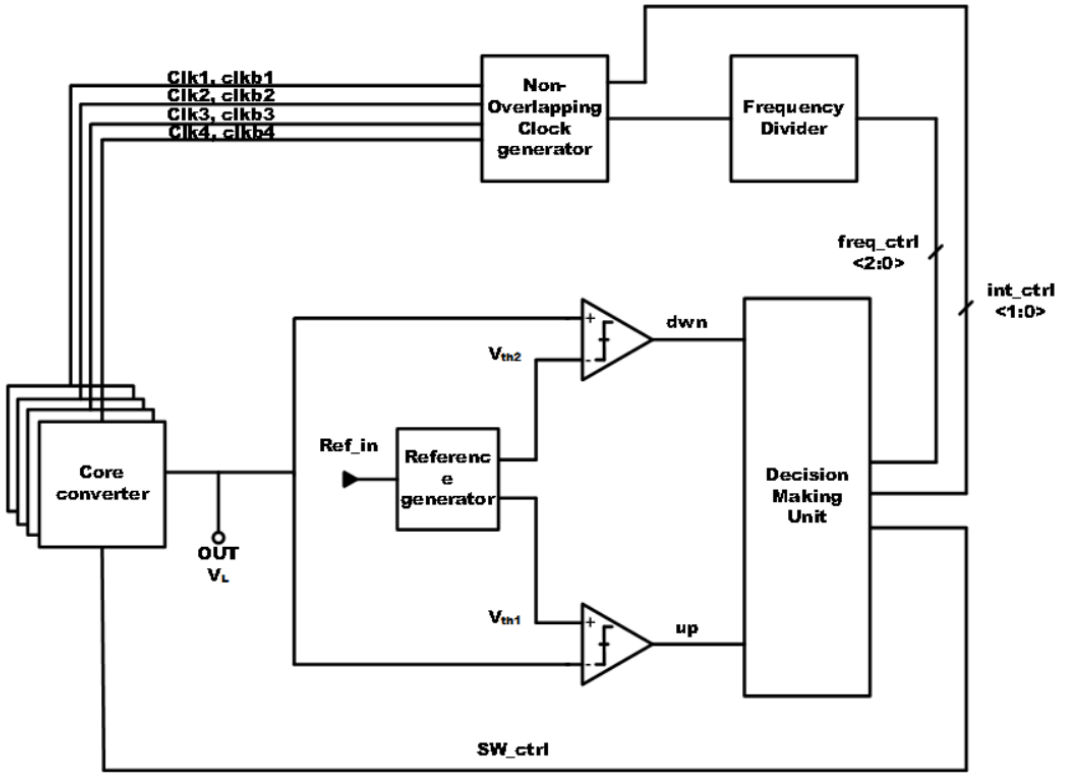


FIGURE 3.1: Voltage regulation using switch and capacitor modulation

3.2 Multi-gain switched capacitor converter.

The switched capacitor core is designed to support a wide range of output voltages. 1/2, 2/3, 1/3, 2/5 and 2/7 are the five gain configurations combined in Figure 3.2. Gain topology is set by gain selection logic controlled manually by the user. Once the gain value is set, switches and capacitances of the core converter change their orientations with the settings given in Table 3.2. After the gain topology is set, when the converter is

started to be clocked, it switches between common phase and gain phase. With switching between two phases, transfer of charges from the input to the output is done by way of the flying capacitances. Table 3.1 shows each of the switches and in what setting and phase they are activated.

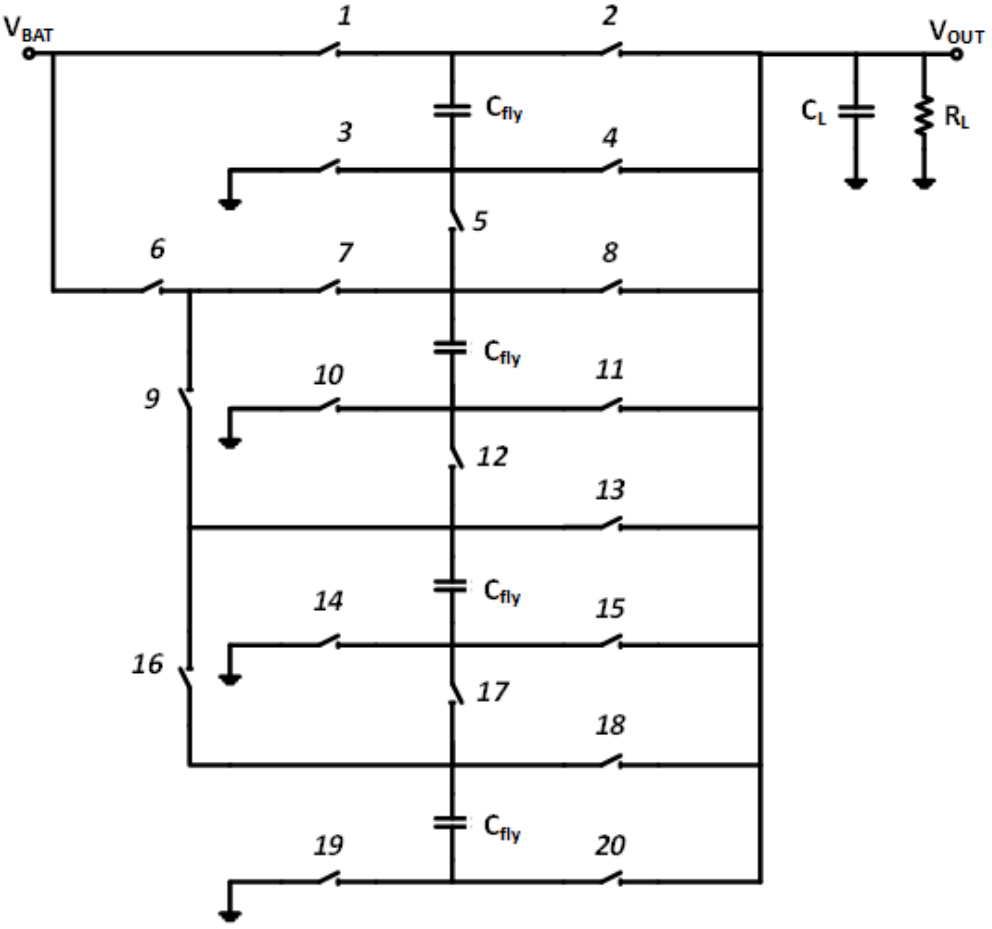
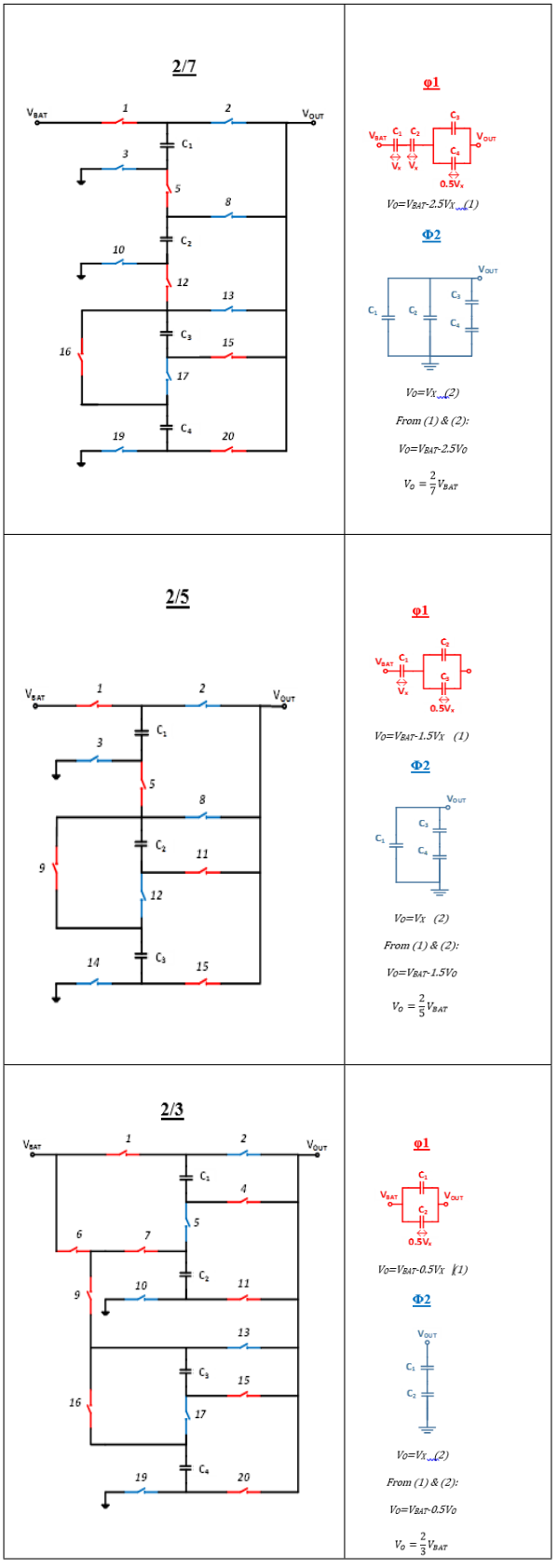


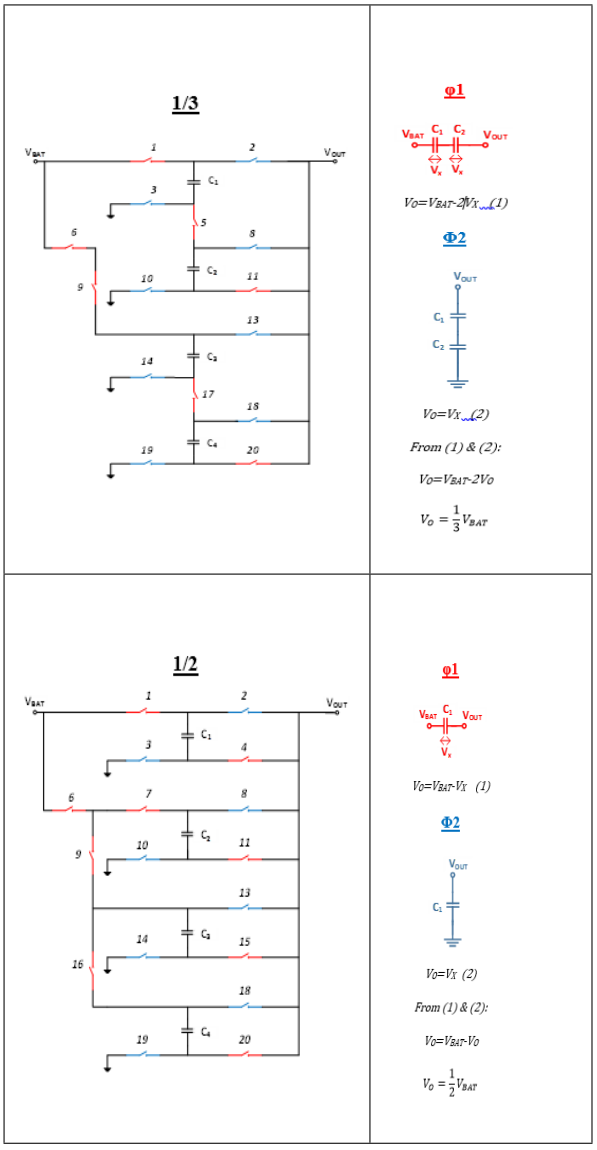
FIGURE 3.2: Proposed SC topologies combined

TABLE 3.1: Switches and its phases

SW	**phase**	**SW**	**phase**
1	Φ1	3	Φ2 [2/7,2/5,1/2,1/3]
2	Φ2	4	Φ1 [2/3, 1/2]
7	ON all except 1/3	9	Φ1 [2/5,2/3,1/2,1/3]
8	Φ2 [2/7, 2/5, 1/2, 1/3]	10	Φ2 [2/7,2/3,1/2,1/3]
13	Φ2 [2/7, 1/2, 2/3, 1/3]	15	Φ1 [2/7,2/5,1/2,2/3]
14	Φ2 [2/5, 1/2, 1/3]	16	Φ1 [2/7,2/3,1/2]
19	Φ2 [2/7, 1/2, 2/3, 1/3]	20	Φ1 [2/7,2/3,1/2,1/3]
5	Φ1 [2/7, 2/5, 1/3] ϕ [2/3]	6	Φ1 [2/3,1/2,1/3]
11	Φ1 [2/5, 1/2, 2/3, 1/3]	12	Φ1 [2/7] ϕ2 [2/5]
17	Φ1 [1/3] ϕ2 [2/7, 2/3]	18	Φ2 [1/2,1/3]

TABLE 3.2: Core-topologies and phase-illustration




1/3
φ1
Φ2
1/2
φ1
Φ2

3.2.1 Switch type selection

The choice of using NMOS or PMOS switches depends on the switch location in the core converter [2]. The NMOS transistor is preferred if it is connected to ground due to its ability as a good pull down device and vice versa for the PMOS. Moreover, NMOS is preferred over PMOS because it's high mobility and smaller size for the same on-resistance. If a switch is neither connected to ground nor VDD, it is preferred to be implemented as a pass-gate as shown in Figure 3.3.

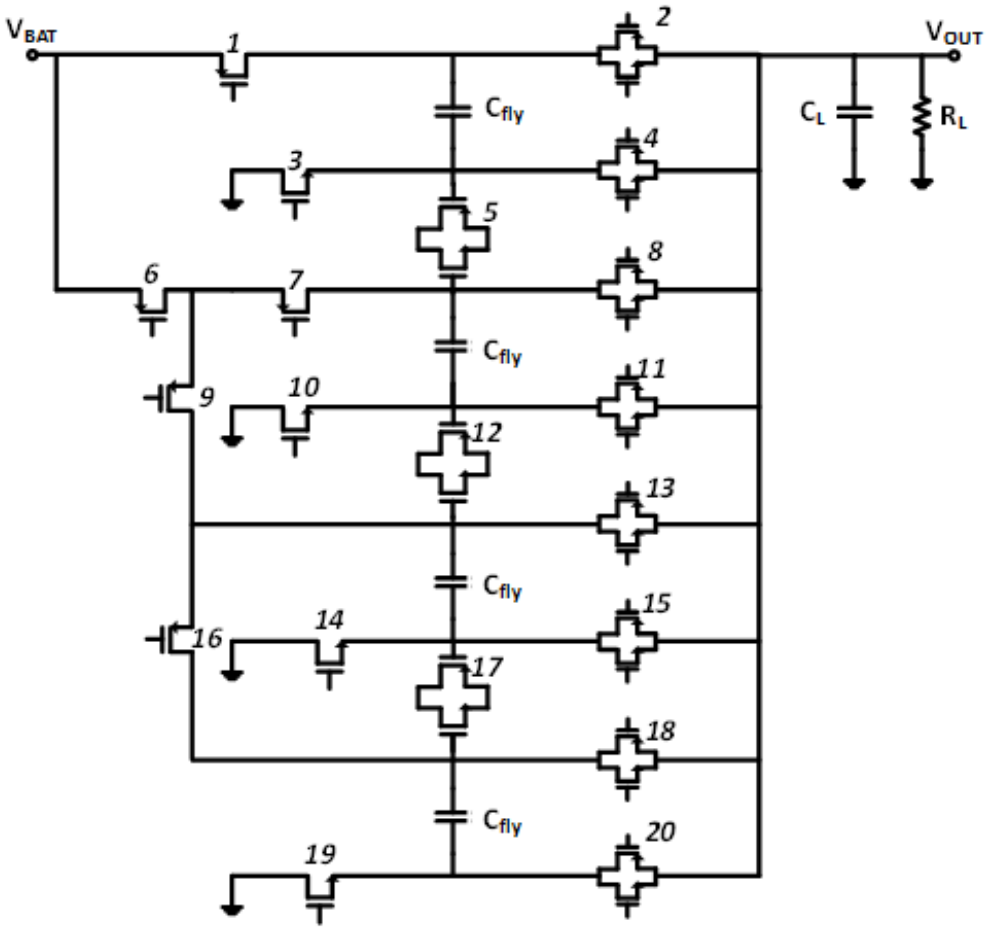


FIGURE 3.3: Proposed SC core topology implemented in CMOS

3.2.2 Capacitor selection

Choosing which capacitance to use, depends on two main properties; capacitance per unit area and bottom-plate capacitance (α) [2] [7] [5]. There are three popular types of capacitors, which are shown in Table 3.3.

TABLE 3.3: Summary of the possible capacitances used in SC DC-DC converter [2]

Capacitor type	Features
MOM capacitance	• MOM capacitance is formed from regular metal layers. • Does not require additional mask or extra process. • Capacitance per unit area 1.5 fF/um^2 • Bottom plate parasitic capacitance (α) is 5 to 10% of the whole capacitance.
MOM capacitance	• MiM capacitance is formed by two metal layers with a thin dielectric layer between them. This layer has very high dielectric constant enabling a better capacitance density. • It requires additional masks and process steps. • They are built far from the substrate to reduce the bottom plate capacitance. • Capacitance per unit area 5 fF/um^2 • Bottom plate parasitic capacitance (α) is less than 1% of the whole capacitance.
MOS Capacitance.	• MOS capacitance is implemented using transistor's gate-oxide capacitor. The gate dielectric has the highest dielectric which enable a better capacitance density. • It does not require any additional masks or process steps. • They are built far from the substrate to reduce the bottom plate capacitance. • Capacitance per unit area 10 fF/um^2 • Bottom plate parasitic capacitance (α) is 5 to 10% of the whole capacitance.

MOS Capacitance is chosen to be implemented due to its high capacitance per unit area and because it does not require any extra mask or process. Normal CMOS transistor has a diode between drain/source and the substrate, as shown in Figure 3.4. This diode is off and acts as bottom plate capacitor. Using triple well CMOS-transistor as a capacitor, as shown in Figure 3.5, will reduce its bottom plate capacitance. The deep N-well CMOS transistor will add other diodes in series with the pre-existing diode, reducing the total amount of parasitic capacitance.

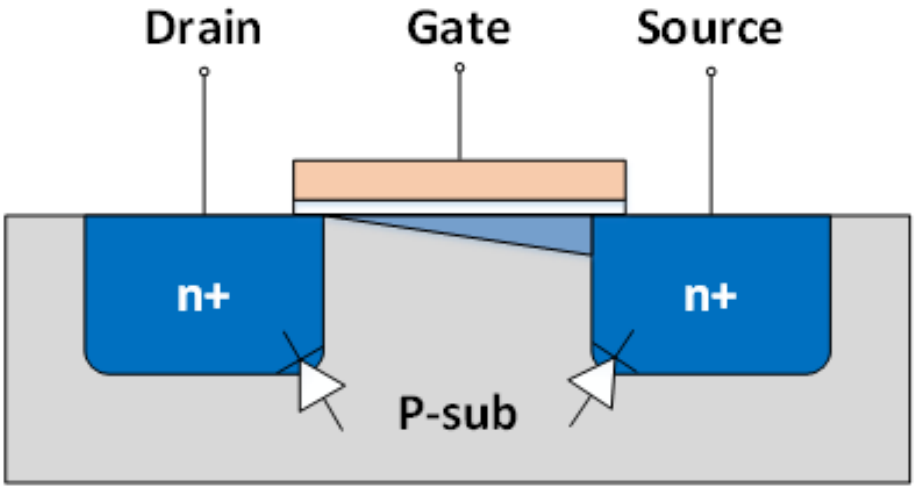


FIGURE 3.4: Conventional NMOS transistor cross-section showing bottom plate capacitor.

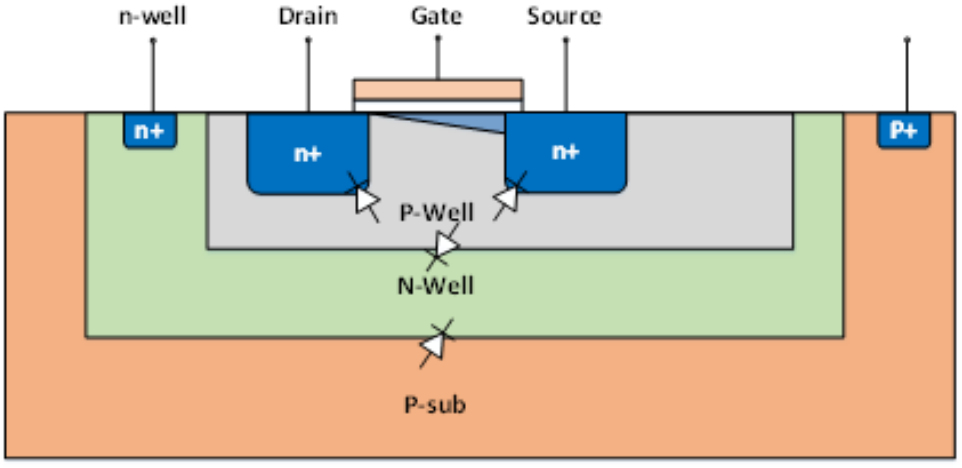


FIGURE 3.5: Deep NMOS transistor cross-section showing bottom plate capacitor.

3.3 Feedback control loop

Controlling the converter for high efficiency using only one parameter is difficult, especially if the converter supplies a wide range of output load current values. In order to keep the efficiency high in this wide range, a feedback control that uses frequency scaling is used as a main control scheme. Additionally, the number of interleavers are scaled at very low current loads and switch width scaling is used.

The basic operation of these control schemes is as follows; Firstly, two threshold voltages are generated (V_{TH1} and V_{TH2}) to be used as references that the output voltage of the converter is compared to. When the converter initially starts, all the cores work with minimum switch width and the decision making unit gradually increases the frequency until the output voltage reaches the minimum threshold voltage (V_{TH1}). When the output voltage crosses (V_{TH1}), the converter keeps the frequency constant until it drops below (V_{TH1}) or it crosses (V_{TH2}). In these cases, it increases or decreases the frequency respectively. This way, the comparator tries to maintain a steady state frequency and output voltage by measuring output voltage and keeping it between (V_{TH1}) and (V_{TH2}).

At low-output load currents, the decision making unit decreases the frequency until it reaches minimum frequency. If the (V_L) is still bigger that (V_{TH2}), the decision making unit starts turning off interleavers until the steady state output voltage is achieved in equation 3.1 or only one interleaver is left operating. Conversely, at high-output load currents, the decision making unit starts increasing the frequency until it reaches its maximum. If (V_L) is still smaller than (V_{TH1}), the DMU starts to scale the switch sizes up until the steady state condition in equation 3.1 is achieved or maximum switch size is achieved. When the load current value jumps from high to low or from low to high suddenly, the opposite of the procedure explained above is followed.

3.3.1 Frequency Scaling and frequency divider.

The nominal clock input to the converter was chosen to be 12 MHz. This clock value is not suitable for all the current loads since the switching frequency with high efficiency is directly proportional to the output current load as shown in equation 3.2 [4]. A frequency divider as shown in Figure 3.6 is used to scale the frequency that goes into the non-overlapping clock generator block. Frequency divider takes in the external clock and divides it into seven different clocks and the working/output clock is selected by the decision making unit according to the control unit decision as explained above.

$$I_L = 4C_{fly}\Delta f_{sw} \tag{3.2}$$

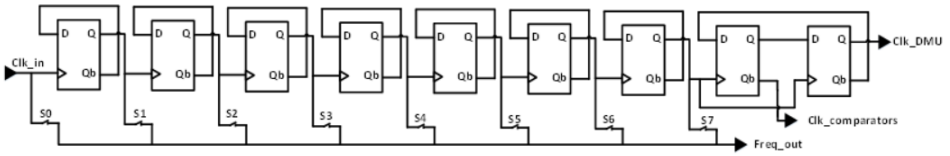


FIGURE 3.6: Proposed frequency divider.

Frequency division is achieved by seven cascaded stages of divide-by-2 circuits that consist of D-flip flops. Eight switches in series with the input clock and divided clocks are used to allow/block the frequency selected to the comparator. These switches are controlled by the decision making unit. The additional two D-flip flops to the right of Figure 3.6 are used to generate slower and ninety-degree phase shifted clocks, which are used for the comparators and the decision making unit to overcome any race conditions in the DMU and instability in the loop.

3.3.2 Interleavers and switch scaling.

At low-output currents, the efficiency of the converter decreases since the control circuitry current dissipation becomes comparable or larger than the output load current. One way of improving the efficiency is to turn off some of the interleavers to get rid of the circuitry overhead that is used to control these interleavers. Power dissipated in the control circuitry is shown in equation 2.8 and a portion of this dissipation will be eliminated as a result. 4-phase non overlapping clock generator is turned off when the current is too low, and it is reconfigured into a single inverter to generate an 180o phase shift. On the other hand, the output ripple magnitude increase as we turn off the interleavers since the output discharges more before it is recharged again. This is usually acceptable because, when the output current is very low, the circuitry that the converter feeds is in sleep mode or performance degradation is acceptable.

At high-output currents, the converter works at maximum frequency to meet the steady state output voltage condition. If the converter fails regulate to the desired value, switch width scaling is applied and the switch sizes are increased gradually until the converter output reaches the desired value (decreasing the on-resistance minimizes the voltage losses) as explained in section 2.3.1 by allowing more charge to transfer to the load.

3.3.3 Decision making unit

The decision making unit (DMU), as shown in Figure 3.8, controls the converter to achieve the maximum possible efficiency. The DMU consists of a 3-bit up/down counter

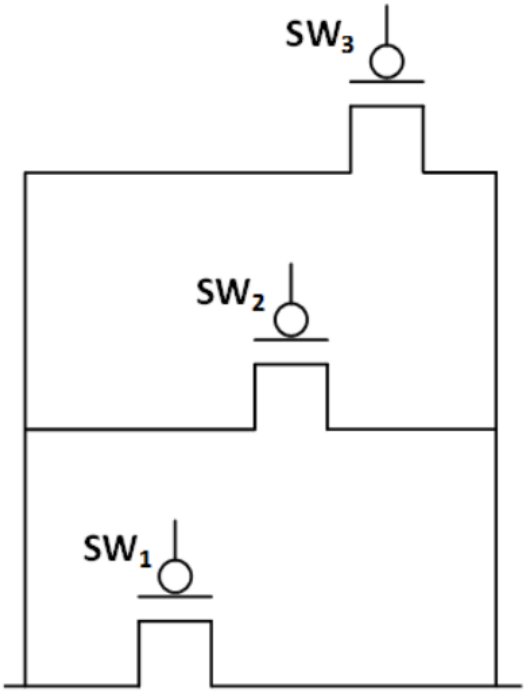


FIGURE 3.7: Switch size scaling example.

which is used to control the frequency scaling technique and a finite state machine to control the number of interleavers used and the switch width scaling as shown in Figure 3.9.

The up/down counter counts up or down each time the comparator decisions indicate that the output voltage is lower than V_{TH1} or higher than V_{TH2} respectively. The counter output controls the output-switches of the frequency divider to double, halve or keep the converter frequency after each decision. A block diagram of the DMU is shown in Figure 3.9. The Finite State Machine state diagram is shown in Figure 3.9 and works as explained throughout this chapter.

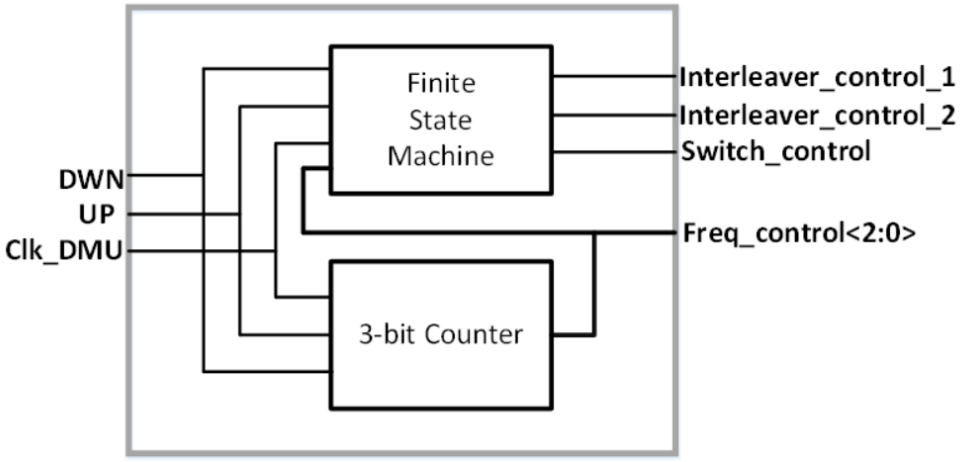


FIGURE 3.8: Proposed decision making unit.

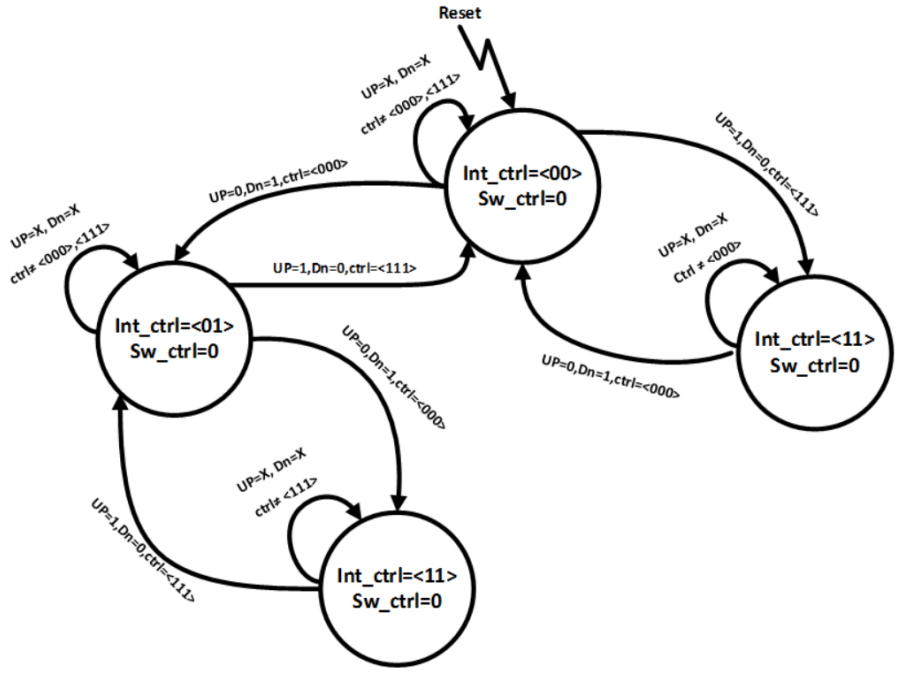


FIGURE 3.9: Proposed finite state machine.

Chapter 4

Layout

This chapter presents layout design and floor planning. Layout was done with Cadence Layout XL. While designing and floor-planning the converter, the following rules were taken in consideration.

- Make layout as symmetric as possible.
- Use wide and high metal layers for the input, output and the power rails of the converter.
- Add as many Vias as you can to decrease path resistance.
- Put as much bypass capacitance as you can.
- Clock must have the same delay for all the 4 cores and have same delay for the 2 comparators.

UMC CMOS technology provides 8 metal layers and the lowest resistance is the highest metal. Consequently, metal-8 is used in all power rails and in the input/output traces. In addition to making this metal wider to decrease the resistance, adding as many vias as possible at connections between metal layers is very important. These approaches make the layout more reliable and prevents the currents from tunneling through a small number of vias, especially in the wires near the flying capacitors where the resistance adds to efficiency drops. Additionally, increasing the width of the metal increases the parasitic capacitance, which can help in output ripple suppression.

The core is designed to be as symmetric as possible as shown in Figure 4.1. One core is laid-out and copied to four sides symmetrically to reduce mismatch. The rest of the circuitry is put in the middle of the four cores in order to make sure that the clock delay is nearly identical for all four cores.

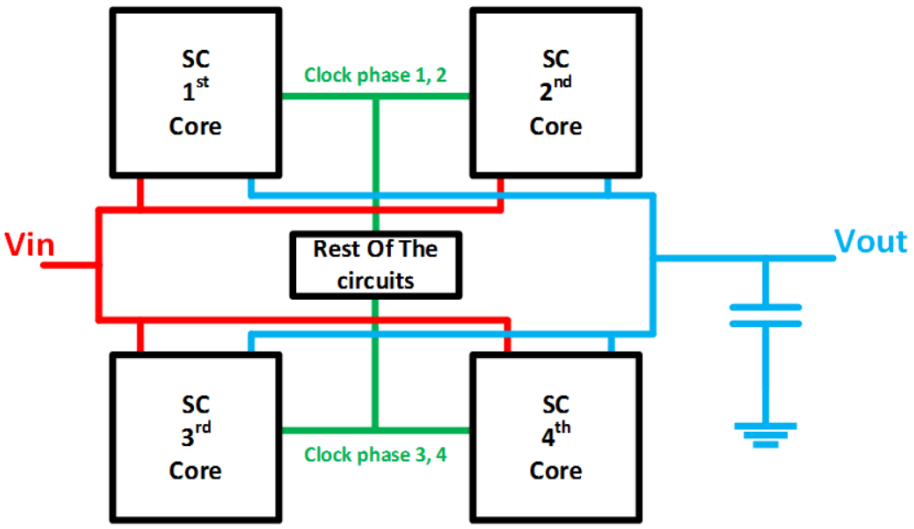


FIGURE 4.1: Initial layout proposal.

Figure 4.2 shows the overall layout of the deigned converter. It occupies an active area of 0.725 mm^2. The area of single flying capacitor [48.7 pF] is 0.035 mm^2 and the size of the single core, which contains four capacitors of 194.8 pF size, is 0.156 mm^2.

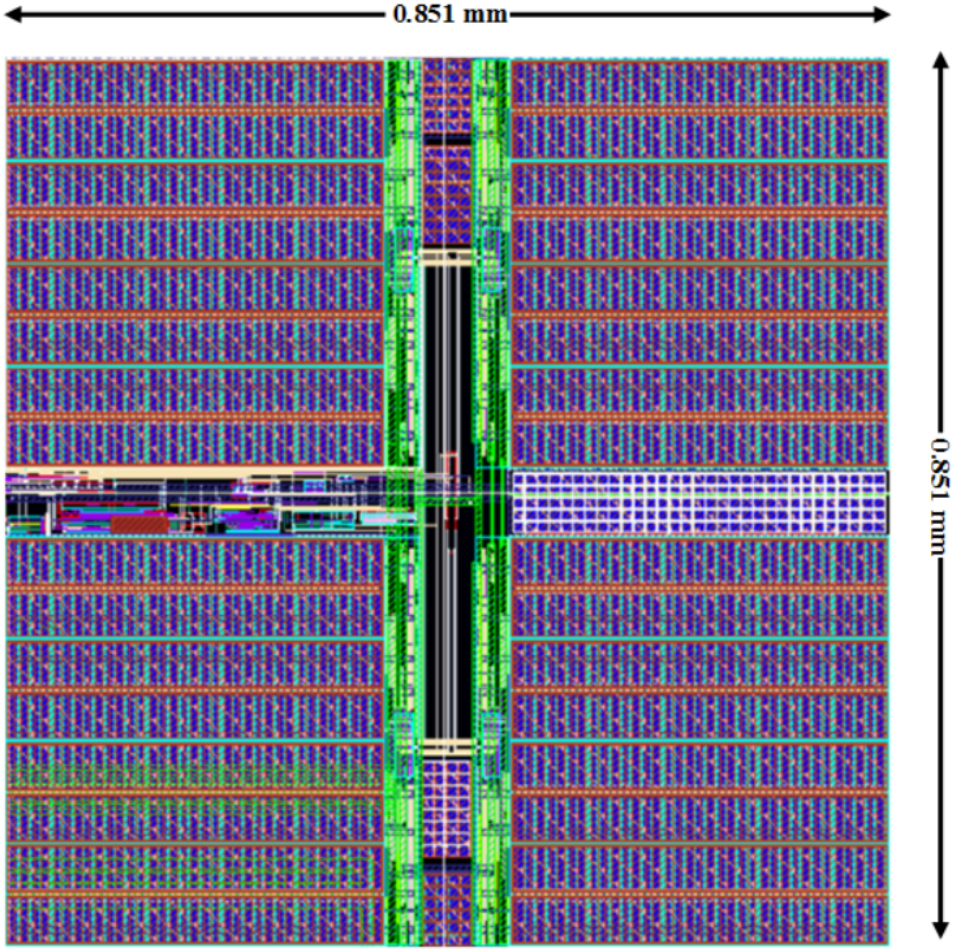


FIGURE 4.2: Overall layout.

Chapter 5

Measurements and Simulations

Based on the proposed architecture, the circuit was designed using 65 nm Bulk CMOS technology and was fabricated by UMC. CMOS capacitors were used as flying capacitors due to their high capacitance density compared to other types of capacitance in order to minimize the area. The core converter uses 48.7 pF for each flying capacitor and the total capacitance in the core is 780 pF. The efficiency in the results were calculated using the Equation 2.9. Only 1/2, 2/3 and 1/3 were successfully measured and the rest were not able to be measured due to a misconnection in the layout, which disabled the modes. Simulation and measurement results are shown in the figures below and general conditions of the simulation are listed in the Table below. M stands for measurement results, S stands for simulation results, and Scale shows the results with interleaving and switch size scaling enabled:

Table 5.1: Summary of general simulation conditions.

Input voltage	3.3V	**Temperature**	27 o C
Process model	Typical	**Output voltage**	0.94V $\sim$ 2.2V
Output ripples	5.4mV$\sim$ 14.6mV	**Output Capacitance**	5nF

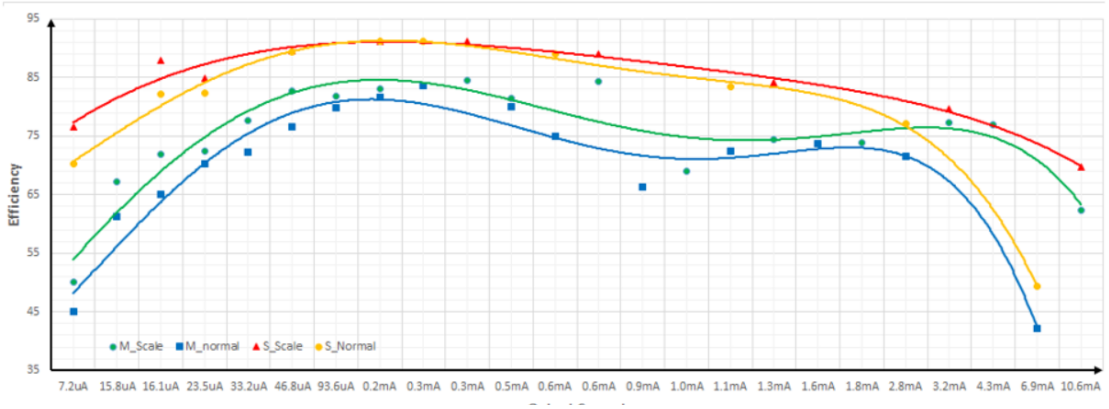


FIGURE 5.1: Efficiency versus output load current for simulated and measured 1/2 topology

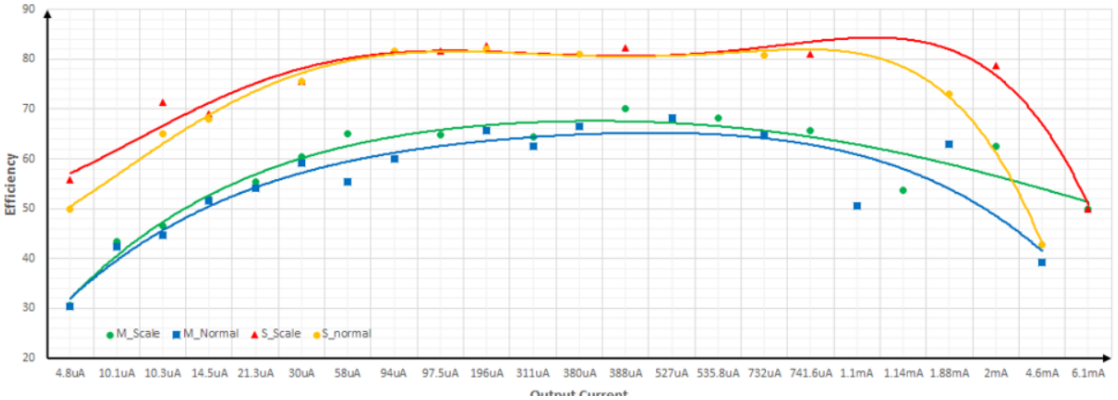


FIGURE 5.2: Efficiency versus output load current for simulated and measured 1/3 topology

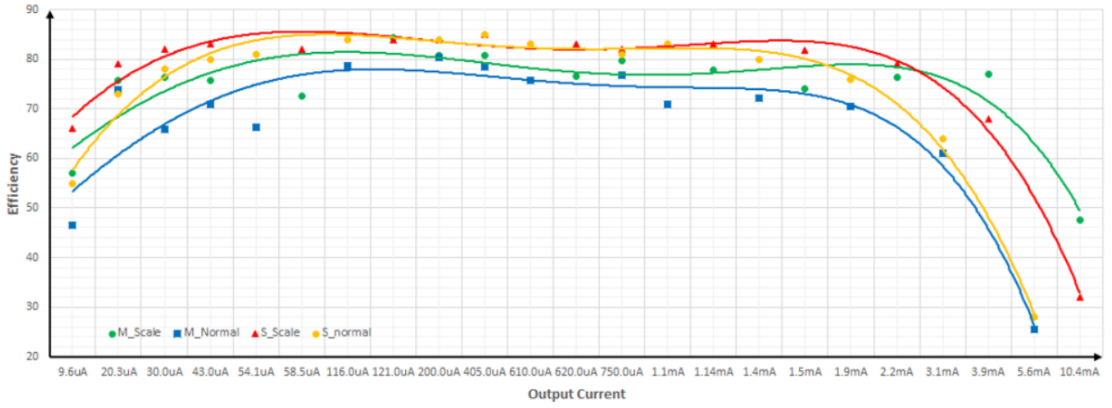


FIGURE 5.3: Efficiency versus output load current for simulated and measured 2/3 topology

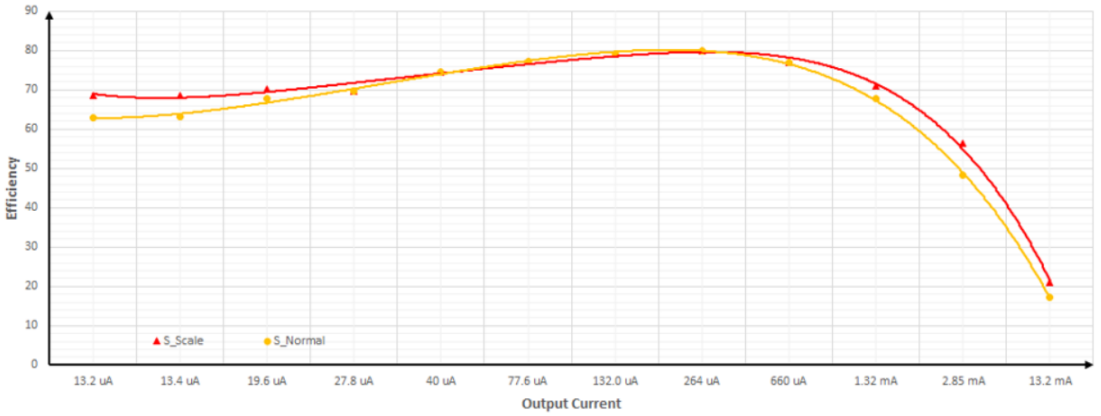


FIGURE 5.4: Efficiency versus output load current for 2/5 topology

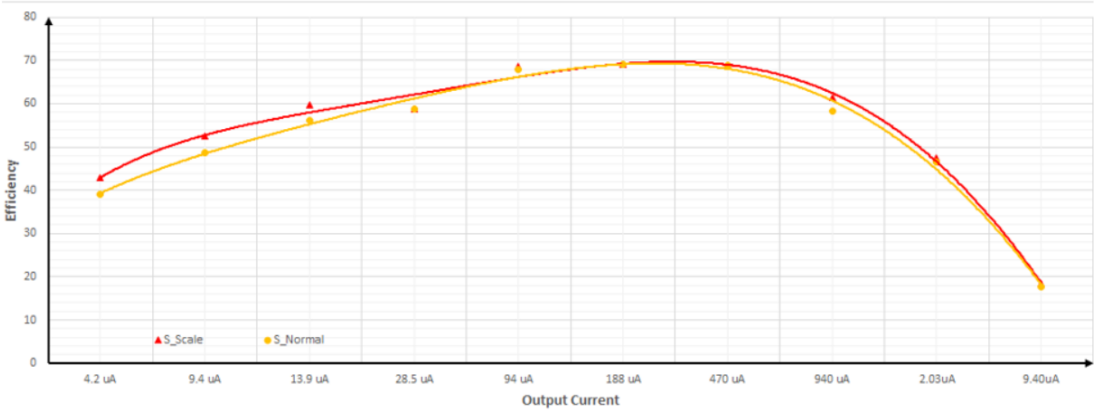


FIGURE 5.5: Efficiency versus output load current for 2/7 topology

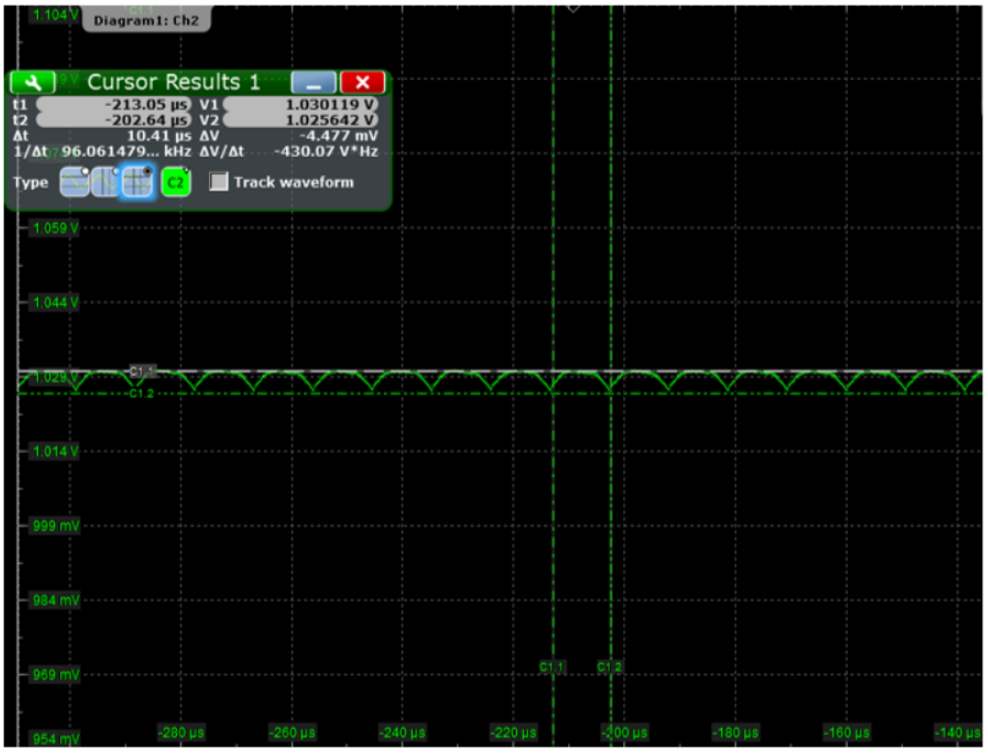


FIGURE 5.6: Output voltage, ripples and switching frequency for 1/3 topology

The efficiency curves show that at low output load currents, the interleavers scaling achieved efficiency gain around ($\sim$ 6%) in both of the simulated and measurements for most of the configurations. This is due to turning off the control circuitry as explained in chapter 3. At high output load currents, switch scaling achieved efficiency gain around 4% in almost all the configurations. This is due to decreasing the switch resistance by increasing the switch size as explained in chapter 3. There is a drop in the efficiency due to parasitic resistances, capacitance and inductance of both of chip and the PCB, shown in Figure 5.7, which is designed to measure the chip.

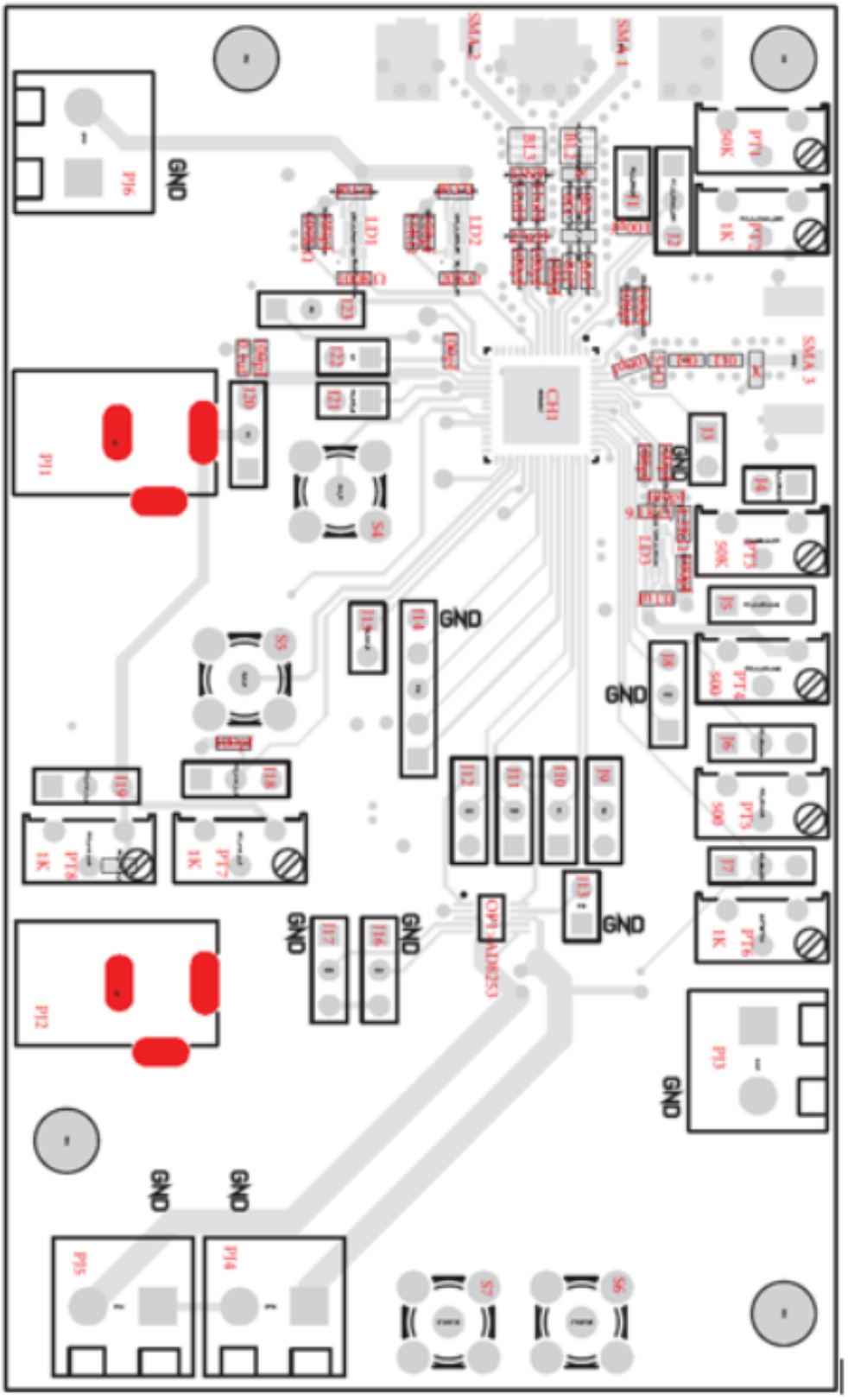


FIGURE 5.7: Output ripples versus output load current for 1/2 topology

Figures below show the switching frequency, output ripples and output ripples variations with respect to output current and Table XX shows the summary for the measured topologies.

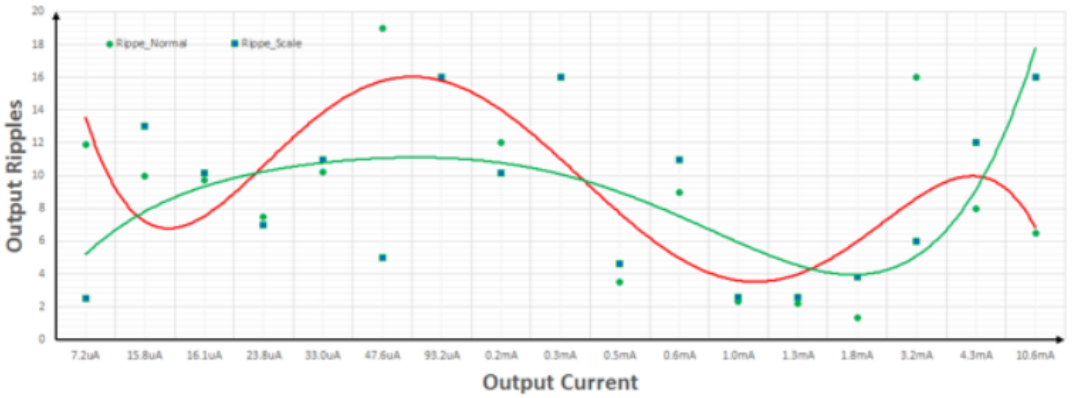


FIGURE 5.8: Output voltage and switching frequency versus output load current for 2/3 topology

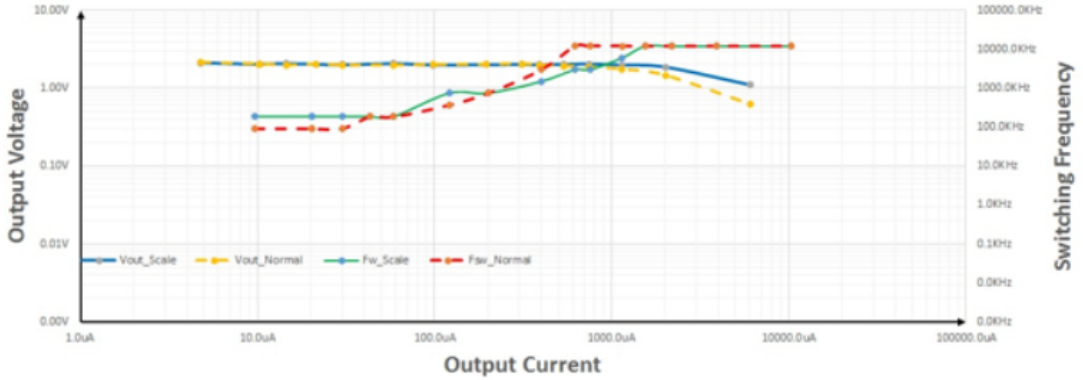


FIGURE 5.9: Ripples versus output load current for 2/3 topology

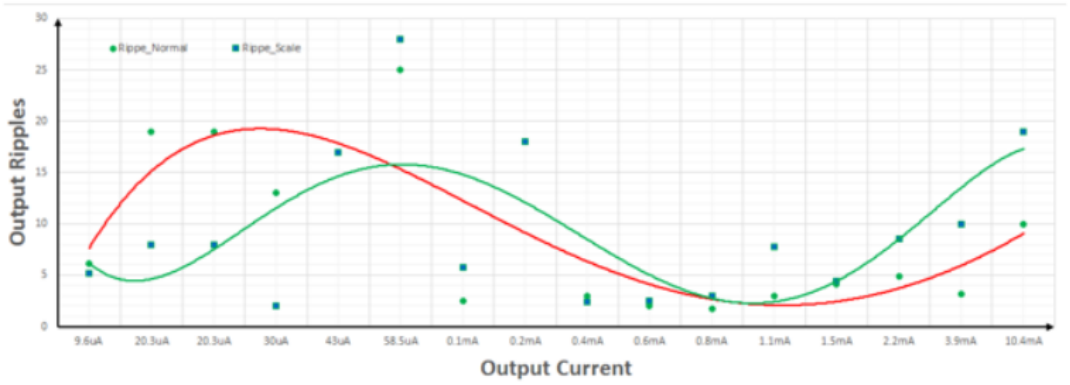


FIGURE 5.10: Printed circuit board used in testing.

TABLE 5.2: Summary of general simulation conditions.

Topology: 1 / 2										
Scaling						Without Scaling				
Rout	**Vout**	**Iout**	**Efficiency**	**Sw. Frequency**	**Ripples**	**Vout**	**Iout**	**Efficiency**	**Sw. Frequency**	**Ripples**
221.7K	1.628	7.22	50.09658	187.5KHz	2.5	1.63	7.2	45.01726	750KHz	11.9
100K	1.6	15.8	67.1983	93.75KHz	13	1.6	15.8	61.28485	93.75KHz	10
98.5 K	1.607	16.1	71.92855	93.75KHz	10.14	1.6	16.1	65.05051	93.75KHz	9.7
67K	1.62	23.84	72.4436	187.5KHz	7	1.61	23.5	70.33835	187.5KHz	7.5
47.6K	1.6	33	77.6699	187.5KHz	11	1.6	33.2	72.18372	187.5KHz	10.2
33K	1.564	47.6	82.78721	187.5KHz	5	1.57	46.8	76.64528	187.5KHz	19
16.5K	1.56	93.2	81.7406	375KHz	16	1.566	93.6	79.887	375KHz	16
10K	1.587	153	83.14022	750KHz	10.14	1.5788	153.4	81.54475	750KHz	12
4.979K	1.567	314	84.42946	1.5MHz	16	1.568	311	83.53427	1.5MHz	16
3.2K	1.57	475.8	81.42642	3MHz	4.6	1.56	473	80	3MHz	3.5
2.6K	1.571	597.2	84.26301	3MHz	11	1.576	593	74.92128	12MHz	9
1.77K	1.61	995.8	69.03932	12MHz	3	1.48	860	66.38502	12MHz	2.3
1.316K	1.6	1305	74.4385	12MHz	2.6	1.512	1138	72.5189	12MHz	2.2
0.88K	1.56	1805	73.87643	12MHz	3.8	1.455	1621.1	73.76241	12MHz	1.3
463	1.5	3150	77.23693	12MHz	6	1.31	2790	71.54686	12MHz	16
324	1.4348	4333.5	76.96705	12MHz	12	1.3	2700	71.5	12MHz	8
100	1.086	10580.9	62.2912	12MHz	16	0.785	6910	42.14724	12MHz	6.5

Topology: 1 / 3										
Scaling						Without Scaling				
Rout	**Vout**	**Iout**	**Efficiency**	**Sw. Frequency**	**Ripples**	**Vout**	**Iout**	**Efficiency**	**Sw. Frequency**	**Ripples**
221.7K	1.07	4.776	30.60438	93.75KHz	1.19	1.07	4.776	30.36435	93.75KHz	1.19
100K	1.029	10.14	43.31283	93.75KHz	10	1.029	10.01	42.40897	93.75KHz	10
98.5 K	1.029	10.3	46.54677	93.75KHz	4.47	1.028	10.3	44.56397	93.75KHz	4.47
67K	0.982	14.5	52.04884	93.75KHz	5.821	0.998	14.631	51.5107	93.75KHz	5.821
47.6K	1.03	21.3	55.40152	187.5KHz	5	1.02	21.15	54.02705	187.5KHz	5
33K	0.99	30	60.40268	187.5KHz	11	0.985	30.1	59.10785	187.5KHz	11
16.5K	0.99	58.14	65.08209	375KHz	16	0.87	58.5	55.47744	375KHz	16
10K	1	97.5	64.79266	750KHz	6.4	0.97	94	60.06588	750KHz	6.4
4.979K	0.985	195.2	65.8353	1.5MHz	3.88	1	197.2	65.73991	1.5MHz	3.88
3.2K	1.026	310.6	64.37891	3MHz	5	1	310	62.62626	3MHz	5
2.6K	1.025	388	70.06695	3MHz	1.4	1	380	66.56157	3MHz	1.4
1.77K	0.965	535.84	68.12722	3MHz	13	0.958	527	68.29897	3MHz	13
1.316K	0.99	741.56	65.74113	6MHz	2	0.99	731.98	64.87267	6MHz	2
0.88K	1.025	1136	53.78788	12MHz	7.16	0.982	1084	50.61543	12MHz	7.16
463	0.9665	2025	62.4623	12MHz	9	0.89	1880	63.03995	12MHz	9
100	0.62	6100	49.8504	12MHz	35	0.505	4600	39.10774	12MHz	35

Topology: 2 / 3										
Scaling						Without Scaling				
Rout	**Vout**	**Iout**	**Efficiency**	**Sw. Frequency**	**Ripples**	**Vout**	**Iout**	**Efficiency**	**Sw. Frequency**	**Ripples**
221.7K	2.12	9.6	57.10438	187.5KHz	5.2	2.13	9.6	46.5892	93.75KHz	6.12
100K	2.035	20.3	67.66667	187.5KHz	8	2.045	20.4	60.48717	93.75KHz	19
98.5K	2.046	20.3	75.81928	187.5KHz	8	2.05	20.3	73.74623	93.75KHz	19
67K	2.07	30	76.27962	187.5KHz	2	1.97	30	65.89312	93.75KHz	13
47.5K	2.034	43	75.72468	187.5KHz	17	2.03	42.7	70.99181	187.5KHz	17
33K	2	58.5	72.50418	187.5KHz	28	1.98	54.1	66.2449	187.5KHz	25
16.9K	2.07	121	84.33333	750KHz	5.8	1.97	116	78.69146	375KHz	2.5
10K	1.999	200	80.76768	750KHz	18	2	199	80.40404	750KHz	18
4.979K	2.01	401	80.87598	1.5MHz	2.4	2.02	405	78.45224	3MHz	3
3.2K	2.02	620	76.66973	3MHz	2.5	2.05	610	75.78788	12MHz	2
2.6K	2.01	754	79.73169	3MHz	3	1.99	748	76.71202	12MHz	1.7
1.77K	2.025	1143	77.93182	6MHz	8	1.92	1086	70.99489	12MHz	3
1.316K	2.05	1543	74.07498	12MHz	4	1.87	1399	72.20097	12MHz	4
0.888K	1.99	2190.2	76.4327	12MHz	8.5	1.75	1927	70.57279	12MHz	5
463	1.867	3890	76.95094	12MHz	10	1.45	3130	61.12458	12MHz	3.2
100	1.1	10360	47.56657	12MHz	19	0.617	5620	25.38704	12MHz	10

Chapter 6

Conclusion

This work presents an all CMOS switched capacitor (SC) DC-DC converter that uses a 4-way interleaver. The converter was implemented in 65nm Bulk CMOS process by UMC. The converter's peak efficiency is 84% at 600uA load current. It can supply output current in the range from 20uA to 4.3mA with efficiency higher that 75%. The converter can be configured into 5 different gain topologies to support various output voltages between 0.94 V and 2.2 V from a 3.3 V input supply. The converter uses a combination of frequency, switch and interleaving scaling techniques to control the output voltage level in order to achieve maximum efficiency. The converter's total area is 0.725 mm^2.

Design	[5]	[9]	[10]	[3]	[4]	**This Work**
Technology	130nm	65nm	45nm	32nm SOI	45nm	65nm
Chip area	$0.25mm^2$	-	$0.16mm^2$	$0.378mm^2$	-	$0.725mm^2$
Capacitor Type	Ferroelectric	-	Gate oxide	Gate oxide	MIM	Gate oxide
Conversion ratio	Step-down 1-1/2-1/3	Step-down 1/2	Step-down 2/3	Step-down 1/3-1/2-2/3	Step-down 1/2	Step-down 1/2 1/3 2/3 2/5 2/7
Output current	20uA-1mA	-	8mA	-	0.1mA-4mA	20uA-5mA
Efficiency	93%	-	69%	79.76%	85%	84.4%
Average output ripples	-	4mV	-	-	2mV	8mV

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