Low Phase Noise Frequency Synthesizer

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by

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in

Electronics and Computer Engineering

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Electronics and Computer Engineering.

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Abstract

The time-efficient design of a complete phase-locked loop (PLL) frequency synthesizer requires good knowledge of non-ideal effects of each sub-block on the system performance. This thesis is an attempt to study the different aspects of the design of RF frequency synthesizers to be used in wireless transceivers. New techniques for duty cycle correction for the reference clock, reference frequency multiplier design and biasing method to regulate the voltage controlled oscillator current were proposed in order to improve the noise performance of the system. Moreover, a new technique for automatic bands calibration for fast PLL locking is also presented. First, the system level behavior of different blocks from the phase noise point of view were analyzed and simulated in MATLAB. Secondly, the transistor level design was implemented in 65nm UMC CMOS process, operating with voltage supplies of 1.2-V, 2.5-V, and 3.3-V. The operational frequency range was from 2GHz to 2.5GHz with a programmable reference frequency from 40MHz to 640MHz. The achieved integrated RMS phase jitter from 10KHz to 10MHz with 40MHz reference frequency and a reference multiplication factor of 16 at 2.16GHz output frequency is 246fs. The output frequency range and performance specifications (power consumption, phase noise, and locking speed) for the proposed design makes it a competitive solution for Cellular and ISM Band applications (GSM, 4G, WiFi, etc.) when compared to current implementations.

Keywords: phase-locked loop, frequency synthesizer, duty cycle correction, frequency multiplier, voltage controlled oscillator, phase noise, spurious tones, fast lock.

Düşük Faz Gürültülü Frekans Sentezleyicisi

Ihsan F. I. Albittar

Öz

Zaman verimli bütün bir faz kilitlemeli döngü frekans sentezleyici PLL tasarımı, sistem performansını etkileyen her bir alt bloğun ideal olmayan etkileri hakkında iyi bir bilgi birikimi gerektirir. Bu tez kablosuz vericilerde kullanılmak üzere tasarlanmış RF frekans sentezleyicileri farklı yönleriyle inceleyen bir çalışmadır. Ayrıca, sistemin gürültü performansını artırmak amacıyla referans saat için görev döngüsü düzelticiler, referans frekans çarpıcı tasarımı ve gerilim kontrollü osilatörlere bias akımı sağlamaya yönelik yeni teknikler önerilmiştir. Öncelikle, farklı blokların sistem seviyesi davranışı, faz gürültüsü kavramı bakış açısıyla MATLAB'da analiz edilmiştir ve simulasyonları tamamlanmıştır. Daha sonra transistor seviyesinde tasarımı UMC 65nm CMOS teknolojisi kullanılarak, 1.2-V, 2.5-V ve 3.3-V besleme gerilimlerine uygun olarak çalışabilen şekilde gerçeklenmiştir. Programlanabilir referans frekans aralığı 40MHz'den 640MHz'e kadar değiştirilerek çalışma frekansı 2GHz ile 2.5GHz aralığında değiştirilebilmektedir. Referans çarpım faktörü olarak 16 kullanılarak, 40MHz referans frekansı ve 2.16GHz çıkış frekansıyla 10KHz ile 10MHz aralığında ulaşılabilen tümleşik RMS faz seğirmesi 246fs'dır.

Anahtar Sözcükler: Faz Kilitlemeli Döngü, frekans sentezleyicisi, görev döngüsü düzelticiler, frekans çarpıcı, gerilim kontrollü osilatör, faz gürültüsü, sahte tonlar, hızlı kilitleme.

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Abbreviations

BER	**B**it **E**rror **R**ate
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CP	**C**harge **P**ump
DAC	**D**igital-to-**A**nalog **C**onverter
DCC	**D**uty **C**ycle **C**orrection
DDS	**D**irect **D**igital **S**ynthesis
DECT	**D**igital **E**nhanced **C**ordless **T**elecommunications
DLL	**D**elay-**L**ocked **L**oop
FS	**F**requency **S**ynthesizer
IF	**I**ntermediate **F**requency
LNA	**L**ow **N**oise **A**mplifier
LO	**L**ocal **O**scillator
LPF	**L**ow **P**ass **F**ilter
PD	**P**hase **D**etecotr
PFD	**P**hase **F**requency **D**etecotr
PLL	**P**hase-**L**ocked **L**oop
PN	**P**hase **N**oise
ppm	**p**arts **p**er **m**illion
PVT	**P**rocess, **V**oltage, and **T**empreture
PWM	**P**ulse **W**idth **M**odulation
RF	**R**adio **F**requency
ROM	**R**ead-**O**nly **M**emory
ΣΔ/SD	**S**igma **D**elta
SNR	**S**ignal **N**oise **R**atio
SOC	**S**ystem **O**n **C**hip
VCO	**V**oltage-**C**ontrolled **O**sillator
XO	**C**rystal **O**scillator

Chapter 1

Introduction

1.1 Motivation

The continuous growth in the wireless communication market has generated new challenges and problems. Designing compact portable devices with low cost and long battery life have been the goal in the last decade. Moreover, the bandwidth need for individual users has increased dramatically, driven by the desire to accessing ubiquitous applications. Researchers from all sub-fields of communication systems from system design to integrated circuits implementation have focused their efforts to attain the goal of widespreading these applications.

Numerous applications of wireless communication devices such as cellular phones, global positioning systems, wireless local area networks and IoT devices use various standards to control the communication link of sending or receiving either voice or data over the air. The explosive demand of emerging new applications create new standards which require wider bandwidth and better noise performance for higher data rates. This has created an immense engineering task for Radio Frequency (RF) and system designers. As a result of the competition among manufacturers and the increasingly challenging requirements, wireless system design research has been at the center stage for a long time.

Frequency synthesizers are one of the essential building blocks in almost any System On Chip (SOC); They generate clocks for digital computational logic, synchronize communications between different systems, and synthesize RF carrier signals for wireless communication systems. Frequency synthesis has always been a fundamental major challenge in any transceiver because of various noise and frequency stability requirements. Although this seems like a simple task, generating a high quality, accurate and

spectrally pure waveform that meet the system requirements is not a trivial task. Multi-band transceivers with higher complexity have emerged with the emerging of new wireless standards for 4G, and in the near future 5G, which makes it even tougher task to design synthesizers suitable for multi standard solutions.

This thesis is an attempt to study the different aspects of the design of an RF frequency synthesizer (FS) for use in wireless transceivers. It gives details starting from the system level design to transistor level implementation of the building blocks and system integration/verification. The design of frequency synthesizer is prolific in many aspects since it includes designing high-speed analog RF blocks (voltage-vontrolled oscillator), high-speed digital blocks (programmable frequency divider), low speed analog (charge pump and filter) and low speed digital (phase frequency detector) circuits. Designing a PLL FS requires good knowledge of the impact of block implementation non-idealities on the overall system performance.

1.2 The main goal of the research

The main goal of the research is to design a low phase noise frequency synthesizer working in the frequency range from 2GHz-2.5GHz that will be implemented in 65nm UMC CMOS process. The phase noise is the most critical performance metric for any frequency synthesizer. Therefore, the proposed system in this research as illustrated in Fig. 1.1 takes extra steps compared to a normal frequency synthesizer to enhance the phase noise performance. A frequency multiplier and a duty cycle correction loop were implemented to improve the overall phase noise. Furthermore, a new CMOS VCO biasing technique is used.

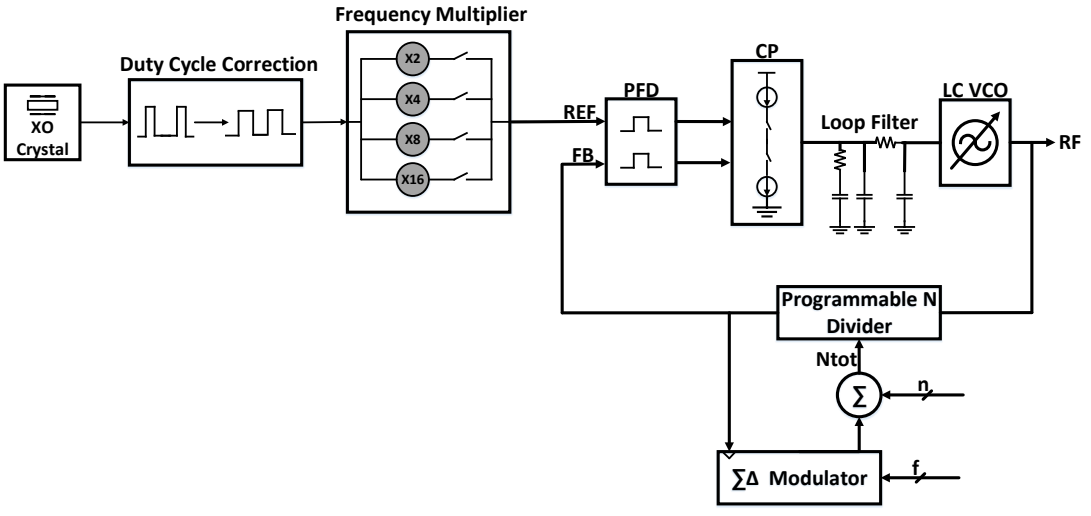


FIGURE 1.1: The proposed top level frequency synthesizer system

1.3 Thesis Organization

Chapter 2 defines the functionality and performance specifications for frequency synthesizers. Furthermore, the impact of a synthesizer performance on a wireless transceiver is briefly highlighted.

Chapter 3 focuses on the system level design of the charge pump PLL. The chapter start by modeling the PLL system, then a phase noise model for each block and its contribution to the output is given. The outcome of this chapter is clear performance specifications of the synthesizer building blocks.

In Chapter 4, a novel technique for duty cycle correction is presented and analysed. The chapter starts by highlighting the importance of the duty cycle correction, then details the design of the duty cycle correction method. It defines a method to show the functionality with and without supply noise model.

In Chapter 5, a novel technique for a frequency multiplier which has the ability to multiply the reference frequency up to 16 times is presented. It shows the non-idealities of the proposed technique alongside the simulation results.

In Chapter 6, a low phase noise VCO with a feedback loop for regulating the bias current is proposed. Furthermore, a new technique for automatic band calibration for fast PLL locking is presented. The chapter explains the design steps, methodology and the analysis.

Chapter 7 summarizes the overall system verification and concludes the thesis.

Chapter 2

RF Frequency Synthesizer

2.1 Introduction

This chapter introduces a high-level description of frequency synthesizers and their specifications. The main purpose of frequency synthesizers in RF transceiver is briefly explained with special attention to the impact of synthesizer non-idealities on the overall performance. Some equations are developed to calculate the synthesizer phase noise and spur levels. Finally, different frequency synthesizer types are explained with the advantages and limitations of each.

2.2 Frequency Synthesizer

2.2.1 What is Frequency Synthesizer ?

A frequency synthesizer is basically a source that is capable of generating a precise set of programmable frequencies from a fixed reference frequency. Simply put, it is a frequency multiplier. The spectrum purity of frequency synthesizer (phase noise and spur levels) is the most important performance metric that can affect the performance of RF transceiver.

2.2.2 Frequency Synthesizer Specifications

It is very important to understand the specifications in order to meet the desired requirements in a specific application. The most important performance parameters for synthesizers are listed below.

1. **Range** The extent of frequencies that the synthesizer can generate.

2. **Resolution** The least difference between two successive frequencies that the synthesizer can generate.

3. **Spectral purity** Synthesizer are ideally expected to generate a pure sinusoidal waveform which is represented by a Dirac delta function in the frequency domain. Practically, synthesizer output contains power at frequencies offset from the desired frequency. This non-ideality can be seen in the frequency domain as noise skirts commonly known as phase noise and spurious tones. Phase noise arises from the circuit noise sources in the synthesizer such as thermal noise, shot noise and 1/f flicker noise. On the other hand, spurs are deterministic components that are a result of the architecture and implementation of the synthesizer.

   A **spur** is specified by its frequency and magnitude relative to that of the carrier and is measured in dBc.

   Phase noise is measured as the total noise power in a 1-Hz bandwidth at a frequency offset f_m from the carrier frequency f_{LO} divided by the total power of the carrier. Phase noise is expressed in dBc/Hz where the "c" indicates that the noise power is normalized to the carrier power. Fig. 2.1 shows the practical power spectrum from a frequency synthesizer. **Phase jitter** is the time domain representation for phase noise, therefore it is equal to the integrated phase noise over a specific band.

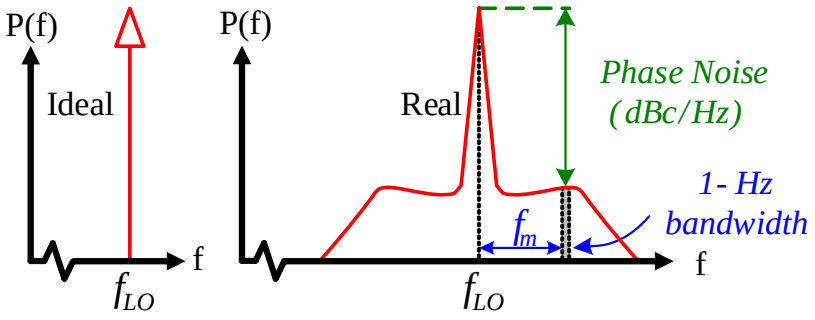


FIGURE 2.1: Oscillator power spectrum

4. **Frequency stability** This is determined by the stability of the output frequency of the synthesizer across temperature. The accuracy of the reference frequency, which usually comes from a crystal oscillator has a major impact on the frequency stability. It is worth mentioning that a crystal oscillator with a wide temperature range and high stability is expensive. The stability is measured in parts per million (ppm).

5. **Lock time** This is the time required for the synthesizer to jump from one specific frequency to another within a given frequency tolerance in response to a user input. The jump size is normally determined by the maximum jump the frequency synthesizer will have to accomplish and settle when operating in its allocated frequency band.

6. **Others** Power consumption, area and supply voltage are the other specifications for a synthesizer.

2.2.3 Frequency Synthesizer in RF Transceiver

There are several architectures for implementing both the receiver and the transmitter sides in an RF transceiver system. All of these need a tunable local oscillator (LO) which is generated by a frequency synthesizer. The main role of having a frequency synthesizer is to translate signals to different frequency bands for transmission and/or reception. For instance, the necessity of a local oscillator in a conventional super-heterodyne receiver is to down-convert the incoming signal to an intermediate frequency (IF). Since there are a group of channels that need to be received, the local oscillator will tune its frequency in order to distinguish the channels such that after down-conversion the received signal is at the same IF. Other architectures might have different requirements and more than one synthesizer such as the double IF architecture [1].

The frequency generated must be defined with very high accuracy ranging from 0.1 ppm for GSM to 25 ppm for DECT [2]. Similarly, the spectral purity of the frequency synthesizer (phase noise and spurs) will have a great impact on the overall performance of an RF transceiver. Generally, the selectivity and sensitivity are two key performance factors of a radio system.

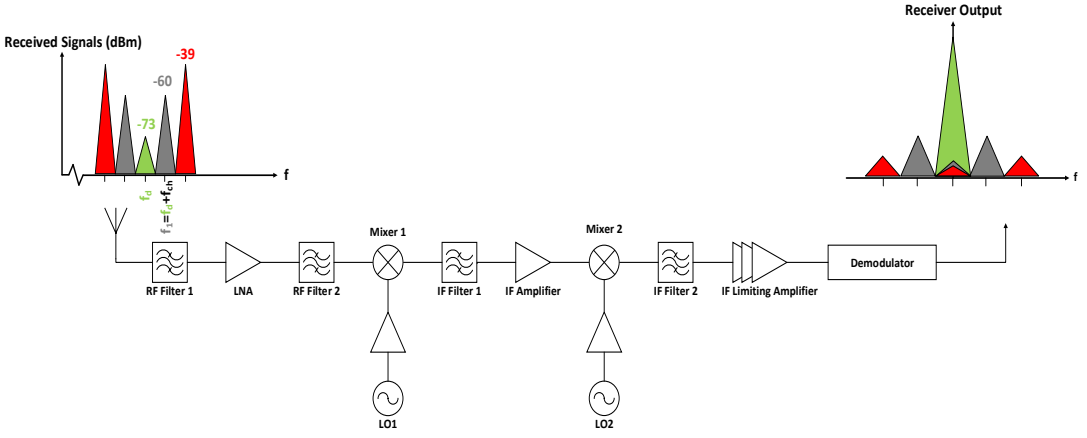


FIGURE 2.2: Conventional super-heterodyne dual-conversion receiver

The selectivity is defined as the ability to receive a specific channel in the presence of neighboring interferes. The existence of these interferers maybe due to other systems in the same standard using the same frequencies or even systems with different standards that use similar frequencies. In an ideal case, the system receives a strong channel without interferers. Unfortunately, this will not always be the case and the system can face circumstances where the desired channel is much weaker than the interferers. The ability of the system to extract the desired signal and still produce an output with a given signal-to-noise defines the selectivity of the receiver. A common problem is called the "near-far" [3] issue, which is illustrated in Fig. 2.2. The receiver receives signals from various neighboring channels with different power levels at f_o. The desired signal does not necessarily have the highest power. Actually, this case is considered practical because it is possible to have a nearby transmitter of neighboring channel while the desired signal's transmitter is far away. In a conventional super-heterdoyne receiver, the desired signal is translated to (IF) and then to base-band frequency. RF filter1 is responsible to filter away out of band as well as neighboring channels. Then, an appropriate (LO) is chosen for the translation process. However, RF filter1 is not infinitely sharp and selective, hence the output of the low noise amplifier (LNA) and RF filter2 is mixed with the first local oscillator (LO1). Thus, some of the neighboring channels power will be frequency translated by the (LO1) during the mixing action. Moreover, the non-linearity that exist in the blocks in the receiver chain can cause distortion and result in some of the energy in the neighboring channels to generate distortion on top of the desired signal. If the signals involved in the distortion products are too strong, the resulting interference will degrade the reception of the desired signal. Hence, each block in the RF receiver chain has an impact on the selectivity of the system and the LO, in turn the frequency synthesizer, has its share of this impact.

The sensitivity of a receiver is defined as the smallest RF signal that can be received at the input with a given signal-to-noise ratio, or bit error rate (BER) for digital communication systems [3]. The ability of a receiver to recover signals with a wide dynamic range is important since this directly affects the maximum range of a transmission link as well as its capability to cope with variations in the communication channel. Any noise sources in the system limits the performance.

2.2.4 Phase noise and Spurs level impact

The spectral purity of the LO has a great impact on the system performance when translating the desired signal either by up-conversion or down-conversion. Practically, the phase noise and spurs of an LO in an RF receiver can cause some of the neighboring channel powers to mix on top of the desired signal. Hence, the receiver is blocked due

to high power neighboring channels and suffers when extracting the desired signal. As a corollary, the designer should pay attention to the radio standard requirements which will determine the phase noise and spur levels of the frequency synthesizer. Fig. 2.3 explains the mechanism of this phenomenon [3].

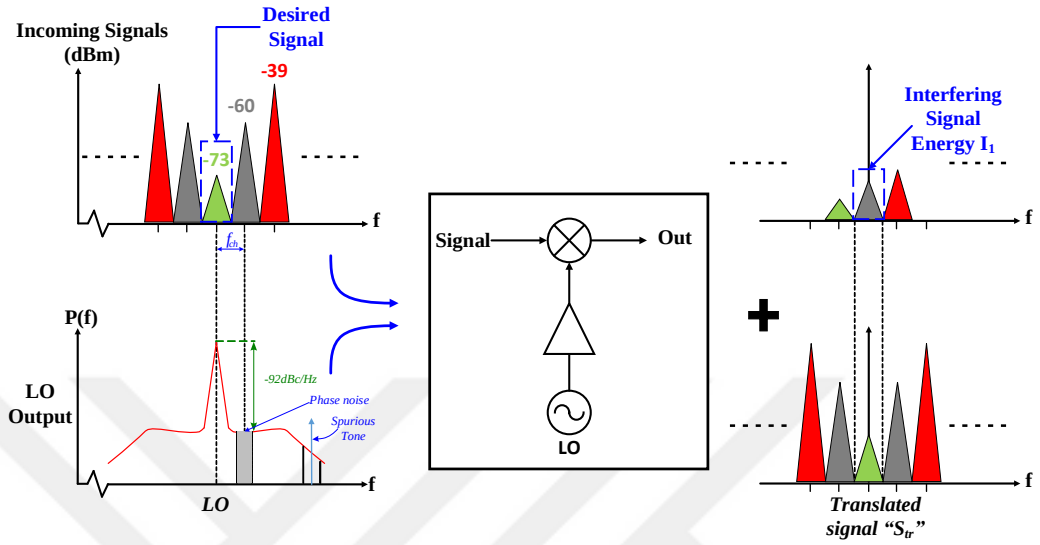


FIGURE 2.3: An example of local oscillator phase noise (the strength profile of an incoming signal for DECT cordless telephone standard)

Mathematically, the output spectrum of the mixer is the convolution of the LO and the incoming signals spectrum. For simplicity, the effect of phase noise will be broken up into smaller linear equations and summed for the results. If the carrier power is P_c and the desired signal power is S_d, both in dBm, mixing them together with a conversion gain G_c, the frequency translated signal S_{tr} will have a power in dBm given by

$$S_{tr} = P_c + S_d + G_c. \tag{2.1}$$

Since LO signal (f_{LO}) also down-converts the rest of the neighboring channels, their effect should be highlighted. According to their impact, we will divide them into harmless and harmful parts. Mixing these channels with LO carrier power is harmless, because it will be filtered out and do not directly affect the selectivity. The harmful part is due to the output LO power spectrum noise (spurious tones and phase noise). If we assume a signal power at i channels away from the desired signal is S_i in dBm, then at the same IF frequency at the output of the mixer there will exist signal power I_i due to the mixing of LO power at an offset $\Delta f = i.f_{ch}$ with S_i. Hence, the total output power is the summation of all these interferer signals I_i and the desired signal S_d. Spurious tone might be treated as a single frequency with power $P_c + X_{spur}$ where X_{spur} in dBc indicating the strength of the spur with respect to the carrier. Assuming the mixer conversion gain

is the same at this frequency then I_i is given by

$$I_i = P_c + X_{spur} + S_i + G_c. \tag{2.2}$$

If we consider the interferes as noise, so the SNR will be the difference in dB between S_{tr} and I_i which is given by

$$SNR = S_{tr} - I_i = S_d - X_{spur} - S_i \tag{2.3}$$

$$X_{spur} \leqslant S_d - S_i - SNR. \tag{2.4}$$

For a typical SNR = 15dB, $S_d = -73dBm$, $i = 2$, $S_2 = -39dBm$ then $X_{spur} \leqslant -49dBc$. This result shows the minimum requirement of spurious tone at $\Delta f = 2f_{ch}$ should be smaller than $-49dBc$.

Although, phase noise and spurious tone have the same impact of mixing the neighboring channels on top of the desired signal, different methods are used to find their impact and determine the interferer power I_i at the limit performance. In the first neighboring channel, the phase noise power will be calculated by integrating the phase noise power density $\mathcal{L}(f)$ from f_c+$0.5f_{ch}$ to f_c+$1.5f_{ch}$. Assuming a uniform distribution channel, the integration can be approximated by multiplying the phase noise at f_c+f_{ch} by the integration bandwidth f_{ch}. Then the interferer I_i will be given by

$$I_i = P_c + S_i + G_c + \mathcal{L}(i.f_{ch}) + 10log(f_{ch}) \tag{2.5}$$

$$SNR = S_{tr} - I_i = S_d - \mathcal{L}(i.f_{ch}) - 10log(f_{ch}) - S_i \tag{2.6}$$

$$\mathcal{L}(i.f_{ch}) \leqslant S_d - S_i - SNR - 10log(f_{ch}). \tag{2.7}$$

For SNR = 15dB, $S_d = -73dBm$, $i = 1$, $S_1 = -60dBm$, and $f_{ch} = 1.728MHz$, then $\mathcal{L}(fch) \leqslant -90.4dBc/Hz$.

For each specific radio standard, the noise blocking requirements specify the maximum allowed signal power in the neighboring channels which are used to calculate the tolerable spurs and phase noise. Usually, the standard indicates the maximum allowed phase noise and spur level at each neighboring channel for the minimum required performance.

2.3 Frequency Synthesizer Architectures

A brief discussion about various frequency synthesizer architectures available for use in practical systems is given in this section. Furthermore, we highlight the drawbacks of each approach especially emphasizing noise-bandwidth trade-off and frequency resolution. Functionality of some of the architectures will also be explained.

2.3.1 Direct Digital Synthesis

Fig. 2.4 illustrates the basic block diagram of a Direct Digital Frequency Synthesizer (DDS). Simply, the signal is first generated in the digital domain and then by the use of a DAC and a LPF, it is reconstructed in the analog domain. According to the frequency setting word, the phase accumulator output increases linearly at every clock cycle until the accumulator maximum count is reached, then the accumulator starts from zero again. The look-up table stored in the ROM converts the digital phase to a digital amplitude. A Digital-to-Analog Converter (DAC) converts the digital amplitude values into an analog signal. The output spectral purity is then improved by passing the DAC output through the LPF.

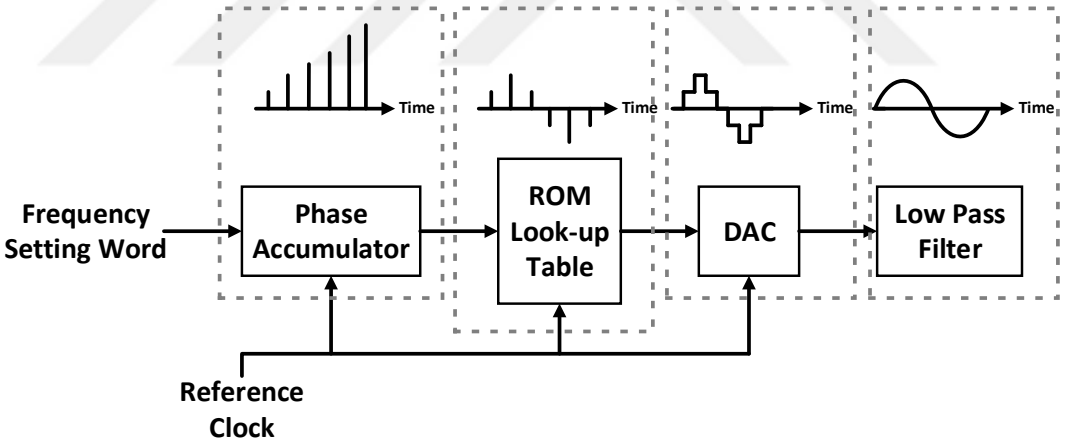


FIGURE 2.4: DDS block diagram

The frequency of the sawtooth pattern at the phase accumulator output determines the DDS output frequency that is f_{out}. The f_{out} is given by

$$f_{out} = f_{clk}\frac{L_{fsw}}{L_{acm}} \tag{2.8}$$

where L_{fsw} is the frequency setting word length, L_{acm} is the accumulator length, and f_{clk} represents the reference clock frequency.

The reference clock frequency divided by the accumulator length (i.e. $\frac{f_{clk}}{L_{acm}}$) in equation (2.8) is defined as the minimum frequency increment. In order to increase the output frequency (f_{out}) without changing the reference clock (f_{clk}), some addresses of the ROM can be skipped. Furthermore, the aforementioned technique is also used to achieve fractional output frequencies, which is one of the many advantages that DDS technique brings.

Other advantages of DDS include fast switching (output frequency generation in few clock cycles) and compact integration (no off chip components). The fast switching capability of DDS is prevalent in extreme agile applications such as frequency-hopped spread-spectrum systems. Also, in digital domain L_{fsw} can be used to accomplish the frequency and phase modulation.

On the contrary, the main disadvantage is that the spectral purity of the DDS output is limited by the DAC's resolution and speed. The finite resolution during quantization process gives rise to inexact representation of the sinusoidal wave and hence results in spurious outputs. However, the output can be made free of spurious tones, if the output frequency is a harmonic of the reference clock frequency. Another disadvantage is that this architecture suffers from high power consumption in high frequency applications.

2.3.2 Integer-N Phase Locked Loop

Fig. 2.5 illustrates the integer-N phase-locked loop, in which the output frequency F_{out} is determined by

$$F_{out} = NF_{ref} \tag{2.9}$$

where the division ratio is represented by N and F_{ref} is the reference clock frequency. From the stability point of view, the PLL closed loop bandwidth should be chosen to be at least ten times lower than the reference clock frequency [4]. Since F_{out} is an integer multiple of F_{ref}, fine frequency resolution requires a low F_{ref}, which results in low PLL bandwidth. Here, low PLL bandwidth signifies slower dynamic response. As a result of the trade-off between resolution and bandwidth (dynamic response), the use of the integer-N phase locked loop has limited applications in high performance RF systems.

2.3.3 Fractional-N Phase Locked Loop

The fractional-N synthesis has advantages in the resolution-bandwidth trade-off. In order to understand the need of the fractional synthesis and the problem of the integer synthesis, we will start by showing their differences. The forced limited bandwidth of

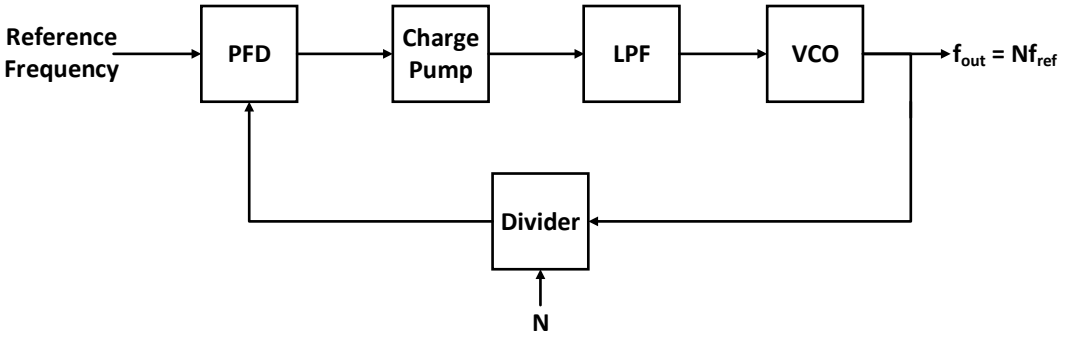


FIGURE 2.5: Phase Locked Loop Integer-N block diagram

the integer PLL for two main reasons. Firstly, integer-N PLL suffers from high reference spurs, therefore a sufficient attenuation is required to attenuate these spurious tones and this can be achieved by decreasing the bandwidth. Secondly, if we substitute N to be unity in equation (2.9), we can conclude that the minimum output frequency is f_{ref} and this minimum value represents the minimum output frequency step, which is the channel spacing. According to the recent trends to save the bandwidth and have an efficient transmission and reception, the channel spacing becomes very narrow. Therefore, low PLL bandwidth is required. For low channel bandwidth systems, to get high output frequencies, the division ratio N increases dramatically. As N gets larger, amplification of the reference clock and PFD/CP noise at offset frequencies around the carrier gets larger, as will be shown later. Moreover, the VCO phase noise is considered as one of the most important contributor in the overall phase noise performance and the small bandwidth limits the rejection of this noise. Consequently, VCO phase noise becomes the limit of the synthesizer noise performance at frequencies higher than the PLL bandwidth.

In fractional-N synthesizers, the VCO frequency is divided by a fractional number in order to keep the reference frequency high. This implies that changing to an adjacent channel will not require a change in the integer part of N, it will be enough to change the fraction part in N. Since the division ratio can be a rational number, thus f_{ref} does not need to be low anymore.

Several approaches have been proposed to implement the aforementioned concept as suggested by [5]-[7]. All the techniques used in frequency synthesizer depend on the fact that the frequency is divided on average by a rational number. Pulse swallowing technique is the most common approach of implementing a fractional divider. Basically, the digital frequency divider is a counter which counts the number of edges received at its input and changes its state once it reaches its maximum or minimum count.

The pulse swallower circuit as shown in Fig. 2.6 is introduced before the integer divider M. This type of circuit swallows a pulse at a rate of f_{sw}. Therefore, the output frequency

on average f_{out} of the frequency synthesizer at locked condition is given by

$$f_{out} = M f_{ref} + f_{sw}. \tag{2.10}$$

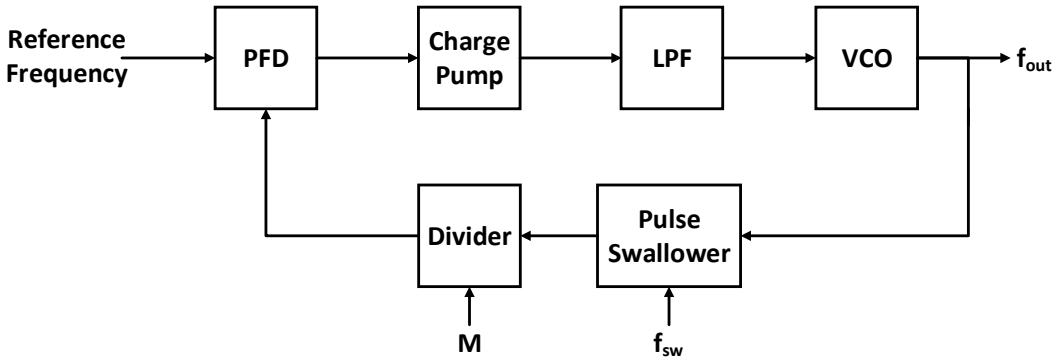


FIGURE 2.6: Simple fractional-N synthesizer using a divider and pulse swallower

Equation (2.10) shows that a rational division is obtained by ensuring f_{sw} is a non-integer multiple of the reference frequency f_{ref}. Another approach would be to let f_{sw} equal to f_{ref} but limit the operation for a certain percentage of the time. For instance, suppose a frequency synthesizer, which has a pulse swallower is disabled 80% of the time and the remaining 20% is enabled and swallowing at a rate of f_{ref}. The frequency divider, M, which acts as a counter will not see the swallowed pulse. Therefore, the division ratio toggles between M when the pulse swallower is disabled and M+1 when it is enabled. As a result of the previous example, the average division ratio N is given as

$$N = (M+1) \cdot (20\%) + (M) \cdot (80\%) = M + 0.2. \tag{2.11}$$

Similarly, the dual-mode divider as shown in Fig. 2.7 divides f_{ref} by N, when the carry-out signal from the accumulator is LOW. However, if the carry-out signal is HIGH, the division ratio would be N+1. The dithering modulator dynamically varies the division ratio N by an accumulator, which accumulates its output every reference cycle. As a result of this accumulation, a fractional division value between N and N+1 is obtained.

If the accumulator length is L_{acm}, then the accumulator overflows by F times every L_{acm} clock cycles. That means the divider divides the VCO output by (N+1).F times for every L_{acm} cycles and then by N for the rest of the VCO cycles. Therefore, the average division ratio N_{avg} is formulated as

$$N_{avg} = N + \frac{F}{L_{acm}}. \tag{2.12}$$

The process of alternating the division ratio between two values periodically in order to get a specific rational value introduces quantization noise into the system. Fractional spurious tones also appear at the output spectrum of the frequency synthesizer at a fractional offset frequency. Since they are closer to the carrier than the reference spurs, they are filtered less and show up higher at the output. However, the alternating process is deterministic, hence it is possible to compensate for the quantization error (instantaneous phase error as shown in Fig. 2.7) by introducing an opposite behaviour. The compensation scheme is known as Automatic Phase Interpolation [6],[8].

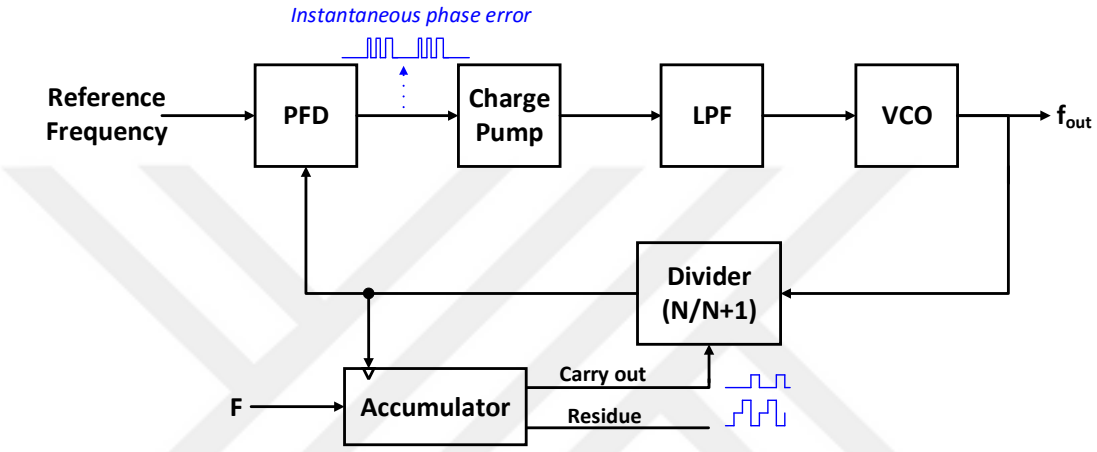


FIGURE 2.7: Classical fractional-N synthesizer

The most common method for fractional-N synthesizer is to use the Sigma-Delta ($\Sigma\Delta$) Modulation technique [9]. The main difference between this technique and the aforementioned techniques is the randomization of the divider control bits in order to avoid the periodicity in the division ratio. Basically, the accumulator which is used in the previous techniques can be seen as a first order Sigma-Delta modulator. However, the use of higher-order Sigma-Delta modulators offer advantages in attenuating the quantization noise due to higher-order noise shaping of the modulator, which has high-pass characteristics. Hence, the noise can be shaped and pushed outside the PLL loop bandwidth. This method can achieve very fine frequency resolution but it is limited by the size of the digital address.

2.3.4 Delay Locked Loop Synthesis

A Delay Locked Loop (DLL) is a recent approach to frequency synthesis which has been proposed in [10]. Instead of using a voltage controlled oscillator in PLL, voltage controlled delay line is utilized in DLL. The delay line output of DLL is a delayed version of the input by one reference period T_{ref}. Therefore, a voltage controlled delay line consisting

of N delay stages will have a delay of T_{ref}/N at each stage. The output frequency of the phase combiner is given by $N \cdot f_{ref}$. The complete block diagram of the DLL synthesizer is shown in Fig. 2.8.

The distinct advantage of this approach is compact area as there is no need for high Q tanks. However, the DLL approach suffers from generating a fine resolution output frequencies because it is hard to implement a very fine resolution delay line.

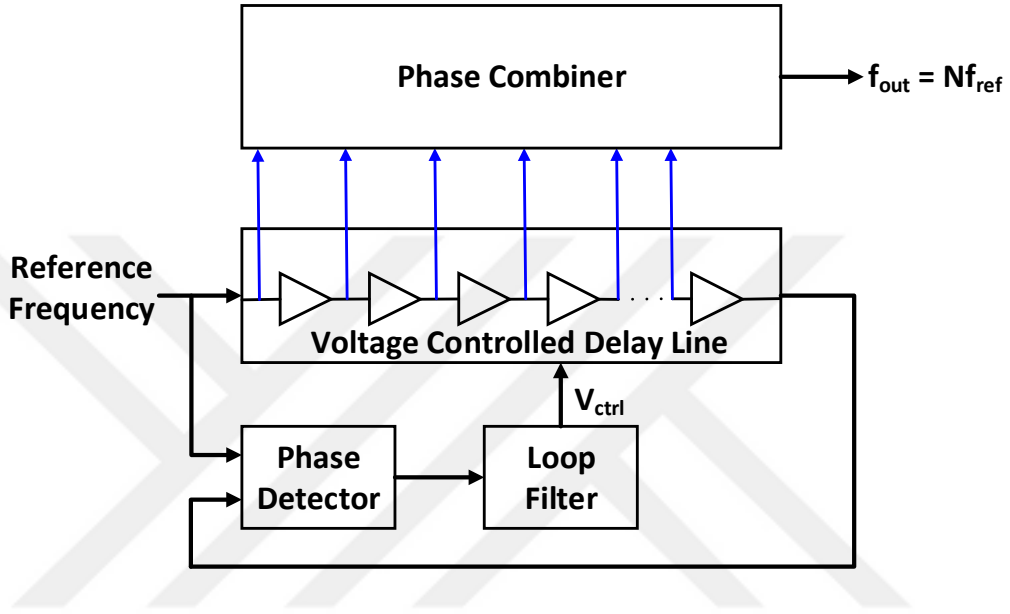


FIGURE 2.8: DLL block diagram

2.4 Summary

This chapter started by defining the performance specifications of frequency synthesizers. The main role of frequency synthesizers in RF transceiver is then briefly described with emphasizing the non-ideal effects of synthesizer on the overall performance. The chapter ends with a description of different types of frequency synthesizer implementations. The system design of charge pump PLL frequency synthesizer with detailed analysis is introduced in the following chapter.

Chapter 3

Charge Pump PLL Frequency Synthesizer

3.1 Introduction

A high-level description of frequency synthesizers was introduced in the previous chapter in terms of their use, advantages, limitations and different frequency synthesizer types. This chapter will go a step further and give details on the analysis of PLLs, especially charge pump PLL using a linearized model.

The idea of any PLL is based on using a negative feedback loop to synthesize different frequencies from a reference input. Simply, it depends on phase locking of a reference clock and a feedback clock to get a precise output frequencies. PLLs are large-signal non-linear systems yet under certain conditions, such as lock or close to lock states, might be linearized by considering the phase of the signals as the state variables. As a result, this allows the analysis to be linear and therefore easier to design a PLL.

3.2 PLL linear model

A PLL linear model is built by introducing phase signals at the input and output of the system. This requires adequate linear models for each of the building blocks. Once a linear model of the PLL is developed, one may use it to study the loop stability, open and closed loop response, phase noise, and settling time. It is worth mentioning again that these models are strictly valid only when the loop is in lock or close to lock. Throughout the thesis, several design tools such as Verilog, MATLAB, besides Cadence

Spectre design capture environment are utilized to study the system. They will be used for modeling and simulating the PLL FS at different levels of abstraction.

This section starts by studying the high-level abstraction for each block separately in order to develop a linear system model in the frequency domain, then extracting the main performance parameters, which will be shown at the end of this chapter.

3.2.1 Simplified PLL system

A simplified block diagram of a PLL is composed of a Phase Detector (PD), which compares the phases between a reference frequency and the feedback frequency in order to generate an error signal to modify a control voltage through a law pass filter to control the Voltage-Controlled Oscillator (VCO), which in turn produces the output frequency. Ideally, this process continues until the PD inputs aligned. Fig. 3.1 illustrates the simplified top level PLL. The basic functionality of the phase detector is to produce an

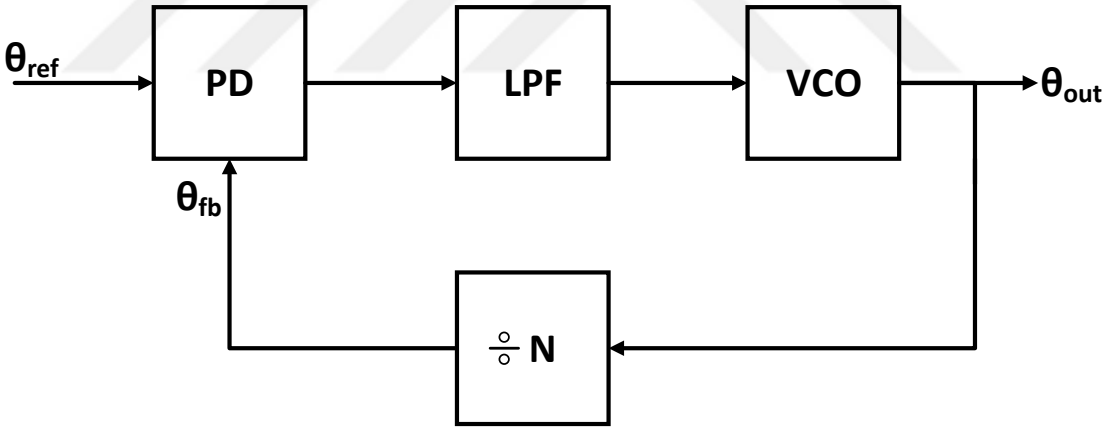


FIGURE 3.1: Simplified PLL Block Diagram

output voltage which is proportional to the phase difference θ_e of the signals applied to its inputs. However, the output of the PD is not a constant voltage and the phase error is proportional to the average value of the PD output. Consequently, a low pass filter of transfer function of F(s) is required to extract the desired signal (average voltage only) and supply it to the control pin of the VCO. Finally, The phase detector is a continuous-time circuit with a transfer function as shown in Fig. 3.2(a), and the equivalent model is shown in Fig. 3.2(b). Equation (3.1) shows the linear range of an ideal PD with

proportionality constant K_{phase}. It is important to indicate that K_{phase} depends mainly on the type of PD, so will the transfer function, as it will be discussed later.

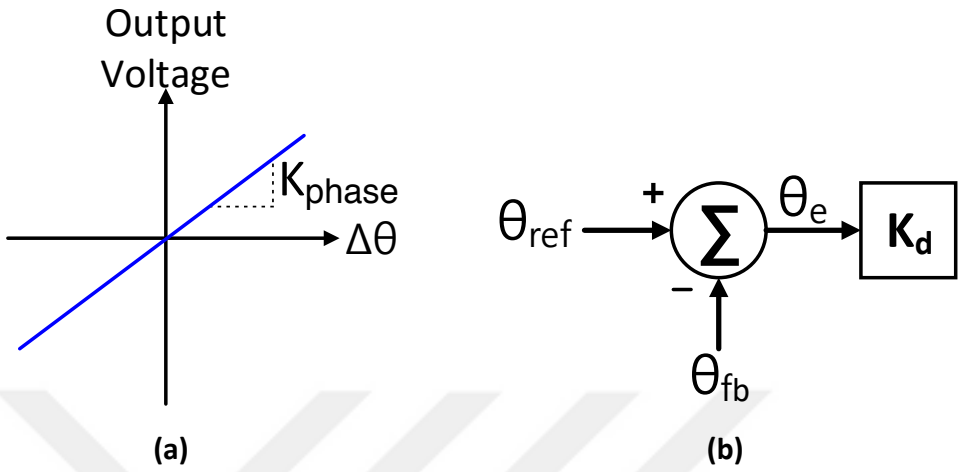


FIGURE 3.2: Phase Detector (a) transfer function and (b) linear model

$$V_{ctrl} = K_{phase}(\theta_{ref} - \theta_{fb}). \tag{3.1}$$

From a behavioral point of view, a VCO is a device which produces a sinusoidal (or square) waveform of frequency proportional to the control voltage V_{ctrl}. Mathematically, it is expressed by equation (3.2), and Fig. 3.3 illustrates the transfer function as well as the VCO linear model.

$$f_{out} = f_o + K_o V_{ctrl} \tag{3.2}$$

where f_o is the free running VCO frequency (at $V_{ctrl} = 0$) and K_o is the proportionality constant with units of [MHz/V]. As it was previously stated that a linear model will be built by using the phase of the signals, it would be helpful to relate V_{ctrl} to the output phase of the VCO. The angular frequency (ω) and the phase (θ) are related as

$$\omega = \frac{d\theta}{dt}. \tag{3.3}$$

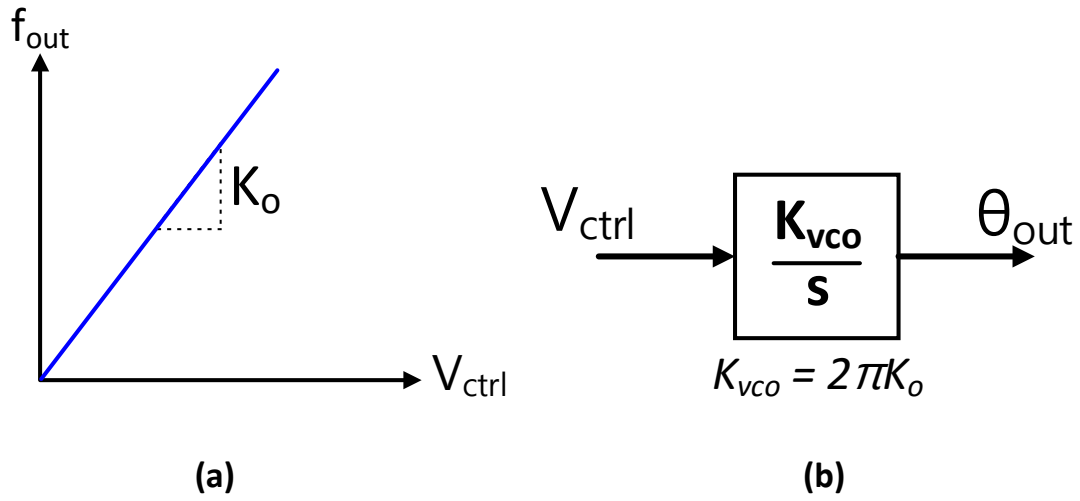


FIGURE 3.3: VCO (a) transfer function and (b) linear model

Therefore, the output phase (θ_{out}) of the VCO is the integral of the frequency as expressed below multiplied with the V_{ctrl} in [V] and K_{vco} in [rad/V].

$$\theta_{out}(s) = \frac{K_{vco}}{s} \cdot V_{ctrl}. \tag{3.4}$$

Same approach can be used to find the transfer function of the frequency divider, then the input (θ_{in}) and output (θ_{out}) phases are related by

$$\theta_{out}(s) = \frac{\theta_{in}(s)}{N}. \tag{3.5}$$

The control theory is applied on the complete simplified PLL linear model as depicted in Fig. 3.4 in order to find the open loop transfer function $A(s)$ and the closed loop transfer function $B(s)$ expressions.

$$A(s) = \frac{\theta_{fb}(s)}{\theta_e(s)} = K \cdot \frac{F(s)}{s} \tag{3.6}$$

$$B(s) = \frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{NKF(s)}{s + KF(s)} \tag{3.7}$$

where

$$K = \frac{K_{phase}K_{vco}}{N}. \tag{3.8}$$

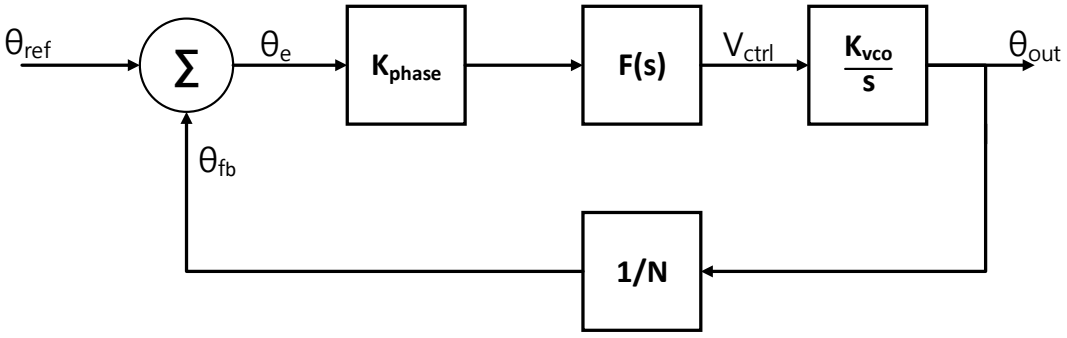


FIGURE 3.4: The complete simplified PLL linear model

The error function $E(s)$ is useful to determine the steady-state phase error θ_e, so it is expressed mathematically as

$$E(s) = \frac{\theta_e(s)}{\theta_{ref}(s)} = 1 - \frac{B(s)}{N} = \frac{1}{1 + A(s)} = \frac{s}{s + KF(s)}. \tag{3.9}$$

From the aforementioned analysis and the PLL description through the chapter, one can conclude that the output phase θ_{out} should follow the input phase θ_{in} such that the phase error θ_e is constant, either a small value or zero. Since the frequency is the derivative of the phase, a constant phase error between input and output is equivalent to zero frequency error. We still need to quantify the extend of the PLL phase and frequency tracking. This will be studied by applying various excitations at the input and calculating the response, namely the phase error. Thus, two cases will be analysed to remove any ambiguity on the PLL performance in the locked state.

The first case is ***Phase Step Excitation***. The input is excited by a phase step signal at $t = 0$. Mathematically, this is expressed in the time domain using a unit step function $u(t)$ as

$$\theta_{ref}(t) = u(t) \cdot \Delta\phi. \tag{3.10}$$

Alternatively, it can be expressed in the s-domain as

$$\theta_{ref}(s) = \frac{\Delta\phi}{s}. \tag{3.11}$$

From Fig. 3.4, the phase error is given by

$$\theta_e(s) = E(s) \cdot \theta_{ref}(s) = \frac{\Delta\phi}{s} \cdot \frac{s}{s + KF(s)}. \tag{3.12}$$

Frequency domain is used to ease the analysis, because it is hard to predict the response in the time domain. Thus, the inverse Laplace transformation is used to find $\theta_e(t)$. Initially, the phase error value was $\Delta\phi$, however the point of interest is the steady-state value, which is $\theta_e(\infty)$.

Hence,

$$\theta_e(\infty) = \lim_{s\to 0} s \cdot \theta_e(s) = \lim_{s\to 0} \frac{s \cdot \Delta\phi}{s + KF(0)} = 0. \tag{3.13}$$

It is obvious from the equation above that the PLL will track the step phase changes with zero steady-state phase error. This is correct as long as the loop filter has no zero at the origin ($F(s) \neq 0$).

The second case is ***Frequency Step Excitation***. This is similar to the first case, but here the input angular frequency will change as

$$\omega_{ref}(t) = \omega_o + \Delta\omega \cdot u(t). \tag{3.14}$$

This corresponds to a phase ramp of slope $\Delta\omega$, which is expressed in the s-domain as

$$\theta_{ref}(s) = \frac{\Delta\omega}{s^2}. \tag{3.15}$$

Similarly, the steady-state phase error is found by

$$\theta_e(s) = \frac{\Delta\omega}{s^2} \cdot \frac{s}{s + KF(s)} \tag{3.16}$$

$$\theta_e(\infty) = \lim_{s\to 0} \frac{\Delta\omega}{s + KF(s)} = \frac{\Delta\omega}{KF(0)}. \tag{3.17}$$

From the equations above, the response of the PLL to a frequency step depends on its loop filter gain at DC and the loop gain constant K. According to this result, there are two possibilities to maintain the PLL functionality. Firstly, a constant steady-state phase error which corresponds to zero frequency error between the input and output, thus the PLL is in lock condition. This case occurs if $F(0) = 1$, which means that the steady-state phase error will be inversely proportional to the loop gain K. For a small phase error, a large K is required. As a corollary, faster loop response due to larger closed-loop bandwidth is achieved [11]. Secondly, a zero steady-state phase error for a frequency step can be obtained by achieving an infinite gain from the loop filter at DC. Usually, infinite gain is practically impossible. Fortunately, this gain can be realized by using a loop filter with a pole at the origin such as a pure integrator.

3.2.2 Charge pump PLL

Charge Pump (CP) PLL is the architecture used to implement the frequency synthesizer in this study. Furthermore, the analysis of the simplified PLL will be extended in this subsection in order to define the main performance parameters.

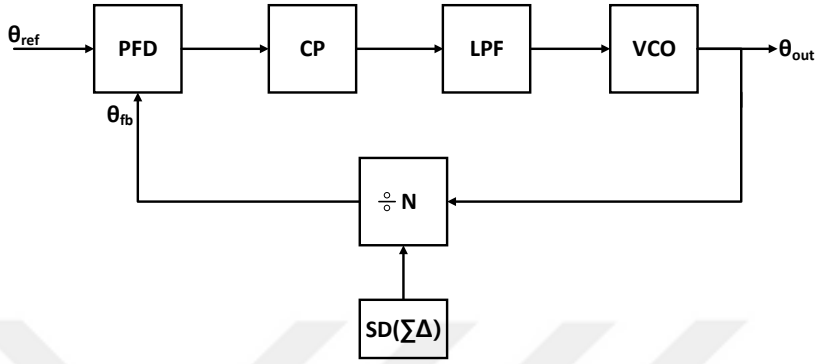


FIGURE 3.5: Charge Pump PLL block diagram

The block diagram of the CP PLL illustrated in Fig. 3.5 replaces the PD with PFD. From a functional perspective, these two approaches are identical. Both of them are digital blocks to detect the phase difference between the reference signal and the feedback signal. However, the major differences between them are the linear operating range and the ability of detecting the frequency difference. The most common architectures for PD are XORs and edge-triggered JK-Flipflop, which produce a square wave signal with an average value proportional to the phase error at the output. The loop filter of the PLL then filters out the high frequency contents and provide the VCO with the average value. Fig. 3.6 summarizes different architectures of PD and PFD functionalities.

A much more common architecture of digital phase detector is the tri-state phase detector, often called a Phase Frequency Detector (PFD). This type has the ability to detect the phase and the frequency differences by producing two outputs, UP and DN. If the reference phase θ_{ref} is ahead of the feedback phase θ_{fb} (positive phase error $+\theta_e$), UP signal is generated with the width of pulses proportional to the magnitude of the phase error θ_e. Conversely, if the reference phase θ_{ref} is lagging behind the feedback phase θ_{fb} (negative phase error $-\theta_e$), DN signal has pulses with widths proportional to the magnitude of the phase error θ_e. If the reference phase θ_{ref} and the feedback phase θ_{fb} are aligned, then the PFD does not produce an output (ideally). Since the VCO input is an analog signal V_{ctrl}, the two digital outputs from PFD should be converted to analog signals. This is achieved by using the charge pump which did not exit in the simplified model. The charge pump converts the digital UP and DN pulses into positive and negative current pulses respectively. Subsequently, the current is fed to the loop

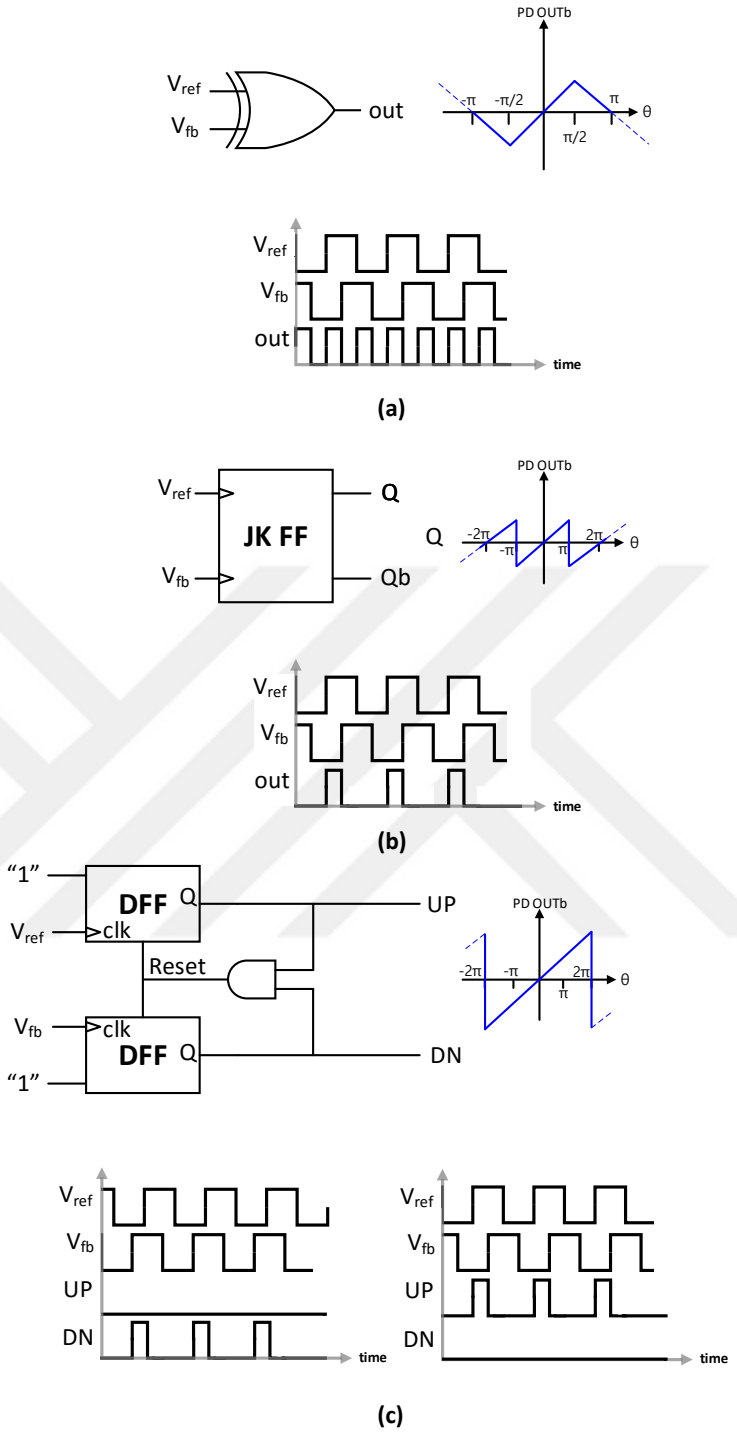


FIGURE 3.6: Phase detector operations (a)XOR, (b)JK-FF, (c)PFD/CP

filter $F(s)$, which filters these pulses to produce the VCO control voltage. This basically means that V_{ctrl} is constructed by successive voltage increments/decrements because of pumping positive/negative charges into this loop filter.

The functionality of PD and PFD/CP as explained above uses the assumption that the

two inputs have equal frequencies. Unfortunately, this is not a real case. In reality, they either have different phases or frequencies or both. If PD faces a case of different input frequencies, the detector output becomes totally wrong as the difference increases, which results in the PLL unlocking forever. However, the way the PFD/CP works in Fig. 3.7 shows its ability to correct for the frequency difference [11]. For instance, if the reference signal has a higher frequency than the feedback signal, the PFD stays in the (+1) state for a longer time. As a result, this forces the charge pump to pump more charges into the loop filter to increase the VCO control voltage, hence increase the feedback frequency. In contrast, the PFD stays in the (-1) state for a longer time when the feedback signal has a higher frequency. Consequently, the charge pump discharges the loop filter to decrease the VCO frequency. To sum it up, PFD/charge pump has advantages over

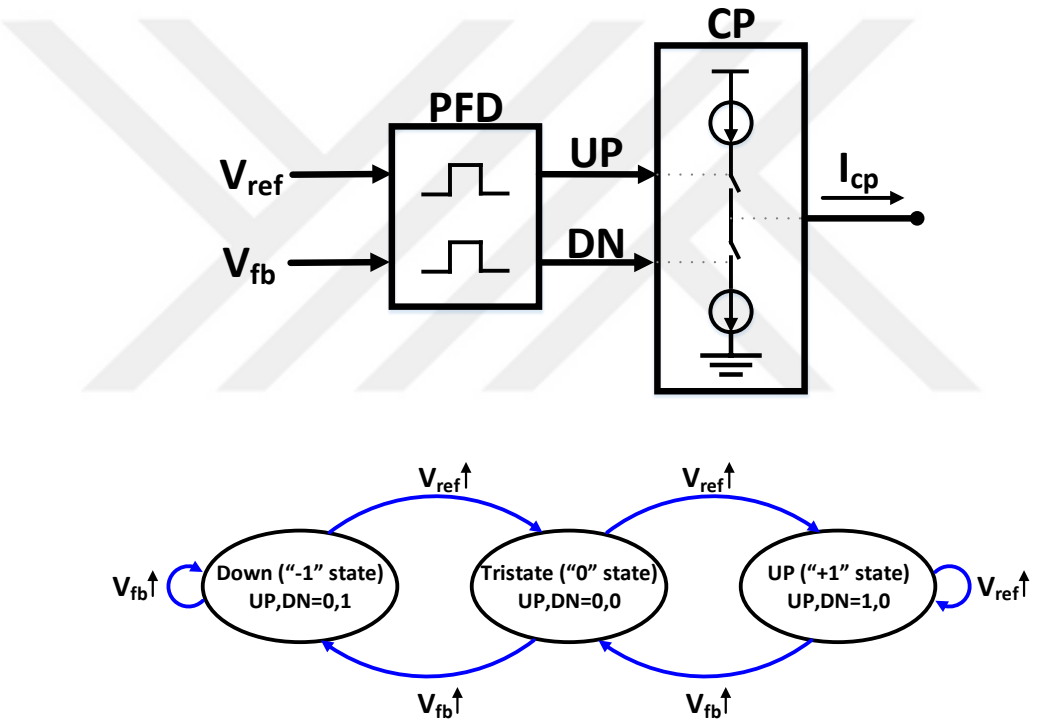


FIGURE 3.7: PFD/CP state diagram

other digital PDs. Mainly, PFD/charge pump has a wider linear range of $\pm 2\pi$ which has a direct impact on the PLL performance. PFD/charge pump also detects the frequency difference and helps the loop in correcting them.

The phase detector in the charge pump PLL is composed of two parts: a purely digital PFD and analog charge pump which converts the digital signals (UP and DN) into current pulses. Consequently, the output of the PFD/CP in these type of PLLs is not voltage anymore. Therefore, the simplified PLL linear model should be modified to include the added elements in the CP PLL. Since PLL can be seen as a frequency multiplier, the

reference frequency is assumed to be considerably smaller than the output frequency, hence we can consider it as a slowly varying. This assumption eases the analysis and allows us to use the average value of the charge pump current instead of the instantaneous value and relate it to the phase error θ_e.

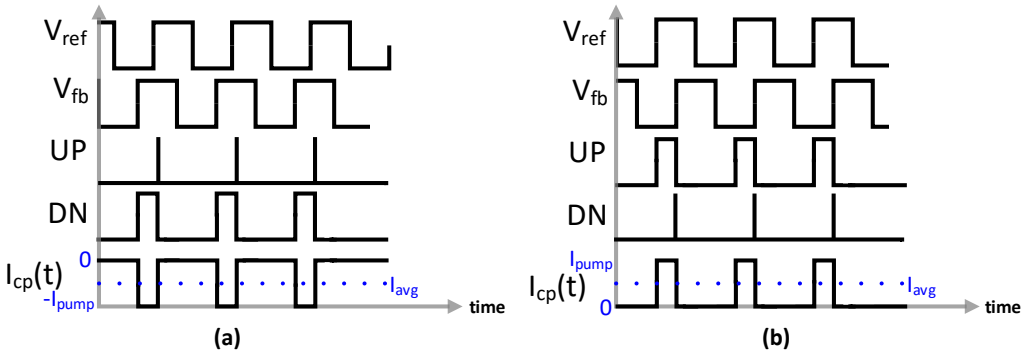


FIGURE 3.8: Reference, Feedback, UP, DN and CP current signals in both cases: (a) when the feedback signal precedes the reference signal, (b) when the reference signal precedes the feedback signal

The charge pump current turns on every reference cycle (T_{ref}) when there is UP or DN signal. These signals determine the on-time of this current as illustrated in Fig. 3.8. Thus, the average charge pump current is

$$I_{average} = I_{pump} \cdot (\frac{t_{on}}{T_{ref}}). \tag{3.18}$$

The on-time of the charge pump current is directly related to the phase error θ_e. Therefore, the phase detector constant K_{phase} is given by

$$K_{phase} = \frac{I_{average}}{\theta_e} = \frac{I_{pump}}{2\pi}. \tag{3.19}$$

Finally, the complete linear model of the CP PLL is shown in Fig. 3.9. This model will be used to design the PLL system and extract the main performance parameters such as the loop filter component values, stability, spur level, settling time and phase noise.

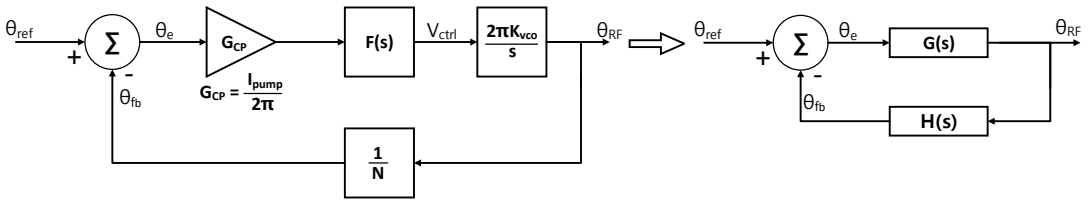


FIGURE 3.9: Linear model of the CP PLL

In a similar fashion of the simplified PLL linear model, the control theory is applied to the complete CP PLL linear model. The forward loop gain G(s) is given by

$$G(s) = \frac{\theta_{RF}}{\theta_e} = \frac{I_{pump}F(s)K_{vco}}{s} \tag{3.20}$$

and the reverse loop gain is given by

$$H(s) = \frac{\theta_{FB}}{\theta_{RF}} = \frac{1}{N}. \tag{3.21}$$

The open loop gain is

$$A(s) = G(s)H(s) = \frac{\theta_{FB}}{\theta_e} = \frac{I_{pump}F(s)K_{vco}}{sN}. \tag{3.22}$$

Finally, the closed loop gain is

$$B(s) = \frac{G(s)}{1 + G(s)H(s)} = \frac{\theta_{RF}}{\theta_{REF}} = \frac{NI_{pump}F(s)K_{vco}}{sN + I_{pump}K_{vco}F(s)}. \tag{3.23}$$

Undoubtedly, the PLL depends strongly on the type and the order of the loop filter used. Commonly, a PLL is described in terms of the order and the type of the loop. The type of PLL is defined by the number of poles at zero frequency, and the order of the loop filter designed in a PLL defines its order. The order of the loop is one order higher than the loop filter transfer function $F(s)$.

First let's start designing the loop filter by a single capacitor that can store the charges from the CP to produce the average control voltage to VCO. However, this leads to instability because of two poles at the denominator, one due to the integrator (VCO) and the other due to this capacitor. Therefore, a series resistance should be added with this capacitor to cancel the capacitor pole impact to ensure the loop is stable. Unfortunately, this resistance generates ripples on the control voltage with amplitude $(I.R)$, thus another capacitor should be introduced in parallel with this branch to reduce the ripples. This loop filter has two poles (second order), therefore the PLL is called a third order PLL. Nevertheless, this is insufficient to attenuate the spurs level that can modulate the carrier. Hence, an RC filter following the loop filter is added to get better spur attenuation. Consequently, a third order LPF is formed and this becomes fourth order type II CP PLL.

3.2.3 Fourth order type II CP PLL

In order to determine the component loop filter values, open loop gain bandwidth and phase margin of the loop is used. This method depends on locating the point of minimum phase shift at the unity gain frequency of the open loop response (refer Fig. 3.10) in order to ensure the loop stability [12]. As a role of thumb, higher phase margin leads to higher stability, slower loop response and more attenuation of spurs at f_{ref}. Hence, a compromise between these trade-offs should be taken into the consideration.

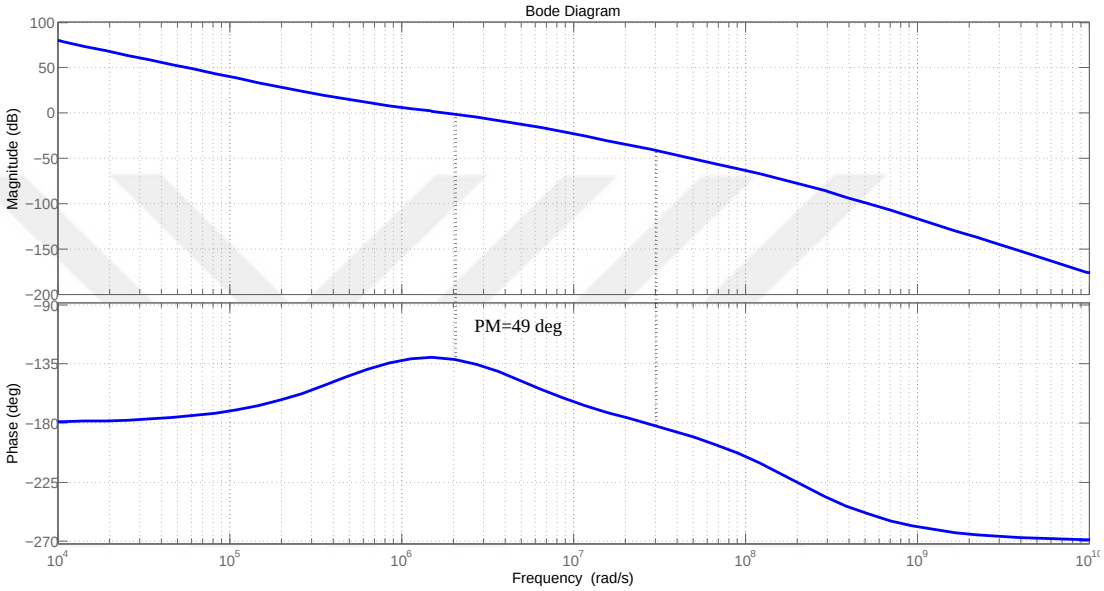


FIGURE 3.10: The open loop response of the fourth order type II CP PLL

As stated in the previous section, the low pass filter has to be third order as shown in Fig. 3.11. Thus, the impedance of this filter is given by

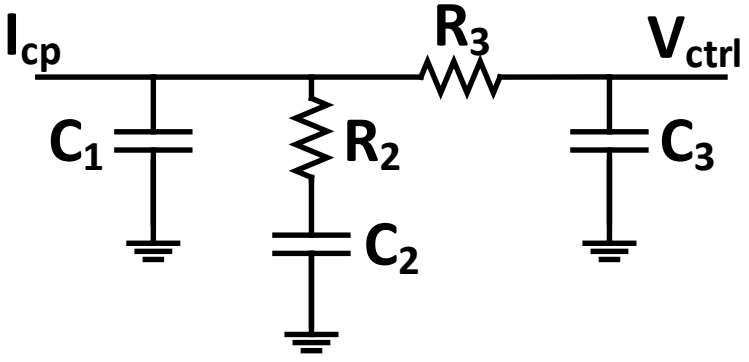


FIGURE 3.11: Third order low pass filter

$$F(s) = \frac{sC_2R_2 + 1}{s^3C_1C_2R_2 + sC_1 + sC_2} \cdot (\frac{1}{1 + sR_3C_3}). \tag{3.24}$$

The third order low pass filter transfer function can be resolved by decomposing the function into time constant functions. These functions define the poles and zeros for the low pass filter that are mathematically represented as below

$$T_1 = R_2 \cdot \frac{C_1C_2}{C_1 + C_2} \tag{3.25}$$

$$T_2 = R_2 \cdot C_2 \tag{3.26}$$

$$T_3 = R_3 \cdot C_3. \tag{3.27}$$

Since the pole defined by T_3 is responsible to attenuate the reference spurs, the attenuation amount in dB is given by:

$$Attn = 10log[(2\pi f_{ref}R_3C_3)^2 + 1]. \tag{3.28}$$

By substituting the equations from 3.24 to 3.28 in equations 3.22 and 3.23 and use the MATLAB model, the loop parameters can be easily calculated for a given attenuation factor, loop bandwidth and phase margin.

3.3 CP PLL Phase noise

This section focuses on the main performance aspect of a frequency synthesizer in RF transceiver which is the phase noise. Each block in the loop has its own output noise and this noise contributes to the overall output phase noise of the frequency synthesizer. Therefore, noise is modeled as an input to the summing junctions of a voltage, current, or phase noise sources at each block's output in the linear model as illustrated in Fig. 3.12. The transfer function between these noise sources and the output phase has to be determined in order to study how each noise source propagates to the output. Equation (3.29) shows the contribution of each noise source in the overall CP PLL phase noise.

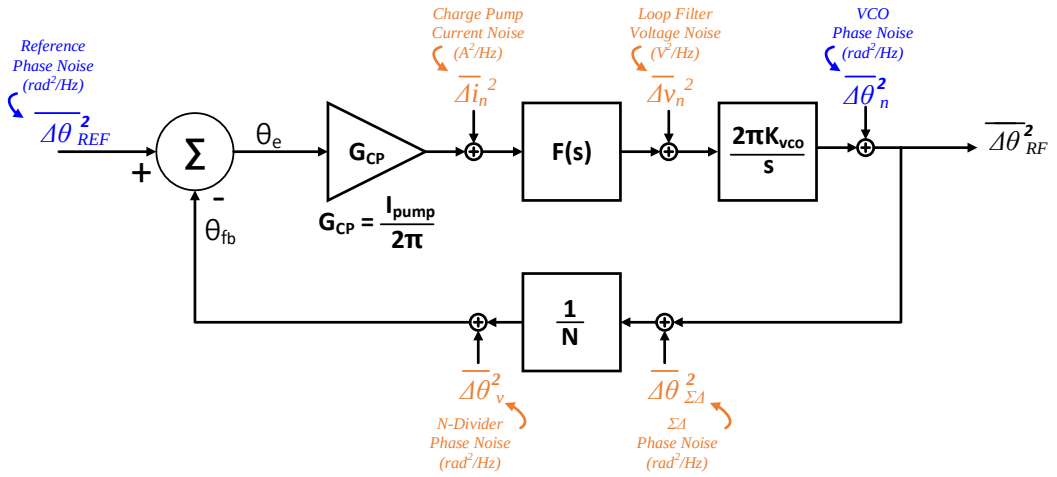


FIGURE 3.12: CP PLL linear model with added noise sources

$$\overline{\Delta\theta_{RF}}^2 = |T_1|^2 \cdot \overline{\Delta\theta_{REF}}^2 + |T_2|^2 \cdot \overline{\Delta\theta_n}^2 + |T_3|^2 \cdot \overline{\Delta i_n}^2 + |T_4|^2 \cdot \overline{\Delta v_n}^2 + |T_5|^2 \cdot \overline{\Delta\theta_v}^2 + |T_6|^2 \cdot \overline{\Delta\theta_{\sum\Delta}}^2. \tag{3.29}$$

3.3.1 Phase noise of oscillators

The noise power in the oscillator is dependent on:

- Oscillator Q.
- Oscillation frequency f_o.
- Carrier offset frequency Δf.
- Active devices noise contribution.
- Oscillation amplitude and non-linear effect.

Lesson's equation models the oscillator single side band phase noise as given in equation (3.30) [13]. However, the noise of the oscillator changes according to its type.

$$\mathcal{L}(\Delta f) = 10log[\frac{2KTFR}{P_c}[1 + \frac{1}{4Q^2}(\frac{f_o}{\Delta f})](1 + \frac{f_c}{\Delta f})] \tag{3.30}$$

where f_c is the flicker corner frequency, F is the noise figure of the oscillator and P_c is the average oscillation signal power. Furthermore, the phase noise is shaped as illustrated in Fig. 3.13.

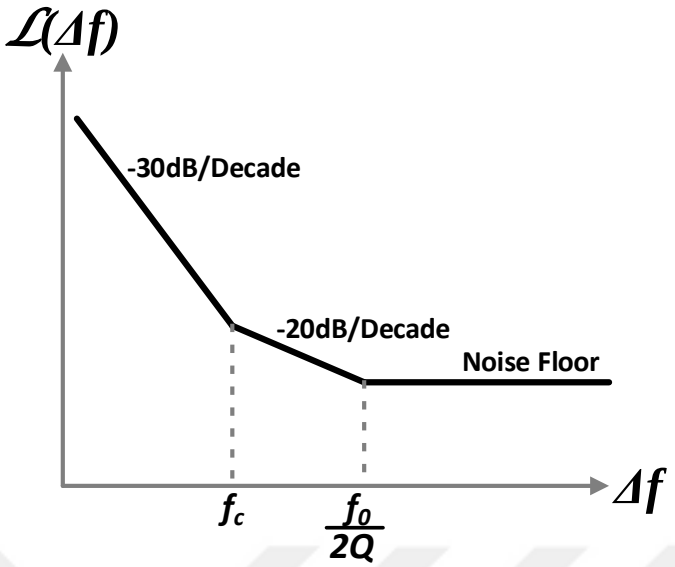


FIGURE 3.13: Oscillator phase noise

The CP PLL has two oscillators, reference oscillator and VCO, hence the expected phase noise from these blocks should follow Fig. 3.13. However, the design performance concern is at the PLL's output not each block stand alone. Therefore, their impact at the output is shaped by the transfer function of the CP PLL.

The reference oscillator phase noise is translated to the output through the closed loop transfer function given by

$$T_1 = \frac{\overline{\Delta\theta_{RF}}^2}{\overline{\Delta\theta_{REF}}^2} = B(s). \tag{3.31}$$

Fig. 3.14 illustrates the effect of the transfer function on the reference phase noise. The closed loop transfer function behaves as a low pass filter with a finite loop bandwidth. Equation (3.23) shows that, at low frequencies ($f < f_{bw}$), $B(s) = N$, which in turn increases the in-band noise by $20log(N)$. At high frequencies ($f_{bw} < f < f_{p3}$) the transfer function has $-40dB$ per decade and at very high frequencies ($f > f_{p3}$), it has $-60dB$ per decade dependence with frequency for a fourth order loop, hence the reference phase noise is shaped accordingly.

Obviously, the dominant phase noise at the output of the CP PLL at very low frequencies as shown in Fig. 3.14 can easily be predicted. The flicker noise of the oscillator is amplified with a flat response in this region. It is worth mentioning that any circuit such as the duty cycle correction and the frequency multiplier before the reference input of the CP PLL loop will be translated by the same transfer function as the reference oscillator.

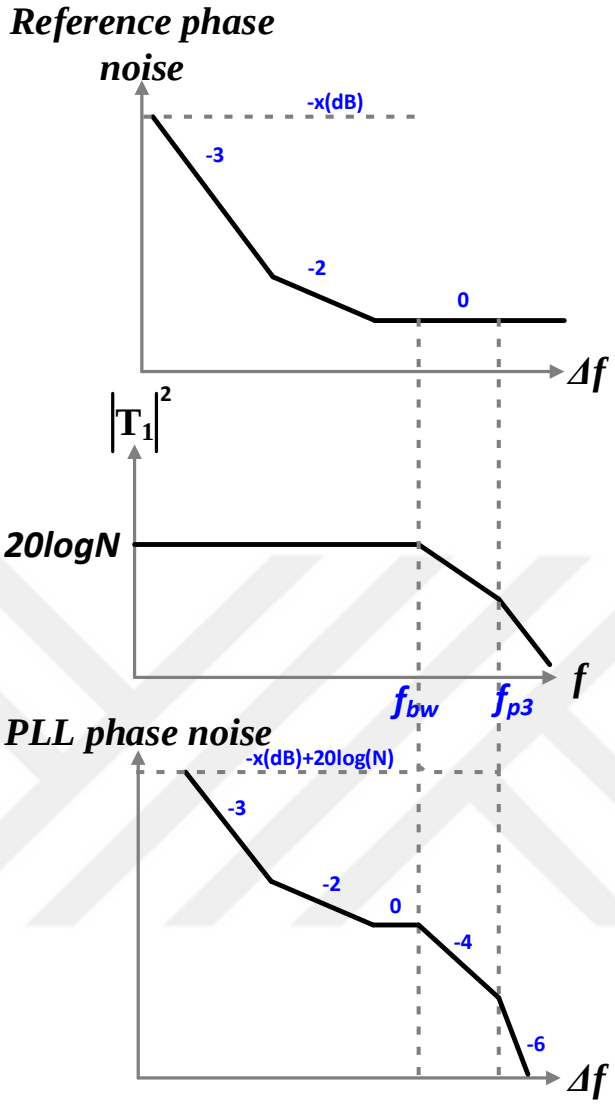


FIGURE 3.14: PLL output phase noise due to reference phase noise

The VCO phase noise is translated to the output through the transfer function given below

$$T_2 = \frac{\overline{\Delta\theta_{RF}}^2}{\overline{\Delta\theta_{REF}}^2} = \frac{B(s)}{G(s)} = \frac{Ns}{Ns + I_{pump}K_{vco}Z(s)}. \tag{3.32}$$

Fig. 3.15 illustrates the impact of the transfer function on the VCO phase noise. The transfer function has a high pass filter characteristics. Equation (3.32) shows that, at low frequencies ($f < f_{bw}$), the transfer function has $+40dB$ per decade dependence with frequency and at high frequencies ($f_{bw} < f$), this dependency approaches unity. Consequently, the VCO phase noise propagates to the CP PLL output without any filtring. Hence, the overall CP PLL phase noise is dominated by the VCO phase noise at

frequencies higher than the loop bandwidth. Finally, we have modeled the phase noise and the transfer function for each block using MATLAB and the translated phase noise for the reference oscillator, the duty cycle correction block, the frequency multiplier and the VCO implemented in the proposed system. The results are shown in the Fig. 3.16 to 3.19.

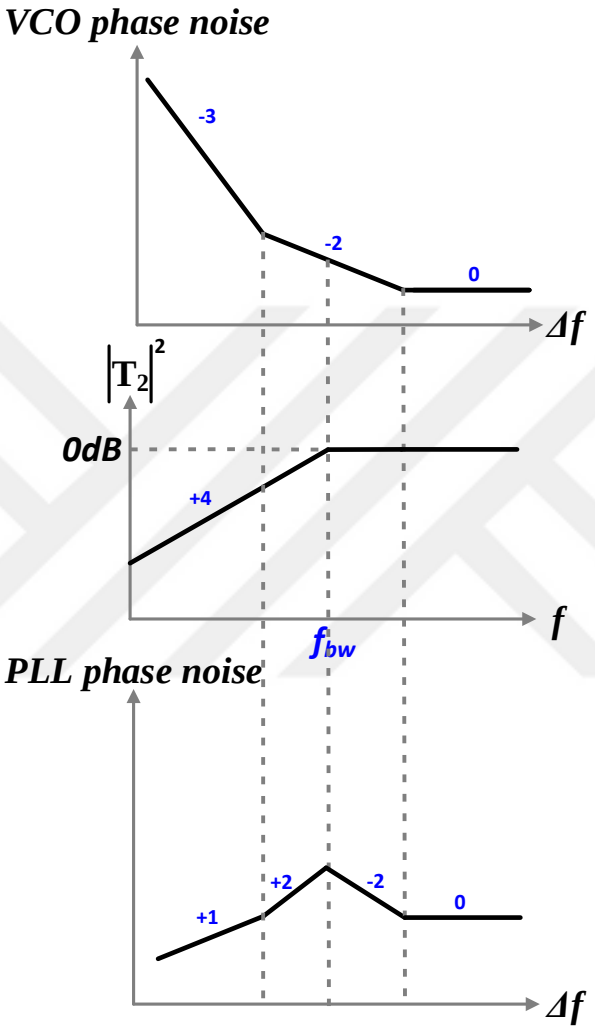


FIGURE 3.15: PLL output phase noise due to VCO phase noise

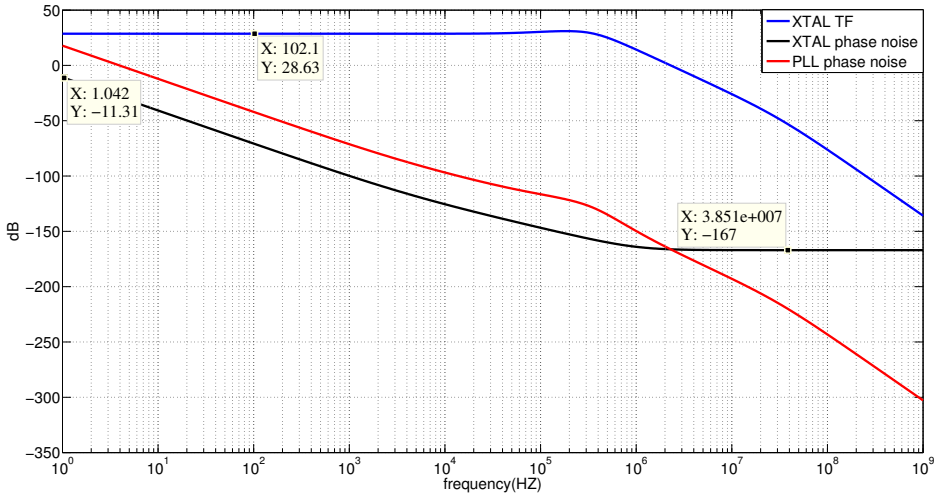


FIGURE 3.16: Reference oscillator MATLAB model result

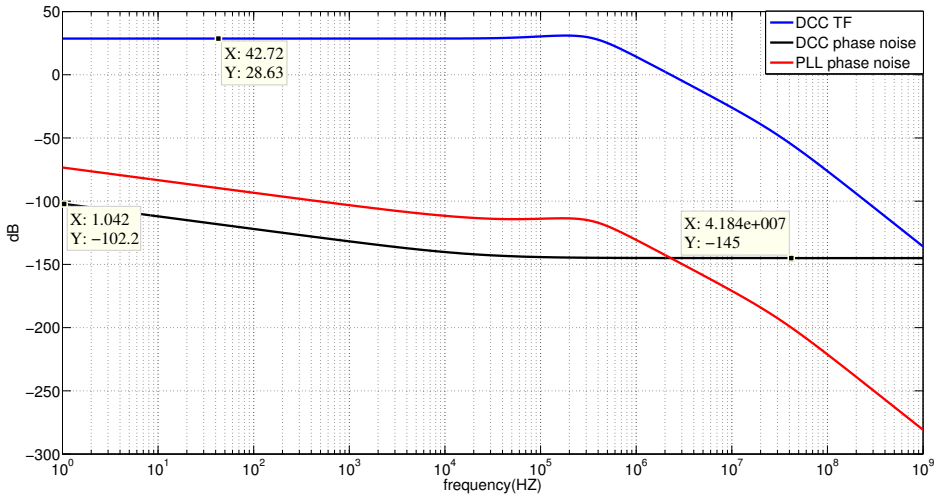


FIGURE 3.17: Duty cycle correction MATLAB model result

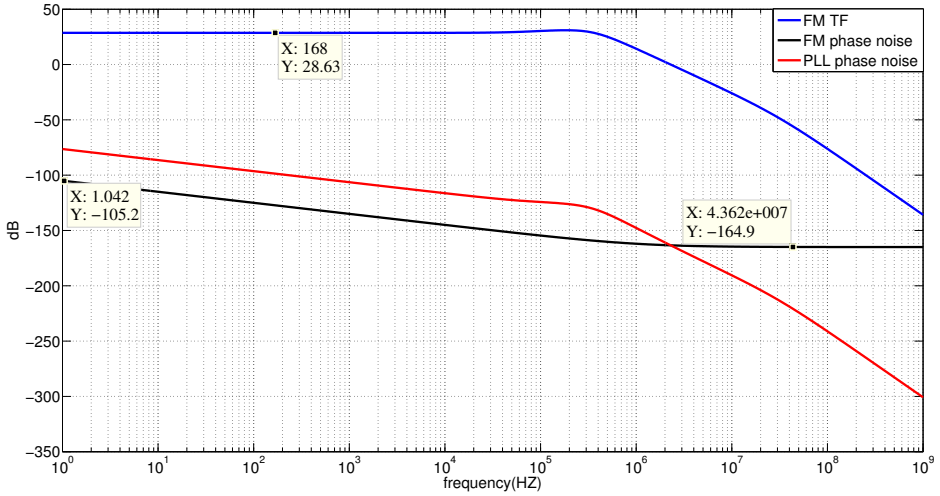


FIGURE 3.18: Frequency multiplier MATLAB model result

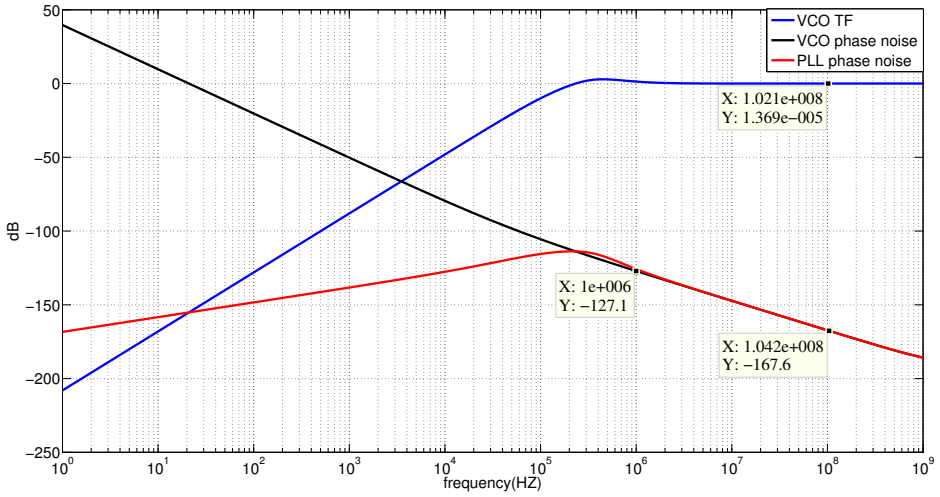


FIGURE 3.19: VCO MATLAB model result

3.3.2 Phase noise of PFD/Charge pump

Thermal noise of the PFD results in timing jitter on both rising and falling edges of the UP and DN pulses. This timing jitter is translated to an equivalent phase jitter on the VCO output through the control voltage, elevating its phase noise floor.

Charge pump noise is produced by the charge pump output current, which is proportional to how long it is on at steady state. Both up and down current sources are on for a short time every reference cycle [14]. This on-time is generated due to the difference in arrival times for the control signal edges (UP and DN). Therefore, PFD/CP noise can be modeled as one block, which has an output current noise.

The PFD/CP noise is modeled by

$$\overline{i_n}^2 = \alpha_{cp} \cdot noisefloor \cdot (1 + \frac{f_c}{f}) \tag{3.33}$$

where f_c is the flicker corner, α_{cp} is the percentage of the time where the CP is on at steady state.

The relationship between the output phase noise and the current noise source of the charge pump is given by a transfer function

$$T_3 = \frac{\overline{\Delta\theta_{RF}}^2}{\overline{\Delta i_n}^2} = \frac{2\pi B(s)}{I_{pump}}. \tag{3.34}$$

The charge pump noise sees a low pass filter transfer function, and thus it goes through a similar transfer function as the reference oscillator noise. Since CP has the most amount of thermal noise generation, the overall CP PLL phase noise is dominated by the CP thermal noise at low frequencies. However, the charge pump current noise has a different amplification factor as shown in Fig. 3.20. Accordingly, the CP current peak has a big impact on improving the CP PLL output phase noise. By using MATLAB model for the charge pump, the block phase noise, the transfer function and the translated phase noise is shown in Fig. 3.21.

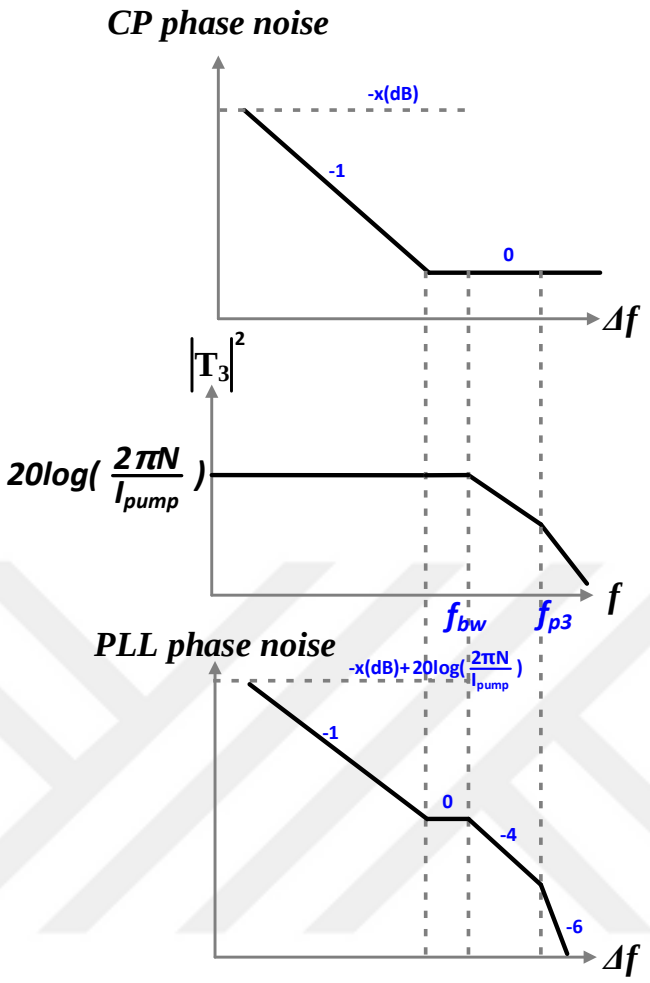


FIGURE 3.20: PLL output phase noise due to PFD/CP phase noise

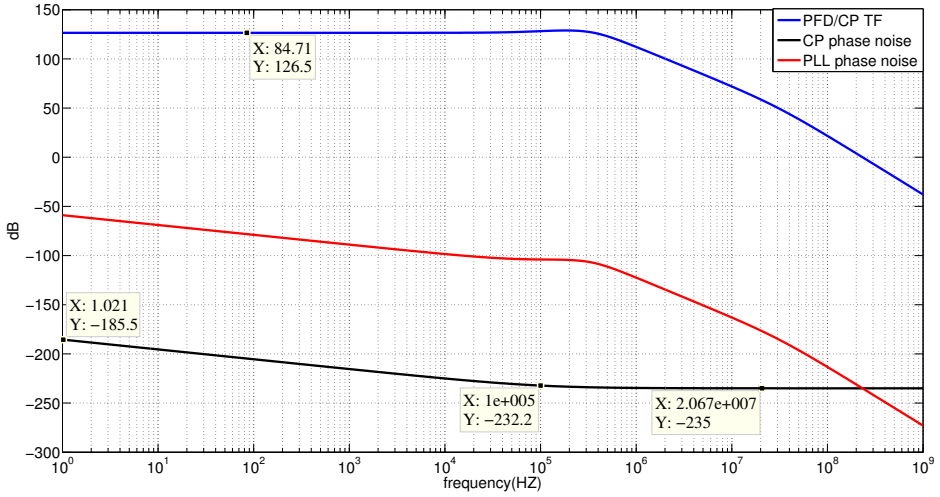


FIGURE 3.21: CP MATLAB model result

3.3.3 Phase noise of loop filter

The loop filter noise is modeled as a voltage noise source, which mainly depends on the filter implementation. In fact, the loop filter is an impedance in the case of a CP PLL. It can be implemented by passive or active components. As stated previously, a passive loop filter is implemented, hence resistors R_1 and R_3 shown in Fig. 3.11 are the noise contributors. Since the thermal noise of a resistor as given by equation (3.35) is proportional to its value, the noise contribution depends on the resistors value.

$$\overline{v_n}^2 = 4KTR. \tag{3.35}$$

As a result, the loop filter adds noise to the loop by transferring the filter output voltage noise to the CP PLL output by the transfer function below

$$T_4 = \frac{\overline{\Delta\theta_{RF}}^2}{\overline{\Delta v_n}^2} = \frac{2\pi B(s)}{I_{pump}F(s)}. \tag{3.36}$$

Fig. 3.22 visualizes the impact of the interaction between the closed loop transfer function and the loop filter by a piece-wise linear representation. At low frequencies, each resistor produces noise at the filter output. At high frequencies, R_1 is attenuated by two poles while R_3 is attenuated by a single pole. Hence, R_3 dominates the noise produced at the loop filter output and it has a $-40dB$ per decade dependence. By using MATLAB model for the loop filter, the block phase noise, the transfer function and the translated phase noise is shown in Fig. 3.23.

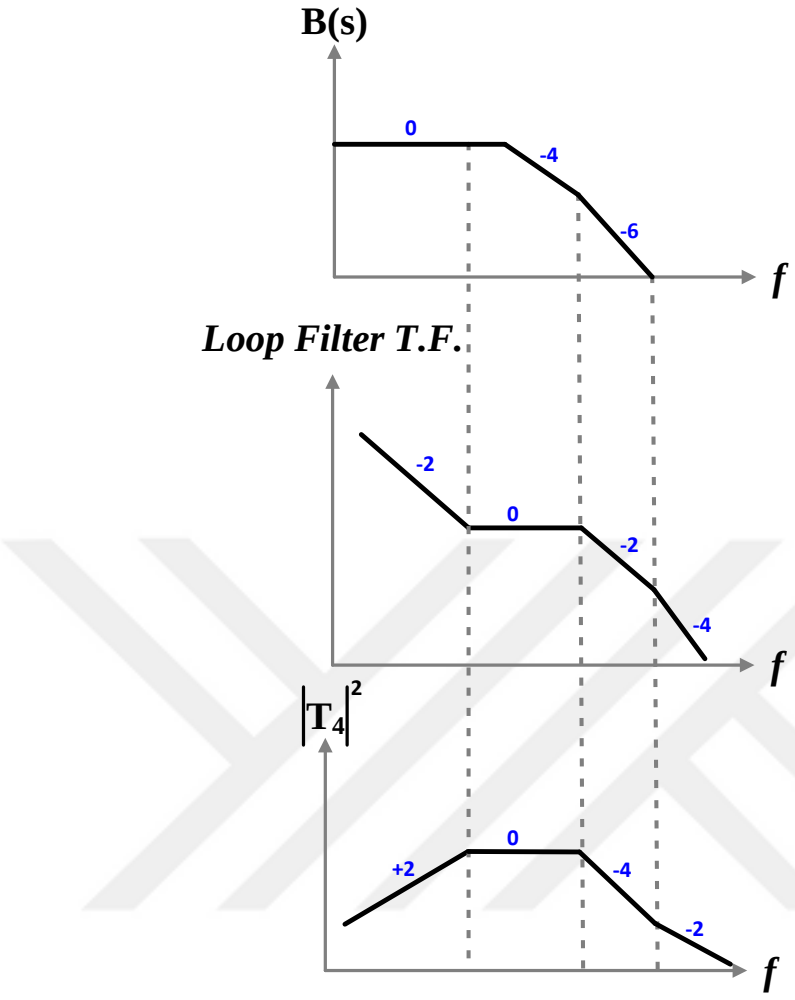


FIGURE 3.22: a piece-wise linear representation of B(s), F(s) and T_4

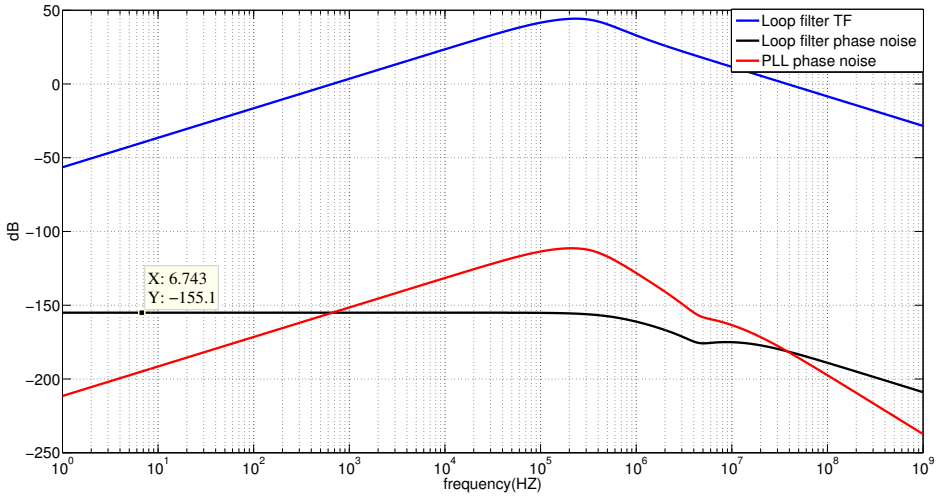


FIGURE 3.23: Loop filter MATLAB model result

3.3.4 Phase noise of frequency divider

The divider phase noise is best understood by considering the noise in the time domain as timing jitter. The output signal of the divider in the time domain may have extra jitter due to the noise of the divider active devices. The noise can be modeled using flicker and thermal noise sources at the divider output.

Since the divider attenuates the phase by $(1/N)$, it is expected to also attenuate the overall phase noise at the output by the same ratio, therefore gives an improvement of $20logN$. A divider also produces phase noise due to its own device noise sources, hence, practical dividers usually do not achieve this improvement and the actual frequency divider phase noise is given by

$$\mathcal{L}(\Delta f)_{out} = \mathcal{L}(\Delta f)_{DIV} + \frac{1}{N^2} \cdot \mathcal{L}(\Delta f)_{VCO}. \tag{3.37}$$

It is evident from equation (3.37) that, as the division ratio increases the output phase noise of the divider is approximately equal to the divider phase noise. However, this does not imply the perfect solution for the divider output noise, because as N increases, the divider circuitry increases, hence the noise increases.

Now, the transfer function of the frequency divider output noise to the output CP PLL is given by

$$T_5 = \frac{\overline{\Delta\theta_{RF}}^2}{\overline{\Delta\theta_v}^2} = B(s). \tag{3.38}$$

Equation (3.38) is similar to the reference oscillator case, hence one can easily predict the transfer function impact on the output noise of the frequency divider. Furthermore, the frequency divider phase noise is also considered as one of the dominant contributors of the overall phase noise at low frequency. By using MATLAB model for the frequency divider implemented in the proposed system, the block phase noise, the transfer function and the translated phase noise is shown in Fig. 3.24.

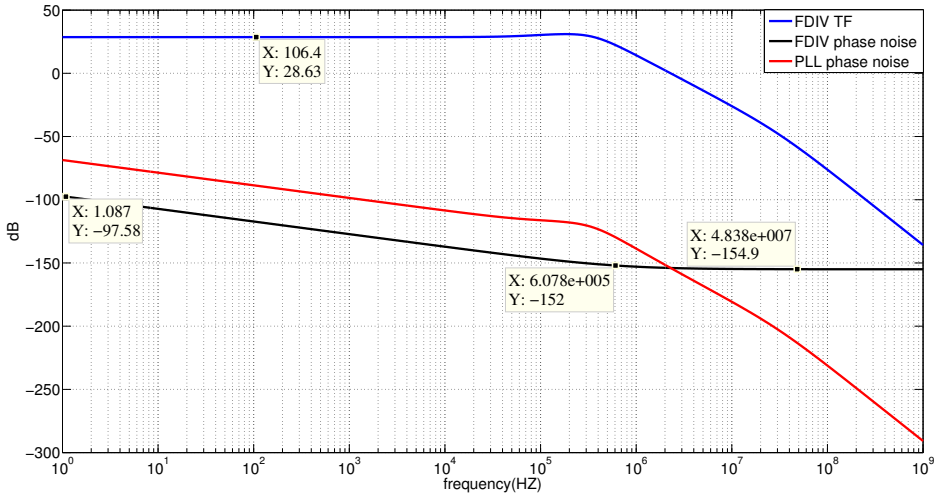


FIGURE 3.24: Feedback divider MATLAB model result

3.3.5 Phase noise of Sigma Delta ($\sum\Delta$) modulator

In a fractional-N synthesizer, the integer divider value is dithered to achieve fractional values. If accumulator is used to perform the dithering operation, a periodic error signal creates spurious tones in the synthesizer output. Hence, sigma-delta modulator is considered the best choice for dithering operation for its superiority in attenuating the reference spurious tones. On the other hand, the sigma delta modulator adds quantization noise which is shaped according to its order. The quantization noise spectrum for an m^{th}-order MASH-type SDM is given by [15]

$$\mathcal{L}(f)_{SD} = \frac{(2\pi)^2}{12 f_s}[2sin(\frac{\pi f}{f_s})]^{2(m-1)} \tag{3.39}$$

where f is the offset frequency, f_s is the sampling frequency and equals to the reference frequency, m is the sigma delta modulator order. The order of the PLL loop filter must be higher than or equal to the order of the $\sum\Delta$ modulator in order to attenuate the out-of band noise. Since a third order loop filter is implemented, third order sigma delta can be implemented.

The $\sum\Delta$ output noise is transferred to the CP PLL output by the transfer function given below

$$T_6 = \frac{\overline{\Delta\theta_{RF}}^2}{\overline{\Delta\theta_{\sum\Delta}}^2} = \frac{B(s)}{N}. \tag{3.40}$$

Some observations from equation (3.39) and equation (3.40) are:

- As sampling frequency increases, the $\sum\Delta$ phase noise decreases, which means as the reference frequency increases, the $\sum\Delta$ phase noise improves.
- The transfer function is similar to the reference oscillator, frequency divider and charge pump, but with $0dB$ at low frequencies. Since the $\sum\Delta$ functionality is to push the quantization noise to high frequencies and there is no amplification factor at low frequencies, the $\sum\Delta$ phase noise contributes only at high frequencies.

By using MATLAB model for the $\sum\Delta$ implemented in the proposed system, the block phase noise, the transfer function and the translated phase noise is shown in Fig. 3.25.

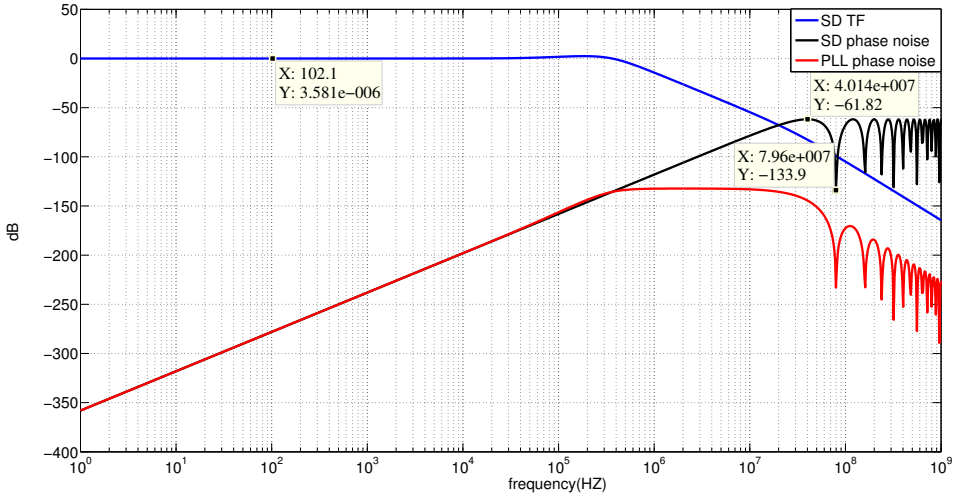


FIGURE 3.25: Sigma Delta MATLAB model result

3.3.6 Optimal loop bandwidth of a PLL

Since the choice of the loop bandwidth involves trade-offs between stability, phase noise, lock time and spurs, it is considered the most critical design parameter. The loop bandwidth that is optimal for phase noise performance is usually the best choice for many clocking applications.

According to the previous discussions, we can conclude that the loop bandwidth should be as wide as possible in order to minimize the output phase noise caused by the VCO and $\sum\Delta$ phase noise. Whereas, the loop bandwidth should be as narrow as possible in order to achieve the minimum phase noise from the in-band noise sources (reference oscillator, PFD/CP and frequency divider). Furthermore, the loop bandwidth needs to be less than $1/10^{th}$ the reference input frequency ($f_{ref}/10$) as a role of thumb to maintain the loop stability and to have sufficient spurs attenuation at the output. Therefore, to attain the best phase noise performance at the output, the best value to set the loop bandwidth

is where the VCO phase noise crosses the worst contributor in the in-band phase noise. Fig. 3.26 shows the estimated overall phase noise performance of the proposed system. The total RMS Phase Jitter from 10KHz to 10MHz is 520fs for this phase noise profile.

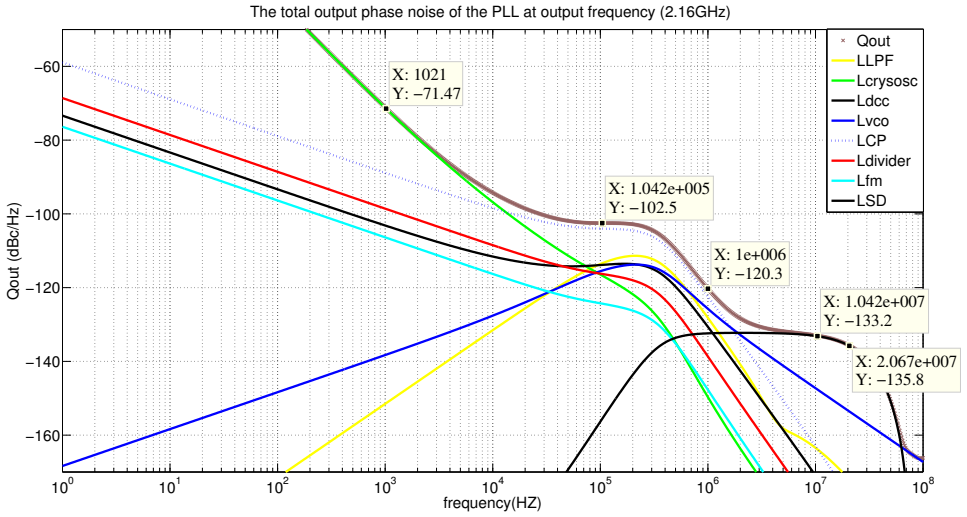


FIGURE 3.26: The overall PLL phase noise performance MATLAB model result

3.4 Overall specifications performance

Before summarizing the extracted loop specifications from MATLAB, a brief discussion is introduced to complete the explanation behind choosing these values.

3.4.1 Loop Bandwidth

The loop bandwidth should be designed to satisfy the optimum phase noise, guarantee stability and proper response speed. Since, the reference frequency is programmable from 40MHz to 640MHz, the loop bandwidth should be programmable as well. The typical PLL bandwidth in our design is 350KHz.

3.4.2 PFD and Charge pump

Since, the charge pump current contributes in the phase noise and stability, the charge pump current is programmable from 40μA to 280μA. This gives post production control to optimize this parameter.

3.4.3 VCO

The VCO gain K_{vco} should be chosen carefully in order to satisfy the phase noise and the tuning range. As the tuning range increases, K_{vco} should increase as well. However, a large value of K_{vco} causes the phase noise to degrade. We have chosen an optimal value of K_{vco} for the design, which is 38MHz/V nominally and the tuning range of the VCO is from 2GHz to 2.5GHz.

3.4.4 Loop filter

As mentioned earlier, the loop bandwidth should be programmable, which implies that the loop filter should be programmable as well. The nominal values of the loop filter components are summarized in the last section.

3.4.5 Summary

Table (3.1) illustrates the important typical specifications for the fourth order type II CP PLL. It is worth noting that all the MATLAB results in this chapter are with specific parameter values as shown in the table below. The reference frequency is assumed to be 40MHz, the division ratio is chosen to be 27, multiplication factor is 2, charge pump current is 80μA and the output frequency 2.16GHz. In the following chapters, deep analysis is introduced individually for each duty cycle correction, frequency multiplier, and VCO blocks as well as their specifications performance.

Table 3.1: Specifications Summary

Parameters	**Values**
Reference Frequency	40MHz
Reference Frequency Multiplication Factors	2, 4, 8, 16
Charge Pump Current (I_{pump})	40μA - 280μA.
Loop Filter Components	R2=19KΩ, C2=98pF, C1=7pF, R3=1.5KΩ, C3=7.4pF
Loop Bandwidth	350KHz
Phase Margin	49^o
VCO Gain (K_{vco})	38MHz/V
Division Ratio (N)	[50-63], [25-32], [12-16], [6-8], [3-4]

Chapter 4

Duty Cycle Correction

4.1 Introduction

Frequency Multipliers to be used with Frequency Synthesizers require duty cycle of nearly 50% and low phase noise contribution to the overall system phase noise for proper operation. This chapter proposes a mixed signal solution based on the fact that the average DC value of a signal is proportional to its duty cycle. The solution uses a feedback loop for coarse and fine duty cycle correction resolution. Proposed Duty Cycle Correction (DCC) circuit can correct input duty cycle variations from 40% to 60% for a 40MHz input frequency with 50%±0.3% accuracy. Furthermore, in order to estimate the output clock phase noise, a simulation method with supply white noise model is proposed.

Frequency doublers or quadruplers are blocks that require a clock with duty cycle of 50% for optimal operation. Although frequency dividers or quadrature oscillators tend to generate clocks with 50% duty cycle, this is not the case with the crystal oscillators, which may have duty cycle somewhere between 40% to 60%. Thus, the frequency doubler/quadrupler either has to compensate for the variations or duty cycle correction becomes a necessity.

4.2 Problem statement

Fig. 4.1 shows the possible usage of a frequency doubler/quadrupler. Increasing the reference clock frequency in a synthesizer reduces the phase noise contribution of loop components and enables higher loop bandwidth, which results in more rejection of VCO phase noise [16], [17]. For a multiplication factor of two and a perfect 50% duty cycle at the input, the output of the doubler is shown in Fig. 4.2(a). In this case, the frequency

multiplier works properly and the output clock is doubled, creating a monotonous clock. On the other hand, if the duty cycle of the reference crystal clock is not 50%, the frequency multiplier will face two possibilities. Firstly, it may not work properly because the pulse width is less than the delay used to generate a doubled clock. Secondly, it may work as shown in Fig. 4.2(b), which shows a frequency of $2f_{xo}$ with a strong XO tone buried in it. The XO tone will cause the synthesizer output spectrum to have strong reference spurs, and those spurs might not get sufficient attenuation by the frequency synthesizer loop filter. Hence, it will have a detrimental impact on the performance of the frequency generation block. Equation (4.1) shows the level of spur power at the output of a third order PLL system as a function of the duty cycle of the reference clock.

$$Spur_n = [I_{cp}(0.5 - DC) \cdot sinc(n(0.5 - DC))]^2 \cdot \left| Z(s)\frac{K_{VCO}}{s} \right|^2 \left| \frac{H_{CL}(s)}{G_{FL}(s)} \right|^2 . \tag{4.1}$$

Where,

I_{cp}: Charge pump up/down current pulse amplitude.

DC: Duty cycle value.

n: The spur order.

$Z(s)$: The loop filter transfer function.

K_{VCO}: The VCO gain at the oscillating frequency.

$H_{CL}(s)/G_{FL}(s)$: The closed/forward loop transfer function.

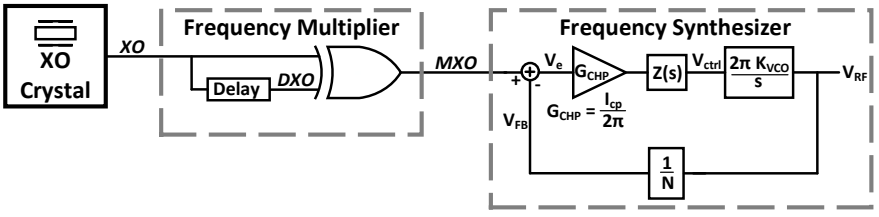


FIGURE 4.1: Block diagram of the top level system.

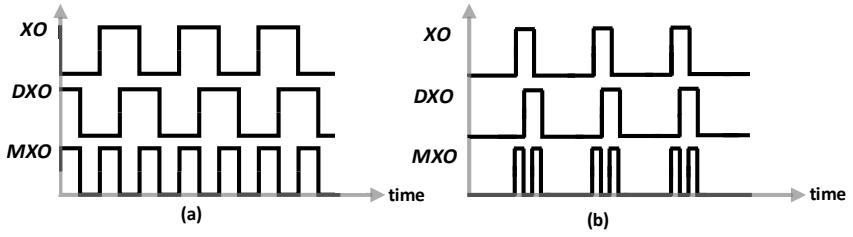


FIGURE 4.2: The frequency multiplier functionality. (a) When the duty cycle of the input clock is 50%. (b) When the duty cycle of the input clock is not 50%.

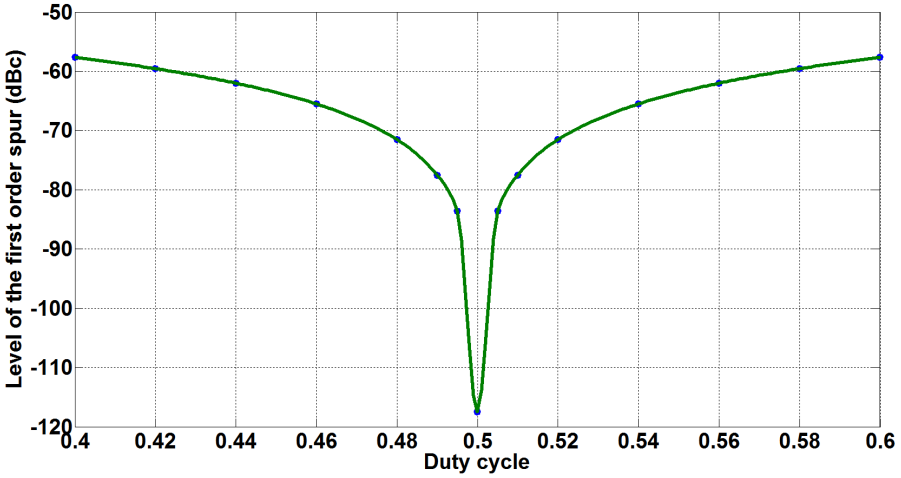


FIGURE 4.3: The level of spurs offset from the output frequency as a function of duty cycle error.

Using a MATLAB model for the synthesizer in Fig. 4.1, the level of spurs offset from the output frequency of 2.16GHz was expressed as a function of duty cycle error using (4.1) and is shown in Fig. 4.3. For these calculations, the same frequency synthesizer loop parameters as given in Chapter 3 were used.

In addition to generating high level spurs, as the number of multiplication stages increase to 4 or higher values, the functionality will be difficult to achieve because of irregular intermediate clocks. Furthermore, the frequency synthesizer in Fig. 4.1 will miss edges if the clock has a shape as given in Fig. 4.2(b) and this will cause locking problems.

As a corollary of the issues explained above, duty cycle correction becomes a necessity before the frequency doublers/quadruplers in order to eliminate the possibility of faulty operation or unwanted spurs at the output of the frequency generation block that follows these blocks.

4.3 Duty Cycle Correction approaches

DCC is used in many applications ranging from DLL outputs in SDRAMs for proper operation to High Speed IO Links for optimal eye opening [18]−[20]. The functionality of a DCC is to get a periodic clock signal and produce a periodic signal of the same frequency but with 50% duty cycle with acceptable tolerance. There are various approaches that correct the duty cycle of an incoming clock to 50%. The conventional method uses either a PLL or a DLL to generate double the input frequency, and using a divide-by-two circuit to generate a 50% duty cycle clock at the desired output frequency. This technique suffers from complexity, power consumption, phase noise degradation, and large area [21], [22].

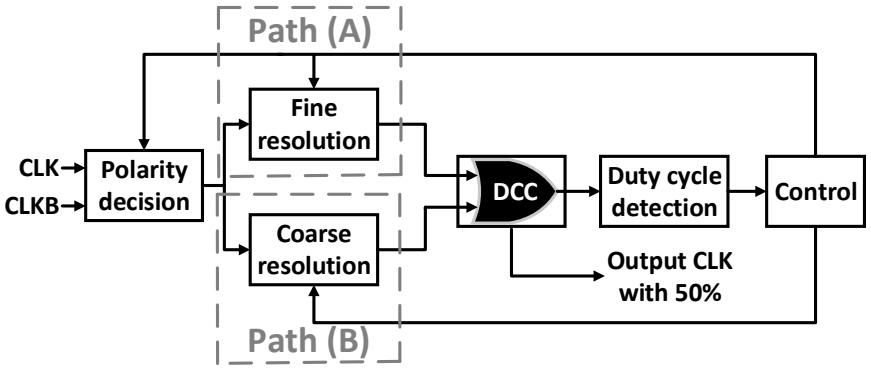


FIGURE 4.4: The proposed block diagram.

Another common approach delays one of the edges of the original clock to correct and generate a duty cycle of 50%. This technique finds the pulse width of the input clock and uses various controlled delay lines with Pulse Width Modulation (PWM) to provide a control signal that corrects the duty cycle [22]. The PWM can be implemented fully digital, fully analog, or as mixed signal. The digital PWM is superior to the analog one in simplicity, for faster lock, low power consumption, higher immunity to noise and higher stability. However, it suffers from limited delay resolution, limited frequency range operation and intrinsic jitter [22], [23]. For both methods, delaying clock edges is susceptible to supply noise. Especially, the frequency doubler/quadrupler will need both edges to work, the impact of the supply noise on the phase noise performance needs to be considered.

4.4 Proposed architecture overview

Fig. 4.4 shows the block diagram of the proposed solution and the flow chart in Fig. 4.5 explains the functionality of this design. The circuit first determines if the input clock already has a duty cycle of 50% or not, and if it does, clock is passed to the output without modifications. If the duty cycle is not 50%, the loop decides to pass the clock or the inverted clock depending on whether it has less or more than 50% duty cycle. Path (A) and path (B) delays edges to correct for the duty cycle error with fine and coarse resolution. First, path (B) delays one of the edges with coarse resolution towards 50% duty cycle. Once path (B) settles down, if finer resolution is needed, path (A) delays the other edge or the same edge. This fine resolution operation takes place only when path (B) fails to achieve the required duty cycle error and the loop stops when the output clock reaches this limit. Fig. 4.6 shows the proposed top level schematic.

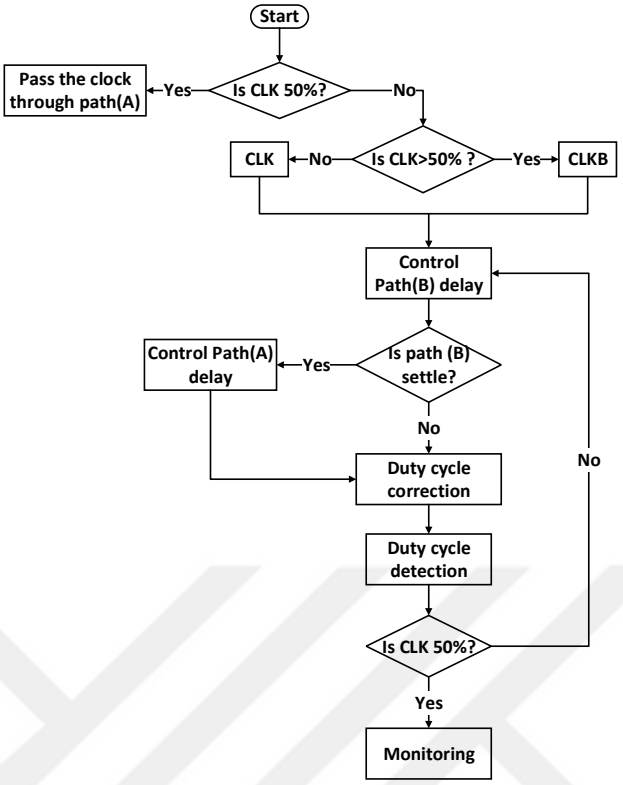


FIGURE 4.5: The proposed architecture's functionality.

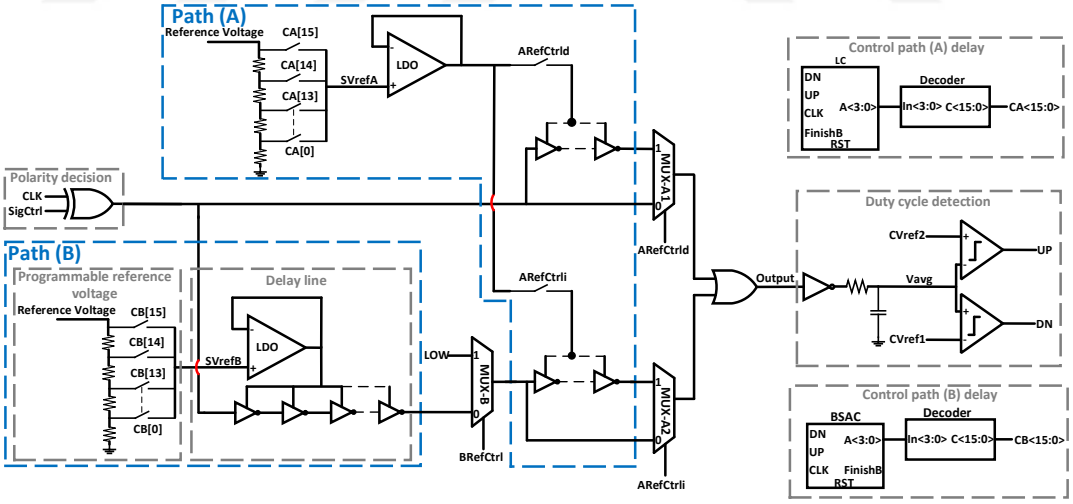


FIGURE 4.6: The proposed schematic.

4.4.1 Duty Cycle Detection

Duty cycle is detected at the output by passing the clock through a low pass filter to find the DC average of the clock signal and comparing this to two references close to VDD/2. The DC voltage "Vavg" in Fig. 4.6 indicates the duty cycle value. For instance,

if the DC value is equal to mid-supply, it means the duty cycle is 50%, which is shown in equation (4.2). Two comparators are used to compare this DC value to "CVref1" and "CVref2". Two reference voltages offset from the VDD/2 in positive and negative direction are used to create a dead-band and prevent undesirable oscillation between two values around 50%. This region limits the settling error to ±0.3%, but according to Fig. 4.3, this only causes a maximum spur level of -95dBc. Depending on the comparison results, the duty cycle detection block generates an "up" (Vavg < CVref2) or a "dn" (Vavg > CVref1) signal that goes into the up/down counters as shown in Fig. 4.6. These signals increase or decrease the delay on the lines accordingly.

$$DutyCycle = \frac{V_{avg}}{VDD} \cdot 100\%. \tag{4.2}$$

4.4.2 Polarity Decision

In the design, path (A) and path (B) outputs are ORed together to generate the output clock. This stretches the width of the pulse to increase the duty cycle, hence duty cycle can only be corrected up. When the input clock has more than 50% duty cycle, the clock needs to be inverted before passed into the DCC. Therefore, it is inverted using an XOR gate as shown in Fig. 4.6.

4.4.3 Delay Paths (A) & (B)

The two paths are used to delay the clock with fine and coarse resolutions to correct the duty cycle error. These delay lines consists of buffers, a LDO and a programmable reference voltage. The LDO for each path changes the buffers' supply voltage in order to get the required delay, by changing the reference voltages "SVrefA" and "SVrefB" that are generated by a programmable reference DAC. If the input duty cycle is 50%, path (A) passes the clock unchanged to the OR gate via MUX-A1, and path (B) passes "LOW" to the same OR gate. If the duty cycle is not 50%, path (B) delays the clock with coarse resolution to increase the duty cycle. If path (B) settles to the desired accuracy, path (A) passes the signal unchanged to the OR gate. If fine resolution is needed, path (A) increases or reduces the duty cycle by delaying the clock through the inverters controlled by "ARefCtrli" or "ARefCtrld", respectively. Path (A) uses less number of inverters than Path (B) to achieve eight times higher resolution.

4.4.4 Control Unit

The control unit takes in the "up" and "dn" from the duty cycle detection circuitry and generates the control bits "SigCtrl", "CA<0:15>", "CB<0:15>", "ARefCtrld", "ARefCtrli", "BRefCtrl" and "FinishB" to modify the delay cells to correct for duty cycle. The up/down counters and the decoders in Fig. 4.6 constitute the core of the control unit. The counter named BSAC in the figure implements a binary search algorithm to generate the bits "CB<0:15>". Use of this algorithm speeds up the iteration towards 50% duty cycle. Once path (B) settles down, "FinishB" signal is generated. This signal turns on the linear counter named LC to generate "CA<0:15>" bits. These two counters are used to program the reference voltages of a reference DAC that control the supply voltages for path (A) and path (B). "RefCtrld" and "RefCtrli" determine if path (A) should increase or reduce the duty cycle with fine resolution as explained above. Finally, the control bit "SigCtrl" sets the polarity of the input clock.

In the case of duty cycle disturbances, the control unit is also responsible for detecting and modifying the loop. If the maximum value of the programmable reference voltage is reached and an internal signal called "CNTR", which is a digital representation of "Vavg" to be within the required limits or not, is not triggered, the loop waits for 1200 cycles and if it does not leave the current state, control unit resets the whole loop. This prevents the case where the clock polarity is wrong and the loop settles to the maximum values and gets stuck there.

4.5 Simulation results

During initial start-up, a main reset pulse turns on the design and resets the control circuitry to no duty cycle correction settings. A second pulse is initiated after 624 cycles in order to give the duty cycle detection block enough time to settle. Following this, the loop starts working as explained above.

The circuit was simulated in Cadence Spectre across correctable input clock duty cycle range over Process, Voltage, and Temperature (PVT) variations with supply range of 1.2V±100mV and temperature range of -40°C to 125°C. The simulations were done with and without supply white noise model for identifying the impact of the supply noise.

4.5.1 DCC Functionality and analysis

Simulation results showed that the circuit is stable and locks to a state firmly with the desired output duty cycle accuracy. The circuit performance met the design targets with

a small tolerance. The settling time of the DCC loop can be divided into two parts. The first part consists of the time it takes the averaging filter to settle down to generate "Vavg", before the circuit starts to correct the duty cycle. This time can be estimated by (4.3).

$$T_{settled} = \begin{cases} -\tau \cdot \ln\left[1 - \frac{V_{avg}}{V_{ini}}\right], & DC < 50\% \\ \\ -\tau \cdot \ln\left[\frac{V_{avg}}{V_{ini}} - 1\right], & DC > 50\% \end{cases} \tag{4.3}$$

where V_{ini} is the initial voltage on the integrator capacitor and τ is the time constant of the (R.C). The second part of the settling time depends on how long the circuit needs to converge to 50% duty cycle. The counter input clock period plays the main role in determining this time. Worst case simulated settling time from cold-start for our design is 140us.

The input and output clock waveforms (voltage vs. time) are shown in Fig. 4.7. CLKIN waveform shows the input clock signal, while the CLKOP waveform shows the output clock signal. The simulation of the circuit with input duty cycle 40%, 60%, and 50% is shown in Fig. 4.7 , from top to bottom respectively. As a result of PVT simulation to show the design robustness, the worst case duty cycle settles to 49.82% after correction in all cases.

The case of duty cycle disturbance was simulated across PVT by changing the duty cycle from 52% to 48% and to 50% eventually. The results are shown in Fig. 4.8 . When the duty cycle changes from less than 50% to more than 50% or vice verse, the loop resets the state and starts from the beginning. The top graph in Fig. 4.8 shows the input duty cycle variations. The mid-graphs show "Vavg" settling in time after the disturbance occurs and it settles within the required limits in all cases. When the duty cycle of the input clock changes from 52% to 48%, a reset pulse is generated by the control unit to reset the loop. Finally, the output duty cycle value, which always settle to 50%±0.3%, is shown in the bottom graph.

According to the previous simulation results, the proposed duty cycle correction technique is able to correct the duty cycle error across PVT variations. Additionally, Monte Carlo simulations of the comparators in the duty cycle detection circuit for random mismatch across temperature shows a standard deviation of 1.6mV, which corresponds to ±0.133% duty cycle error. This error adds to the overall resolution of the duty cycle correction.

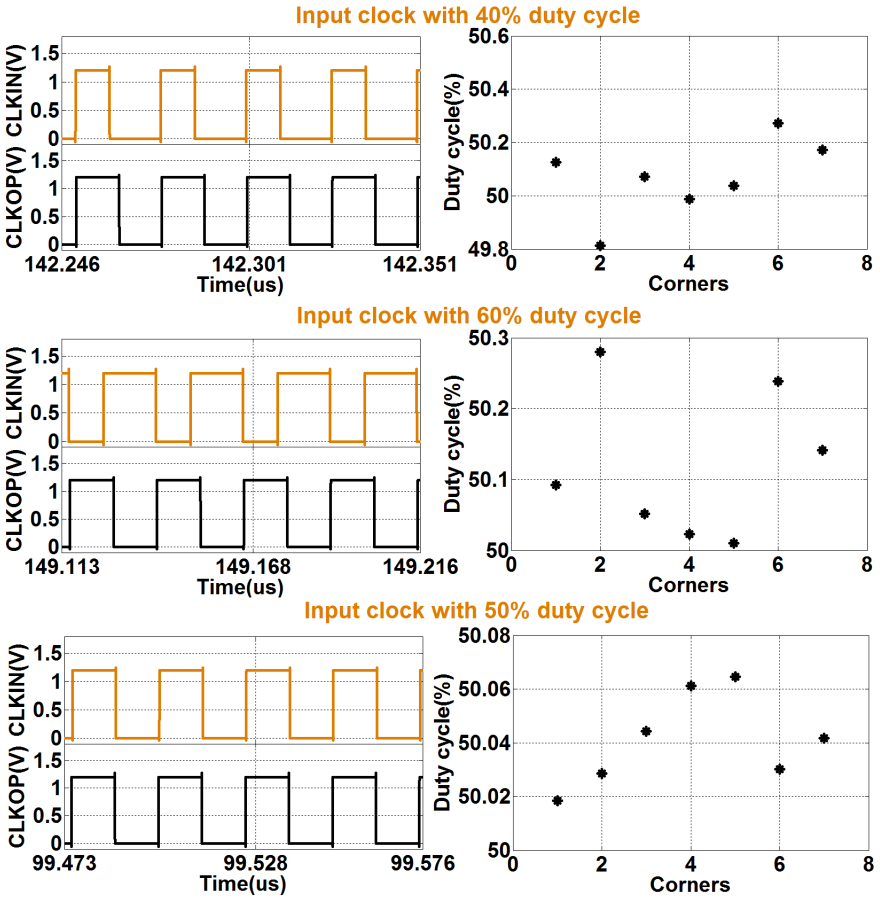


FIGURE 4.7: Proposed DCC circuit simulation results for the case with the input clock (CLKIN) having different input duty cycles: 40%, 60%, and 50%.

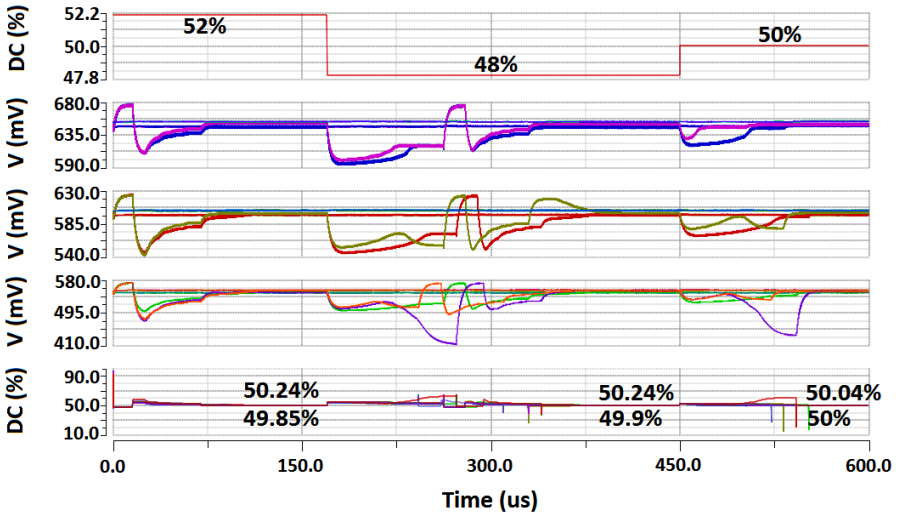


FIGURE 4.8: DCC circuit simulation results showing input clock (CLKIN) duty cycle disturbances, going from 52% to 48% and to 50% eventually.

4.5.2 Phase noise (PN) and jitter analysis

Path (B) is the main contributor of phase noise and jitter. Noise mostly comes from the delay cell that is made up of cascade of buffers for delaying the clock and the controlled supply from the LDO. Since path (A) has a small delay compared to path (B), its contribution to overall phase noise can be neglected when compared to path (B). Furthermore, the remaining digital cells, which work only during the correction period has negligible or no contribution to phase noise.

Noise voltage variations at the output of an inverter is converted to time error during the state transition, which can be seen as jitter [24]. Jitter in inverters can be expressed as the sum of three major components as shown in (4.4) [24].

$$\frac{\overline{\Delta_{td}^2}}{\Delta f} = \frac{\overline{i_{ch}^2} + \overline{i_{Rds}^2}}{(\omega I_L)^2} + \overline{v_{ng}^2}\left(\frac{g_{m,sat+\omega 2C_M}}{\omega I_L}\right)^2 + \overline{v_{sn}^2}\left(\frac{C_{j,t}}{I_L}\right)^2. \tag{4.4}$$

The first part in the above equation represents the generated jitter by the channel noise current source (i_{ch}) and the parasitic resistance thermal noise source (i_{Rds}) from each inverter. When we consider the case of a delay line with a cascade of inverters, other noise sources exist as shown in [24]. These can be given as: 1) Noise amplification by the inverters' transconductance ($g_{m,sat}$); 2) Miller capacitance effect ($2C_M$), which couples the noise from input to output; 3) Parasitic junction capacitances ($C_{j,t}$), which couple noise from supply to output. These mentioned effects are shown in (4.4) with the second and third terms, which are functions of the gate voltage noise (v_{ng}) and the supply noise (v_{sn}) ,respectively.

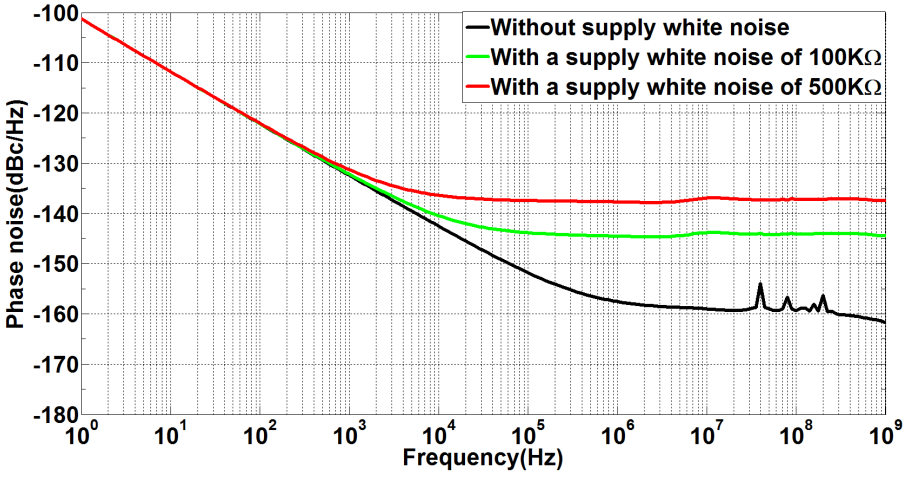


FIGURE 4.9: Phase noise simulation results for the case without supply white noise (black line) and with supply white noise (green and red lines) at duty cycle error 48%.

Phase noise and jitter tests are important to verify the impact of DCC on frequency synthesizers. Spectre simulations show that the phase noise without supply noise is estimated to be -157.6dBc/Hz at 1MHz offset frequency as shown in Fig. 4.9 (black line), and the RMS phase jitter (from 10KHz to 10MHz) is 224fs.

A 2-stage differential input-single ended output LDO was simulated for output white noise. Without any supply noise filters at the output, the white noise floor is -154.7 dBV/$\sqrt{\text{Hz}}$, which corresponds to the noise of a 20KΩ resistor. In order to also consider the noise coupled from other sources and worst case scenario, we have simulated our circuit with the white noise of 100KΩ resistor injected onto the supply. Simulated phase noise for this setting is -144.6dBc/Hz at 1MHz offset frequency as shown in Fig. 4.9 (green line), and the RMS phase jitter is 1.08ps. Even when supply white noise is modeled as the white noise of a 500KΩ resistor generating thermal noise, the simulated phase noise is -137.7dBc/Hz at 1MHz offset frequency as shown in Fig. 4.9 (red line), and the RMS phase jitter is 2.38ps. Furthermore, MATLAB simulations of the same frequency synthesizer loop parameters as mentioned in Chapter 3 were run to see the effect of DCC jitter on the overall jitter performance of a synthesizer. The integrated RMS phase jitter from 10KHz to 10MHz without DCC and reference frequency at 40MHz (with different loop filter components and division ratio) is 795fs. If we use a doubler with DCC to double the reference frequency of the synthesizer, the integrated RMS phase jitter on the same bandwidth with supply noise model using 100KΩ is 520fs. This result shows an obvious advantage of using a doubler to increase the reference frequency and the contribution of DCC and doubler phase noise is minimal. Finally, Table 4.1 summarizes the proposed design performance.

Table 4.1: Performance Summary

Technology	UMC 65nm
Supply	1.2V
XO frequency	40MHz
Input duty cycle error	40%-60%
Output duty cycle error	50%±0.3%
RMS jitter (w/o supply white noise)	224fs
Current consumption	0.26mA

4.6 Conclusion

In this chapter, a mixed signal duty cycle correction mechanism is presented. The design corrects input duty cycle variations from 40% to 60% by using coarse and fine resolution

delay lines. Furthermore, we have analyzed the spur generation as a function of duty cycle error, and the impact of duty cycle correction on the overall phase noise. The circuit is implemented in 65nm UMC CMOS process. Operating from 1.2-V supply, the circuit only dissipates 0.26mA.

Chapter 5

Frequency Multiplier

5.1 Introduction

A low jitter frequency multiplier, which requires far less power, area, and design complexity than reference multiplying PLL or DLL circuits can be used to generate the reference frequency for a low phase noise frequency synthesizer. This chapter proposes a mixed signal solution based on the fact that the average DC value of a signal is proportional to its duty cycle. The solution uses a feedback loop with coarse and fine delay resolution to generate a 90^o phase shifted clock that is used to produce a doubled frequency signal with 50% duty cycle. This method can be used to multiply the input frequency of 40MHz by multiples of 2 up to 16.

The performance of the integrated frequency synthesizers relies on a clean fixed reference frequency, which is usually derived from a crystal oscillator (XO). Due to the stringent phase noise requirements of the high performance frequency synthesizers, multiples of the crystal oscillator frequencies are usually required to provide different frequencies at the input [25], [26]. Unfortunately, the commercial low cost crystal oscillators are limited in the frequency range. Therefore, the ability of multiplying a fixed reference frequency while preserving the phase noise requirements becomes desirable. PLLs allow multiplication of reference frequencies to produce different operating frequencies. However, this approach is sometimes overkill for some applications, especially if the input frequency needs only to be doubled. For those applications, a simpler doubler would be better to double the frequency.

5.2 Reference multiplication benefits

Increasing the reference clock frequency of a fractional-N frequency synthesizer is an effective way of improving the overall phase noise. A top level block diagram of a frequency synthesizer with a reference multiplication is shown in Fig. 4.1. According to the analysis done in Chapter 3 through equations (3.31)-(3.38), it is evident that the reference multiplication results in a lower feedback divider ratio, which in turns reduce the magnitude of the in-band transfer function for reference oscillator, charge pump and feedback divider. Ideally, reducing N by factor of 2, gains 6dB phase noise improvement at the output of the frequency synthesizer. Practically, PFD/CP tends to generate more noise as the comparison frequency increases. A practical model has been proposed in [27] and states that the PFD noise deteriorates in conformity with $10log(F_{comp})$. Consequently, the total in-band phase noise is improved by 3dB as shown in equation (5.1), in which 1Hz normalized phase noise is used to predict the PLL in-band phase noise.

$$PLL_{noise(in-band)} = PN1Hz + 10log(F_{comp}) + 20log(N). \tag{5.1}$$

On the other hand, the VCO and Sigma Delta contribute the most in the out-of-band phase noise. Generally, a strenuous trade-off between the in-band and out-band phase noise limits the improvement in the overall phase noise profile of a frequency synthesizer. However, the reference multiplication helps in improving the high frequency phase noise as well. Equation (3.39) shows that the SD quantization noise is shaped by the OSR. As a result of doubling the reference frequency, the SD phase noise is improved by about 18dB in a 3^{rd} order SDM at the same frequency offset. Finally, it enables higher loop bandwidth, which results in more rejection of VCO phase noise [16],[28].

5.3 Frequency multiplier approaches

Despite the fact that the cascaded architecture of an injection locked integer-N PLL or multiplying DLL reference multiplier, with an LC fractional-N PLL achieves overall phase noise improvement. This architecture suffers from design complexity which comes from the reference injection process. This process is very sensitive to PVT, therefore achieving the required low phase noise and spur levels can not be obtained easily [25]-[29]. Furthermore, this method is not suitable for low power or compact area applications. Without injection process, the architecture has less sensitivity to PVT but worse phase noise performance. In short, designing two PLL is not a simple task which is always suffer from complexity, high power consumption and large area.

In [17],[30],[31], a very simple reference doubler scheme is introduced. This method can achieve less power consumption, smaller area and less design complexity than other architectures. However, increasing the reference multiplication factor to higher than two, faces many difficulties. The non-50% input duty cycle clock to the next multiplication stage leads to faulty functionality as depicted in Fig. 4.3. Furthermore, the jitter accumulation becomes higher with the increased number of stages.

In [16], a differential XO is used to achieve reference multiplication with less power consumption, area and design complexity than the injection method. However, the power consumption is higher and occupies larger area than the simple method introduced in [17],[30],[31]. Even though the differential XO has many advantages such as better phase noise performance than the single ended, it has higher cost.

5.4 Proposed architecture

5.4.1 Reference multiplication

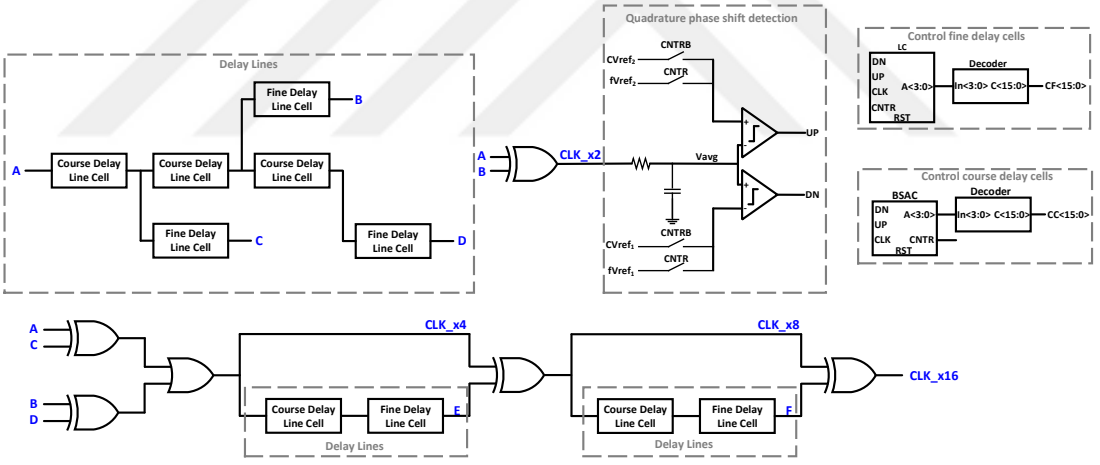


FIGURE 5.1: The proposed schematic.

Reference multiplication is achieved by generating multiple signals with different phases from a stable reference signal using a feedback loop. The proposed circuit starts by determining the optimum delay for the 90^o phase shift of signal (B). This optimum delay is the key for achieving the multiplication, where as the other phases of the signals (C), (D), (E) and (F) are obtained by the delay lines directly.

Instead of shifting the doubler's output (CLK_x2) by 90^o phase shift again to obtain the quadrupler operation, four signals (A), (C), (B) and (D) can do the same job by XORing different phases of 0, 45, 90 and 135^o as shown in Fig. 5.2. For instance,

the required delay for 45^o phase shift signal (C) is obtained by the half delay amount determined for the 90^o phase shift signal (B). Consequently, the delay lines are designed to be automatically adjusted to obtain the required delays for the other phases of the signals (C), (D), (E) and (F). The delay equations are summarized as below.

$$T_{delay}|_C = \frac{T_{delay}|_B}{2} \tag{5.2}$$

$$T_{delay}|_D = \frac{3}{2} T_{delay}|_B. \tag{5.3}$$

Similarly, CLK_x8 can be generated by delaying CLK_x4 by

$$T_{delay}|_E = \frac{T_{delay}|_B}{4}. \tag{5.4}$$

Finally, CLK_x16 is generated by delaying CLK_x8 by

$$T_{delay}|_F = \frac{T_{delay}|_B}{8}. \tag{5.5}$$

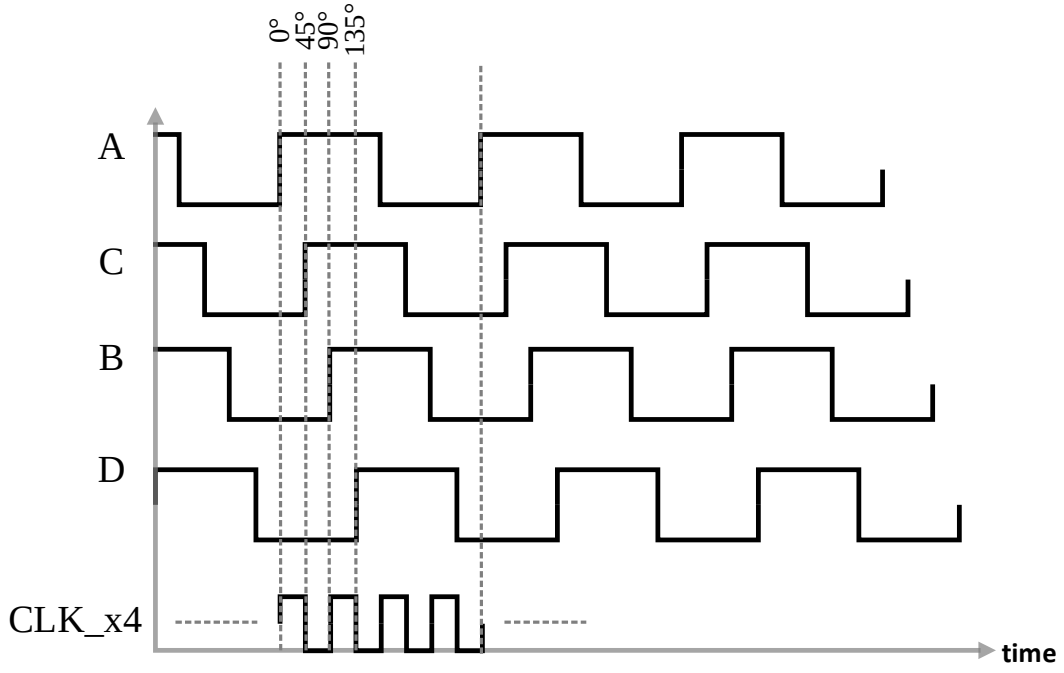


FIGURE 5.2: Summary of the proposed idea.

5.4.2 Quadrature phase shift detection

A 90^o phase shift is detected at the output (CLK_x2) by passing the XORed clock through a low pass filter to find the DC average of the clock signal and comparing this to two references close to VDD/2 as shown in Fig. 5.1. The DC voltage "Vavg" in Fig. 5.1 indicates the output duty cycle value which corresponds to the phase difference between the XO clock (A) and the 90^o phase shift signal (B). For instance, if the DC value is equal to mid-supply, it means the duty cycle is 50% and the phase difference is 90^o as shown in equation (5.6). Two comparators are used to compare this DC value to ("CVref1", "fVref1") and ("CVref2", "fVref2"). Two reference voltages offset from the VDD/2 in positive and negative direction are used to create a dead-band and prevent undesirable oscillation between two values around 50%. This region limits the settling error to ±0.2%. Depending on the comparison results, the quadrature phase shift detection block generates an "up" (Vavg < (CVref2, fVref2)) or a "dn" (Vavg > (CVref1, fVref1)) signal that goes into the up/down counters as shown in Fig.5.1. These signals increase or decrease the delay on the lines accordingly.

$$DutyCycle = \frac{V_{avg}}{VDD} \cdot 100\% = \begin{cases} \frac{\phi_B - \phi_A}{\pi} \cdot 100\%, & (\phi_B - \phi_A) < \pi \\ \frac{\phi_B - \phi_A}{2\pi} \cdot 100\%, & (\phi_B - \phi_A) > \pi \end{cases} \tag{5.6}$$

5.4.3 Control unit

The control unit takes in the "up" and "dn" from the quadrature phase shift detection circuitry and generates the control bits "CC<0:15>", "CF<0:15>" and "CNTR" to modify the delay cells. The up/down counters and the decoders in Fig. 5.1 constitute the core of the control unit. The counter named BSAC in the figure implements a binary search algorithm to generate the bits "CC<0:15>". Use of this algorithm speeds up the iteration towards 90^o phase shift. Once course delay settles down, "CNTR" signal is generated. This signal turns on the linear counter named LC to generate "CA<0:15>" bits. These two counters are used to program the coarse and fine resolution delay lines. Furthermore, this control bit sets the two reference voltage levels for the quadrature phase shift detection block. When "CNTR" is LOW, a wide dead region is used to speed up the settling ("CVref1", "CVref2"). Otherwise, the dead region is tight for the fine resolution process ("fVref1", "fVref2"). In the case of any disturbances after the loop settles, the control unit is also responsible for detecting and modifying the loop. If the maximum value of the programmable delay lines are reached and an internal signal called "DVavg", which is a digital representation of "Vavg" to be within the required limits or not, is not triggered, the loop waits for 1400 cycles and if it does not leave the current state, control unit resets the whole loop.

5.4.4 Delay lines

Delay lines are used to delay the clock with coarse and fine resolution to correct for quadrature phase shift. Both coarse and fine resolution delay cells consist of tri-state buffers as shown in Fig. 5.3. Fine delay line uses less number of delay stages than coarse delay line to achieve higher resolution. The control unit as explained above determines the required delay for optimum quadrature phase shift. According to this decision, the required delay for each clock multiplication factor is adjusted automatically by the delay lines, which are designed to follow the delay equations as explained above.

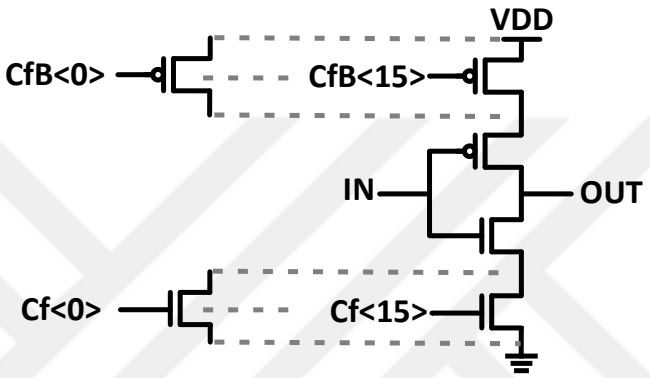


FIGURE 5.3: Example of delay cell in the fine resolution delay line

5.4.5 Analysis of the non-ideal effects

Firstly, the functionality of the frequency multiplier might not work properly if the input duty cycle is not close to 50% as explained in Chapter 3. This input duty cycle requirement is not only at the input of the system, but also for each clock multiplication stage. However, this issue is resolved by introducing the feedback loop in the proposed architecture, which is maintaining the 90^o phase shift and the automatic adjustment of the delay lines.

Secondly, the imprecise delay between the required signals that produce the multiplied clocks causes a frequency and duty cycle error at the frequency multiplier output. As a consequence of this error, spurious tones are generated at the frequency synthesizer output. These spurs are different from the one discussed in Chapter 3, because they are generated from a periodic error which accumulates from one multiplication stage to another. Fig. 5.4 shows the impact of this error on the frequency domain of a periodic square wave. For instance, if f_o is CLK_x2, which is 80MHz, the output spectrum in the ideal case has harmonics of nf_o, where n is an odd number. In the actual case, the output spectrum has the same harmonics of an ideal case besides an intermediate harmonics of

120MHz, 160MHz and 200MHz. These harmonics correspond to reference spurs at the frequency synthesizer output, in which their magnitude are directly proportional to the error value. Therefore, this error should be minimized as much as possible as shown in the simulation result section. Since the PLL has a limited bandwidth, the spurs at high frequencies are attenuated efficiently as discussed in Chapter 2 and Chapter 3. As a result, if the error is small and the spurs are at high frequencies, the impact of these spurs on the overall performance is negligible.

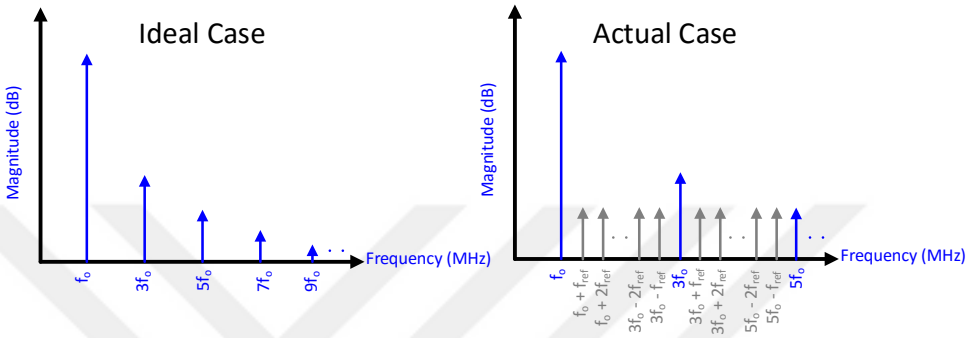


FIGURE 5.4: The impact of the non-ideal multiplication.

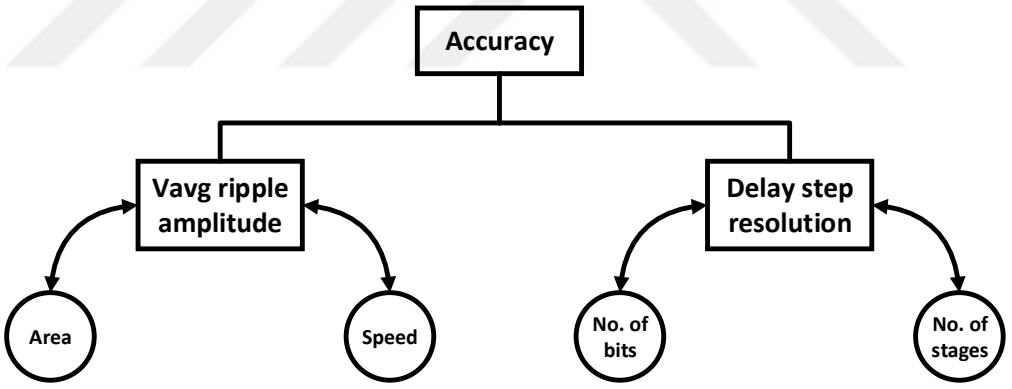


FIGURE 5.5: The output accuracy limitations.

Thirdly, the output accuracy is determined by the delay step resolution and the low pass filter output ripples as illustrated in Fig. 5.5. The delay step resolution can be improved by increasing the control bits and decreasing the delay step. In this design, the 16-steps for each the coarse and fine resolution delay lines were enough and any extra improvement in the delay step is useless, because "Vavg" ripples will be larger than the dead region. In order to achieve better accuracy, the ripples should get more attenuation by increasing the low pass filter time constant. On the other hand, this enlarges the occupied area and lowers the operational speed.

The settling time of the frequency multiplier loop is divided into two parts. The first part consists of the required time of the averaging filter to settle down to generate "Vavg". This time is estimated by

$$T_{settled} = \tau \cdot \ln|1 - \frac{V_{avg}}{V_{ini}}| \tag{5.7}$$

where V_{ini} is the initial voltage on the integrator capacitor and τ is the time constant of the (R.C). The second part of the settling time depends on how long the circuit needs to converge to the correct delay amount. The counter input clock period plays the main role in determining this time and it has to wait the low pass filter output to settle in order to give a correct decision. Consequently, this time is directly proportional to the low pass filter (R.C) time constant. Worst case simulated settling time from cold-start for our design is 130us.

5.5 Simulation Results

5.5.1 Frequency multiplier functionality

Simulation results are given for typical conditions, T=85^{o}C and VDD=1.2V. Fig. 5.6 illustrates that the circuit is stable and locks to a state firmly. Fig. 5.7 shows the input clock waveform (A), the 90^o phase shifted signal (B), CLK_x2 (80MHz), CLK_x4 (160MHz), CLK_x8 (320MHz) and CLK_x16 (640MHz). Fig. 5.8 shows the output frequency, duty cycle and the error values. It is obvious that the error is changing periodically around the desired value and its peak value increases as the multiplication factor increases. The output clocks are represented by the frequency domain as shown in Fig. 5.9 in order to quantify the error impact on the performance. As explained above, the third harmonic will be attenuated by the PLL bandwidth because it is at high frequency. For the actual cases, the high frequencies harmonics will be attenuated in the same manner as the third harmonic. However, the close harmonic to the fundamental frequency such as the case of CLK_x2, the harmonic at f =120MHz might cause a spur at the output. However, it is evident from the figure that those harmonics have much less magnitude than the fundamental frequency, hence their impact is negligible.

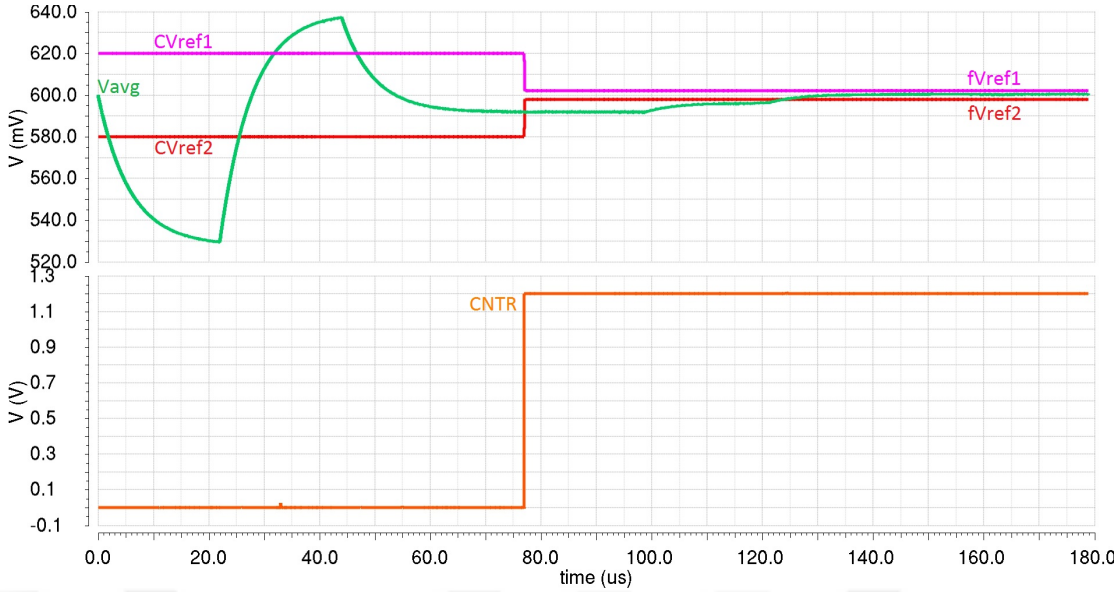


FIGURE 5.6: The simulation result of the settling behaviour.

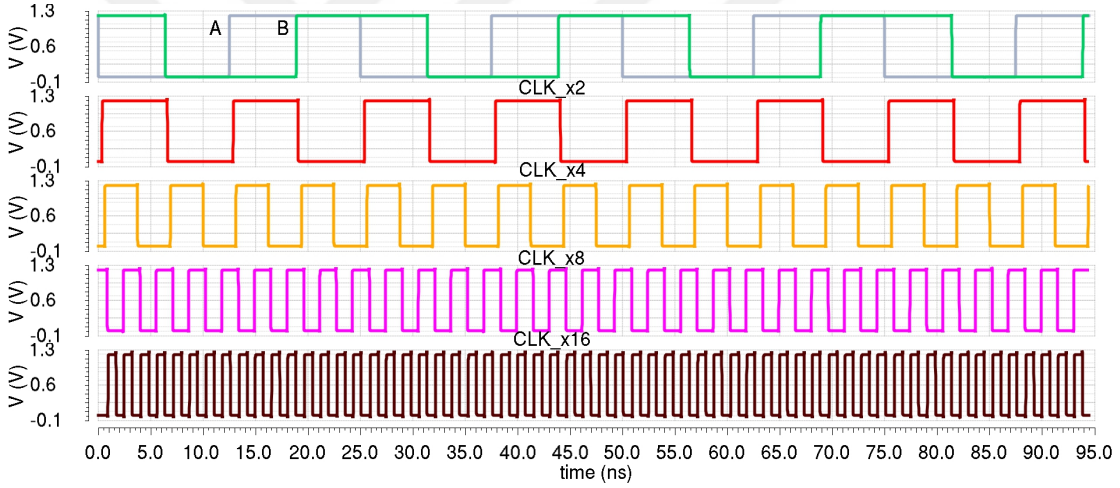


FIGURE 5.7: Transient simulation showing the input clock (A), 90^o phase shifted clock (B) and the output clocks.

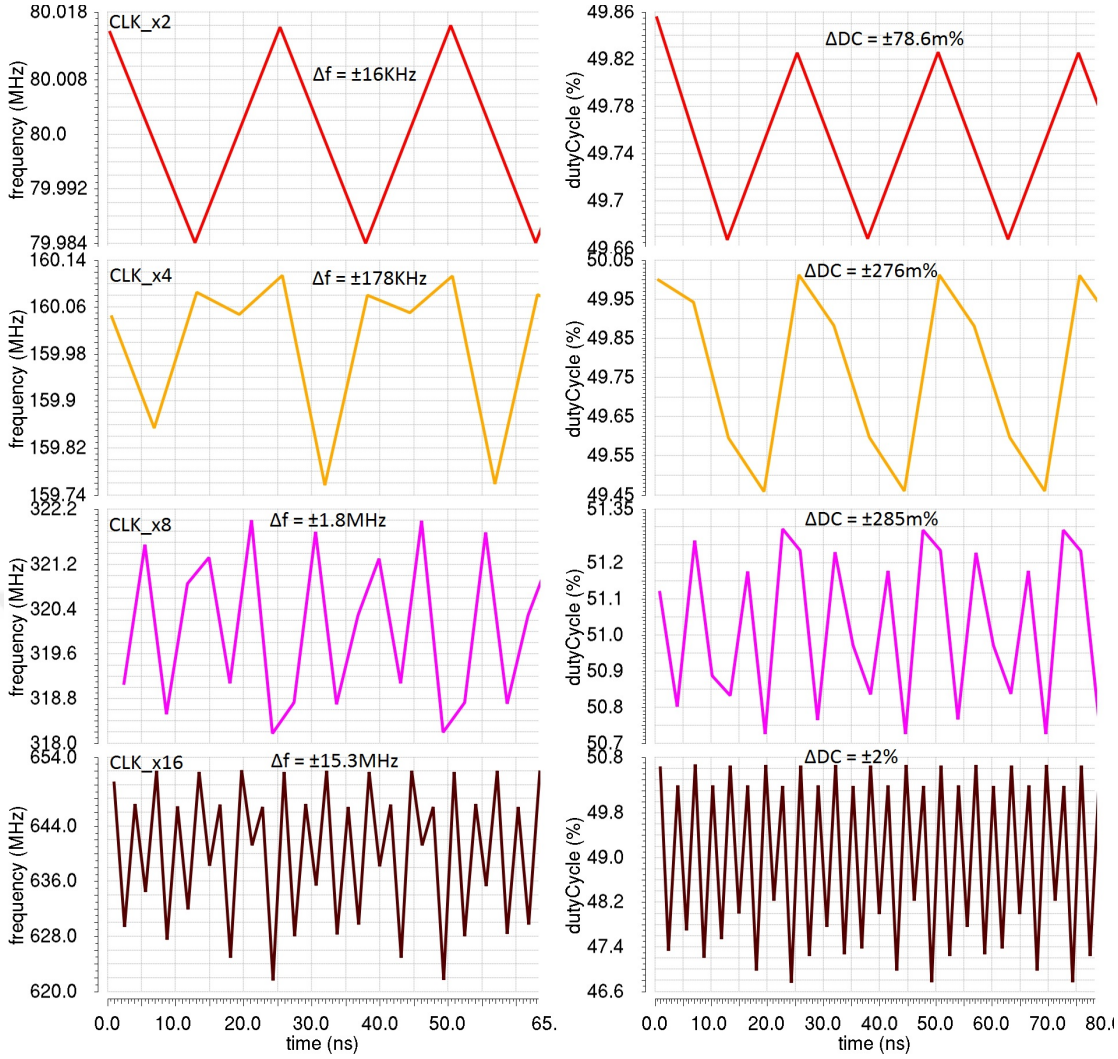


FIGURE 5.8: Output frequencies and duty cycles.

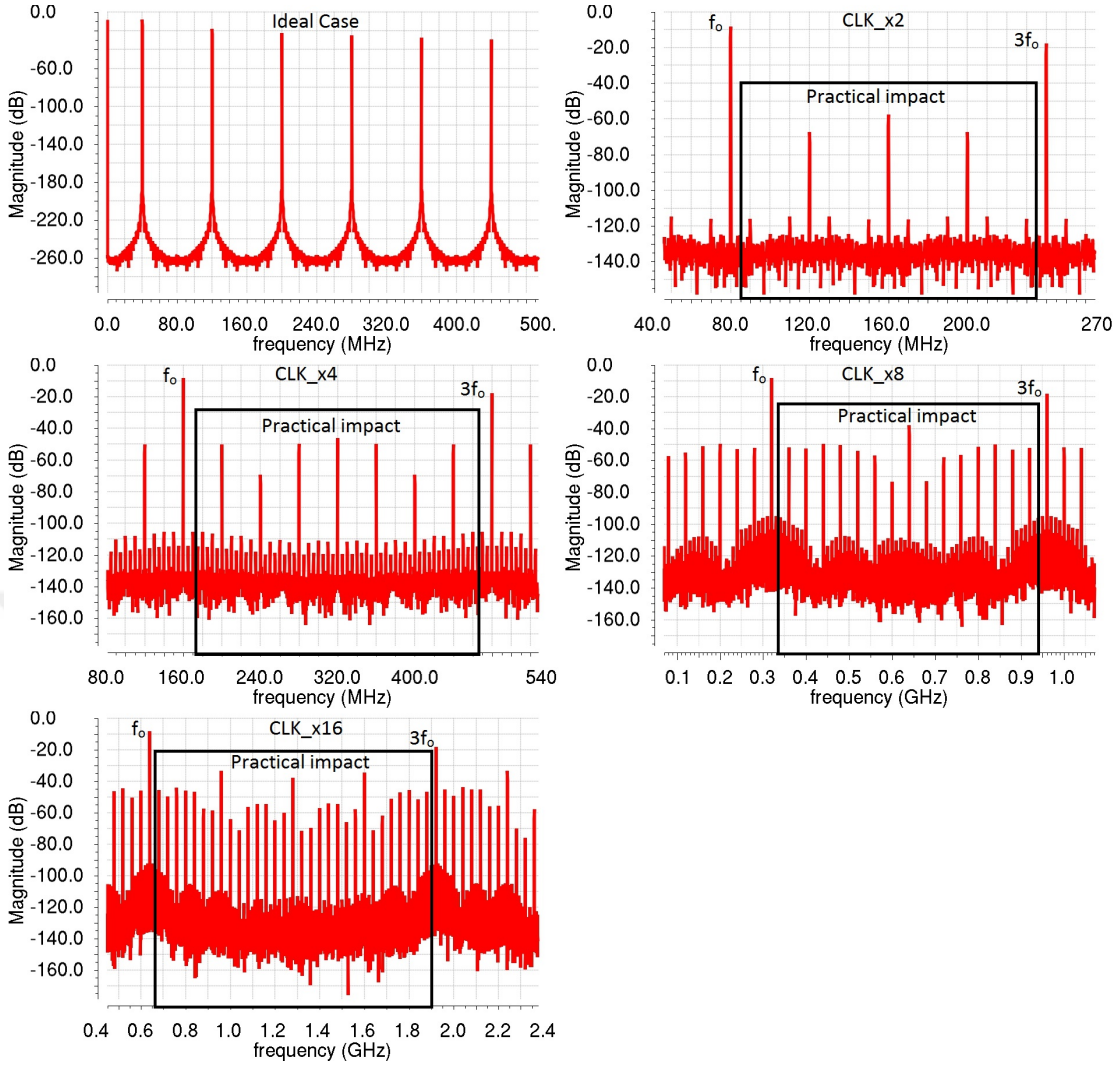


FIGURE 5.9: The frequency domain of an ideal reference clock and the actual output frequencies.

5.5.2 Phase noise and jitter analysis

Noise mostly comes from the delay cells that is made up of cascade of gates for delaying the clock. Since fine delay cell has a small total delay compared to coarse delay cell, its contribution to overall phase noise can be neglected. Furthermore, the remaining digital cells, which work only during the correction period ,has negligible or no contribution to phase noise. Fig. 5.10 shows the simulated phase noise at CLK_x2 (80MHz) and CLK_x16 (640MHz), indicating the phase noise value at 1MHz offset frequency and the thermal noise.

The same frequency synthesizer loop parameters (with different loop filter components and division ratio) as mentioned in Chapter 3 were run to see the effect of the frequency multiplier phase noise on the overall jitter performance of the frequency synthesizer.

When CLK_x16 is the reference frequency, the integrated RMS phase jitter from 10KHz to 10MHz is 246fs. Referring to the jitter values mentioned in Chapter 4 at 40MHz (795fs) and 80MHz (520fs) reference frequencies, the overall frequency synthesizer phase noise performance has improved by using CLK_x16 as a reference frequency.

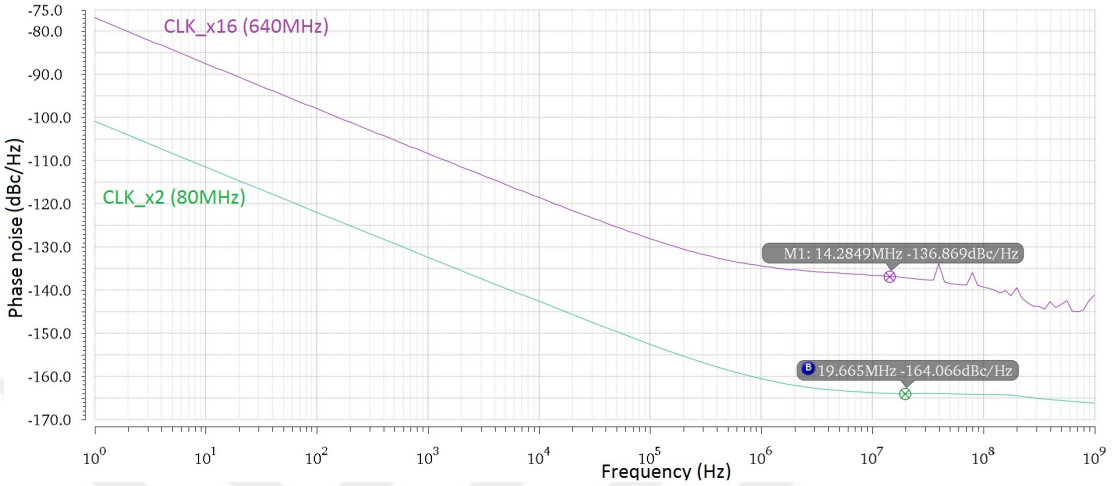


FIGURE 5.10: The simulated phase noise at CLK_x2 and CLK_x16.

5.6 Conclusion

In this chapter, a mixed signal frequency multiplication mechanism is presented. The design can multiply the input reference frequency (40MHz) by a multiple of 2 up to 16 by using a feedback loop to adjust the delay lines. Furthermore, we have analyzed the accuracy-speed trade-off and the effects of non-idealities on the spurs generation. The circuit is implemented in 65nm UMC CMOS process. Operating from 1.2-V supply, the circuit dissipates 0.46mA to 1.2mA at output frequencies 80MHz to 640MHz.

Chapter 6

Voltage Controlled Oscillator

6.1 Introduction

Voltage Controlled Oscillators are widely used in many applications ranging from function generators to frequency synthesizers. In this work, VCO is designed for frequency synthesizer to provide a stable local oscillator signal to RF transceiver. In frequency synthesizers, LO signals are generated for frequency up-conversion in transmitter and for frequency down-conversion in receiver.

The VCO output is a periodic signal (mostly a sinusoidal wave or a square wave) and its frequency is controlled by the input voltage. The operation of the VCO depends fundamentally on the non-linearity of the circuit elements. However, the VCO -as a system- can be assumed linear with an input control voltage and the output is a frequency as shown in Fig. 6.1. Recalling the linear transfer function from Chapter 3, the VCO linear transfer function is given by

$$H(s) = \frac{K_{vco}}{s}. \tag{6.1}$$

The output frequency is given by

$$\omega_{out} = \omega_o + K_{VCO} V_{in}. \tag{6.2}$$

Where,
K_{vco}: The VCO gain.
V_{in}: The input control Voltage.

ω_o: The free running angular frequency.

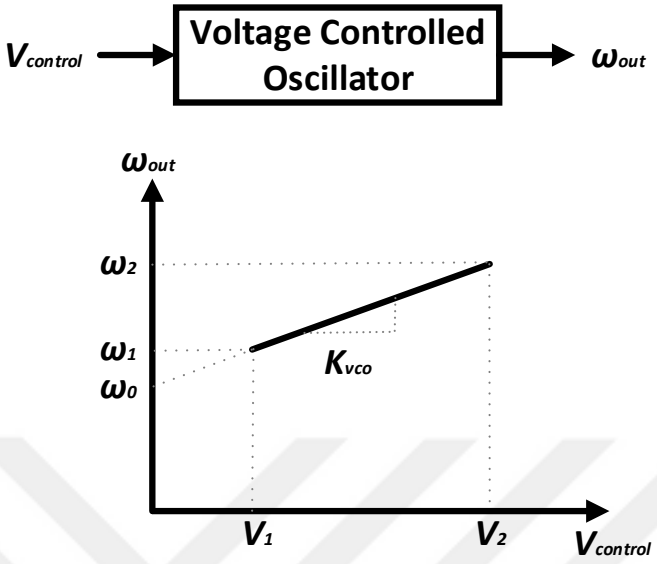


FIGURE 6.1: Linear model of VCO.

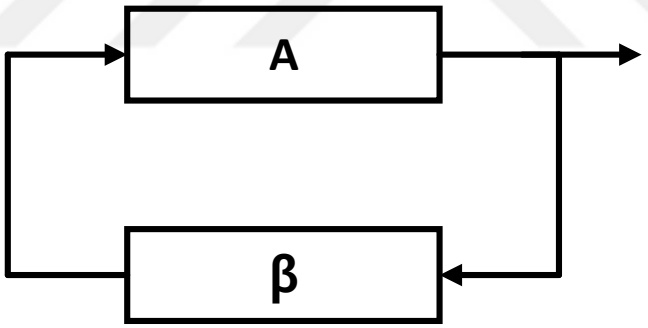


FIGURE 6.2: Simple feedback model.

The oscillator's principle of operation is based on positive feedback loop to amplify the noise and produce a periodic signal at a certain frequency. The Barkhausen stability criterion determines the oscillation condition for an electronic circuit. Consider a simple feedback model as shown in Fig 6.2, where "$A(j\omega)$" is the forward gain of the circuit and "$\beta(j\omega)$" is the transfer function of the feedback path, then the loop gain as per Barkhausen criterion is given by "βA". The circuit sustains steady-state oscillations only at frequencies for which:

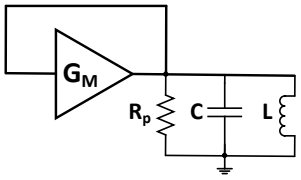
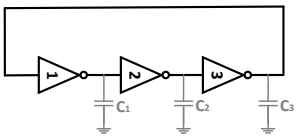
1. The absolute magnitude of the loop gain is equal to unity, that is $|\beta A| = 1$.

2. A positive feedback is required, which means that the phase shift around the loop should equal to 2πn; n= 0, 1, 2, so on.

6.2 Types of oscillators

Generally, there are two main types of on-chip VCOs; Ring and LC-based oscillators. Ring oscillators consist of delay stages with which the frequency of oscillation is adjusted. Usually, they have wide tuning range and compact area. However, the operating frequency is highly sensitive to PVT variations due to its dependence on RC delays. Furthermore, ring oscillators have large numbers of active elements, therefore more noise is injected, which results in poor phase noise performance. LC-based oscillators consist of a frequency selective circuit (LC tank), which determines the oscillation frequency combined with an active circuit to compensate for the tank losses. They have narrower tuning range and occupy larger chip area due to the spiral inductors. Nevertheless, they operate at higher frequency with less power consumption compared to ring oscillators. As a role of thumb, LC-based VCOs have better phase noise performance and their output frequencies are more stable across PVT variations. Table 6.1 summarizes the differences between LC-based and Ring oscillators.

Table 6.1: Comparison between LC-based and Ring oscillators

Parameter	**LC Oscillator**	**Ring Oscillator**
Output frequency	GHz range	MHz-GHz range
Phase noise	good (due to selectivity)	poor
Power consumption	High	Moderate (few mA's)
Tuning range	Acceptable	Wide
Area on chip	Large	Small
Applications	RF VCO's 	Digital applications (clock) 

Ring oscillators are tuned by varying the current consumption of the delay stages in order to change the charging time. The oscillation frequency is given by

$$F_{osc} = \frac{1}{2NT_d} \tag{6.3}$$

where ‘‘N’’ is the number of the delay stages used (must be odd in order to guarantee the oscillation phase condition or it can be even for differential stages) and ‘‘T_d’’ is the time required to charge and discharge one stage.

On the other hand, LC oscillators are tuned by either varying the inductance (it depends on the geometry, which is almost impossible for the on-chip inductors) or varying the capacitor (it is achieved by varactors). The oscillation frequency is given by

$$\omega_{osc} = \frac{1}{\sqrt{LC}} \tag{6.4}$$

where ‘‘L’’ is the inductor value and ‘‘C’’ is the total capacitance seen by the inductor.

6.3 LC-based VCO oscillators and topologies

6.3.1 One port concept

The one-port model treats the oscillator as two one-port networks connected together. Suppose we have a simple tank circuit along with its parasitic resistance ‘‘R_p’’ as depicted in Fig 6.3. This tank is used to resonate the inductor with a capacitor to maximize the loop gain and oscillate at a certain frequency. Unfortunately, the inductor and capacitor introduce losses due to their finite Quality Factors. Consequently, there never can be a steady state oscillation and any ringing dies after awhile, due to the losses in the resistors. This necessitates the use of an active circuit to compensate for these losses, in the form of a positive feedback to create a negative resistance and sustain the oscillation. The equivalent resistance seen by the tank circuit in this case is evaluated by equation (6.5).

$$R_{eqv} = \frac{-R_a R_p}{R_p - R_a} \tag{6.5}$$

such that;
R_p : Parallel resistance of a coil ($R_p \approx Q^2 R_s$).
R_a : Resistance of the active circuit ($R_a = \frac{-2}{g_m}$).

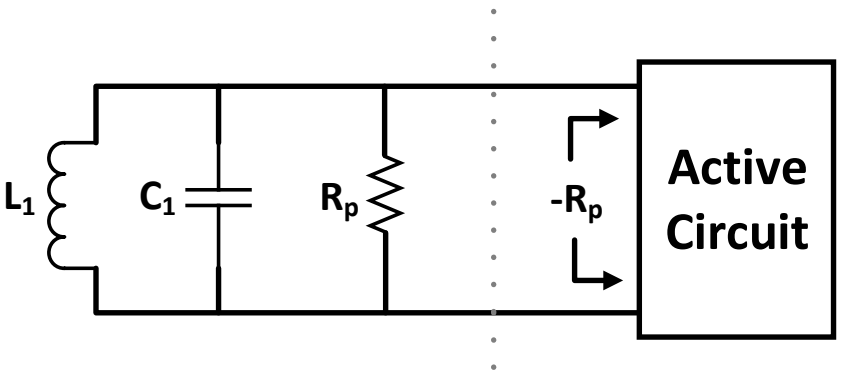


FIGURE 6.3: Cancellation of tank circuit losses by negative resistance.

Finally, the required loop gain for starting up an oscillation is $g_m R_p > 1$. The implication is to have R_p larger than R_a for building up the signal until it reaches steady state, R_p becomes equal to R_a eventually in the steady state.

6.3.2 Topologies

1. **Colpitt oscillator topology (Fig. 6.4(a))**: Colpitt oscillator requires higher gain than the cross coupled structure to start-up the oscillation. Furthermore, it has a single ended output, hence no common mode noise rejection [11],[32].

2. **Complementary MOS (CMOS) oscillator topology (NMOS + PMOS) (Fig. 6.4(b))**: In CMOS oscillator, the loop gain is higher than NMOS only or PMOS only topologies, hence it is good for building up an oscillation. Furthermore, it has better phase noise performance in the current limited region (region at which the output amplitude increases with increasing the current consumption). This is because of the double transconductance (g_m) compared to NMOS only or PMOS only topologies in this region as depicted in Fig 6.5.

   However, CMOS phase noise performance is worse in the voltage limited region (region at which the output amplitude is approximately constant and not affected by increasing the current consumption). In this region, a CMOS oscillator swing suffers from tighter headroom and the maximum output amplitude is the supply voltage (VDDA). Thus, it is commonly used in low power applications [11],[32],[33].

3. **(NMOS or PMOS) only oscillator topology (Fig. 6.4(c,d))**: Theoretically, the output amplitude is 2VDDA in the voltage limited region, therefore it has better phase noise than CMOS topology in this region. NMOS only topology provides higher g_m for the same current consumption and area than PMOS only oscillator

topology, thus it has better start-up performance and less parasitics. However, it is sensitive to supply variation, because the output DC voltage is VDDA.

On the other hand, PMOS only oscillator topology has the same swing as NMOS only but with zero output DC voltage. Although it depends on the technology, PMOS devices generally have better flicker noise than NMOS [11].

4. **Top biased topology (Fig. 6.4(e))**: Biasing the NMOS only topology by PMOS current source has an impact on the cross coupled transistors. Connecting the cross coupled to ground degrades the tank quality factor. This degradation comes from the cross coupled resistance, which is in shunt with the tank resistance. As a corollary, the noise increases.

   On the other hand, the top biased PMOS only topology does not face the quality factor degradation problem [32],[34].

5. **(NMOS or PMOS) with supply biasing topology (Fig. 6.4(f))**: This topology always operate in the voltage limited region and it suffers from a high current consumption. This current needs to be controlled carefully since it is very sensitive to PVT variations [32],[34].

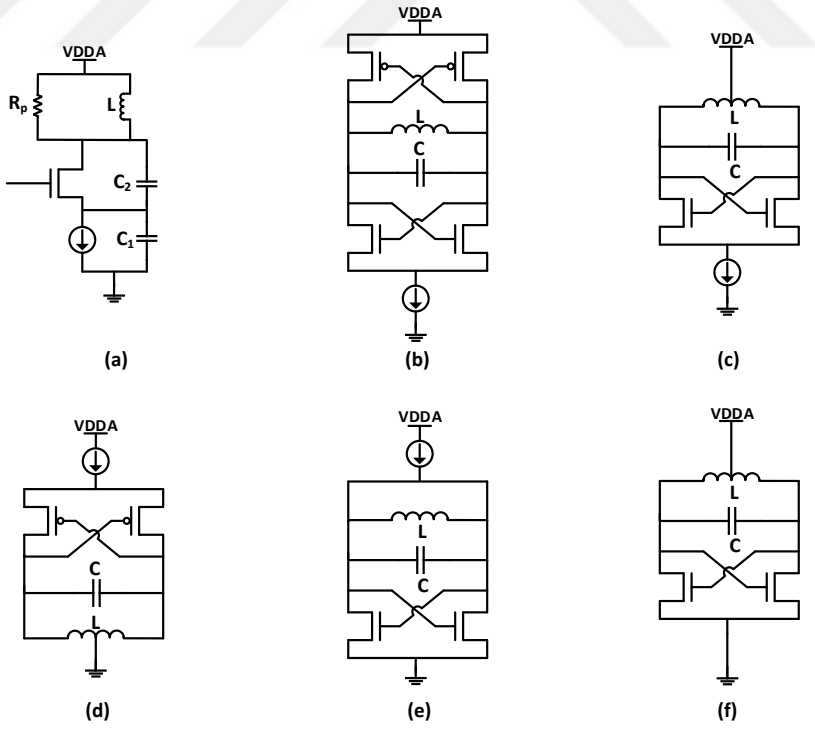


FIGURE 6.4: LC topologies; (a) Colpitt (b) CMOS (c) NMOS only (d) PMOS only (e)NMOS with top biasing (f) NMOS with supply biasing.

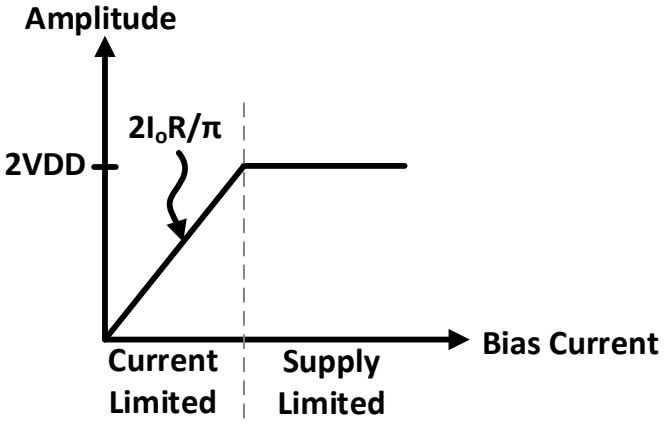


FIGURE 6.5: Biasing regions.

6.4 The proposed design

CMOS LC oscillator architecture is chosen in this project because it provides better phase noise performance than the other architectures at the same current consumption. However, some modifications are done in order to enhance the LC CMOS performance. These modifications are mainly to get the superior phase noise result. The required performance specifications are summarized in Table (6.2).

TABLE 6.2: Required performance specifications

Spec	**Value**
VDDAH	3.3±10%
VDDA	2.5±10%
Maximum frequency (GHz)	2.5
Tuning range (GHz)	0.5
K_{vco} (MHz/V)	40
PN at 1MHz offset from 2.2GHz carrier (dBc/Hz)	<-125
VCO core current consumption (mA)	3.2
Buffer current consumption (mA)	1.5

The proposed design gets rid of one of the elements that contribute the most to the phase noise, which is the current source transistor. The design depends on an LDO and feedback loop for regulating the bias current. Fig. 6.6 shows the block diagram of the proposed idea.

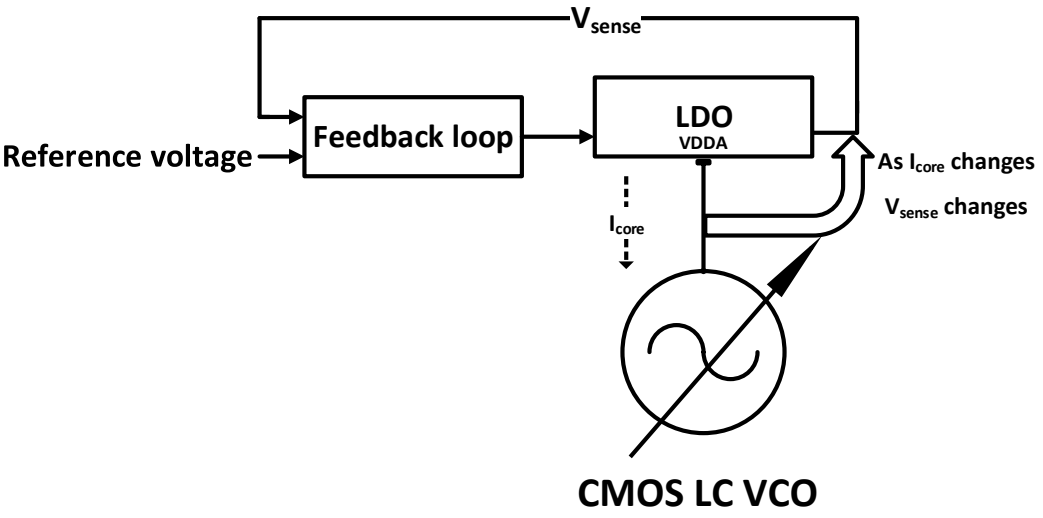


FIGURE 6.6: Top level block diagram.

6.4.1 Design methodology

6.4.1.1 Core design

Multiple theories were developed and numerous studies have been published in the recent years, examining methods for understanding and optimizing the performance of frequency oscillators [33]-[40].

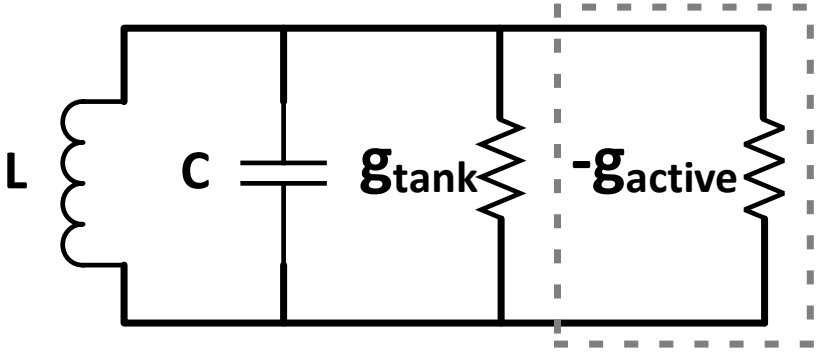


FIGURE 6.7: Parallel LC oscillator model.

Fig. 6.7 shows the parallel LC oscillator model in steady state, where the conductance g_{tank} represents the tank loss and g_{active} is the effective negative conductance of the active devices that compensate the losses in the tank. By considering the bias current as an independent variable, the operation regions as shown in Fig. 6.8 are specified for a typical LC oscillator. In the current limited region, the tank amplitude V_{tank} linearly grows with the bias current until the oscillator enters the voltage-limited region. In the

voltage-limited region, the amplitude is limited to V_{limit}, which in general is fixed by the supply voltage and/or the operation mode of the LC-core transistors (active devices). Generally, the tank voltage as shown in Fig. 6.8 can be expressed as

$$V_{tank} = \begin{cases} \frac{I_{bias}}{g_{tank}}, & (I - limited) \\ V_{limit}, & (V - limited) \end{cases} \tag{6.6}$$

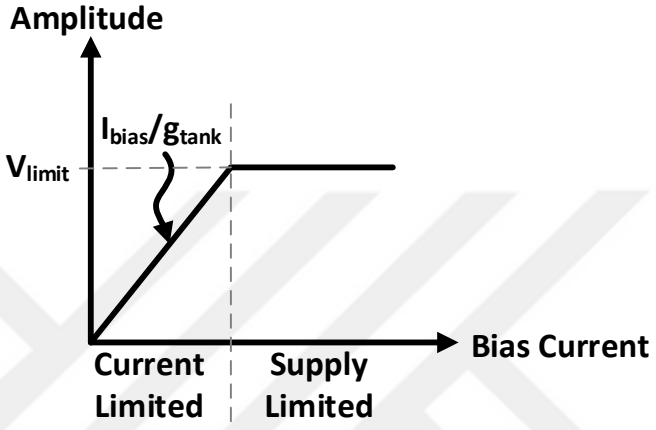


FIGURE 6.8: The general tank voltage for LC oscillator

CMOS LC VCO is modeled as shown in Fig. 6.9. The total parasitic capacitances of the NMOS and PMOS transistors are expressed by C_{nmos} and C_{pmos} respectively, g_m and g_o are the small-signal transconductance and output conductance of the core transistors, respectively. The symmetric inductor model is illustrated in Fig. 6.10 [41] and Fig. 6.11 shows the model of the MOSCAP varactor in LC tank circuit.

The frequently used parameters in the optimization process are the tank loss g_{tank}, effective negative conductance -g_{active}, tank inductance L_{tank} and tank capacitance C_{tank} [33], which are mathematically represented as below

$$2g_{tank} = g_{on} + g_{op} + g_v + g_L \tag{6.7}$$

$$2g_{active} = g_{mn} + g_{mp} \tag{6.8}$$

$$L_{tank} = 2L \tag{6.9}$$

$$2C_{tank} = C_{pmos} + C_{nmos} + C_L + C_v + C_{load} \tag{6.10}$$

where g_v and g_L as given by the equations below, are the effective parallel conductance of the varactor and the inductor, respectively.

$$g_v = \frac{\omega C_v}{Q_v} \tag{6.11}$$

$$g_L = \frac{1}{R_p} + \frac{R_s}{(\omega L)^2}. \tag{6.12}$$

The quality factor of the on-chip coils are low enough to allow some approximations to ease the design flow as shown in the equations below

$$2g_{tank} \approx g_L \tag{6.13}$$

$$2C_{tank} \approx C_v + C_{load}. \tag{6.14}$$

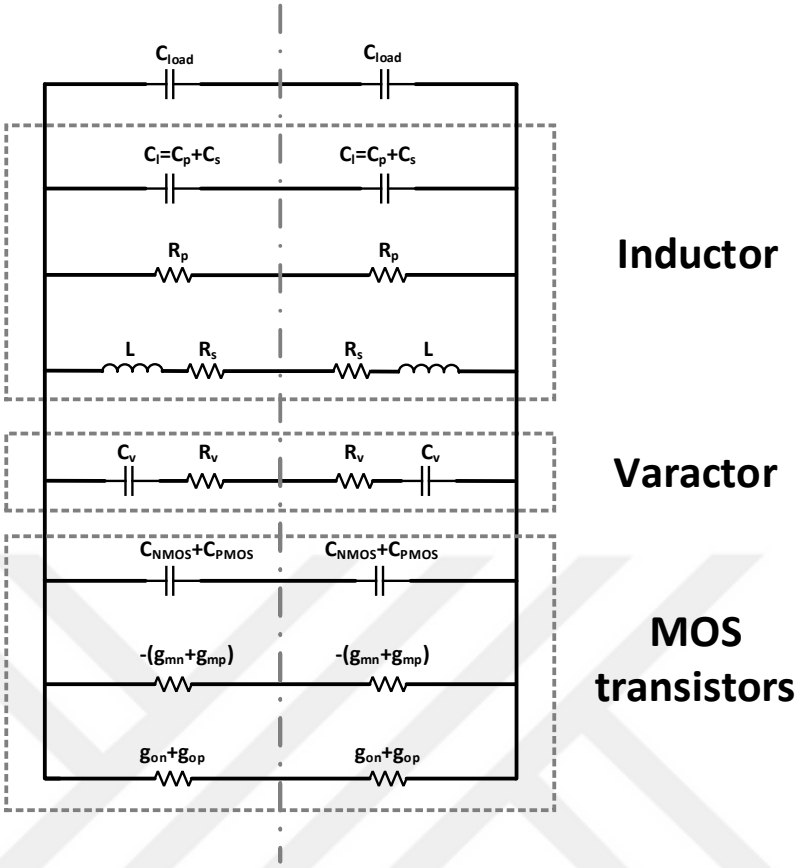


FIGURE 6.9: Equivalent CMOS LC VCO model.

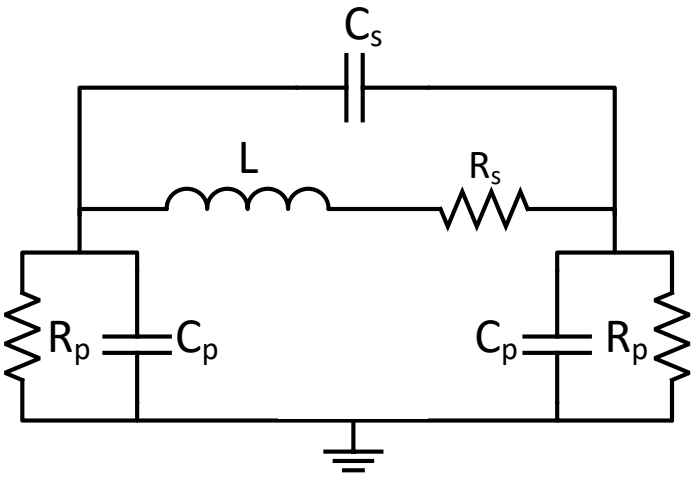


FIGURE 6.10: Symmetric inductor model.

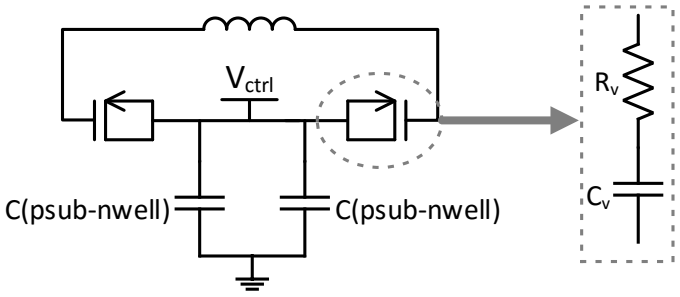


FIGURE 6.11: MOSCAP varactor in LC tank.

Finally, the design methodology illustrated in Fig. 6.12 takes into consideration the core elements and the interaction between them.

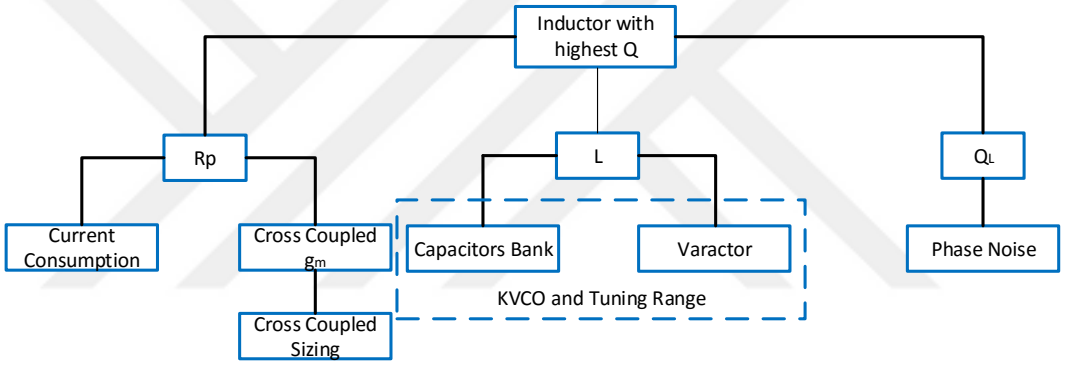


FIGURE 6.12: Design Methodology

6.4.1.2 Inductor design

Regardless the VCO topology, the most important step is to choose the inductor which gives the highest quality factor (Q). This is obvious from Lesson's equation (3.30), which states that the phase noise is inversely proportional to Q^2. However, this is not always the optimum solution. The highest quality factor of an inductor gives a small R_p, but the oscillation's amplitude is proportional to the current and R_p, therefore the oscillator needs higher power consumption in such a case. It is worth mentioning that the inductance value is also proportional to the area, hence as L increases, the area increases too.

After many iterations to find the optimum inductance value that meet the area, phase noise and start-up limitations. "L_SLCR30K_RFVIL" is the most suitable inductor in our technology. Fig. 6.13 shows the simulation results for the inductance value and the

quality factor in the desired frequency range. Furthermore, the tank loss (R_p) versus frequency is shown in Fig. 6.14, and R_p ranges from 589 to 773Ω. The lowest R_p requires the highest g_m, which means either higher power consumption or large cross coupled device dimensions. Hence, the worst case scenario of R_p should be taken in our consideration during the design step to insure the start-up operation. This inductor has outer diameter of 214.66μm, metal width of 6.12μm, metal spacing of 2.3μm, and the number of turns is 3.5.

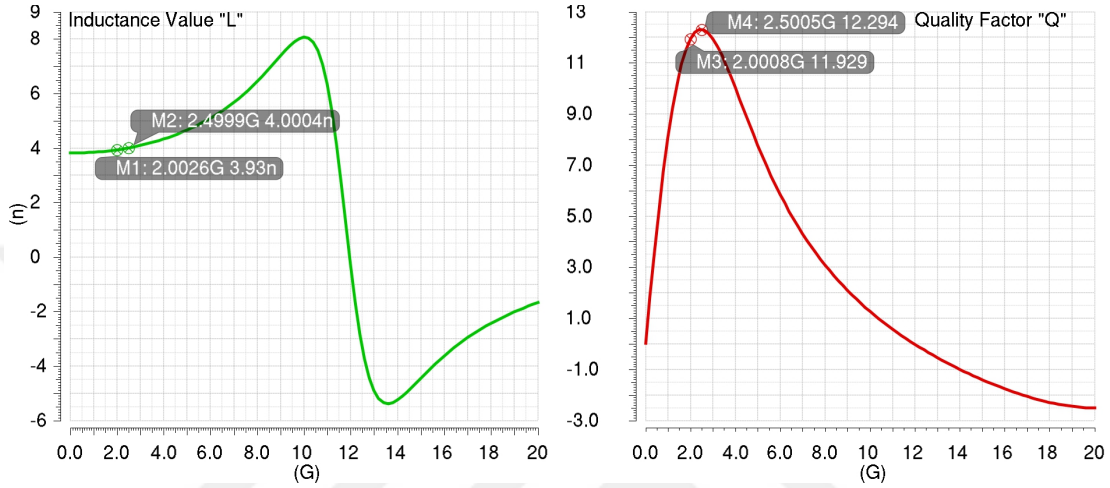


FIGURE 6.13: Inductor simulation (L and Q)

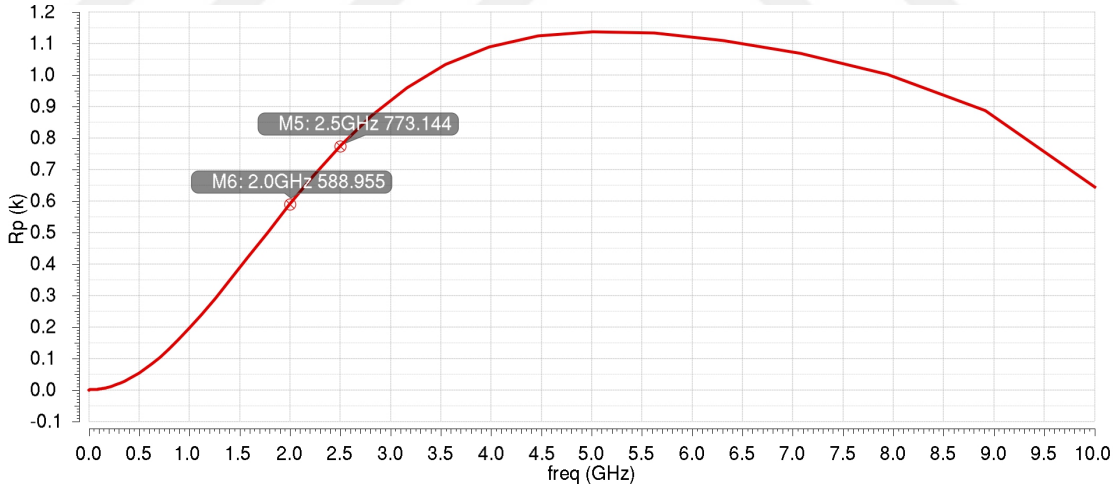


FIGURE 6.14: Inductor parallel resistor

6.4.1.3 MOS transistors design

The assigned current budget to the VCO core is enough to allow the operation to be on the verge of the voltage-limited region (maximum swing). This ensures the optimal operation for a given current and inductance value. The dimensions of the cross-coupled pairs

are chosen such that the transconductance provides the equivalent negative conductance value required to sustain oscillation as given by

$$g_{active} \geqslant \alpha g_{tank} \tag{6.15}$$

where $\alpha \approx 3$ in most cases [33].

$$g_{mn} = g_{mp} = \frac{1}{2} g_{active}. \tag{6.16}$$

By using a fair assumption of $g_{active} = 4g_{tank} = \frac{4}{R_p}$ to insure the oscillation start-up, we conclude that $g_{mn} = g_{mp} = 3.4m\mho$. Now, the dimensions of the core devices can be easily calculated by using

$$(\frac{W}{L})_n = \frac{g_{mn}^2}{2I\mu_n C_{ox}} \tag{6.17}$$

$$(\frac{W}{L})_p = \frac{g_{mp}^2}{2I\mu_p C_{ox}}. \tag{6.18}$$

A major challenge in most oscillator designs is to meet the phase noise system requirements. An ideal oscillator has a frequency response that is an impulse at the frequency of oscillation. Practically, oscillators exhibit skirts which is caused by instantaneous jitter in the phase of the waveform. Noise that causes variations in the phase of the signal is referred to as phase noise.

Leeson stated that the phase noise in oscillators can be approximated by [32],[35]

$$\mathcal{L}(\omega_m) = \frac{4KTRF}{V_1^2} (\frac{\omega_o}{2Q\omega_m})^2 \tag{6.19}$$

where $\mathcal{L}(\omega_m)$ is the total phase noise at a frequency offset of ω_m from the oscillating frequency ω_o. Q is the quality factor of the tank. R is the resistive loss, V_1 is the oscillation amplitude, K is Boltzmann's constant and T is the temperature in Kelvin. F represents the noise figure of the oscillator as given below [32]

$$F = 1 + \frac{2\gamma IR}{\pi V_1} + \frac{\gamma IR}{2V_{eff}} = 1 + \gamma \frac{2IR}{\pi V_1} (1 + \frac{\pi V_1}{4V_{eff,bias}}). \tag{6.20}$$

γ is a technology dependent parameter, which is typically between $\frac{5}{2}$ for short channel transistors and $\frac{2}{3}$ for long channel transistors. V_{eff} is the overdrive voltage of the current source transistor.

Equation (6.20) illustrates the phase noise in the white noise region (thermal noise). Furthermore, it apprehends all the frequency translations and the non-linearity impacts. The first part in the above equation represents the generated noise by the resonator. The noise in the differential pair, which is independent of the differential transistors sizes, is represented by the second term. The last term comes from the current source transistor noise.

When the amplitude of oscillation is smaller than the power supply or somehow the operation is on the verge between the current limited and the voltage limited regions, V_1 is given by

$$V_1 = \frac{2}{\pi} R I_o. \tag{6.21}$$

Finally, the total phase noise expression can be expressed by the equation below

$$\mathcal{L}(\omega_m) = \frac{4KTR}{V_1^2}(\frac{\omega_o}{2Q\omega_m})^2(1+\gamma\frac{2IR}{\pi V_1}(1+\frac{\pi V_1}{4V_{eff,bias}})). \tag{6.22}$$

Table (6.3) shows the design guide summary for the optimum phase noise performance. it indicates other encouraging reasons for replacing the conventional biasing technique by a current source to the one presented here. It is worth mentioning that the current source needs a current from BandGap reference, which usually deteriorates the phase noise.

TABLE 6.3: Noise design guide summary

Parameter	**Design Target**	**Limitations**
Inductor	Maximize Q with reasonable inductance value	Available inductors in design kit
Swing	Largest possible swing	-Voltage-limited region -Reliable operation $V_{ds} >$ VDD -Current budget
Differential pair	Minimize width, maximize V_{od}	Start-up condition $g_m > \frac{2}{R_p}$
Current source transistor	Minimize g_m	-Required I -V_{od} to keep it into saturation
Bank circuit	Minimize loading (large switch width)	-Parasitics -Tuning range

6.4.1.4 Varactor design

Varactors are the main components, which affect K_{vco}. As their sizing increases, K_{vco} increases, which in turns degrades the overall CP PLL phase noise. Generally, there are three main types of varactors [11];

- I-MOS varactor (inversion MOS varactor).
- A-MOS varactor (Accumulation MOS varactor).
- Junction varactor (Diode or P-N junction varactor).

I-MOS varactor is a PMOS transistor, which has its bulk connected to supply voltage and has a sharp transition in capacitance with voltage. A-MOS varactor is a NMOS transistor in n-well and has smooth transition in capacitance with voltage. Furthermore, it has the highest quality factor among any other types. Diode varactor has the lowest quality factor and commonly used in narrow tuning range applications due to its operation in reverse bias region only [11].

Since A-MOS has the highest quality factor, it is the most suitable varactor in order to prevent any phase noise degradation. It has one drawback as shown in Fig. 6.15 though, the curve of A-MOS varactor saturates quickly, which limits the control voltage range. However, this issue can be resolved by biasing circuit to maintain the varactor's operation within the linear range. Moreover, this circuit usually has a neglectable contribution in the overall VCO phase noise. In the proposed design, the linear range is chosen to be from -250mV to 100mV across the varactor terminals.

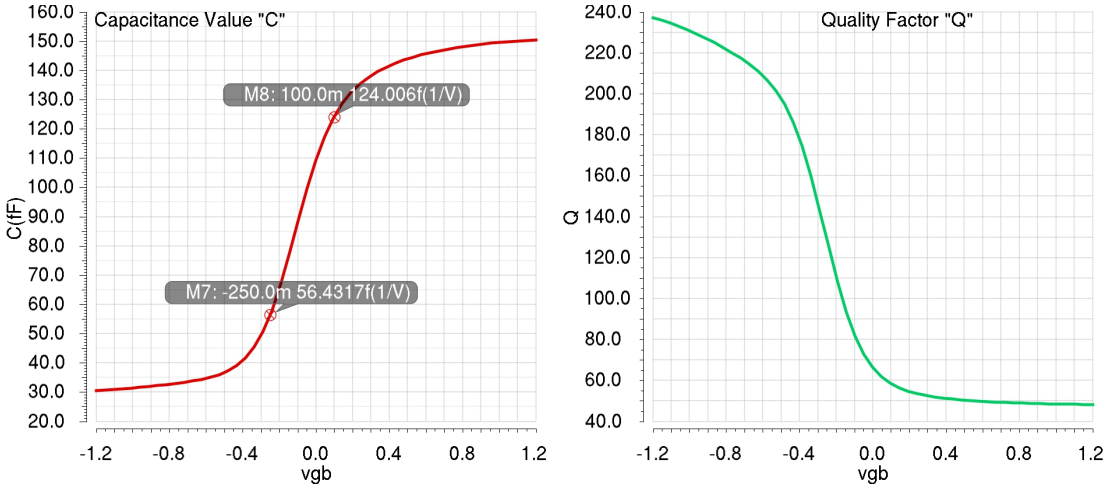


FIGURE 6.15: Varactor simulation (C and Q)

6.4.1.5 Capacitors bank circuit design

In applications where a substantially wide tuning range is required to cover the desired frequency band as well as to cover for PVT variations, discrete tuning may be added to achieve a capacitance range well beyond single varactor range while keeping a moderate value of K_{vco}. This is done by using a bank of capacitors in parallel with the varactors and switch them on and off to adjust the frequency of the VCO. However, the switches add resistive and capacitive parasitics, which in turn degrade the LC VCO performance. The resistive parasitics degrade the quality factor of the LC tank. The capacitive parasitics load the VCO output, hence they change the output frequency and the output amplitude.

In the capacitor switch shown in Fig 6.16(a), a single switch is used to switch both differential capacitors. With differential swing at the switch terminals, only half of its on-resistance appears in series with each unit capacitor as shown in Fig 6.16(b). Therefore, the resistive loading of the bank circuit on the tank is minimized [42].

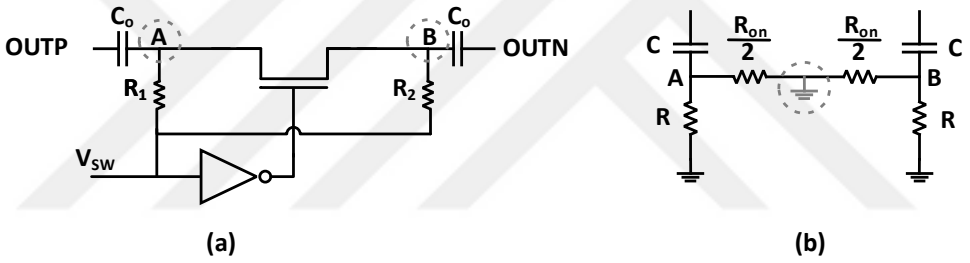


FIGURE 6.16: Capacitor switch (a)Single switch (b)equivalent circuit

Ideally, the switches should have R_{on} of 0Ω without capacitive parasitics. Practically, the trade-off between R_{on} and parasitics should be taken into consideration during the design of the switch sizes. Furthermore, the transistor should have an odd number of fingers for symmetrical loading.

The capacitors are chosen to achieve a sufficient overlap between the sub-bands to avoid any blind zones in the frequency range across PVT variations. Binary weighted 8-bit bank circuit is designed as shown in Fig. 6.17; the required frequency range is divided to 256 sub-bands. Finally, the final VCO core schematic is shown in Fig. 6.18.

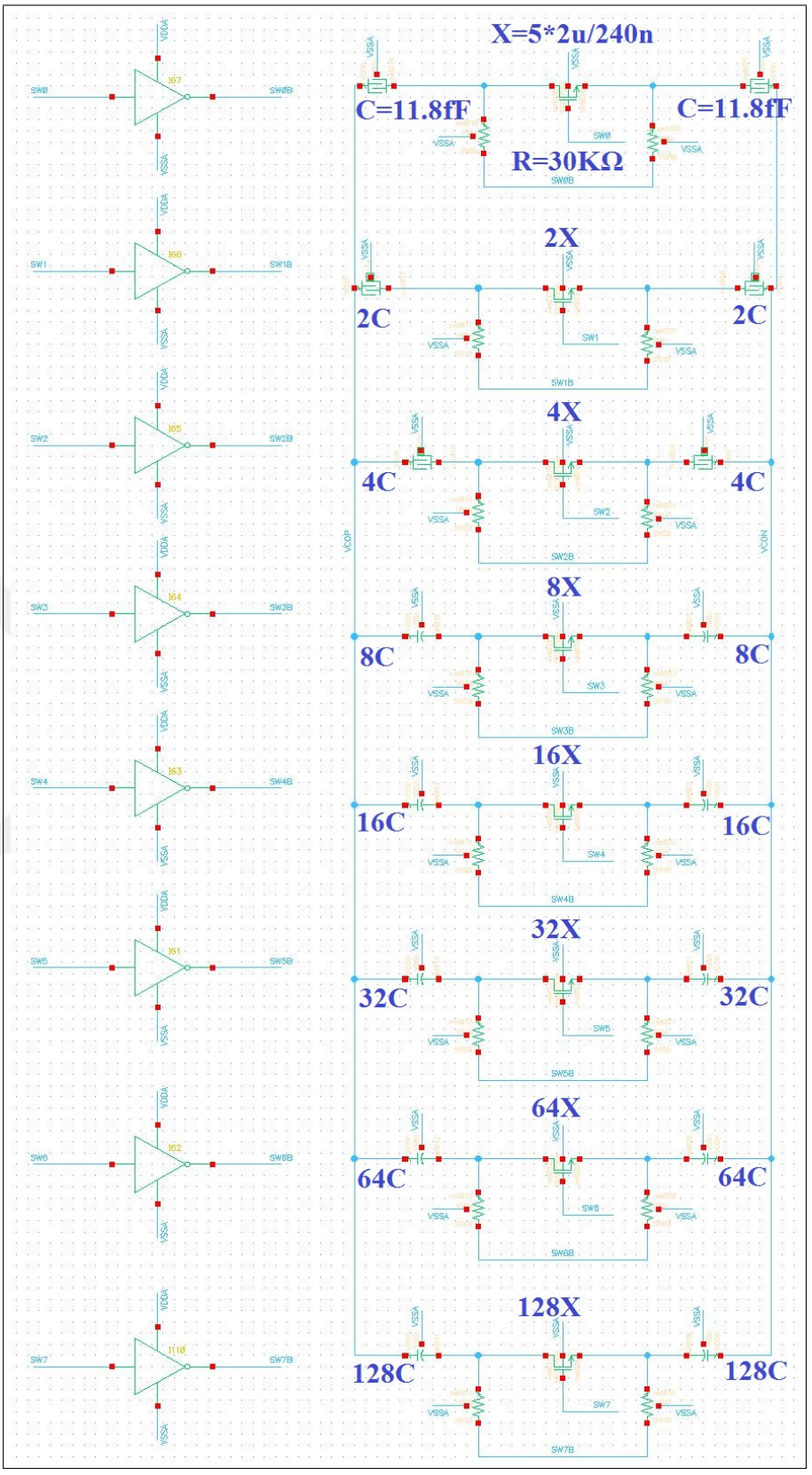


FIGURE 6.17: Bank circuit schematic.

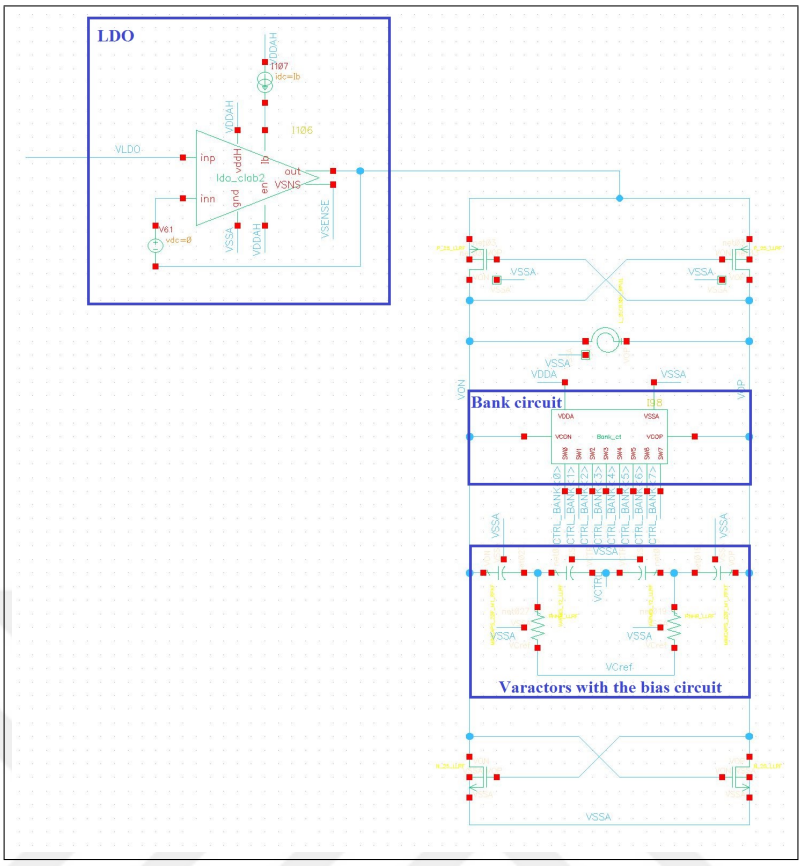


FIGURE 6.18: VCO core schematic.

6.4.1.6 Buffer design

The buffer is necessary to isolate the VCO from the load impedance (loading effect), which causes the VCO output frequency to change during operation. There are many types of buffers such as inverters, source followers and common source amplifiers. The main requirement for the buffers is low phase noise, hence the lowest phase noise architecture is the most suitable one.

Inverter with feedback resistor as shown in Fig. 6.19 fits the requirements; especially since this architecture does not need a BandGap reference for a current source transistor. As a result, the impact on the overall phase noise of the frequency synthesizer is minimal as shown in the simulation result section.

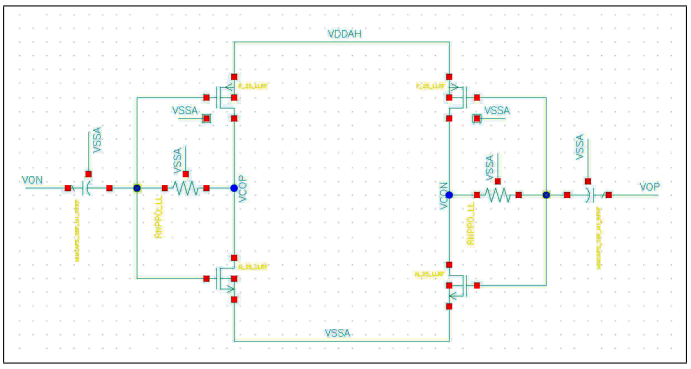


FIGURE 6.19: Buffer schematic.

6.4.1.7 LDO design

From the aforementioned discussion, the current source is one of the highest contributors in the output phase noise.. However, the current source is useful to limit the current variation across PVT.

The proposed design uses an LDO with a feedback loop instead of the current source in order to adjust V_{gs} for the core PMOS transistors to minimize the current variation across PVT. Although, the phase noise degrades due to the LDO output voltage noise, which is approximated in equation (6.23), it does not contribute as much as feeding the VCO with a current source as it will be shown later. Fig. 6.20 shows the LDO schematic with the sensing circuit. The sensing circuit senses the core current and translates this current into a voltage with a simple resistor and feed it to the feedback circuit.

$$\overline{V_{n,out}^2} = 8KT\gamma g_{m6}^2(g_{m1}+g_{m3})\cdot(r_{o1} \parallel r_{o3})^2\cdot(r_{o5} \parallel r_{o6})^2 + 4KT\gamma(g_{m5}+g_{m6})\cdot(r_{o5} \parallel r_{o6})^2. \tag{6.23}$$

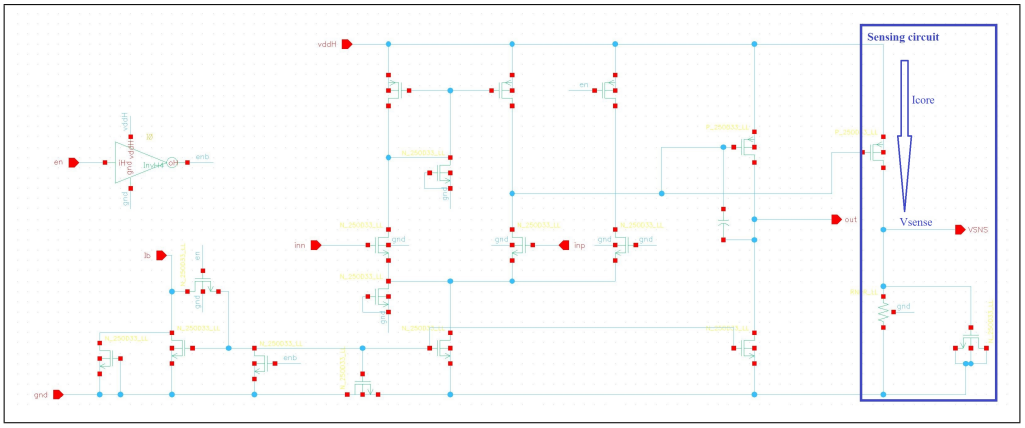


FIGURE 6.20: LDO schematic and the sensing circuit.

6.4.1.8 Feedback loop design

The design consists of comparators, up/dn counter, resistive divider and analog switches as shown in Fig. 6.21. The comparators are used to compare V_{sense} from the LDO to "Vref" and "Vref2". Two reference voltages in positive and negative direction are used to create a dead-band and prevent undesirable oscillation. The comparison results, up and down signals, control the up/down counter, which increase or decrease the $VLDO$ to regulate the VCO supply through the resistive divider and the analog switches. Once V_{sense} settles down in the dead-band, the loop stops. The functionality of this loop is summarized in the flow chart as illustrated in the Fig. 6.22.

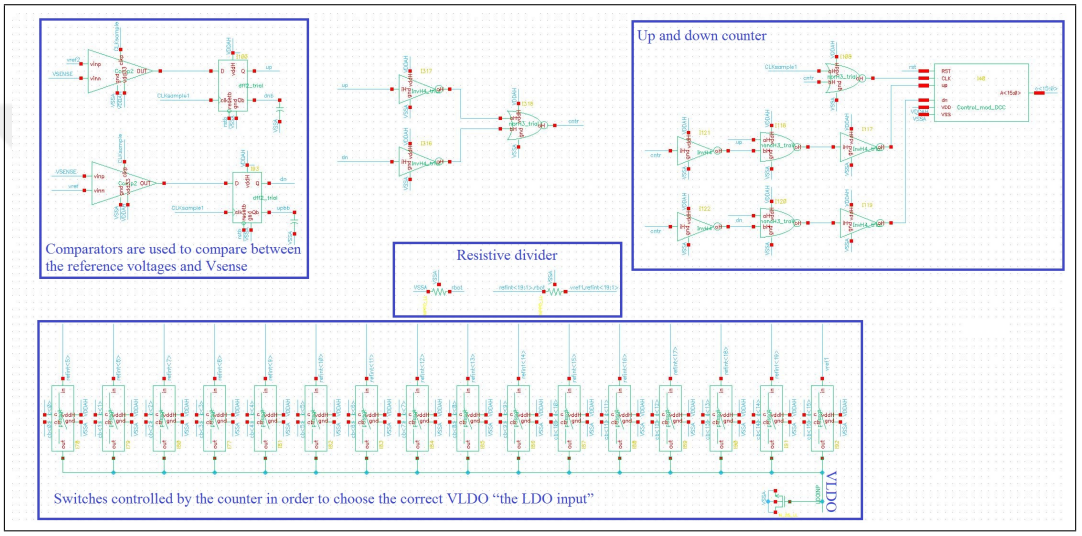


FIGURE 6.21: Feedback loop schematic.

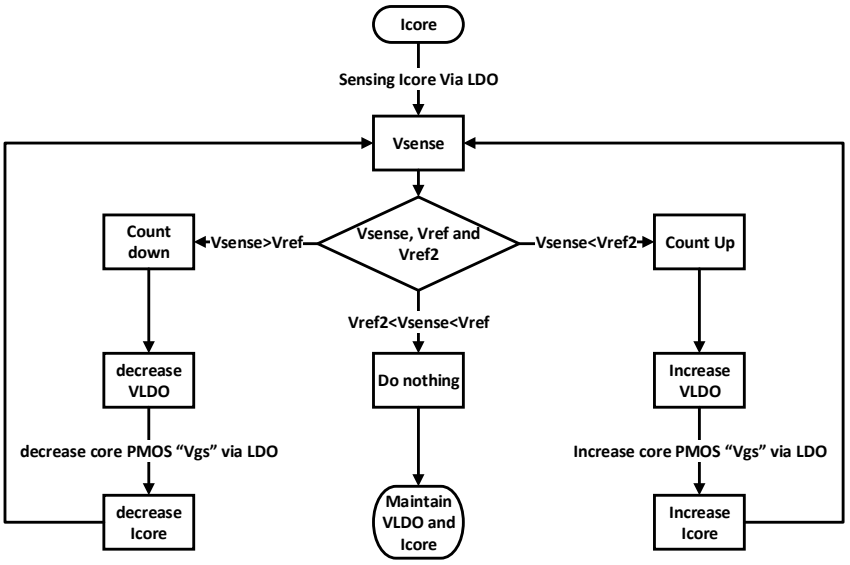


FIGURE 6.22: Feedback functionality to maintain less core current variations.

6.4.1.9 Fast VCO bands calibration

The block diagram of the proposed automatic bands calibration for fast PLL locking is illustrated in Fig. 6.23.

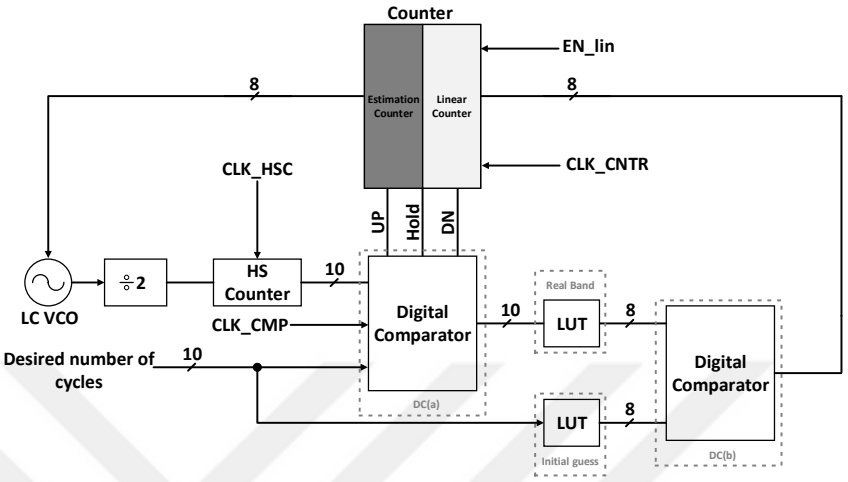


FIGURE 6.23: Block diagram of the proposed calibration system

LUT is a combinational logic, which translates the number of cycles to a band value. The initial guess comes from the expected value in the LUT. Thus, the band is chosen directly (ideal case). However, this value might change due to PVT variations and mismatch (reality) as shown in Fig. 6.24. Hence, a counter is required to overcome the bands variation. This counter counts up or down and it can be implemented either linearly or by using the BSA (binary search algorithm) technique [43]-[46]. The linear counter takes long time to find the correct band. Although the BSA technique is much faster than the linear counting, as the number of discrete bands increase, the conversion time increases as well. Therefore, the proposed solution uses the estimation method to converge very fast. This method depends on a reference value (initial guess) and an actual value (real band). The difference between the two values represents the bands variation, and this value is used by the counter to jump directly toward the correct band (estimation counter). Furthermore, the proposed solution has the ability to deal with the worst case scenario across PVT with random variations (ex. the difference between the adjacent bands are not equal). The counter starts using linear counting (EN_lin) after three cycles in order to avoid toggling around the correct band due to estimation errors. Consequently, robustness and speed are maintained by the combination of estimation, which converges very close to the correct band and linear settling, which does not need to count for many cycles to find the correct band (maximum two cycles). Finally, once "Hold" signal is HIGH, the loop stops.

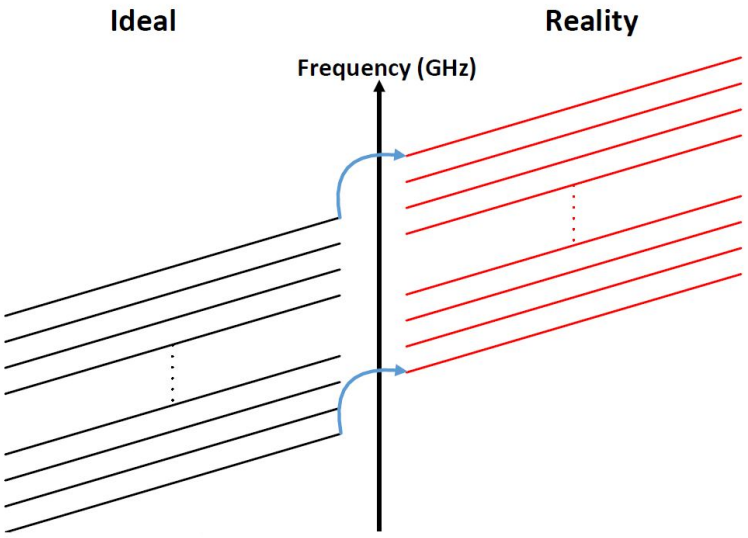


FIGURE 6.24: VCO bands variations across corners and mismatch

The proposed functionality is summarized below and illustrated in the flow chart in Fig. 6.25.

- The desired band is calculated through LUT (initial guess) from the desired number of cycles. This band value passes directly to LC VCO.
- The high speed counter (HS Counter) counts the divided VCO cycles over one CLK_HSC period (500ns).
- DC(a) extracts the actual number of cycles in one CLK_CMP period and generates three signals: UP, DN and Hold. "UP" and "DN" signals are used only when the counter switches the operation from estimation to linear. "Hold" determines whether the band value is correct or not, by comparing the desired number of cycles with the actual number of cycles. This signal works regardless of the counter's operation.
- According to the counted VCO cycles, LUT (real band) determines the band's value.
- DC(b) calculates the difference between the initial guess and the real band.
- For the first three cycles the counter works as estimation counter then it starts counting linearly. Depending on DC(b) output value and polarity, the estimation counter counts up or down.

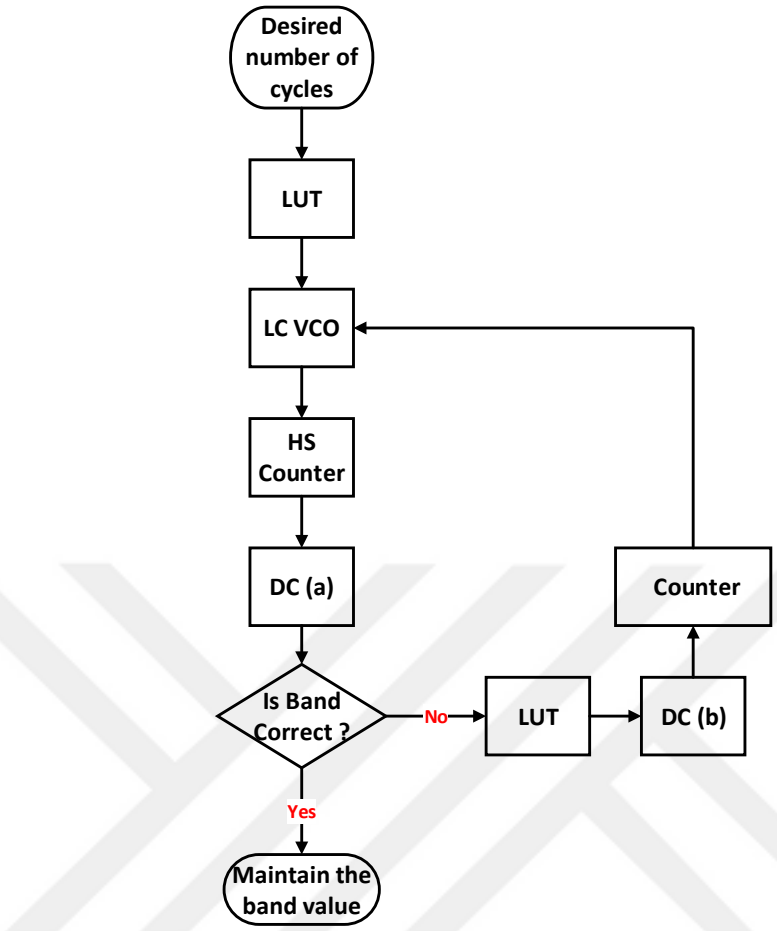


FIGURE 6.25: The proposed functionality of the fast VCO bands calibration

6.5 Simulation results

Simulation results are given for typical conditions, T=85°C, VDDHA=3.3V, VDDA=2.5V, and Fig. 6.26 shows the top level schematic for the test bench.

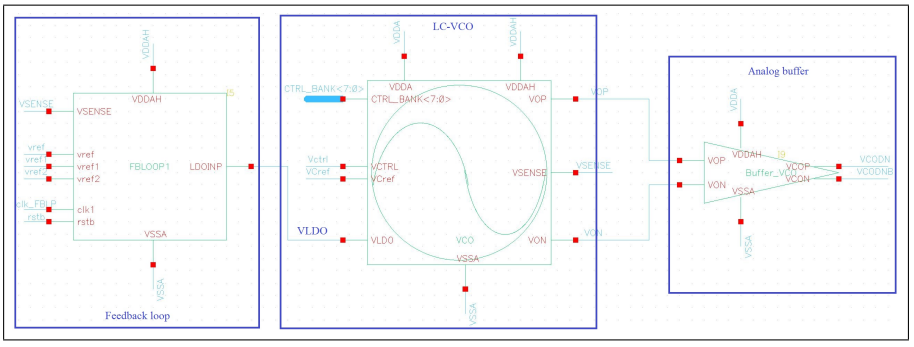


FIGURE 6.26: Top level schematic.

6.5.1 Transient simulation results

Fig. 6.27 shows the VCO and buffer outputs transient simulation. The figure shows the VCO swing is $1.8V_{p-p}$ and the output buffer swing is $1.1V_{p-p}$.

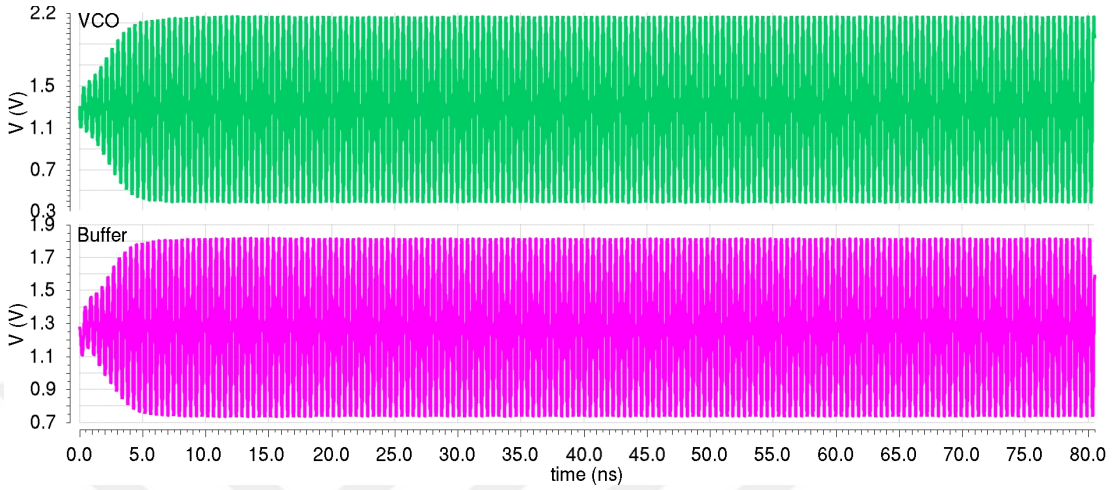


FIGURE 6.27: VCO and Buffer transient outputs

Fig. 6.28 illustrates how V_{sense} is trying to follow up the current variation. It is obvious that V_{sense} settles down when Vref2<Vsense<Vref. Furthermore, the graph shows that VLDO is approximately 2.54V.

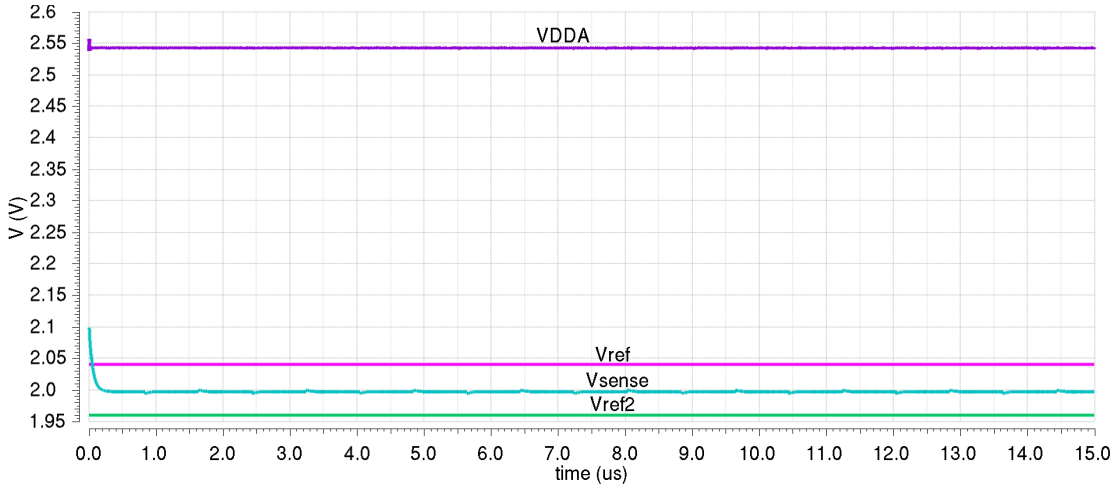
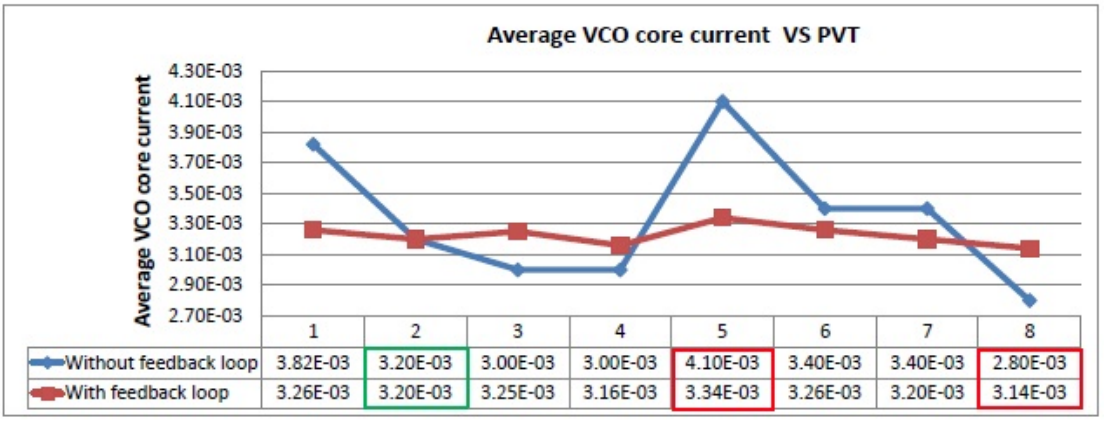


FIGURE 6.28: Feedback loop simulation result at typical conditions

Finally, the circuit was simulated in Cadence Spectre over PVT variations with supply range of 3.3V±10%, 2.5V±10% and temperature range of -40°C to 125°C. The current variations without the feedback loop as depicted in Fig. 6.29 are $+900\mu$A and -400μA. It is obvious from the figure that the feedback loop decreases the variations to be $+140\mu$A and -60μA.



	1	2	3	4	5	6	7	8
Without feedback loop	3.82E-03	3.20E-03	3.00E-03	3.00E-03	4.10E-03	3.40E-03	3.40E-03	2.80E-03
With feedback loop	3.26E-03	3.20E-03	3.25E-03	3.16E-03	3.34E-03	3.26E-03	3.20E-03	3.14E-03

FIGURE 6.29: Average VCO current variations across corners.

6.5.2 Phase Noise simulation results

Fig. 6.30 shows the phase noise result from the VCO regulated by the LDO. The feedback loop has negligible impact since it is a digital circuit. Phase noise at 1MHz offset from 2.2GHz carrier frequency is -127.2dBc/Hz. Furthermore, the phase noise result at the buffer's output is illustrated in Fig. 6.31. It shows that the buffer causes a slight degradation to the VCO phase noise at frequencies less than 100MHz. However, it adds significant noise at higher frequencies, but this is far away from the carrier.

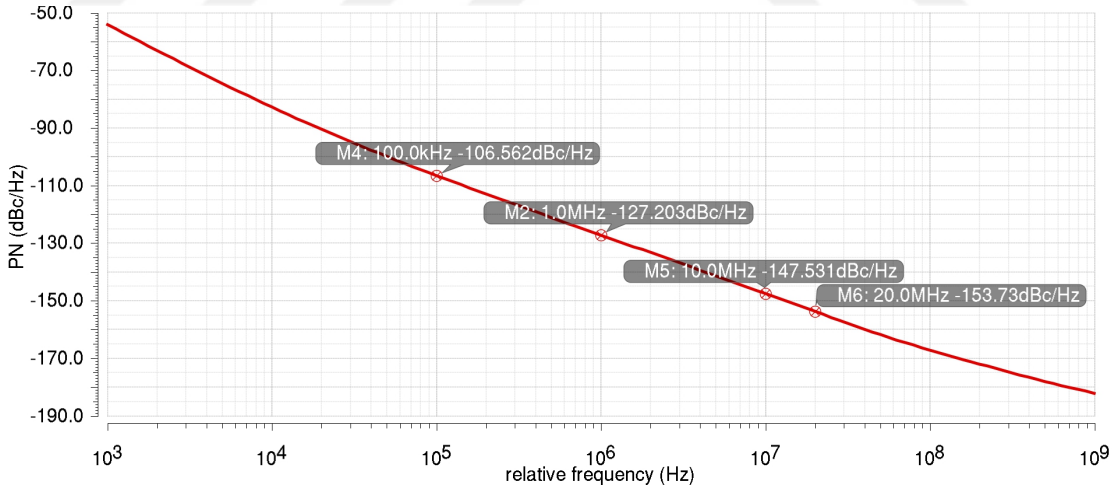


FIGURE 6.30: VCO phase noise.

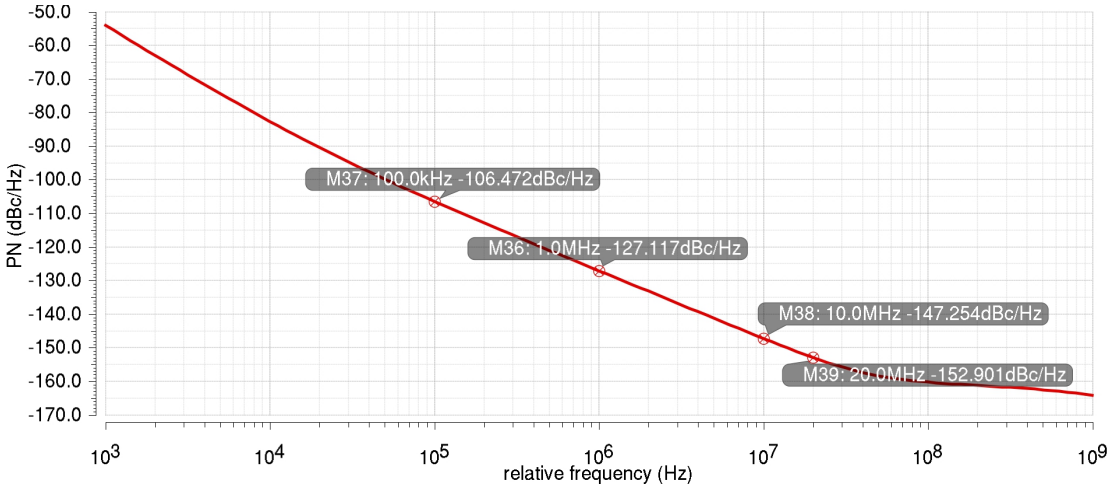


FIGURE 6.31: VCO and buffer phase noise.

6.5.3 Tuning range and K_{vco} simulation results

Fig. 6.32 shows the frequency bands at different input bits (0 to 7), as well as the K_{vco} variations for the same bands. Fig. 6.33 shows the lowest frequency band and K_{vco} variation in this band. The overlap between the bands is on average 2.53 (15.2MHz/6MHz). The K_{vco} variation across all the bands changes from 52.2MHz/V to 21.2MHz/V at 0.6V control voltage. Finally, the tuning range is from 2.83GHz to 1.976GHz.

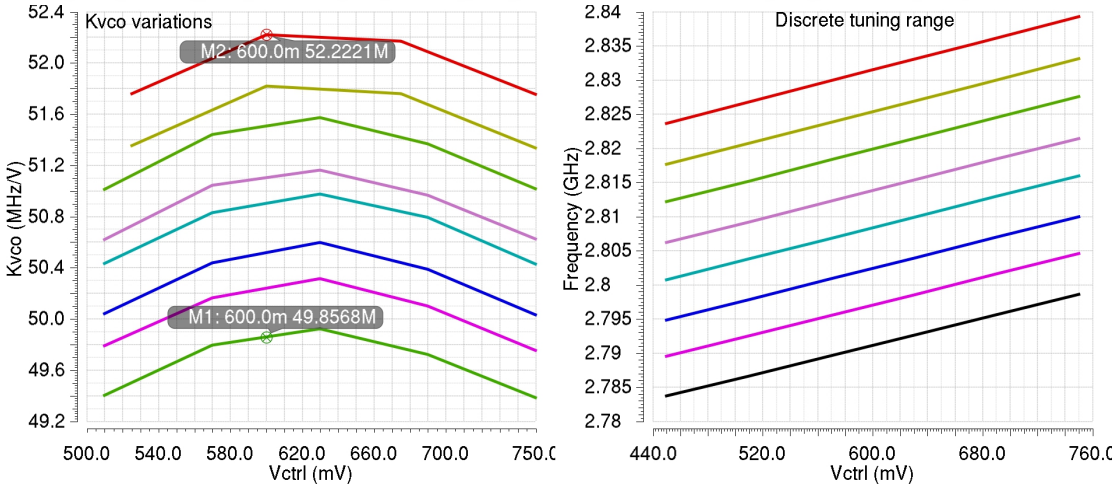


FIGURE 6.32: High frequency bands and K_{vco} variation.

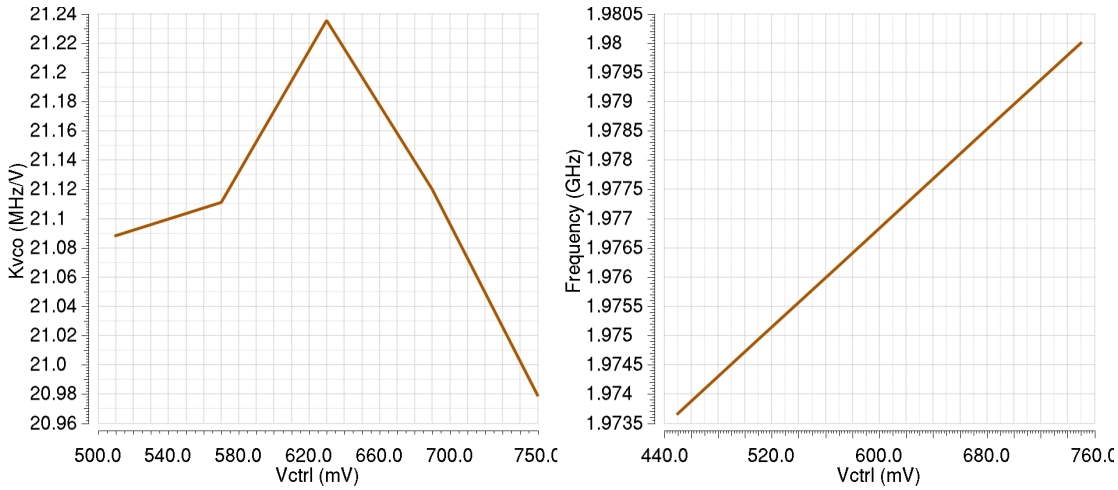


FIGURE 6.33: The lowest frequency band and K_{vco} variation.

6.5.4 Fast VCO bands calibration results

Fig. 6.34 shows the PLL output frequency locks to the correct band during the fast bands calibration process. The initial guess was close to the correct frequency band (167) as expected. Then, the estimation counter is turned on to jump directly to the correct band (169). The time required for the bands calibration is 568ns.

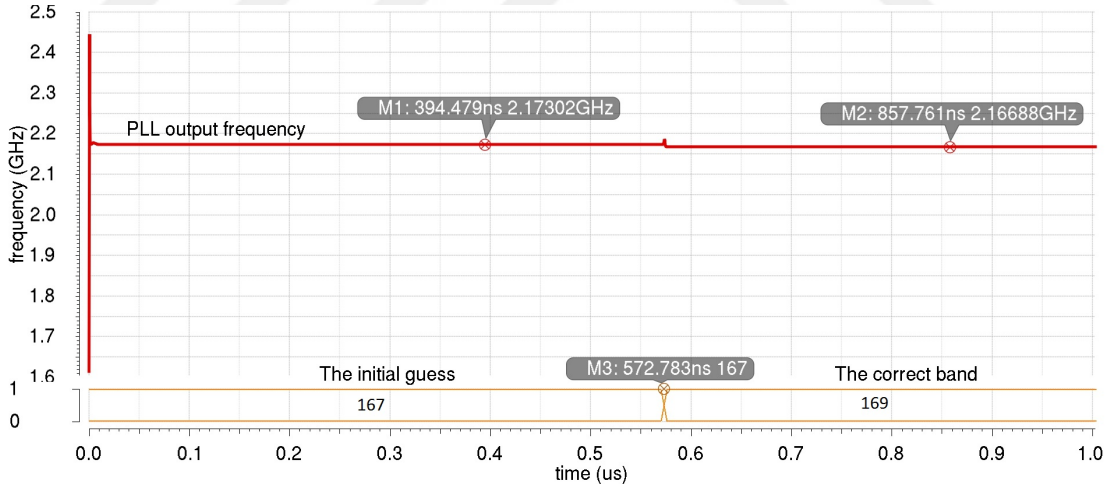


FIGURE 6.34: PLL output frequency during the bands calibration process

6.6 Conclusion

This chapter demonstrated the VCO concept, different topologies, theory of operation, the LC CMOS analysis and the design methodology. Then, a low phase noise VCO with a feedback loop for regulating the bias current is proposed. Furthermore, a new

technique for automatic bands calibration for fast PLL locking is presented. The design is implemented in UMC 65nm technology and simulation results are reported to ensure that it is satisfying the required specs at supply 2.5-V and 3.3-V. Finally, table (6.4) concludes the main performance parameters and compare with other recent state of the art designs.

TABLE 6.4: Comparison of VCO performance

VCO [Ref]	**[47]**	**[48](VCO3)**	**[49]**	**This work**
CMOS process (nm)	65	28	180	65
$F_o(GHz)$	3.6	25	1.7	2.2
FTR (%)	15.8	14.96	44	22.2
$\mathcal{L}\Delta f$ (dBc/Hz)	-122	-101.5	-123.4	-127.2
Δf (Hz)	1M	1M	1M	1M
P_{diss} (mW)	11	7.2	18	11.1
FOM (dBc/Hz)	-182	-180	-175	-183
FOM_T (dBc/Hz)	-186	-183.5	-188	-190

* $FOM = \mathcal{L}(\Delta\omega) - 20log(\frac{\omega_o}{\Delta\omega}) + 10log(\frac{P_{diss}}{1mW})$

* $FOM_T = FOM - 20log(\frac{FTR}{10})$

* This work : $P_{diss} = P_{LDO} + P_{vco}$

Chapter 7

System verification and thesis conclusion

7.1 System verification

The final task is to integrate the PLL frequency synthesizer in transistor level and verify that it is working properly before starting the layout phase and eventually fabrication. Each block has been separately designed in transistor level and verified using test benches with typical operating conditions and with PVT variations.

The transient simulation of the top level PLL circuit was done to ensure stability, locking and spurs levels. Phase noise simulations were done using a MATLAB model of the synthesizer. The operational conditions of this simulation are given below:

- Bandwidth = 350KHz.
- Phase margin = 49^o.
- Reference frequency = 80MHz.
- Division ratio = 27.1.
- Charge pump current = 80μA.
- Output frequency = 2.168GHz.

Fig. 7.1 shows the transient simulation of the control voltage, which indicates that the circuit has locked correctly. Fig. 7.2 shows the frequency domain of the PLL output signal. It is shown that the reference spur is -86.38dBc. This implies that the impact of this spur on the overall performance in wireless transceiver is negligible.

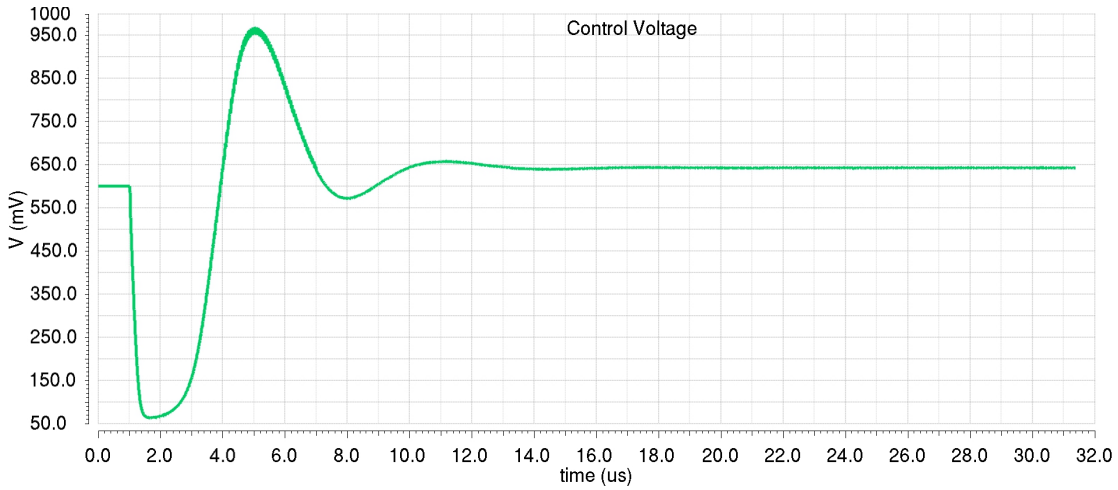


FIGURE 7.1: PLL control voltage.

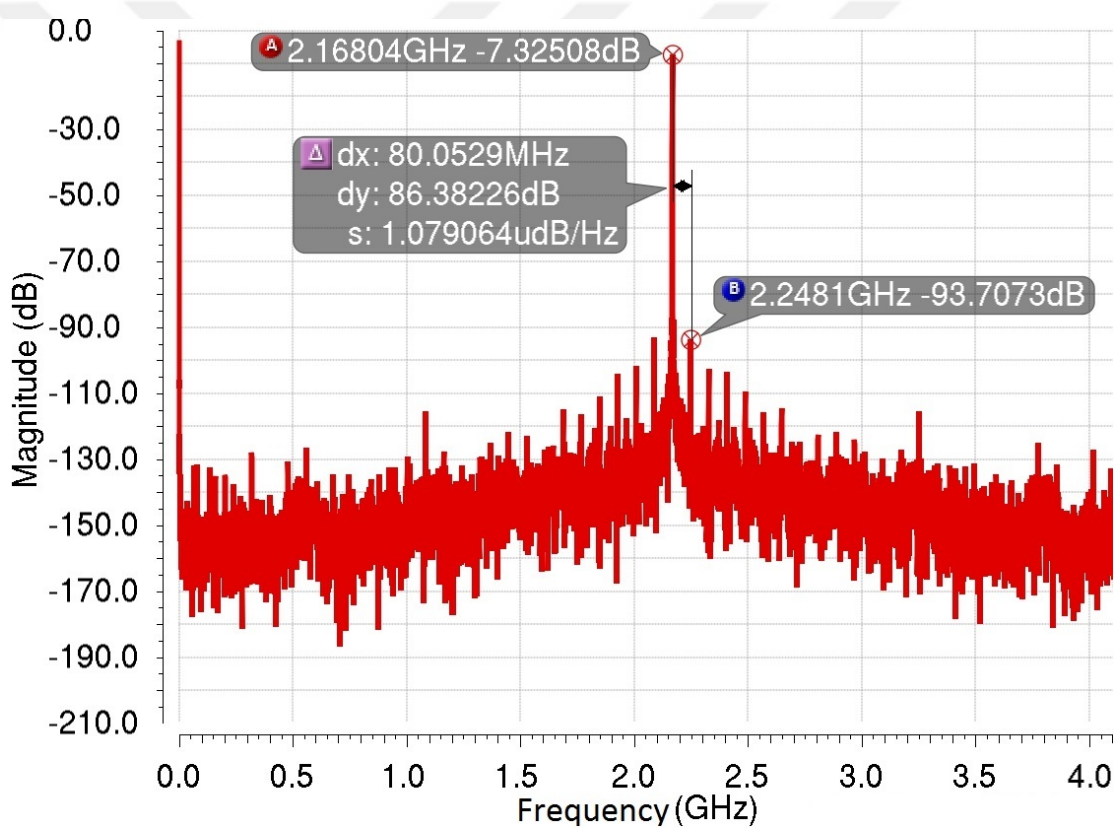


FIGURE 7.2: The frequency domain of the PLL output signal.

7.2 Thesis Conclusion

The system level design of a fractional-N PLL FS was successfully designed with the aid of MATLAB describing the PLL in the s-domain. This model facilitated the analysis of the system stability and was used to predict the closed loop synthesizer phase noise. The

transistor level design was implemented in 65nm UMC CMOS process, operating with voltage supplies of 1.2-V, 2.5-V, and 3.3-V. A new PLL FS design has been proposed, which is competitive with current implementations in terms of phase noise, locking speed, and power consumption.

Firstly, a novel technique of duty cycle correction mechanism has been proposed to correct the input duty cycle error from 40% to 60%. Moreover, the spur generation as a consequence of this error and the impact of duty cycle circuitry on the overall system phase noise performance has been presented.

Secondly, a new mixed signal frequency multiplier circuit was presented to multiply the input reference frequency (40MHz) by multiples of 2 up to 16. Furthermore, the non-ideal effects of the design was analysed and tested to show that it has a negligible impact on the overall performance.

Thirdly, the LC CMOS VCO operation theory, analysis, and design methodology was presented in the thesis. This study helped to introduce a new design of low phase noise VCO with a feedback loop to regulate the bias current. Moreover, a fast PLL locking was obtained by the proposed automatic VCO bands calibration.

Finally, the operational frequency range was from 2GHz to 2.5GHz with a programmable reference frequency from 40MHz to 640MHz. Table (7.1) summarizes the overall phase noise performance of the proposed PLL with 80MHz reference frequency and 2.16GHz output frequency.

Table 7.1: The overall phase noise performance of the proposed PLL

Offset frequency	**Phase noise (dBc/Hz)**
1KHz	-71.47
100KHz	-102.5
1MHz	-120.3
3MHz	-130
10MHz	-133.2
20MHz	-135.8

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