High Performance LNA Design for Next Generation Wireless

A thesis submitted to the
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by

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in

Electronics and Computer Engineering

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Electrical and Electronics Engineering.

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High Performance LNA Design for Next Generation Wireless

Amr Abdelhamid

Abstract

Nowadays, wireless communication systems are the most growing field in telecommunications industry. New standards have been introduced and the number of frequency bands that need to be supported increase enormously. The receiving end of any communication system has a key component which is the Low Noise Amplifier (LNA). LNA is placed as the first block in the receiver. The design of LNAs is one of the most challenging aspects in radio frequency (RF) systems. The most important parameters to measure the performance of LNA are gain and noise figure while stability, linearity, and return loss are examples of others. Nowadays, the limitations on power consumption and area are two major bottlenecks in LNA design because of the increased number of supported bands that increases the number of LNAs, matching networks and duplexers in the solution. Furthermore, as the demand of diversity and carrier aggregation increase, the number of LNAs increases further. For instance, a receiver solution that supports 2G, 3G and 4G standards with diversity for multiple bands may easily have more than 15 LNAs. This increase in the number of LNA in a single receiver requires a decrease in the power and area consumption of each LNA. In this thesis, we have studied the ways to decrease those two parameters while still complying with the state-of-art common source based LNA specifications. Two designs have been introduced, one of them is the widely used common source LNA with inductive load and degeneration. The other one is our new approach common gate LNA without any load inductors and it does not need a matching network as well. This thesis is divided into two main parts. The first part presents some design aspects and a comparative study for the implemented LNAs. The second part of this thesis presents two LNAs design, one of them is CS based LNA with load and source inductors which is often preferred and used in the wireless communication chips that is available in the market. This LNA operates at frequency 1.9 GHz and achieves 27 dB gain and noise figure less than 2.4 dB. The second design is a new approach to reduce the area and power consumption while still getting a good performance compared with the fist design. It operates at 2.4 GHz and achieves more than 22 dB gain and less than 2.3 dB noise figure. Both designs are implemented in UMC 65nm CMOS technology.

Yeni Nesil Kablosuz İçin Yüksek Performanslı LNA Tasarımı

Amr Abdelhamid

Öz

Günümüzde, telsiz iletişim sistemleri telekomünikasyon endüstrisinde en hızlı büyüyen alandır. Bu alana yeni standartlar getirildi ve desteklenmesi gereken frekans bantlarının sayısı hızlı bir şekilde arttı. İletişim sistemlerinin alıcı tarafı bir anahtar bileşene sahiptir; alçak gürültülü kuvvetlendirici (LNA). LNA birinci blok olarak alıcıda yerleştirilir. Radyo frekans sistemlerinde LNA'ların tasarımı en zorlayıcı durumlardan biridir. Kararlılık, doğrusallık ve geri dönüş kaybı diğerlerine örnekken LNA'nın performansını ölçen en önemli değişkenler verim ve gürültü faktörüdür. Günümüzde sorunun çözümünde alıcı-vericilerin, uyumlama devresinin ve LNA'ların sayısını arttıran desteklenmiş bantların sayısını arttırdığından güç tüketiminin ve alanın kısıtlanması LNA tasarımında iki ana engeldir. Çeşitlilik ve taşıyıcı toplama talebi arttıkça, LNA'lerin sayısı daha da artacaktır. Örneğin; birden fazla bant için çeşitlilikle 2G, 3G ve 4G standartlarını destekleyen bir alıcı çözümü 15 LNA'dan fazlasına sahiptir. Tek bir alıcıdaki LNA sayısındaki bu artış her bir LNA için güç ve alan tüketiminde bir düşüşü gerektirir. Bu tezde, en gelişmiş ortka kaynak tabanlı LNA tanımlamalarına uyumlu kalarak, yukarıda bahsedilen iki değişkeni azaltan yollar çalışıldı. İki tasarım tanıtıldı. Bir tanesi endüktif yük ve dejenerasyon ile kullanılan ortak kaynak LNA'dır. Diğeri ise yük endüktifi olmayan ortak geçit LNA'dır ve ilave olarak uyumlama devresine ihtiyaç yoktur. Bu tez iki ana kısıma ayrılmıştır. Birinci kısımda bazı tasarım durumları ve uygulanmış LNA'ların karşılaştırma çalışması anlatıldı. Tezin ikinci kısmında ise iki tane LNA tasarımı anlatıldı. Bir tanesi piyasada mevcut olan kablosuz iletişim çiplerinde daha çok tercih edilen endüktif yük ve dejenerasyonlu ortak kaynak tabanlı LNA'dır. Bu LNA 1.9 GHz frekansta çalışır ve 27 dB verime ulaşır ve 2.4 dB'ten daha az gürültü faktörü vardır. İkinci tasarımda ise birincise kıyasla daha iyi bir performans elde ederken alan ve güç tüketimi azaltan yeni bir yöntemdir. Bu tasarım, 2.4 GHz'de çalışır ve 22 dB'den fazla verim verir ve 2.3 dB gürültü faktörüne sahiptir. İki tasarım da UMC 65nm CMOS teknolojisinde uygulanmıştır.

To my parents and my sister, Ranya.

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Chapter 1

Introduction

1.1 Motivation

Low Noise Amplifier is the first stage in a receiver after the antenna. The noise figure of this block dominates the noise figure of the entire receiver according to Friis's equation given in [1]. Because of this, maximizing the gain while, at the same time, minimizing the noise figure is the most important design approach in LNA implementations. Other than having a high gain and low noise figure, there are other performance metrics that are important. Impedance matching between the antenna and the LNA input, linearity, and stability are examples of those metrics. To have a maximum power transfer, LNA requires a good impedance match to the antenna. As the number of wireless communication standards increases, the number of frequency bands that needs to be supported increases continuously. Because of this, the need for a multi-standard transceiver has been arising which means a drastically increase in the number of RF modules.

Furthermore, the possibility of carrier aggregation not only increases the number of RF modules, but also the number of receiver chains. For instance, a receiver that supports 2G, 3G, and 4G standards with diversity for multiple bands may easily have more than 15 LNAs. Because all of this, RF designers need to come up with other LNA configurations than CS LNA with inductive load and degeneration. CS based LNA is widely used in transceiver [2], [3], [4], and [5]. It is important to note that as the number of LNA increases, with the current CS based LNAs, the number of external components for matching will increase drastically, which will also increase the cost and volume of the solution due to the increase of PCB area. Furthermore, it is not viable to get a wide-band matching through a CS design, which may be a major issue for the yield of the solution as the on-board components may have a variation of %10 or more easily.

Another design aspect designers should take care of is non-linearity as it can cause problems such as gain compression, blocking and intermodulation. One common way to quantify non-linearity is input-referred third-order intercept point (IIP3), normally expressed in dBm and is desired to be as high as possible. Power consumption is another design specification that needs to be closely inspected. Considering only the noise performance and linearity can lead to a biasing solution that makes the power consumption simply too big to be practically realized. Increased incorporation of RF systems into hand-held device makes it necessary to minimize power consumption in order to maximize battery life. Inductors off- and on-chip are used as a solution to resonate at the desired frequency to obtain real valued impedances. Because of this resonance, the bandwidth for this type of LNA is low. Inductors use a lot of area on chip and all the matching components off chip use valuable PCB area. To make matters even worse inductors on chip require expensive manufacturing steps to get a high Q.

1.2 Thesis Objective

The objective of this thesis is to develop a prospective LNA design which differs from the state-of-art common source based LNA to reduce the power consumption and the area of the chip and PCB as well, while at the same time still having an acceptable performance. To accomplish this task, a comparative study of the most recent LNAs is presented and a detailed analysis of the effective parameters is discussed. After this detailed study, two designs are presented. One of them is the commonly used CS based LNA with parallel RLC load at the output and inductive degeneration at source that operates at 1.9 GHz. This design achieves gain higher than 27 dB and a noise figure lower than 2.4 dB. The other one is a new approach that does not need an inductive load neither matching network which means a great reduction in area of the chip and the PCB as well. This LNA operates at 2.4 GHz and achieves a gain higher than 22 dB and a noise figure lower than 2.3 dB. However, the performance of this LNA is less than the CS LNA. The performance is still acceptable.

1.3 Thesis Organization

The remainder of the thesis is organized as follows: Chapter 2 reviews the fundamentals of the LNA design such as noise figure, impedance matching, and linearity. A comparative study of the previously designed LNA stating the pros and cons of each design is presented in this chapter. Chapter 3 presents the design methodology of the two prospective LNAs explaining the tradeoffs and figure of merits that have been considered through the design

and the simulation results. Chapter 4 concludes the work in this thesis and the future work.

Chapter 2

State of Art

2.1 Performance Metrices

In this chapter, a general overview on some key parameters in LNA design will be presented along with a comparative study of some state-of-art LNA design and investigation about the pros and cons of each of them.

2.1.1 Noise

Noise is an undesired phenomena that lowers the quality of the signal that is processed by the amplifier. The signal quality in an amplifier is measured by Signal-to-Noise Ratio (SNR), which is defined as the ratio between the signal and the noise powers [1]. There are three main noise sources induced from electronics components: Thermal noise, shot noise, and flicker noise. Thermal noise also known as Johnson noise since it was first observed by J. B. Johnson [Johnson, 1928]. It presents in any passive resistor (including semiconductor) above absolute temperature. This noise is caused by a random motion of charge carriers in a conductor and is independent of bias. As it will be demonstrated in the following sub-sections, thermal noise is the main noise contributor in an LNA design that is implemented in a digital CMOS process. Shot noise occurs in pn-junctions and depends on dc bias current. It can be modelled as a white noise source. It is one of the major noise contributors in LNA design that uses a Bipolar Junction Transistor (BJT) as the voltage to current conveyor. Since this thesis is mainly focuses on the LNA design in a digital CMOS process, we will not provide any detailed analysis on the effect of shot noise in LNA noise performance. Flicker noise also called $1/f$ noise arises due to the traps in the semiconductor and occurs only when a dc current is flowing. It has an effect in both bipolar and MOSFET transistors and it dominates the thermal noise for

lower frequencies and can be neglected for higher frequencies. As shown in figure 2.1, the frequency that $1/f$ noise value crosses the thermal noise floor is called "$1/f$ corner frequency" [6]. The corner frequency is in the range of hundreds of megahertz in MOS technology nowadays. Since the LNAs, are mainly operates at higher frequencies than the $1/f$ corner frequencies of many processes, its contribution is negligible in LNA noise performance under linear operation. However, due to the limited linearity of an LNA and high-level blocker signals, the $1/f$ noise of certain elements in an LNA design, especially bias elements, can be up converted to the frequency of interest and adds to the overall noise power of the design. The following is a brief review about the main noise sources in various design elements that are used in a LNA design.

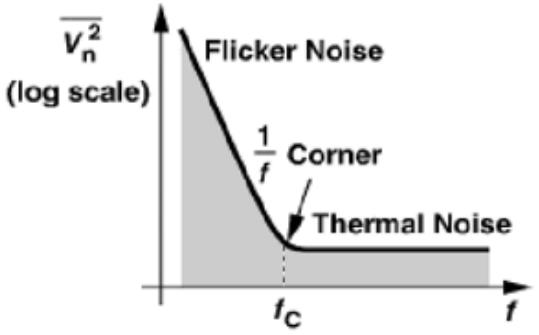

FIGURE 2.1: Flicker noise corner frequency [1].

2.1.1.1 Resistors

The thermal noise is the major noise source in a resistor. It can be modeled as a voltage source with a PSD density of, $V_n^2(f)$,in series with noiseless resistor as shown in figure 2.2, where $V_n^2(f)$ is given by

$$V_n^2(f) = 4kTR \tag{2.1}$$

where k is the boltzmann's constant $\left(1.38\times10^{-23}JK^{-1}\right)$, T is the temperature in Kelvins, and R is the resistance value. It appears to have the same value for all frequencies, white noise [6]. The noise can also be modeled as a current source, $I_n^2(f)$, in shunt with noiseless resistor and with a PSD value of

$$I_n^2(f) = \frac{4kT}{R} \tag{2.2}$$

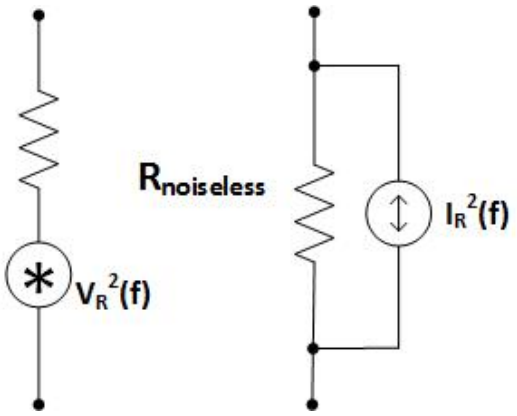

FIGURE 2.2: Noise model of a resistor.

2.1.1.2 MOSFETs

Thermal and flicker noise are the dominant noise sources for active MOSFET transistors. The flicker noise can modeled either as a voltage source in series with the gate or as a current source between source and drain.

$$V_g^2(f) = \frac{K}{WLC_{ox}f} \tag{2.3}$$

$$I_d^2(f) = \frac{Kg_m^2}{WLC_{ox}f} \tag{2.4}$$

where K is a device specific constant. The variables W, L, g_m, and C_{ox} represent the transistor's width, length, trans-conductance, and gate capacitance per unit area, respectively [6]. The thermal noise in MOSFET transistors operating in saturation region can be modeled as a current source tied between drain and source terminals as shown in figure 2.3 with the PSD value of:

$$I_d^2 = 4kT\gamma g_m \tag{2.5}$$

where γ is the excess noise coefficient. Its value is $2/3$ for long channel transistors and can rise to 2 for short channel devices.

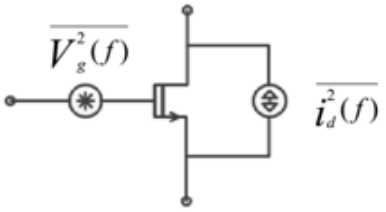

FIGURE 2.3: Noise model of a transistor [6].

As mentioned before, the dominant noise depends on the frequency of operation. If an amplifier is working at a frequency less than the corner frequency, then the flicker noise will dominate. If the operating frequency is higher than the corner frequency, which is usually the case in LNA, the thermal noise will dominate.

2.1.1.3 Capacitors and Inductors

Capacitors and inductors do not produce random noise. However, due to the non-idealities of the capacitors and finite quality factor 'Q' of the inductors the parasitic resistances produce some thermal noise. On- and off- chip inductors are used for matching, degeneration, and loading purpose when designing an LNA. While the performance of the off-chip inductors is better than that of the on-chip inductors (higher Q-factor), the desire to decrease the number of off-chip inductors used on the board increased to reduce the board complexity and cost.

As a conclusion, the noise from capacitors and inductors with limited Q can be modeled with the effective value of the resistance at the frequency of interest and the noise due to that parasitic resistance as shown in figure 2.4. As a reminder, since the value of the resistance that is used to model the quality factor of passives is mainly frequency dependent, the noise contribution is frequency dependent as well.

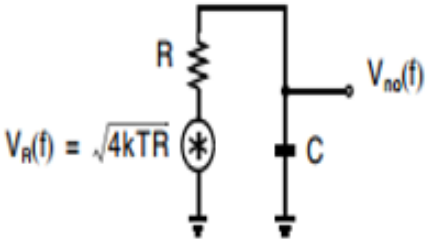

FIGURE 2.4: Equivalent noise model circuit [6].

2.1.1.4 Noise Factor (f) and Noise Figure (NF)

The noise figure (NF) is a measure of the amount of noise added to the signal by the circuit components and measured in dB scale. On the other hand, the noise factor (F) is the value of NF in linear scale, and defined as the ratio between the SNR_{out} and SNR_{in} of the circuit component [1]. Noise factor (F) of an LNA can expressed in terms of its gain and the noise power at its input and output as follows:

$$F = \frac{SNR_{out}}{SNR_{in}} = \frac{S_{in}}{N_{in}} \times \frac{N_{out}}{S_{out}} = \frac{S_{in}}{N_{in}} \times \frac{G \times N_{in} + N_{amp}}{G \times S_{in}} = 1 + \frac{N_{amp}}{G \times N_{in}} \tag{2.6}$$

where S_{in} and S_{out} are the signal power level for input and output, N_{in} and N_{out} are the input and output noise power level, and G is the gain.

For a cascade system of N stages as shown in figure 2.5, the overall noise factor can be obtained in terms of the noise factor and gain of each stage. The total noise factor can be expressed by the Friis's equation:

$$F_{sys} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_N - 1}{G_1 G_2 \ldots G_{N-1}} \tag{2.7}$$

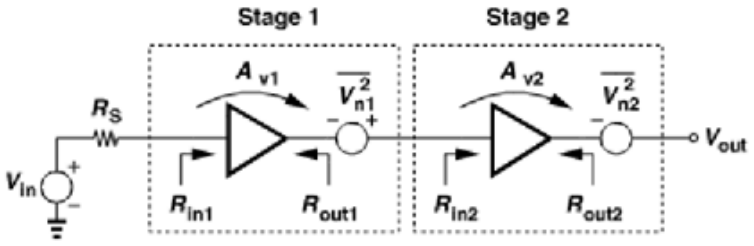

FIGURE 2.5: Noise of cascaded stage [1].

2.1.2 Gain

Gain shows how much the signal is amplified and is defined as the voltage ratio of the output signal and input signal. This ratio is called the "voltage gain" and it is expressed in dB as

$$Gain = 20 \log \left(\frac{V_{out}}{V_{in}}\right) \tag{2.8}$$

Another definition of gain is the power gain which is the ratio between the output power and the input power. In this thesis voltage gain is used unless stated otherwise.

2.1.3 Input Matching

Matching the impedance of the antenna to the impedance of the input port of the LNA is required to get maximum power transfer from the antenna to the LNA. This is usually done by putting additional passive networks between the antenna and the input of the LNA. These networks are called matching networks.

In the common source LNA, the input impedance is dominated by the gate-to-source capacitance C_{gs}. To achieve a purely resistive impedance, extra components should be added. Degenerating the source with an inductor as shown in figure 2.6 can achieve such

a goal. The input impedance of this common source inductively degenerated amplifier can be derived as:

$$Z_{in} = sL + \frac{1}{sC_{gs}} + \frac{g_m L}{C_{gs}} \tag{2.9}$$

The last term of this equation is purely real and can be matched to 50Ω by proper biasing and sizing as it will be discussed in more details in chapter 3.

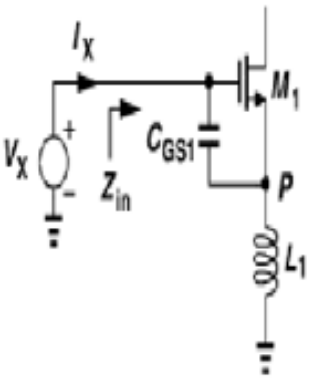

FIGURE 2.6: Inductively Degenerating MOSFET [1].

In the common gate LNA, the input impedance is approximately $1/g_m$ when it is loaded with a large inductor at its source. However, the common-gate LNA can also be biased via a resistor. Using a resistor is a good option for a wideband design and smaller area. However, the DC voltage drop across the resistor will reduce the total available headroom of the amplifier. Furthermore, the NF of the solution will increase by 6 dB which is not acceptable for high performance receiver designs. On the other hand, using an inductor consumes larger area and because it is a frequency dependent component it will reduce the operating bandwidth of the amplifier. However, the linearity and the noise figure performance of the amplifier is superior without any headroom reduction. Thus, it is a trade-off between performance and cost.

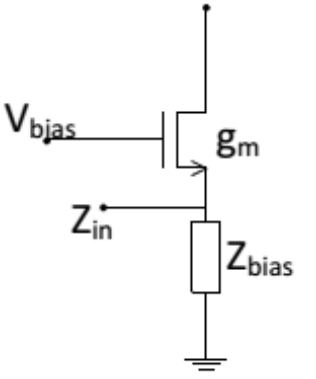

FIGURE 2.7: Common gate LNA [1].

2.1.4 Linearity

Nonlinearity of a system is mainly due to the distortion in active components like transistors. Many measures of linearity are exist, the most commonly used are the 1-dB compression point (P_{1dB}). Second order intercept point ($IP2$) and third order intercept point ($IP3$) are other two commonly used parameters that represents the linearity performance of the amplifier by using the second and third order intermodulation nonlinearity, respectively [1].

2.1.4.1 The 1-dB Compression Point

A nonlinear system can be approximated as:

$$y = a_1 x + a_2 x^2 + a_3 x^3 + \dots \tag{2.10}$$

given an input signal

$$x = A\cos(w_T t) \tag{2.11}$$

From equations 2.10 and 2.11, we can extend the output to be as follows:

$$y = \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos\left(w_T t\right) + \frac{a_2 A^2}{2}\cos(2w_T t) + \frac{a_3 A^3}{4}\cos(3w_T t) \tag{2.12}$$

From the above equations we can conclude that for sinusoidal input applied to a nonlinear system, the output exhibits frequency components that are multiples of the input frequency.

For most of circuits, a_3 is less than zero. Therefore, the fundamental gain ($a_1 A + \frac{3a_3 A^3}{4}$) will decrease as the input amplitude, A, increase which mean that the output failed to respond linearly with the input. Figure 2.8 shows that the 1-dB compression point is the point at which the input signal level causes the small signal gain to drop by 1 dB below its nominal value.

$$20\log \mid a_1 + \frac{3a_3 A_{1dB}^2}{4} \mid = 20\log \mid a_1 \mid -1 \tag{2.13}$$

$$IP_{1dB} = \sqrt{0.145 \mid \frac{a_1}{a_3} \mid} \tag{2.14}$$

2.1.4.2 The 3^{rd} Order Intercept Point

When two signals with different frequencies (also known as "two tones") are applied to a nonlinear system, many undesired components will be produced at the output because of

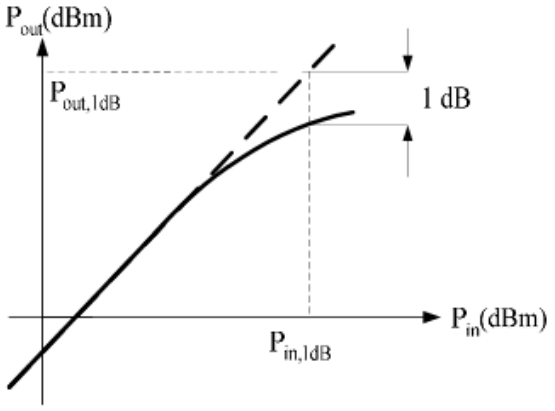

FIGURE 2.8: 1-dB compression point.

the harmonics and intermodulation of these two signals. Some of these undesired signals have frequencies that are very close to the desired signal. Moreover, in some cases like it is demonstrated in figure 2.9 the third order intermodulation products, IM3, of these signals can fall right on the frequency band of desired signal and degrade the overall performance of the system just like noise. The only difference between the distortion and the noise is that earlier component is a deterministic signal that can be eliminated using special techniques, such as dynamic biasing, feedback and feedforward techniques. But most of these techniques provides limited improvement due to the frequency dependency [1]. The following equations will give further illustration of the inter-modulation effect considering the nonlinear system defined by equation 2.10. Assume the two tones input signal is given by

$$x = A\big[\cos(w_1 t) + \cos(w_2 t)\big] \tag{2.15}$$

then the output will be

$$\begin{aligned} y = {} & a_1 A[\cos(w_1 t) + \cos(w_2 t)] \\ & + a_2 (A[\cos(w_1 t) + \cos(w_2 t)])^2 \\ & + a_3 (A[\cos(w_1 t) + \cos(w_2 t)])^3 + \dots \end{aligned} \tag{2.16}$$

extracting this equation gives the following terms:

$$y_{w_1} = \big(a_1 A + \frac{9 a_3 A^3}{4}\big) \cos(w_1 t) \tag{2.17}$$

$$y_{w_2} = \big(a_1 A + \frac{9 a_3 A^3}{4}\big) \cos(w_2 t) \tag{2.18}$$

$$y_{2w_1 \pm w_2} = \big(a_1 A + \frac{9 a_3 A^3}{4}\big) \cos(2w_1 \pm w_2) t \tag{2.19}$$

$$y_{2w_2 \pm w_1} = \big(a_1 A + \frac{9 a_3 A^3}{4}\big) \cos(2w_2 \pm w_1) t \tag{2.20}$$

If the desired input signal is at frequency w_o and it happens to satisfy $w_o = 2w_1 - w_2$, then the intermodulation product at $2w_1 - w_2$ will corrupt the signal as it falls directly above the desired channel which compromises the received signal quality. "Two-tone" test is a common method for the non-linearity characterization. Two sinusoidal signals with the same amplitude, A, are applied to the input. The power level of the applied tones to the system where their 3rd order inter-modulation product power becomes equal to the power of tones at the output of the system is defined as "input-referred third-order intercept point" ($IIP3$) of the amplifier. Since $IIP3$ is a weakly nonlinear measure of the system, it is calculated by extrapolation of data for lower distortion levels as shown in figure 2.10 [1].

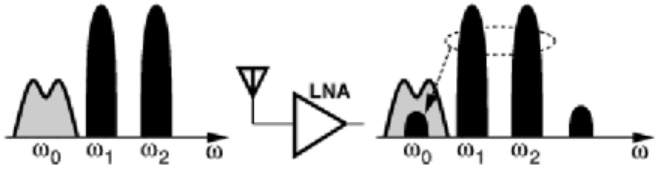

FIGURE 2.9: Intermodulation in a nonlinear system [1].

The value of $IIP3$ can be calculated in terms of the nonlinearity coefficients of the amplifier given in 2.10 as follows:

$$\mid a_1 IIP3 \mid = \mid \frac{3}{4} a_3 IIP3^3 \mid \tag{2.21}$$

$$IIP3 = 20 \log \sqrt{\frac{4}{3} \mid \frac{a_1}{a_3} \mid} \tag{2.22}$$

For a multi-stage system, the $IIP3$ of the system is expressed as:

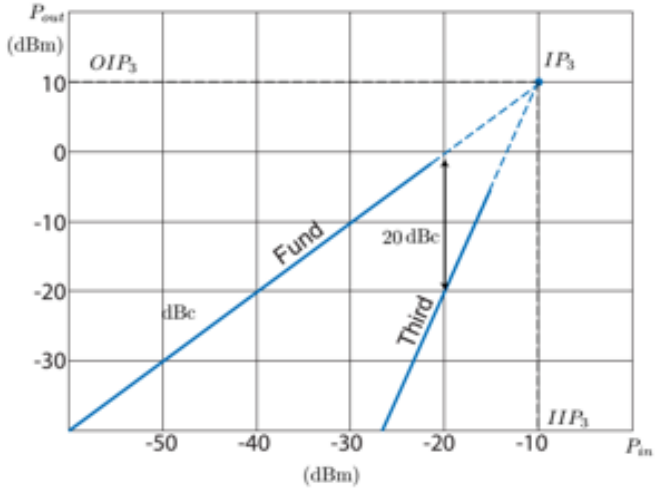

FIGURE 2.10: Intercept point for $IIP3$.

$$\frac{1}{IIP3_{sys}} = \frac{1}{IIP3_1} + \frac{A_1}{IIP3_2} + \frac{A_1 A_2 \dots A_{N-1}}{IIP3_N} \tag{2.23}$$

where $IIP3_i$ and A_i $(i = 1, 2, \dots N)$ are the $IIP3$ and the available power gain of the i^{th} stage, respectively. In order to have a better insight about the linearity performance of a bandwidth limited (narrowband) receiver and determine the bottlenecks along the chain in terms of linearity, $IIP3$ (two-tone test) are applied in two different conditions: in-band and out-of-band $IIP3$. In-band signals are the signals fall within the desired signal band and processed with the highest gain along the chain, which makes the linearity of the last stage of the receiver more important as can be shown in equation 2.23.

On the other hand, out-of-band $IIP3$ scenario uses the signals that fall beyond the desired signal bandwidth. Due to the narrowband response of the system, out-of-band signals are attenuated in each stage (i.e effectively lower or negative gain), which makes the linearity of the first stage blocks more important. Indeed, due to the frequency allocation, most of the large blockers in a wireless system exist at higher frequency offsets (like TV signals for GSM network). Thus, linearity of the LNA plays an important role in the overall linearity performance of the system.

2.1.4.3 The 2^{nd} Order Intercept Point

Similar to $IIP3, IIP2$ is also defined according to a two-tone test applied to a non-linear system. By extracting equation 2.16, a second order intermodulation, $IM2$, component arises and causes linearity problems.

$$y_{w_1 \pm w_2} = a_2 A^2 \cos(w_1 \pm w_2) \tag{2.24}$$

Equation 2.24 shows that the amplitude of this component is rising by double of the slope of the fundamental component on log scale. $IIP2$ is the power level of the applied tones to the system where their 2^{nd} order inter-modulation product power becomes equal to the power of tones at the output of the system as shown in figure 2.11.

The $IIP2$ problem in LNA is mainly due to the $IM2$ products $(w_1 \pm w_2)$ that fall within the desired RF signal bandwidth. Especially, the blockers at $F_{TX} \pm F_{RX}$ mix with the large TX signal (transceiver own signal) and create a tone within the desired RF signal bandwidth that lowers the signal quality of the receiver. Futhermore, $IM2$ components that fall within the IF band of the receiver as shown in figure 2.12 can lower the signal quality of the receiver as well if they are not eliminated at the output of the LNA by using a high pass filter. Since, LNAs are generally AC-coupled to the mixers in narrowband receivers, high pass filter characteristics occur without any extra cost. However, this issue still requires extra caution for wide-band receivers. Generally $IIP2$

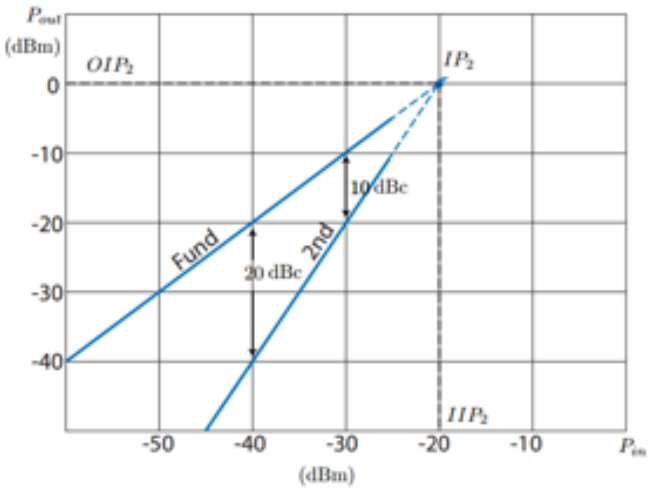

FIGURE 2.11: Second-order intercept point.

performance of a single ended LNA is much worse than the $IIP3$ performance. Thus, this makes the use of differential and well-matched LNA necessary. Using differential LNAs, ideally, achieve infinite $IIP2$ because of the symmetry of the circuit. In reality, however, asymmetry of the circuit due to some random mismatch causes the $IIP2$ to be finite but still quite high. Nonetheless, a differential LNA requires a differential input, thus doubles the number of pins and matching components along with the necessity of single ended to differential signal conversion from the antenna port. An off-chip or on-chip balun transformer can be used to convert the single ended antenna to differential input LNA; off-chip balun are low loss and have less effect on the noise figure of the circuit but they consume large area and have higher cost. On the other hand, on-chip baluns have higher loss and difficult to design. Fortunately, most of the duplexers that are used to provide separation between the RX and TX paths already provide a single-ended to differential conversion from the antenna port to the RX inputs. However, differential LNA still requires two pins on the package and higher number of matching components which is one of the bottlenecks for the next-generation wireless standards as the number of frequency bands and consequently narrowband LNAs constantly increases.

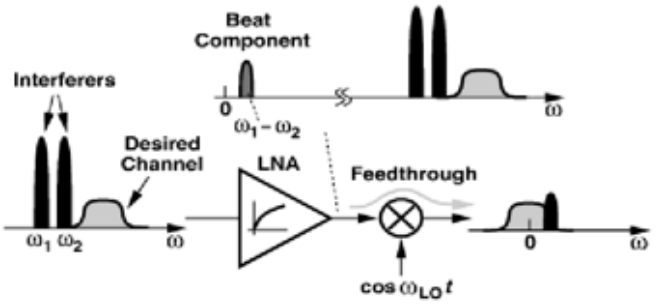

FIGURE 2.12: Effect of even-distortion on direct conversion [1].

2.2 LNA Topologies

This section presents a comparative study of some of the state-of-art LNA design and investigation about the pros and cons of each topology.

2.2.1 Conventional Common Source Topology

A common-source (CS) LNA is one of the most widely used architectures in RF design. This architecture can achieve a remarkable gain while keeping the noise figure at a very low levels. Matching the input at the gate of the transistor in CS-LNA can be achieved by using a source degeneration inductor which produces a real impedance that can be matched to the antenna impedance by proper biasing and sizing as we will discuss later. The main drawback of this topology is the area consumption. The on-chip inductors used for loading and degenerating purposes occupy a huge area on the silicon while the off-chip inductor used to improve the matching between the antenna and the input increases the area of the PCB. Furthermore, most of the time designers have to use both internal and external components to provide a sufficient matching at the frequency of interest. Beside this, the use of inductors in matching causes the input impedance to be frequency dependent which makes it a narrowband LNA. Furthermore, because of the huge increase in demand of multi-standard receivers the number of used LNA in a single receiver increases to satisfy this variety in frequency bands which requires reduction in area and power consumption. This topology introduces a trade-off between the performance (i.e. noise figure and gain) and the cost (i.e the area of chip and PCB).

Input matching

The input impedance of the CS LNA that has a source degeneration inductor as shown in figure 2.13 can be written as follows:

$$V_x = \frac{I_x}{sC_{gs1}} + (I_x + g_m V_{gs}) sL_1 \tag{2.25}$$

$$V_g s = \frac{I_x}{sC_{gs1}} \tag{2.26}$$

$$Z_i n = \frac{V_x}{I_x} = \frac{1}{sC_{gs1}} + sL_1 + \frac{g_m L_1}{C_{gs1}} \tag{2.27}$$

where C_{gs1} and g_m are the parasitic gate-to-source capacitance and the trans-conductance of M_1, respectively. Equation 2.27 shows that input matching can achieved by setting the real part of it $\left(\frac{g_m L_1}{C_{gs}}\right)$ to be equal to R_s. In recent technologies, the desired value of the degeneration inductor is very small and it can not be implemented with these small values. Practically, this inductance can be realized using the bond wires between

the chip and the pad in the package. However, this inductance can still be higher than the required values for certain frequency bands. To obtain a 50Ω impedance an external parallel capacitor to the gate-to-source capacitor, C_{gs}, of the transistor is connected to reduce the value of the transit frequency, w_T, which is given by $w_T = \frac{g_m}{C_{gs}}$.

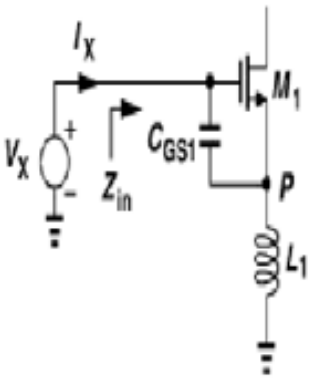

FIGURE 2.13: Input impedance of inductively-degenerated CS stage [1].

Noise figure

One of the main advantage of the CS LNA with inductive degeneration is its low noise. The NF is mainly dominated by the thermal noise of the input transistor. Furthermore, the use of external matching network provides slightly higher gain than unity, which improves the noise and gain performance of the CS LNA. NF can be calculated with the following equations neglecting the channel-length modulation effect, body effect, and C_{GD} for simplicity.

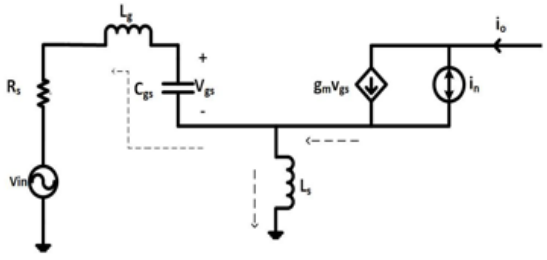

FIGURE 2.14: Equivalent circuit for NF analysis.

$$V_{in} = V_{gs}sC_{gs}(R_s + sL_g) + V_{gs} + sL_s(I_o + V_{gs}sC_{gs}) \tag{2.28}$$

$$I_o = g_m V_{gs} + i_n \tag{2.29}$$

substituting for V_{gs} from equation 2.29 in equation 2.28:

$$V_{in} = sL_s I_o + \frac{1 + s^2 C_{gs}(L_s + L_g) + R_s sC_{gs}}{g_m(I_o - i_n)} \tag{2.30}$$

where $1+s^2C_{gs}(L_s+L_g)=0$ at resonance frequency, w_o, at the best matching condition.

$$V_{in} = jI_o(L_s w_o + R_s\frac{C_{gs}}{g_m w_o}) - ji_n R_s\frac{C_{gs}}{g_m}w_o \tag{2.31}$$

We can calculate the output noise current by setting $V_{in}=0$ in equation 2.31:

$$I_{o,n} = i_n\frac{R_s}{\frac{g_m L_s}{C_{gs}}+R_s} \tag{2.32}$$

From the input matching requirement $R_s=\frac{g_m L_s}{C_{gs}}$, we get:

$$I_{o,n}^2 = KT\gamma g_m \tag{2.33}$$

From equation 2.31, the trans-conductance of the circuit can be derived as follows:

$$\frac{I_o}{V_{in}} = \frac{g_m}{w_o C_{gs}}\frac{1}{2R_s} = \frac{w_T}{w_o}\frac{1}{2R_s} \tag{2.34}$$

where $w_T=\frac{g_m}{C_{gs}}$ is the transit frequency. From the equations above we get that the noise figure of the CS LNA with inductive degeneration:

$$NF = 1+\frac{kT\gamma g_m}{4kTR_s}\left(\frac{2R_s w_o}{w_T}\right)^2 = 1+g_m R_s\gamma\left(\frac{w_o}{w_T}\right)^2 \tag{2.35}$$

Looking at the output node, we can use resistive or inductive load. Both of these strategies have their own pros and cons. The resistive load will have a smaller area consumption but on the other hand it will produce noise that will be added to the noise of the input transistor and causes an increase in the noise figure of the circuit.

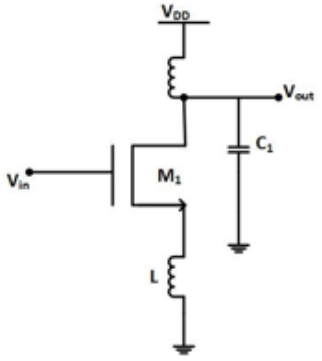

FIGURE 2.15: Inductive load and degeneration CS stage.

Another issue is that using a passive resistance at the output will make the circuit operate at a lower frequency because of the bandwidth specified by the feedback capacitance between the gate and drain, C_{GD}. For the new technologies and as the voltage supply is

getting lower, the gain will decrease as stated in equation 2.36.

$$\mid A_v \mid = g_m R_D = \frac{2I_D}{V_{ov}} \frac{V_{RD}}{I_D} = \frac{2V_{RD}}{V_{ov}} \tag{2.36}$$

Alternatively, when using an inductor load the voltage drop across it is ideally zero which is suitable for operating with lower voltage supply as it provides higher headroom and consequently better linearity especially for in-band blockers. Moreover, as discussed in section 2.1.1.3 the inductor does not produce noise (ideally) which helps the designer to lower the noise figure as much as possible. The drawback of this inductive load is it consumes a huge area on chip and it may cause an instability issue by resonating with the gate-to-drain capacitance (feedback capacitance), C_{GD}, and produce a negative resistance at some frequencies.

To overcome the instability and poor isolation between the input and output, cascode transistor is used. This transistor provides a good isolation between the input and the output by reducing the miller capacitance effect of the feedback capacitor between the input and output, Cgd, as described in equations 2.37 and 2.38. The input capacitance introduced by the miller effect on the capacitor C_{gd} in a CS configuration without cascode is higher than its counterpart when using cascode transistor since $\mid A_{v,CS} \mid = g_{m,CS} R_L$ in the following formula.

$$C_{Miller,CS} = (1 + \mid A_{v,CS} \mid) C_{GD} \tag{2.37}$$

$$C_{Miller,Cascode} = (1 + \mid A_{v,Cascode} \mid) C_{GD} = 2C_{GD} \tag{2.38}$$

The cascode device enhances the stability of the system as well since it reduces the loop gain that is formed by the feedback capacitor of CS LNA. The noise added by cascode transistor can be generally neglected at frequency of operation since it has a path to the ground through a low impedance produced by the gate to source capacitance, C_{gs}, of the cascode device as shown in figure 2.16.

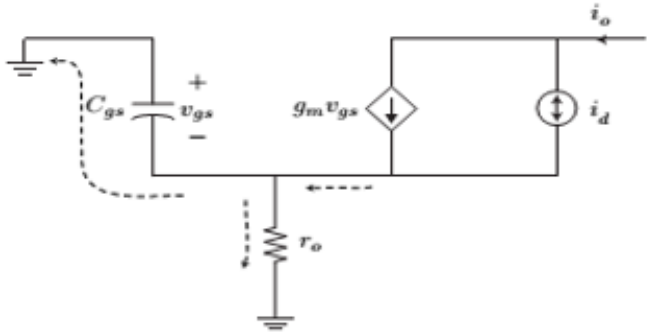

FIGURE 2.16: Noise contribution of cascode device [1].

The design presented in [4] is conventional cascode common source LNA with two on-chip inductors used as a load impedance and source degeneration. Figure 2.17 shows

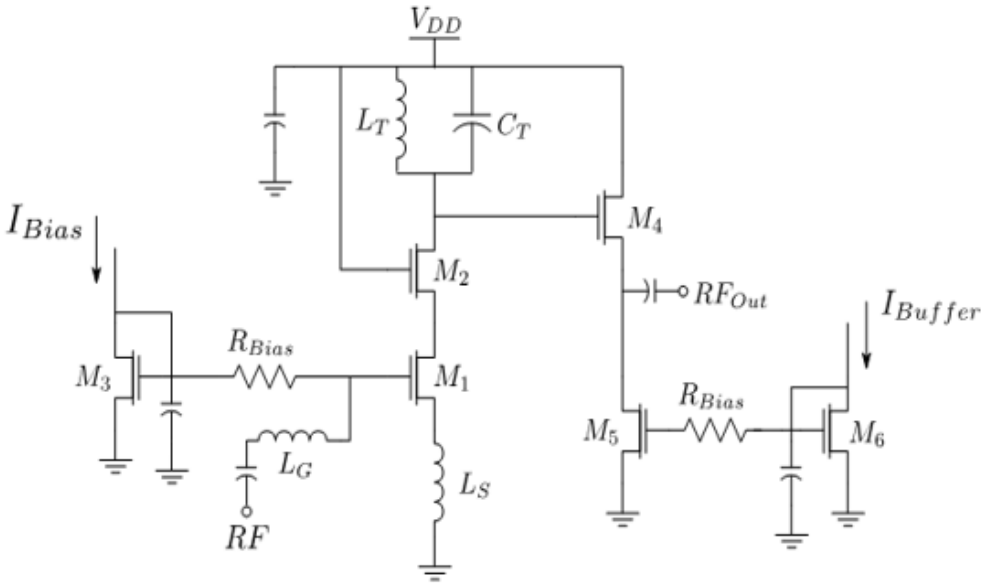

FIGURE 2.17: Proposed design in [4].

that this design consists of three stages: input matching network, core amplifier, and output buffer to match the output impedance. L_G and L_S are used for matching and their values are chosen according to equation 2.27 to achieve an operating frequency $w_o = \frac{1}{\sqrt{C_{gs}\left(L_g+L_s\right)}}$. The parasitic resistance of the degeneration inductor L_S will degrade the gain and produce a thermal noise added to the noise figure of the circuit. However, the linearity will be better because it will act as a feedback as shown in equation 2.39

$$\mid A_v \mid = \frac{g_m Z_L}{1 + g_m Z_s} \tag{2.39}$$

where Z_L is the load impedance and Z_S is the degeneration impedance at the frequency of interest. The core of the amplifier consists of two transistors, M_1 and M_2, and the output tank circuit (C_T and L_T) that resonates at the frequency of interest. The cascode device, M_2, is used to reduce the Miller effect on capacitor C_{GD1} between the gate and drain of the common source stage by reducing the voltage gain of this stage to approximately $\frac{g_{m,s1}}{g_{m,s2}}$ which make this design more stable in higher frequency due to the isolation between output and input. M_4 and M_5 are used as a buffer to match the output impedance to a 50Ω impedance. The diode connected devices, M_3 and M_6, are used for mirroring the current and bias the core amplifier and output buffer. The design in this article implemented in $0.18\mu m$ CMOS technology and operates at $2.4GHz$ and has a gain of $14.5dB$ while achieving a $2.8dB$ noise figure and $-7.8dBm$ $IIP3$. It occupies an area

of $0.15mm^2$ and consumes a power of $5mW$ for the core of the amplifier from a $1.8V$ voltage supply.

2.2.2 Conventional Common Gate Stage

Common Gate, CG, stage is more attractive in LNA design because of its resistive input impedance that makes it easy to match the input to a 50Ω antenna without a need of an external matching component which reduces the cost of the overall system design. Furthermore, since it is not necessary to use any extra frequency dependent component such as inductors and capacitors for the impedance matching, the design becomes a wideband design and provides a very good power transfer from antenna to the LNA for a wide frequency range. This advantage has a great benefit in the wireless communication systems nowadays because of the multi-standard requirements in the receiver design. The main drawback is its high noise figure compared to the common source topology.

Input Impedance

The input impedance of the CG is $R_{in} = \frac{1}{g_m}$ neglecting the channel length modulation and body effect. Thus, the LNA can be matched with a proper sizing of the input transistor to have $R_s = \frac{1}{g_m} = 50\Omega$. This analysis is based on neglecting the channel-length modulation and C_{gs} capacitance which will affect the input impedance at in high frequencies. The input impedance of the CG in the presence of r_o is given by equation 2.41 and shown in figure 2.18. This equation shows that the input impedance is a function of load impedance as well higher than 50Ω since a higher load impedance is desired for higher gain.

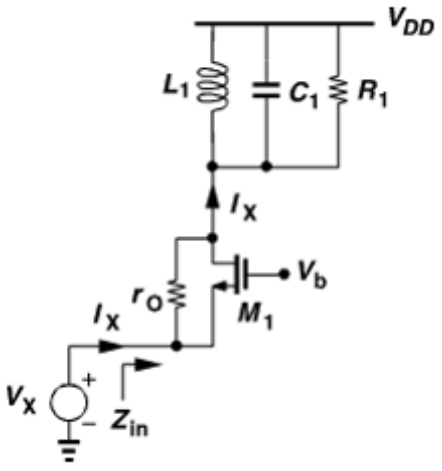

FIGURE 2.18: Input impedance of CG stage [1].

To overcome this issue, a cascode device is used to increase the output-input isolation of the amplifier and make its gain less dependent on the output load. This will also give us more freedom on satisfying the matching requirements while increasing the gain of the amplifier and as a result of this the input impedance will be lower. The input impedance of the cascode CG stage is given by equation 2.42

$$V_X = r_o(I_X - g_m V_X) + I_X R_1 \tag{2.40}$$

$$Z_i n = \frac{R_1 + r_o}{1 + g_m r_o} \tag{2.41}$$

$$R_{in} \approx \frac{1}{g_{m1}} + \frac{R_1}{g_{m1} r_{o1} g_{m2} r_{o2}} + \frac{1}{g_{m1} r_{o1} g_{m2}} \tag{2.42}$$

The last two terms in equation 2.42 are neglected since $g_{m1} r_{o1} g_{m2} r_{o2} \gg R_1$ and $\frac{1}{g_{m1}} \gg \frac{1}{g_{m1} r_{o1} g_{m2}}$. Thus, $R_{in} \approx \frac{1}{g_{m1}}$. As a reminder, the impedance due to the C_{gs} and the source inductor (in case an in inductor is used to provide DC current path) are not included. These two impedances may have significant effects on the input impedance depending on the frequency of operation.

Noise Figure

For the NF analysis of CG stage, the thermal noise of M_1 is modeled as a voltage source at the gate of the transistor, $\overline{V_{n1}^2} = \frac{4kT\gamma}{g_m}$. The output noise of the circuit due to M_1

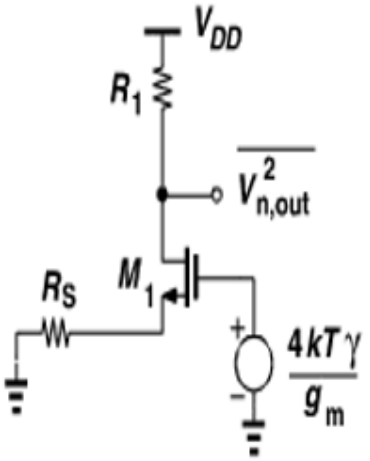

FIGURE 2.19: Noise analysis of CG-LNA [1].

and R_1 is given by equation 2.43

$$\overline{V_{n,out}^2} = \frac{4kT\gamma}{g_m}\left(\frac{g_m R_1}{1 + g_m R_s}\right)^2 + 4kTR_1 \tag{2.43}$$

$$NF = 1 + \frac{1}{4kTR_s}\frac{\overline{V_{n,out}^2}}{A_v^2} \tag{2.44}$$

where A_v is the gain from the antenna to the output of LNA given, at perfect matching condition, by equation 2.45

$$A_v = \frac{1}{2} g_m R_1 \tag{2.45}$$

$$NF = 1 + \gamma + \frac{4R_s}{R_1} \tag{2.46}$$

From equation 2.46, the NF of CG stage is at least $3dB$ (with $\gamma \approx 1$) if $\frac{4R_s}{R_1} \ll 1+\gamma$. Using cascode device will not affect the noise figure that much because the noise contribution of the cascode device can be neglected since the input transistor acts as a degeneration as shown in figure 2.16.

The proposed design in [7] is an inductorless gm-boosted common gate LNA. This design consists of two common gate amplifiers, one of them is the main input amplifier consists of a CG transistor and a passive resistive load and the other one acts as a gm-boosted amplifier as shown in figure 2.20.

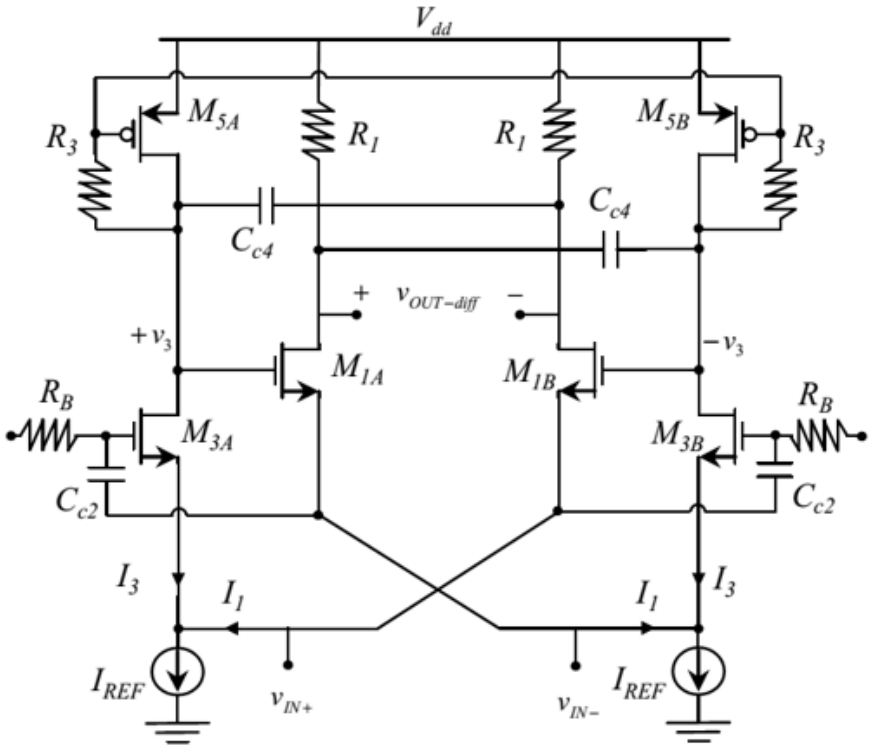

FIGURE 2.20: The proposed design presented in [7].

The two capacitors, C_{C2}, are used for cross coupling to boost the gm-boost amplifier without extra DC power consumption, P_{dc}. The diode connected transistors, M_{5A} and M_{5B}, are used to avoid an excessive voltage drop through the load resistor R3. CC4 capacitors cancel the effect of the C_{GD} of M_{1A-B} transistors and enhance the gain bandwidth of the circuit. To ensure stability of the LNA, the value of these capacitors, C_{C4}, must be carefully chosen. The equivalent gain and input impedance of the design

are given in equations 2.47 and 2.48 where C_{C2} assumed as an AC short circuit in high frequency.

$$A_v \approx g_{m1}R_1(1 + 2g_{m3}R_3) \tag{2.47}$$

$$Z_{in} \approx \frac{1}{(g_{m1}(1 + 2g_{m3}R_3) + 2g_{m3})} \tag{2.48}$$

This design has been implemented in $0.13\mu m$ CMOS technology achieves a gain of $20dB$ with a noise figure of $4dB$ and $IIP3$ $-12dBm$. It consumes $1.32mW$ in an area of $0.007mm^2$.

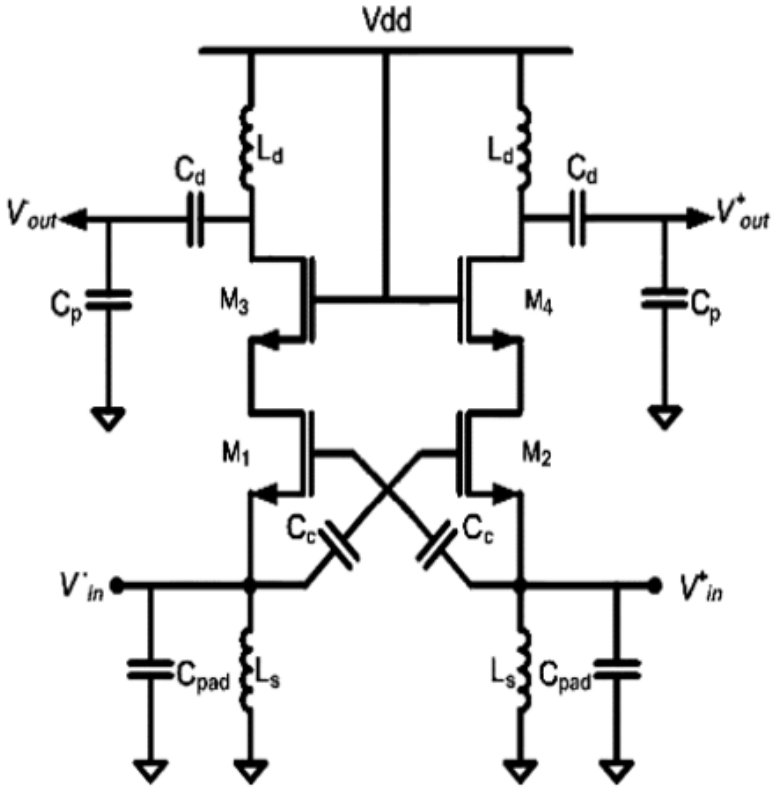

FIGURE 2.21: The proposed design presented in [8].

The paper in [8] presents a common gate LNA with a capacitive-cross coupling to improve the noise figure and reduce the power consumption without degrading the linearity and stability of the conventional common gate amplifier. The circuit shown in figure 2.21 presents the CCC-CGLNA introduced in [8]. This circuit designed and implemented in $180nm$ RF CMOS process and operates at a frequency of $6GHz$. M_1 and M_2 are two input transistors biased and sized properly to a get a good input matching. The cascode transistors, M_3 and M_4, are used to increase the gain and enhance the reverse isolation between output and input. The two capacitors, C_C, are used to cross couple M_1 and M_2. LS are two on-chip inductors used to tune out the total capacitances at the source of the

input transistors including the pad capacitances. This design achieves a gain of $7.1dB$ and a noise figure of $3dB$. The measured $IIP3$ is $11.4dBm$ and the power consumption is $6.48mW$ from a $1.8V$ supply voltage. The area consumption is $0.95mm^2$ including pads.

Hybrid Common Source – Common Gate LNA

A noise reduction and linearity improvement technique for a differential cascode CS-LNA was proposed in [5]. The proposed circuit is shown in figure 2.22 , a cascode CS-LNA treated as CS-CG two stage amplifier.

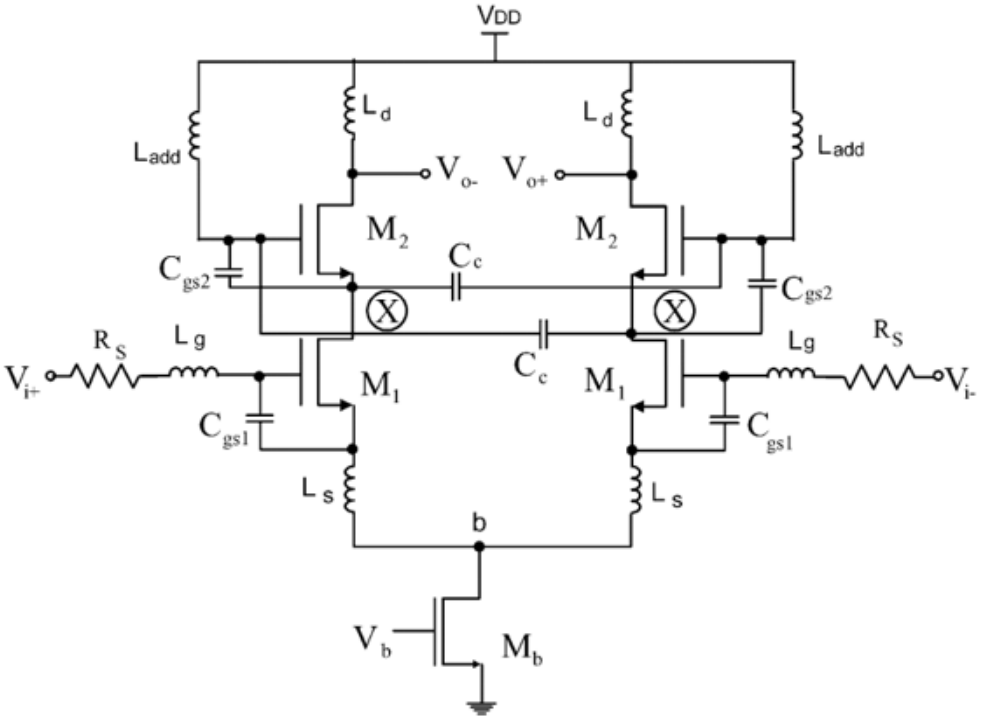

FIGURE 2.22: The proposed design presented in [5].

The first stage as a convention CS amplifier with the source inductive degeneration. The cascode device acts as a second stage CG amplifier. This CG stage is implemented with a capacitive cross-coupled technique using two capacitors, CC, connected between the source and gate of the cascode devices as shown in figure 2.23.

The inductors, L_s, shown in this figure is substituted by an inductor, L_{add}, connected to the gate of the transistor in this proposed design. Those inductors are added to reduce the noise and nonlinearity contributions of the cascode transistors. The inductor L_{add} is implemented as a bonding wire inductor. The capacitive cross-coupling boost the transconductance of the cascode transistors .

$$G_{m,eff} = \frac{2C_C}{C_{gs} + C_C} g_{m1} \tag{2.49}$$

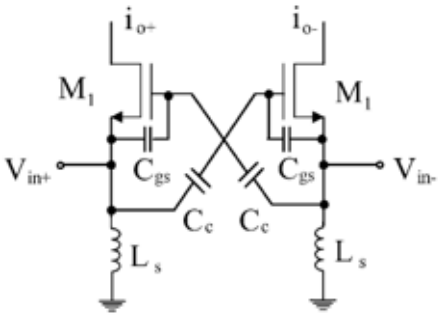

FIGURE 2.23: CCC CG-LNA schematic in [5].

when $C_C \gg C_{gs}$, the effective transconductance is doubled, and the input capacitance at the source of the CG stage is increased by 4 times [5].

$$C_{in} = 2\frac{G_{m,eff}}{g_{m1}}C_{gs} \tag{2.50}$$

The design was implemented in TSMC $0.35\mu m$ CMOS technology achieving power gain of $8.6dB$ at $2.2GHz$ and noise figure equals $1.92dB$ with $IIP3$ $-2.55dBm$ consuming $16.2mW$ in an active area of $1.3mm^2$.

2.2.3 Active/Passive Feedback LNA

Inductor-less LNAs are generally based on common-gate or shunt-feedback topologies. A feedback can be used with a CS stage to match the input impedance using the transconductance of the input amplifier if the frequency of operation is lower than the transit frequency, f_T, of the transistor by an order of magnitude. The feedback device can be passive or active. The passive feedback does not consume power which makes it a good alternative in low power designs. Figure 2.24 shows the simplest CS stage with resistive feedback LNA. Neglecting the channel-length modulation, the input impedance of this circuit can be given by

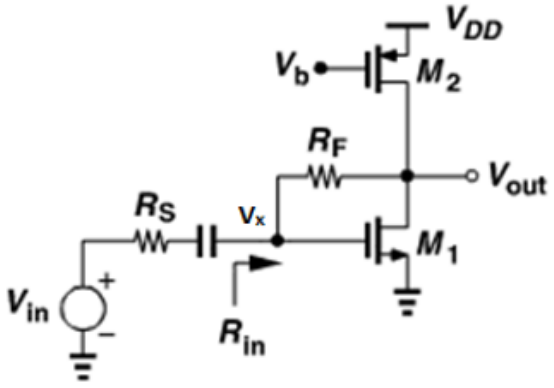

FIGURE 2.24: CS stage with resistive feedback.

$$\frac{V_x - V_{out}}{R_f} = g_{m1} V_x \tag{2.51}$$

$$\frac{V_{out}}{V_x} = 1 - g_{m1} R_f \tag{2.52}$$

$$I_{in} = \frac{V_{out} - V_x}{R_f} = \frac{1 - g_{m1} R_f - 1}{R_f} V_x \tag{2.53}$$

$$R_{in} = \frac{1}{g_{m1}} \tag{2.54}$$

For perfect matching, the gain of the amplifier becomes

$$A_v = \frac{1}{2}\left(1 - \frac{R_f}{R_s}\right) \tag{2.55}$$

The noise figure of this topology is given in [1] by equation 2.56:

$$NF = 1 + \frac{4R_s}{R_f} + \gamma + \gamma g_{m2} R_s \tag{2.56}$$

From the above equation, the NF exceeds $3dB$ for $\gamma \approx 1$ even if $\frac{4R_s}{R_f} + \gamma g_{m2} R_f \ll 1$.

The design shown in Figure 2.25 is an inductor-less low noise amplifier that is presented in [9] and implemented in $90nm$ CMOS using resistive feedback and non-linearity cancellation.

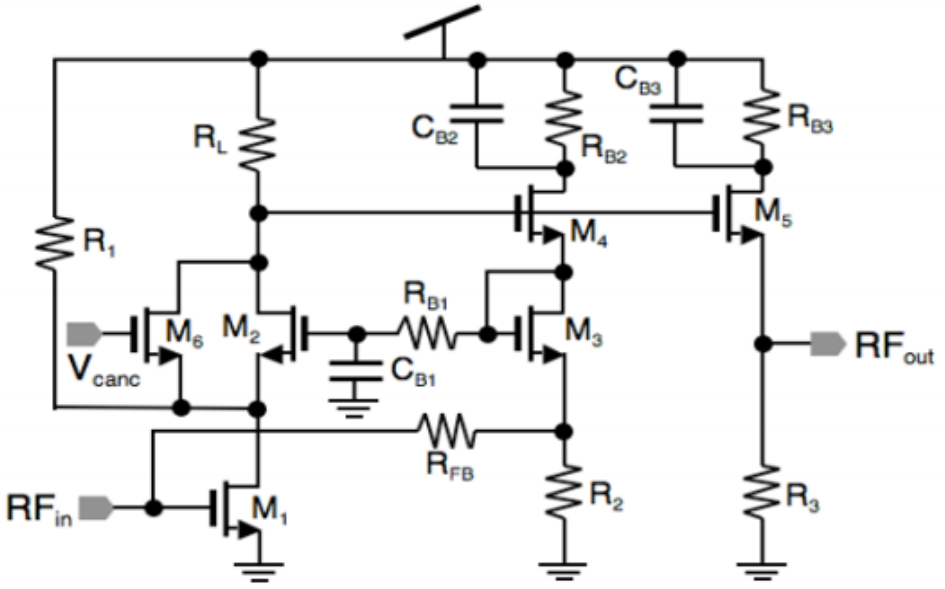

FIGURE 2.25: The proposed schematic of resistive feedback LNA with non-linearity cancellation [9].

Transistors M_1, M_2 and resistor R_1 form a gm-enhanced cascode amplifier. The output is fed back to the input through a source follower M_4, a level shifter M_3, and the feedback

resistor R_{FB}. The level shifter M3 is used to bias the gm-enhanced cascode by forming a DC feedback loop. To cancel the $IP3$ limiting non-linearity of transistor M2, transistor M_6 is used with a little effect on the gain and input matching of the LNA. M_5 and R_3 are used to drive a 50Ω output buffer. This design operates from 0.5 – 7.25GHz achieving gain of 25.2dB with NF less than 2.5dB and OIP3 13dB in low noise mode. In high linearity mode, the operation frequency range is 0.5 – 6.2GHz with gain 24.4dB and NF less than 3.1dB and OIP3 of 22dB. The power consumption is 42mW from a 2.7V supply in an active area of 0.016mm^2.

Multiple feedback paths are also used in some designs to have more flexibility in biasing and sizing the input and cascode transistors. The design presented in [10] and shown in figure 2.26 is using three feedback paths to boost the performance. The design is a

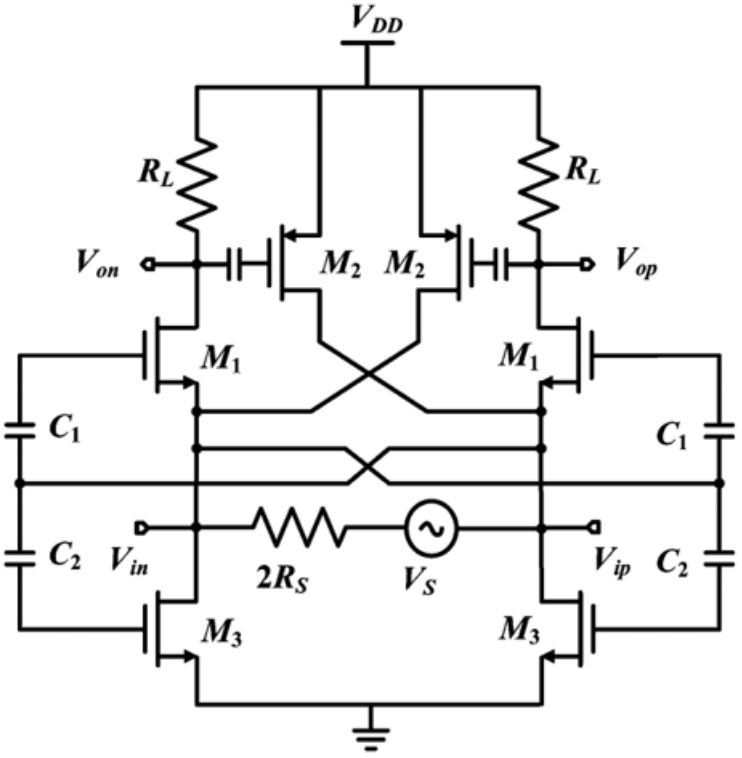

FIGURE 2.26: The proposed design presented in [10].

fully differential CG-LNA with multiple feedback paths. Using capacitive-cross coupling technique, indeed, increase the effective transconductance of the amplifier as described in one of the implemented designs discussed in section 2.2.2. But at the same time, restrict the value of transconductance to be 10mS for a 50Ω impedance matching which limit the gain. Another positive feedback loop can be added to the CCC CG-LNA to increase the gain by adding degree of freedom when choosing the value of the transconductance. This feedback is shown in the single ended model in figure 2.27 which the positive loop is implemented with M_2. By using this negative-positive feedback paths, the input

impedance of the design is increased to be

$$R_{in} = \frac{1}{g_{m1}(1 + A_{NEG})(1 - A_{POS})} \tag{2.57}$$

where $A_{POS} = g_{m2}R_L$ is the positive feedback gain, which varies from 0 to 1 for stability and $A_{NEG} \approx 1$ which comes from the capacitor ratio in the CCC technique.

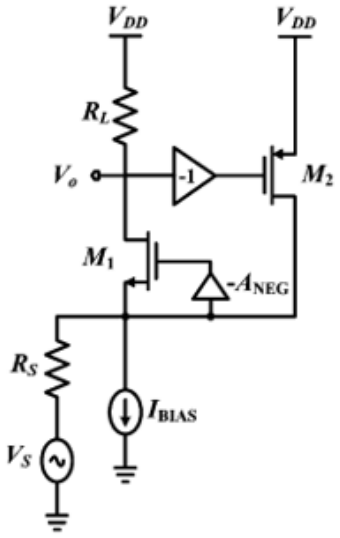

FIGURE 2.27: Negative-positive feedback in CG-LNA [10].

By this technique, the design overcomes the restriction of $g_{m1} = 10mS$ for an input impedance of 50Ω. The g_{m1} can be increased and, hence, increasing the gain. The main idea of the proposed design in [10] is to add another positive feedback path which add more flexibility on choosing the LNA transconductance that achieves the minimum noise figure. The capacitive cross coupled transistor, M_3, creates the second positive feedback path beside the one created by M_2 as shown in the single-ended model in figure 2.28. By this technique, the input impedance of the CG-LNA is increased and the input matching condition is given by

$$R_s = \frac{1}{g_m 1(1 + A_{NEG})(1 - A_{POS} - B_{POS})} \tag{2.58}$$

where $A_{NEG} = 1$, $A_{POS} = g_{m2}R_L$, and $B_{POS} = \frac{g_{m3}}{2g_{m1}}$. Thus, A_{POS} and B_{POS} give the flexibility of choosing g_{m1} that achieves high gain and optimum noise figure. A prototype of this design is fabricated in $90nm$ CMOS technology. The measured voltage gain is higher than $20dB$ in a frequency range 0.1 – $1.77GHz$. The minimum measured noise figure is $1.85dB$ and an $IIP3$ of $-2.85dBm$. The power consumption of the LNA is $2.8mW$ form a $2V$ voltage supply and it occupies an area of $0.03mm^2$.

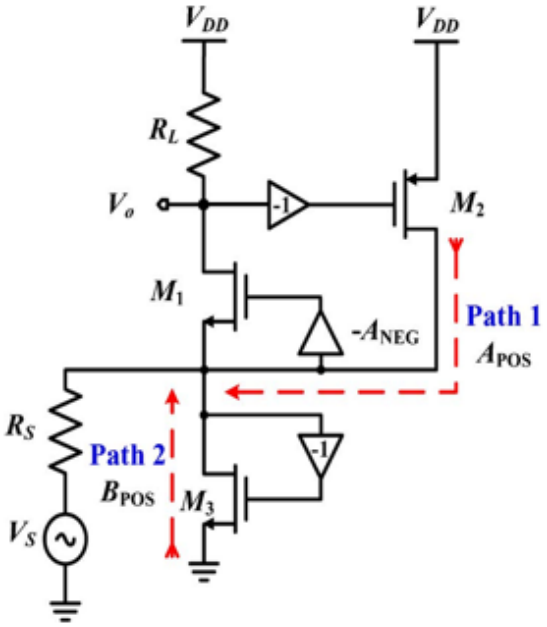

FIGURE 2.28: Simplified single-ended model of the proposed design [10].

2.2.4 Noise-Canceling LNA

From the analysis of the above topologies we found that the noise in the circuit comes from three main sources: the noise of R_S, the noise of the input transistor, and the noise of the resistive load whether it is active or passive load. The aim of this topology, noise-cancelling LNA, is to cancel the second term by identifying two nodes at which the signal is in-phase and the noise is out-of-phase and then sum their voltage with proper scaling such that the signal components add and the noise components cancel each other as demonstrated in figure 2.29. Figure 2.30 shows the implementation of the noise-

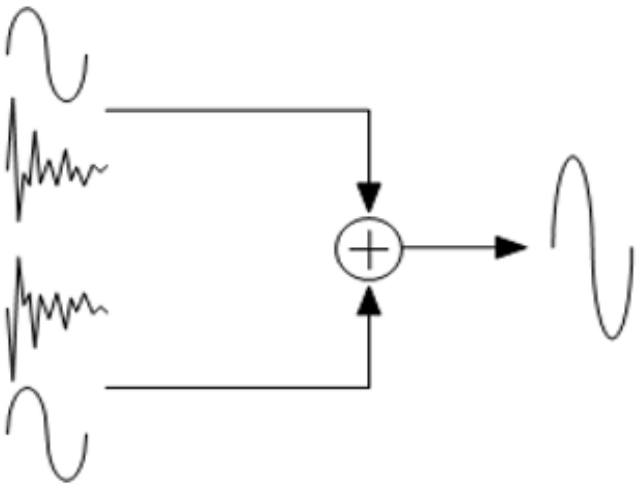

FIGURE 2.29: Conceptual illustration of noise cancelling [11].

cancelling LNA using one CS amplifier, one CS amplifier with resistive feedback, and a

source follower. The only path for I_{in} is through R_f which means that nodes X and Y will have out-of-phase signals due to the inverting amplifier and in-phase noise due to the path for the noise current from the gate of the transistor [11]. As discussed in the

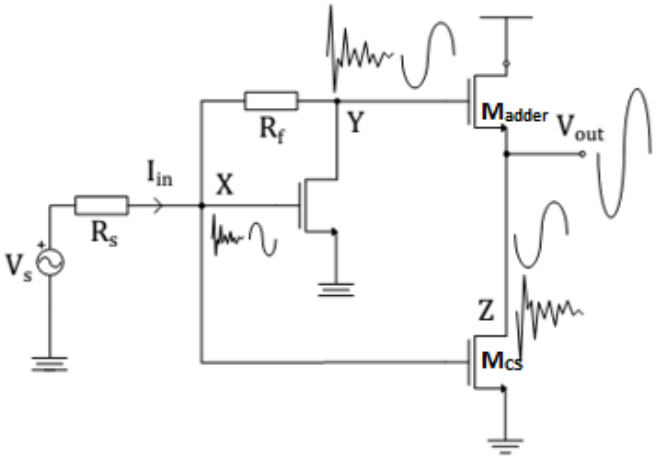

FIGURE 2.30: Noise cancelling LNA implementation [11].

previous section, the input impedance and the gain of the resistive feedback common source stage is given by equations 2.54 and 2.55 assuming perfect matching.
The total rms output noise voltage can be written as

$$V_{n,out} = V_{n,y} + V_{n,z} = V_{n,y} + A_{v2}V_{n,x} \tag{2.59}$$

$$V_{n,out} = I_n(R_f + R_s) + A_{v2}I_nR_s \tag{2.60}$$

To have a total noise-cancelling, $V_{n,out} = 0$.

$$A_{v2} = -\left(1 + \frac{R_f}{R_s}\right) \tag{2.61}$$

From Figure 2.30, the gain $A_{v2} = -\frac{g_{m,CS}}{g_{m.adder}}$ which gives the relation between M_{CS} and M_{adder} by the following equation

$$g_{m,CS} = g_{m,adder}\left(1 + \frac{R_f}{R_s}\right) \tag{2.62}$$

In [12] a wideband inductor-less LNA is presented. The design consists of a CG stage in parallel with a scaled-admittance CS stage. Figure 2.31 shows the proposed design presented in [12], the circuit inside the dashed box is implemented on silicon. The CS stage is scaled n-times up to lower the noise figure, the output impedance of the CG and CS stages are not equal because of that. Two source followers buffer, M_{SFCG} and M_{SFCS}, are used to balance the output impedance of those two stages. To get a balanced output operation, the DC level at the gate of the two buffers should be equal. To achieve this, a

scaled replica of CG stages are used to generate the DC level and a capacitor is used to AC-couple the output of the CS stage to its source follower. This design is implemented in $65nm$ CMOS process and it achieves a voltage gain of $15dB$ for frequency range from $100MHz$ to $2.5GHz$ with a NF below $3.5dB$ in an active area of $0.009mm^2$. A CG-CS

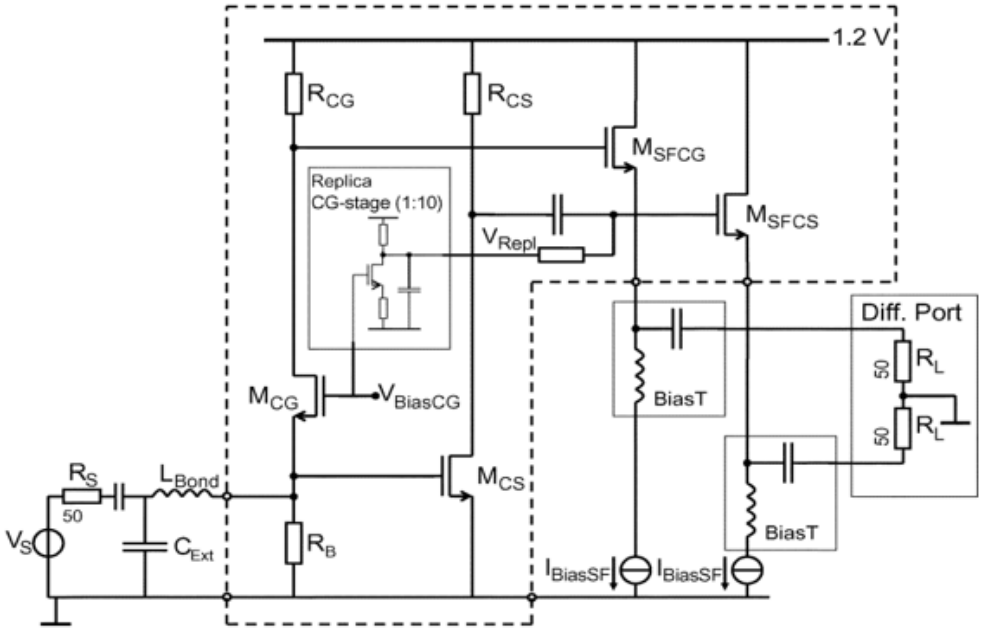

FIGURE 2.31: The proposed design presented in [12].

LNA is one of the most popular topologies in noise cancelling LNA. The idea behind it is simply emphasized in figure 2.32. The thermal channel noise current modeled

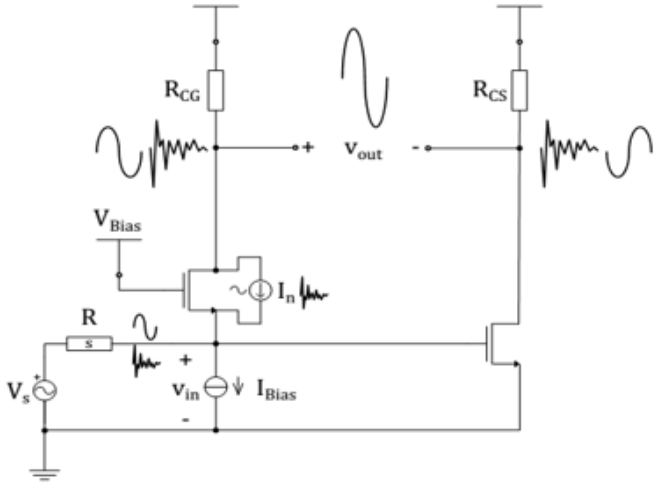

FIGURE 2.32: CG-CS noise cancelling LNA [11].

between the input and output of the common gate transistor creates two noise voltages at the output node of the CG device and the input node of the LNA. These voltages are correlated and out-of-phase. The inverting CS amplifier will invert the phase of the

noise voltage of the CG device presented at its input and since the output is differential, the noise will be cancelled.

$$v_{n,in} = \frac{Z_{in}}{Z_{in} + R_s} i_n R_s \tag{2.63}$$

$$v_{n,CG} = -\frac{Z_{in}}{Z_{in} + R_s} i_n R_{CG} \tag{2.64}$$

The output noise voltage, $v_{n,out}$ produced by the channel noise of the CG stage is given by

$$v_{n,out} = -\frac{Z_{in}}{Z_{in} + R_s} i_n R_{CG} - \frac{Z_{in}}{Z_{in} + R_s} i_n R_s A_{v,CS} \tag{2.65}$$

To have a full noise cancellation at the output, the gain of the common source stage is restricted to be

$$A_{v,CS} = -\frac{R_{CG}}{R_s} \tag{2.66}$$

The idea presented in [13] is mainly to use a local negative feedback between the parallel CG-CS LNA in the conventional noise-cancelling LNA. This feedback will lead to a higher gain and lower noise figure under low power and voltage constraints. Figure 2.33 shows the proposed design presented in this article. The g_m of M_2 is boosted by a factor

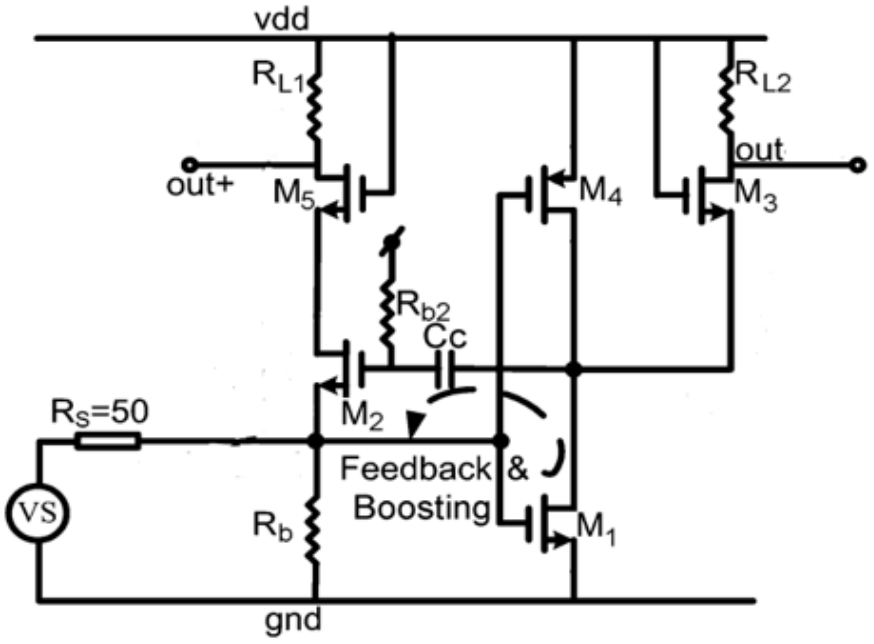

FIGURE 2.33: The proposed design presented in [13].

of $\left(1 + A_{VM}\right)$ where A_{VM} is the loop gain of the negative feedback loop and given by 2.67. Thus, the input impedance will be equal to $R_{in} = \frac{1}{g_{m2}\left(1+A_{VM}\right)}$. This boosting give the opportunity to reduce the transconductance of M_2, g_{m2}, which decrease the power consumption and noise figure.

$$A_{VM} = \frac{g_{m1} + g_{m4}}{g_{m3}} \tag{2.67}$$

The gain of this LNA will be increased to be

$$A_V = g_{m2}(1 + A_{VM})R_{L1} + (g_{m1} + g_{m4})R_{L2} \tag{2.68}$$

The design is implemented in $0.13\mu m$ RF CMOS process and achieved a measured gain of $19dB$ and a noise figure of $2.8 - 3.4dB$ over a $-3dB$ bandwidth of $0.2 - 3.8GHz$. The area consumed by the design is $0.025mm^2$ with a power consumption of $5.7mW$ from $1V$ supply voltage.

Table 2.1 shows a comparison between the different designs discussed in this section.

TABLE 2.1: Comparison between discussed designs.

Ref		Freq. Band [GHz]	NF [dB]	Gain A_v [dB]	IIP3 [dBm]	Power Consumption [mW]	Process	Area [mm^2]
[4]		2.4	2.8	14.5	-7.8	19.8	0.18μm	0.15
[5]		2.2	1.92	8.6	-2.55	16.2	TSMC 0.35μm	1.3
[7]		0.1-2.7	4	20	-12	1.32	0.13μm	0.007
[8]		6	3	7.1	11.4	6.48	180nm	0.95
[9]	High Linearity	0.5-6.2	2.1-3.1	24.4	22	42	90nm	0.016
	Low Noise	0.5-7.25	1.8-2.5	25.2	13			
[10]		0.1-1.77	1.85	23	-2.85	2.8	90nm	0.03
[12]		0.2-5.2	<3.5	13-15.6	>0	21	65nm	0.009
[13]		0.2-3.8	2.8-3.4	19	-4.2	5.7	130nm	0.025

Chapter 3

Low Noise Amplifier Design

In this project, two LNA designs have been implemented in UMC 65nm CMOS technology. One of them is the conventional cascode common source LNA with inductive degeneration and RLC tank load impedance. However, this architecture consumes large area due to the on- and off-chip inductors. It is preferable in wireless communication chips because of its high gain and low noise figure. The area consumption of CS LNA does not make it a good candidate in the multiband receivers as the number of LNAs in single chip is getting higher but it is still one of the most preferable topologies when it comes to narrowband receivers. The second design is a new approach common gate based design to reduce the area and power consumption while, at the same time, achieving a comparative performance. A negative feedback has been used in this design to boost the input transconductance which lead to an increase in the gain and decrease in noise figure as well. The boosted transconductance results in reducing the power consumption compared to the conventional common gate design.

3.1 Cascode Common Source with Inductive Degeneration LNA Design

This is the most common used topology in LNA design. It has been chosen due to its simplicity and high performance. CS-LNA can achieve a very high gain and low noise figure at the same time. However, the main drawback of it is its large area because of the on- and off-chip inductors used for degeneration, load, and matching purposes. A detailed analysis of this topology is given in section 2.2.1.

Input Impedance and Matching Network

The input impedance of the cascode CS stage with inductive degeneration inductor is discussed in details in section 2.2.1 and is given by equation 3.1.

$$Z_{in} = \frac{1}{sC_{gs}} + sL + \frac{g_{m1}L}{C_{gs}} \tag{3.1}$$

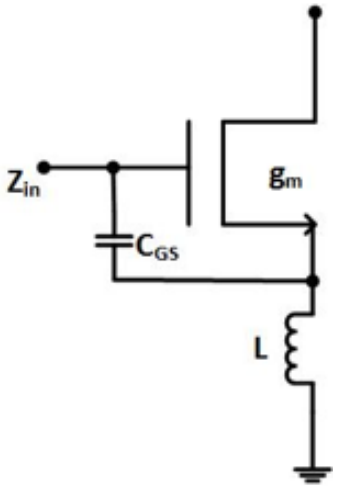

FIGURE 3.1: Input impedance of CS-LNA with inductive degeneration.

To obtain a good matching, T-matching network is used off-chip. The matching network consists of two inductors, one shunted, L_{in}, and one in series with the gate, L_g and one capacitor, C_{in}, in series with the gate to provide DC block for proper biasing of the LNA. Figure 3.2 shows the used network.

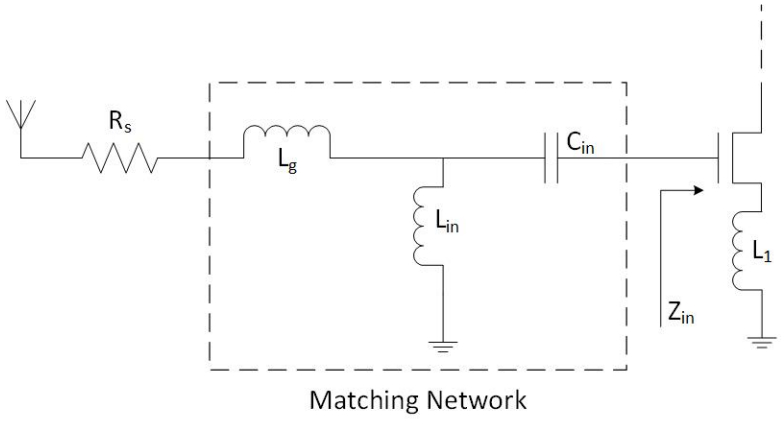

FIGURE 3.2: Off-chip matching network.

Gain

The gain of this circuit is given by

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{R_{in}}{R_{in} + R_s} g_{m1}(R_{out} \parallel Z_L) \tag{3.2}$$

$$R_{out} = r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2} \tag{3.3}$$

$$Z_L = \frac{1}{Y_L} = \frac{1}{\frac{1}{R_L} + jwC_L\left(1 - \frac{1}{w^2 LC_L}\right)} \tag{3.4}$$

Noise Figure

There are three sources of noise in this LNA, thermal noise from the input transistor and cascode transistor, M_1 and M_2 , and the other source is the load resistor, R_L, which produce a thermal noise as well. The flicker noise is neglected in the analysis since the design is operated at high frequency. The thermal noise of cascode device can be neglected because of the input transistor acts like a degeneration with high resistance, r_{o1}, to the cascode transistor so the noise produced by M_2 can be neglected with respect to other sources. Noise figure analysis has been described in details in section 2.2.1. The noise figure is given by equation 2.35. The off-chip matching network used in this design has a good impact in noise. It produces a gain slightly higher than unity from the antenna to the input of LNA which in return reduce the noise figure of the circuit.

Circuit Implementation

Figure 3.3 shows a simplified schematic of the proposed design. The LNA has chosen to be fully differential in order to increase the gain and decrease the even-order distortion of the input signals. M_1 and M_2 are the input CS-stage transistors while M_3 and M_4 are cascode transistors used to increase the gain, input-output isolation, and decrease the input capacitance as the Miller capacitance has been reduced. Equations 2.37 and 2.38 show how the cascode device can reduce the input capacitance by reducing the gain between the gate and drain of input transistor to be $A_{v,Cascode} = \frac{g_{m,CS}}{g_{m,cascode}}$.

L_1 is a differential inductor used for source degeneration. It lowers the gain of the LNA at high frequency as it acts like a negative feedback and thus improve the linearity. Furthermore it introduces the real part of the input impedance Z_{in}. This inductor is an on-chip inductor since its value is low.

The output impedance consists of a parallel RLC circuit which resonates at the frequency of operation allowing the gain to reach its peak value. A number of external control bits are used to control the values of output resistors and capacitors to change the gain of LNA and the resonant frequency of the load tank in order to maintain a good linearity for

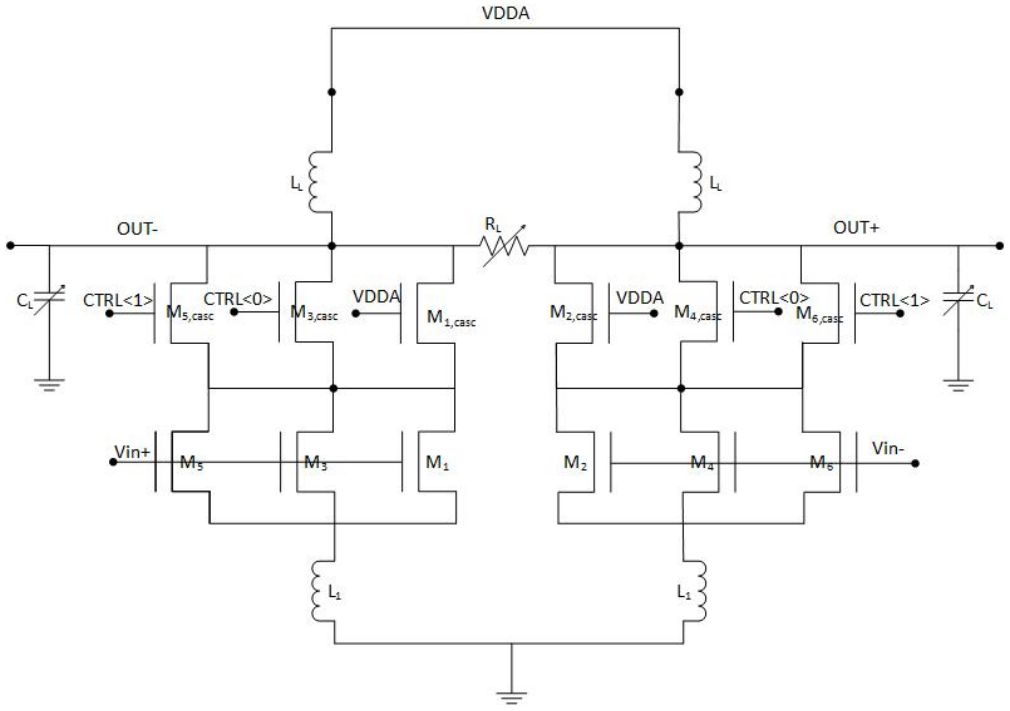

FIGURE 3.3: Simplified schematic for the proposed cascoded CS-stage LNA.

the overall receiver and maximize the selectivity of the LNA depending on the frequency of the desired signal being received. Another controllability is added to the design in order to reduce the power consumption of the circuit by reducing the effective width of the input transistors with the cost of reduced gain and increased NF. Figure 3.4 shows the complete proposed schematic.

The design is implemented in UMC $65nm$ CMOS technology and operates at a frequency of $1.9GHz$ (PCS band). It achieves a gain higher than $27dB$ and noise figure of $2.3dB$. The LNA consumes a power less than $5.5mW$ from a $1.2V$ supply occupying an area of $0.1mm^2$. The design parameters are summarized in table 3.1.

TABLE 3.1: Design parameters of CS-LNA.

Parameters	Value	Multiplier
M_1, M_2	$\frac{4.5}{0.06}\mu m$	8
M_3,M_4,M_5,M_6	$\frac{1.5}{0.06}\mu m$	8
$M_{1,casc}$, $M_{2,casc}$	$\frac{4.5}{0.06}\mu m$	8
$M_{3,casc}$, $M_{4,casc}$,$M_{5,casc}$, $M_{6,casc}$	$\frac{1.5}{0.06}\mu m$	8
R_L	$1.3 - 16K\Omega$	–
C_L	$100 - 300fF$	–
L_L	$13nH$	–
L_1	$1nH$	–

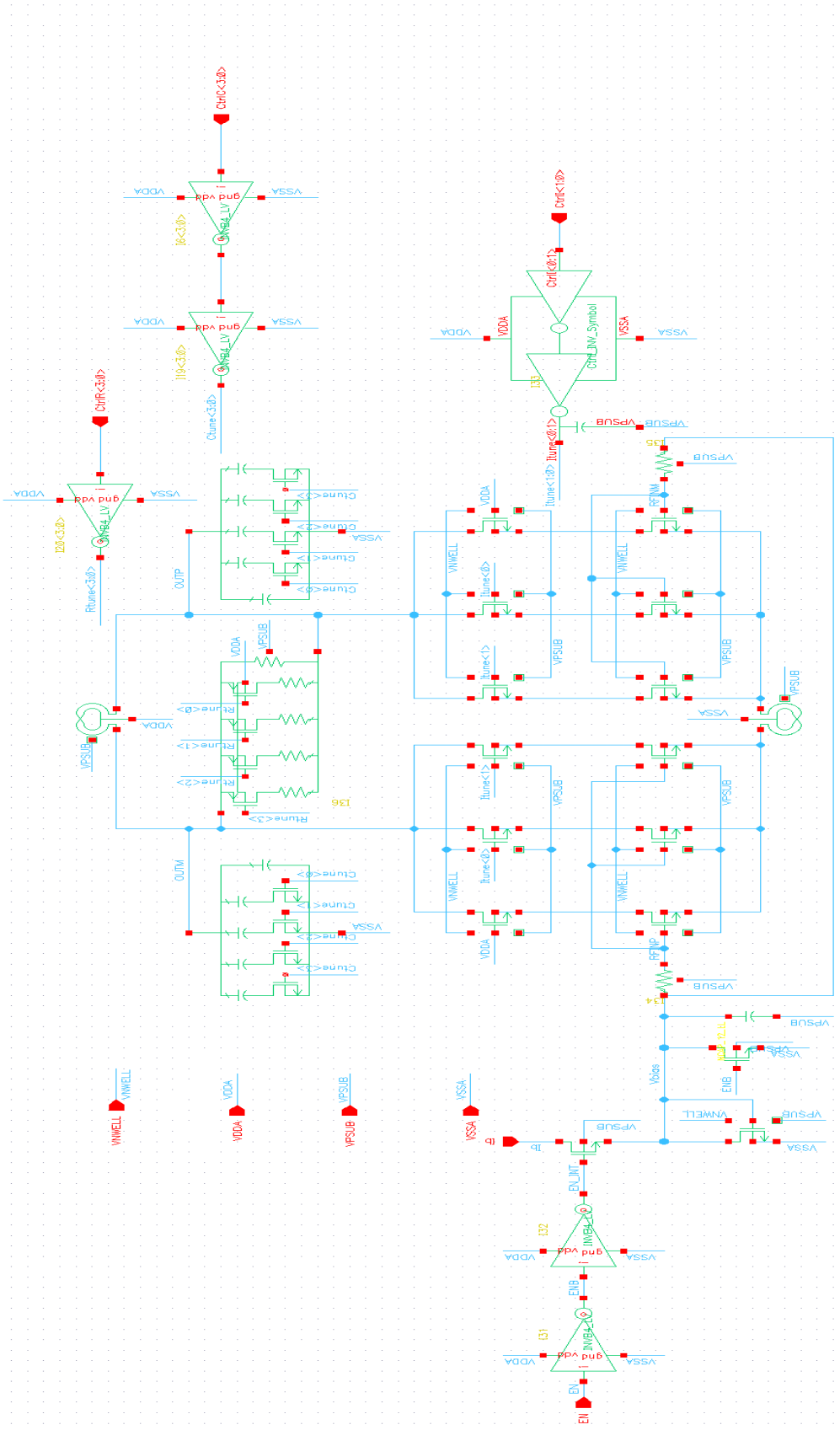

FIGURE 3.4: Full schematic of proposed CS-LNA.

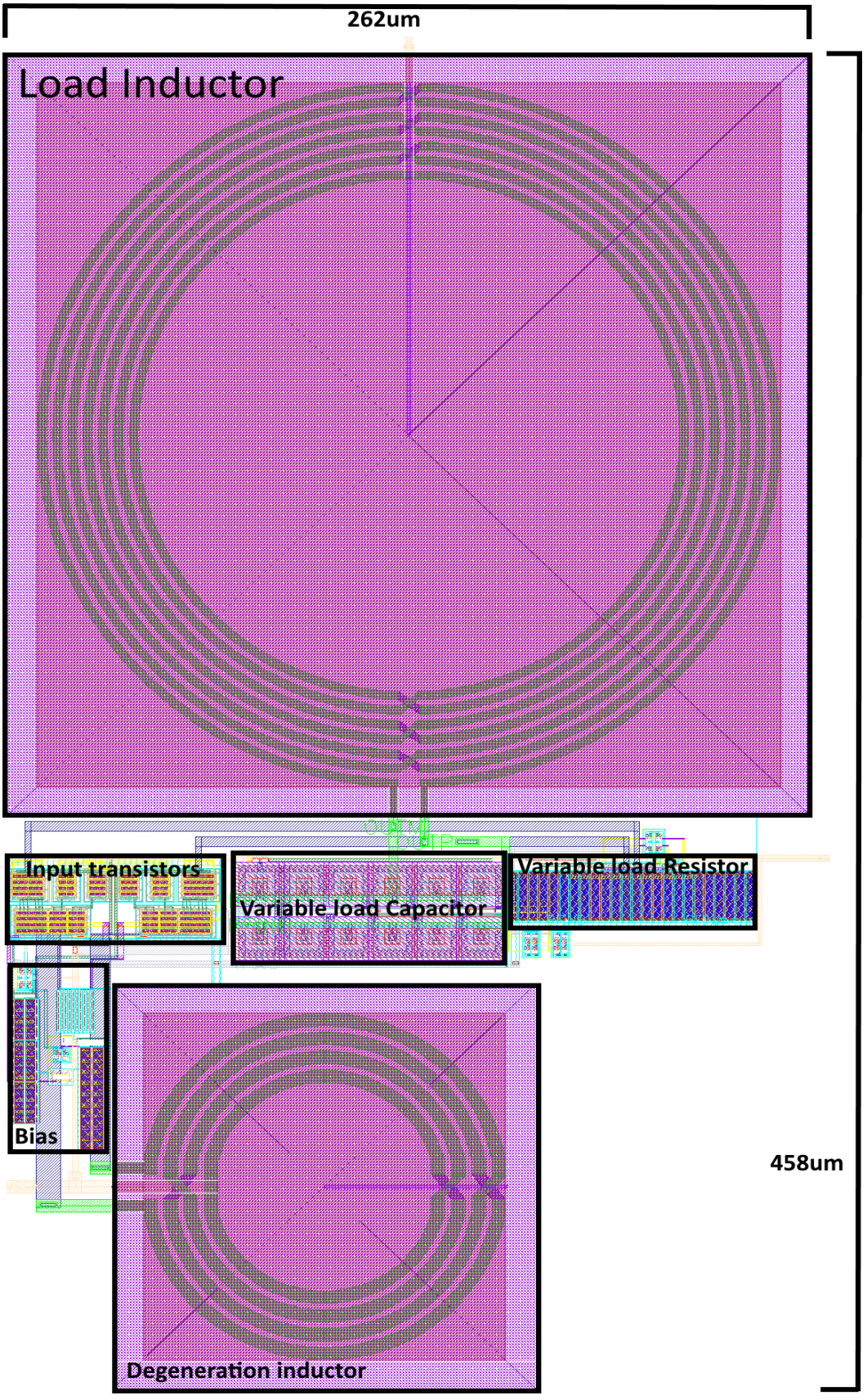

FIGURE 3.5: Layout of proposed CS-LNA.

Simulation Results

Simulations of the proposed design have been done using Cadence Virtuoso. As the load is programmable, we can control the gain and noise figure achieved by this LNA by changing the external control bits and hence, changing the output load. A simulation for gain and noise figure for all resistive load values is shown in figures 3.6 and 3.7, respectively. We can notice that the gain can change from $23.3dB$ to $27.8dB$ with a noise figure between $2.3 - 2.4dB$.

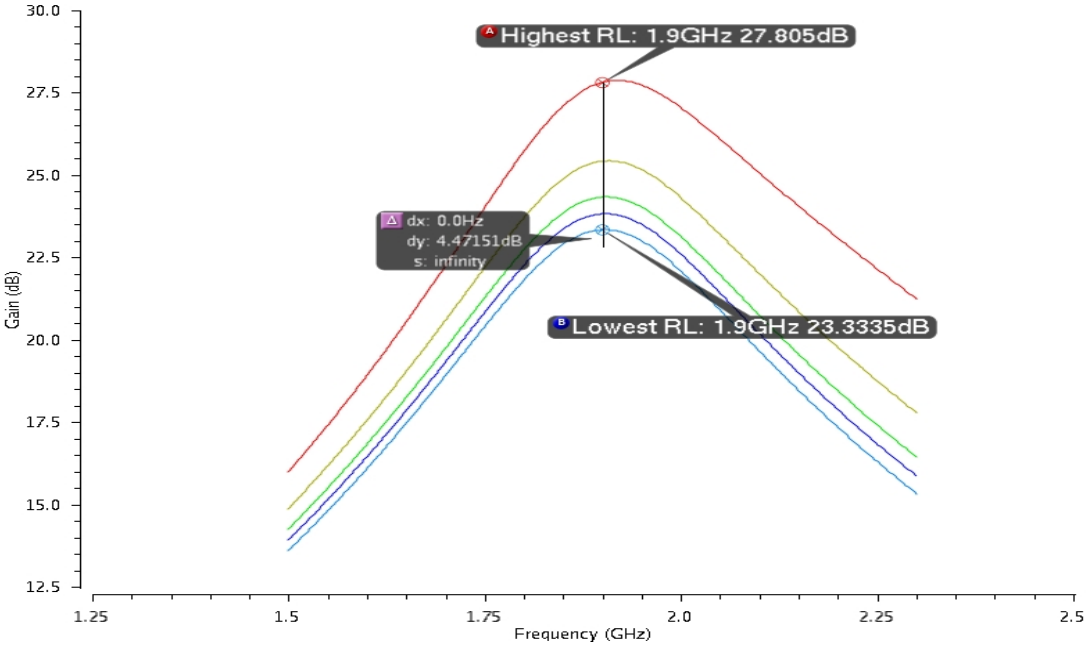

FIGURE 3.6: Gain simulation results for variable output load.

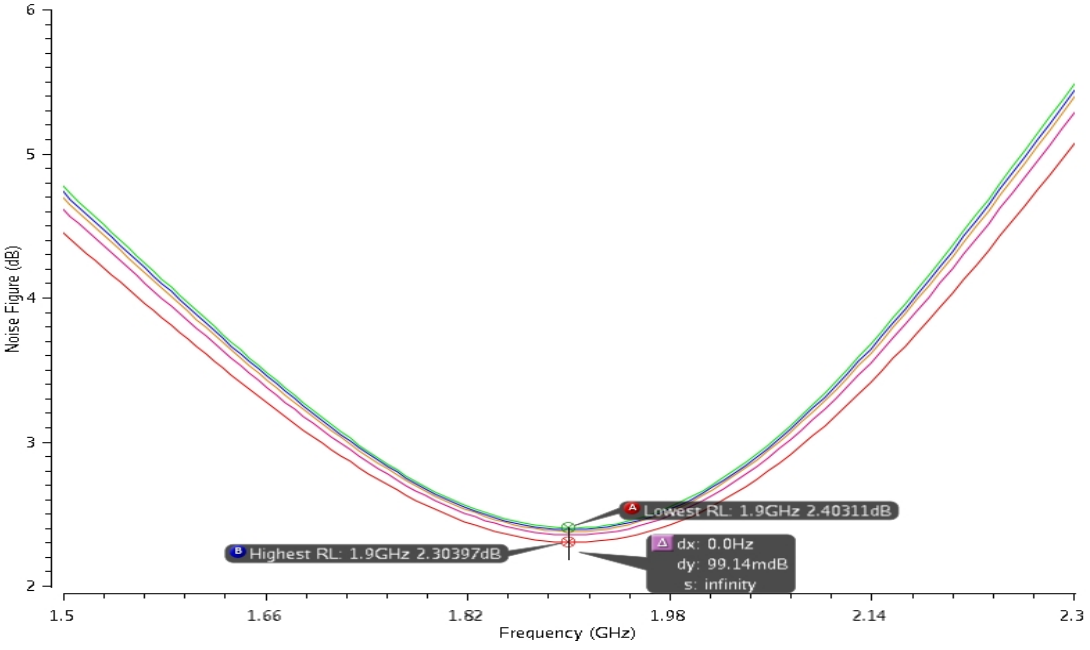

FIGURE 3.7: Noise simulation results for variable output load.

The external control bits of the input and cascode transistors can change the current consumption of the design by switching on and off some of the input transistors and changing the effective transconductance. Figures 3.8 and 3.9 show the simulation results of gain and noise figure with respect to current consumption.The power consumption can have the values $3.32mW$, $4.3mW$, and $5.26mW$.

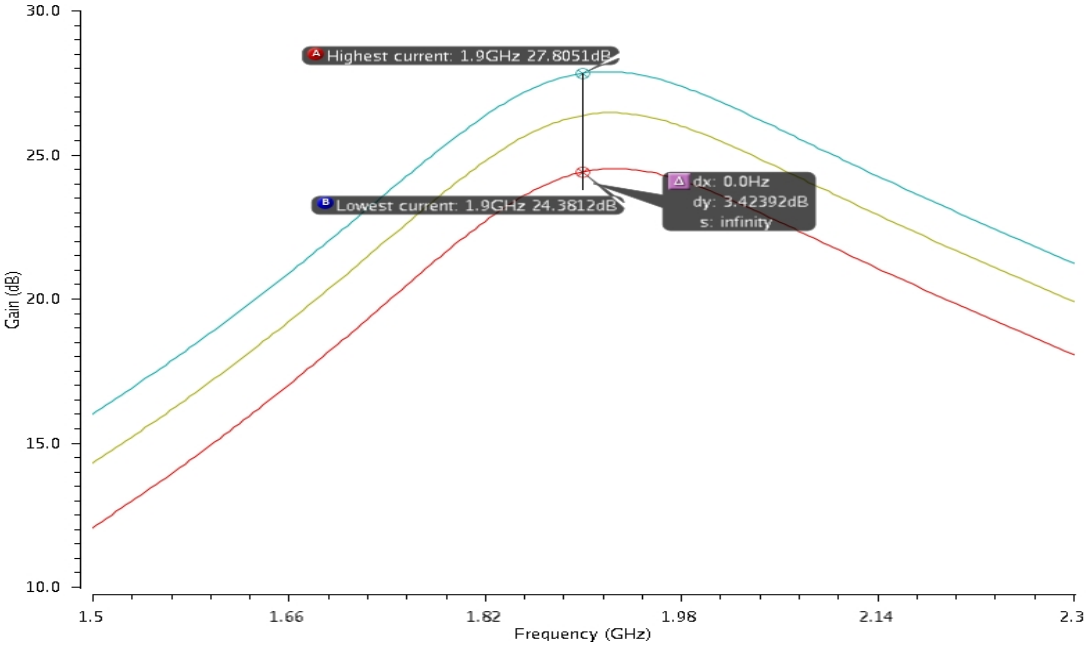

FIGURE 3.8: Gain simulation results for variable power consumption.

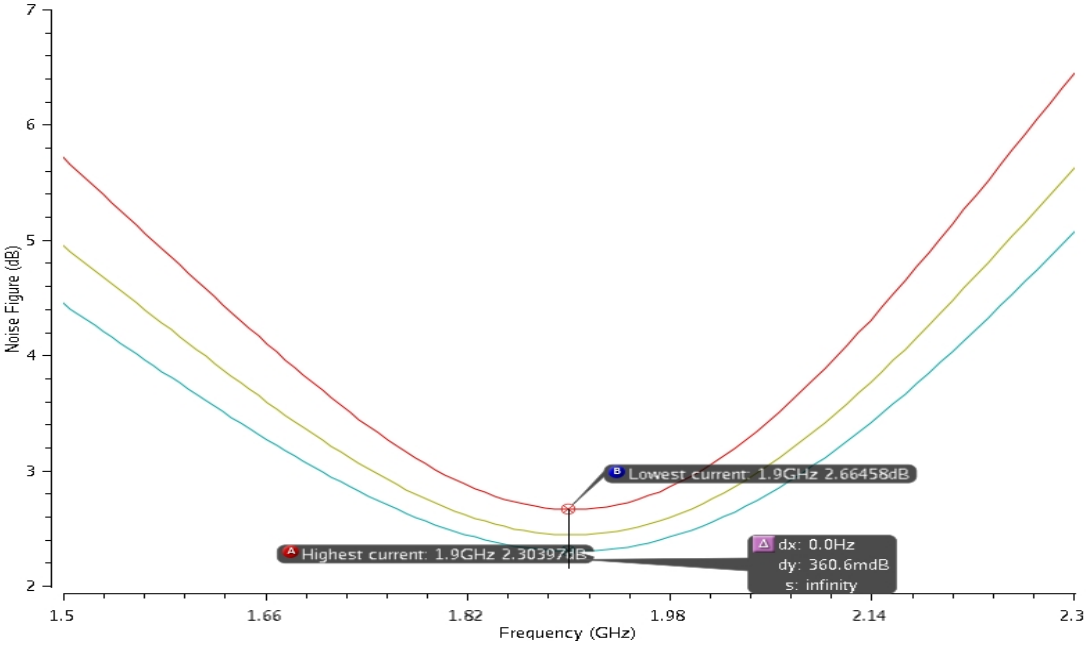

FIGURE 3.9: Noise simulation results for variable power consumption.

As shown form the results, the gain and noise figure are getting better when consuming more power. This tradeoff between noise figure, gain and power consumption is expected

from the analysis given in section 2.2.1. Figures 3.10 and 3.11 show the simulation results for gain and noise figure of the LNA before and after the extraction at its default control settings. The extracted results are slightly different than the schematic ones because of the parasitic resistances and capacitances produced by metal wiring during layout. Post-layout achieved gain is higher than the original gain by $0.5dB$ while the noise figure still the same. The slight increase in gain is expected to be due to the difference in RF models with multiple devices and converged RF transistors in actual layout.

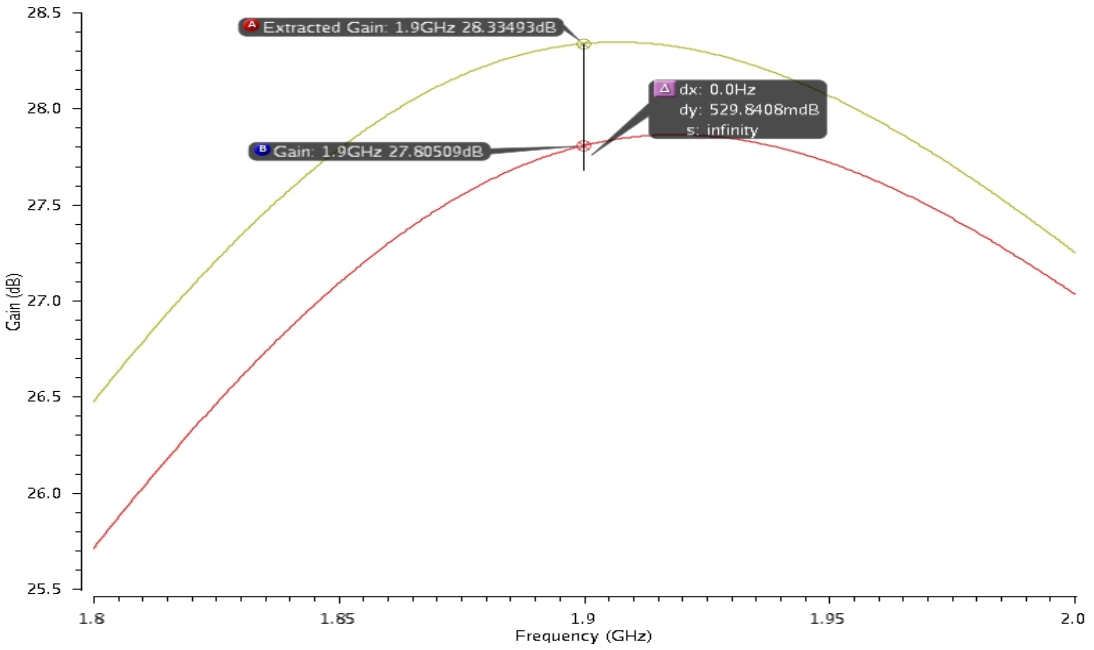

FIGURE 3.10: Gain simulation results for CSLNA.

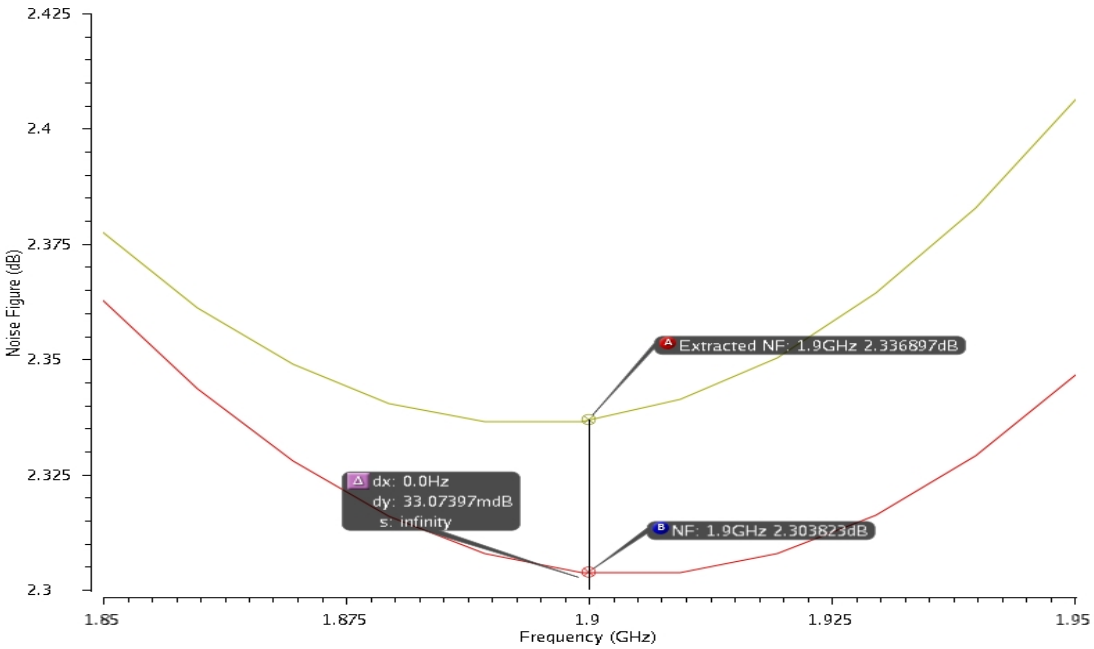

FIGURE 3.11: Noise simulation results for CSLNA.

S_{11} shows how good is the matching between the input impedance and the impedance of the antenna. Simulation results of S_{11} are presented in figure 3.12. The extracted capacitors and resistors changes the input impedance which in accordance lead to a change in S_{11} results . The use of external matching network gives the design more flexibility to change the values of capacitors and inductors in order to have best matching condition for all frequencies in personal communication service, PCS, band ($1900MHz$ – $1990MHz$).

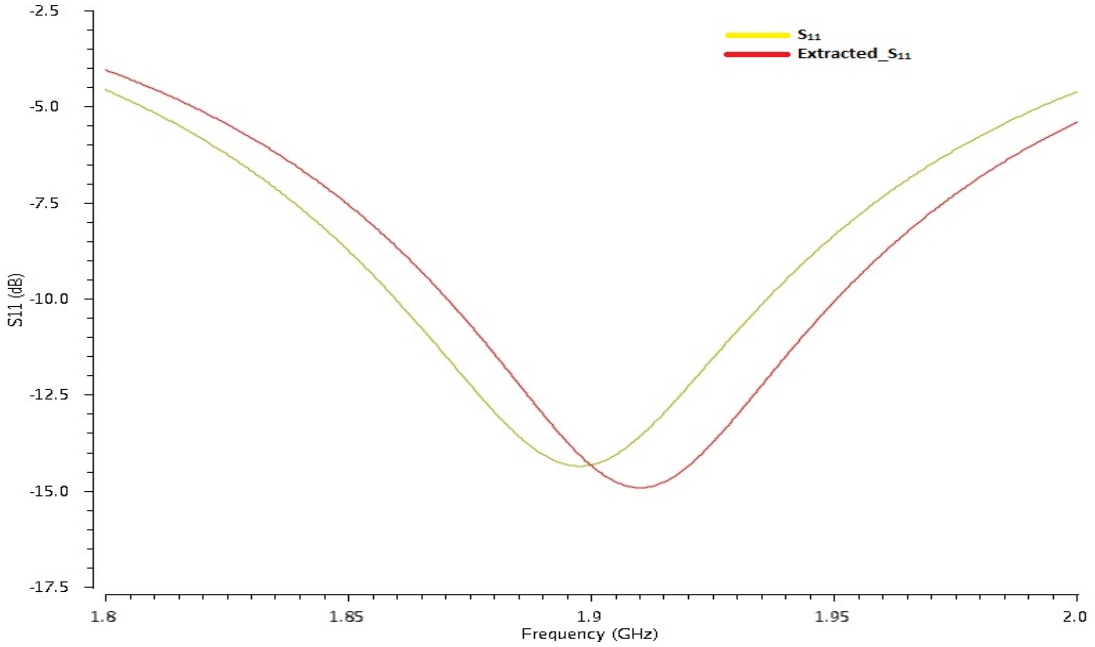

FIGURE 3.12: S_{11} simulation results for CSLNA.

The input-referred intercept point, $IIP3$, for the proposed common source design is simulated using a two-tone test for a $1.9GHz$ operating frequency. The two tones are applied with the same amplitude and a frequency offset of $10MHz$. An $IIP3$ value of $0.45dBm$ is obtained as shown in figure 3.13.

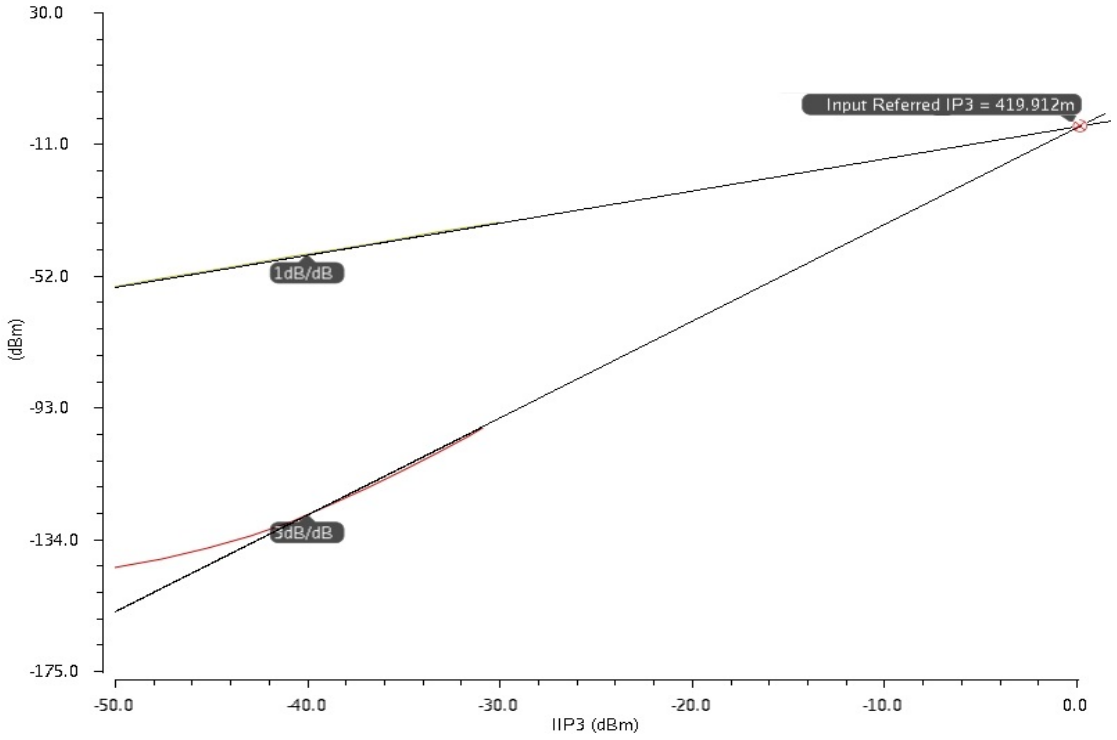

FIGURE 3.13: IIP3 simulation results for CSLNA.

3.2 Cascode Common Gate Capacitive Cross Coupled LNA Design

Common gate LNA is widely used for the applications that need wideband input matching. On the other side, the noise figure of this topology is higher than that of the CS topology and the gain is limited since the input transconductance is chosen to not exceed $g_m = \frac{1}{R_s} = 20mS$. The design proposed in this section uses a negative feedback technique to break the trade-off between the input impedance and the noise figure and gain. As shown in section 2.2.2, the minimum noise figure that can be achieved with conventional CG LNA neglecting the noise contribution of the load is given by

$$F \approx 1 + \frac{\gamma}{g_m R_s} \tag{3.5}$$

which gives a noise figure $\approx 3dB$ at perfect matching, $g_m R_s = 1$. From equation 3.5, the only way to decrease the NF of CG-LNA is to increase its g_m. However, the input matching will be deteriorated . Gm-boosted technique is used to increase the effective transconductance and as a result, reducing the noise figure [14]. The circuit in figure 3.14 shows a gm-boosting technique using a negative feedback amplifier between the source and gate of the input transistor. This circuit has an effective transconductance of $(1+A)g_m$, and its noise factor is reduced to

$$F = 1 + \frac{\gamma}{(1+A)^2 g_m R_s} \tag{3.6}$$

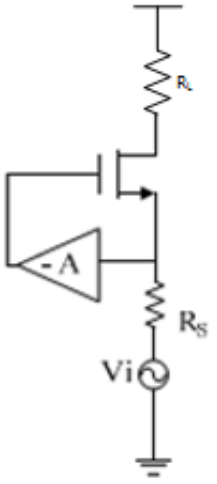

FIGURE 3.14: Simplified G_m-boosted CGLNA.

And to match the input, $R_s = \frac{1}{(1+A)g_m}$) then the noise factor will be

$$F = 1 + \frac{\gamma}{(1+A)} \tag{3.7}$$

which means that the thermal noise contribution of the input transistor is decreased by the factor $(1 + A)$. The inverting amplifier stage can be implemented using active stage but this will contribute to the noise figure of the circuit. Because of this, passive methods for gm-boosting is more attractive [8].

The use of capacitive cross-coupling technique, CCCT, can be seen as a gate voltage booster. It limits the boosting gain to $A = 1$ without increasing the DC power which make it a good choice for low power applications [7]. Figure 3.15 shows the use of CCCT in a fully differential CG-LNA.

$$A = \frac{C_1}{C_1 + C_{gs}} \tag{3.8}$$

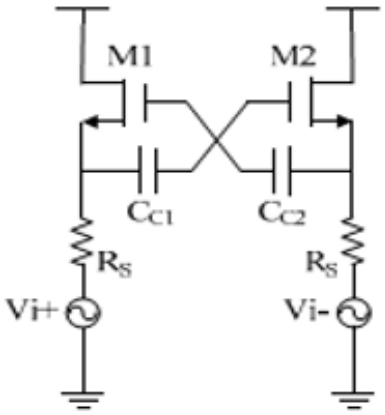

FIGURE 3.15: G_m-boosted CGLNA [14].

And since $C_1 \gg C_{gs}$, then $A \approx 1$ and the noise factor and gain are given by

$$F = 1 + \frac{\gamma}{2} \tag{3.9}$$

$$A = G_{m,eff} R_L = 2 g_m R_L \tag{3.10}$$

Equation 3.10 shows that while consuming the same amount of current, the CCC CG-LNA provides double gain when compared to the conventional CG-LNA. Hence, the CCC CG-LNA can achieve the same gain with a lower noise figure while reducing the power consumption. From the small signal model shown in figure 3.16, the input impedance can be found by the following equations:

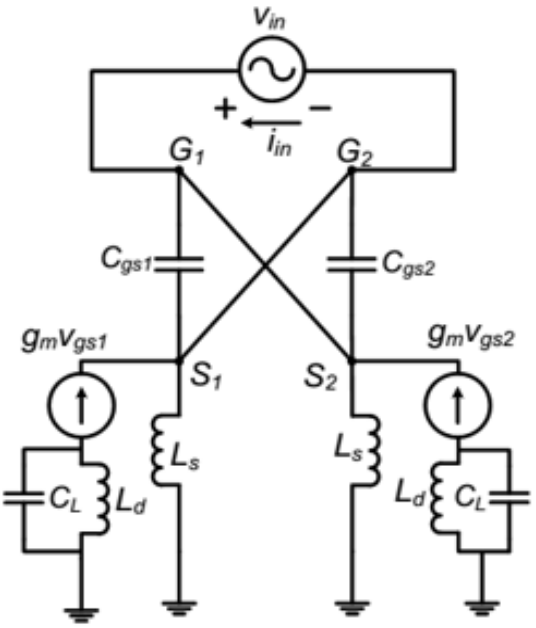

FIGURE 3.16: Small signal analysis of CCC CG-LNA [15].

$$R_{in,diff} = \frac{v_{in}}{i_{in}} \tag{3.11}$$

where i_{in} is given by:

$$i_{in} = v_{in}\left(sC_{gs1} + sC_{gs2} + \frac{1}{2sL_s} + g_{mi}\right) \tag{3.12}$$

The two CCC capacitors are considered as short circuit in our analysis. Since both the differential amplifiers have the same parameters and they are biased and sized with same values, then $C_{gs1} = C_{gs2} = C_{gs}$ and by substituting in equations 3.11 and 3.12:

$$R_{in,diff} = \frac{1}{2sC_{gs} + \frac{1}{2sL_s} + g_{mi}} \tag{3.13}$$

$$R_{in} = \frac{R_{in,diff}}{2} = \frac{1}{4sC_{gs} + \frac{1}{sL_s} + 2g_{mi}} \tag{3.14}$$

The resonance frequency is given by

$$w_o = \frac{1}{\sqrt{4C_{gs}L_s}} \tag{3.15}$$

And at that frequency the input impedance of this topology is

$$R_{in} = \frac{1}{2g_{mi}} \tag{3.16}$$

Circuit Implementation

A simplified schematic of the proposed fully differential CCC-CGLNA is shown in Figure 3.17. This design is a fully integrated design without need to an off-chip matching network. Differential transistors M1 and M2 are biased and sized for $g_m = 21.6mS$ to have a high gain and low noise figure with an acceptable S_{11}.

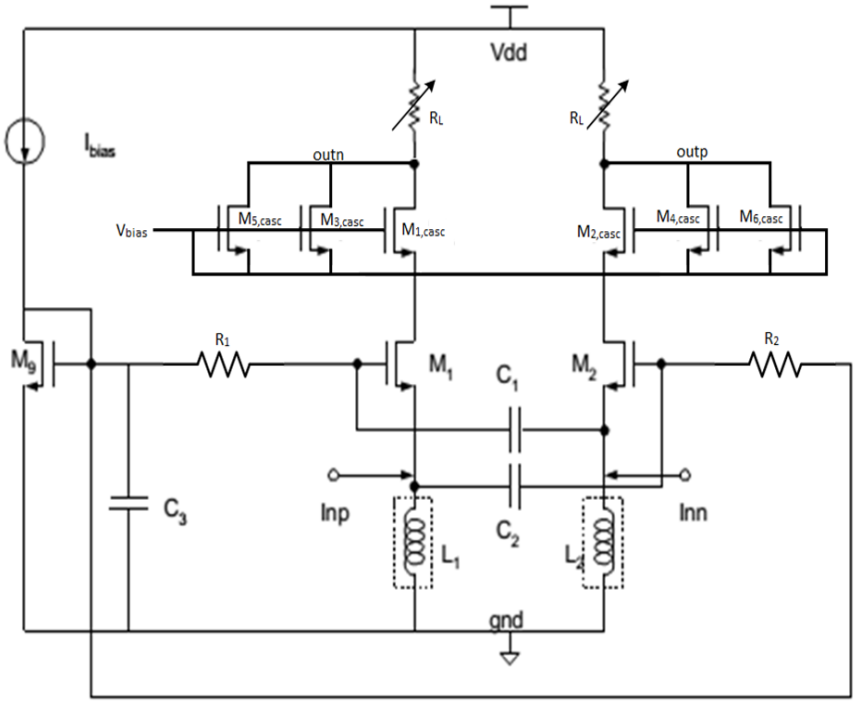

FIGURE 3.17: Simplified schematic of CG-LNA with CCC

Two cascode transistors are used in the design to improve the reverse isolation from the output to the input, S_{12}, and make the circuit more stable. R_1 and R_2 are two large resistors used to isolate the high frequency signal path from the biasing circuitry. The two cross-coupling capacitors, C_c, have a value of $2pF$. An on-chip inductor, L_1, is used to resonate with the gate-source capacitor, C_{gs}, and the input parasitic capacitance at the frequency of interest.

A programmable resistive passive load is used in the LNA design in order to make gain programmable for linearity optimization of the receiver. However, change in the output load leads to a change in noise figure as well. The cascode transistors of this design is programmable and can be controlled by digital control bits to improve the gain and noise figure with the cost of degradation in input matching. Figure 3.18 shows the full schematic of the proposed design.

The design is implemented in UMC $65nm$ CMOS technology and operates at a frequency of $2.4GHz$. The power consumption is less than $5mW$ from a $1.4V$ supply occupying an

area of $0.0784mm^2$. The LNA achieves a gain of $21dB$ after extraction of the parasitic with a noise figure less than $2.2dB$. The design parameters are summarized in table 3.2.

TABLE 3.2: Design parameters of CG-LNA.

Parameters	Value	Multiplier
M_1, M_2	$\frac{7.2}{0.06}\mu m$	12
$M_{1-6,casc}$	$\frac{7.2}{0.06}\mu m$	4
R_L	$463 - 810\Omega$	–
L_1	$5nH$	–
C_C	$2pF$	–
R_1, R_2	$6K\Omega$	–

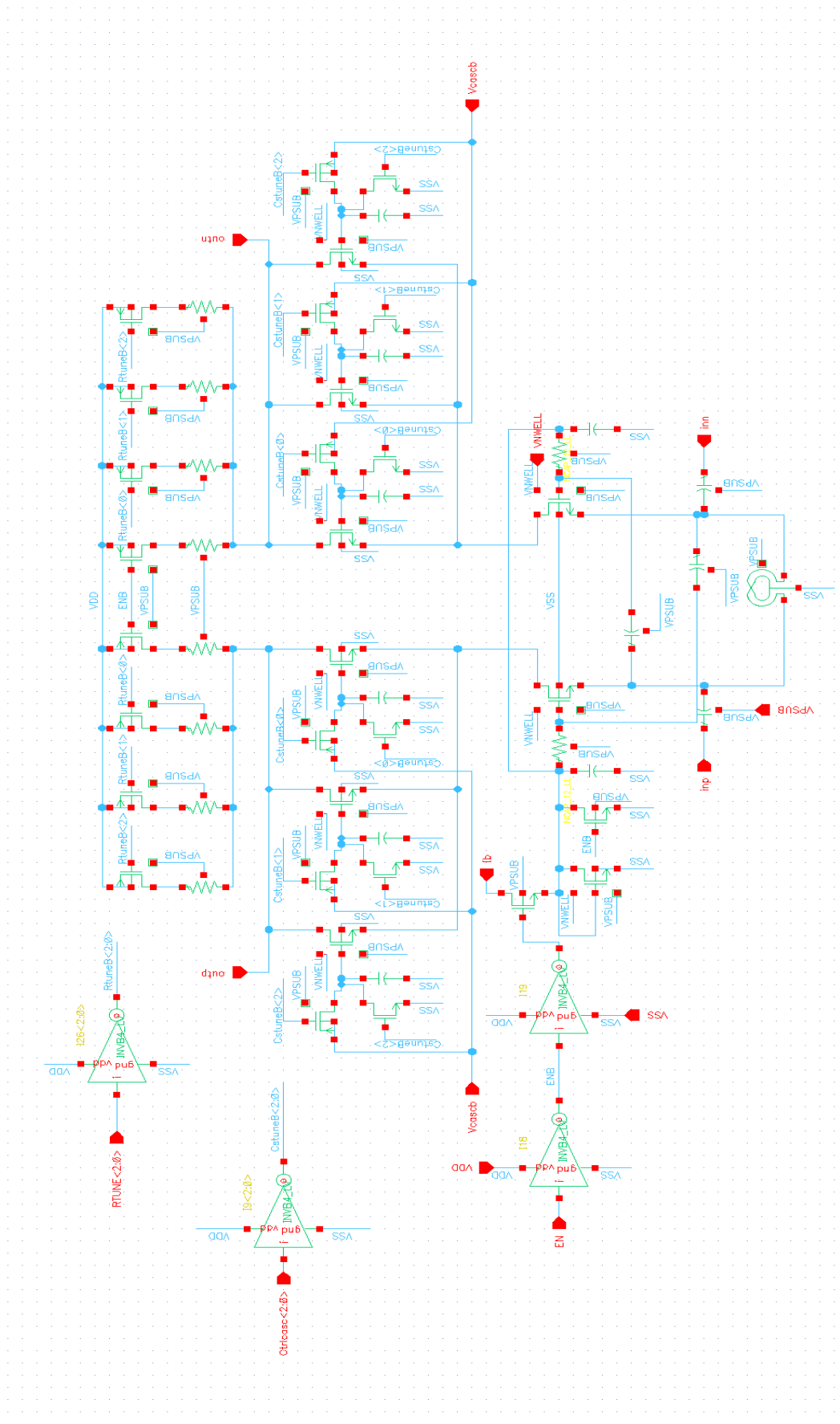

FIGURE 3.18: Full schematic of proposed Cg-LNA.

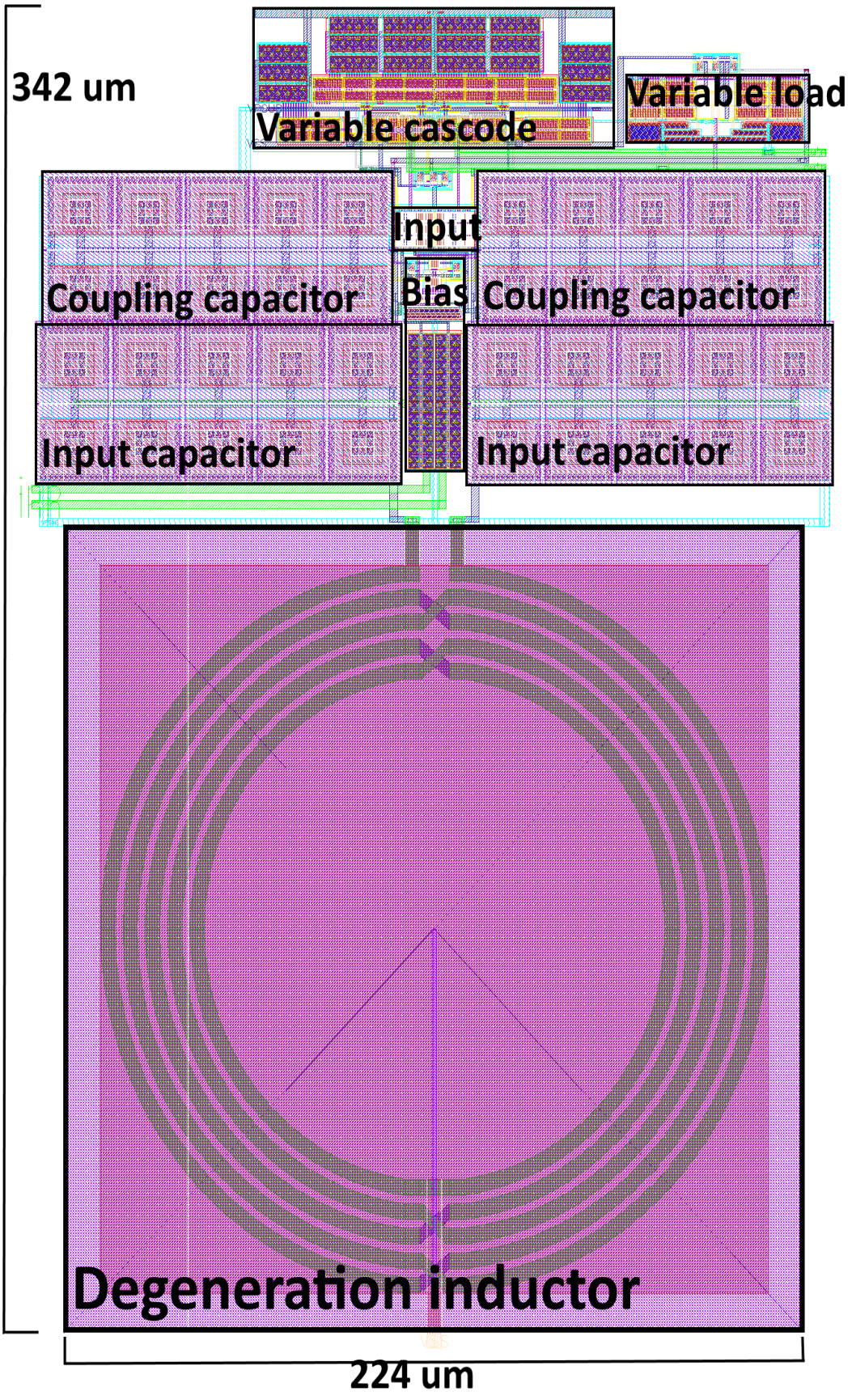

FIGURE 3.19: Layout of proposed CG-LNA.

Simulation Results

Cadence virtuoso tools are used to design and simulate this LNA.The simulation results in figure 3.20 shows the variation of gain while changing the output load. These results have been simulated at largest cascode size setting. The gain has a range from 17.57 dB to 22.66 dB highest load with the load variation.

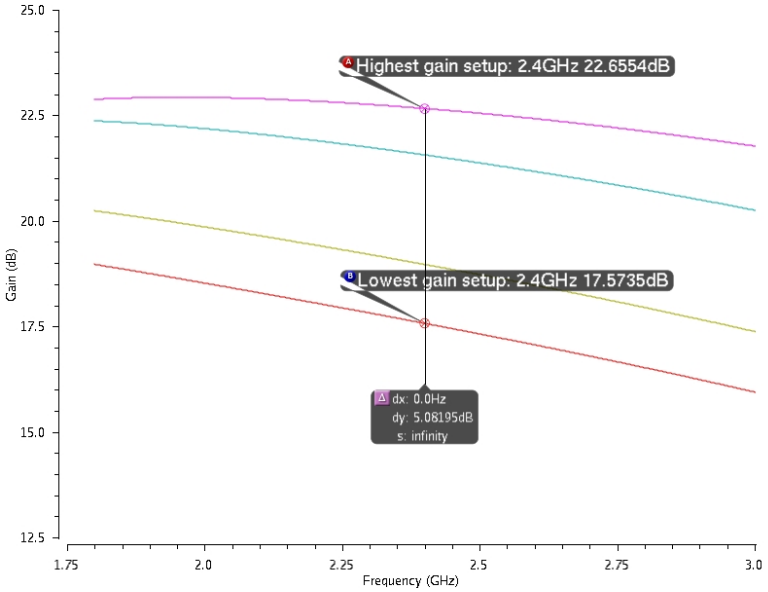

FIGURE 3.20: Gain simulation results for variable resistive load.

Noise figure simulations with the same conditions of largest cascode size are shown in figure 3.21. The results show a variation range between 2.22 –2.26dB.

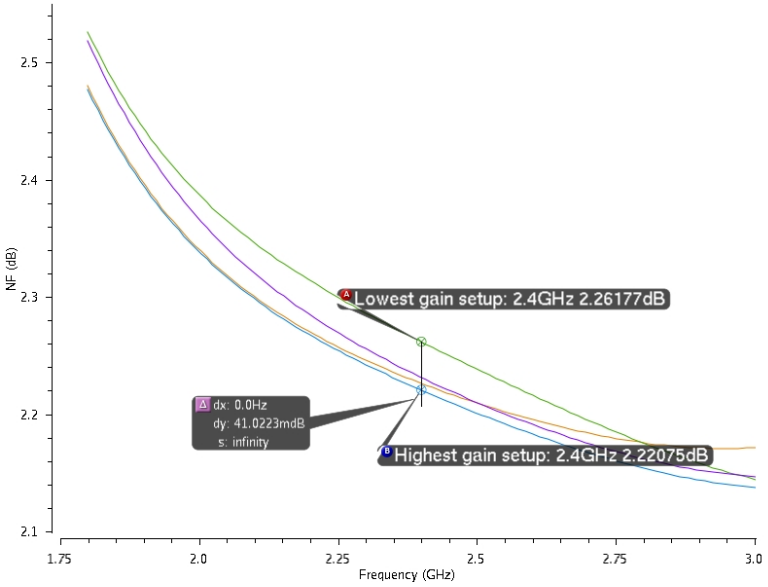

FIGURE 3.21: Noise simulation results for variable resistive load.

From this simulation results for gain and noise figure an optimum output load is chosen and a parametric analysis is run with respect to the size of cascode devices. Increasing

the size of cascode transistors lead to an improvement in gain and noise figure with the cost of degradation in input matching. Figures 3.22, 3.23, and 3.24 show the variation in results.

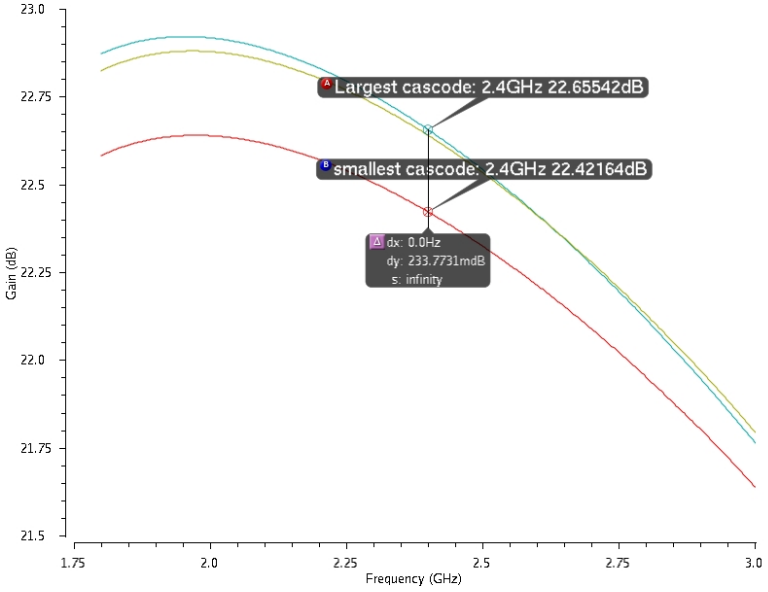

FIGURE 3.22: Gain simulation results for variable cascode size.

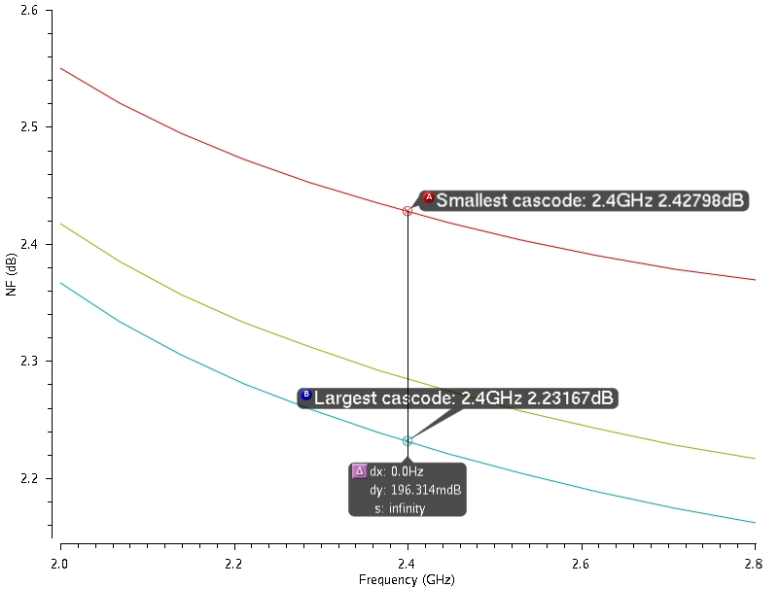

FIGURE 3.23: Noise simulation results for variable cascode size.

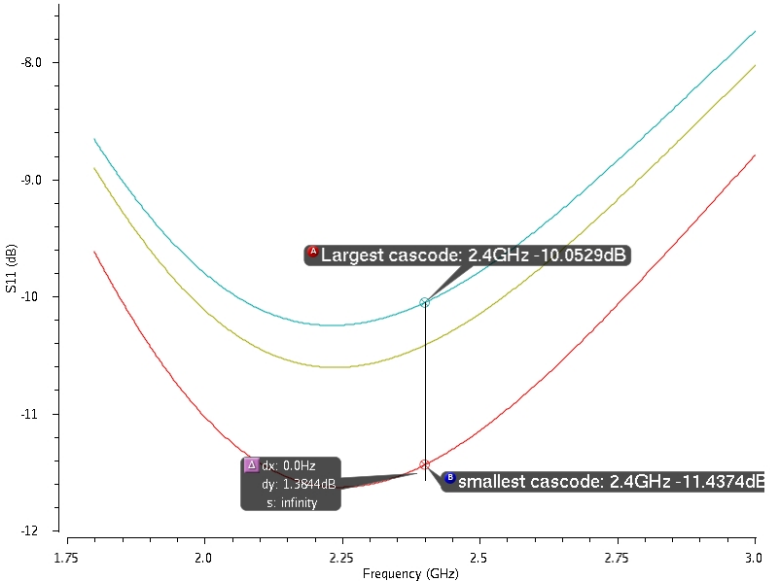

FIGURE 3.24: S_{11} simulation results for variable cascode size.

The simulation results for the voltage gain, noise figure, and S_{11} are given in figures 3.25, 3.26, and 3.27. There is a decrease of $1.6dB$ in gain after the extraction of the parasitic because of the resistance and capacitance introduced from the layout due to the used metal layers. S_{11} has been decreased by almost $1-dB$ to become $-11dB$ which is acceptable in our system. Noise figure is increased by approximately $0.5dB$ after extraction. This increase comes from the parasitic resistances from the metalization and the reduction in gain as well.

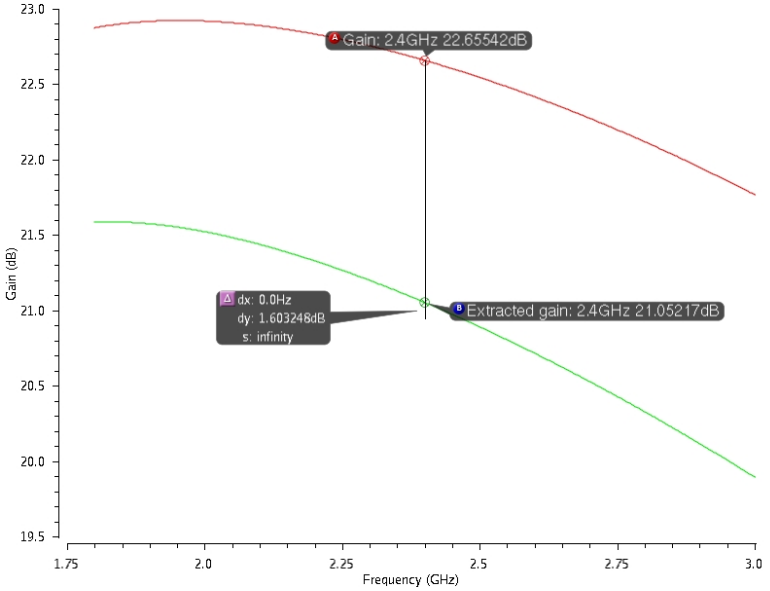

FIGURE 3.25: Gain simulation results for proposed CG-LNA.

The input-referred intercept point, $IIP3$, for the proposed CCC common gate design is simulated using a two-tone test for a $2.4GHz$ operating frequency. The two tones are

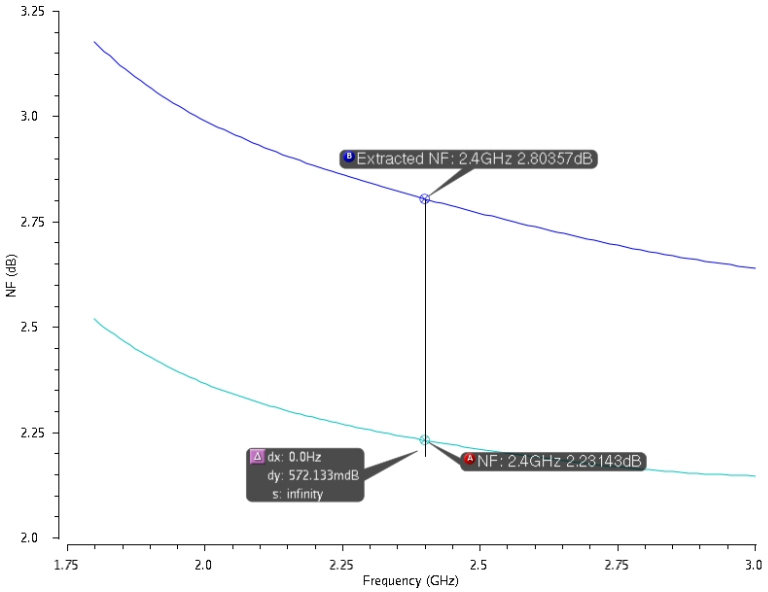

FIGURE 3.26: Noise simulation results for proposed CG-LNA.

applied with the same amplitude and a frequency offset of $10MHz$. An $IIP3$ value of $-3.98dBm$ is obtained as shown in figure 3.28.

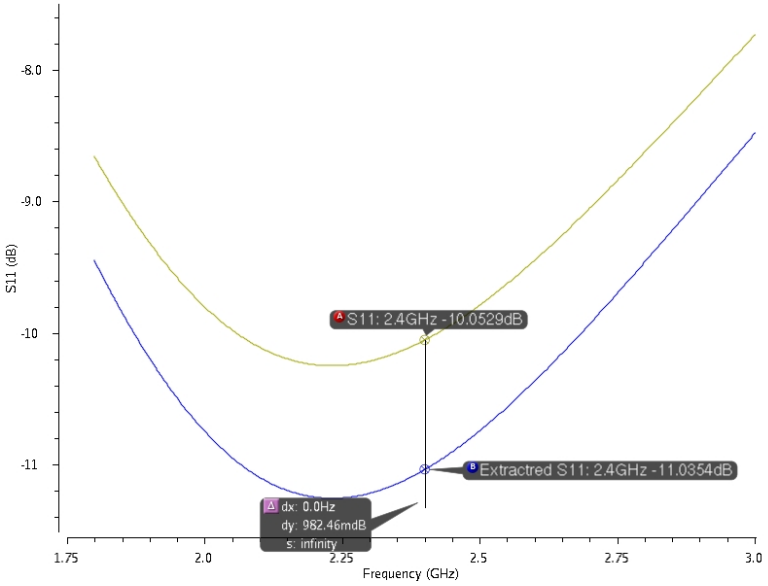

FIGURE 3.27: S_{11} simulation results for proposed CG-LNA.

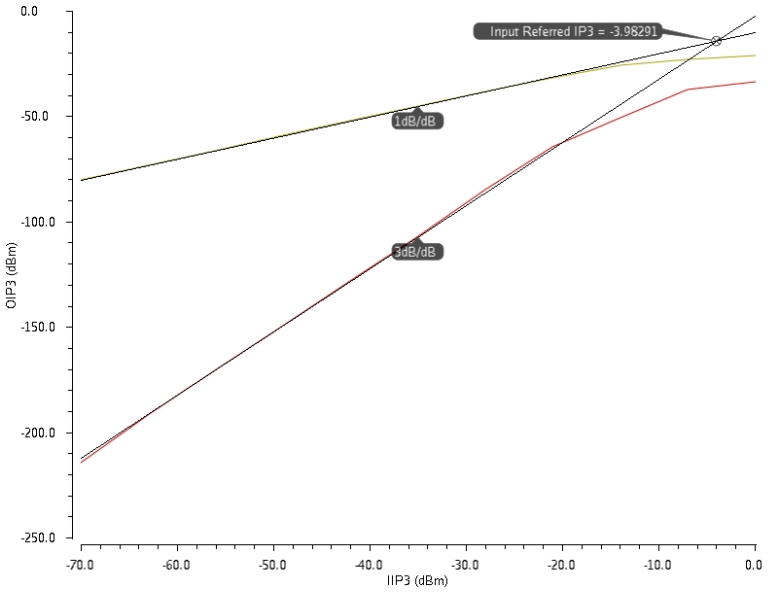

FIGURE 3.28: IIP3 simulation results for CGLNA.

Table 3.3 summarizes the results of the two designs presented in this report and compares them with the discussed designs in chapter 2. Both designs are implemented in UMC 65nm CMOS technology.

TABLE 3.3: Performance comparison between different LNA designs.

Ref		Freq. Band [GHz]	NF [dB]	Gain A_v [dB]	IIP3 [dBm]	Power Consumption [mW]	Process	Area [mm^2]
[4]		2.4	2.8	14.5	-7.8	19.8	0.18μm	0.15
[5]		2.2	1.92	8.6	-2.55	16.2	TSMC 0.35μm	1.3
[7]		0.1-2.7	4	20	-12	1.32	0.13μm	0.007
[8]		6	3	7.1	11.4	6.48	180nm	0.95
[9]	High Linearity	0.5-6.2	2.1-3.1	24.4	22	42	90nm	0.016
	Low Noise	0.5-7.25	1.8-2.5	25.2	13			
[10]		0.1-1.77	1.85	23	-2.85	2.8	90nm	0.03
[12]		0.2-5.2	<3.5	13-15.6	>0	21	65nm	0.009
[13]		0.2-3.8	2.8-3.4	19	-4.2	5.7	130nm	0.025
This work	CS-LNA	1.9	2.3-2.66	24.3-27.8	0.42	3.32-5.26	65nm	0.1
	CG-LNA	2.4	2.23-2.4	17.6-22.6	-4	4.13-5.1	65nm	0.074

Chapter 4

Conclusion and Future Work

The design presented in this thesis achieve a good performance compared to the previously designed LNA. The CS-LNA achieves a very high gain with low noise figure and acceptable matching. It is still a narrow band LNA because of the frequency dependent components used in the matching network and the degeneration inductor. The design has a good linearity and low power consumption.

The other design, CG-LNA, has a very promising performance. It achieves a good gain and lower noise figure than the CS one due to the utilization of the capacitive-cross coupling. It covers larger band compared to other CS ($\sim 100MHz$) and achieves a good linearity.

The next step in this work is to optimize the CS-LNA to be used in a wideband by using multiple LNAs with shared degeneration inductors to reduce the area and at the same time work for multistandards. The CG-LNA can be optimized further and it can be implemented with single input differential output which will reduce the number of pads and and avoid using balun transformer.

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