DC-DC Regulators For Ultra Low Power Applications

A thesis submitted to the
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by

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in

Electronics and Computer Engineering

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Electronics and Computer Engineering.

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"There is no better than adversity. Every defeat, every heartbreak, every loss, contains its own seed, its own lesson on how to improve your performance the next time."

Malcolm X

DC-DC Regulators For Ultra Low Power Applications

Sherif ELHOSAINY

Abstract

This dissertation introduces a new linear regulator that can be used in a parallel hybrid linear switching regulator system. The purpose of the novel system is to make use of the high power efficiency of the switching regulator and the good transient response of the linear regulator. The designed linear regulator achieves 32 different output voltages ranging from $380mV$ to $1V$ with a step of $20mV$ with the control of a programmable digitally controlled resistor DAC. The circuit consumes only $7\mu A$ of quiescent current and can supply up to $10mA$ current with a maximum output load capacitance of $10nF$. The linear regulator typically operates in inactive mode and gets activated automatically only in transient conditions enhancing the transient performance of the switched regulator with negligible degradation in efficiency. A new feedforward technique is used to improve the transient response of the linear regulator operating with such low power consumption. The linear regulator can limit the overshoot resulting from a sudden load current change from no load to full load, to $100mV$. The circuit design and layout are done on UMC $65nm$ CMOS.

Keywords: Linear regulators; Ultra low power; Switching regulator; LDO; Parallel hybrid linear switching regulator

Ultra Düşük Güçlü Uygulamalar İçin Voltaj Regülatorleri

Sherif ELHOSAINY

Öz

Bu tezde paralel-melez doğrusal-anahtarlama regülasyon sistemlerinde kullanılmak üzere yeni bir doğrusal regülatör tanıtılmıştır. Bu özgün sistem anahtarlama regülatörünün yüksek güç veriminden ve doğrusal regülatörün hızlı tepkisinden faydalanmaktadır. Tasarlanan regülatör $380mV$'dan $1V$'a kadar $20mV$ adımlarla değişen tam 32 farklı çıkış voltajını üretebilmektedir. Bu 32 referans voltajı dijital olarak kontrol edilebilen programlanabilir bir direnç DAC'i ile elde edilmektedir. Devre sadece $7\mu A$ akım ile çalışmakta ve $10nF$ 'maksimum çıkış yük kapasitansı için $10mA$ kadar akım sağlayabilmektedir. Doğrusal regülatör genel olarak pasiftir ve yük akımı atlamalarında otomayik olarak çalışarak anahtarlama regülatörünün performansını geliştirmektedir. Bunların yanı sıra, böyle düşük güç tüketimi ile çalışan doğrusal regülatörlerin tepkisini hızlandırmak için yeni bir teknik kullanılmıştır. Devrenin tasarımı ve modellemesi UMC 65nm CMOS ile yapılmıştır.

Anahtar Sözcükler: Doğrusal regülatör; Ultra düşük güç; Anahtarlama regülatörü; LDO; Paralel melez doğrusal anahtarlama regülatörü

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Abbreviations

AC	**A**lternating **C**urrent
BW	**B**and **W**idth
DC	**D**irect **C**urrent
EMI	**E**lectro **M**agnetic **I**nterference
ESR	**E**lectric **S**eries **R**esistance
HDO	**H**igh **D**rop **O**ut voltage
IC	**I**ntegrated **C**ircuits
I-V	Current Voltage
LDO	**L**ow **D**rop **O**ut voltage
LHP	**L**eft **H**and **P**ole
MOM	**M**etal **O**xide **M**etal
MOSFET	**M**etal **O**xide **S**emiconudor **F**ield **E**ffect **T**ransistor
NMOS	**N** type **M**etal **O**xide **S**emiconudor
PM	**P**hase **M**argin
PMOS	**P** type **M**etal **O**xide **S**emiconudor
PSRR	**P**ower **S**upply **R**ejection **R**ation
RF	**R**adio **F**requency
RHP	**R**igh **H**and **P**ole
SC	**S**witching **C**apacitor
SOC	**D**irect **C**urrent
SR	**S**lew **R**ate
UGB	**U**nity **G**ain **B**andwidth
VDD	Supply Voltage
Vgs	**G**ate **S**ource **V**oltage
Vod	**O**ver **D**rive **V**oltage

Chapter 1

Introduction

1.1 The importance of power management

In the past few decades, the integrated circuit industry has been developing too quickly with new and vast challenges to suit different applications, starting with simple control circuits and sensors attached to machines, passing through the design of transceivers and ending with highly complex circuits and processors[1]. Each of these applications, being portable or not, always has at least one DC power supply such as a battery supplying the whole application. Batteries provide a decaying voltage level with time as shown in Figure 1.1. Also, the voltage level changes with many factors such as load current, temperature, etc. [2] These voltage sources can be modeled as an ideal supply and a series resistance as shown in Figure 1.2. When connecting this supply with a load, the real voltage applied to the load is given by:

$$V_{real} = V_{Battery} * \frac{R_{load}}{R_{load} + R_{series}}$$

which is why the voltage level changes with the load.

Different electronic circuits demand different and stable DC supply levels so that they can perform the optimum required performance. These circuits might be integrated into one system and share one battery. Power management blocks are responsible for transferring a voltage level to different stable and constant voltage levels with a variety of design specs defined by the applications they are serving. One of the most important of these specs is the efficiency of the power management block, which plays the major

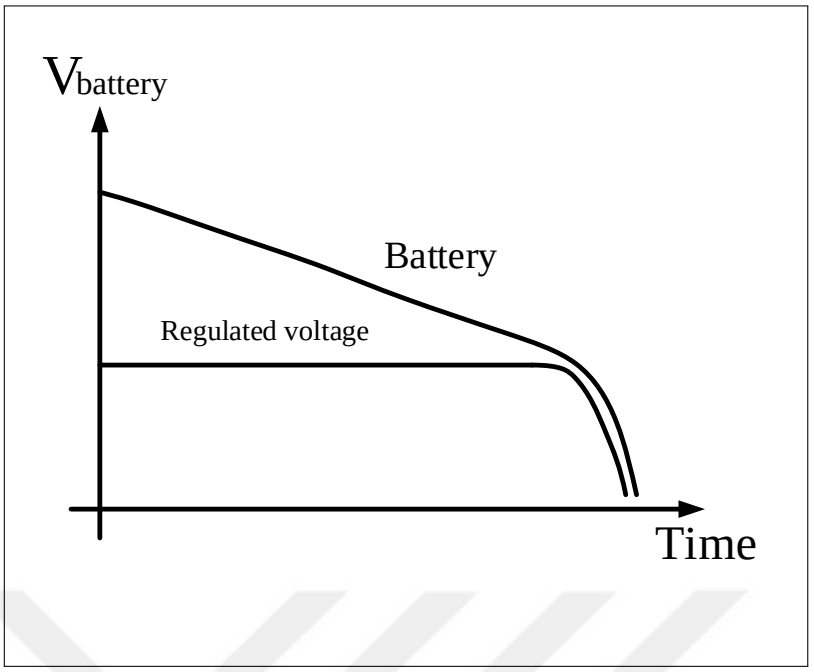

FIGURE 1.1: Battery and required regulated voltage vs time

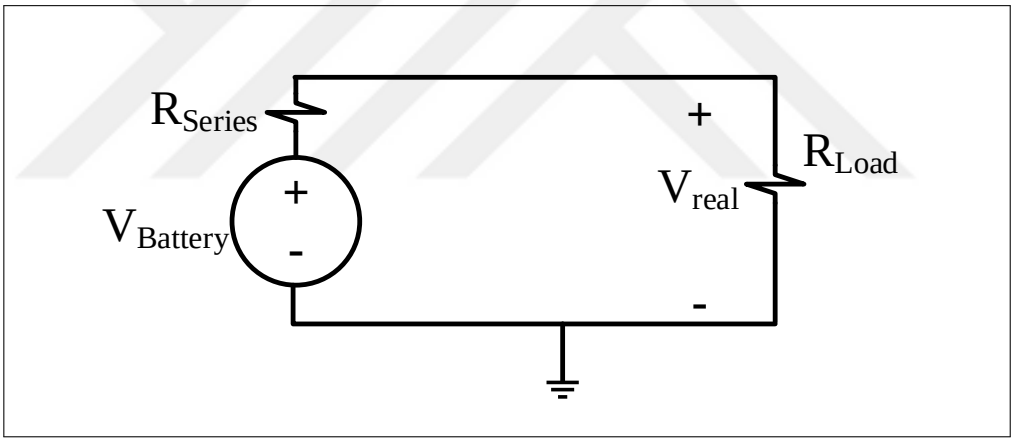

FIGURE 1.2: Battery modeling

role in the battery lifetime of portable devices that are growing vastly. Similarly, for ultra-low power applications, increasing the regulator's efficiency is the primary market demand. Other specs such as PSRR and noise are critical to analog and RF circuits due to the fact that these circuits are noise sensitive [3]. Because of all the mentioned reasons, design of power management blocks is critical for the systems they are used in, and researchers are investing a tremendous amount of time and effort to achieve better results.

1.2 Organization of Thesis

Chapter 2 explains the main theory of operation of different types of DC-DC regulators. In Chapter 3, linear regulators will be discussed in detail. Chapter 4 discusses the new idea of the parallel hybrid regulators and the proposed circuit design. The conclusion will be discussed in Chapter 5.

Chapter 2

Types of Regulators

DC-DC regulators can be categorized into two main categories, the first being the switching regulators, and the second being the linear regulators[1].

2.1 Switching Regulators

Switching regulators consist of energy transfer components such as inductors or capacitors, and transistors which are used as ON/OFF switches. Since the transistors remain in triode or cut off, switching regulators can provide very high efficiency which can reach 100% theoretically. On the other hand, switching regulators are complex to design, and they are area inefficient due to the energy transfer component used. Switching regulators can be divided into subcategories according to the energy component types, namely switched capacitor converters and magnetic (inductor) switching mode converters.

2.1.1 Inductor-Based Switching Regulators

Off-chip inductor based converters as shown in Figure 2.1 are often used for applications such as power amplifiers that require high efficiency [4]. Inductor based converters can generate different output DC levels by changing the duty cycle of the feedback signal using pulse width controller. The inductor is used for averaging the pulses generated by the switching operation of the regulators. Although this type of converters can operate at a very high efficiency, they have several drawbacks. The main drawback is the bulky,

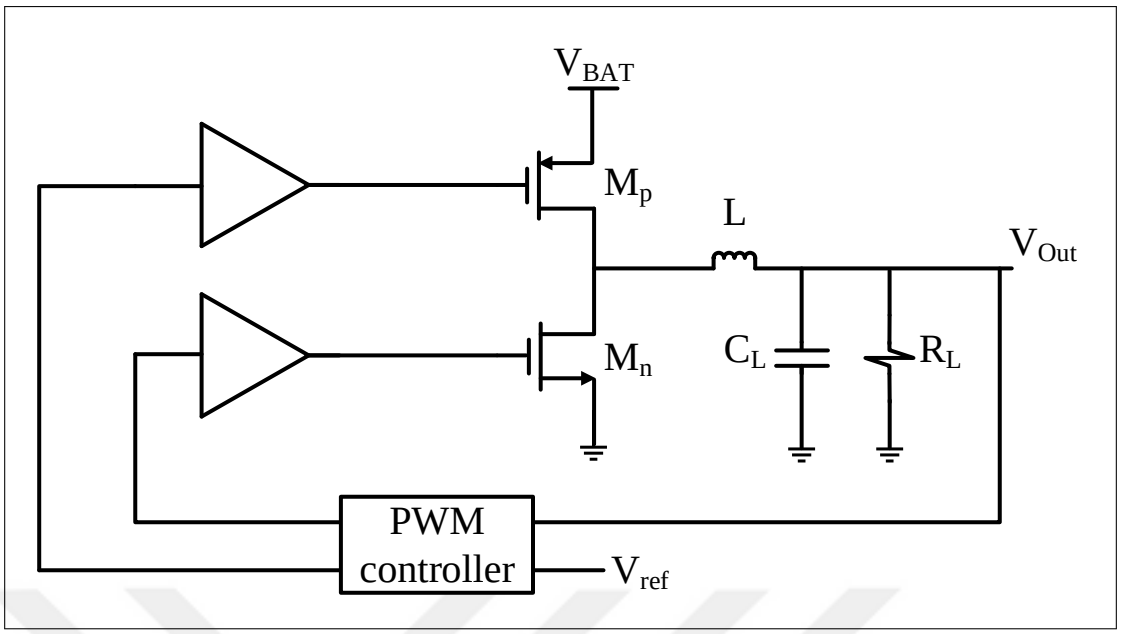

FIGURE 2.1: Inductor based converters

high quality-factor off-chip inductor. These off-chip inductors prevent the converter from being fully integrated. There have been efforts to replace the off-chip inductor with on-chip spiral ones, but these converters suffer from high losses due to higher series inductor resistance and higher switching frequency due to smaller inductor size. Inductor based switching converters also generate electromagnetic interference (EMI) and spur problems due to their switching actions. As a result of these disadvantages, the energy component in the switching converter can be replaced by capacitors that may be integrated on-chip. The resulting converters are categorized as switched capacitor DC-DC converters.

2.1.2 Switched capacitor DC-DC converter

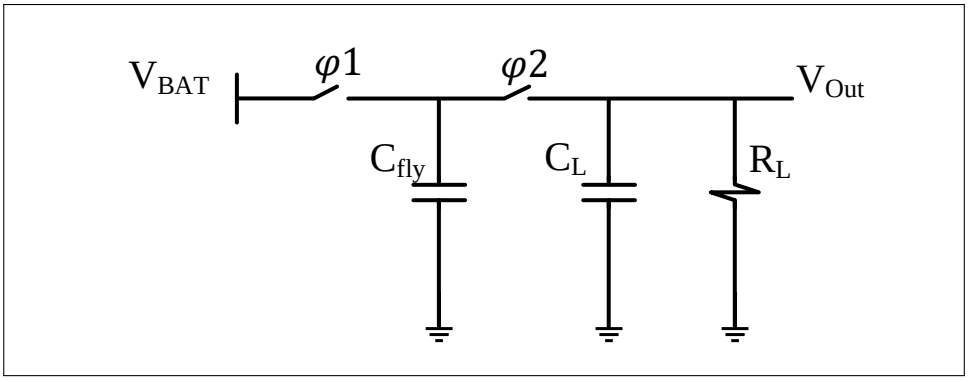

FIGURE 2.2: Switched Capacitor based converters

Switched capacitor regulators, as shown in Figure 2.2, is designed using only capacitors and switches. The substitution of the inductor with a capacitor makes it possible to fully-integrate the regulator. The regulator can provide a variety of voltage conversion ratios, V_{Out}/V_{BAT}, depending on the switched capacitor configuration. The operation of the circuit in Figure 2.2 is defined by the switch configurations. The switches are controlled by signals of the same frequency but with 180°phase difference and preferred to be non-overlapping. The configuration of the switches allows the flying capacitor C_{fly} to be charged from the battery during the first half cycle and to discharge to the load capacitance C_L in the second half cycle. Switched capacitor converters suffer from various losses that limit their efficiency. The main sources of losses are conduction losses, bottom plate capacitor losses and gate-drive losses. Extensive research have been done to analyze and show the impact of these losses on the overall efficiency of these converters. [5][6][7][8]

2.2 Linear Regulators

The second type of DC-DC regulators is the linear regulators. Linear regulators are one of the most widely used blocks in the IC industry. As each SOC is composed of digital, analog, and RF circuits, different linear regulators with different specifications are often designed and integrated to suit each of these circuits. The function of DC-DC regulators is not only to convert a DC voltage to another DC voltage but also to convert it with high integrity. The requirements for these circuits are defined as follows:

- Conversion: The DC-DC regulator should be able to convert the input DC level to the desired output DC level accurately.
- Regulation: The output voltage should be a regulated voltage or a constant output voltage with an allowed variance against a range of variations at the load current and the DC input voltage.
- Power supply rejection: The regulator should reject the noise or the ripples at input DC voltage from the output DC voltage.

- Efficiency: The main function of the regulator is to transfer a form of power to another. The power efficiency of the regulator is one of the most important specifications of a regulator, and it is defined as the ratio of the output and input power of the converter. It is enhanced by decreasing the power consumed by the regulator itself.

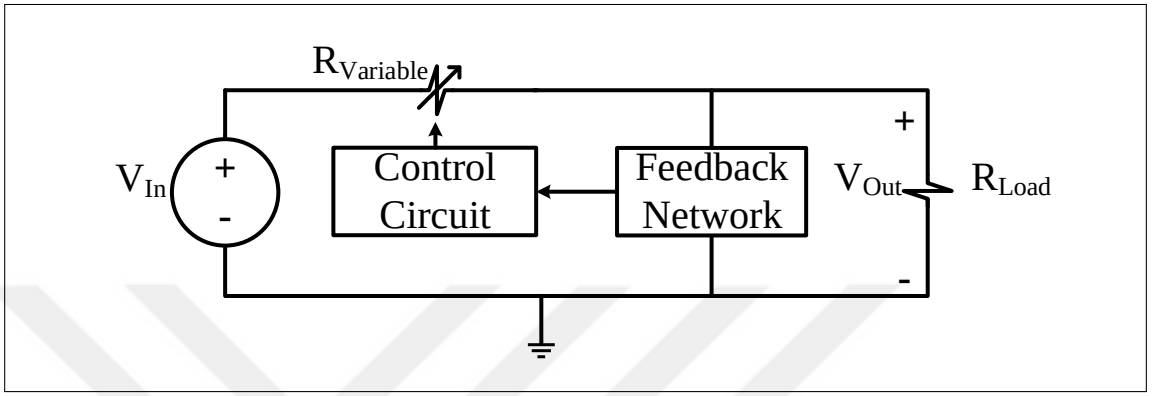

FIGURE 2.3: Linear regulator model

2.2.1 Theory of operation

The linear regulator can be modeled by an ideal voltage source V_{In}, a variable series resistance, a feedback network, and a control circuit as shown in Figure 2.3. Assuming that the feedback network loading effect is negligible, the output voltage will be a potential divider of the input voltage between R_{load} and $R_{variable}$, shown in Equation 2.1

$$V_{Out} = V_{In} * \frac{R_{load}}{R_{load} + R_{Variable}} \tag{2.1}$$

If the output voltage changes as a result of the change of either the input voltage or the load resistance, the feedback network will report this change to the control circuit which will respond linearly to change the value of the variable series resistance to regulate the output voltage to the required value.

This model is realized by the block diagram shown in Figure 2.4. The pass element resembles the variable series resistance, and the error amplifier is the control circuit. Each of these blocks can be implemented by different circuits. The choice between those components and circuits are based on the design specifications of the linear regulator.

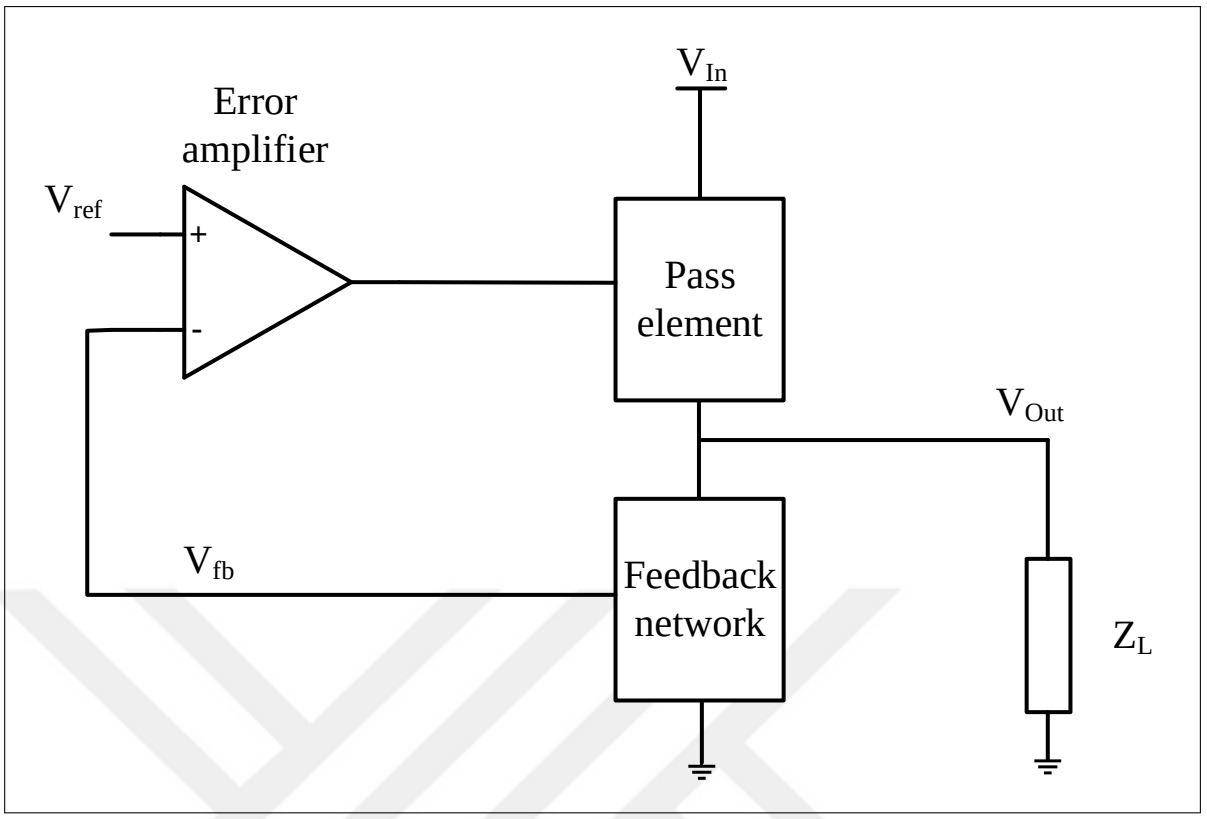

FIGURE 2.4: Linear regulator block diagram

Linear feedback network has four main categories:

1. voltage-mixing, voltage-sampling
2. current-mixing, current-sampling
3. voltage-mixing, current-sampling
4. current-mixing, voltage-sampling

Since we need to sample the output voltage and to mix it with the reference voltage, voltage-mixing, voltage-sampling are commonly used in linear regulators, and this is simply achieved by a potential divider. The error amplifier can be any type of operational amplifier like a single stage common source amplifier, cascaded amplifier, cascode amplifier, or folded cascode amplifier, etc. as long as the amplifier achieves certain specs of gain and bandwidth.

The pass element can be implemented using NMOS or PMOS. PMOS is commonly used as a pass element since the minimum dropout voltage across its terminals is the overdrive

voltage of the transistor, which is smaller than the minimum dropout voltage that can be applied on the NMOS, which is limited by V_{gs}.

Linear regulators are divided into two main categories: low dropout voltage "LDO" and high dropout voltage "HDO". As mentioned previously, PMOS has a lower limit of dropout. Therefore, it is used in LDOs. However, NMOS is used in HDOs as there is no need for its low dropout limit. Furthermore, it achieves better performance regarding stability and power supply rejection.

2.2.2 Efficiency

From the power efficiency definition mentioned earlier, the power efficiency of LDO can be given by Equation 2.2.

$$\eta = \frac{P_{Out}}{P_{In}} = \frac{V_{Out} * I_{Out}}{V_{In} * I_{In}} = \frac{V_{Out} * I_{Out}}{V_{In} * (I_q + I_{Out})} \tag{2.2}$$

where P_{Out} is the power provided by the LDO to the load, P_{In} is the power provided from the supply line to the LDO, I_{In} is the current entering the LDO, I_{Out} is the current delivered to the load, and I_q stands for quiescent current which is the current used in the feedback network and error amplifier.

For a certain conversion from V_{Out} to V_{In}, and certain load current, I_{Out}, it is clear that in order to increase the power efficiency, we should minimize the quiescent current. However, if the quiescent current is assumed to be zero, the efficiency will be defined as Equation 2.3

$$\eta = \frac{V_{out} * I_{out}}{V_{In} * I_{out}} = \frac{V_{out}}{V_{In}} \tag{2.3}$$

This efficiency is called the ideal efficiency of the LDO, and it is limited by the conversion ratio which is the main and only drawback of the linear regulators compared to switching regulators.

2.3 Systems design

Different loads require different regulator specs. Usually, the choice of the type of the regulator is decided depending on the required specifications. Once this is decided, we

can go further with choosing from the different topologies of a particular regulator type. Table 2.1 presents a comparison of switching regulators and linear regulators. Figure 2.5 shows a practical power management system for a SOC. For *Load*1, putting two LDOs in series helps to increase the PSRR, which may be used for RF blocks since RF blocks are very sensitive to noise. The configuration for *Load*2 is less immune to noise, so it is used for conventional analog circuits, and the configuration for *Load*3 is much less immune to noise which is mainly used for digital circuits.

TABLE 2.1: Comparison between Linear regulators and switching regulators.

	Linear regulator	Switched regulator
Power Efficiency	High efficiency only with low drop-out voltages	High, and doesn't depend on the conversion ratio
Transient response speed	High	Low
Output Noise	Low	High
Complexity	Simple	Complex
Cost	Low	High

The combination of the linear and the switching regulators are categorized into two main categories, explained below and represented in Figure 2.6:-

1. Series hybrid linear switching regulators.

   This system is a series combination of switching regulator and linear regulator, where the total conversion ratio is divided between the two regulators. The switching regulator realizes the bigger portion of the conversion ratio to make use of its higher conversion efficiency. The second portion of the conversion is done by the linear regulator to achieve a high PSRR. This system optimizes the power efficiency of the switching regulator with a high PSRR of the linear regulator.

2. Parallel hybrid linear switching regulators.

   This system is a parallel combination of switching regulator and linear regulator. The idea is to divide the load into low-frequency load current supplied by a switching regulator and high-frequency load current provided by a linear regulator. This system is not commonly used for supplying regular loads. However, it is utilized in dynamic power supply modulation of power amplifiers [9], where a dynamic, power efficient, and fast power supply regulator is required.

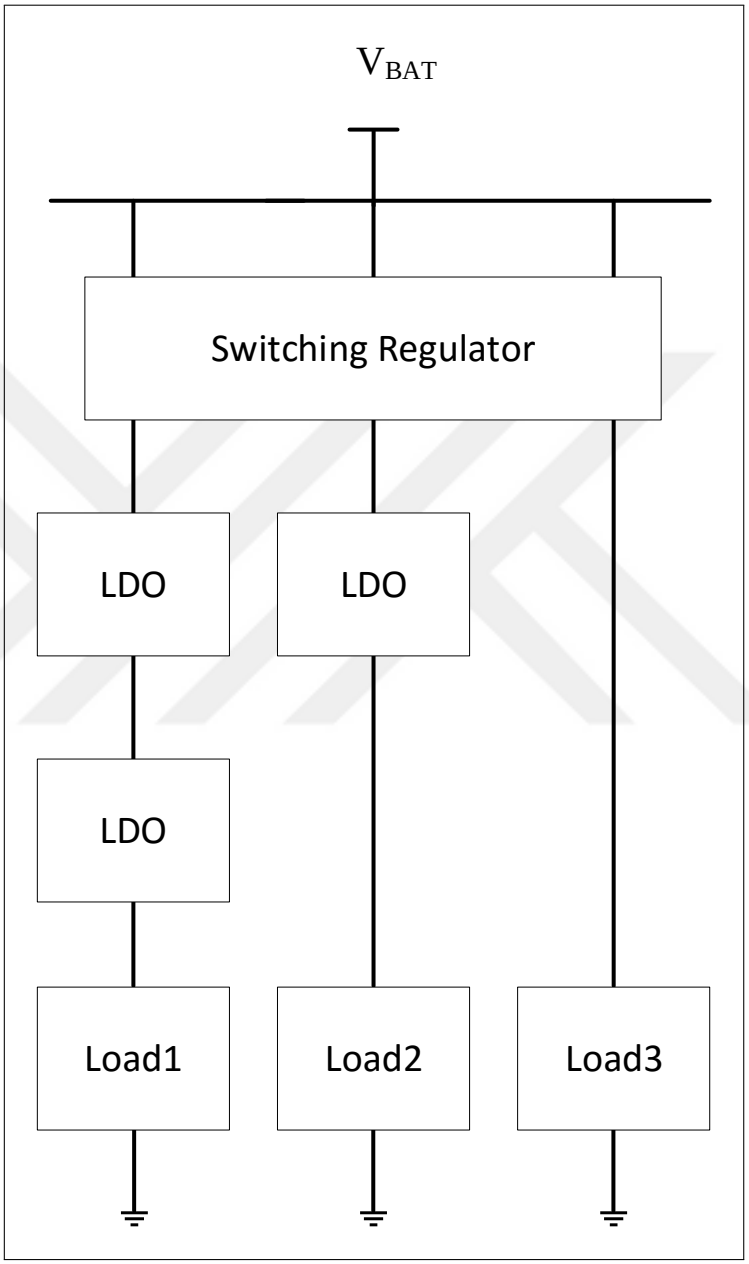

FIGURE 2.5: Power management system for a SOC

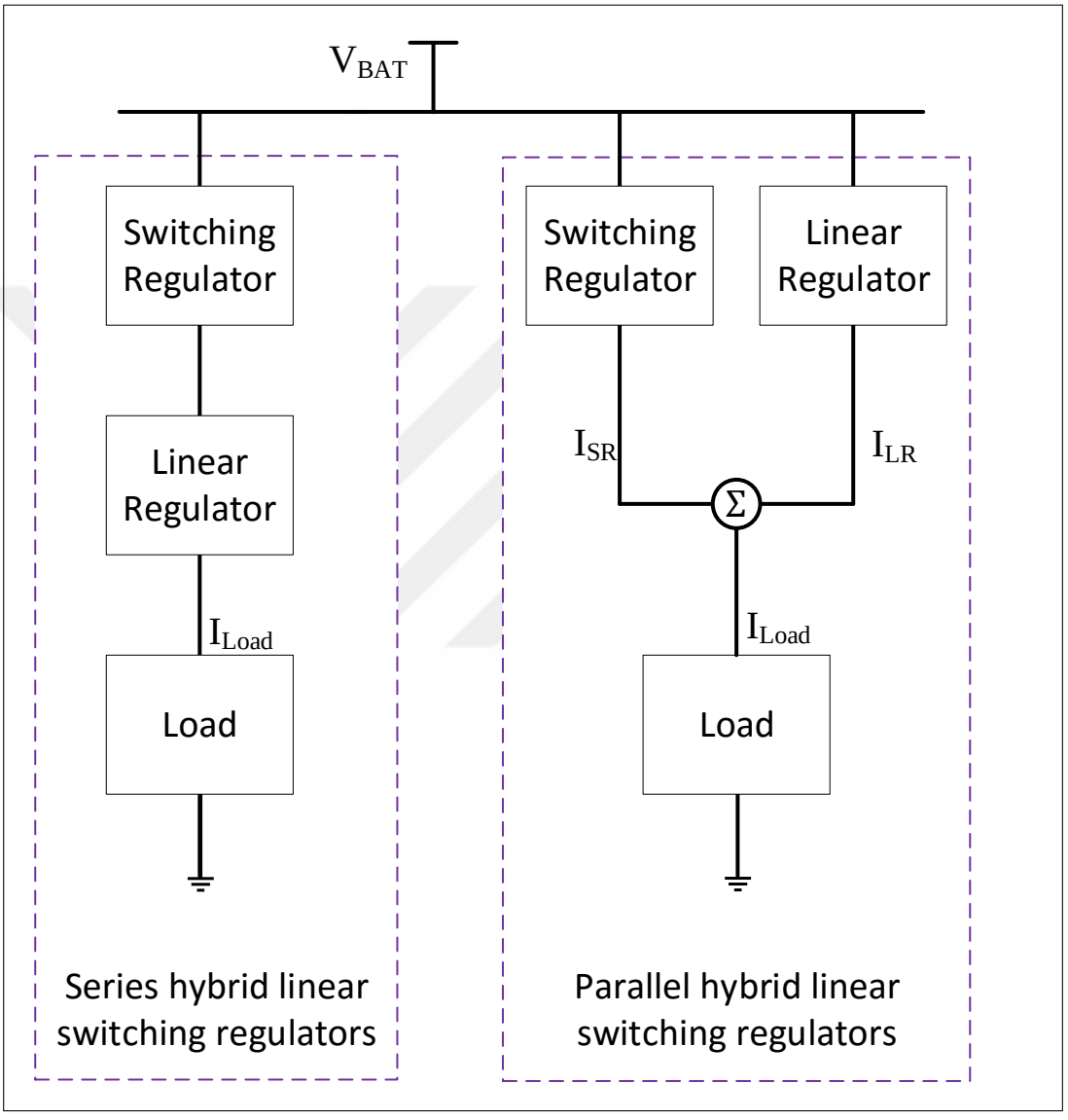

FIGURE 2.6: Types of hybrid regulator systems

Chapter 3

Linear Regulators

In this section, the characterization and the parameters of the LDOs are categorized based on different analysis of these circuits. Figure 3.1 shows a regular LDO circuit.

3.1 DC Analysis

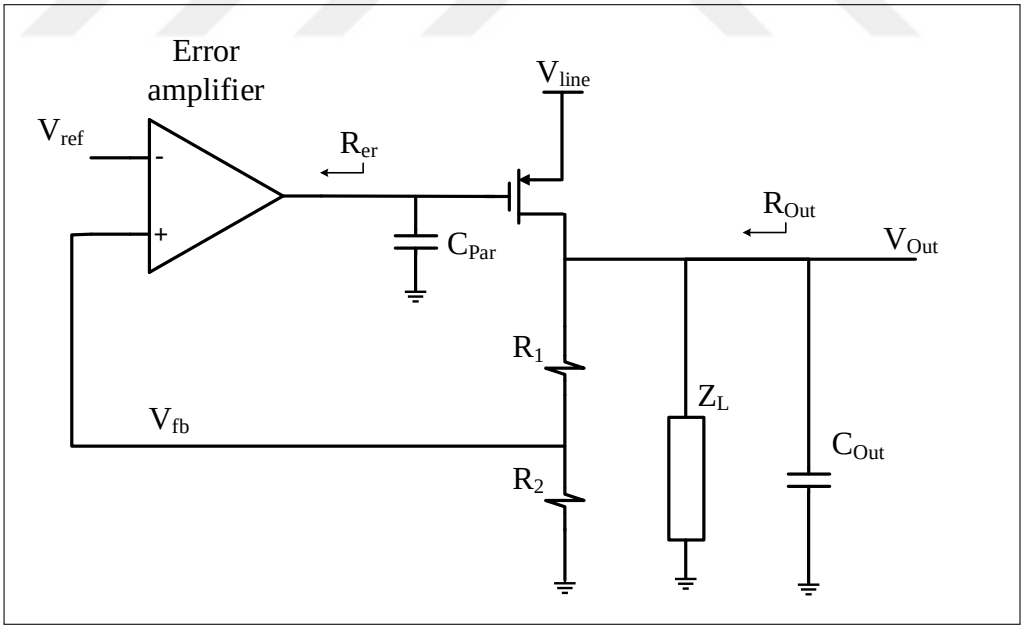

FIGURE 3.1: Regular LDO

The primary parameter characterizing the LDO from the DC perspective is the output voltage regulation. This regulation has two types, Load regulation, and Line regulation.

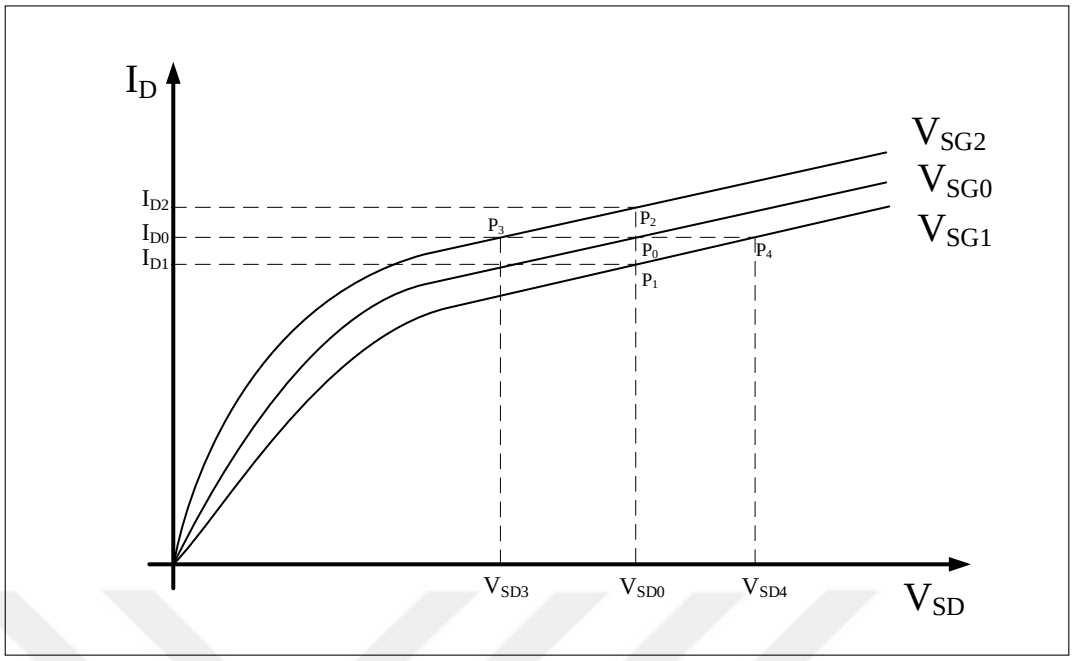

FIGURE 3.2: IV characteristics of the PMOS

1. Load regulation is the ability to supply different load currents with a constant output voltage. Qualitatively, it can be explained using the I-V curve of the MOSFET in Figure 3.2. Assumimg that the operation point is P_0 in Figure 3.2 initially, and the load current, which is the drain current of the PMOS decreases, while the input voltage is constant. Since the line voltage doesn't change and the aim is to provide a constant output voltage which happens to be the drain voltage, the circuit maintains a constant V_{sd} and decreases the drain current by lowering V_{sg}, hence the operation point moves to P_1. The control loop is responsible for doing this; when the load current decreases, V_{fb} increases and consequently, the gate voltage of the PMOS increases which in turn decreases V_{sg} and reduces the load current. On the contrary when the load current increases, the operation point moves to P_2. Loop gain has the key role for load regulation since it is responsible for adjusting the gate voltage to the necessary value finely, and this is shown in detail in the analytical analysis below. Quantitatively, the load regulation is defined by Equation 3.1.

$$LoadRegulation = \frac{\Delta V_{Out}}{\Delta I_{Out}} = R_{OLDO} \tag{3.1}$$

where ΔI_{Out} is the change in the load current, ΔV_{Out} is the change in the output voltage as a result of the load current change, and R_{OLDO} is equivalent output

resistance of the LDO.

From the feedback theory R_{OLDO} is defined by Equation 3.2

$$LoadRegulation = \frac{\Delta V_{Out}}{\Delta I_{Out}} = R_{OLDO} = \frac{R_{On}}{1 + A\beta} \tag{3.2}$$

where R_{On} is the output resistance of the PMOS, β is the potential divider ratio, and A is the open loop gain resulting from the error amplifier and the PMOS common source stage. From Equation 3.2, it is clear that increasing the loop gain is the key factor in decreasing the variation in the output voltage resulting from the changing load current, i.e. enhance the load regulation.

2. The second regulation type is the line regulation, which is the ability to provide a constant output voltage while changing the input line voltage. Qualitatively, similar to load regulation, it can be explained from the MOSFET I-V curve in Figure 3.2. Lets assume that the operation point is at P_0 initially and the line voltage which is the voltage at the source of the PMOS decreases, while the load current is constant. In order to maintain a constant load current while the line voltage decreases, the loop increases V_{sg} by decreasing the PMOS gate voltage and changes the operating point to P_3. However, this correction is limited by the minimum overdrive voltage of the PMOS. The opposite happens if the line voltage increases and the operation point moves to P_4. Quantitatively, the line regulation is defined in Equation 3.3.

$$LineRegulation = \frac{\Delta V_{Out}}{\Delta V_{In}} \tag{3.3}$$

$$\frac{\Delta V_{Out}}{\Delta V_{In}} = \frac{A_{PE}(\Delta V_{In} - \Delta V_G)}{\Delta V_{In}} \tag{3.4}$$

$$\frac{\Delta V_{Out}}{\Delta V_{In}} = A_{PE} - A_{PE}\frac{\Delta V_G}{\Delta V_{In}} \tag{3.5}$$

$$\frac{\Delta V_{Out}}{\Delta V_{In}} = A_{PE} - A_{PE}A_{er}\beta\frac{\Delta V_{Out}}{\Delta V_{In}} \tag{3.6}$$

$$\frac{\Delta V_{Out}}{\Delta V_{In}}(1 + A_{PE}A_{er}\beta) = A_{PE} \tag{3.7}$$

$$\frac{\Delta V_{Out}}{\Delta V_{In}} = \frac{A_{PE}}{1 + A_{PE}A_{er}\beta} \tag{3.8}$$

$$LineRegulation = \frac{\Delta V_{Out}}{\Delta V_{In}} \approx \frac{1}{A_{er}\beta} \tag{3.9}$$

where A_{PE} is the PMOS common source stage gain, A_{er} is the error amplifier gain, and ΔV_{In} is the change in the input line voltage [1].

Equation 3.9 shows that similar to Load regulation, error amplifier gain controls the line regulation.

3.2 AC Analysis

Analyzing the LDO from an AC perspective, it is a negative feedback circuit with several poles and zeros. In order to ensure stable operations, the design needs to meet the Phase and Gain Margin requirements.

Typically, LDOs have two dominant poles. Going back to Figure 3.1, the first pole is located at the output node of the LDO and defined by Equation 3.10, and the second pole is located at the gate of the pass element and defined by 3.11. Other parasitic poles usually exist within the error amplifier due to internal nodes.

$$\omega_{P1} = \frac{1}{C_{Out} R_{Out}} \tag{3.10}$$

$$\omega_{P2} = \frac{1}{C_{Par} R_{er}} \tag{3.11}$$

where C_{Out} is the equivalent capacitance at the output node of the LDO, R_{Out} is the equivalent resistance at the output node of the LDO, R_{er} is the output resistance of the error amplifier, and C_{par} is the equivalent capacitance at the gate of the PMOS. C_{par} is dominated by the PMOS gate capacitance, as this transistor is always designed large to support a high load current. Two methods are used to stabilize this circuit.

1- The first and the commonly used is to make the output pole the dominant pole by adding a large off-chip capacitor in the range of microfarads [2][3][10]. This large capacitor makes the output node a dominant pole and assures an adequate phase margin. This method has several drawbacks: Firstly, this is not a fully integrated solution, which is highly desired in today's low cost solutions. Secondly, off-chip capacitor comes with ESR which introduces another pole and zero. The ESR value varies with temperature and process making the stability a little more complicated.

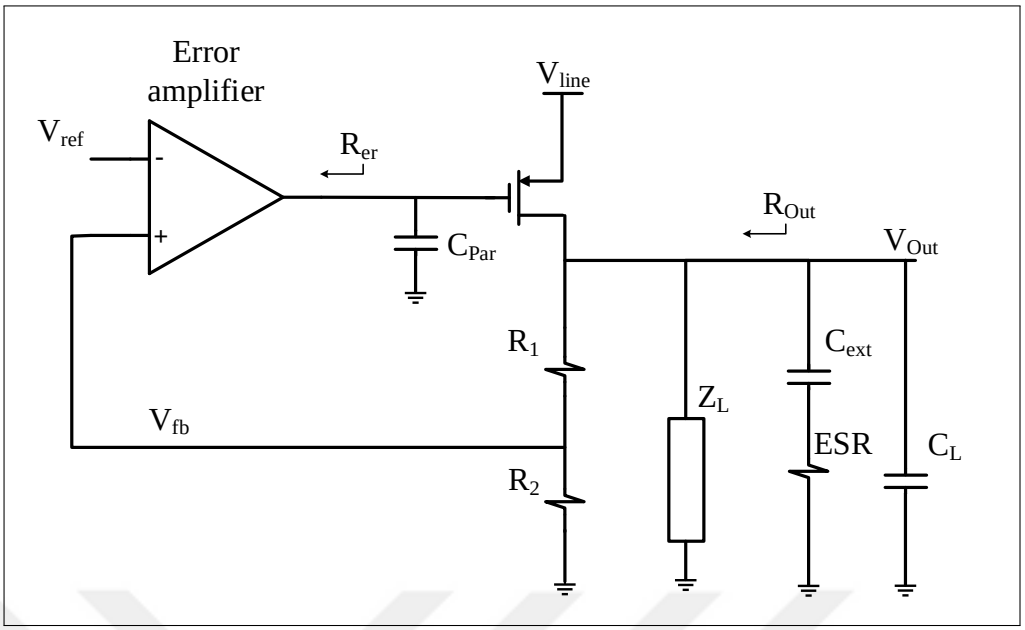

FIGURE 3.3: Regular LDO with external capacitance

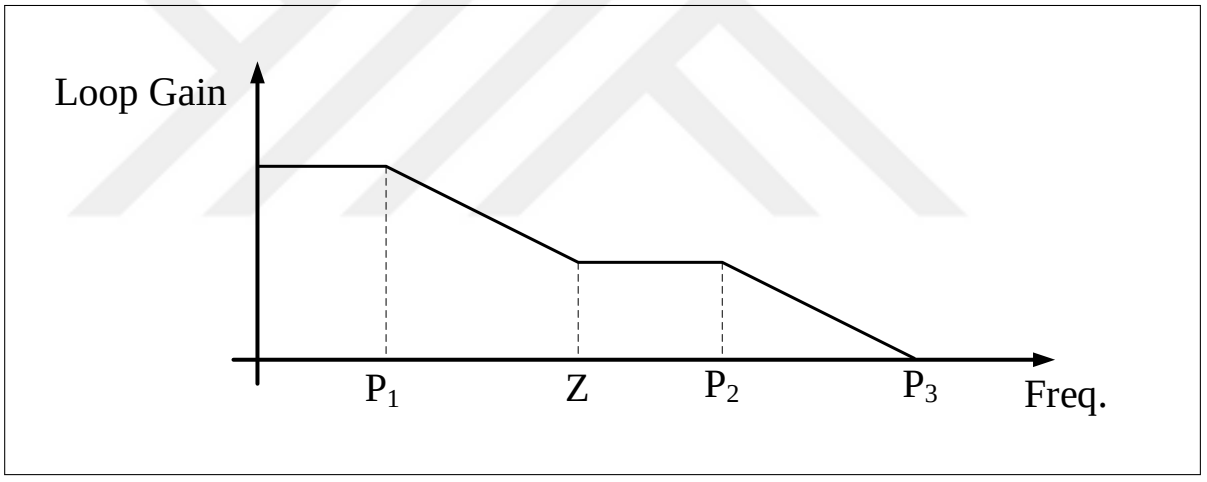

FIGURE 3.4: Frequency response of external capacitor LDO

Equations 3.12, 3.13, 3.14, and 3.15 define the values of the poles and the zero of the circuit in Figure 3.3 that utilizes output compensation.

$$\omega_{P1} = \frac{1}{C_{ext} R_{Out}} \tag{3.12}$$

$$\omega_{P2} = \frac{1}{C_{Par} R_{er}} \tag{3.13}$$

$$\omega_{P3} = \frac{1}{C_L R_{esr}} \tag{3.14}$$

$$\omega_Z = \frac{1}{C_{ext} R_{esr}} \tag{3.15}$$

where C_{ext} is the added external capacitor, C_L is the load capacitance, and R_{esr} is the ESR. Figure 3.4 represents a typical frequency response for this method with an acceptable phase margin [2].

2- The second method is called capless LDO. The stability of the circuit is achieved by making an internal pole the dominant one [10][11][12]. Introducing a large capacitor using Miller theorem is one of methods utilized for achieving the compensation.

Miller theorem states that if a capacitor is connected between input and output of a negative high gain amplifier, the equivalent capacitors at the input and output are defined by Equations 3.16 and 3.17.

$$C_{In} \approx C_{Mi}|A_{Mi}| \tag{3.16}$$

$$C_{Out} \approx C_{Mi} \tag{3.17}$$

where C_{In} is the equivalent input capacitor and C_{Out} is the equivalent output capacitor. However, Miller capacitor introduces a right-hand plane zero, which deteriorates the stability by decreasing the phase of the loop. This problem can be solved by adding a resistance in series with the Miller capacitor. The new zero frequency is defined by Equation 3.18. The RHP zero can be converted to LHP zero by making sure that the series resistance is larger than the transconductance of the amplifier. The LHP zero frequency can be set to cancel any other parasitic pole to enhance the stability, or based on the design conditions, the designer can eliminate the zero by setting the series resistance equal to the transconductance of the amplifier. The problem of this method is, the values of the Miller resistance and capacitance are usually large if the load capacitance is large, and this slows down the response of the regulator.

$$\omega_Z = \frac{1}{C_{Mi}(g_m^{-1} - R)} \tag{3.18}$$

It is also important to mention that a comparison between External capacitor LDO and capless LDO is unfair, since each approach has advantage for different specs such as PSRR and transient response.

3.3 Transient Analysis

While DC analysis defines the steady state operation of the LDO, transient analysis describes the transient response of the LDO due to sudden load changes. As described in the DC load regulation, when the load current changes, the operating point changes. Due to the finite response speed of the LDO, the circuit takes some time to respond. The limit in speed is due to the limited bandwidth of the LDO and the slew rate delay caused by the error amplifier. Figure 3.5 shows a typical LDO response due to sudden load change from no load to full load. Due to this sudden increase in the current, the output voltage drops by ΔV_S, which is called the overshoot or the undershoot. This is an important spec of the LDO and it needs to be minimized, since especially undershoot cause regulation to disappear for this short amount of time. ΔV_S is defined by Equation 3.19.

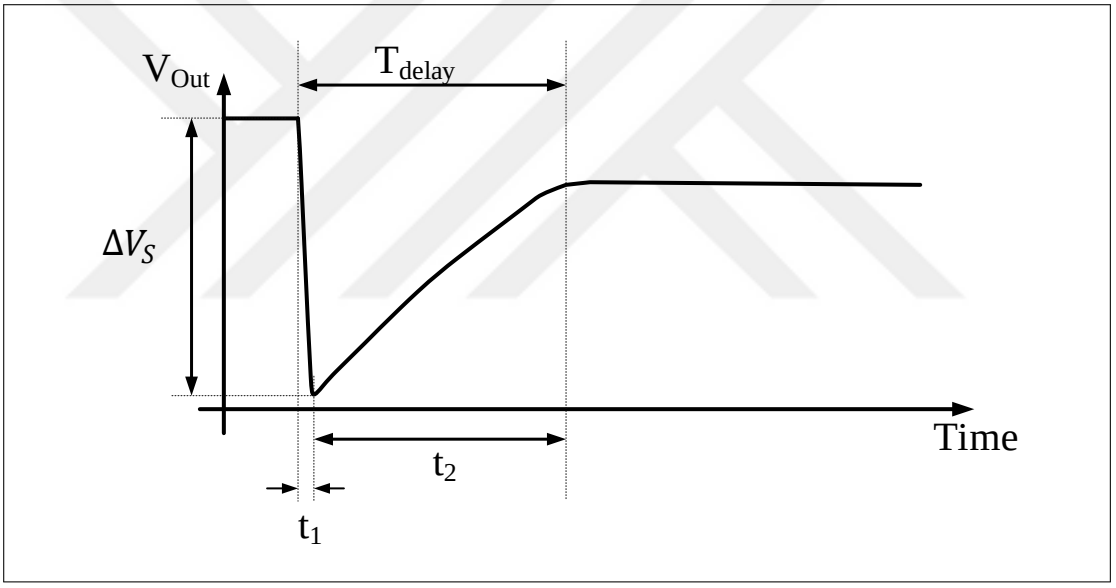

FIGURE 3.5: Transient response of regular LDO

$$\Delta V_S = \frac{\Delta I_{Out}}{C_{ext} + C_L} t_1 + V_{esr} \tag{3.19}$$

where V_{esr} is the voltage change due to the ESR, and t_1 is the time taken by the LDO to respond and it's given by Equation 3.20.

$$t_1 = \frac{1}{BW} + t_{SR} = \frac{1}{BW} + \frac{\Delta V}{I_{SR}} C_{Par} \tag{3.20}$$

where BW is the closed loop bandwidth of the LDO, t_{SR} is the delay caused by the slew rate effect, ΔV is the change in the voltage seen by C_{Par}, and I_{SR} is the current of the output stage of the amplifiers. t_2 in Figure 3.5 is the time it takes the PMOS device to charge the output capacitor and it depends on the phase margin of the feedback loop. From Equation 3.19, it is apparent that decreasing t_1 decreases the undershoot, and from Equation 3.20, t_1 is a function of the bandwidth and slew rate which depend on the error amplifier current. Consequently, there is a tradeoff between the power efficiency and the undershoot. Additionally, increasing the output capacitor minimizes the undershoot. This is one of the reasons that LDOs with external capacitors are more efficient for high-speed applications. Capless LDOs are slower than external capacitor LDOs and various techniques have been proposed ([10][11][12]) to enhance their transient response.

Chapter 4

Implemented System and Proposed Circuit

4.1 Parallel Hybrid Regulators

Researchers have been trying to tackle the issue of a fast, all integrated and highly efficient converter for a long time. Parallel hybrid regulator is a good approach, as the combination makes use of the high-speed regulation of a linear regulator and the high power efficiency of a switching regulator. One problem with the parallel hybrid regulators is that the distribution of load on both regulators is not always clear [9]. And because the linear regulator load contribution is not defined, it might supply most of the load. Consequently, power efficiency of the whole system may suffer as a result.

This work redefines the system with small modifications to assure that the previously mentioned problem doesn't exist. Since the advantage of the linear regulator is its high speed of regulation, the linear regulator should be off in supplying stable loads, and the high efficiency switching regulator supplies the load solely. The linear regulator only gets activated in sudden load changes to prevent any overshoot and undershoot in the output voltage, then goes back to idle mode. This assures that the system benefits from the high power efficiency of the switching regulator at stable loads and the high-speed regulation of the linear regulator in sudden load changes.

4.2 Proposed Linear Regulator

For the proposed parallel system explained in the previous section, the linear regulator needs to be off or disconnected at steady state with minimum power consumption to maintain the high power efficiency of the system. At sudden load changes, the linear regulator senses the output voltage variation and gets activated to regulate the output voltage with high speed until the switching regulator responds, and then the linear regulator goes back to sleep mode again. Figure 4.1 shows the circuit diagram for the proposed linear regulator that accomplishes this functionality. This circuit is composed of a class AB output stage and two feedback loops that work simultaneously to create three regions of operations shown in Figure 4.2. Details of the working principle of this circuit are given below.

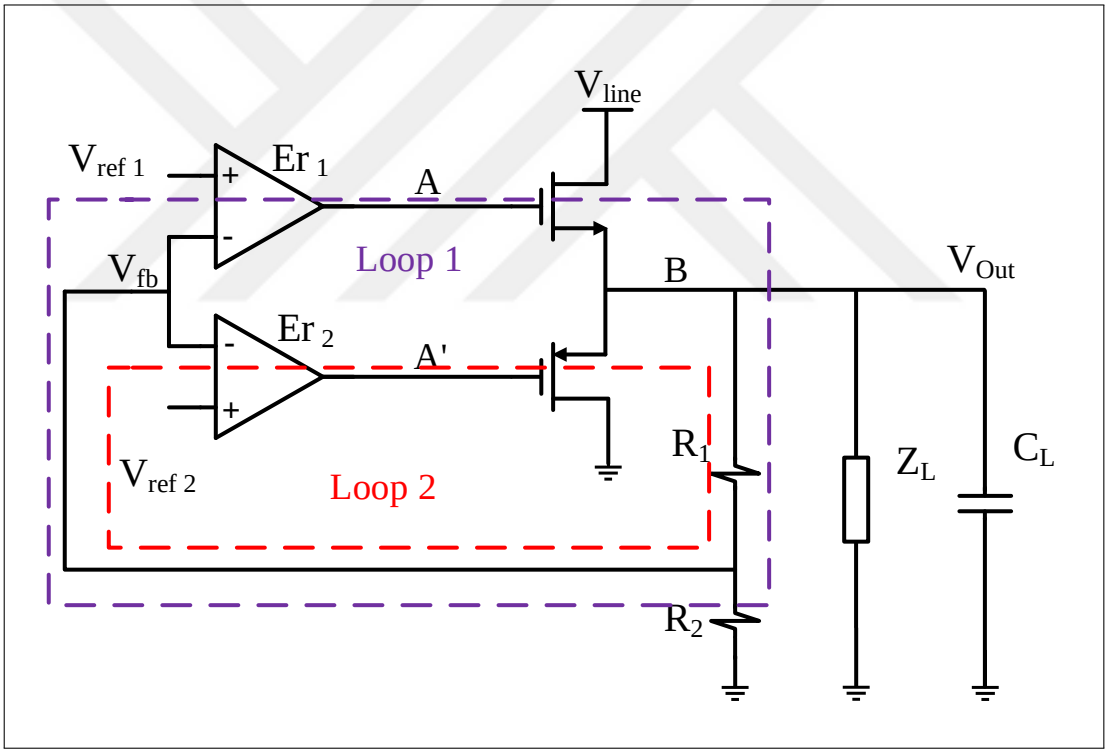

FIGURE 4.1: Circuit diagram for the proposed linear regulator

4.2.1 DC Analysis

As mentioned previously, the linear regulator is expected to kick-in during transient changes to help regulate the output voltage. The operation of the linear regulator is divided into three regions of operation. The first region of operation is Region zero

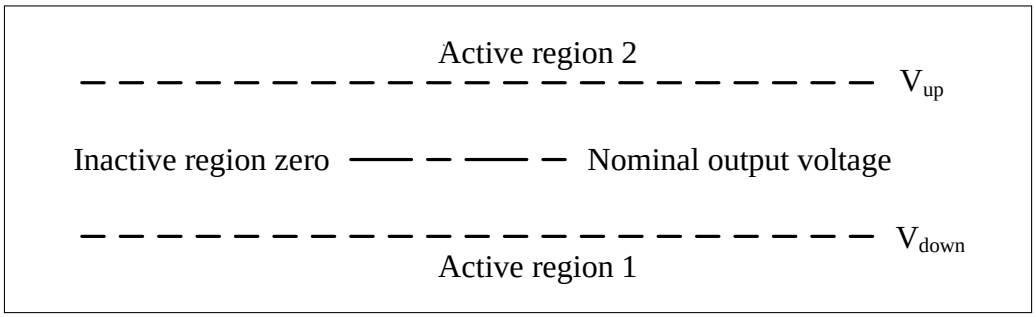

FIGURE 4.2: Regions of operation of the linear regulator

defined in Figure 4.2. The output voltage lies between V_{up} and V_{down}, and they are defined by Equations 4.1 and 4.2, which are set slightly offset from the desired nominal output value.

$$V_{down} = V_{ref1}\frac{R_1 + R_2}{R_2} \tag{4.1}$$

$$V_{up} = V_{ref2}\frac{R_1 + R_2}{R_2} \tag{4.2}$$

In this region of operation, V_{fb} lies between V_{ref1} and V_{ref2} and both of the loops are disabled as follows. The first loop tries to regulate the output voltage to V_{down} by trying to decrease the output voltage. It achieves this by pulling down the gate of the NMOS device, eventually shutting it down by pulling the gate to ground. Oppositely, the second loop tries to regulate the output voltage to V_{up} by pulling up the PMOS gate, eventually shutting the PMOS device. When the output voltage is within the range of the nominal output voltage, the output stage is completely disabled, and the only power consumption in the linear regulator is the power consumed in the error amplifiers.

In the case of sudden increase in the load current, the switching regulator often is not able to respond to this fast change and the output voltage decreases to go below V_{down} and enter Region 1. As V_{Out} decreases below V_{down}, V_{fb} decreases below V_{ref1} and Er_1 pulls the NMOS gate voltage up. This switches on the NMOS and allows it to regulate the output voltage to V_{down} by supplying the current shortfall. The second loop also attempts to regulate the output to V_{up} by turning off the PMOS as explained in Region zero. After the switching regulator responds and regulates the output voltage to the nominal output voltage into Region zero, the first loop shuts down the NMOS again. For the case of a sudden decrease in the load and the slow response of the switching

regulator, the output voltage overshoots and increases above V_{up}, V_{fb} also increases above V_{ref2}. The first loop tries to regulate the output voltage to V_{down} by reducing the gate voltage of the NMOS device and turning it off. However, since V_{fb} is larger than V_{ref2} for the second loop, the gate voltage of the PMOS decreases and the device turns on, regulating the output voltage by draining the excess amount of current. After the switching regulator responds and regulates the output voltage to the nominal output voltage into Region zero, the second loop shuts down the PMOS again.

4.2.2 AC Analysis

Analyzing the circuit in Figure 4.1 from AC perspective, the circuit contains two loops and each loop has two main poles at nodes A and B and one zero. The poles of this nodes are given by Equations 3.11 and 3.10, and the zero is given by Equation 4.3.

$$\omega_z = \frac{gm}{C_{gs}} \tag{4.3}$$

Taking a closer look at the poles and the zero values, the RHP zero is located at a higher frequency compared to the two poles. To ensure the stability of the circuit, the frequency of the two poles need to be allocated far from each other, i.e. one pole is dominant enough to stabilize the circuit and provides enough phase margin. Since the system is designed for ultra low power applications, the error amplifiers are designed with low current resulting with a high output resistance for the error amplifiers. Consequently, the internal pole is located at a very low frequency.

The output capacitance associated with the output pole is determined by the switching regulator and set to be in the range of $10nF$ in this case, which is not enough to make the output node pole the dominant one. Furthermore, the value of the first pole changes dramatically for different load current values. For example, if the operation of the linear regulator is in the active region with high load current, R_{Out} value is estimated to be small and ω_{P_1} is located at high frequency. When the switching regulator is responding and the linear regulator is in Region zero as described in the DC Analysis section, R_{Out} value increases and moves ω_{P_1} to a lower frequency. This results in the frequency of ω_{P_1} to change from high frequency to a low frequency, which may be even lower than the internal pole frequency. Hence, the system is not stable and needs to be compensated.

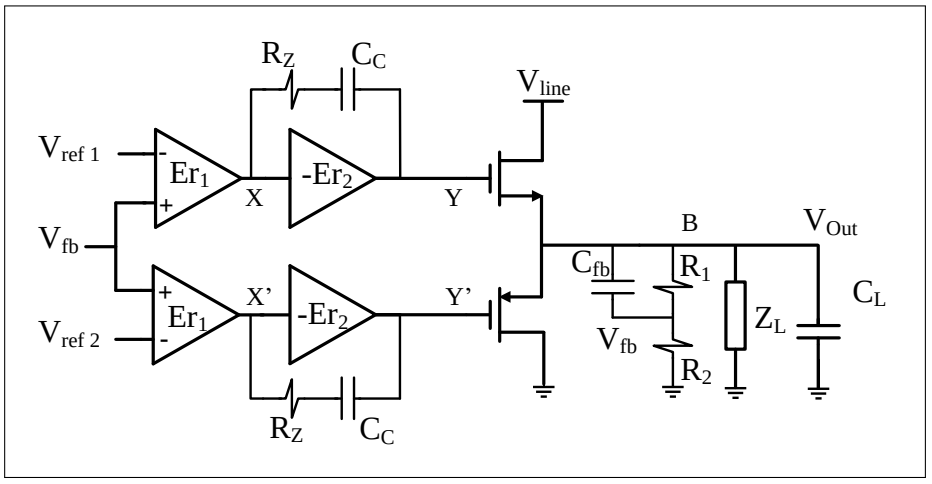

FIGURE 4.3: Proposed linear regulator with the compensation solution

Simple compensation techniques are applied to stabilize the circuit presented in Figure 4.3. The error amplifiers are implemented by two stage common emitter amplifier. Adding a Miller compensation capacitor creates a dominant pole to stabilize the circuit. The equivalent capacitors' values are defined by Equations 4.4 and 4.5.

$$C_{In_M} \approx C_c|A_2| \tag{4.4}$$

$$C_{Out_M} \approx C_c \tag{4.5}$$

where C_{In} is the equivalent input capacitor, C_{Out} is the equivalent output capacitor, and A_2 is the gain of Er_2.

R_z is added to convert the RHP zero to a left LHP zero. Also, a second zero is introduced by adding C_{fb} to flatten the gain and increase the UGB. Adding C_{fb} also introduces another pole but at a higher frequency compared to the zero. The poles and the zeros are defined as follows:

$$\omega_{P_X} = \frac{1}{C_{In_M} R_X} \tag{4.6}$$

$$\omega_{P_Y} = \frac{1}{C_Y R_Y} \tag{4.7}$$

$$\omega_{P_B} = \frac{1}{C_{Out} R_{Out}} \tag{4.8}$$

$$\omega_{P_{fb}} = \frac{R_1 + R_2}{C_{fb} R_1} \tag{4.9}$$

$$\omega_{Z_{Cc}} = \frac{1}{C_c(g_m^{-1} - R_z)} \tag{4.10}$$

$$\omega_{Z_{fb}} = \frac{1}{C_{fb} R_1} \tag{4.11}$$

where ω_{P_X} , ω_{P_Y}, ω_{P_B}, and $\omega_{P_{fb}}$ are the poles located at nodes X, Y, B and V_{fb} respectively, $\omega_{Z_{Cc}}$ and $\omega_{Z_{fb}}$ are the zeros created by coupling capacitor and feedback capacitor respectively, and g_m is the transconductance of Er_2.

The configuration of the poles and zeros is set as follows: ω_{P_X} is the dominant pole, $\omega_{Z_{Cc}}$ cancels the first non dominant pole ω_{P_Y}, and $\omega_{Z_{fb}}$ is located in the frequency range of ω_{P_B} to ensure the stability of the circuit.

4.2.3 Transient Analysis

As explained in the transient analysis section in Chapter 3, the linear regulator suffers overshoot or undershoot due to sudden load changes. Analyzing the proposed linear regulator in Figure 4.3 and applying Equations 3.19 and 3.20, the linear regulator suffers a high overshoot and undershoot because of the following reasons:

1. Since the applications of this work are ultra low power, the error amplifiers are designed with a very low current. Low current error amplifiers have high resistive output nodes which result in a low bandwidth of the circuit. From Equation 3.20, low bandwidth leads to high t_1.

2. The slewing time is estimated to be high due to the low current used in the error amplifiers and the high C_{Par}, this leads to high t_1 according to Equation 3.20.

3. The relatively low output capacitance and the high t_1 result in high overshoot and undershoot according to Equation 3.19.

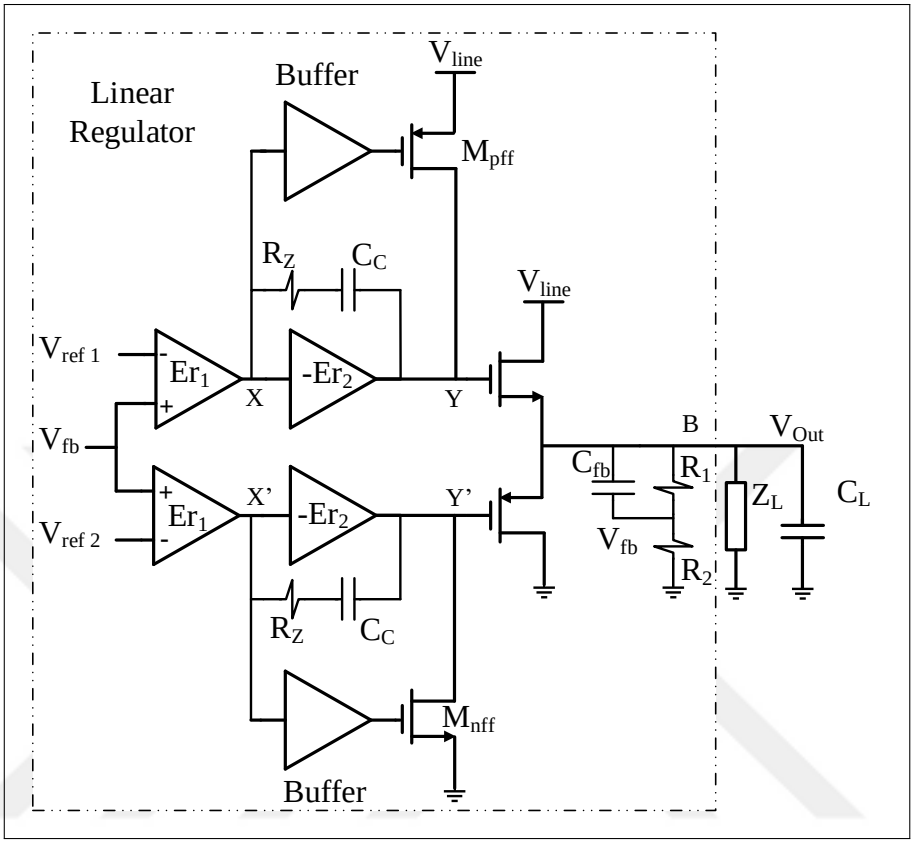

FIGURE 4.4: Proposed linear regulator with the compensation and transient solutions

Figure 4.4 shows a proposed solution to enhance the transient response parameters. The solution is done by adding a switching current instead of increasing the DC current to reduce the power consumption. Two feed-forward paths are added to the linear regulator to realize the switching currents contributions. The feed-forward paths are composed of analog buffers and pull-up switch M_{pff} for the NMOS and pull-down M_{nff} switch for the PMOS.

To explain the work of the feed-forward paths, let us consider the case of a sudden drop in the output voltage due to an increase of the load current and before the loop linearly regulates the output voltage. The feedback voltage drops and consequently the voltage at node X drops. So, the voltage at node Y increases by charging the high equivalent capacitance at this node, C_{Par}, with the low DC current used at the amplifier. This delay is limited by the slew rate of the amplifier. By adding the feed-forward path, the voltage decrease at node X is buffered to pull the gate of M_{pff} low. When the gate of

M_{pff} is pulled to ground, M_{pff} is switched on to charge C_{Par} with the added current which is a function of the dimensions of M_{pff}. After the loop is regulated, the voltage at node X returns to its normal value and is buffered to generate VDD at the gate of M_{pff} to turn it off again. This limits the undershoot by eliminating the slew rate delay without increasing the power consumed in the error amplifiers in steady-state. The reverse operation happens in the other path when the output voltage overshoots.

Analytically, the delay due to slew rate is defined by Equation 4.12.

$$t_{SR} = \frac{\Delta V}{I_{SR}} C_{Par} \tag{4.12}$$

After adding the feedforward path, the slew rate delay can be redefined by 4.13.

$$t_{SR} = \frac{\Delta V}{I_{DC_{SR}} + I_{SW_{SR}}} C_{Par} \tag{4.13}$$

where $I_{DC_{SR}}$ is the current of the second stage of the error amplifiers, and $I_{SW_{SR}}$ is the current added by the feedfarward path through M_{pff}, which is defined by Equation 4.14.

$$I_{SW_{SR}} = 1/2\mu C_{ox}(W/L)(VDD - V_{th})^2 \tag{4.14}$$

where $\mu, C_{ox}, (W/L)$, and V_{th} are the mobility, oxide capacitance, dimensions, and thershold voltage of M_{pff} respectively.

By setting the delay due to slew rate to be less than 10% of the bandwidth delay, the slew rate part of the delay in Equation 3.20 can be ignored. Figure 4.5 shows the response with and without the feedfarward path.

4.2.4 Design and Results

The circuit in Figure 4.4 is implemented using $7\mu A$ current distributed as follows:

- The first stage of the error amplifiers consume $2\mu A$ each.
- The second stage of the error amplifiers consume $1\mu A$ each.

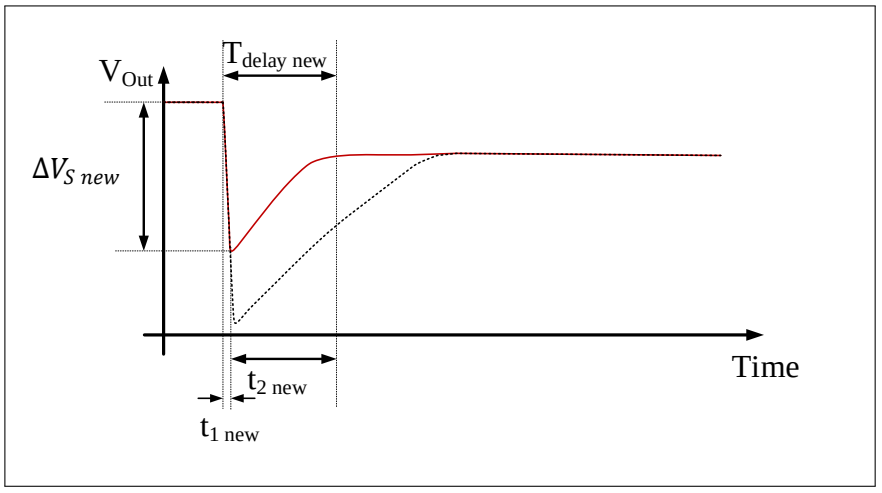

FIGURE 4.5: Transient response of the linear regulator with and without the feedfarward path

- The feedback network consumes $1\mu A$.

The linear regulator is designed to have 32 output voltages ranging from $380mV$ to $1V$ with step of $20mV$. The programmability is done by using a resistor-DAC for R_1 using simple switches with 5 bit controls. Figure 4.6 shows the programmable feedback network.

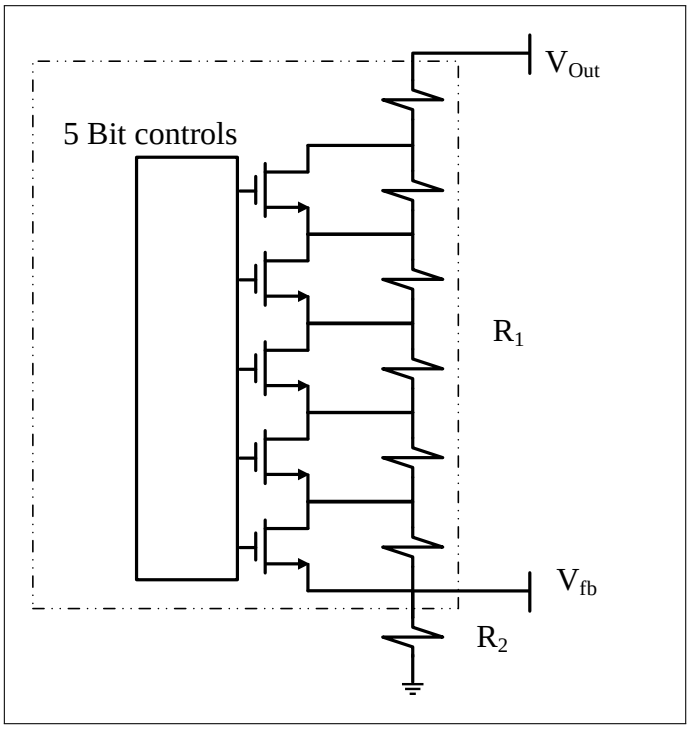

FIGURE 4.6: Programmable feedback network with 32 variable configurations

The DC functionality of the linear regulator is tested using the test bench in Figure 4.7, where the linear regulator is programmed to have an output voltage of $1V$ and connected to a load resistance of $100ohms$. A current source with a variable DC current is connected at the output node to model the switching regulator. The current source is used to push a variable current ranging from 0 to $20mA$ to the load. Figure 4.8 shows the results of the output voltage, current supplied by the NMOS and current drained by the PMOS. The results illustrate that at Region zero, the NMOS and the PMOS are switched off. Only at Region 1 the NMOS is switched on to supply current to the load, and only at Region 2 the PMOS is switched on to drain current from the current source. The maximum current the linear regulator can supply or drain is $10mA$.

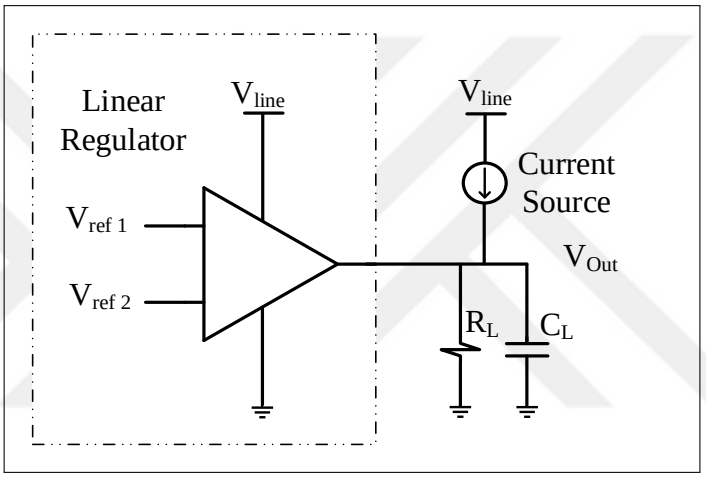

FIGURE 4.7: Test bench used to simulate the linear regulator for DC and Transient analysis

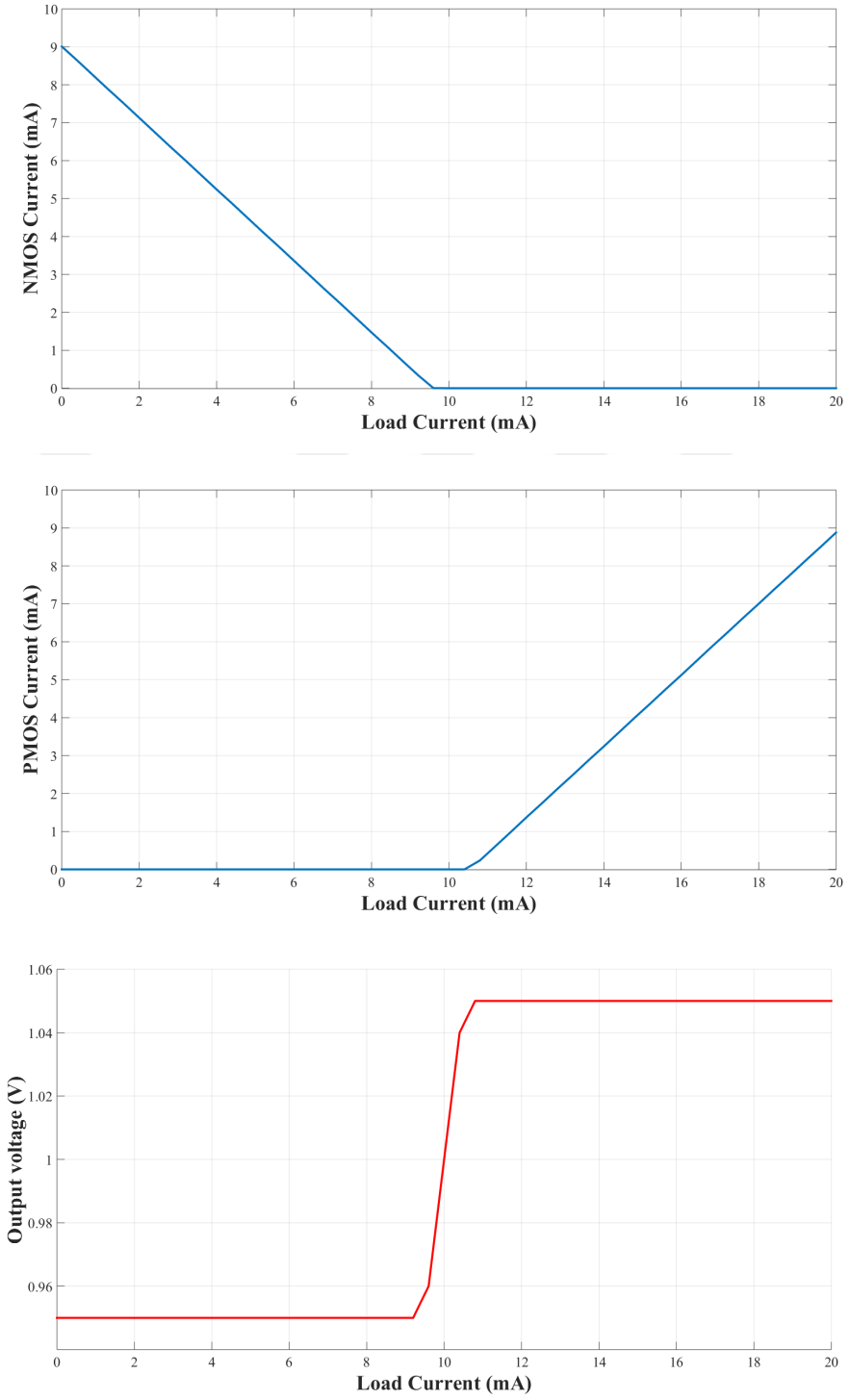

FIGURE 4.8: DC Analysis (a) Current supplied by the NMOS (b) Current drained by the PMOS (c) Output voltage in different regions of operation.

The stability of the linear regulator is simulated using the same test bench in Figure 4.7. The changing current changes the operating point and hence the frequency response. Figure 4.9 presents the frequency response of the first loop. It shows that as the variable current supplied by the current source increases, and the current supplied by the linear regulator decreases, the pole at the output node shifts to a lower frequency. The minimum phase margin is approximately 67°across all load values.

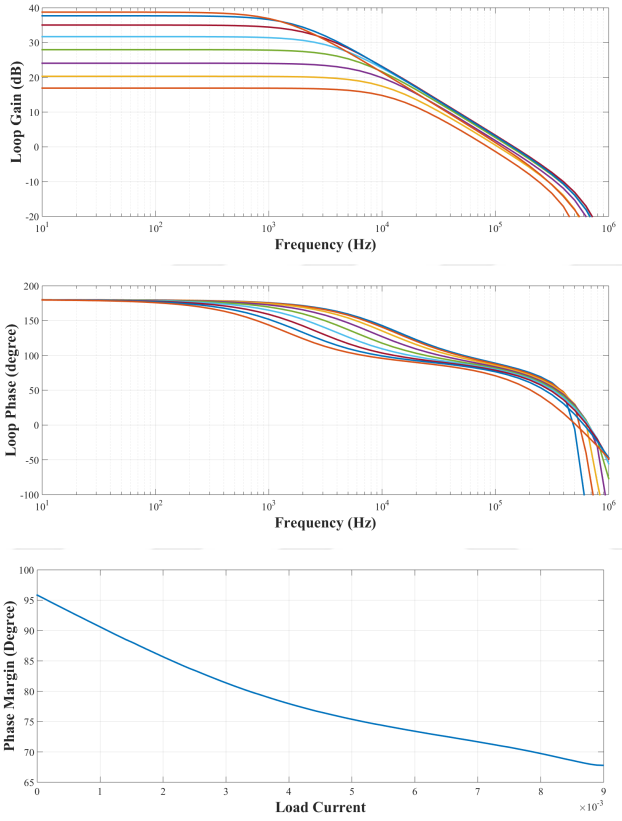

FIGURE 4.9: Frequency response of the linear regulator (a) Loop gain (b) Loop phase (c) Phase Margin.

The transient response of the linear regulator is simulated using the same test bench in Figure 4.7. The current source supplies sudden transient current pulses to the load changing from $10mA$ to 0 to test the undershoot. Output NMOS device supplies the current to the load during these transients. Also, the current source is set to supply a transient current changing from $10mA$ to $20mA$ to test the overshoot, where the PMOS should drain current from the output node. Figure**??** ws the simulation results of the transient response of the linear regulator for the maximum and minimum output voltages. The results show that the maximum undershoot and overshoot is less than $100mV$ from V_{up} and V_{down}.

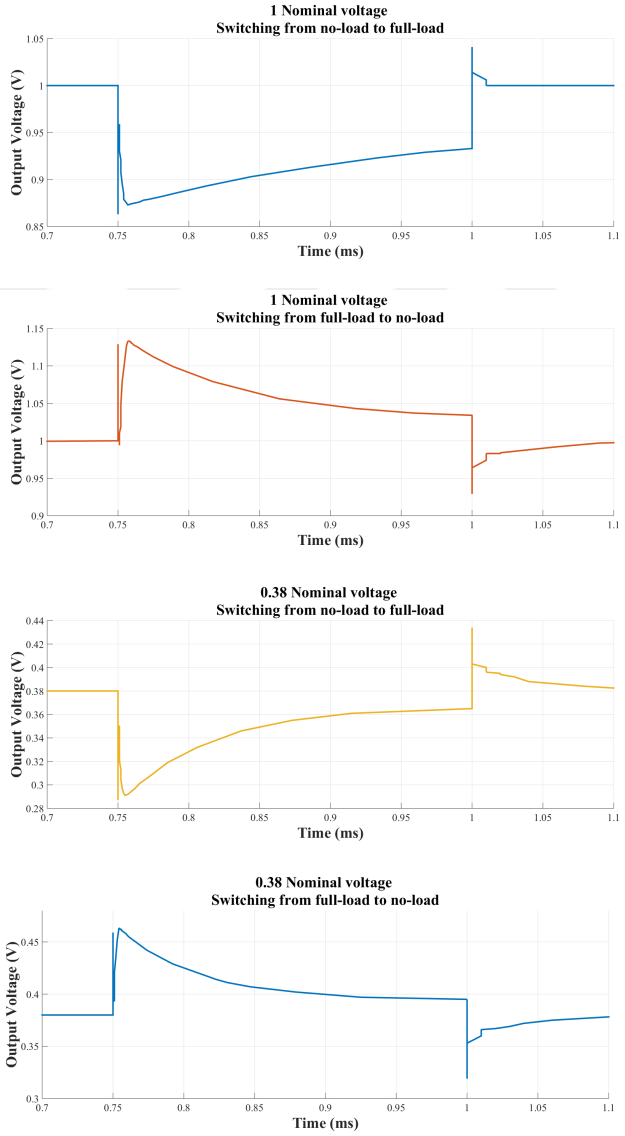

FIGURE 4.10: Transient response (a) Changing from no load to full load at nominal output of 1 Volt (b) Changing from Full load to no load at nominal output of 1 Volt (c) Changing from no load to full load at nominal output of 0.38 Volt (d) Changing from full load to no load at nominal output of 0.38 Volt.

4.2.5 Layout

Figure 4.11 shows the layout of the final design shown in Figure 4.4. The dimensions of the layout are $275\mu m * 265\mu m$ and most of this area is composed of the compensation capacitors, which are $100pF$ in size. The capacitor layout is a combination of MOM cap and NMOS cap stacked together to save area. However, the area is still dominated by the capacitance which occupies 70% of the total area. The differential stage of the error amplifiers is laid out with a complete consideration for matching to avoid DC offsets. Figure 4.12 shows the differential stage of error amplifier layout.

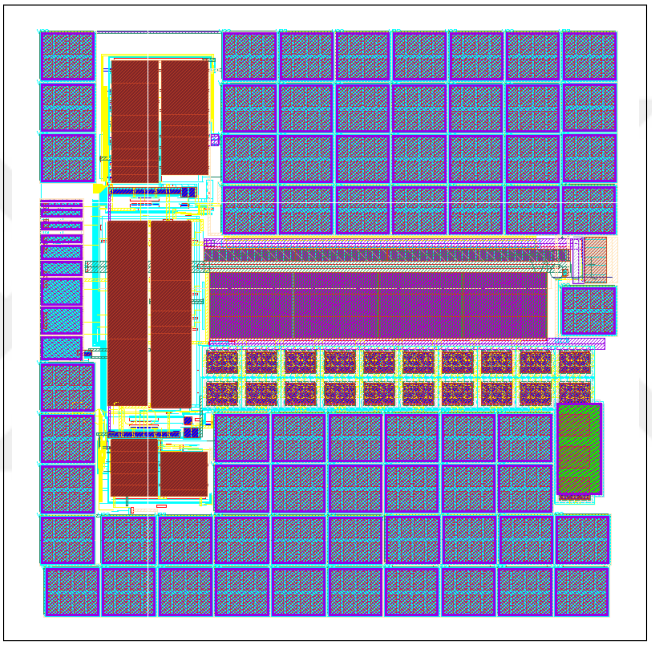

FIGURE 4.11: Linear regulator layout

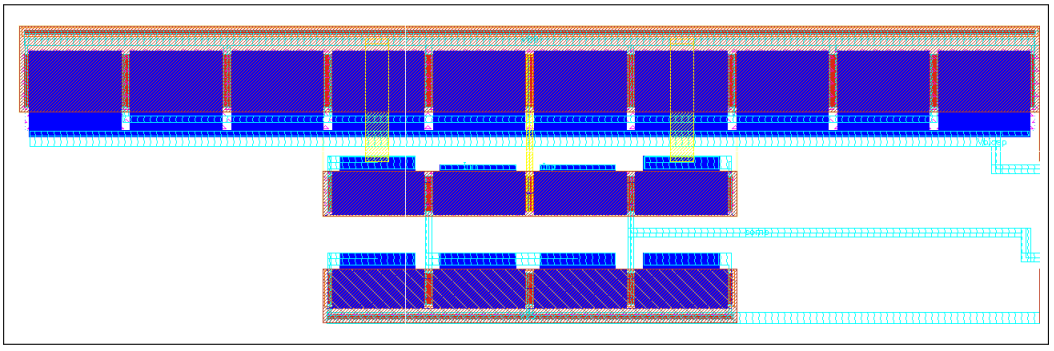

FIGURE 4.12: Differential stage of the error amplifier layout

Chapter 5

Conclusion

This dissertation presented the circuit design, layout, and simulated performance for a linear regulator for a parallel hybrid-linear-switching regulator system. The design consumes only $7\mu A$ quiescent current and can supply or drain up to $10mA$ current to and from the load. The circuit is designed to be normally inactive where the switching regulator supplies the load solely with its high power efficiency. The linear regulator gets activated only in sudden transient changes in the output voltage and limits the overshoot and undershoot to less than $100mV$. The circuit is designed to transfer an input voltage of $1.2V$ to 32 different output voltages ranging from $380mV$ to $1V$ with a step of $20mV$. The total circuit area is $72.875 * 10^{-3}mm^2$ in a $65nm$ CMOS technology.

The system in this work shows a novel way to achieve a better transient response than the switching regulator, which increases the frequency of the control circuit for a fast response at the expense of power efficiency. The linear regulator presented can accomplish the fast response and it is flexible for different design specifications of load current, capacitor, and output voltage.

Future work: In this dissertation, the power efficiency of the system during transient condition has not been discussed. Future work would include decreasing the output capacitor of the system in order to decrease the power wasted during switching on and off the power management unit. Consequently, the non-dominant pole moves to a higher frequency, and a smaller compensation capacitor can be used, which saves the large area of the design and results in a larger bandwidth of the loop that enhances the transient response.

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