Ultra Low Power, Low Noise, and Fully Integrated Receiver for Short Range Wireless Communications

A thesis submitted to the
Graduate School of Natural and Applied Sciences

by

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in partial fulfillment for the
degree of Master of Science

in

Electronics and Computer Engineering

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Electronics and Computer Engineering.

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Hasan El Gibaly

Abstract

The use of electronic circuitry has increased in the recent years in many aspect of life especially in medical applications. This is due to their precise and fast results in analyzing fatal diseases such as cardiovascular diseases, which need a real time observation. The need for a real time observation raises the challenge to find a solution, which should be power efficient, high sensitive, low noise, and small enough to be attached to or injected into user body. The solution simply contains two main devices. First, the sensors network which collects data and information from the user body. The second device is the transceiver, which sends this data to an external unit for analysis and diagnoses. This work cycle repeats itself millions of times per second, which causes a high power consumption. Therefore, a power optimized system is needed to sustain a long lasting operation.

This work introduces an ultra low power, low noise, and fully integrated receiver designated for short range communication systems. The system uses MOSFET weak inversion region of operation in order to decrease the supply voltage and hence, the total power consumption. In addition, the system uses an on-chip matching network for area optimization. This system consists of three main blocks: Radio frequency low noise amplifier (RFLNA), mixer, and baseband amplifier. This system manages to achieve a gain of 45.85 dB while consuming 1023 μA from 0.7 supply voltage, a single side band noise figure (SSBNF) of 8.4 dB single side band noise figure (SSBNF), and a third order interception point (IIP_3) of -37.7 dB_m. The system is designed using UMC 65 nm CMOS technology.

Keywords: RF Receiver, Ultra low power, Low noise, 2.5 GHz ISM band, Fully integrated

Kısa Menzilli Kablosuz İletişim için Ultra Düşük Güç, Düşük Gürültü ve Tam Entegre Alıcı

Hasan El Gibaly

Öz

Son yıllarda yaşamın bir çok alanında, özellikle tıbbi uygulamalarda artan elektronik devre kullanımı, araştırmacılar ve devre tasarımcılar için yeni zorluk oluşturmaktadır. Gerçek zamanlı gözlem gerektiren kardiyovasküler gibi ölümcül hastalıkların analiz ve teşhis edilme sürecinin hızlı ve kesin olması önemlidir. Buda küçük bir batarya ile uzun süre dayanabilen yada çevresinden enerji üretebilen yüksek duyarlıklı, düşük gürültülü ve kullanıcının vücuduna tutturulabilecek yada enjekte edilebilecek çözümler bulmayı zorlaştırmaktadır. Bu amaçla geliştirdiğim sistem genel anlamda üç ana cihazdan oluşmaktadır. İlki veri ve bilgi toplamaktan sorumlu sensör ağı, ikincisi, toplanan datayı ana birime gönderen alıcı , üçüncüsü ise toplanan verinin analiz ve teşhis işleminin yapıldığı harici ana birim. Bu çalışma döngüsü saniyede milyonlarca defa kendini tekrarladığı için çok fazla güç tüketmektedir. Bu sebeple uzun ömürlü bir sistem üretmek için güç tüketimi optimize sistemi gerekmektedir.

Bu çalışma kısa menzilli iletişim sistemleri için tasarlanmış Ultra Düşük Güç, Düşük Gürültü ve Tam Entegre Alıcı sistemini sunmaktadır. Sistemin besleme voltajını düşürebilmek için zayıf inversiyon bölgesinde çalışan MOSFET'ler kullanılmıştır. Bu sayede güç tüketimi azaltılmış ve çip üzerinde alan optimizasyonu sağlanmıştır. Sistem üç ana bloktan oluşmaktadır; RF LNA, Karıştırıcı ve taban bant yükselteç. Ayrıca sistem, 0.7 V besleme ve 1023 uA akım tüketimi ile 45.85 dB güç kazancı, 8.4 dB gürültü figürü (SSBNF) ve -37.7 dB üçüncü dereceden eksen kesme noktası ,IIP3 değerlerine sahiptir. Son olarak sistem UMC 65nm CMOS teknolojisi kullanılarak tasarlanmıştır.

Anahtar Sözcükler: RF Alıcı, Ultra Düşük Güç, Düşük Gürültü, 2.5 GHz ISM bant, Tam Entegre

To Allah, the creator.

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To Marwan and Gihad, who gave their help when I needed it the most.

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to whom it may concern, Thanks.

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Abbreviations

AC	**A**lternating **C**urrent
ADC	**A**nalog to **D**igital **C**onverter
AGC	**A**utomatic **G**ain **C**ontrol
BAN	**B**ody **A**rea **N**etwork
BB	**B**aseband
BER	**B**it **E**rror **R**ate
BJT	**B**ipolar **J**unction **T**ransistor
BLE	**B**luetooth **L**ow **E**nergy
BPSK	**B**inary **P**hase **S**hift **K**eying
BLE	**B**luetooth **L**ow **E**nergy
BT	**B**luetooth
BW	**B**andwidth
CG	**C**ommon **G**ate
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CS	**C**ommon **S**ource
DAC	**D**igital to **A**nalog **C**onverter
DC	**D**irect **C**urrent
DR	**D**ynamic **R**ange
DSSS	**D**irect **S**equence **S**pread **S**pectrum
ESD	**E**lectro **S**tatic **D**ischarge
F	**N**oise **F**actor
FOM	**F**igure of **M**erit
GFSK	**G**aussian **F**requency **S**hift **K**eying
IC	**I**ntegrated **C**ircuit
ICP$_{1dB}$	**I**nput referred 1dB **C**ompression **P**oint

IF	**I**ntermediate **F**requency
IIP$_2$	**I**nput referred Second Order **I**ntercept **P**oint
IIP$_3$	**I**nput referred Third Order **I**ntercept **P**oint
IL	**I**nsertion **L**oss
IM	**I**ntermodulation
IM$_2$	Second order **I**ntermodulation
IRR	**I**mage **R**ejection **R**atio
ISM	**I**ndustrial **S**cientific **M**edical
LNA	**L**ow **N**oise **A**mplifier
LO	**L**ocal **O**scillator
MOS	**M**etal **O**xide **S**emiconductor
NF	**N**oise **F**igure
NMOS	**N**-channel **M**etal **O**xide **S**emiconductor
OOK	**O**n **O**ff **K**eying
OQPSK	**O**ffset **Q**uadrature **P**hase **S**hift **K**eying
PA	**P**ower **A**mplifier
PCB	**P**rinted **C**ircuit **B**oard
PMOS	**P**-channel **M**etal **O**xide **S**emiconductor
PSD	**P**ower **S**pectral **D**ensity
Q	**Q**uality factor
RF	**R**adio **F**requency
RX	**R**eceiver
SNR	**S**ignal to **N**oise **R**atio
TX	**T**ransmitter
VCO	**V**oltage **C**ontrolled **O**scillator
VDD	**S**upply **V**oltage
WSN	**W**ireless **S**ensor **N**etwork
WBAN	**W**ireless **B**ody **A**rea **N**etwork
XO	**C**rystal **O**scillator

Chapter 1

Motivation

1.1 Thesis Motivation

Automated remote health monitoring has become increasingly critical in preventing chronic diseases, which affects the growing numbers of individuals. For example, Cardiovascular diseases (CVD) have become number one cause of death globally. According to world health organization media center (WHOMC), "an estimated 17.5 million people have died from CVDs in 2012, representing 31% of all global deaths" [1]. This necessitates the continuous monitoring of heart and blood vessels to reduce the number of the cases. Wireless body area networks (WBANs) provide suitable solutions, with specifications oriented to monitor patients remotely and reduce health care costs. The system consists of a sensors network, which is put on or close to the patient's body or injected underneath the skin. This allows a real time monitoring of a patient's condition regardless of his location. Usually, the main constraints for such systems are a small area for more compact solutions and a very low power consumption in order to maximize battery life. Most of the recent publications about short range radios (WSN and WBAN) offers optimizations for low power only. None of these works tried to optimize both the area and power together. Some solutions require an off-chip matching network/balun for power amplifier (PA) and/or the low noise amplifier (LNA) [2], which increases the size of the solution. The proposed work presents an ultra low power, low noise, and fully integrated receiver that works in 2.5 GHz ISM band.

1.2 Thesis Objective

The objective of this thesis is to develop an RF receiver design with new proposed techniques to reduce the power consumption and the area of the chip, while sustaining an acceptable performance. In order to fulfill this task, a comparative study of the receiver types and radio standards is presented. In addition, a detailed analysis of the effective parameters on receiver performance is discussed. After these detailed studies, the proposed design is presented. The proposed design uses MOSFET weak inversion region of operation in order to decrease the total power consumption and also utilizes an on-chip matching network for area optimization. The proposed system achieves a gain of 45.85 dB while consuming 1023 μA from 0.7 supply voltage, a single side band noise figure (SSBNF) of 8.4 dB, and a third order interception point (IIP_3) of -37.7 dB_m. The system is designed using UMC 65 nm CMOS technology. The schematics, simulations and physical verification (layout) are done using Cadence.

1.3 Thesis Organization

This thesis is organized as follow; Chapter 2 reviews low power radios standards and receiver architectures. In addition, it reviews some of the receiver design fundamentals such as noise, matching and linearity. Chapter 3 presents a comparison between different types of basic blocks in receiver design, e.g. LNAs and mixers. Chapter 4 discusses the design procedures for the receiver. Chapter 5 concludes this work and summarizes the results and the proposed enhancements for future work.

Chapter 2

Introduction

2.1 Low Power Radios

Recently, the research direction changed from providing radio communication with high data rate to connectivity with portable devices and sensors [3]. In this approach, the challenge is to provide the basic connectivity with the minimum power consumption. Wireless sensor networks (WSNs) are examples of ultra low power radio communication systems. WSNs consist of small sensors combined with a radio transceiver. Those sensors are used for monitoring and reporting data back to a central controller. Each node should be small, cheap and long lasting. With minimum power consumption, the energy needed can be harvested from heat, motion, etc. of the surrounding environment

Similar to WSN, WBANs consist of wearable or implantable devices. WBANs are used for health monitoring and early detection of medical conditions. There are various forms of WBANs, such as sports sensors connected to mobile phones or sports watches, which are used to monitor parameters like heart rate and activity. The full potential of low power radios will materialize as the technology matures.

2.1.1 Low Power Radios Standards

2.1.1.1 Bluetooth

Created by Ericsson in the late nineties, Bluetooth (BT) is a wireless standard intended for providing a short range connection to devices such as computers, phones, etc. Bluetooth operates at 2.4 GHz in industrial scientific medical (ISM) band, with data rate of 1 MBit/s in a 1 MHz channel and using gaussian frequency shift keying (GFSK) modulation. With the introduction of BT v4.0, support for a new low power communication protocol has been added, called Bluetooth low energy (BLE). BLE has a data rate of 1 Mbit/s with an average throughput of 270 Kbit/s and uses GFSK modulation [4].

2.1.1.2 ZigBee

ZigBee was devised in 2003 based on 802.15.4 standard. It operates at different frequency bands like 868 MHz, 915 MHz and 2.4 GHz. The data rate varies from 20 Kbit/s in 868 MHz band to 250 Kbit/s in 2.4 GHz band with binary phase shift keying (BPSK) modulation for lower data rates and offset quadrature phase shift keying (OQPSK) for highest data rate with signal spreading over 5 MHz wide channel to enhance resistance to interference using direct sequence spread spectrum (DSSS) [5].

2.1.1.3 WBANs

WBANs support a large number of real time health monitoring systems. For narrow band systems, the standard (IEEE 802.15.6) specifies the general requirements. The output power for standard compliance should be around -10 dB_m and data rate for an on off keying modulation (OOK) is 1 Mbit/s. On the receiver side, the required sensitivity level for 1 Mbit/s data rate is -90 dB_m [6].

2.2 Receiver Front End

This section briefly describes the function of a receiver front end and its components, including some requirements for ultra low power designs.

2.2.1 Architectures

2.2.1.1 Heterodyne

The superheterodyne receiver was invented in 1918 by E.H. Armstrong, which is considered the traditional way of building a receiver front end. Figure 2.1 provides a block diagram for superheterodyne receiver architecture. The input from the antenna is filtered by RF filter. After filtering the unwanted signals, the RF signal is amplified by a LNA to strengthen its power. Afterwards, a mixer, a.k.a. a multiplier, is used to bring down the signal to a lower intermediate frequency (f_{IF}). This operation is done by multiplying the RF signal with a reference signal from local oscillator (LO) such that $f_{LO} = f_{RF} \pm f_{IF}$. Products of the multiplication will appear at various frequencies, among them the difference frequency between the RF and LO frequency f_{IF}. Then IF filter is used to attenuate all signals except f_{IF} (image rejection filtering).

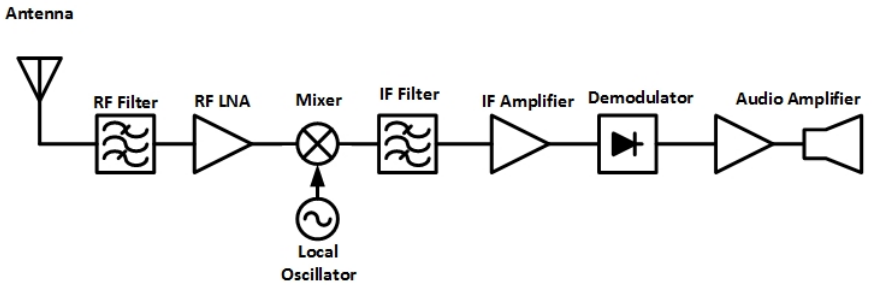


FIGURE 2.1: Superheterodyne receiver block diagram.

The main drawback of the superheterodyne architecture is the extensive use of on-chip components. On-chip components, especially inductors, have a low quality factor (Q), which rarely exceeds 20. This limits the filtering performance for the RF and IF filters. Furthermore, The IF filter will also be an issue since the inductors required to build a passive filter at low frequencies will be physically huge and it may not be possible to be integrated on-chip. However, the IF filter can be designed using an active filter e.g.(Sallen-Key topology). Yet, it is not the ideal solution.

2.2.1.2 Homodyne/Direct Conversion

The direct conversion architecture was build upon the concept of using a f_{LO} exactly the same as f_{RF}, which yields to $f_{IF} = 0$. For this fundamental concept it is also

called (zero IF receiver), Figure 2.2 provides a block diagram for homodyne receiver architecture. This solution is attractive for two reasons. Firstly, the image frequency does not pose any problems, since it coincides with wanted signal frequency. This also means that twice as much of the wanted signal power enters the mixer, improving the SNR by 3 dB and effectively reducing the mixer noise figure. Secondly, the output signal is now at baseband, which means that the circuits after the mixer are operating at very low frequencies and can be implemented in a power efficient manner. In addition, the IF filter is now a low pass filter and it is easier to be implemented on-chip. However, since both upper and lower sidebands of RF signal are converted to the same output frequencies, additional measures are needed to keep information apart. This is done by using a quadrature mixer. Quadrature mixer is basically two separated mixers operating with LO signals 90° apart. This effectively treats the RF signal as two separate amplitude modulated carriers, in other words, sine and cosine, which according to Fourier theory are orthogonal to each other.

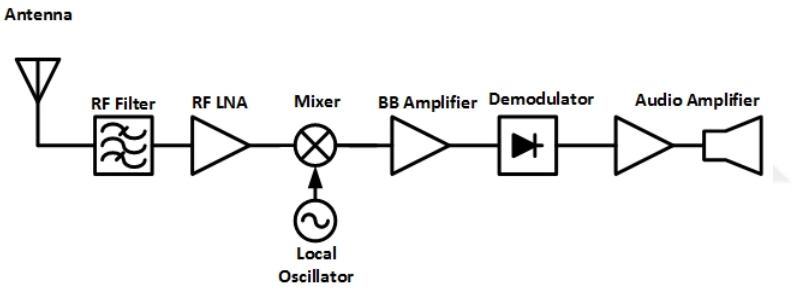


FIGURE 2.2: Homodyne receiver block diagram.

However, there are some issues with the direct conversion architecture. Noise tends to increase at very low frequencies. When a current passes through an electrical component, like transistor, it will emit electrical noise. In low frequencies, the dominant noise is known as flicker noise. A property of this noise is that its spectral content is inversely proportional to the frequency and it is often known as $1/f$ noise (more detailed analysis for noise is given in the following section). Since the receiver output signals appear at baseband, they are sensitive to low frequency noise and thus flicker noise should be minimized. Another issue is that the LO frequency is same as RF signal frequency and if they are not perfectly matched, LO energy will leak into signal path. Apart from leading to unwanted emission through the antenna, some of the leaked energy will reflect back into the mixer and self mixed with LO, creating a DC offset at the mixer output.

2.2.1.3 Low IF Receiver

The basic idea behind low IF receiver is to get the benefits of direct conversion architecture while eliminating the noise problem. This is done by using LO frequency with a small frequency difference from RF signal frequency. Thus, it is the same as the superhetrodyne receiver with LO frequency near to RF signal (basically hundreds KHz up to 1 MHz). At the baseband side, the desired signal will not be at low frequencies where most of flicker noise is. This makes it easier to deal with.

2.2.2 Basic Definitions

In this section, a general overview on some key parameters in receiver design is presented.

2.2.2.1 Noise

Noise is a natural phenomenon. In communication systems, noise is defined as the fault or the unwanted random disturbance of a useful signal. The quality of the signal is measured by signal to noise ratio (SNR), "which is defined as the ratio of signal power to the noise power, expressed in decibels." [7]

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{2.1}$$

There are three main types of noise. Thermal noise, shot noise, and flicker noise. Thermal noise or Johnson noise (as it was first observed by J. B. Johnson) is inevitable and can not be avoided or terminated. Generally, it is generated by the motion of charge carriers (usually electrons), inside an electrical conductor, which happens regardless of any applied voltage. Shot noise is defined as the noise generated due to the discrete arrival time of electrons when they flow across a barrier. It is one of the major noise contributors in designs that use bipolar junction transistor (BJT). This thesis will not provide any analysis of shot noise as all of the blocks designed using complementary metal oxide semiconductor (CMOS) process. Flicker noise, also known as $1/f$ noise, is usually related to direct current. Flicker noise has pink noise power spectral density (PSD). This means that it dominates the circuit noise for low frequencies and is neglected in high frequencies as shown in Figure 2.3. The value which flicker noise becomes less than the

thermal noise is called flicker noise corner frequency. The following section presents noise analysis for the main components used in designs.

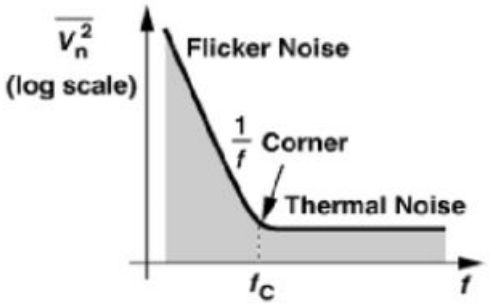


FIGURE 2.3: Flicker noise corner frequency [7].

2.2.2.1.1 Resistors

Thermal noise is the main type of noise that resistors generate. It can be modeled as a voltage source with a PSD of $v_n^2(f)$ in series with noiseless resistance as shown in Figure 2.4, where $v_n^2(f)$ is given by

$$v_n^2(f) = 4kTR \tag{2.2}$$

k is the Boltzmann's constant ($1.38 \times 10^{-32} J/K$), T is the temperature in Kelvins, and R is the resistance value. The noise can also be modeled as a current source, $i_n^2(f)$, in shunt with a noiseless resistor. The current source has a PSD value of

$$i_n^2(f) = \frac{4kT}{R} \tag{2.3}$$

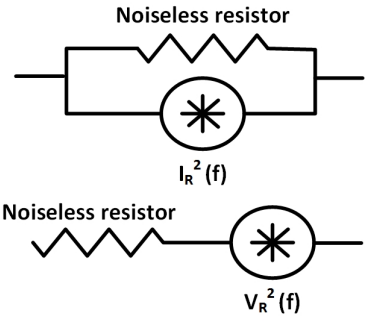


FIGURE 2.4: Noise model for resistance.

2.2.2.1.2 MOSFETs

Unlike resistors, flicker noise is the most effective noise source for MOSFETs. Flicker noise can be modeled either as a voltage source in series with the gate or as a current source between source and drain as follows

$$v_g^2(f) = \frac{K}{WLC_{ox}f} \tag{2.4}$$

$$i_g^2(f) = \frac{Kg_m^2}{WLC_{ox}f} \tag{2.5}$$

where K is a device specific constant. The variables W, L, g_m, and C_{ox} represent the transistor's width, length, transconductance, and gate capacitance per unit area, respectively[8]. The thermal noise for MOSFETs operating in inversion region can be modeled as a current source tied between drain and source terminals as shown in Figure 2.5 with a PSD value equals

$$i_d^2(f) = 4KT\gamma gm \tag{2.6}$$

where γ is the excess noise coefficient. Its value is 2/3 for long-channel transistors and can go up to 2 in short-channel transistors. As mentioned earlier, the dominant noise type in MOSFETs depend on frequency of operation. Therefore, in RF blocks thermal noise dominates, while in baseband flicker noise is the dominant source. Figure 2.5. shows a simplified model for the MOSFET flicker and thermal noise sources.

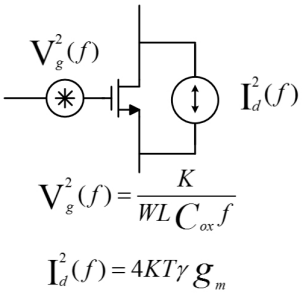


FIGURE 2.5: Noise model for MOSFET.

2.2.2.1.3 Capacitors and Inductors

Ideally, capacitors and inductors do not produce random noise. However, due to the finite Q, the parasitic resistances produce thermal noise. On-chip and off-chip inductors are used for matching, degeneration, and loading purposes. The off-chip inductors provide a better performance in comparison with on-chip inductors, because of the limited Q

of on-chip inductors. However, in order to decrease the overall cost, on-chip inductors are used. Noise from capacitors and inductors with limited Q can be modeled with the effective value of the parasitic resistance at the frequency of interest and the noise due to that parasitic resistance as shown in Figure 2.6. Since the value of the parasitic resistance is frequency dependent, therefore, the noise generated by it is also frequency dependent.

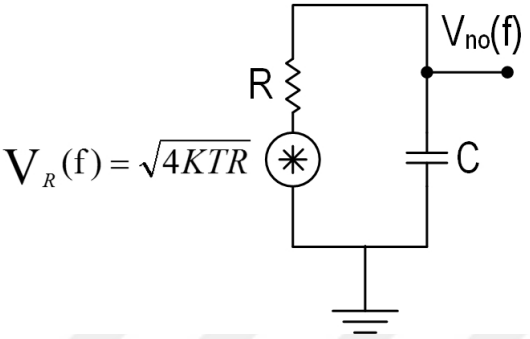


FIGURE 2.6: Noise model for capacitor.

2.2.2.1.4 Noise Factor (F) and Noise Figure (NF)

The noise figure (NF) is a measure of the amount of noise added to the signal by the circuit components in decibels. The noise factor (F) is the value of NF in linear scale, and defined as the ratio between the SNR_{in} and SNR_{out} [7]. For a cascade system of N stages as shown in Figure 2.7 , the total noise factor can be calculated by using the noise factor and gain of each stage. The noise factor can be expressed by the Friis's equation

$$F_{sys} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_N - 1}{G_1 G_2 ... G_{N-1}} \tag{2.7}$$

where $F_{1...N}$ is the noise factor of each stage and $G_{1...N}$ is the gain of each stage.

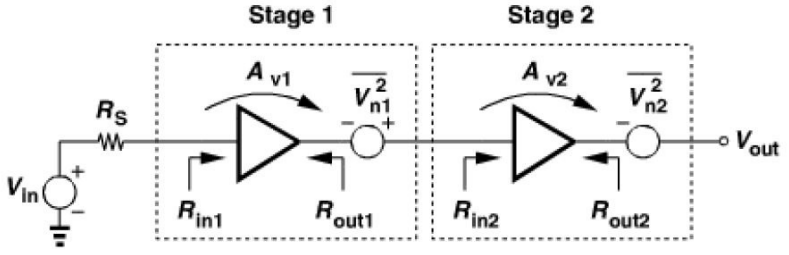


FIGURE 2.7: Noise in a cascade of stages [7].

2.2.2.1.5 Gain

Gain measures the ability of a circuit to increase the amplitude of a signal from its input port (or ports) to its output port (or ports). It is measured by the ratio between input and output power, voltage, or current. It is usually written in decibels. In this work the voltage gain definition is used, which can be written as

$$Gain = 20log\left(\frac{V_{out}}{V_{in}}\right) \tag{2.8}$$

2.2.2.1.6 Matching

Matching the impedance of the input port of the RF LNA to the impedance of the antenna is required to achieve maximum power transfer from the antenna to the RF LNA. For example, for common source RF LNA, the input impedance greatly depends on the gate to source capacitance C_{gs}. In order to achieve a purely resistive impedance, extra components need to be added. Degenerating the source with an inductor (L) can achieve this purpose. The input impedance of inductively degenerated common source amplifier is given by

$$Z_{in} = sL + \frac{1}{sC_{gs}} + \frac{g_m L}{C_{gs}} \tag{2.9}$$

The last term of this equation is purely real and can be matched to 50Ω antenna. This part is discussed in details in the following chapter.

2.2.2.2 Linearity

Nonlinearity of a system is mainly because of the distortion in active components such as transistors. The most commonly used measurements that represent the linearity performance are" the 1 dB compression point (P_{1dB}), the second order intercept point (IP2) and the third order intercept point (IP3)." [7]

2.2.2.2.1 1 dB Compression Point

Assuming a given input signal x which can be written as

$$x = Acos(w_T t) \tag{2.10}$$

is fed into a nonlinear system, which can be approximated as

$$y = a_1 x + a_2 x^2 + a_3 x^3 + ... \tag{2.11}$$

Substituting Eq. 2.10 into Eq. 2.11 gives

$$y = \frac{a_2 A^2}{2} + (a_1 A + \frac{3a_3 A^3}{4})cos(w_T t) + \frac{a_2 A^2}{2} cos(2w_T t) + \frac{a_3 A^3}{4} cos(3w_T t) + ... \tag{2.12}$$

From Eq. 2.12 it is observed that for a sinusoidal input applied to a nonlinear system, the output contains frequency components that are multiples of the input frequency. For most circuits, a_3 is less than zero. Therefore, the fundamental gain $(a_1 A + \frac{3a_3 A^3}{4})$ decreases as the input amplitude, A, increases, which means that the output fails to respond linearly with the input. Figure 2.8 shows that the 1 dB compression point is the point at which the small signal gain is 1 dB below its nominal value due to the input signal level. It can be calculated by equating the fundamental gain with first harmonic gain minus one (both in decibels) as follows [7]

$$20log\left|a_1 + \frac{3a_3 A_{1dB}^2}{4}\right| = 20log|a_1| - 1 \tag{2.13}$$

$$IP_{1dB} = \sqrt{0.145\left|\frac{a_1}{a_3}\right|} \tag{2.14}$$

2.2.2.2.2 Third Order Interception Point

Recalling the analysis done in the previous section, but instead of using single tone as an input signal, there are two signals with very close frequencies that are applied to a nonlinear system as shown in Figure 2.9. Numerous unwanted signals appear at the output terminal of the system due to the harmonics and intermodulation between the two signals. In addition, some of those unwanted frequencies may fall on the frequency band of the wanted signal which affects system performance.

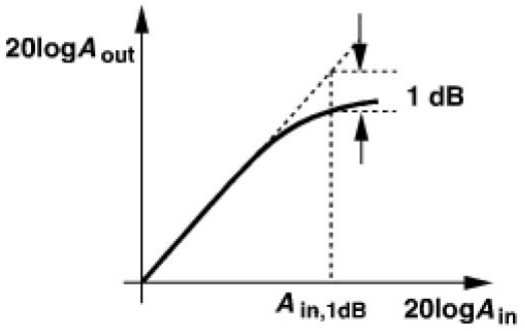


FIGURE 2.8: Definition of 1 dB compression point [7].

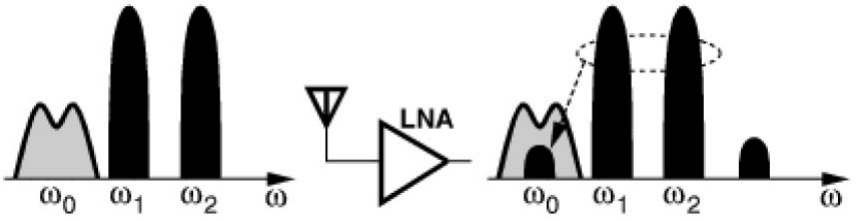


FIGURE 2.9: Damage due to IIP_3 [7].

Defining a nonlinear system by Eq. 2.11 and assuming that each of the two input signals is given by

$$x = A[cos(w_1 t) + cos(w_2 t)] \tag{2.15}$$

the output signals are

$$y = a_1 A[cos(w_1 t) + cos(w_2 t)] + a_2 (A[cos(w_1 t) + cos(w_2 t)])^2 + a_3 (A[cos(w_1 t) + cos(w_2 t)])^3 + ... \tag{2.16}$$

Decomposing and summing similar factors produce

$$y(w_1) = (a_1 A + \frac{9 a_3 A^3}{4}) cos(w_1 t) \tag{2.17}$$

$$y(w_2) = (a_1 A + \frac{9 a_3 A^3}{4}) cos(w_2 t) \tag{2.18}$$

$$y(2w_1 \pm w_2) = (a_1 A + \frac{9 a_3 A^3}{4}) cos(2w_1 \pm w_2) t \tag{2.19}$$

$$y(2w_2 \pm w_1) = (a_1 A + \frac{9 a_3 A^3}{4}) cos(2w_2 \pm w_1) t \tag{2.20}$$

The problem occurs if the wanted input signal of frequency w_0 follows the definition of

$$w_0 = 2w_1 \pm w_2 \tag{2.21}$$

Therefore, the intermodulation result is at the same frequency of the wanted signal, which leads to the damage and corruption of the input signal and the overall quality. In order to characterize nonlinearity performance of the system, two sinusoidal signals with the same amplitude, are applied to the input. The power level of the applied tones to the system where their third order intermodulation product power becomes equal to the power of tones at the output of the system is IIP_3 of the system. Since IIP_3 is a weak nonlinear measurement of the system, it is calculated by extrapolation of data for lower distortion levels as shown in Figure 2.10. To determine the IIP_3, the fundamental and IM amplitudes are equalized as follows

$$\left| a_1 A_{IIP_3} \right| = \left| \frac{4}{3} a_3 A_{IIP_3}^3 \right| \tag{2.22}$$

resulting in

$$A_{IIP_3} = \sqrt{\frac{4}{3} \left| \frac{a_1}{a_3} \right|} \tag{2.23}$$

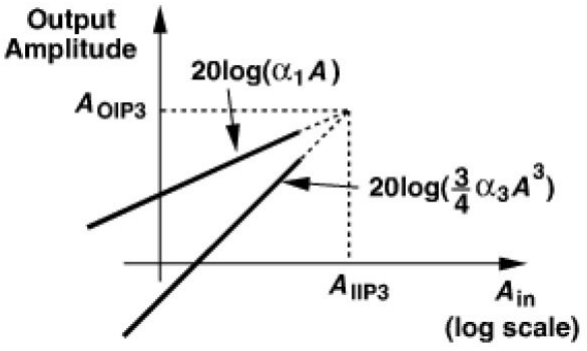


FIGURE 2.10: Definition of IP_3 [7].

2.2.2.2.3 Second Order Interception Point

Similar to IIP_3, IIP_2 is also defined according to a two tones test applied to a nonlinear system. By extracting Eq. 2.16, a second order intermodulation component (IM_2) arises and causes linearity problems.

Eq. 2.24 shows that the amplitude of the IM_2 component rises with double the value of the slope of the fundamental component on a log scale. IIP_2 is the power level of the applied tones to the system where their second order intermodulation product power becomes equal to the power of tones at the output of the system as shown in Figure 2.11, which concludes the relation between the wanted output signal power and the P_{1dB}, IIP_3 and IIP_2 points.

$$y(w_1 \pm w_2) = a_2 A^2 cos(w_1 \pm w_2) \tag{2.24}$$

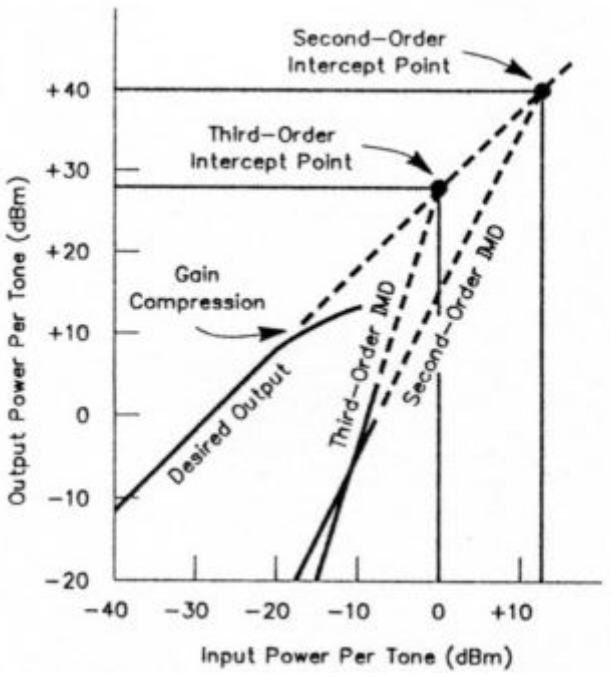


FIGURE 2.11: Relation between wanted output signal power and P_{1dB}, IIP_3 and IIP_2 points [9].

2.2.2.3 MOSFET in Weak Inversion

Subthreshold (weak inversion) biasing has become a standard technique for low power circuit design and is widely used in CMOS analog circuits. This approach is the main focus of this thesis. In this section, a quick detailed analysis for MOSFETs in weak inversion is presented.

2.2.2.3.1 Drain Current In Weak Inversion

In weak inversion region, n-MOSFET is similar to an npn BJT [10], where source acts as emitter, substrate as base and drain as collector. Therefore, the concentration of electrons in the p-type substrate at the source $n_p(0)$ is given by

$$n_p(0) = n_{po} exp\left(\frac{\psi_s}{V_T}\right) \tag{2.25}$$

where n_{po} is the equilibrium concentration of electrons in substrate, V_T is the thermal voltage, and ψ_s is the surface potential. Using the same approach to calculate the concentration of electrons in substrate at the drain $n_p(L)$ gives

$$n_p(L) = n_{po} exp\left(\frac{\psi_s - V_{DS}}{V_T}\right) \tag{2.26}$$

Recalling the drain current due to the diffusion of electrons in substrate from [10], it is given by

$$I_D = qAD_n \frac{n_p(L) - n_p(0)}{L} \tag{2.27}$$

where q is the electron charge, D_n is the diffusion constant for electrons, and A is the area through which I_D flows and it is defined as the product of transistor width (W) with its thickness (X). Substituting and arranging the equations gives

$$I_D = \frac{W}{L} qXD_n n_{po} exp\left(\frac{\psi_s}{V_T}\right)\left[1 - exp(-\frac{V_{DS}}{V_T})\right] \tag{2.28}$$

In weak inversion, changes in the surface potential $\Delta\psi_s$ are controlled by the changes in the gate to source voltage ΔV_{GS} through a capacitive voltage divider as follow

$$\frac{d\psi_s}{dV_{GS}} = \frac{C_{ox}}{C_{ox} + C_{dep}} = \frac{1}{n} \tag{2.29}$$

where C_{ox} is the oxide metal capacitance and C_{dep} is the depletion region capacitance. By integrating and finding the values for ψ_s with respect to V_{GS} and substituting in Eq. 2.28 gives

$$I_D = \frac{W}{L} I_t exp\left(\frac{V_{GS} - V_t}{nV_T}\right)\left[1 - exp(-\frac{V_{DS}}{V_T})\right] \tag{2.30}$$

where

$$I_t = qXD_n n_{po} exp\left(\frac{k_2}{V_T}\right) \tag{2.31}$$

and k_2 is the integration constant, with the assumption that $V_{GS} = V_t$, $\frac{W}{L} = 1$, and $V_{DS} \gg V_T$. I_t represents the drain current. Figure 2.12 shows the drain current versus the drain to source voltage V_{DS} with W = 200 nm, L = 200 nm, n = 1.5, and $I_t = 0.1$ μA. Note that while the short-channel effect (λ) is neglected in deriving the equation, it appears in Figure 2.12. In addition, the drain current saturates at $V_{DS} > 3V_T$. This is justified by observing that the last term in Eq. 2.30 approaches unity. Therefore, the minimum drain to source voltage V_{DS} required to force a current I_D in a MOSFET operates in weak inversion region is independent of the overdrive voltage, which is defined as $V_{ov} = V_{GS} - V_t$, where V_t is the threshold voltage. This opposes the case of MOSFET in strong inversion. Figure 2.12 and Eq. 2.30 show that even when $V_{GS} < V_t$, the drain current is not zero. For more clarification, Figure 2.13 indicates the relation between I_D and V_{GS}.

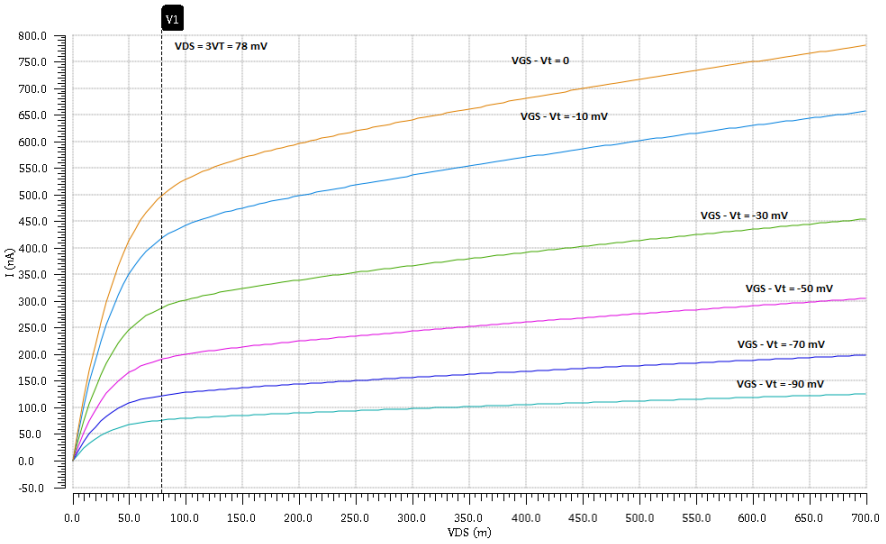


FIGURE 2.12: I_D versus V_{DS} for different values of V_{ov}

2.2.2.3.2 Transconductance in Weak Inversion

Transconductance or g_m for a MOSFET operates in weak inversion region can be calculated by recalling Eq. 2.29 and 2.30

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{W}{L}\frac{I_t}{nV_T} exp\left(\frac{V_{GS} - V_t}{nV_T}\right)\left[1 - exp(-\frac{V_{DS}}{V_T})\right] = \frac{I_D}{nV_T} \tag{2.32}$$

Eq. 2.32 shows that g_m of a MOSFET operates in weak inversion region differs from g_m of the BJT only by the factor n. Using Eq. 2.32, the ratio of MOSFET transconductance

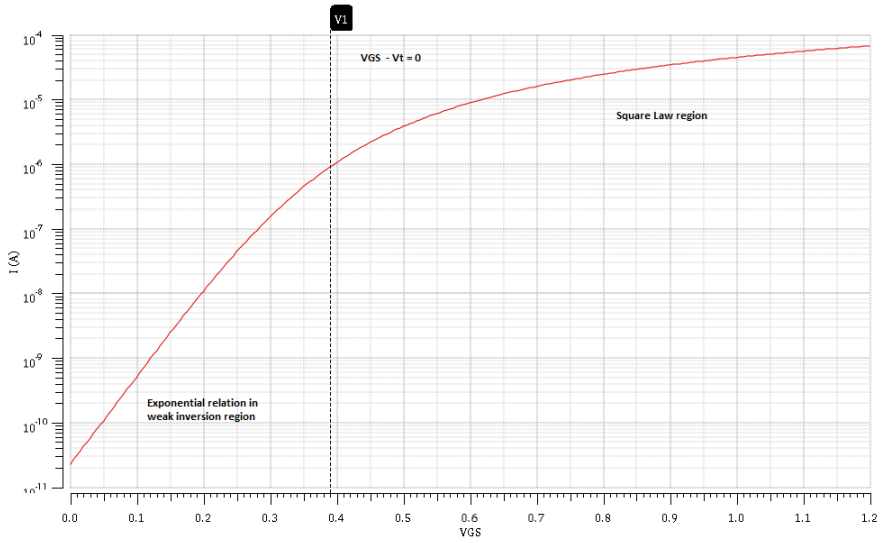


FIGURE 2.13: I_D on a log scale versus V_{GS}

to its drain current in weak inversion region is found to be

$$\frac{g_m}{I_D} = \frac{1}{nV_T} \tag{2.33}$$

Eq. 2.33 shows that the ratio of the transconductance to the drain current is independent of the overdrive voltage and approximately constant. On the contrary, this ratio for the MOSFET in saturation or strong inversion depends on V_{ov} as shown in the following equation. [10]

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad \text{and} \quad \frac{g_m}{I_D} = \frac{2}{V_{ov}} \tag{2.34}$$

In Figure 2.14, there is a region in between weak and strong inversion called moderate inversion, where both diffusion and drift currents are significant and can not be neglected. Comparing Eq. 2.32 and 2.34, it appears that g_m in weak inversion can not increase by changing the ratio W/L, in contrast with g_m in strong inversion. However, if the current density is constant, g_m will have a direct proportion with W/L as shown in Figure 2.15.

2.2.2.3.3 Transition Frequency in Weak Inversion

The transition frequency in weak inversion can be defined as [10]

$$f_t = \frac{1}{2\pi} w_t = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gb} + C_{gd}} \tag{2.35}$$

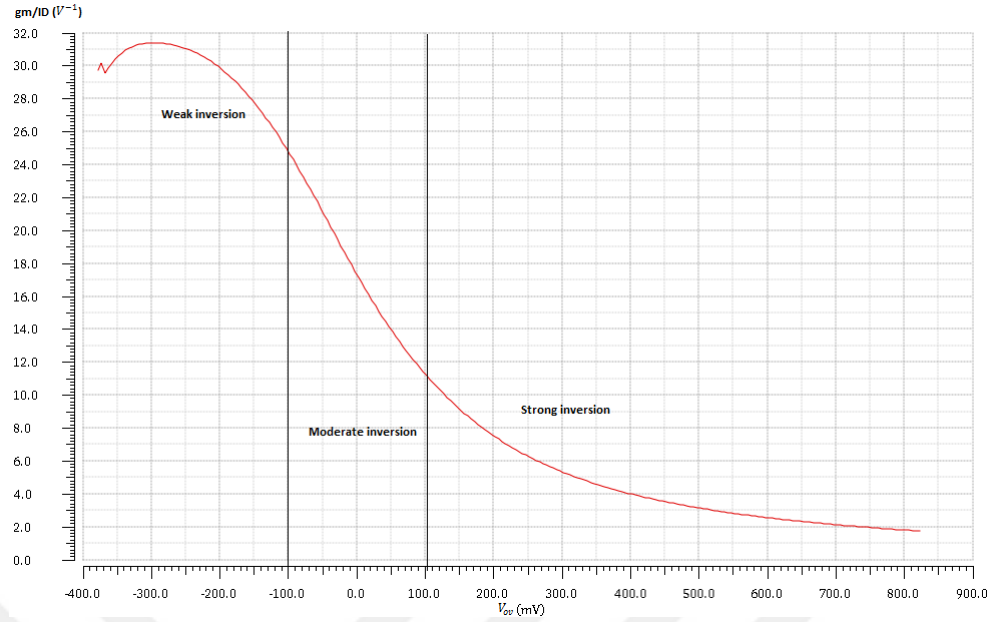


FIGURE 2.14: g_m/I_D versus V_{ov}

Eq. 2.35 describes the transition frequency by using small signal model of MOSFET in high frequency. In weak inversion, $C_{gs} \simeq C_{gd} \simeq 0$. This is because the inversion layer contains little charges. On the other hand, C_{gb} is the series combination of the capacitance of the metal to oxide layer and the depletion capacitors.

$$C_{gb} = WL\frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}} \tag{2.36}$$

Substituting from Eq. 2.32 and Eq. 2.36 in 2.35 gives

$$f_t = \frac{1}{2\pi}\frac{\frac{I_D}{V_T}\frac{C_{ox}}{C_{ox}+C_{dep}}}{WL\frac{C_{ox}C_{dep}}{C_{ox}+C_{dep}}} = \frac{1}{2\pi}\frac{I_D}{V_T}\frac{1}{WLC_{dep}} \tag{2.37}$$

2.2.2.3.4 Noise Analysis in Weak Inversion

Although it is already mentioned in previous section, MOSFET operates in weak inversion region does not follow the same definition for thermal noise. Therefore, additional analysis is given as follows. It is already known that thermal noise PSD for n-MOSFET is [11]

$$S_{iw} = \frac{-4KT\mu Q_I}{L^2} \tag{2.38}$$

where Q_I is the total inversion charges in the channel and μ is the effective mobility. Using Eq. 2.38 and the expression of the total inversion charge in terms of the channel charge densities at the ends of the channel from [11]. The PSD of the thermal noise S_{iw}

is given as [12]

$$S_{iw} = -4KT\mu\frac{W}{L}\frac{\frac{2}{3}(Q_{IS}^2 + Q_{IS}Q_{ID} + Q_{ID}^2) - nC_{ox}\phi_t(Q_{IS} + Q_{ID})}{Q_{IS} + Q_{ID} - 2nC_{ox}\phi_t} \tag{2.39}$$

where Q_{IS} and Q_{ID} are channel charge density at source and drain respectively. This definition holds for all MOSFET regions of operation and will be used to define thermal noise in weak inversion MOSFET. In weak inversion, $|Q_{IS(D)}| \ll nC_{ox}\phi_t$. Therefore, the previous equation can be written as

$$S_{iw} \simeq -4kT\mu\frac{W}{L}\frac{Q_{IS} + Q_{ID}}{2} = kT\frac{g_{ms} + g_{md}}{2} \tag{2.40}$$

For a MOSFET in weak inversion region $g_{ms} \gg g_{md}$. Therefore,

$$S_{iw} = 2kT\gamma g_{ms} \tag{2.41}$$

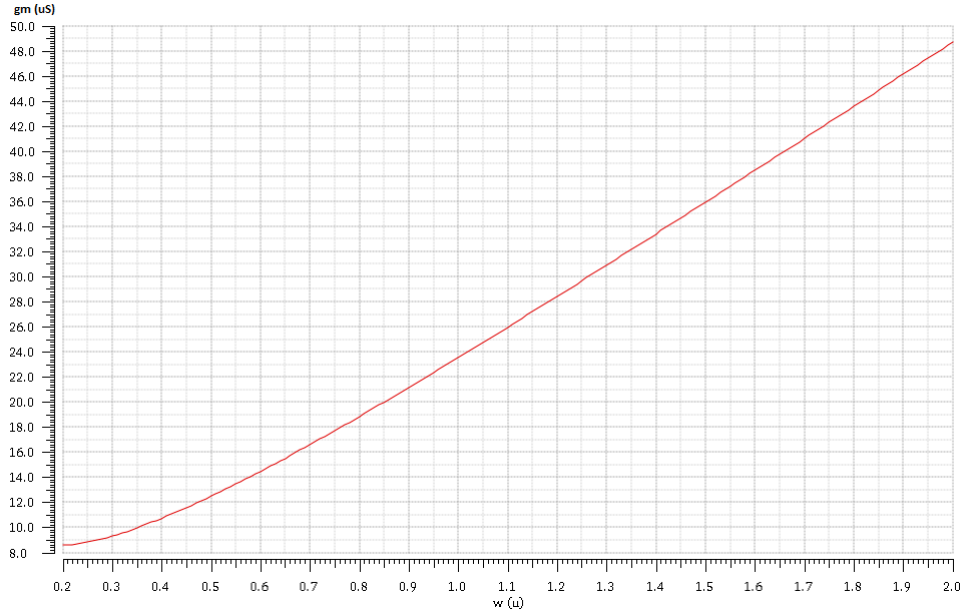


FIGURE 2.15: g_m versus W

Chapter 3

Introduction to Ultra Low Power Low Noise Receiver Design

This chapter briefly presents the main blocks for receiver design with a comparison between the most used topologies for each block.

3.1 LNA

In this section, a brief description of the main topologies of LNA designs are presented with a comparison between their performance according to the fundamental definitions illustrated earlier in Chapter 2.
There are two main topologies for RF LNA: Common gate (CG) and Common source (CS) LNAs.

CG LNA, shown in Figure 3.1, with proper sizing, the real part of its input impedance reaches 50Ω without any need for extra components. This reduces the total cost of the overall system. In addition, since it is not necessary to use any extra frequency dependent component such as inductors and capacitors for the impedance matching, the design becomes a wideband design and provides a very good power transfer from antenna to the LNA for a wide frequency range. However, the main drawback is its high noise figure compared to the common source topology. According to Figure 3.2, which assumes a CG LNA in strong inversion, $g_m = \frac{1}{R_S}$ and the gain equals $\frac{R_1}{R_S}$ [7]. Therefore, the total

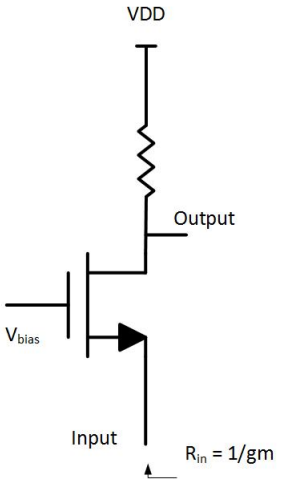


FIGURE 3.1: Common gate LNA.

PSD noise at the output node $\overline{V^2_{n,out}|_{M1}}$ equals to

$$\overline{V^2_{n,out}|_{M1}} = \frac{4kT\gamma}{g_m}(\frac{R_1}{R_S + \frac{1}{g_m}})^2 = kT\gamma\frac{R_1^2}{R_S} \tag{3.1}$$

while taking in consideration that the noise due to the output resistance R_1 is $4kTR_1$. To evaluate the noise factor, the output noise is divided by the gain multiplied by the source resistance noise R_S, which gives

$$NF = 1 + \gamma + \frac{R_s}{R_1}(1 + \frac{1}{g_m R_S})^2 = 1 + \gamma + 4\frac{R_s}{R_1} \tag{3.2}$$

From Eq. 3.2, the noise factor is ideally 2, which results into a NF of about 3 dB with $\gamma \simeq 1$ and $4\frac{R_s}{R1} \ll 1 + \gamma$. In conclusion, the CG LNA is better than CS LNA in many

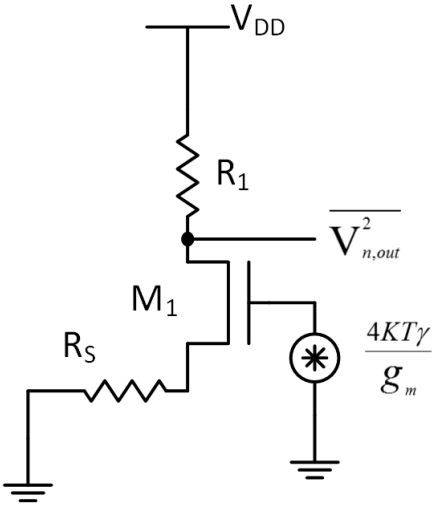


FIGURE 3.2: Common gate noise model.

aspects except noise. Therefore, for a system requiring a strict low noise figure, CS LNA is preferred.

Normally, in RF applications CS LNA source is connected to a small inductance to ground. This inductance is used to provide more stability and matching in RF region, while being zero impedance at DC which does not reduce the available headroom. Furthermore, for narrowband applications, an output LC tank circuit is used as a load, which produces a stability issue. To solve this issue, a cascode device is used. Therefore the commonly used topology for CS LNA in RF band is inductively degenerated cascode CS LNA as shown in Figure 3.3.

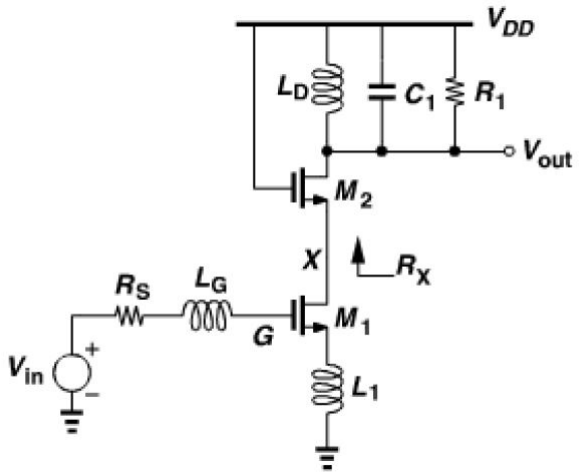


FIGURE 3.3: Inductively degenerated cascode CS LNA [7].

A detailed analysis for this topology starts as follows: Using Figure 3.4 to calculate input impedance of inductive degenerated CS LNA gives

$$Z_{in} = \frac{V_x}{I_x} = \frac{1}{C_{GS}S} + L_1 S + \frac{g_m L_1}{C_{GS}} \tag{3.3}$$

where the last part of Eq. 3.3 is real and can be adjusted to have a 50Ω resistance. In addition, $\frac{g_m}{C_{GS}} \simeq \omega_T = 2\pi f_T$. With this approximation, the real part of input impedance can be written as $L_1\omega_T$ which highlights a problem. For example, in 65 nm $f_T \simeq 160$ GHz, which leads to $L_1 \simeq 50$ pH [7]. This small value for the inductance can not be realized in real fabrication process. The solution is to decrease the f_T of the MOSFET by manually adding C_{GS}. This decreases f_T and makes L_1 value reasonable. The main

advantage of the degeneration inductance is that it works as a feedback resistance in the resonance frequency which increases stability, while being a short circuit in DC which does not reduce the available headroom. The additional inductance L_G shown in Figure 3.3 is to resonate with C_{GS}.

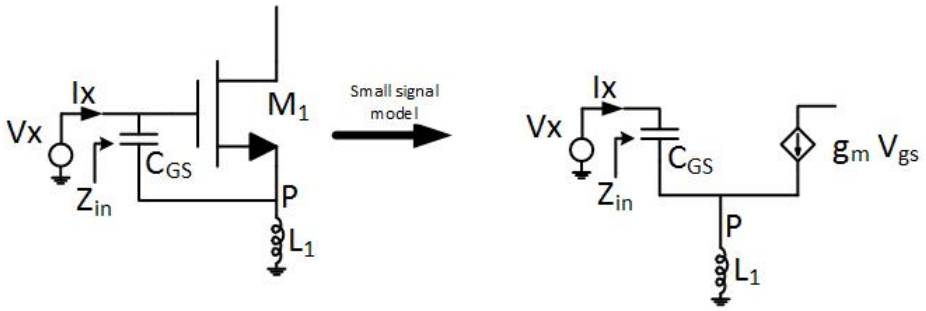


FIGURE 3.4: Input impedance CS LNA with a small signal model.

Using Figure 3.5, NF is calculated with the appearance of degeneration inductance. There are two paths for the current to go through. First, through the source and degeneration inductance and second, through the gate capacitance to the ground. The later creates a voltage drop a cross C_{GS} which creates a current in the voltage dependent current source that equals $g_m V_{GS}$.

$$V_{GS} = -(g_m V_{GS} + i_d) \times \frac{j\omega L_s}{j\omega L_s + \frac{1}{j\omega C_{GS}} + j\omega L_g + R_s} \times \frac{1}{j\omega C_{GS}} \tag{3.4}$$

where V_{GS} is gate to source voltage difference. At resonance, the denominator simplified to R_s which gives

$$V_{GS} = -(g_m V_{GS} + i_d) \times \frac{j\omega L_s}{R_s} \times \frac{1}{j\omega C_{GS}} V_{GS}(1 + \frac{g_m L_s}{C_{GS} R_s}) = -i_d \frac{L_s}{C_{GS} R_s} \tag{3.5}$$

However, $\omega_T \times L_s = R_s$, therefore

$$|g_m v_{GS}| = |\frac{i_d}{2}| \quad or \quad \overline{I^2_{n,out}|_{M1}} = \frac{i_d^2}{4} = kT\gamma g_m \tag{3.6}$$

Therefore, the total noise figure equals

$$NF = 1 + \frac{R_g}{R_s} + g_m R_s \gamma \frac{\omega_0}{\omega_T} \tag{3.7}$$

which is same as the NF for CS LNA with grounded source. [7].

Using output LC tank circuit as an output load is beneficial for many reasons. It gives a minimum voltage drop in DC which increases the available swing across output node. In addition, it provides a peak gain at a certain frequency in narrowband applications. However, this inductive load creates a problem, which is the negative resistance due to the feedback from gate to drain capacitance C_{GD}. Therefore, a cascode device is used as shown in Figure 3.3 to decrease this effect. However, additional analysis is needed to see the effect of the cascode on the noise figure.

Using Figure 3.6 with M_1 modeled as r_o, which is quite high. In high frequencies, most of the drain noise flows through C_{GS}. While in low frequencies, the noise flows into r_o creating a noise current equals in magnitude to the high frequency noise current, but in the opposite direction. Therefore, the noise circulates in the device. In other words, the cascode device does not produce noise at the output node.

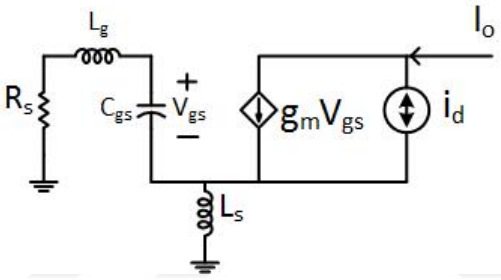


FIGURE 3.5: Circuit equivalent for NF calculation.

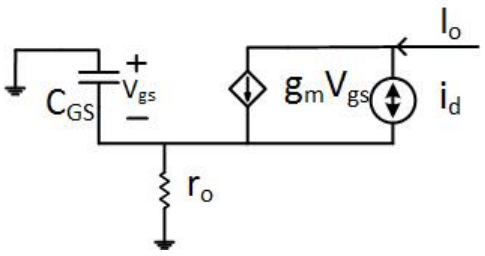


FIGURE 3.6: Circuit equivalent of the cascode device for NF calculation.

3.2 Mixer

In this section, a brief comparison between main topologies for mixer design is be presented in terms of their performance according to the fundamental definitions illustrated earlier in Chapter 2.

3.2.1 Mixer Noise Figure

Before going through the analysis of the mixer NF, the definition for NF should be redefined first. Assuming a noiseless mixer as shown in Figure 3.7, the noise in the signal band plus the noise in the image band both are down converted to intermediate band. Therefore, the output SNR is half the input SNR. For this reason, NF of a noiseless single side band (SSB) is 3 dB regardless of any noise sources.

Consider the same noiseless mixer but with only the noise in the signal band is down converted. In this case, the output SNR is the same as the input SNR, thus, NF is equal to zero. This is called a double sideband (DSB) noise figure as shown in Figure 3.8

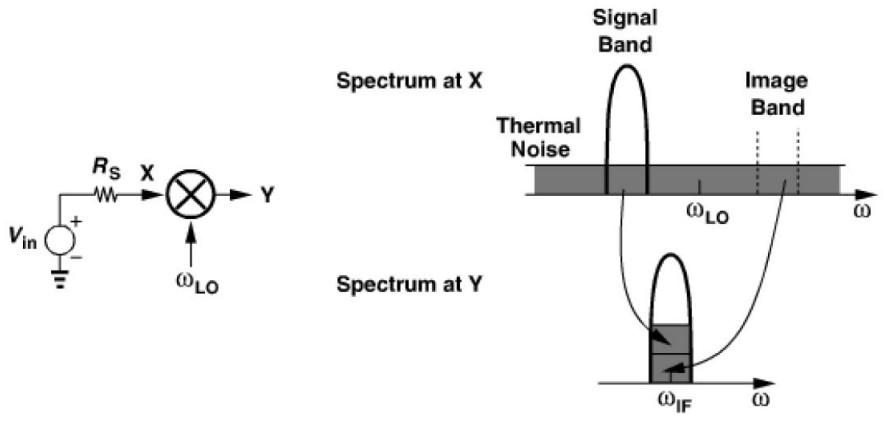


FIGURE 3.7: SSB NF [7].

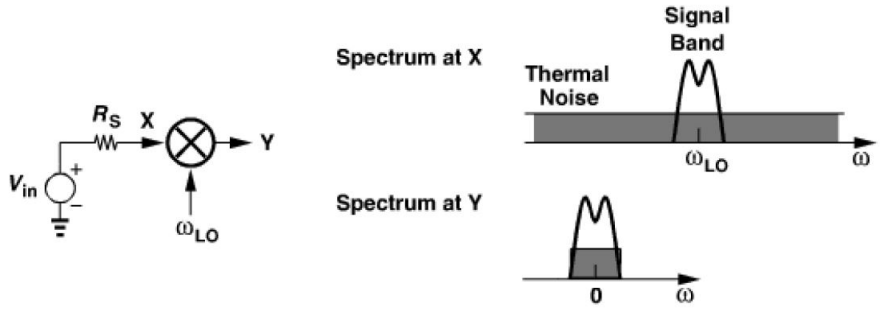


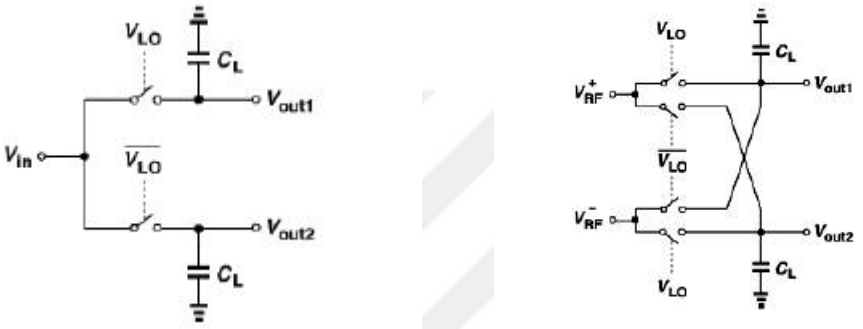
FIGURE 3.8: DSB NF [7].

3.2.2 Mixer Topology

There are two main topologies for mixer design. Passive mixer and active mixer.

3.2.2.1 Passive Mixer

Passive mixer, from its name, does not consume any power, and thus does not provide any gain. Passive mixers have two main topologies as shown in Figure 3.9 depending on its input port: single balanced as shown in Figure 3.9a or double balanced as shown in Figure 3.9b. The first one requires single input, while the other one requires differential input. Both of the two topologies are called balanced because of balanced local oscillator (LO) fed into the mixer gates.



(A) Single balanced sampling mixer. (B) Double balanced sampling mixer.

FIGURE 3.9: Passive mixer topologies [7].

For gain calculation, it is easier to consider one branch of a single balanced mixer and then multiply the final result by two to get the full conversion gain. In addition, the LO signal has a duty cycle of 50% and assuming that mixer input is a voltage source [7]. There are two states for the output node. First state is when the LO is high and the switch is on, $y_1(t)$, and second state is when LO is low, and the switch is off, $y_2(t)$ as shown in Figure 3.10.

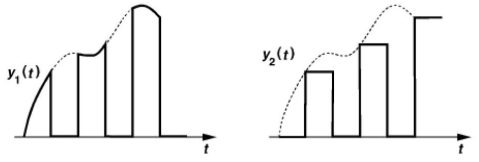


FIGURE 3.10: Output waveform [7].

Starting with $y_1(t)$ [7]

$$y_1(t) = x(t)\Big[\prod\Big(\frac{t}{T_{LO}/2} - \frac{1}{2}\Big) * \sum_{k=-\infty}^{+\infty} \delta\Big(t - kT_{LO}\Big)\Big] \tag{3.8}$$

and using Fourier's transformation gives

$$Y_1(f) = X(f) * \left[\frac{1}{j\omega}\Big(1 - e^{-j\omega T_{LO}/2}\Big)\frac{1}{T_{LO}}\sum_{k=-\infty}^{+\infty}\delta\Big(f - \frac{k}{T_{LO}}\Big)\right] \tag{3.9}$$

Calculating the summation for k $\pm = 1$ computes $Y_1(f)$ at the frequency of interest $Y_1(f)|_{IF}$

$$Y_1(f)|_{IF} = X(f) * \left[\frac{1}{j\omega}\Big(1 - e^{-j\omega T_{LO}/2}\Big)\frac{1}{T_{LO}}\delta\Big(f \pm \frac{1}{T_{LO}}\Big)\right] \tag{3.10}$$

Simplifying what in the brackets and convolving with $X(f)$ gives

$$Y_1(f)|_{IF} = \frac{X(f - f_{LO})}{j\pi} - \frac{X(f + f_{LO})}{j\pi} \tag{3.11}$$

For $y_2(t)$ it can be written as

$$y_2(t) = \left[x(t)\sum_{k=-\infty}^{+\infty}\delta\Big(t - kT_{LO} - \frac{T_{LO}}{2}\Big)\right] * \prod\Big(\frac{t}{T_{LO}/2} - \frac{1}{2}\Big) \tag{3.12}$$

Using Fourier's transformation gives

$$Y_2(f) = \left[X(f) * \frac{1}{T_{LO}}\sum_{k=-\infty}^{+\infty}e^{-j\omega T_{LO}/2}\delta\Big(f - \frac{k}{T_{LO}}\Big)\right]\frac{1}{j\omega}\Big(1 - e^{-j\omega T_{LO}/2}\Big) \tag{3.13}$$

Using k $\pm = 1$ to compute summation results in

$$Y_2(f)|_{IF} = \frac{1}{T_{LO}}\big[-X(f - f_{LO}) - X(f + f_{LO})\big]\left[\frac{1}{j\omega}\big(1 - e^{-j\omega T_{LO}/2}\big)\right] \tag{3.14}$$

$$Y_2(f)|_{IF} \approx \frac{-X(f - f_{LO}) - X(f + f_{LO})}{2} \tag{3.15}$$

Calculating the total output value produces

$$|Y_1(f) + Y_2(f)|_{IF} = \sqrt{\frac{1}{2\pi^2} + \frac{1}{4}}[|X(f - f_{LO})| + |X(f + f_{LO}|] \tag{3.16}$$

$$= 0.593[|X(f - f_{LO})| + |X(f + f_{LO}|] \tag{3.17}$$

This result is for one node and by multiply by 2 the total output value at the two nodes is

$$|Y_1(f) + Y_2(f)|_{IF} = 1.186[|X(f - f_{LO})| + |X(f + f_{LO}|] \approx 1.48dB \tag{3.18}$$

Through calculation, although the passive mixer is not used for amplification, it provides a 1.48 dB conversion gain.

Another parameter worth mentioning is LO self mixing. LO self mixing happens when the LO signal leaks to the mixer input, and mixed with itself. This produces a DC offset at the output. This happens due to the mismatch between the two MOSFET playing the role of switches as shown in Figure 3.11.

The leakage finds its way to the mixer input by C_{GS1} and C_{GS2}.

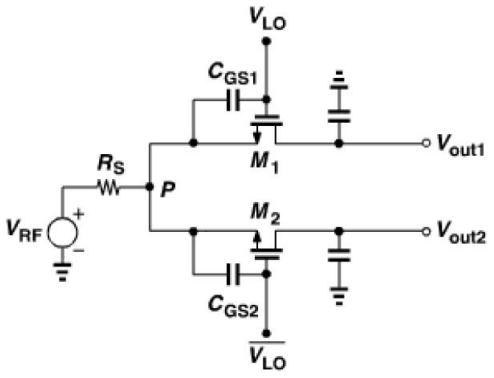


FIGURE 3.11: LO leakage path [7].

There is no accurate way to measure the value of DC offset due to self mixing. However, the DC offset created is in the range of 10 $\sim$ 20 mV [7].

In order to calculate the noise of the mixer, it is needed to recall the same procedures used to obtain the gain for single balanced sampling mixer. This is done by dividing the observation into two periods: "ON" state and "OFF" state as shown in Figure 3.12, where R_1 represents the switch resistance.

In noise calculation, V_{in} is assumed zero. Therefore,

$$\overline{V_{n,LPF}^2} = \overline{V_{n,R_1}^2} \times \frac{1}{1 + (R_1 C_1 \omega)^2} \tag{3.19}$$

What happens here is that the noise is shaped by RC circuit (low pass filter), where $\overline{V_{n,R_1}^2} = 2kTR_1$.

For noise calculation, the analysis is divided into three stages, the first stage is to compute the spectrum of V_{n1}, which is the noise component in on state, while excluding the low frequency component in noise of R_1, repeat for V_{n2}, which is the noise component in the off state. Then add the contribution of low frequency component to final results [7]. For V_{n1} it is the convolution product between $\overline{V_{n,LPF}^2}$ and the PSD of a square wave. Hence [7]

$$\overline{V_{n1}^2}(f) = 2 \times \left(\frac{1}{\pi^2} + \frac{1}{9\pi^2}\right)\left(\frac{2kTR_1}{1 + (2\pi R_1 C_1 f)^2}\right) \tag{3.20}$$

which at low frequency becomes

$$\overline{V_{n1}^2} = 0.226(2KTR_1) \quad [7] \tag{3.21}$$

For V_{n2}

$$\overline{V_{n2}^2} = kT\left(\frac{1}{4C_1 f_{LO}} - \frac{R_1}{2}\right) \tag{3.22}$$

The total noise value at the output node of the mixer at IF is:

$$\overline{V_{n,out,IF}^2} = kT\left(3.9R_1 + \frac{1}{2C_1 f_{LO}}\right) \tag{3.23}$$

For flicker noise, passive mixer has the advantage of a very low flicker noise output. The only drawback for passive mixers is that they require a rail to rail LO to operate properly.

3.2.2.2 Active Mixer

Active mixers are the type of mixers used to provide a gain beside the mixing or conversion operation. Figure 3.13 provides a typical schematic for single balanced active mixer, while double balanced active mixer as shown in Figure 3.14 is just two single balanced ones. Active double balanced mixers require a differential input like the passive double balanced mixer. Active mixers use current mode to perform the mixing operation. Using Figure 3.13 to illustrate, first, the active mixer converts the input RF voltage to a current through M_1. This current is down converted by two current switches M_2 and

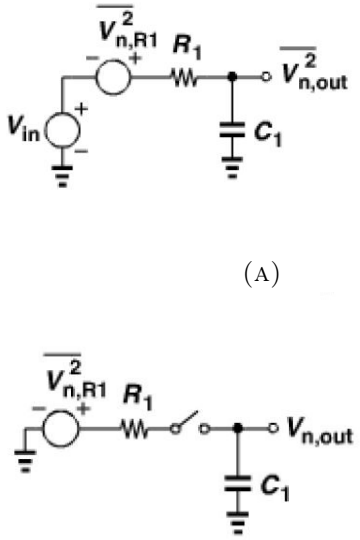


FIGURE 3.12: Mixer equivalent circuit for (A) on state (B) off state [7].

M_3, then a resistive load is used to reconvert the current to voltage at the IF frequency. The maximum output gain can be obtained through a single balanced active mixer as [7]

$$A_{v,max} = \frac{2}{\pi} g_{m1} R_{D,max} = \frac{4}{\pi} \frac{V_{R,max}}{V_{GS1} - V_{th1}} \tag{3.24}$$

where $V_{R,max}$ is the maximum allowed voltage across the load resistance. Therefore, from Eq. 3.24, decreasing the supply voltage reduces the available gain from active mixer. This is a drawback, because it limits optimizing the power consumption through decreasing the V_{DD}. The second drawback is the high amount of current required in order to provide a suitable conversion gain. The third drawback is noise, unlike passive mixers, active mixers produce flicker noise at their output [7]. For those mentioned reasons and for ultra low power and low noise applications, passive mixers are chosen for this work.

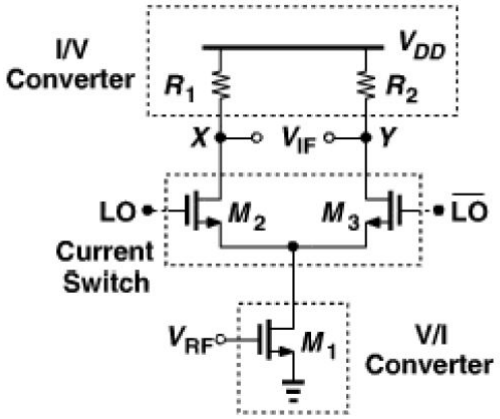


FIGURE 3.13: Single balanced active mixer [7].

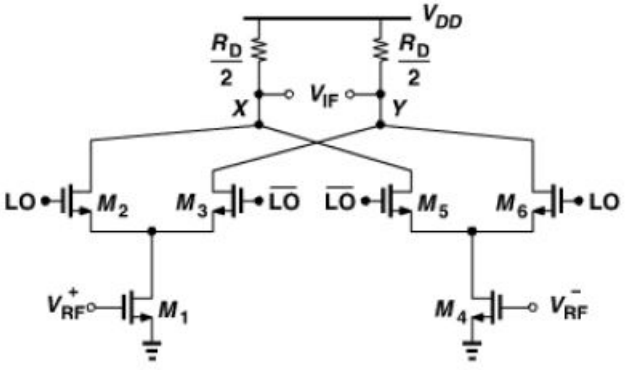


FIGURE 3.14: Double balanced active mixer [7].

Chapter 4

Ultra Low Power Receiver Design

This chapter presents the design procedures for each block of the ultra low power and low noise receiver using UMC 65 nm technology with detailed analysis for each block according to previously mentioned fundamental definitions in Chapters 2 and 3. For receiver architecture, low IF architecture is used.

4.1 LNA

For ultra low power and low noise applications, the promising LNA topology is cascode common source inductively degenerated LNA or (CCSLNA) as shown in Figure 4.1.

The proposed technique for power consumption reduction is to decrease the supply voltage. In order to decrease the supply voltage, MOSFETs in design are biased to work in weak inversion region. In order to calculate the minimum V_{DD} required to supply the circuit, the minimum V_{DS} needed for both M_1 and M_2 should be calculated. According to Figure 2.12, in order to have approximately constant current value I_D, there should be a V_{DS1} of $\approx 400mV$ for M_1. Furthermore, by the assumption that the cascode device M_2 needs V_{DS2} of $\approx 300mV$ to work properly. The supply voltage V_{DD} is set to be 0.7 V. In addition, the DC biasing voltage for M_1 should be in the range of $100 \sim 200$ mV lower than V_t according to Figure 2.12 and by knowing that V_t for UMC 65 nm low leakage low threshold RF MOSFETs, which are the MOSFETs used in this work is $\approx 400mV$, this leads to a V_{GS} of $300 \sim 400$ mV. Furthermore, in order to calculate the

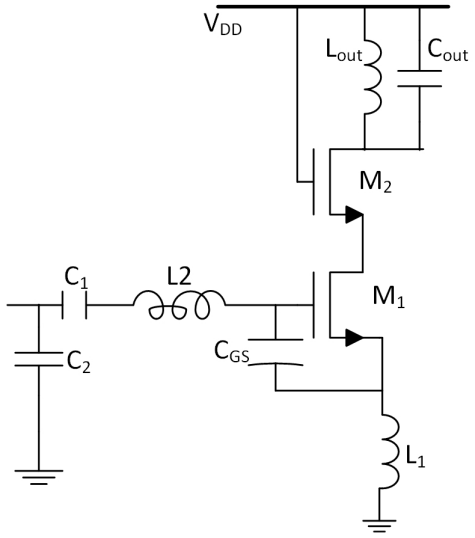


FIGURE 4.1: Proposed design for CCSLNA.

maximum allowed current consumption, it is assumed that the maximum allowed power consumption is $200uW$ or less for the LNA. Therefore, the maximum drain current I_D is

$$I = \frac{P}{V} \approx 285uA \tag{4.1}$$

The following step is to calculate the MOSFETs length and width in order to achieve the calculated I_D. Recalling Eq. 2.30 and using the minimum length offered by the technology, $L = 60nm$, the width of the device is $W = 45.6u$, which gives a g_m of $\approx 5m\Omega^{-1}$. In addition, the input impedance can be written as

$$Z_{in} = \frac{1}{C_{GS}S} + (L_1 + L_2)S + \frac{g_m L_1}{C_{GS}} \tag{4.2}$$

The real part is set to equal 50Ω to achieve maximum power transfer. By having a $g_m \approx 5m\Omega^{-1}$, the required degeneration inductance value for a C_{GS} of $\approx 400fF$ is 6.44 nH. Furthermore, the values for L_2, C_1, and C_2 are chosen to resonate the imaginary part of Z_{in}. The design is done in UMC 65nm CMOS technology with a carrier frequency of 2.5 GHz (ISM band). It provides a gain higher than 20dB and noise figure of 4.8 dB with a power consumption less than 194 μW from a 0.7 supply voltage. The design parameters are mentioned in Table 4.1. Table 4.2 summarizes the cascode CS LNA performance parameters and compares it to designs found in the literature. The designed CS LNA is superior in power consumption, supply voltage, and linearity, while providing an acceptable gain, noise figure and input matching.

Table 4.1: Design parameters for cascode CSLNA.

Parameters	Value	Multiplier
M_1	$\frac{5.7}{0.06}\mu$	8
M_2	$\frac{12}{0.06}\mu$	4
L_1	6.44 nH	-
L_2	7 nH	-
L_{out}	8.2 nH	-
C_1	2 pF	-
C_2	514 fF	-
C_{GS}	367 fF	-
C_{out}	102 fF	-

Table 4.2: LNA performance comparison.

References	[13]	[14]	[15]	[16]	[17]	This work
CMOS Tech.[nm]	180	180	180	180	180	65
Supply [V]	-	0.9	-	-	$1.5 \sim 1.8$	0.7
DC current [uA]	-	-	1200	4400	630	277
Power Cons [μW]	13500	960	-	-	-	194
S_{11}	-10.37	-18.1	-	-	-19	-11.25
Gain [dB]	$11.79^{\bullet}$	$14.4^{\bullet}$	$33^{\star}$	$18^{\star}$	$21.4^{\star}$	$22^{\star}$
NF [dB]	3.89	1.6	2.2	3.5	5.2	4.8
IIP_3 [dB_m]	-3	-9	-8.7	-3	-11	+4.6

• Power gain.
⋆ Voltage gain.

4.2 Mixer

Considering the mixer topologies mentioned in Chapter 3, the suitable topology for this work is single balanced sampling passive mixer. As previously mentioned, passive mixers need rail to rail LO signal in order to operate properly. Therefore, a mixer pre-driver is needed to support rail to rail square wave signal at the gates of the mixer.

4.2.1 Mixer Pre-driver

Mixer pre-driver is a circuit used to provide rail to rail square wave signal from a crystal oscillator (XO) with a sine wave output. The technique for transforming sine wave to square wave is by using a chain of inverters. Figure 4.2 provides a model diagram for mixer pre-driver, which consists of a primary inverter, a transmission gate to give an equal delay to the upper inverter while maintaining the same 180° phase difference, and the last two inverters to drive the gate capacitance of the mixer. This pre-driver uses biased-gate technique to provide a DC voltage near threshold voltage of both n and p MOSFETs to make them operate properly and support rail to rail square wave output while using a supply voltage of 0.7 V. This DC bias voltage is provided by a 3 bit digital to analog converter (DAC).

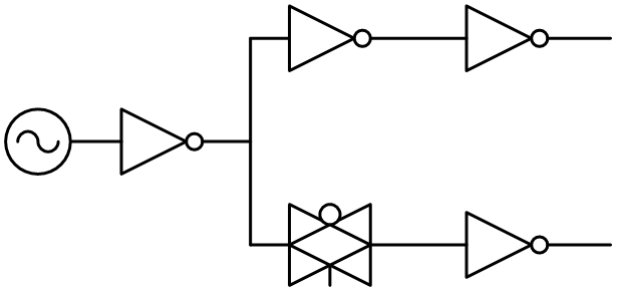


FIGURE 4.2: Mixer pre-driver model diagram.

Figure 4.3 shows the output square wave at the two nodes of the mixer pre-driver. They are rail to rail with minimum overlap and they settle down in 12 ns. Figure 4.4 shows the output signal after the settle down period with intersection point less than $V_{DD}/2$. This pre-driver consumes an approximate average current of 180μA from 0.7 supply voltage.

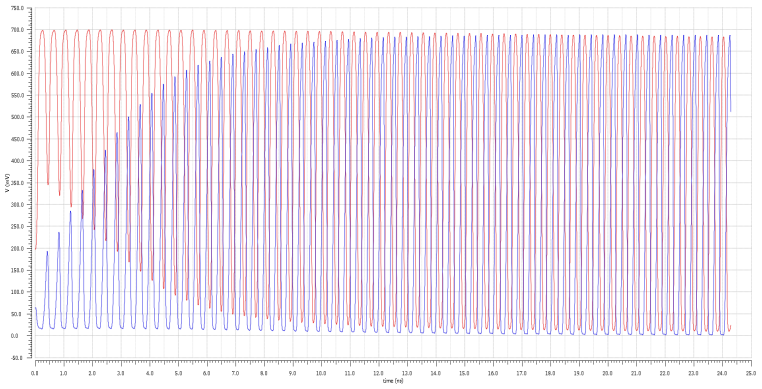


FIGURE 4.3: Mixer pre-driver output signal.

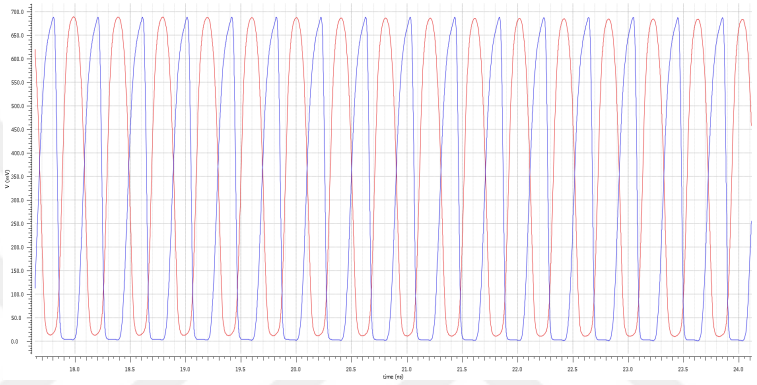


FIGURE 4.4: Mixer pre-driver signal after settling.

4.2.2 Mixer Design

Figure 4.5 provides a block diagram for the designed mixer. The capacitance tied to the source of the two MOSFETs are to block the DC voltage from the LNA output. As already mentioned, LNA uses LC tank as output load, therefore, the DC voltage of this node is equal to $\approx V_{DD}$. This voltage saturates the MOSFETs if connected directly to them. Note that the resistance of the MOSFETs should be minimized at the frequency of operation.

Another parameter that needs observation is the threshold voltage of the MOSFETs used in the mixer. In order to have the minimum value for V_t, MOSFET body terminal should be connected to its source terminal to have a $V_{SB} = 0$. This minimizes the threshold voltage of the MOSFET, as it is defined as [18]

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}\right) \tag{4.3}$$

where V_{t0} is the threshold voltage value when V_{SB} is zero, γ is the body effect coefficient for given technology, and ϕ_0 is given by [18]

$$\phi_0 = 2\phi_F + \Delta\phi \tag{4.4}$$

Therefore, as Eq.4.2 shows, $V_{SB} = 0$ gives $V_t = V_{t0}$. The MOSFETs used in mixer design are triple well devices, allowing to connect the MOSFET body terminal to its source terminal. Figure 4.6 shows the output of the mixer at 1 MHz. While there are some ripples, those ripples are high frequency components which are going to be filtered out in the following stage (baseband amplifier) due to its limited bandwidth. Figure 4.7 shows mixer output versus frequency and it has a 3 dB cut off frequency of $\approx$ 5 MHz. Figure 4.8 shows the noise figure of the front end (LNA and mixer combined) at 1 MHz which is 8.11 dB. However, recalling the two definitions for SSB and DSB noise figure, and spectre calculates the noise SSB, shown NF is 3 dB higher than DSB result. Therefore, the DSB NF of the front end is 5.11 dB, or in other words, the NF added to the system due to the mixer is $\approx$ 0.3 dB which is quite low. It is worth mentioning that from Figure 4.8, flicker noise corner is $\approx$ 100 KHz, which is quite far from the wanted signal bandwidth at 1 MHz.

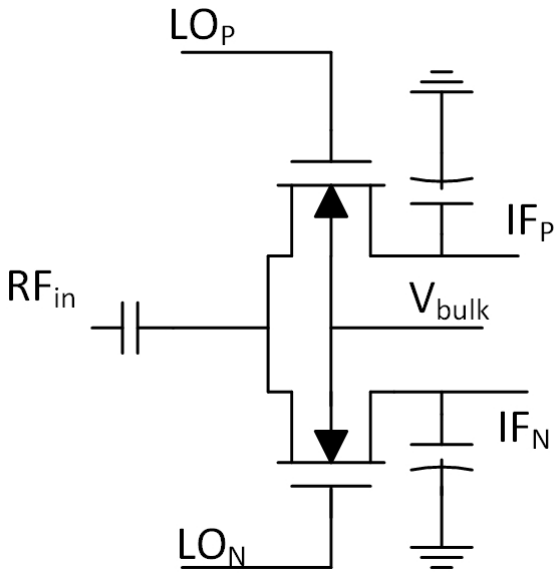
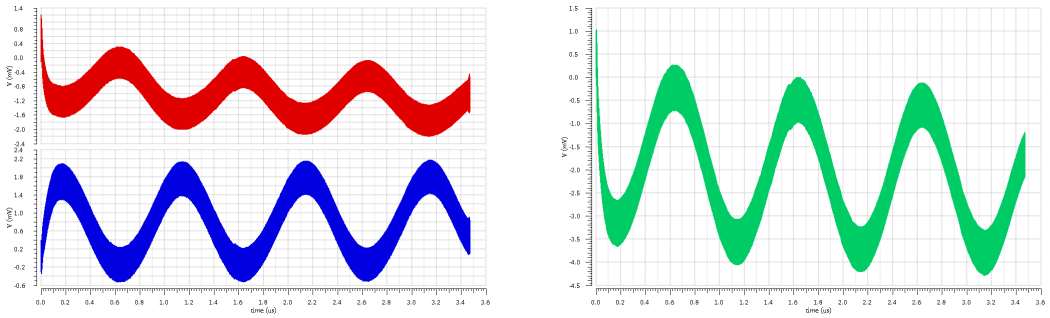


FIGURE 4.5: Mixer block diagram.



(A) (B)

FIGURE 4.6: Mixer output signal A) each node separately B) Differential.

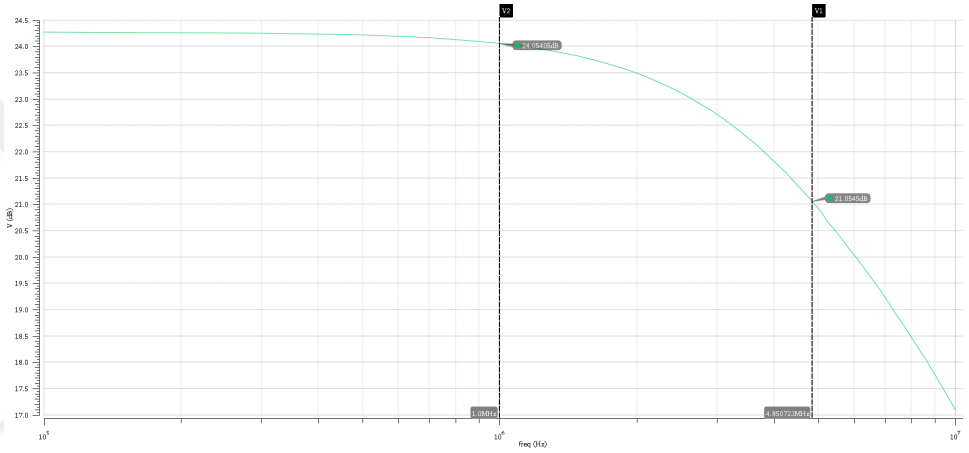


FIGURE 4.7: Mixer gain versus frequency.

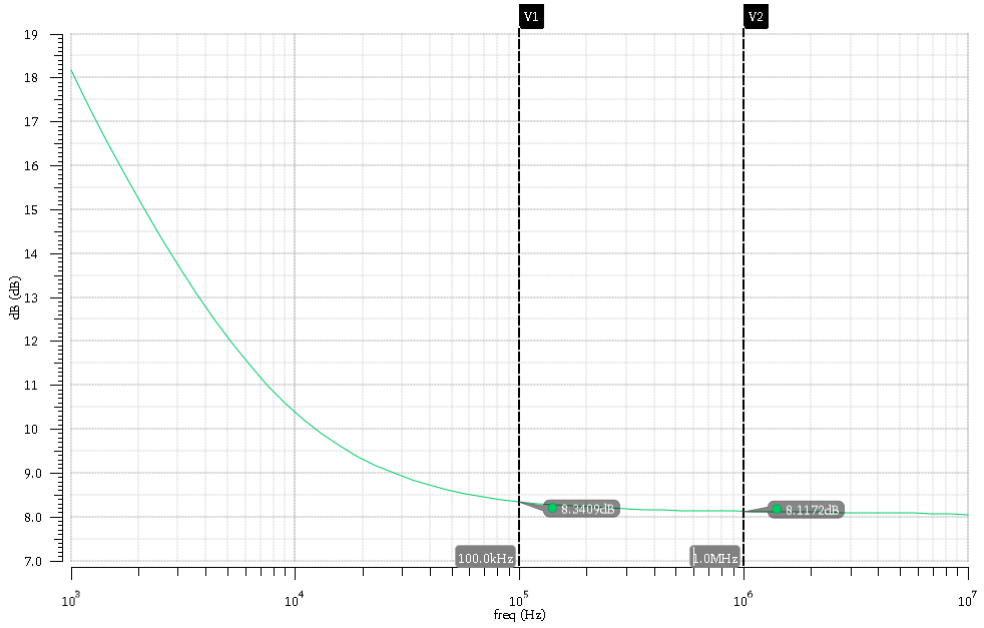


FIGURE 4.8: Front end NF i.e. LNA and mixer combined.

4.3 Baseband Amplifier

The designed front end provides a maximum gain of 23.4 dB under the strict requirement that the power consumption is minimized as previously mentioned. For the minimum input signal of -90 dB_m, the signal can only reach -66.6 dB_m, which is 315 μV_{p-p}. This value is too small to be resolved. Therefore, additional amplification is needed. This additional amplification can not be done in RF because of the limitation on RF LNA and mixer power consumption, therefore, it is done in the baseband. Mixer provides a differential output, which allows using a differential amplifier with no additional single ended to differential ended converters. The most important benefit of using differential amplifier is that it ideally does not generate second order distortion terms.
The proposed design is a differential amplifier with two modes for output load: Active load (p-MOSFET current source) and passive load (resistive). The two modes are for different power consumption and gain depending on RF input level. Figure 4.9 provides a model diagram for the amplifier. Recall that the gain of a CS amplifier is simply

$$A_v = g_m \times R_{out} \tag{4.5}$$

In order to increase the gain, increase either g_m of the MOSFET or the output load. While increasing the g_m may be more complex (recall Eq. 2.32), it is easier to increase the output impedance.

P-MOSFET current source provides a very high output impedance (r_o), which boosts the signal amplitude for small input levels, while in case of moderate or high input signal, resistive output is used. A constant voltage drop across the load is needed in order to maintain a constant V_{DS} for both M_{n1} and M_{n2}, thus maintaining the two MOSFETs in inversion region. In resistive load mode it is not a problem because of the fixed voltage drop across the resistors, while in active load mode a common mode feedback circuit is needed to maintain this voltage drop constant. Figure 4.9 provides a circuit diagram for the amplifier with common mode feedback circuit.

Figure 4.10 shows the amplifier gain in active load mode. The amplifier has a constant gain of 23.85 dB over a bandwidth of 10 MHz, while the feedback circuit has a gain-bandwidth product at 8 MHz with a phase margin of 45°, which is quite acceptable

recalling that the wanted signal is at 1 MHz. Figure 4.11 shows the amplifier gain variation versus temperature. It has a 1.4 dB variation over a range of $40C°$. Figure 4.12 shows the amplifier gain when resistive load is used; it has a constant gain of 16.8 dB and a 3 dB cut off frequency of 28 MHz.

Figure 4.13 shows the noise figure of the full system for both active load and resistive load. It is remarkable that, for active load the increase in the noise figure for the full system is only 0.3 dB and with resistive load it is 0.32 dB. The amplifier consumes 380 μA in active load configuration, while consuming 178 μA in resistive load configuration, which gives a power consumptions of 266 μW and 124.6 μW respectively. The full system bandwidth is limited by the mixer as shown in Figure 4.7. The system has a 3 dB cut off frequency of 4.8 MHz. The full system has an IIP_3 of -37.7 dB_m in active load mode, while achieving an IIP_3 of -21.6 dB_m in resistive load mode. However, it is quite enough as the wanted signal is at 1 MHz. Figure 4.14 - Figure 4.17 show the system IIP_3 for high and low gain configuration (simulation is done using rapid IIP_3 engine), input matching, and layout view for the system. Table 4.3 summarizes the RX performance parameters and compares it to similar designs.

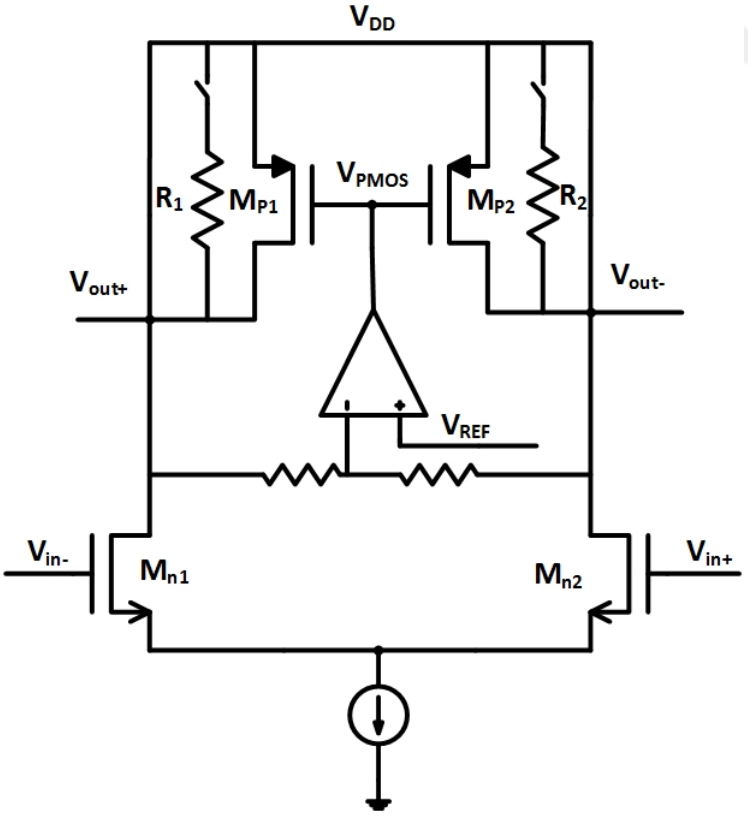


FIGURE 4.9: Model diagram for baseband amplifier.

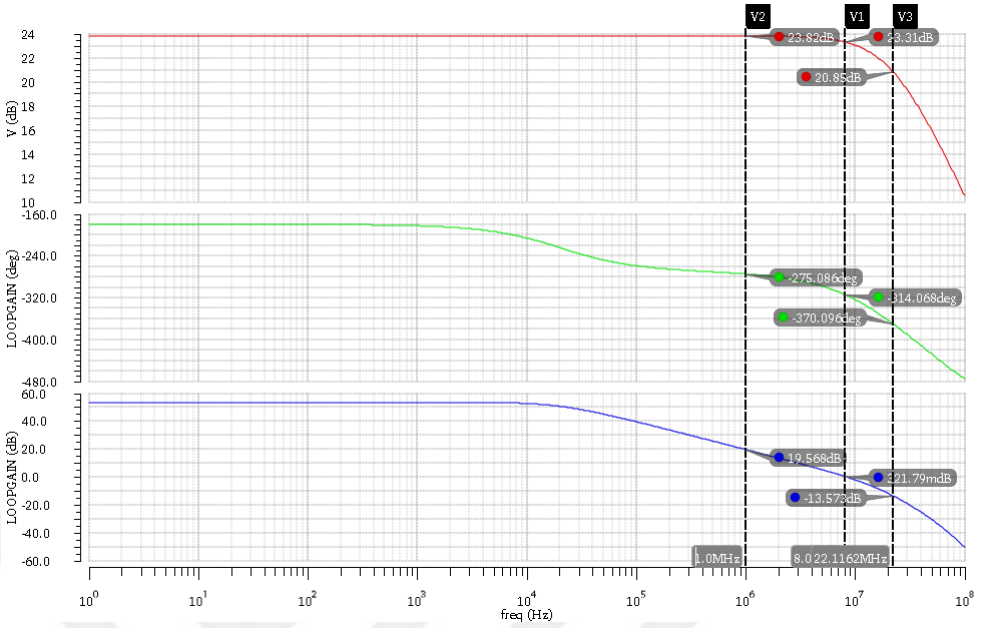


FIGURE 4.10: Amplifier gain (red) with common mode feedback circuit phase margin (green) and gain (blue).

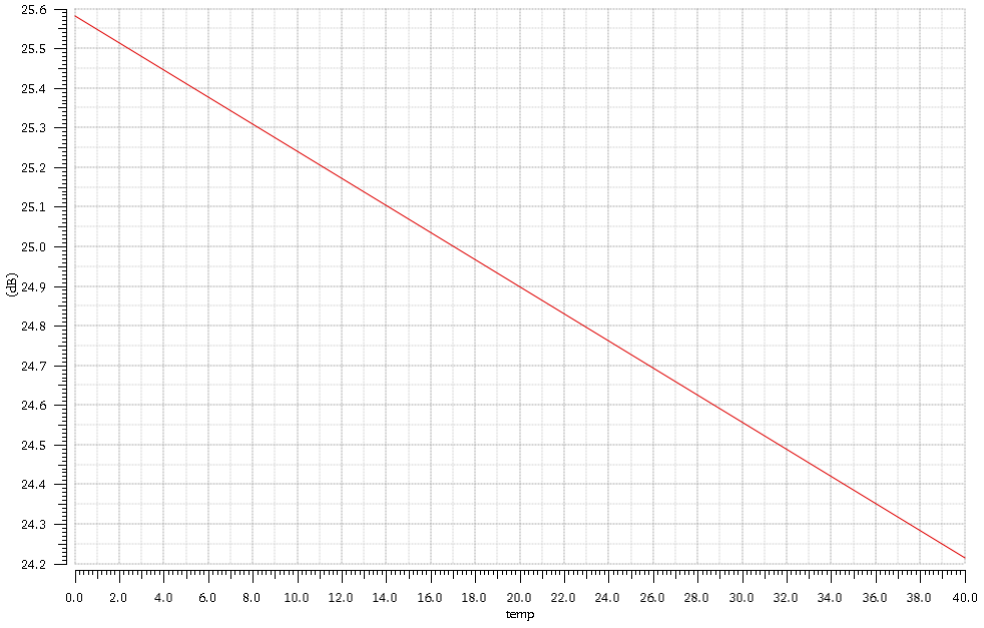


FIGURE 4.11: Amplifier gain versus temperature.

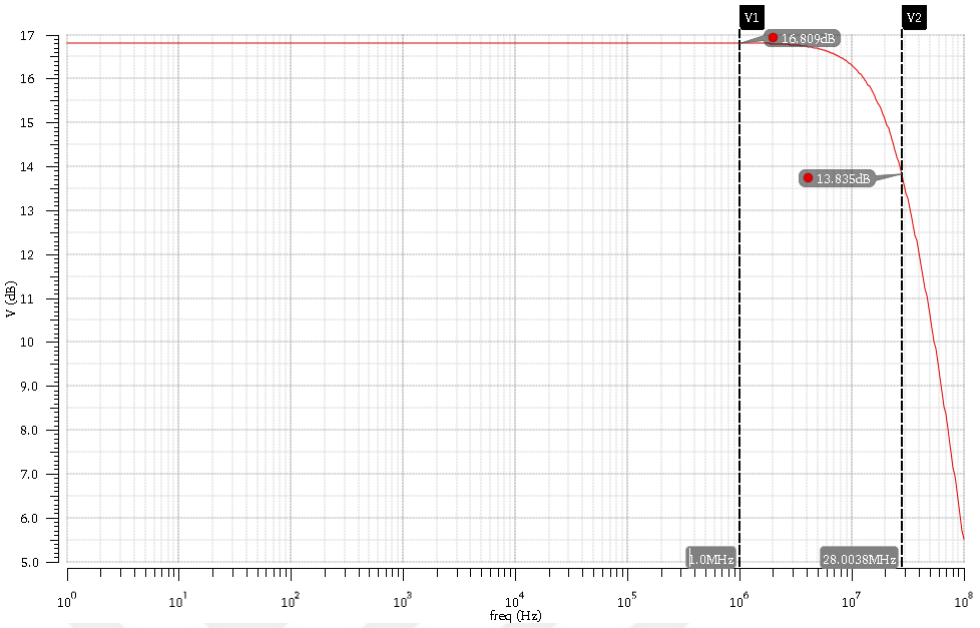


FIGURE 4.12: Amplifier gain with resistive load.

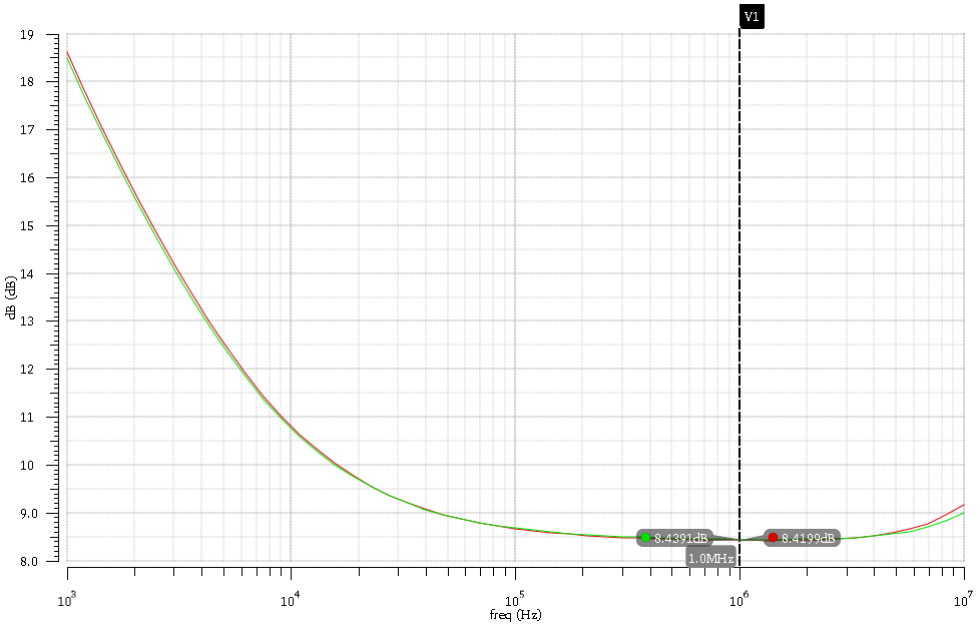


FIGURE 4.13: System NF for active and resistive load baseband amplifier.

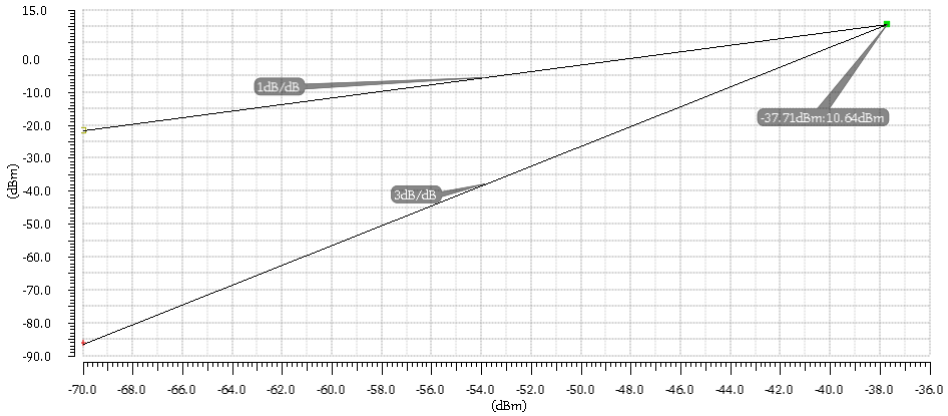


FIGURE 4.14: IIP_3 for high gain configuration.

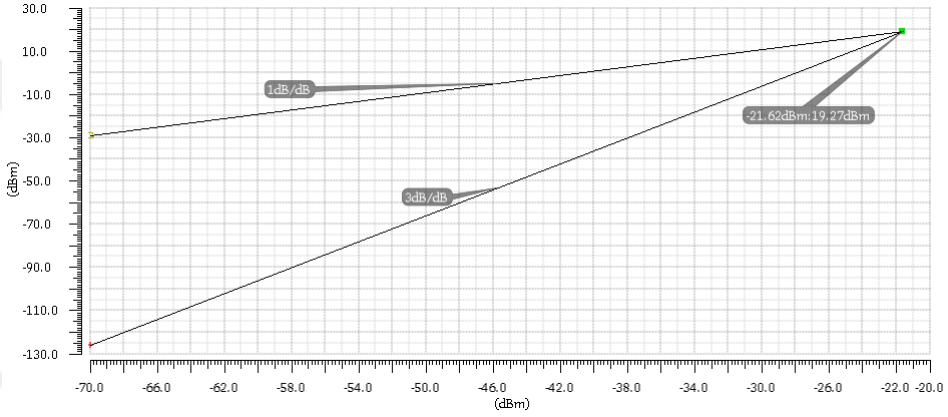


FIGURE 4.15: IIP_3 for low gain configuration.

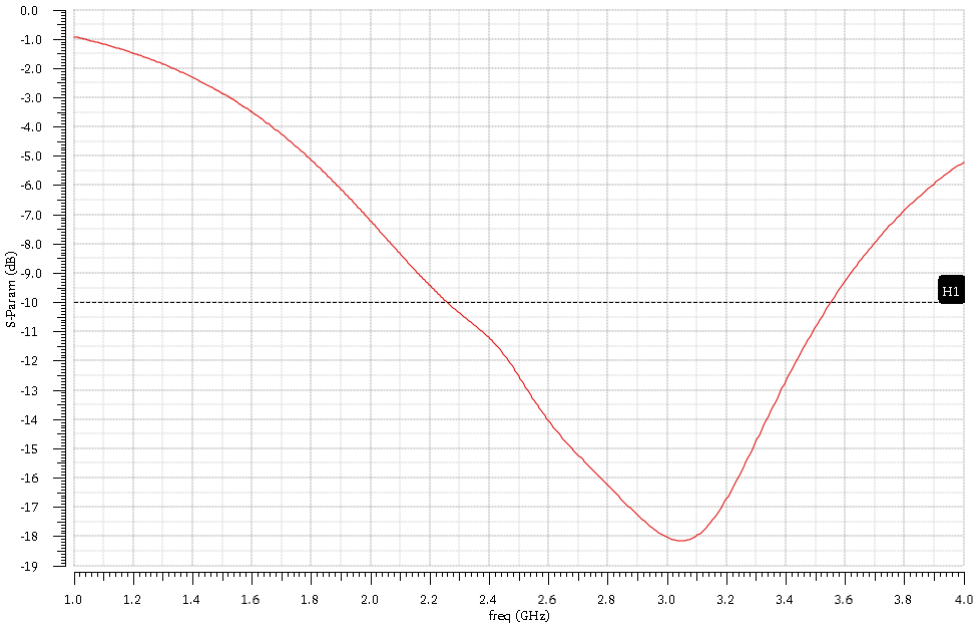


FIGURE 4.16: S_{11}.

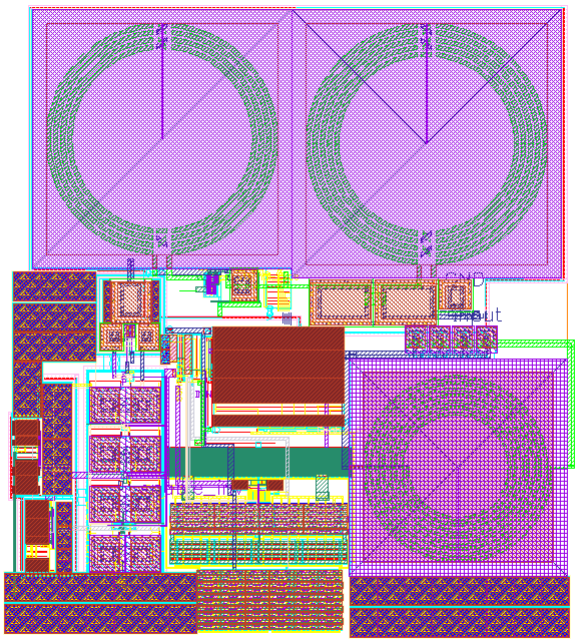


FIGURE 4.17: Layout view.

TABLE 4.3: System performance comparison.

References	[19]	[20]	[21]	[22]	This work
CMOS Tech.[nm]	180	65	180	90	65
Supply [V]	1.2	0.85	1	1.2	0.7
DC current [μA]	-	500	1200	-	1023* | 820*
Power Cons [μW]	1400 (2600*)	550	500	3600	716 | 574
S_{11}	$<$ -25	$<$ -16	-	$<$ -20	-11.25
Gain [dB]	43	41	30.5	75	45.85 | 38.8
NF [dB]	5	9.6	19@10 MHz	9	(5.4 | 5.42)
IIP_3 [dB_m]	$-37^\bullet$	-30	-21^+	-12.5	-37.7 | -21.6
Area [mm^2]	-	0.15	$2.32^\dagger$	0.35	0.194

$*$ including the pre-diver AC current.
$\star$ including VCO power consumption.
$\bullet$ Calculated by subtract gain value from OIP_3.
$+$ Calculated by adding 10 dB to 1-db compression point.
$\dagger$ Including pads.

Chapter 5

Conclusion and Future Work

5.1 Conclusion and Future Work

This work presented an ultra low power, low noise and area optimized RF receiver design. This receiver works at 2.5 GHz ISM band and is designed in UMC 65 nm CMOS technology. The schematics, simulations and physical verification (layout) are done using Cadence. The main approach for power consumption optimization in this work is the use of MOSFETs in weak inversion region. Compared to similar works as shown in Table 4.3, the designed receiver achieves a high gain (more than 45 dB) with low noise figure (less than 5.4 dB), and less than -11 dB input matching. The design has an IIP_3 of -21.6 dB_m, optimizes die area (less than 0.195 mm^2), and achieves an ultra low power consumption of (700μW). This receiver is designated for ultra low power and low noise applications.

The next step for this work is to decrease the V_{DD} further by reducing the supply voltage further and optimize the CSLNA area by decreasing the number of inductors.

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