High Gain, High Bandwidth, Wide ICMR, and Highly Linear Fully Differential Amplifier with Large Dynamic Range and Process Corner Configurable Output Stage

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in

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This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Electronics and Computer Engineering.

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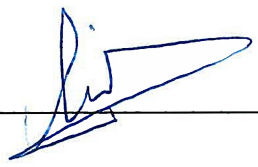
Signed: 

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"Make things as simple as possible, but not simpler."

Albert Einstein

High Gain, High Bandwidth, Wide ICMR, and Highly Linear Fully Differential Amplifier with Large Dynamic Range and Process Corner Configurable Output Stage

Amir Mozammel Hokmabadi

Abstract

Pre-ampifier is one of the most important building blocks in designing analog to digital converters (ADC). Most of the ADCs have a pre-amplifier implemented for driving the large input capacitance of the ADC or amplifying the weak naturally occurred input signals. One of the key factors in designing a pre-amplifier is its signal to noise and distortion ratio (SINAD) as the noise and distortion introduced by the pre-amplifier might degrade the effective number of bits (ENOB) of ADC.

This work introduces a high gain, high bandwidth, wide input common mode range (ICMR), and highly linear fully differential folded cascode pre-amplifier for a 14-bit analog to digital converter. The system uses native n-channel transistors as differential input pair to achieve a wide ICMR with minimum transconductance variation. The total harmonic distortion (THD) of the pre-amplifier is minimized over different process corners. A process corner configurable class AB output stage is implemented to provide a rail to rail output signal. Additionally, a process corner configurable compensation circuit is implemented to ensure the stability of system over different process corners. The pre-amplifier achieves a closed-loop gain of $130dB$, a unity gain bandwidth of $200MHz$, a THD of $-92.2dB$, and a phase margin of $68°$. The pre-amplifier is designed using TSMC 180nm CMOS technology.

Keywords: High Gain, High Bandwidth, Wide ICMR, Fully Differential, Differential Amplifier, Process Corner Configurable, Rail to Rail Output

Büyük Dinamik Aralığa Sahip ve İşlem Köşesi Ayarlanılabilen Çıkış Katına Sahip, Yüksek Kazanç, Yüksek Band Genişliği, Geniş ICMR ve Son Derece Doğrusal Tam Diferansiyel Ön Yükselteci

Amir Mozammel Hokmabadi

Öz

Ön yükselteç, analogdan dijitale çevirici (ADC) blokların tasarımında en önemli kısımlardan birisidir. ADC'lerin bir çoğunda ön yükselteçler ADC'nin geniş girdi kapasitansını çalıştırabilmek yada zayıf doğal olarak oluşan girdi sinyalini güçlendirmek amacıyla kullanılmaktadırlar. Ön yükselteç tasarlarken en önemli faktörlerden birisi sinyal-gürültü ve bozulma oranı (SINAD) çünkü ön yükseltecin ürettiği gürültü ve bozulma efektif bit sayısını (ENOB) düşürebilir.

Bu çalışma, yüksek kazanç, yüksek bant genişliği, geniş giriş ortak mod aralığı (ICMR) ve 14 bitlik bir analogdan dijitale çevirici için son derece doğrusal tam diferansiyel katlanmış kask ön-yükselteciyi tanıtıyor. Sistem, minimum transkondüksiyon varyasyonu ile geniş bir ICMR elde etmek için diferansiyel giriş çifti olarak doğal n-kanal transistör kullanmaktadır. Ön-yükseltecin toplam harmonik bozulması (THD), farklı işlem köşelerinde en aza indirgenmiştir. Uçtan uça besleme gerilimleri arasinda çıktı sinyali sağlayabilmesi için ayarlanabilen AB sınıfı çıktı katı olan ADC tercih edilmiştir. Ek olarak, farklı çalışma şartlarında sistemin kararlılığını sağlayabilmek için işlem köşesi ayarlanabilen bir dengeleme devresi dizayn edilmiştir. Ön yükselteç, 130 dB kapalı döngü kazancı, 200 MHz birim kazanç bant genişliği, -92.2 dB THD ve 68 derece faz payı elde etmektedir. Ön yükseltici TSMC 180 nm CMOS teknolojisi kullanılarak tasarlanmıştır.

Anahtar Sözcükler: Yüksek kazanç, Yüksek Band genişliği, Geniş ICMR, Tam Diferansiyel, Diferansiyel Yükseltici, Ayarlanabilir İşlem Köşesi, Uçtan uça Besleme Gerilimleri Arasındaki Çıktı

To my parents and siblings

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Abbreviations

ADC	**A**nalog to **D**igital **C**onverter
AFFC	**A**ctive-**F**eedback **F**requency-**C**ompensation
CG	**C**ommon-**G**ate
CMFB	**C**ommon-**M**ode **F**eedback
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CMRR	**C**ommon-**M**ode **R**ejection **R**atio
CS	**C**ommon-**S**ource
DC	**D**irect **C**urrent
DR	**D**ynamic **R**ange
ENOB	**E**ffective **N**umber **O**f **B**its
GBWP	**G**ain **B**and**w**idth **P**roduct
ICMR	**I**nput **C**mmon **M**ode **R**ange
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
Op-Amp	**Op**erational **Amp**lifier
OTA	**O**perational **T**ransconductance **A**mplifier
OVSR	**O**utput **V**oltage **S**wing **R**ange
PM	**P**hase **M**argin
PSD	**P**ower **S**pectral **D**ensity
PSRR	**P**ower **S**upply **R**ejection **R**atio
RHP	**R**ight **H**alf **P**lane
SAR	**S**uccessive **A**pproximation **R**egister
SINAD	**Si**ngal to **N**oise **A**nd **D**istortion Ratio
SNR	**S**ignal-to-**N**oise **R**atio
THD	**T**otal **H**armonic **D**istortion
UGB	**U**nity **G**ain **B**andwidth

UGF	**U**nity **G**ain **F**requency
VLSI	**V**ery-**L**arge-**S**cale **I**ntegration

Chapter 1

Introduction

1.1 Thesis Motivation

An operational amplifier (op-amp) is one of the most important and fundamental building blocks of many analog circuit designs. It is used in many applications such as transceivers, multimedia systems, radar and medical devices. An op-amp which has been designed to provide transconductance, called operational transconductance amplifier (OTA), should provide high input and output impedance. The amplifier's performance is usually evaluated according to various factors such as gain, bandwidth, noise figure, slew rate, linearity, etc. However, there is no global standard acceptable values for these factors and they are usually defined according to the application of amplifier. Hence, performance parameters of an amplifier needs to be set in order to suit its application.

The tremendous advancement of digital signal processing and easiness of manipulating signals in digital domain have created a great tendency towards digital circuit design. Moreover, compared to analog signals, digital signals are less susceptible to noise and more suitable for high resolution applications. However, since all natural signals are analog, analog to digital converter (ADC) is required to digitize the input signal before performing any digital signal processing. For example, applications such as DVD players, digital communication systems, voice activated devices and medical imaging use ADCs to convert the raw analog input signal into digital signal.

One of the most important factors for measuring an ADC's performance is its effective number of bits (ENOB). An ADC's ENOB denotes its dynamic range and resolution by

the number of bits it can use to represent the analog input value. As the demand for high performance and high resolution applications increases, the need for high resolution ADCs with large ENOB rises. ENOB of an ADC is expressed as

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{1.1}$$

where SINAD is the singal to noise and distortion ratio. From Eq.1.1 it is obvious that to increase the ENOB of an ADC one needs to increase its SINAD. For example, a 14-bit ADC should have a SINAD of 86.04 dB.

Most of the analog to digital converters, such as flash ADCs, sigma-delta ADCs, pipeline ADCs, successive approximation register (SAR) ADCs, and algorithmic ADCs, have a sampling block to sample and hold the analog input signal. This sample and hold block is usually implemented by using switched capacitor circuits which results in a high input capacitance for the ADC. Since the raw analog input signal is usually weak, an operational amplifier is used to amplify or/and buffer the input signal. This amplifier is usually referred as pre-amplifier.

For high performance applications and high resolution ADCs, the pre-amplifier is required to provide high gain and high unity gain frequency (UGF). High gain is required for accurate charge transfer and high UGF is essential for high speed applications. Additionally, as per Eq.1.1, the linearity and noise of the pre-amplifier are essential factors for defining the ENOB of ADC. Many rail to rail operational amplifiers have been proposed in [5–22] to increase the SNR, and as a result increase the dynamic range of amplifier, by providing wide input common mode range (ICMR) and large output voltage swing range (OVSR). But none of them are suitable for high performance applications because of their high total harmonic distortions. A pre-amplifier with large total harmonic distortion (THD) degrades the ENOB of the ADC and as a result, limits the ADC's resolution. The proposed work presents a high gain, high bandwidth fully differential amplifier with common mode feedback and process corner configurable compensation. The proposed amplifier is designed to have a high dynamic range by minimizing the THD and utilizing an input stage with wide ICMR.

1.2 Thesis Objective

The objective of this thesis is to design a high gain and high bandwidth operational amplifier with large dynamic range and new proposed wide ICMR input stage. The proposed design uses a process corner configurable compensation circuit to meet the bandwidth requirement and ensure the stability of the amplifier over different process corners. It also uses a process corner configurable class AB output stage to provide rail to rail OVSR and minimize the THD over different process corners.

Figure 1.1 illustrates the proposed operational amplifier's application. The op-amp is designed to buffer the single ended signal coming from a sensor and drive a 14-bit pipeline ADC with performance parameters summarized in Table 1.1. The pre-amplifier will operate in unity gain feedback configuration at 5 MHz. Since the sampling frequency of ADC is 10 MHz, the main objective of this design is to minimize THD and noise at 5 MHz to prevent the amplifier from limiting ADC's ENOB. The proposed design achieves a gain of 130 dB, a phase margin (PM) of 68°and a THD of -91.88 dB. The system is designed using TSMC 180 nm CMOS technology. The schematics and simulations are done using Cadence Virtuoso Analog Design Environment.

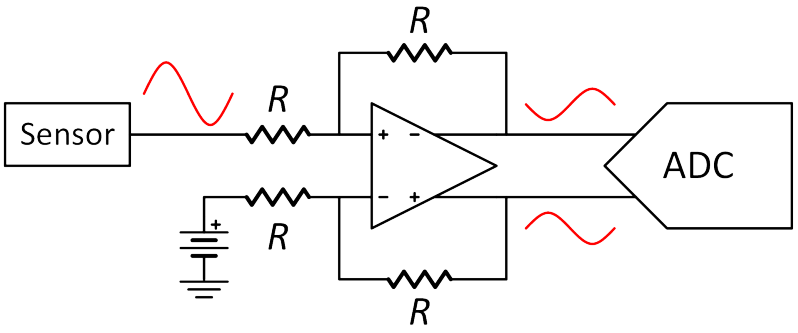

FIGURE 1.1: Amplifier application block diagram.

TABLE 1.1: ADC specs

Architecture	Pipeline ADC
Resolution	14-bit
Sampling frequency	10 MHz
Input amplitude	2.2 V_{pp} (differential)
Input capacitance	4 pF (differential)
SINAD	79.72 dB
ENOB	12.95

1.3 Thesis Organization

This thesis is organized into 6 chapters. In chapter 2, fundamental elements in designing an amplifier are explained. Different topologies for designing fully differential amplifier and the key factors for evaluating an amplifier's performance are briefly reviewed as well. Frequency compensation techniques and different topologies for output stage implementations are briefly explained. Finally gain boosting techniques are reviewed at the end of chapter 2.

In chapter 3, various commonly implemented rail to rail amplifier configurations are reviewed. Advantages and disadvantages of these design configurations are studied as well.

In chapter 4, the proposed design and its specifications are introduced. In later sections, a completed analysis of proposed system as well as design steps and schematics are introduced.

Chapter 5 includes the simulation results and performance analysis of high gain, high bandwidth, wide ICMR and large dynamic range amplifier. Later, process corner simulation results are presented in this chapter.

Finally, chapter 6 concludes this thesis and suggests possible improvements and future works.

Chapter 2

Fundamentals of Amplifier Design

2.1 Introduction to MOS Transistors

A typical metal-oxide-semiconductor field-effect transistor (MOSFET) has four terminals: gate (G), source (S), drain (D), and body (B) terminals. Depending on the type of doping, a substrate may have two types: a p-type substrate and an n-type substrate. Furthermore, considering the physical structure, a MOSFET may be fabricated in two types: enhancement-type MOSFET and depletion-type MOSFET. The difference between enhancement-type and depletion-type MOSFETs will be explained in Section 2.1.1 and Section 2.1.2 in more details. Figure 2.1 shows a cross-sectional view of an enhancement-type n-channel MSOFET (NMOS) and p-channel MOSFET (PMOS) integrated on a p-type substrate. This integration is commonly known as complementary metal-oxide-semiconductor (CMOS) [1].

A MOSFET may operate in one of the following four regions: cut-off, triode, weak inversion, and strong inversion (saturation). If V_{GS} is significantly larger than the threshold voltage (V_{TH}) of MOSFET ($V_{GS} > V_{TH}$), it is considered as operating in saturation region. Sometimes the saturation region is called linear region as well. In analog circuit design, MOSFETs used to design amplifiers are biased to operate in saturation region. The drain-source current (I_D) of a MOSFET operating under saturation mode is approximated by

$$I_D = \frac{1}{2}\mu C_{ox}(\frac{W}{L})(V_{GS} - V_{TH})^2 \tag{2.1}$$

where μ is carriers mobility, C_{ox} is thickness of silicon oxide underneath the gate, W and L are channel width and length, respectively, V_{GS} is the gate to source voltage, and V_{TH} is threshold voltage. (V_{GS} - V_{TH}) is called the overdrive voltage (or sometimes effective voltage) [23].

2.1.1 Enhancement Mode MOSFET

For simplicity, in this section and Section 2.1.2, we will consider a p-type substrate NMOS. In a typical enhancement-type NMOS, there are two highly doped n-type regions on a p-type substrate behaving as drain and source. The entire surface is coated with silicon dioxide (SiO_2) and the gate contact is placed on top of SiO_2 layer (Figure 2.1). With zero gate voltage, if a voltage source is connected across drain and source terminals, with positive terminal at drain and negative terminal at source , a reversed biased p-n junction between drain and substrate will be created in series with a forward biased p-n junction between source and substrate. Hence, there will be no current flowing from drain to source as there is no conducting channel.

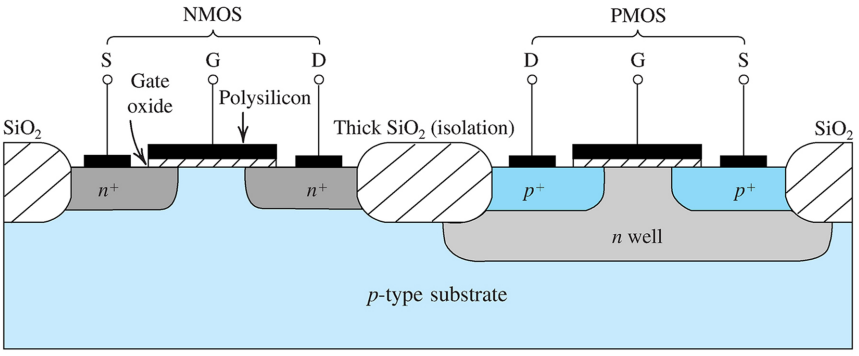

FIGURE 2.1: Cross-section of an enhancement-type CMOS integrated circuit [1].

Keeping the same drain-source voltage (V_{DS}), if we apply a positives voltage at gate terminal, minority carriers in substrate will be accumulated between drain and source. If the applied positive voltage is greater than threshold voltage of transistor, accumulated carriers create a conducting n-channel between drain and source and current starts to flow from drain to source. The conductivity of this induced n-channel depends on the amount of positive voltage applied at gate terminal [1]. In other words, for $V_{GS} - V_{TH} \leq 0$, there is no current flowing from drain to source and the device is off (assuming $V_{SB} = 0$). But applying a positive V_{GS} greater than V_{TH} enhances the channel and turns the device on. An enhancement-type n-channel transistor (NMOS) has a positive V_{TH}; whereas, an

enhancement-type p-channel transistor (PMOS) has a negative V_{TH}. Both enhancement devices are normally off [2]. $I_D - V_{GS}$ characteristics for the two types of devices for a very small $|V_{DS}|$ are shown in Figure 2.2.

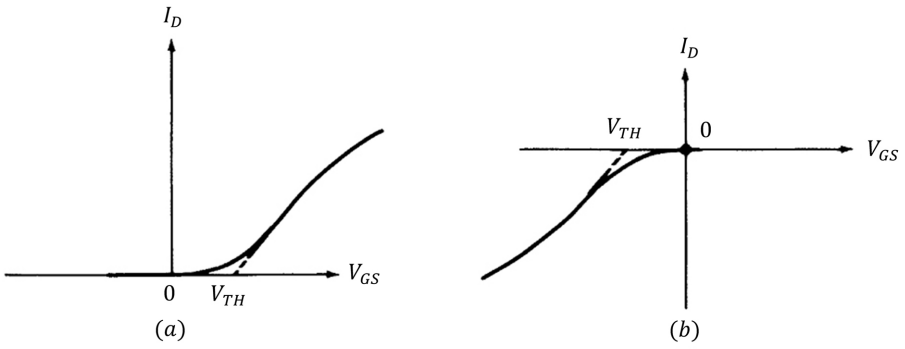

FIGURE 2.2: $I_D - V_{GS}$ characteristic for very small $|V_{DS}|$ and $V_{SB} = 0$ for (a) n-channel enhancement device and (b) p-channel enhancement device [2] (modified).

2.1.2 Depletion Mode MOSFET

As discussed in Section 2.1.1, enhancement devices have no physically fabricated conducting channel between drain and source. But, considering NMOS transistor, if there was a previously created n-channel between drain and source, there would be a current flow through the channel due to applied voltage between the drain and source even at zero gate voltage. For this reason, depletion-type devices are normally on. The diffused channel is created during the fabrication of transistor by utilizing ion implantation techniques. Hence, compared to their enhancement-type counterpart, fabrication of depletion-type MOSFETs requires additional masks. Figure 2.3 shows a cross-sectional view of a depletion-type CMOS integrated circuit.

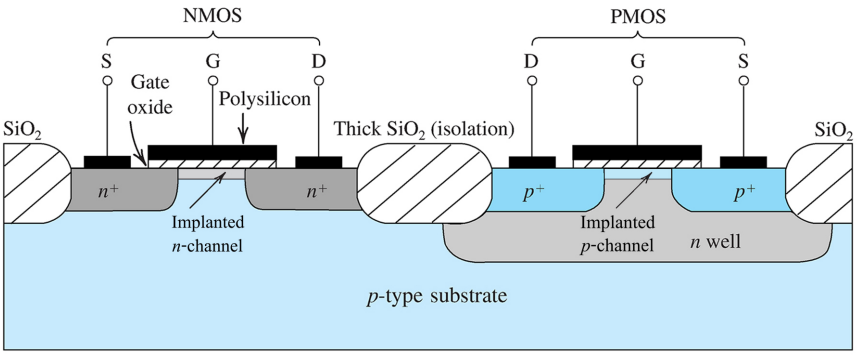

FIGURE 2.3: Cross-section of a depletion-type CMOS integrated circuit [1] (modified).

The main advantage of depletion-type MOSFET is that its drain to source current can be controlled even for negative gate voltage. In other words, an n-channel depletion-type MOSFET has a negative threshold voltage. Similarly, a p-channel depletion-type MOSFET has a positive threshold voltage. Figure 2.4 shows $I_D - V_{GS}$ characteristics for the two types of devices for a very small $|V_{DS}|$.

Applying a negative voltage at gate terminal repels the free electrons from n-channel and thus reduces its conductivity. If the applied negative voltage is sufficient enough, current through the channel from drain to source becomes zero and the device turns off. In this case, negative V_{GS} depletes the channel from its carriers. On the other hand, similar to enhancement NMOS, applying a positive voltage at gate terminal of a depletion NMOS, attracts more electrons into the channel, and consequently enhances the channel. In other words, a depletion-type MOSFET can operate in enhancement-mode or depletion-mode by applying positive V_{GS} or negative V_{GS}, respectively [1, 2].

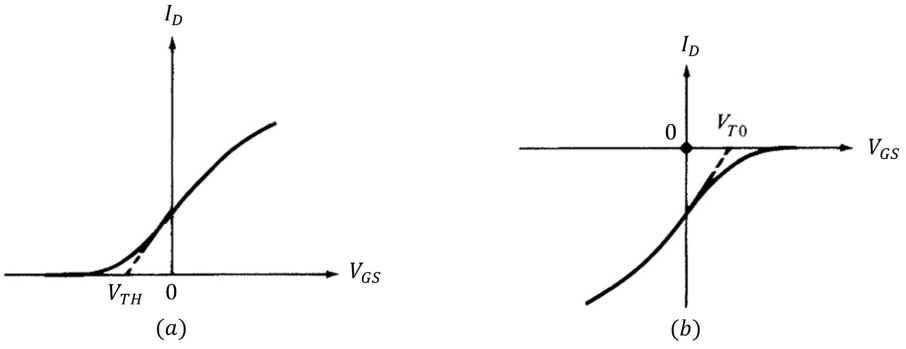

FIGURE 2.4: $I_D - V_{GS}$ characteristic for very small $|V_{DS}|$ and $V_{SB} = 0$ for (a) n-channel depletion device and (b) p-channel depletion device [2] (modified).

Compared to enhancement-type devices, depletion-type devices cost more as they require extra fabrication steps. There is also cheaper structure for fabricating depletion-type devices which requires only one extra mask. In this method, instead of diffusing an n-channel between drain and source, natural silicon (Si) is used to from a conducting n-channel. To do so, an extra mask is used to prevent doping of silicon wafer and thus creation of p-substrate. In other words, instead of forming a transistor on p-substrate, this transistor is fabricated on native silicon wafer (Figure 2.5). This process reduces threshold voltage of MOSFET. For a p-substrate fabrication, this method is only applicable for n-channel devices. Such an n-channel depletion device is usually called native n-channel MOSFET (or native MOSFET).

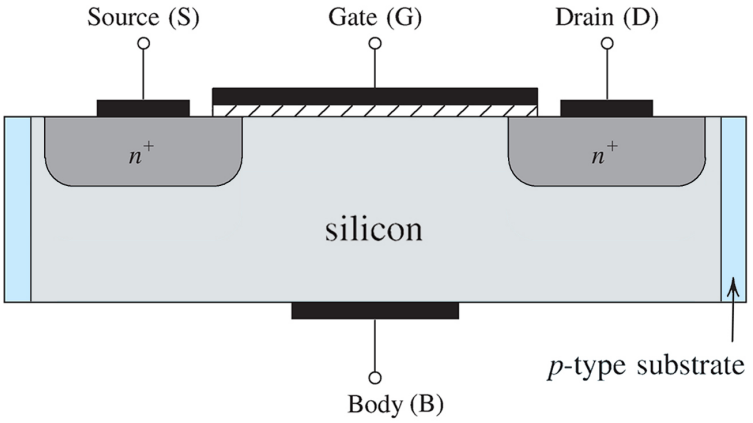

FIGURE 2.5: Cross-section of native n-channel MOSFET

2.2 Performance of CMOS Amplifiers

Some key factors for measuring an op-amp performance include gain, bandwidth, offset, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), ICMR, OVSR, slew rate, noise, and linearity.

2.2.1 Frequency Response

The main objective of an op-amp is to amplify the input signal. The magnitude of amplification (gain) is usually denoted by A. Figure 2.6 shows the circuit symbol of a typical op-amp. If the input signal is sufficiently small, the output voltage (v_o) can be defined by

$$v_o = A(v_i^+ - v_i^-) \tag{2.2}$$

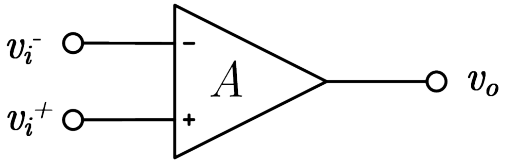

FIGURE 2.6: Circuit symbol of op-amp

There are three different gain expressions for amplifiers: voltage gain, power gain, and current gain [1]. The most commonly used definition to specify an op-amp's gain is voltage gain, which is usually expressed in decibels by

$$\text{Gain} = 20 \log \left(\frac{v_o}{v_i^+ - v_i^-} \right) \tag{2.3}$$

Since Eq.2.3 is independent of input signal frequency, it is considered as DC gain of the amplifier. This gain, for a practical op-amp, is shaped by dominant poles of the amplifier and thus is a function of frequency. The gain and phase of a system is usually represented by Bode plot. As show in Figure 2.7, a Bode plot consists of two subplots: magnitude plot and phase plot. Using Bode plot of an amplifier, it is possible to understand three important specifications of the amplifier: DC gain, -3 dB frequency (also known as 3 dB cutoff frequency), bandwidth, and phase margin.

FIGURE 2.7: Bode plot. (red) magnitude in decibel, (blue) phase in degree.

DC gain is the of amplifier for DC input signal. As the frequency of input signal increases and reaches first dominant pole, the gain of the amplifier starts to decrease by a factor of -20 $dB/decay$. 3 dB cutoff frequency of an amplifier is defined as the frequency at which the gain of amplifier drops by 3 dB below its DC gain. Additionally, the frequency at which the gain of amplifier becomes 0 dB (i.e. unity), is called unity gain bandwidth (UGB) of amplifier. UGB is sometimes referred as bandwidth or gain bandwidth product (GBWP) of the amplifier.

Phase margin plays an important role in defining a system's stability. To calculate the phase margin of an op-amp, its phase at UGB frequency is subtracted from 180°. For an

amplifier operating in feedback configuration, if the PM is zero, oscillation will occur. An amplifier is considered to be stable if its phase margin is about 45°to 60°. An amplifier with a phase margin less than 45°requires frequency compensation to become stable. Although an amplifier with PM of 45°is considered to be stable, to prevent the amplifier from exhibiting ringing, usually a PM greater than 60°is desired.

2.2.2 Offset Voltage

Offset voltage (v_{os}) is another important factor for evaluating an amplifier's performance. If an op-amp operates in a unity gain configuration as shown in Figure 2.8, according to Eq.2.2, the output and input voltages should be equal. However, due to the transistor mismatching, the output voltage differs from the input voltage by an error voltage (v_e) expressed by

$$v_e = v_o - v_i = v_{os} + v_o/A \tag{2.4}$$

where v_{os} is the offset voltage and A is the open-loop DC gain of amplifier. If the open-loop DC gain of amplifier is high enough, then the offset voltage dominates the error. Beside causing error, offset voltage reduces the amplifier's OVSR as well and, thus, degrades the output dynamic range of amplifier.

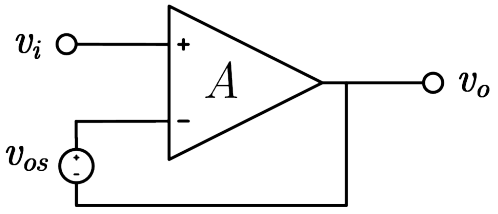

FIGURE 2.8: Unity gain configuration

2.2.3 Common Mode Rejection Ratio

A differential amplifier's task is to amplify differential-mode input signal and reject any common-mode signal. Meaning of the words "differential-mode" and "common-mode" will become clear in Section 2.3. CMRR shows the ability of an amplifier in performing such a task. To calculate the CMRR of an amplifier, we simply divide the differential

gain of amplifier by its common-mode gain:

$$\text{CMRR} = 20\log(\frac{A_d}{A_{cm}}) \tag{2.5}$$

2.2.4 Power Supply Rejection Ratio

Another problem that amplifiers suffer from is the noise or ripple at the power supply being couple to the output signal. Power supply rejection ratio is the ability of an amplifier to prevent the noise or ripple generated by power supply from affecting the output signal. PSRR is measured as the gain of the amplifier from supply rails to its output an is often expressed in decibels.

2.2.5 Input Common Mode Range

ICMR is the range of input voltages that keep the amplifier functioning. Figure 2.9 shows a general CMOS differential amplifier connected to a common-mode input. For this amplifier, all the transistors are required to operate in the saturation region. If we assume $M1$ and $M2$ are perfectly matched (i.e. $V_{TH1} = V_{TH2}$), to keep $M5$ in saturation region, minimum input common-mode voltage (V_{cm_min}) needs to be

$$V_{cm\_min} = V_{OV5} + V_{TH1} \tag{2.6}$$

Similarly, assuming $M3$ and $M4$ are perfectly matched, to keep $M1$, $M2$, $M3$, and $M4$ in the saturation region, maximum common-mode input voltage (V_{cm_max}) is required to be

$$V_{cm\_max} = V_{DD} - V_{OV3} + V_{TH1} \tag{2.7}$$

Hence, for this amplifier, ICMR is defined as

$$V_{OV5} + V_{TH1} < \text{ICMR} < V_{DD} - V_{OV3} + V_{TH1} \tag{2.8}$$

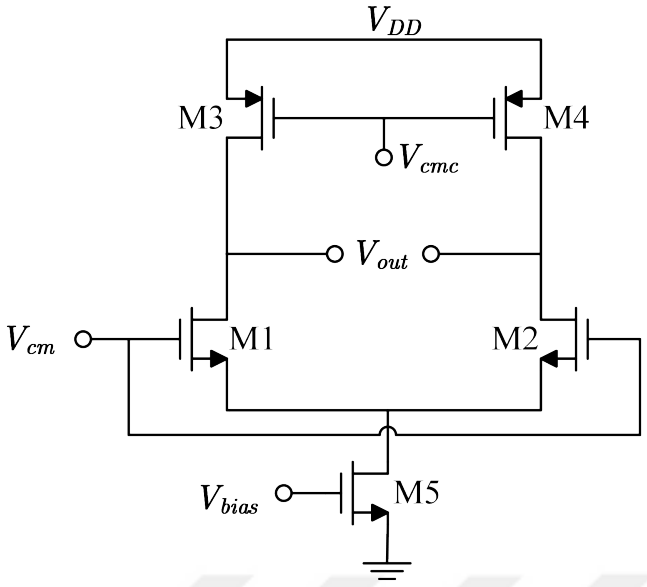

FIGURE 2.9: A general CMOS differential amplifier.

2.2.6 Output Voltage Swing Range

The output voltage swing range (OVSR) defines how far the output of amplifier can reach supply rail or ground. This is the highest peak-to-peak output voltage that the amplifier can deliver without clipping or saturating the output signal. Regarding the amplifier in Figure 2.9, we can write

$$V_{OV5} + V_{OV1} < \text{OVSR} < V_{DD} - V_{OV3} \tag{2.9}$$

2.2.7 Slew Rate

If we connect a capacitive load to the output of the amplifier in Figure 2.9, for large output signals, the maximum rate of charging this capacitor is limited by the DC current of amplifier. This phenomenon is known as slew rate and can cause distortion to the output signal. If we denote the output capacitor and the output DC current by C_L and I_D, respectively, the slew rate of amplifier is defined as Eq.2.10 and is usually specified in units of $V/\mu S$.

$$\text{SR} = \frac{I_D}{C_L} \tag{2.10}$$

2.2.8 Noise

Any unwanted signal or disturbance that is coupled to the desired signal is considered as noise. Noise is a natural phenomenon and it exists in almost every system. Since noise is a random value, its magnitude is expressed by power spectral density (PSD) in units of V^2/Hz or $V/\sqrt{Hz}$. The quality of a signal is measured by signal-to-noise ratio (SNR). SNR compares the power of desired signal to the power of unwanted noise and is expressed in decibels:

$$\text{SNR} = 10 \log \frac{P_{signal}}{P_{noise}} \tag{2.11}$$

There are three main types of noise in electronic components: thermal noise, shot noise, and flicker noise. Thermal noise (also referred as Johnson or Nyquist noise) is generated due to the motion of electrons inside a conductor. This type of noise is white, independent of bias conditions, and proportional to absolute temperature. Shot noise, which exists in pn junctions, occurs due to the fact that DC current is not continuous. The third type of noise, flicker noise, is significantly large in MOS devices. Flicker noise occurs because of the existence of holes in semiconductors. These holes trap the flowing electrons for some time and then release them which in fact results in a noise. Since this type of noise is reversely proportional to frequency, it is also referred as $1/f$ noise.

The noise of a resistor is mainly dominated by its thermal noise. We can model the noise of a resistor by a voltage source or current source with a PSD of $v_n^2(f)$ or $i_n^2(f)$, respectively. For a resistor, $v_n^2(f)$ and $i_n^2(f)$ are expressed by

$$v_n^2(f) = 4kTR \qquad \text{and} \qquad i_n^2(f) = \frac{4kT}{R} \tag{2.12}$$

where k is the Boltzmann's constant ($1.38 \times 10^{-32} J/K$), T is the temperature in Kelvins, and R is the resistance value [24].

MOSFET devices introduce both thermal noise and flicker noise. We can model the thermal noise by a voltage source and the flicker noise by a current source with a PSD of $v_g^2(f)$ and $i_d^2(f)$, respectively, which are defined by

$$v_g^2(f) = \frac{K}{WLC_{ox}f} \qquad \text{and} \qquad i_g^2(f) = 4kT\gamma g_m \tag{2.13}$$

where K is a process dependant parameter. W and L are the width and length of the transistor, respectively. The variables g_m, and C_{ox} represent the transistor's transconductance, and gate capacitance per unit area, respectively. For a long channel device, $\gamma = 2/3$ [24].

2.2.9 Linearity

A system is considered to be linear if we can express its output as a linear function of its input. In practice, op-amps are not linear systems and they suffer from distortion due to the non-linear behavior of circuit components such as transistors. For a memory-less non-linear op-amp, the output of system for any arbitrary input signal, $x(t)$, can be approximated by Eq.2.14. Here we use a third order function for approximation, but higher orders can be used to achieve more accuracy.

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.14}$$

Applying a sine wave to such a non-linear system generates harmonics (integer multiples) of the input frequency. For example, if we apply $x(t) = Acos\omega t$ to the system of Eq.2.14, the output of the system would be

$$\begin{aligned} y(t) &= \alpha_1 Acos(\omega t) + \alpha_2 A^2 cos^2(\omega t) + \alpha_3 A^3 cos^3(\omega t) \\ &= \alpha_1 Acos(\omega t) + \frac{\alpha_2 A^2}{2}(1 + cos2\omega t) + \frac{\alpha_3 A^3}{4}(3cos\omega t + cos3\omega t) \\ &= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})cos\omega t + \frac{\alpha_2 A^2}{2}cos2\omega t + \frac{\alpha_3 A^3}{4}cos3\omega t \end{aligned} \tag{2.15}$$

In the above equation, the first term is a DC shift, the second term is the fundamental, the third term is second order harmonic, and the fourth term is the third order harmonics [25]. The harmonic distortion is defined as the ratio of amplitude of harmonic signal to the amplitude of fundamental. The THD of a system is the square root of sum of squares of all the harmonic distortions. However, since second and third harmonic distortions (HD2 and HD3) are dominant, we usually consider HD2 and HD3 for the THD calculation.

2.3 Topologies for Fully Differential Amplifier

In this section we study two main commonly known design topologies for fully differential amplifier. In electronic circuits, a fully differential amplifier is represented by the schematic model shown in Figure 2.10. Voltages v_i^+, v_i^-, v_o^+, and v_o^- are single-ended voltages meaning they are measured with respect to the ground. The difference between v_i^+ and v_i^- defines differential-mode voltage input (V_{idm}) and the difference between v_o^+ and v_o^- defines differential-mode output voltage (V_{odm}). Additionally, common-mode input and output voltages are defined as shown in Eq. 2.17. An ideal differential amplifier amplifies only V_{idm} and rejects V_{icm} [26].

$$V_{idm} = v_i^+ - v_i^- \qquad V_{odm} = v_o^+ - v_o^- \tag{2.16}$$

$$V_{icm} = \frac{v_i^+ + v_i^-}{2} \qquad V_{ocm} = \frac{v_o^+ + v_o^-}{2} \tag{2.17}$$

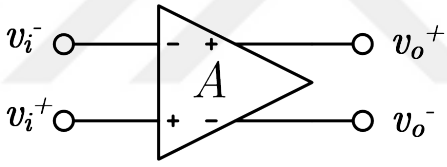

FIGURE 2.10: Fully differential amplifier circuit symbol

Fully differential amplifiers have several advantages over general single-ended amplifiers:

1. Output signal of differential amplifier is less susceptible to noise. The coupled noise to input signal is common to both positive and negative input terminals of the amplifier. Since differential amplifier rejects common-mode input signal, this coupled noise is rejected. As a result, the effect of noise on the output of amplifier is minimized.

2. In a differential amplifier, even order harmonic distortion components are also canceled. As a result, compared to its regular counterpart, a differential amplifier has less distortion and better linearity.

3. Since the output signal of a fully differential amplifier is defined differential, the amplitude of output signal can reach a value twice the amplitude of a single-ended

amplifier's output signal. In other words, the output voltage swing of fully differential amplifier is twice that of single-ended amplifier.

4. Compared to a single-ended amplifier, since the output voltage swing of a fully differential amplifier is larger and its output signal is less affected by noise, the output dynamic range of a fully differential amplifier is larger than a single-ended amplifier.

2.3.1 Fully Differential Two Stage Amplifier

One of the simplest and most elegant architectures for deigning multistage fully differential amplifiers is the one shown in Figure 2.11. The circuit consists of a differential amplifier as the first gain stage and a common-source amplifier with current-source load as the second gain stage. Since this configuration has two dominant pole, compensation is required to ensure the stability of system. Frequency compensation techniques will be studied in details in Section 2.4.

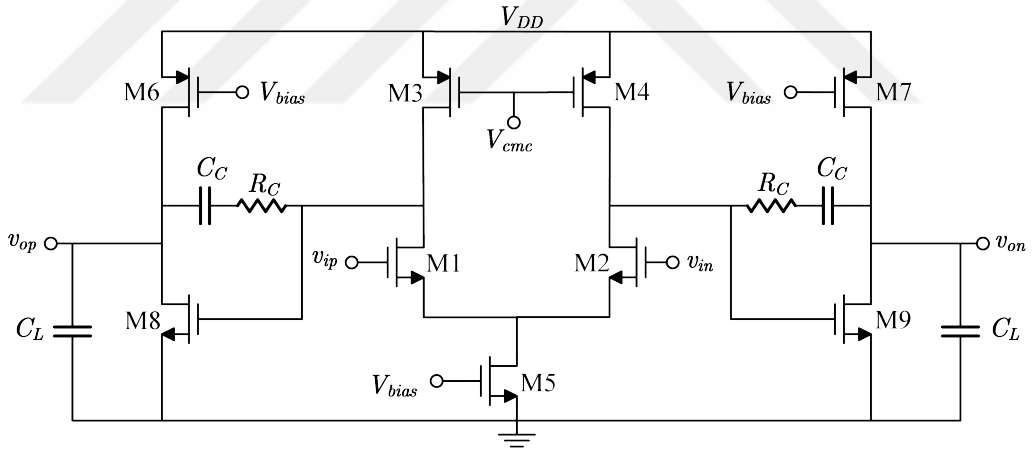

FIGURE 2.11: A CMOS fully differential two stage amplifier

Gain, ICMR, CMRR, OVSR, and frequency components of the op-amp in Figure 2.11 are expressed by Eq.2.18, Eq.2.19, Eq.2.20, Eq.2.21, and Eq.2.22, respectively.

$$\text{Gain} = [-g_{m1}(r_{o1}||r_{o3})][-g_{m8}(r_{o8}||r_{o6})] \tag{2.18}$$

$$V_{OV5} + V_{TH1} < \text{ICMR} < V_{DD} - V_{OV3} + V_{TH1} \tag{2.19}$$

$$\text{CMRR} = [g_{m1}(r_{o1}||r_{o3})][2g_{m3}r_{o5}] \tag{2.20}$$

$$V_{OV9} < \text{OVSR} < V_{DD} - V_{OV7} \tag{2.21}$$

$$\begin{aligned} f_{p1} &= \frac{1}{2\pi R_1 g_{m8} R_2 C_C} \qquad f_{p2} = \frac{g_{m8}}{2\pi C} \qquad f_z = \frac{g_{m8}}{2\pi C_C} \\ R_1 &= r_{o1}||r_{o3} \qquad R_2 = r_{o8}||r_{o6} \qquad C = C_{db8} + C_{db6} + C_{gd6} + C_L \end{aligned} \tag{2.22}$$

2.3.2 Fully Differential Folded Cascode Amplifier

Folded cascode amplifier is the most popular single state amplifier. Figure 2.12 shows the structure of a typical fully differential folded cascode amplifier. Here, $M1$ and $M2$ form the input differential pair, and $M5$ and $M6$ are the cascode transistors. Folded cascode architecture uses cascode transistors in the output branch to increase the output impedance of the amplifier and thus achieve more gain. Note that since the amplifier has only one dominant pole, it's naturally stable and does not require compensation.

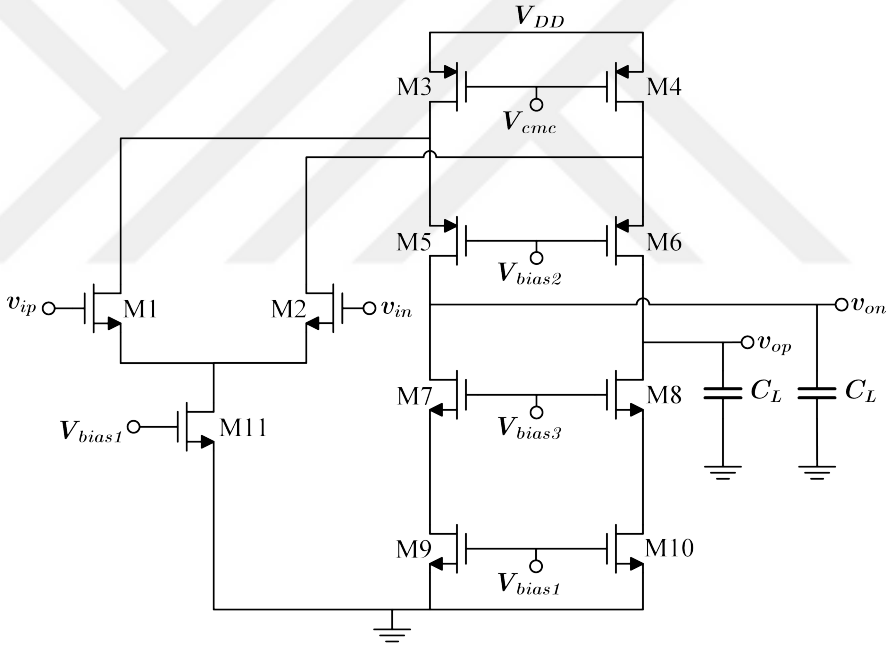

FIGURE 2.12: A CMOS fully differential folded cascode amplifier

Gain, ICMR, OVSR, and frequency components of the op-amp in Figure 2.12 are expressed by Eq.2.23, Eq.2.24, Eq.2.25, and Eq.2.26, respectively.

$$\text{Gain} = g_{m1}\{[g_{m5} r_{o5}(r_{o1}||r_{o3})]||(g_{m7} r_{o7} r_{o9})\} \tag{2.23}$$

$$V_{OV11} + V_{TH1} < \text{ICMR} < V_{DD} - V_{OV3} + V_{TH1} \tag{2.24}$$

$$V_{OV9} + V_{OV7} < \text{OVSR} < V_{DD} - V_{OV3} - V_{OV5} \tag{2.25}$$

$$f_{p1} = \frac{1}{2\pi C_L R_o}$$
$$R_o = [g_{m5} r_{o5} (r_{o1} || r_{o3})] || (g_{m7} r_{o7} r_{o9}) \tag{2.26}$$

Compared to two stage op-amp, folded cascode amplifier has better PSRR since there is no pole splitting. Additionally, since its non-dominant poles are near unity gain frequency, folded cascode is faster than two stage op-amp. Finally, since folded cascode amplifier does not require compensation, the capacitive loading does not rely on compensation capacitor. Hence, contrary to two stage amplifier, the load capacitance of a folded cascode amplifier is not limited. But the two stage architecture has other advantages such as better noise performance and larger OVSR [27].

2.4 Frequency Compensation

Operational amplifiers are mostly designed to operate under the feedback configuration. As a result of having single dominant pole, single stage amplifiers are considered to be naturally stable and achieve a PM of 90°. However, due to having multiple poles, multiple stage amplifiers suffer from closed-loop stability. A two stage amplifier may achieve a phase angle of 180°before the unity gain frequency. In this case, if we connect the amplifier to a feedback circuit, it will start to oscillate because of having a PM of 0°. To achieve a PM of at least 45°and ensure the stability of op-amp, altering the amplifier circuit is required to manipulate the poles of amplifier and thus increase the PM. This process is known as frequency compensation [4]. There are various techniques for frequency compensation but the most straightforward way is to introduce a dominant pole at a frequency lower than the UGF and to make the gain drop faster and reach the unity gain before the phase angle reaches -180°.

2.4.1 Pole Splitting Miller Compensation

Miller compensation is the most common frequency compensation technique used in very-large-scale integration (VLSI) designs. This useful technique, which is base on Miller's theorem, is illustrated in Figure 2.13. By using Miller's theorem, we can split the compensating capacitor C_C into two separate capacitors: one connected to the input terminal (C_1) and the other one connected to the output terminal of second gain stage

(C_2). The capacitors C_1 and C_2 introduce a pair of dominant and non-dominant poles, respectively.

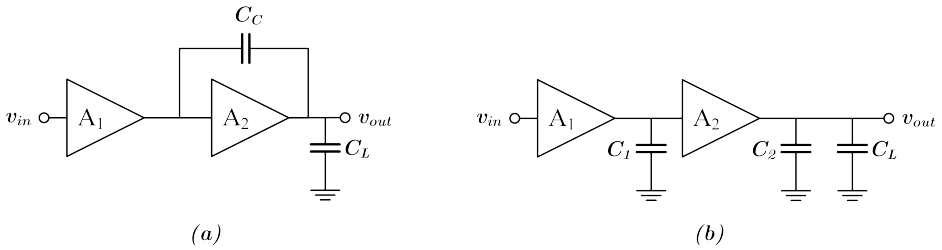

FIGURE 2.13: Miller compensation technique: (a) actual circuit, (b) Miller equivalent circuit.

According to Miller's theorem $C_1 = C_C(1-A_2)$ and $C_2 = C_C(1-\frac{1}{A_2})$. Hence, increasing the gain of second stage, moves the dominant pole to a lower frequency while shifting the non-dominant pole to a higher frequency. Since in a two stage amplifier A_2 is usually large, the dominant pole introduced by C_1 is smaller than unity gain frequency and therefore, makes the gain drop faster to increase the PM. The disadvantage of this technique is that it reduces the bandwidth of the amplifier. Another drawback is that it introduces a right half plane (RHP) causing a negative phase shift. Consequently, it reduces the closed-loop stability of the op-amp. To cancel this RHP zero, a resistor is connected in series with the compensation capacitor [1].

2.4.2 Active Compensation

Active-feedback frequency-compensation (AFFC) is another compensation technique which can overcome the problem of bandwidth reduction while ensuring the stability of op-amp. Figure 2.14 shows the basic structure of an AFFC amplifier. As it is obvious from its name, contrary to Miller compensation which uses passive-capacitive-feedback, this technique utilizes active-capacitive-feedback for compensation. Another advantage of this technique is that, unlike Miller compensation, active compensation does not introduce any RHP zero.

A basic AFFC amplifier consists of three main blocks: input block, high-gain block (HGB), and high-speed block (HSB). The HSB itself consists of a feedforward stage (FFS) and a feedback stage (FBS) connected in series with a compensation capacitor C_a. The location of the non-dominant poles and the bandwidth of the amplifier is controlled by HSB.

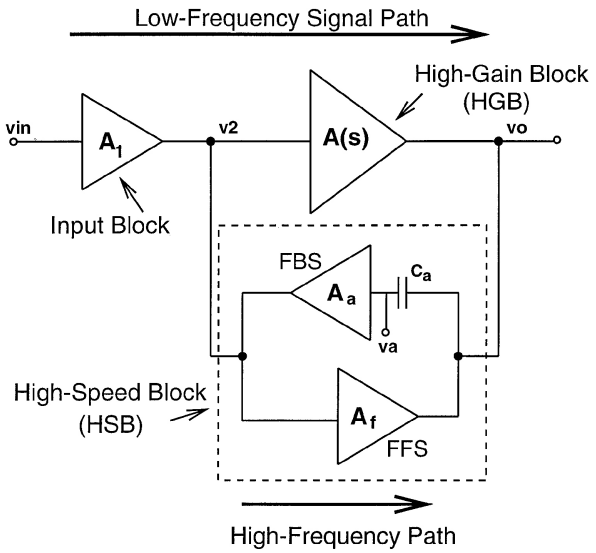

FIGURE 2.14: Basic structure of an AFFC amplifier [3].

At high frequencies, any change in the output signal will be directly sensed at the input terminal of FBS. This signal is then amplified by FBS and directed to the output terminal of the input stage. Afterwards, this amplified feedback signal is feedforwarded to the output again, through the FFS. This process reduces the original output signal change and, therefore, enhances the bandwidth of AFFC amplifier [3].

2.5 Common Mode Feedback

Consider the single-stage fully differential amplifier of Figure 2.15. Here, the operating points must be set to values that make $M1$-$M5$ operate in the saturation region. At the same time, we need to set the DC common-mode output voltage (V_{ocm}) to the value that maximizes the output swing. However, since the output terminal is a high impedance node, V_{ocm} is very sensitive to mismatches in the transistors. Additionally, setting V_{ocm} to a desired value is not possible because I_{D5} and $|I_{D3}| + |I_{D4}|$ are set independently from each other.

For setting V_{ocm} to a desired DC voltage $V_{desired}$ that maximizes the output swing and ensures all transistors operate in saturation region, we must adjust V_{SG3} and V_{SG4} so that $I_{D5} = |I_{D3}| + |I_{D4}|$. To achieve such a goal, a negative feedback loop is required to adjust V_{cmc} to set $V_{ocm} = V_{desired}$. Such a feedback loop is refereed as common-mode feedback (CMFB) loop [4].

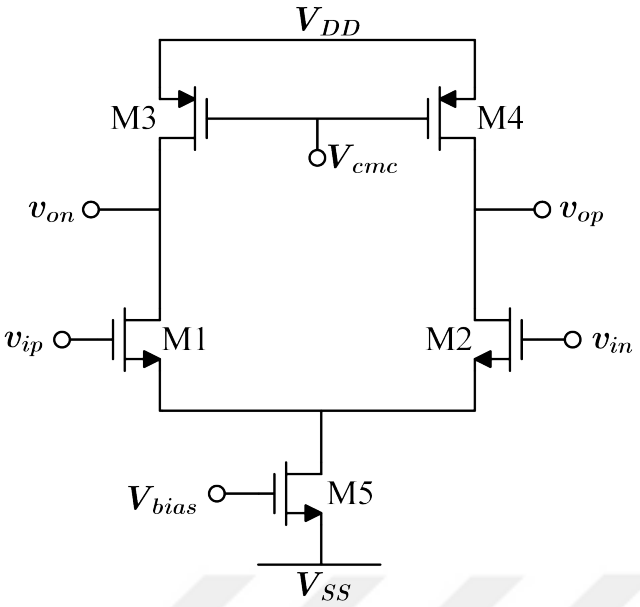

FIGURE 2.15: A typical, single-stage, fully differential amplifier [4] (modified).

2.6 Output Stages

The loads connected to the output of op-amps usually have low resistance and high capacitance. To drive a low resistance load properly, an op-amp is required to have low output impedance. However, to achieve a high gain, the output impedance of op-amp is generally designed to be as high as possible. Also, to drive high-capacitance load, the amplifier is required to provide large current. To overcome this problem, an output amplifier (or commonly known as output stage) is cascaded to the output of amplifier. If a sinusoidal wave is applied to the input of output amplifier, the portion of the cycle that output stage conducts current is called the conduction angle. Output stages are classified according to their conduction angle.

2.6.1 Class A Output Stage

Figure 2.16 shows a class A amplifier and its output current waveform. Class A amplifier is biased at a current I_D which is larger than the peak current of output signal, i_d. Hence, a class A amplifier conducts current for the full period of input signal. For this reason, the conduction angle of class A amplifier is considered to be 360°. Here, class A amplifier is implemented with common-source amplifier. It is possible to implement class A amplifier using common-drain amplifier (source follower).

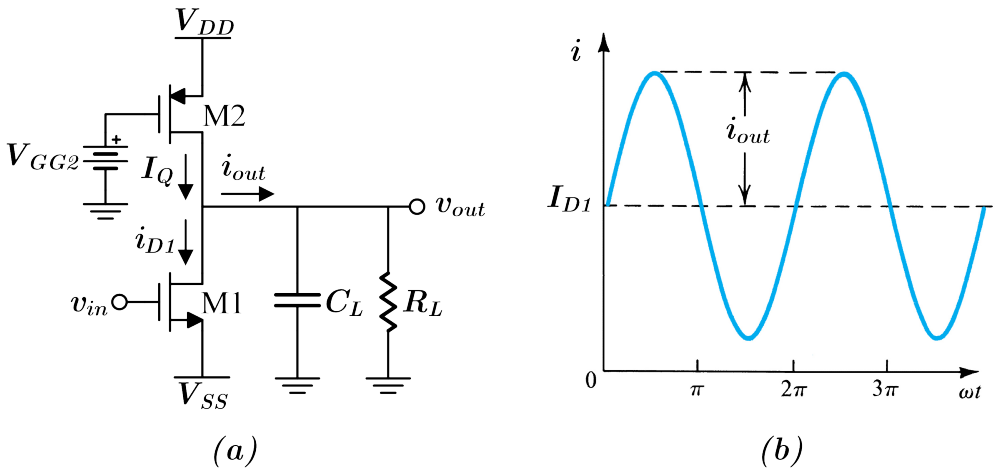

FIGURE 2.16: (a) Class A amplifier. (b) Output current waveform.

The efficiency of class A amplifier is expressed by

$$\begin{aligned}\text{Efficiency} &= \frac{P_{R_L}}{P_{Supply}} = \frac{\frac{v^2_{out(peak)}}{2R_L}}{(V_{DD}-V_{SS})I_Q} = \frac{\frac{v^2_{out(peak)}}{2R_L}}{(V_{DD}-V_{SS})(\frac{V_{DD}-V_{SS}}{2R_L})} \\ &= (\frac{v_{out(peak)}}{V_{DD}-V_{SS}})^2\end{aligned} \tag{2.27}$$

Maximum efficiency is achieved when $v_{out(peak)} = V_{DD} = |V_{SS}|$ which gives 25%. Therefore, class A amplifiers suffer from poor efficiency.

2.6.2 Class B Output Stage

Figure 2.17 shows a class B amplifier and the drain current waveform of one of its two transistors. Class B amplifiers are also known as push-pull amplifiers. Class B amplifier is biased at zero DC current. Hence, in a class B amplifier, a transistor conducts current for only half of the period of input signal. For this reason, the conduction angle of class B amplifier is considered to be 180°. The negative half of the output signal is generated by the other transistor. Combination of these two currents results in a full sine wave at the output terminal of the class B amplifier. Here, class B amplifier is implemented with common-source amplifier. It is possible to implement class B amplifier using common-drain amplifier (source follower).

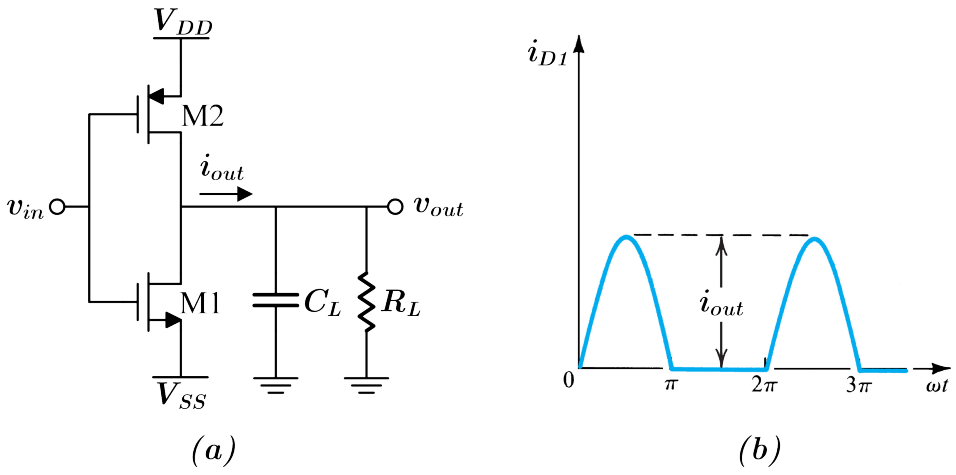

FIGURE 2.17: (a) Class B amplifier. (b) Drain current waveform of single transistor.

The efficiency of class B amplifier is expressed by

$$\text{Efficiency} = \frac{P_{R_L}}{P_{Supply}} = \frac{\frac{v_{out(peak)}^2}{2R_L}}{(V_{DD} - V_{SS})(\frac{1}{2})(\frac{2v_{out(peak)}}{\pi R_L})} = \frac{\pi}{2}\frac{v_{out(peak)}}{V_{DD} - V_{SS}} \tag{2.28}$$

Maximum efficiency is achieved when $v_{out(peak)} = V_{DD} = |V_{SS}|$ which gives 78.5%. Class B amplifiers attain a good efficiency but their drawback is that at crossover points, both transistors may turn off and zero conduction may occur. This fact may lead to distortion at the output signal. To overcome this problem, class AB amplifiers are introduced.

2.6.3 Class AB Output Stage

Figure 2.18 shows a class AB amplifier and the drain current waveform of one of its two transistors. Class AB amplifiers are also known as push-pull amplifiers. In class AB amplifier, the transistors are biased at nonzero DC current slightly larger than zero and much smaller than the peak current of output signal. Hence, a transistor in a class AB amplifier conducts current for slightly larger than half of the period of input signal. For this reason, the conduction angle of class B amplifier is considered to be larger than 180°but much smaller than 360°. This way of biasing prevents the transistors from turning off at crossover points. Similar to class B amplifiers, the negative half of the output signal is generated by the other transistor. Just like class B amplifiers, it is possible to implement class AB amplifier using common-drain transistors (source

follower). Since class AB amplifiers are intermediate class between A and B, depending on their conduction angle, their maximum efficiency is between 25% and 78.5%.

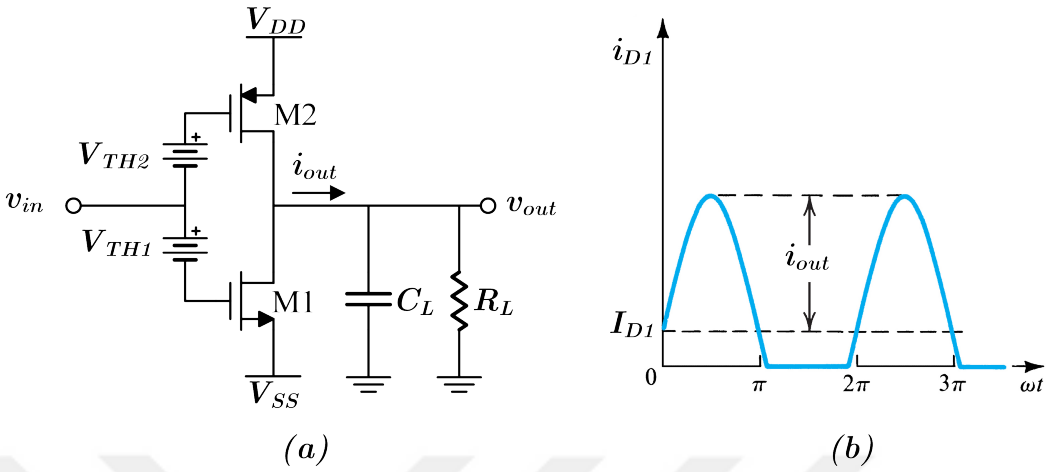

FIGURE 2.18: (a) Class AB amplifier. (b) Drain current waveform of single transistor.

2.7 Gain Boosting

In analog circuit design, cascode is often used to increase the gain of amplifiers. A cascode is combining a common-source (CS) transistor with a common-gate (CG) transistor. To further increase the gain, we can cascode more transistors in a stack. Unfortunately, since each cascode transistor will reduce the OVSR by a factor of V_{ov}, this cannot be an optimal solution for the application for which the OVSR is the biggest concern. To overcome this problem, gain boosting techniques are introduced.

2.7.1 Normal Cascode Circuit

Cascoding is connecting a CG transistor to the output of a CS amplifying transistor to provide current buffering. Figure 2.19 illustrates the cascoding technique. The cascode circuit has two advantages over normal CS configuration. First, it increases the output impedance of the amplifier which leads to a higher gain. The output impedance of cascode circuit is

$$R_o = r_{o1} + (1 + g_{m2}r_{o1})r_{o2} \approx g_{m2}r_{o1}r_{o2} \tag{2.29}$$

which implies that the output impedance of CS amplifier is increased by a factor of $g_{m2}r_{o2}$. Since the gain of amplifier is calculated by multiplication of its transconductance and output impedance, an increase in the output impedance directly increases the gain.

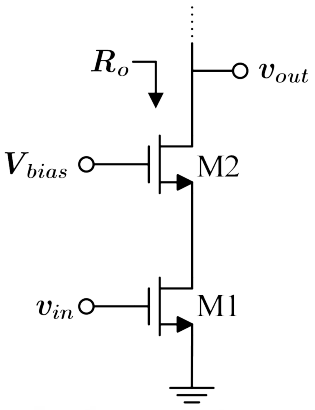

FIGURE 2.19: Simple cascode circuit.

The second advantage is that it reduces the input capacitance of the amplifier which results in a better frequency response. The impedance seen by the gate-drain capacitance of $M1$, $Cgd1$, is approximately $1/g_{m2}$ which is very small. As a result, the gain from the input node to the output node of $M1$ is small. Thus by applying the Miller theorem, the effective $Cgd1$ seen by the input signal is very small, compared to a normal CS.

2.7.2 Regulated Cascode Circuit

The main purpose of gain boosting is to increase the output impedance without cascoding more devices and sacrificing the OVSR. Figure 2.20 shows a regulated (gain boosted) cascode circuit.

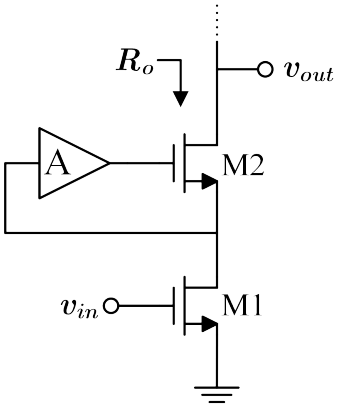

FIGURE 2.20: Regulated (gain-boosted) cascode circuit.

The output impedance of this cascode circuit is

$$R_o = r_{o1} + (1 + g_{m2}Ar_{o1})r_{o2} \approx g_{m2}Ar_{o1}r_{o2} \tag{2.30}$$

Eq.2.30 shows that, compared to a normal cascode device, the output impedance of gain-boosted cascode is increased by the gain of feedback amplifier, A. So, by adjusting the value of A, it is possible to further increase the gain of amplifier without cascoding extra transistors. The feedback amplifier controls the drain voltage of $M1$ by adjusting the gate voltage of $M2$. Therefore, it minimizes the effect of variations in the drain current on the drain voltage of $M1$.

Chapter 3

Literature Review

In the design of amplifiers, rail to rail input and output topologies are introduced to achieve wide ICMR. The method of rail to rail input is mostly about preserving a constant input transconductance throughout the ICMR. Usually a class AB push pull stage is used to a provide rail to rail output. However, to obtain rail to rail input, different solutions have been introduced. In this section, we will review some of the most important and fundamental rail to rail implementation.

In the literature, particular methods have been used with the aim of maintaining an almost constant g_m throughout the entire ICMR [5–22]. Most of these configurations utilize complementary differential input pair which consists of an NMOS and a PMOS input pair. The problem with these implementations is that the value of the g_m at the center of ICMR is twice its value when the input common mode voltage (V_{icm}) is near the supply rails. The reason is the existence of a big overlap region where both NMOS and PMOS input pairs are active. This g_m variation results in important disadvantages such as DC gain variation, bandwidth variation, variable slew rate, and compensation problems [8, 9, 11, 13, 18, 19].

One of the solutions to overcome the problem of g_m variation complementary input pair implementations to use current switches for increasing or decreasing the tail current in order to stabilize gm throughout the entire ICMR. In this method, for the region where only one pair of the complementary pair is active, the tail current is increased by four times compared to the region in which both of the input pairs are active. This fact introduces a moderately constant g_m over the ICMR. Eq.3.1 explains the reason we need

to increase the tail current by a factor of four. According to Eq.3.1, for doubling the g_m we need to quadruple the drain current. When V_{icm} is close to supply rails, increasing the tail current by a factor of four, doubles the g_m. As a result, this method would efficiently produce a constant g_m for the entire ICMR.

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \tag{3.1}$$

Level shifting is another introduced technique for stabilizing g_m [7]. In this method, by using the DC level shifters, the DC bias points of p-channel and/or n-channel input pair are shifted to overlap in a way that the overall g_m of the amplifier remains constant. Alternatively, a dual n-channel input pair is employed in [8] in preference to a p-channel and n-channel complementary input pair. A single input pair along with the DC level shifters are used in order to move up the common mode voltage so that the input pair still remains active for V_{icm} values close to negative supply voltage. The same method has been used in [9, 19].

[18] noted that various guidelines must be followed for the implementation of constant g_m circuits. Initially, we need to keep the large and small-signal performances of the amplifier constant regardless of the alterations in the common-mode. Next, we should make sure that our implementation is universal and robust, i.e., the accuracy of implementation is independent of a particular model or exact match requirements. We will review [5–9] deeper to investigate how well these designs fit into these requirements and possible design constraints and we will investigate the possible restrictions of their deigns.

3.1 Complementary Input Pair

Using complementary input pair is the most common method to achieve rail to rail operation. In [5], they discussed about the implementation of a complementary input pair in order to attain a rail to rail input. To minimize the g_m variation over ICMR, a g_m control circuit is introduced. Although is has been reported that the g_m control circuit can be implemented using zener diode, because of the complexity of the feedback loop, they have utilized a current switching circuit to control the g_m. Figure 3.1 illustrates the schematic of complementary input stage and the current switching circuit.

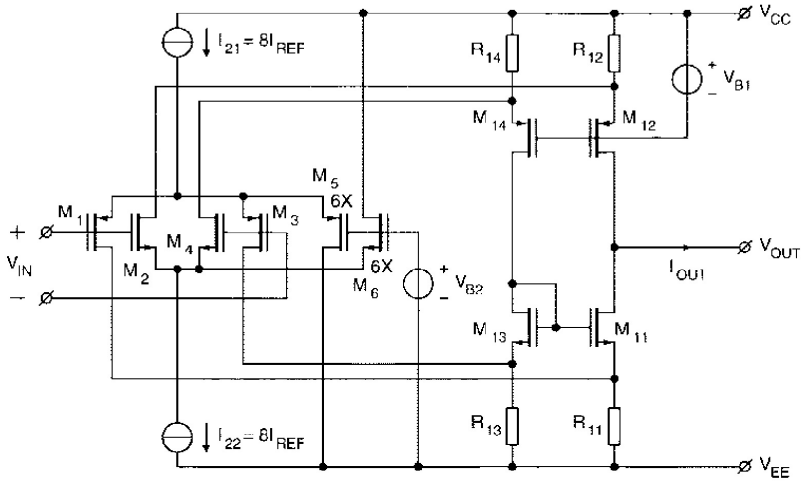

FIGURE 3.1: Complementary input stage with current switching g_m control circuit [5]

In Figure 3.1, $M5$ and $M6$ control the tail current of PMOS and NMOS input pair, respectively. When V_{icm} is in the middle of ICMR, $M5$ sinks some portion of the tail current of PMOS input pair ($M1$ and $M3$). Similarly, $M6$ drains some portion of the tail current of NMOS input pair ($M2$ and $M4$). When the V_{icm} is high, the NMOS input pair is active and PMOS input pair is off. In this case all the tail current of PMOS pair passes through $M5$. Similarly, for low V_{icm} values, the PMOS input pair is active and NMOS input pair is off. In this case $M6$ drain all the til current of NMOS pair. When the V_{icm} is equal to V_{B2}, the tail currents of input pairs are halved, i.e. the current switching transistors consume three-fourths of the current. Hence, the current through the input pair is reduced by a factor of four and the g_m is halved accordingly.

The problem with this implementation is that the accuracy of the model is strongly dependant on the proper matching between NMOS and PMOS input pair. Also using current switches suggests that a particular model is used for keeping g_m constant. This implementation changes the tail current of the input pair by relying on the square model shown in Eq.3.1. However, this model neglects the channel length modulation effect and is not accurate. These two problems might result in some some deviations after the fabrication. [5] reports the g_m variation to be 5%.

Another problem with this method of implementation is that at different input common mode voltages different pair will be functioning. This problem leads to the dependence of offset voltage of the amplifier on V_{icm}.

3.2 Complementary Input Pair with Dummy Input

In [6], the explanation of another implementation is presented for achieving a rail to rail input stage. The idea is employing the implementation of complementary input pairs, but a different method is proposed to maintain a constant g_m over ICMR. In this design, the same idea of changing the tail current is used, but rather than employing current switches, two dummy input pairs are utilized for changing the tail current. Figure 3.2 illustrates the input stage employed in [6].

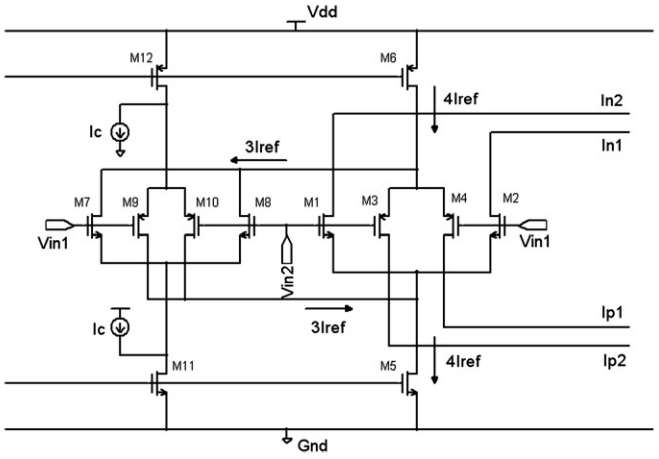

FIGURE 3.2: Complementary input stage with dummy input pair [6]

In this figure, besides the input pair, the exist a NMOS and a PMOS dummy pair connected to the tail current source of actual PMOS and NMOS input pair, respectively. The main purpose of using these dummy pairs is to reduce the tail current of actual input pairs when the V_{icm} is in the mid range of ICMR. When the V_{icm} is close to the supply rails, the dummy pair has no effect on the system. But when the V_{icm} is in the mid range, the dummy pair drains 75% of the tail current and minimizes the g_m variation.

The conclusions drawn from [6] explain that, compared to [5], g_m variation is better. But to keep the g_m constant, the geometry aspect ratio of complementary input pair must follow Eq.3.2. Since μ_n and μ_p does not follow the same variation with respect to temperature, the g_m accuracy has a strong dependence on temperature.

$$\frac{\mu_n}{\mu_p} = \frac{(W/L)_p}{(W/L)_n} \tag{3.2}$$

3.3 Complementary Input Pair with Overlapped Regions

So far, in order to provide a constant g_m, researchers utilize variation of the tail current source of complementary input pairs. However, to achieve this aim, another implementation of complementary inputs was performed in [7]. Figure 3.3 shows the schematic of complementary input pair proposed by [7]. They suggested that by shifting the transition regions of the complementary inputs there is no need for changing the tail current to attain a constant g_m.

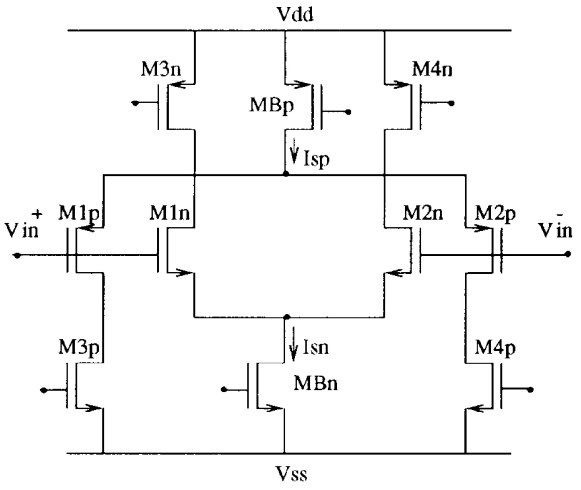

FIGURE 3.3: Complementary input stage with overlapping [7]

Figure 3.4 shows the usual transition regions of a complementary input. As shown in this figure, NMOS pair and PMOS pair overlap in the mid range of ICMR. Hence, the problem of g_m becoming double in the mid range rises which necessitates the reduction of the tail current in the middle of ICMR. In [7], they proposed that by designing the transition regions such that they overlap at the right point, the need for compensating the circuit in the regions where both of the input pairs are active would no longer be needed. This ideal is illustrated in Figure 3.5, where the PMOS pair transition region is moved in order to overlap with the NMOS pair transition region to prevent doubling the g_m in mid range of ICMR.

For shifting the transition regions, source followers are used as a level shifter. The transition region is determined by the aspect ratio and drain current of the level shift circuit. The correct sizing for optimal shift in the transition region is very important in this design because any incorrect sizing would result in g_m variation.

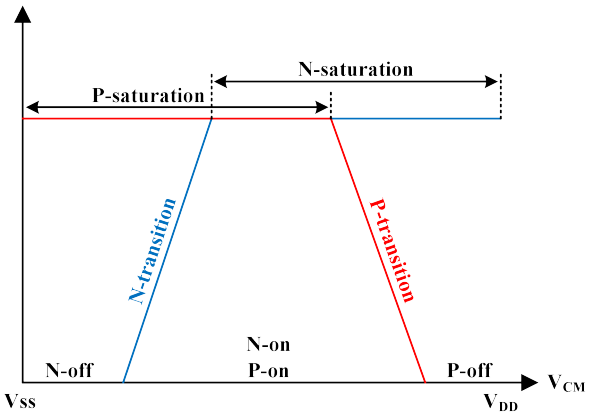

FIGURE 3.4: Typical complementary input transition region (modified) [7]

Another problem with this design is that, similar to [6], it requires strict matching between NMOS and PMOS transistors, as any mismatch would result in change of transition slope. Although the idea of employing level shifters for achieving a rail to rail input was initially proposed in [7], for improving this idea, the problems occurred in complementary pair input implementations are resolved in [8, 9, 19].

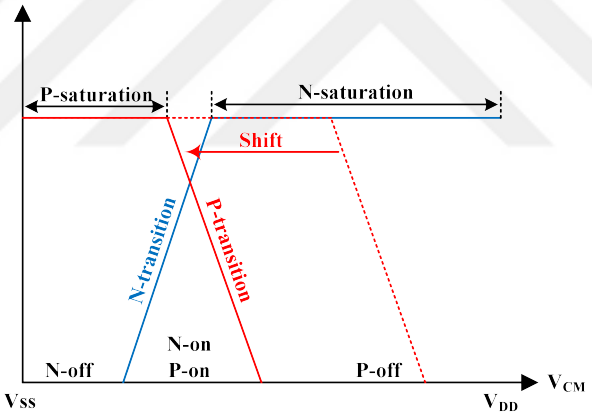

FIGURE 3.5: Shifted complementary input transition region (modified) [7]

3.4 Dual n-channel Input Pair

As mentioned in [8], by using level shifters there is no need to use complementary input pair to maintain a constant g_m over the ICMR. Also [8] reports that instead of using a complementary input pair, dual NMOS (dual n-channel) transistors can be used for achieving rail to rail operation. It suggests that by using dual n-channel input pair the the issue of restrict matching in [5–7] is no longer troublesome because in this implementation the matching needs to be done between two NMOS pair. Compared to matching NMOS

transistors with PMOS transistors, matching between NMOS transistors can be easily achieved.

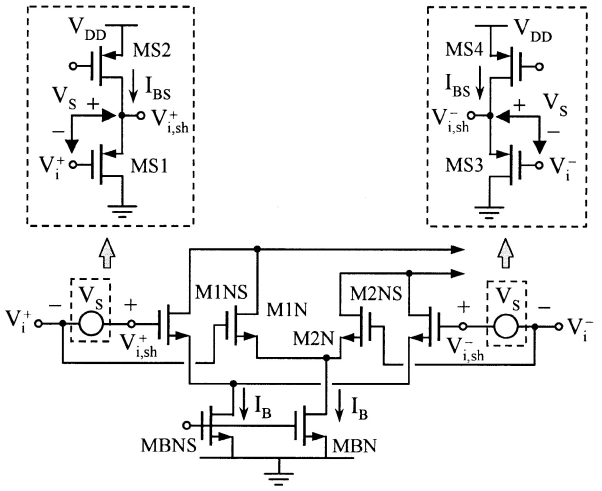

FIGURE 3.6: Dual n-channel input pair [8]

In Figure 3.6, a two n-channel input pairs is displayed, in which one of them is connected to a level shifter. The level shifter increases the V_{icm} at one of the input pairs, which helps one input pair to stay active while the V_{icm} approaches the negative supply voltage. However, while the V_{icm} approaches the positive supply voltage, the level shifter enters into the triode region, which results in disabling the input pair connected to the level shifter. Therefore, just one input pair would be differentially active when V_{icm} is near the supply rails. On the other hand, in the middle of the ICMR, all input pairs are going to be active and the differential g_m would be doubled. Consequently, in order to attain a constant g_m over the entire ICMR, a canceling circuit is required.

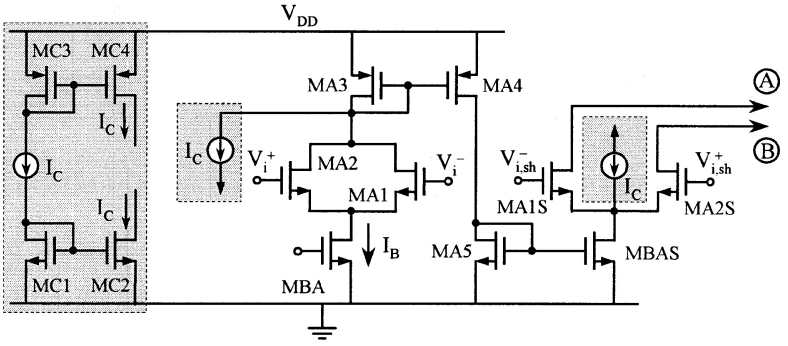

FIGURE 3.7: cancellation circuit [8]

Figure 3.7 shows the cancellation circuit used in [8] for maintaining a constant g_m. The circuit consists of a differential pair that are cross-connected to the drains of input pair

in Figure 3.6 to cancel the differential g_m of the input stage. Furthermore, the emphasis on the differential g_m in [8], is because of the common-mode gm not being constant.

3.5 Dual p-channel Input Pair

The use of level shifters to attain rail to rail operation by implementing dual channel input pair is applicable to n-channel transistors as well. [9] presents a dual p-channel input pair to attain a rail to rail input. As shown in Figure 3.8, they use level shifters on both input pairs to maintain a constant gain over the ICMR. In this design they use a sensing circuit instead of cancellation circuit. The purpose of using sensing circuit is to maintain a constant tail current regardless of the region of V_{icm}.

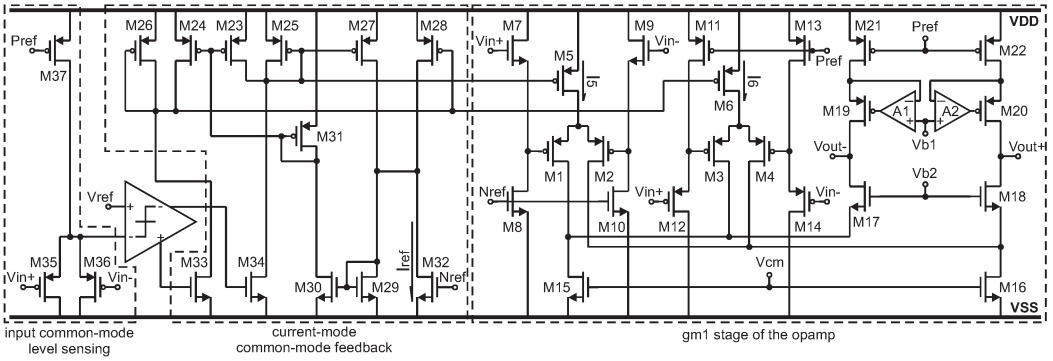

FIGURE 3.8: Dual p-channel input pair [9]

A fully differential comparator is used in the sensing circuit. The level of the input signal is sensed and compared to a reference voltage (V_{ref}) to control the currents of input pairs and maintain a constant g_m for all the values of V_{icm}. The transition point between the two pair is determined by V_{ref} and the slope of transition depends on the gain of comparator.

Chapter 4

Wide ICMR Fully Differential Amplifier Design

4.1 Proposed Design

For high accuracy applications, op-amps with high-accuracy settling time, small rise time, and small overshoot is required which brings up the necessity of having a high DC gain. Additionally, if the amplifier is supposed to operate in a feedback configuration, as the DC gain of the amplifier increases, the error between the overall gain of feedback circuit and the feedback factor decreases. Moreover, high OVSR and minimal noise are other important factors to make an op-amp suitable for high resolution applications.

To achieve wide ICMR, many rail to rail solutions have been addressed but they all suffer from transconductance (g_m) variations. A constant g_m is one of the key factors in defining an amplifier's linearity. Also, most of rail to rail designs are complex and occupy more area. For the applications that does not require an amplifier with a rail to rail input but with a wide ICMR, there needs to be a better solution with less complexity and smaller g_m variation. In this regard, we propose a folded cascode amplifier with native input transistors. As discussed in Section 2.1.2, by having a negative threshold voltage, native transistors are capable of operating even with negative gate voltage. According to Eq.2.24, the ICMR of a folded cascode amplifier is limited by the threshold voltage of input transistor. Hence, having a negative threshold voltage improves the ICMR of the amplifier.

4.2 Design Specifications

Figure 4.1 illustrates a detailed block diagram of the application of our proposed amplifier. Operating in a unity gain feedback configuration, the amplifier will receive an input signal with 1.65 V DC voltage and 2.2 peak-to-peak (V_{pp}) AC voltage magnitude. It will convert the input signal to a differential signal with common mode DC voltage of 1.65 V and differential AC magnitude of 2.2 V_{pp}. Since the amplifier will drive a 14-bit ADC, strong linearity and high output dynamic range are the the most important factors in designing the amplifier.

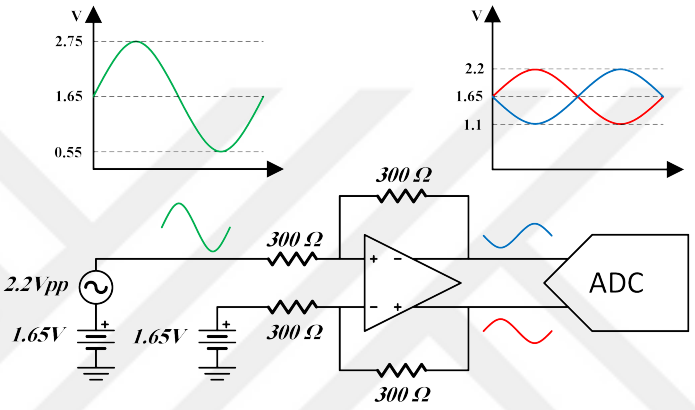

FIGURE 4.1: Detailed block diagram of proposed amplifier's application.

Target Design specifications are calculated as:

- A DC gain of at least 120 dB is required to minimize the error in the feedback gain.
- A unity gain bandwidth of 200 MHz is desired for fast response of the amplifier to the input signal.
- A phase margin of at least 60°is desired to prevent the output of amplifier from ringing.
- The output dynamic range of amplifier is required to be greater than 86 dB in order not to limit the ENOB of ADC.
- The THD of the amplifier must be less than -86 dB, otherwise the ENOB of the ADC will be determined by the pre-amlifier.

- To increase the output dynamic range of the amplifier, the OVSR is required to be rail to rail.

- The output dynamic range (DR) of an amplifier is calculated by

$$\mathrm{DR} = 10\log\frac{P_{signal}}{P_{noise}} = 10\log\frac{V^2_{pp(signal)}}{V^2_{noise}} \tag{4.1}$$

  Since the OVSR is rail to rail the noise of amplifier defines the DR of amplifier. According to Eq.4.1, to obtain a DR of 86 dB, the maximum noise of amplifier is required to be 165 μV at 5 MHz.

- To achieve a good noise figure, a large CMRR is required in order to reject the common mode input noise. Here, we define a minimum CMRR of 100 dB.

- For a sinusoidal input at frequency of f_0 and peak voltage of v_p, to have a distortion free operation, the minimum slew rate of amplifier is calculated by $SR = 2\pi f_0 v_p$. Since the frequency of the input signal to our amplifier is 5 MHz and the peak voltage of sinusoidal is 2.75, the minimum slew rate is required to be 87 $V/\mu s$ to minimize the distortion.

Table 4.1 summarizes the target design specification.

TABLE 4.1: Summary of target specifications for the proposed design

Specification	Target Value
DC gain	$\geq 120dB$
UGBW	$200MHz$
Phase margin	$\geq 60^\circ$
Output dynamic range	$\geq 86dB$
THD	$\leq -86dB$
OVSR	$3.3V_{pp}$
CMRR @ $5MHz$	$\geq 100dB$
Slew rate	$\geq 87V/\mu s$
Total Integrated Noise @ $5MHz$	$\leq 165\mu V$
Load capacitance	$4pF$ (differential)
Supply voltage	$3.3V$

4.3 Fully Differential Folded Cascode Amplifier

4.3.1 Bias Circuit

The first step in designing an amplifier is to design a bias circuit to provide proper biasing voltages for our transistors. Figure 4.2 shows the wide swing bias circuit used in our design. In this circuit, Vn and Vp outputs are used for biasing the NMOS and PMOS current sources, respectively. Also, Vncas and Vpcas provide the bias voltage for NMOS and PMOS cascode transistors, respectively. A 50 μA current is used as a reference current for this bias circuit. This bias circuit has a PWD (power down) digital input for shutting down the bias circuit, which itself results in powering down the amplifier. When PWD is high, M1 becomes open and block the reference current and M7 becomes closed and connects Vn to the ground. To power up the amplifier, PWD needs to be grounded.

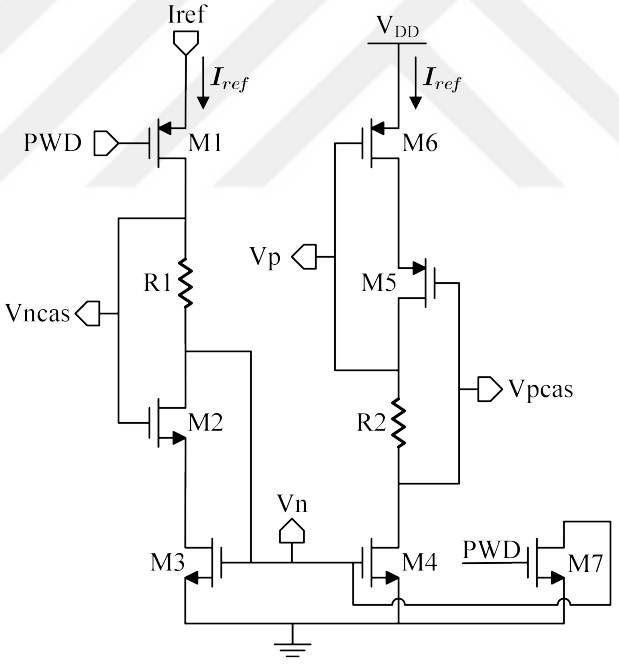

FIGURE 4.2: Schematic of bias circuit.

Consider the cascode circuit in Figure 4.3. In this circuit, all four transistors are biased with the bias voltages generated by bias circuit in Figure 4.2. Assuming $V_{TH9} = V_{TH2} = V_{TH3}$ and $V_{TH10} = V_{TH5} = V_{TH6}$, the OVSR for this cascode circuit is defined as

$$V_{OV3} + I_{ref}R_1 \leq \text{OVSR} \leq V_{DD} - (I_{ref}R_2 + V_{OV6}) \tag{4.2}$$

By choosing the resistance values of R_1 and R_2 such that $I_{ref}R_1 = V_{OV3}$ and $I_{ref}R_2 = V_{OV6}$, the OVSR becomes

$$2V_{OV3} \leq \text{OVSR} \leq V_{DD} - 2V_{OV6} \tag{4.3}$$

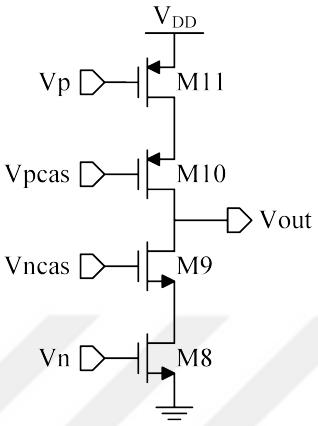

FIGURE 4.3: A cascode circuit.

So by choosing proper aspect ratios for the transistors in Figure 4.2, we can reduce the overdrive voltages, and increase OVSR and ICMR of the amplifier accordingly. Table 4.2 lists the design parameters for the bias circuit.

TABLE 4.2: Design parameters for bias circuit

Parameter	Value	Finger	Multiplier
M_1, M_7	$2.84\mu m/0.36\mu m$	4	2
M_2	$0.92\mu m/0.46\mu m$	2	1
M_3, M_4	$2.92\mu m/1.48\mu m$	2	1
M_5	$0.92\mu m/0.46\mu m$	2	3
M_6	$2.92\mu m/1.48\mu m$	2	3
R_1, R_2	12.297 $K\Omega$	-	-

To generate the reference current for the bias circuit in Figure 4.2 (I_{ref}), a constant transconductance (constant g_m) circuit is used. Figure 4.4 shows the schematic of constant g_m and its start up circuits. In this circuit, instead of using capacitors, transistors M_{16}, M_{21}, and M_{24} are used as capacitors for better matching.

In this constant g_m circuit, we set $(W/L)_8 = (W/L)_9$ and as a result $ID_8 = ID_9$. Hence, we must have $ID_{12} = ID_{13}$. By applying KVL to the loop consisting of M_{12}, M_{13}, and R_5 we have

$$V_{GS12} = V_{GS13} + ID_{13}R_5 \tag{4.4}$$

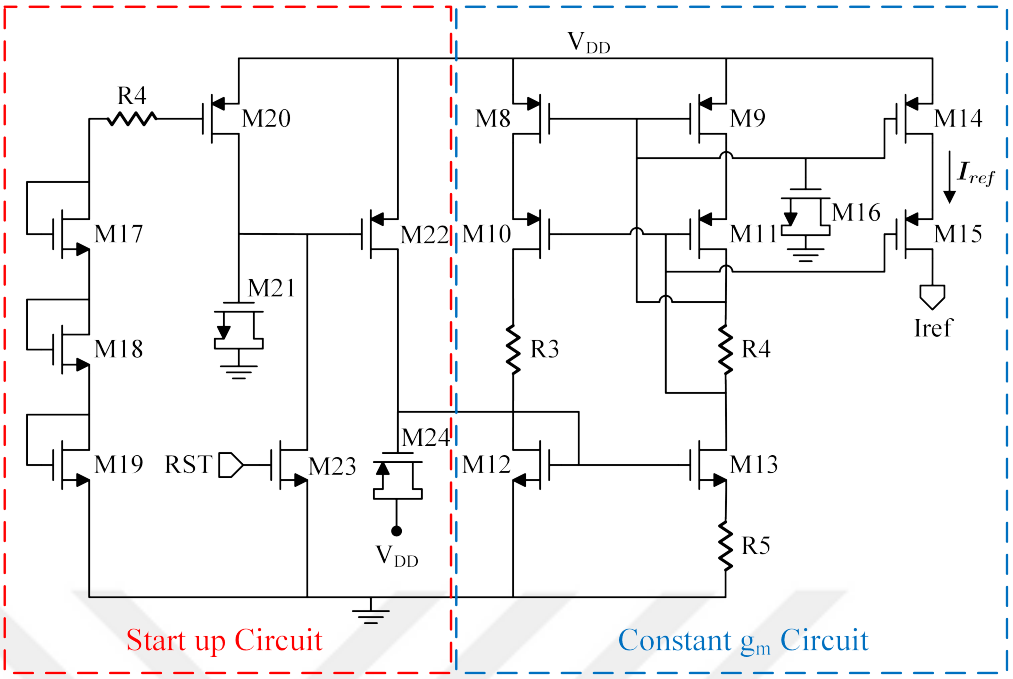

FIGURE 4.4: Schematic of constant g_m circuit.

Since $V_{OV} = V_{GS} - V_{TH}$, if we subtract V_{TH} from both sides we can write

$$V_{OV12} = V_{OV13} + ID_{13}R_5 \tag{4.5}$$

and recalling that $V_{OV} = \sqrt{\frac{2ID}{\mu C_{ox}(W/L)}}$ and $ID_{12} = ID_{13}$, we have

$$\sqrt{\frac{2ID_{12}}{\mu_n C_{ox}(W/L)_{12}}} = \sqrt{\frac{2ID_{12}}{\mu_n C_{ox}(W/L)_{13}}} + ID_{13}R_5 \tag{4.6}$$

By simplifying the latter equation, we can write

$$g_{m12} = \frac{2\left[1 - \sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}}\right]}{R_5} \tag{4.7}$$

Thus, the transconductance of $M12$ is determined by R_5 and the aspect ratio of $M12$ and $M13$. Since the transconductance is not a function of supply voltage, temperature and process parameters, the circuit is called constant transconductance or constant g_m circuit. The drawback of this circuit is that the resistance value of R_5 changes with temperature. To solve this problem, usually an external resistor with small temperature

coefficient is used as R_5. Another solution is to replace R_5 with equivalent switched-capacitor circuit [23]. The design parameters for constant g_m circuit is listed in Table 4.3.

TABLE 4.3: Design parameters for constant g_m circuit

Parameter	Value	Finger	Multiplier
M_8, M_9, M_{20}, M_{22}	$5.84\mu m/1.46\mu m$	2	4
M_{10}, M_{11}	$1.84\mu m/0.46\mu m$	2	8
M_{12}	$5.84\mu m/1.46\mu m$	2	1
M_{13}	$5.84\mu m/1.46\mu m$	2	8
M_{14}	$5.84\mu m/1.46\mu m$	2	10
M_{15}	$1.84\mu m/0.46\mu m$	2	20
M_{16}	$1.84\mu m/0.46\mu m$	2	128
M_{17}, M_{18}, M_{19}, M_{23}	$3.84\mu m/0.96\mu m$	2	1
M_{21}, M_{24}	$1.84\mu m/0.46\mu m$	2	16
R_3	$9.702K\Omega$	-	-
R_4	$14.511K\Omega$	-	-
R_5	$4.894K\Omega$	-	-

4.3.2 Folded Cascode Amplifier with Gain Boosting

Figure 4.5 illustrates the schematic of the proposed folded cascode amplifier. The transistors M_1 and M_2 are native NMOS transistors. Using native devices with negative V_{TH} as input transistors increases the ICMR of the amplifier. Figure 4.6 shows the drain current (ID) of a native NMOS with geometry aspect ratio of $W = 1.2\mu m$ and $L = 1.2\mu m$ versus its gate-source voltage (Vgs). Such a native device operates for gate voltages greater than -1 V.

The drawback of native devices is that they suffer from low transconductance. Therefore, to achieve the target desired gain, gain boosting technique is utilized. In Figure 4.5, CS amplifiers M_9, M_{10}, M_{19}, and M_{20} along with their current sources M_7, M_8, M_{21}, and M_{22}, respectively, perform gain boosting for the cascode transistors M_{15}, M_{16}, M_{13}, and M_{14}, respectively. Recalling that the output impedance of a gain boosted cascode is multiplied by the gain of boosting amplifier we can define the output impedance of the proposed amplifier as

$$\begin{aligned} R_{o+} &= [g_{m16}r_{o16}r_{o18}g_{m10}(r_{o10}||r_{o8})]|||[g_{m14}r_{o14}r_{o12}g_{m20}(r_{o20}||r_{o22})] \\ R_{o-} &= [g_{m15}r_{o15}r_{o17}g_{m9}(r_{o9}||r_{o7})]|||[g_{m13}r_{o13}r_{o11}g_{m19}(r_{o19}||r_{o21})] \end{aligned} \tag{4.8}$$

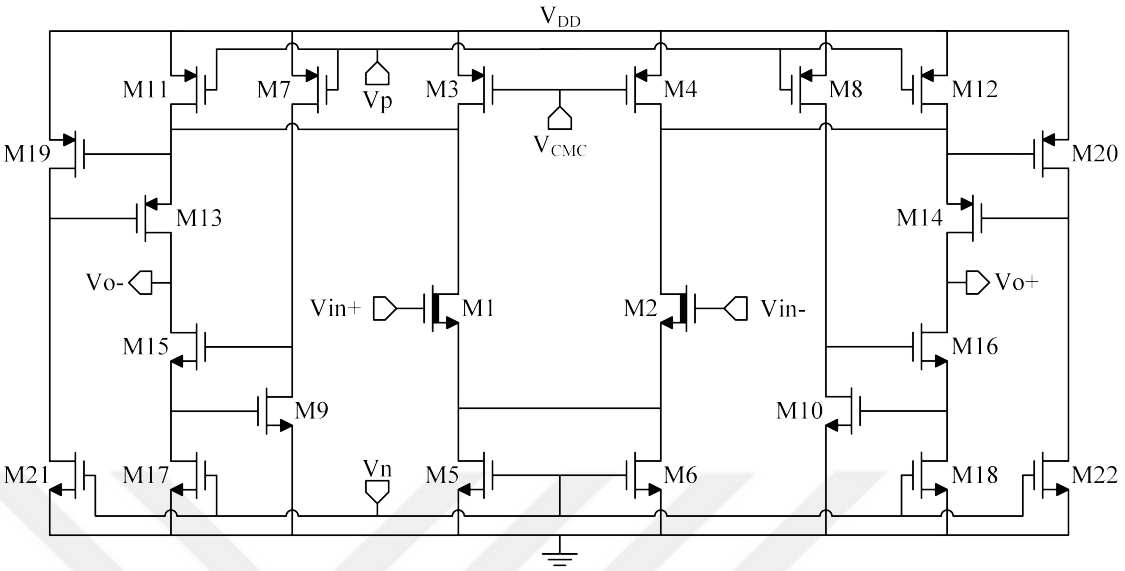

FIGURE 4.5: Schematic of proposed folded cascode amplifier with gain boosting.

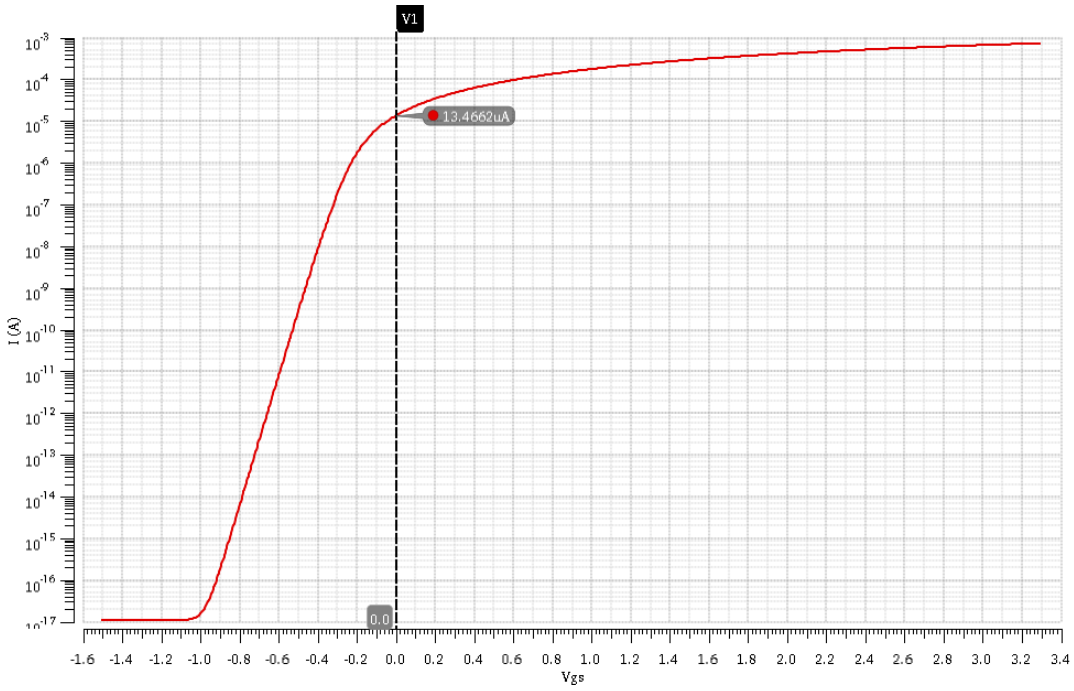

FIGURE 4.6: ID on a log scale versus V_{gs}.

Assuming $g_{m10} = g_{m20}$, $g_{m9} = g_{m19}$, $r_{o10} = r_{o8} = r_{o20} = r_{o22}$, and $r_{o9} = r_{o7} = r_{o19} = r_{o21}$, we can conclude that the output impedance of the amplifier has been increased by a factor of $\frac{g_{m10}r_{o10}}{2}$ and $\frac{g_{m9}r_{o9}}{2}$ for positive and negative output terminals, respectively. The geometry aspect ratios of transistors in the proposed amplifier are listed in Table 4.4.

TABLE 4.4: Aspect ratio of transistors in the proposed folded cascode amplifier

Parameter	Value	Finger	Multiplier
M_1, M_2	$4.84\mu m/1.24\mu m$	4	14
M_3, M_4, M_5, M_6, M_7, M_8	$2.92\mu m/1.48\mu m$	2	12
M_9, M_{10}	$0.92\mu m/0.46\mu m$	2	4
M_{11}, M_{12}	$2.92\mu m/1.48\mu m$	2	48
M_{13}, M_{14}	$0.92\mu m/0.46\mu m$	2	24
M_{15}, M_{16}	$0.92\mu m/0.46\mu m$	2	8
M_{17}, M_{18}	$2.92\mu m/1.48\mu m$	2	8
M_{19}, M_{20}	$0.92\mu m/0.46\mu m$	2	12
M_{21}, M_{22}	$2.92\mu m/1.48\mu m$	2	4

The bias voltages of NMOS and PMOS transistors (Vn and Vp, respectively) are generated by the bias circuit shown in Figure 4.2. In this design, the drain of M_3 and $M1$ are shorted in order to form a single current source but with one difference; The gate voltage of M_3 is controlled by CMFB circuit, whereas $M1$ is a constant current source. The same approach applies to M_4 and M_{12}. By separating the current sources, the load for CMFB circuit reduces. As a result, the gain of the CMFB amplifier decreases and phase margin of CMFB circuit increases.

4.3.3 Common Mode Feedback

For fully differential operational amplifiers it is required to use a CMFB circuit for controlling the common mode output voltage. Figure 4.7 shows the CMFB amplifier used in our design. Here, M_1 and M_2 are native NMOS transistors. The amplifier detects the common mode output voltage by the resistive divider R_1 and R_2 and sets the V_{CMC} voltage to a value that keeps the outputs of folded cascode amplifier balanced around the reference voltage V_{CM}. In our design, the voltages V_{out+} and V_{out-} come from the outputs of class AB output stages. Table 4.5 shows the design parameters for CMFB circuit.

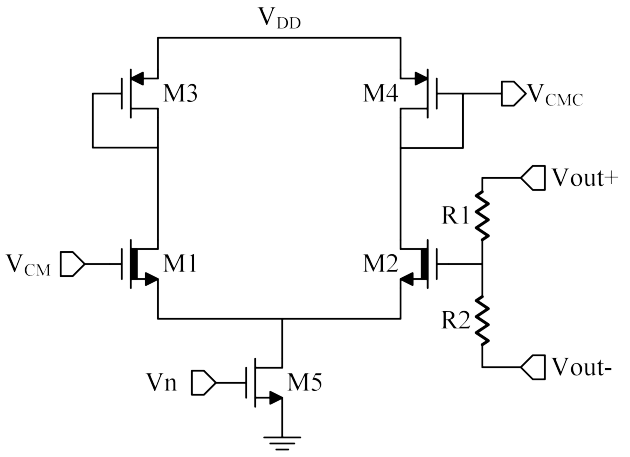

FIGURE 4.7: Schematic of CMFB amplifier

The common mode feedback must be connected in a negative feedback configuration. If the common-mode output voltage increases, CMFB decreases the upper currents sources. If the common-mode output voltage decreases, CMFB increase the upper currents sources. By controlling the upper current source, M_3 and M_4 in Figure 4.5, CMFB stabilizes the output voltage. The gain of CMFB circuit in Figure 4.7 is expressed by

$$\text{Gain} = -g_{m2}(r_{o2}||r_{o4}||\frac{1}{g_{m4}}) \approx -\frac{g_{m2}}{g_{m4}} \tag{4.9}$$

TABLE 4.5: Design parameters for CMFB circuit

Parameter	Value	Finger	Multiplier
M_1, M_2	$4.84\mu m/1.24\mu m$	4	2
M_3, M_4	$2.92\mu m/1.48\mu m$	2	20
M_5	$2.92\mu m/1.48\mu m$	2	12
R_1, R_2	$30K\Omega$	-	-

4.4 Process Corner Configurable Class AB Output Stage

To obtain a high dynamic range, achieving a high OVSR is of great importance. But folded cascode amplifiers suffer from low OVSR, which results in the dynamic range degradation. Additionally, folded cascode amplifiers have large output impedance and our amplifier will be operating in a unity gain feedback configuration using 300 Ω feedback resistors. To drive such a low resistance efficiently, the output impedance of the amplifier

is required to be low. Hence, using a class AB output stage is required for providing rail to rail output voltage swing as well as low output impedance.

Performance of output stage effects slew rate and linearity of the amplifier. If the current provided by the output stage is not sufficient for achieving a desired slew rate, the resulting output signal will be distorted. Moreover, in a push-pull output stage, if charging current provided by PMOS transistor does not equate the discharging current sank by NMOS transistor, the output signal will be distorted. The solution to these two problems is adjusting the aspect ratio of PMOS and NMOS transistors correctly to satisfy the slew rate requirement as well as having identical strength in providing and sinking current.

However, the problem is that while manufacturing the device, there may be variability in the manufacturing which results in the change of characteristics of devices such as threshold voltage. These variations in the manufacturing are clustered into three different lots (known as process corners): slow, typical, and fast. It is important to make sure that the design will meet the requirements over different process corners. To overcome this problem, we designed a process corner configurable class AB output stage. Figure 4.8 shows the proposed output stage.

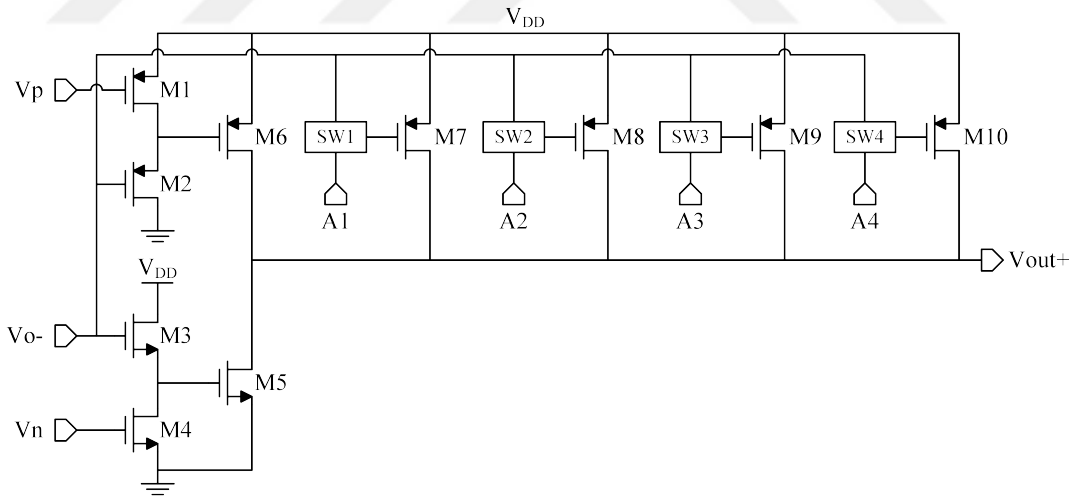

FIGURE 4.8: Schematic of process corner configurable class AB output stage

Here, the control bits $A_4A_3A_2A_1$ are used to configure the output stage to operate over different process corners. When a control bit goes high, the corresponding switch closes and a pushing transistor is added to the output. For simplicity, by keeping the aspect ratio of pulling transistor (M_5) constant, we only change the aspect ratio of pushing transistor. Meaning that when the pulling strength changes over different process corners,

by using control bits, the pushing strength of the output stage is adjusted to be equal to the pulling strength. Table 4.6 lists the geometry aspect ratio of transistors in output stage (Figure 4.8) and Table 4.9 shows the values of $A_4A_3A_2A_1$ for different process corners.

TABLE 4.6: Aspect ratio of transistors in class AB output stage

Parameter	Value	Finger	Multiplier
M_1	$2.92\mu m/1.48\mu m$	2	6
M_2	$0.92\mu m/0.46\mu m$	4	22
M_3	$0.92\mu m/0.46\mu m$	4	4
M_4	$2.92\mu m/1.48\mu m$	2	2
M_5	$2.4\mu m/0.36\mu m$	4	140
M_6	$2.4\mu m/0.36\mu m$	4	15
M_7	$2.4\mu m/0.36\mu m$	4	7
M_8	$2.4\mu m/0.36\mu m$	4	12
M_9	$2.4\mu m/0.36\mu m$	4	35
M_10	$2.4\mu m/0.36\mu m$	4	46

For area optimization purposes, we used incremental design, i.e., each time a PMOS pushing transistor switches on, it is added to the previously switched on transistor. Since the distortion of system is very sensitive to the output stage, to minimize the distortion of switches, we used a common-drain amplifier (source follower) with enable, as a switch (represented by SW in Figure 4.8). Figure 4.9 shows the schematic of switch used in process corner configurable output stage. When En is high, M_3 is off, M_4 is on, the drain of M_2 is grounded and a source follower is formed. Whereas, when En is low, M_3 is on, M_4 is off, the drain of M_2 is connected to V_{DD} and M_1 and M_2 enter the cutoff region. The aspect ratio of transistors in source follower of Figure 4.9 are listed in Table 4.7.

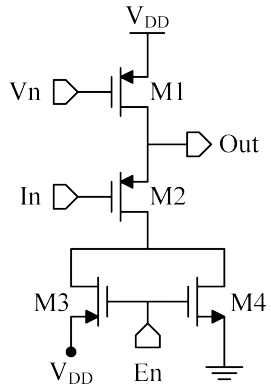

FIGURE 4.9: Schematic of source follower with enable

TABLE 4.7: Aspect ratio of transistors in source follower with enable

Parameter	Value	Finger	Multiplier
M_1	$2.92\mu m/1.48\mu m$	2	6
M_2	$0.92\mu m/0.46\mu m$	4	22
M_3, M_4	$2.48\mu m/0.36\mu m$	4	4

4.5 Process Corner Configurable Miller Compensation

Although folded cascode amplifiers are naturally stable, after adding an output stage, it is required to compensate the circuit to ensure the stability of amplifier. Fully differential folded cascode amplifiers are usually compensated by parallel compensation which is simply adding a parallel capacitor to the output of amplifier and push the dominant pole of the amplifier to a lower frequency. As a result the phase margin of the amplifier increases. The drawback of this compensation is that it requires large capacitors. In our design, adding an additional gain stage (i.e. the CS output stage) makes it possible to use miller compensation technique. The UGF of the proposed amplifier is determined by

$$f_T = \frac{1}{2\pi}\frac{g_{m1}}{C_C} \tag{4.10}$$

where f_T and C_C are the UGF and compensation capacitor, respectively. Recalling that over different process corners capacitance value of C_C and transconductance of transistors vary, the need for a process corner configurable compensation circuit arises. Figure 4.10 illustrates the compensation circuit used to compensate the proposed folded cascode amplifier. Here, the control bits $B_3B_2B_1$ are used to adjust the capacitance value of the compensation circuit. The resistor R is used to cancel the RHP zero introduced by the adding the compensation capacitor.

The design parameters for compensation circuit and the values of control bits $B_3B_2B_1$ for different process corners are listed in Table 4.8 and Table 4.9, respectively.

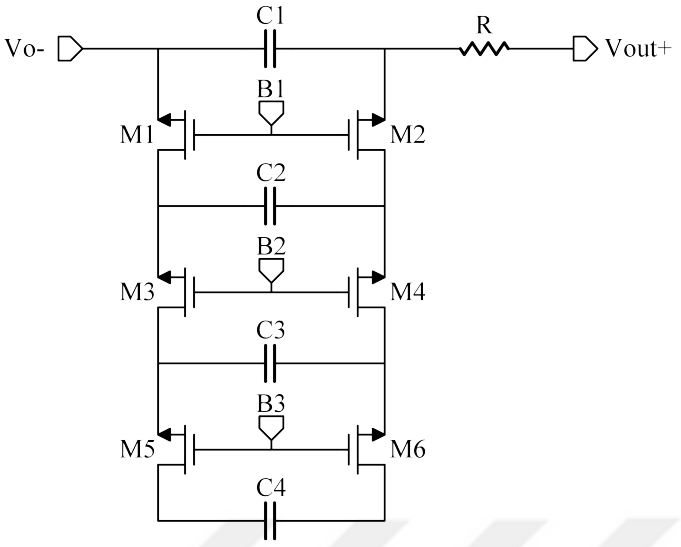

FIGURE 4.10: Schematic of process corner configurable class AB output stage

TABLE 4.8: Design parameters for compensation circuit

Parameter	Value	Finger	Multiplier
M_1 to M_6	$2.84\mu m/0.36\mu m$	4	4
C_1	$3.6pF$	-	-
C_2, C_3	$800fF$	-	-
C_4	$400fF$	-	-
R_1	109Ω	-	-

TABLE 4.9: Different process corners and their corresponding control bits for class AB output stage and compensation circuit

Process corner	$A_4A_3A_2A_1$	$B_3B_2B_1$
TTTT	0011	001
FFFF	0001	111
FFFS	0001	001
FFSF	0000	111
FFSS	0000	001
SSFF	1111	111
SSFS	1111	000
SSSF	0111	011
SSSS	0111	000

Chapter 5

Simulation Results

5.1 Schematic Simulations

5.1.1 AC Response

Figure 5.1 shows the closed loop AC response of the proposed amplifier. The amplifier obtains a DC gain of $130dB$, $3dB$ cutoff frequency of $48Hz$, UGBW of $198.3MHz$ and a phase margin of 68°.

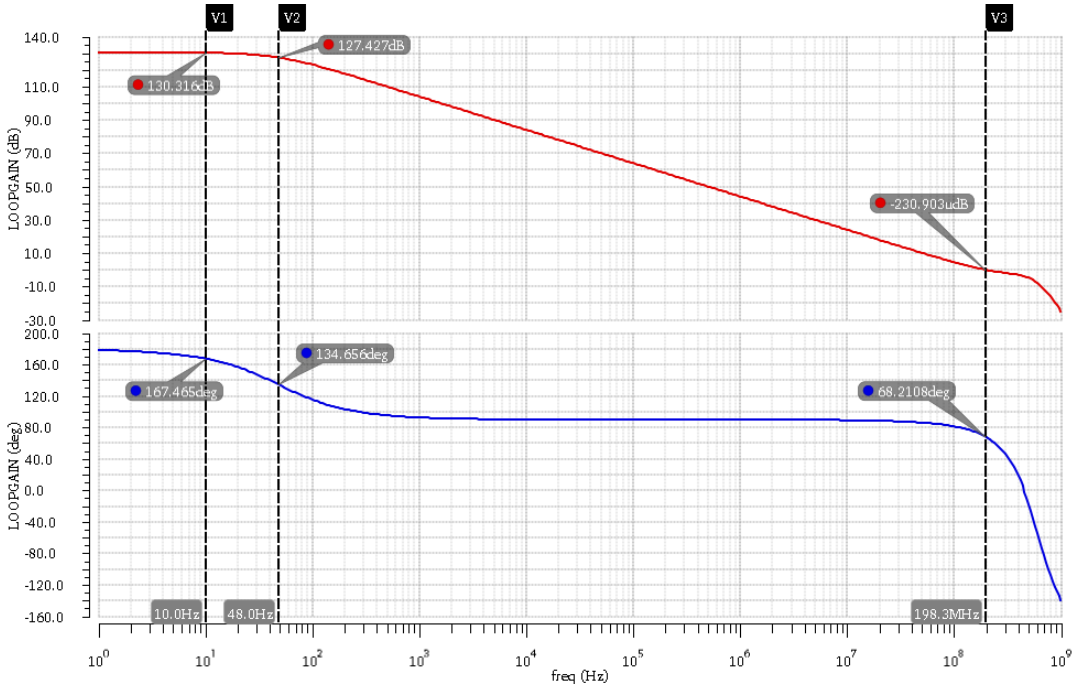

FIGURE 5.1: AC response of the proposed amplifier; (red) Loop gain, (blue) Phase response

Figure 5.2 shows the effect of the compensation circuit on AC response of the proposed amplifier. Adding compensation circuit increases the phase margin but decreases the $3dB$ cutoff frequency and UGBW.

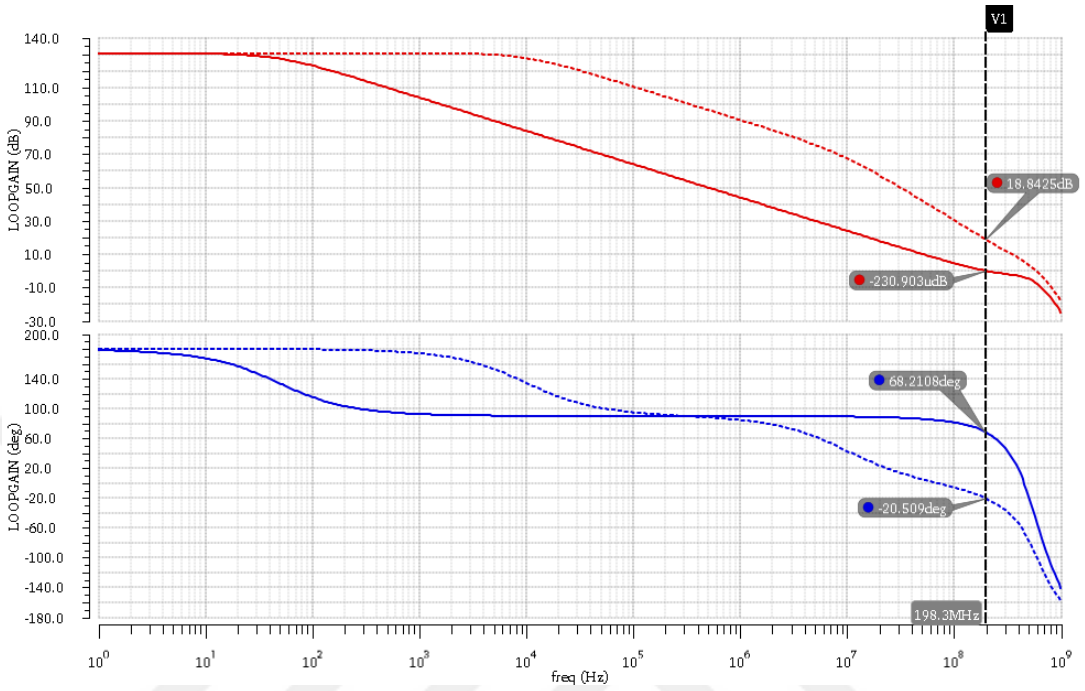

FIGURE 5.2: AC response of the proposed amplifier (solid line) with and (dashed line) without compensation circuit.

5.1.2 Transconductance variation

Figure 5.3 plots the transconductance of the input stage versus input common mode voltage (V_{icm}). For the interval of interest (i.e. $0.55V < V_{icm} < 2.75V$), the g_m variation is calculated by Eq.5.1 and for the interval in which the amplifier operates (i.e. $0.181V < V_{icm} < 2.945$), the g_m variation is calculated by Eq.5.2.

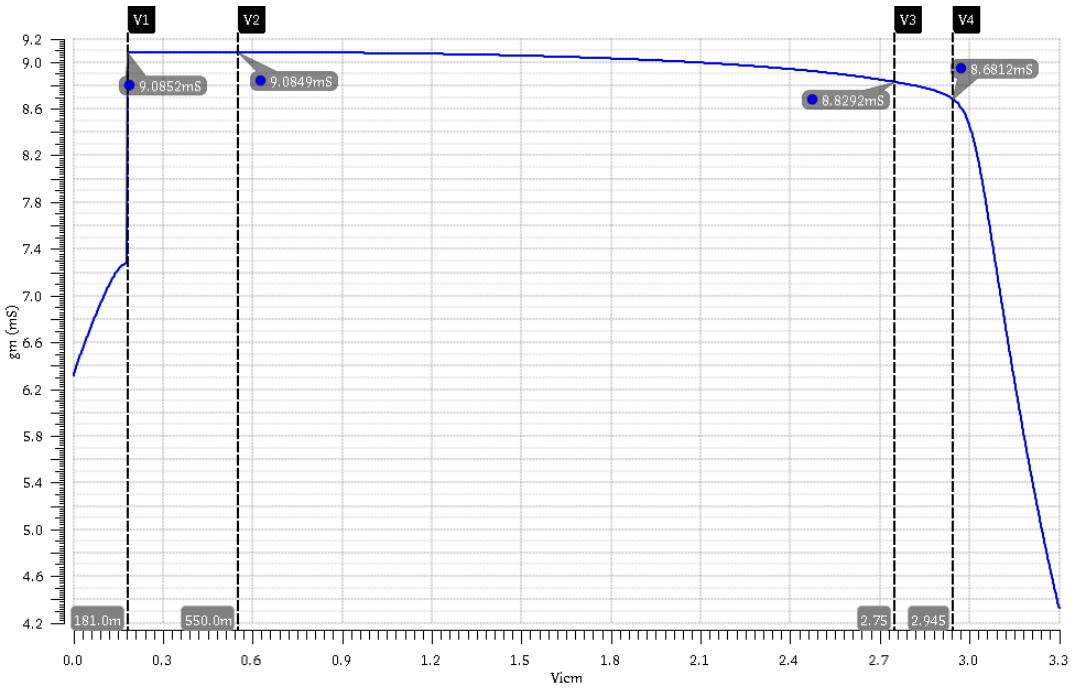

FIGURE 5.3: g_m versus input common mode voltage

$$g_m(variation) = \frac{9.0849 - 8.8292}{9.0849} = 0.0282 = 2.82\% \tag{5.1}$$

$$g_m(variation) = \frac{9.0852 - 8.6812}{9.0852} = 0.0445 = 4.45\% \tag{5.2}$$

5.1.3 Input Common Mode Range

Figure 5.4 shows the DC gain of the proposed amplifier versus input common mode voltage (V_{icm}). From this figure, we can find the ICMR of the amplifier. There are different interpretations for ICMR but here we use $3dB$ gain cutoff interpretation. The range of V_{icm} values for which the DC gain of the amplifier is not degraded by more than $3dB$ is considered as ICMR of the amplifier. According to Figure 5.4, the ICMR of the amplifier is measured as

$$0.181V < \text{ICMR} < 2.945V \tag{5.3}$$

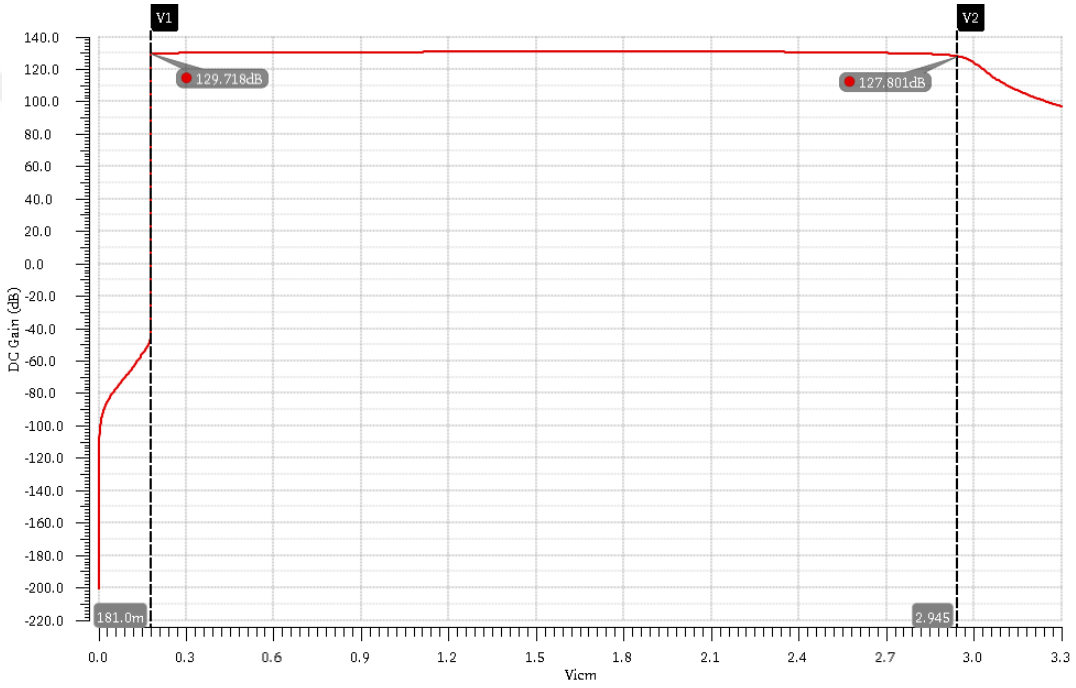

FIGURE 5.4: DC gain of the proposed amplifier versus input common mode voltage

5.1.4 Common Mode Rejection Ratio

Figure 5.5 plots the differential and common mode gain, and CMRR of the proposed amplifier versus frequency. The CMRR ratio of the amplifier is defined as

$$\text{CMRR} = 20\log(\frac{A_d}{A_{cm}}) = A_d(dB) - A_{cm}(dB) \tag{5.4}$$

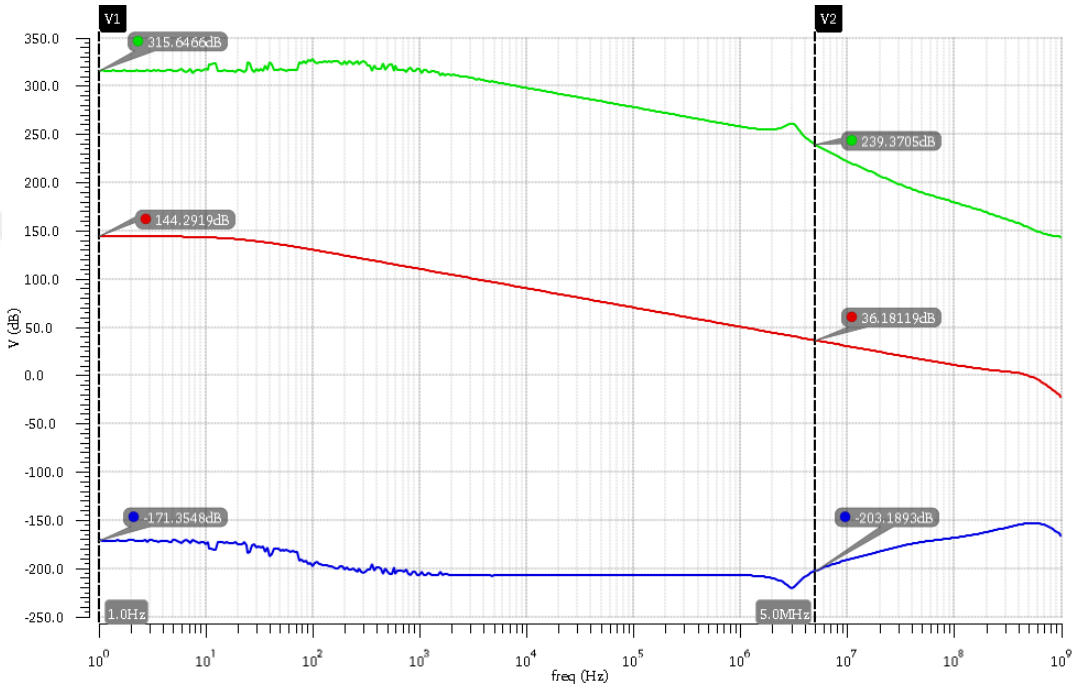

FIGURE 5.5: (red) Differential gain, (blue) common mode gain, and (green) CMRR of the proposed amplifier versus frequency

5.1.5 Power Supply Rejection Ratio

Figure 5.6 shows the PSRR of the proposed amplifier. Here, the x-axis is the frequency in which the supply voltage ripples. To measure the PSRR of the amplifier, we simply add AC component to the supply voltage and measure the AC gain at the output of the amplifier. Figure 5.6 shows how much the supply voltage variations will effect the output of the amplifier at different frequencies. The minimum PSRR is measured to be $-89dB$.

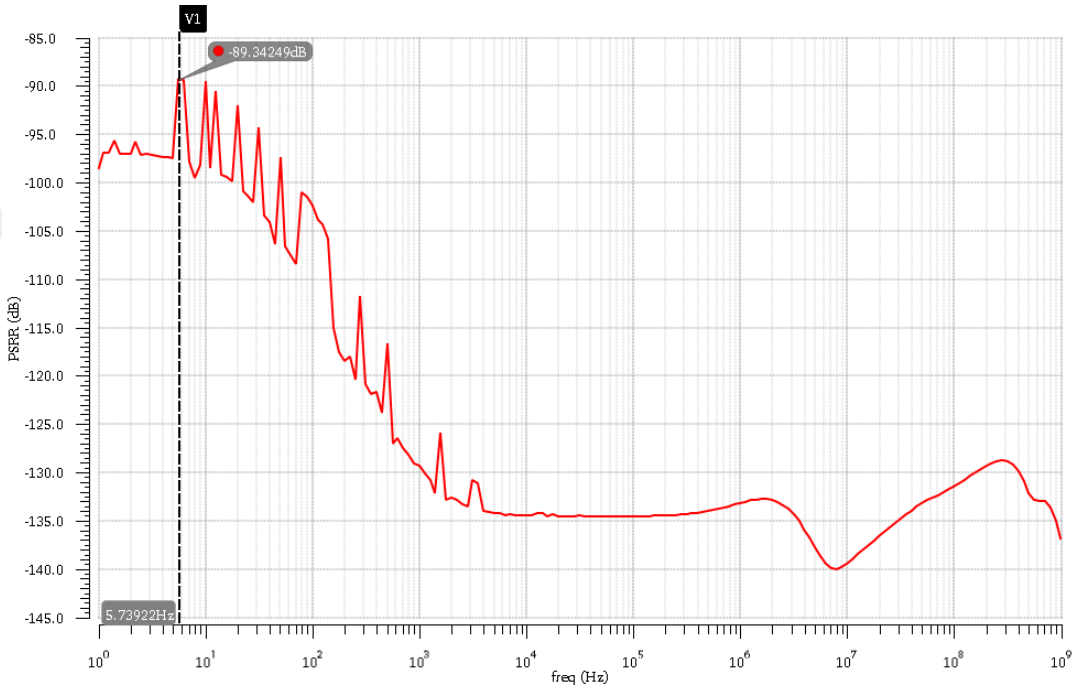

FIGURE 5.6: Power supply rejection ratio of the proposed amplifier versus supply voltage ripple frequency

5.1.6 Noise

Minimizing the noise of amplifier was one of the design goals regarding the proposed amplifier. Figure 5.7 shows the spot noise and Figure 5.8 shows the total integrated noise of the proposed amplifier versus frequency.

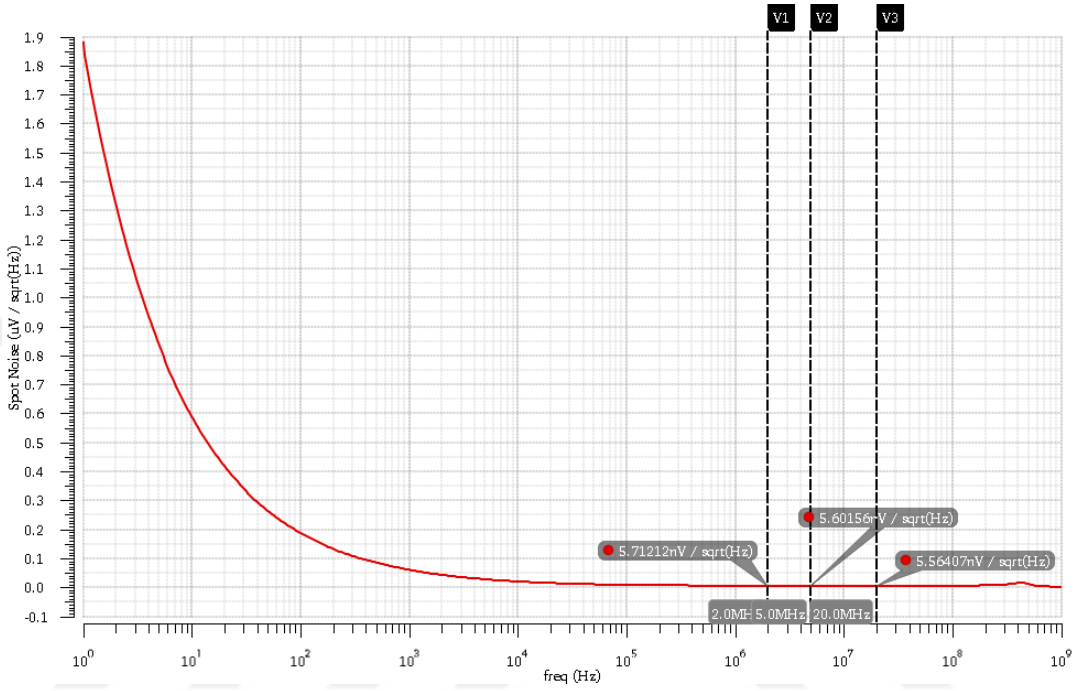

FIGURE 5.7: Spot noise of the proposed amplifier versus frequency

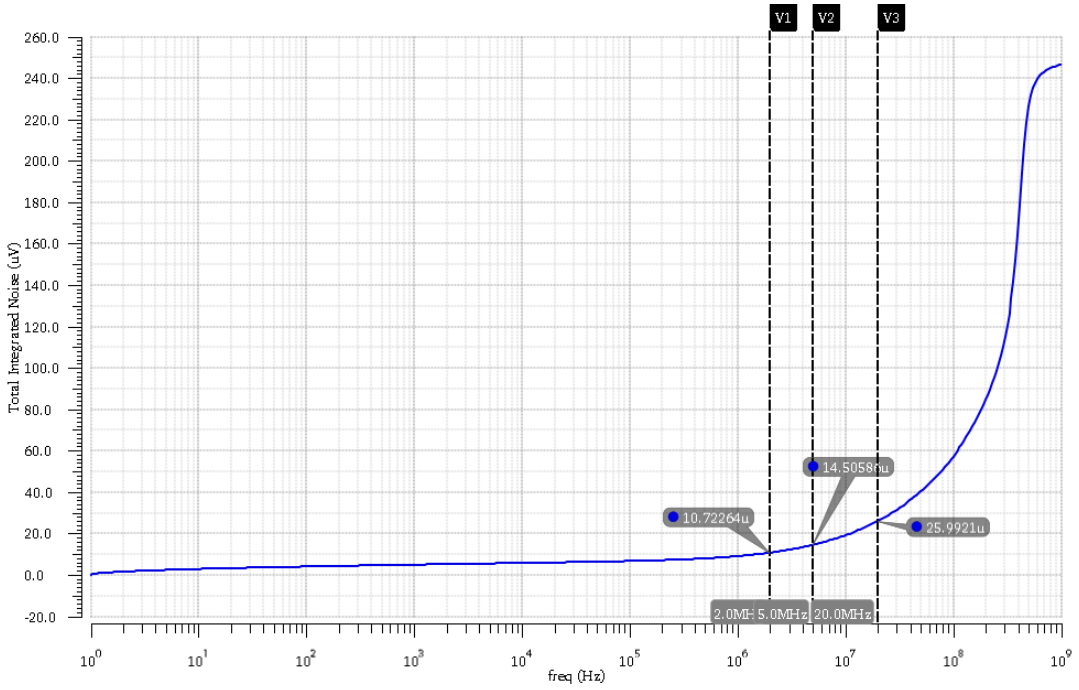

FIGURE 5.8: Total integrated noise of the proposed amplifier versus frequency

5.1.7 Output Voltage Swing Range

To measure the output voltage swing range of the amplifier, we sweep the input voltage and measure the DC voltage at the output of the amplifier. Figure 5.9 plots the DC output voltage of the proposed amplifier versus the input voltage. The range in which the output voltage changes linearly is defined as OVSR. As expected, the output of the amplifier is rail to tail.

According to Figure 5.8 the integrated noise of the amplifier at $5MHz$ is $14.505\mu V$. Recalling Eq.4.1, we can calculate the dynamic range of the proposed amplifier as

$$\mathrm{DR} = 10\log\frac{V^2_{pp(signal)}}{V^2_{noise}} = 10\log\frac{3.3^2}{(14.505\times10^{-6})^2} = 107dB \tag{5.5}$$

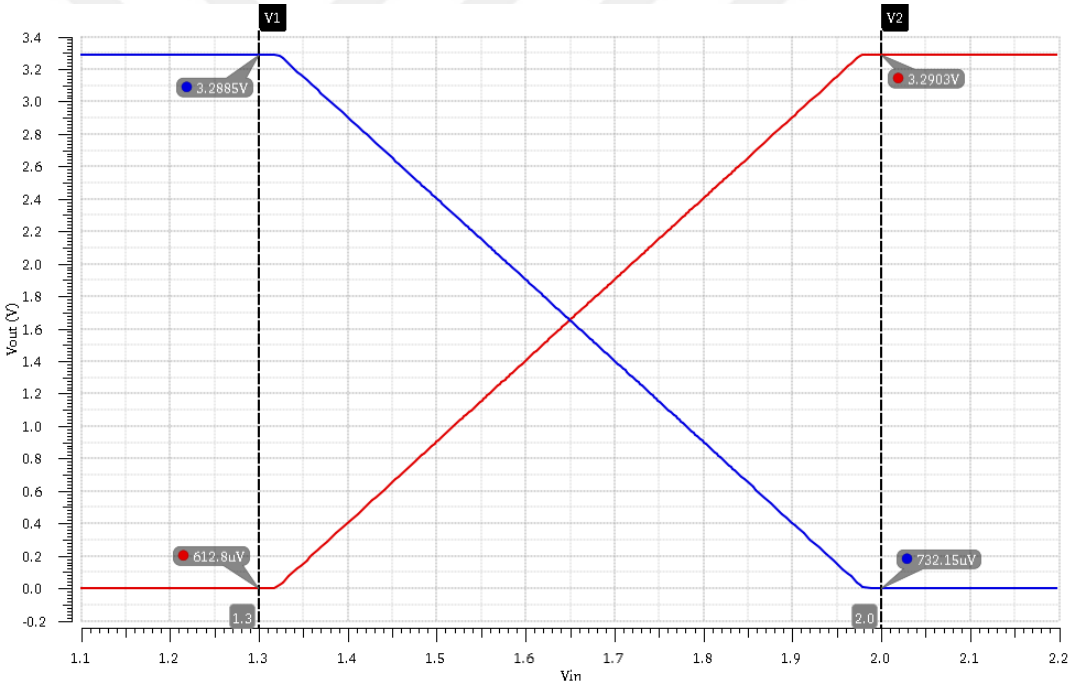

FIGURE 5.9: Output voltage swing range of the proposed amplifier for (red) positive and (blue) negative output terminals

5.1.8 Total Harmonic Distortion

The THD of the amplifier is the most important factor for measuring the performance of the proposed amplifier. Figure 5.10 plots the THD of the proposed amplifier versus the frequency of input signal. At $5Mhz$, the THD is measured to be $-92.2dB$. It is worth mentioning that the THD is simulated for the case that the amplifier is connected to a single-ended input signal rather than to a differential input signal.

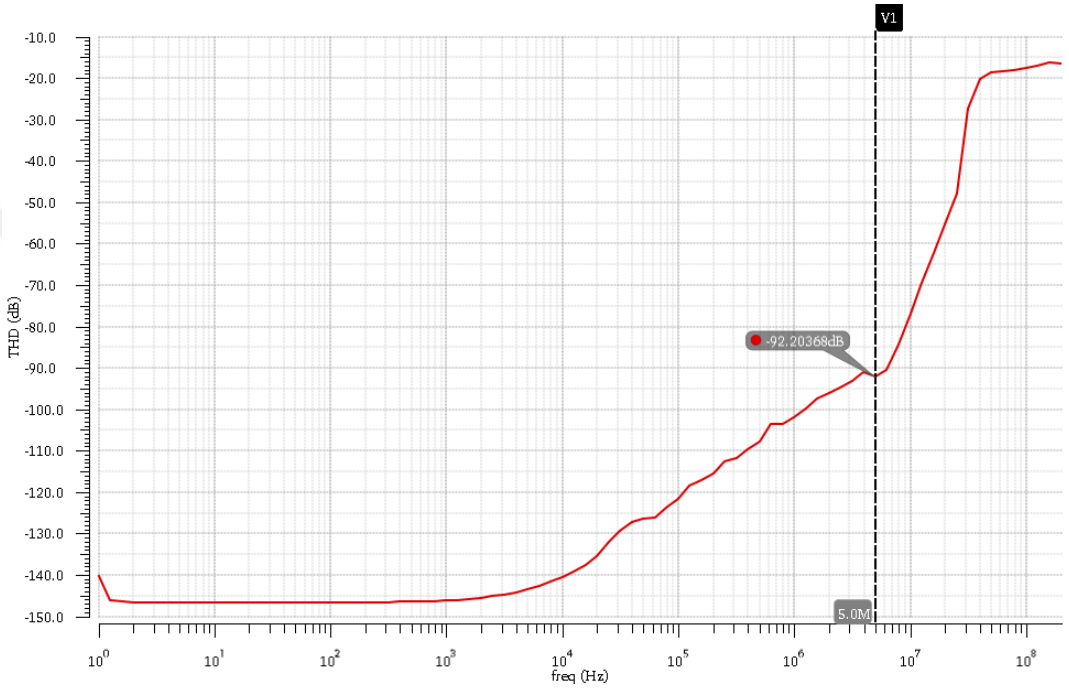

FIGURE 5.10: Total harmonic distortion of the proposed amplifier versus input signal frequency

5.1.9 Transient Response

This section includes the simulation results for transient response of the proposed amplifier to sinusoidal and square input signals. Figure 5.11 shows the transient response of the proposed amplifier to a single-ended input sinusoidal signal. The input signal has a DC voltage of $1.65V$ and a peak-to-peak AC voltage of $2.2V$. The amplifier converts this single-ended input into a differential output with half the magnitude of the input signal. The DC output voltage is set to $1.65V$ by the CMFB circuit. Figure 5.12 zooms into Figure 5.11 to illustrate the transient delay of the amplifier. The proposed amplifier exhibits a delay of $1.03ns$.

Figure 5.13 and Figure 5.14 illustrate the transient response of the proposed amplifier to a square input wave for positive output terminal and negative output terminal, respectively. From these two figures, we can calculate the maximum slew rate (SR), the settling time (T_S), and the overshoot percentage (OS).

$$\begin{aligned} \mathrm{SR}^+ &= 90.75V/\mu s \\ \mathrm{SR}^- &= 90.40V/\mu s \end{aligned} \tag{5.6}$$

$$\begin{aligned} T_s^+ &= 40ns \\ T_s^- &= 38ns \end{aligned} \tag{5.7}$$

$$\begin{aligned} OS^+ &= \frac{2.90 - 2.75}{2.75} = 4.45\% \\ OS^- &= \frac{2.95 - 2.75}{2.75} = 7.27\% \end{aligned} \tag{5.8}$$

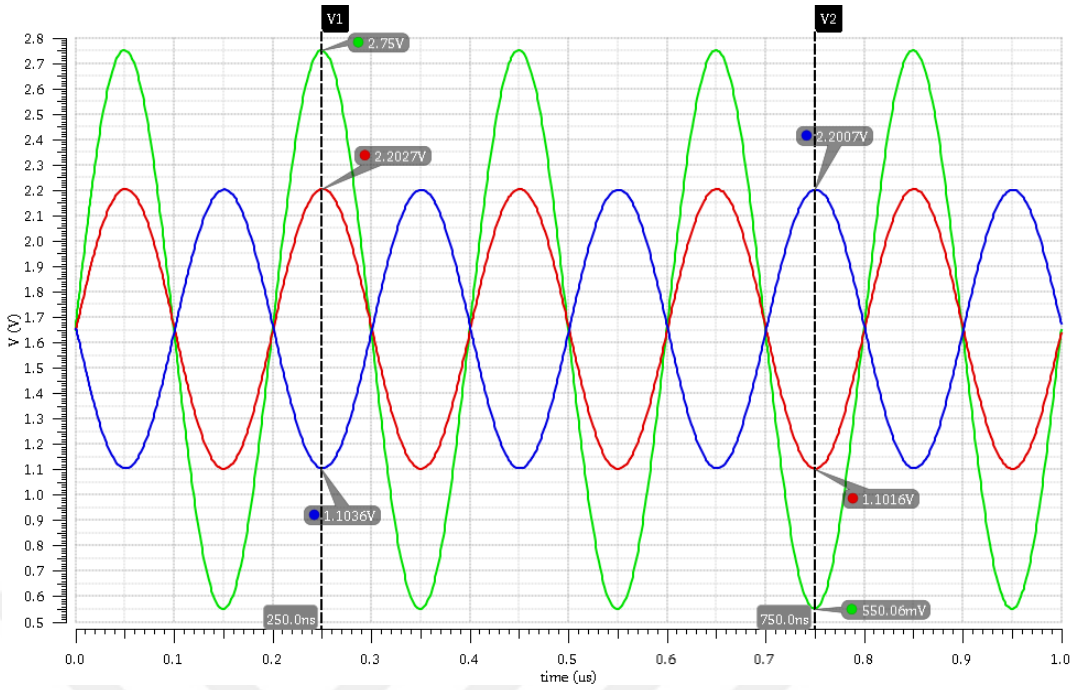

FIGURE 5.11: Transient response of the proposed amplifier; (green) input signal and output signal at (red) positive and (blue) negative output terminals

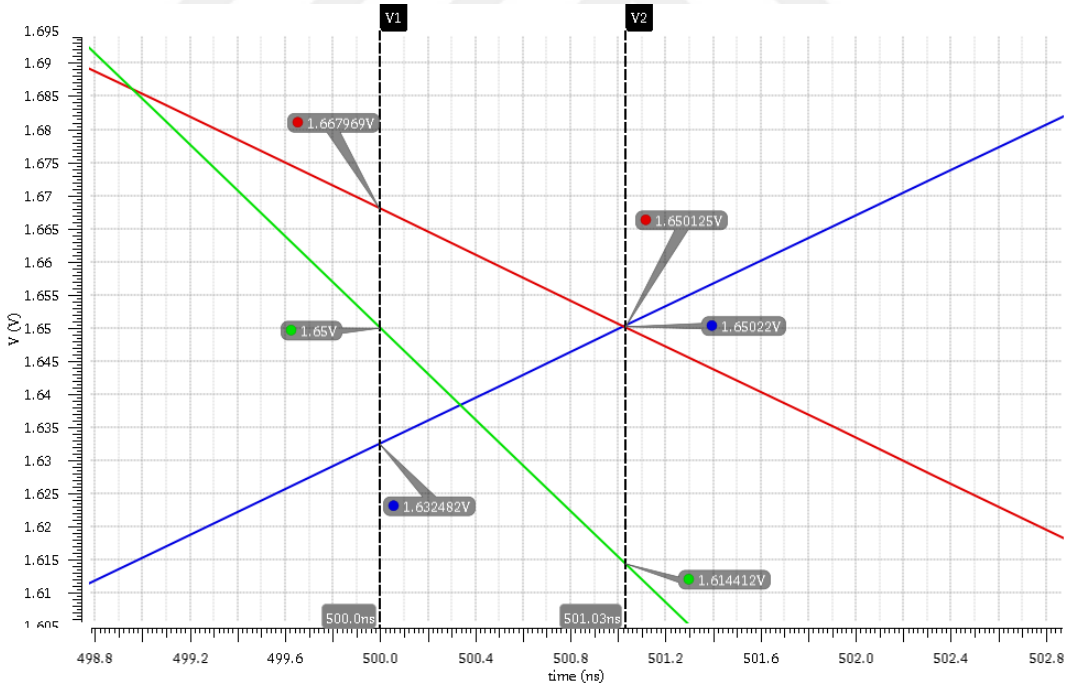

FIGURE 5.12: Transient delay of the proposed amplifier; (green) input signal and output signal at (red) positive and (blue) negative output terminals

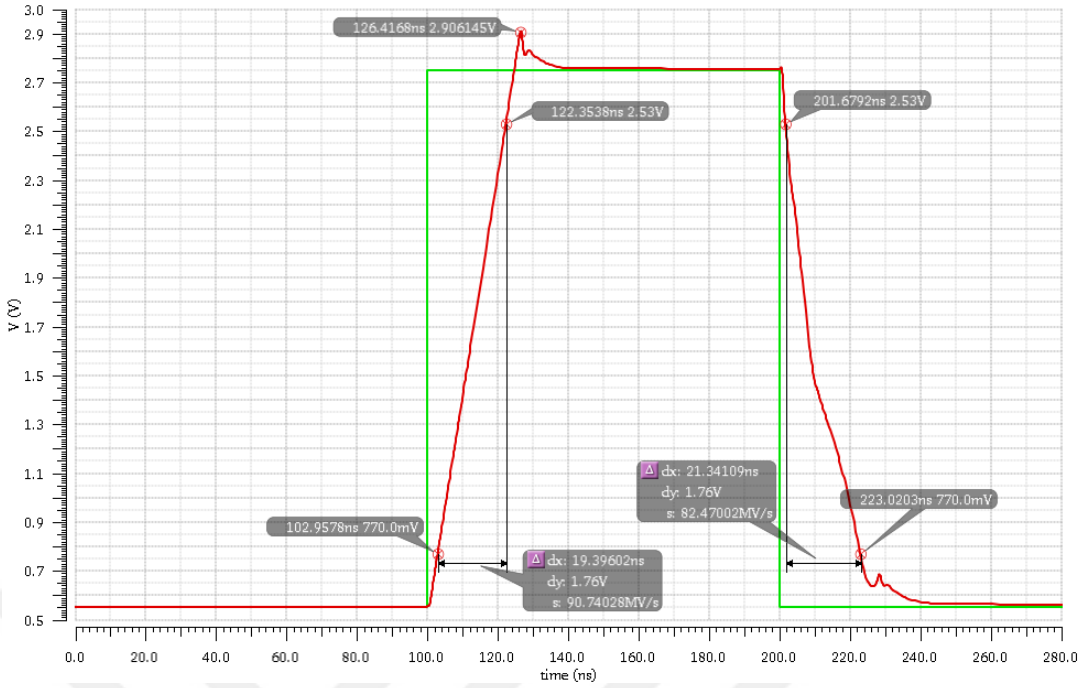

FIGURE 5.13: Transient response of the proposed amplifier to a square input wave; (green) input signal and output signal at (red) positive output terminal

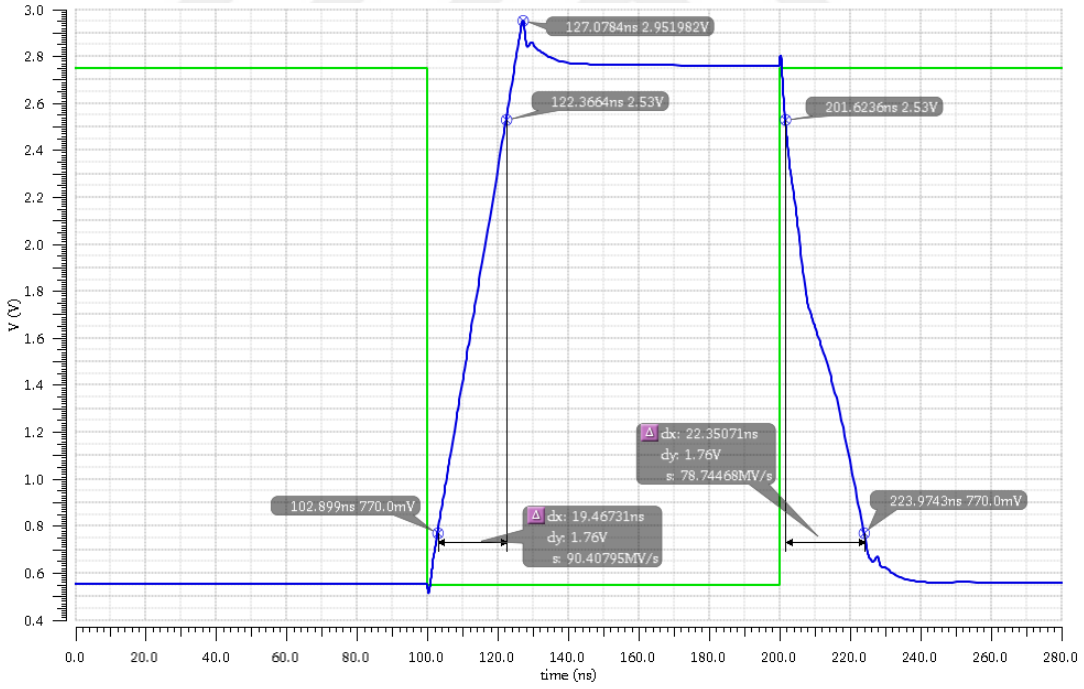

FIGURE 5.14: Transient response of the proposed amplifier to a square input wave; (green) input signal and output signal at (blue) negative output terminal

Table 5.1 compares the target design specifications with the simulation results.

TABLE 5.1: Target specifications versus simulation results

Specification	Target Value	Simulation Result
DC gain	$\geq 120dB$	$130dB$
UGBW	$200MHz$	$198.3MHz$
Phase margin	$\geq 60^{\circ}$	68°
Output dynamic range	$\geq 86dB$	$107dB$
THD	$\leq -86dB$	$-92.2dB$
OVSR	$3.3V_{pp}$	$3.3V_{pp}$
CMRR @ $5MHz$	$\geq 100dB$	$240dB$
Slew rate	$\geq 87V/\mu s$	$90.40V/\mu s$
Total Integrated Noise @ $5MHZ$	$\leq 165\mu V$	$14.505\mu V$

5.2 Temperature Simulations

This section includes the simulation results for the performance of the proposed amplifier over different temperatures. Figures 5.15 to 5.18 show DC gain, UGBW, phase margin, and DC power consumption of the proposed amplifier over different temperature values, respectively. Also Figures 5.19 to 5.21 show the spot noise, total integrated noise, and total harmonic distortion of the amplifier at $5MHz$ over different temperature values, respectively.

As shown in Figure 5.17, the phase margin of the amplifier drops below 60°for the temperatures above 93°C until it reaches 51.5°at 120°C. Although the amplifier is stable from -40°C to 120°C, it may exhibit some ripples for the temperature values above 93°C.

From Figure 5.21, we can conclude that the proposed amplifier can drive a 14-bit ADC over the temperature range from -8°C to 53°C without degrading the ENOB. For the temperature values beyond this range, the ENOB of the ADC will be determined by the proposed pre-amplifier. The maximum THD occurs at -40°C and it is measured to be $-78dB$.

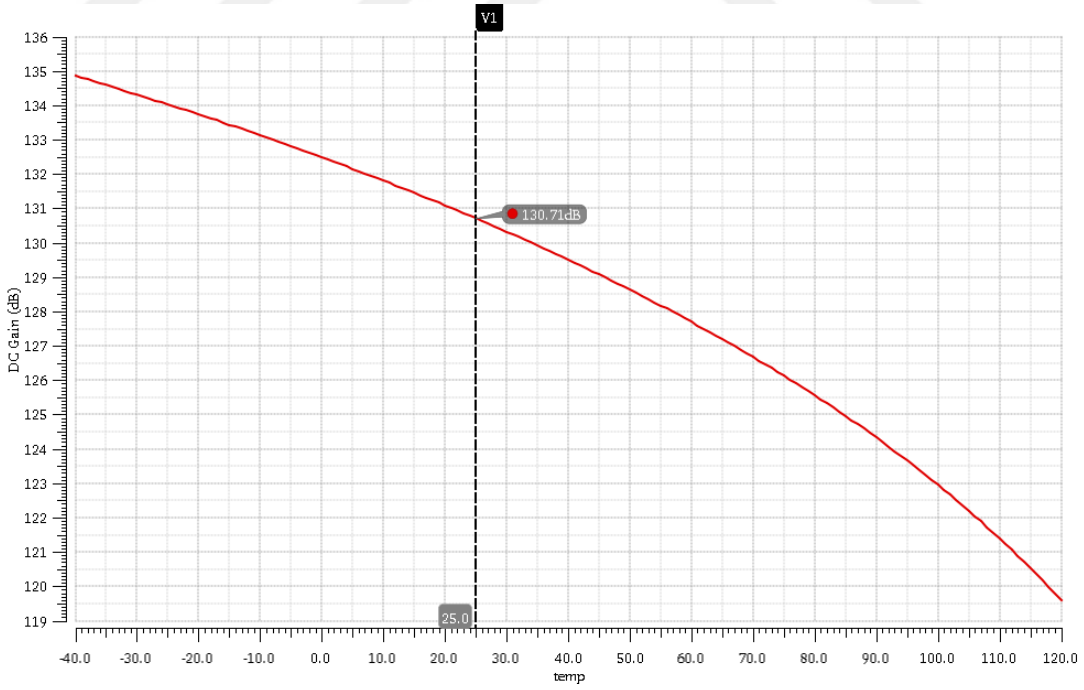

FIGURE 5.15: DC gain of the proposed amplifier versus temperature

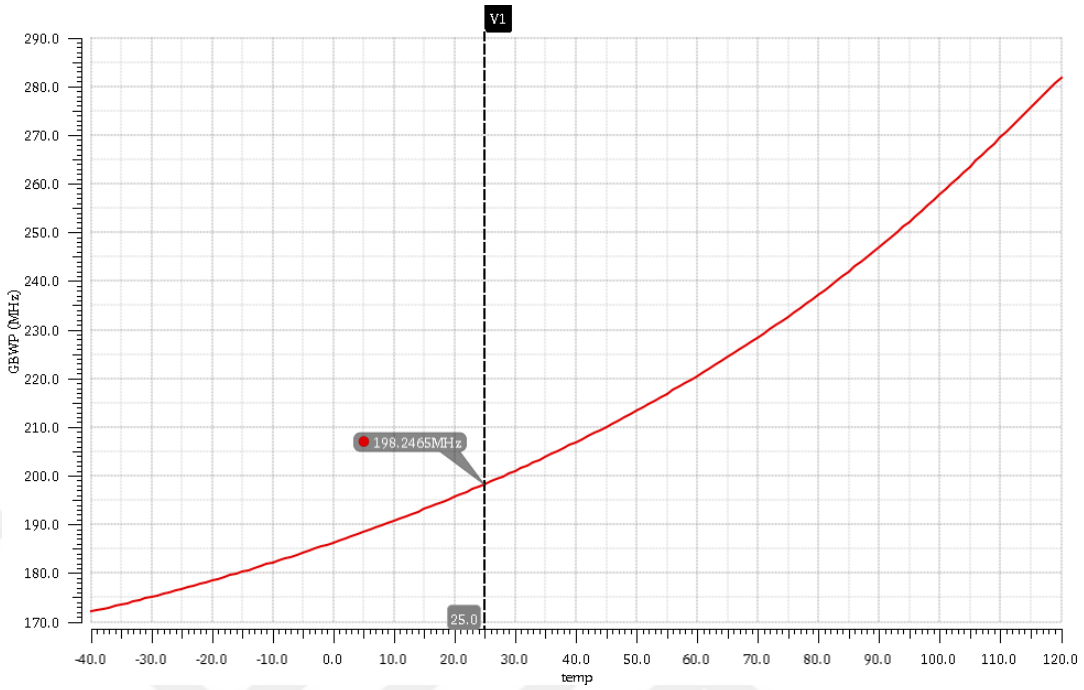

FIGURE 5.16: Unity gain frequency of the proposed amplifier versus temperature

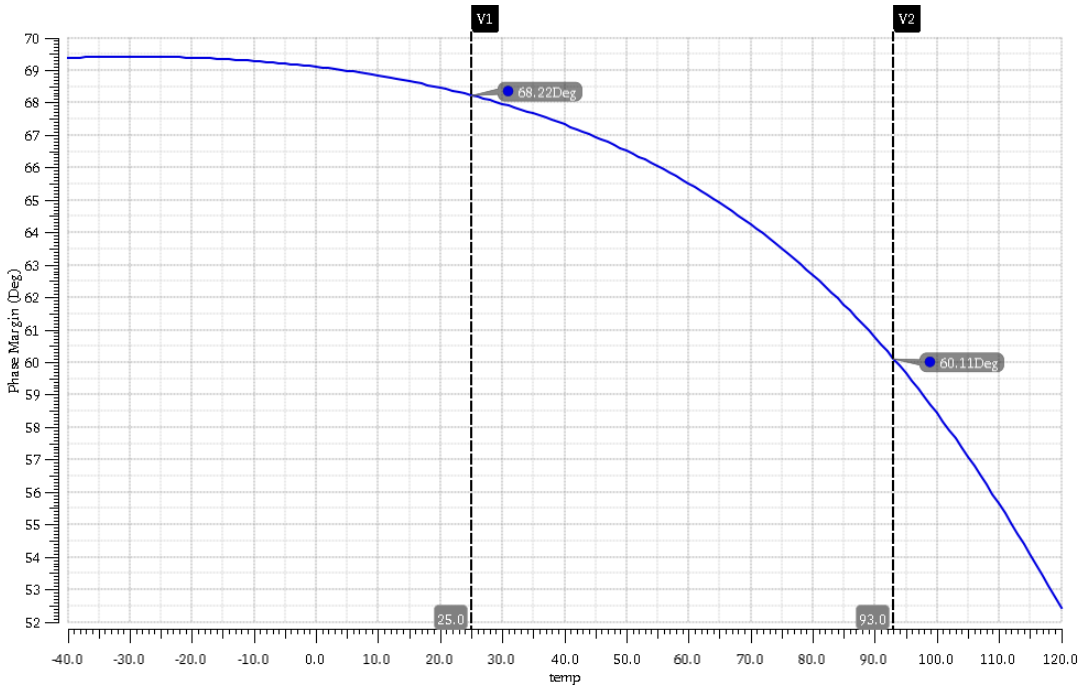

FIGURE 5.17: Phase margin of the proposed amplifier versus temperature

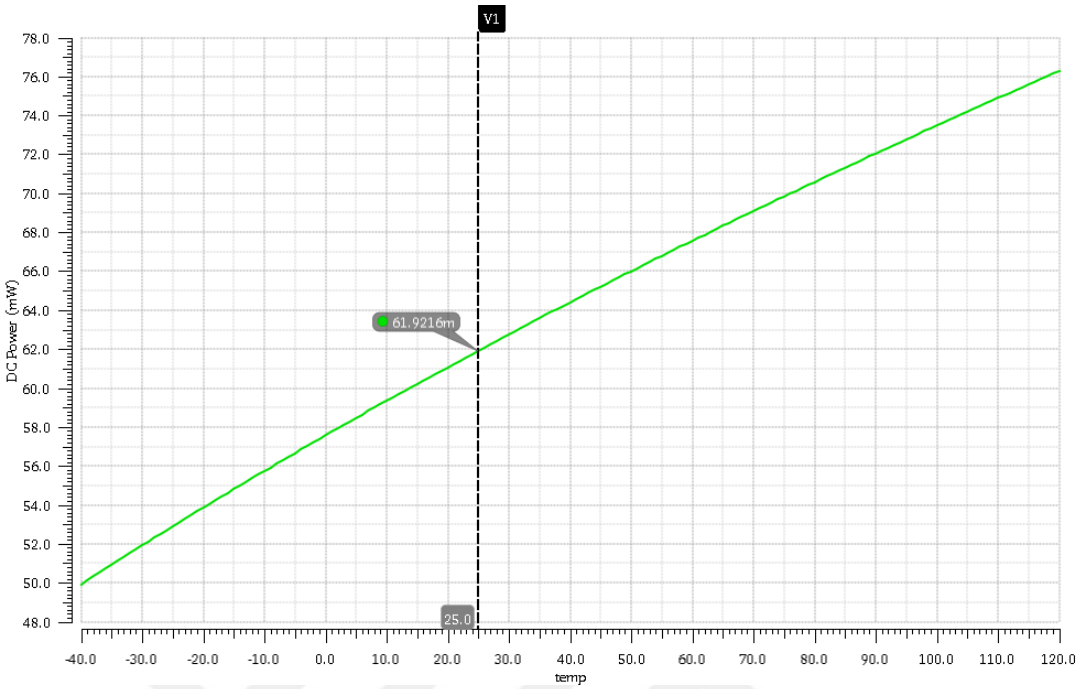

FIGURE 5.18: DC power consumption of the proposed amplifier versus temperature

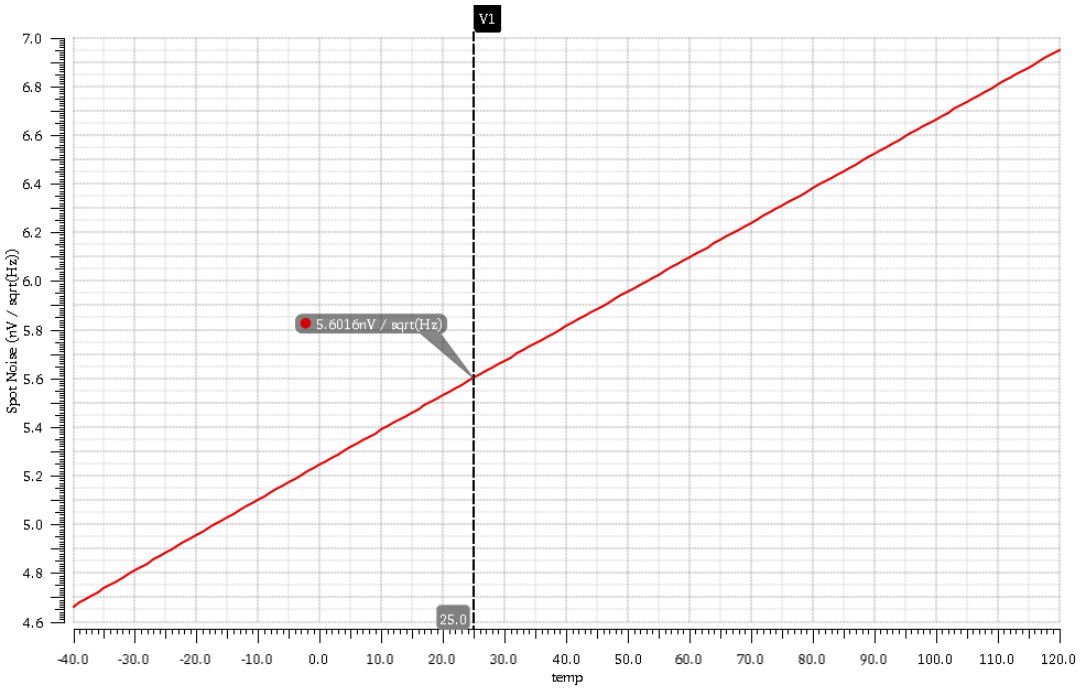

FIGURE 5.19: Spot noise of the proposed amplifier at $5MHz$ versus temperature

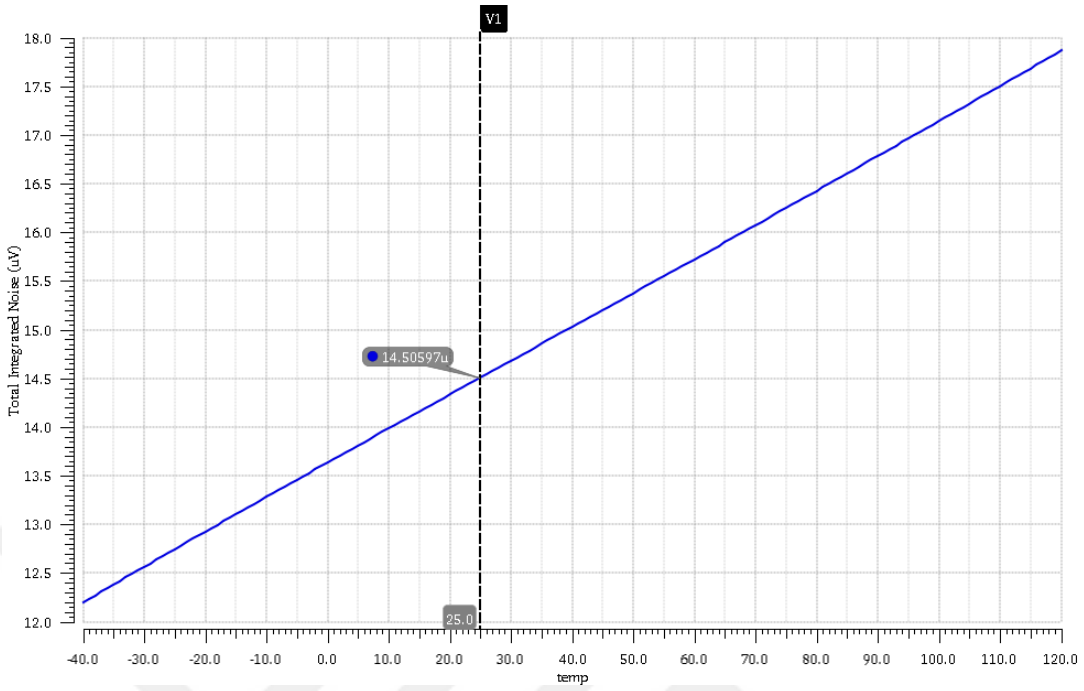

FIGURE 5.20: Total integrated noise of the proposed amplifier at $5MHz$ versus temperature

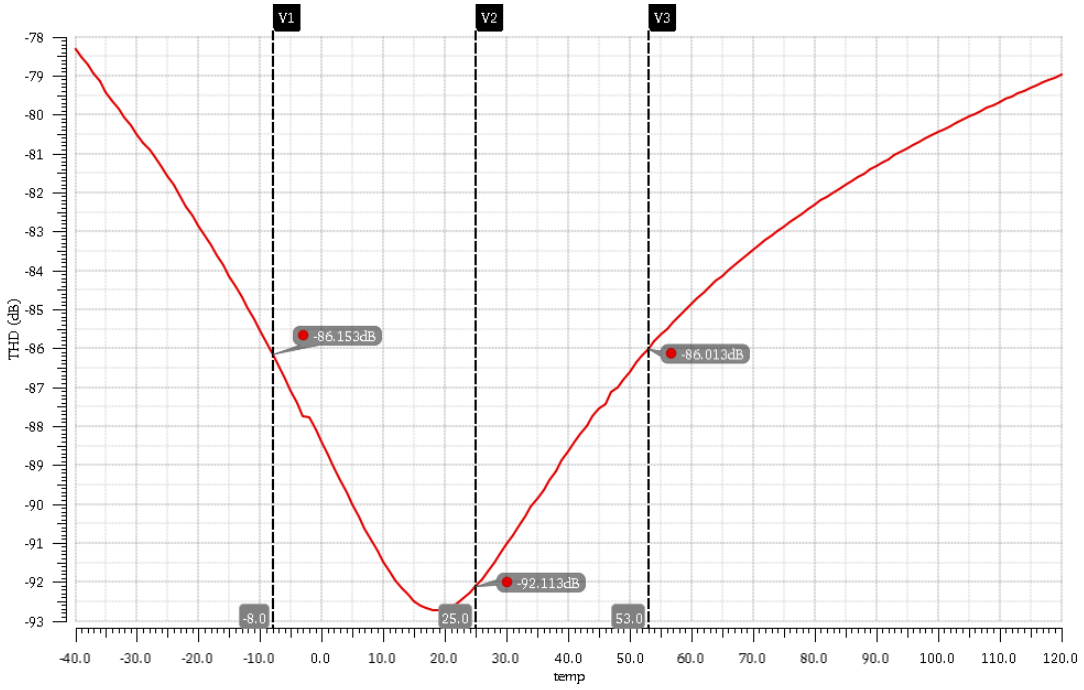

FIGURE 5.21: Total harmonic distortion of the proposed amplifier at $5MHz$ versus temperature

5.3 Process Corner Simulations

This section presents the process corner simulation results for the proposed amplifier. Throughout this section, different process corners will be denoted by four letters; e.g. FFSS. First two letters represent NMOS and PMOS devices and the third and fourth letters represent resistor and capacitor, respectively. For simplicity, NMOS and PMOS are assumed to be over the same process corner and during the corner simulations they are tied to each other.

5.3.1 AC Response

The AC response simulations of the amplifier over different process corners are presented in this sections. Figures 5.22 to 5.29 illustrate the DC gain, $-3dB$ frequency, UGBW, and the phase margin of the proposed amplifier over different process corners.

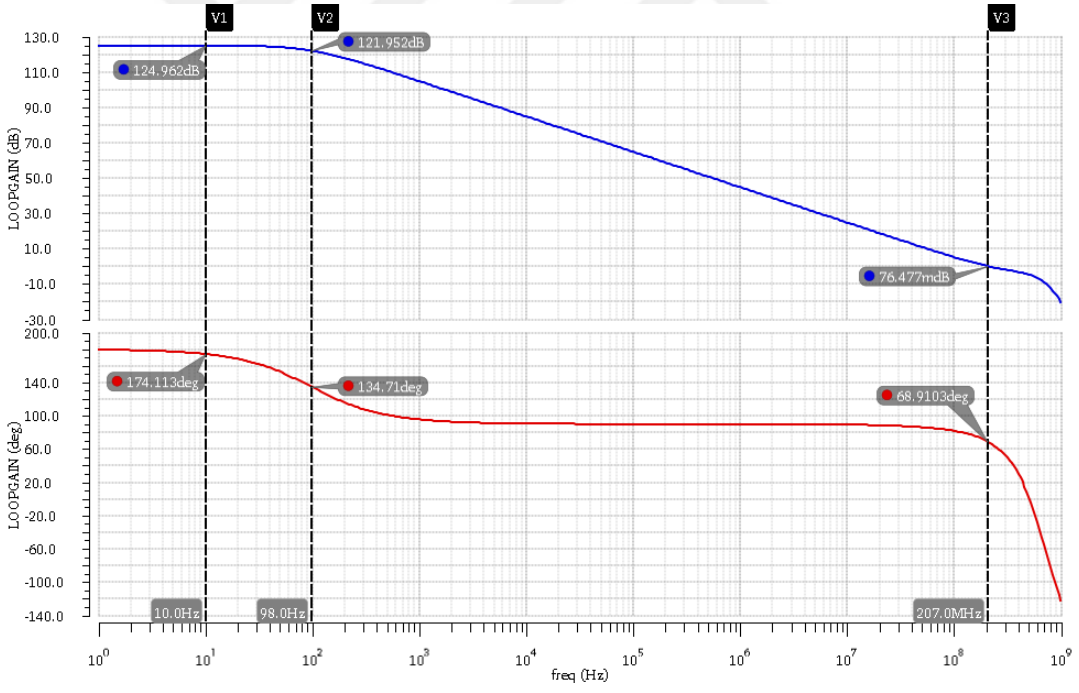

FIGURE 5.22: AC response of the proposed amplifier over FFFF process corner

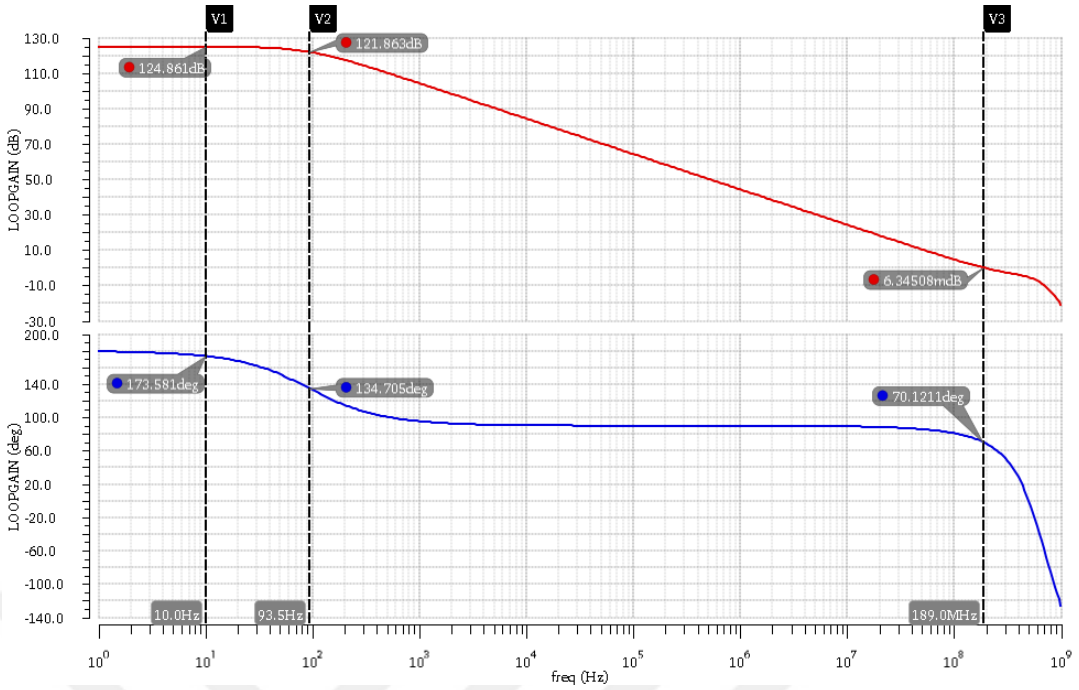

FIGURE 5.23: AC response of the proposed amplifier over FFFS process corner

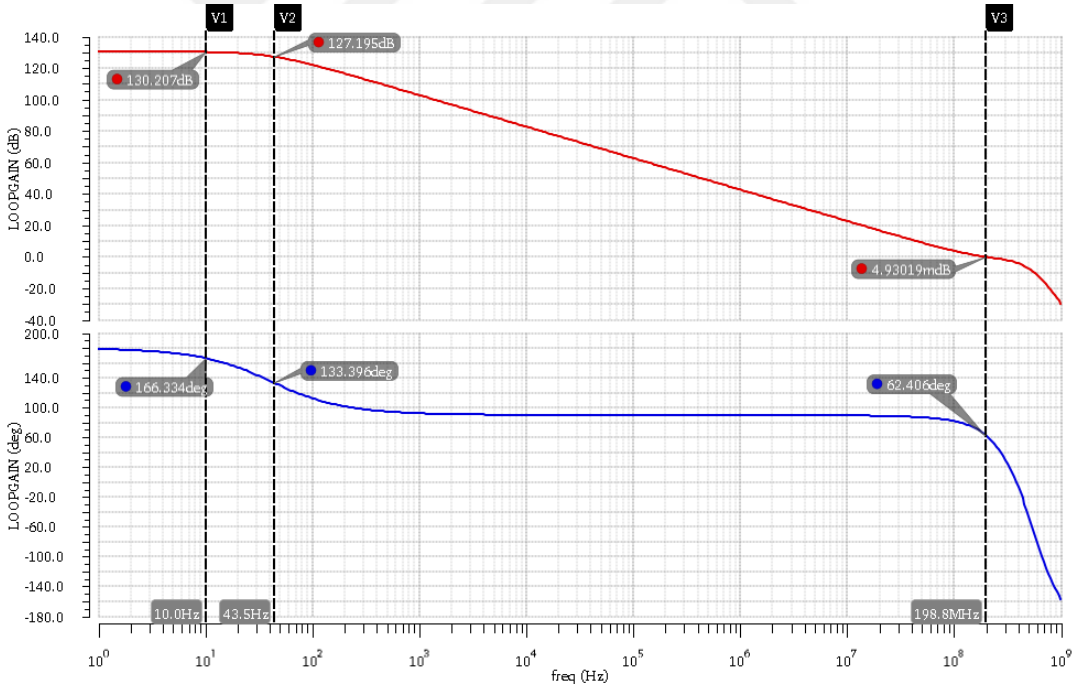

FIGURE 5.24: AC response of the proposed amplifier over FFSF process corner

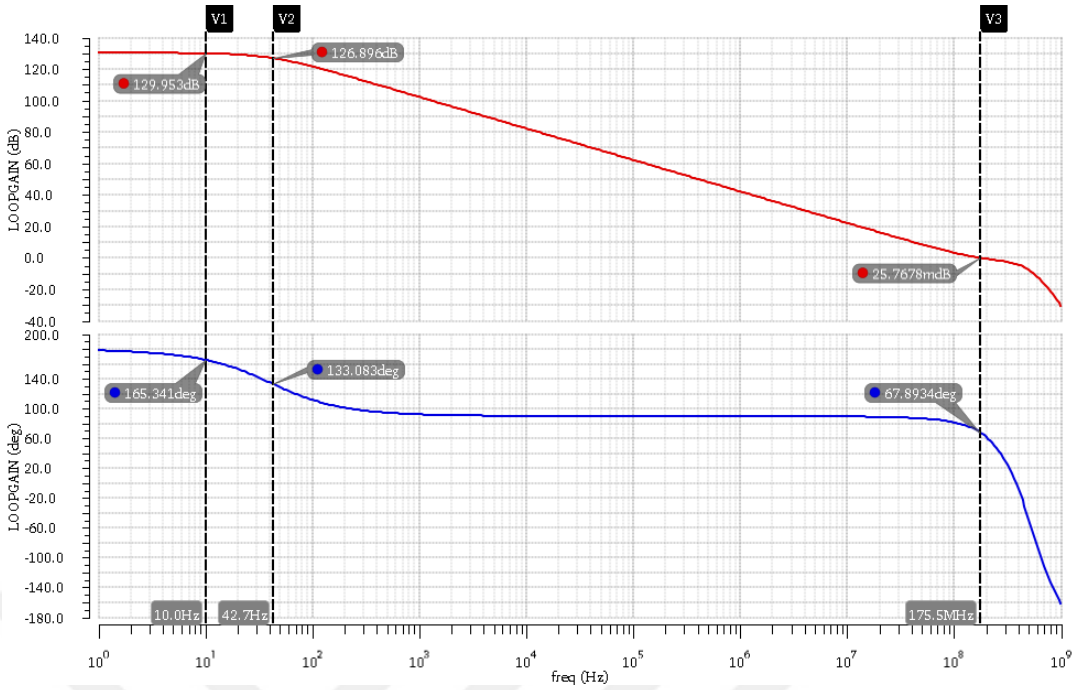

FIGURE 5.25: AC response of the proposed amplifier over FFSS process corner

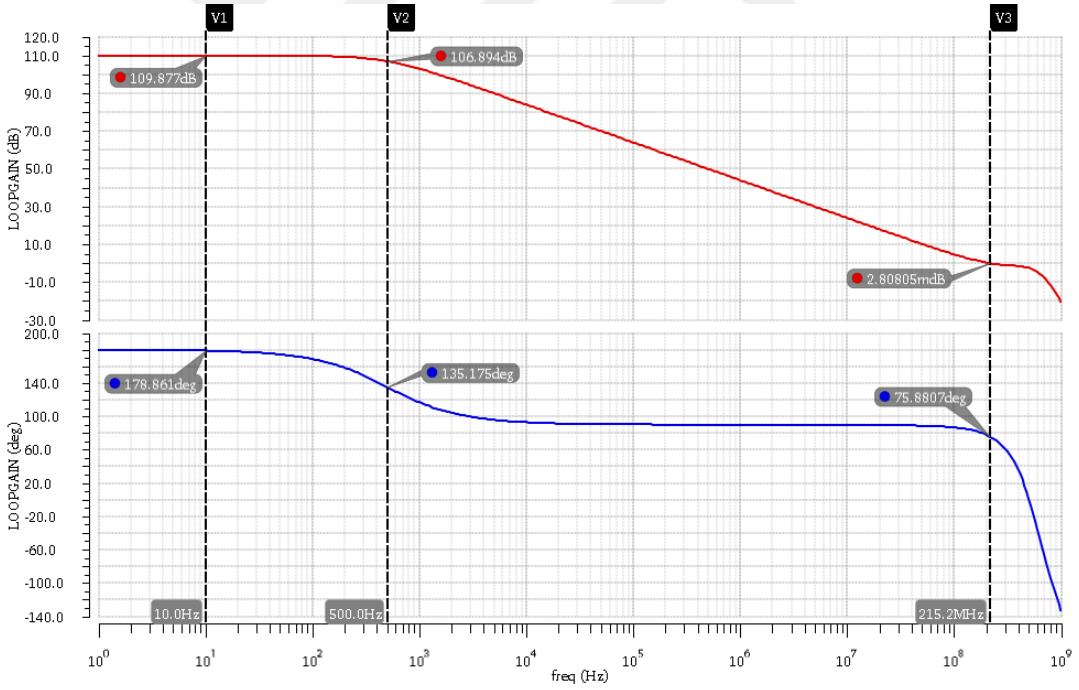

FIGURE 5.26: AC response of the proposed amplifier over SSFF process corner

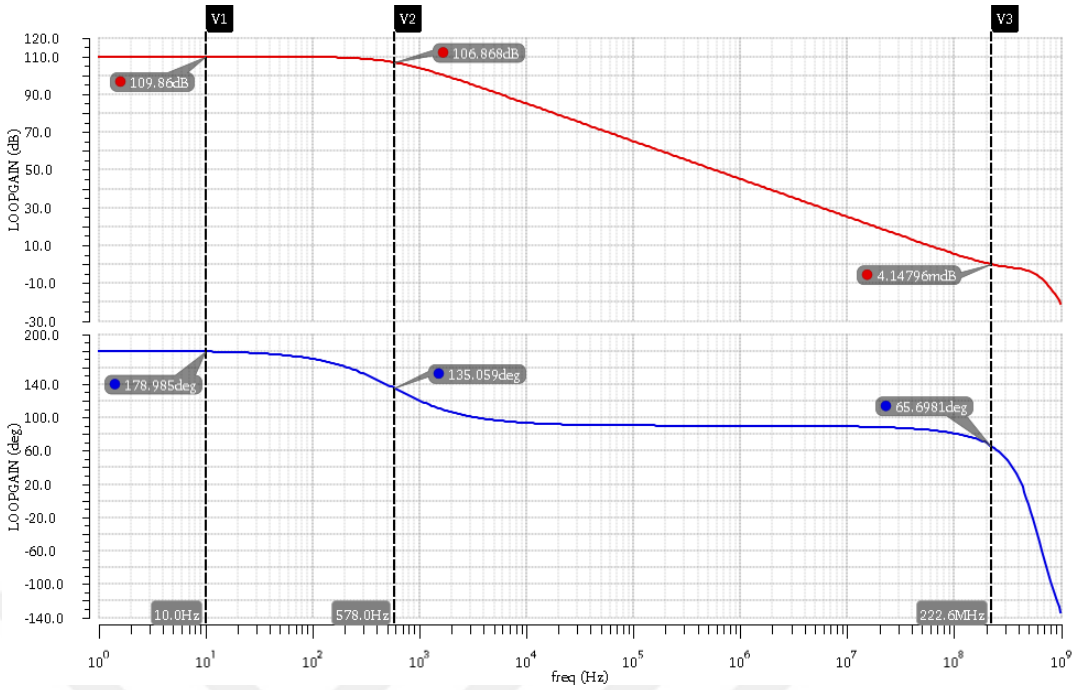

FIGURE 5.27: AC response of the proposed amplifier over SSFS process corner

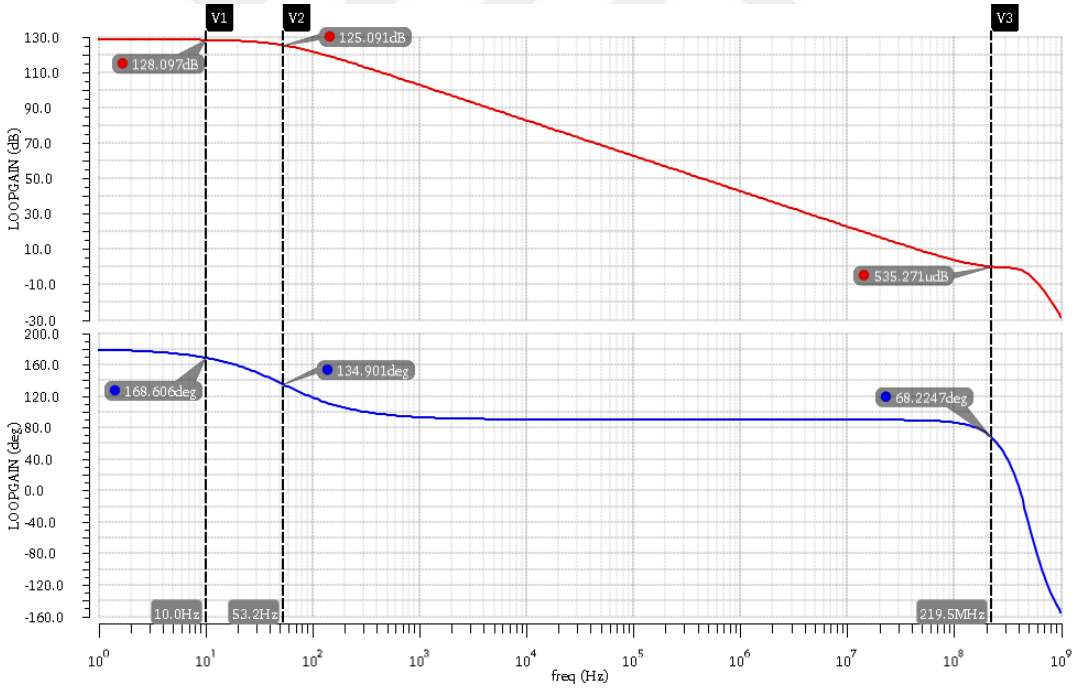

FIGURE 5.28: AC response of the proposed amplifier over SSSF process corner

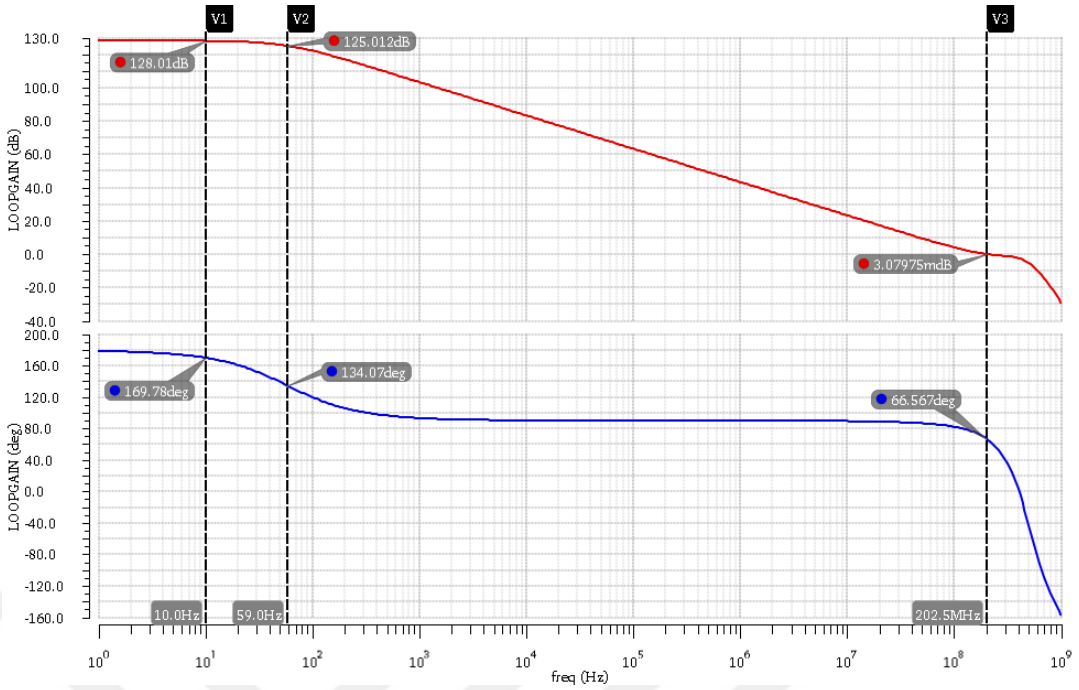

FIGURE 5.29: AC response of the proposed amplifier over SSSS process corner

5.3.2 Noise

The spot noise and total integrated noise of the proposed amplifier over different process corners are presented in this section.

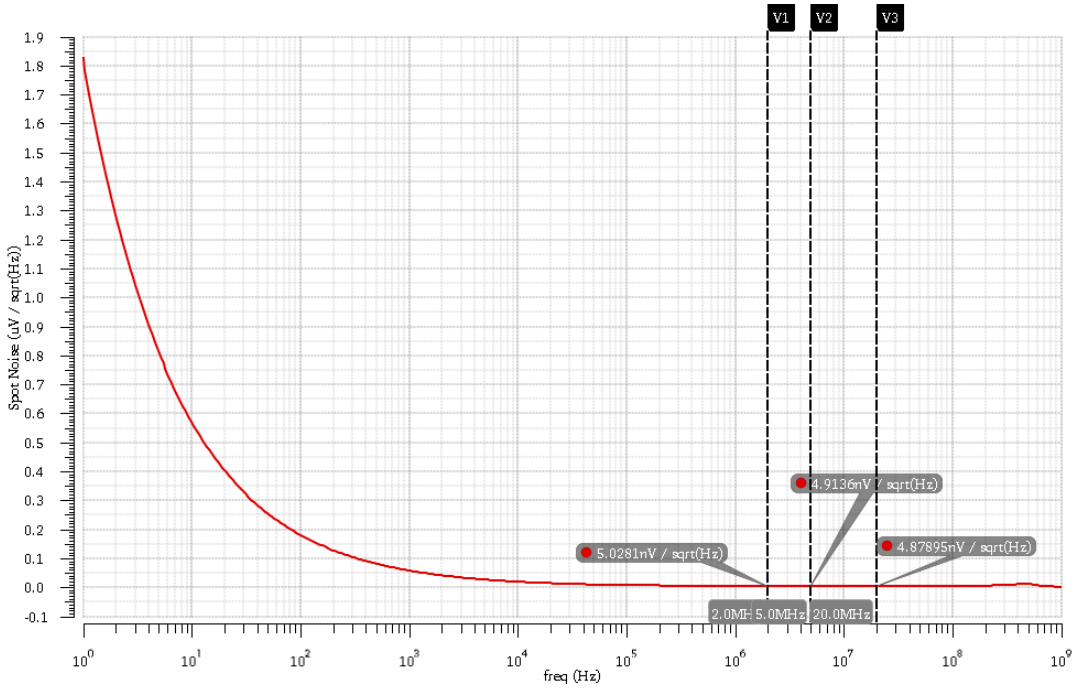

FIGURE 5.30: Spot noise of the proposed amplifier versus frequency over FFFF process corner

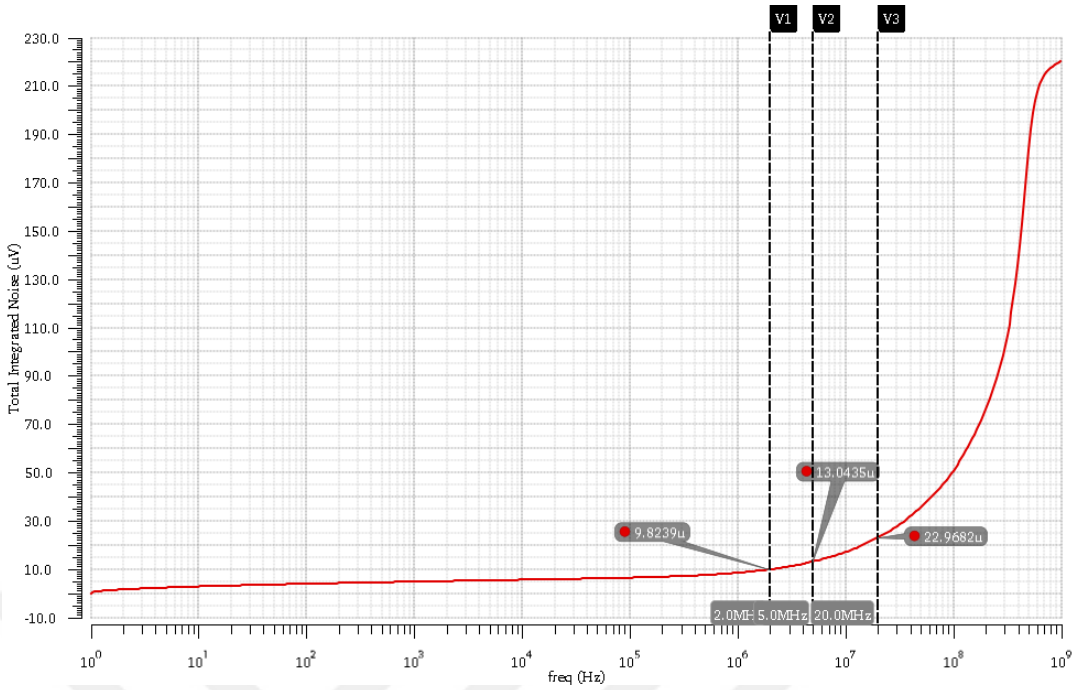

FIGURE 5.31: Total integrated noise of the proposed amplifier versus frequency over FFFF process corner

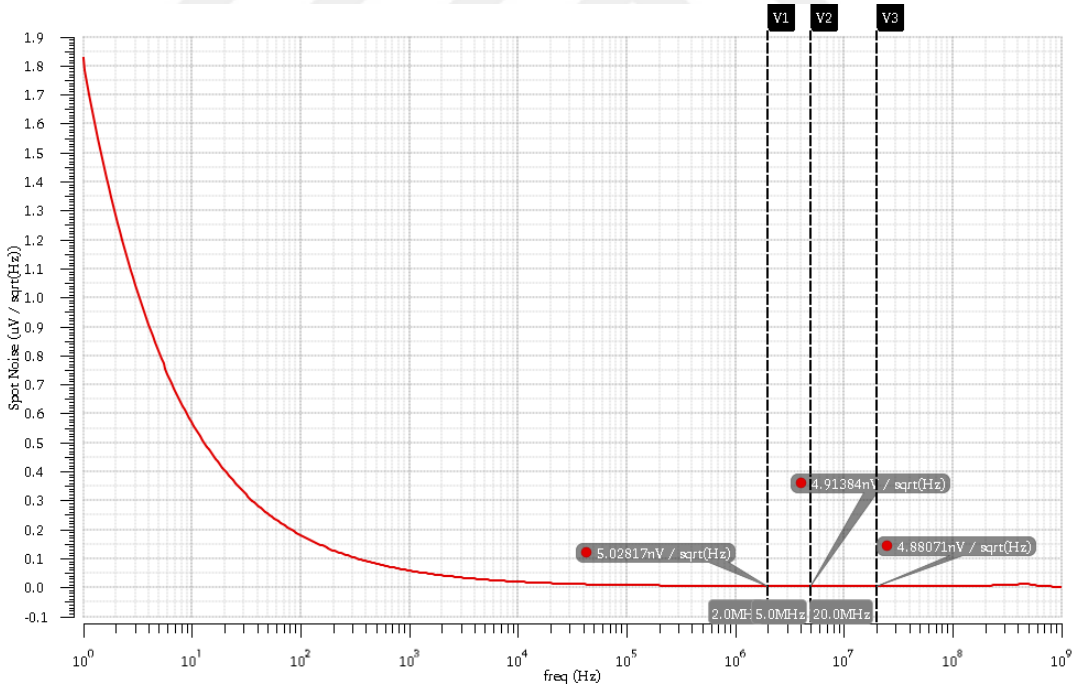

FIGURE 5.32: Spot noise of the proposed amplifier versus frequency over FFFS process corner

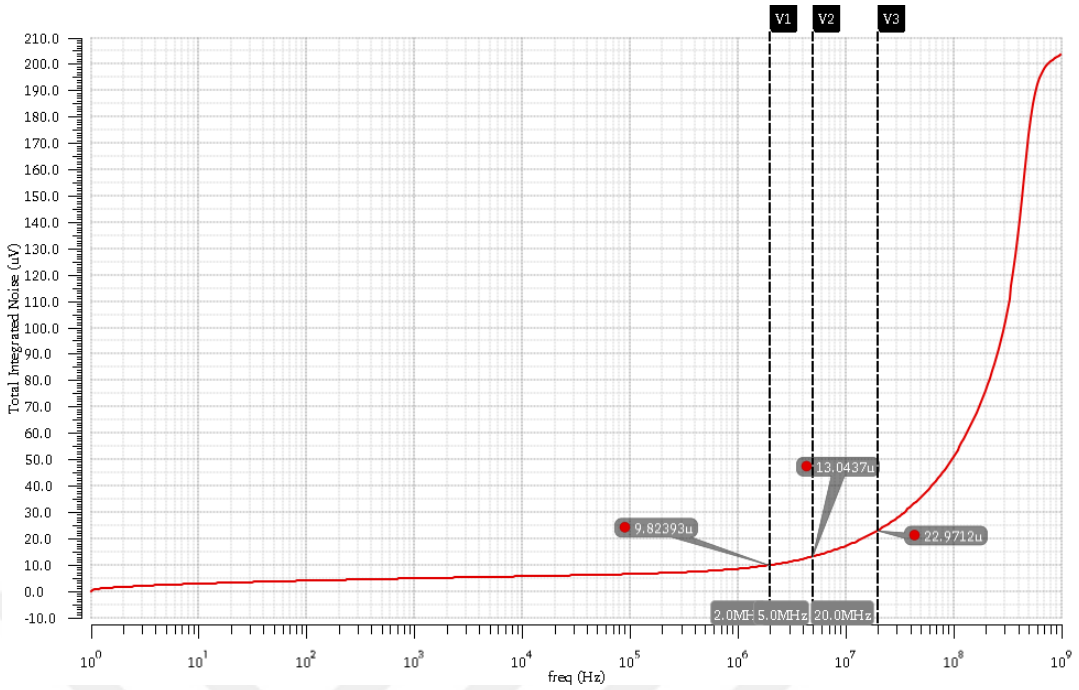

FIGURE 5.33: Total integrated noise of the proposed amplifier versus frequency over FFFS process corner

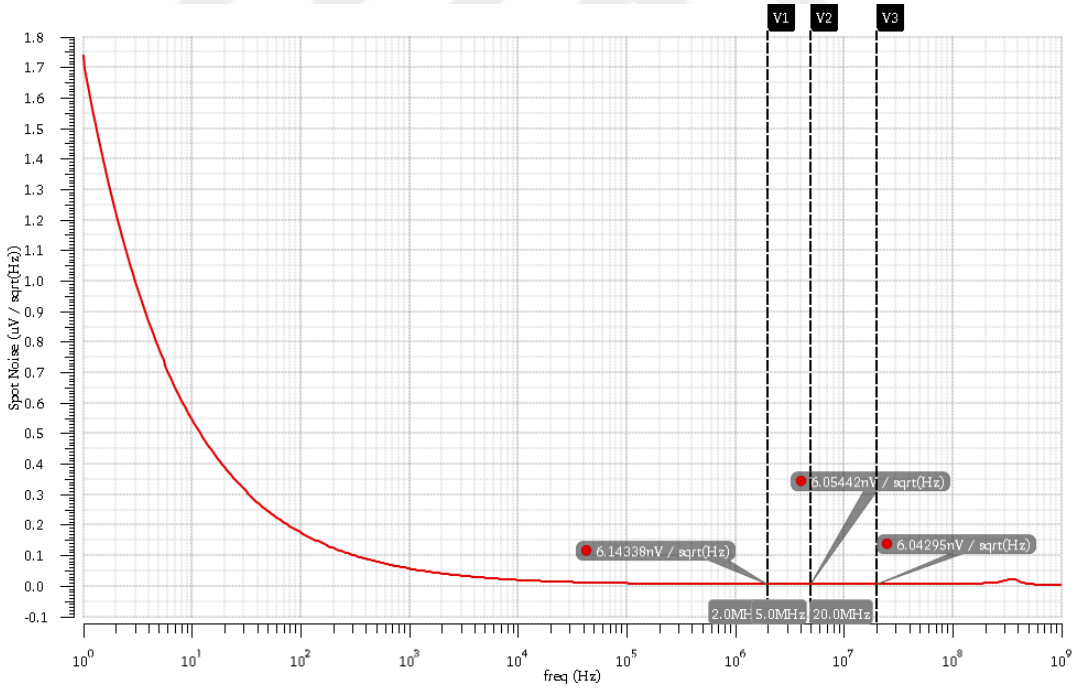

FIGURE 5.34: Spot noise at of the proposed amplifier versus frequency over FFSF process corner

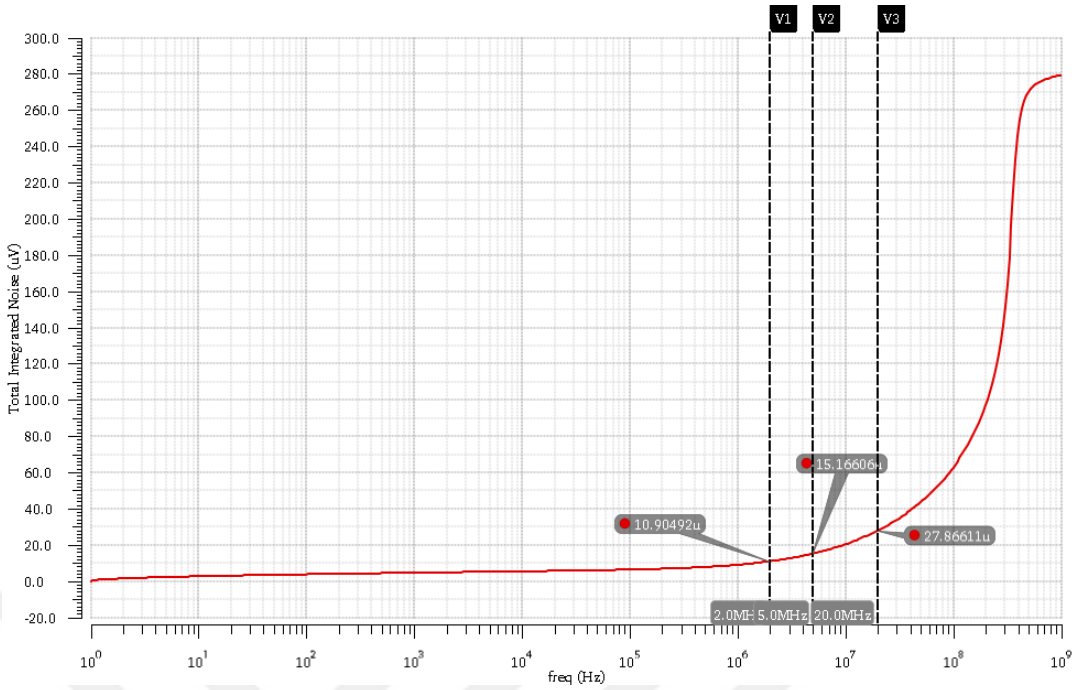

FIGURE 5.35: Total integrated noise of the proposed amplifier versus frequency over FFSF process corner

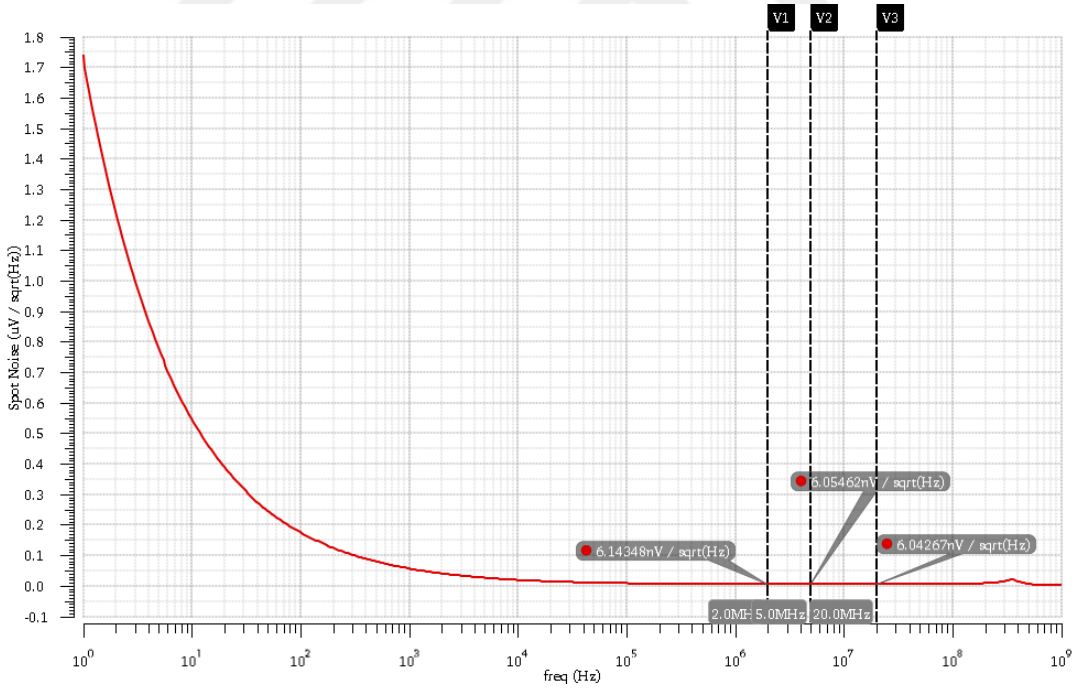

FIGURE 5.36: Spot noise of the proposed amplifier versus frequency over FFSS process corner

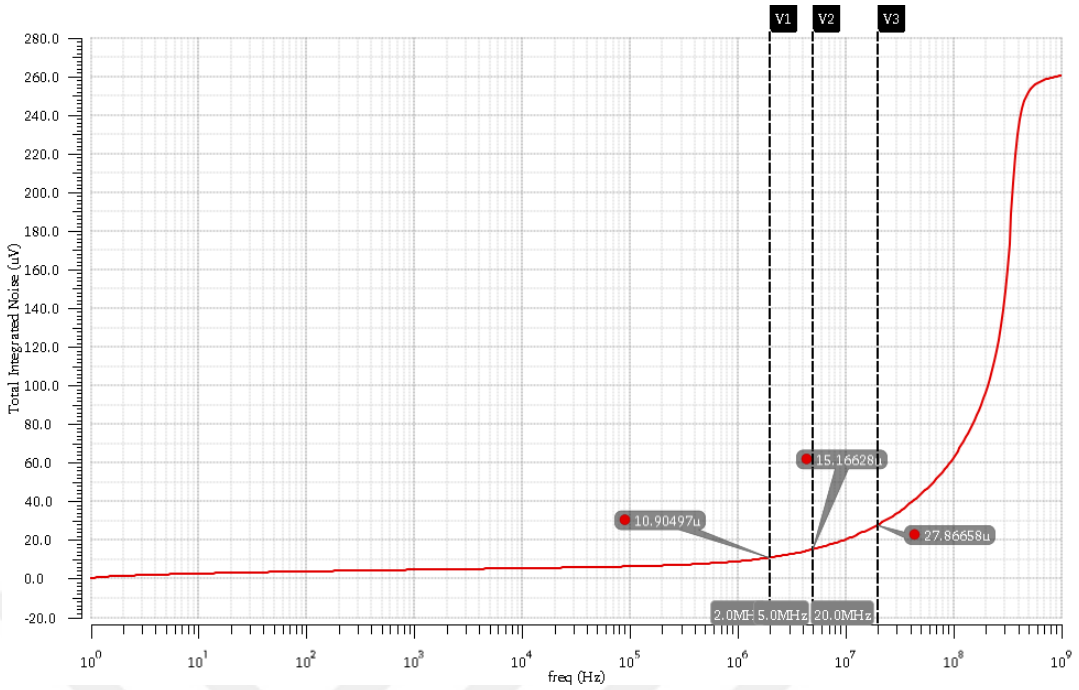

FIGURE 5.37: Total integrated noise of the proposed amplifier versus frequency over FFSS process corner

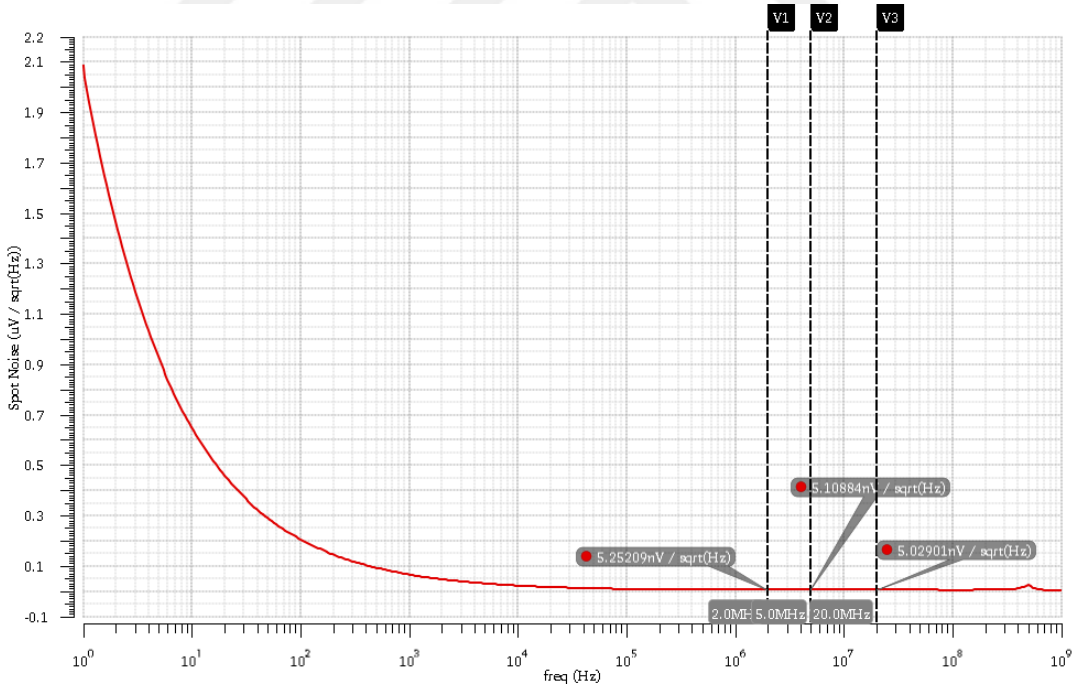

FIGURE 5.38: Spot noise of the proposed amplifier versus frequency over SSFF process corner

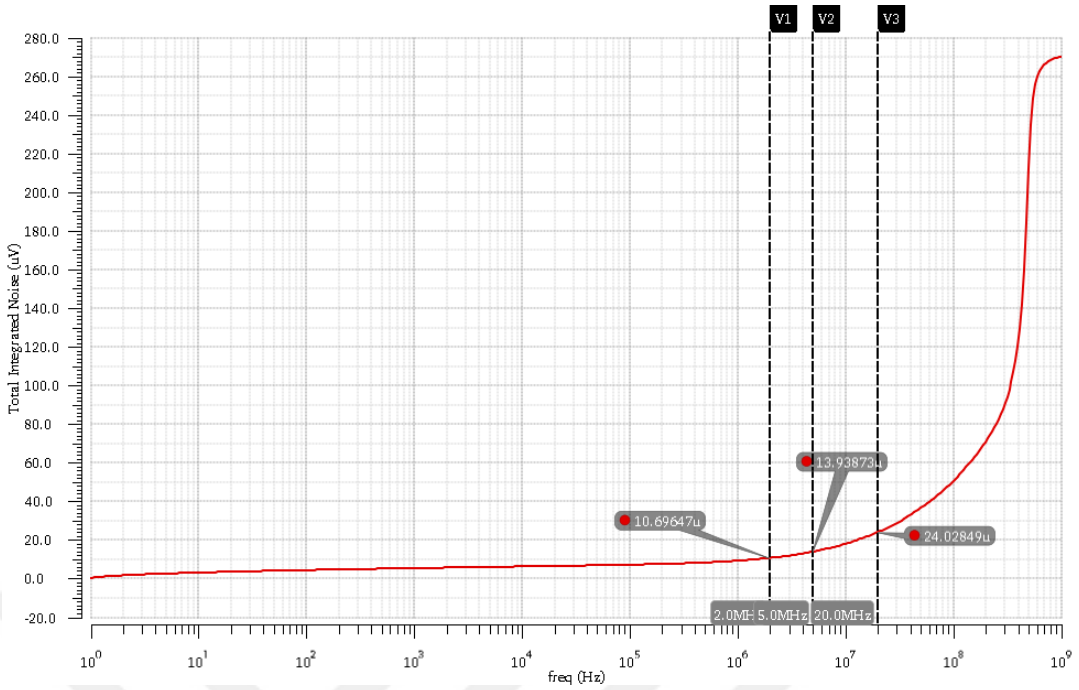

FIGURE 5.39: Total integrated noise of the proposed amplifier versus frequency over SSFF process corner

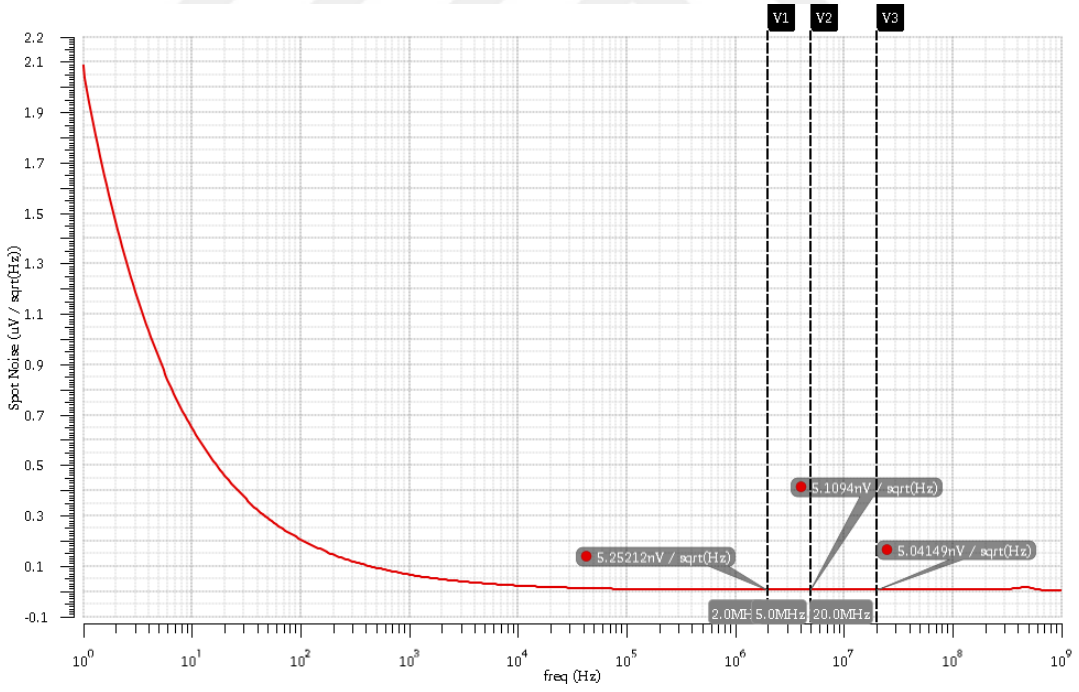

FIGURE 5.40: Spot noise of the proposed amplifier versus frequency over SSFS process corner

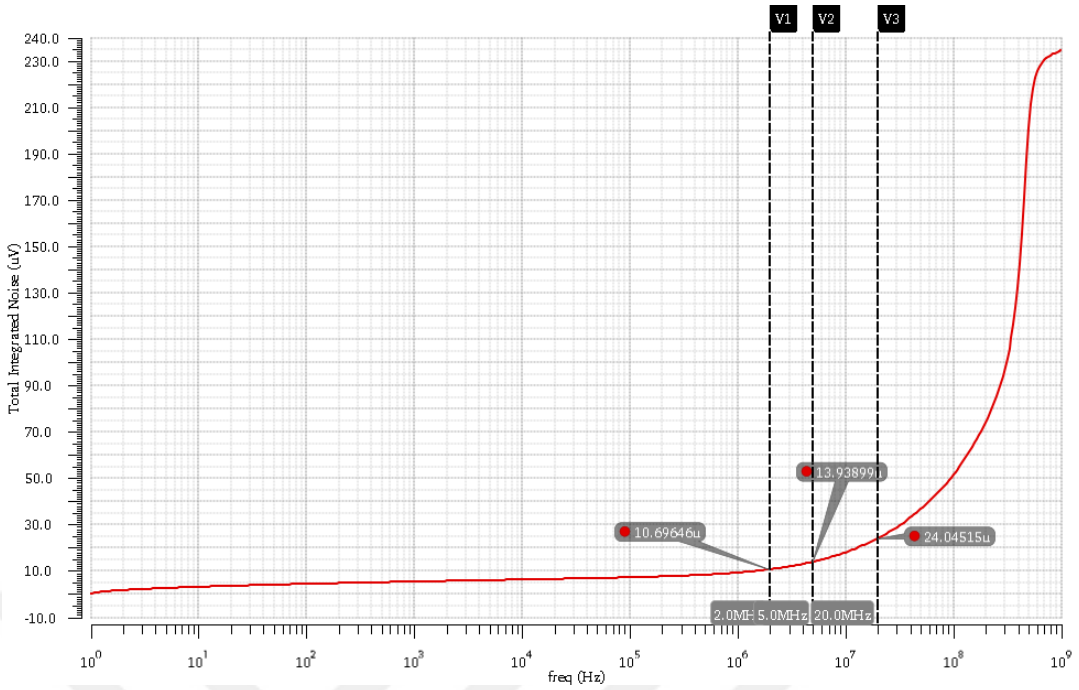

FIGURE 5.41: Total integrated noise of the proposed amplifier versus frequency over SSFS process corner

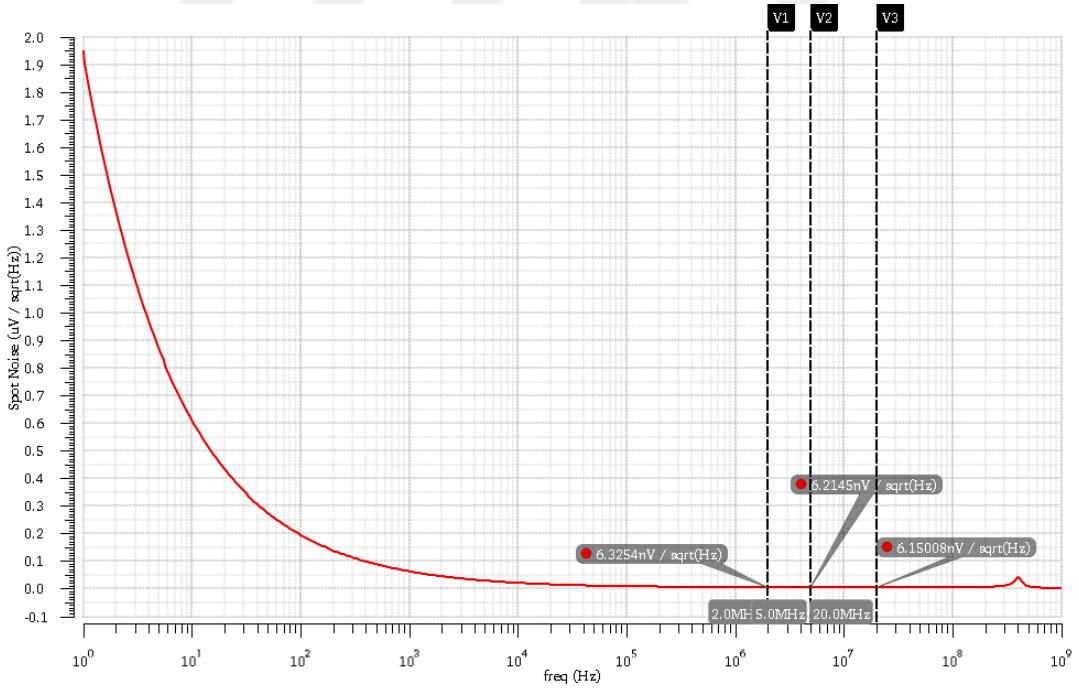

FIGURE 5.42: Spot noise of the proposed amplifier versus frequency over SSSF process corner

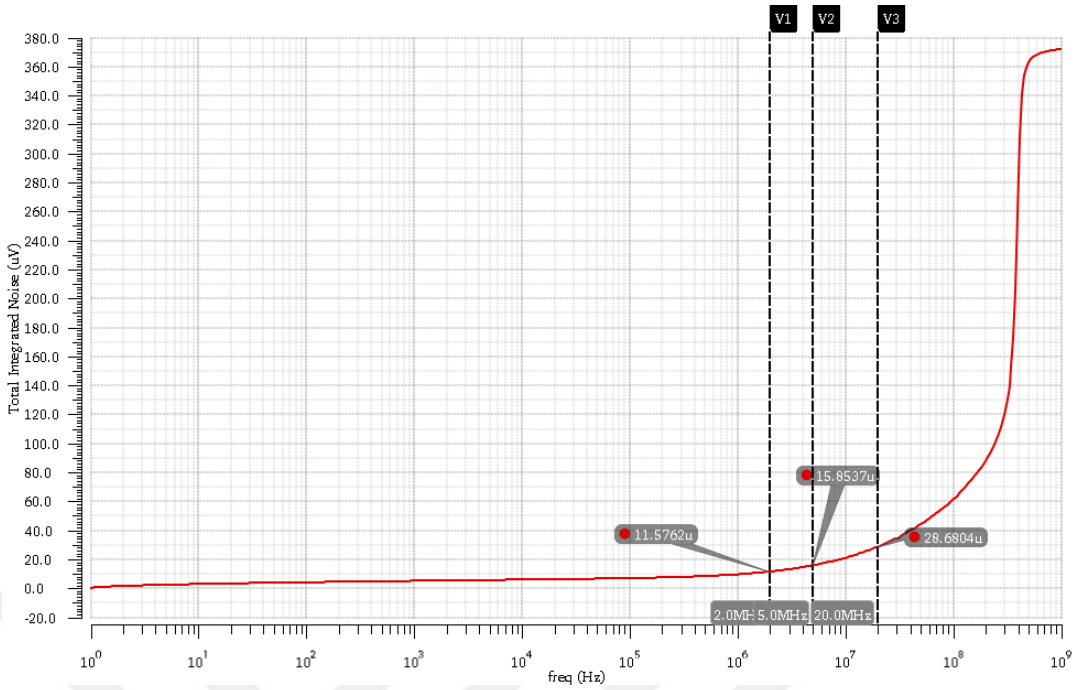

FIGURE 5.43: Total integrated noise of the proposed amplifier versus frequency over SSSF process corner

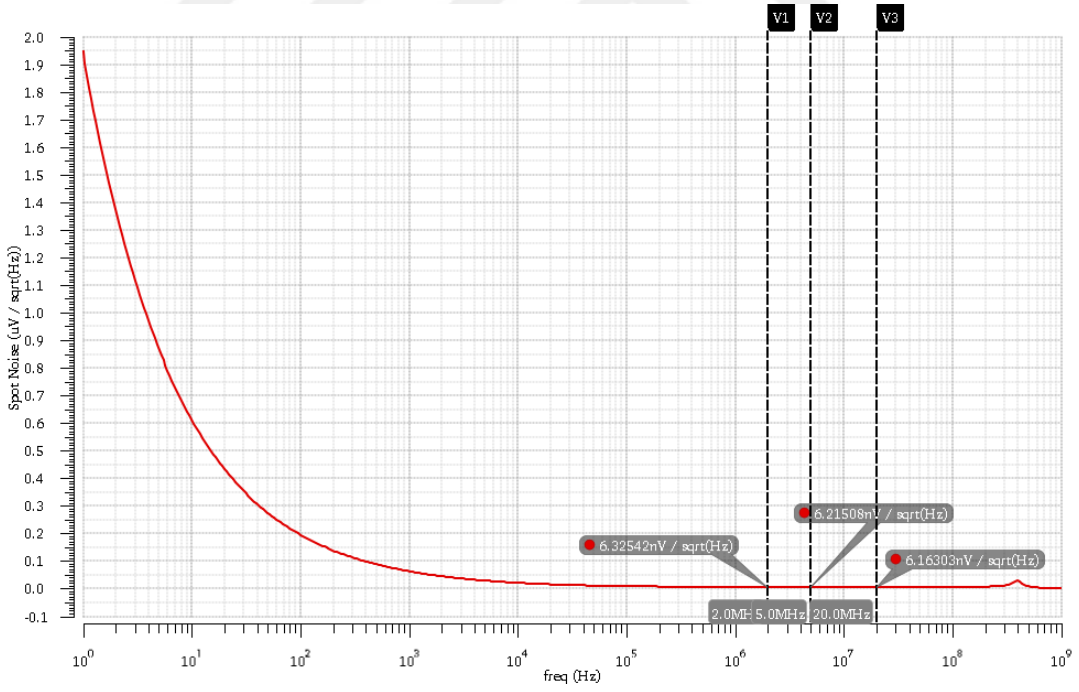

FIGURE 5.44: Spot noise at of the proposed amplifier versus frequency over SSSS process corner

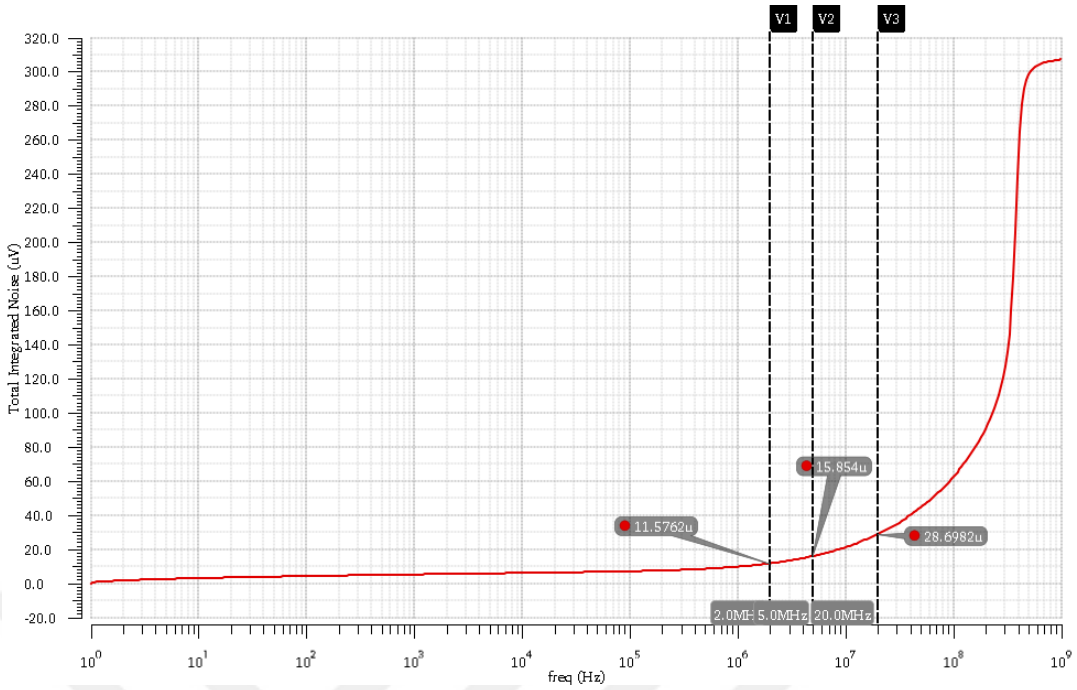

FIGURE 5.45: Total integrated noise of the proposed amplifier versus frequency over SSSS process corner

5.3.3 Total Harmonic Distortion

The THD of the proposed amplifier versus the input signal frequency over different process corners is presented in this section.

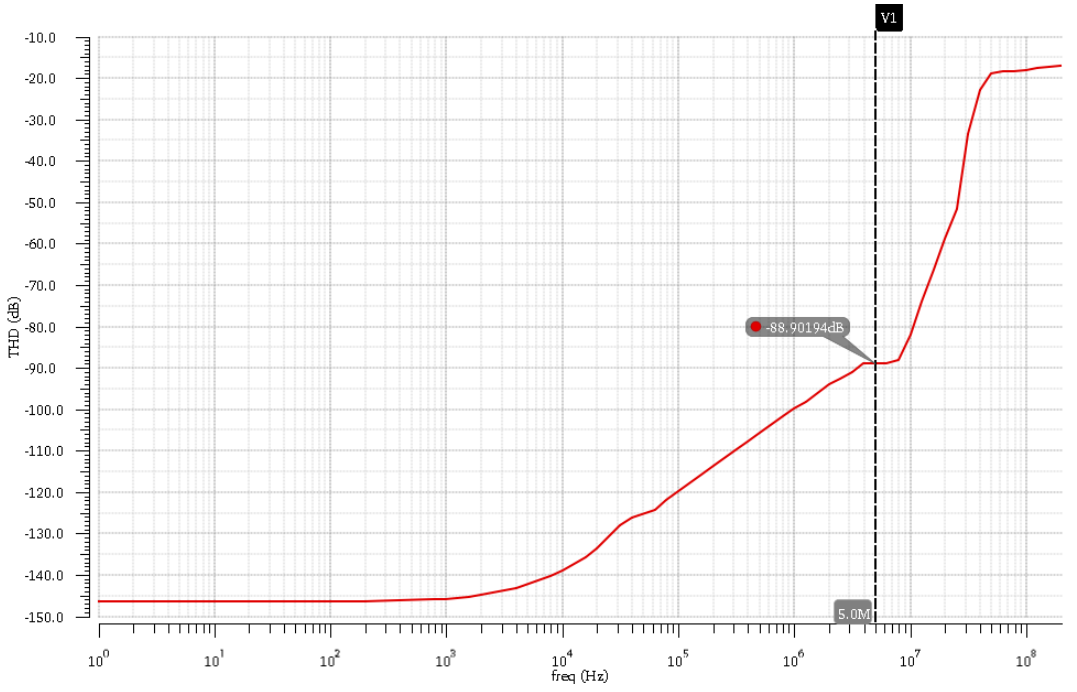

FIGURE 5.46: Total harmonic distortion over FFFF process corner

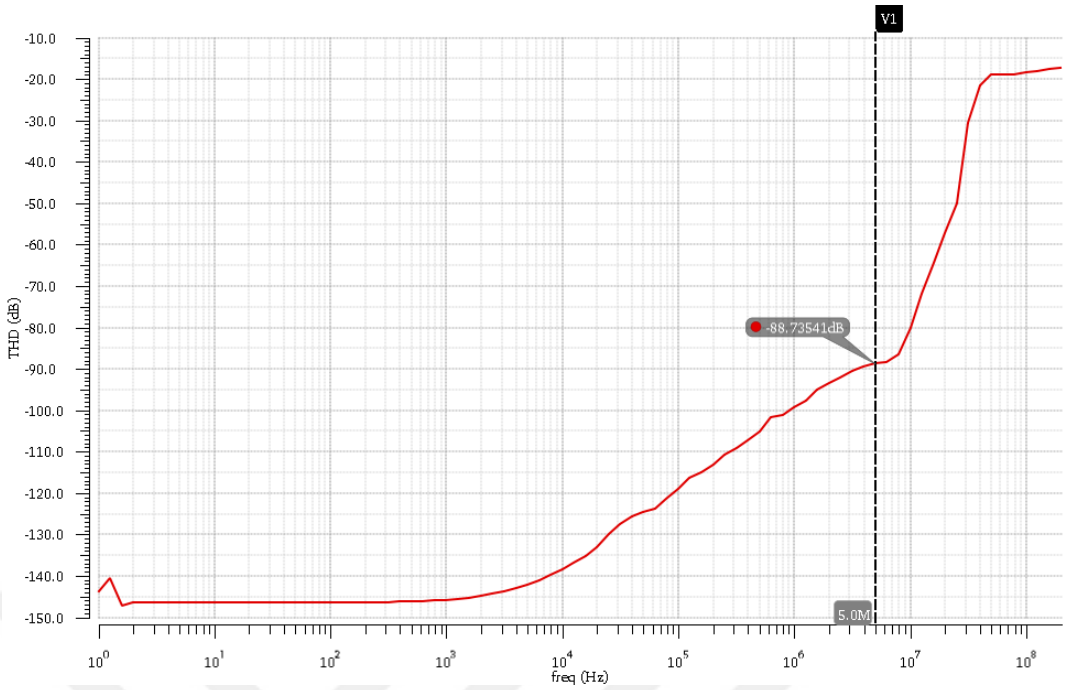

FIGURE 5.47: Total harmonic distortion over FFFS process corner

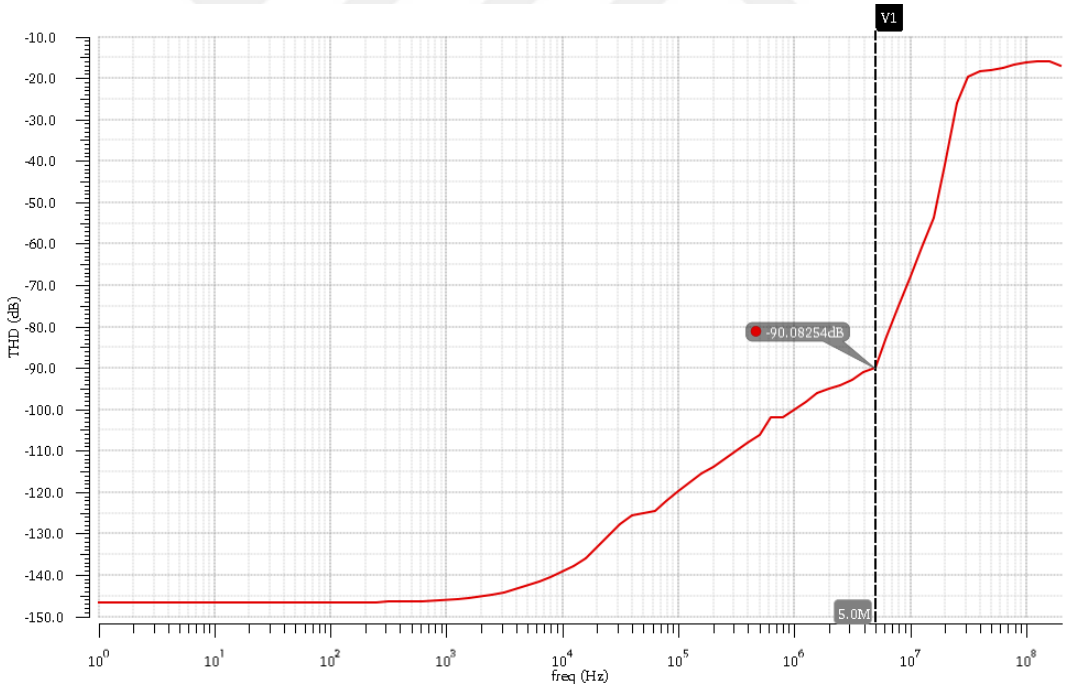

FIGURE 5.48: Total harmonic distortion over FFSF process corner

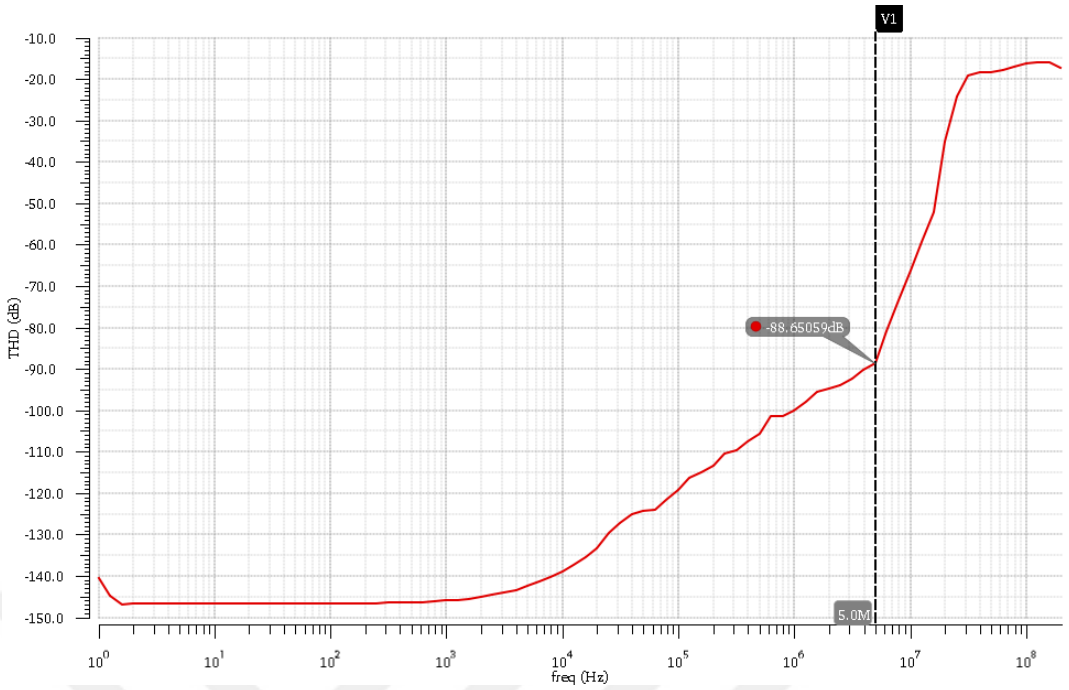

FIGURE 5.49: Total harmonic distortion over FFSS process corner

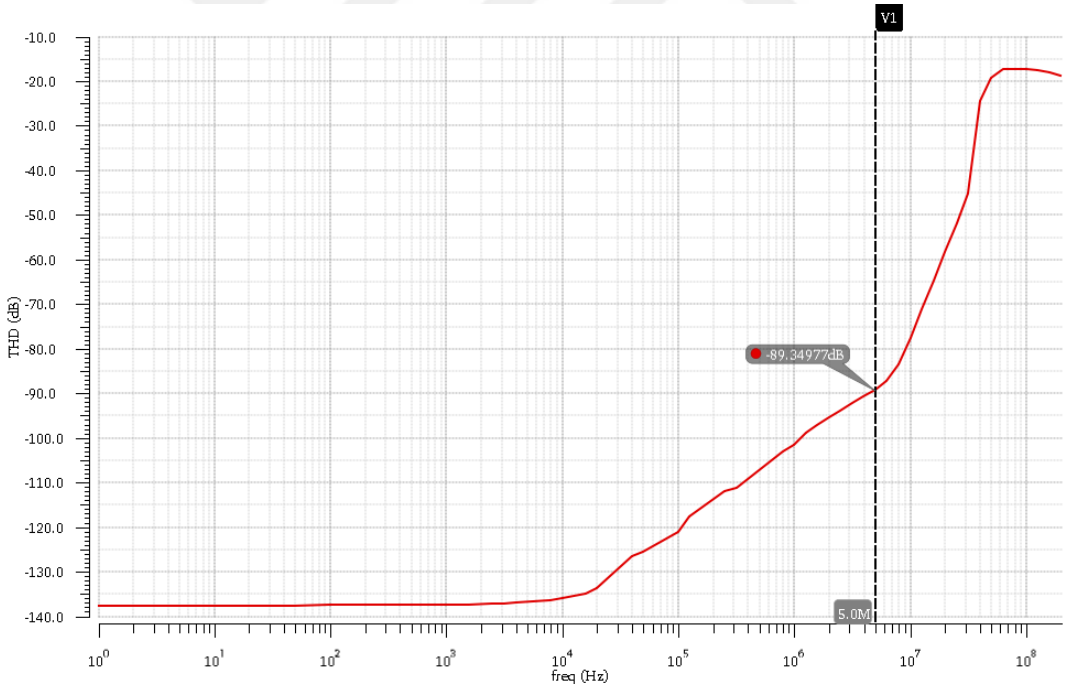

FIGURE 5.50: Total harmonic distortion over SSFF process corner

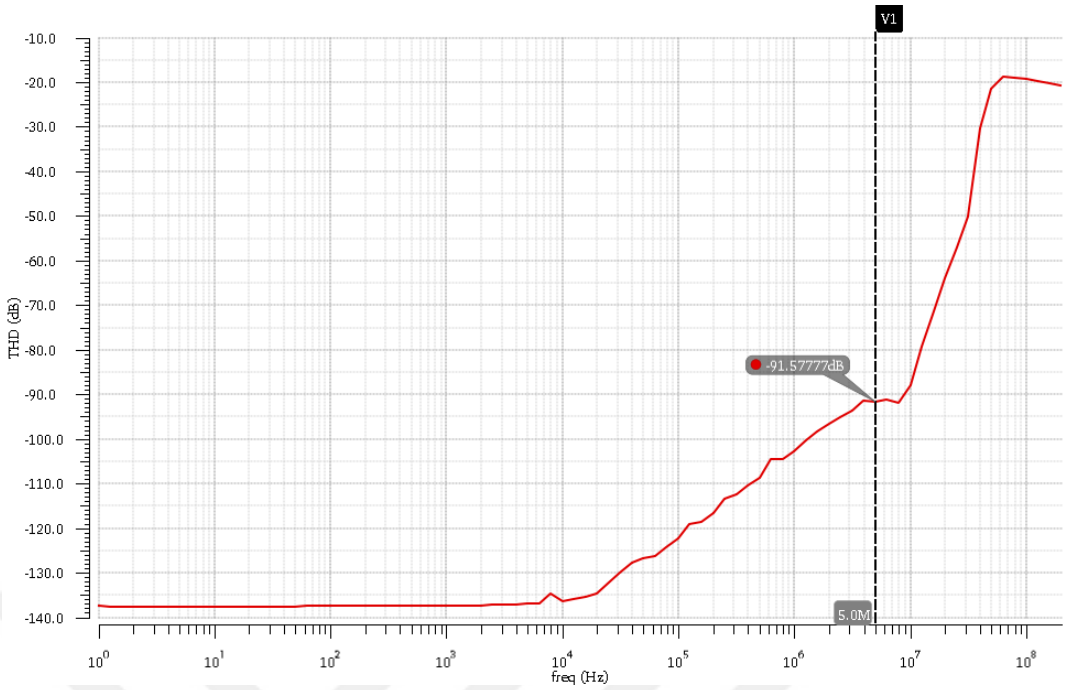

FIGURE 5.51: Total harmonic distortion over SSFS process corner

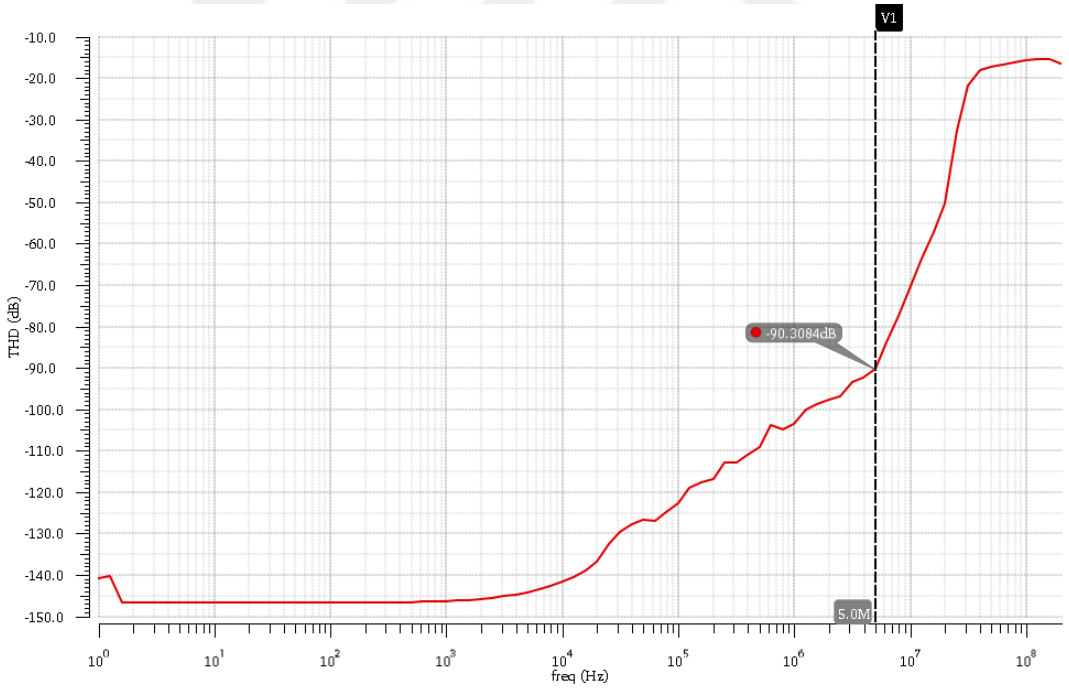

FIGURE 5.52: Total harmonic distortion over SSSF process corner

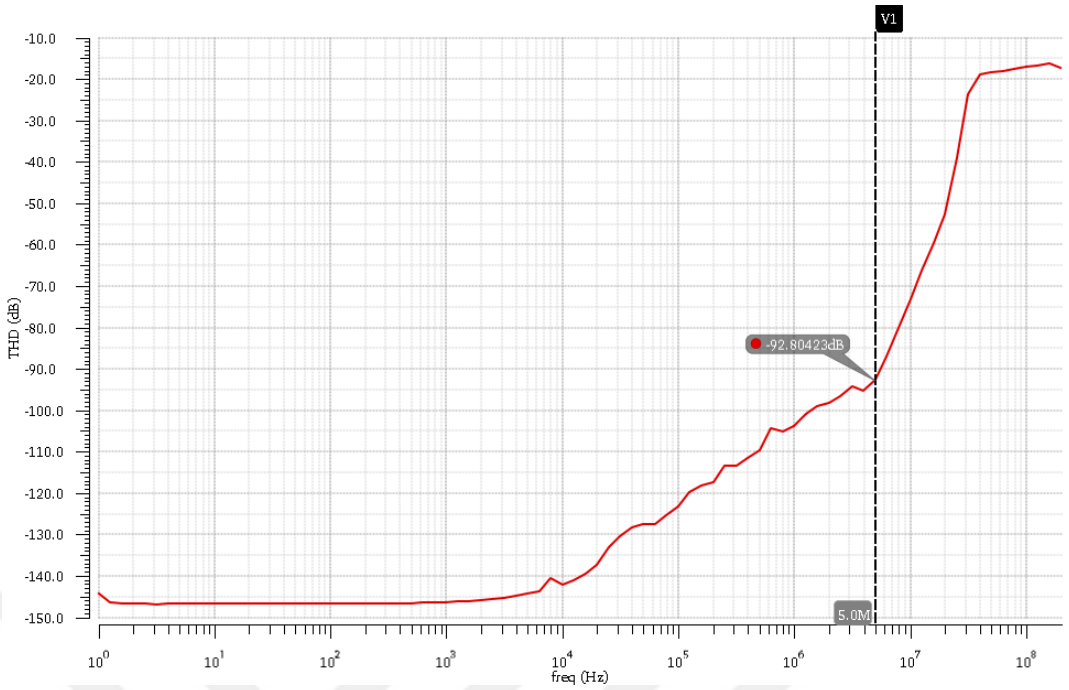

FIGURE 5.53: Total harmonic distortion over SSSS process corner

Table 5.2 summarizes the performance of the proposed amplifier over different process corners.

TABLE 5.2: Amplifier performance over different process corners

Process Corner	UGBW (MHz)	PM (deg)	Spot Noise (nV)	Integrated Noise (μV)	THD (dB)
FFFF	207	68	4.91	13.04	-88.9
FFFS	189	70	4.91	13.04	-88.73
FFSF	198.8	62	6.05	15.16	-90.08
FFSS	175.5	67	6.05	15.16	-88.65
SSFF	215.2	75	5.1	13.93	-89.34
SSFS	222.6	65	5.1	13.93	-91.57
SSSF	219.5	68	6.21	15.85	-90.3
SSSS	202.5	66	6.21	15.85	-92.8

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This work presents a high gain, high bandwidth, wide input common mode range, and highly linear fully differential folded cascode amplifier with large output dynamic range and process corner configurable output stage. The main approach to achieve a wide ICMR in this work is the use of native transistors in the input pair of the amplifier. The amplifier achieves an ICMR from $0.181V$ to $2.945V$ and a closed loop DC gain of $130dB$. Although the amplifier is designed to operate at $5MHz$, the UGBW of the amplifier reaches $200MHz$, while exhibiting a THD of $-92.2dB$ and a spot noise of $5.6nV$ at $5MHz$. The large output dynamic range of the amplifier, which is measured to be $107dB$, is achieved by using rail to rail class AB output stage. By using a corner configurable class AB output stage as well as a corner configurable compensation circuit, the amplifier is ensured to meet the design requirements over different process corners.

6.2 Future Work

The main performance factor in this work was minimizing THD and output referred noise. However, power consumption is of a great importance for evaluating the performance of the amplifier. The next step for this work is to optimize the power consumption of the amplifier.

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