Low Power CMOS Thermometer Sensor with a Bandgap Reference for LSI Applications

A thesis submitted to the
Graduate School of Natural and Applied Sciences

by

Muhammad Arsalan ATHAR

in partial fulfillment for the
degree of Master of Science

in

Electronics and Computer Engineering

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Electronics and Computer Engineering.

APPROVED BY:

Assist.Prof. Hakan Doğan .....
(Thesis Advisor)

Assist.Prof. İhsan Çıçek .....

Prof. Şenol Mutlu .....

This is to confirm that this thesis complies with all the standards set by the Graduate School of Natural and Applied Sciences of İstanbul Şehir University:

DATE OF APPROVAL: 28/05/18

SEAL/SIGNATURE:

Declaration of Authorship

I, Muhammad Arsalan ATHAR, declare that this thesis titled, "Low Power CMOS Thermometer Sensor with a Bandgap Reference for LSI Applications" and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signed: 

Date: 23/05/18

Low Power CMOS Thermometer Sensor with a Bandgap Reference for LSI Applications

Muhammad Arsalan Athar

Abstract

Life-assisting medical devices such as CMOS (LSIC)s, which operate with low power and occupy a minimum area for long time operation and minimum cost, are becoming more and more important in health care industry. Most of the life log devices use two major blocks containing thermometer sensor along with bandgap circuits. These on-chip voltage reference(BGC)s and temperature sensors are the most fundamental blocks for analog circuits that play an important role in internet of things or low cost system on chip applications. Moreover, voltage references are very common in mixed-signal designs such as ADCs, DACs, PLLs and most significantly used in power management circuits. Regarding the second part related to on-chip thermometer sensors, CMOS based thermometers are prominent for their small area using low power consumption. These sensors are employed in thermal applications to monitor the features of the circuits in terms of temperature variation at process corners and mismatches. In this thesis, we explain the design of a thermometer circuit that utilizes a BGR for low cost, low power applications. The proposed CMOS thermometer sensor enunciates a linear characteristic between temperature range from $-40°C$ to $125°C$ with an inaccuracy of $3°C$. This circuit operates for voltage supply ranges from 0.6 to 0.8V and with a static power consumption of 64nW at typical $27°C$. The circuit utilizes the temperature dependency of threshold voltage of MOSFET. Results of the sensor is verified across different corner and mismatch cases with Monte Carlo Simulations. In the second part of the thesis, two low power (BGC)s designs in CMOS 65nm technology, which are optimized for low power, and area, are presented. First design can generate a reference voltage between temperature ranges $-40°C$ to $125°C$ with 2mV inaccuracy. Temperature Coefficient for this design is around 62ppm/°C and the PSRR is 57dB @ 1 KHz in the supply range from 1V to 2V. The design consumes $5\mu W$ in the overall temperature range. Second design works in the same temperature range of $-40°C$ to $125°C$ with an uncertainty of 8mV. Temperature coefficient is approximately 111ppm/°C and the PSRR is 33.3dB @ 1 KHz between 1.2V to 2V supply voltage range. Power consumption is less than $1\mu W$ and requires much less area compared to the first design. Both designs are simulated using Cadence Spectre using UMC 65nm CMOS technology.

Keywords: CMOS Thermometer, Low Power Bandgap, LSI, Temperature Sensors, Voltage References

LSI Uygulamaları için Düşük Güç Tabanlı Geniş Bant ve Termometre Sensörü

Muhammad Arsalan Athar

Öz

Düşük güç tüketimine sahip, minimum alan kullanan ve düşük fabrikasyon maliyetiyle uzun sure çalışan CMOS LSI gibi yaşam destekli tıbbı cihazlarına ilgi sağlık sektöründe giderek artmaktadır. Yaşam boyu kullanımı olan cihazların çoğunda termal sensör ve geniş bant aralığı devreleri içeren iki ana blok kullanılır. Chip-üstü gerilim referans BGR ve sıcaklık sensörleri nesnelerin internet (IoT) ve düşük maliyetli SOC uygulamalarında önemli rol oynayan analog devrelerin en temel kısımlarıdır. Dahası, gerilim referans devreleri ADC, DAC ve PLL gibi karışık sinyal tasarımlarında da çok yaygındır ve en önemlisi güç yönetim devrelerinde kullanılmaktadırlar. Tezin ikinci kısmında değinilen çip-üstü sıcaklık sensorleriyle ilgili olaral, CMOS tabanlı termometreler düşük güç tüketimi ve küçük alanlarıyla ön plana çıkmaktadırlar. Bu sensörler thermal uygulamalarda süreç köşelerinde sıcaklık değişimi ve uyuşmazlıkları değişimini izlemek için kullanılmaktadır. Bu tezde, düşük maliyetli ve düşük güç kullanımına sahip uygulamalar için BG referansı kullanan bir termometre devresi tarasımı açıklanmaktadır.

Önerilen CMOS termometre sensörü, $-40°C$ ila $125°C$ aralığındaki sıcaklıklarda ve $3°C$'lik yanlışlıkla doğru doğrusallık göstermektedir. Bu devre 0.5 ila 0.8 V aralığında çalışmakta ve $27°C$ de 64nW güç tüketimine sahiptir. Devre, tek nokta kalibrasyonlu MOSFET'in eşik voltajının sıcaklığa bağımlılığını faydalı hale getirmektedir. Sensör sonuçları farklı küvşelerde ve uyumsuzluklarda test edilip doğulanmıştır. Sıcaklı sensörüyle çalışacak şekilde iki BGR devresi de önerilmiş ve tasarlanmıştır. Ilk tasarım -40 Â°C ila 125Â°C arasında çalışacak şekilde tasarlanmış olup, 2mVlik yanlışlık ile sonu vermektedir. Sıcaklık katsayısı ise 62ppm/°Cdir. Bu tasarımın PSRR değeri 1V ila 2V aralığında, 1KHzâte 33.9dBâdir, ve güç tüketimi yaklaşık olarak 5uW. Ikinci tasarım ise $-40°C$ ila $125°C$ sıcaklık aralığında 8mV hata oranı ile çalışmaktadır. Sıcaklık katsayısı 111ppm/°Cdir. PSRR değeri ise 1KHz 1.2V ve 2V aralığında 33.3dB. Güç tüketimi 1uW düşüktür. Sistem UMC 65nm CMOS teknolojisine sahip Cadence analog ve dijital tasarım araçları kullanılarak tasarlanmış ve simüle edilmiştir.

Anahtar Sözcükler: CMOS termometre, Düşük Güç Bant Aralığı, LSI, Sıcaklı Sensörleri, Gerilim Referansları

To Allah, the creator.

Acknowledgments

I would like to express my profound gratitude and appreciation to my research Advisor Prof. Hakan Doğan. Without his guidance, encouragement and continuous motivation this would not have been possible to complete my Master's degree in Electrical Engineering from İstanbul Şehir University. I could not think of having an advisor and mentor better than him. He inspired me to render best of my contribution in the field of RF Mixed Signal Designs. My sincere most thanks also goes to Prof. Mustafa Aktan who taught me courses and remained my academic instructor. Beside my career advisors I would like to extend my warmest thanks to Assist.Prof. İhsan Çıçek, and Prof. Şenol Mutlu for taking out time and being a part of my thesis committee.

Thanks to my friend Yasir and Fahd Khan for always being so helpful whenever I needed him. I am forever thankful to my dearest Cousin Muhammad Nabeel Asghar for their unparalleled love and support. I am also very thankful to my RF Lab team members, including Hasan El Gibaly, Mohamed Kamar, Amr Mozammil and Ramy who despite being overloaded with their work, always took time to help me develop circuit design skills that was much needed for the thesis. Thanks to Taha, Abdullah, Sajid, Toqeer, Sikander, Junaid, Rafay, Arsalan and Naveed and all those Turkish friends Zeliha Donmez and Zeynep Bostan who contributed to my wonderful experience in Istanbul.

Finally thanks to my friend Ali Uzun for Turkish translation of the abstract and keyword.

This thesis was supported by Tubitak under the project with number 215E289.

Contents

List of Figures

List of Tables

Abbreviations

AC	**A**lternating **C**urrent
ADC	**A**nalog to **D**igital **C**onverter
BJT	**B**ipolar **J**unction **T**ransistor
BGR	**B**and **G**ap **R**eference
BGC	**B**and **G**ap **C**ircuit
BW	**B**andwidth
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CS	**C**ommon **S**ource
CTAT	**C**omplementary **T**o **A**bsoulute **T**emperature
PTAT	**P**ropotional **T**o **A**bsoulute **T**emperature
DAC	**D**igital to **A**nalog **C**onverter
DC	**D**irect **C**urrent
IC	**I**ntegrated **C**ircuit
LDO	**L**ow **D**ropout **V**oltage
LSIC	**L**arge **S**cale **I**ntegration **C**ircuit
MOS	**M**etal **O**xide **S**emiconductor
MC	**M**onte **C**arlo
NMOS	**N**-channel **M**etal **O**xide **S**emiconductor
OTA	**O**perational **T**ransconductance **A**mplifier
PPM	**P**arts **P**er **M**illion
PMOS	**P**-channel **M**etal **O**xide **S**emiconductor
PSRR	**P**ower **S**upply **R**ejection **R**atio
RTD	**R**esistance **T**emperature **D**etectors
SVT	**S**tandard **T**hin **O**xide **T**hreshold **V**oltage
TC	**T**emperature **C**oefficient

TECH	**T**echnolgy
TSMC	**T**aiwan **S**emiconductor **M**anufacturing **C**ompany
UMC	**U**nited **M**icroelectronics **C**orporation
VDD	**S**upply **V**oltage
VDS	**D**rain **S**ource **V**oltage
VNTC	**V**oltage **N**egative **T**emperature **C**oefficient
VPTAT	**V**oltage **P**ropotional **T**o **A**bsolute **T**emperature
VOUT	**O**utput **V**oltage
VREF	**R**eference **V**oltage
VT	**T**hermal **V**oltage
VTH	**T**hreshold **V**oltage

Chapter 1

Motivation

1.1 Thesis Motivation

- In modern technology, there is a big demand for CMOS based temperature sensors to be used in thermal management. These solutions are used in various fields such as industrial, medical, space and defense systems.
- A wide use of temperature sensors are built on bipolar junction based transistors (BJTs).
- The accuracy of BJT sensors are usually limited due to the effect of saturation currents. In addition, they usually require more power and are bulky.
- CMOS based thermometer designs which have less complexity and low power, have been explored in this design.
- Additionally, design of BGRs were explored to be used with the temperature sensor as a reference.
- Main design consideration for the BGR is to achieve low power operation in the micro or nano-watt region for smart sensors or medical applications.
- Two BGR designs are proposed that meet the target specifications.

1.2 Thesis Objective

The main objective of this thesis is to develop a CMOS thermometer sensor and a bandgap circuit with new proposed designs to reduce the power consumption and the area of the chip. The proposed CMOS thermometer sensor enunciates a linear characteristics between temperatures range from $-40°C$ to $125°C$ with inaccuracy of $3°C$. This circuit operates from voltage supply ranges from 0.6 to 0.8V and with a static power consumption of 64nW at typical $27°C$. The circuit utilizes the temperature dependency of threshold voltage of MOSFET. Results of the sensor are verified across different corners and mismatches with Monte Carlo simulations. In the second part of the thesis, two low power bandgap reference (BGR) circuits designs in CMOS 65nm technology, which are optimized for low power and area, are presented. First Design can generate a reference between temperature ranges $-40°C$ to $125°C$ with 2mV inaccuracy. Temperature Coefficient for this design is around 62ppm/°C and the PSRR is 57dB @ 1 KHz in the supply range from 1V to 2V. The design consumes $5\mu W$ in the whole temperature range. Second design works in the same temperature range of $-40°C$ to $125°C$ with an uncertainty of 8mV. Temperature coefficient is approximately 111ppm/°C and the PSRR is 33.3dB @ 1 KHz between 1.2V to 2V supply voltage range. Power consumption is less than $1\mu W$ and requires much less area compared to the first design. Both designs are simulated using Cadence spectre using UMC 65nm CMOS technology.

1.3 Thesis Organization

This thesis is organized as follow; Chapter 2 reviews the CMOS based conventional low power thermometer sensors. In addition, it also analyzes the design of bandgap circuits. Chapter 3 proposes the low power thermometer design. Chapter 4 explains the design of the low power bandgap circuit designs. Chapter 5 concludes this work, summarizes the results, and recommends future work for these systems.

Chapter 2

Introduction

2.1 SoC based CMOS Thermometer Sensors

2.1.1 On-chip Thermometer Sensors

Thermometer sensors are often used to measure the temperature in analog or digital devices. There are different types of temperature sensors used in market today. Previously, off chip components such as thermocouplers and RTDs were commonly used for sensing temperature [1]. However, mostly integrated CMOS Sensors are used recently due to their low cost, low power consumption and small area requirements.

2.1.2 Conventional CMOS Based Temperature Measurement

A literature survey illustrates in CMOS technology, different kinds of temperature sensors have been focused in CMOS technology. Most customary temperature based sensors are constructed on bipolar junction transistors (BJTs) [2]. These measuring device estimates temperature by relating a temperature-dependent voltage to a temperature-insensitive voltage. These two voltages are generated by means of two appropriately-defined temperature features of a vertical PNP transistor. First is the complementary-to-absolute temperature (CTAT) aspect of the base to emitter voltage V_{BE} and Second is the proportional-to-absolute temperature (PTAT) element of the difference between two base to emitter voltages V_{BE}. The accuracy of BJT sensor is limited by effect of saturation currents that leads to errors of few degrees. In addition, it requires more

power consumption and area. For this project, the topologies of CMOS designs have been selected on the basis of their less complexity and low power consumption. Out of these topologies, two CMOS designs [3, 4] are shown in Figure 2.1. Sensitivity, which is change in output voltage with respect to the change in temperature is an important key performance indicator (KPI) for our design. After simulating, we decided against the use of these two circuits due to their high sensitivity limitation while reducing power which is more than 2mV. To overcome this constraint, a new design has been proposed with low temperature sensitivity which will be discussed in Chap 3.

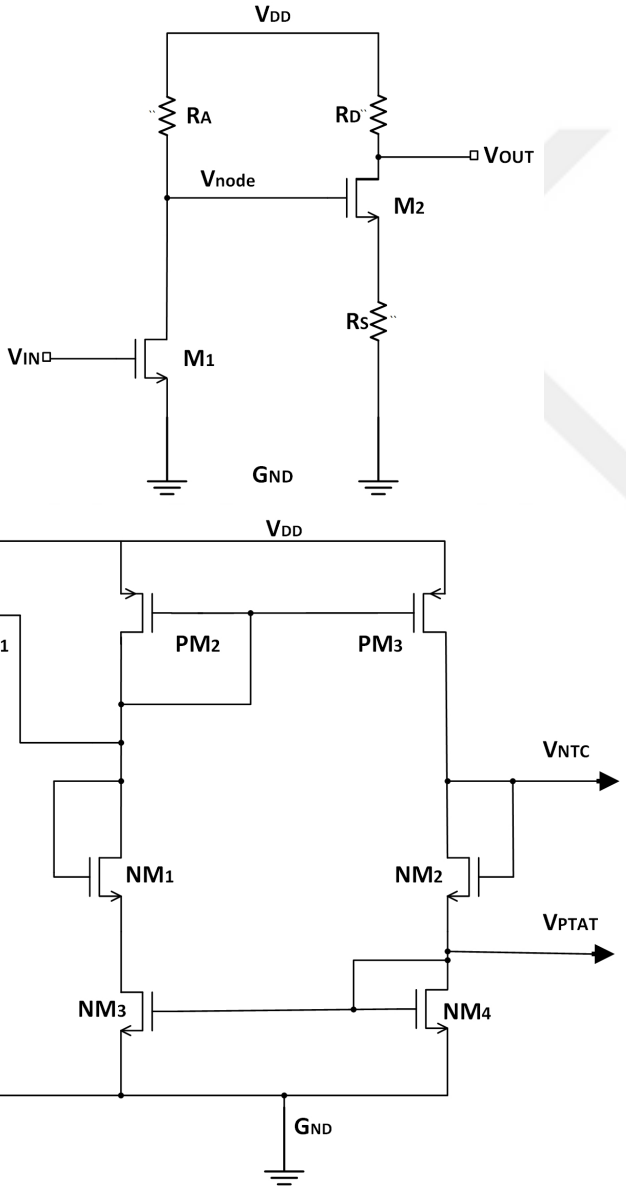

FIGURE 2.1: First design uses two-transistor topology with source degeneration and second design uses PMOS active loads with two outputs VNTC and VPTAT[5].

2.2 Voltage Reference Circuit

2.2.1 Bandgap Reference Circuit

BGRs are one of the basic building blocks of analog, digital and mixed-signal designs. They provide a constant reference voltage for Opamps, LDOs and ADCs regardless of temperature, supply and process variations. There is an enormous demand of low power CMOS BGR circuits due to their use in power management units in RF receivers and transmitters. Literature survey shows that various types of BGRs have been designed in the past. Here Brokaw and classical Widlar BGR circuits are worth-mentioning [6, 7].

2.2.2 Conventional CMOS based BGRs

Most conventional design for CMOS based BGR is shown in Figure 2.2. However, this design is not suitable for ultra-low power and low area solutions. Our main design consideration is to achieve low power even at the cost of larger chip area. We require it to operate in few μ Watts or Nano-Watt range for smart sensors or medical sensors. Conventional designs use relatively high power and large resistors to achieve voltage reference functionality [8]. It produces a voltage of bandgap energy of silicon i.e 1.2V.

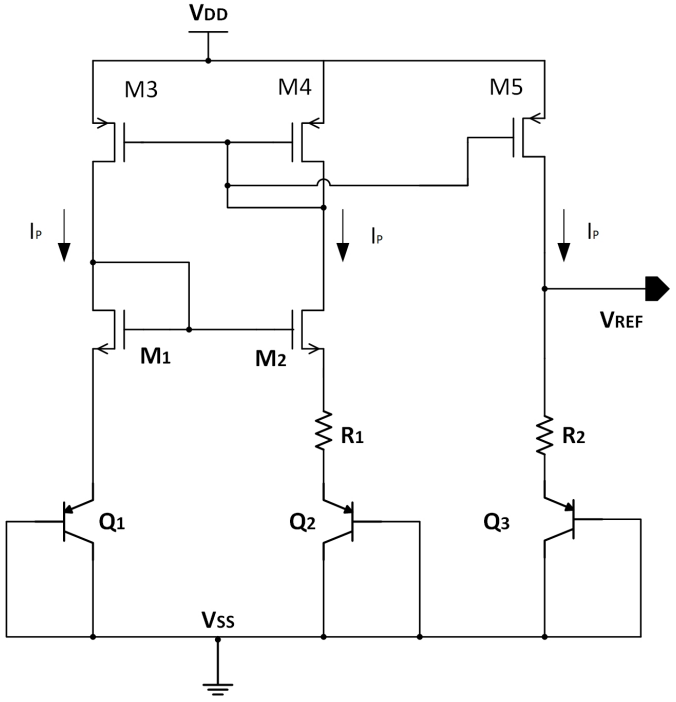

FIGURE 2.2: Conventional CMOS bandgap design using BJTs and resistors.

2.3 Parameters Defining Both Thermometer Sensors and Bandgaps Circuits

2.3.1 Temperature Coefficient (TC)

It is the stability of the generated bandgap Voltage with respect to temperature. The principle of bandgap designs is to equalize the negative (TC) of PN junction with the positive (TC) of the thermal Voltage V_T. TC is measured in ppm/°C.

2.3.2 Power Supply Rejection Ratio (PSRR)

It is the ability of the bandgap to maintain its output voltage against the changes in voltage supply. PSRR is measured in decibels (dB).

2.3.3 Supply Independent Variation

It is the same as Power Supply Rejection Ratio. Cadence parametric analysis has been used to show the behavior of the bandgap circuits in terms of supply independent variation.

2.3.4 Temperature Inacccuracy

The maximum inconsistency from the real value at a certain temperature in a specific range of the thermometer sensor is called the Inaccuracy of the thermometer. This is usually corrected with one point or two point calibration methods. Temperature inaccuracy is measured in degrees Celsius.

2.3.5 Variation Across Process Corners

Corner analysis is the method widely used to simulate and check the design performance for process and parameter variations. Predefined parameter sets (corner models) representing the worst case combinations in terms of circuit parameters are used. The disadvantages of corner analysis include: a) the designer may not know what the critical

corners are in terms of mismatches and correlation parameters b) the possibility that a design may function satisfactorily at the corners but fail within the envelope of the corners [9].

2.3.6 Monte Carlo Simulations

The designer can choose between two non-identical types of parameter variation or use them in conjunction with each other.

Process: This type of Monte Carlo mode simulates the deviation of the electrical parameters originated by unavoidable process instabilities in production. These instabilities disturb all the devices in a circuit in the same manner. Therefore, the process parameters, which are randomly selected in each simulation run, are globally allocated to all device instances in a design.

Matching: The type of variation processes statistical dissimilarities between matched designed devices, which is produced by roughness of edges, variation in doping, effects of boundary, etc. A device with each and every instance owns that takes an individual random value around typical mean. Matching parameters are derived from real measurements of special test typologies circuits that are designed in an optimal way with respect to perfect matching.

Chapter 3

Low Power Thermometer Sensor

This chapter briefly presents the main blocks for low power thermometer design that uses common source degeneration topology[10]. Our purpose is to design the circuit at ultra-low power with decent performance.

3.1 Proposed thermometer Sensor

The design contains two parts. First part consists of the startup circuit and the second part contains the sensing circuit.

3.1.1 Start-Up Circuit

In transient operation, the sensor works in a stable operating region and there are two regions of operation that satisfy this. One is the normal condition when constant DC voltage supply is applied and all the transistors are in active mode to allow the proper functioning of the sensor. The second region is unusual zero current operation. This condition also remains stable and the V_{REF} output becomes 0V. In order to avoid this zero current operation, additional circuitry is used to disrupt this condition. This additional startup circuit does not affect the normal operation of the sensor and turns off after startup.

3.1.2 Sensing Mechanism

For our selected design proposed in Figure 3.1, we obtain current which has a linear relation with varied temperature as shown in Eq.3.1. This is achieved by using a PTAT current source with a resistor Rs. Due to the design's lower voltage characteristics of 0.6V, thin oxide LVT of 0.2V threshold voltage are preferred to overcome the low headroom limitation. In addition to minimize the short channel effects, devices with long channels are chosen. Transistors M1 and M2 are sized in such a way that their drain-source voltages (V_{DS}) are more than $3\phi_t$ (ϕ_t=kT/q), known as the sub threshold V_{TH} MOSFET saturation region.

For $V_{DS} > 3\phi_t$ (ϕ_t=kT/q), The current at drain I_D is given by:

$$I_D = I_o exp((V_{GS} - V_{TH})/n\phi_t)) \tag{3.1}$$

where I_o is the current at drain side when gate-source voltage (V_{GS}) equals V_{TH}:

Since

$$I_o = \mu_o C_{ox}(W/L)(n-1)\phi_t \tag{3.2}$$

W and L are the channel width and length, μ_o is the mobility of the carrier,n is the subthreshold slope factor and C_{ox} is the capacitance of gate oxide. Using Kirchhoffâs voltage law:

$$V_{GS1} = V_{GS2} + I_{OUT}R_S \tag{3.3}$$

Substituting the value of I_D from Eq. 3.1 in Eq. 3.3, we get

$$n\phi_t log_e(I_{REF}/I_o) + V_{TH1} = n\phi_t log_e(I_{OUT}/KI_o) + V_{TH2} + I_{OUT}R_S \tag{3.4}$$

In order to make the currents equal, we have $V_{TH1} = V_{TH2}$, $I_{REF} = I_{OUT}$

Therefore,

$$I_{OUT} = n\phi_t log_e(K/R_S) \tag{3.5}$$

So the output voltage depends upon the Iout as given below,

$$V_{REF} = V_{OV2} + I_{OUT} R_S \tag{3.6}$$

Where K is the constant value to keep the currents equal. V_{OV2} is overdrive voltage of M2 in subthreshold region. Comparing it to conventional PTAT designs discussed in Chapter 2, the sub-V_{TH} voltages allows the use of comparatively smaller resistor [10]. To generate currents in the region of nano nAmperes, a 450K polysilicon resistor R_S is used. The absolute temperature dependence of ϕ_t provides a PTAT I_{OUT} current.

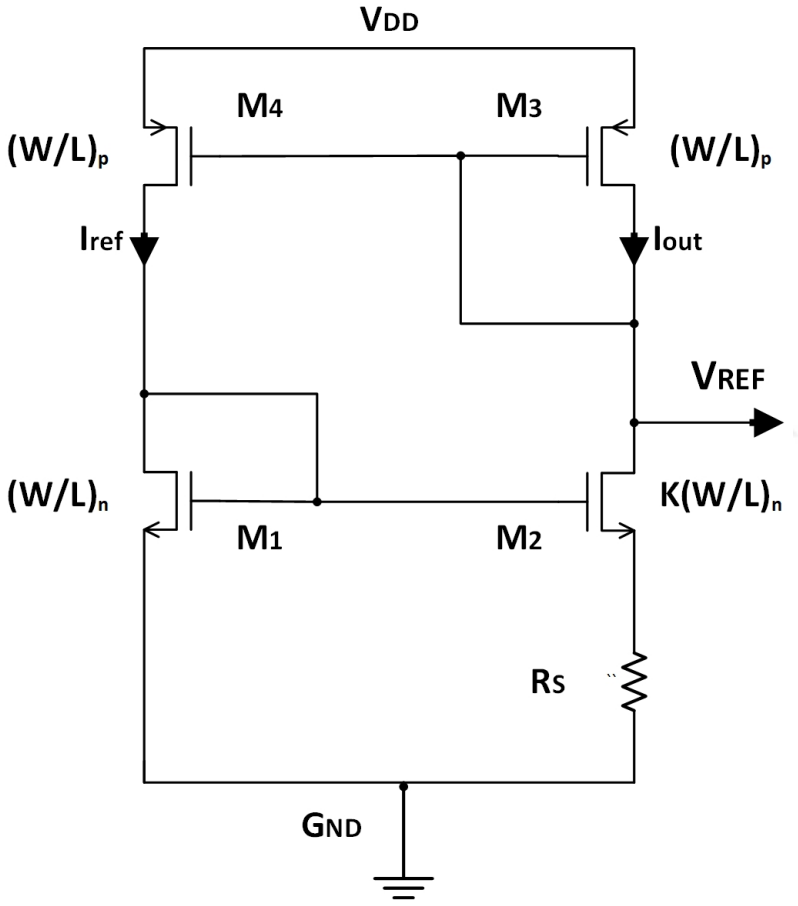

FIGURE 3.1: Proposed design of temperature sensor.

3.1.3 Complete Schematic Using Start-Up

The startup circuit for our proposed design is composed of transistors M5-M9. The sizes of M7-M9 are intentionally kept small to increase the On-resistance and a high voltage amount drops across them during normal operation of the circuit. For zero current operation, the gate voltages of M3-M4 are pulled to VDD and the gate voltages of M1-M2 are pulled to GND. This makes the drain of transistor M6 approach VDD, which in turn sets M5 on, therefore, transistors M3 M4 start conducting. Figure 3.2 shows complete schematic with the startup circuit. The Startup circuit is integrated with the main thermometer design. The design was simulated for supply voltages from 0.6 to 0.8V.

3.1.4 Simulation Results

This section contains the process variations and Monte Carlo simulation results for our proposed thermometer sensor. All the simulation results have been plotted using UMC 65nm Technology.

3.1.4.1 Process Corners

In order to see the response of the circuit across process corners of SS, TT and FF, the temperature was swept from $-40°C$ to $125°C$ for three supply voltages 0.6V, 0.7V and 0.8V. The output voltage ranges between 370mV and 740mV in these simulations simulations as shown in Figure 3.3. The circuit was able to maintain its direct propotional relation between output voltage and temperature across the whole temperature range. Sensitivity of the sensor is around 2mV per degree celsius.

3.1.4.2 Monte Carlo Results

The Monte Carlo simulation were run with 100 points at typical $27°C$ using three supply voltages that are 0.6V,0.7V and 0.8V. Figure 3.4 shows the mean value and the standard deviation for the output voltage. The mean voltage are measured to be 452mV, 547mV and 643mV respectively with the standard deviation of around 8mV for all values.

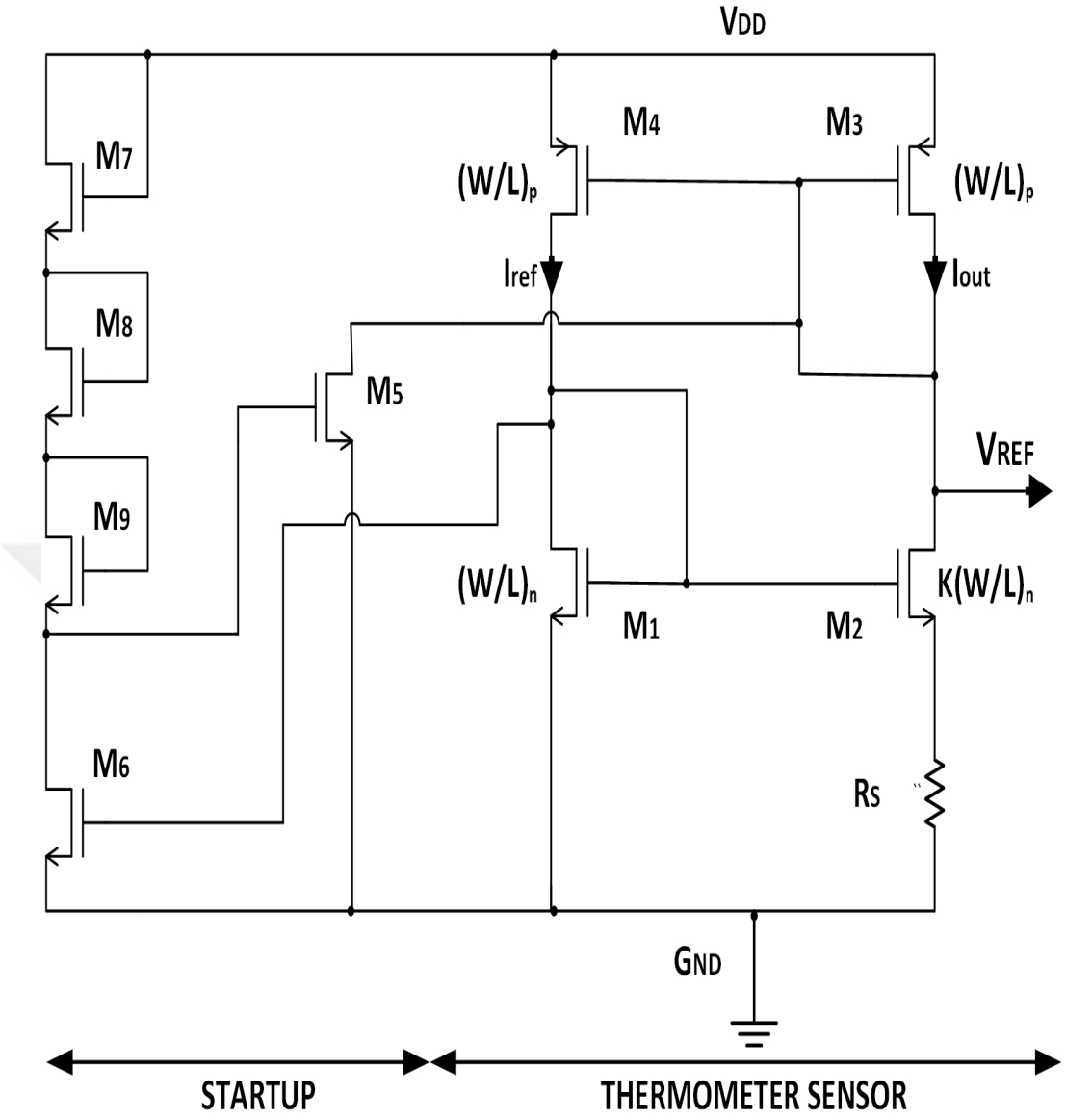

FIGURE 3.2: Proposed design of temperature sensor with startup circuit.

Figure 3.5 shows the direct relation of Output voltage curves over the entire temperature range in Monte Carlo simulations.

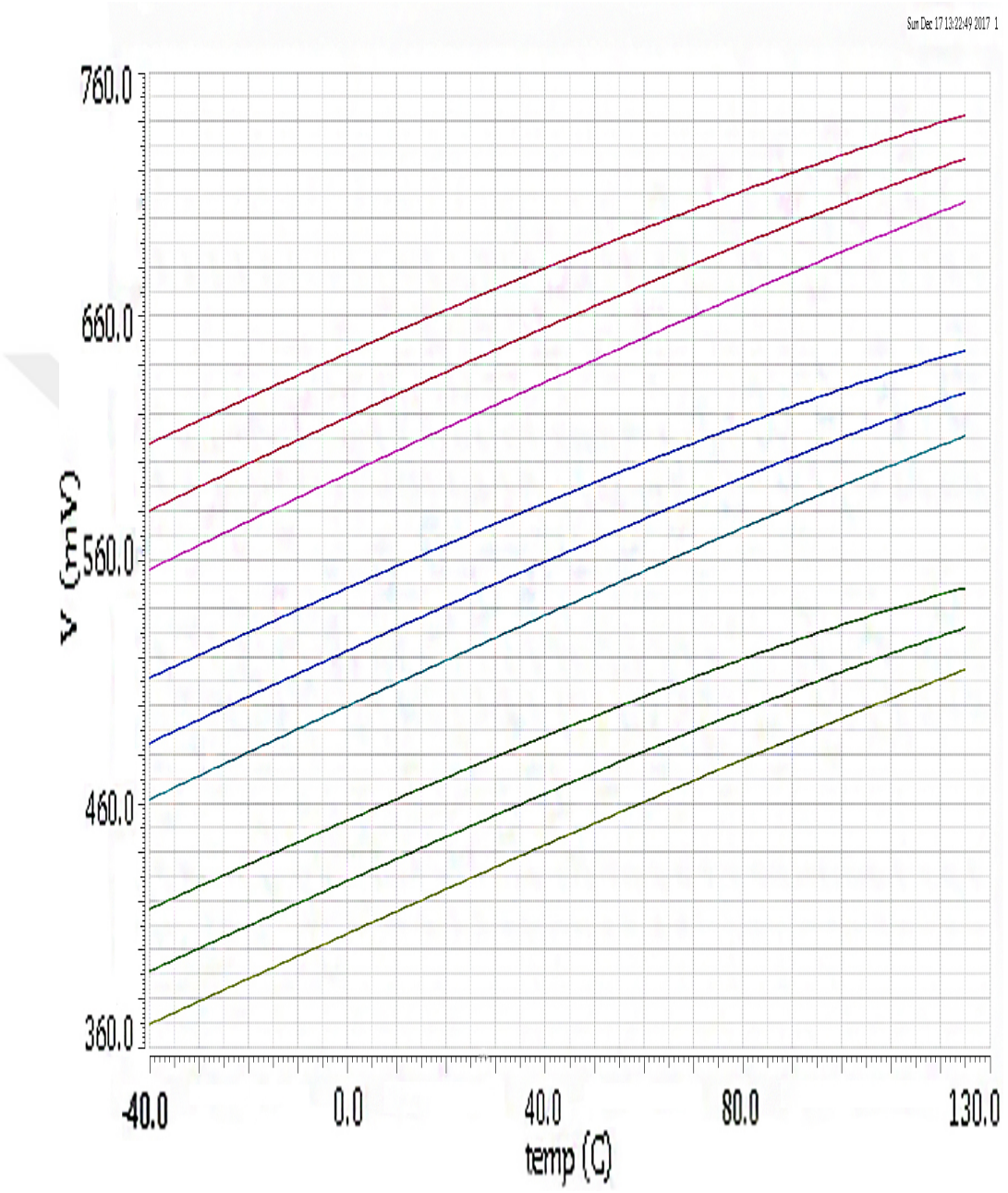

FIGURE 3.3: Proposed corners results of sensor output voltage with respect to temperature. Supply voltage sweeps from 0.6 - 0.8V. The headroom for output voltage is in between 370 - 740mV at TT, FF and SS corners.

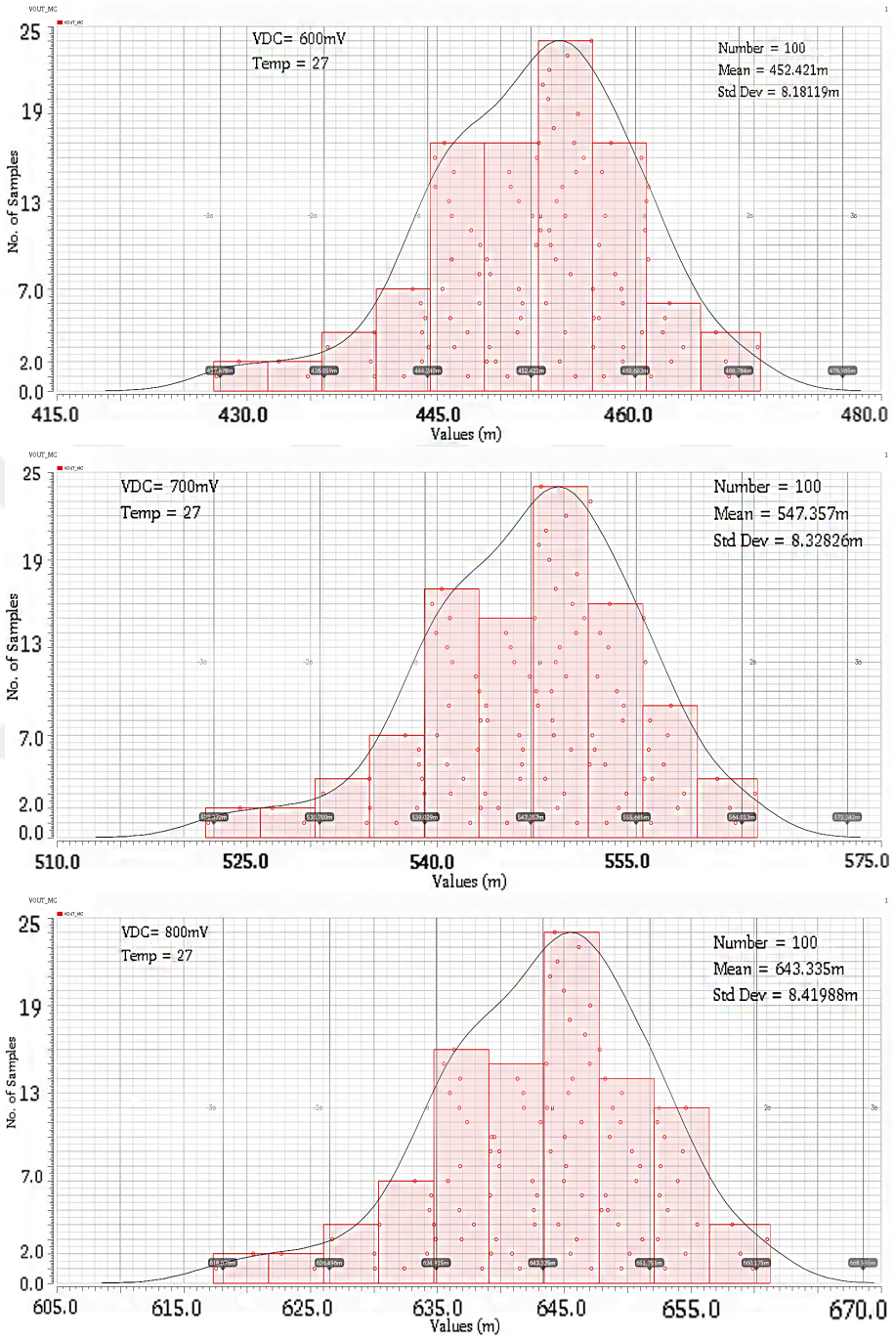

FIGURE 3.4: Process and mismatches of output voltage run at 27°C with 100 points Monte Carlo simulations defining standard deviation (Histogram Plots).

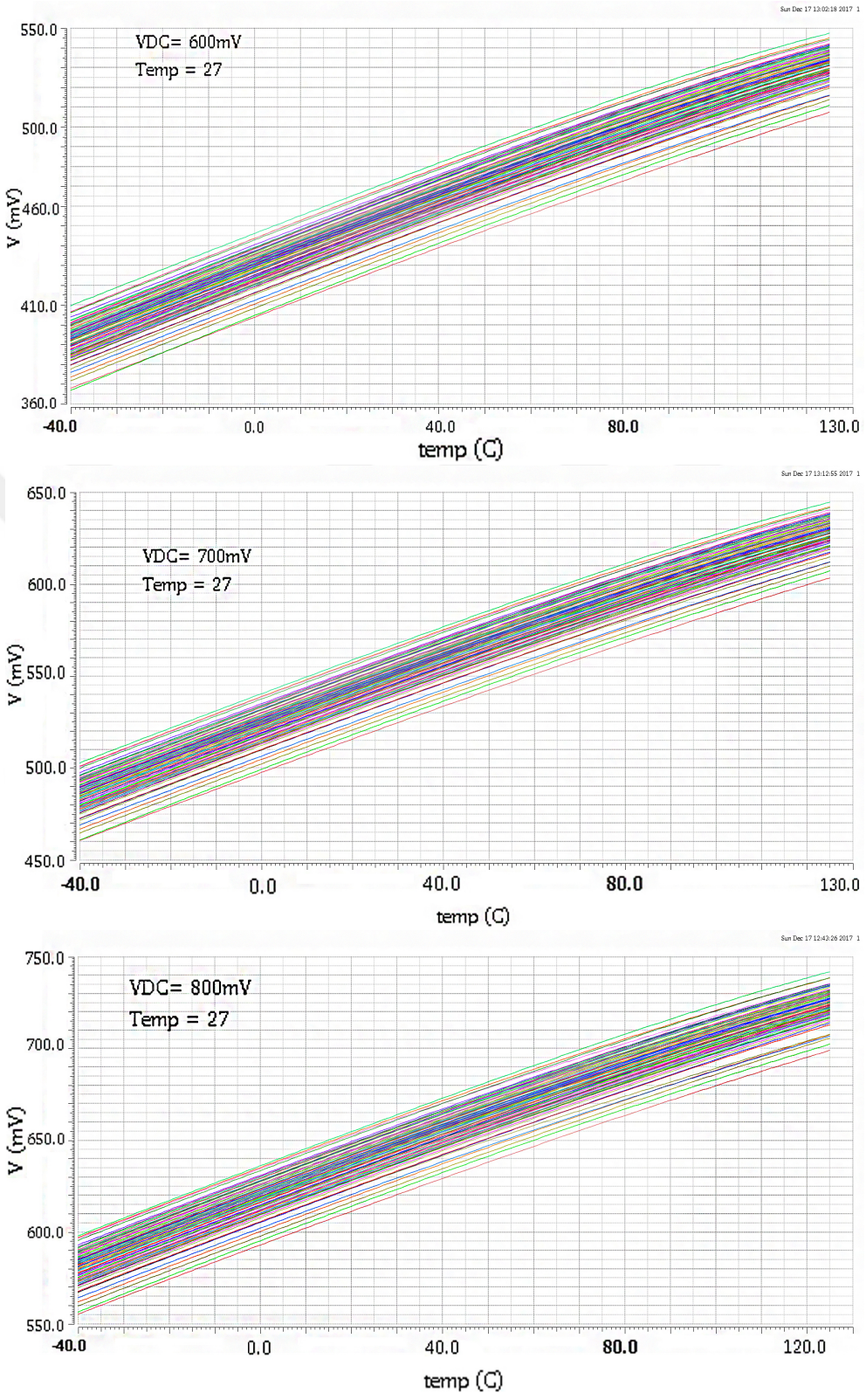

FIGURE 3.5: Process and mismatches of output voltage curves run at 27°C with 100 points Monte Carlo simulations. The supply voltage is 0.6, 0.7 and 0.8Volts.

The temperature inaccuracy of the sensor is shown in Figure 3.6. When the temperature sensor is modeled with a straight curve using the minimum and the maximum values, the inaccuracy of the sensors was determined to be less than 3°C. The layout of our proposed thermometer sensor is shown in Figure 3.7. The area of our sensor is 42um by 18um which is equal to $756um^2$.

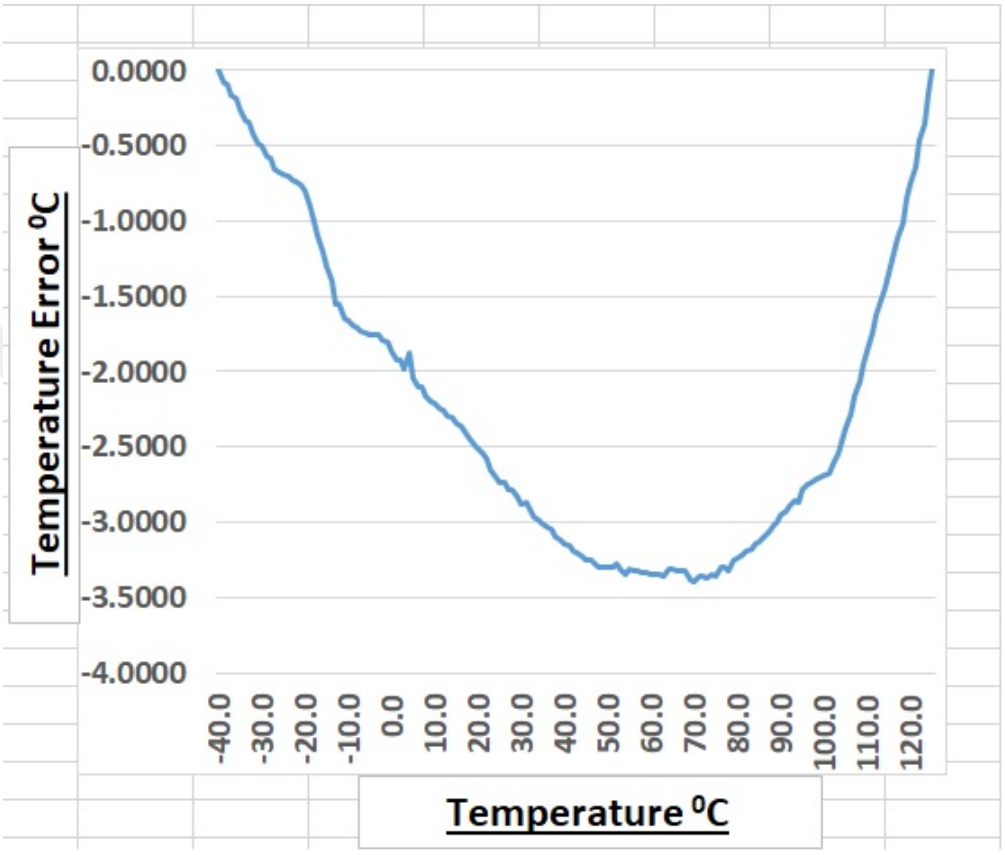

FIGURE 3.6: Inaccuracy of the temperature sensor is approximately 3°C.

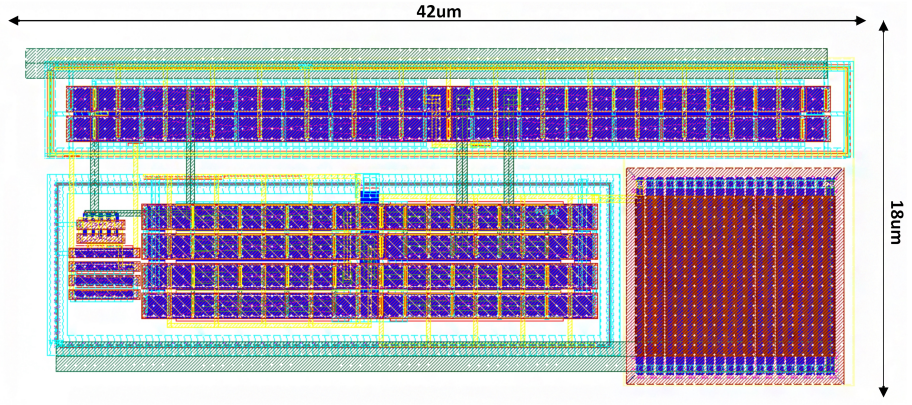

FIGURE 3.7: Process layout of the proposed thermometer sensor(Area = $756um^2$).

The performance of the proposed thermometer sensor is compared with other published work in Table 3.1 of our work is given as follows:

TABLE 3.1: System Performance Comparison of thermometer Sensor.

References	[11]	[12]	[13]	[14]	This work
CMOS Tech.(nm)	180	180	180	65	65
Supply (V)	1.2	1.2	1.2	1	0.6 - 0.8
Sensitivity (mV/C)	-	-	-	-	2
Inaccuracy (C)	(+1.3/-1.4)	(+1.5/-1.4)	(+0.5/-0.5)	(+1.5/-1.5)	$(+3.5/-3.5)^{\bullet}$
Temp.Range (C)	(0 - 100)	(0 - 100)	(0 - 100)	(0 - 110)	(-40 - 125)
Power Cons (W)	65n	71n	20u	500u	64n(0.6V)

• Simulated Results.

Chapter 4

Low Power Bandgap References

4.1 Proposed Bandgap Design

This part explains the designs of two separate bandgap circuits. Both designs utilize startup circuits for zero current state operation. The first design is a sub-1V bandgap reference and the other is known as subthreshold bandgap voltage reference.

4.1.1 Sub-1V Bandgap Reference

The startup for our proposed design comprises of transistors M8 through M11. Out of these, M8 and M9 perform the role of inverter. The size of M8 is intentionally kept large to decrease the On-resistance for a minimum voltage drop across it during normal operation of the circuit. The chain of series connected transistors (M9) are designed to have high impedance which results in high voltage drop across it. For zero current operation, the gate voltages of M5 - M7 and M8 are pulled to V_{DD}, making them high impedance. Consequently, output of the inverter comprising of M8 and M9 pulled down. This turns on M10 and M11 which forces the injection of current by M11 in the bandgap core and by M10 in operational transconductance amplifier (OTA). The drain voltage of M5 increases and the OTA starts to operate. In return, the OTA pushes the drain voltage of M6 to increase by pulling down the gate voltages of M5 - M7. As the gate voltage of M8 reduces, it causes the drain voltages of M8 and M9 to increase and therefore M10 and M11 cuts off.

The proposed design for the first bandgap reference circuit is shown in Figure 4.1 which includes a number of features. Firstly, the design has a lowered power consumption due to reduction of power supply to as low as 1V [15, 16]. The design consists of BJTs which helps in achieving a low temperature coefficient (TC).

Another feature of the proposed design is its low area occupies due to the utilization of a relatively smaller resistor compared to traditional design as discussed earlier in Chapter2. The minimum supply voltage is limited to 1V in this design. If the supply voltage falls below this minimum requirement, the voltage across the bandgap bias transistor (M5-M6) does not allow the BJT to operate in active mode. In order to generate the Bandgap output voltage, V_{REF}, both PTAT and CTAT voltages are combined. The CTAT component is generated by the V_{BE} of Q1 and the PTAT component is generated by the difference in V_{BE} of Q1 and Q2.

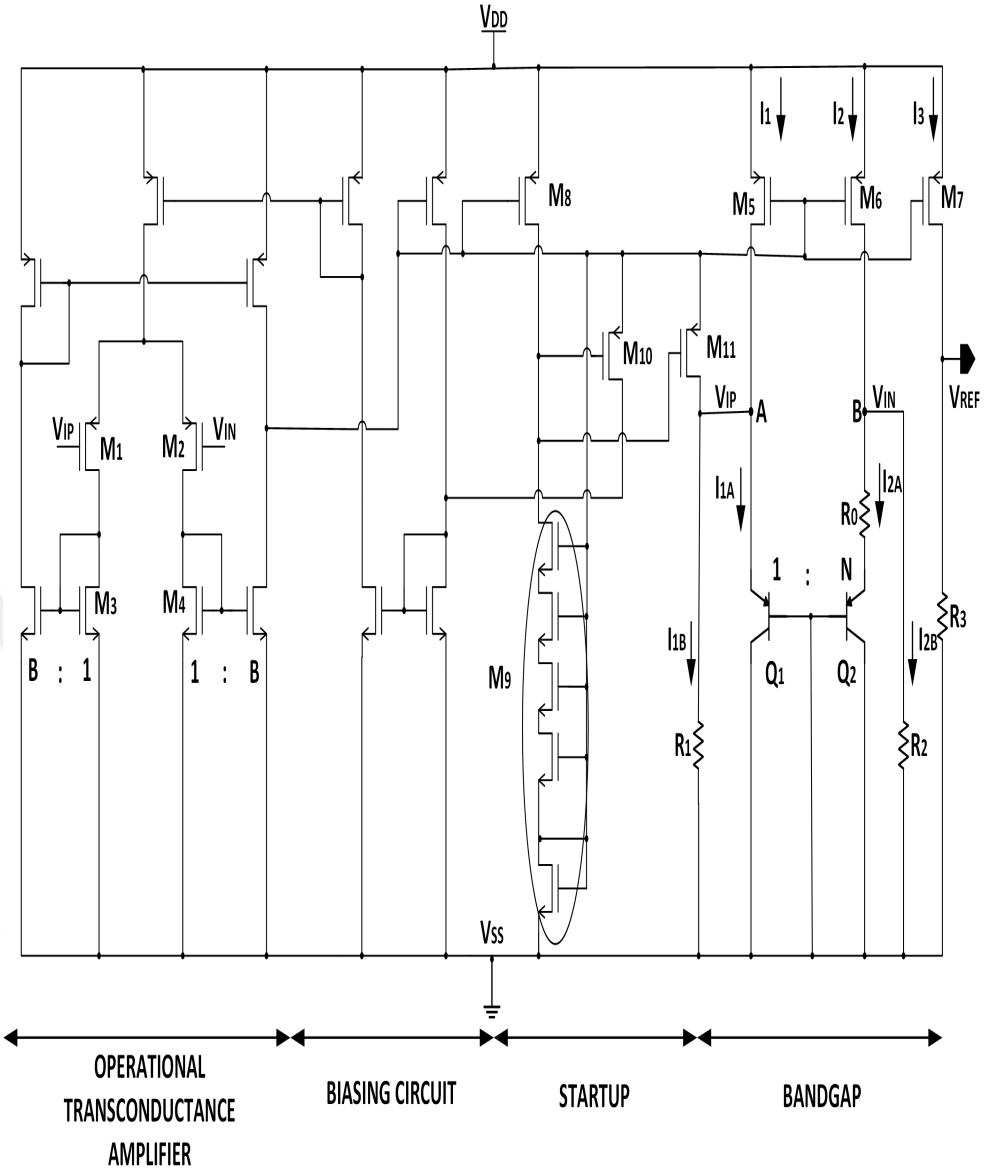

FIGURE 4.1: First projected design sub-1V bandgap reference circuit. It consumes 5uW power at 27°C Temperature.

The two BJTs in the circuit Q1 and Q2 act as a pn-junction diodes. The general diode equation for the current is given by

$$I_D = I_S exp\left(\frac{qV_{BE}}{KT}\right) \tag{4.1}$$

For a unit size diode,

$$V_{BE} = V_T \ln\left(\frac{I_D}{I_S}\right) \tag{4.2}$$

For N unit diode,

$$V_{BE} = V_T \ln\left(\frac{NI_D}{I_S}\right) \tag{4.3}$$

The difference in the two V_{BES} is defined as,

ΔV_{BE} = V_{BE1} - V_{BE2}

ΔV_{BE} = V_T ln(NI_{D1}/I_S)- $V_T$ln(NI_{D2}/I_S). By solving this equation, we get

$$\Delta V_{BE} = V_T \ln N \tag{4.4}$$

If $R_1 = R_2$, the OTA tries to to keep the Voltages A and B equal.

$$V_A = V_B \tag{4.5}$$

Setting $R_1 = R_2$, also causes the currents in the two branches of the bandgap to be equal. As I_3 is mirror of I_1 and I_2,

$$I_1 = I_2 = I_3 \tag{4.6}$$

Furthermore, the following currents are set equal as well.

$$I_{1A} = I_{2A} \tag{4.7}$$

$$I_{1B} = I_{2B} \tag{4.8}$$

Then, we can conclude from the schematic that,

$$I_{2A} = \left(\frac{\Delta V_{BE}}{R_0}\right) \qquad (I_{2A} \propto V_T) \tag{4.9}$$

$$I_{2B} = \left(\frac{V_{BE1}}{R_1}\right) \qquad (I_{2B} \propto V_{BE1}) \tag{4.10}$$

$$I_2 = I_{2A} + I_{2B} \tag{4.11}$$

Therefore, we can calculate the reference voltages V_{REF} as,

$$V_{REF} = (R_3)(I_3) \tag{4.12}$$

$$V_{REF} = (R_3)\left(\frac{\Delta V_{BE}}{R_0} + \frac{V_{BE1}}{R_1}\right) \tag{4.13}$$

Or

$$V_{REF} = (R_3)\left(\frac{V_T \ln N}{R_0} + \frac{V_{BE1}}{R_1}\right) \tag{4.14}$$

Eq. 4.14 presents the generated bandgap voltage. The bandgap uses symmetrical operational transcondactance amplifier (OTA) which has input common mode of around 700mV. The output voltage of the OTA drives all the PMOS transistors in the bandgap circuit. The loop gain A_v and gain bandwidth product GBW of the symmetrical OTA are calculated as [17],

$$A_V = g_{m1} B R_{M4} \tag{4.15}$$

$$GBW = \frac{B g_{m1}}{2\pi C_L} \tag{4.16}$$

where g_{m1} is the transcondance of input transistors.

B is the width multiplier.

R_{M4} is the impedance at the drain side of input transistor M2.

and C_L is the capcitances seen at the output of the OTA.

4.1.1.1 Simulation Results

The stability of the Opamp used in the bandgap shown in Figure 4.1 was verified in spectre simulations. Using the stability analysis, the loop gain is 40db and phase margin is 61degree as shown in Figure 4.2.

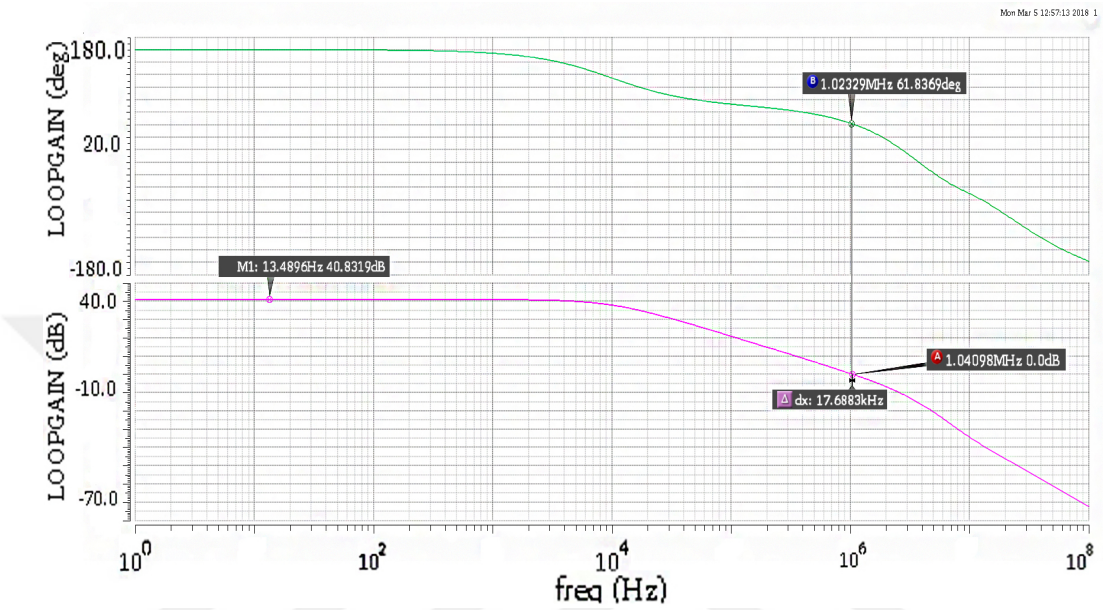

FIGURE 4.2: Loop gain and loop phase of the operational transconductance amplifier. The OTA has a gain of 40dB and 61° phase margin at 1.02MHz frequency.

The temperature is swept across the whole range of −40°C to 125°C and the output reference voltage fluctuates between 498mV to 500mV (ΔV=2mV). This yields in the temperature coefficient of the bandgap circuit around 62ppm/°C, as shown in Figure4.3.

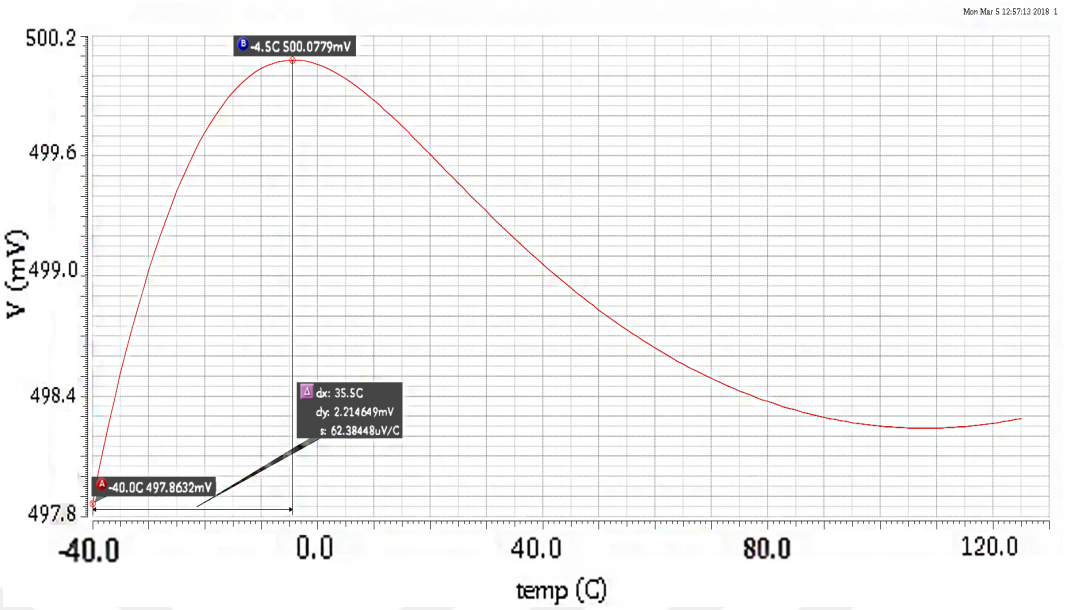

FIGURE 4.3: Temperature coefficient of bandgap circuit is approximately at 62ppm/°C with a temperature variation of 2mV.

In order to simulate the Power Supply Rejection Ratio, 1V AC voltage was applied on top of the supply voltage. PSRR of the circuit is 57 dB at low frequencies as shown in Figure 4.4.

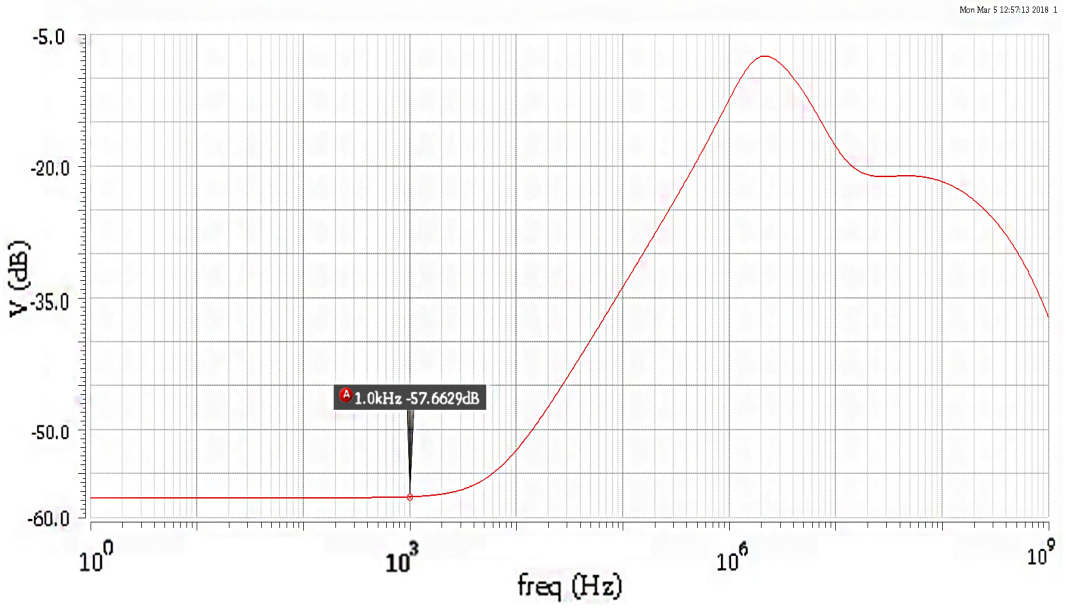

FIGURE 4.4: The power supply rejection ratio is -57dB at 1 KHz frequency.

The supply independent variation was also simulated for the circuit. For this simulation, parametric analysis was used for determining the variation in output voltage, as the

supply changes from 0 to 2.0V. The output voltage remains stable around 500mV with an error of 0.5mV at typical 27°C as shown in Figure 4.5

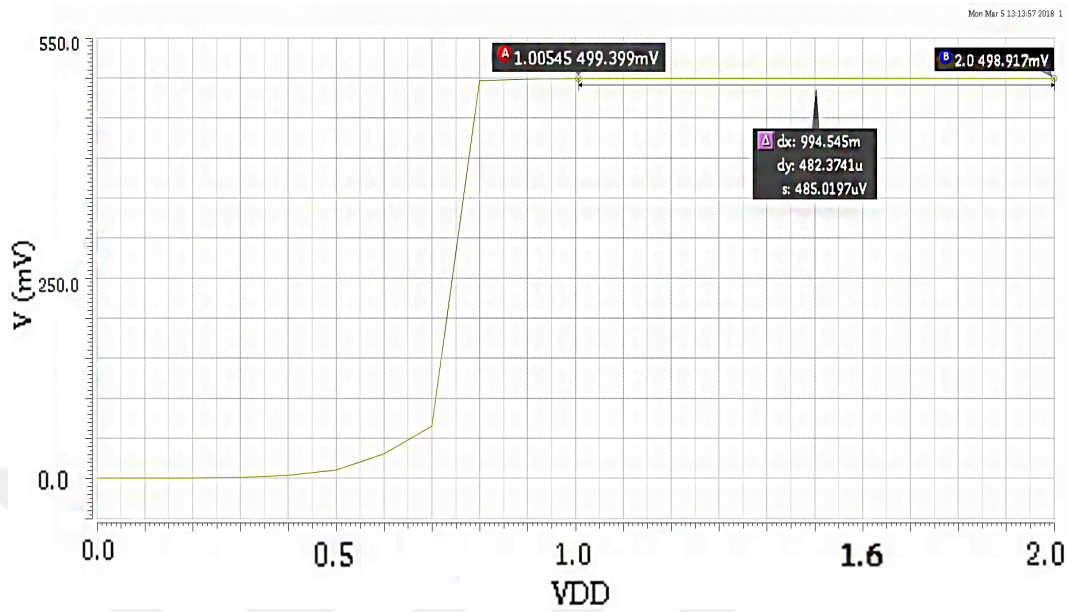

FIGURE 4.5: The supply independent output voltage variations is around 0.5mV at 27°C typical corner .

This circuit was also tested in transient operation to check the output when the supply is raised from 0 to full value in 100us and 10ns respectively. Figure 4.6 shows the settling of the output voltage for different process corners. The simulation was repeated with Monte Carlo mismatches and in all cases the output settles down successfully as shown in Figure 4.7.

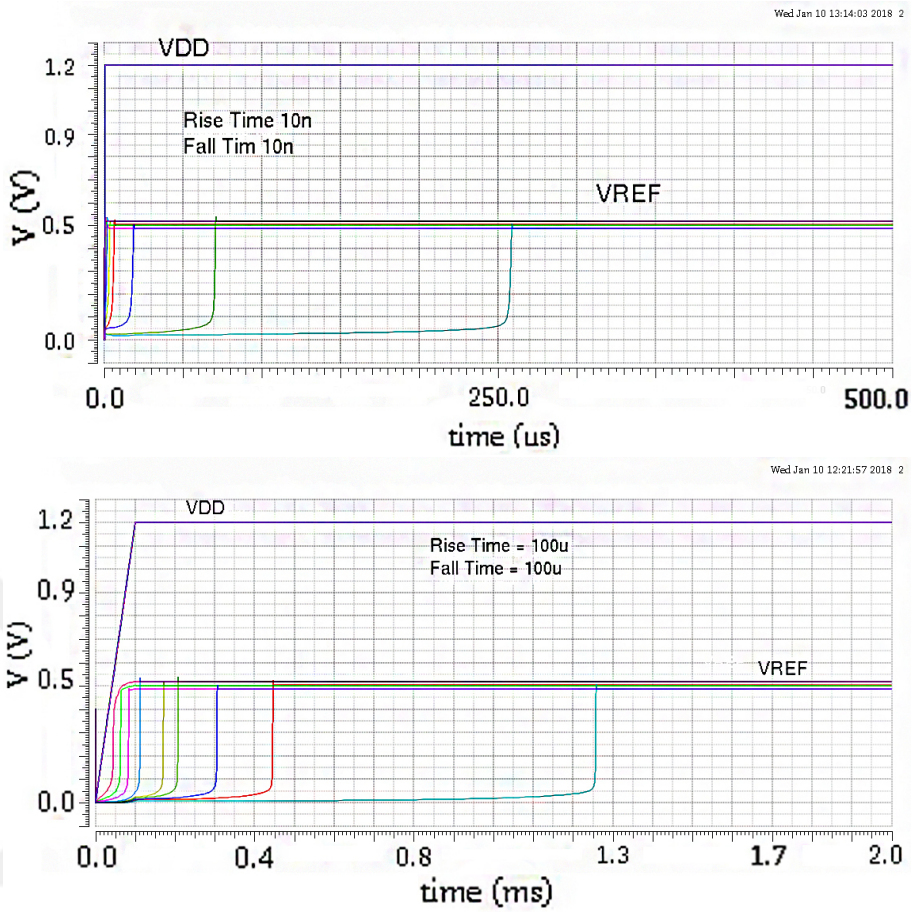

FIGURE 4.6: Process corners at 10nsec and 100usec rise and fall time in transient simulation for VREF

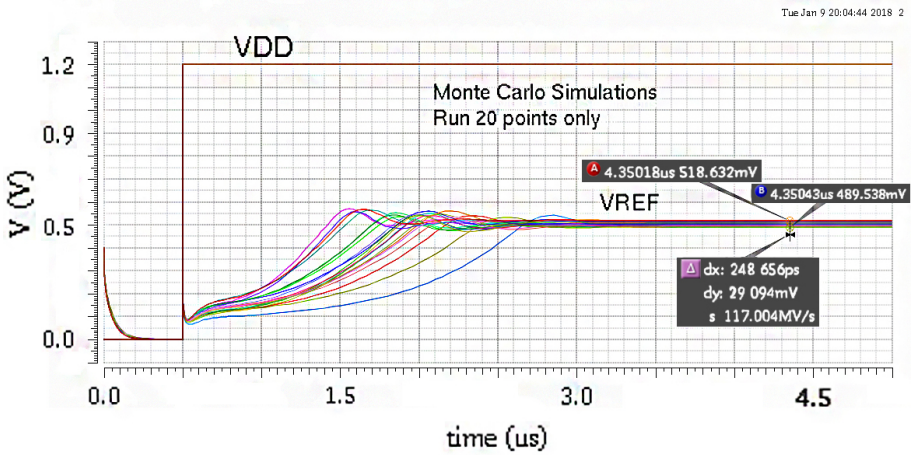

FIGURE 4.7: Monte Carlo transient operation for VREF

4.1.2 Subthreshold Bandgap Reference

The startup circuit for our proposed design comprises of transistors M15-M20 of which, M17-M18 make up the first inverter and M19-M20 make up the second inverter. The size of M17 is intentionally kept large to decrease the on-resistance. This causes minimum voltage drop across it during normal operation of the circuit. The chain of series connected transistors (M18) have high impedance which results in high voltage drop across it. For zero current operation, the gate voltages of M12-M13 are pulled to V_{DD} which results in the output of first inverter (M17-M18) to be low and the output of the second inverter becomes V_{DD}. This makes the transistors M15-M16 to turn on which in turn decreases the gate voltages of M10-M11. As M15 turns on, the input of first inverter goes low, which causes the output of second inverter to go low, therefore M15 and M16 are turned off in response.

This design uses less current while generating acceptable temperature coefficient. All the transistors work in subthreshold regions and the design is resistorless, achieving the functionality with less area and power consumption. The design incorporates a combination of CTAT and PTAT voltages Of which, CTAT voltage is generated from the threshold voltage of MOSFET M3 while PTAT is produced by self-cascode configuration from M4 through M9 in bandgap part [18, 19]. The output voltage is obtained by adding gate source voltages of M3, M5 and M7 transistors and subtracting those of M4, M6, M8 and M9 [20, 21]. This produces a V_{REF} output voltage of 925mV. The supply voltage used here is 1.2V for good PSRR and there is no need to use an OTA in this design. Figure 4.8 shows the circuit schematic of our proposed design.

The working principle can be explained as follows:

The subthreshold drain current I_D of a MOSFET is given as,

$$I_D = KI_o exp\Big(\frac{V_{GS} - V_{TH}}{\eta V_T}\Big)\Big(1 - exp\Big(\frac{-V_{DS}}{V_T}\Big)\Big) \tag{4.17}$$

Also,

$$I_o = \mu_o C_{ox}\Big(\eta - 1\Big)V_T^2 \tag{4.18}$$

For $V_{DS} > 0.1$V. current I_D is independent of V_{DS} and is given by,

$$I_D = KI_o exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \tag{4.19}$$

From the schematic, we have

$$V_{GS1} = V_{GS2} + V_{DS_{M14}} \tag{4.20}$$

The Currents I_P in M1 and in M2 are equal to each other and Eq. 4.18 can be rewritten as,

$$V_{DS_{M14}} = \eta V_T \ln\left(\frac{K_2}{K_1}\right) \tag{4.21}$$

The resistance of the MOS M14 is approximated as,

$$R_{M14} = \frac{1}{K_{M14}\mu_o C_{ox}(V_{REF} - V_{TH})} \tag{4.22}$$

From Eq. 4.18, Eq. 4.19 and Eq. 4.20, the expression for I_P can be written as,

$$I_P = \frac{V_{DSM14}}{R_{M14}} \tag{4.23}$$

Or

$$I_P = K_{M14}\mu_o C_{ox}(V_{REF} - V_{TH})\eta V_T \ln\left(\frac{K_2}{K_1}\right) \tag{4.24}$$

The output reference voltage of the circuit is generated from coupled transistors of M3 to M9. Therefore,

$$V_{REF} = V_{GS3} - V_{GS4} + V_{GS5} - V_{GS6} - V_{GS8} - V_{GS9} + V_{GS7} \tag{4.25}$$

Transistor M14 acts as current controlled resistor while threshold voltage of transistor M3 manifests as CTAT. In addition, transistors from M4 through M9 function as PTAT of the bandgap circuit. Therefore, reference voltage V_{REF} can written as

$$V_{REF} = V_{GS3} + \eta V_T \ln\left(\frac{2K_4K_6K_8K_9}{K_5K_7}\right) \tag{4.26}$$

Or

$$V_{REF} = V_{TH} + \eta V_T \ln\left(\frac{3I_P}{K_3I_O}\right) + \eta V_T \ln\left(\frac{2K_4K_6K_8K_9}{K_5K_7}\right) \tag{4.27}$$

Eq.4.27 shows that output voltage is the addition of the gate source voltage V_{GS3} and the thermal Voltage V_T scaled through transistor aspect ratios. Because V_{TH} has a negative temperature coefficient TC and V_T has a positive temperature coefficient TC. Hence, we can get output reference voltage V_{REF} independent of temperature by adjusting the transistor sizes.

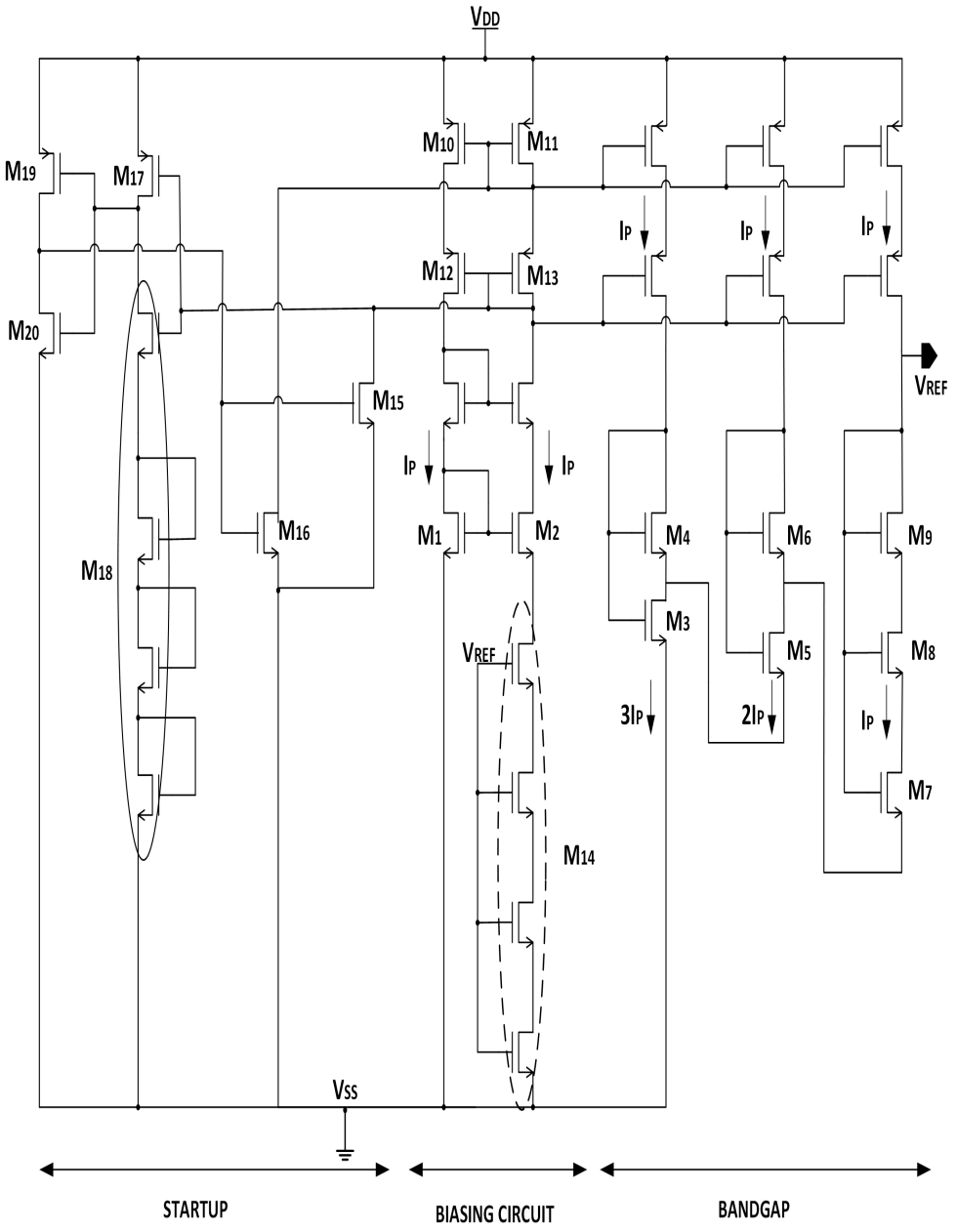

FIGURE 4.8: Second projected design subthreshold bandgap reference circuit. It consumes approximately 1uW power consumption at 27°C temperature.

4.1.2.1 Simulation Results

The temperature was swept across range of −40°C to 125°C to observe the dependence of the output voltage and it ranges between 925mV to 933mV (ΔV=8mV). This results in the temperature coefficient of the bandgap circuit of around 111ppm/°C, as shown in Figure 4.9

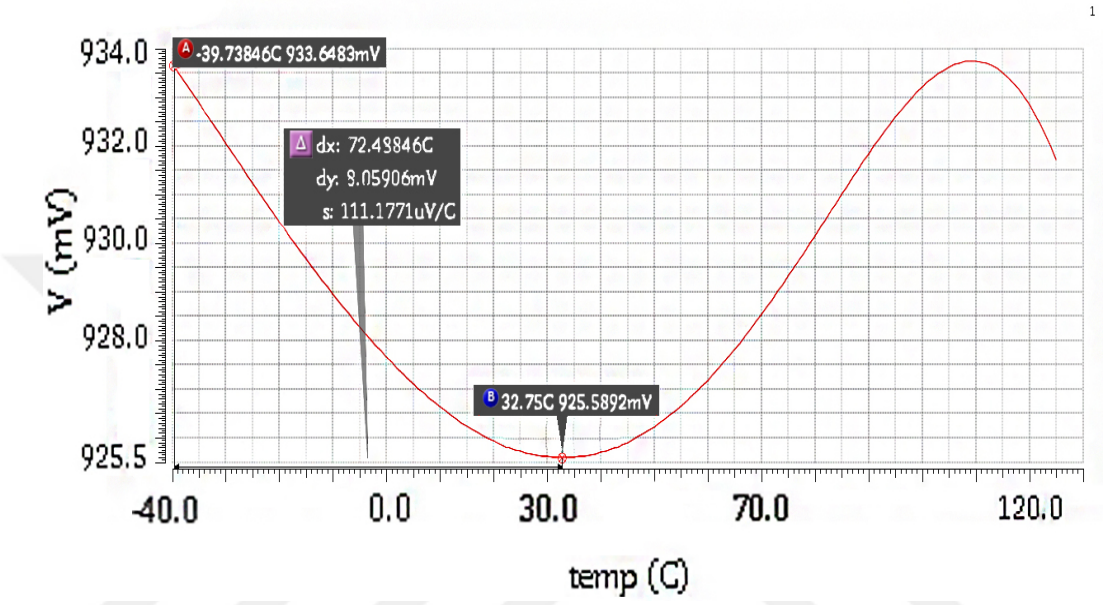

FIGURE 4.9: Temperature coefficient of bandgap circuit is approximately at 111ppm/°C with a temperature variation of 8mV.

To plot power supply rejection ratio, 1V AC voltage was applied on top of the supply voltage. The gain from the supply to the output, which shows that the PSRR value is 33dB as shown in Figure 4.10.

The supply independent variation was also simulated for the circuit. For this simulation, parametric analysis was used to determine the variation in output voltage as supply changes from 0 to 2.0V. The output voltage remains stable around 925mV with an error of 6mV at typical 27°C as shown in Figure 4.11.

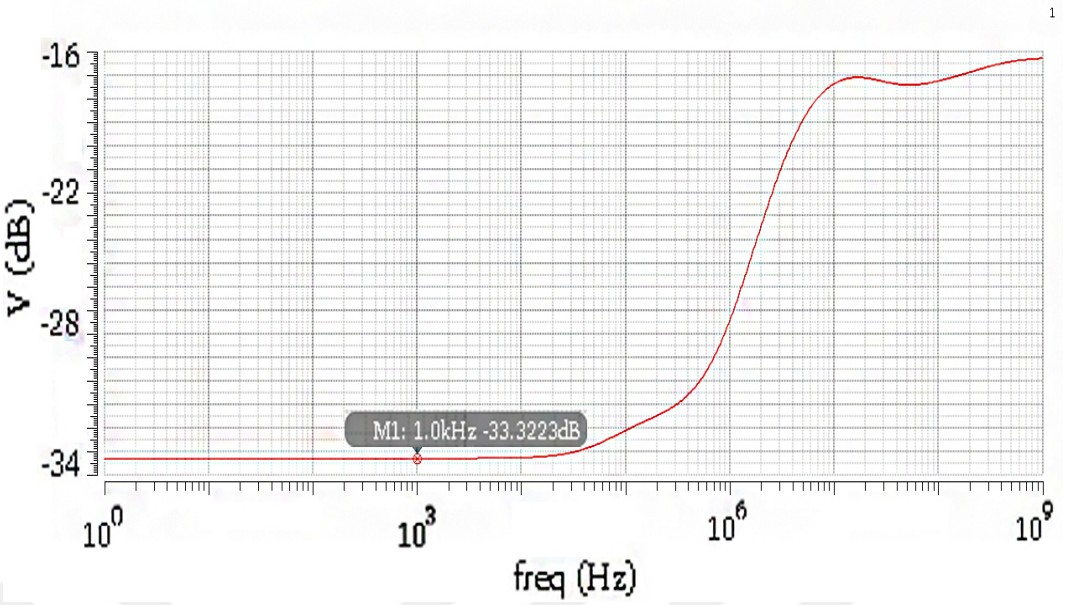

FIGURE 4.10: The power supply rejection ratio is 33.3dB at 1 KHz frequency.

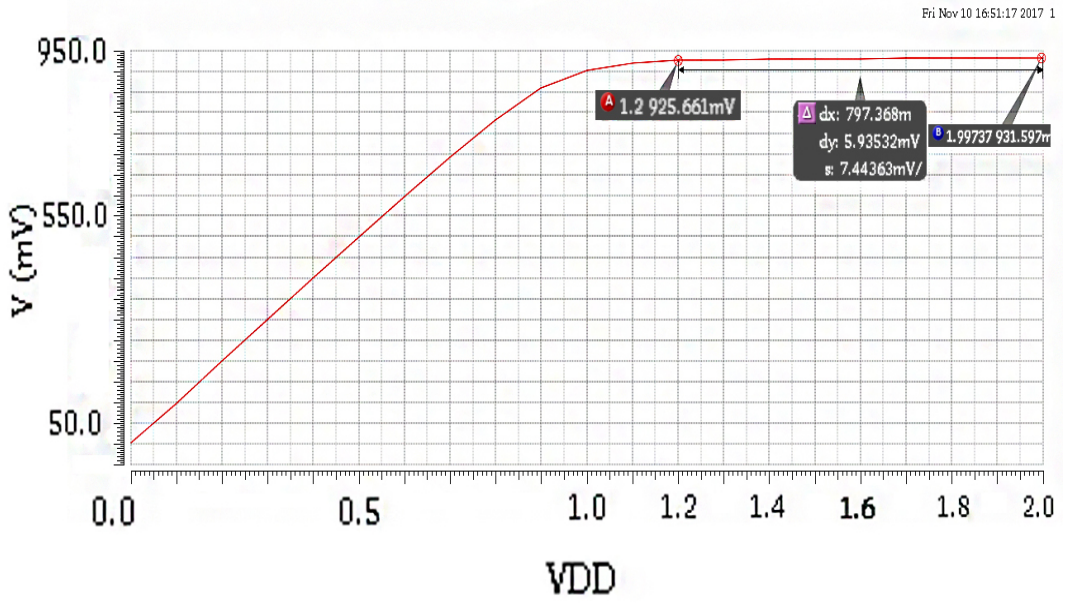

FIGURE 4.11: The supply independent output voltage variations is around 6mV.

The performance of the proposed Bandgap circuit is compared with other published works in Table 4.1 below.

TABLE 4.1: System Performance of Comparison of Proporsed Bandgap Circuits.

References	[22]	[23]	[24]	[25]	This work
CMOS Tech.(nm)	180	180	180	180	65
Supply (V)	1.8	1.1	0.8-2.5	1.2	1^{*} | $1.2^{\dagger}$
Power Cons (μW)	12	21	3.3	43.2	5^{*} | $1^{\dagger}$
Temp. Coeff (ppm/C)	65	6.5	271	4.5	62^{*} | $111^{\dagger}$
PSSR (dB)	40	-	-	-	57^{*} | $33.3^{\dagger}$
VREF (mV)	266	1012	221	767	500^{*} | $925^{\dagger}$

$*$ Sub-1V bandgap voltage reference.
† Subthreshold bandgap voltage reference.

Chapter 5

Conclusion and Future Work

5.1 Conclusion and Future Work

This thesis presents the design of a thermometer circuit that utilizes a Bandgap reference for low cost, low power applications. The design pronounces a linear characteristics between temperatures range from $-40°C$ to $125°C$ with an inaccuracy of less than $3°C$. This circuit works in supply ranges from 0.6 to 0.8V with a static power consumption of 64nW at typical corner and $27°C$. Results of the sensor are verified at different process corners and with mismatches. Two BGR designs are proposed and designed to operate with the temperature sensor. First design attains an inaccuracy of 2mV for temperature ranges from $-40°C$ to $125°C$. temperature coefficient of around $62ppm/°C$ is achieved. The PSRR of this design is 57dB at 1 KHz in the range from 1V to 2V.Power Consumption is around $5\mu W$. Second design operates under the same temperature range of $-40°C$ to $125°C$ with an error of 8mV. Temperature coefficient is approximately $111ppm/°C$. The PSRR is 33.3dB at 1 KHz between 1.2V and 2V supply range and the power consumption is less than $1\mu W$. The schematics, simulations and post-layout are done with Cadence design tools using UMC 65nm CMOS technology.

The next step for this work is to reduce inaccuracy of thermometer sensor by using any calibration methods.The sub threshold bandgap circuit requires more PSRR and less temperature coefficient and supply limitation.

Bibliography

[1] Babani Mohammed, Abba. A comparative study between different types of temperature sensor . 03(01):11–13, 2015.

[2] Man Wang, Bo Law. A sub-1V BJT-based CMOS temperature sensor from −55°C to 125°C. *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 48(01):3114–3117, 2012.

[3] Hyunsik Shim, Daeyong Jeong. A process-variation-tolerant on-Chip CMOS thermometer for auto temperature compensated self-refresh of low-power mobile DRAM. *IEEE Journal of Solid-State Circuits*, 48(10):2550–2557, 2013.

[4] Daeyong Lee, Hyunjoong Shim. A sub-1.0-V on-Chip CMOS thermometer with a folded temperature sensor for low-power mobile DRAM. 63(06):553–557, 2016.

[5] Vijay Pandey, Abhishek Nath. Study and design of 40nW CMOS temperature sensor for space applications. *TELKOMNIKA (Telecommunication Computing Electronics and Control)*, 13(3):813, 2015.

[6] A Paul Brokaw. A simple three-terminal IC bandgap refernce. *IEEE Journal of Solid-State Circuits*, 09(06):388–393, 1974.

[7] Robert J. Widlar. New developments in IC voltage regulators. *IEEE Journal of Solid-State Circuits*, 6(1):2–7, 1971.

[8] Paul R Gray and Robert Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, Inc., 1990.

[9] Matthias Sylvester. Circuit sizing w / corner models challenges applications. *MunEDA*, 2013.

[10] Aatmesh Kamakshi, Divya Akella Shrivastava. A 23nW CMOS ultra-low power temperature sensor operational from 0.2V. *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, S3S 2015*, pages 7–9, 2015.

[11] Jae Jeong, Seokhyeon Sim. 65nW CMOS temperature sensor for ultra-low power microsystems. *Proceedings of the Custom Integrated Circuits Conference*, 2013.

[12] Zhiyoong Jeong, Seokhyeon Foo. A fully-integrated 71nW CMOS temperature sensor for low power wireless sensor nodes. *IEEE Journal of Solid-State Circuits*, 49(8): 1682–1693, 2014.

[13] Wei Wu, Chun-Kuan Chan. A 80kS/s 36μW resistor-based temperature sensor using BGR-free SAR ADC with a unevenly-weighted resistor string in 0.18μm CMOS. *011 Symposium on VLSI Circuits-Digest of Technical Papers*, pages 222–223, 2011.

[14] Jabeom Hwang, Sewook Koo. A 0.008mm2 500μW 469kS/s frequency-to-digital converter based CMOS temperature sensor with process variation compensation. *IEEE Transactions on Circuits and Systems I*, 60(9):2241–2248, 2013.

[15] F.Pruzzi Malcovati, P.Maloberti. Curvature compensated BiCMOS bandgap with 1 V supply voltage. *Proceedings of the 26th European Solid-State Circuits Conference*, pages 7–10, 2000.

[16] Philip Leung, Ka Nang Mok. A sub-1-V 15ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device. *IEEE Journal of Solid-State Circuits*, 37(4):526–530, 2002.

[17] Willy M.C. Sansen. *Analog Design Essentials*, volume 859. Springer, 2006.

[18] Ken Ueno. CMOS voltage and current reference circuits consisting of subthreshold MOSFETs–micropower circuit components for power-aware LSI applications–. InTech, 2010.

[19] Hirose Ueno, Ken Member. A 300 nW, 15 ppm/° C, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold MOSFETs. *IEEE Journal of solid-state circuits*, 44(7):2047–2054, 2009.

[20] Ken Hirose, Tetsuya Ueno. A CMOS bandgap and sub-bandgap voltage reference circuits for nanowatt power LSIs. *2010 IEEE Asian Solid-State Circuits Conference, A-SSCC 2010*, pages 70–80, 2010.

[21] Iman Fakharyan and Mehdi Ehsanian. A sub-1V nanowatt CMOS bandgap voltage reference with temperature coefficient of 13ppm/° C. *Electrical Engineering (ICEE), 2015 23rd Iranian Conference*, pages 1129–1132, 2015.

[22] Srivatsava Maddikatla, Sunil Kumar Jandhyala. An accurate all CMOS bandgap reference voltage with integrated temperature sensor for IOT applications. *Proceedings of IEEE Computer Society Annual Symposium on VLSI, ISVLSI*, 2016: 524–528, 2016.

[23] Phillip Rincon-Mora, Gabriel A.Allen. A 1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference. *IEEE Transactions on Circuits and Systems I*, 33(10):1551–1554, 1998.

[24] Hongchin Lin, Yen Tai Lin. A simple subthreshold CMOS voltage reference circuit with channel- length modulation compensation. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 53(9):882–885, 2006.

[25] R Sun, N Sobot. A novel 1.2-V 4.5-ppm/C curvature-compensated CMOS bandgap reference. *CCECE, 2010 23rd Canadian Conference on*, 61(4):1026–1035, 2010.