Impact of Channel Length Scaling on Electrical Transport Properties of Silicon Carbide Nanowire based Field Effect Transistors (SiCNW-FETs)

A thesis submitted to the
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by

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in

Electronics and Computer Engineering

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Electronics and Computer Engineering.

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I, Ali UZUN, declare that this thesis titled, 'Impact of Channel Length Scaling on Electrical Transport Properties of Silicon Carbide Nanowire based Field Effect Transistors (SiCNW-FETs) ' and the work presented in it are my own. I confirm that:

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Abstract

The rapid evolution of technology forces the existing electronic devices to be much more smaller as well as to able to operate at higher frequency with low power consumption. However, current devices (ex. CMOS (Complementary Metal Oxide Semiconductor)) mostly based on Silicon (Si) and Si based transistor technology is almost saturated in terms of device size and operating frequency. In order to overcome these issues and realize much faster and smaller transistor with new geometry, 1-D nanostructures (such as nanowires (NWs) and nanotubes (NTs)) and their electrical transport properties have become focus of tremendous research in recent years. Silicon carbide (SiC) nanostructures, a wide band gap semiconductor with excellent properties such as as high break-down voltage, high thermal conductivity, high drift velocity physical and chemical properties as well as compatibility with existing Si devices, have been intensly studied in terms of material properties, fabrication, characterization as well as their various applications. SiCNWs are one of the most promising candidate to be used as channel material or substrate.

In this study, we synthesize 3C-SiCNWs via Metal-Organic Chemical Vapor Deposition (MOCVD) method and fabricate SiCNW-FETs in order to examine the channel length dependent electrical transport characteristic of SiCNW with varying channel lengths ranging from 120 nm to 1.5 μm. Further we report the important performance parameters of SiCNW-FET devices and compare them with recently reported studies. The device with the 120 nm channel length has led a very high on/off current ratio (I_{on}/I_{off} $= 1.34 \times 10^4$) and very strong gating effect. Furthermore, the transconductance and the hole mobility have been determined as 6.9 nS and 1.696 $cm^2/V.s$, respectively, at V_{ds} of 0.05 V. This study shows good promise of the SiCNW-FET devices to be used in advanced solid-state nanoelectronic devices capable of operating at high frequency and high temperature.

Keywords: SiCNW-FET, SiC Nanowire, Transconductance, Channel Length Scaling, I_{on}/I_{off} Current Ratio, Electrical Characterization

Kanal Uzunluğu Ölçeklemenin Silisyum Karbür Nano Tel Tabanlı Alan Etkili Transistörlerin (SiCNW-FET) Elektrisel İletim Özelliklerine Etkileri

Ali Uzun

Öz

Teknolojinin hızlı evrimi, mevcut elektronik cihazların daha küçük boyutta düşük güç tüketimi ile yüksek frekansta çalışmaya zorlamaktadır. Bunula birlikte, çoğunlukla Silisyum tabanlı transistörler (örn. CMOS - Tamamlayıcı Metal Oksit Yarıiletken), Si teknolojisinin cihaz boyutu ve çalışma frekansı bakımından neredeyse fiziksel sınıra ulaşması sebebiyle daha fazla küçültülememektedir. Bu problemlerin üstesinde gelmek ve daha küçük ve verimli transistörlerin üretilebilmesi için 1-boyutlu yapılar (özellikle nano teller ve nano tüpler) ve bu yapıların elektrisel özellikleri son yıllarda fazlaca çalışılmaya başlanmış ve araştırma odağı haline gelmiştir. Geniş bant aralıklı bir yarıiletken olan Silisyom Karbür, sahip olduğu yüksek kırılma gerilimi, yüksek ısı iletkenliği, yüksek sürüklenme hızı, fiziksel ve kimyasal özellikleri ve mevcut Si cihazlarla kolay entegre edilebilirlik gibi mükemmel özelliklerinden dolayı araştırmacılar tarafından malzeme özellikleri, imalat, karaterizasyon ve farklı uygulamamları çokca çalışılmaktadır. SiC, kanal malzemesi veya substrat olarak kullanılabilecek umut verici aday materyallerden biridir.

Bu çalışmada, Modüler İnce Film Katman Kaplama Sistemi (MOCVD) ile 3C-SiC sentezi ve kanal uzunluğuna bağlı elektriksel iletim özelliklerini incelemek için kanal uzunlukları 120 nm ile 1.5 μm arasında olan SiCNW-FETs üretimi ve test işlemleri yapılmıştır. Ayrıca, SiCNW-FET cihazlarının önemli performans parametrelerini raporlanmış ve yakın zamanda yayınlanmış çalışmalarda elde edilen sonuçların kıyaslaması yapılmıştır. Kanal uzunluğu 120 nm olan NW-FET cihaz yüksek bir açık-kapalı akım oranı sergilemiştir ($I_{on}/I_{off} = 1.34 \times 10^4$). Aynı cihaz 0.05 V V_{ds} güç tedariğiyle 6.9 nS geçis iletkenliği ve 1.696 $cm^2/V.s$ yük hareketliliği göstermiştir. Bu çalışma, SiCNW-FET'lerin yüksek frekans ve yüksek sıcaklıkta çalışabilen gelişmiş katıhal dijital nanoelektronik cihaz ve develerde kullanılmak üzere iyi bir gelecek vaat ettiğini göstermektedir.

Anahtar Sözcükler: SiCNW-FET, Geçis iletkenliği, Silisyum Karbür Nano tel, Kanal Uzunluğunlğu Ölçeklemesi, $I_{açık}/I_{kapalı}$ akım oranı

I would like to dedicate this work to my parents and to my sister and brother, who always stood behind me all the times with their prays and support and kept believing in me.

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Abbreviations

Ar	Argon
BSE	Back-Scattered Electron Detector
C.L.	Channel Length
CMOS	Complementary Metal Oxide Semiconductor
D.	Dimensions
Dia.	Diameter
EBL	E-beam Lithography
FET	Field Effect Transistor
HMDS	Hexamethyldisilane
H_2	Hydrogen
In_2O_3	Indium(III) oxide
IPA	Isopropyl Alcohol
K	10^3
M	10^6
MIBK	Methyl-isobutyl-ketone
MOCVD	Metal-Organic Chemical Vapor Deposition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
Ni	Nickel
N_2	Nitrogen
NW	Nanowire
NW-FET	Nanowire Field Effect Transistor
O_2	Oxygen
PMMA	Polymethlmetharcylate
QD	Quantum Dot
Ref.	Reference

rpm	Revolution per Minute
SE	Secondary electron
SEM	Scanning Electron Microscopy
SMU	Source Measure Unit
SI	International System of Units
Si	Silicon
SiC	Silicon Carbide
SiCNW-FET	Silicon Carbide Nanowire Field Effect Transistor
SiO_2	Silicon Dioxide
T.W.	This Work
VLS	Vapor Liquid Solid
VS	Vapor Solid
XRD	X-Ray Diffraction
0-D,1-D,2-D and 3-D	Zero, One, Two and Three Dimensional

Physical Constants

Electron Charge	q	=	1.602×10^{-19} C
Permittivity of Vacuum	ϵ_o	=	8.854×10^{-14} F/cm
Relative Dielectric Constant of SiO_2	ϵ	=	3.9

Symbols

Symbol	Name	Unit
V	Voltage	Volts
S	Siemens	V/A
g_m	Transconductance	A/V
μ_h	Carrier Mobility	$\mathrm{cm}^2/V.s$
η_h	Carrier Concentration	cm^{-3}
h	Oxide Thickness	meter
r	Nanowire Diameter	meter
L	Channel Length	meter
I	Current	Amper
I_d	Drain-Source Current	Amper
C	Capacitance between NW and substrate	Farad
V_{ds}	Drain - Source Voltage	Voltage
V_{gs}	Gate - Source Voltage	Voltage
I_{on}/I_{off}	On-Off Current Ratio	
A	Cross-section Area of NW	

Chapter 1

Introduction

In this chapter, a brief introduction about one dimensional (1-D) nanostructures, properties silicon carbide nanowires (SiCNWs) as a promising semiconductor material and other commonly studied semiconductor materials is given. Additionally, a summary of previous studies on electrical transport properties of SiCNW-FETs and obtained performance parameters are provided. Finally, the motivation behind the work and thesis organization are presented.

1.1 Research Background

Recent developments in nanotechnology have attracted researchers interest into nanostructures. It is relatively a new class of materials where the dimensions are less than 100 nm. They are categorized into four groups such as zero-dimensional, one-dimensional, two-dimensional and three-dimensional nanostructures abbreviated as (0-D), (1-D), (2-D), and(3-D), respectively. Briefly, 0-D structures such as quantum dots (QDs) have all dimensions (x,y,x) of less than 100 nm. If the nanostructure has only one dimension greater than 100 nm, it is called 1-D nanostucture like nanowires (NWs), nanotubes, nanoroads, nanowhiskers etc. Structures with their two dimentions greater than 100 nm, are named 2-D nanostructures such as nanoplates and nanoflakes. Finally 3-D nanostructues have all their dimension greater than 100 nm such as nanoballs, nanocoils, and nanoflowers. A summary of nanostructures and features are given in Table 1.1. Although different forms of these nanostructures have been studied, 1-D nanostructures have gained

great interest due to their high surface-to-volume ratios, quantum size effects as well as their promising electrical, mechanical and optical properties. 1-D semiconductor nanostructures, especially nanowires have been examined extensively because of their high potential to be used in nanoscale electronics, sensors, photonics, flexible circuit, biosensing [6–9] applications as passive element (interconnects) and active element (functional unit such as transistor, diode). Number of other semiconductor nanowires materials such as ZnO, Ge, SnO, InP, GaAs, AlN, GaN, SiC [10–14] have been studied. Silicon carbide nanowires (SiCNWs) combine remarkable properties of 1-D materials with that of superior intrinsic features of SiC characteristics such as great thermal conductivity, breakdown electric field, electron drift velocity, chemical stability and biocompability, offer great opportunities for high power and high frequency devices capable of operating at high temperatures and harsh environments [15].

Table 1.1: Summary of nanostructures.

Nanostructures	**# of D. > 100 nm**	**Example Structure**
0-D	0	quantum dots,hollow cubes,nanospheres
1-D	1	nanowires, nanotubes, nanoroads,
2-D	2	nanoplates,nanowalls ,nanoflake
3-D	3	Nanoballs,nanocoils,nanoflowers

Silicon Carbide (SiC), a IV–IV group compound semiconductor and exists in nature more than 200 polytypes and 3C-, 4H- and 6H- are most commonly seen ones. Often times, 4H- and 6H-SiC polytypes are called as α-SiC and 3C-SiC is called as β-SiC and zinc-blende structure due to its cubic crystal structure. Among the common polytpes 3C-SiC is widely studied one since it can be synthesized on Silicon (Si) substrate with larger size and low prices in relatively low temperatures compared to 4H- and 6H-SiC [16]. In this thesis, we studied electrical transport characteristics of a single 3C-SiCNW based FETs with varying channel length ranging from 120 nm to 1.5 μm.

1.2 Literature Review

Due to its excellent features such as high breakdown voltage, high thermal conductivity, high drift velocity physical and chemical properties as well as compatibility with existing Si technology, SiCNWs have drawn tremendous attention. SiCNWs can provide

significant advantages in order to deal with current limitations of Si in terms of temperature, power consumption and operating frequency. Up to now, few theoretical and experimental studies had been conducted on electrical transport properties of SiCNW-FETs devices; and most of the experimental studies show similar performance in terms of transconductance (g_m), carrier mobility (μ_h), and on/off current ratio (I_{on}/I_{off}). Further, these earlier studies struggle with the issues of very low I_{on}/I_{off} ratio, weak gating effect, low carrier mobility, and high off-state leakage current.

The first studies on electronic transport through SiCNW-FETs were conducted by Seong *et al.* [17, 18] and Zhou *et al.* [19, 20]. In their studies, Seong *et al.* designed a SiCNW based FET device (with NW diameter: $\sim$ 90 nm and channel length: 35 μm) with transconductance of 0.17 nS and estimated electron carrier mobility of 15 $cm^2/V.s$ for V_{ds} voltage of 0.02 V. When it comes to Zhou *et al.*'s study, the SiCNW-FET (NW diameter: $\sim$ 10 nm, channel length: 1.5 μm) showed a carrier mobility of 15.9 $cm^2/V.s$,which yields transcondcutance of 0.5 nS at V_{ds} equals to 0.05 V. It can be concluded that second devices had slightly better performance than the study done by Seong and his team in terms of transconductance (g_m) and electron carrier mobility (μ_n).

Apart from experimental studies, some theoretical analysis were presented by Rogdakis *et al.* [21, 22] on electronic transport properties of 3C-SiCNW-FET. Based on the study, simulated SiCNW-FET (NW diameter: 10 nm, channel length: 750 nm) has resulted an I_{on}/I_{off} ratio of 20×10^4, where the measured value in [19] is 10×10^3. Rogdakis *et al.* conducted an experiment to investigate the effect of NW doping level and NW-dielectric interface quality on I-V curve characteristics such as g_m and I_{on}/I_{off} ratio by comparing the performance of SiCNW-FETs in both experimentally and theoretically. In his theoretical study [22], the FET device with 9 nm channel length exhibited trasconductance of 43.2 μS and I_{on}/I_{off} ratio of 1.6×10^5. Some other experimental studies [23–25] have showed similar results with the previous ones. Table 1.2 present summary of previous studies.

Nevertheless, most of the reported studies of the SiCNW-FETs present n-type semiconductor behavior. First time Chen *et al.* [26] reported the fabrication of p-type SiC-NWFETs that exhibit transconductance of 12 nS and hole mobility of 6.4 $cm^2/V.s$ with channel length of 3.2 μm [11], while Li *et al.* later reported slightly lower values of

transconductance (0.75 nS) and hole mobility (4.2×10^{-2} $cm^2/V.s$) with channel length of 3.5 μm [27].

TABLE 1.2: Summary reported studies with on-off current ratio, transconductance, hole mobility, and hole density at V_{ds} of 0.05.

C.L.	**NW Dia.**	g_m **(S)**	μ (cm^2/Vs)	V_{ds} **(V)**	**Carrier**	**Ref.**
3.5 μm	90 nm	1.7×10^{-10}	15	0.02	Electron	[18]
1.5 μm	10-25 nm	10×10^{-10}	15.9	0.05	Electron	[19]
4.4 mm	90 nm	-	0.11	-	Electron	[22]
500 nm	20-40 nm	9×10^{-10}	0.11	1	Electron	[28]
500 nm	40-80 nm	-	1.46×10^{-7}	-	Electron	[29]
3.2 μm	200 nm	12×10^{-9}	6.4	1	Hole	[26]
3.5 μm	90 nm	7.5×10^{-10}	4.2×10^{-2}	0.5	Hole	[27]

Despite the advancement in fabrication of nanodevices, common issues such as weak gating effect ($g_m < 1$ nS [30]), low I_{on}/I_{off} ratio, low carrier mobility, poor interface quality between NW/dielectric, and off-state leakage current still persist and indicates that this technology is not mature enough and requires some more work.

1.3 Motivation Behind the Work

The down-scaling trend in integrated circuit (IC) technology is about to reach an end-point with conventional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) (also called planar MOSFET) devices because of physical limitation of silicon [31]. Additionally, heat dissipation, operating frequency and off-state power consumption are other challenges in IC with current semiconductor materials. These factors as well as irresistible demand in processing power lead researchers to explore new semiconductor materials in order to replace silicon, which is the extensively used semiconductor industry. Due to superior features of SiC (high breakdown voltage, high operating temperature and high switching frequency etc.), it is one of promising candidate to enhance the semiconductor industry to meet the needs. In this study, we have investigated the fabrication and electrical transport characteristics of SiC nanowire based FETs with different channel length. Furthermore, the figures of merit for transistor performance such as transconductance (g_m), carrier mobility (μ_h), on/off current ratio (I_{on}/I_{off}), and gating effect are

presented for the fabricated SiCNW-FET devices. The dependence of these key performance parameters on SiNW-FETs with varying gaps between electrodes (drain - source) from 120 nm to 1.5 μm is also discussed.

1.4 Thesis Organization

The purpose of this MS thesis to fabricate SiCNW-FET devices with varying channel length and observe the effect of channel length on fundamental transistors parameters. In this scope, different SiCNW-FET devices were fabricated with various channel length and the $I-V$ characteristics including transconductance (g_m), on-off current ratio (I_{on}/I_{off}), carrier μ (μ) and carrier concentration (n_h) were systematically measured.

The thesis is organized as follows:

✓In the first chapter, an introduction to nanostructues and their properties is discussed. Further, previously conducted studies on electrical transport properties of SiCNWs are given with the obtained performance parameters as literature review. At the end, the motivation behind the work and thesis organization are presented.

✓In the second chapter, fabrication process of SiCNW-FET starting from nanowire synthesis to final device has been explained in details. Furthermore, the equipment used in nanowire characterizations such as SEM, XRD etc. and fabrication processes such as MOCVD are also introduced briefly. Finally, the details of fabricated FET devices such as channel length, nanowire diameter, electrode geometry and thickness etc. have been explained.

✓In the third chapter, electrical characterizations of devices have been explained. In addition, the test setup and measurements devices have been described. Further, fundamental transistor parameters have been covered and the obtained values for the fabricated devices have been presented. Additionally, a comprehensive comparison of achieved results with the previously reported studies has been proposed.

✓In the last chapter, a summary of research results and findings are given with the existing issues. Further, possible future of SiCNW research and its electronics applications are discussed.

Chapter 2

SiC Nanowire Synthesis and FET Device Fabrication

In this chapter, the details about the fabrication process of SiCNW-FETs starting from nanowire synthesis to final device has been explained in details. Furthermore, the equipment used in nanowire characterizations such as SEM and XRD and growth process also introduced briefly. Finally, the details of fabricated FET devices such as channel length, nanowire diameter, electrode geometry and thickness etc. have been explained.

2.1 NW Fabrication Methods

1-D nanostructures can be synthesized by many different methods such as nanoparticles self-assembly, carbon nanotube templating, DNA based templating, top-down and bottom-up. Among those, top-down and bottom-up methods are commonly preferred ones as shown in Figure 2.1. Both approaches have advantages and drawback in term of complexity, process cost, and flexibility with respect to 1-D nanostructures synthesis. The two approaches are briefly explained below.

(a) (b)

FIGURE 2.1: NW synthesis approaches[1] (a) Top-Down Methods (b) Bottom-Up Methods

2.1.1 Top Down Methods

Top-down methods involves the process transforming a bulk materials into desired structure by utilizing several lithography, etching and deposition process. This method allows to obtain preciously controlled structures and to integrate into dense design. A good example of top-down method usage is microelectronics (ex. CMOS technology) applications. Because the structures are getting smaller and smaller, fabrication cost and complexity are becoming very difficult to handle. So that, semiconductor industry is searching for new strategies to meet the demands considering economical limits.

NWs can be synthesized by top-down method with highly controlled size in variety geometry such as vertical and planar. Wang *et al.* [32] and Henry *et al.* [33] successfully demonstrated fabrication of Si nanowires with diameter of 20 nm and nanopillar with diameter of 50 nm, respectively. Although NWs has been successfully fabricated via this method, because of the complicated and expensive processes with a low yield of NWs it is persisting there as drawbacks of this approach.

2.1.2 Bottom Up Methods

Bottom-down methods involves the process assembling of small nanoscale blocks into a bigger nanostructures. As the device sizes get close to atomic size, that cannot be obtained by lithography methods, this method can provide a breakthrough solution to technological challenges. This method provides more control and flexibility over the structure geometry and size which can enable to design and realize new devices with geometry and functionality. However, this method is still in development stage, there are some issues remaining.

Although there are some challenges in nanostructures fabrication such as surface defects, doping, and growth orientation, this is the common method used in NW synthesis. Various ways of bottom-up methods have been demonstrated such as Vapor Liquid Solid (VLS) and Vapor Solid (VS) methods. The details and sub-methods of VS are going to be discussed in the following chapter.

2.2 SiCNWs Growth

Variety of methods to synthesize SiC nanowires have been developed. Some of these methods are Chemical Vapor Deposition (CVD), which includes Metal Organic Vapor Phase Epitaxy, Chemical Vapor Reaction, Chemical Vapor Infiltration and Metal Organic Chemical Vapor Deposition, and Physical Vapor Deposition and Sputtering. A brief overview of mentioned methods with some key parameters used in 3C-SiCNW growth is given in Table 2.1.

The SiCNWs used in this study were grown via Metal Organic Chemical Vapor Deposition (MOCVD) method. The growth process in a MOCVD system as as follow; a substrate covered with catalyst material is placed on graphite susceptor and loaded to the system. Source material is transferred to the reactor chamber using a carrier gas, where the growth happens, at certain flow rate. At the beginning of the process, the system is purged a couple of times at low pressure to make sure that all contamination are deported from the chamber.

TABLE 2.1: Typical 3C-SiCNW growth methods and main parameters [5]

Growth Methods	Chemical Vapor Deposition (CVD) (includes Metal Organic Vapor Phase Epitaxy, Chemical Vapor Reaction, Chemical Vapor Infiltration and Metal Organic Chemical Vapor Deposition), and Physical Vapor Deposition and Sputtering
Precursor	Methytrichlorosilane, Drichlorometilsilane, Methane, Propane, Silane, Diethylsilane, Hexamethyldisilane
Starting Materials	Si+SiO_2 with methane; Si+C; SiC powder;
Substrate	(100),(111) Silicon
Catalyst	Ni, Fe, Au, Pt, Pd, Fe/Co, Al
Growth Temperature	From 1000 to 1400 °C

Then the system heated up to desired temperature for NW-growth. Next, the deposition occurs via series of consecutive chemical reaction at the substrate surface and lasts a few minutes to hours based on the system. After the growth is completed high quality nanowires were obtained. Figure 2.2 shows a typical flow diagram for an MOCVD system.

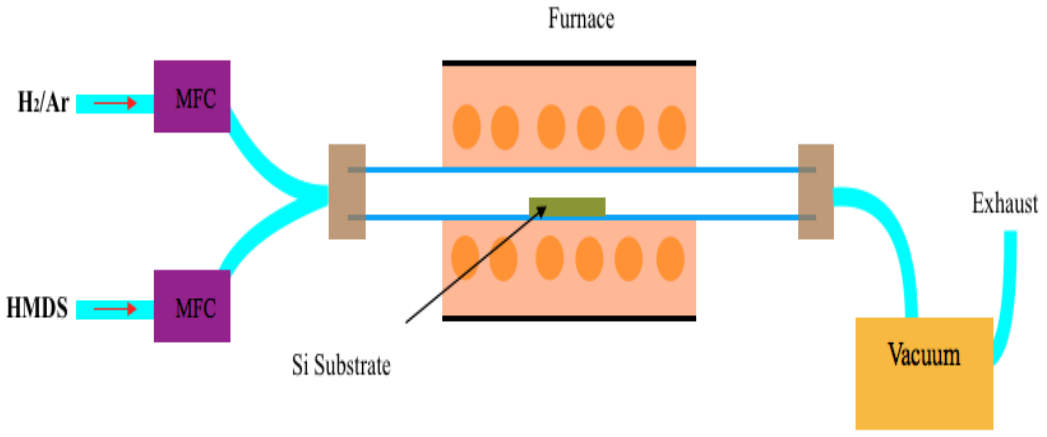


FIGURE 2.2: Flow diadram of a MOCVD system

SiCNWs were synthesized in a horizontal RF-induction heated furnace with hexamethyldisilane (HMDS) as a source precursor. The NWs were grown on oxidized Si substrate

with 300 nm SiO_2 layer coated with Ni particles, which have diameter of 30 nm, as catalyst. A Si substrate was cleaned via a two stage solvent bath in order to remove possible contamination (oils and organic residues from the process or environment) on the surface. A bath of aceton and isopropanol (IPA) were prepared separately by using glass beaker. First, the Si wafer was sonicated in aceton bath for about 5 min with an ultrasonic bath shown in Figure 2.4 a. Once the aceton bath is completed, the substrate was soaked in the IPA solvent for 2-3 min. Then, the silicon wafer was rinsed in de-ionized (DI) water. Although the solvent remove contamination on the wafer surface, solvent themselves might leave some residue on the surface of the substrate. Thus to have a residue free wafer, a two-step solvent method was implemented. Finally, a nitrogen (N) gun was used to wipe out all the remaining DI water and others chemicals from the surface of the wafer. After the cleaning process, NWs in IPA solution were deposited on the cleaned wafer (a highly-doped SiO_2/Si substrate with oxide layer of 300 nm). When the IPA solution with SiCNWs dry, the Si wafer was placed in the center of graphite susceptor (seen in Figure 2.4 b) and loaded to the quartz tube. At the beginning of the process, the reactor were evacuated to 50 $mTorr$ and purged three times in order to remove the contamination inside the quartz tube. Then the system was heated to 1100 °C with 100 standard cubic centimeters per minute (sccm) H_2 and 500 sccm Ar flow within 5 mins. After the temperature stabilizes at 1100 °C, the growth process begins. During the growth, the process temperature was maintained for 15 mins where HMDS source was added to the system via H_2 as carrier gas at flow rate of 10 sccm at 1100 °C with flow of 200 ccm H_2 and 500 sccm Ar. The pressure during the growth was measured as 1 ATM. After the growth process, the reactor has cooled down to 300 °C with 100 sccm H_2 and 200 sccm Ar gas flow. The growth process and parameters are also presented in Figure 2.3 as a function of time. The image of used MOCVD system is shown in Figure 2.5 a.

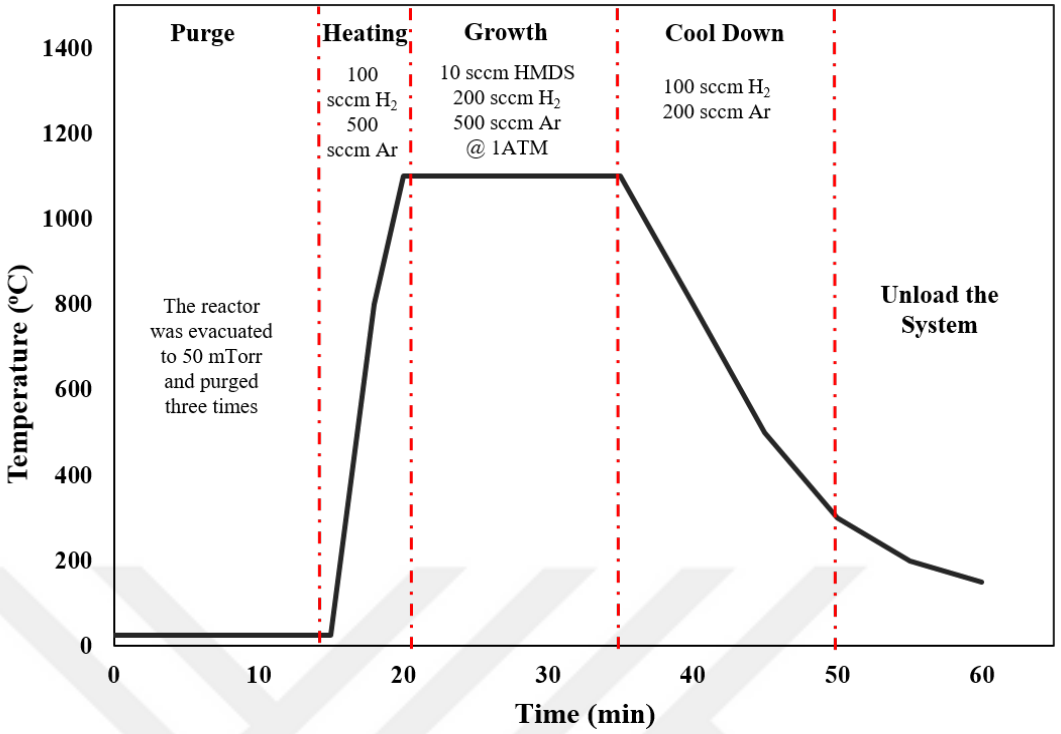
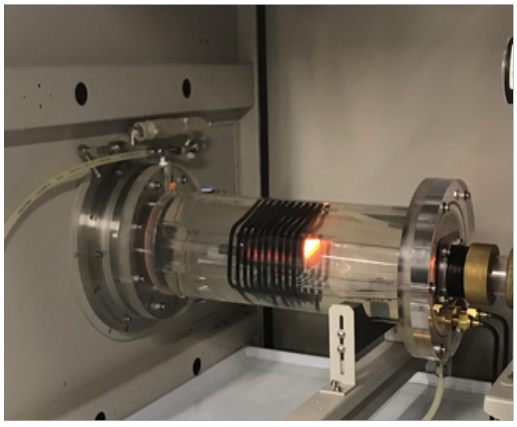


FIGURE 2.3: SiCNW growth process with gas flows and temperature as a function of time in MOCVD system.

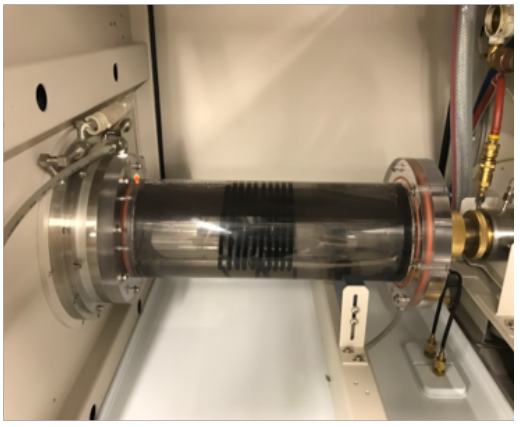
(a) (b)

FIGURE 2.4: (a) Image of ultrasonic bath used for wafer cleaning (b) Image of quartz tube where the nanowire growth take place.

(a)



(b)



(c)

FIGURE 2.5: (a) A photograph of MOCVD system used in SiCNW growth (b) Image of quartz tube during a run. (c) Image of quartz tube.

2.3 SiCNW Characterization

The fabricated nanowires have been characterized via the following equipment; scanning electron microscopy (SEM) and x-ray diffraction (XRD). Crystal structure of as-synthesized nanowires have been analyzed by x-ray diffraction (XRD). Surface morphology has been observed by scanning electron microscopy (SEM). A brief introduction about these equipment and obtained results are discussed in the following section.

2.3.0.1 Scanning Electron Microscope (SEM)

A scanning electron microscope is a microscopy method that provides surface image of desired specimen by using focused beam of electrons. SEM might be really handy when it comes to deal with surface topography of the sample. It provides far better images than the regular optical microscope in terms of resolution and quality. Generally, SEM consists of an electron gun and a couple of electromagnetic lens which operates in vacuum. Electrons generated by electron gun are accelerated to energies level in range of 1-40 keV in the SEM. Then those electrons are used to create focus electron probe by lenses on the specimen. In order to create image, a detector collects the reflected electrons from the surface and creates an image of scanned area of surface via analyzing the observed electrons. Often SEM has two type of detectors, back-scattered electron (BSE) and secondary electron (SE). Although, BSD can give great image about morphology and topography, SE detector has capability to detect electrons with low energy which enables it to provide images at higher magnification. Finally, generated image is displayed on monitor. Figure 2.6 a displays main components and work flow of a typical SEM schematically.

In our experiment, we have used a Phenom XL (shown in Figure 2.6 b) desktop scanning electron microscopy. The microscope can provide images at magnification range from 80× to 1000×. with a resolution up to 10 nm.

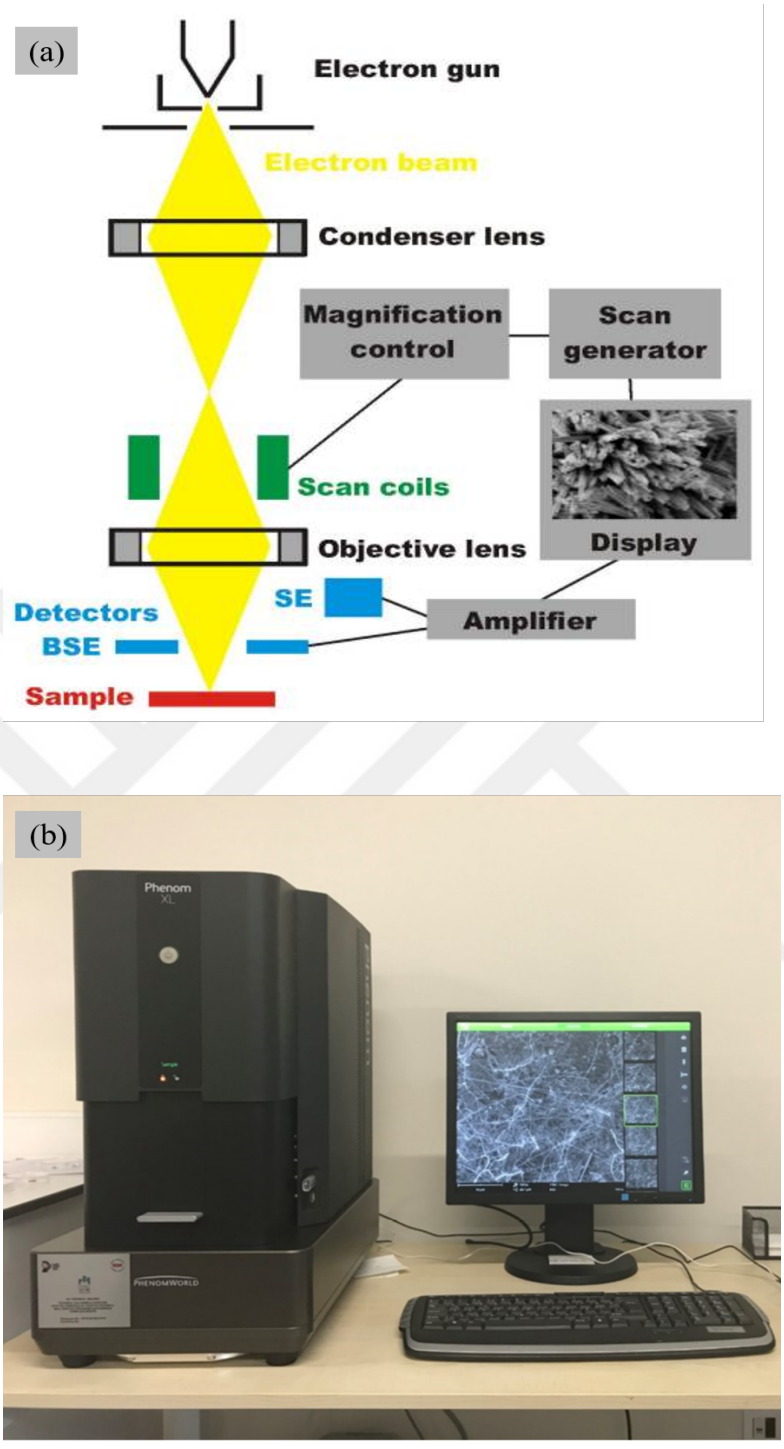


FIGURE 2.6: (a) Schematic representation of a SEM [2] (b) The SEM used in this study.

A number of SEM images of SiCNWs grown at 1100 °C with Ni nanoparticle on a SiO_2/Si substrate has been captured. The captured SEM images at various magnification (such as 2K, 5K, 7K and 10K) are given in Figure 2.7. The images demonstrate that SiC nanowires are distributed over the Si substrate with different densities and have diameter

ranging from 40 nm to 70 nm. The length of the NWs are in range of few μm to tens of μm.

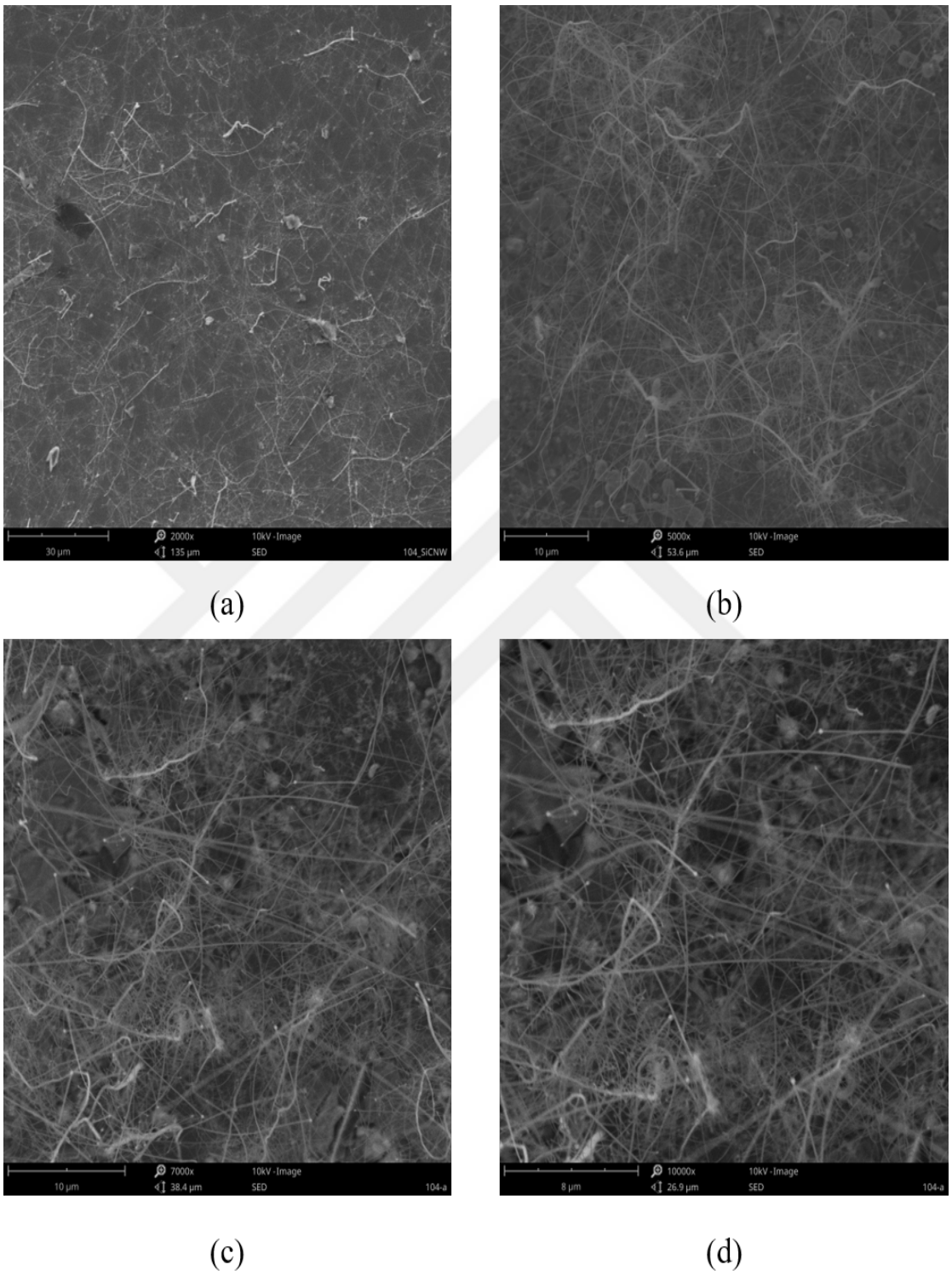


FIGURE 2.7: SEM images of as-synthesized nanowires with diameter of 65 nm and length of 50 μm on the Si substrate with 300 nm SiO_2 layer at different magnifications. (a) At 2K (Scale bar - 30 μm) (b) At 5K (Scale bar - 10 μm) (b) At 7K (Scale - is 10 μm) (b) At 10K (Scale - is 8 μm)

2.3.0.2 X-Ray Diffraction (XRD)

X-ray diffraction is a non-destructive method which uses x-ray to analyze the materials' crystal structure. Based on the measurements in scattering angle, polarization, wavelength and energy of diffraction of x-ray beams from atoms within the sample, it reveals crystalline phase and order, structure properties and atomic arrangement of the analyzed material. Figure 2.8 shows a typical XRD schematic with its main components.

Following the synthesis, XRD analysis was conducted to examine the presence of the SiC nanowires. Captured plot is given in Figure 2.8 b. The y-axis has no unit and x-axis shows the diffraction angle (2θ). The figure shows two strong peaks approximately at 35.6° and 59.9°, which correspond to (111) and (220) planes, respectively. The diffraction patters indicate that 3C-SiC was the main crystalline phase of nanowires (JCPDS card no. 29-1129).

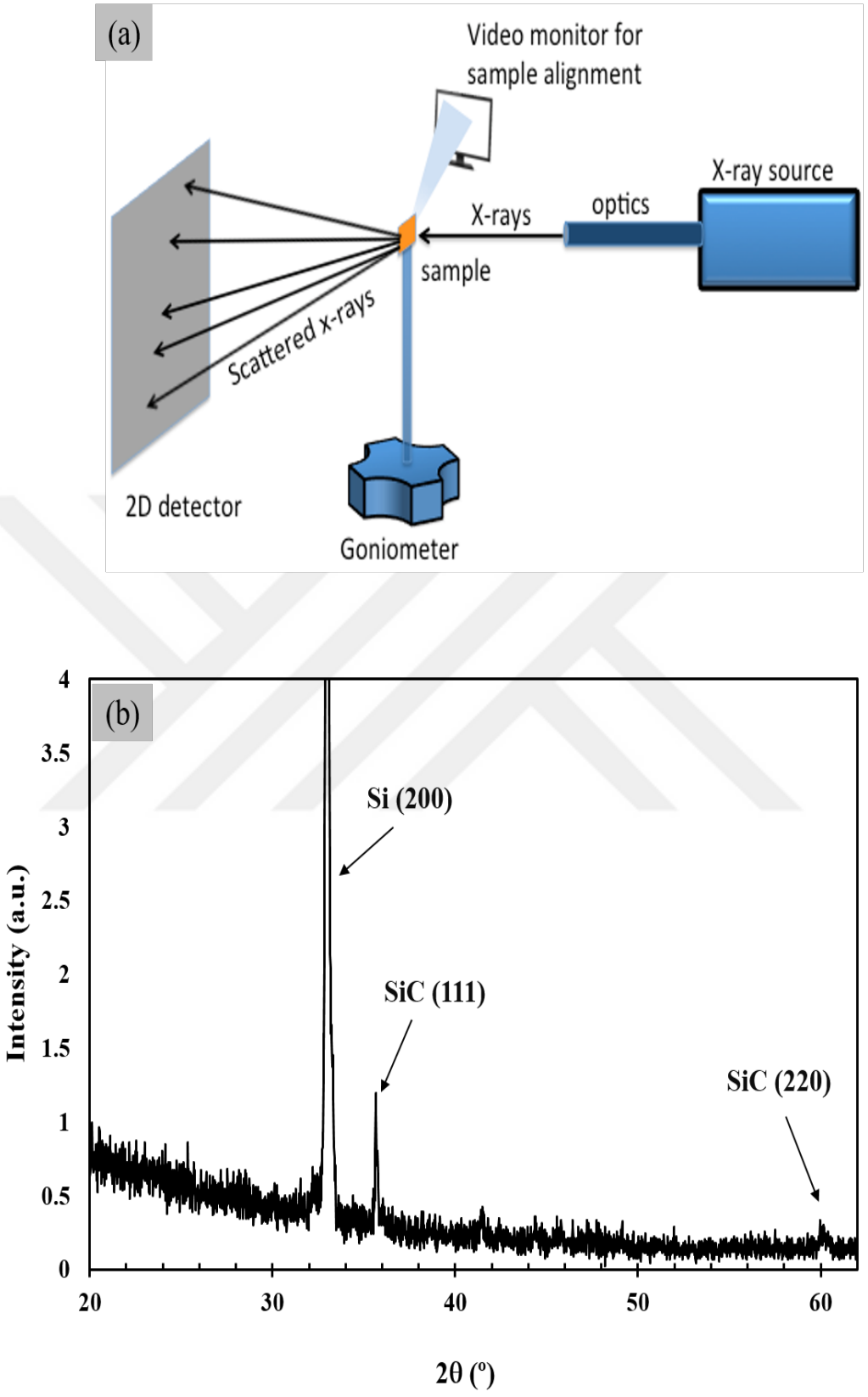


FIGURE 2.8: a) Schematic representation of an XRD [3]. b) XRD pattern of as-grown SiCNWs have zinc-blend structure.

2.4 SiCNW-FET Device Design and Fabrication

2.4.0.1 NW-FET

1-D semiconductors in the form of NW are promising candidates to be the main building blocks in various device applications such as optoelectronics, power electronics, analogue and digital electronics, flexible electronics and display etc. because of their excellent electrical transport properties, high sensitivity, high aspect ration and chemical stability. Further, NW-FETs can sustain the down-scaling in transistor size in IC due to its highly controllable growth and fabrication process. Additionally, NW-FETs have the capability to contribute the off state current leakage and power consumption, which are still bottleneck in Complementary Metal Oxide Semiconductor (CMOS) based devices. NW-FET is a transistor type that utilizes a single nanowire or an array of nanowire as channel material rather than bulk silicon. NW-FETs are three terminal devices with Drain, Source, and Gate similar to traditional transistors. Electrical transport characteristic of a NW-FET is being controlled via an electrical field applied from gate terminal of the device. There are variety of NW-FET architectures out there. Commonly used ones such as back-gate, semi-cylindrical top-gate, and cylindrical gate-all-around NW-FETs are given in Figure 2.9. Each architecture provides particular advantages. The gate-all-around NW-FET schematic, in which the gate material wrap around the nanowire entirely, provides fully control over the channel. In other words, the transistor can respond to the changes in gate voltage very fast and block current flow during the OFF state of the device. Although this architecture can exhibit superior electrical characteristic such as low leakage in OFF state and better stability [34], high cost and difficulties in fabrication process make this structure is not widely used in studies. When it comes to back-gate NW-FET architecture, it is more optimal for sensing applications because the NW surface (the channel) is not covered with electrode material so it has more active area to interact with the target matter. Besides the sensing applications, back-gate NW-FET can also be used in analog and digital electronics. Despite the limited control of back-gate NW-FET over channel compared to gate-all-around NW-FET, back-gate NW-FET devices has been studied extensively due to its relatively simple fabrication process and low cost. It can be fabricated on a commercially available highly doped or degenerated SiO_2/Si wafer used as back-gate terminal of the device. Lastly, semi-cylindrical top-gate

NW-FET architecture can provide less control over the channel compared to gate-all-around NW-FET architecture but better than back-gate NW-FET. This is also not a commonly preferred architecture.

In this study, we fabricated SiCNW-FETs according to the back-gate NW-FET architecture and electrical measurements were carried out by applying gate voltage from back-side of highly-doped substrate. Because of high doping, bulk wafer can be used without metallization.

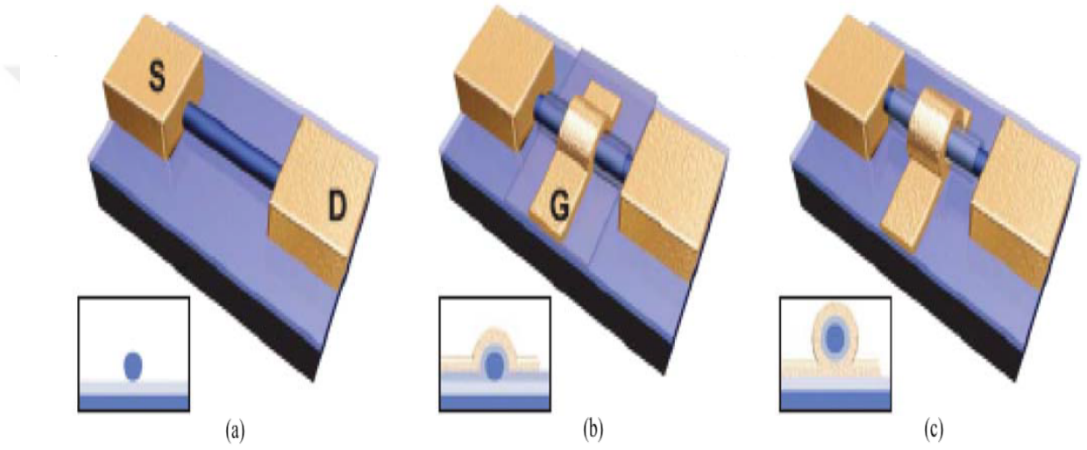


FIGURE 2.9: Schematic representations of NW-FET architectures [4]. (a) Back-gate NW-FET (b) Semi-cylindrical top-gate NW-FET (c) Cylindrical gate-all-around NW-FET. Insets show the cross section of NW-FET at the midpoint of each device.

2.4.0.2 Design Specifications

In this thesis, effect of scaling in channel length on SiCNW based transistor performance has been studied. The key performance parameters including transconductance (g_m), on-off current ratio (I_{on}/I_{off}), carrier mobility (μ) and carrier concentration (n_h) have been calculated for each devices and the effect of channel scaling on these parameters have been examined. For this purpose, a single SiCNW based FET with multiple electrodes designed and channel length of the NW-FET devices were determined to be 120 nm, 220 nm and 1.5 μm.

SiCNW-FET devices were fabricated in back gate NW-FET architecture with a bilayer Cr/Au electrodes, in which the thicknesses are 3 nm and 100 nm) on a highly doped

SiO_2/Si wafer which served as back gate terminal. The width of electrodes are 1 μm on the NW-electrode contact and 200 μm on the electrode- probe contact. Table 2.2 presents the design specifications of fabricated SiCNW-FETs.

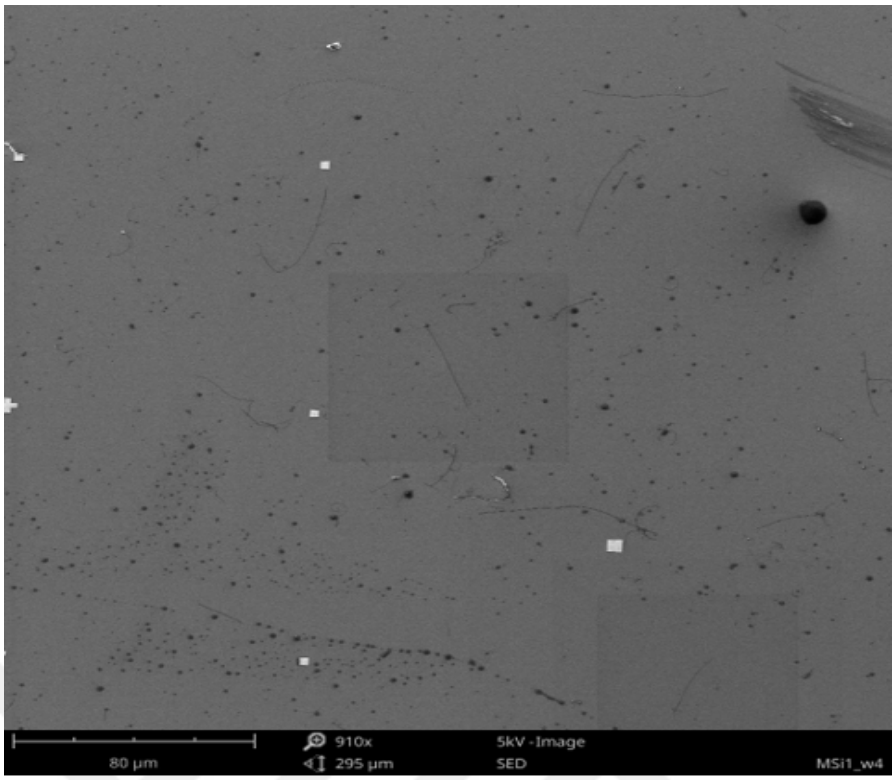
TABLE 2.2: Device specifications including channel length, electrode materials and thickness, substrate and FET architecture

C.L.	**Electrodes**	**Substrate**	**Architecture**
120 nm	Cr(3nm)/Au(100nm)	Highly-Doped p-type SiO_2/Si	Back gate
220 nm	Cr(3nm)/Au(100nm)	Highly-Doped p-type SiO_2/Si	Back gate
1.5 μm	Cr(3nm)/Au(100nm)	Highly-Doped p-type SiO_2/Si	Back gate

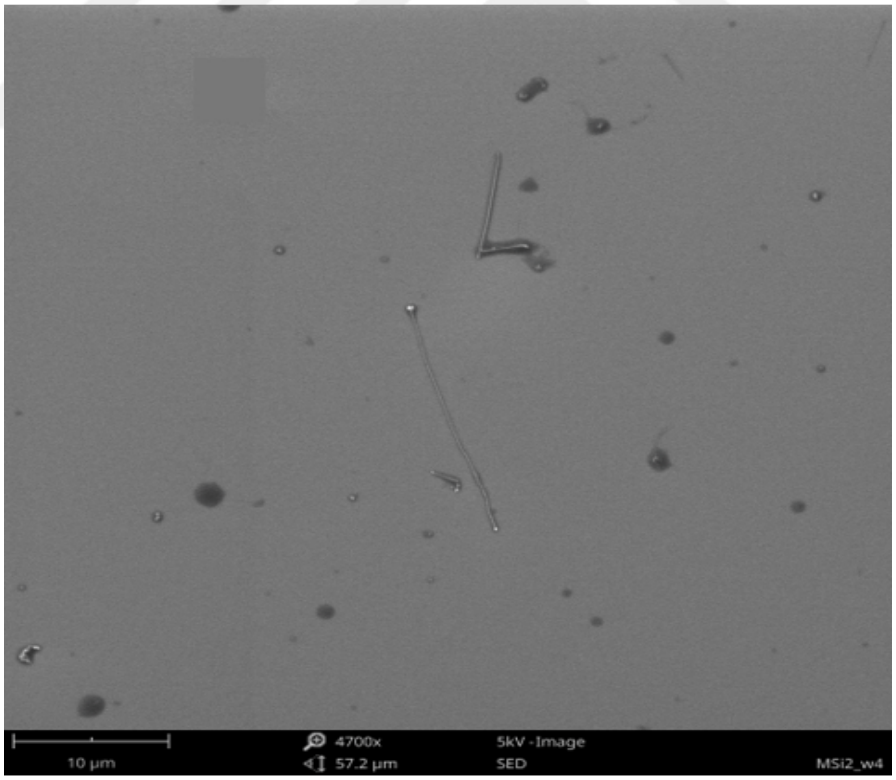
2.4.0.3 Device Fabrication

One way to investigate the electrical characteristics of SiCNW is to configure a single SiCNW as back-gate NW-FET architecture (seen in Figure 2.12). In this architecture, SiCNW-FET devices are fabricated on highly doped or degenerated SiO_2/Si wafer. The fabrication process and details from NW to NW-FET devices will be described below.

Firstly, SiCNWs, synthesized via CVD method using 30 nm Ni catalyst on a Si wafer coated with 300 nm SiO_2 layer, were suspended in some micro-liters of IPA via ultrasonic bath. Then, evaporating some of the IPA, a dense IPA solution which includes SiCNWs was obtained. Then a few drops of NWs dispersed in IPA were deposited on specifically prepared highly doped p-type SiO_2/Si substrate. After the solution dries on the substrate, an SEM was used to locate the NWs to determine the possible nanowires to fabricate the FET devices. A low and high magnification images of NWs on highly doped wafer are given in Figure 2.10. It is obvious that the NWs were distributed over the substrate. Because of very small size of NWs, in order to make easy to locate their coordinates aligned markers were placed on the surface. The white rectangles (aligned markers) seen in the images helps to locate the coordinates of nanowires end points.



(a)



(b)

FIGURE 2.10: SEM image of NWs dropped on SiO_2/Si wafer. The FET devices were fabricated on a selected NW with diameter of 65 nm and length of 50 μm. (a) At 2K (Scale bar is 30 μm) (b) At 5K (Scale bar is 10 μm)

After the selected nanowire's location are determined, the next step is to define the electrodes. The electrodes were defined by the E-beam lithography (EBL) with varying channel lengths within 120 nm to 1.5 μm range. The EBL process was done via Torr E-Beam and Thermal Evaporator. To make the lift-off process more easy, a bilayer coating was applied. First, the Si_2/Si substrate was spin coated with 495 polymethyl methacrylate C4 (PMMA) at 4000 revolutions per minute (rpm) for 55 s. Then, coated substrate was baked at 160 °C for 2 mins. The thickness of coated layer was 200 nm. The second layer was coated on top of the first layer using 950 PMMA C2 with a thickness of 100 nm. Coating and baking conditions were kept same as first layer. Next, the e-beam exposure and lift off took place in an order. Then, the e-beam exposed sample was developed in a methyl-isobutyl-ketone (MIBK) mixture and IPA (with 1:3 ratio respectively) for 1 min and 5 seconds (sec) in MIBK and IPA (1:3). After that, the sample was kept into IPA for 30 sec and followed by dryimg process with nitrogen (N_2) gas. And then, metal deposition for metal electrodes was performed through E-beam evaporation with a 3 nm chromium (Cr) as sticking layer and 100 nm gold (Au) layer. After metallization, the wafer was kept in IPA and dried with N_2 gun.

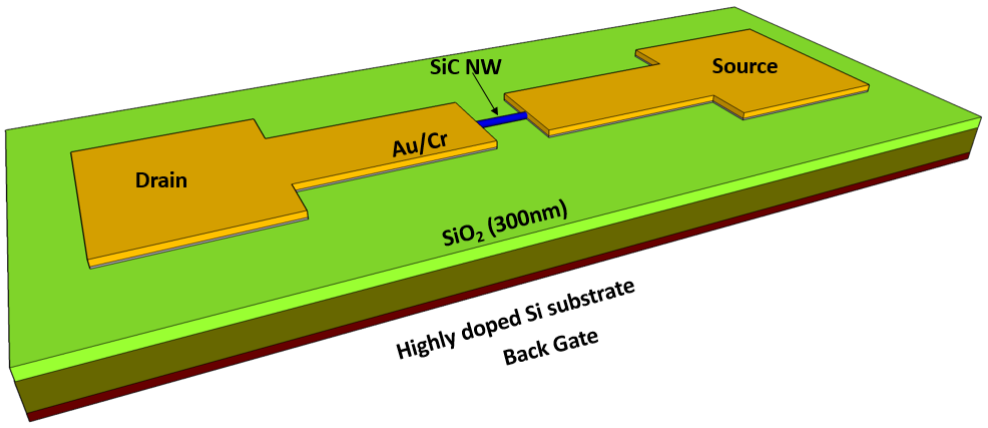
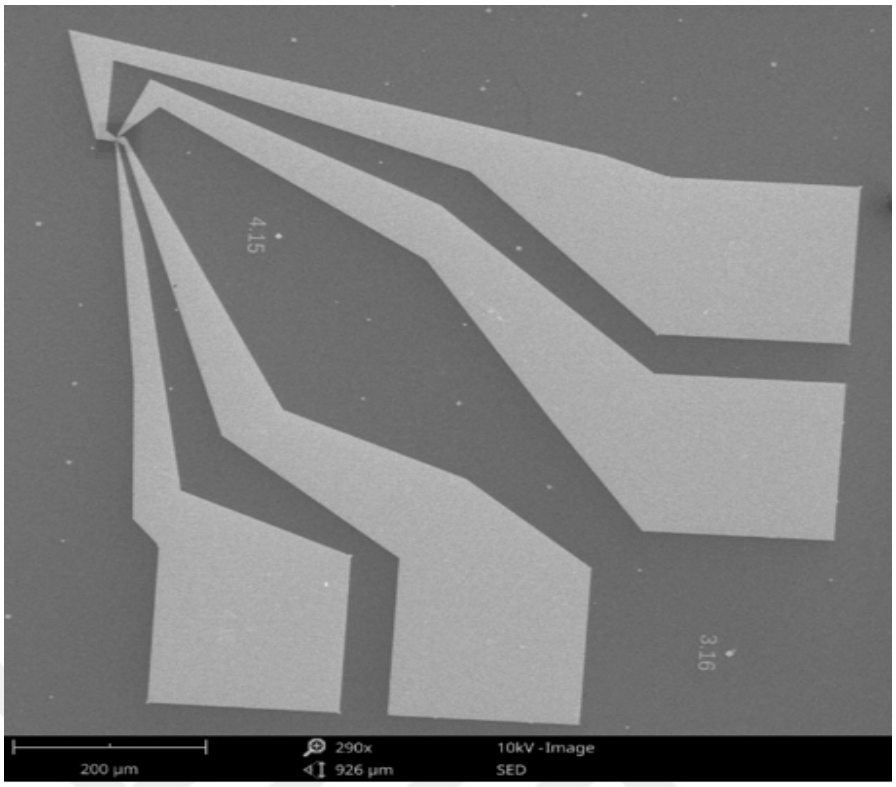


FIGURE 2.11: A schematic view of back-gate SiCNW-FET

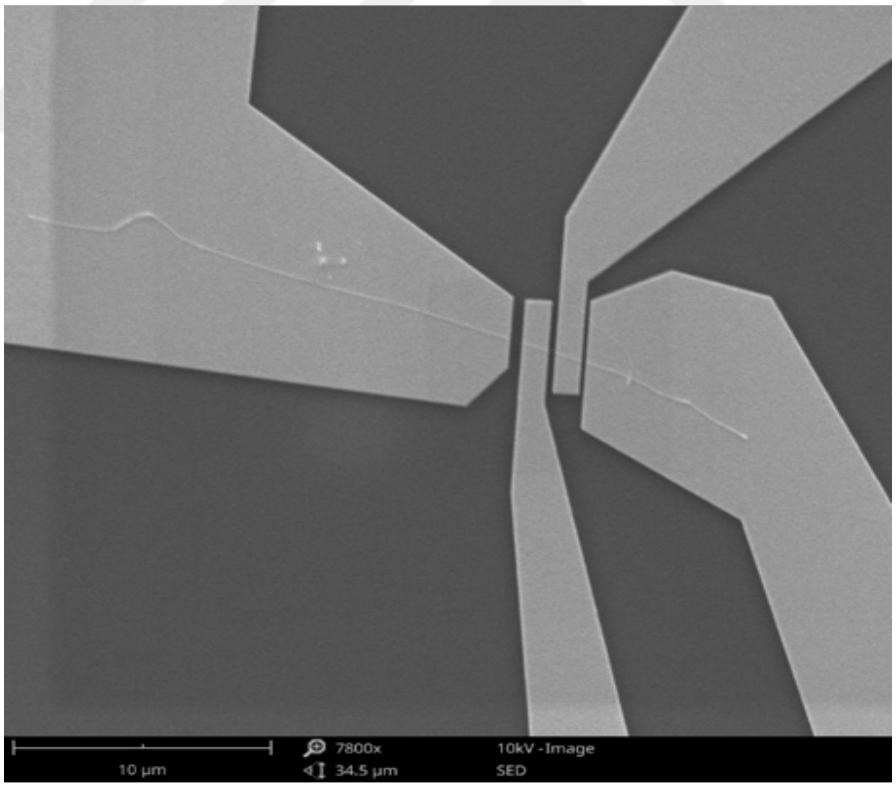
To avoid from peeling off in the Au layer during lift-off process, a Cr with thickness of 3 nm was deposited as an adhesion layer. Cr metal is know as good adhesion material which ensures obtaining better electrode pattern. Then, a Au layer with a 100 nm thickness, which is a very good conducting material used in electrical characterization, was deposited on top of the Cr layer. Figure 2.11 displays a schematic view of back-gate

SiCNW-FET with the details of electrodes and Si substrate. At the end, O_2 plasma treatment was applied to chip in order to remove remaining resists and residues from the exposed chemicals in previous processes.

After the FET fabrication process completed, the devices were checked with SEM in order to make sure that the targeted devices with desired pattern and channel length are achieved. Figure 2.12 a and b show images of actual devices with different magnification. First images (Figure 2.12 a) ensures that a continues electrodes from NW to probing points was obtained. Also there is no connection between any of electrodes pair which might cause a short circuit. Second image (Figure 2.12 b) presents that the electrodes were fabricated on a single SiCNW and all electrodes are connected to the nanowire.



(a)



(b)

FIGURE 2.12: SEM images of fabricated multi-electrodes FET. (a) Low magnification image of FET with four electrodes (b) High magnification image of FET showing channel length and NW.

Chapter 3

Electrical Characterization of 3C-SiCNW

In this chapter, measurement setup and electrical transport characterization of 3C-SiCNWs will be introduced. Furthermore, fundamental $I-V$ characteristics including transconductance (g_m), on-off current ration (I_{on}/I_{off}), carrier mobility (μ_h), carrier concentration (η_h) are briefly explained and obtained results from fabricated NW-FET devices will be presented. And effect of annealing on these parameters will be discussed. Finally, electrical characterization of SiCNW-FETs will be given with a comprehensive comparison with reported devices and performances.

3.1 The Experimental Setup and Equipment

The electrical measurements were carried out with a Keityhly 2634B source-meter and probe station. A schematic view of electrical measurement setup is given in Figure 3.1. A two channel source-meter was used to supply desired voltages to the terminals (drain, source and gate) of the devices. One channel of source-meter was attached to drain terminal of devices as bias voltage. The second channel of source-meter was used for gate voltage. During the measurements the source terminal of FETs were grounded. As it mentioned before, because the FET devices were designed as back-gate NW-FET on a SiO_2/Si wafer used as gate terminal. Measurement process was controlled a computer connected to Keithly 2634B source-meter via KUSB-488B connector. A LabView script

written for $I_d - V_{ds}$ and $I_d - V_{gs}$ curves measurements of 3 terminal devices were used in order to drive the characterization.

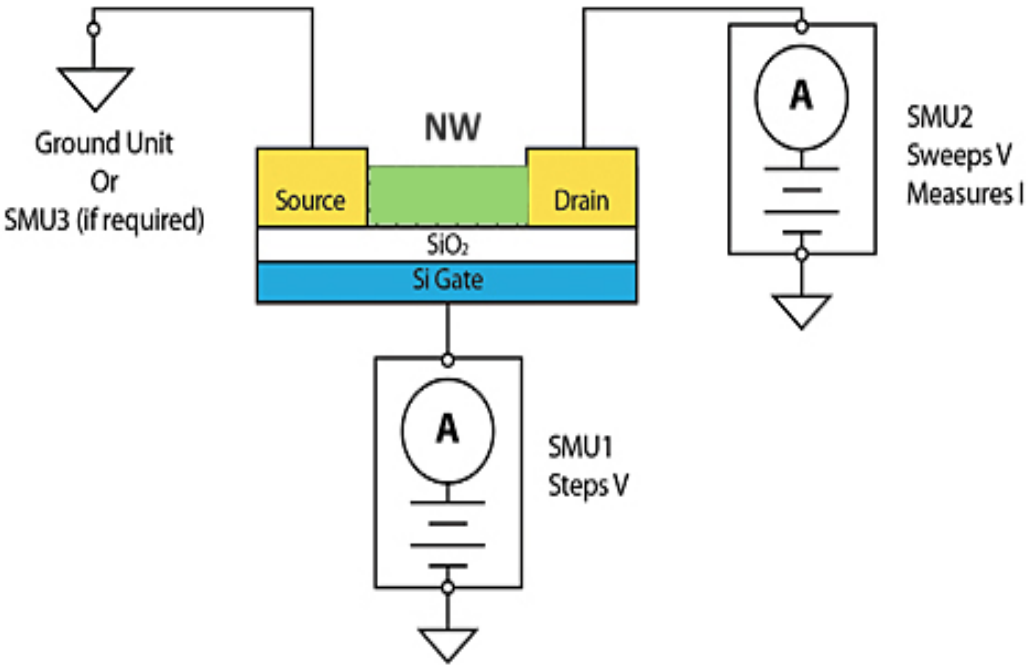
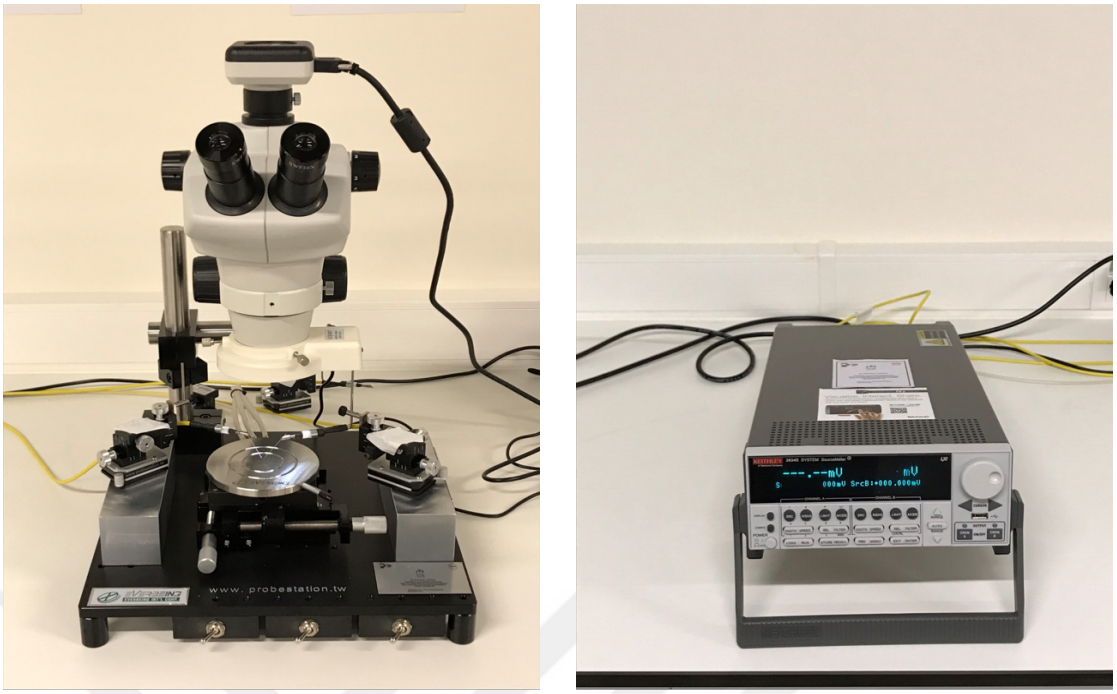


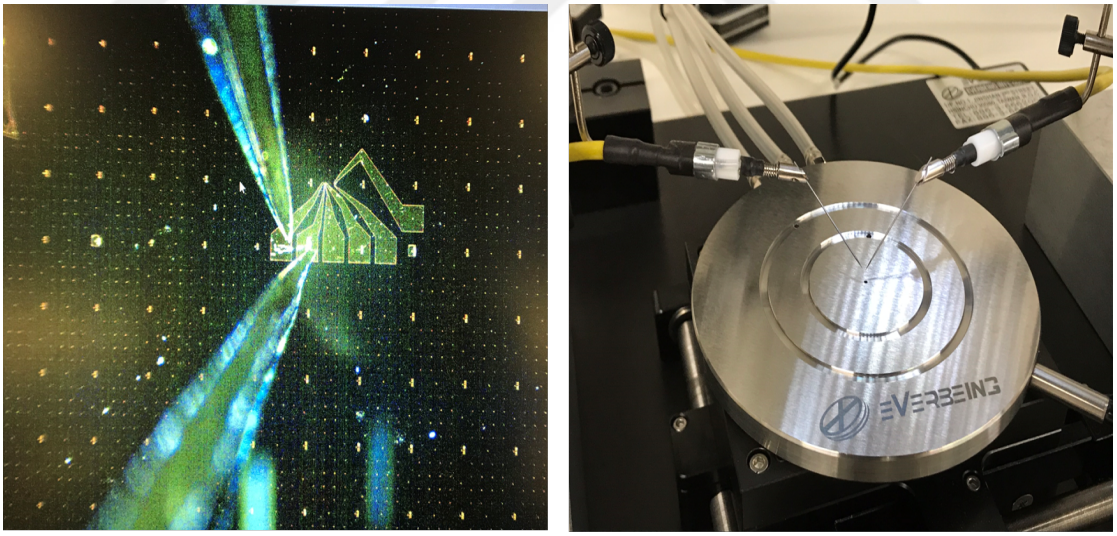
FIGURE 3.1: Test configuration of SiCNW-FET with Keithley 2634 B Source Meter.

To have electrical measurements, firstly the FET devices were located on the probe station (seen in Figure 3.2 a). To avoid damaging the electrodes, a small vacuum pump was used to suck the wafer piece to keep it at the initial position. Figure 3.3 b shows a zoomed image of the surface where the wafer piece was placed and probed. Then by using the optical microscopy corresponding electrodes were probed gently via the metal tips as shown in Figure 3.3 a. Other side of the probes were connected to the two channel of Keithly 2634B source-meter. A photography of source-meter used in measurement is given in Figure 3.2 b. After the probing completed, the electrical measurements have been carried out for each devices under the same condition.



(a) (b)

FIGURE 3.2: A photography of a) probe station and b) Keithly 2634B source-meter used in the experiments.



(a) (b)

FIGURE 3.3: a) An image of probed SiCNW-FET devices on probe station. b) A zoomed image of the plate where the wafer piece was loaded for probing.

3.2 Contact Issues and Annealing

Poor contact quality between nanowire and electrode degrade NW-FETs performance. This is a commonly faced issue in NW-FET devices and the reasons might be the shape of nanowires and possible residues between nanowire-metal junction. Annealing is a necessary process in order to increase the contact quality between SiCNW and electrodes by removing the resist residues between the nanowire-metal sandwich [35]. It is known that annealing lead to formatting a nickel-silicide phases between Ni layer and SiCNW [36], which reduces the contact resistance and make the device to show better electrical performance. Therefore, an annealing was done at 400 °C for 5 min under 5 sccm Ar flow. The annealing process has been very successful such that about twenty-fold increase in current has been measured in most devices. A comparison of the $I-V$ curves of the SiCNW-FET device before and after the annealing process is given Figure 3.4 for the SiCNW-FET with 120 nm channel length.

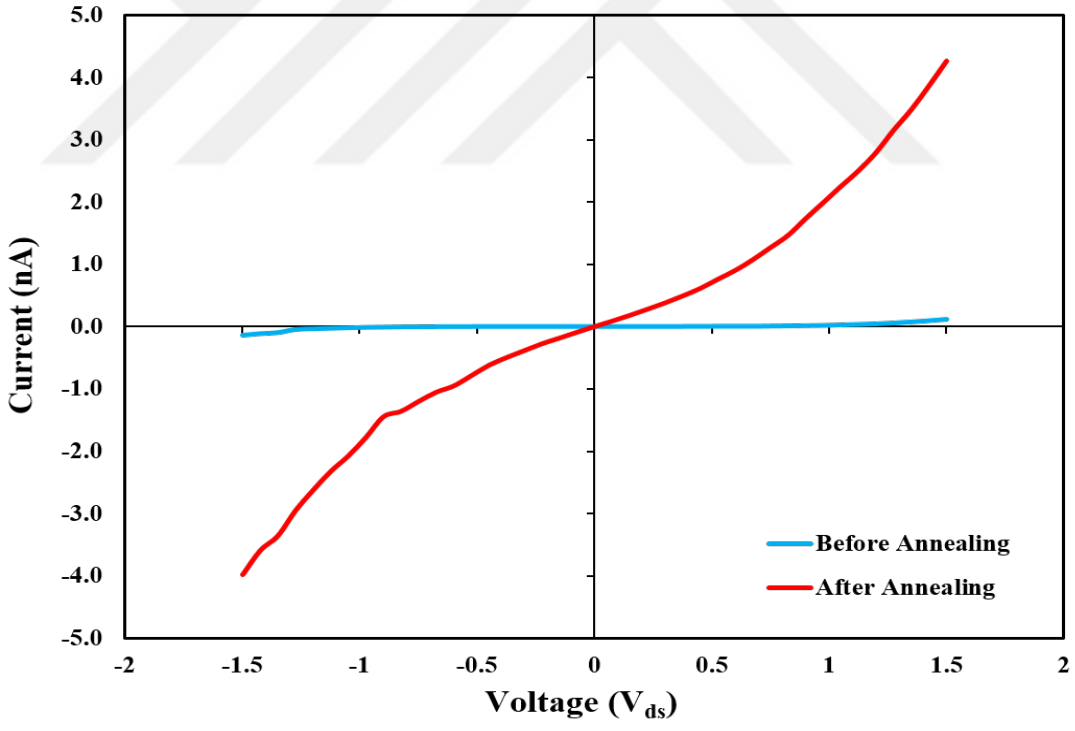


FIGURE 3.4: Comparison of $I-V$ characteristics of the SiCNW-FET device with 120 nm channel length before and after the annealing process ($V_{gs}=0$ V). About thirty-fold current increase is attained after annealing at 400 °C for 5 min with 5 sccm Ar flow.

3.3 Electrical Characterization of SiCNW-FETs

Electrical transport measurements have been conducted on a probe station with a Keithly 2634B source-meters at room condition. From the $I-V$ curves fundamental transistors parameters (transconductance - g_m), on-off current ration - I_{on}/I_{off}) are obtained. Further, using measured g_m value and the given equations carrier mobility (μ_h), carrier concentration (η_h), and gate capacitance (C) of SiCNWs were calculated.

3.3.1 Electrical Properties of SiCNWs

The electrical characteristics of a NW-FET can be interpreted by several figure of merit performance parameters such as transconductance (g_m), carrier mobility (μ_h), and on/off current ratio (I_{on}/I_{off}) are briefly described and the values for fabricated devices are given. A higher value of these parameters indicate that the devices have better electrical performance.

3.3.1.1 Transconductance

Transconductance (g_m) indicates the sensitivity of drain-source current (I_d) to change in gate (V_{gs}) voltage. In other words, it shows how well the transistor adjusts the I_d current when the V_{gs} voltage has changed. The SI unit is S which is current over voltage (A/V). The value of g_m depends on different factors such as channel length, gate width, mobility etc. of the device. Transconductance can be calculated from slope of linear portion of $I_d - V_{gs}$ curve.

3.3.1.2 Carrier Mobility

Carrier mobility (μ_h) also called electron-hole mobility depending on major carrier in semiconductor, represents how fast electron can move in the medium (metal or semiconductor). The units is $cm^2/V.s$. It depends on mostly material itself but also nanowire geometry such as width and height of NW. Carrier mobility can be estimated from the equation 3.3.2 using the obtained g_m from $I_d - V_{gs}$ curve of device.

3.3.1.3 Carrier Concentration

Carrier concentration(η_h), also knows as carrier density reveals the amount of electron or hole per unit volume. In other words, it is the total number of carrier (electron or hole) in conductance band. The SI unit is (cm^{-3}). Carrier concentration of a NW can be obtained via the equation 3.3.4.

3.3.1.4 On-Off Current Ration

On-Off current ration (I_{on}/I_{off}) is the ratio of current on on state and off state of a transistor. It shows how well the transistor can block the current flow in OFF state. The current leakage is essential because it increase the power consumption and decrease the efficiency of circuit. It is difficult to realize NW-FET with a high I_{on}/I_{off} value , because nanowire based devices cannot be turn off well compared to conventional CMOS devices.

3.3.2 Current-Voltage ($I-V$) Characteristics of 3C-SiCNW-FETs

To determine the figures of merit of the SiCNW-FET devices such transconductance (g_m), carrier mobility (μ_h), on/off current ratio (I_{on}/I_{off}), and gating effect drain-source current versus gate voltage (I_d-V_{gs}) and drain-source current versus grain-source voltage (I_d-V_{ds}) measurements have been conducted for each devices. (I_d-V_{gs}) curves were obtained by applying a gate voltages from -30 V to 10 V with the bias voltages of V_{ds} = 0.05 V. The (I_d-V_{ds}) curve measurements have been done by a voltage sweep at the drain-source voltage (V_{ds}) from -1.5 V to 1.5 V at V_{gs} of -20 V, 0 V and 20 V. Recorded I_d-V_{ds} and I_d-V_{gs} curves were given in Figures 3.5, 3.6, and 3.7 for NW-FET devices with channel length of 120 nm, 220 nm, and 1.5 μm, respectively. We could not conduct the I_d-V_{ds} measurements at higher V_{ds} bias voltages since the voltages greater than 3 V could damage the electrodes and cause a peel-off. The measured I_d-V_{ds} curves show that all the devices have non-ohmic contact behaviour since the curves are not linear. Further the reason for quadratic I_d-V_{ds} could be due to the NW-Au electrode contact. This is commonly seen in NW-FET devices since the NW resistant is dominated by contact resistance. The I_d-V_{gs} curves exhibit very strong decrease in drain-source current as the gate voltage varies from -30 V to 0 V indicating that the NWs are p-type.

It can be postulated that host atoms of Si or C are replaced by impurity atoms with less valence electrons leading to creation of hole carriers in the SiC nanowires. Thus, an acceptor energy level is established in the band gap close to the valence band resulting p-type conductivity.

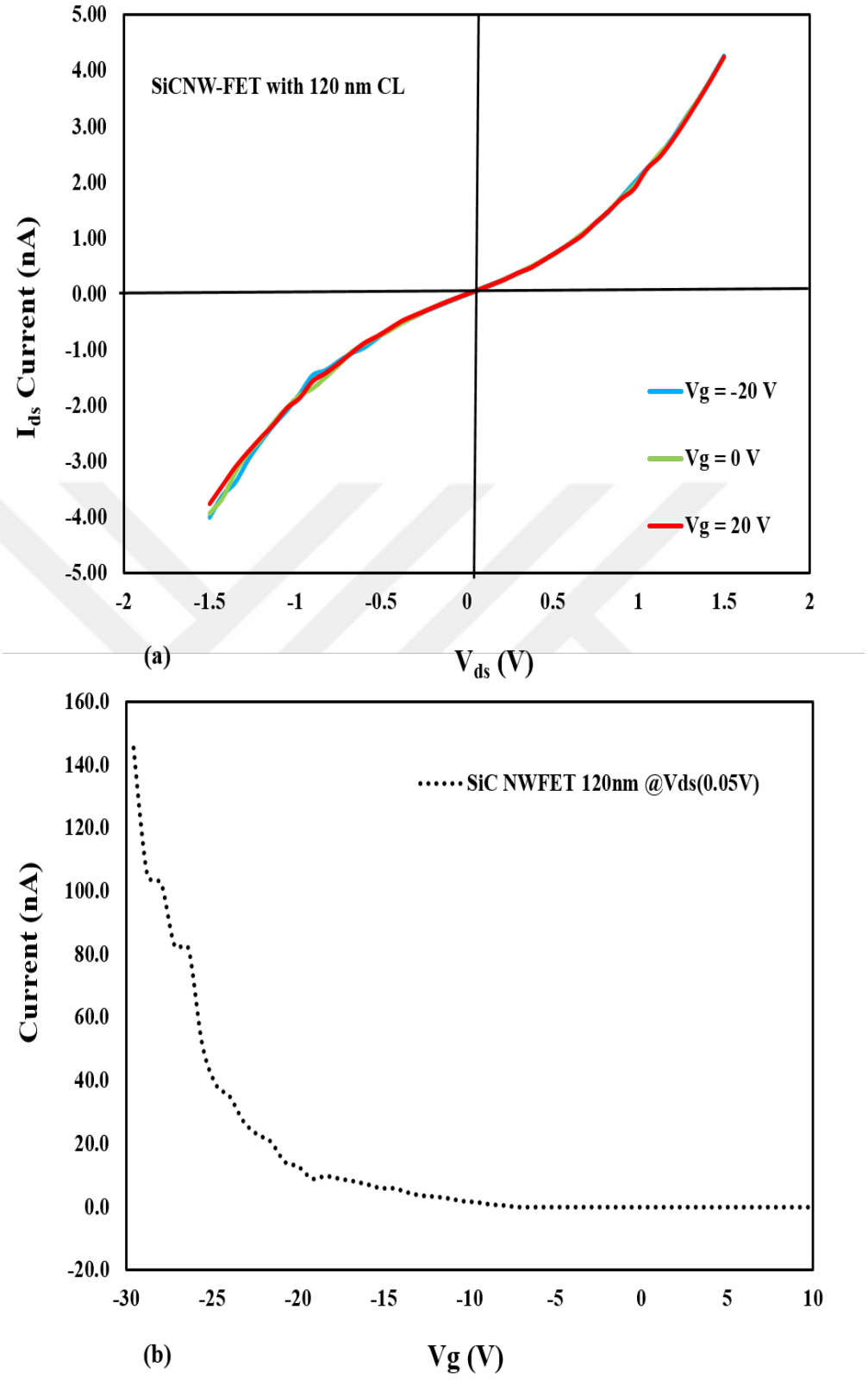


FIGURE 3.5: Obtained $I-V$ curves of the SiC-NWFET devices with channel lengths of 120 nm at V_{ds} = 0.05 V. The device show very strong gating effect. (a) $I_d - V_{ds}$ curve (b) $I_d - V_{gs}$ curve.

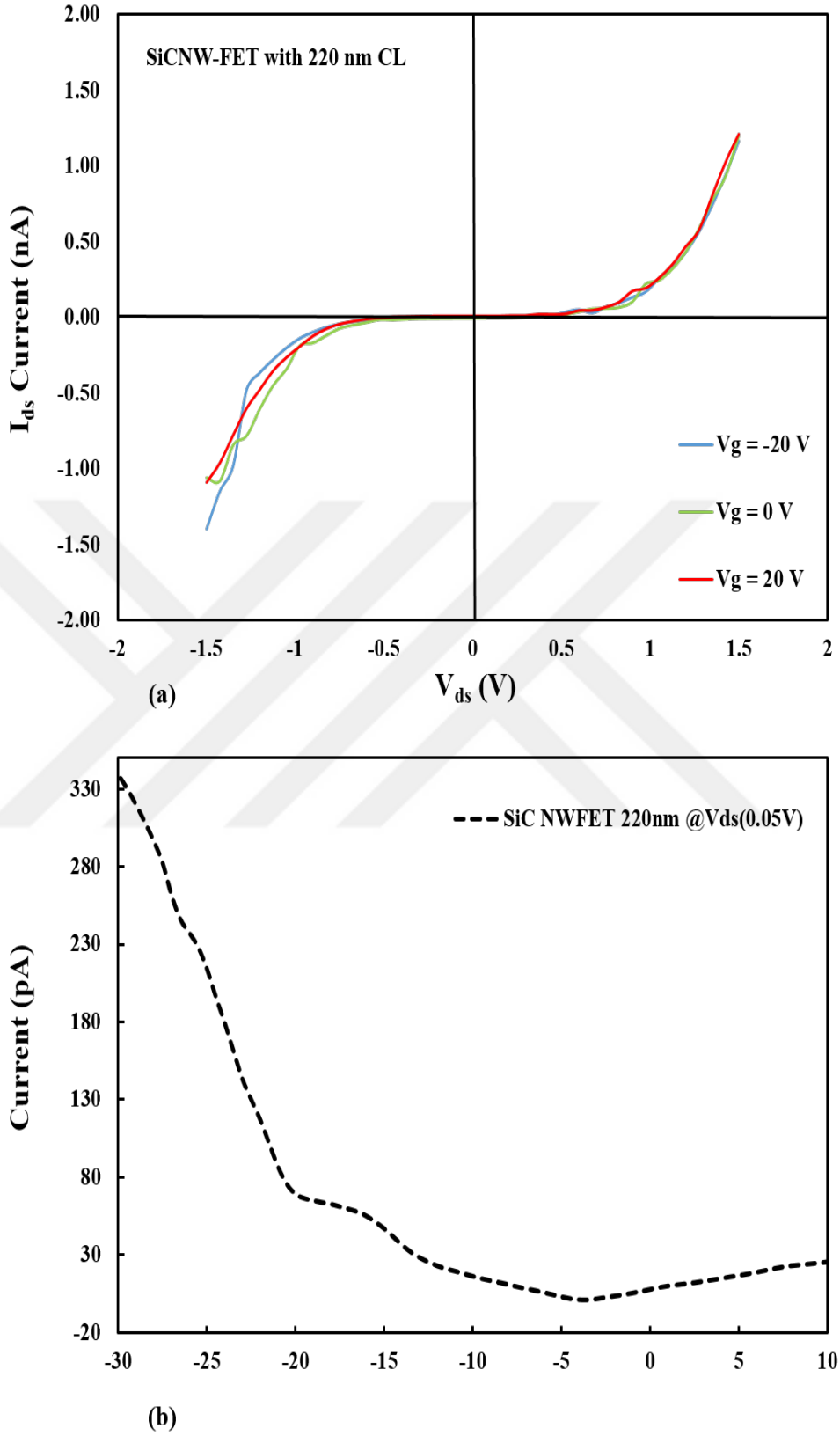


FIGURE 3.6: Obtained $I-V$ curves of the SiC-NWFET devices with channel lengths of 1.5 μm at $V_{ds} = 0.05$ V. (a) $I_d - V_{ds}$ curve (b) $I_d - V_{gs}$ curve.

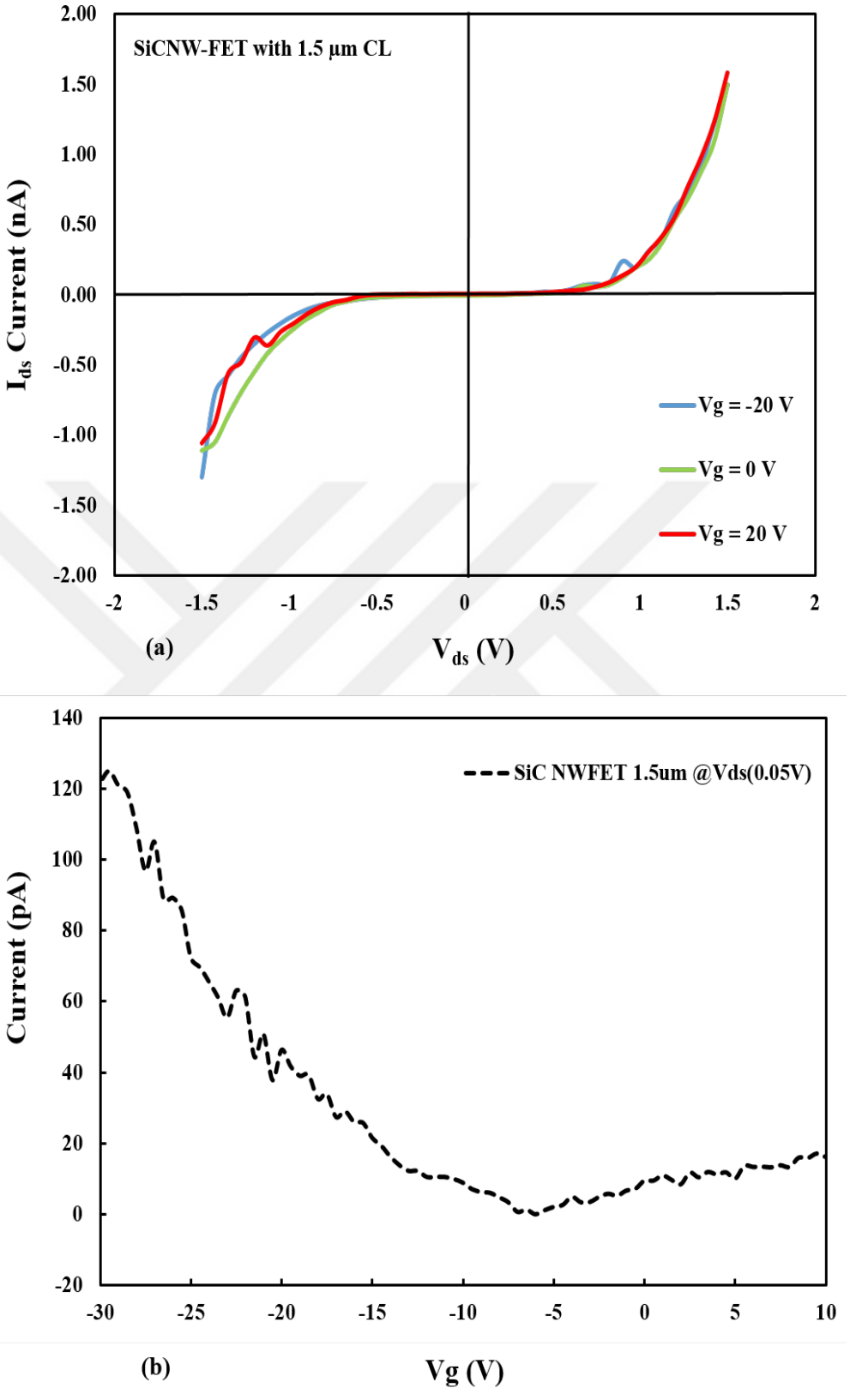


FIGURE 3.7: Obtained $I-V$ curves of the SiC-NWFET devices with channel lengths of 1.5 μm at V_{ds} = 0.05 V.(a) $I_d - V_{ds}$ curve (b) $I_d - V_{gs}$ curve.

Further, the SiC-NWFET devices have shown very high on-off current ratio (I_{on}/I_{off} = 1.34×10^4, 1.04×10^4, and 1.5×10^3) indicating very strong gating effect unlike the reported earlier studies. This result is significantly better than that of the values reported in experimental studies [19, 26, 27] and comparable with the theoretical study [24] in terms of on-off current ratio. Also, other NW-FET devices with channel length of 220 nm and 1.5 μm showed the I_{on}/I_{off} of 1.0×10^4 and 1.5×10^3, respectively.

Transconductance (g_m) was estimated from the linear portion of $I_d - V_{gs}$ curve, also known as transfer characteristic curve by using the Eq.3.3.1. In this study, transconductance was obtained from the slope between -30 V and -20 V and the measured values are 6.9 nS, 2.73×10^{-2} nS, and 7.72×10^{-3} nS for SiCNW-FET devices with channel length of 120 nm, 220 nm, and 1.5 μm, respectively. The g_m of NW-FET with 120 nm channel length is highest reported value at this (120 nm) channel length and bias voltage (V_{ds}=0.05 V).

$$g_m = \frac{dI_d}{dV_{gs}} \tag{3.3.1}$$

After obtaining the g_m of devices, carrier mobility (μ_h) can be calculated from the Eq.3.3.2, where L is the channel length, C is the coupling capacitance between SiCNW and the substrate (back-gate). C can be estimated from the cylinder-plate capacitance model shown in Eq.3.3.3, in which ϵ and ϵ_o are dielectric constants of SiO_2 (∼3.9) and permittivity of vacuum (8.854×10^{-14} F/m), where h is the SiO_2 layer thickness and r is the radius of nanowire.

$$\mu_h = g_m L^2/(CV_{ds}) \tag{3.3.2}$$

$$C = 2\pi\epsilon\epsilon_o L/(\ln 2h/r) \tag{3.3.3}$$

The device with 120 nm has an estimated carrier mobility of 1.69 $cm^2/V.s$ at V_{ds}=0.05 V, which is highest in previous reported studies for p-type SiCNW-FETs [26, 27]. The devices with 220 nm and 1.5 μm have the carrier mobility of 6.71×10^{-3} and 1.89×10^{-3}, respectively, at V_{ds} of 0.05 V.

Further, the hole carrier concentration (η_h) can be obtained from the Eq.3.3.4, where p is the hole carrier concentration, q is the electron charge, and A is the NW cross-sectional area. The estimated hole concentration is 3.72×10^{20} cm^{-3} at V_{ds} voltage of 0.05 V. Other devices with 220 nm and 1.5 μm have the carrier concentration of 3.61×10^{20} cm^{-3} and 3.97×10^{20} cm^{-3}, respectively, at V_{ds} of 0.05 V. It is important to note that SiC can become degenerate for acceptor concentrations above 1.0×10^{21} cm^{-3} [37].

$$I = \eta_h q \mu_h V_{ds} A / L \tag{3.3.4}$$

A summary of obtained values for parameters including g_m, μ_h, η_h, C, V_{th} and R_{on} of SiCNW-FET devices and some other experiments details are given in Table 3.1.

TABLE 3.1: Summary of performance parameters for fabricated 3C-SiCNW-FETs with 120 nm, 220 nm and 1.5 μm channel length

3C-SiCNW-FETs	**NW-FET 1**	**NW-FET 2**	**NW-FET 3**
Diameter (nm)	65	65	65
C.L. (nm)	120	220	1500
C (F)	1.17×10^{-17}	2.14×10^{-17}	1.46×10^{-16}
g_m (nS)	6.9	2.73×10^{-2}	7.72×10^{-3}
μ_h ($cm^2/V.s$)	1.69	6.71×10^{-3}	1.89×10^{-3}
η_h (cm^{-3})	3.72×10^{20}	3.61×10^{20}	3.97×10^{20}
V_{th} (V)	-10.22	-10.24	-10.25
R_{on} (Ω)	357 K	92.9 M	299 M
V_{ds} (V)	0.05	0.05	0.05

3.4 Results and Comparison with Other Studies

Until now, very few theoretical and experimental studies have been conducted to investigate electrical transport properties of SiCNWs. All reported results show that the devices perform similar electrical characteristics. In most of these studies, the nanowires showed n-type semiconductor behavior but only in two studies [26, 27] NW-FET devices exhibited p-type behaviour. Thus, we compared our results with these two studies. Because of the very big difference in values of both V_{ds} and channel length we recalculated hole mobility (μ_h) and hole concentration (η_h) of Chen *et al.*'s and Li *et al.*'s parameters with following assumptions:

- The channel length of the reported SiCNW-FET devices in [26, 27] are 3.2 μm and 3.5 μm, respectively, where out device has channel length of 120 nm.

- The $I_d - V_{gs}$ measurements were carried out at V_{ds} voltages of 0.5 V and 1 V in [26] and [27], respectively. In this, we conducted the electrical measurements at $V_{ds} = 0.05$ V.

Thus, we calculate the performance parameters as these devices have channel length of 120 nm and V_{ds} of 0.05 V.

Having determined the important FET parameters, a comparison of these parameters with the recently reported p-type SiCNW-FETs has been provided as seen Table 3.2.

TABLE 3.2: Comparison of the on-off current ratio, transconductance, hole mobility, and hole density at the same V_{ds} of 0.05 V with the various channel lengths of the p-type SiCNW-FETs

C.L.	**NW Dia.**	I_{on}/I_{off}	g_m	μ_h	η_h	**Ref.**
3.2 μm	100 nm	1.5	12	1.45	7.19×10^{19}	[26]
3.5 μm	90 nm	1.6	0.75	1.57	2.99×10^{20}	[27]
120 nm	65 nm	1.34×10^4	6.9	1.69	3.72×10^{20}	T.W.

The devices presented in this study showed far better performance in terms of I_{on}/I_{off} ration compared to other two studies. A comparable on-off current ratio was achieved with graphene based tunnelling field effect transistors [38].

3.5 Effect of Channel Scaling on Performance of SiCNW-FETs

Further, we investigated the channel length dependent transport characteristics including on-off current ratio, transconductance, hole mobility, and hole concentration of single SiCNW based FETs with various channel length ranging from 120 nm to 1.5 μm. It can been seen that the values of I_{on}/I_{off}, g_m, and μ_h decrease with the increase in channel length as seen in table 3.3. The value of carrier density (η_h) stayed constant with a small fluctuation. A similar study was conducted by Jo *et al.* [39] to examine the effect of channel length scaling on In_2O_3 nanowire FETs by utilizing a movable Pt (Platinum) coated tip act as drain electrode on NW. The same phenomena, a decrease in g_m with

increasing channel length, was observed in their study as well. However, in contrast to our observation in μ_h they reported a decrease in μ_h as the channel length increases.

TABLE 3.3: Channel length dependence of SiCNW-FETs figure of metrit parameters on-off current ratio, transconductance, hole mobility, and hole density at V_{ds} of 0.05 V for the various channel lengths such as 120 nm, 220 nm, and 1.5 μm

C.L.	$\boldsymbol{I_{on}/I_{off}}$	$\boldsymbol{g_m}$ $\boldsymbol{(nS)}$	$\boldsymbol{\mu_h}$ $\boldsymbol{(cm^2/V.s)}$	$\boldsymbol{\eta_h}$ $\boldsymbol{(cm^{-3})}$
120 nm	1.34×10^4	6.9	1.69	3.72×10^{20}
220 nm	1.0×10^4	2.73×10^{-2}	6.71×10^{-3}	3.61×10^{20}
1500 nm	1.5×10^3	7.72×10^{-3}	1.89×10^{-3}	3.97×10^{20}

Apart from the channel scaling analysis, although the device with 120 nm channel length showed better performance than the other two reported devices in terms of g_m and μ_h, the devices with 220 nm and 1.5 μm channel length performed a bit poor performance. Such a low value in g_m causes low I_d current, might be because of high contact resistance in some electrode pairs. As we observed from the $I_d - V_{ds}$ curves, the R_{on} values of these two devices, the contact resistance is too high which could causes poor results.

Chapter 4

Conclusion and Future Work

4.1 Conclusions

The down scaling trend in device size and the increasing demands for faster and more power efficient devices encourage global efforts to search for alternative materials and geometry for new device design and integration with current technologies. 1-D nanostructures, namely nanowires, are one of the promising candidate and are being studied in recent years. In this MS.Thesis, we studied on electrical transport characteristics of single SiCNW-FETs which have very similar electronic features with Si. The focus of study was to explore the impact of channel scaling on NW-FET performance parameters such as I_{on}/I_{off}, g_m, and μ_h. In Chapter 1, I have introduced the class of nanostructures and their high potential to be used in various areas such as nanoscale electronics, sensors, photonics etc. Also, similar studies on electrical transport properties of SiCNWs nanowire based transistors were summarized. In Chapter 2, SiC nanowire synthesis methods and commonly used bottom-up approach were discussed. Further, the details about device fabrication from NWs synthesis to final NW-FET processes were explained. The equipment used in the experiments and their function were explained. In Chapter 3, the scaling effects on figures of merit of the SiCNW-FET devices such as transconductance (g_m), on/off current ratio (I_{on}/I_{off}), and mobility (μ_h) as a function of channel length was investigated. For that purpose, drain-source current versus gate voltage ($I_d - V_{gs}$) and drain-source current versus grain-source voltage ($I_d - V_{ds}$) measurements for each devices have been done. Performance parameters were calculated for every device and

compared with previously reported studies. It was observed that there is a negative correlation between the values of I_{on}/I_{off}, g_m, and μ_h and channel length of the device.

Electrical transport characteristics of the MOCVD-grown SiCNW-FET devices with varying channel lengths from 120 nm to 1.5 μm have successfully been demonstrated. SiCNW-FETs have shown very high on/off current ratios (Ion/Ioff =1.34×10^4, 1.04×10^4, and 1.5×10^3) and strong gating effects, particularly with the smallest channel length of 120 nm. A comprehensive comparison of the important FET parameters with the recently reported p-type SiCNW-FETs has also been provided. As a consequence, very high on-off current ratio, strong gating effect, and very low off-state current make SiCNWFETs very promising candidates for high frequency and high temperature electronic and sensing applications.

4.2 Future Work

In this study, electrical transport properties of the MOCVD-grown SiCNW based FET devices with varying channel lengths ranging from 120 nm to 1.5 μm and impact of channel scaling on SiCNW-FETs performance have been explored. Although the devices exhibited very high I_{on}/I_{off} ratios, g_m and μ_h values are relatively low compared to CMOS devices. This is due to the commonly faced problems degrade performance of our devices. Despite the advancement in fabrication technologies of nanostructures and nanodevices, common issues such as weak gating effect, low on/off ratio, low carrier mobility, poor contact quality and interface quality between NW-dielectric junction, and high off-state leakage current still persist out there to be resolved. Also, these issues indicate that the corresponding technology is still in developmental stage and requires some more work to. In order to realize new devices with high performance (high g_m and μ_h), it is essential to fully understand the synthesis of high quality nanostructures. The electronic controllability issues originated from gate architecture of NW-FET such as weak gating effect, low on/off ratio, high off-state leakage current can be improved by implementing the gate-all-around NW-FET devices with low cost and complexity. Apart from the development in fabrication methods, electrical modeling of SiCNW-FET devices are still out there to be figured out. That might be the next step of the study.

SiCNWs merge particular features of one-dimensional materials with that of superior intrinsic SiC characteristics and enable to realize advanced devices that can function at high frequency, high power and harsh environment.

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