ISTANBUL OKAN UNIVERSITY

INSTITUTE OF SCIENCES AND ENGINEERING

DESIGN AND ANALYSIS OF HIGH POWER SEPIC CONVERTER

A THESIS

submitted by

IBRAHIM HALIL HAYIRLI

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2019

Program: Power Electronics and Clean Energy Systems

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ABSTRACT

DESIGN AND ANALYSIS OF HIGH POWER SEPIC CONVERTER

A high power SEPIC converter is proposed to be used in automotive and railway LED applications. The input voltage of the converter varies between 16 V and 36 V. The output voltage of the converter is 24 V and it delivers 10 A current to the load. The stability of the converter is guaranteed by moving one of the dominant pole to lower frequency and canceling the other pole with a zero. The phase margin is higher than 56^o across all input voltage values. The transients of the switch is damped using a passive snubber circuit. Electromagnetic analyses are performed using Ansys SiWave™ to determine voltage drop, current distribution, near and far field and resonance behavior of SEPIC converter. Measurement results indicate that the SEPIC converter is stable under various operating conditions.

Keywords: SEPIC, LED driver, DC-DC Converters, MOSFET, Light Emitting Diodes

KISA ÖZET

Yüksek güçlü SEPIC dönüştürücü otomotiv ve demiryolu LED uygulamalarında kullanılmak üzere hazırlanmıştır. Dönüştürücünün giriş voltajı 16 V ile 36 V arasında değişmektedir. Dönüştürücünün çıkış voltajı 24 V'tur ve yükü 10 A akım ile beslemektedir. Dönüştürücünün kararlılığı, baskın kutuplardan birini düşük frekans marjinine taşımak ve diğer kutupa da bir sıfır eklenerek iptal etmek suretiyle garanti edilmektedir. Faz marji, tüm giriş voltaj değerleri boyunca 56 dereceden daha yüksektir. Anahtar üzerindeki geçişler snubber devresi ile bastırılmıştır. Elektromanyetik analizler, SEPIC dönüştürücünün gerilim düşümü, akım dağılımı, yakın ve uzak alan ve rezonans davranışını belirlemek için Ansys SiWave kullanılmıştır. Ölçüm sonuçları, SEPIC dönüştürücünün değişken yükler altında kararlı olduğunu göstermektedir.

Anahtar Kelimeler: SEPIC, LED Sürücü, DC-DC Çeviriciler, MOSFET, Diyot

To Zeynep Bade Hayırlı..

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SYMBOLS

V_{in} Input Voltage

V_{out} Output Voltage

L_1–L_2 Coupled Inductors

C_c Coupling Capacitor

C_f Output Filter Capacitor

R_L Output Load

D Duty Cycle

F_s Switching Frequency

ACRONYMS

SEPIC Single Ended Primary Inductor Converter

DC Direct Current

AC Alternating Current

SSA State Space Average

PCC Peak Current Controlled

CCM Continuous Current Mode

DCM Discontinuous Current Mode

OVR Over Voltage Ripple

PCC Peak Current Controlled

PWM Pulse Width Modulation

PID Proportional-Integral-Derivative

PFC Power Factor Correction

THD Total Harmonic Distortion

GA Genetic Algorithm

MPPT Maximum Power Point Tracking

PV Photovoltaic

BLDC Brushless Direct Current Motor

I. INTRODUCTION

1.1. Background

1.1.1. Inductance

Inductance is one of the main components of power converters. The converters work by transferring the energy stored on the inductance to the output or the next loop of circuit. The equation of voltage and current relationship for inductance is given below:

$$V = L\frac{di}{dt} \tag{1.1}$$

Time dependent change of the inductance current causes a voltage change. L indicates the value of inductance. If saturation effect is not considered, it is assumed that the value of inductor is fixed. In DC-DC converters, current and voltage waveforms are rippled due to switching, however it is desired to fix the average current and voltage waveforms. The equation of average voltage and current relationship for inductance is given below:

$$V = \bar{L}\frac{d\bar{I}}{dt} \tag{1.2}$$

If average current is constant, the differential of current will be zero. In that case, the average voltage of inductance will also be zero.

1.1.2. Capacitance

Capacitance is the other main part of power converters. The converters work by transferring the energy stored on the capacitance to the output or the next loop of circuit. The equation of voltage and current relationship for capacitor is given below:

$$i = \frac{1}{C}\int vdt \tag{1.3}$$

Average voltage of capacitor is constant and according to the above equation, steady

state average current of capacitor is zero because voltage is constant with respect to time. Capacitor impedance varies with respect to working frequency of the power converter. Temperature of capacitor is affected by the capacitor impedance.

1.2. Literature Review

Selection of components is important part of designing SEPIC converter. They have very significant role in conversion of power. Coupling capacitors and coupled inductors are widely used in DC-DC converters. Effect of coupled inductors in SEPIC converters are discussed in [1]. In order to prevent ripple currents, a suitable coupling capacitor has been used and tightly or loosely coupled inductors are selected according to this coupling capacitor. Inductors can be used in two different formats which are coupled inductors and transformers. There is an air gap in coupled inductors, but transformers do not have that. In ideal transformers, amount of power flow is equal at input and output. This is not the case for coupled inductors [2]. They have different roles in circuits. Inductors store energy; transformers transfer energy. Coupled inductors are slightly different from uncoupled ones because coupled inductors have small volume when compared to the uncoupled inductors. Coupled inductors see equal impedance with coupling capacitor at resonant frequency and coupled inductor provides full duty cycle adjustment through resonant frequency. This is explained in technical literature in [3], [4], [5], [6]. Coupled inductors are used advantageously in SEPIC converters [7]. Input and output current ripple of the coupled inductor is related to the magnetic coupling factor. When small leakage inductance level is achieved in coupled inductance, the magnetic coupling factor is almost equal unity. Thus, that type of coupled inductor has a critical role for stability when high magnetic coupling factor is desired [1].

Capacitor selection for SEPIC converters is explained in [8]. Coupling capacitor provides isolation and also protection between input and output. The coupling capacitor should be chosen to handle the rms current flowing over the top depending on the output

power. In SEPIC converters, load current is supplied by the output capacitor, therefore large ripple currents occur on the capacitor. Thus, output capacitor is chosen to withstand the high rms current capacity [8].

SEPIC converter is analyzed with coupled and uncoupled inductors in [9]. While doing this analysis, State-Space Averaged (SSA) method is used and simulated with different input voltages. Thus, results showed the effects of coupled and uncoupled inductors under different input variations for SEPIC converters.

In [10], stability region of Peak Current Controlled (PCC) SEPIC converters is determined with ratio of the input and output inductance. This stability region is achieved by using ac models of SEPIC converter and its controller. In [11] and [12], AC models are used to achieve that. There are some specific studies about stability in the literature for Peak Current Controlled SEPIC converters. In [13], it is observed that when a voltage applied to the input below a certain threshold value, instability occurs. In that case, stability is achieved once the input inductance is decreased, or output voltage value is increased.

In [10] and [14], stability issues for Peak Current Controlled SEPIC converter are discussed. In [14], RC damping circuit parallel with coupling capacitor is introduced to specify the stability region. The role of RC damping section is to prevent the oscillations on the voltage of the coupling capacitor. To increase damping factor, a large coupling capacitor is used however as indicated in [10] that when large capacitor is used, the ratio of output and input inductances must be greater than ratio of output voltage and input voltage which is called conversation ratio. This is necessary to guarantee the stability.

SEPIC converter design considering output voltage ripple is explained in [15]. According to that design, minimum size of capacitor and inductance are obtained achieve minimum output voltage ripple. Peak switching current has also been calculated with

respect to continuous current mode (CCM) and discontinuous current mode (DCM) [15]. Acceptable ripple level on output voltage is achieved in [16], [17]. In [18], buck converter is examined for output voltage ripple in two modes. One of them is continuous conduction mode (CCM), the other one is discontinuous conduction mode (DCM) by using critical inductance. Lowest output voltage level is reached with using minimum inductance under CCM and DCM. Input voltage range is 21–27 V, output voltage is 18 V with 52 kHz switching frequency.

Single ended primary inductor (SEPIC) converter is designed in [19] and [20], for the purpose of decreasing switching losses using soft switching method. In addition to coupled inductor, an auxiliary inductor has been used and soft switching is achieved. Thus, reduced switching losses, voltage stresses and high efficiency are obtained. Proposed prototype of these converters are 80 W and 65 W, respectively [19] and [20].

In [21], a new topology for SEPIC converter to decrease the output voltage ripple (OVR) in continuous and discontinuous conduction mode has been proposed. An auxiliary capacitor, inductor and a switch have been added to avoid output voltage ripple. Also, with these extra components, zero voltage switching is obtained. When compared to classical single ended primary converter, the new topology has a disadvantage that the stress on the switch is high.

There are a lot of applications of SEPIC converters. Such as vehicles, aircraft, photovoltaic systems, electric motors, LED lights, etc. LED (Light emitting diode) lighting applications are the most popular because of their efficiency, compact structure, easy to change their color and long life. In [22], a new kind of LED driver is proposed using SEPIC converter. That modified topology uses lower voltage capability switches and result is comparable with other buck-boost converters.

Light emitting diodes (LEDs) are replaced with classical bulbs to reduce energy consumption in lighting applications. Advantages of LEDs are explained in [23]. Light

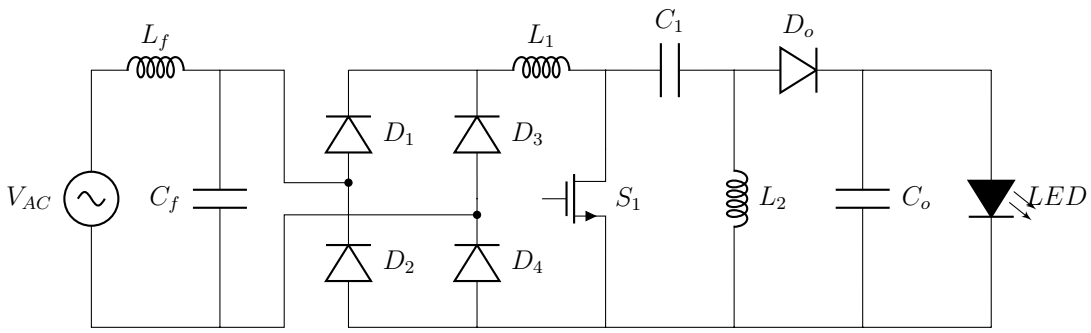

Fig. 1.1. The modified SEPIC converter in [22].

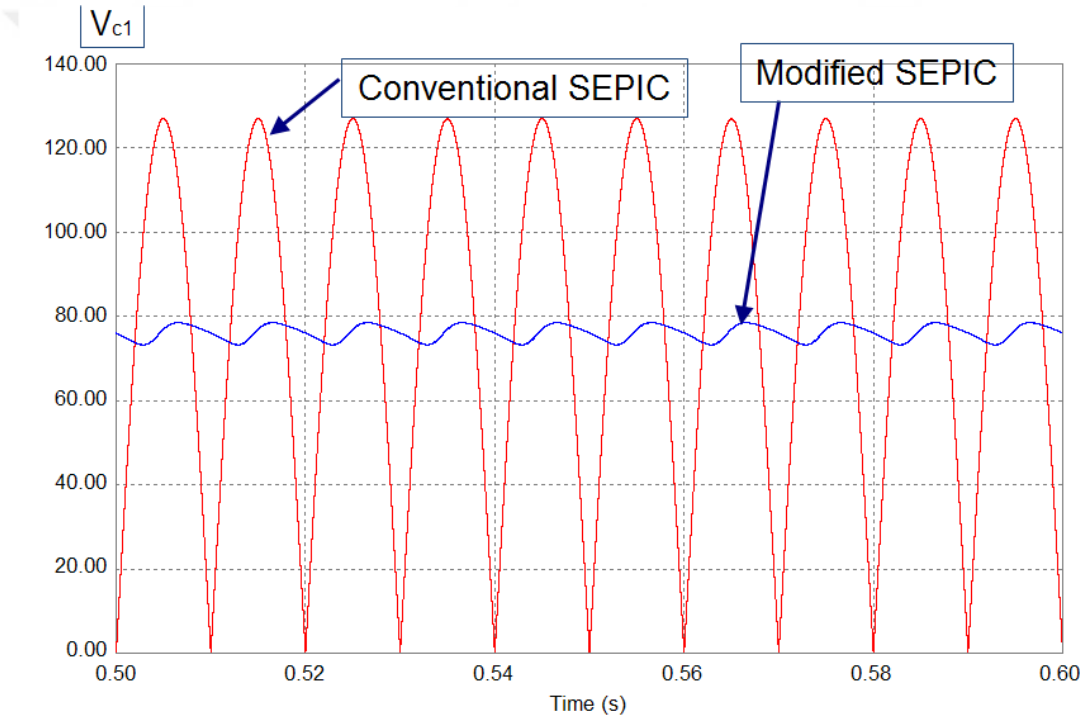

Fig. 1.2. Comparison results [22].

emitting diodes (LEDs) are supplied by DC voltage that can be achieved with using AC-DC converter (rectifier) or DC-DC converters (SEPIC, Cuk, Zeta). They are called driver for LED applications and they have wide range of output voltage [22].

In [24], a SEPIC converter is proposed with high power factor ratio and adjustable brightness. That converter is designed for high brightness applications and it is also

proper for offline light emitting diodes (LEDs) applications. Controlling of the brightness is achieved by using a current feedback loop. In that loop, 250 kHz PWM (pulse width modulation) signal is generated by using saw-tooth carrier signal and input voltage has not been needed to be measured. Thus, the circuit has a simple feedback loop. Consequently, high power factor is achieved. The efficiency is higher than 75%.

Automobile LED applications of SEPIC converter is proposed in [25]. Proportional-integral (PI) regulator has been used for controlling the converter. Classical drivers (buck-boost converters) are not a good choice for this type of applications [25]. LEDs are replaced with other lamps in automotive industry because of efficiency [26], [27], [28], [29].

Another vehicle light emitting diode (LED) application is proposed in [30]. In that paper, a hybrid control scheme is used for dimming. In this way, complexity in wiring of the vehicle is reduced, thus cost advantage is achieved. In [30], a proposed configuration is presented to offer high efficiency and makes sure that all LEDs have equal brightness.

Single ended primary inductor (SEPIC) converters has been widely used for vehicle applications. In [31], battery management application using SEPIC converter for electric vehicles are introduced. An ultra-capacitor is used to protect battery from peak currents. The purpose of using SEPIC converter in that study is to provide an isolation between capacitor and battery, therefore SEPIC converter acts as an interface between them. Because of developments on acceleration and driving performance by using ultra capacitor, more utilization from the battery is achieved. In that case, performance of vehicle is positively affected by using SEPIC converter.

In [32], digitally controlled SEPIC converter is designed using PI controller and PFC. The PFC is used to reduce THD and improve efficiency. Some other methods in literature using PFC are given in [32] and [33]. The gains of PI controller are tuned using

(GA) in [32].

One of the most popular application of SEPIC converter is photovoltaic (PV) systems. In [34], a system is designed which includes photovoltaic lights. The control is achieved with a microcontroller. Maximum power point tracking (MPPT) algorithm is used in that microcontroller to charge the battery. The system is more efficient with MPPT algorithm. In an attempt to control the current of LEDs, PI regulator algorithm is used to adjust the brightness of LEDs.

In [35], other different application for photovoltaic systems have been proposed. Proposed SEPIC converter has an advantage when compared to the other classical SEPIC converters that have high output conversation ratio. Classical SEPIC converter can increase output voltage five times with respect to the input voltage, however the proposed converter given in [35] increases the voltage ten times. It is achieved by adding diode and a capacitor. The proposed converter uses PI controller.

SEPIC converters are also used in brushless dc motor (BLDC) applications [36]. BLDC motors have widely used because of their high flux density, high torque capability and efficiency when compared to the other motor types. This feature of BLDC motor is suitable for home applications. Because of reducing energy consumption, BLDC motor is used with SEPIC converter in [36].

Photovoltaic systems need DC-DC converter to regulate and keep constant voltage output of solar panels. In [37], a SEPIC converter for street lights feed by solar panels is designed. SEPIC converters are widely used to control street lights because of their advantages [38], [39], [40].

Robust dynamic performance in SEPIC converter using proportional-integral-derivative (PID) controller is achieved in [41]. The performance of the converter is tested with applying various input voltage and load conditions. Reasonable results of steady state

error, output voltage ripple and overshoot are obtained. Reference voltage is equal to output voltage in the proposed converter. It is shown that the dynamic performance of the controller is excellent.

1.3. Outline of Thesis

The thesis is organized as follows. In Chapter 2, the design of SEPIC converter is described and the design specifications of SEPIC have been given. Some of the design parameters are achieved by using approximations. In Chapter 3, MATLAB/Simulink® and Ansys SiWave™ simulations have been presented. Closed loop simulation of SEPIC has been proposed by using MATLAB/Simulink® and electromagnetic fields simulations have been done by using Ansys SiWave™. In Chapter 4, experimental results of SEPIC have been validated with simulations under various load conditions. Finally, the conclusion is given in Chapter 5.

II. DESIGN OF SEPIC CONVERTER

SEPIC (single-ended primary-inductor) converter is primarily used where input voltage above or below the output voltage. Classical buck-boost converter has an output voltage that can be up above or below the input voltage, but it has negative polarity. The SEPIC converter overcomes that problem so input voltage polarity is the same as the output voltage polarity. In this way, the ground line in the circuit is used for both input and output. Also, the voltage differences on the circuit are at the same polarity such as the sum of the input voltage and output voltage does not rise to high values.

2.1. Switching Characteristic of Inductance

The basic switching circuit for inductance is shown in Fig. 2.1. Only one of the switches S_1 and S_2 is open at the same time.the switch S_1 is open, there is a voltage drop V_1 on the inductance, while the S_2 switch is closed, there is a negative voltage drop V_2 on the inductance. As the voltage applied to the inductor is constant, the inductance current will increase or decrease with V/L ratio. Switch change, inductance voltage and current changes are shown in Fig. 2.2.

When the voltage drop on the switch has been neglected with switch S_1 off, there is a

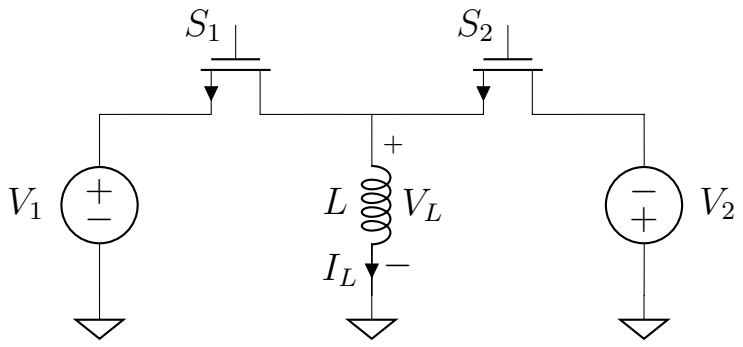

Fig. 2.1. Basic switching circuit for inductance.

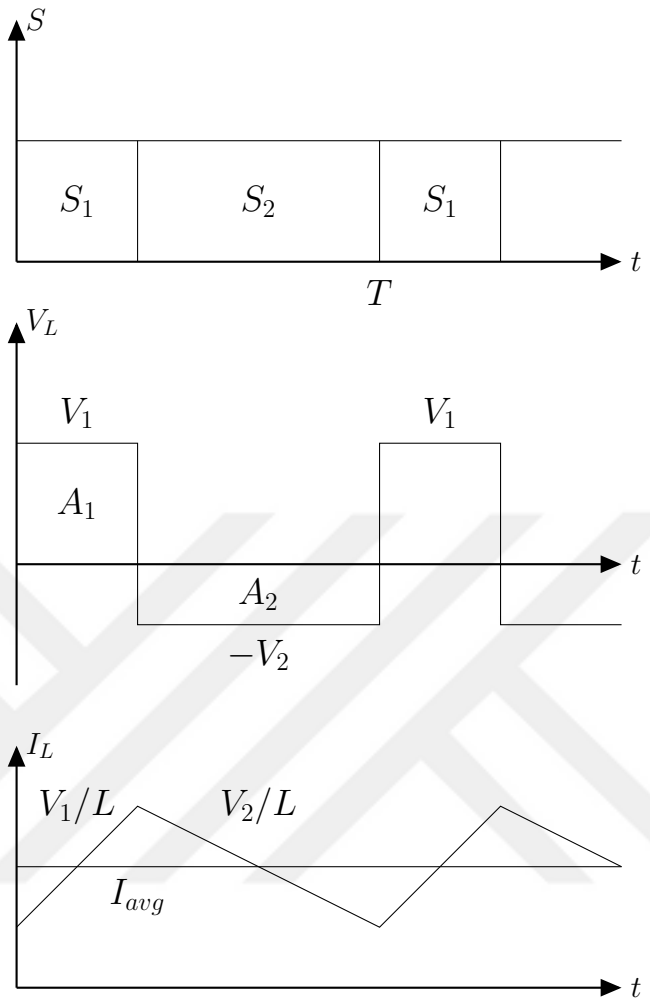

Fig. 2.2. Inductance current-voltage changes with switches.

V_1 voltage on the inductance. In this case, the inductance current is

$$i = \frac{1}{L} \int v dt \tag{2.1}$$

increased by the slope of V_1/L. When switch S_2 is switched off, the voltage $-V_2$ is applied to the inductor. In this case, the inductance current decreases with $-V_2/L$. The average current must be constant so that the current of the inductance does not increase to infinity over time. In this case, the areas indicated by A_1 and A_1 in the voltage curve must be equal to each other. If this equality is not ensured, energy will accumulate in the inductance and the average current will change over time. In order to prevent this,

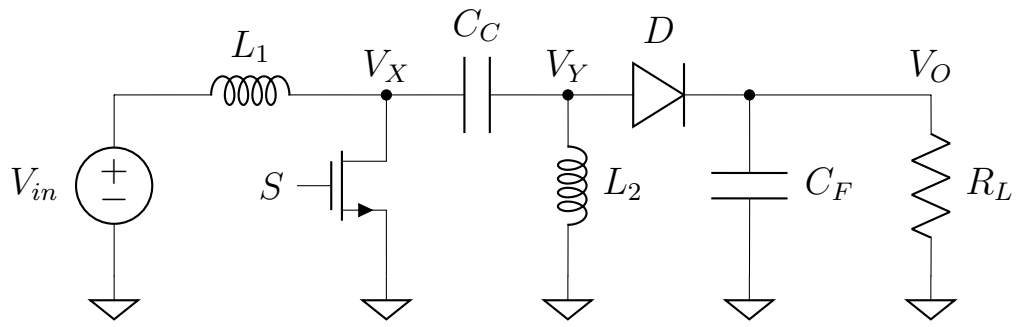

Fig. 2.3. SEPIC converter circuit diagram.

the control algorithms used work to make the switching times the average inductance voltage equal to zero. The switching period is T, as shown in Fig. 2.2

2.2. SEPIC

As can be seen from Fig. 2.3, the input and output of the SEPIC converter is isolated by C_C coupling capacity. The C_F capacity is used as a filter and reduces the oscillations on the output. R is the load resistance. The L_1 inductance at the input acts as a filter and reduces the input oscillations. L_2, the node between the diode and C_C to the ground level by pulling the diode is not in the conduction of this node determines the voltage.

It is necessary to make some assumptions when analyzing SEPIC. The first assumption is the that the C_C and C_F capacities are large enough and the voltage fluctuation is small. Another assumption is that there is no voltage drop on the diode. It is assumed that the resistance of the inductors and the transistor used as a switch is too small to be ignored from the calculations. The last assumption is that the currents of inductances do not drop to zero at every cycle. This type of operation is called continuous conduction mode. If the inductance current falls to zero during the cycle, it is called the discontinuous conduction mode.

When the switch remains in the short-circuit mode, it is called t_{on} When the switch

remains in the open-circuit mode, it called t_{off}. Considering that the total time is T, the following equations have been written.

$$D_{on} = \frac{t_{on}}{T} = \frac{t_{on}}{t_{on} + t_{off}} = 1 - D_{off} \tag{2.2}$$

$$D_{off} = \frac{t_{off}}{T} = \frac{t_{off}}{t_{on} + t_{off}} = 1 - D_{on} \tag{2.3}$$

In general, D_{on} is briefly referred to as D.

Firstly, the voltage drop on C_C capacity must be achieved to specify the voltage relationship between input and output. At the steady state, the average current will be DC. Average current change will be zero over time. In this case, the average voltage drop on the inductances L_1 and L_2 will be zero. The average value of the V_y node will be at the ground potential. Because one end of the L_1 inductance is connected to V_{in} and the average voltage drop is zero, the V_x node will also have a value of V_{in}. In this case, the average voltage of C_C capacity will be V_{in}. The end of the C_C is connected to L_1 and the other end will be up to V_{in}.

Although the average value of V_x is V_{in}, the voltage in V_x will change over time due to the switch S being turned on and off. When the S switch is in conduction, the V_x node will be on the ground. In this case, as shown in Fig. 2.4, the value of V_x is 0 V when the switch S is on. Since the other end of the L_1 inductance is connected to V_{in}, the current of L_1 inductance will increase with V_{in}/L_1. The current will flow from the input to the V_x node. When the switch S switches from the off to the on position, the voltage of the V_x node will be the sum of the voltage drop on the output voltage V_O, diode voltage and C_C capacity. If the voltage drop on the diode is accepted as zero, the voltage of the V_x node will be V_{in} + V_O. In this case, the voltage drop above the L_1 inductance will be equal to $-V_O$ and the current L_1 will be $-V_O/L_1$. Since the average voltage on the inductance L_1 must be zero, the integral of the voltage of L_1 in Fig. 2.4 must be zero in a period. In this case, the relation between input and output is written as follows in

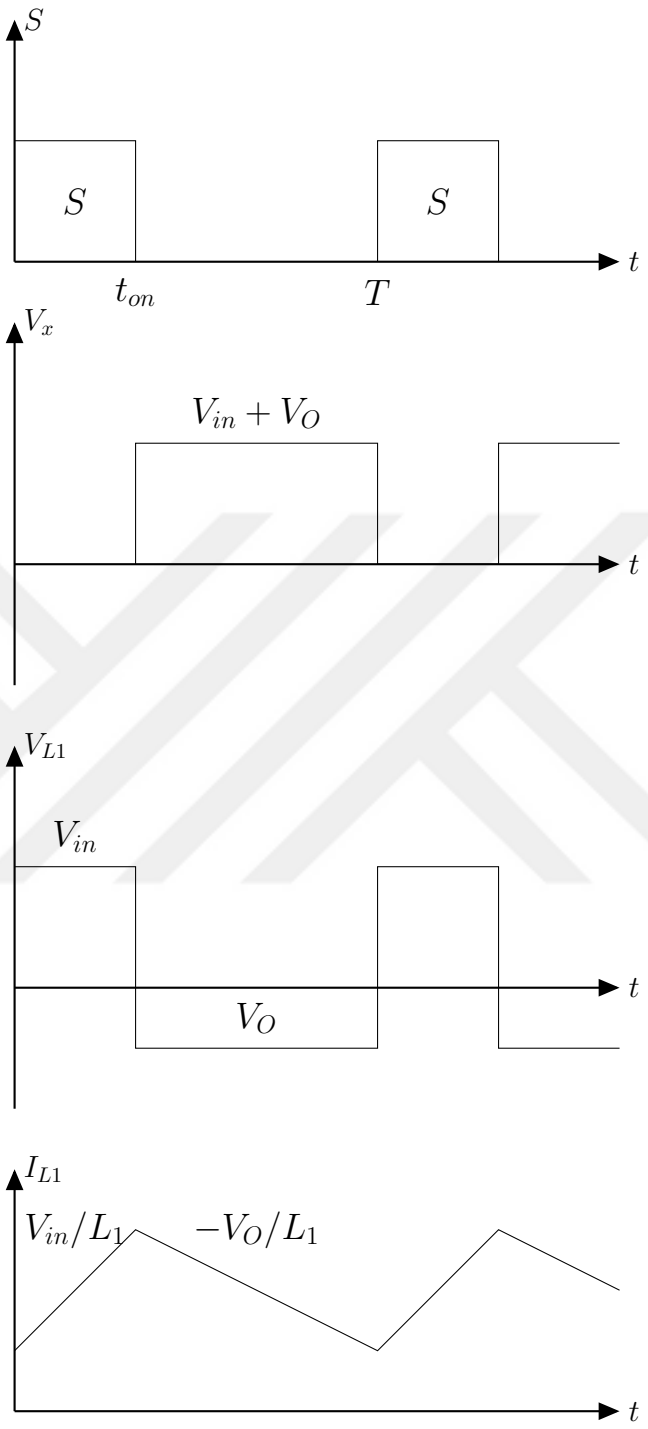

Fig. 2.4. Voltage changing of V_x and current changing of L_1.

terms of open-close ratio of switch S.

$$V_{in}.t_{on} - V_O.t_{off} = 0 \tag{2.4}$$

$$V_{in}\frac{t_{on}}{T} - V_O\frac{t_{off}}{T} = 0 \tag{2.5}$$

$$V_{in}.D_{on} - V_O.D_{off} = 0 \tag{2.6}$$

$$\frac{V_O}{V_{in}} = \frac{D_{on}}{D_{off}} \tag{2.7}$$

$$D_{on} = \frac{V_O}{V_{in} + V_O} \tag{2.8}$$

As seen in (2.4)–(2.8), the relationship between input and output voltages is determined by adjusting the duty cycle ratios. In this way, the value of the output voltage may be higher, lower or equal than the value of the input voltage.

The average current flowing through the C_C capacity will be zero, so the DC current will be zero. Otherwise, the load on the C_C capacity will accumulate and the voltage of the C_C capacity will increase or decrease. The DC current will not flow through the C_C. The voltage over the C_C will remain constant. In this case the output current will be provided by L_2.

As seen from Fig. 2.5, the voltage drop on the L_2 inductance will be equal to the V_y node. When the S switch is in conduction, one end of the C_C capacity will be at ground potential, and the other end will be at $-V_{in}$. When the switch changes from off to on position, the voltage of the V_y node will be V_O. If the current of the L_2 inductance is assumed to flow from V_y to the node, the current at switch S is in $-V_{in}/L_2$, while the switch is in the open circuit, it is V_O/L_2. The average current of L_2 will also be equal to the output current. Because the average voltage drop on L_2 is zero, the integral of V_{L_1} in a period will be zero. Since the output current will flow through R_L, the following relationship has been obtained between the average current and the output voltage.

$$I_{avg} = I_O = \frac{V_O}{R_L} \tag{2.9}$$

The principle of energy conservation between input and output can be expressed in

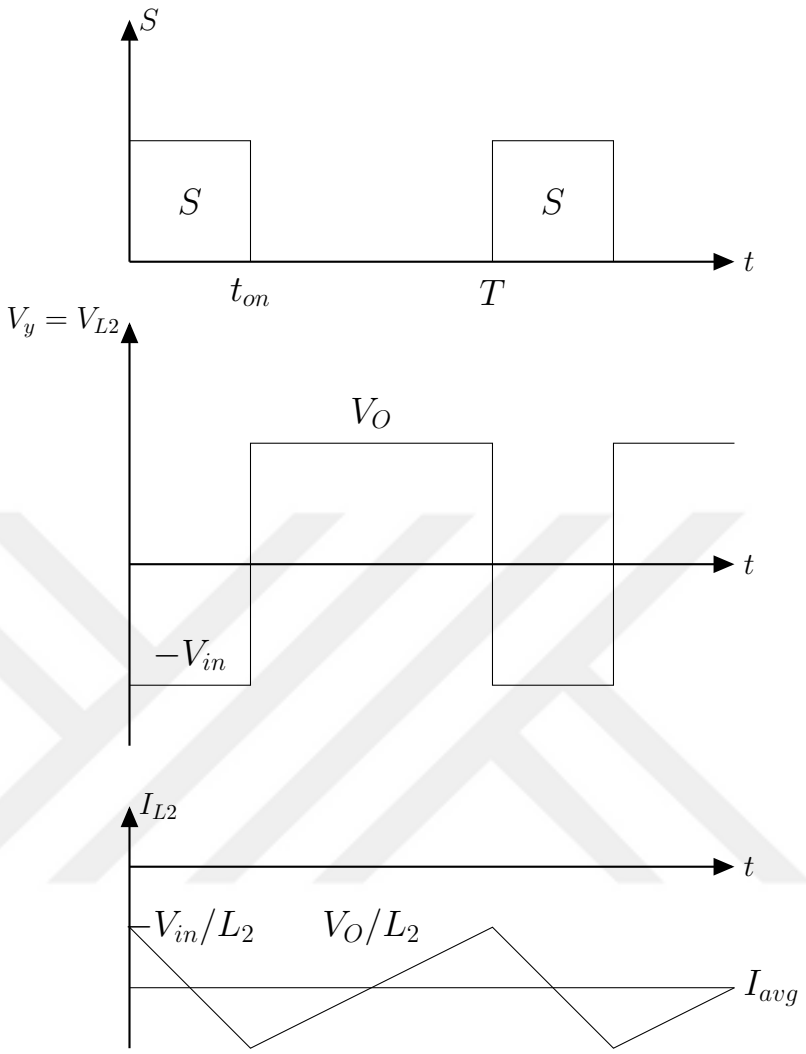

Fig. 2.5. Voltage changing of V_y and current changing of L_2.

(2.10). The input current is also equal to the current of the inductance L_1. As seen from the relationship between the input and output currents, the input current may be higher, lower, or the same as the output current.

$$I_{in}.V_{in} = I_{L_1,avg}.V_{in} = I_O.V_O \tag{2.10}$$

$$I_{L_1,avg} = I_O.\frac{V_O}{V_{in}} = I_O.\frac{D_{on}}{D_{off}} \tag{2.11}$$

The voltage drop on the inductances L_1 and L_2 varies between V_{in} and V_O. In this case,

as can be seen from Fig. 2.6. L_1 and L_2 can be implemented on the same core. Thus, the space on the PCB can be reduced. L_1 and L_2 separate inductances will flow energy from the input to the output through C_C. However, when L_1 and L_2 are performed on the same core, the efficiency will increase as a way through which the energy will flow from the input to the output. When L_1 and L_2 are performed on the same core, in order to simplify the design and allow the currents of L_1 and L_2 to be the same, the values of the inductances L_1 and L_2 are selected the same.

2.3. Stress Calculations of Components

For selecting the circuit elements to be used in SEPIC, the voltage drops on the elements and the currents flowing through them must be known. The maximum value of the drain to source voltage of the switch S is $V_{in} + V_O$. During the on-off time of switching, the drain to source voltage may exceed this value. When in conduction, the current flow will be the sum of the currents of L_1 and L_2. In this case, the current equation will be written as follows

$$I_s = I_{L_1} + I_{L_2} = I_O.\frac{D_{on}}{D_{off}} + I_O = \frac{I_O}{D_{off}} \tag{2.12}$$

Maximum voltage drop is $V_{in} + V_O$ on the diode at reverse biased. At forward biased, current flow on the diode is equal to output current.

Since the voltage on the C_C capacity is V_{in}, the selected capacity must be based on at least V_{in} voltage. When the switch S is in conduction, the current of the inductance L_2 will flow through the C_C. When the switch S is not in conduction inductance L_1 current will flow through C_C. In this case, the RMS current of the C_C capacity can be written as the sum of the RMS of both currents as follows

$$I_{C_c} = \sqrt{I_{L_2}^2.D_{on} + I_{L_1}^2.D_{off}} = \sqrt{I_O^2.D_{on} + (I_O.\frac{D_{on}}{D_{off}})^2.D_{off}} = I_O.\sqrt{\frac{D_{on}}{D_{off}}} \tag{2.13}$$

The voltage on the inductances L_1 and L_2 are V_{in} or V_o according to the state of the switch S. While the average current of L_1 is equal to the input current, the current of L_2 is equal to the output current. However, the peak current is higher than the average current according to the duty cycle. The permissible value of the peak current depends on the value of the inductance and should be smaller than the saturation current of the selected inductance.

2.4. Design Calculations of SEPIC

The input voltage of the proposed SEPIC converter is between 16 V and 36 V and the output voltage is regulated to 24 V or 20 V depending on the dimming request. Assuming that the voltage drop on the diode is 1 V, the minimum and maximum values of the duty cycle are defined as

$$D_{on,min} = \frac{V_{O,min} + V_D}{V_{in,min} + V_{O,max} + V_D} = \frac{20\ V + 1\ V}{36\ V + 20\ V + 1\ V} = 0.37 \tag{2.14}$$

$$D_{on,max} = \frac{V_{O,max} + V_D}{V_{in,min} + V_{O,max} + V_D} = \frac{24\ V + 1\ V}{16\ V + 24\ V + 1\ V} = 0.61 \tag{2.15}$$

The value of the inductance has been selected from the peak to peak current change to be 40% of the highest current. Since the highest input current occurs at the lowest input voltage, the change from peak to peak current can be written as follows

$$\Delta I_L = I_{in}.40\% = I_O.\frac{V_O}{V_{in,min}}.40\% = 10\ A.\frac{24\ V}{16\ V}.40\% = 6\ A \tag{2.16}$$

In that case, if the switching frequency is selected as 200 kHz, the values of the inductances L_1 and L_2 has been calculated as follows

$$L_1 = L_2 = L = \frac{V_{in,min}}{\Delta I_L.f_{sw}}.D_{on,max} = \frac{16\ V}{6\ A.200\ kHz}.0.61 = 8.1\ \mu H \tag{2.17}$$

where f_{sw} is the switching frequency. The peak currents of the inductances must be selected lower than the saturation current. The peak currents of L_1 and L_2 are calculated

as follows

$$I_{L_1}(peak) = I_O.\frac{V_O + V_D}{V_{in,min}}.(1 + \frac{40\%}{2}) = 10\ A.\frac{24\ V + 1\ V}{16\ V}.(1 + \frac{40\%}{2}) = 18.75\ A \tag{2.18}$$

$$I_{L2}(peak) = I_o.(1 + \frac{40\%}{2}) = 10\ A.(1 + \frac{40\%}{2}) = 12\ A \tag{2.19}$$

If L_1 and L_2 are realized on the same core, the L_1 and L_2 will reduce to half of the above calculated value due to the coupled inductance. In this case, the minimum inductance value is 4.05 μH. However, the realized inductance value is 4.7 μH due to the extra turn in order to guarantee the minimum inductance value.

The drain to source voltage of the MOSFET will be at least the sum of the maximum values of the input voltage and output voltage. Assuming that the voltage on the switch is increased by up to 50% at the transition states, required minimum voltage for the MOSFET $V_{DS,min}$ is selected as follows

$$V_{DS,min} = (V_{in,max} + V_{O,max}).(1 + 50\%) = (36\ V + 24\ V).(1 + 50\%) = 90\ V \tag{2.20}$$

The current flowing from MOSFET in worst case scenario is calculated as follows

$$I_S = \frac{I_O}{D_{off}} = \frac{I_O}{1 - D_{on,max}} = \frac{10\ A}{1 - 0.61} = 25.6\ A \tag{2.21}$$

Maximum voltage drop on the diode is 60 V. The output current will flow through the diode and a 50% margin is added on it. It should be able to carry a current of 15 A. The power consumption of the diode will be the product of the voltage drop and its current when it is in conduction. If the voltage drop on the diode is 1 V, then the power consumption of the diode will be 10 W for 10 A output current.

Voltage drop of the C_C capacitor is the same as the input voltage. When the values of the capacitor is reduced at high voltages, then the voltage value of the C_C capacitor is selected approximately three times higher than the input voltage. In that case, the C_C

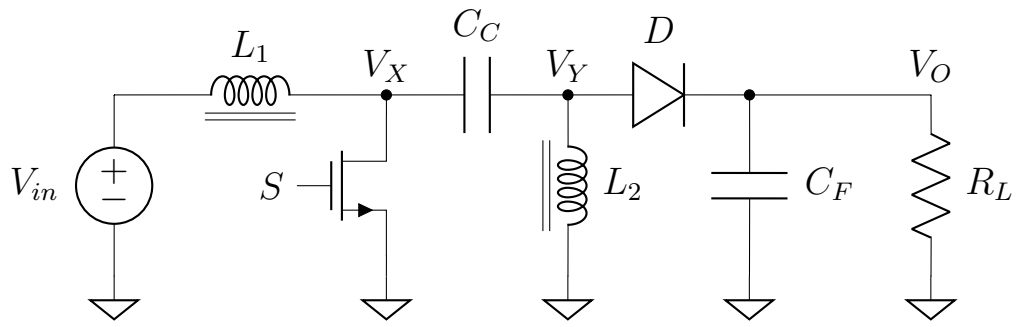

Fig. 2.6. SEPIC circuit on same core.

capacity should be at least 100 V. The RMS current of the C_C capacitor is calculated as follows

$$I_{C_C} = I_O . \sqrt{\frac{D_{on,max}}{1 - D_{on,max}}} = 10\ A . \sqrt{\frac{0.61}{1 - 0.61}} = 12.5\ A \tag{2.22}$$

Voltage ripple on the C_C capacitor ΔV_{C_C} is calculated using the following formula

$$\Delta V_{C_C} = \frac{I_{C_C} . T}{C_C} = \frac{I_{C_C}}{C_{C_C} . f_{sw}} \tag{2.23}$$

Limiting the voltage ripple on the C_c capacitor to 10% of the DC voltage results in the following capacitor value

$$C_C = \frac{I_{C_C}}{\Delta V_{C_C} . f_{sw}} = \frac{12.5\ A}{3.6\ V .\ 200\ kHz} = 17\ \mu F \tag{2.24}$$

In order to guarantee low output impedance up to 400 MHz, the C_F capacitance is realized using parallel electrolytic and ceramic capacitors. The target output impedance is selected as 1 Ω up to 400 MHz. Resonance frequency of one of these capacitors is also selected as the switching frequency in order to suppress the switching noise.

2.5. Stability

To stabilize the SEPIC converter in the closed-loop configuration, the switch network is replaced by their average model [3], [8]–[10], [12]–[14]. In this model, the duty cycle

is an input and switch voltages and currents are determined according to the duty cycle value. AC analysis is possible by sweeping the modulation frequency since the duty cycle is a modulated signal given by

$$d\left(t\right) = D_0 + D_{mod} \sin \omega_{mod} t \tag{2.25}$$

The compensation network consists of two capacitance and a resistor and forms a zero and a pole. Although SEPIC converter has a fourth order transfer function, two of poles are very close at low frequency. One of these poles are canceled by the zero of the compensation network. The other poles are above the gain-bandwidth product and their effect to the stability is negligible.

The impedance of the feedback circuit is given by

$$Z_F = \frac{1}{s\left(C_{FB1} + C_{FB2}\right)} \cdot \frac{1 + sC_{FB2}R_{FB2}}{s\left(\frac{C_{FB1}C_{FB2}}{C_{FB1}+C_{FB2}}\right)R_{FB2} + 1} \tag{2.26}$$

in which the first part is the integrator capacitance and is multiplied by opamp gain due to the Miller effect. Therefore, this capacitance and the parallel combination of R_1 and R_2 determines the dominant pole.

Since the opamp gain is 74 dB (approximately 5000) and gain-bandwidth product of the loop is 2 kHz, the dominant pole frequency is 0.4 Hz. The values of R_1 and R_2 are selected as 20 kΩ and 1.1 kΩ, respectively. The sum of C_{FB1} and C_{FB2} should satisfy the following condition

$$\left(C_{FB1} + C_{FB2}\right) \geq \frac{1}{\left(20\ k\Omega || 1.1\ k\Omega\right) \cdot 5000 \cdot 2\pi 0.4} = 76\ nF \tag{2.27}$$

The second pole frequency is 100 Hz. Placing the zero exactly at this frequency makes the system behavior as a first order. In order to reduce the settling time, the zero is placed at 200 Hz. Since this compensation also brings a pole, the pole frequency is selected as four times of the gain-bandwidth frequency in order not to affect the phase

margin significantly. These requirements result in three equations and three unknowns as follows

$$C_{FB1} + C_{FB2} = 76\ nF \tag{2.28}$$

$$R_{FB2}C_{FB2} = \frac{1}{2\pi 200\ Hz} \tag{2.29}$$

$$\frac{C_{FB1}C_{FB2}}{C_{FB1} + C_{FB2}}R_{FB2} = \frac{1}{2\pi 8\ kHz} \tag{2.30}$$

The result of these equations are rounded to standard capacitance and resistor values. Therefore, C_{FB1} is 82 nF, C_{FB2} is 2.2 nF, and R_{FB2} is 10 $k\Omega$.

2.6. Snubber Circuit

SEPIC converter shown in Fig. 2.6 has two switching elements, one is the MOSFET and the other is the diode. During their on and off transients, inductances and their parasitic capacitances resonate. This unwanted resonances damped using an RC snubber network. The value of L_1 inductance is 4.7 μH and it is higher than the parasitic inductance of PCB. The drain-source parasitic capacitance of the switch is 680 pF. Parasitic capacitances are assumed to be twice the switch capacitance (1.36 nF). The resonance frequency of the snubber circuit is calculated as

$$f_{ring} = \frac{1}{2\pi\sqrt{C_P L}} = \frac{1}{2\pi\sqrt{2.04\ nF \cdot 4.7\ \mu H}} \approx 1.63\ MHz \tag{2.31}$$

To critically damp the snubber circuit ζ should be one. Therefore, the resistance of the snubber circuit is calculated as follows

$$R_S = \frac{1}{2\zeta}\sqrt{\frac{L}{C}} = \frac{1}{2 \cdot 1}\sqrt{\frac{4.7\ \mu H}{2.04\ nF}} \approx 24\ \Omega \tag{2.32}$$

Using the resonance frequency and the snubber resistance, the snubber capacitance

value has been calculated as follows

$$C_S = \frac{1}{2\pi f_{ring} R_S} = \frac{1}{2\pi \cdot 1.63\ MHz \cdot 24\ \Omega} \approx 4.08\ nF \tag{2.33}$$

III. SIMULATION RESULTS

3.1. Stability Analysis

The phase and gain margin of the closed-loop SEPIC converter is determined using SPICE simulations. The magnitude and phase response of the loop for 16 V, 24 V and 36 V input voltage values are shown in Fig. 3.1. Simulation results indicate minimum 56° phase margin across all input voltage conditions.

The AC analysis results are also verified with time domain simulations for 16 V, 24 V and 36 V input voltage levels. The converter is powered with zero initial conditions and no load. The output settles close to final value within 25 ms. At 50 ms, the maximum load is connected to the output. The output settles within 20 ms without ringing, as shown in Fig. 3.2.

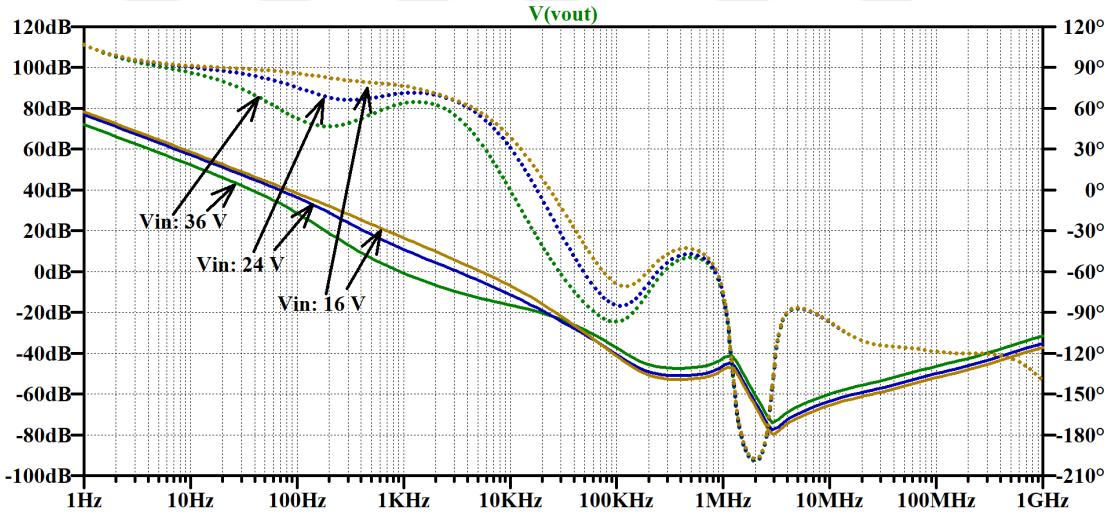

Fig. 3.1. Stability analysis of the SEPIC converter with average switch model.

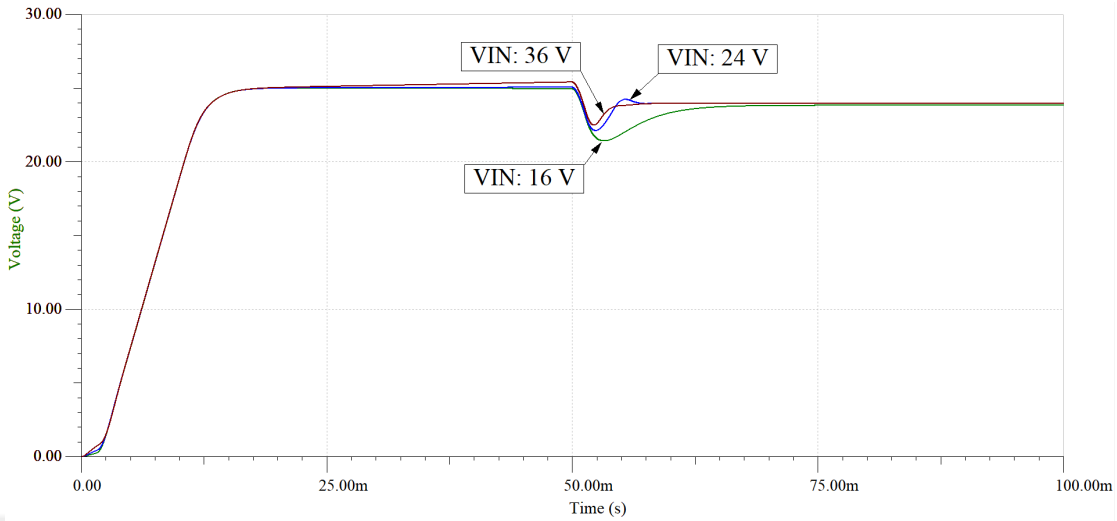

Fig. 3.2. Simulation of power-up and load regulation.

3.2. Electromagnetic Analysis

Ansys SiWave™ signal and power integrity tool is used to determine current distribution and power consumption on the PCB lines, supply resonance due to PCB parasitics, electrical and magnetic near-field and far-field performance of the SEPIC converter. The input voltage is selected as 36 V, since the phase margin is the lowest for this input voltage value. The output current is 10 A, which is the maximum output current. The capacitance models are obtained from the respective manufacturer measurement results. The inductance parasitic resistance is assumed assumed as 100 mΩ.

Top and bottom layer current distributions are shown in Figs. 3.3 and 3.4, respectively. Since the bottom layer is used as ground plane, the current density on bottom plate is lower than the current distribution on the top layer. The corners are drawn as mitered corner to achieve homogeneous current flow. This technique reduces the resistance at the corners where current flow changes direction.

The top and bottom power consumptions are shown in Figs. 3.5 and 3.6, respectively. The power consumption of top layer is higher than bottom layer. The maximum power consumption occurs close to the switch transistors due to compact layout between C_C

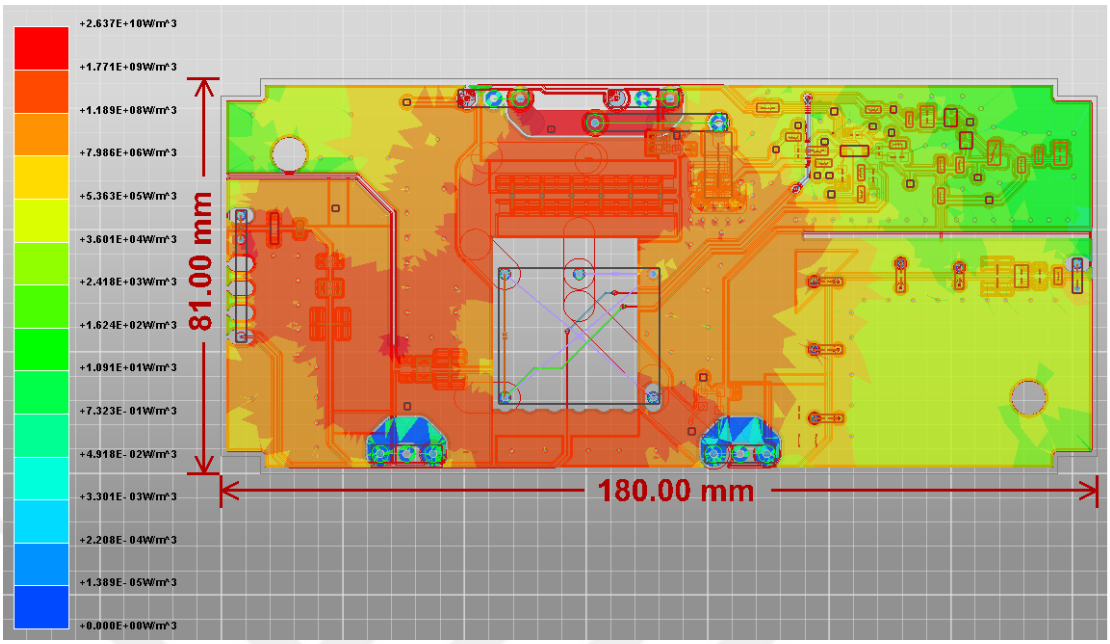

Fig. 3.3. Top layer current distribution.

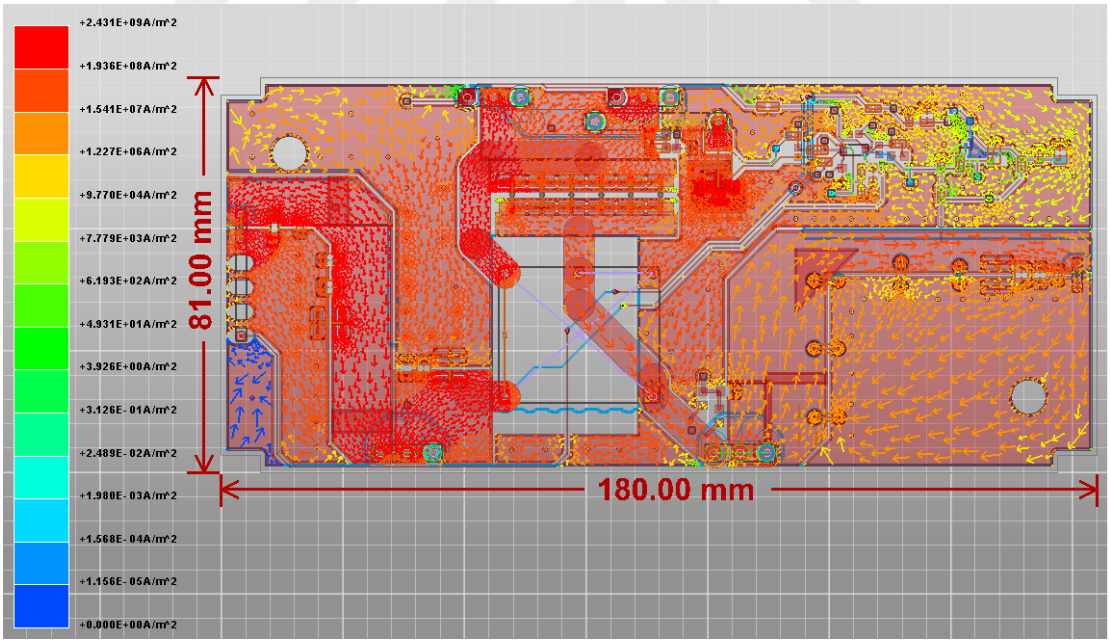

Fig. 3.4. Bottom layer current distribution.

capacitance and the MOS transistors.

Resonance analysis is performed for 10 modes with a minimum frequency of 10 MHz.

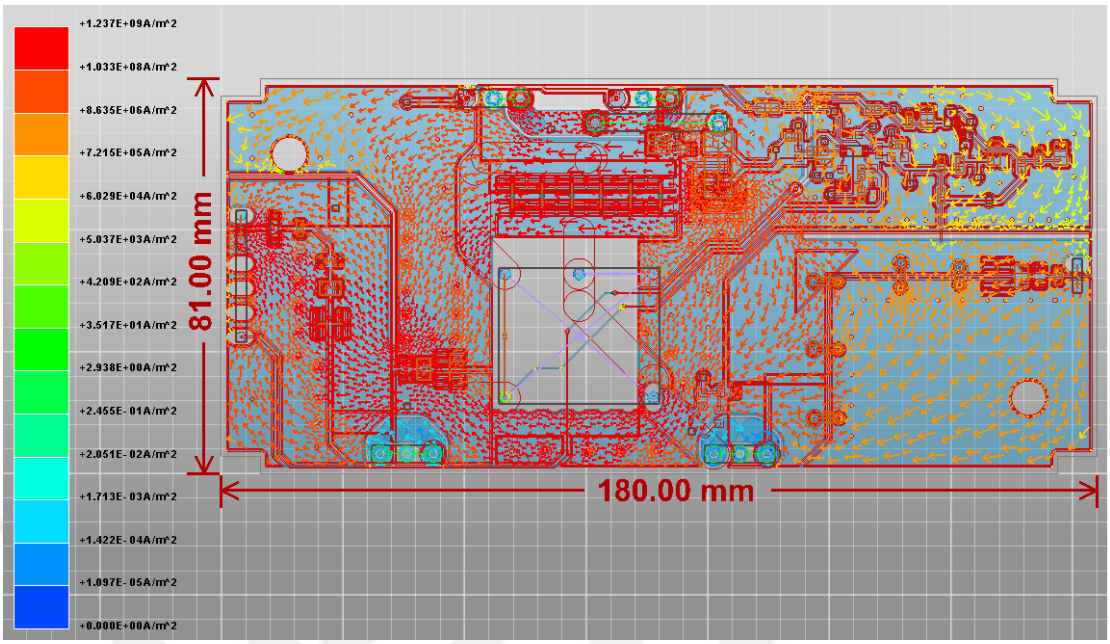

Fig. 3.5. Top layer power consumption.

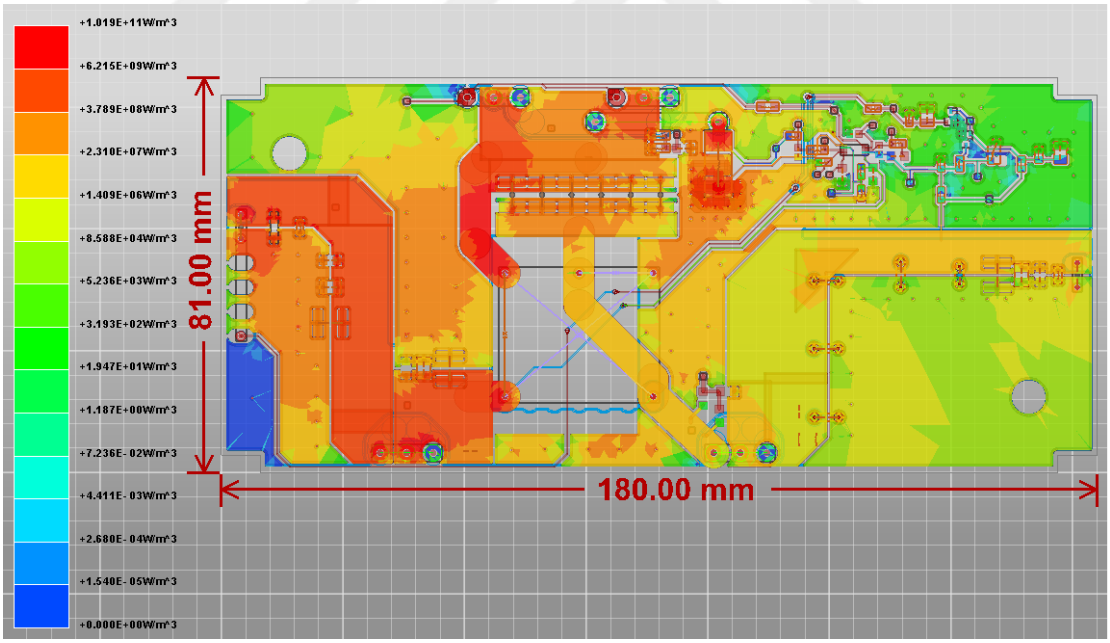

Fig. 3.6. Bottom layer power consumption.

The first mode is at 11 MHz, but it does not create a resonance on the whole PCB, as shown in Fig. 3.7.

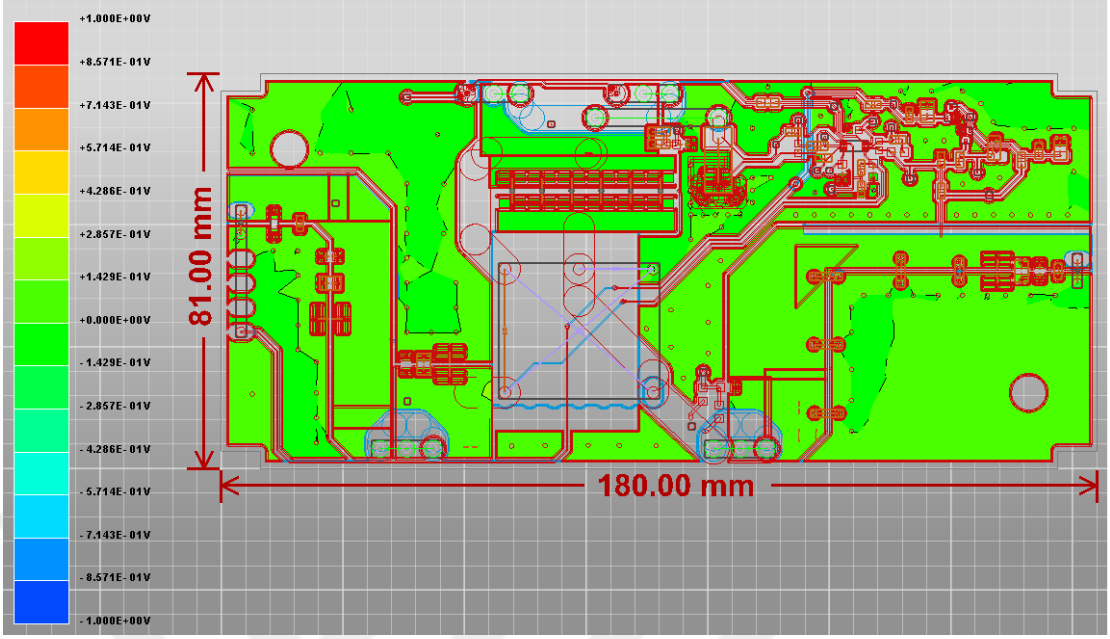

Fig. 3.7. Resonance analysis.

Near-field analysis is performed between 1 Mhz and 10 GHz. The frequency sweeps of electrical and magnetic fields are shown in Figs. 3.8 and 3.9, respectively. The worst case electrical field distribution occurs at around 2.4 GHz, as shown in Fig. 3.8. The maximum electrical field density for 2.4 GHz happens close to the diode connection. The worst case magnetic field density occurs at 1 MHz close to the inductor connection.

Far-field simulations are performed between 1 MHz and 10 GHz. Up to 250 MHz, the maximum total far-field is flat, as shown in Fig. 3.10. The first peak occurs at 372 MHz and the highest peak is at 2.45 GHz.

3.3. MATLAB/Simulink® Simulations

A digitally controlled open loop simulation model has been prepared in MATLAB/ Simulink® environment using SEPIC electrical models, as shown in Fig. 3.11. MOSFET has been used from Simulink Simscape library.

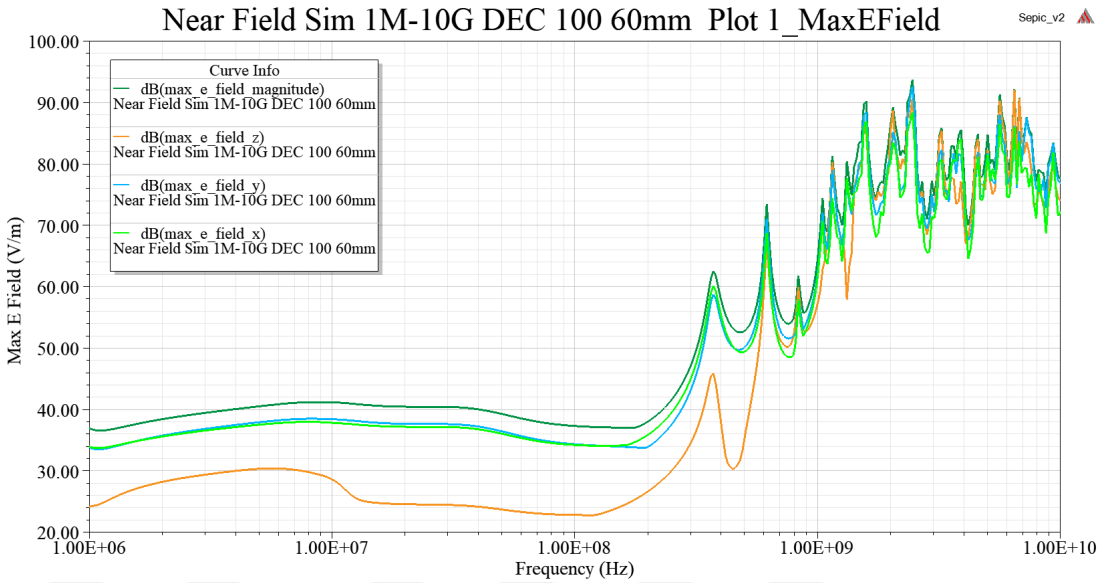

Fig. 3.8. Electrical near field response.

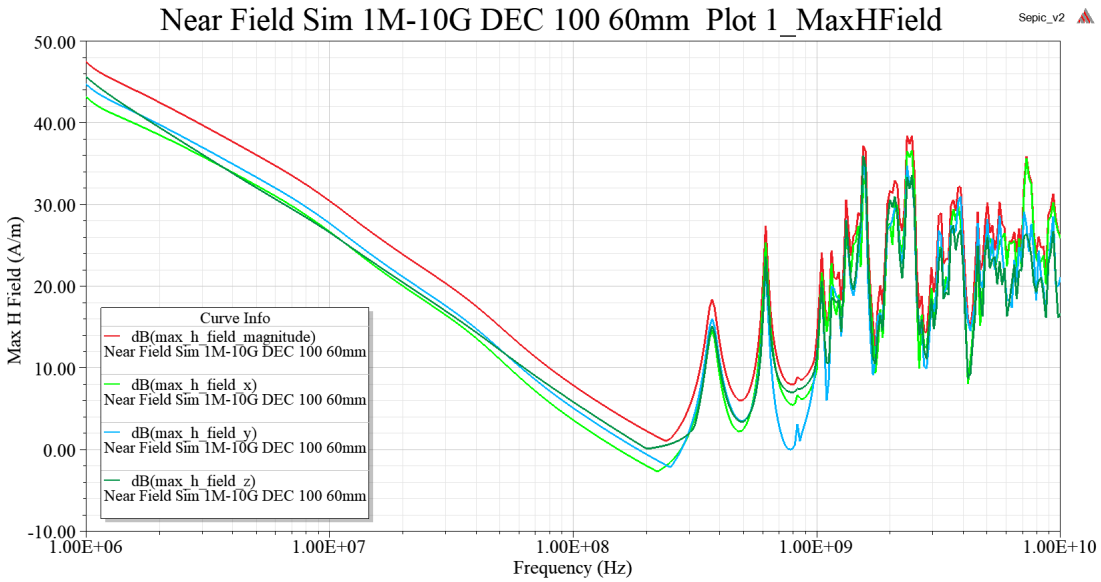

Fig. 3.9. Magnetic near field response.

Open loop MATLAB/Simulink® simulation results have been shown in Figs. 3.12, 3.13 and 3.14 under various load conditions.

In order to test the controller algorithm in SEPIC circuit, closed loop simulation model with digital control has been prepared in MATLAB/Simulink® environment by using

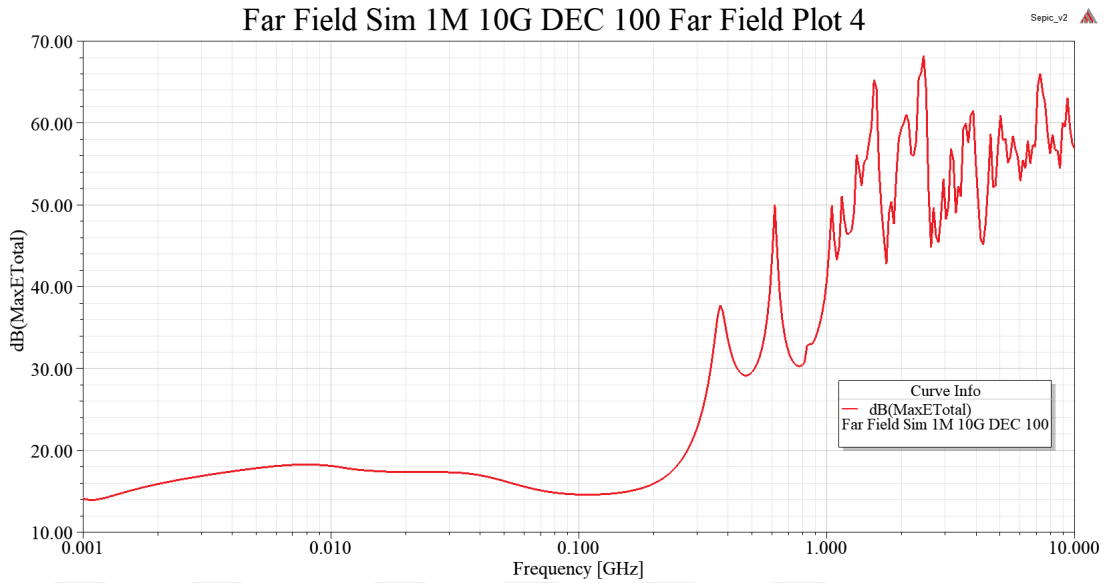

Fig. 3.10. Maximum total far-field response.

Table 3.1. Simulation Parameters

L_1	$4.7\mu H$
L_2	$4.7\mu H$
C_C	$27.2\mu F$
C_F	$2200\mu F$
D	$\%40$
R_L	2.4Ω
f_{sw}	$200kHz$

SEPIC electrical models, as shown in Fig. 3.15. Closed loop simulation results have been shown Figs. 3.17 through 3.21. Reference input voltage has been chosen as 24 V. The simulation results show that the SEPIC converter reaches the reference voltage with reasonable overshoot.

It is shown that the digitally controlled SEPIC converter has the benefits of easy to modify the control algorithm in the software as oppose to the analog designed version explained in Sections 3.1 and 3.2.

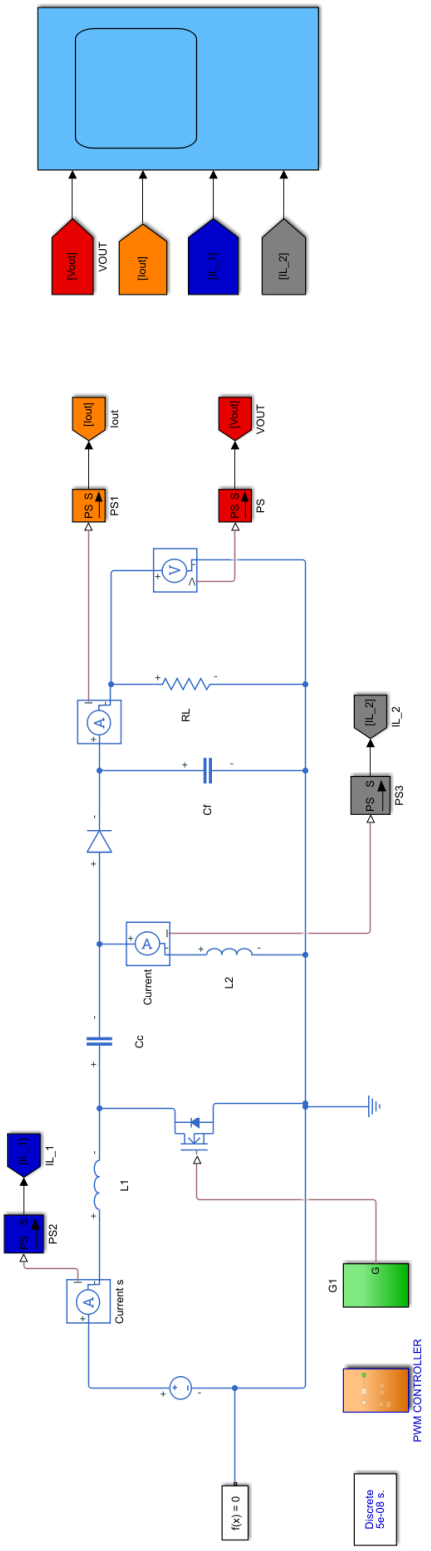

Fig. 3.11. Open Loop Simulink Simulation of SEPIC.

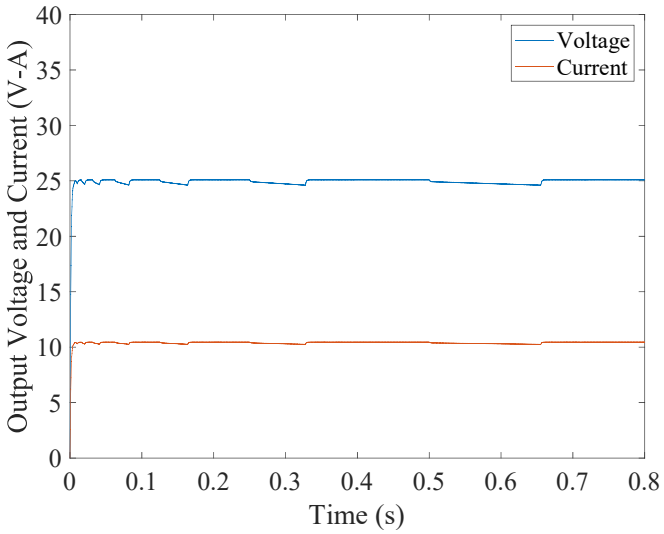

Fig. 3.12. Open loop simulation result with 2.4 Ω load.

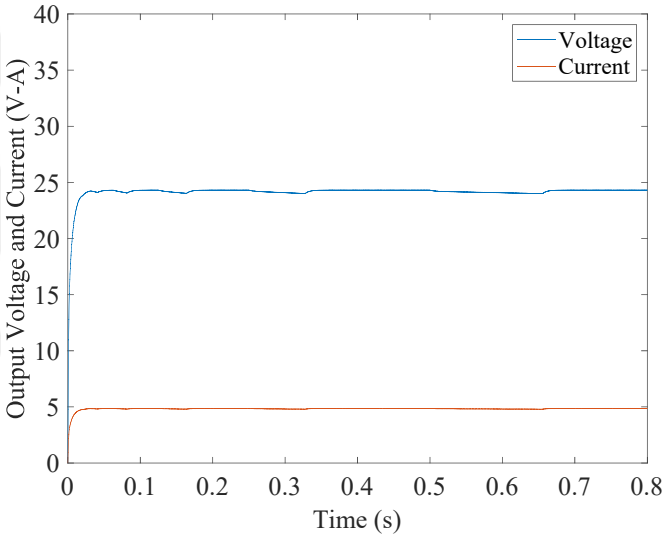

Fig. 3.13. Open loop simulation result with 5 Ω load.

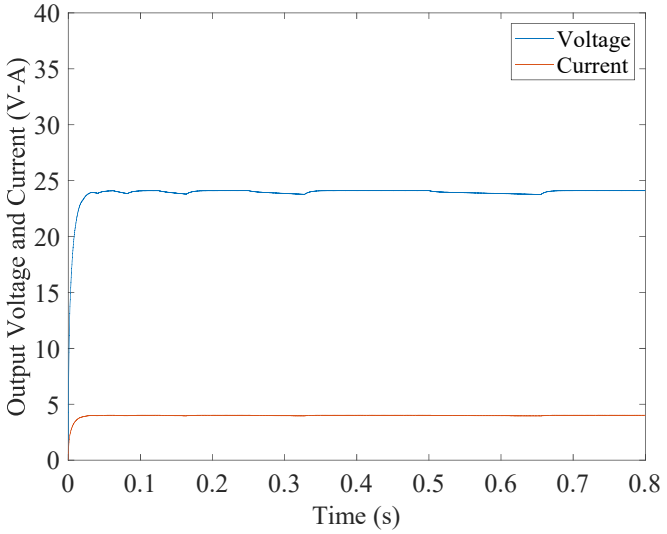

Fig. 3.14. Open loop simulation result with 6 Ω load.

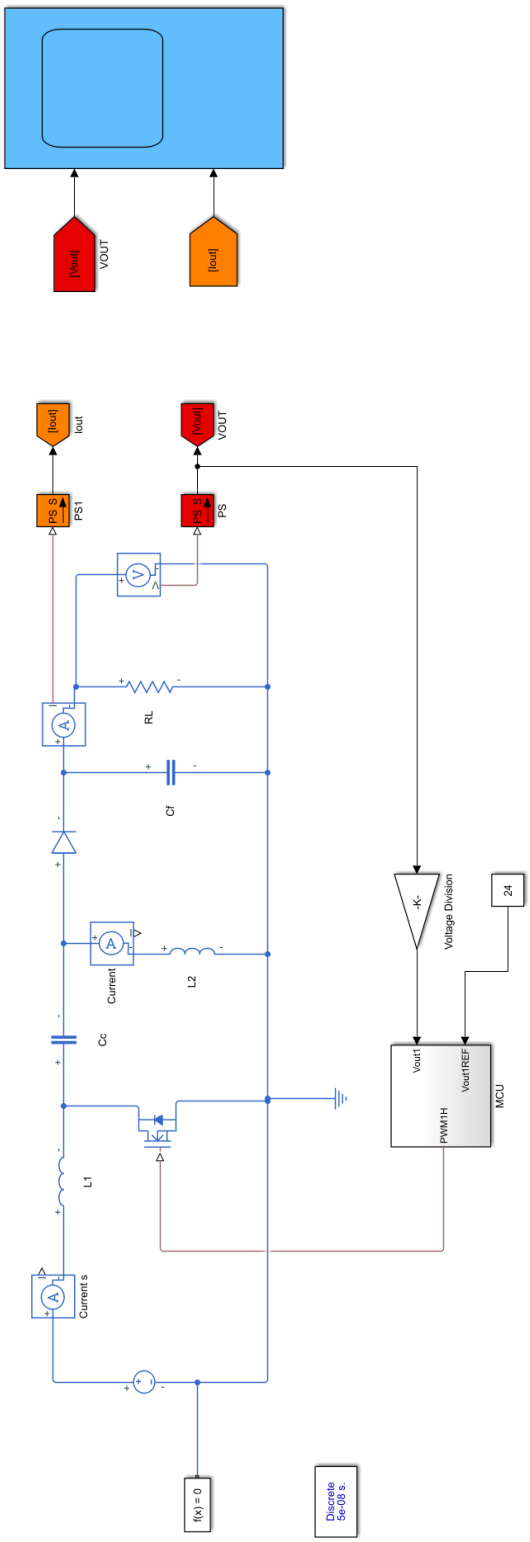

Fig. 3.15. Closed loop Simulink simulation of SEPIC.

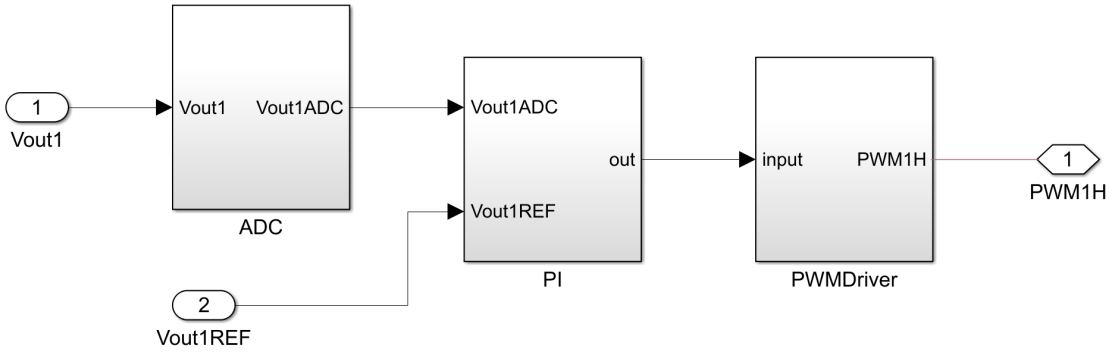

Fig. 3.16. Inside of MCU block.

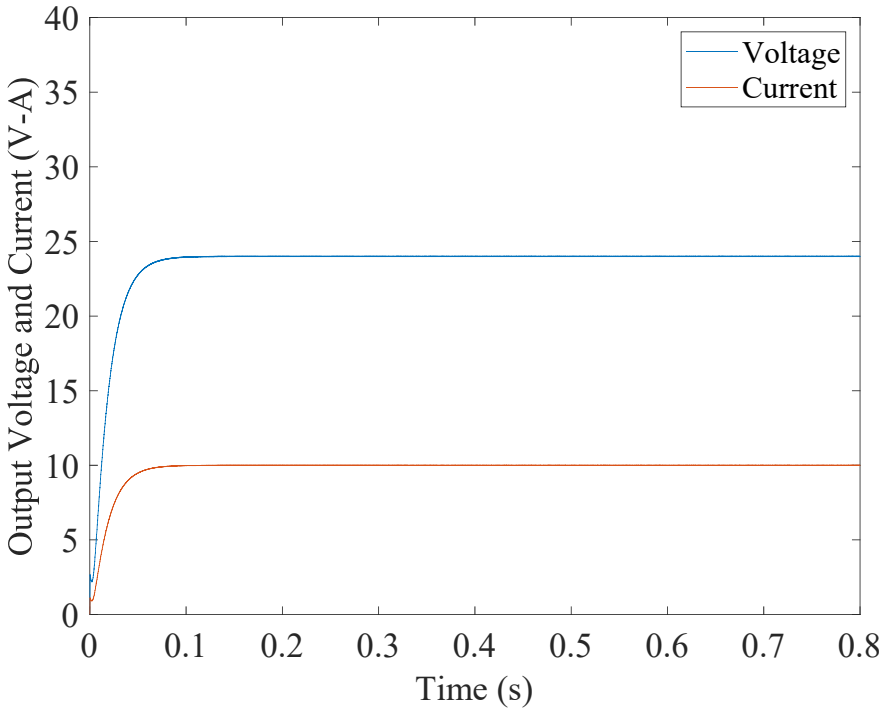

Fig. 3.17. Closed loop simulation result with 2.4 Ω load.

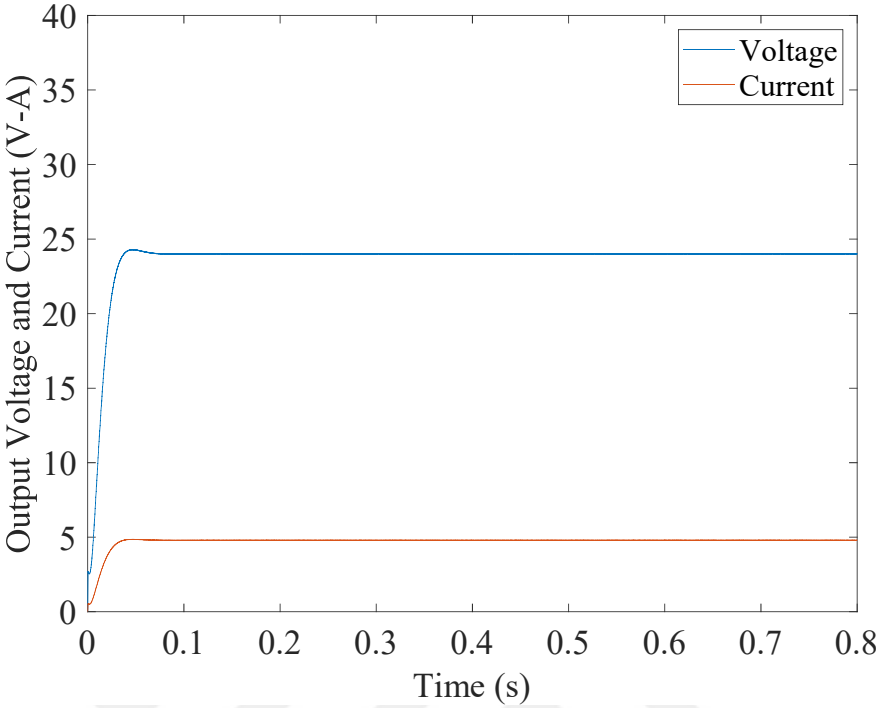

Fig. 3.18. Closed loop simulation result with 5 Ω load.

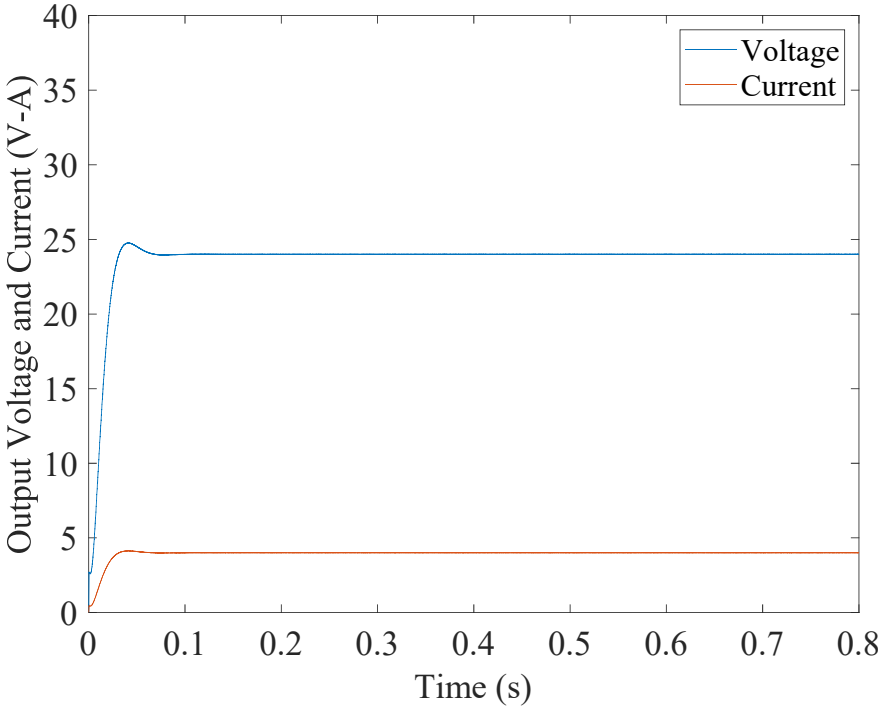

Fig. 3.19. Closed loop simulation result with 6 Ω load.

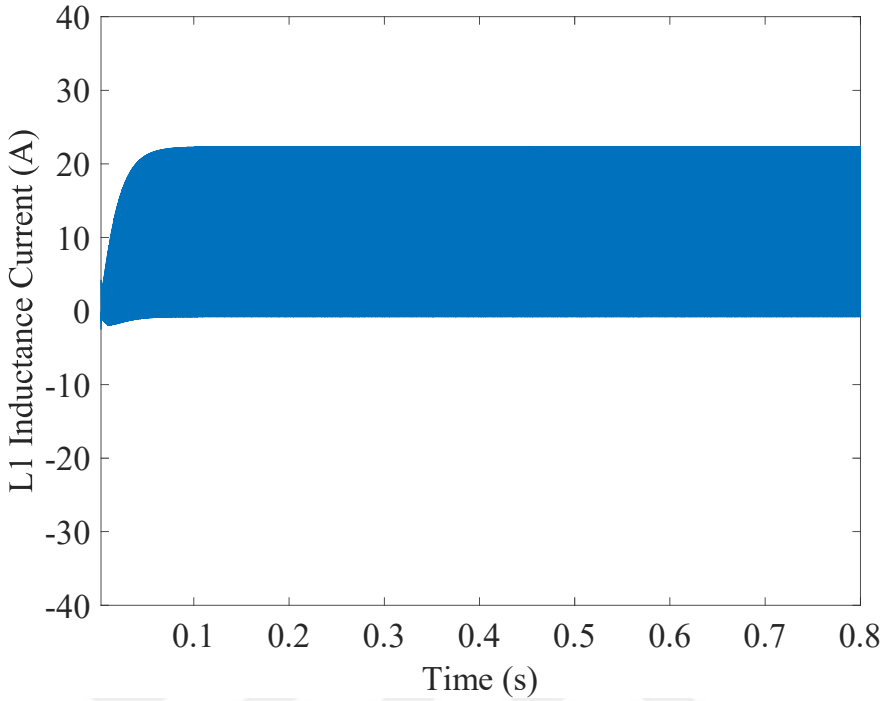

Fig. 3.20. L_1 inductance current of closed Loop simulation.

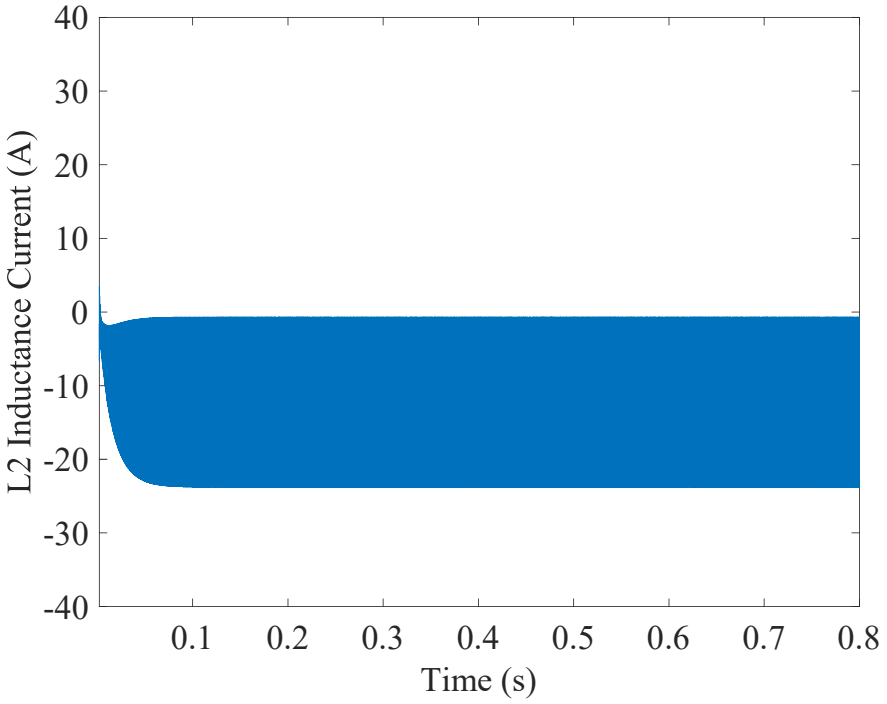

Fig. 3.21. L_1 inductance current of closed loop simulation.

IV. EXPERIMENTAL RESULTS OF ANALOG SEPIC CONVERTER

Design and simulations have been performed for SEPIC LED driver. An analog version of the prototype of SEPIC converter has been prepared to validate simulation results. Main purpose of the high power SEPIC is to keep output voltage and current constant for LEDs. The electrical performance of the prototype SEPIC converter shown in Fig. 4.1 is measured. The experimental setup consists of a power supply, oscilloscope, multimeter, current probes and the load resistances. Texas Instruments LM5022 integrated circuit has been used as a controller.

The load is selected as 2.2 Ω, since it is a standard resistance value. Therefore, the output current is slightly higher than the maximum specified current value. Fig. 4.2 shows the transient response of output voltage for power-up with maximum load. The output voltage settles to its final value less than 50 ms. Fig. 4.3 illustrates output voltage at steady state for 24 V input. The root-mean-square of the ripple is 161 mV.

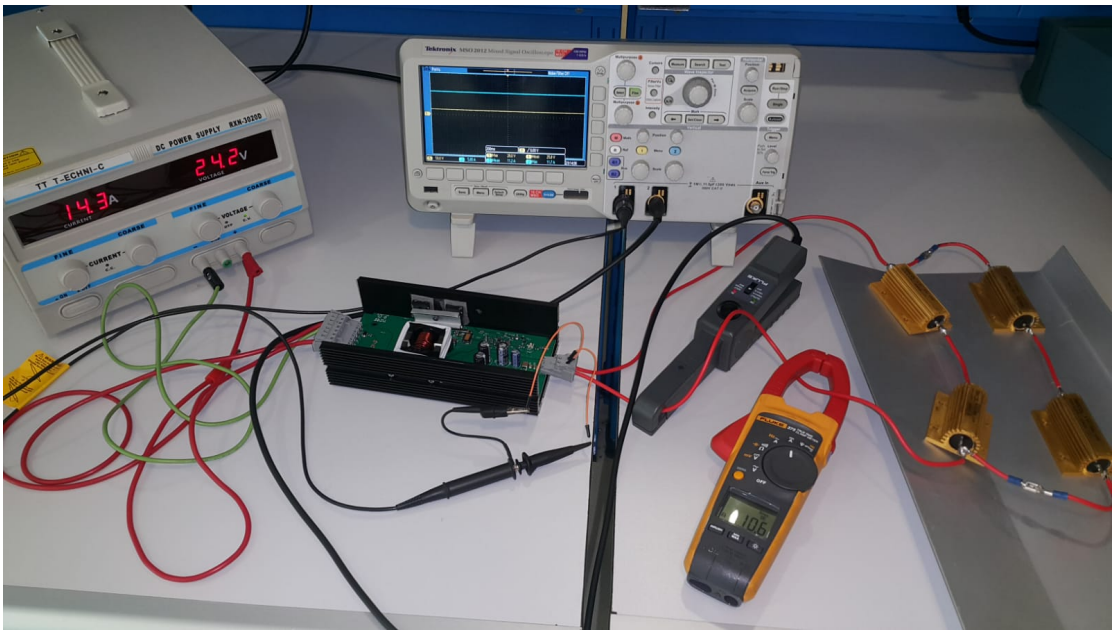

Fig. 4.1. Experimental Setup.

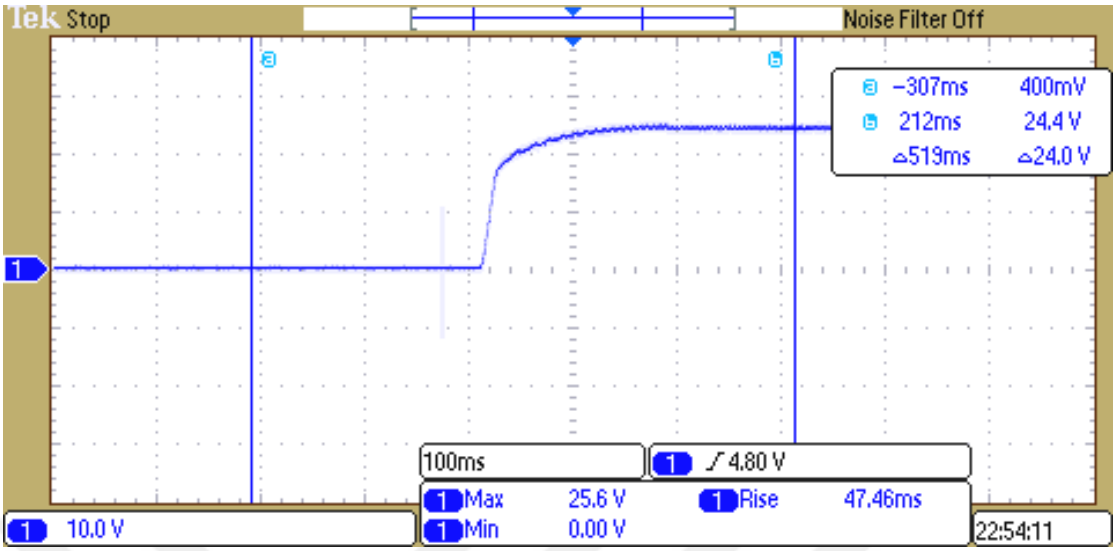

Fig. 4.2. 2.2 Ω load 24 V input.

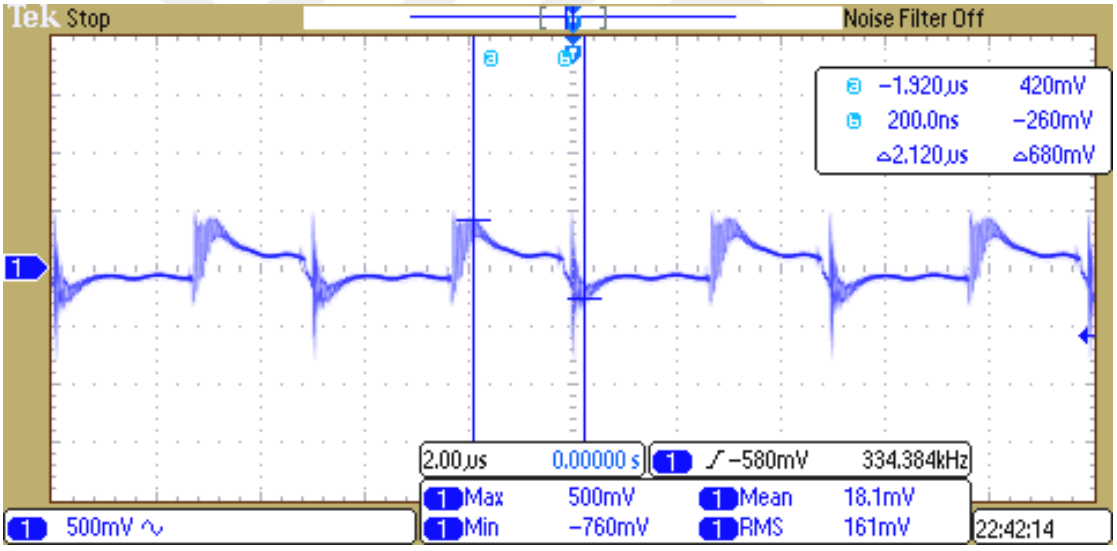

Fig. 4.3. 2.2 Ω load 24 V input.

The snubber circuit performance for 24 V input with 2.2 Ω load is shown in Fig. 4.4. No ringing is observed between drain and source of the switch transistor.

Electrical and magnetic fields are measured between 10 MHz and 400 MHz using Rohde&Schwarz FSH8™ spectrum analyzer on the top of the converter box 60 mm above the PCB, as shown in Figs. 4.5 and 4.6, respectively. RS E 02 and RS H 400-1 probes

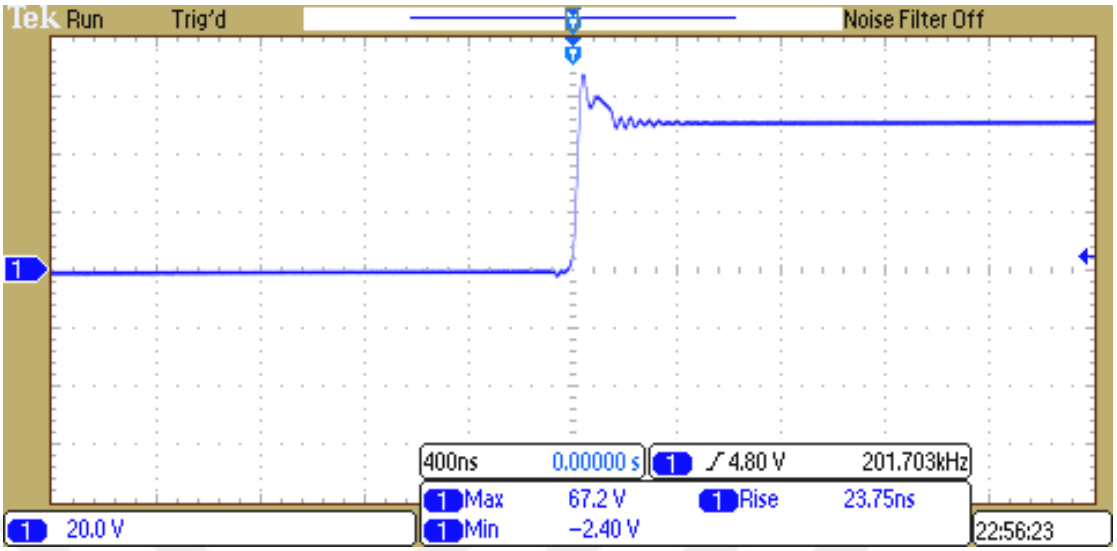

Fig. 4.4. Snubber performance for 2.2 Ω load at 24 V input.

are used for electrical and magnetic field measurements, respectively. Above 240 MHz, the electrical and magnetic fields are below the noise level of the equipment. Electrical and magnetic fields show similar behavior since at measurement distance, the magnetic field is dominant and it is not possible to separate electrical and magnetic field measurements as in simulations. The maximum electrical field is 56 dBμV at 17.2 MHz. The maximum magnetic field is 62.3 dBμV at 27.1 MHz. Due to the switching activity, the electrical and magnetic fields show spikes. The magnetic near-field simulation shown in Fig. 3.9 indicates the magnetic field reaches to its minimum around 200 MHz. Measurement result in Fig. 4.6 shows that the magnetic field reduces as in the simulation till 200 MHz and above this frequency it is below the equipment noise level. The resonances above 200 MHz shown in Fig. 3.9 are not observed in the measurement, because there is no signal at these resonance frequencies. The efficiency of the proposed SEPIC converter is measured around 78%. The main power loss is due to the switching and conducting losses of MOSFET switches.

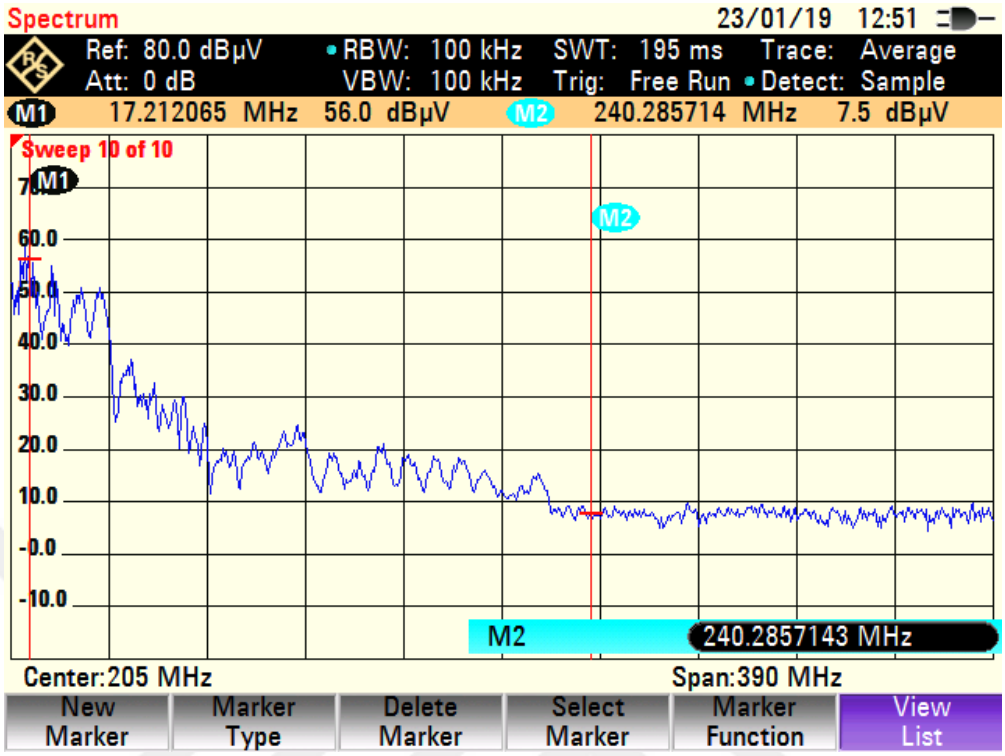

Fig. 4.5. Electrical field measurement.

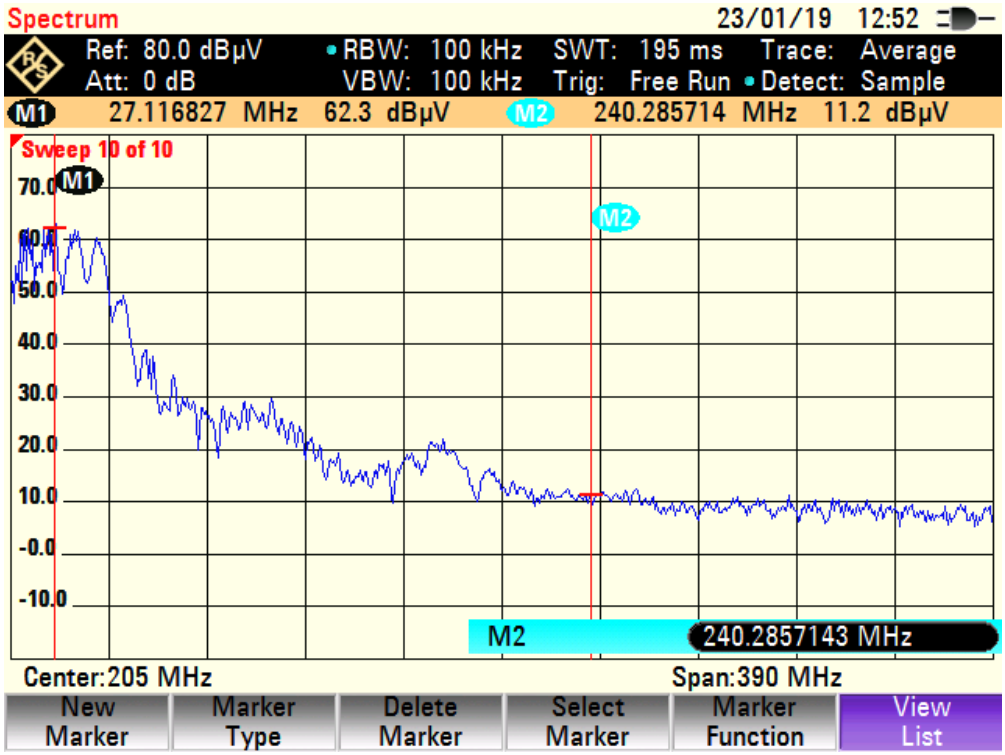

Fig. 4.6. Magnetic field measurement.

V. CONCLUSION

A 240 W output power SEPIC converter is proposed for LED applications. The closed loop stability analysis using average switch model and both analog and digital control simulations indicate that the converter is stable under all possible input voltage and load conditions. A snubber circuit is designed to reduce resonance due to the switching. DC current distribution, power consumption, resonance, near-field and far-field analysis of the SEPIC converter are performed using Ansys SiWave™ signal and power integrity tool. Experimental results of the analog design version of the prototype SEPIC converter also agree with the digitally controlled simulation results.

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