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ISTANBUL AYDIN UNIVERSITY

INSTITUTE OF NATURAL AND APPLIED SCIENCES

NEW CONTROL METHOD FOR DUAL VOLTAGE RECTIFIER

M.Sc. THESIS

Engr. Rai Muhammad Omar

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ONAY FORM

T.C.
İSTANBUL AYDIN ÜNİVERSİTESİ
FEN BİLİMLER ENSTİTÜSÜ MÜDÜRLÜĞÜ

Yüksek Lisans Tez Onay Belgesi

Enstitümüz Elektrik- Elektronik Mühendisliği Ana Bilim Dalı Elektrik- Elektronik Mühendisliği (İngilizce) Tezli Yüksek Lisans Programı **Y1713.300009** numaralı öğrencisi **Rai Muhammad OMAR**' ın **"NEW CONTROL METHOD FOR DUAL VOLTAGE RECTIFIER"** adlı tez çalışması Enstitümüz Yönetim Kurulunun 11.09.2019 tarih ve 2019/18 sayılı kararıyla oluşturulan jüri tarafından oy birliği ile Tezli Yüksek Lisans tezi olarak Kabul..edilmiştir.

Öğretim Üyesi Adı Soyadı	İmzası
Tez Savunma Tarihi : 27/09/2019	
1)Tez Danışmanı: Prof. Dr. Murtaza FARSADI	
2) Jüri Üyesi : Prof. Dr. Ayşen DEMİRÖREN	
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DECLARATION

I hereby declare that all information in this thesis document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results, which are not original to this thesis.

Engr. Rai Muhammad Omar

FOREWORD

After thanks to Allah our creator, I would like to thank my mother and my father who raised me to become a good person. They were patient during my mistakes and my bad times and helped me in all times and everything I have accomplished is because of their effort. I hope I can make them happy and return even some of what they gave me during their whole lives.
I would like to thank my thesis advisor Prof Dr. MURATZA FARSADİ for his guidance, support, and help during my work in the thesis. I thank him for everything I learned from him.

I thank all my teachers starting from my school time until today as they had great influence on me and made me love education and I hope I can become one day a good teacher as they were

September 2019 **Engr. Rai Muhammad Omar**

(Electrical and Electronics Engineering)

TABLE OF CONTENT

ABBREVIATIONS

BJT	: Bipolar Junction Transistor
ce	: Change of Error
D1	: Diode 1
D2	: Diode 2
DV	: Dual Voltage
e	: error
FLC	: Fuzzy Logic Controller
L	: Inductor
LLC	: Inductor Inductor Capacitor
NB	: Negative Big
NS	: Negative Small
PB	: Positive Big
PFC	: Power Factor Correction
PID	: Proportional Integral Derivative
PWM	: Pulse Width Modulation
$\mathbf{S_1}$	: Switch 1
$\mathbf{S_2}$	: Switch 2
SM	: Single Output Mode
SPTT	: Single Pole Triple Throw
$\mathbf{v_{AB}}$	: Voltage between point A and B
$\mathbf{v_{c1}}$	: Voltage across Capacitor 1
$\mathbf{v_{c2}}$	: Voltage across Capacitor 2
w.r.t	: With Respect To

LIST OF FIGURES

LIST OF TABLES

A NEW CONTROL METHOD FOR DUAL VOLTAGE RECTIFIER

ABSTRACT

In this thesis, novel single-phase AC-DC converter dependent on double voltage-rectifier (DV-rectifier) and voltage-sigma design will be proposed. Double DC-Buses, i.e.; a consistent DC voltage BUS and a customizable DC voltage BUS, will be given by the DV-rectifier. Voltages of the two DC-Buses will be stacked together on the Output port through down-stream DC-DC transformers (DCXs). The DC Output voltage is controlled by directing the voltage of the DC-BUS of the DV-rectifier. Consequently, voltage controlling won't be required for the DC-DC transformers, which will dependably work at their upgraded task point to guarantee high effectiveness. Since the voltage of the customizable DC-BUS is lower than the steady DC-BUS, multi voltage-level qualities can be achieved with the DV-rectifier, which will profit for decrease of exchanging misfortunes and improvement of conversion proficiency. To accomplish Current control of AC input port and voltage Regulation of the two DC-Buses at the same time, multi-mode task and smooth mode transition methodologies will be proposed for the DV-rectifier. Task standards, control techniques and characteristics of the DV-rectifier and DC-DC transformer-based AC-DC converter will be examined in detail.

Keywords: *AC-DC converter, dual-voltage-rectifier, dual-dc-bus, sigma structure*

ÇİFT VOLTAJ DÜZELTICI İÇİN YENİ BİR KONTROL YÖNTEMİ

ÖZET

Bu tezde çift gerilim doğrultucuya (DV-doğrultucu) ve voltaj-sigma tasarımına bağlı yeni tek fazlı AC-DC dönüştürücü önerilmektedir. Çift DC-Otobüsler, yani; tutarlı bir DC voltaj BUS ve özelleştirilebilir DC voltaj BUS, DV-doğrultucu tarafından verilecektir. İki DC-Butos'un gerilimleri, dc-DC transformatörleri (DCXs) aracılığıyla Çıkış portu üzerinde bir araya getirilecektir. DC Çıkış gerilimi, DV-doğrultucunun DC-BUS geriliminin yönlendirilmesiyle kontrol edilir. Sonuç olarak, yüksek etkinliği garanti etmek için yükseltilmiş görev noktalarında güvenilir bir şekilde çalışacak olan DC-DC transformatörleri için voltaj kontrolü gerekli olmayacaktır. Özelleştirilebilir DC-BUS'un gerilimi sabit DC-BUS'tan daha düşük olduğundan, dv-doğrultucu ile çok voltaj seviyesinde nitelikler elde edilebilir, bu da alışveriş talihsizliklerinin azalması ve dönüşüm yeterliliğinin iyileştirilmesinden fayda sağlayacaktır. Aynı anda iki DC-Butos'un AC giriş portu ve voltaj Regülasyonunun güncel kontrolünü gerçekleştirmek için DV-doğrultucu için çok modlu görev ve düz mod geçiş metodolojileri önerilecektir. DV-doğrultucu ve DC-DC transformatör tabanlı AC-DC dönüştürücünün görev standartları, kontrol teknikleri ve özellikleri ayrıntılı olarak incelenecektir.

Anahtar Kelimeler: *AC-DC dönüştürücü, çift voltaj-doğrultucu, çift dc-bus, sigma yapısı*

1 INTRODUCTION

AC to DC converters are the important interface of the primary AC grid and different DC loads. They have been broadly utilized in electric vehicle charging, battery charging, smart grids and power supplies for different types of data centers and telecom industries, and so forth. With the fast advancement of EV and battery storages, AC to DC converters with wide DC output voltage ranges are important to meet the necessities of batteries and DC loads. The most effective method to accomplish high productivity and adaptable voltage control on both the AC input side and DC output side has been a developing examination theme in different AC to DC power systems[1]–[3]. Accordingly, new topological and control varieties and advancements have been consistently developing.

Meet the necessities of AC current guideline, DC o/p voltage guideline and electric disengagement, non-segregated boost-type PFC is normally utilized as a front-end rectifier and in charge of AC side regulation and another isolated DC to DC converter is utilized for voltage, charge and power control of DC output [4]. Typically, double stage AC to DC converter, and a constant DC BUS is given by the front-end rectifier and utilized as the contribution for down-stream DC-DC converter [5]. For this situation, the weight of DC o/p volt regulation in a wide range is altogether brought by the down-stream DC to DC converter. Therefore, the general conversion efficiency of the AC to DC converter is damaged by both the two-stage power handling stages and wide DC o/p voltage range [6]. Numerous endeavors have been tried to improve the change proficiency of the front-end rectifier and the downstream DC to DC converter, and consequently improve the general effectiveness of whole AC to DC converter [7], [8]. Soft-switching or multilevel techniques are viable for lessening the exchanging losses of active switches at the PFC stage [9], [10], on the other hand, bridgeless technique can be utilized to diminish conduction losses [11]–[13]. Soft switched DC to DC converters are utilized for down-stream DC to DC converter in a dual stage AC to DC converter. Among different soft switching DC to DC converters, LLC resonant converters are favored because of its amazing soft switching execution for both

primary side and secondary side gadgets, low volt stresses of switching components and simple reconciliation of magnetic parts [14], [15]. It is as yet difficult to accomplish high proficiency with an LLC resonant converter when the o/p voltage is should have been regulated in a variable range. There are many advanced parameter plan techniques, advanced topologies, altered adjustment systems suggested for LLC resonant converters, the productivity is as yet unavoidable to be harmed by the volt regulation range [16]–[18]. It's been approved that the best environment of a resonant converter is working it at series resonant frequency (f_R) of the resonant tank. When converters are utilized as unregulated DC transformer (DC-DC transformer) and dependably works at its streamlined conditions, high proficiency can be accomplished for the DC to DC stage [19]. However, for the DC to DC power stage in a dual stage AC to DC converter planned with wide output voltage applications, DC-DC transformer isn't acknowledged, particularly when the voltage of DC bus or the contribution of the DC to DC arrange is consistent. To conquer this disadvantage, variable volt DC bus is proposed for front-end rectifier [20], [21]. With wide range DC bus volt, the standardized voltage gains scope of the down-stream DC-DC stage can be decreased fundamentally, and subsequently better for the efficiency of the DC-DC stage. Tragically, the voltage of the DC bus. Since a Boost converter is utilized, DC bus voltage should be high than the peak amplitude of the AC input volt to guarantee well regulation of AC current. Proficiency of a rectifier drops if the DC bus voltage increments. In this manner, variable DC bus volt is better for the DC to DC arrange, however not suitable for front-end rectifier. Subsequently, it is extremely hard to consider the effectiveness and voltage Regulation scope of the rectifier and DC-DC stage at the same time.

In [7], AC to DC converter with sigma engineering and three-port rectifier was proposed. Dual DC o/ps are given by three-port rectifier, and two DC o/ps are proportionate parallel associated at load port through downstream DC-DC converter. So, it is a current-sigma engineering and the complete load Current is proportional to sum of two DC Outputs of the front-end rectifier. The Current-sigma engineering is a decent answer for Non-isolated AC to DC power converter, particularly consistent DC Output application. For Isolated AC to DC power transformation with variable DC Output, a DC-DC converter with wide voltage gain range is yet required for the current-sigma model. In this thesis, novel AC to DC converters with double DC-Buses

and voltage-sigma design will be proposed. Unique in relation to the Current-sigma design proposed in [7], the volts of the two DC buses will be added at the output port. Consequently, the o/p volt can be completely regulated by front-end rectifier, and DC-DC transformer can be utilized in the down-stream DC to DC level. The voltage sigma design is considerably much more appropriate for isolated AC to DC power converter with wide DC o/p. More vitally, the operation standards, attributes, modulation and controlling of AC to DC converters proposed in this thesis will be changed as in [7].

The real commitment of this thesis will be to propose a novel double voltage-rectifier (DV-rectifier)- based AC to DC converter, with which a consistent voltage DC bus and a variable voltage DC bus will be accommodated the down-stream DC to DC stage. The DC Output voltage will be legitimately Regulated by the front-end DV-rectifier and there is no voltage regulation necessity for the down-stream DC to DC arrange. In this way, unregulated DC-DC transformer can be utilized to improve proficiency of DC to DC arrange. Furthermore, multi-voltage-level can be created by the dual voltage rectifier to decrease conversion losses.

1.1 Problem Definition

The function of any AC/DC or DC/DC converter module is to meet one or more of the following requirements:

i: to match the secondary load to the primary power supply

ii: to provide Isolation between primary and secondary circuits iii: to provide protection against the effects of faults, short circuit or over heating

iv: to simplify compliance with safety, performance or EMC legislation [22].

The term topology refers to the different forms of switching and energy storage element combinations that are possible for the transmission, control and regulation of an output voltage or current from an input voltage source [22]. Different types of topologies for control switching are mainly divided into two main categories

1.2 Non-Isolated Converter

Non-isolated converters, in which the input source and the output load share a common Current path during operation.

1.3 Isolated Converter

Isolated converters, in which the energy is transferred via mutually coupled magnetic components (transformers), wherein the coupling between the supply and the load are achieved solely via an electromagnetic field, thereby permitting galvanic Isolation between input and output [22].

There are two basic types of electrical converters.

1.4 AC to DC Converters

These types of converters are used when we need our output in DC form. They are of two main types which are commonly used in electrical circuits. It may consist of transformer in it which steps up or steps down the input voltage according to our requirement. Basic circuit diagram of these type of converter is shown in figure 1.1.

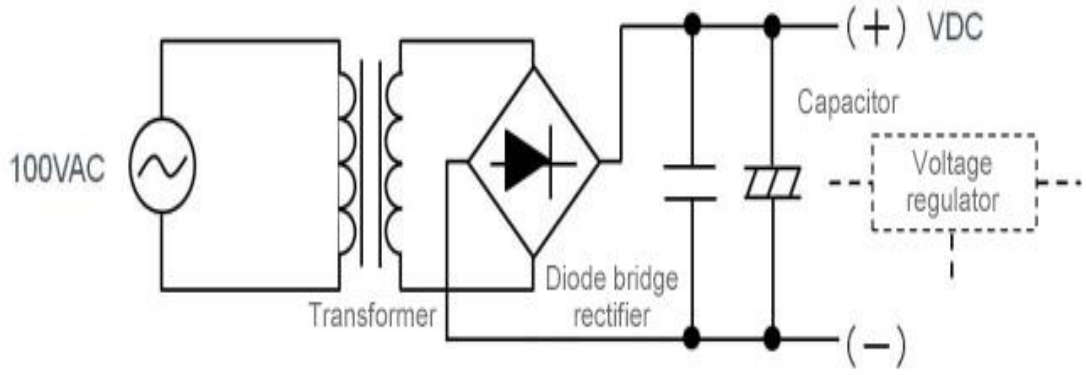


Figure 1.1 Block Diagram of AC to DC Converter.

Above mentioned AC to DC power supply circuit is not commonly used because of their losses due to transformer. Because there are different types of power losses occur like hysteresis lose and eddy Current lose. Second type of AC to DC converter uses bridge diode for rectification of voltage. {A diode bridge in a bridge circuit configuration that provides the same polarity of Output for either polarity of input. When used in its most common application, for conversion of an alternating-

Current (AC) input into a direct-Current (DC) Output, it is known as a bridge rectifier. A bridge rectifier provides full-wave rectification from a two-wire AC input, resulting in lower cost and weight as compared to a rectifier with a 3-wire input from a transformer with a center-tapped secondary winding. The essential feature of a diode bridge is that the polarity of the Output is the same regardless of the polarity at the input. The diode bridge circuit was first used by Polish electro technician Karol Pollak [23].

1.5 DC-DC Converters

For Non-isolated DC/DC converters there are five basic transformer-less topologies:

a) Buck or step-down converter
b) Boost or step-up converter
c) Buck-boost or step-up-down converter
d) Two-stage Inverting Buck-boost (Ćuk converter)
e) Two stage non-inverting Buck-boost (Sepic converter, ZETA converter)

Our scope in this thesis is to only discuss Buck and Boost Converters and we shall stick to these two types of DC-DC converters. There are several controlling techniques available for controlling Outputs of these circuits in which PWM is widely used.

1.5.1 Buck Converter

In the circuit diagrams the P-FET or N-FETs are shown only as simple switches.

As the name suggests, the buck-converter or sometimes called the step-down converter, converts a high input voltage to a stabilized low Output voltage. A simple buck-converter is shown in figure 1.2 and the voltage-Current waveforms of circuit elements are shown in figure 1.3

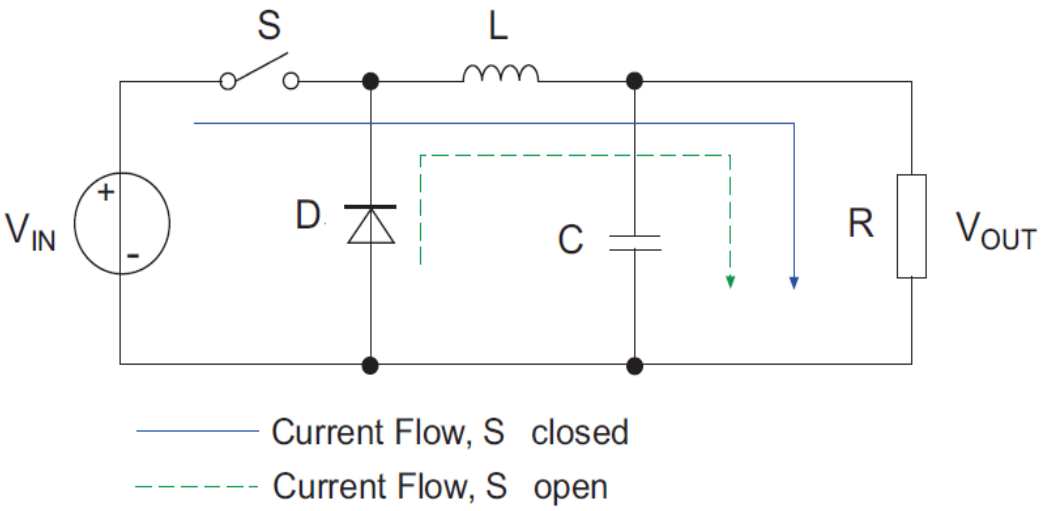


Figure 1.2 Simple Buck-Converter.

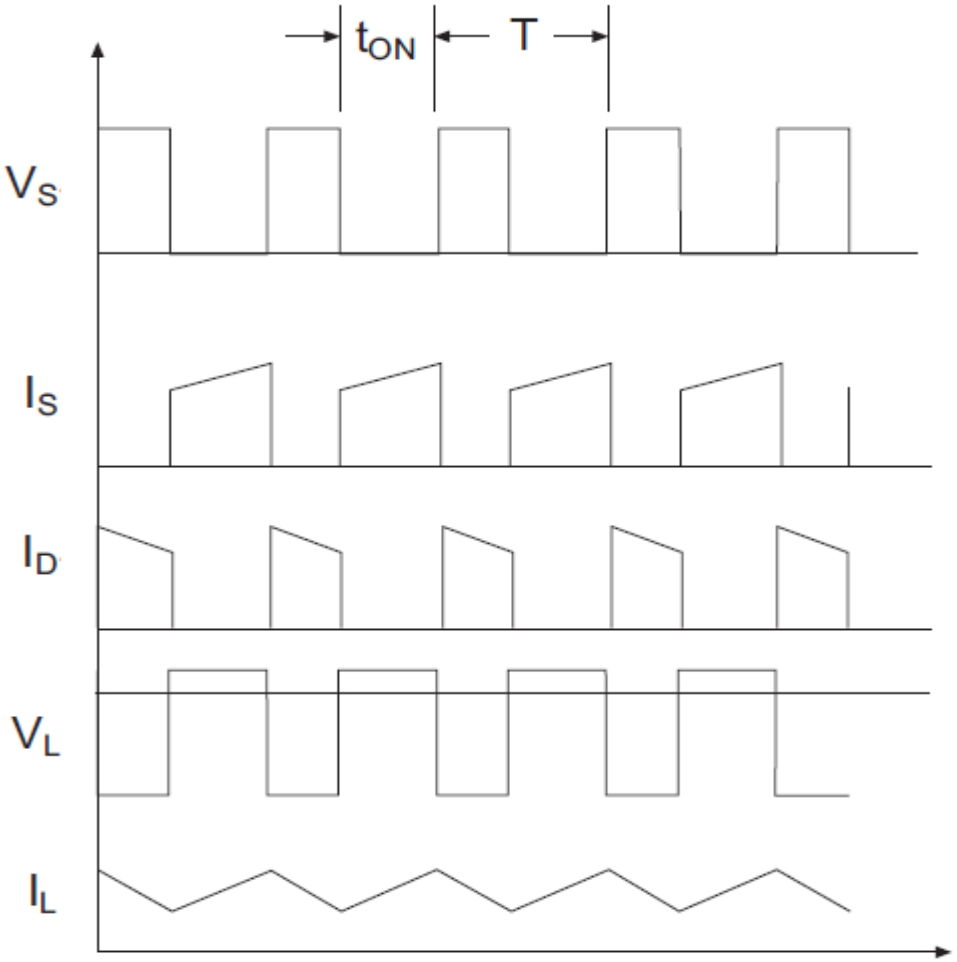


Figure 1.3 Buck Regulator Characteristics.

$$\boldsymbol{V_{OUT} = V_{IN}\frac{t_{ON}}{T} = \delta V_{IN}}\text{ , valid when } \boldsymbol{V_{IN} > V_{OUT}} \quad \textbf{1.1}$$

The transfer function of the buck-converter can be derived as:

For ON state: Input Power = $(V_{IN} - V_{OUT})t_{ON}$ **1.2**

For OFF state: Output Power = $\boldsymbol{V_{OUT}t_{OFF}}$, **1.3**

Where,

$$t_{OFF} = T - t_{ON} \text{ and}$$

$$\delta = \frac{t_{ON}}{T}$$

Substituting gives:

$$\boldsymbol{(V_{IN} - V_{OUT})t_{ON} = V_{OUT}(T - t_{ON})} \quad \textbf{1.4}$$

$$\boldsymbol{V_{IN}t_{ON} = V_{OUT}T}$$

$$\boldsymbol{V_{OUT} = V_{IN}(\frac{t_{ON}}{T})}$$

$$\boldsymbol{\frac{V_{OUT}}{V_{IN}} = \delta} \quad \textbf{1.5}$$

Equation 1.5 is the transfer function of Buck-Converter

1.5.2 Boost Converter

Boost converter is also called as step-up converter. As it is clear by its name it converts low voltage input to a higher Output voltage. A simplified form of boost converter is shown in figure 1.4 and its voltage-Current graphs in figure 1.5

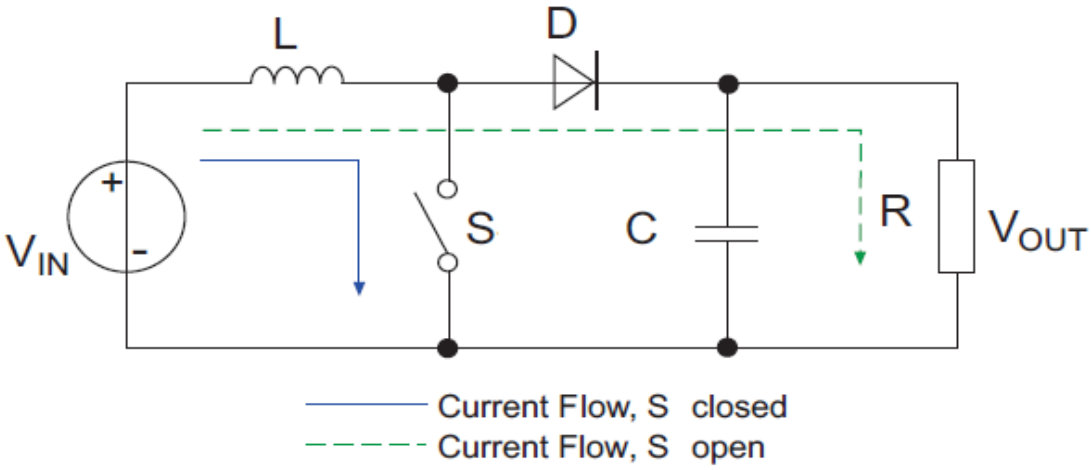


Figure 1.4 Simple Boost Converter.

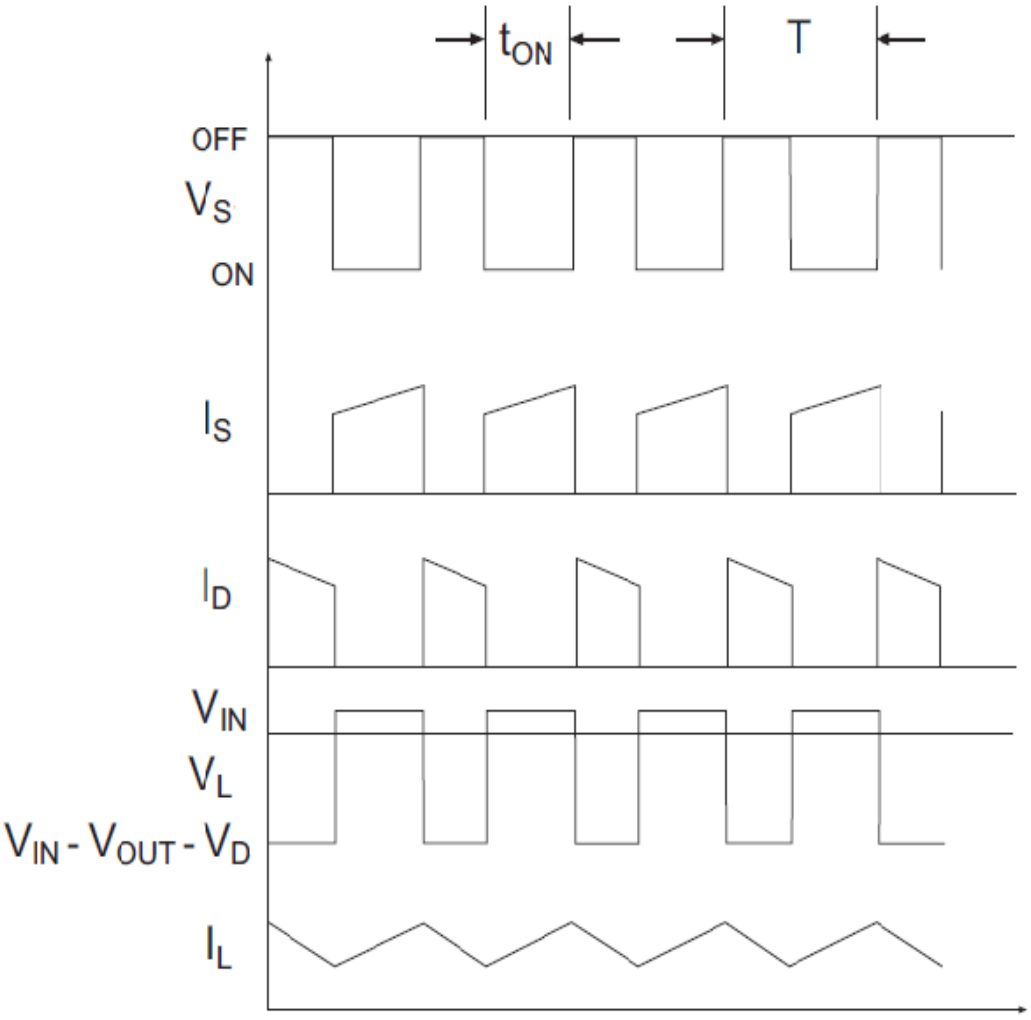


Figure 1.5 Boost Converter Characteristics.

For ON state: Input Power $= V_{IN} t_{ON}$

For ON state: Output Power $= (V_{OUT} - V_{IN}) t_{OFF}$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-\delta} \qquad \textbf{1.6}$$

Eq 1.6 is the transfer function for boost-converter

1.5.3 Buck-Boost Converter:

It is also known as fly back converter. This converter converts an input voltage to an Output voltage which can be higher or lower in magnitude as compared to input voltage. A simple fig. of a buck-boost converter is shown in 1.6 and their associated graphs in figure 1.7

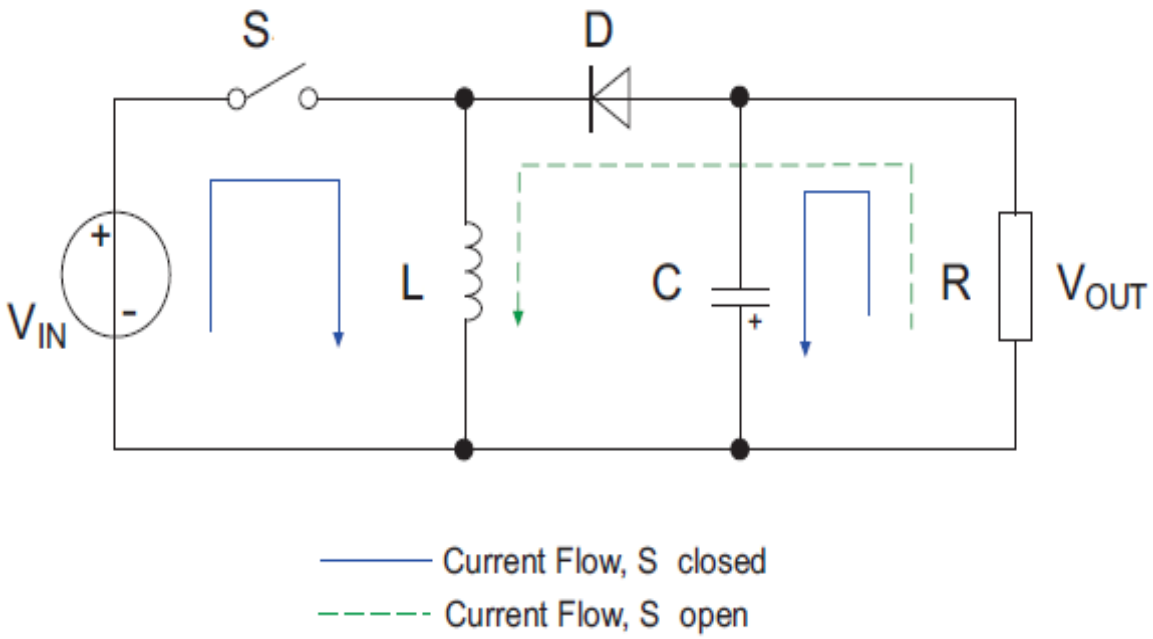


Figure 1.6 Simple Buck-Boost Design.

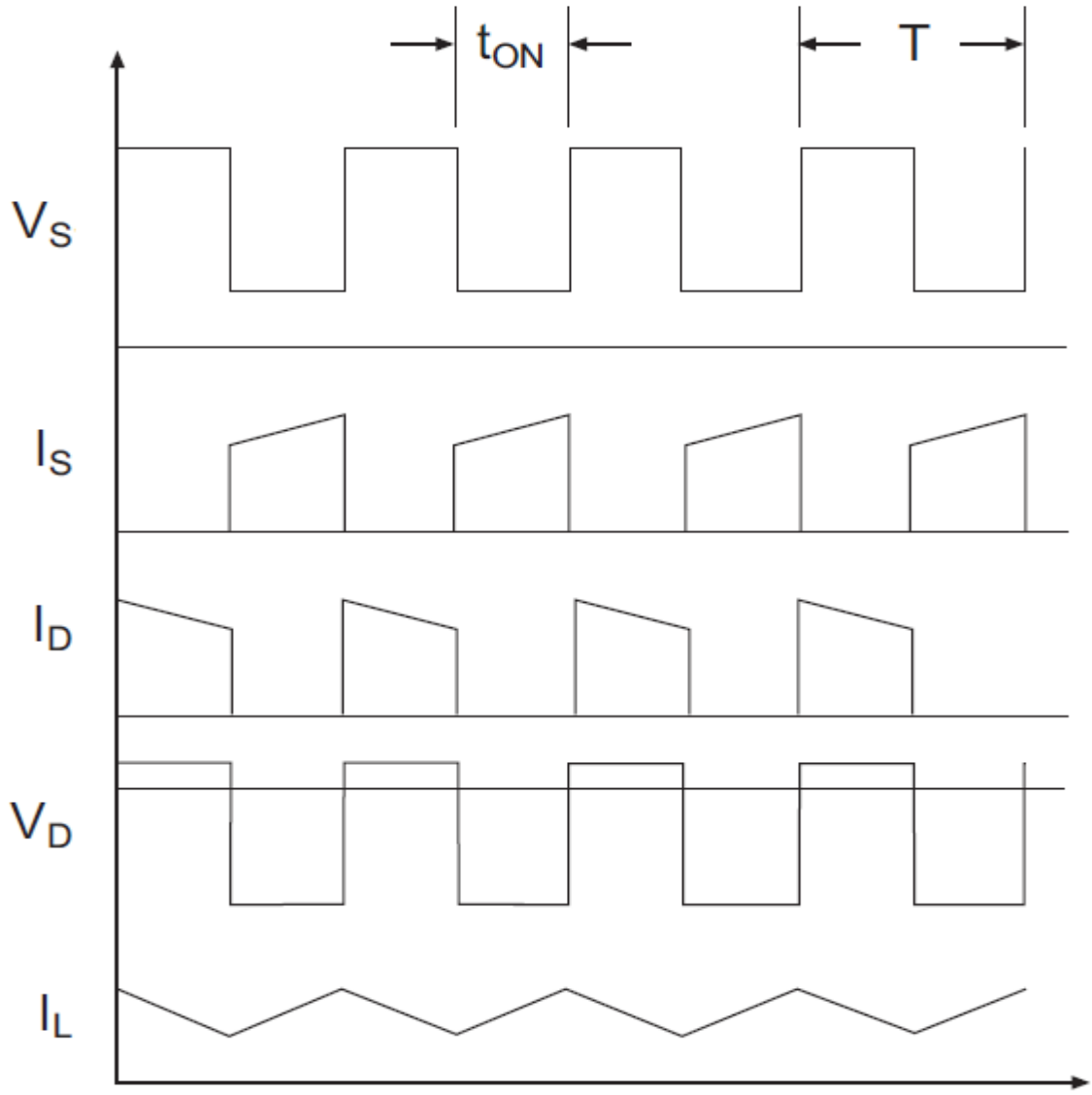


Figure 1.7 Buck-Boost Characteristics.

In this circuit when switch S is in ON state, a Current IL, which increases as $\frac{V_{IN}}{I_L}$, flows through inductor L. Diode D blocks any Current to flow into theR_L. In this state, the Output Current is supplied by Output capacitor C. When switch S is in OFF state, the energy stored in capacitor L causes the end of switch of the inductor to become negative. The Current now flows to the load. The inductor Current now decreases in proportion to $\frac{V_{OUT}}{L}$. This type of topology is best suitable for producing -ve voltages only.

$$V_{OUT} = V_{IN}\frac{-\delta}{1-\delta} \quad V_{IN} > V_{OUT}\ OR\ V_{IN} < V_{OUT} \tag{1.7}$$

The derivation of buck-boost transfer function is same as that of discussed in the previous section, only the main equations are:

For ON state: Input Power $= V_{IN}t_{ON}$

For OFF state: Output Power $= -V_{OUT}t_{OFF}$

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\delta}{1-\delta} \tag{1.8}$$

Equation 1.8 is the transfer function of buck-boost converter.

2 MAIN CIRCUIT AND PROPOSED DESIGN

2.1 Voltage Conversion of a Conventional Two-Stage AC to DC Converter

The block diagram of a regular Boost-PFC-based two-stage AC to DC converter is shown in Fig. 2.1(a), the voltage connection between input voltage v_{in} and Output voltage V_{Hi} of the PFC stage is delineated in Fig. 2.1(b), while the conceivable relations among V_{Hi} and the Output voltage V_o of the DC-DC stages are shown in Fig. 2.1(c)-(e). The pulsed input voltage v_{in} is ventured up to a steady DC-BUS voltage V_{Hi} and utilized as the input of the DC-DC stage, at that point V_{Hi} is changed over to movable DC Output voltage with a Boost-type, Buck-type, or a Buck-Boost type DC-DC converter, as delineated in Fig.2.1(c), (d) and (e), separately.

With a consistent voltage V_{Hi}, improved operation points for a Boost-type and Buck-type DC to DC stage is the most reduced and highest Output voltage, individually, while the best effectiveness point can be set at a specific load voltage when a Buck-Boost DC to DC is utilized. Nonetheless, regardless of which type DC to DC stage is utilized, it is hard to acknowledge high effectiveness inside the whole Output voltage run.

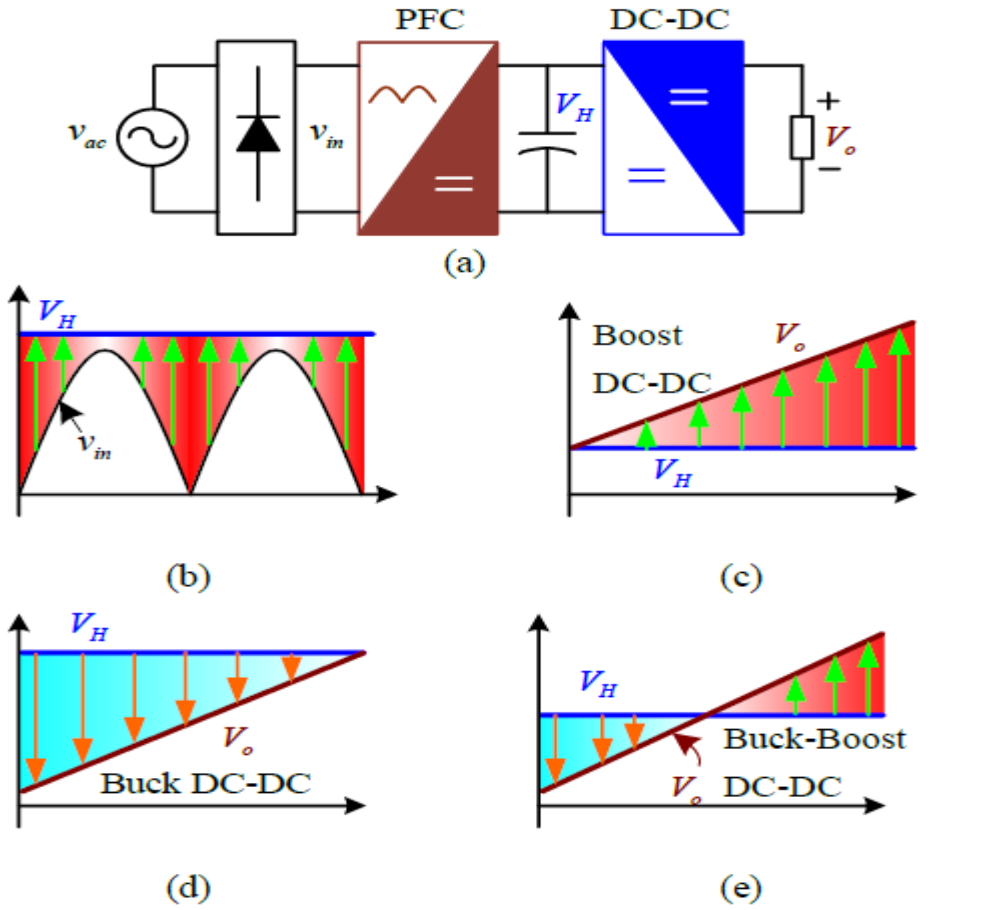


Figure 2.1 Conventional Two Stage AC to DC Converter.

2.2 Voltage Conversion of Proposed Circuit

The block drawing of proposed circuit converter is appeared in Fig. 2.2(a), while the relation between input and output volts of front-end rectifier and downstream DC to DC stage are represented in Fig.2.2(b), individually. To keep away from proficiency, decrease of the DC to DC stage because of wide volt regulation range, the fundamental thought of the proposed AC to DC converter depends on dual DC bus strategy. Two DC buses, that are, a consistent voltage DC bus V_{Hi} and customizable DC bus V_{Low}, are provided by the DV-rectifier.

The volts of V_{Hi} is consistent and will be higher than the maximum amplitude of V_{in} to guarantee well controlling of AC current and high power factor correction, and the voltage of V_{Low} can be controlled between 0 to V_{Hi} as per the necessity of V_o. The two voltages, V_{Hi} and V_{Low}, are added on the output point through the DC to DC converter. Since o/p volt V_o can be straightforwardly controlled by changing the voltage V_{Low}

appropriately, there will be no volt regulation prerequisite for the DC to DC converter. In this manner, Unregulated DC-transformer (DC-DC transformer) with streamlined task criteria can be utilized as the DC to DC stage. As appeared in Fig. 2.1 (c), the connection between V_o, V_{Hi} and V_{Low} is communicated as:

$$V_O = G_{DC-DC}(V_L + V_{Hi}) \quad \textbf{2.1}$$

where G_{DC-DC} is volt gain of the DC to DC transformer. DC to DC converters with volt regulation capacity is just required only once the variation range of V_{Low} can't fulfill the prerequisite of V_o, however, the volt regulation range of the DC to DC stage can in any case be limited altogether, which is an advantage of the design, execution and conversion effectiveness of the DC to DC stage.

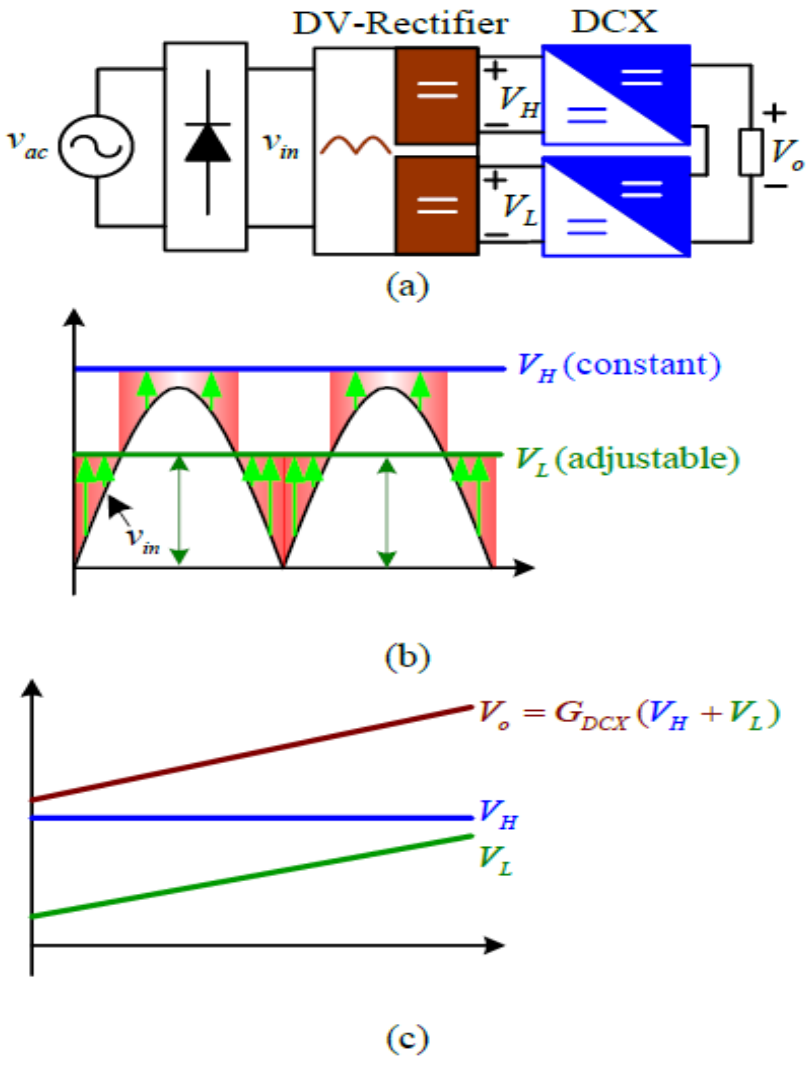


Figure 2.2 Proposed DV Rectifier Block Diagram.

2.3 Topologies of Dual Voltage Rectifier & DC-DC transformer

The dual voltage rectifier is the key to the proposed AC to DC converter. A dual voltage rectifier can be determined by bringing another DC o/p into an ordinary boost power factor corrector or bridgeless boost power factor corrector. Keeping in mind the standard of dual o/p boost converter, a group of dual voltage rectifier topologies are outlined in fig. 2.3 The topologies have appeared in Fig. 2.3 (a) and (b) and are taken from a regular Boost PFC [5]–[7], on the other hand the topologies in Fig. is derived from a bridgeless Boost PFC [11]. Two DC o/p, for example V_{Hi} and V_{Low}, are provided by DV-rectifiers. New branch presented for the movable DC Output V_{Low} has been featured in Fig. Clearly the voltage V_{Hi} is constantly more noteworthy than V_{Low}. Thusly, a functioning switch, for example S_2 in Fig. 2.3(a) and S3 in Fig. 2.3(b) and, is utilized to appropriate the AC input control among V_{Hi} and V_{Low}.

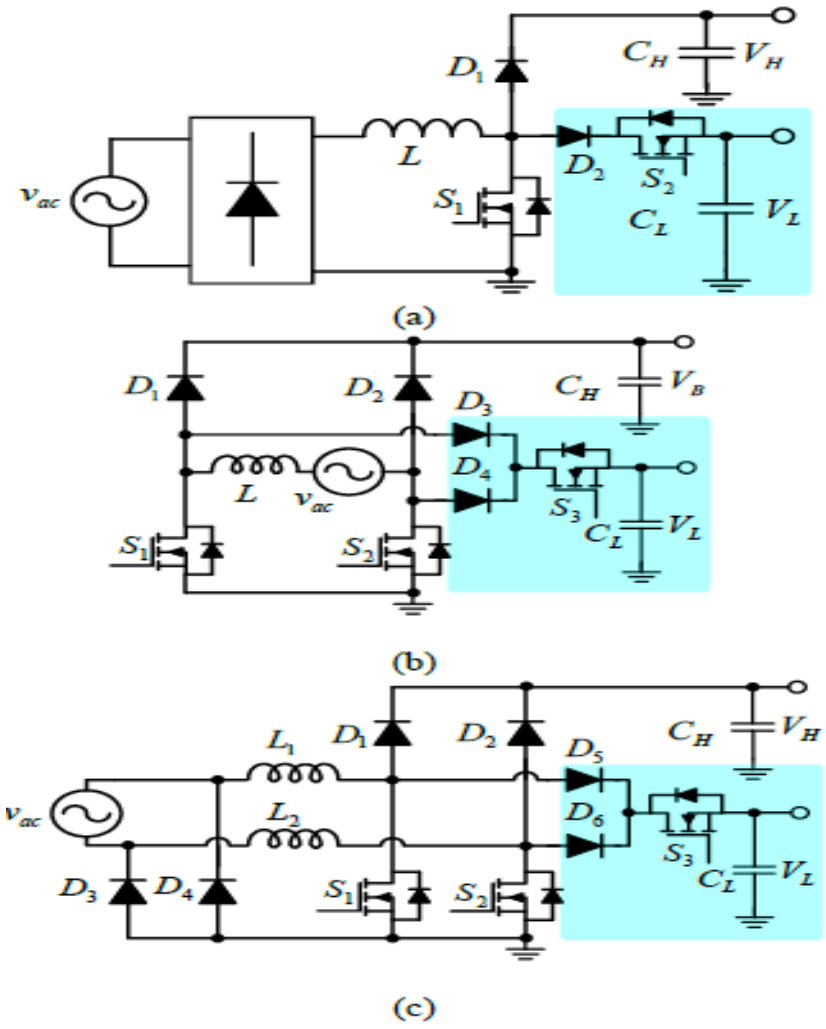


Figure 2.3 Different Types of Boost Topologies.

2.4 LLC Resonant Converter

The DC to DC transformer in the proposed AC to DC converter is utilized to coordinate the load voltage with the two DC Buses with a legitimate transformer turns proportion. Practically all isolated DC to DC converters could be utilized as DC to DC transformer, a soft switching full converter, for example, the LLC resonant converter, is favored because of its high productivity and high-power ratio. In this thesis, the LLC full converter appeared in Fig. 2.4 is utilized as the downstream DC to DC transformer to demonstrate the task of the proposed DC to DC transformer.

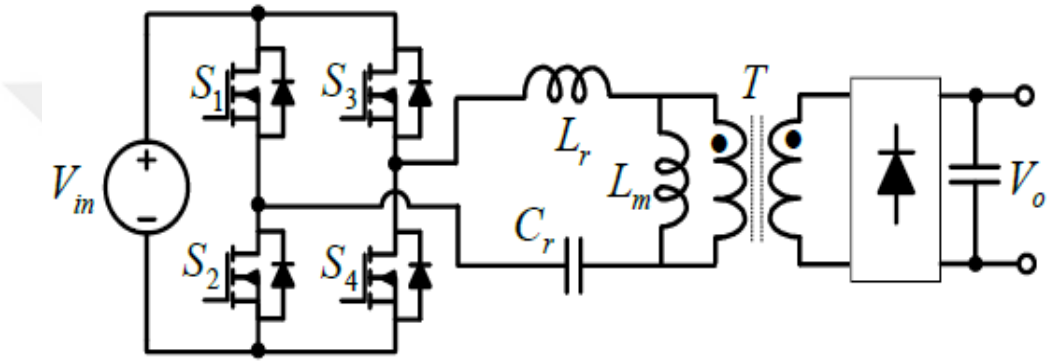


Figure 2.4 LLC Resonant Converter.

2.5 Analysis of the Proposed AC to DC Converter

The proposed AC to DC converter appeared in Fig. 2.5, where the dual voltage rectifier in Fig. 2.3(a) is utilized as the main PFC converter, is utilized to investigate the activity standards, control and qualities of the proposed arrangements.

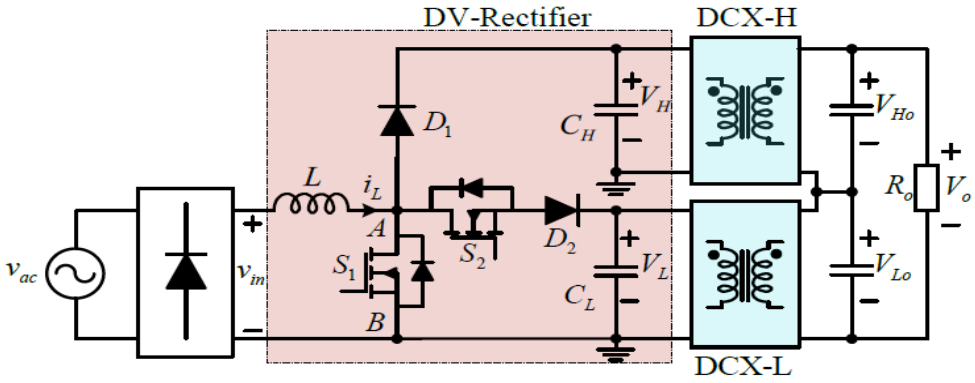


Figure 2.5 Block Diagram of Proposed AC to DC Converter.

2.6 Operational Modes of Dual Voltage Rectifier

To decrease switching losses, there is just one ON dynamic switch, S_1 or S_2, will be switched at high recurrence, the other switch will be kept ON or OFF. As per the switching conditions of S_1 and S_2, the converter has triple activity modes.

2.7 V_{Hi} Single-Output Mode

At the point when the switch S_2 is kept OFF and S_1 works at high switching frequency, the rectifier works in the V_{Hi} single o/p mode (V_{Hi}-SM). Fig. 2.6 demonstrates the comparable circuit of the V_{Hi} single o/p mode. Clearly, the equal cct of the front-end rectifier is equivalent to the customary boost power factor corrector (PFC), the single o/p boost converter is worked by inductor L, the switch S_1, and the diode D_1. At this instance, all the power is provided to the V_{Hi} port, and the post voltage V_{AB} will change between volt 0 and V_{Hi} with S_1 On & Off, respectively.

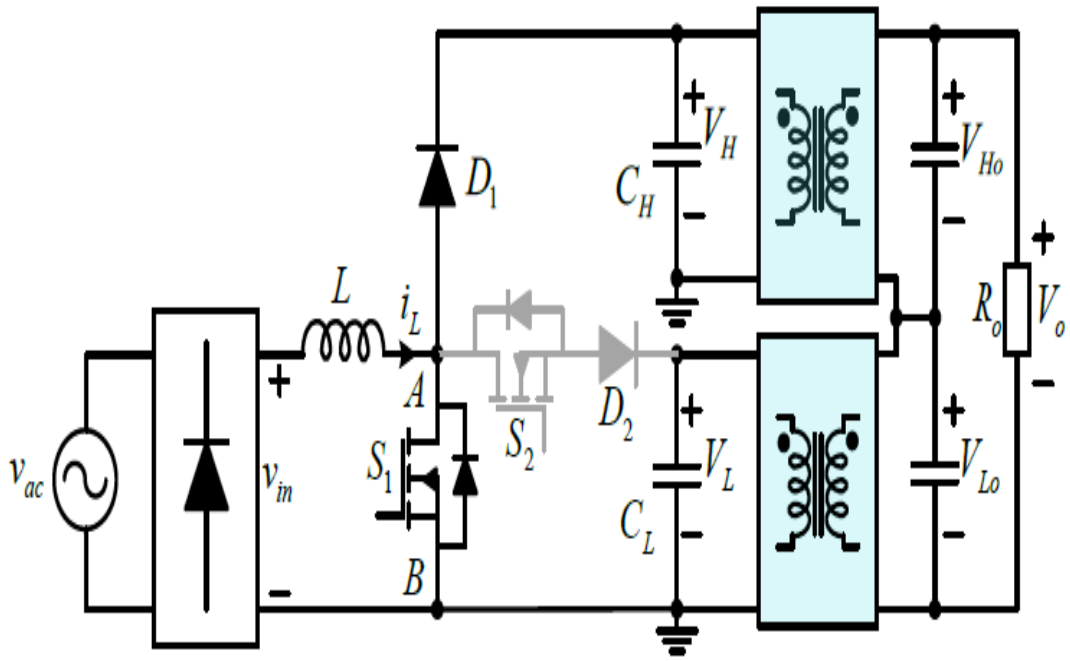


Figure 2.6 V_{Hi} Single Output Mode.

2.8 V_{Low} Single Output Mode

The rectifier will work in the V_{Low} single-Output mode (V_{Low}-SM) if the switch S_2 is dependably ON and S_1 works at max frequency. The equal circuit of the V_{Low} single o/p mode is appeared in Fig. 2.7. Since V_{Hi} is more prominent than V_{Low}, the diode D_1

will be reversed biased and hence no power transferred to V_{Hi} port. Another Boost PFC converter is developed by the inductor L, the switch S_1 and the diode D_1. Though S_1 is switching ON and OFF state, the voltage v_{AB} switches among 0 and V_{Low}. It ought to be noticed, since the proportionate cct of the rectifier is a Boost converter, the volt V_{Low} must be more noteworthy than the information volts v_{in} to ensure the converter works properly. Thusly, the rectifier can possibly work in the V_{Low} single o/p mode when v_{in}<V_{Low}.

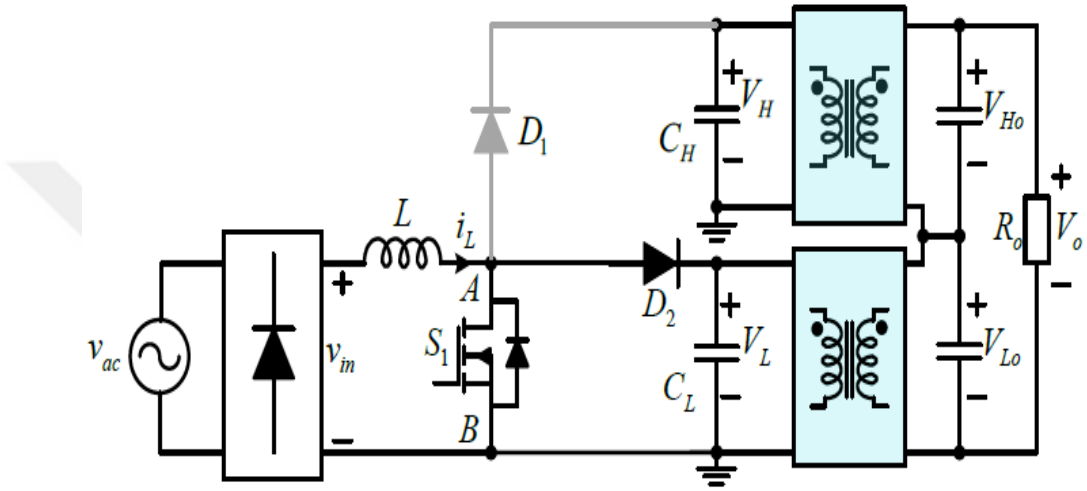


Figure 2.7 V_{Lo} Single Output Mode.

2.9 V_{Low} and V_{Hi} Dual Output Mode

If switch S_1 is kept OFF and just the switch S_2 is a high-frequency switch, the DV-rectifier will work in the V_{Low} and V_{Hi} double Output mode. The comparable circuit of this mode is appeared in Fig. 2.8, where an equivalent Boost PFC is formed by the inductor L, the switch S_2, the diode D1 and D2. Not the same as the V_{Low}-SM and the V_{Hi} -SM, the input power is provided to the V_{Low} and V_{Hi} port on the other hand as S_2 is turned ON and OFF. Henceforth, the voltage vAB changes among V_{Low} and V_{Hi}. Clearly, to influence the equivalent Boost converter to work typically, the inductor L must be charged when S_2 is ON with the goal that the inductor L can be discharged when S_2 is OFF. In this manner, the DV-rectifier can possibly work in the DM when

$$V_{Hi} > v_{in} > V_{Low}$$

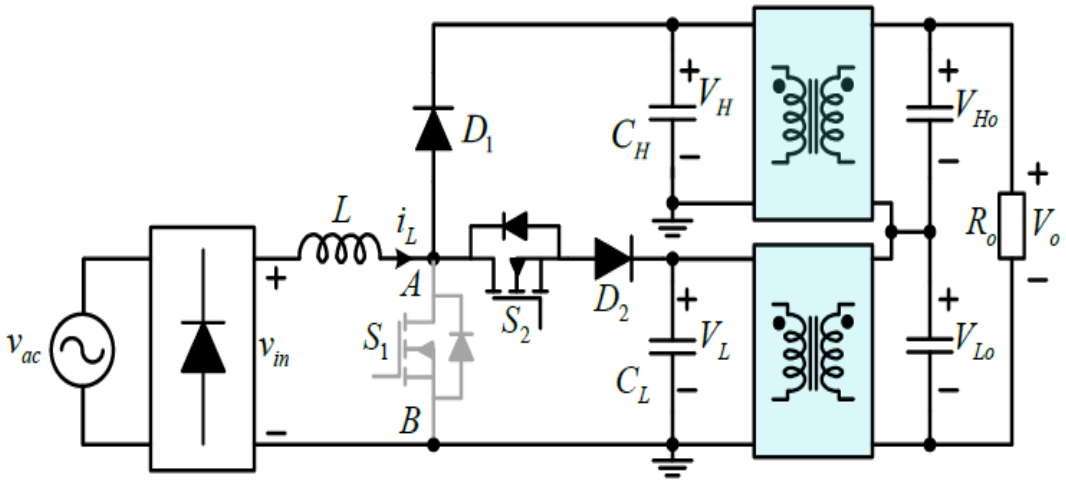


Figure 2.8 V_{Lo} and V_{Hi} Dual Output Mode.

2.10 Operation Mode Consideration

As appeared in Fig. 2.2(b) and Fig. 2.2(c), the voltage V_{Hi} is consistent and higher than the maximum amplitude of v_{in}, for example V_M, while voltage of V_{Low} can be Regulated between 0 to V_{Hi} to coordinate the Output voltage V_o. In light of the working standard of Boost converter, operation area of various modes can be inferred. Fig. 2.9 demonstrates the conceivable activity areas of the V_{Low} -SM and DM in half time of the grid voltage w.r.t voltage V_{Low}. Since the voltage V_{Hi} is steady and constantly higher than V_M, the DV-rectifier can work in the V_{Hi} single-Output mode inside whole input voltage range. In this manner, the stage point scope of V_{Low} -SM, DM and V_{Hi} -SM fulfill:

$$V_{LOW} - SM: \tag{2.2}$$

$$0 \leq \omega t \leq arcsin\frac{V_{LOW}}{V_M} \; and \; \pi - arcsin\frac{V_{LOW}}{V_M} \leq \omega t \leq \pi$$

$$DM: \quad arcsin\frac{V_{LOW}}{V_M} \leq \omega t \leq \pi - arcsin\frac{V_{LOW}}{V_M} \tag{2.3}$$

$$V_{HIGH} - SM: \quad 0 \leq \omega t \leq 0 \tag{2.4}$$

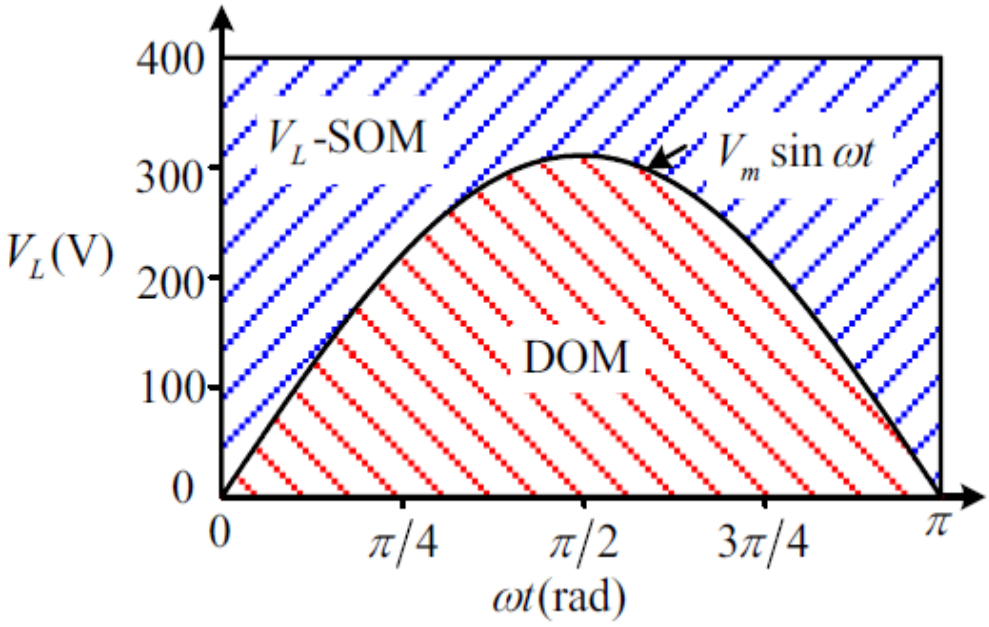


Figure 2.9 Operation Region of V_{Lo}-SM and DOM.

As per the Output power of V_{Lo} and V_{Hi} ports, there might be numerous sorts of power dissemination strategies to decide the activity modes fifty-fifty time of the grid voltage. Considering $V_{Lo} \leq V_{Hi}$, so as to decreases switching losses, the V_{Lo}-SM is favored when the stage point fulfills $0 \leq \omega t \leq \arcsin V_{Lo}/V_M$ and $\pi - \arcsin V_{Lo}/V_M \leq \omega t \leq \pi$, while the DM is favored when the stage edge fulfill $\arcsin V_{Lo}/V_M \leq \omega t \leq \pi - \arcsin V_{Lo}/V_M$. The V_{Hi} -SM is the last decision to fulfill the Output power necessity of the V_{Hi} port. The optimized mode determination plot is represented in Fig. 2.10, where θ_L speaks to the phase angle in which the DV-rectifier works in the V_{Lo}-SM and DM to fulfill the Output power necessity of the V_{Lo} port.

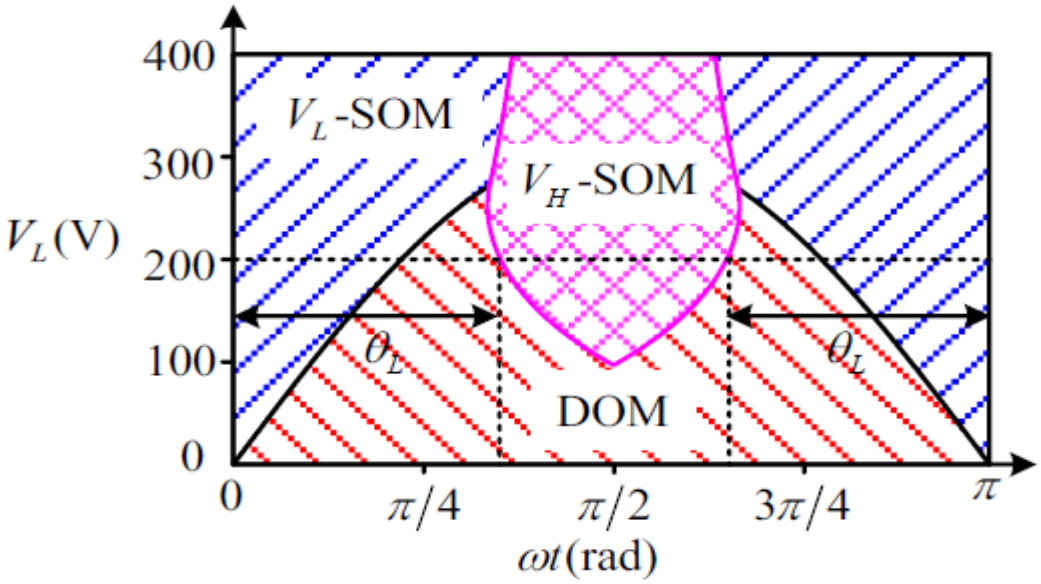


Figure 2.10 Optimized Scheme of Mode Selection.

2.11 Relationship Between the Power Ratio and Phase Angle θ_L

According to condition shown in Fig. 2.10, the input power will be delivered to the V_{Lo} port only in the range of $0 \leq \omega t \leq \theta_L$. Hence, the value of θ_L defines the power transferred to the V_{Lo} port or power ratio between the V_{Lo} and V_{Hi} port. The input ac voltage and Current will be expressed as:

$$v_{ac} = V_M sin\omega t \quad \textbf{2.5}$$

$$i_{ac} = I_M sin\omega t \quad \textbf{2.6}$$

where V_M and Im are the maximum (peak) amplitude of the input voltage and Current, respectively. The input power is calculated as:

$$\boldsymbol{p_{ac} = v_{ac} i_{ac} = \frac{V_M I_M}{2}(1 - cos2\omega t) = P_{OUT}(1 - cos2\omega t)} \quad \textbf{2.7}$$

The average input power $P_{average}$ is:

$$P_{average} = P_{OUT} = \frac{V_M I_M}{2} \quad \textbf{2.8}$$

The input power can be provided to the V_{Lo} port only when the DV-rectifier works in the V_{Lo}-SM and DM. As appeared in Fig. 2.7, all the input power is provided to the

V_{Lo} port when the DV-rectifier works in the V_{Lo}-SM. In this way, the prompt power pL_V_{Lo}-SM:

$$p_{LOW-V_{LO-SM}} = p_{ac} = \frac{V_M I_M}{2}(1 - cos2\omega t) \quad \textbf{2.9}$$

Nevertheless, when the DV-rectifier works in the DM, input power is sustained to the V_{Low} port just when S_2 is ON. In this manner, the instantaneous power provided to the V_{Low} port is determined as:

$$p_{LO-DM} = I_M sin\omega t \cdot d_2 \cdot V_{Lo} = I_M sin\omega t \cdot \frac{V_{HIGH} - v_{in}}{V_{HIGH} V_{Lo}} \cdot V_{Lo} \quad \textbf{2.10}$$

The rectifier will work in the DM only when the phase angle will be θ_L>arcsinV_{Low} /V_M. Therefore, the average power delivered to the V_{Low} port is calculated as:

$$P_{Lo} = \quad \textbf{2.11}$$

$$\begin{Bmatrix} \frac{2}{\pi}\int_0^{arcsin\frac{V_L}{V_M}} p_{LOW_{V_{LOW}-SM}} d\omega t + \frac{2}{\pi}\int_{arcsin\frac{V_{LOW}}{V_M}}^{\theta_{LOW}} p_{LOW_{mode2}}\, d\omega t & \theta_{LOW} \geq arcsin\frac{V_{LOW}}{V_M} \\ \frac{2}{\pi}\int_0^{\theta_{LOW}} p_{LOW\_V_L-SM} d\,\omega t & \theta_{LOW} < \arcsin\frac{V_L}{V_{ML}} \end{Bmatrix}$$

Hence, the power ratio between the V_{Lo} and V_{Hi} port can be extracted as:

$$k_{pow} = \frac{P_L}{P_H} = \begin{cases} \dfrac{V_L V_m \sin 2\theta_L - 2V_L V_m \theta_L - 4V_H V_L \cos\theta_L + 2V_H V_L\sqrt{1-\frac{V_L^2}{V_m^2}} + 2V_H V_m \arcsin\frac{V_L}{V_m}}{\pi V_m (V_H - V_L) - V_L V_m \sin 2\theta_L - 2V_L V_m \theta_L - 4V_H V_L \cos\theta_L + 2V_H V_L\sqrt{1-\frac{V_L^2}{V_m^2}} + 2V_H V_m \arcsin\frac{V_L}{V_m}} & \theta_L \geq \arcsin\frac{V_L}{V_m} \\ \dfrac{2\theta_L - \sin 2\theta_L}{\pi - 2\theta_L + \sin 2\theta_L} & \theta_L < \arcsin\frac{V_L}{V_m} \end{cases}$$

2.12

k_{power} is an element of both the phase angle θ_L and voltages V_{Lo}, V_{Hi} and V_M. Fig. 2.11 demonstrates the bends of k_{power} when vac=220VAC and V_{Hi} =400V as for θ_L and sin(θ_L), separately. As appeared in Fig. 11(a), k_{power} increments monotonically with the expanding of stage point θ_L. As appeared in Fig. 2.11(b), k_{power} and sin(θ_L) pursues a similar relationship too. Both θ_L and sin(θ_L) can be utilized as a controlling

factor to Regulate the power proportion between the V_{Low} and V_{Hi} ports. Practically speaking, utilizing sin(θ_L) as a control variable will be a lot simpler in light of the fact that the data of sin(θ_L) has been incorporated into the input voltage vac.

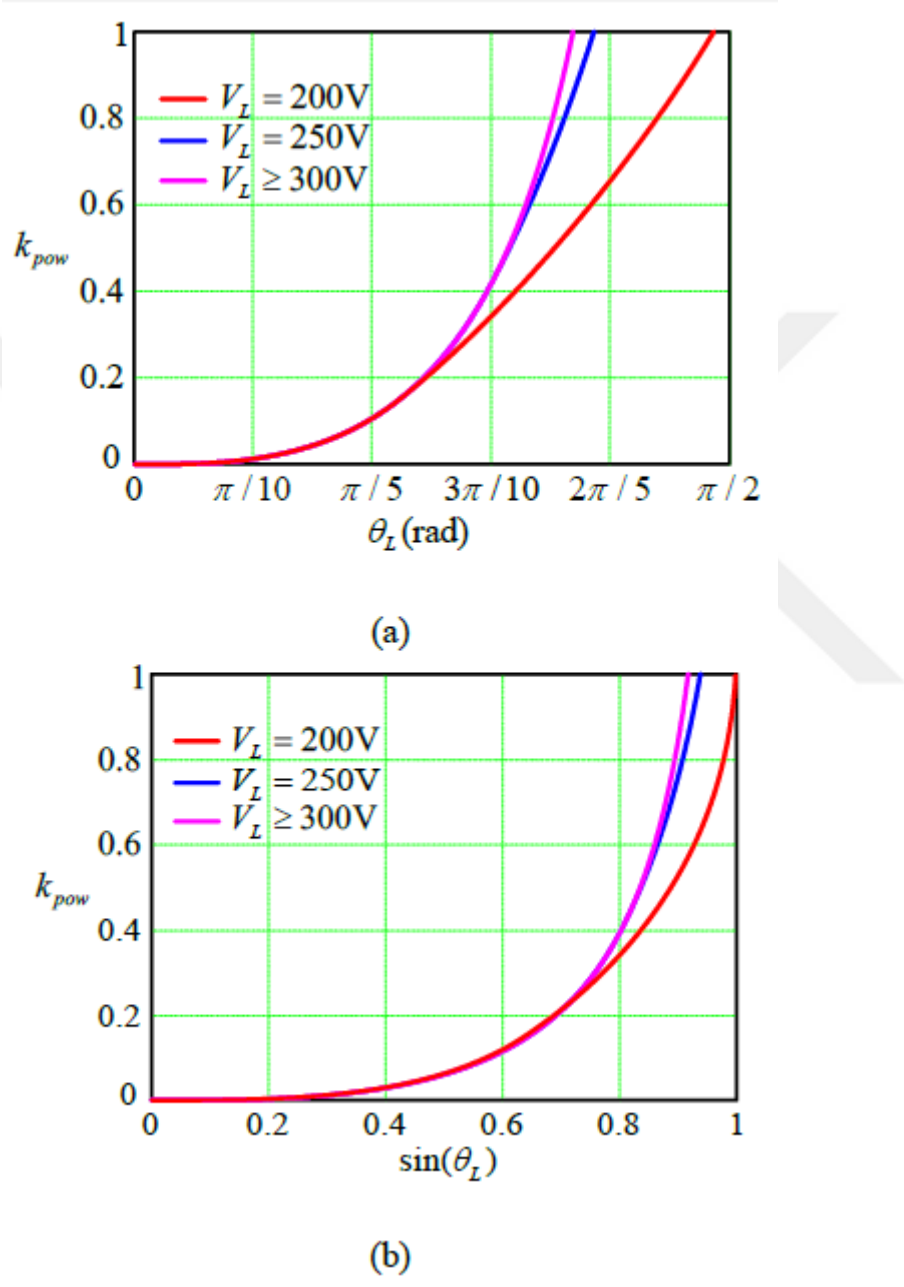


Figure 2.11 Curves of $k_{pow}$with respect to (a) θL and (b) sin(θL).

Assuming the DC to DC transformers are unit gain, since the two Outputs of DC to DC transformers in the proposed converter are associated in arrangement, control

proportion k_{power} is likewise equivalent to the voltage proportion kvolt among V_{Lo} and V_{Hi}

$$k_{power}(\theta_L) = k_{volt} = \frac{V_{Lo}}{V_{HIGH}} \quad \textbf{2.13}$$

As indicated by 2.12 and 2.13, the arrangement of phase angle θ_L_solu comparing to certain V_{Low}, V_{Hi} and V_M can be explained. Fig. 2.12 demonstrates the bends of θ_L_solu and sin(θ_L_solu) as for various estimation of V_{Low} when vac=220VAC and V_{Hi} =400V, in which three task areas are incorporated. As appeared in Fig.2.12(a), when V_{Lo} <$V_{Lo\,min}$, there is no accessible arrangement of θ_L for a given estimation of V_{Low} which implies the dual voltage rectifier can't work regularly in area 1. It is on the grounds that the power provided to V_{Lo} port can't fulfill the necessity of the DC to DC transformer. Whenever V_{Lo} min≤V_{Lo} <V_{Lo} criti, the DV-rectifier works in area 2, in which θ_L_solu is bigger than θ_{Lo}_SM. θ_{Lo}_SM is the limit phase angle among the V_{Low} -SM and DM and can be determined as:

$$\theta_{L-SM} = \begin{cases} arcsin\dfrac{V_{Lo}}{V_{Hi}} & V_{Lo} \le V_M \\ \dfrac{\pi}{2} & V_{Lo} > V_M \end{cases} \quad \textbf{2.14}$$

Since θ_L_solu>θ_L_SM in area 2, both V_{Low} -SM and DM are utilized to fulfill the power necessity of the V_{Low} port. All the more explicitly, the activity phase angle scope of DM in the half period time of the line voltage is 2(θ_L_solu-θ_L_SM). in the end, when V_{Lo} ≥V_{Lo} criti, the dual voltage rectifier works in segment 3, in which θ_L_solu<θ_L_SM. It implies the converter just works in V_{Lo}-SM to supply capacity to the V_{Lo} port. A similar end can be acquired from Fig. 2.12(b), where sin(θ_L_SM) is determined as:

$$\sin(\theta_{Lo-SM}) = \begin{cases} \dfrac{V_{Lo}}{V_M} & V_{Lo} \le V_M \\ 1 & V_{Lo} > V_M \end{cases} \quad \textbf{2.15}$$

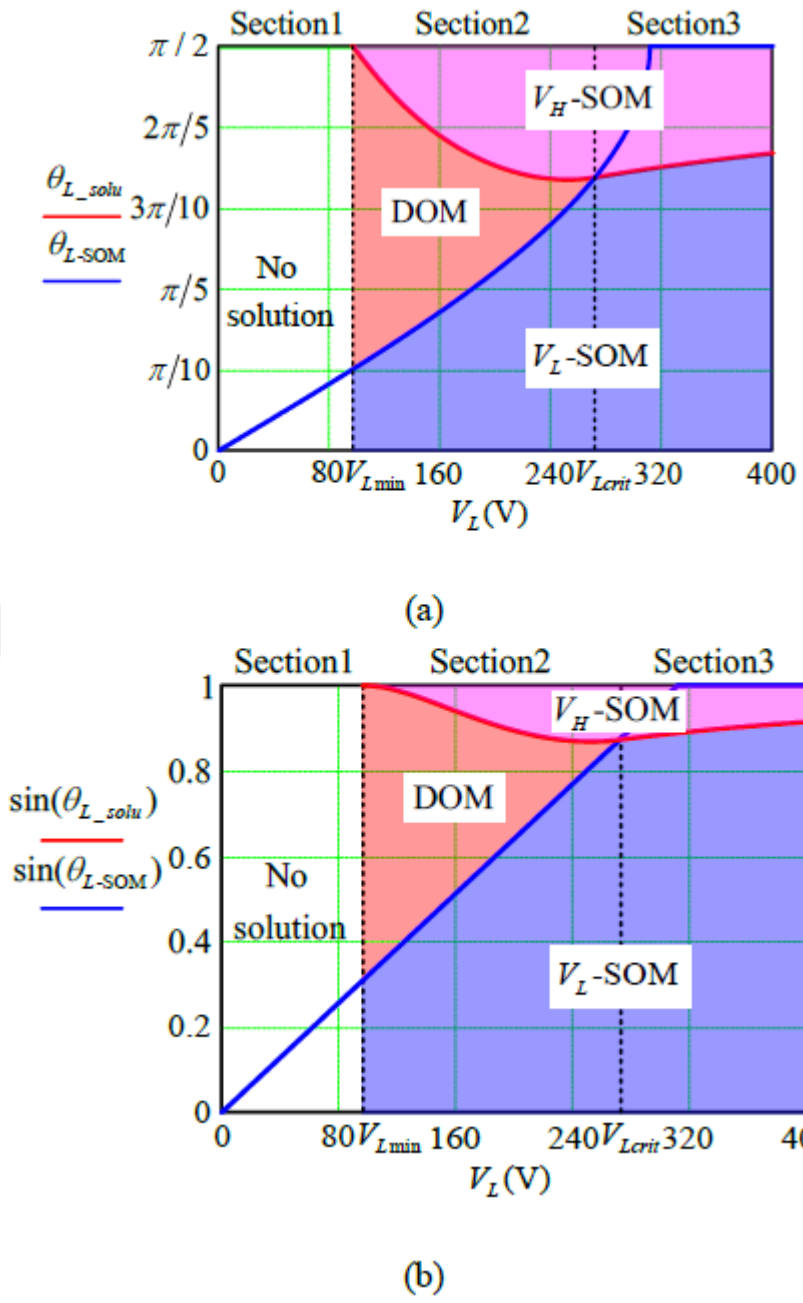


Figure 2.12 Curves of θ_{L_solu} and sin(θ_{L_solu}) with respect V_L, (a) curves of θ_{L_solu} and (b) curves of sin(θ_{L_solu}).

As given in Fig. 2.11, k_{power} increases as with the increase of θ_L. When θ_L=π/2, the DV-rectifier will only work in V_{Lo}-SM and DM, and the power supplied to the V_{Low} port is maximized. According to 2.12, the maximum normalized power of V_{Lo} port will be given as:

$$\lambda_{max} = \frac{P_{L\,max}}{P_{average}} = \frac{k_{power}(\theta_L)}{k_{power}(\theta_L)+1}\Big|_{\theta_L=\frac{\pi}{2}} \quad \textbf{2.16}$$

$$= \mathbf{1} - \frac{\boldsymbol{V_{Hi}}}{\boldsymbol{V_{Hi}} - \boldsymbol{V_{Lo}}}\left[\frac{\mathbf{1}}{\boldsymbol{\pi}}\left(\boldsymbol{\pi} - \mathbf{2}\boldsymbol{arcsin}\frac{\boldsymbol{V_{Lo}}}{\boldsymbol{V_M}}\right) - \frac{\mathbf{2}\boldsymbol{V_{Lo}}}{\boldsymbol{\pi}\boldsymbol{V_M}}\mathbf{cos}\left(\boldsymbol{arcsin}\frac{\boldsymbol{V_{Lo}}}{\boldsymbol{V_M}}\right)\right] \quad \textbf{2.17}$$

Clearly, λ_{max} is a component of V_M, V_{Lo} and V_{Hi}. Then again, to work the converter ordinarily, the standardized power ratio of V_{Lo} port is determined as:

$$\lambda_L = \frac{V_{Lo}}{V_{Lo} + V_{HIGH}} \quad \textbf{2.18}$$

For the proposed converter, $\lambda_{max} \geq \lambda_L$ ought to be fulfilled, generally the power required by the V_{Lo} port can't be fulfilled. Fig. 2.13 demonstrates the bends of λ_{max} and λ_L concerning the voltage V_{Lo}. Clearly, the operation scope of the V_{Lo} port ought to be over the compact line of λ_L. The intersection focuses between the compact and dashed lines defines to min. V_{Lo} voltage with a specific line voltage. It is seen that the base accessible voltage of V_{Lo} diminishes with diminishing of AC grid voltage.

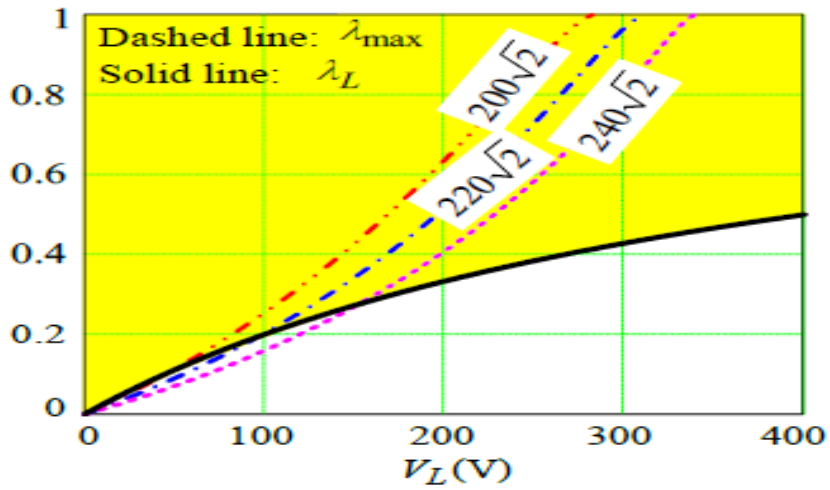


Figure 2.13 Curve of the Maximum Power Ratio λ_{max} and λ_L Versus the Voltage V_{Lo}.

3 CONTROL SCHEME

3.1 PWM Control Strategy

Fig. 3.1 demonstrates the control strategy block figure of the proposed AC to DC converter. The main rectifier oversees inward current controlling and the two DC-interface bus volt ctrl, while the down-stream DC to DC transformer is utilized to Regulate the heap voltage, Current or power control. As appeared in Fig. 3.1 a voltage control circle and a Current control circle are utilized for the DC to DC transformer, so consistent voltage and steady Current Output can be accomplished. As indicated by the examination over, the DC-interface voltage V_{Hi} is steady while the DC voltage V_{Lo} is movable to coordinate the DC Output voltage, with the goal that the DC to DC transformers can generally works close to their maximum frequency to accomplish high efficiency. To accomplish this, the voltage reference of V_{Lo} and V_{Hi} ought to fulfill:

$$(V_{HIGH-REF} + V_{LOW-REF}) \cdot G_{DC-DC} = V_{OUT} \qquad \textbf{3.1}$$

The operation frequency of the two DC to DC transformers, f_{DC-DC}, is dependably the equivalent. Accordingly, just a single controller and one frequency modulator (PFM) are required for the two DC to DC transformers, which can streamline the usage of control. It ought to be noticed that, when the switching frequency of the two DC to DC transformers is the equivalent, the low recurrence swells on V_{Hi} and V_{Lo} will influence the Output voltage swell of each DC to DC transformer, however the complete Output voltage V_o can, in any case, be Regulated to stifle the low frequency voltage swell by somewhat changing the addition G_{DC-DC} of the two DC to DC transformers at the same time.

As appeared in Fig. 3.1, two voltage Regulators are utilized to Regulate the two DC-bus voltages V_{Lo} and V_{Hi}, individually. Since both the Output intensity of V_{Lo} and V_{Hi} ports decide the prerequisite of info control all the while, the aggregate of the Outputs of the two voltage Regulators, v_{mLow} and v_{mHi}, are utilized to create the reference i_{Ref} of AC input Current. Agreeing the control loops of the power factor level, the

reference of AC input Current is acquired by duplicating sampled voltage and the Output of DC-bus voltage regulators. Accordingly, v_{mLow} and v_{mHi} shows to the normal Output intensity of V_{Low} and V_{Hi} ports, individually. Subsequently, the power proportion k_{power} can be shown to by vmL/vmH. Likewise, as appeared in Fig. 2.11, approximated straight connection between the power proportion k_{power} and sin(θ_L) is seen when k_{power}>0.5. In this manner, as appeared in Fig. 3.1, another control variable, v_{kp}, is determined utilizing vmL and vmH to decide the comparing sin(θ_L) required by the Output intensity of V_{Lo} and V_{Hi} ports:

$$v_{kp} = \frac{v_{mLo}}{v_{mHi}} \qquad \textbf{3.2}$$

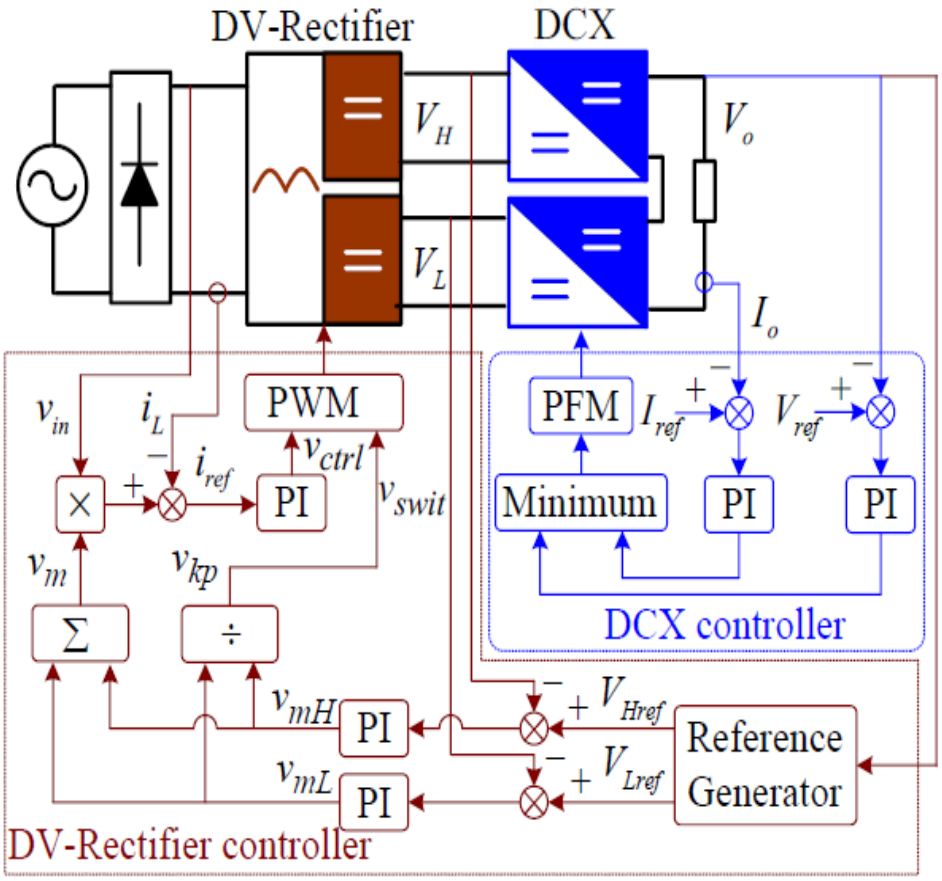


Figure 3.1 Control Block Diagram of Proposed DV-Converter.

As examined over, the control structure of the proposed converter is like that for a traditional two-stage AC to DC converter [20], the main contrast is that two voltage

control connections are expected to Regulate V_{Low} and V_{Hi} for the dual voltage rectifier. By and by, the control loop structure of the DC to DC stage and PFC level is autonomous on one another. For the most part, the voltage loop transfer speed of the PFC stage ought to be lower than the freq. of input voltage to evade the unsettling influence of voltage swells on DC interface voltage bus, the Current loop data transmission of the PFC stage ought to be a lot higher than the freq. of input voltage to accomplish high power factor of input Current. The control data transfer capacity of the DC to DC stage is dictated by the necessity of the DC Output port and typically a lot higher than the voltage circle transmission capacity of the PFC level.

3.2 Pulse Width Modulation (PWM) Technique & Smooth Mode Transition Based on Voltage-Second Balance Principle of Inductor

As indicated by the optimized mode choice appeared in Fig. 2.10, the DV-rectifier works in the V_{Hi}-SM just when the phase angle is in θ_L~(π-θ_L). Something else, the DV-rectifier should work in V_{Lo}-SM or DM. Pulse width modulation methodology is the way to ensure the rectifier work in the advanced mode and switch between various modes easily and unreservedly. The key waveforms of PWM methodology for the proposed rectifier are delineated in Fig. 3.2, where Fig. 3.2(a) represents the case with mode exchanging between V_{Lo}-SM and V_{Hi}-SM, while Fig. 3.3(b) demonstrates the case with mode exchanging among DM and V_{Hi}-SM.

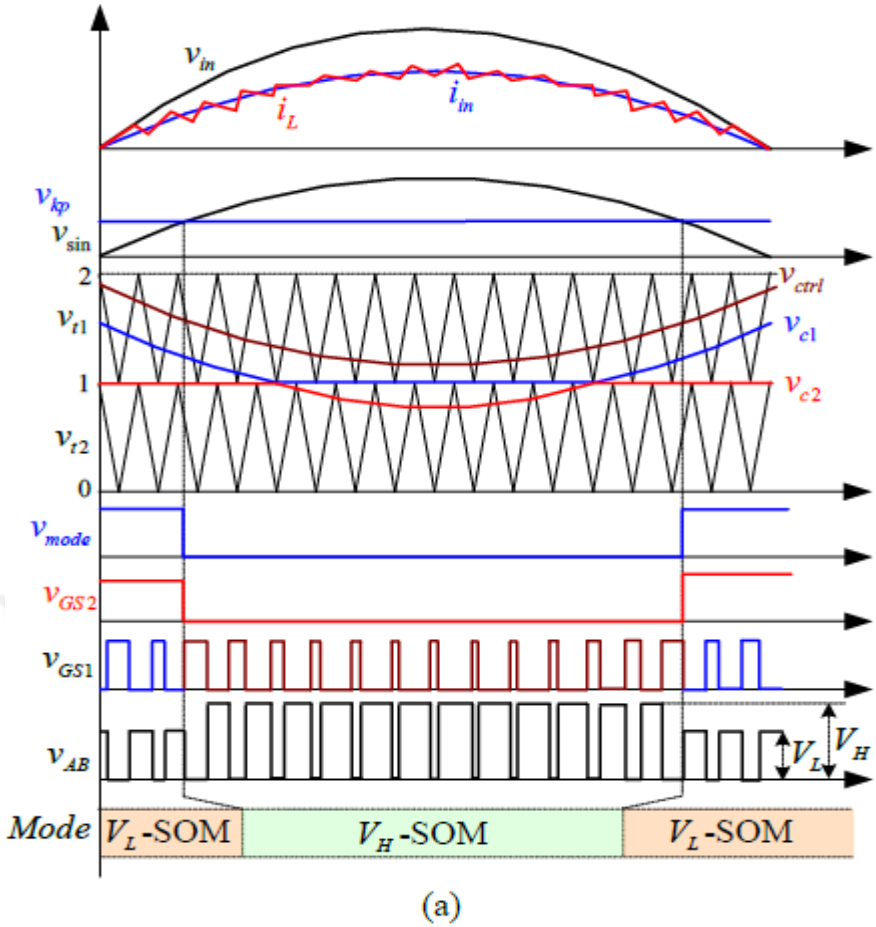
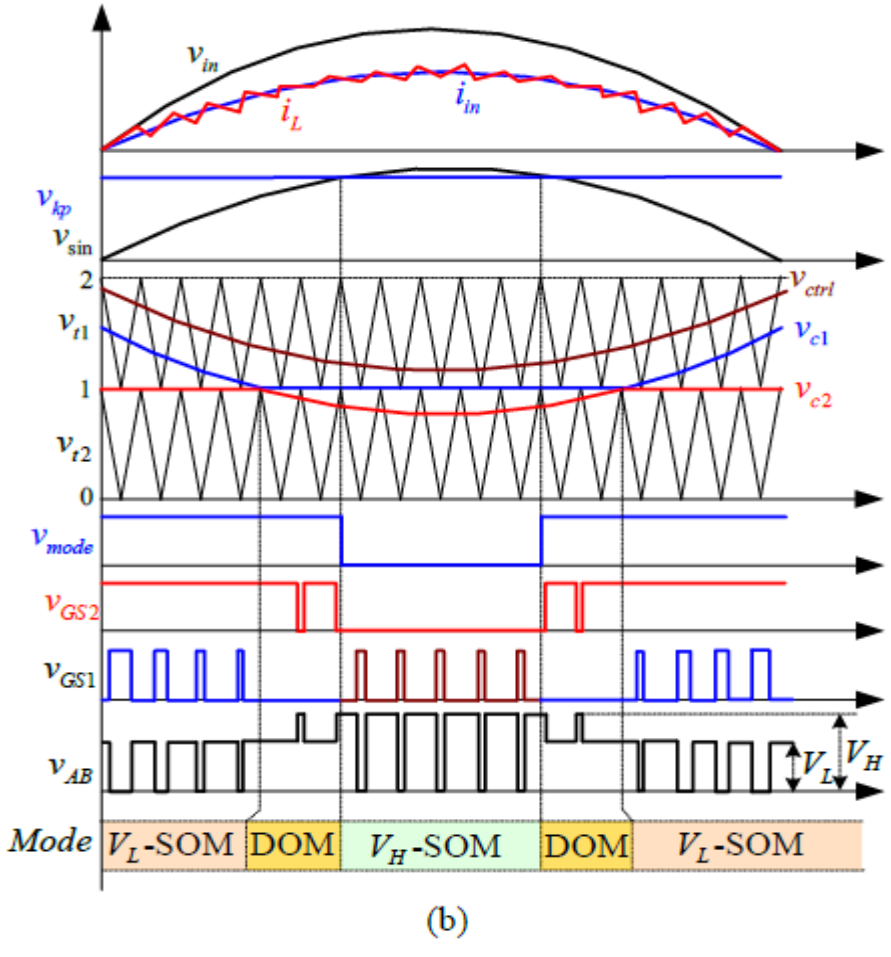


Figure 3.2 Key Waveforms of the PWM Strategy with (a) Mode Switching Between V_L-SOM and V_H-SOM.

As appeared in Fig. 3.2 and 3.3, the mode exchanging signal v_{mode} is created by contrasting v_{kp} and a standard sinusoidal waveform v_{sin}, whose shape is equivalent to the input voltage v_{in} of the rectifier. Three control signals, v_{ctrl}, v_{c1} and v_{c2}, are utilized to create the Pulse width modulation signs of switches S_1 and S_2. Among the three control signals, v_{ctrl} is the Output of the input Current Regulator of the rectifier and legitimately utilized as the control flag of V_{Hi}-SM, while v_{c1} and v_{c2} are acquired dependent on v_{ctrl} and utilized as the control flag of V_{Low}-SM and DM, separately. Double carrier based PWM methodology, which is like the PWM procedure of a three-level Boost converter, is utilized. As appeared in Fig. 15, the lower and higher carrier v_{t1} are 0 and 1, while the valley and pinnacle estimations of bearer v_{t2} are 1 and 2. The signal of S_1, v_{GS1}, is produced by contrasting v_{t1} and v_{ctrl} or v_{c1}, contingent upon the task method of the rectifier, and the door flag of S_2, v_{GS2}, is created by contrasting v_{t2} and v_{c2}.

As appeared in Fig. 3.2 and 3.3, it is seen that the conversion between the V_{Lo}-SM and DM happens normally and easily with the double carrier based PWM technique. In any case, to convey input control among V_{Low} and V_{Hi} ports, mode exchanging between V_{Lo}-SM and V_{Hi}-SM, or among DM and V_{Hi}-SM is controlled by the mode exchanging signal v_{mode}. At the point when mode swapping between V_{Lo}-SM and V_{Hi}-SM, the duty cycle of S_1 will be changed all of a sudden, and when mode exchanging among DM and V_{Hi} -SM, the high frequency switch will be changed from S_1 to S_2 or from S_2 to S_1. To accomplish smooth mode conversion, a fundamental measure is that the voltage-second parity of the inductor L in the rectifier ought to dependably be fulfilled when any mode swapping at any interval, with the goal that the inductor current won't be bothered by any mode transferring.



(b)

Figure 3.3(b) Mode Switching Between DOM and VH-SOM.

As indicated by the task standards and block diagram of the DV-rectifier appeared in Fig. 2.5, the proportional circuit of the proposed DV-rectifier in one exchanging cycle

appears in Fig. 3.4, the exchanging system made from S_1, S_2, D1 and D2 is improved to be a SPTT (Single- Pole Triple Throw, SPTT).

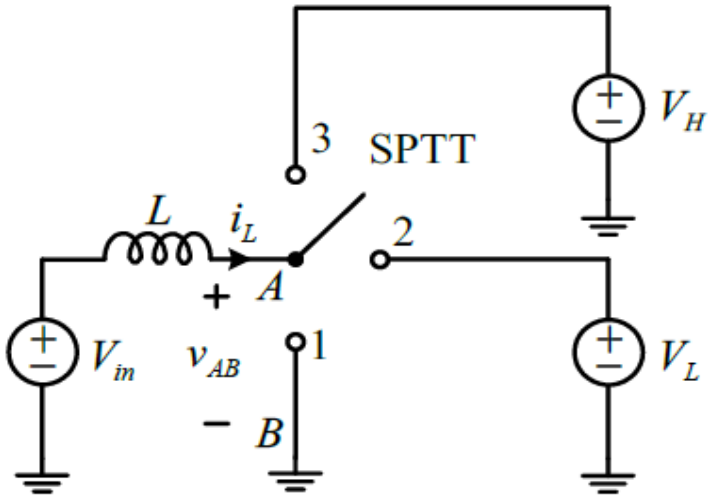


Figure 3.4 Equivalent Circuit of the DV-Rectifier in One Switching Cycle.

When the rectifier functions in the V_{Hi}-SM, the terminal 2 of the SPTT is restricted and the switch pole is associated to terminal 1 and terminal 3 alternatively. Hence, according to the waveforms of PWM strategy revealed in Fig.3.2 & 3.3, the connection between the control signal v_{ctrl} and the average value of vAB is as follows:

$$\bar{v}_{AB} = V_{Hi}\left(1 - d_{1_{VHi-SM}}\right) = V_{Hi}(2 - v_{ctrl}) \qquad \textbf{3.3}$$

where d1_V_{Hi}-SM is the duty cycle of S_1 in the V_{Hi}-SM. When the rectifier works in the V_{Lo}-SM, the terminal 3 of the SPTT is deactivated and the switch pole is connected to terminal 1 and terminal 2 otherwise. So, the relationship among the control signal v_{c1} and the usual value of v_{AB} is as follows:

$$\boldsymbol{\bar{v}_{AB} = V_{Lo}\left(1 - d_{1_{VLo-SM}}\right) = V_{Lo}(2 - v_{C1})} \qquad \textbf{3.4}$$

When the rectifier functions in the DM, the terminal-1 of the SPTT is disabled and the switch pole is connected to terminal-2 and terminal-3 alternatively. In this case, the relationship between the control signal v_{c2} and the average value of $\bar{v}_{AB}$ is as follows:

$$\bar{v}_{AB} = V_{Low} d_{2\_DM} + V_{Hi}\left(1 - d_{2_{DM}}\right) = V_{Low} v_{c2} + V_{Hi}(1 - v_{C1}) \qquad \textbf{3.5}$$

where d2_DM is the duty cycle of S_2 in the DM.

To achieve smooth mode transition among V_{Lo}-SM and V_{Hi}-SM, the average values of v_{AB} conforming to v_{ctrl} and v_{c1} must be constantly the same. Consequently, according to equations 3.3 and 3.4, the following equation is extracted:

$$v_{c1} = \frac{V_{Hi} v_{ctrl} - 2(V_{Hi} - V_{Low)}}{V_{Low}} \qquad \textbf{3.6}$$

In accumulation, as the minimum duty cycle of S_1 is 0, the minimum value of v_{c1} should be limited to 1, therefore

$$v_{c1} = max\left[1, \quad \frac{V_{Hi} v_{ctrl} - 2(V_{Hi} - V_{Low)}}{V_{Low}}\right] \qquad \textbf{3.7}$$

So also, the normal estimations of v_{AB} comparing to v_{ctrl} and v_{c2} ought to be the equivalent to accomplish smooth mode switching between V_{Hi}-SM and DM. Thusly, as per Equations 3.3 and 3.5, the accompanying condition is determined:

$$v_{c2} = \frac{V_{Hi}(v_{ctrl} - 1)}{V_{Hi} - V_{Low}} \qquad \textbf{3.8}$$

In calculation, since the maximum duty cycle of S_2 is 1, the maximum value of v_{c1} should be limited to 1, therefore:

$$v_{c2} = min\left[1, \quad \frac{V_{Hi}(v_{ctrl} - 1)}{V_{Hi} - V_{Low}}\right] \qquad \textbf{3.9}$$

3.3 Comparative Analysis

To help configuration exchange off in designing applications, the examination between the proposed arrangement and different arrangements is essential. Since the proposed arrangement is essentially a dual-stage AC to DC converter with variable DC-connect voltage, the arrangements proposed in [20], [21] and a regular two-organize arrangement with steady DC-interface voltage [4] are chosen for correlation

because of the comparability in structure and applications. Table 3.1 outlines the discoveries from this examination.

Table 3.1

Comparison

	Constant voltage DC-link [4]	Variable voltage single DC-link [20]	Variable voltage single DC-link [21]	Proposed [24]
Optimized design of DC-DC stage	No	Yes	Yes	Yes
Required Voltage Regulation range of DC-DC stage	Wide	Very narrow	No Regulation	Very narrow
Total power rating of DC to DC stage	P_O	P_O	$2P_O$	P_O
Conduction losses and Current stresses and of DC to DC stage	Medium	Low	High	Low
DC-link capacitor	Electrolytic	Electrolytic	Film	Electrolytic
Capacitance of electrolytic capacitor on DC-link	Low	High	N/A	Medium

Maximum voltage of DC-link	Constant, Low	Variable, High	Variable, High	constant, low (V_{Hi}) variable, low (V)
Current of DC port	Smooth, DC	Smooth, DC	Pulse, Sinusoidal	Smooth, DC
Voltage stress of switches in the PFC stage	Low	High	High	Low
Number of power devices in the PFC stage	1 diode-rectifier 2 active switches 2 diodes	6 active switches	4 active switches	1 diode rectifier 2 active switches 2 diodes
Conducting Devices Numbers	3	2	2	3 or 4
Number of power devices in the DC-DC stage	4 active switches 4 diodes	6 active switches -	4 active switches -	8 active switches 8 diodes
Tested overall full-load efficiency	95%	96%	94%	96%

An ordinary two-level AC to DC converter [4] can give a steady DC-link voltage, commonly 400V for single-stage application. It is a lot simpler to choose control switches, diodes and electrolytic capacitors with a 400V DC-interface voltage. Luckily, this favorable position is acquired by the proposed arrangement. Although the proposed converter has two DC-connection, V_{Hi} and V_{Low}, the voltage of V_{Hi} is steady and can be intended to 400V for single-stage application, while the most extreme voltage of V_{Low} won't surpass V_{Hi}. In any case, for the arrangements in [20] and [21], the base voltage of DC-interface is restricted by the peak amp. of AC voltage, while the most extreme voltage of DC-bus is dictated by the voltage range of DC load.

In this manner, with a similar input and Output specs, the highest voltage of DC-interface in [20] and [21] will be a lot higher than the proposed arrangement and the conventional constant DC-connection arrangement. This will prompt a lot of higher voltage stresses of switching gadgets of both at the PFC level and the primary side of the DC to DC level [24]

A noteworthy favorable position of the arrangement in [21] is that the electrolytic capacitors on DC-connect are removed. Therefore, one punishment of wiped out electrolytic capacitor is the pulsed sinusoidal Current on DC side, which results in a lot of higher Current pressures and conduction losses at DC-DC level. Also, the power rating of the DC-DC stage ought to be 2x times of normal Output control Po. For the conventional DC-bus voltage arrangement, arrangement of [20] and the proposed one, electrolytic capacitors are required for the DC-connection to smooth the twice AC voltage frequency control throbbing on the DC-interface Busses. The mathematical procedure of the required DC-interface capacitance is the same. For the most part, the required DC-interface capacitors of the regular two-stage arrangement with steady DC-interface voltage are lower than the arrangements with variable DC interface voltage. For instance, the DC-interface capacitors involve 1/3 volume of the whole model in [20], on the grounds that the voltage worry of DC-connect capacitor is a lot higher than 400V and the voltage swell of the whole DC-interface voltage array must be taken into thought. For the proposed DV-rectifier with two DC Outputs, V_{Hi} with consistent voltage and V_{Low} with variable voltage, so as to accomplish a similar most extreme crest to-crest voltage swells inside the whole DC Output voltage extend, more DC-interface capacitance than a conventional DC-connect voltage PFC circuit will be required also, in any case, the voltage rating of the DC-interface capacitors for the proposed converter is as yet equivalent to the traditional consistent DC-interface voltage arrangement and much lower than that in [20].

In examination with past arrangements, the proposed DV-rectifier acts like a three-level converter, since the two voltages V_{Hi} and V_{Low} are unique and give two voltage levels to the rectifier[24]. The three-level trademark is useful for the decrease of swapping losses and advancement in efficiency. In any case, the DV-rectifier is unique in relation to an ordinary three-level converter, which can just give one DC Output. The down-stream DC-DC arrange can't be improved with an ordinary three-level

converter. This is a noteworthy improvement of the proposed DV-rectifier. Contrasted with the arrangements proposed in [20] and [21], a hindrance of the proposed DV-rectifier got from a customary Boost PFC is higher conduction misfortunes, since more gadgets are directing in each working moment of the DV-rectifier. In [20] and [21], the quantity of conducting gadgets at each working moment is decreased claiming the input diode bridge is wiped out. On the off chance that the bridgeless DV-rectifiers appeared in Fig. 2.3(b) and (c) are utilized, the conduction misfortunes of the DV-rectifiers can be decreased also.

In perspective on the DC-DC arrange, a noteworthy disadvantage of the proposed arrangement is that two DC-DC transformers with more gadgets are utilized. So, it is conceivable to disentangle the DC-DC stage by attaching half-bridge LLC or sharing the Output rectifier inside the two DC-DC transformers.

In perspective on change proficiency, 95% full-load proficient is accomplished in [4] with a customary two stage arrangement, 96% full-load effective is accomplished in [20] with a variable DC-connect voltage arrangement, while just 94% full-load productive is accomplished in [21] with an electrolytic capacitors variable DC-interface voltage arrangement. In spite of the fact that the PFC-phase of the proposed AC to DC converter has higher conduction losses, it will have shown in the next chapter that 96% full-load proficient is accomplished with the proposed arrangement, which checks the viability of the DV-rectifier-based AC to DC converter and voltage-sigma engineering.

The correlation and exchange off appeared Table I demonstrate that every arrangement has its points of interest and drawbacks. The proposed DV-rectifier-based AC to DC converter is a fantastic possibility for high proficiency Isolated AC to DC power conversion with variable DC Output voltage applications.

3.4 Fuzzy Logic Controller

Conventionally, PI, PD and PID controller are most popular controllers and widely used in most power electronic closed loop appliances however recently there are many researchers reported successfully adopted Fuzzy Logic Controller (FLC) to become one of intelligent controllers to their appliances [3].As of their effective method execution, control shut circle support converter and opened circle support converter

will think about the proficiency of the converters. This sort of strategy actualized in this paper is utilizing fluffy rationale controller with input by presentation of voltage yield individually. The presentation of voltage yield in the circuit will be encouraged to fluffy controller to give proper measure on unfaltering state signal. The fluffy rationale controller fills in as insightful controller for this propose. This philosophy can be effectively connected to numerous dc-dc converter topologies, for example, Buck, Boost and Buck-Boost.

Methodology:

In this part, we will discuss about the procedure that how a FLC works. Below figure shows the process of completing our circuit.

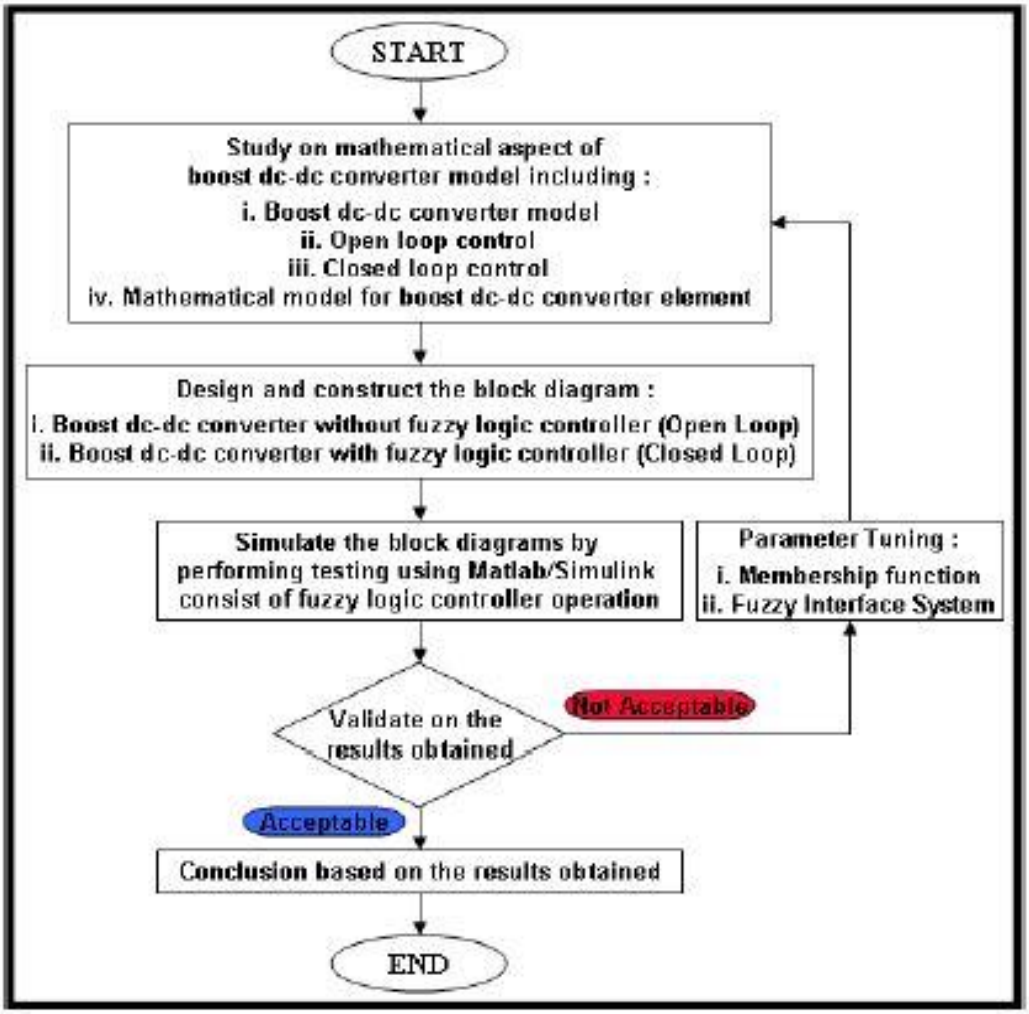


Figure 3.5 FLC Strategy

3.5 Fuzzy Logic Controller for Boost Converter

An investigation of lift converter circuit uncovered that the inductor current plays critical assignment in unique reaction of lift converter. Moreover, it can give the capacity vitality data in the converter. Therefore, any progressions on the inductor current may influence yield voltage and yield voltage will give relentless state condition data of converter. In any case, the three fundamental parameters should be viewed as when design boost converters are power switch, inductor and capacitor. In this objective to achieve the desired output voltage and the stability is by designing the power switch [25].

3.6 Analytical Expressions

There are few types of power switches in order to develop the design. The common power switches are BJT, power MOSFET, IGBT etc. Since the characteristics of the MOSFET are fast switching and voltage driven, they have been chosen for the power switching in this designing requirement. In this case, the parameters value of design requirement for the boost dc-dc converter is been set.

3.7 Fuzzy Logic Membership Function

The boost dc-dc converter is a nonlinear function of the duty cycle because of the small signal model and its control method was applied to the control of boost converters. Fuzzy controllers do not require an exact mathematical model. Instead, they are designed based on general knowledge of the plant. Fuzzy controllers are designed to adapt to varying operating points. Fuzzy Logic Controller is designed to control the output of boost dc-dc converter using Mamdani style fuzzy inference system. Two input variables, error (e) and change of error (ce) are used in this fuzzy logic system. The single output variable (u) is duty cycle of PWM output [26].

$$e(k) = Vref - V(k) \quad \textbf{3.10}$$

$$ce(k) = e(k) - e(k\text{-}1) \quad \textbf{3.11}$$

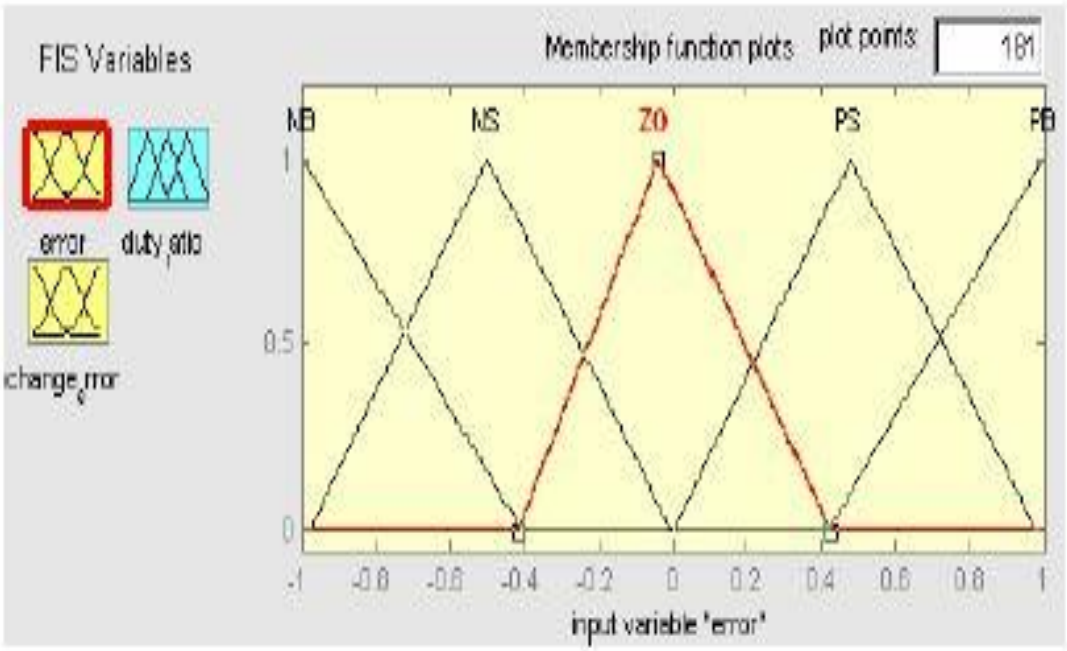


Figure 3.6 The Membership Functions Plot of Error

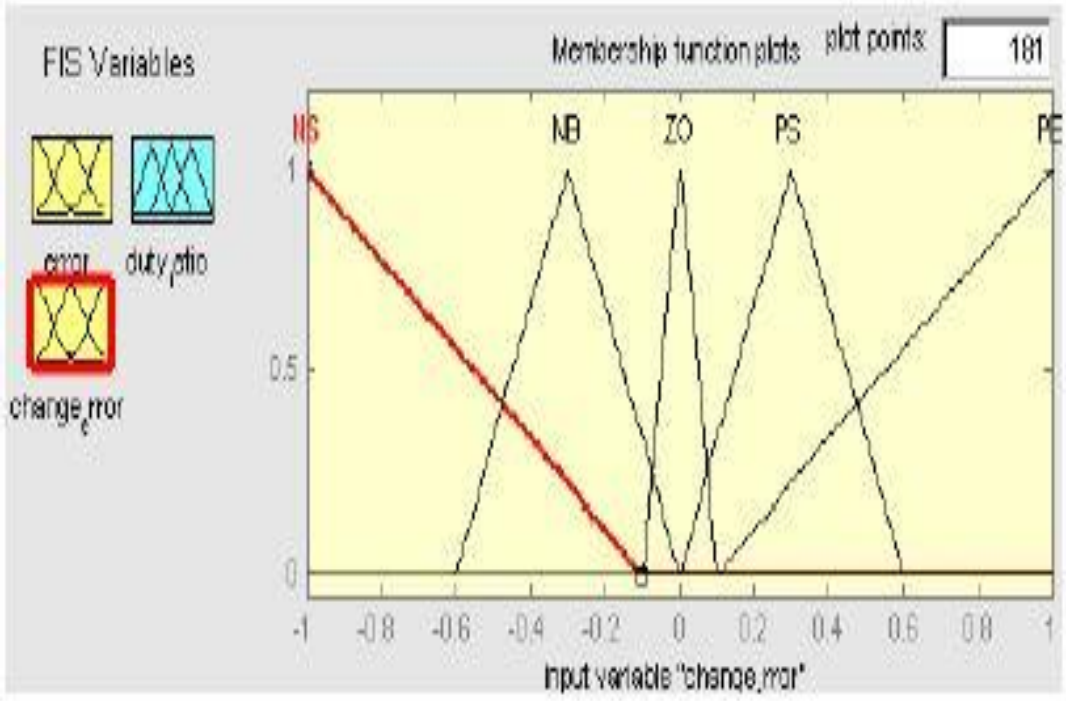


Figure 3.7 The Membership Function Plots of Change Error

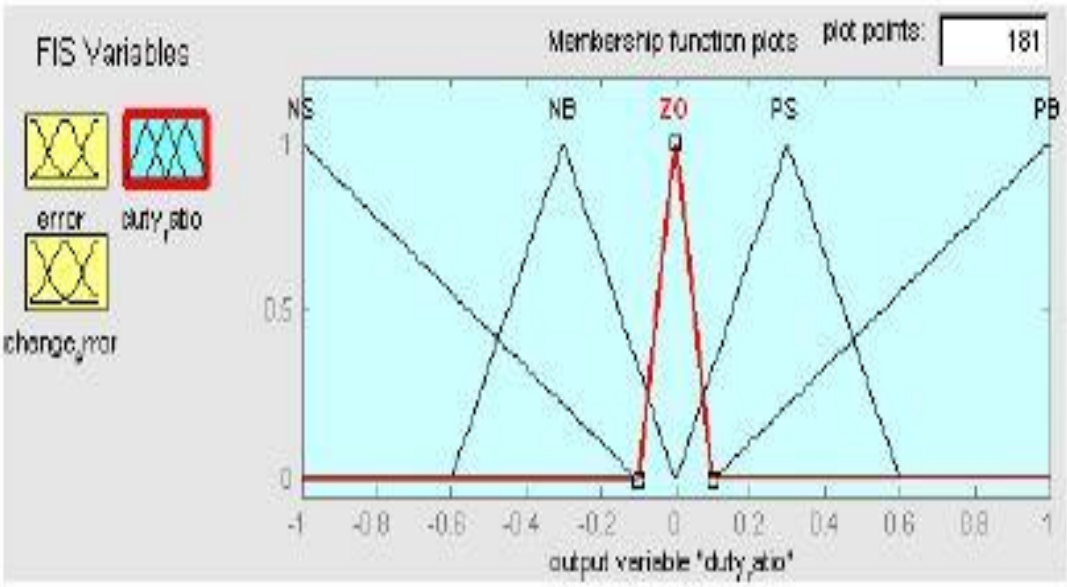


Figure 3.8 The Membership Function Plots of Duty Ratio

3.8 Fuzzy Logic Table Rules

The objective of this dissertation is to control the output voltage of the boost converter. The error and change of error of the output voltage will be the inputs of fuzzy logic controller. These 2 inputs are divided into five groups; NB: Negative Big, NS: Negative Small, ZO: Zero Area, PS: Positive small and PB: Positive Big and its parameter [27]–[29]. These fuzzy control rules for error and change of error can be referred in the table that is shown in Table 2 as per below:

Table 3.2

(de) \ (e)	NB	NS	ZO	PS	PB
NB	NB	NB	NB	NS	ZO
NS	NB	NB	NS	ZO	PS
ZO	NB	NS	ZO	PS	PB
PS	NS	ZO	PS	PB	PB
PB	ZO	PS	PB	PB	PB

4 EXPERIMENTAL RESULTS

4.1 Main Circuit

In this chapter we will discuss about our circuits, then controlling of these circuits and at the end we have shown each circuit output separately. Below shown figure 4.1 is of our complete main circuit.

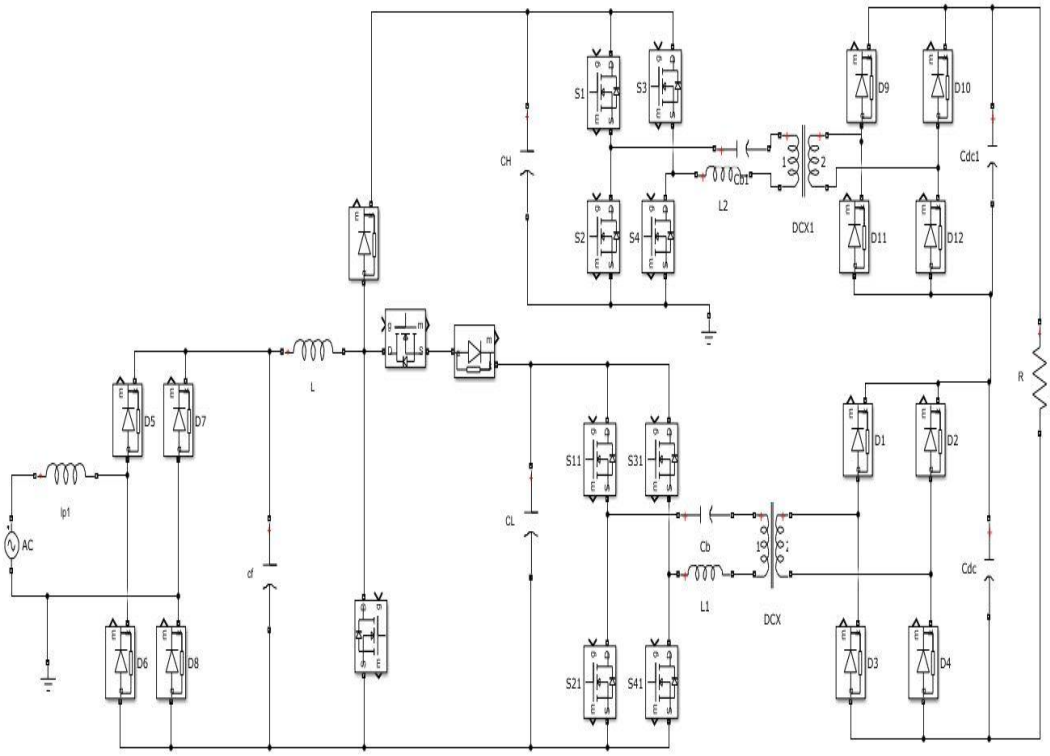


Figure 4.1 Complete Circuit Diagram Of DV-Rectifier

4.2 LLC Resonant Circuit & Control Circuit

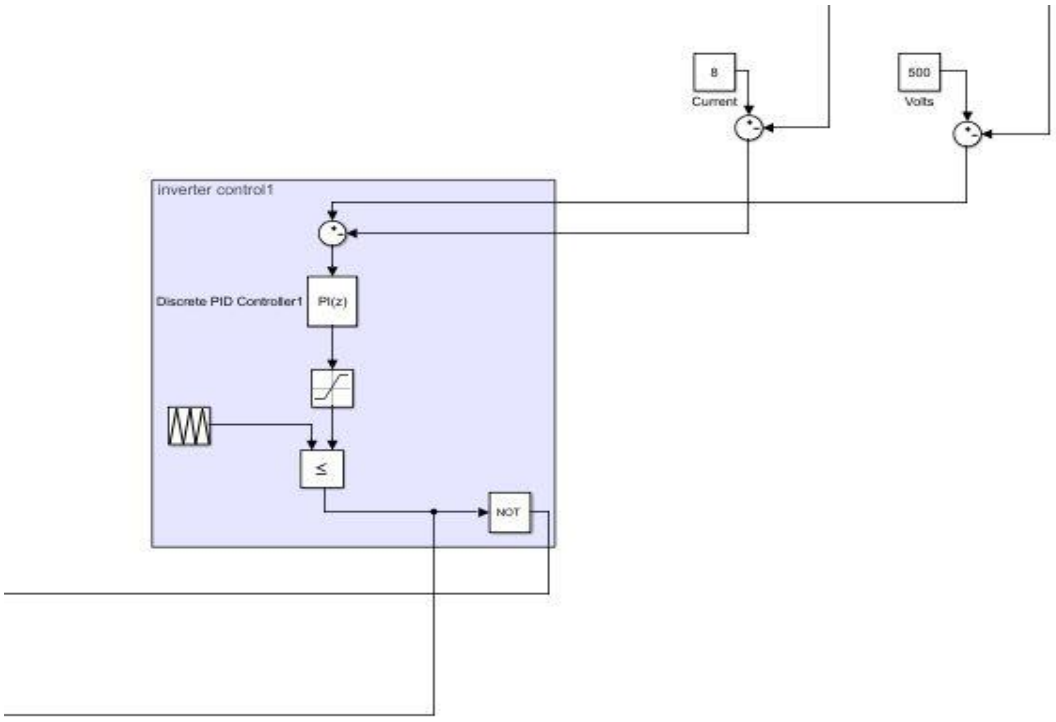


Figure 4.2 LLC Resonant Converter Control Strategy

4.3 PWM Controller

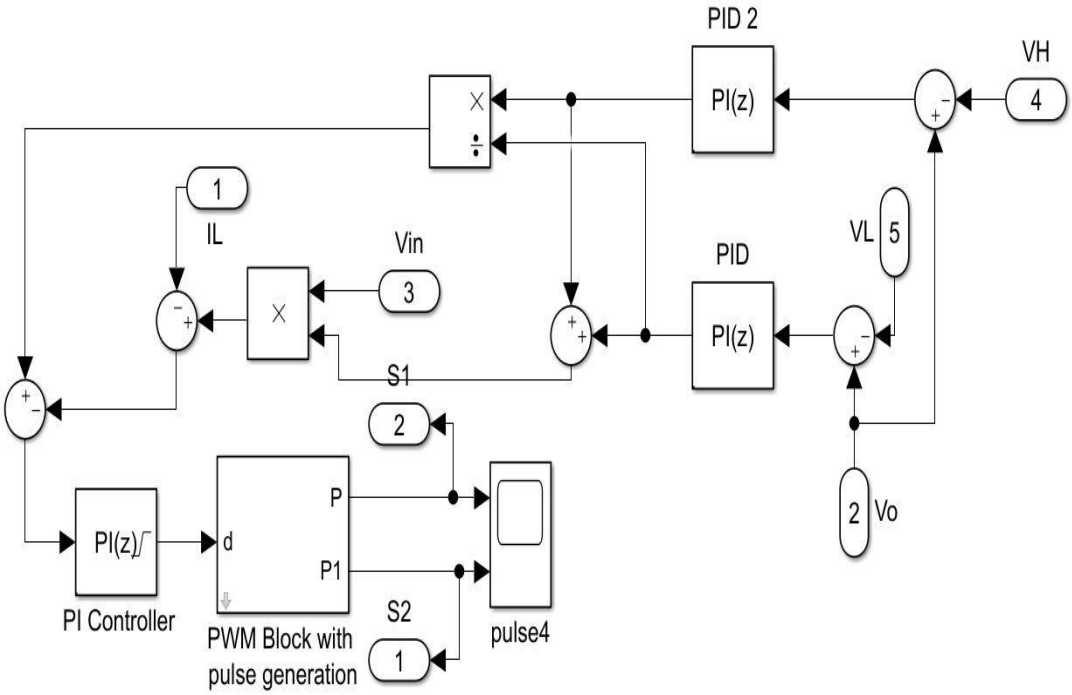


Figure 4.3 PWM Control Circuit for DV-Rectifier

4.3.1 Graphs

4.3.1.1 PWM Controlled DV-Rectifier Input Current and Voltage

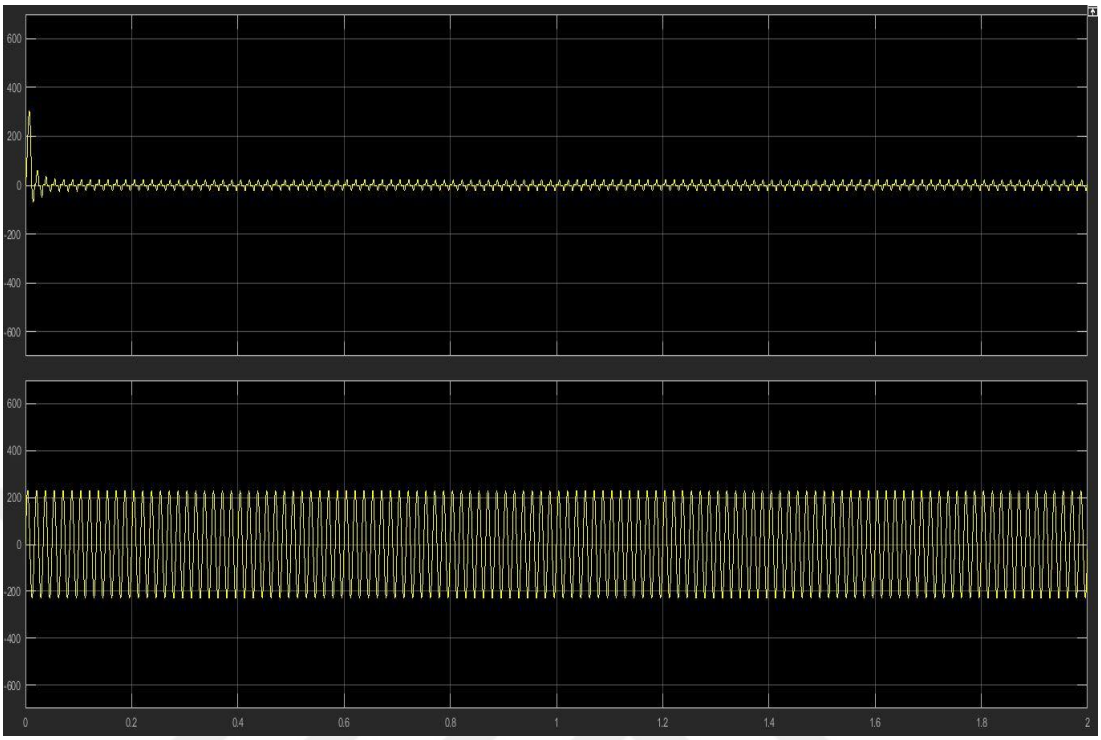


Figure 4.4 PWM Controlled DV-Rectifier Input Current and Voltage

4.3.1.2 Inductor Current

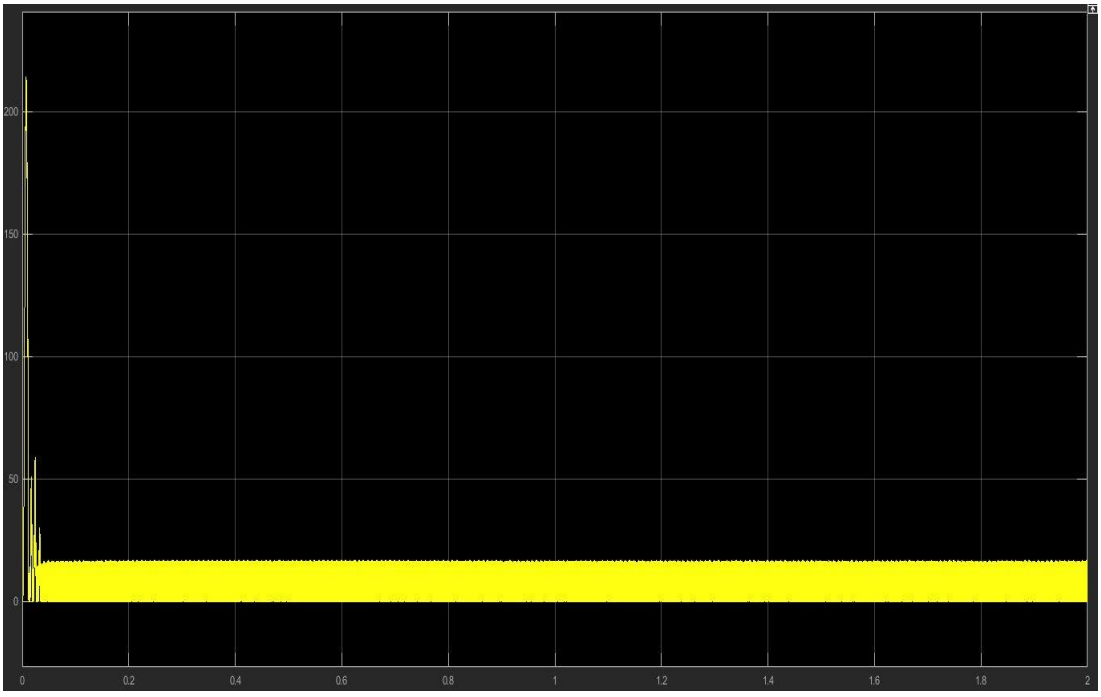


Figure 4.5 Inductor Current

4.3.1.3 Voltage Across Points A&B

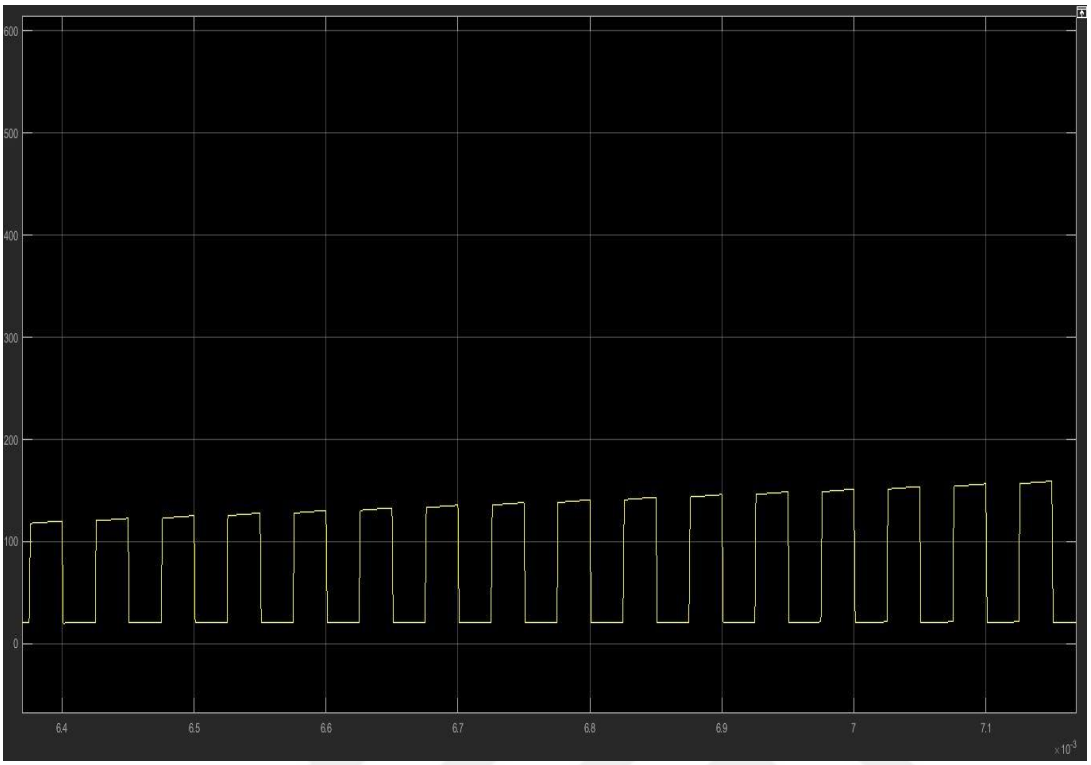


Figure 4.6 Voltage Across Points A & B

4.3.1.4 Voltage at Port V_{Hi} & V_{LO}

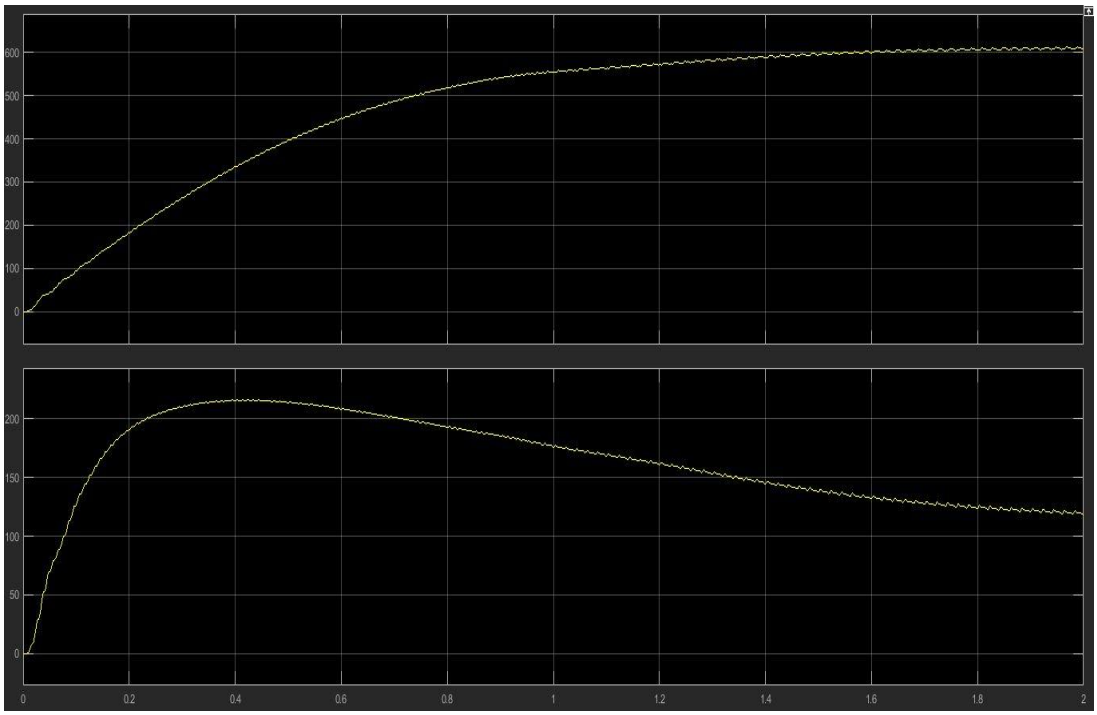


Figure 4.7 Voltage at Port V_{Hi} & V_{LO}

4.3.1.5 Output Current and Voltage Graph When Vin is 230V @ 60Hz and 50Hz Frequency

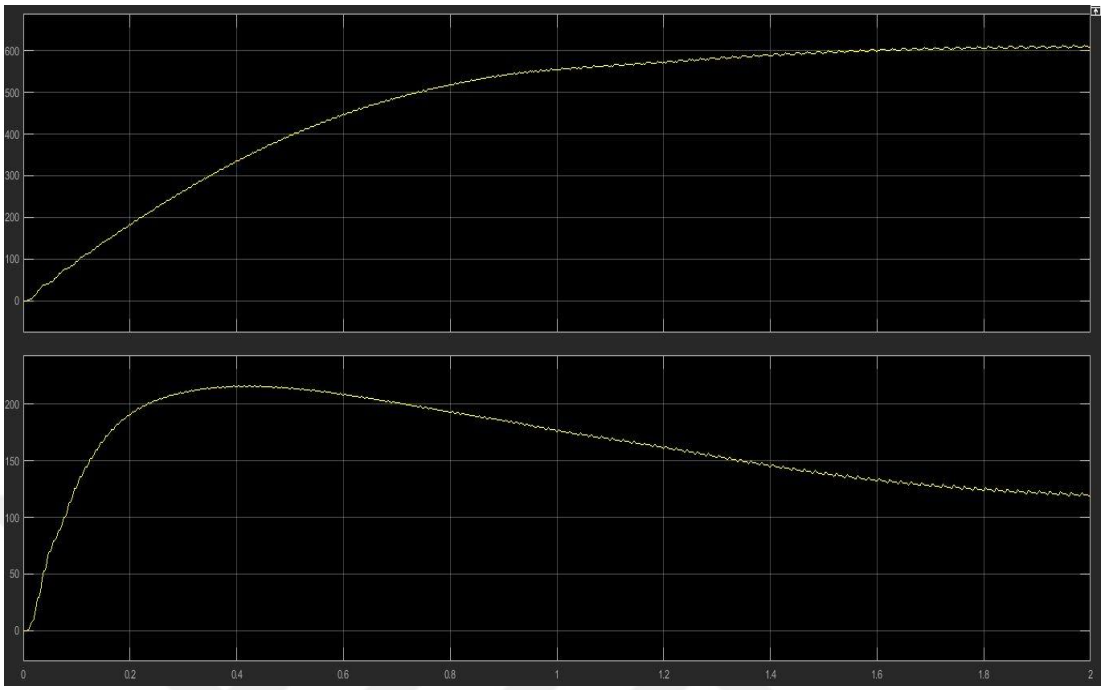


Figure 4.8 Output Current and Voltage Graph when Vin is 230V and 60Hz Frequency

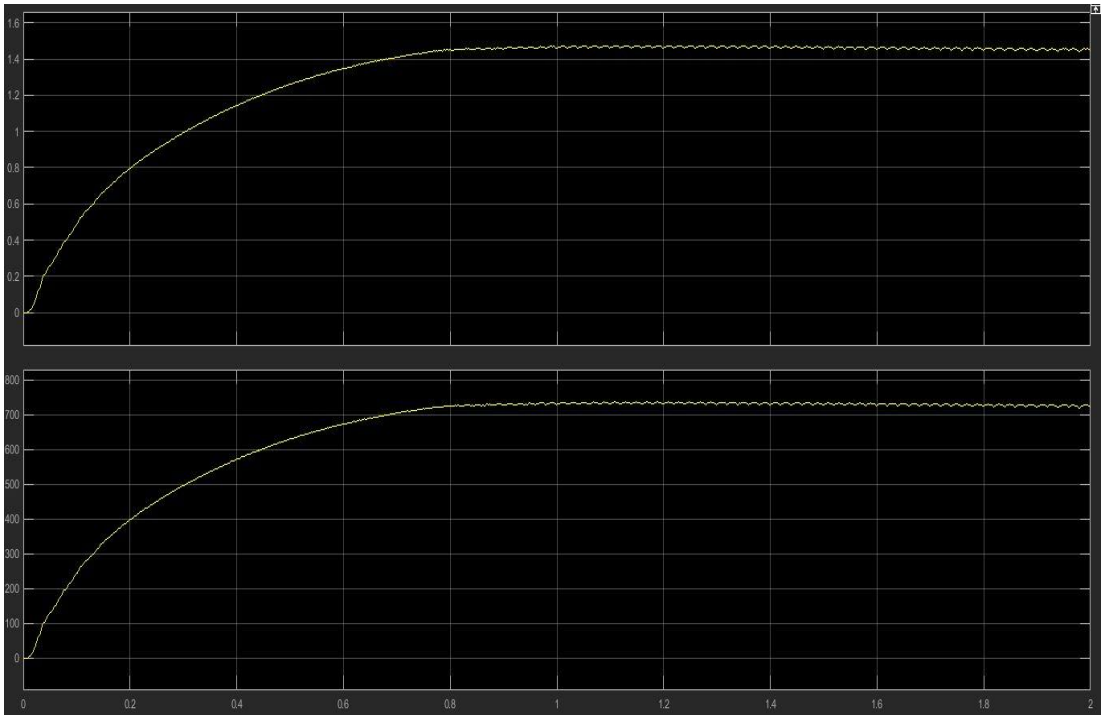


Figure 4.9 Output Current and Voltage Graph when Vin is 230V and 50Hz Frequency

4.3.1.6 Total Harmonic Distortion

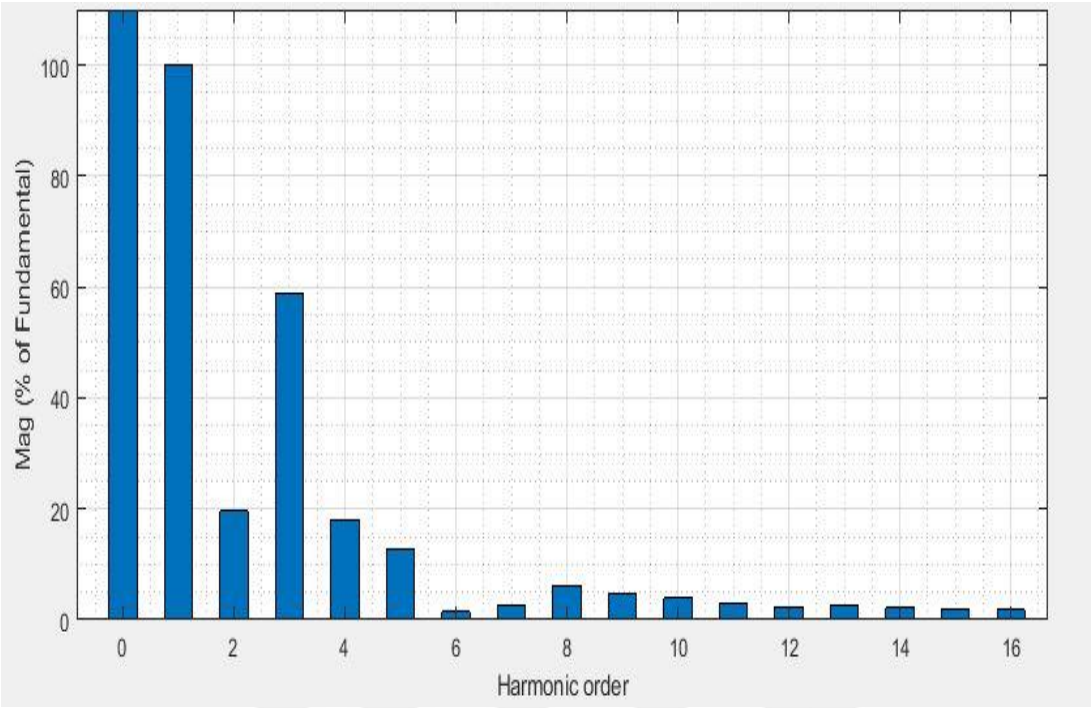


Figure 4.10 Total Harmonic Distortion Graph

4.4 Fuzzy Logic Controller for DV-Rectifier

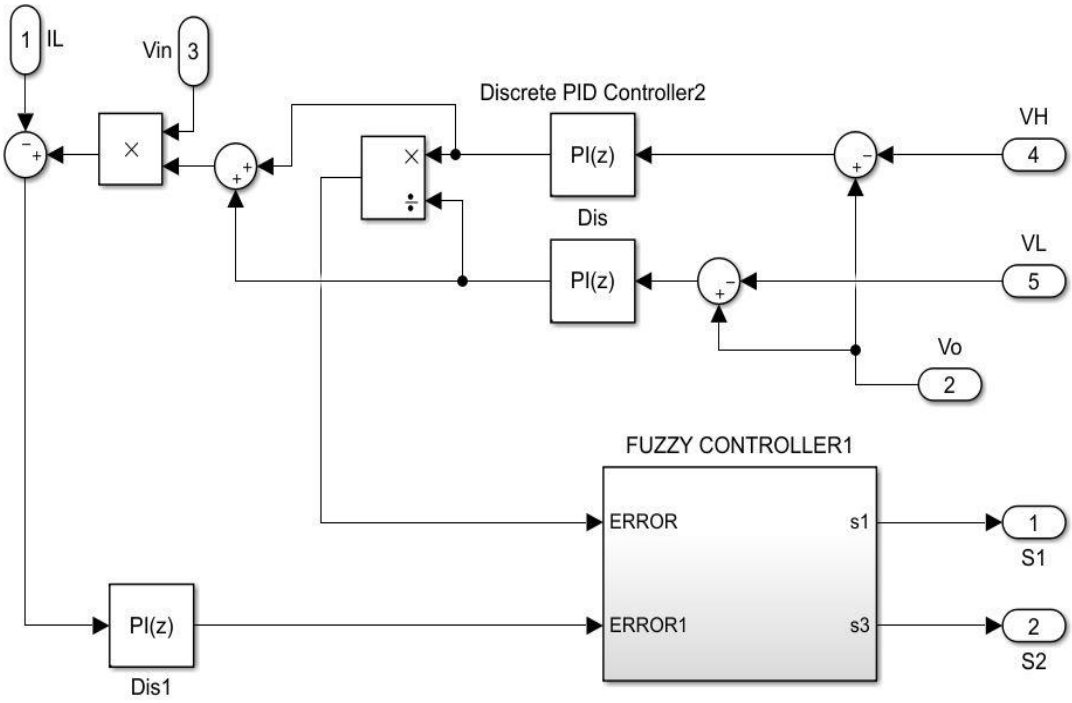


Figure 4.11 Control Circuit Diagram of Fuzzy Logic Controller

4.5 Fuzzy Logic Control Scheme

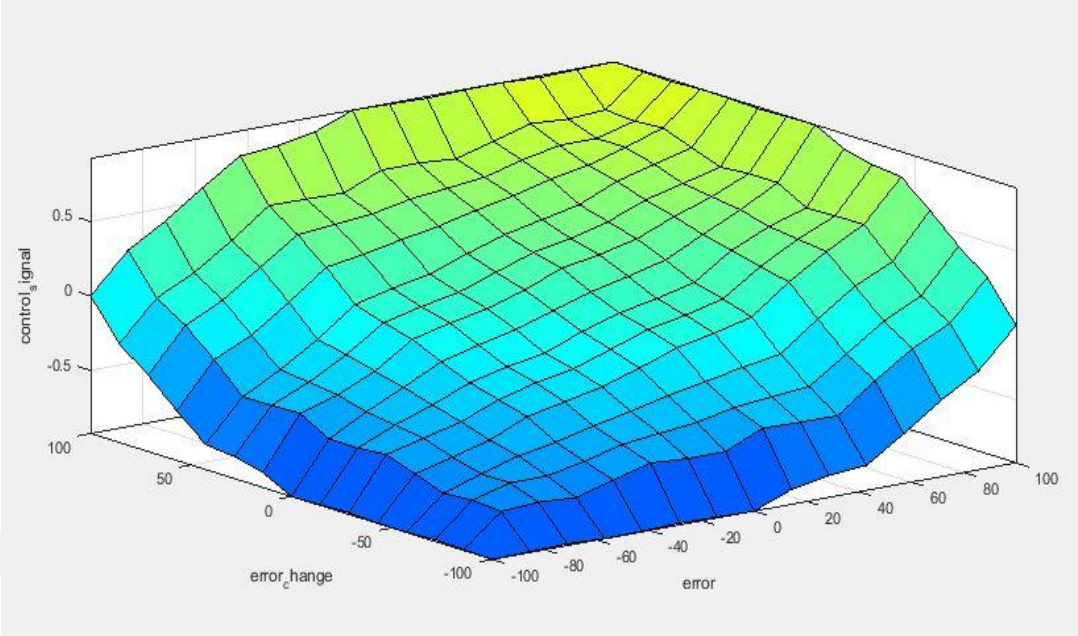


Figure 4.12 Fuzzy Logic Control Scheme

4.5.1 Graphs

4.5.1.1 Fuzzy Logic controlled DV-Rectifier Input Current and Voltage

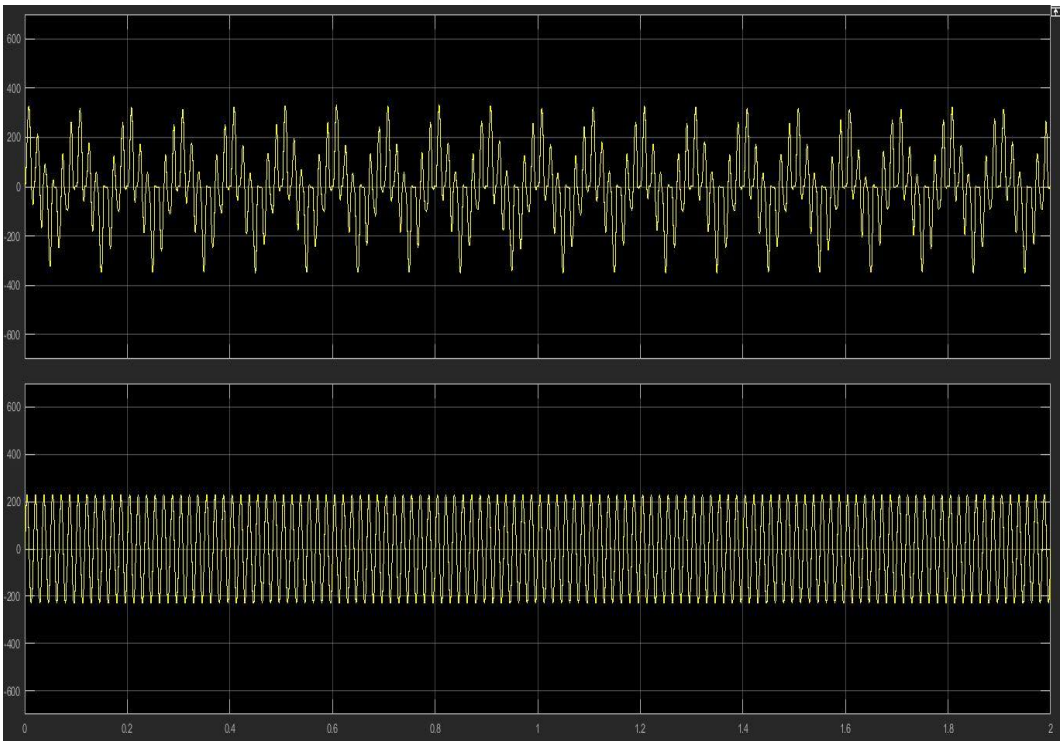


Figure 4.13 Fuzzy Logic Controlled DV-Rectifier Input Current and Voltage Graph

4.5.1.2 Inductor Current

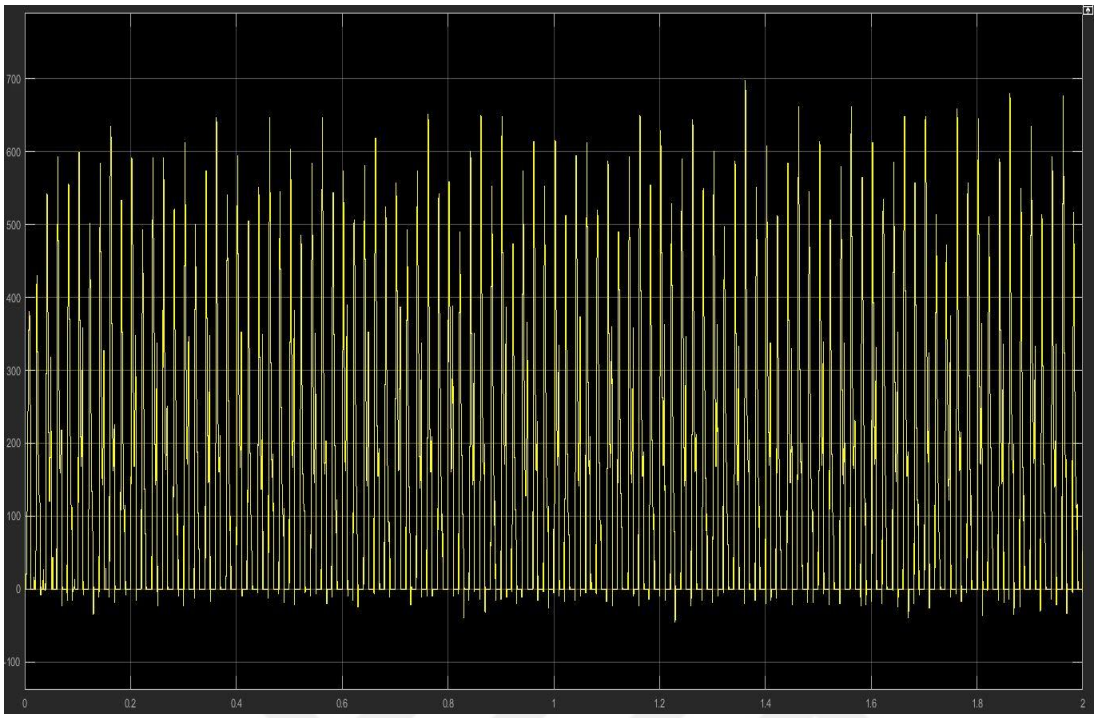


Figure 4.14 Inductor Current

4.5.1.3 Voltage Across Points A & B

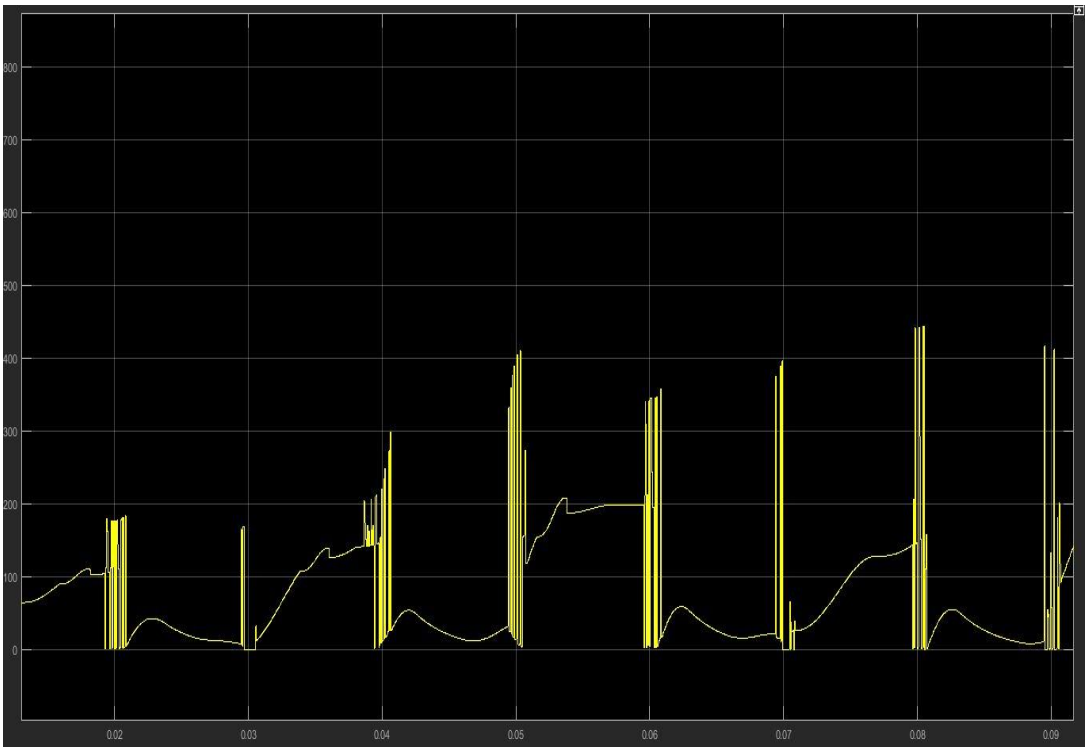


Figure 4.15 Voltage Across Points A & B

4.5.1.4 Voltage at port V_{Hi} & V_{Lo}

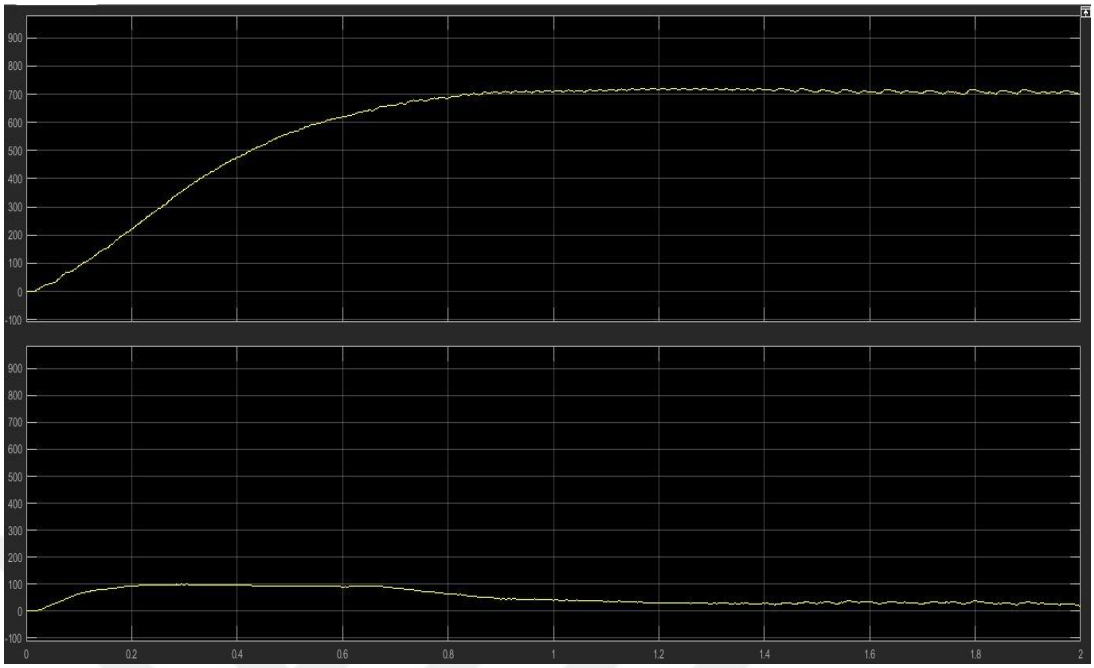


Figure 4.16 Voltage at Port V_{Hi} & V_{Lo}

4.5.1.5 Output Current and Voltage Graph When Vin is 230V @ 60Hz and 50Hz Frequency

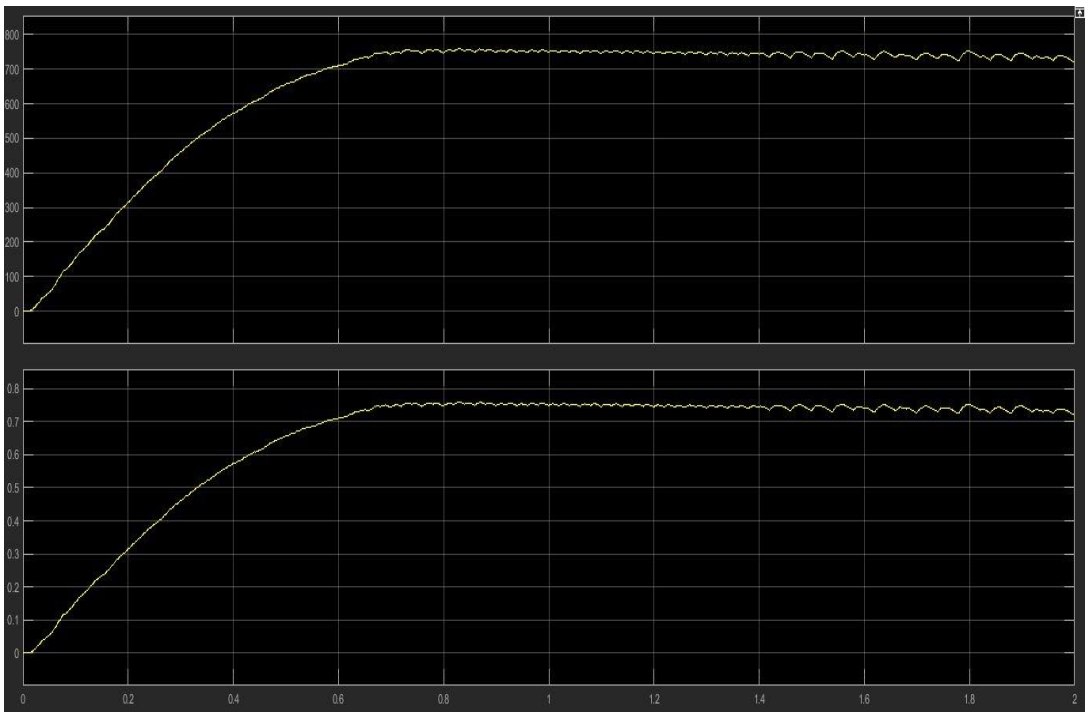


Figure 4.17 Output Current and Voltage Graph When Vin is 230V and 60Hz Frequency

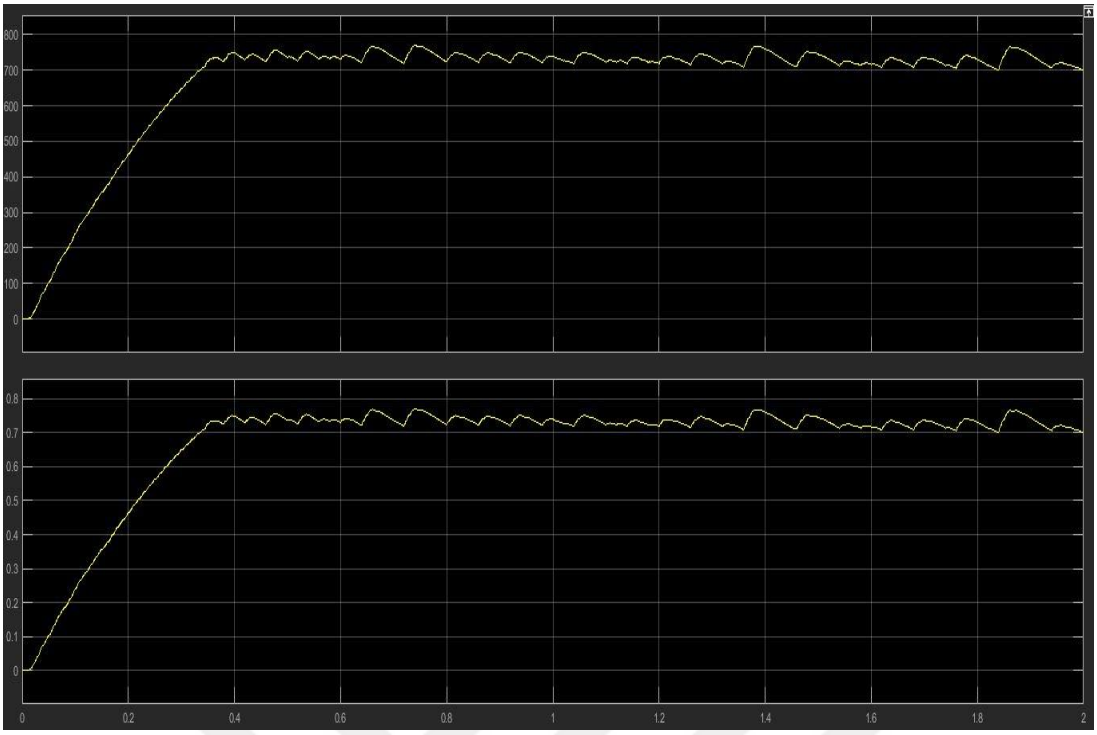


Figure 4.18 Output Current and Voltage Graph When Vin is 230V and 50Hz Frequency

4.5.1.6 Total Harmonic Distortion

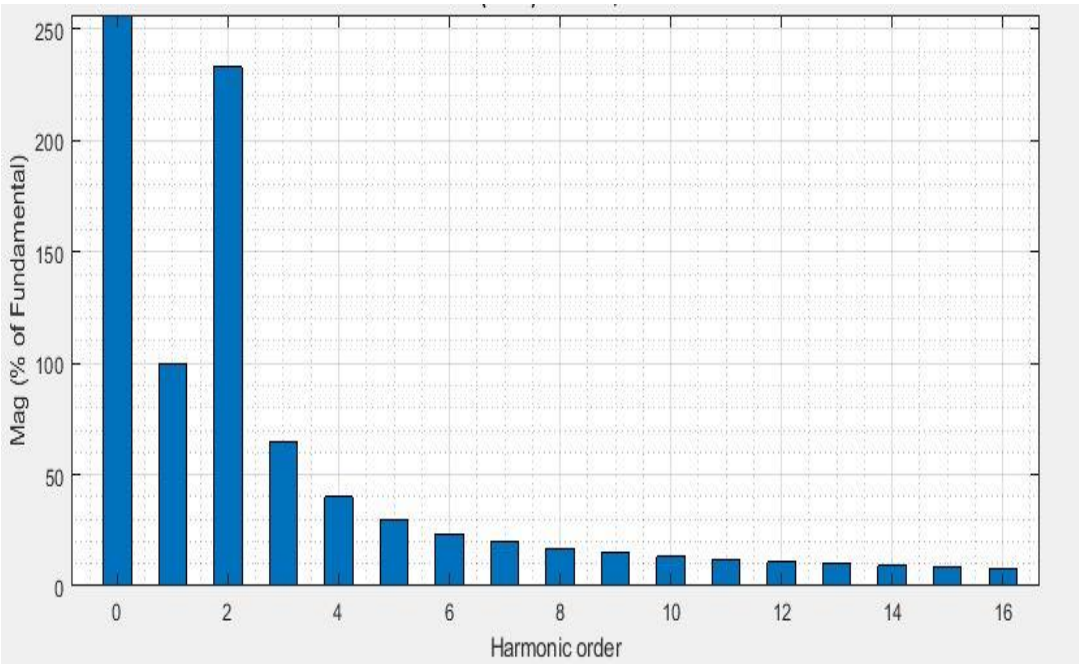


Figure 4.19 Total Harmonic Distortion

5 CONCLUSION AND FUTURE WORK

5.1 Discussion and Conclusion

In this thesis, we have investigated control strategies, theoretical principles and experimental verifications of DV-rectifier which is based on two stages. This DV-rectifier has dual DC buses and at the output sigma architecture. The results suggest us that the output volt regulation maximum power factor value has been achieved. The proposed DV-rectifier has two DC buses having one is constant and the other one is variable. Voltage regulation is done by the two DC buses. Hence, DC-DC converters can work as a DC- transformers and they will work at their maximum efficiency level. DC buses can provide three DC voltage levels which means we can reduce switching loses. For equal distribution of input power, we have used smooth mode and multi-mode control strategies have been applied. Feasibility and its effectiveness have been discussed in detail in this thesis and compared them with experimental results.

Prior study about this converter topology has not been found in the literatures. We have used MATLAB Simulink for the experimental verification of the proposed DV-rectifier. Firstly, we have used PWM control strategy to run the circuit as according to our required input to output. The control feedback error is considered as difference between the reference voltage and input voltage. The rate of change is used as inputs for the PWM block which will then determines the duty cycle of switch. Graphs have been shown in this thesis.

Secondly, more study in this thesis shows the same DV-rectifier topology is derived by Fuzzy Logic Controller (FLC). We have used same software to and input and output characteristics and got graphical results. The graphical results are compared of PWM and FLC driving the DV-rectifier. Robustness and efficiency of both control systems are compared at the end.

Graphical results of both the control schemes are compared and it is found that both schemes have their importance at their places. It is very difficult to say which is better.

As you can see in the graphs that in PWM there are less harmonics at the output and we are getting smoother output with very little distortion. On the other hand, if we look at the graphs of fuzzy logic controller, we see that the output reaches rapidly to our required output level as compared to circuit which is controlled by PWM strategy.

In this thesis, we have also realized that if your input frequency decreases, meanwhile distortion on the output also increases. As we can see in the diagrams, we have shown that when input frequency is 60Hz the distortion in output value is less than as compared to input frequency when it is 50Hz. Hence, we can get a sustainable output if we feed our circuit with a good DC which has almost zero frequency.

5.2 Future Work

As we have discussed earlier if we improve the DC quality with high power factor, we can get a better output and hence improving our DV-rectifier charging quality. This can be done by using bridgeless topology for AC-DC conversion as in it there will be no voltage drop in it. Also, we can improve quality of proposed rectifier by implying better control scheme.

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