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Electrical and Computer Engineering

DESIGN AND SIMULATION OF MULTI STAGE DIGITAL UP CONVERTER FOR SOFTWARE DEFINED RADIO TRANSMITTER

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Master Thesis

Asst. Prof. Dr. Çağatay AYDIN

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DESIGN AND SIMULATION OF MULTI STAGE DIGITAL UP CONVERTER FOR SOFTWARE DEFINED RADIO TRANSMITTER

by

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2019

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

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Mohammed Imad Ashour Al-Hamadani

DEDICATION

First of all, I would like to dedicate and give my great appreciation to my parents, who did their best and sacrificed in everything to facilitate my academic and scientific duties. I would like to thank my brother, my sisters, colleagues and special thanks and appreciation to my professor Assistance Prof. Dr. Majid Salal, with my best wishes and regards.

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ABSTRACT

DESIGN AND SIMULATION OF MULTI STAGE DIGITAL UP CONVERTER FOR SOFTWARE DEFINED RADIO TRANSMITTER

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In this paper, the design and simulation of digital interpolation filter for GSM transmitter based on software-defined radio technology is presented. The interpolation process nowadays plays vital roles in the mobile system due to the traffic challenge. In order to produce intermediate frequencies from baseband signals with a device which should have a small size and low power consumption, the multi-stage interpolation filter under software radio techniques should be used. In a GSM transmitter, the pulse shaping and frequency conversion from 2.166 MHz to 69.333 MHz is processed in one block called multi-stage digital up converter filter. Each stage is implemented separately and joined together in GSM transceiver using FDA tool in MATLAB. The simulation shows a promising result for the new generation of the mobile system.

Keywords: Digital Up Converter, Mobile, GSM, Transmitter, SDR

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LIST OF ABBREVIATIONS

SDR : Software Defined Radio

DUC : Digital Up Converters

GSM :Global System for Mobile

FIR : Finite Impulse Response

RRC : Root Raised Cosine

PFIR : Programmable Finite Impulse Response

CFIR : Compensation Finite Impulse Response

CIC : Cascaded Integrator–Comb

IF : Intermediate Frequency

1. INTRODUCTION

1.1 GENERAL OVERVIEW

It is known that software defined radio (SDR) technology provides radio control and control for a variety of modulation techniques, operating many different ranges of wide and narrow, and security functions of communication (such as hopping) and making the form of the router according to the current requirements and developed over a wide frequency range. We can say that these programs, work on the platforms of general devices of the digital signal processor (DSP) and multi-purpose and general purpose processors can perform such functions as modulation and demodulation, signal generation, coding, a part from that, also the link layer protocols. These programs help in building radio systems. It is programmable and remodeled where a dynamic selection of operations is possible. In our time, communications are progressing very rapidly and significantly, and communication systems that work in parallel with the development of integrated circuit design technologies (IC), new manufacturing processes allow for new functions and advanced in terms of performance. Many applications work very quickly and therefore, they prefer a fixed connection. The design of the transmitter side of the digital modem is to be based on working on the digital up converter (DUC) [1-2]. The DUC is an important component of the wireless transmitter. It translates as well as converts a baseband signal which is complex to signal passband signal. Samples are converted from the basic complex signal that is entered to the highest at the relative sampling rate. The basic range signal is translated and filtered using a higher sampling rate before modulation on the direct vector digital frequency Direct digital synthesis (DDS). DUC generates and sets the pulse signal the intermediate carrier frequency has to be led by the analog converter for the final. The implementation of this process at different stages and multiple sampling rate is effective from the arithmetic aspect [3].

The digital representation of signals and its widespread use has led to great challenges in creating digital signal processing. In digital products modem Digital Finite Impulse Response (FIR) filter applications and sampling techniques are found up / down in large and wide range. The least complexity of the electronic circuit in each electronic product is the main and always important goal of design because it reduces its cost [1-3] . In order to increase the sampling rate or reduce the sampling rate, we need to use interpolators and decimators to perform this process, which is

possible using these two options. In order to change the sample taken from the baseband signal, the up sampler and down sampler is used to raise and lower the samples of the digital signal taken into operation in the DSP system. Unwanted signals and errors related to deformation are generated due to the special requirements for conversion of the sampling rate. In order to get rid of these errors, you must put filtering to this process [4-5]. Consumer electronics that are now used, such as cell phones, wireless devices and multi - media devices, require digital signal processing algorithms DSP for a variety of critical processes to increase the speed, reduce space, and energy consumption. The range of user terminals that need to be connected in this communication world, include cell phones, satellite phones, portable computers and other nomadic computing devices [4,6,7].

In wireless communication, SDR technology is used widely and extensively, and it refers to the category of reusable radio devices which can be a flexible physical layer through reconfiguration. FIR filters are used for digital up converter and digital down converter, which belongs to the SDR technology. DUC is widely used in communication systems to convert signal rate used, that is required when transmitting and converting the signal from baseband signal to intermediate band. The signal rate of the DUC filter which are converted to a higher sample rate as well as the signal is formed with the carrier signal. When taking different sampling rates in digital signal processing applications this also improves the radio flexibility of a software defined radio. This also makes the ability to reduce the need to the filters that are expensive and anti-damaged, as well as the treatment of many different signals and the rate of taking different samples. This technology allows the division of high - speed processing to low - speed, parallel and multi-tasking which can lead to significant savings in computational power and cost [8].

1.2 MOTIVATION

Due to the competition of the wireless communications market and the advanced communication standards, this resulted in short life cycles in the design of the products. This has led to the emergence of new designs and categories of digital data service providers, which can increase the hardware's flexibility, DSP solutions are highly versatile and highly customizable [1]. Because of this, DSP are used which can be modified and programmed widely and in portable devices to perform baseband processing functions such as equalization, filtering and echo cancellation [3]. A good design of the system and the efficient use of resources can greatly improve the cost factor.

With the increasing demand for battery-powered devices, ways to reduce power consumption in memory blocks have received considerable attention. The successful implementation of SDR depends primarily on implementation. The different blocks that are within the communication series with different standards. The wireless is an environment that is constantly changing, where the high rate of innovation is very high. It requires as much perfection as possible through the use of special software solutions with referring to the past years we see that the software platforms they have proven to be highly scalable for hardware solutions. However, the mobile wireless communication and the requirements for frequency bands cannot be met with software only. The SDR that use a hardware front end, but it can change operating frequency on their own, busy bandwidth, and meet different standards in wireless devices by invoking various software algorithms. Through this solution, interoperability is effective, inexpensive and effectiveness can be between the available standards and frequency bands [9,10]. The advantage is that SDR is characterized by the re-configuration of its own devices can support multiple formats of the previous digital packet DBF it seeks to achieve compactness as well as strength in effective treatment and consider these important issues [5].

1.3 PROBLEM STATEMENT

In wireless communication, the problem is to lose the transmitted vector while sending and receiving the signal by the receiver. To avoid this problem, the DUC must be well and designed to transmit the spectrum with a level that can avoid the loss in the spectrum signal, according to the class of the specified spectrum. This is done in multiple stages based on its preference for stage one [11]. In a digital intermediate frequency modulator was introduced and reconfigured for the transmitter of signals and receptors known as SDR, the DUC is designed and applied to the GSM-based on the SDR by used a multiplier technique and the effective speed that performance [4]-[9]. The DUC is the physical unit of wireless pairing devices, that formed to designed pulse interpolation and then the frequency translation [4][9].

1.4 OBJECTIVE

Our objective in this thesis is to design a digital up converter based on GSM and take samples of the baseband signal by factor 16 as well as from the important objectives that to be designed in an efficient way to use available resources and consume as lower energy as possible. And below we mention the objectives of design.

1. To design and simulate the DUC model dealing with a minimum error between transmit and received waveforms using MATLAB/SIMULINK block set

2. To design and simulate mobile system integrated transmitter and receiver signal to check the filter capacity designed to work with the system and efficiency of its work

3. To design and simulate an advanced filter for a mobile transmitter.

4. To design and simulate the complete mobile transmitter and receiver

1.5 THESIS OUTLINE

The first chapter contains general detail of software defined radio SDR of DUC transmitter, motivation, problem statement, and objective. The following chapters are organized as follows:

- **Chapter 2:** Theoretical background of SDR architecture and related work
- **Chapter 3:** Explain how to build and filter the proposed filter using MATLAB Simulink
- **Chapter 4**: This chapter contains the results that obtained from the simulation
- **Chapter 5**: This chapter contains a conclusion and future work.

2. LITERATURE REVIEWS

2.1 THEORETICAL BACKGROUND

A SDR transceiver consists of two parts: transmitter and receiver. The following Figure 2.1 gives a general description of the SDR transceiver.

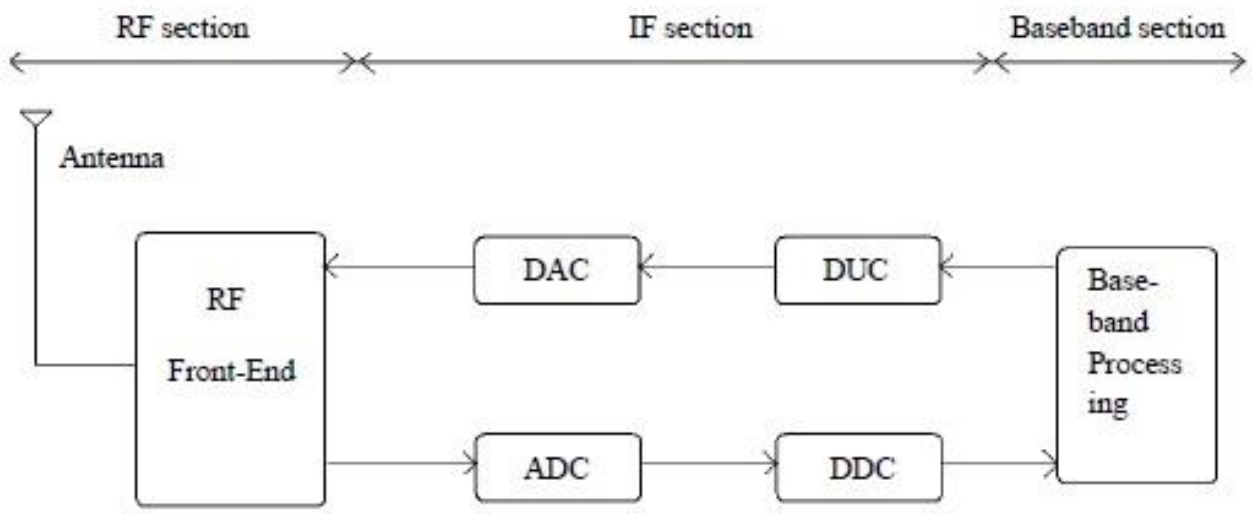

Figure 2.1: General SDR architecture [12].

The software-defined radio consists of three main functional blocks: Radio Frequency (RF) section, Intermediate Frequency (IF) section and baseband section. The RF section consists of essentially analog hardware modules while IF and baseband sections contain digital hardware modules.

In our thesis we will talk about IF section that includes the part which we will talk about DUC.

2.2 RF FRONTEND TOPOLOGIES

Communication, applications, and services have become the necessities of our daily life. These systems are made up of many integrated circuits (Chips). These systems consist of an independent

transmitter and receiver dedicated to the operation of a specific standard. To be compatible with current and future standards, the design of the system must be flexible and reconfigurable. The tunable RF is a promising solution that can be implemented in front-end RF receivers in SDR receivers that can be compatible with multi-level wireless applications in an energy-efficient and cost-effective manner. This filter was designed in transmitter and receiver devices to work with the next generation of wireless standards using GSM, UMTS, Wi-Fi, and LTE. [13-14].

2.3 BASEBAND SECTION

It is possible to say that the baseband of the parts is important because it performs operations such as equality, error correction, frequency hopping, modulation, deformation, and time recovery. The forward error correction is the means to get control of errors in the course of sending data which is sent by the transmitter that contains parts of the redundant data that are not needed and the receiver does not recognize this excessive data as he recognizes data that does not contain obvious errors. In order to minimize the objection that occurs during the transmission or disruptions of the data in the communication systems, its frequency hopping is used to reduce this objection by repeated frequency switching during wireless transmissions.

2.4 FINITE IMPULSE RESPONSE FILTER

It is now possible to integrate complex systems into a single chip (SoC) for remote battery-powered, remote computing and communication. The design of a low-energy circuit is important to the success of scientific exploration in harsh environments. The circuit design shows asynchronous properties interesting along with energy efficiency. As well as the reduction of electromagnetic interference reduction [15]. The immune from transient behavior stable [16] as well as ultra-wide temperatures [17-18].

FIR in the digital signal processing, the filter FIR is common because it processes the signal because of its stability and ease of implementation of the long response. Because of the complexity of the area and the energy consumption of the filters, and to limit this, the researchers proposed algorithms to improve their work with the reduced number of non-zero digits [19]-[20].

FIR is a digital coaxial filter used in DSP, as well as in communications, controls, and automation. The most stringent size and high power budget specifications in mobile applications require the

design of FIR filters to improve the compatibility of the large complexity that is focused differently from the general purpose DSP [21]-[22].

The FIR filter is widely used in applications for different signal processors. The transport bandwidth is arranged primarily by the FIR filter so that the filter order is higher, and is a transition between the pass-band and adjacent stop-band. In communications, many applications require channel equalization, frequency channelization, adaptive noise cancelation in speech processing, noise elimination, and many applications that require other signal processing. Increasing the candidate's output linearly with the candidate's order and the actual execution of the time. These filters for the large orders are a difficult task. Therefore, many transformers have been used in the development of VLSI systems for these filters [23-24].

2.5 ROOT RAISED COSINE FILTER

Raised Cosine is a filter that avoids the interference occurs bandwidth is not taken which is passing through a low pass filter are not to be it can be observed that the shape change from rectangular pulse to a pulse with no sharp edges and smoothly outlined. Therefore, it is known as a pulse shaping process. The rectangular pulse exhibits non-zero amplitude as well as the smooth pulse shows a small number of ripples which are before the interval and after the pulse. These ripples can result in decoding in the data in an incorrect manner at the receiver end as this ripple interferes with the pulses. The interference can be made minimum by maintaining the time domain format and such filter selection provides the desired reduction in bandwidth. It finds its application in wireless devices and cellular phones in order to increase the speed, reduce consumption in energy as well as area. The RRC filter is very helpful in pulse shaping; it makes the signal compatible for the channel. It makes channel interference or noise free, in the hardware implementation of a filter by changing the suitable factors the designed filter can be used in different application area and speed can be optimized [25-26].

2.6 DIGITAL UP CONVERSION AND DIGITAL DOWN CONVERSION

Digital up/down conversion is a process of translating and converting data from the baseband to IF (up conversion) or from IF to baseband (down conversion). At the transmitter, where samples are taken from the baseband of the input and at a sampling rate that is relatively low. The initial signal is filtered at the baseband and then converted to a higher sampling rate also before the

modulation of the carrier frequency is higher. Thus DUC performs the process of up sampling which means increasing the data sample rate and hence the number of samples. At the receiver, received signals are sampled at a relatively high sampling rate which leads to huge amounts of data, but in a large number of these cases the signal is of low interest from this bandwidth. The rest of these data is eliminated because the DDC allows it to do so, allowing much intensive processing to be followed by a signal of interest. Thus DDC performs the process of down sampling which means decreasing the data sample rate and hence producing less number of samples [27,28].

2.7 DIGITAL UP CONVERTER

The DUC is a digital signal converter that performs convert baseband signals to the passband of scroll signals. The sample rate is taken from the baseband signal is relatively low and it is usually the rate of the digital modulation symbol. The signal of the baseband is filtered after sampling of the signal and converted to a higher sample rate before being included by direct carrier frequencies DDS. The DUC filter typically configures the pulse as well as the intermediate frequency modulation which is suitable for driving a final analog converter and that is widely used in the field of telecommunication systems. In a DSP, the rate of taking these samples is considered an important cost factor in its implementation due to the basic system of computing which is a requirement of productivity imposed on the system. Oversampling techniques are used because it is a common way to calibrate requirements on an analog product in a mixed analog system. In the digital part of the system, the need for the interpolation and the decimation filter is important. When the bit rate is high in broadband communication systems, these filters should be designed so that they are very well configured, and these systems are often operated by battery so the energy factor should be considered and how to reduce the consumption. Different and diverse architectures are used for interpolation and filtering. But it is important to know which one of these architectures must work and which is compatible with the system correctly and with fewer resources. The devices in which the area is less believed that the best architectures are to be absorbed in those devices. Cascaded integrator comb (CIC) has been introduced to the community of signal processors as well as being used mainly for effective implementation of interpolation. The most important characteristics that make these filters widely used are that they do not require any multiplication. Adding and subtracting accurately is required to calculate the implementation

of these digital filters. CIC filters are also known by various names, such as the moving average filter or the recursive filter [29-30] as shown in Figure 2.2 the part of the DUC filter in complete antenna.

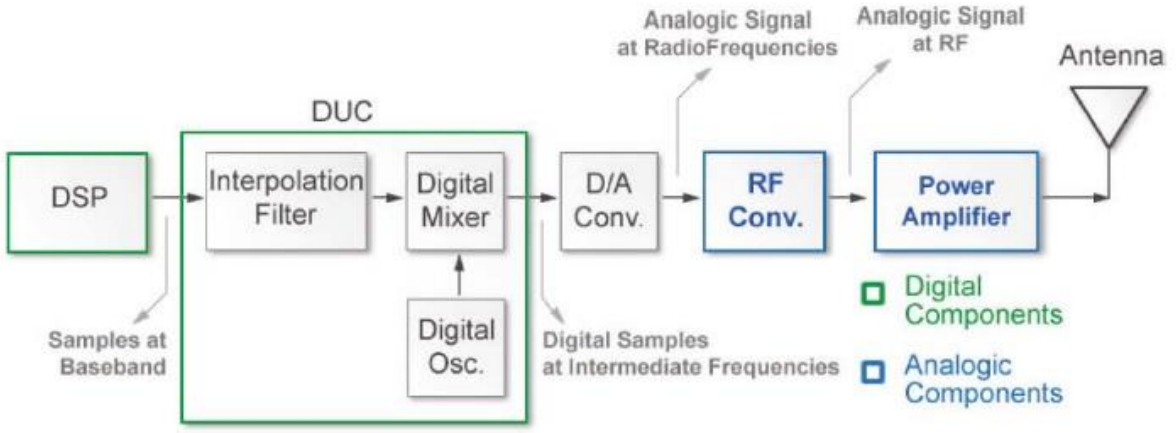

Figure 2.2: Block diagram of a SDR transmitter [31].

2.8 RELATED WORK

Since the SDR technology has held to our life, many researchers have been proposed their work to develop the equipment of this technology. One of the most important part in the SDR system is the DUC in the transmitter part. In 2008, 'implementing WCDMA Digital Up Converter In FPGA' has been proposed [9]. How to design and implement a digital up converter DUC is discussed by the researcher in the Field Programmable Gate Array (FPGA). This signal is generated by the digital signal circuit DUC. This circuit also provides pulse formation, interpolation as well as frequency translation where the signal is converted and rounded from (0Hz) to intermediate frequency. WCDMA DUC the interpolation filter is designed in several stages, divided into four stages to minimize the use of DSP48. In a nutshell, reducing the use of the DSP48 can reduce the complexity of the devices as well as reduce the simulation computational time. The WCDMA DUC was successfully designed according to the Xilinx Virtex-4 FPGA as well as the WCDMA requirements as mentioned in 3GPP TS 25.104 v4.5.0. The simulation process is done before downloading the design in the FPGA board. Samples were taken from the baseband signal and the

pulse was also set by factor 16. The circuit designed by DUC was tested up sampled signal to 61.44MHz as shown in Figure 2.3.

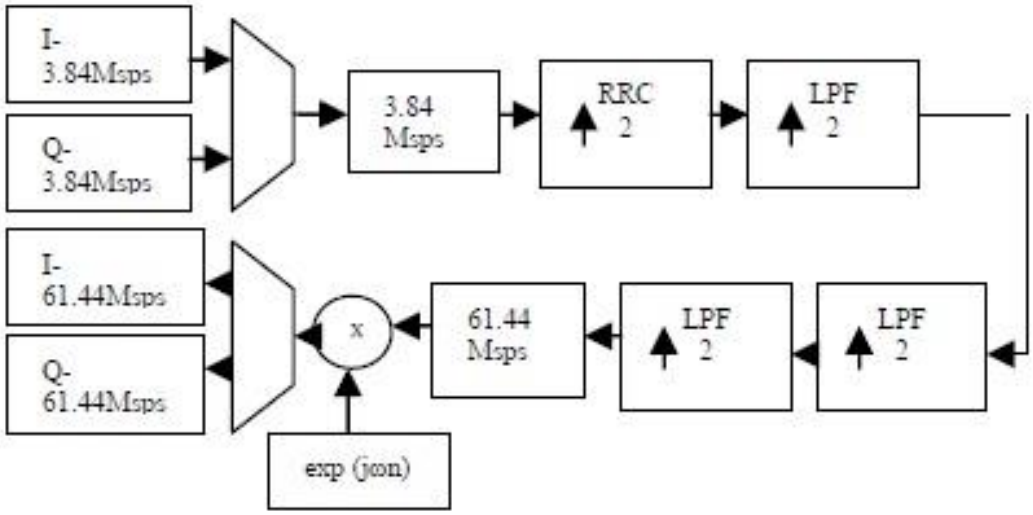

Figure 2.3: WCDMA DUC block diagram [9].

In 2009, 'Efficient Design of Digital Up Converter for WCDMA in FPGA Using System Generator' was presented [32]. In this work, a DUC design was proposed on Xilinx FPGA for WCDMA. A powerful Xilinx System Generator has been adopted to shorten the design cycle and increase productivity. Also, the RRC filter and the half-band filters are designed as DUC sub-units. By using MATLAB FDATool and Xilinx FIR Compiler. Through the Xilinx DDS Compiler, the DDS module was produced. Using the Vitex-5 DSP48E slices, the frequency of the multiplier operation reaches 368.64MHz. The DUC should be in the form of a pulse where a percentage of the bits are taken from the baseband and 16 to 61.44MHz to meet the WCDMA specification. We also implemented the DUC design on the Xilinx XC5VSX50T FPGA device. In this paper, an effective D-1 carrier design was discussed using the Xilinx System Generator for WCDMA. One of the findings was that the design of WCDMA DUC was effective and met all the system requirements mentioned in 3GPP TS 25.104 v6.13.0.

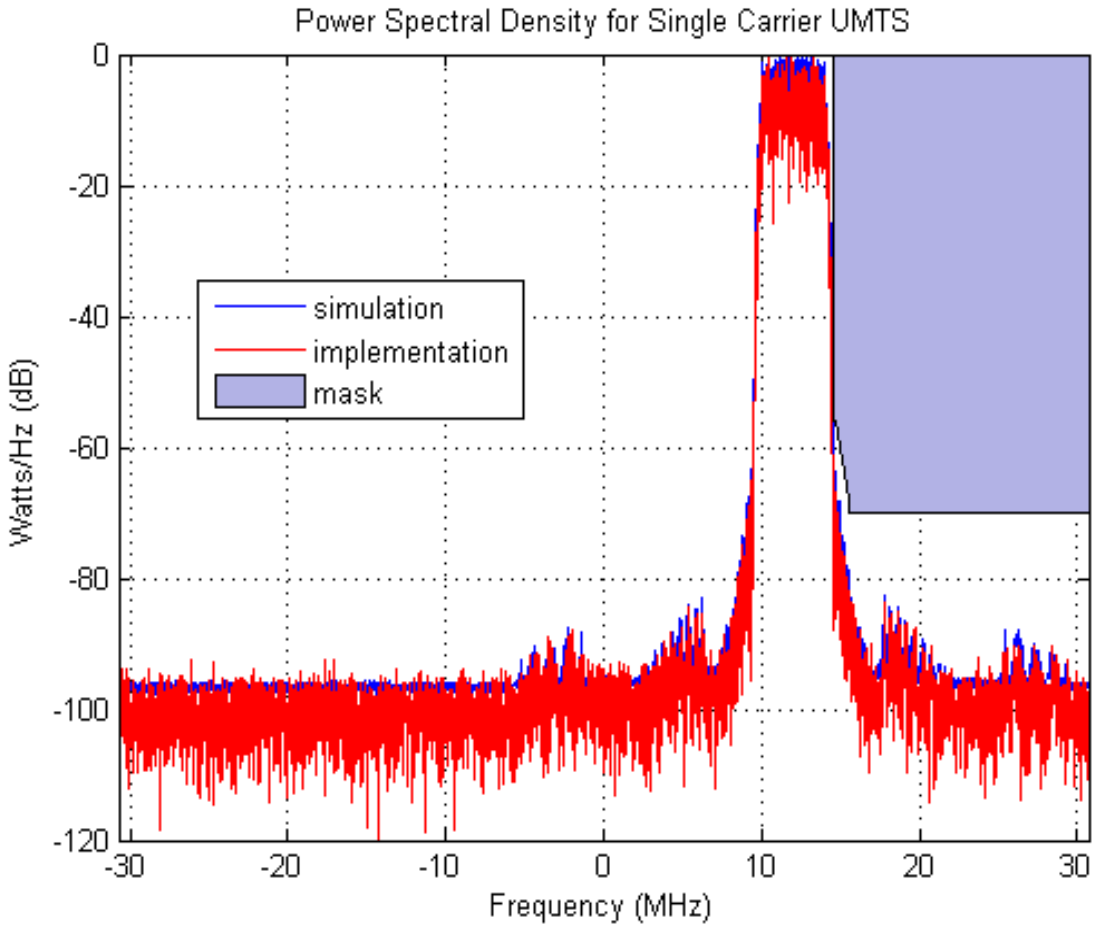

Figure 2.4: PSD result for the DUC design [32].

In 2010, 'FPGA Implementation of Digital Up/Down Convertor for WCDMA System' was presented [33]. The DDC and the DUC for its FPGA, for a single carrier WCDMA system, was implemented in this paper. These circuits are made of complex circuits in the communications system. But the DDC filter is simple because it does not require mixers or filters. The FPGA circuit was developed by using Xilinx System Generator and Xilinx ISE. The two departments were verified on Virtex-4 FPGA. The circuits were implemented on Virtex-4 FPGA. FPGA is found suitable for the real-time implementation of the communication algorithms because of their high performance, small size, flexibility, and competitive price. The DDC and DUC circuits are implemented using the Xilinx System Generator design tool. Experimental results verify the working of the designed circuits.

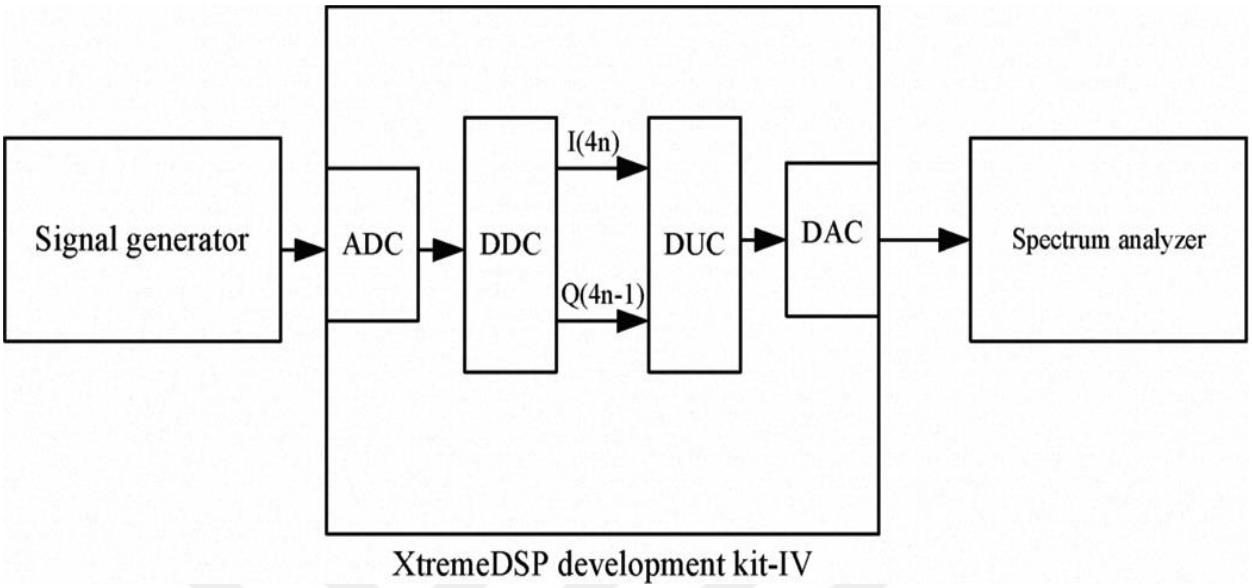

Figure 2.5: Laboratory test bench [33].

In 2013, The Researcher proposed 'Reconfigurable Cost-Effective Design of Digital up Converter for Mobile Communication' [5]. The WCDMA DUC design, which is highly reusable in mobile communication stations, was presented in this paper. The WCDMA DUC filter has been implemented by combining the multiplier less and multiplier based technologies to create a hybrid solution for mobile applications. The performance of the DUC filter has been improved by improving the different sections separately and then integrating them together. The proposed candidate was designed and implemented with Matlab, which was adapted to Xilinx Synthesis Tool (XST) and implemented on Virtex-II Pro based on the xc2vp30-7ff896 FPGA device. The circuit can reach a maximum frequency of 147 MHz from the developed DUC and resources available on the FPGA can be utilized to provide cost-effective solutions to wireless applications that are compatible with SDR. Current circuits suffer from a major drawback and cost is because they are implemented on the DSP 48E slice which is based on Virtex 4 and Virtex 5 FPGAs. So the speed efficient and cost-effective design operation of the digital converter. The development demonstrated in WCDMA DUC has led to improve speed as well as improve resource utilization to provide cost-effective solutions for mobile communications applications based on SDR.

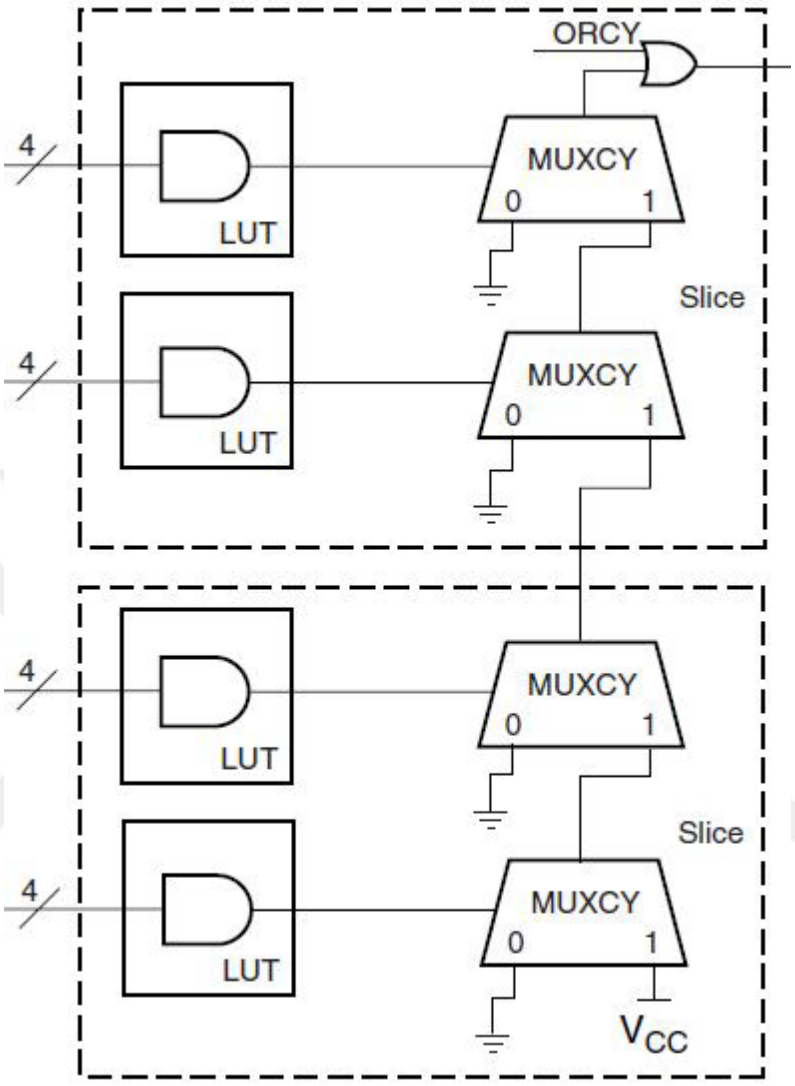

Figure 2.6: Efficient AND OR logic implementation [5].

Also in 2013, 'Efficient Design of Dual Digital Up Converter for WCDMA and CDMA2000 Using System Generator' was presented [34]. The design includes DDS programmable and three stages of the digital filters that have been simulated and designed with simulated Matlab. It is designed with the Xilinx system generator and manufactured with Xilinx Synthesis Tool (XST) targeting spartan 3A based xc3sd1800a FPGA. Using a controller that works to load the filters for each system with the ROM to the digital filters, which are compatible with the programming to conform to the system required to verify the status of Dual mode. The results show that the system design based on the Xilinx System Generator is simple and possible and also responds to the system requirements and to transmit the specific downlink to each system. The proposed design consumes

as little resources as possible to provide cost-effective solutions for applications running on SDR. The system allows program radio to be compatible and solve many problems that are caused by new interfaces. Terminal stations and base stations that work on SDR architectures can support new and multi-platform interfaces during transition periods and these programs are easily updated. The multiple air interfaces can be based on much of spectral band sensing and are done through cognitive radio algorithms.

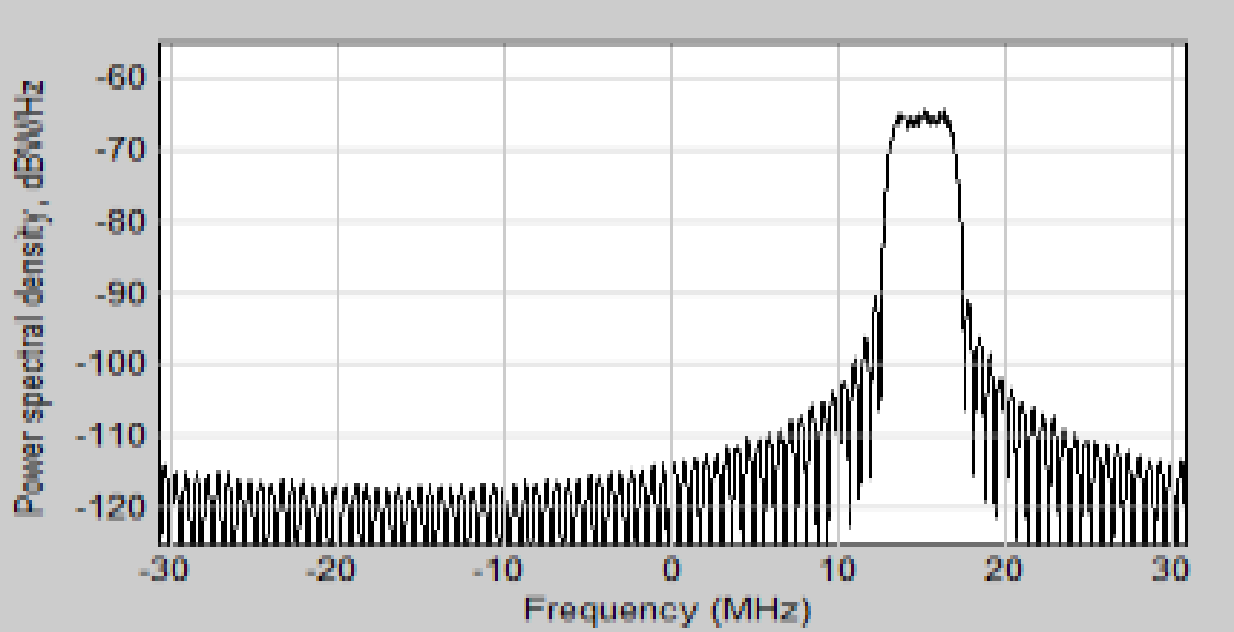

Figure 2.7: Power spectral density for WCDMA DUC - DDS tuned at 15 MHz [34].

In 2014, 'Implementation of digital up-down convertor for WCDMA system' had been proposed [35]. The design and implement digital up-down converter was carried out by MATLAB. The DDC and the DUC are widely used in radio systems. They are more popular than their counterparts due to their small size as well as their low energy consumption and delicate performance. The DUC provides the pulse formation, interpolation, frequency translation, and interpolation. The DUC filter generates and transmits the intermediate frequency signal through the complex core signal. The frequency (0Hz) is transferred to the intermediate frequency. The DUC candidate was designed and designed to comply with wireless communication systems as well as flexible digital filtering. DDC converts the external signal from analog to digital convertor (ADC), which is located in the IF, to the signal, which is located in the basic range of the complex signal. In addition to this work, the DDC decimates the baseband signal without affecting the spectral signal

properties. It is easy to process signals that are marginalized at a low data rate, on low-speed DSP processing. In the modern systems, the introduction and spread of wireless access in data networks is a natural matter and a clear development, as well as is motivated by the promise of user mobility and disposal of wires. This is reflected in recent developments in various fields, including mobile technology. According to WCDMA standards, WCDMA systems can be designed for channel bandwidth 5 MHz. This is because higher bandwidth can result in an increased data rate. The design of digital circuit systems with a large bandwidth is also one of the biggest challenges. So in this work, the interpolator stages of WCDMA DUC were presented and designed on a 5 MHz bandwidth. So, the design of WCDMA DUC results in an efficient system.

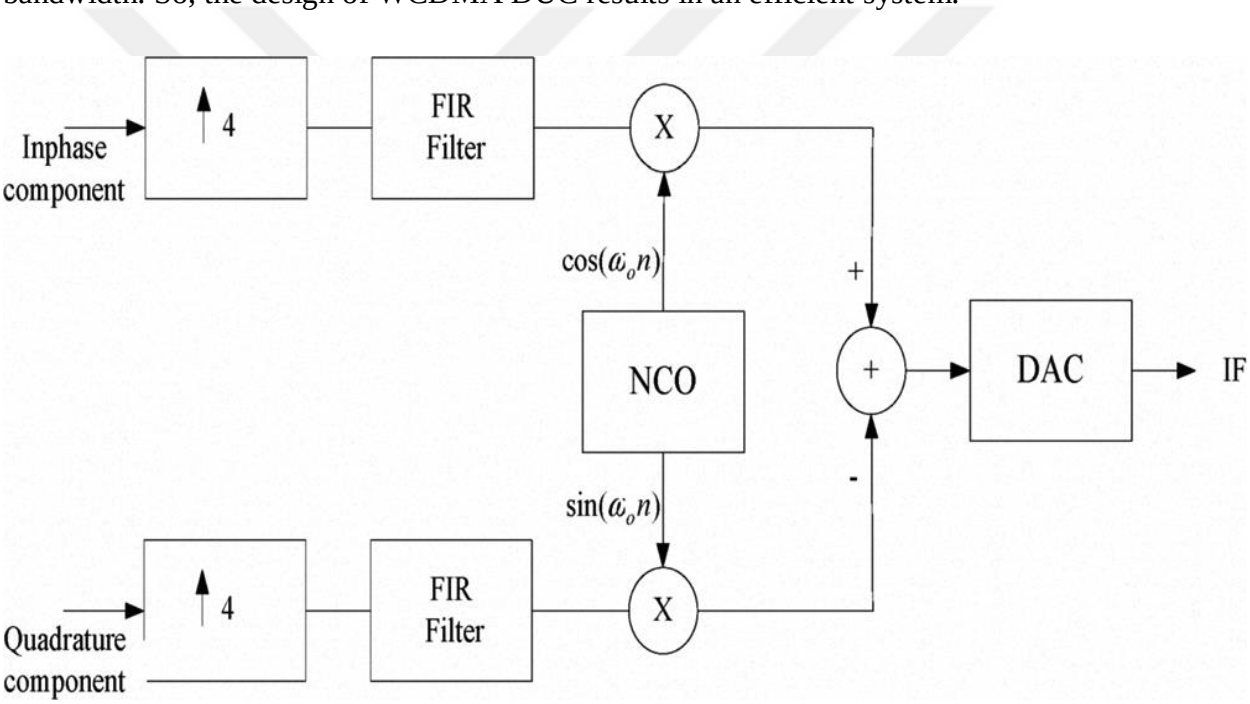

Figure 2.8: Block diagram of digital up converter [35].

In 2015, 'Design of a Multi-Standard DUC Based FIR Filter Using VLSI Architecture' has been proposed [36]. In Digital Signal Processing FIR filter was used to remove the noise or unwanted components from a signal. This paper presented an efficient VLSI architecture of a Multi-Standard DUC based FIR filter that is used to remove the noise in the received channel data bits effectively. The proposed DUC based FIR filter consists of a weight update block with shift add architecture to achieve a lower adaptation delay and efficient area, power, delay. In this proposed architecture for achieving an efficient adaptation delay and area-delay-power implementation, shift add architecture is used to modify the architecture for the implementation of a delayed least mean

square (LMS) adaptive filter using three co-efficient inputs. Number of Look Up Table (LUT) counts, path delay time and power consumption are reduced and the results prove that the Proposed technique produces higher speed when compared to the existing DUC based FIR filter architecture. Finally, the FIR with DUC multi-standard channel filter architecture was designed. The circuit complexity level and the delay were reduced. This FIR filter architecture is used to remove the noise in the received channel data bits effectively. These structures are dealt with in order to address the various problems encountered in the design of the filter and which are re-configurable in multi-standard DUC, which is an important component of Software Defined Radio / cognitive radio networks. Number of Look Up Table (LUT) counts, path delay and power. In these two steps, the best way to make the desired candidate more flexible and efficient, by reducing the strength and area in addition to improving the frequency of the hour of design. The comparisons that were made in the proposed results with the results of the FIR reproducible and reprogramming which were performed on the FPGA show the advantages of the proposed work in terms of speed and energy consumption. compared to the existing reconfigurable RRC filter architecture. Further, the reconfigurable RRC filter architecture is to be enhanced along with an efficient power and area.

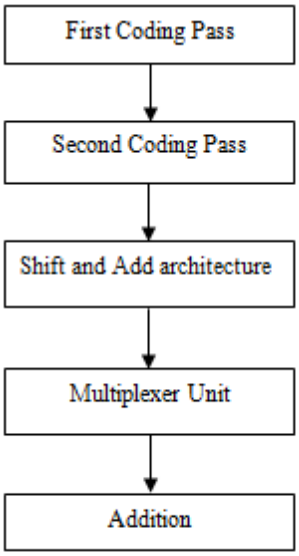

Figure 2.9: Data flow diagram of proposed CG block [36].

In 2017, ‘Model-Based Design for Software Defined Radio on an FPGA’ has been proposed [37]. SDR systems are an important feature of wireless communication systems because of their flexibility and benefits. The design was therefore performed on the FPGA for the selected radio. The well-known SDR system performs all arithmetic operations as well as performs signal processing tasks on the host computer and then transfers the signal to the RF front-end. For the high data rate as well as the complex algorithms the computer in this case is the bottleneck for processing and sometimes the FPGA becomes a hardware accelerator. This paper explains how to implement the SDR-based FPGA design. A complete communication system was designed and implemented. A transmitter with a convoluntary encoder, and a receiver with a Viterbi decoder, according to the FPGA's SDR system, whose effectiveness is verified by the demonstration via air. Work has also been done on improving the algorithms used, for example by changing the frequency of the carrier wave phase displacement and restoring time to improve the efficiency of the devices. A complete communication system model was designed and implemented to encrypt the channel as well as implement all the computational units through its FPGA-based SDR platform. All stages and units in the design can be worked on and modified by users as long as the corresponding FPGA is handled. The work is performed and evaluated through simulations, as well as shown and transmitted via air using SDR devices. In 2018, ‘Software-defined Radios: Architecture, State-of-the-art, and Challenges’ has been proposed [38]. The SDR is a device for transmitting and receiving wireless signals which has a reproducible configuration and programming as well as the possibility of operating many wireless communications protocols and without the need to change or update devices. With the development of the devices, work has also been done on the development of protocols that operate on these devices, and further development and especially in the flexibility of devices and portability, especially the energy efficiency in mobile communications,WiFi, and M2M communication. Thus, SDR has become a very widespread and important field in the various academic and industrial fields. The highly specialized circuit designers of this system will improve and simplify communication protocols as well as enable researchers to be able to experiment with prototypes on distributed networks. This paper was designed specifically for the SDR protocols in the context of wireless communication protocols. The buildings were presented with the SDR and its main parts and then the special design is discussed and how to use the important tools for development. Thus, according to certain measurements, the main contradictions between the SDR architectures related to energy, region,

and computing power were highlighted. Comparisons of SDR architectures were reviewed to serve as a guide for researchers and developers. In this way, a quick and concise presentation of the different design methods as well as the adopted hardware platforms has been provided for SDR. This includes GPPs, GPUs, DSPs, FPGAs. The infrastructure of the design has been explained and its disadvantages and advantages have also been analyzed. It is important to compare them to each other in terms of computational power and power efficiency. Some of the research challenges and topics that could be improved in the future have also been discussed to improve the performance and possibility of SDR. This paper is to take a full and comprehensive view on the techniques of the empowerment of this system as well as its own applications to research this issue from different angles

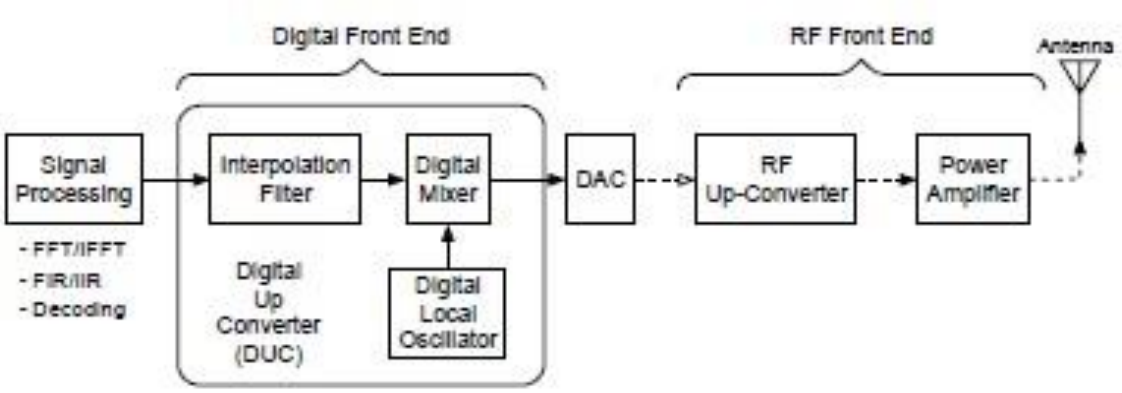

Figure 2.10: Transmitter [38].

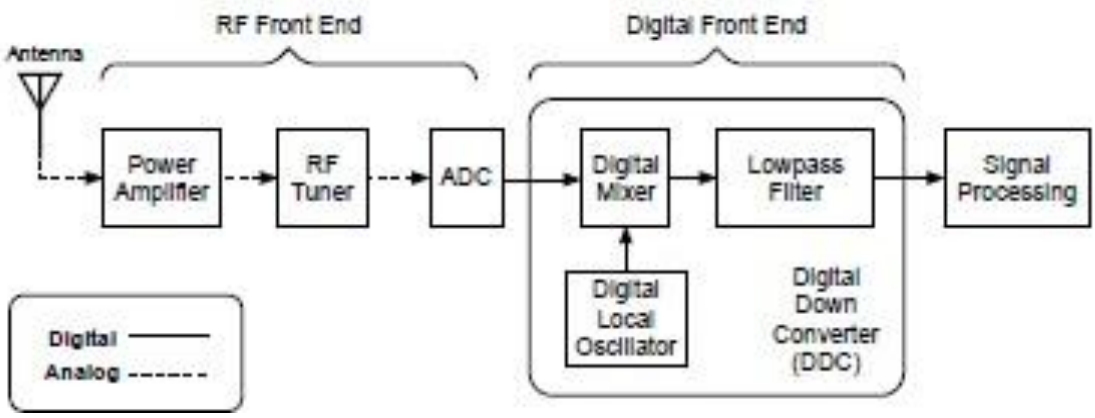

Figure 2.11: Receiver [38].

3. SYSTEM DESIGN AND SIMULATION

3.1 SYSTEM DESIGN

Telecommunication systems represent an important role in our daily use and with great development day by day. In wired and wireless communications when we want transmit a signal, samples shall be taken from the transmitted signal for the purpose of lifting during the transmission process in order to avoid the loss that occurs during transmission and receive signal process. DUC is a technical conversion rate that are taking a sample of the signal and is it widely used for increase the sampling rates for insertion of the signal. The filter first converts the signal from the baseband, which is relatively low to the pass band at a higher signal level. The default work suggested in this design includes the CIC filter, where the filter architecture that was designed by the DUC is covered and FIR cascades are included. The general design of DUC follows a common pattern in DUC applications using the CIC filter. The filtration process consists of the reference samples that have been worked on in three stages, as illustrated in Figure 3.1.

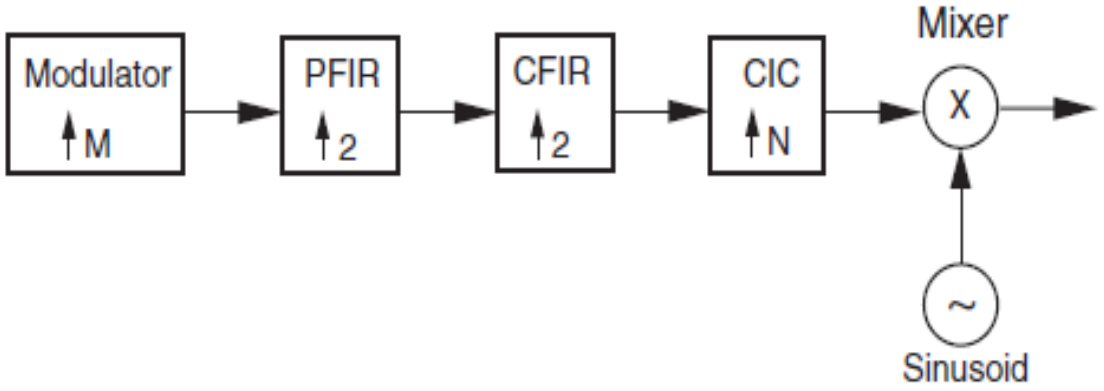

Figure 3.1: DUC architectural consideration [39].

3.2 TARGET SPECIFICATIONS

Requirements that must be worked in accordance with the transmission path of the downlink listed in Table 3.1. These requirements assume a normal base transceiver station (BTS) operating in the GSM 900 band.

Table 3.1: Target specifications GSM downlink transmission path

Parameter	Value	Comments
Channel Bandwidth	200 kHz	
Number of Carriers	4	
Baseband Symbol Rate	270.8333kbaud	
IF Sample Rate	69.3333 Msps	256 x 270.8333kbaud
Modulation Accuracy	5 degrees	RMS Phase error
Input Signal Quantization	12-bit I and Q	Complex
Output Signal Quantization	16-bit I and Q	Complex output is more general than real output

The design was done with the Simulink feature for its ability to use FDA tool in the loop. This special block also contains names and types similar to the original design ports, which provide useful features for work design and validation in the actual application. The panel consists of multiple properties and many purposes that can be used in many designs such as wireless communication applications. By using MATLAB Simulink the transceiver is designed by using communication block set as for data generation, a Random Integer Generator is used to create a signal as shown below.

As illustrated in Figure 3.2 we select the parameters as the M-ary number is set to 16 bit with Initial seed of 37 while we select the sample time is 2.1666 x 10-6 with output data type of double. As for Modulator a Rectangular QAM Modulator is used with the settings as shown in Figure 3.3 below.

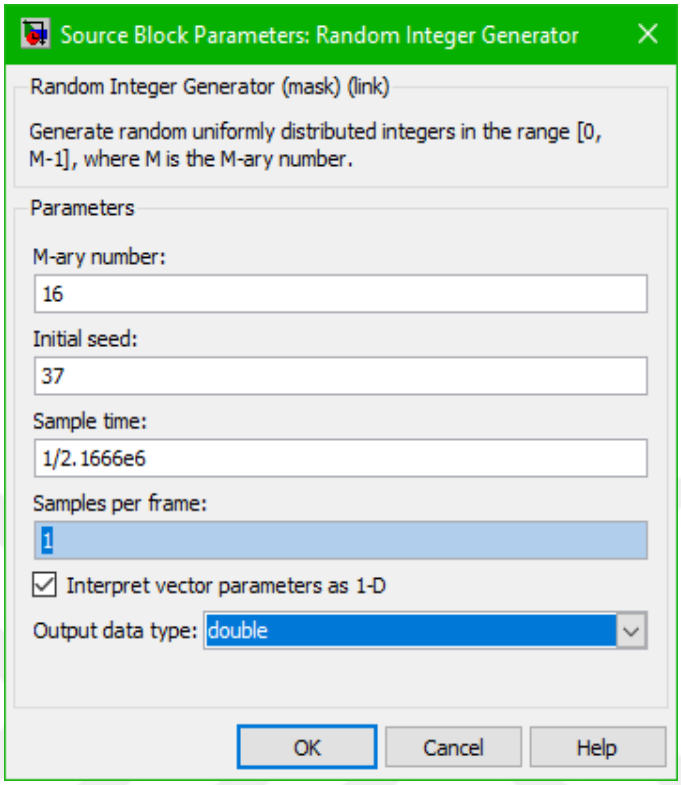

Figure 3.2: Random Integer Generator

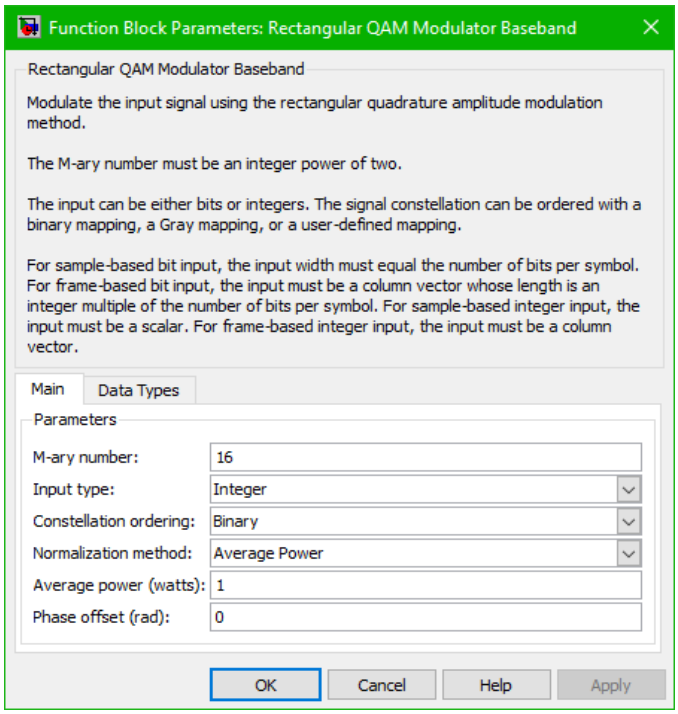

Figure 3.3: Rectangular QAM Modulator

3.3 DUC DESIGN AND SIMULATION

For the proposed design, MATLAB has been used in order to run the design, which has been programming into the Simulink. Many facilities are providing by Simulink tools are designed to be used to control the design during simulation, which is associated with the design of the computer. These ports have a design on the names and tools similar to the original. Figure 3.4 shows the main design of the DUC filter.

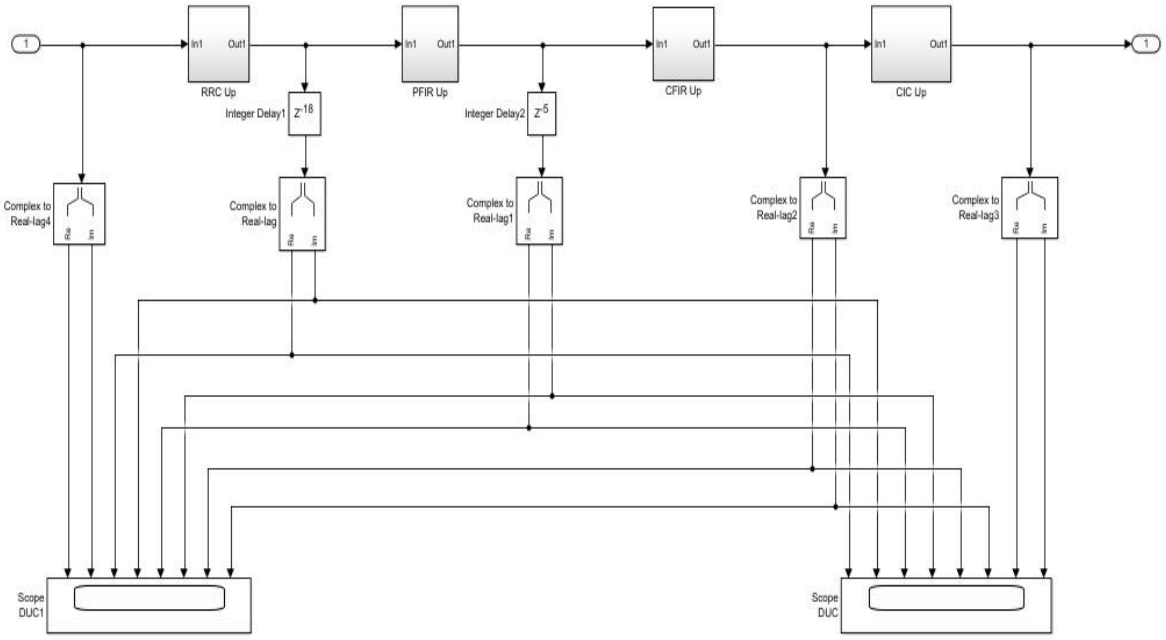

Figure 3.4: DUC block diagram in simulink

The chip rate for GSM is 2.166 MHz as is known and traded in the world of communications. Therefore, the sample rate must be made IF which is taken to be higher than the chip rate. The work will be designed with a sampling factor of 16, which means that the IF rate is 69.333MHz. The system clock must be set from simulink so that the result is consistent as it should be. We need to multiply the IF rate. The pulse is formed in the DUC filter and the interpolation and frequency translation are the processes performed in the design to meet the spectral signal sent in the design in order to meet the GSM requirements. Table 3.2 shows the GSM requirements in IF band.

Table 3.2: GSM requirements in IF band

Clock rate	2.166 MHz
Pass-band width	80kHz
DUC output rate	69.333MHz

The DUC design must be in accordance with the requirements of GSM. As mentioned above, in DUC, filtering shall be an important part to design and shall be designed with high accuracy according to the requirements of the spectral mask. The good way to design and work with high precision is to separate the stages of rate conversion and sampling into several interpolation stages instead of collecting up sample the rate in one stage.

3.4 ROOT RAISED COSINE

The RRC is a favorable condition filter that forms the impulse shaping where the transition bar is formed as a cosine curve to meet the Nyquist Criteria. In this process the signal needs to be removed aliasing effects from that gets in lifting the sample. There is one way to make a filter design by using the (FDA Tool). It is a graphical user interface (GUI) which allows the designer to work and adjust the specifications that he wants to work the candidate and according to specifications.Figure 3.5 shows the RRC filter design for the DUC. Figure 3.6 illustrates the magnitude response of the RRC filter in FDATool windows.

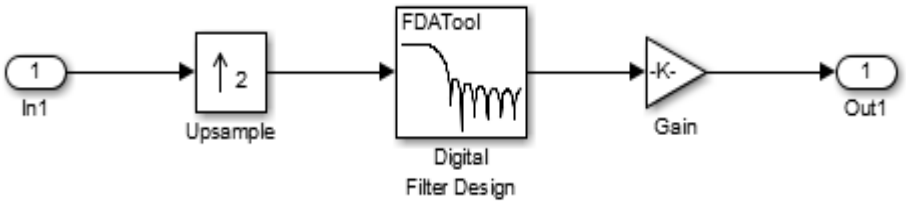

Figure 3.5: RRC filter design

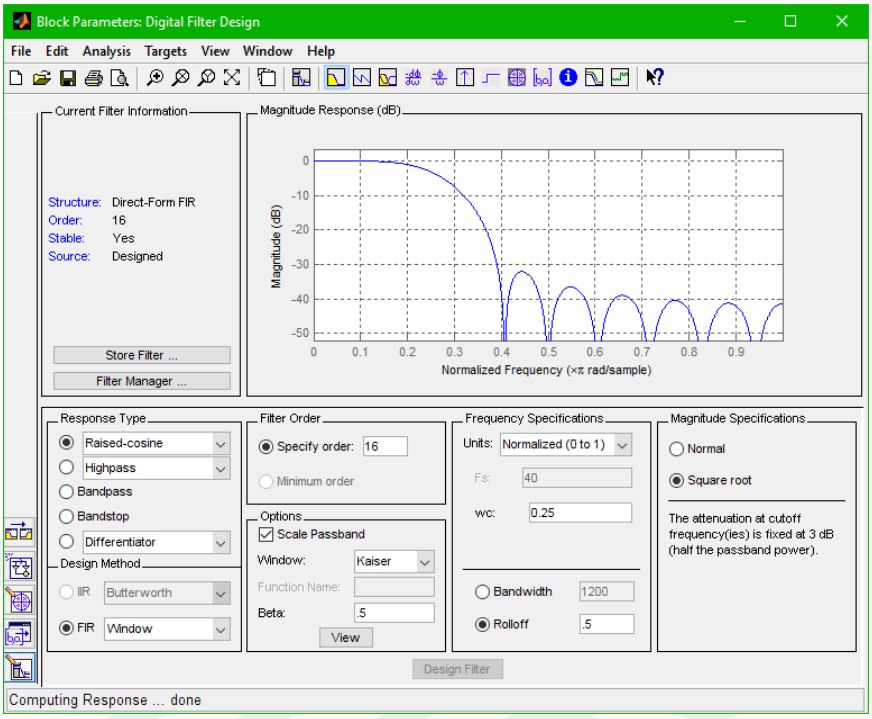

Figure 3.6: FDA tool with magnitude response

In the FDA tool, the response type is set to be Raised-cosine with design method as FIR (Window). As for the filter specified order of 16 and frequency specifications of Normalized (0 to 1) with wc=0.25, and magnitude specifications set to square root.

3.5 PFIR FILTER

After the signal has been up sampled to 4.33 MHz, the next stage is to enter another filter Programmable Finite Impulse Response (PFIR). It has up a sampling of 2 as shown in the Figure 3.7 below.

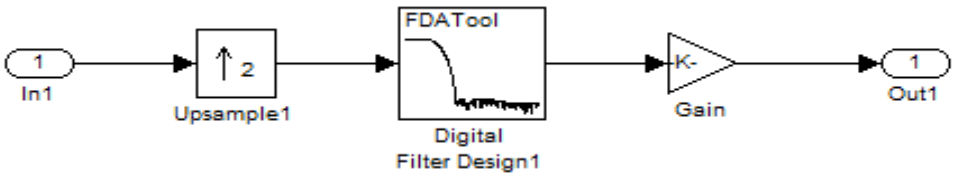

Figure 3.7: PFIR filter design

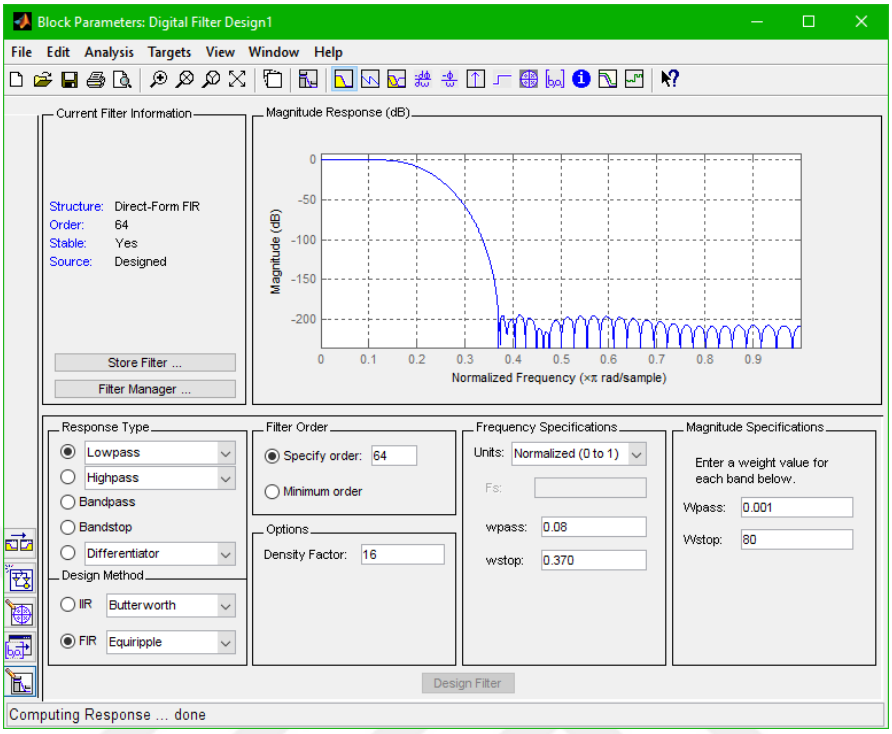

Figure 3.8: FDA Tool for the PFIR filter with magnitude response.

In this FDA Tool as shown in the Figure 3.8, the response type in it is lowpass and design method FIR Equiripple. The filter order is 64, as for the frequency specifications is normalized with wpass = 0.08 and wstop = 0.370.

3.6 CFIR FILTER

The third filter is Compensation Finite Impulse Response (CFIR) filter which will up sample the 8.66 MHz (which we got from the PFIR filter) by 2 as shown in the Figure 3.9 below where it shows the CFIR filter design.

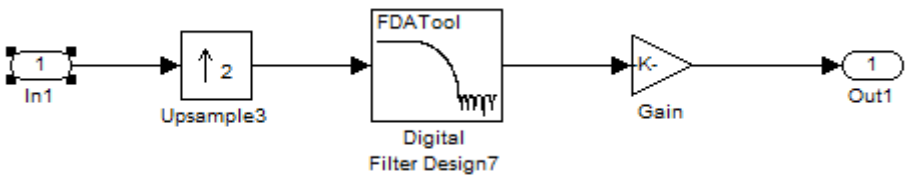

Figure 3.9: CFIR filter design

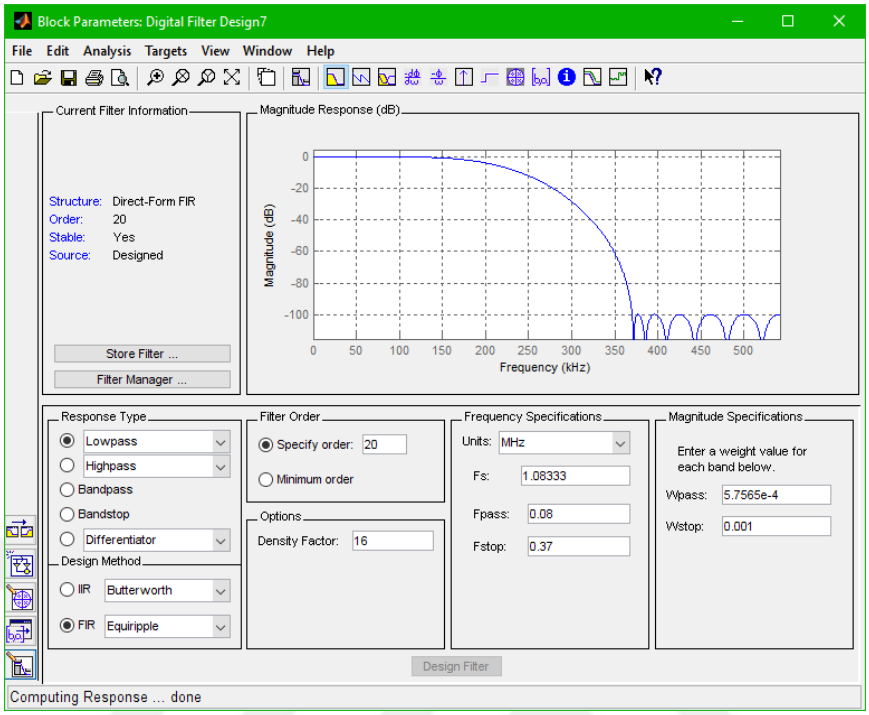

Figure 3.10: FDA Tool for the CFIR with magnitude response

The response type and the design method are the same as the PFIR as shown in the Figure 3.10, except the filter specified order is 20, and frequency specifications are in MHz with Fs=1.08333, Fpass= 0.08 and Fstop= 0.37. as for the magnitude specification, Wpass= 5.7565e-4 (where e-4 is 10^{-4} in Matlab form), and Wstop= 0.001.

3.7 CIC FILTER

Cascaded Integrator–Comb (CIC) is the final filter stage which will the signal go through before transmitting it through the channel. Figure 3.11 show the CIC filter design for the DUC.

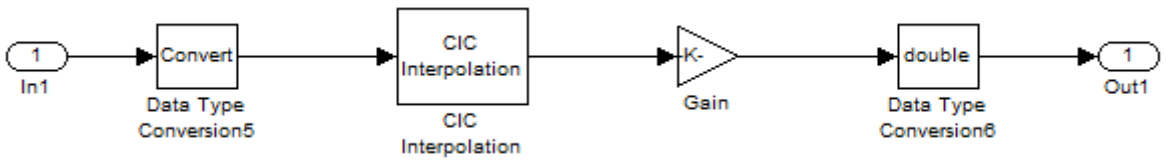

Figure 3.11: CIC filter design

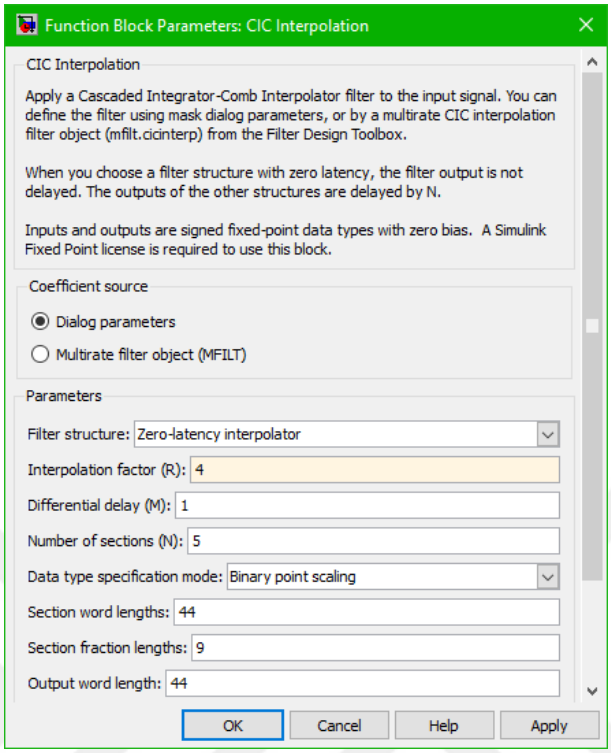

Figure 3.12: CIC interpolation parameters

In CIC interpolation, the coefficient parameters are set to dialog parameter where the filter structure is zero-latency interpolator, and interpolation factor R is 4 with Differentia delay M= 1 and number of sections N= 5, as shown in the Figure 3.12.

4. RESULTS AND DISCUSSION

4.1 RESULTS

This chapter contains the results obtained from the simulation using MATLAB. At the beginning of the process, the signal is created by Random Integer Generator as shown in Figure 4.1. The modulator is then executed by a Rectangular QAM Modulator, thus creating the signal as shown in Figure 4.2. Figure 4.3 shows the eye diagram of transmit signal and Figure 4.4 shows the Constellation diagram.

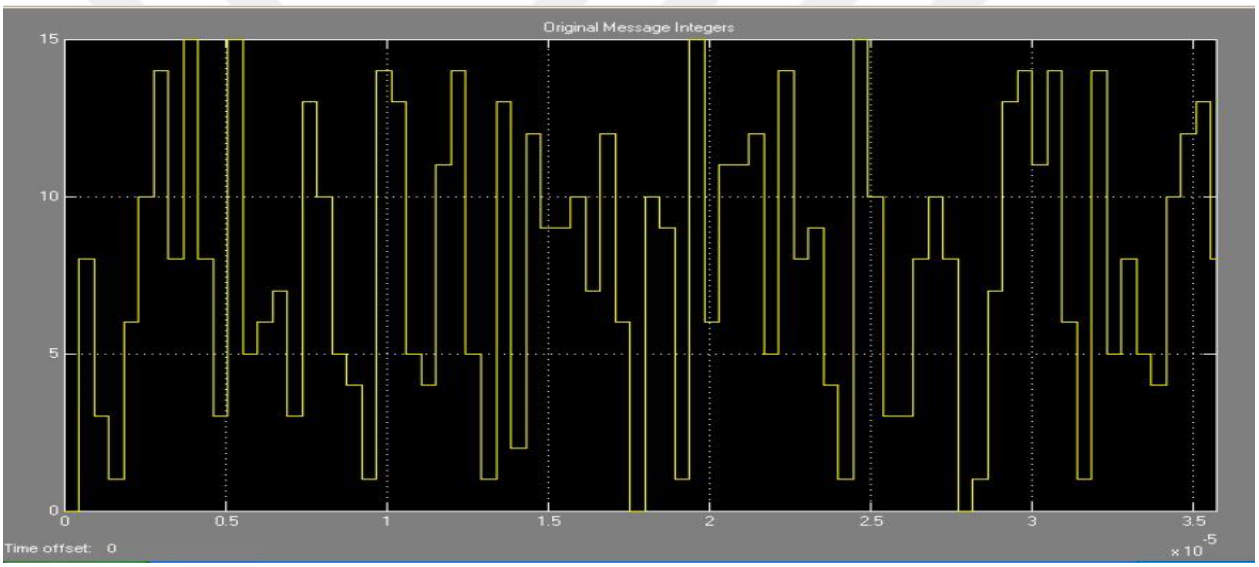

Figure 4.1: Original message integers

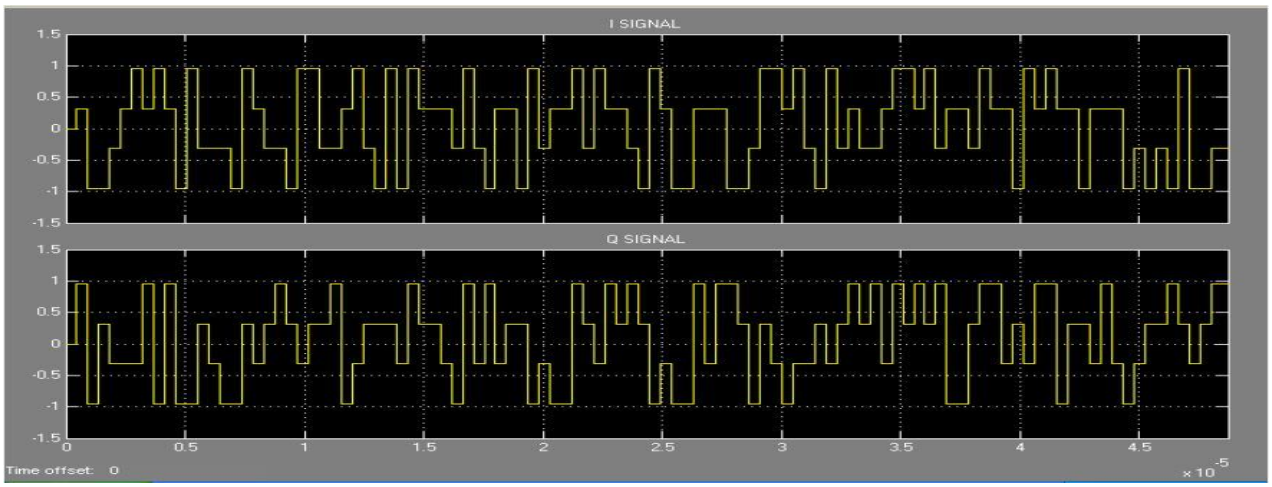

Figure 4.2: In-phase and Quadrature signals before DUC filter

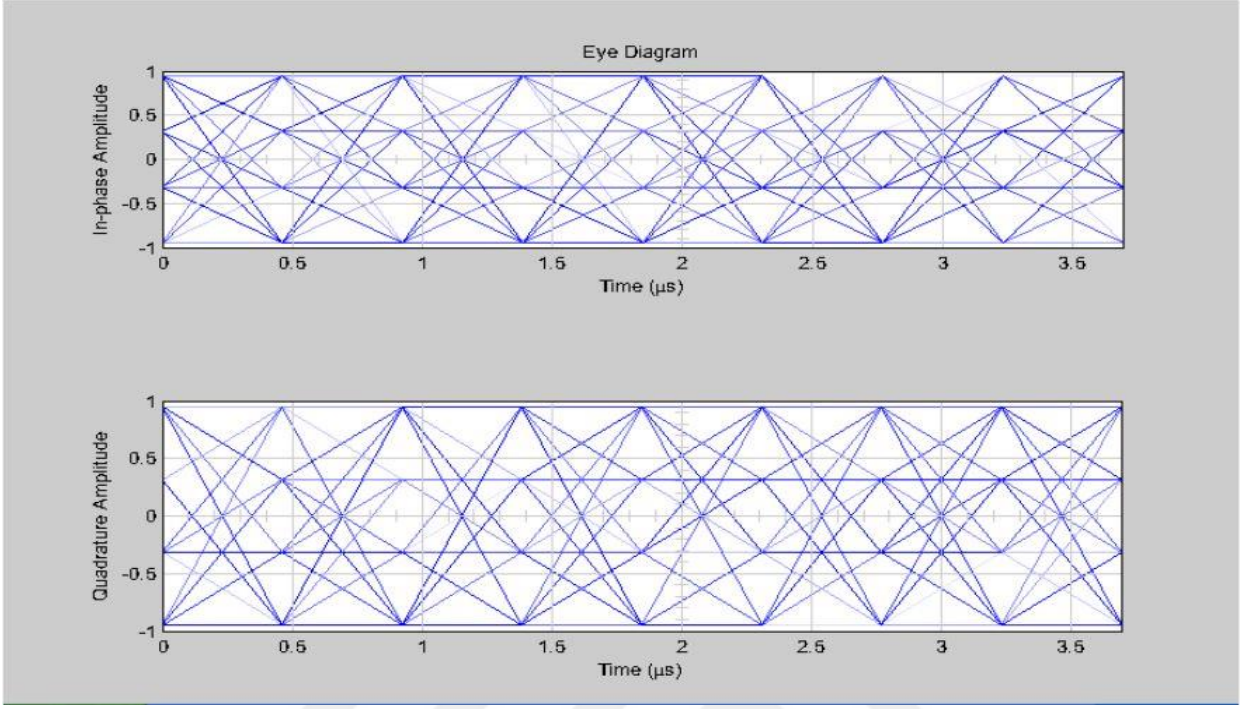

Figure 4.3: Eye diagram of transmit signal

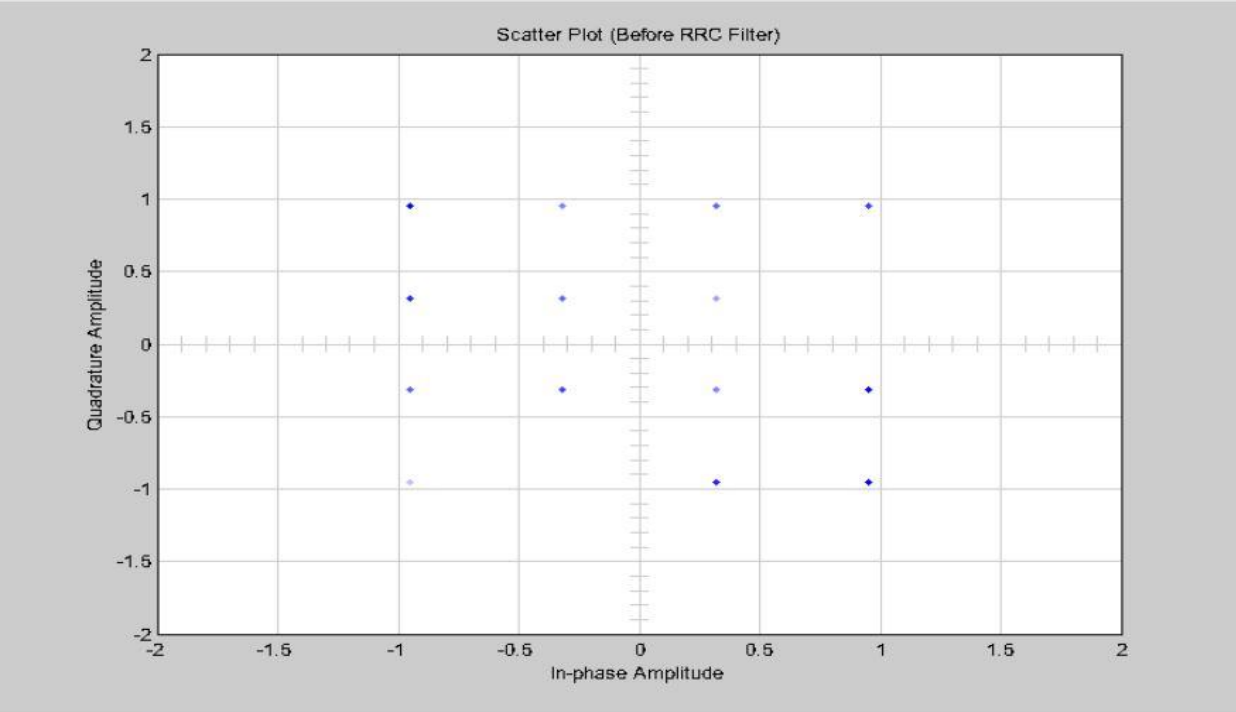

Figure 4.4: Constellation diagram of transmit Signal

At the beginning of process, the signal is formed inside the spectral mask like pulse shaped, thus satisfying the RRC filter design according to the requirements of GSM. The interpolation filter is also prepared according to GSM requirements, in the RRC channel. The signal is taken in samples by factor 8, so the input signal needs to be converted to 2 where the IF is 69.333MHz. The conversion rate is broken to indicate three stages of sequential filtering and since it is impractical to convert the signal at one time. The first sample is selected for the signal taken by Factor 8 and then each filter is calibrated by factor 2. The filter that has been used is the LPF filter because it is easy to operate and does not complicate hardware.

4.2 PULSE SHAPING FILTER

In this step, the pulse of the GSM mask is formed and samples are taken by factor 2. The technology used to adjust the transmitter and receiver signals is the 16QAM. Figure 4.5 illustrating the 16QAM waveforms, which is the output of the FIR filter. FDATool in MATLAB is used to design this filter.

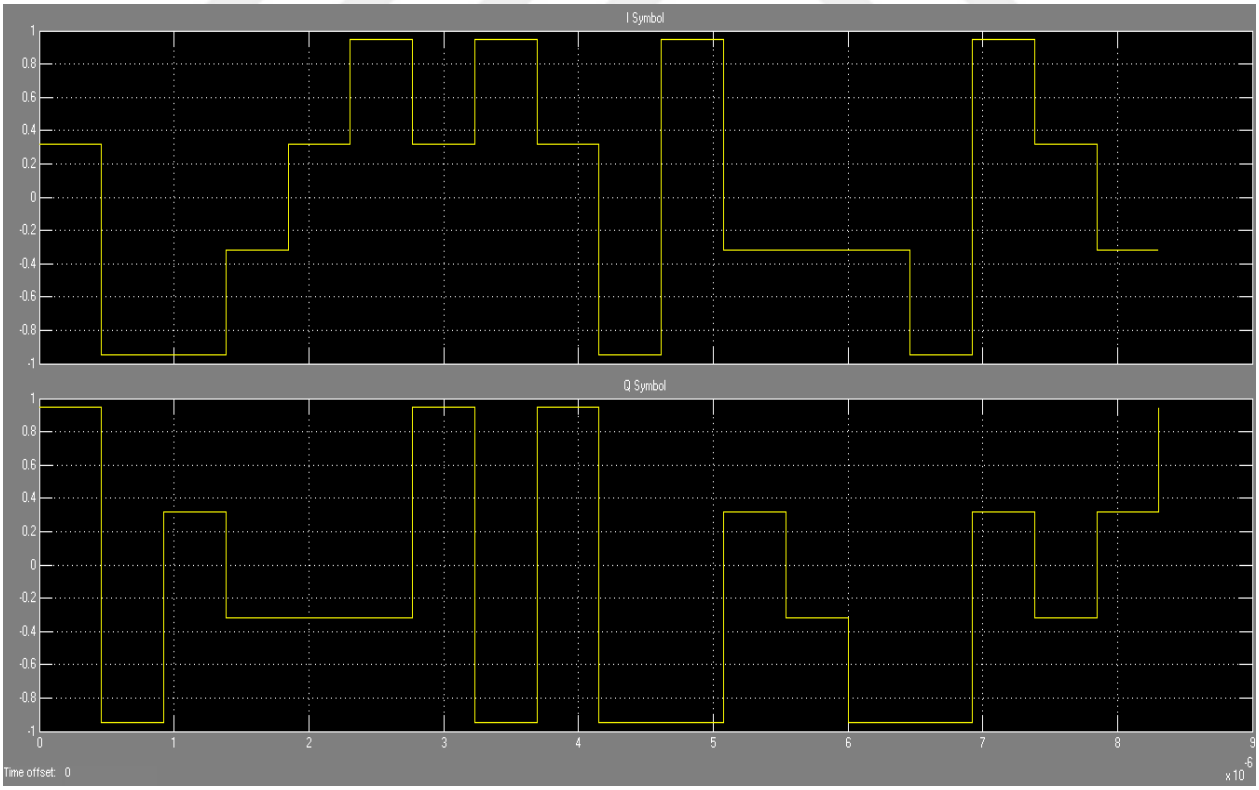

Figure 4.5: Pulse shaped waveform of 16QAM

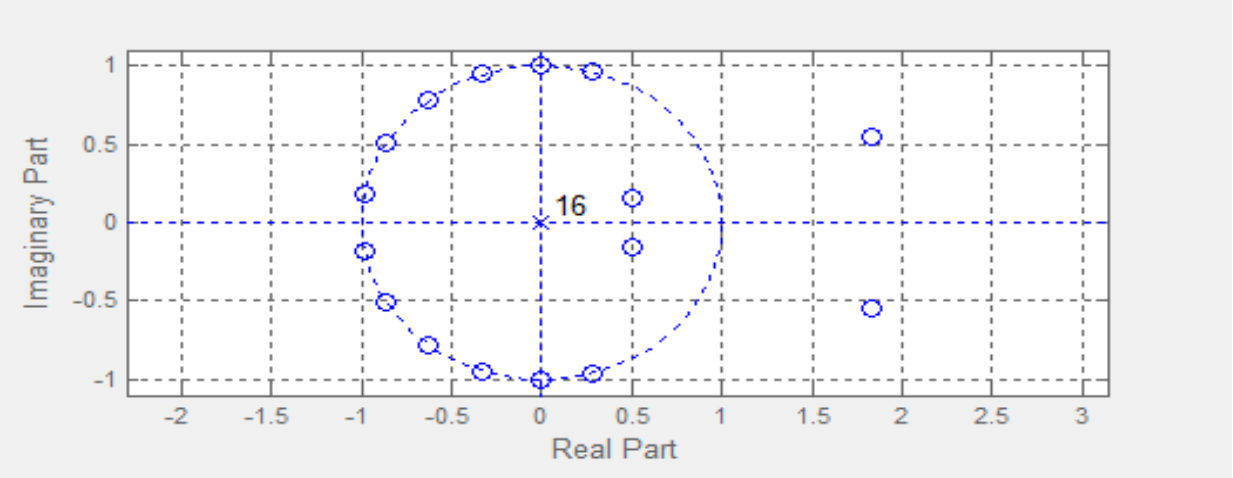

Figure 4.6: Pole/Zero response of RRC filter

The RRC filter sample rate is F1 = 2.166 x 2 = 4.33 MHz. Figure 4.6 shows a closer look at the Pole/Zero response.

4.3 FIRST STAGE FILTER (PFIR)

The first stage in the DUC filter is the Programmable FIR filter which is used to up-sample the GSM signal by 2 and improves the waveforms performance in the baseband level. Figure 4.7 shows the output waveforms of the PFIR filter.

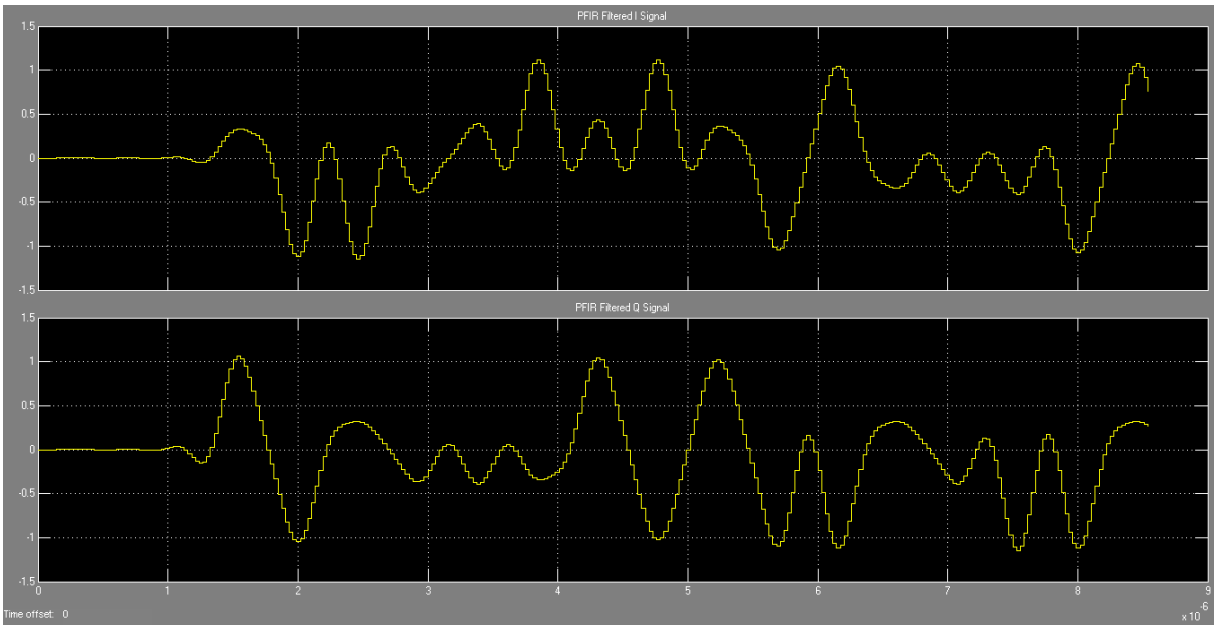

Figure 4.7: The output waveform of first stage PFIR filter

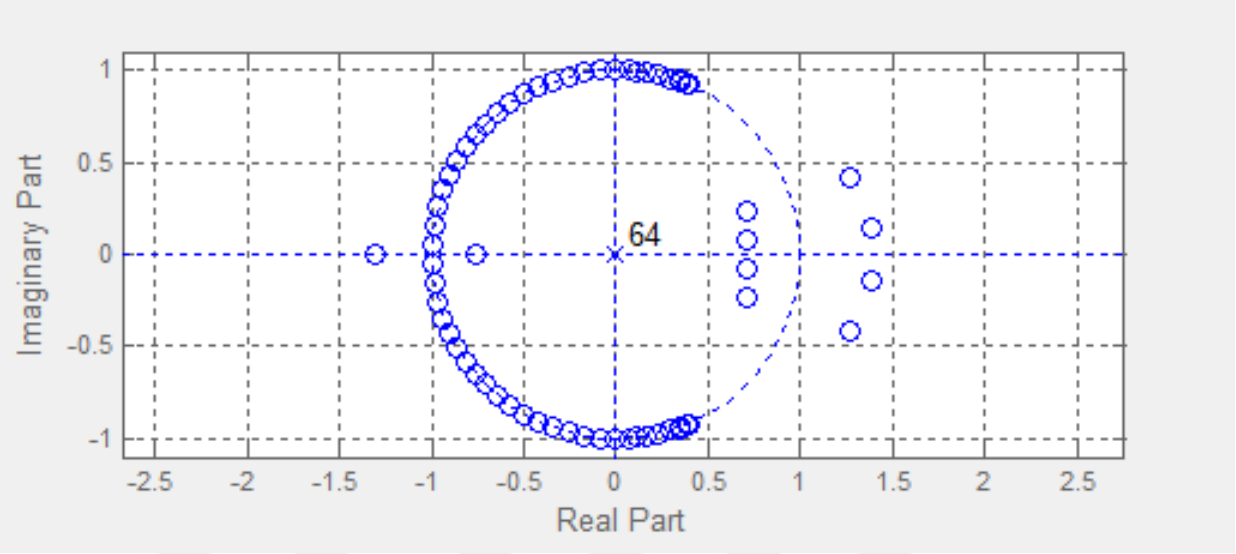

Figure 4.8: Pole/Zero response of PFIR filter

The fiest LPF interpolator filter is F2 = 4.33 x 2 = 8.66 MHz as illustrated in Figure 4.8 a closer look at the Pole/Zero response.

4.4 SECOND STAGE CFIR FILTER

Figure 4.9 shows the output waveforms of the compensating FIR filter. Its clear from this waveform that, the baseband signal is filtered and up-sampled to a higher frequency than first stage output.

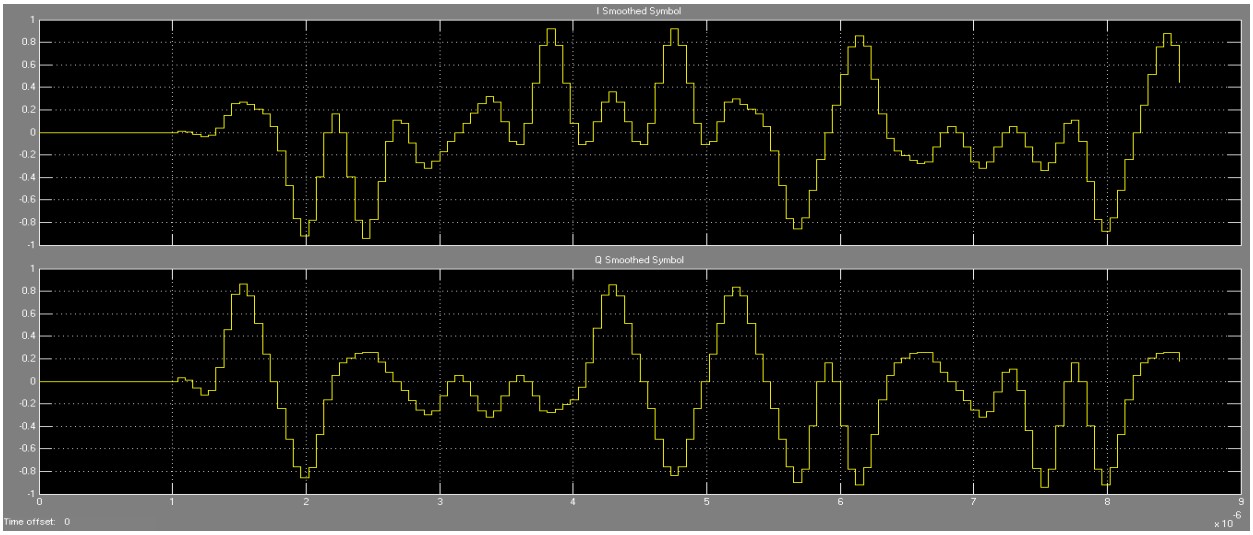

Figure 4.9: The output waveforms of the CFIR filter

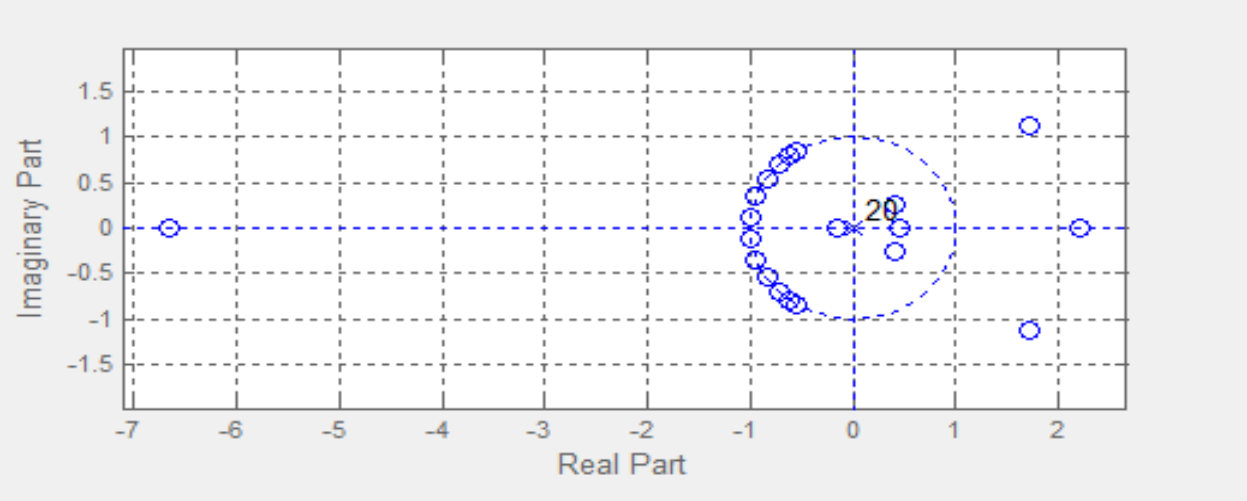

Figure 4.10: Pole/Zero response of CFIR filter

The second stage LPF interpolator filter sample rate is F3 = 8.66 x 2 = 17.328 MHz as shown in Figure 4.7 a closer look at the Pole/Zero response.

4.5 THIRD STAGE CIC FILTER

The CIC filter in the final stage is up-sampled the signal by 4 and 5-cascaded filter and the signal go through before transmitting it through the channel F4= 17.328 x 4 = 69.333 MHz. Figure 4.11 shows the output waveforms of the CIC filter with 69.333MHz.

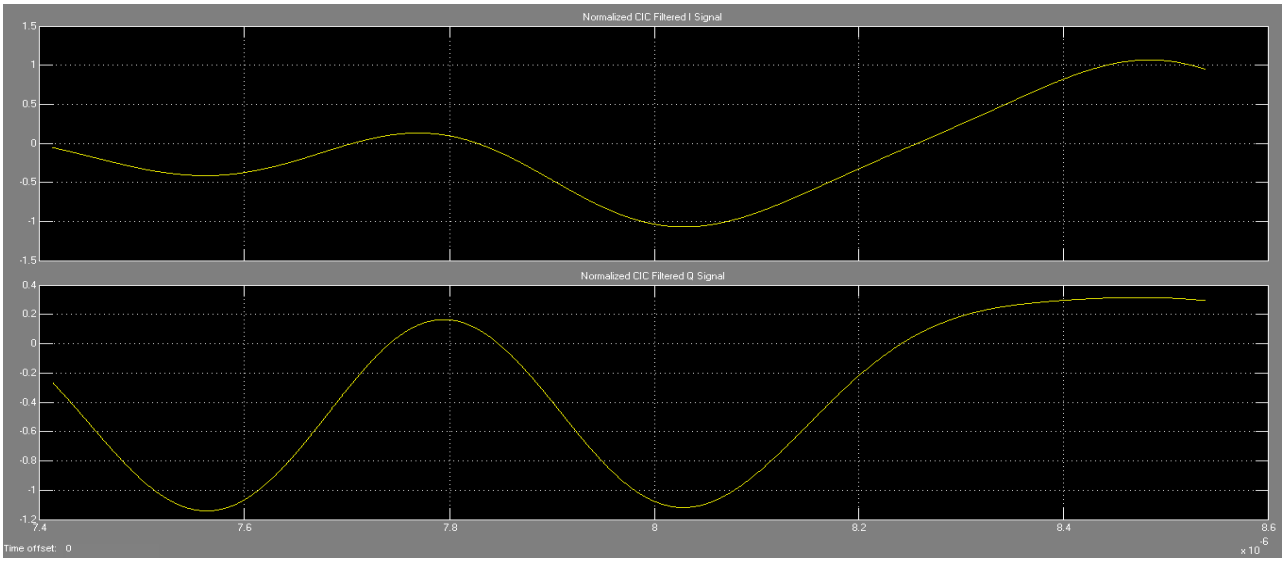

Figure 4.11: The output waveform of the CIC filter

From the results shown in Figure 4.12 and Figure 4.13, the signal was first formed by the RRC filter. The signal samples were taken from 2.166 MHz and raised to 69.333MHz by different stages using the FIR filter, PFIR and CFIR. Finally, the signal is taken from the CIC filter and the channel Set to move the signal

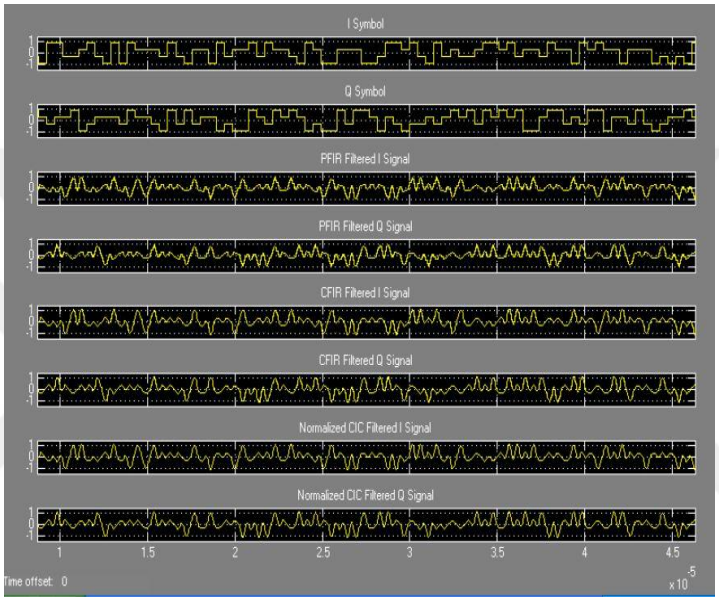

Figure 4.12: The DUC signal with up sampling

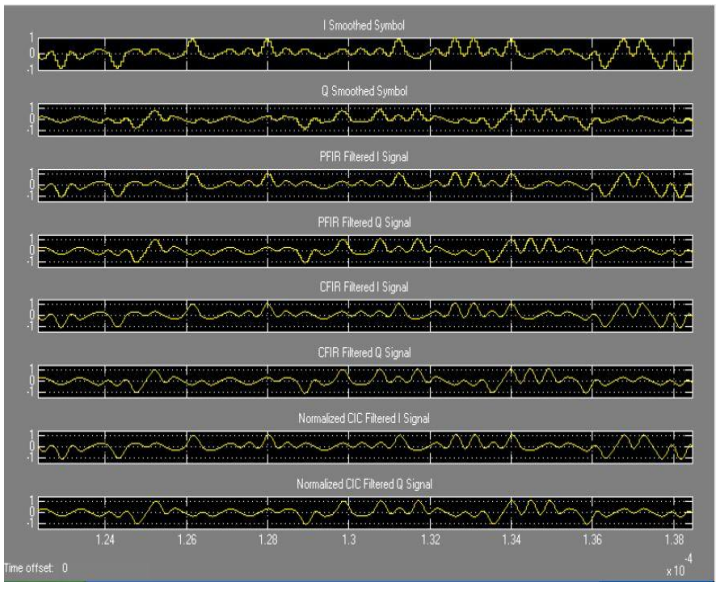

Figure 4.13: In-phase and the Quadrature smoothed signals

After taking the sample rate and raising it from 2.166 MHz to the IF rate of 69.333MHz by separating the sampling operations into several ways to achieve a good result and thus achieve the requirements of GSM. In Figure 4.14 the output of DUC signal

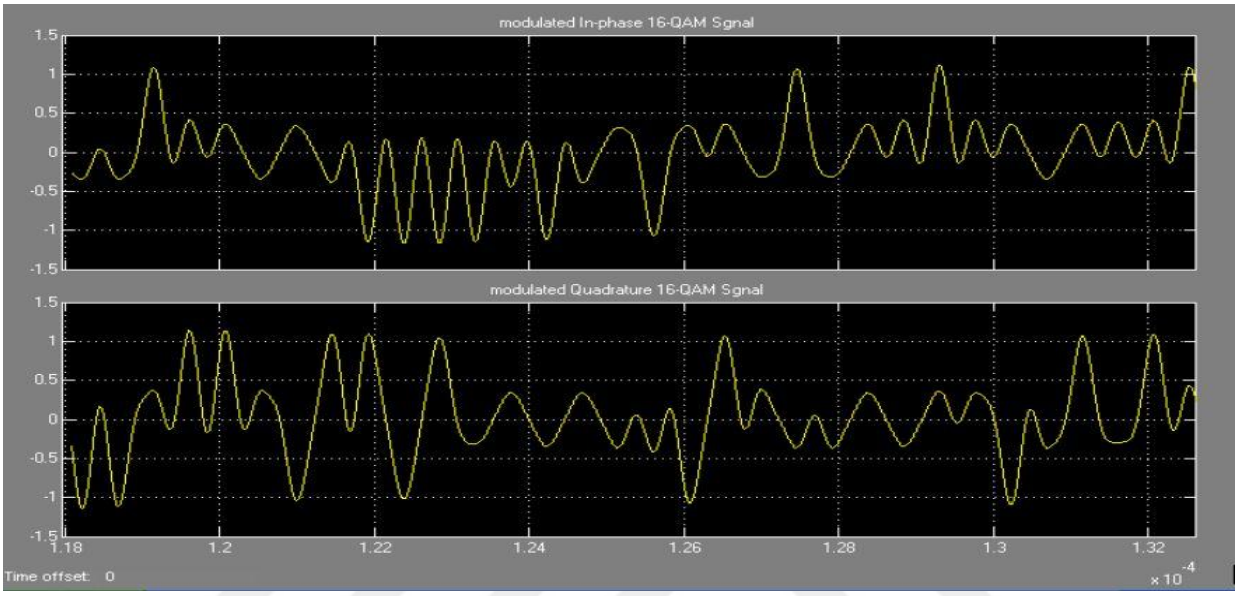

Figure 4.14: The DUC output signal

4.6 TRANSCEIVER

To check the DUC works properly, both signals at the transmitter and receiver are compared to each other by subtracted the two signals as shown in the Figure 4.15 below of the scope.

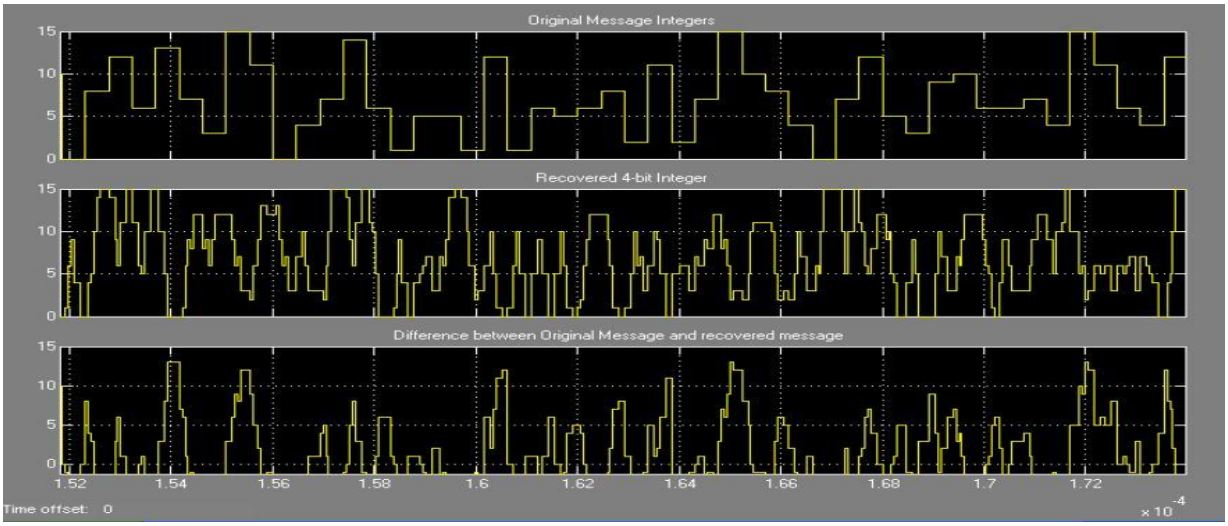

Figure 4.15: Signal compartion

As shown the difference between the original signal and the received signal is very small due to the noise in the channel.

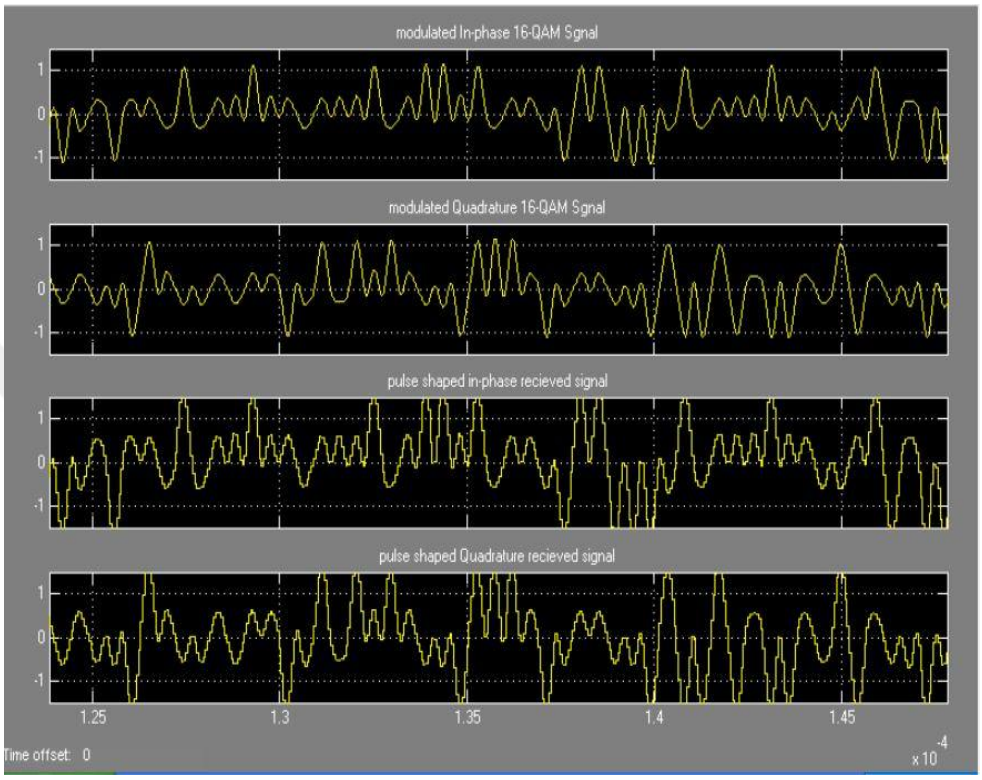

Figure 4.16: Compartion of the In-phase and Quadrature signals

Figure 4.16 above shows the In-phase and the quadrature signals of the original signal and the recovered signal where they are very identical to each other.

With this, the preposed DUC proved to work and meet the requirements that is needed from it.

5. CONCLUSION AND FUTURE WORK

In this paper, the DUC filter is designed according to the requirements of the global GSM. The GSM system is designed to send and receive wireless signals effectively and quickly compared with existing designs that operate on DSP filters. The efficiency of the design is due to the use of FIR filters, which have been used by multipliers basis in the design and implementation of GSM DUC. In this design, pulse shaping filters and other interpolators have been developed separately and then cascaded together to implement the design of GSM DUC. In this paper the DUC filter is designed and implemented for the SDR technology based on GSM systems. The designed filter is providing minimum ripple in passband part to decrease the power consumption and increase the filter memory compared with traditional and current DUC filter. The algorithms are used in the multi-stage Equiriple FIR digital filter and have helped to reduce the length of the filter as well as the computational complexity and thus become better in working to enhance the filter rate. The advanced GSM DUC system has shown improved speed, lower cost and the use of resources to offer efficient solutions for mobile SDR-based mobile request.

The proposed project is designed and simulated using MATLAB only and we can observe from the simulation results that show that the DUC filters are more effective, which makes it can move from the academic idea to implementation on FPGA in real-time mode by other people in future.

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