DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

CURRENT CONTROLLED CURRENT CONVEYORS AND ITS APPLICATIONS

by
Sinem ÖZTAYFUN

July, 2006
İZMİR

CURRENT CONTROLLED CURRENT CONVEYORS AND ITS APPLICATIONS

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Electrical and Electronics Engineering

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İZMİR

M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"CURRENT CONTROLLED CURRENT CONVEYORS AND ITS APPLICATIONS"** completed by **SİNEM ÖZTAYFUN** under supervision of **ASSOC. PROF. DR. UĞUR ÇAM** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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Sinem ÖZTAYFUN

CURRENT CONTROLLED CURRENT CONVEYORS AND ITS APPLICATIONS

ABSTRACT

In this thesis, all types of current conveyors from the invention of the first type, first generation current conveyor, and their applications are discussed and the most emphasized one is current controlled current conveyor. The main variety of the current controlled current conveyor (CCCII) is providing electronic adjustibility by parasitic resistance R_X. This parasitic resistance can be changed by applied bias current I_0. Besides electronic tunability, CCCII has several advantages as less power consumption, less complex structures, and better frequency performance when it is compared with operational transconductance amplifier (OTA) and opamp. Because of its advantages, filters that have controllable functions according to center frequency, gain or quality factor, oscillators with adjustable frequency, and inductance simulations with controllable value are designed. Then, the proposed circuits are simulated by using PSpice simulation program and it is observed that simulation results confirm theory. During the design, it is tried to use minimum number of active and passive components.

Keywords : current controlled current conveyors, filters, oscillators, inductance simulation.

AKIM KONTROLLÜ AKIM TAŞIYICILARI VE UYGULAMALARI

ÖZ

Bu araştırmada, ilk çeşidi olan ilk nesil akım taşıyıcısının buluşundan itibaren tüm akım taşıyıcı çeşitleri ve uygulamaları ele alınmıştır ve üzerinde önemle durulan çeşidi ise akım kontrollü akım taşıyıcısıdır. Akım kontrollü akım taşıyıcısının en önemli üstünlüğü, parazit direnç R_X ile elektronik ayarlanabilirlik sağlamasıdır. Bu parazit direnç uygulanan bias akımı I_0 ile değiştirilebilir. Elektronik ayarlanabilirliğin yanısıra, CCCII ; OTA ve opampla karşılaştırıldığında daha az güç tüketimi, daha az karmaşık yapılar ve daha iyi frekans performansı gibi birçok avantaja sahiptir. Bu avantajlarından dolayı, kesim frekansı, kazancı veya nitelik katsayısına göre kontroledilebilir fonksiyona sahip filtreler, ayarlanabilir frekansı olan osilatör ve kontroledilebilir değere sahip endüktans simülasyonları tasarlanmıştır. Daha sonra önerilen devrelerin simülasyonları PSpice simülasyon programı kullanılarak yapılmış ve simülasyon sonuçlarınn teoriyi doğruladığı gözlenmiştir. Dizaynları sırasında, minimum sayıda aktif ve pasif eleman kullanmaya özen gösterilmiştir.

Anahtar kelimeler : akım kontrollü akım taşıyıcıları, filtreler, osilatörler, endüktans simülasyonu.

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CHAPTER ONE
INTRODUCTION

Current conveyor that is represented by a basic building block with three ports make current, applied to one port, flow through other ports and its ports' impedances have different impedance level. Because of this property, it has an advantage to use in current mode circuits that have priority in terms of speed, bandwidth, accuracy, and less complex circuitry over the voltage mode circuits.

Current conveyor was first introduced as first generation current conveyor (CCI) in 1968 by Adel S. Sedra and Prof. K. C. Smith. The next version of current conveyor, CCII, which was introduced in 1970 by A. Sedra provides versatility in design with new equations by eliminating current in one port. The third version was third generation current conveyor (CCIII) was developed in 1995 by Alain Fabre. Current controlled current conveyor (CCCII) which was designed in 1996, is controllable because of its parasitic resistance adjusted with applied bias current. In the circuits that are designed with this version, there is a programmable property. In chapter two, there is information about curent conveyors, their advantages in spite of OTA and opamp, and their applications.

Because of current controlled current conveyor's programmable property, it is used in design of filters, oscillators, and an inductance simulation which are mentioned in chapter three. In fiter design; by adjusting of bias current, their center frequency, quality factor, and gain can be controllable. The simulation and theoritical results are also compared in this chapter.

In oscillator design, oscillation frequency can be adjustable under a condition which depends on bias current of current controlled current conveyor. Their equations and simulation results also take place in chapter three.

Lastly, inductance simulation is lossless and adjustable according to bias current of CCCII is discussed with its equations. There is also ideal simulation results of lossless inductance simulation in chapter three.

In the last chapter, chapter four, conclusion part takes place.

CHAPTER TWO
THE CURRENT CONVEYOR

2.1 First Generation Current Conveyor (CCI)

In 1968, First generation current conveyor was firstly suggested. Adel S. Sedra's Master thesis under the supervision of Prof. K. C. Smith at the University of Toronto, was design of programmable instruments for incorporation in a system for computer controlled experiments. In that work, a voltage controlled waveform generator was designed. But according to his design the control variable was current not voltage that required. At that time, to convert voltage to current, using a grounded-base pnp transistor and connect its emitter via a resistor to the positive control voltage was the best known solution. But the finite V_{EB} caused a large offset in the voltage to frequency conversion; moreover it depended on temperature and on the flowing current, getting worse the stability and linearity of the entire circuit.

To overcome these drawbacks and convert a better voltage to current convertor, another junctions were used. To compensate for the V_{EB} of the current source pnp transistor, a matched pnp transistor was connected as a diode and additional pnp transistor to arrange the current. The solution of converting a voltage to current was a circuit which was called CCI or first generation current conveyor with five transistors proposed by Sedra and Smith (1968) shown in Figure 2.1.

The operation of this device is such that if a voltage is applied to input terminal Y, an equal potential will appear on the input terminal X. In a similar fashion, an input current I being forced into terminal X will result in an equal amount of current flowing into terminal Y. As well, the current I will be conveyed to output terminal Z such that terminal Z has the characteristics of a current source, of value I, with high output impedance. As can be seen, the potential of X, being set by that of Y, is independent of the current being forced into port X. Similarly, the current through input Y, being fixed by that of X, is short-circuit input characteristics at port X and a dual virtual open-circuit input characteristic at port Y (Sedra and Roberts, 1990).

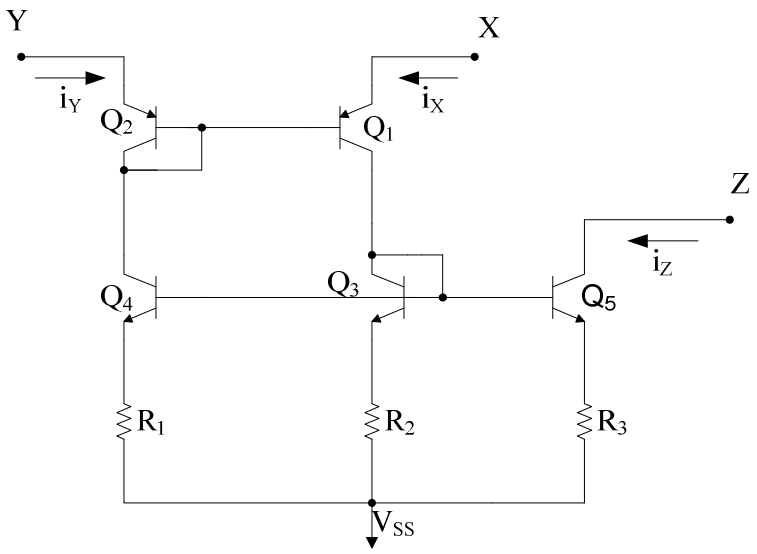


Figure2.1: First order bipolar implementation fo CCI

The circuit of the Figure 2.1 can be considered as an implementation of a three port network represented by the block diagram of Figure 2.2 and described by;

$$\begin{bmatrix} i_Y \\ V_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ V_Z \end{bmatrix} \tag{2.1}$$

where the variables represent total instantenous quantities (Sedra and other, 1990).

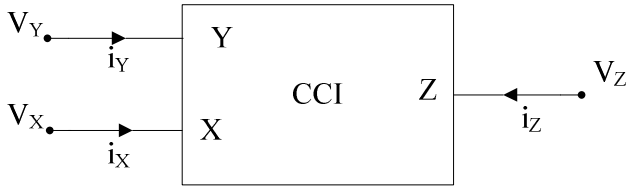


Figure 2.2: Block box representation of CCI

A nullator-norator representation, commonly referred to as a nullor, as shown Figure 2.3 can be used to illustrate the the relationship between port voltages and currents of current conveyor. A nullator (represented by a single elipse) is an ideal two terminal circuit element which enforces both zero voltage and zero current

between its terminals X and Y in the Figure 2.3. A norator (represented by two intersecting elipses) is an ideal two terminal circuit element which imposes no constraints on its branch current and voltage.

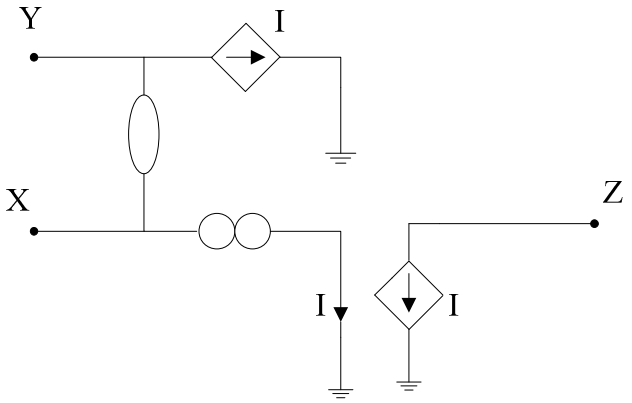


Figure 2.3: Nullator-norator representation of CCI

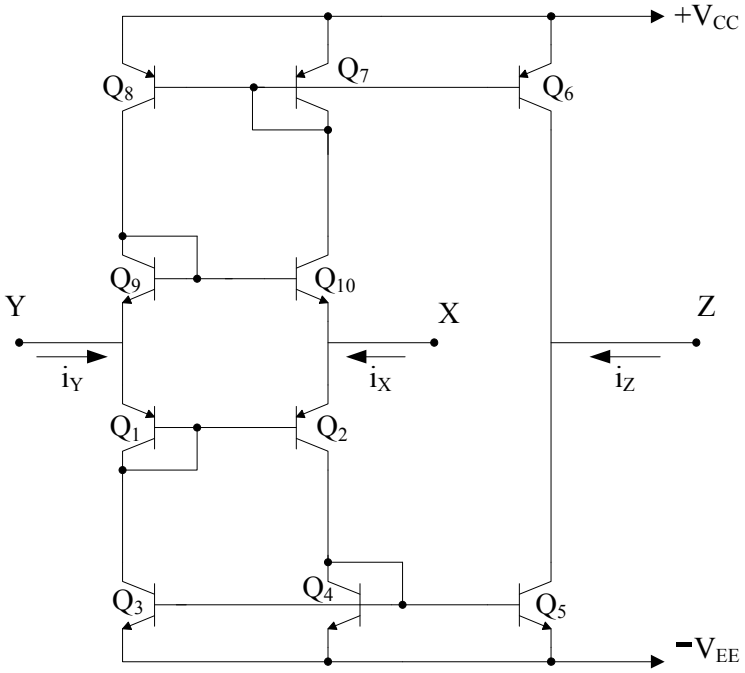


Figure 2.4: A class AB implementation of CCI

Another circuit for current conveyor is a class AB implementation as shown in Figure 2.4 using more detailed than the first circuit of current conveyor quoted from

Sedra and other (1990). In this circuit the polarity of the output current at Z can be inverted by using an mirror stage. Also, the entire circuit may be inverted as pnp transistors is replaced by npn transistors and vice versa, and the negative power supply is is replaced by a positive power supply.

A major problem that hindered fabrication of the CCI im IC form in the 1960s is its use of high quality pnp devices. Since complementary devices are available in CMOS technology, it is easy to fabricate a CMOS current conveyor of the type shown in Figure 2.5 (Sedra and other, 1990).

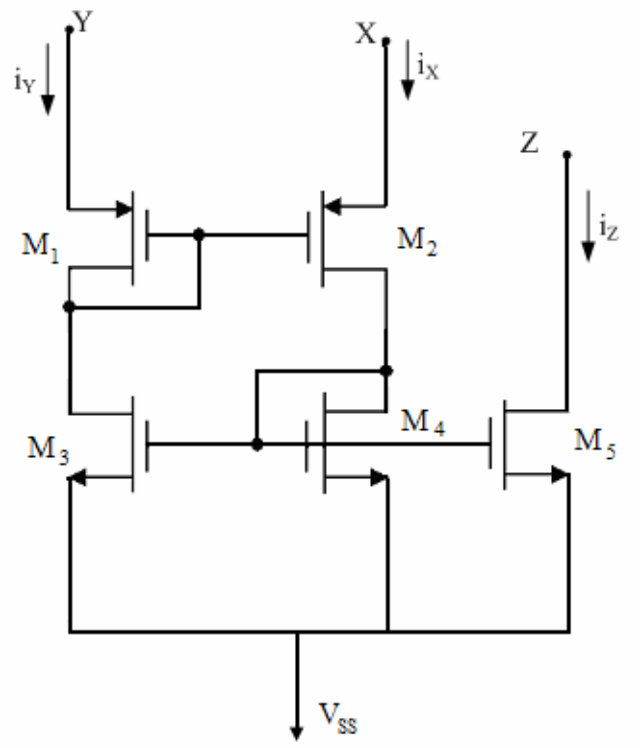


Figure 2.5: First order CMOS implementation of CCI

2.2 Second Generation Current Conveyor (CCII)

In 1970, at the first IEEE International Symposion on circuit theory, later named ISCAS, the second generation of current conveyor which was developed to increase of the versatility was introduced. In this version, there is no current flows in terminal Y. The relationship between ports voltages and currents are described by the following matrix equation .

$$\begin{bmatrix} i_Y \\ V_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ V_Z \end{bmatrix} \tag{2.2}$$

According to this equation terminal Y exhibits an infinite input impedance, voltage of terminal X follows Y voltage that is applied, so X shows a zero input impedance. The current that is supplied to terminal X is conveyed to terminal Z which has a high output impedance in same polarity or opposite polarity, ±1 represents this feature. It can be understood from this property that, there are two types of second generation current conveyor; CCII+ whose terminal Z has same polarity with terminal X and CCII-whose terminal Z has opposite polarity with terminal X. Block box representation of CCII is shown in Figure 2.6 where ± denotes positive and negative types, respectively.

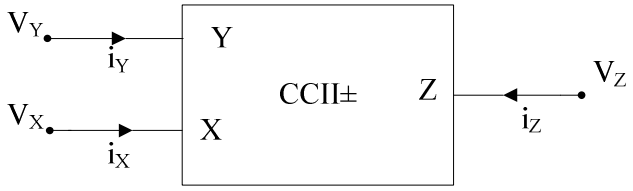


Figure 2.6: Block box representation of CCII±

If current and voltage tracking errors are examined the matrix equation of second generation current conveyor is described by

$$\begin{bmatrix} i_Y \\ V_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta & 0 & 0 \\ 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ V_Z \end{bmatrix} \tag{2.3}$$

where $\beta = 1 - \varepsilon_i$, $|\varepsilon_i| \ll 1$, $\alpha = 1 - \varepsilon_v$, $|\varepsilon_v| \ll 1$, ε_i and ε_v denotes current and voltage tracking errors respectively. Although these errors are very small. They are considered as effects of nonidealities in designs.

A nullor representaion of CCIIs are shown in Figure 2.7. When dependent current source direction is the same as current I, it represents CCII+, and when dependent current source direction is the opposite of current I, it represents CCII-.

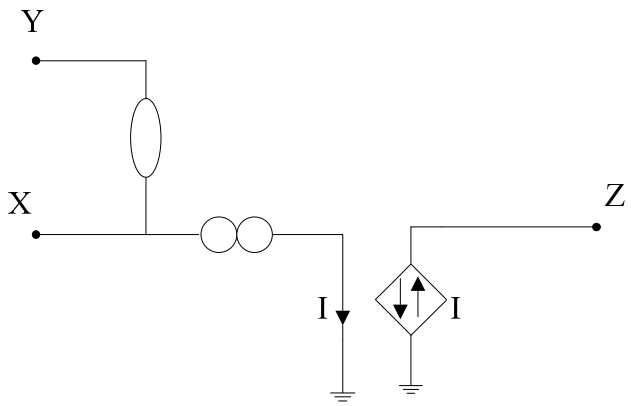


Figure 2.7: Nullor representation of CCIIs

The circuit implementation of the positive second generation current conveyor is shown in Figure 2.8. The first circuit implementaiton is the positive current conveyor since the negative current conveyor can be considered an extension of the positive current conveyor. In the implementation, simple current mirrors are used despite their low impedance and poor current gain. The reason behind this choice follows from the allowable signal swing at the X terminal. The positive signal swing of the X terminal is determined by the state of the transistor M_1 while the negative signal swing is determined by M_2. As long as both transistors remain saturated, the output stage of the opamp will perform as expected. Thus, the negative signal swing is restricted to $V_{ds\ sat2}$ above the negative input bias voltage of the of the n channel

current mirror, while the positive signal swing is restricted to $V_{ds\ sat1}$ below the positive input bias voltage p channel current mirror. Since the supply lines are limited to ± 5V, the use of current mirrors with large input bias voltages would severly restrict the signal swing at terminal X (Sedra and other, 1990).

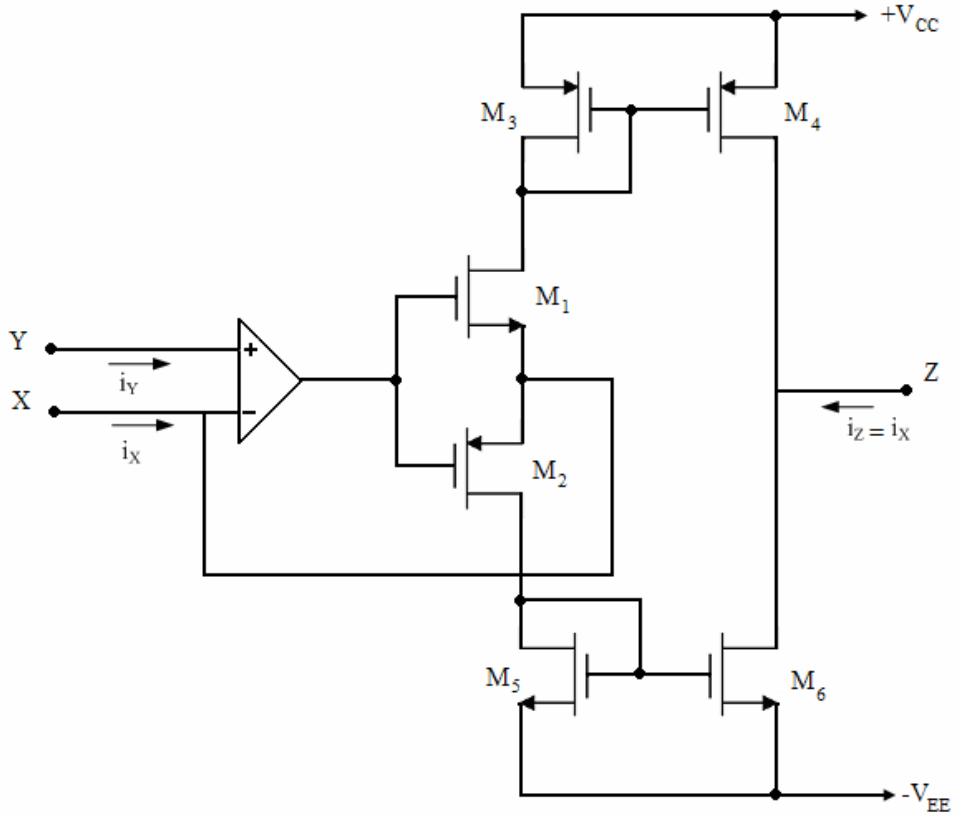


Figure 2.8: Positive second generation current conveyor CCII+

An another implementation of CCII+ with mixed translinear loop is shown in Figure 2.9. The mixed translinear loop consists of Q_1, Q_2, Q_3, and Q_4. When the circuit is DC biased by two I_0 currents, in terminal Y there is a high input impedance. Two complemetary current mirrors which are obtained by Q_7-Q_8 and Q_5-Q_6 pair transistors provide to duplicate at terminal Z the current flowing through terminal X. The difference between this translinear CCII+ and implementation including operational amplifier is exhibiting better frequency response.

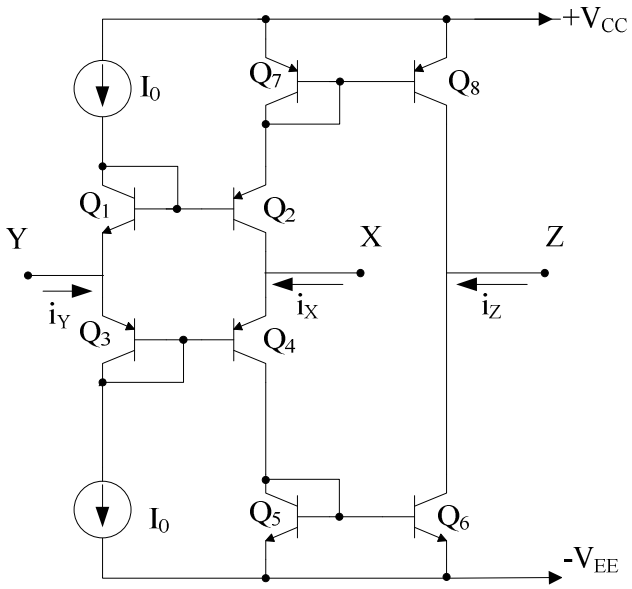


Figure 2.9: Schematic form of the translinear CCII+

A negative current conveyor using simple current mirrors is shown in Figure 2.10. the negative current conveyor circuit can be derived from positive current conveyor through the addition of two current mirrors. Unlike the current mirrors of the positive current conveyor, the additional current mirrors are not restricted to small input voltages. As such, either simple or stacked current mirrors can be used to achieve different current conveyor performances (Sedra and other, 1990).

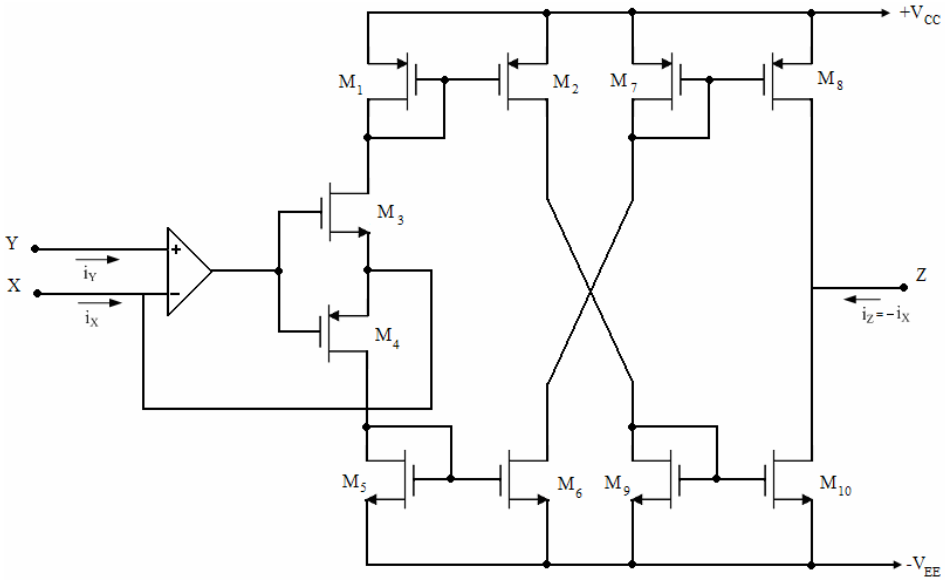


Figure 2.10: Negative second generation current conveyor CCII-

Besides positive and negative types of CCII, there is an another type that dual output second generation current conveyor (DO-CCII). Block box representation of DO-CCII is shown in Figure 2.11. It is combined of CCII structures.

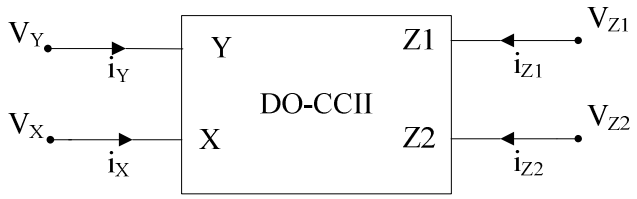


Figure 2.11: Block box representation of DO-CCII

Its definition relation is described by the following matrix equation.

$$\begin{bmatrix} V_X \\ i_Y \\ i_{Z1} \\ i_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ k & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_X \\ V_Y \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{2.4}$$

If k is equal to 1, it will be DO-CCII+ whose both Z outputs have same polarity. If K is equal to -1, it will be DO-CCII whose Z outputs have opposite polarity. Its implementation can be realized with bipolar or CMOS technologies.

2.3 Third Generation Current Conveyor (CCIII)

In 1995, the third generation current conveyor (CCIII) was introduced by Alain Fabre. The main difference between CCI, CCII and third generation CCIII is relation between terminal Y current and terminal X current. In CCI, Y current is equal to X current in the same direction and in the CCII, there is no current flows in terminal Y. But in the CCIII, terminal Y current is equal to X terminal current in the opposite direction. The relationship between port voltages and currents are described by the following matrix equation of an ideal dual output third generation current conveyor whose block box representation is shown in Figure 2.12 where the positive and negative signs define a positive and negative current conveyor, respectively.

$$\begin{bmatrix} i_Y \\ V_X \\ i_{Z+} \\ i_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (2.5)$$

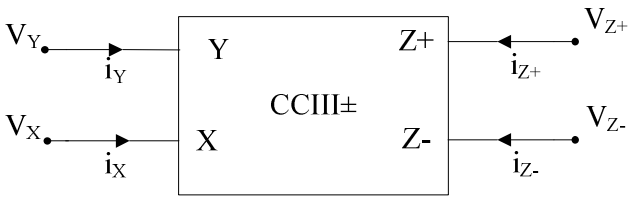


Figure 2.12: Block box representation of CCIII±

This type current conveyor can be useful to take out the current flowing through a floating branch of a circuit. It is also advantageously used as the input cell of probes and current measuring devices.

The CMOS implemantation of third generation current conveyor quoted from Mineai, Yıldız, Kuntman & Türköz (2002) is shown in Figure 2.13.

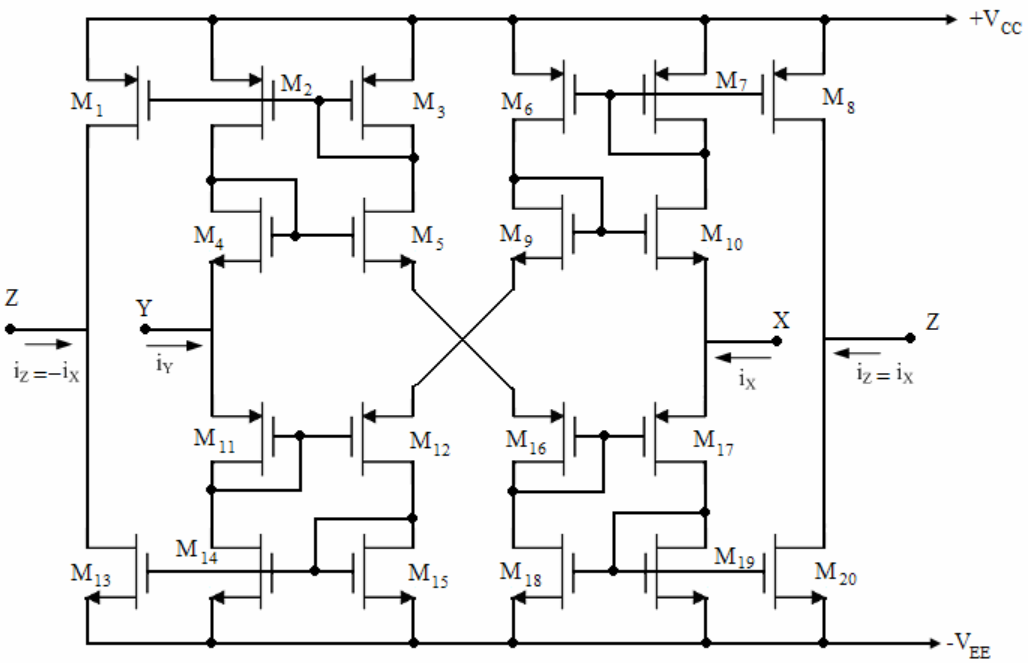


Figure 2.13: CMOS implemantation of dual output third generation current conveyor

2.4 Current Controlled Current Conveyor (CCCII)

The first current controlled current conveyor was developed by Alain Fabre in 1996 with utilization of intrinsic resistance of mixed translinear loop that contains two PNP's and two NPN's transistors is shown in Figure 2.14.

It is characterized by the translinear relationship between collector currents of these transistors (Fabre, 1983).

$$I_1.I_3 = I_2.I_4 \tag{2.6}$$

The circuit is dc biased by two identical currents ($I_1 = I_3 \cong I_0$ by assuming current gains β of the transistors much greater than unity). Thus, it presents a high impedance input port (port Y) and a low impedance output port (port X). This circuit is a voltage follower (Fabre, Saaid, Wiest, and Boucheron, 1996). The voltage difference between points Y and X is given by

$$\Delta V = V_{BE_{Q1}} - V_{BE_{Q2}} = V_T \log(\frac{I_2}{I_0}) \tag{2.7}$$

where $V_T \cong kT/q \cong 26mV$ at 27ºC is thermal voltage.

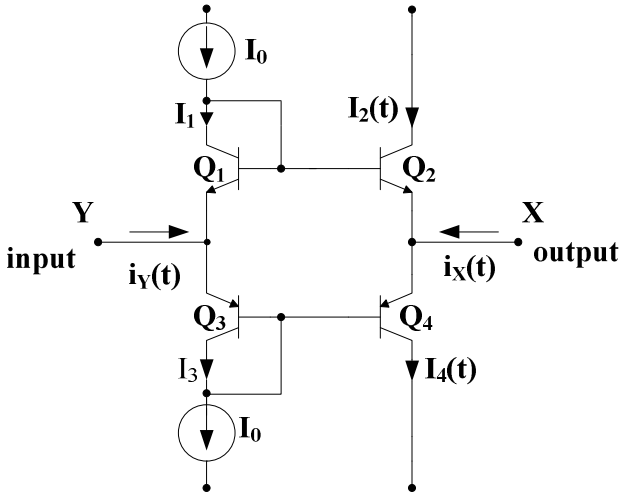


Figure 2.14: Schematic form of the mixed translinear loop

The relationship in equation (2.5), allows to calculate the expressions for the currents $I_2(t)$ and $I_4(t)$. They are given by

$$I_2(t) = \frac{1}{2}\left[(i_X^2(t) + 4I_0^2)^{1/2} - i_X(t)\right] \tag{2.8}$$

$$I_4(t) = \frac{1}{2}\left[(i_X^2(t) + 4I_0^2)^{1/2} + i_X(t)\right] \tag{2.9}$$

By assuming the magnitude of the current $i_X(t)$ much smaller than $2I_0$, so the V_{YX} (ΔV) voltage can be modified as

$$V_{YX}(t) = \frac{V_T}{2I_0} i_X(t). \tag{2.10}$$

The relationship shows that the output small signal resistance of the equivalent voltage follower is equal to

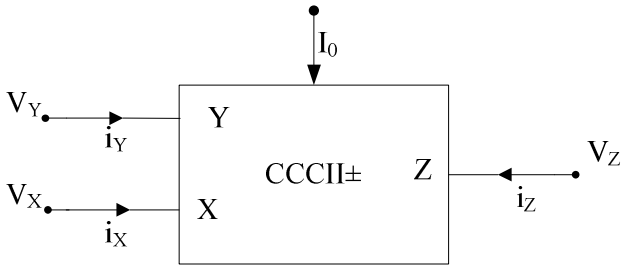
$$R_X = \frac{V_T}{2I_0} \tag{2.11}$$

So, it will be able to be controlled by acting on the bias current I_0 of the loop (Fabre and others, 1996). The parasitic resistance appears at terminal X of current controlled current conveyor.

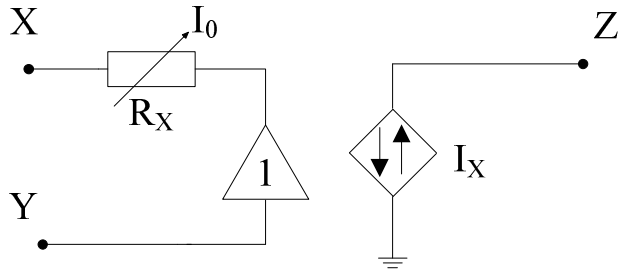
There are two types of current controlled current conveyors as positive and negative. The matrix equation between port voltages and port currents is described by

$$\begin{bmatrix} i_Y \\ V_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ V_Z \end{bmatrix} \tag{2.12}$$

where ±1 determined which type CCCII is positive or negative. The block box representation of current controlled current conveyor and equivalent circuit are shown in Figure 2.15.



(a)



(b)

Figure 2.15: (a) Block box representation of CCCII±,
(b) Equivalent circuit

The port relations of the current controlled conveyors is modified with non-idealities to

$$\begin{bmatrix} i_Y \\ V_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta & R_X & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ V_Z \end{bmatrix} \tag{2.13}$$

$\alpha = 1-\varepsilon_i$, $|\varepsilon_i| \ll 1$, represents the current tracking error and $\beta = 1-\varepsilon_V, |\varepsilon_V| \ll 1$, represents the voltage tracking error. When it is assumed that I_0 has a very high value; so R_X is approximately zero, CCCII acts as a second generation current conveyor.

There are many implementations of current controlled current conveyor like CMOS, bipolar, BiCMOS and others. Figure 2.16 represents the bipolar implementation of positive current controlled current conveyor (CCCII+) that was used in simulations where I_0 is the DC bias current . By addition of two cross-

coupled current mirrors to CCCII+, negative type of CCCII is obtained which is shown in Figure 2.17.

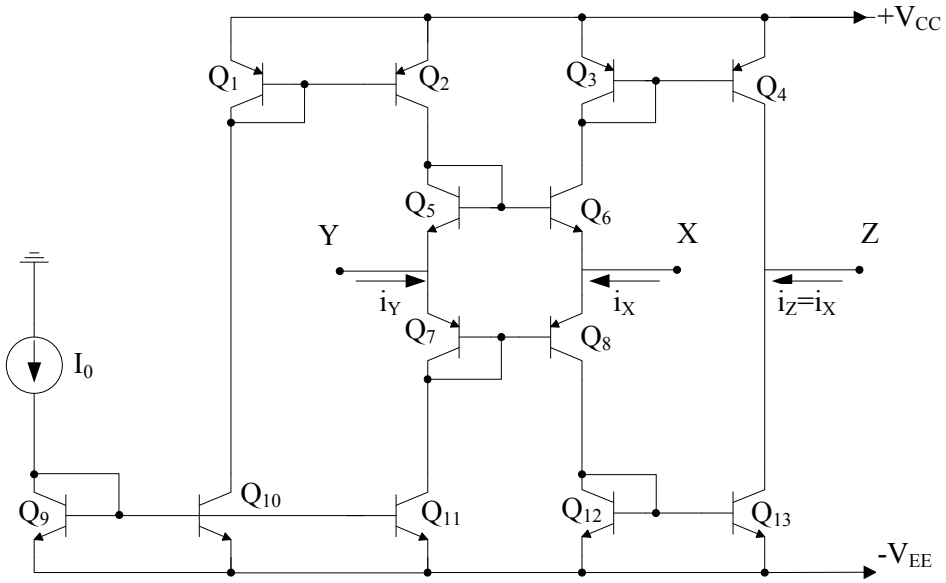


Figure 2.16: Bipolar implementation of CCCII+

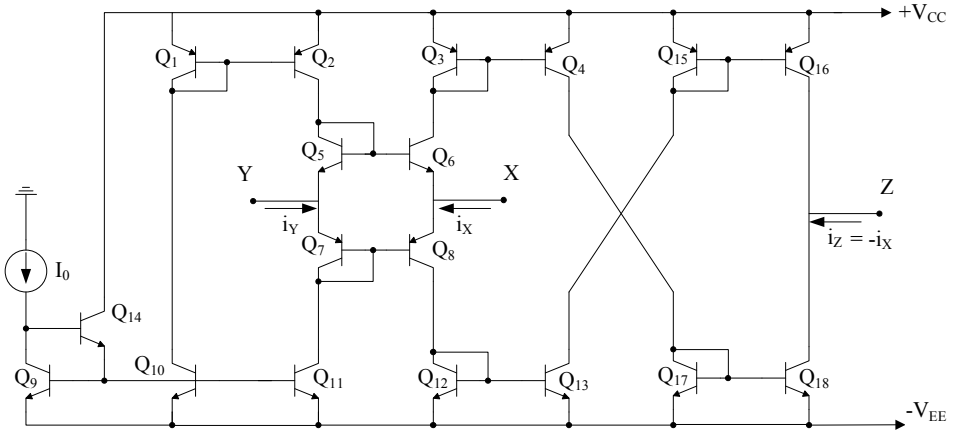


Figure 2.17: Bipolar implementation of CCCII-

Implementation of CCCII+ with CMOS technology quoted from Altuntaş and Toker (2002) is shown in Figure 2.18. It has same circuit topology as the bipolar implementation, but NPN and PNP transistors are replaced with NMOS and PMOS transistors, respectively. For small bias currents I_0, MOS transistors operate in

substhreshold region also called weak inversion that V_{GS} reduces to below V_{TH} (thermal voltage). In this conditon, current equation can be written as

$$I_D = I_{DO}(\frac{W}{L})e^{\frac{V_{GS}}{nV_{TH}}} \tag{2.14}$$

where n is substhreshold slope factor that is typically 1.2 ... 1.5 and I_{DO} is the drain current at V_{DS} is zero and *W/L* ratio is 1. Parasitic resistance at terminal X R_X can be calculated as the same equation in (2.11) under these conditions.

For high bias currents that make transistors operate in saturation region, R_X can be calculated as

$$R_X = \frac{1}{g_{m5} + g_{m9}} \tag{2.15}$$

where g_{m5} and g_{m9} are transcunductance of M5 and M9 transistros, respectively. The formula of transconductance of an MOS transistor is given by

$$g_m = \sqrt{2\beta I_0} \tag{2.16}$$

where β is transconductance parameter. Thus, R_X can be adjusted via I_O. By addition of two cross-coupled current mirrors with NMOS and PMOS transistors to CCCII+, negative type of CCCII quoted from Altuntaş and Toker (2002) is obtained which is shown in Figure 2.19 with CMOS technology.

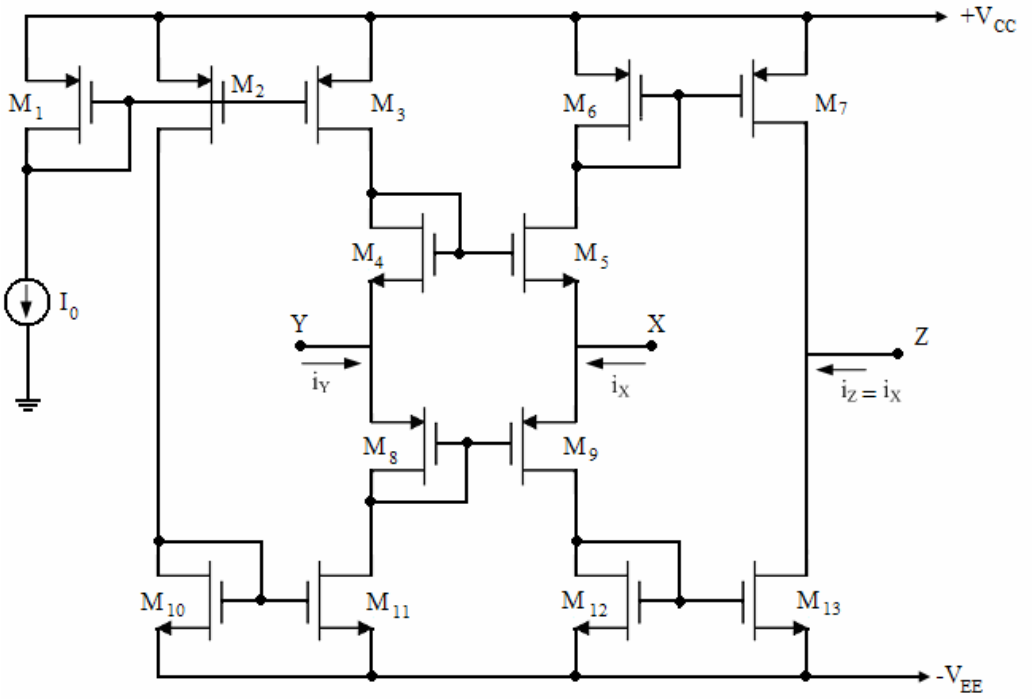


Figure 2.18:CMOS implementation of CCCII+

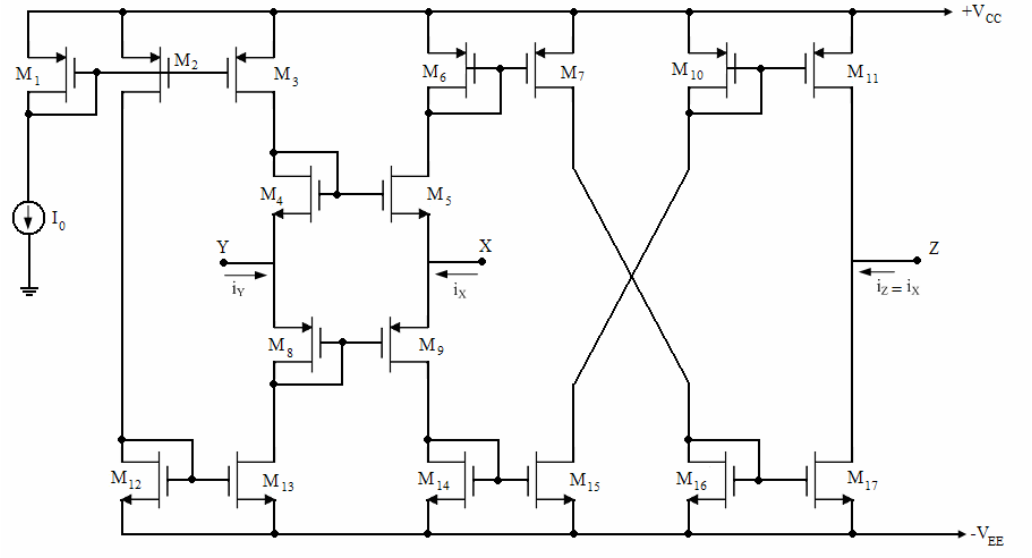


Figure 2.19: CMOS implementaiton of CCCII-

Another type of current controlled current conveyor is dual output one. In this type both negative and positive Z output take place. The matrix equation between port voltages and port currents is described by

$$\begin{bmatrix} i_Y \\ V_X \\ i_{Z+} \\ i_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & R_X & 0 & 0 \\ 0 & +1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{2.17}$$

where V_{Z+} and V_{Z-} are outputs. Nonidealities also are valid for this type. If non idealities are considered for dual output current controlled current conveyor (DO-CCCII), the matrix equation is modified as

$$\begin{bmatrix} i_Y \\ V_X \\ i_{Z+} \\ i_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \beta & R_X & 0 & 0 \\ 0 & +\alpha & 0 & 0 \\ 0 & -\alpha & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{2.18}$$

where β and α are voltage and current tracking errors, respectively.

The block box representation of DO-CCCII is shown in Figure 2.20.

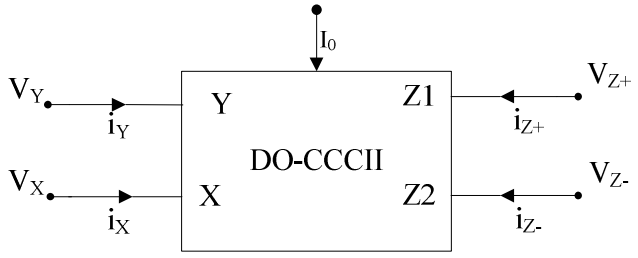


Figure 2.20: Block box representation of DO-CCCII

There is a bipolar implementation of DO-CCCII which is commonly used in applications. It is shown in Figure 2.21 quoted from Mineai, Yıldız, Kuntman & Türköz (2002) that is obtained by modifying the original circuit of the CCCII in Figure 2.16 by adding additional cross-coupled current mirrors to obtain the required minus type output.

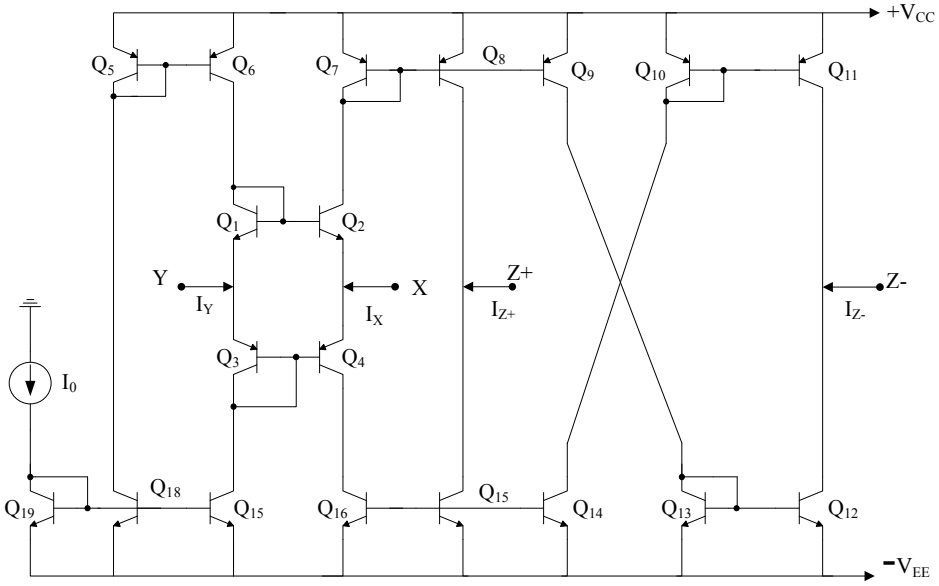


Figure 2.21 Bipolar implementation of dual output CCCII

2.5 Applications of Current Conveyors

First generation current conveyors (CCI) applications (Sedra and others, 1990) can be listed that;

- Wideband current measuring device an alternative to the oscilloscope based on Hall Effect,
- Negative impedance converter (NIC),
- Voltage to current converter,
- Digital to analog conversion with current source output,
- DC offset control of wideband signals.

Second generation current conveyors (CCII) are mainly used in active network synthesis and analog linear systems. Applications (Sedra and others, 1990), (Sedra & Smith, 1970) with CCII are described as;

- Oscillators,
- Filters,
- Gyrators,
- Voltage controlled voltage source,
- Voltage controlled current source,

- Currrent controlled current source,
- Current controlled voltage source,
- Both voltage and current mode amplifier,
- Both voltage and current mode differentiator,
- Both voltage and current mode integrator,
- Both voltage and current mode summer,
- Both voltage and current mode multiplier / divider,
- Current mode biquad filter,
- Inductance simulation that took placed in literature.

Oscillators, filters, and gyrators are constructions with third generation current conveyors (CCIII) (Mineai and others, 2002.).

There are many application areas for current controlled current conveyors (CCCII) because of its advantages will be mentioned in advantage part. CCCIIs are used in several programmable current-mode and voltage-mode signal processing circuits. In literature its applications (Fabre and others, 1996), (Erdal and others, 2004) are;

- Sinusoidal oscillators,
- Analog multiplier / divider,
- Inductance simulation,
- Voltage / current conversion,
- Current / voltage conversion,
- Kerwin-Huelsman-Newcomb (KHN) biquads,
- Both voltage and current mode filters,
- Programmable gain amplifier (PGA),
- Proportional integral-derivative (PID) controller.

2.6 Advantages of Current Conveyors

Current conveyors have advantages when they compared with their counterparts as operational amplifier (opamp), operational transconductance amplifier (OTA). If current conveyor's advantages are considered since their development, first generation current conveyor CCI must be mentioned firstly.

CCI can be used in voltage mode or curent mode like other types of curent conveyors. Current mode function have primacy, when they are compared with voltage mode function that they exhibit higher frequency potential, simpler architecture, lower supply voltage capabilities, greater linearity, and low sensitivity. CCI also has wider frequency range extending from DC to 100MHz.

After invention of CCI, second generation current conveyor (CCII) was developed with features like as high linearity, wide dynamic range and better frequency performance compared with their voltage mode counterparts. At the same time, open loop operation, better performance SR (slew rate) can be listed as advantages of all current conveyor types when they are compared with stucture like OTA and opamp.

The main features of the CCIIIs are low gain errors (high accuracy), high linearity, and wide frequency response. In addition high output resistance at terminal Z of the CCIII is required to enable easy cascadility without need for additional active elements in applications (Minaei, Yıldız, Kuntman, and Türköz, 2002).

Finally, current controlled current conveyors (CCCII) have an advantage of electronic adjustability over the current conveyor (CCII). It exhibits higher speed and better bandwidth than voltage mode operational amplifier which causes limitation by a constant gain bandwidth product. When it is compared with bipolar OTA, mainly there are two primacies of CCCII. The value of the transconductance g_m is

$$g_m = \frac{I_0}{2V_T} \tag{2.19}$$

It is equal to $1/R_X$, where R_X is parasitic resistance of CCCII. For the same value of I_0, the transconductance of the bipolar OTA is four times less than the CCCII. It causes different results. For example, in second order band pass filter with a same frequency f_0, greater power consumption is needed with OTA than CCCII and about three times greater in this example because f_0 is proportional to g_m in OTA implementation. On the other hand, with very high values for the collector currents of the transistors, their maximum operation frequency reduces. It shows that, the frequency potential of circuits with CCCII is greater than the OTA implementations. Additionally, for many implementations with OTA's, circuity becomes more complex. Thus, power consumption and silicon area used increase.

CHAPTER THREE
NEW APPLICATIONS OF CURRENT CONEYORS

Current controlled current conveyors are very useful for the implementation of electronically tunable functions like as; filters operating either in voltage mode or current mode and oscillators. Additionally, inductance simulation is made with CCCII by helping its advantages as great linearity, signal bandwidth, and dynamic range.

3.1 Filter Applications of current conveyors

In this study, three filter applications are realized. First of them is a first order allpass filter operating in voltage mode. In this filter; only one CCCII and two capacitors are used. Its frequency can be adjustable by directly bias current of CCCII.

Second of these filters is a first order allpass filter operating in current mode. There are a dual output CCCII, a dual output CCII, and a capacitor. In this circuit, two outputs take place that one of them is inverting output provides a minus (-) sign of transfer function and so 180° phase difference between this type and normal allpass filter, the other output is noninverting output. Center frequency of this filter is adjustable by bias current of dual output CCCII.

Third of them is a second order bandpass filter consists of a CCCII, two capacitors, and a resistor. Its gain, bandwidth and center frequency depend on bias current.

3.1.1 First Order Allpass Filter In Voltage Mode

The first order allpass filter in voltage mode is represented in Figure 3.1. It reguires only one CCCII+ and two capacitors.

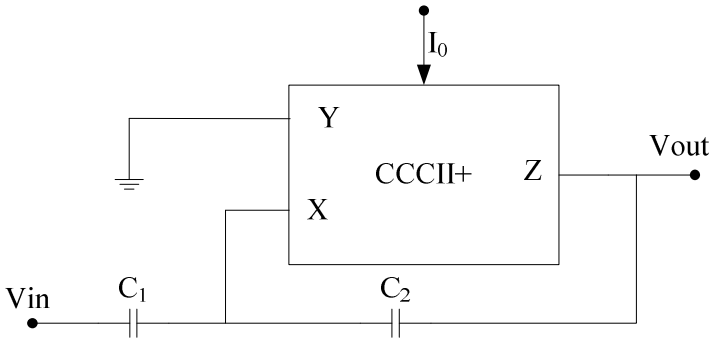


Figure 3. 1 : First Order Allpass Filter In Voltage Mode

The transfer function of this circuit is described by

$$\frac{V_{out}}{V_{in}}(s) = \frac{-sC_1 + s^2 C_1 C_2 R_X}{sC_2 + s^2 C_1 C_2 R_X} \tag{3.1}$$

where R_X is parasitic resistance of CCCII+. When C_1 capacitor is chosen that is equal to two times of C_2 = C, the transfer function is modified as

$$\frac{V_{out}}{V_{in}}(s) = \frac{s - \dfrac{1}{R_x C}}{s + \dfrac{1}{R_x C}} \tag{3.2}$$

and center frequency of this filter is;

$$w_0 = \frac{1}{R_x C} = \frac{2I_o}{V_T C} \tag{3.3}$$

where I_0 is bias current and V_T is thermal voltage approximately 26mV. The phase response of the filter can be expresed as

$$\Phi(\omega) = 180 - 2\arctan(\omega C R_X) \tag{3.4}$$

Equations given above correspond when CCCII is assumed as ideal. If nonideality of CCCII is considered, transfer function and phase response are modified as;

$$\frac{V_{out}}{V_{in}}(s) = \frac{s - \dfrac{\alpha}{R_x C}}{s + \dfrac{\alpha}{2R_x C}} \tag{3.5}$$

$$\Phi(\omega) = 180 - [\arctan(\frac{R_X C\omega}{\alpha}) + \arctan(\frac{2R_X C\omega}{1+\alpha})] \tag{3.6}$$

where α is current tracking error.

The first order allpass filter in Figure 3.1 is simulated using PSpice simulation program. The CCCII+ is simulated using the bipolar implementation circuit in Figure 2.16 with the typical parameters of the bipolar transistors NR100N and PR100N and DC supply voltage ±8.5V. Capacitors's values are chosen as 100pF and 200pF for C_2 and C_1, respectively. The bias current I_0 is applied 20μA to the circuit that makes parasitic resistance R_X 650Ω. Under these conditions gain and phase response of the filter are shown in Figure 3.2 and Figure 3.3, respectively.

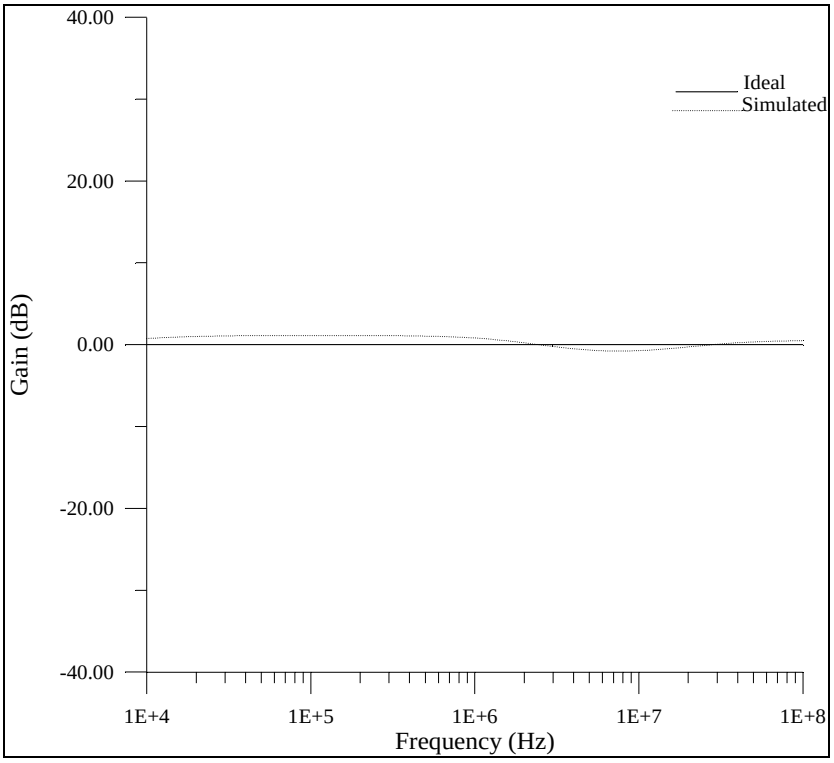


Figure 3. 2 : Gain response of the all-pass filter operating in voltage mode

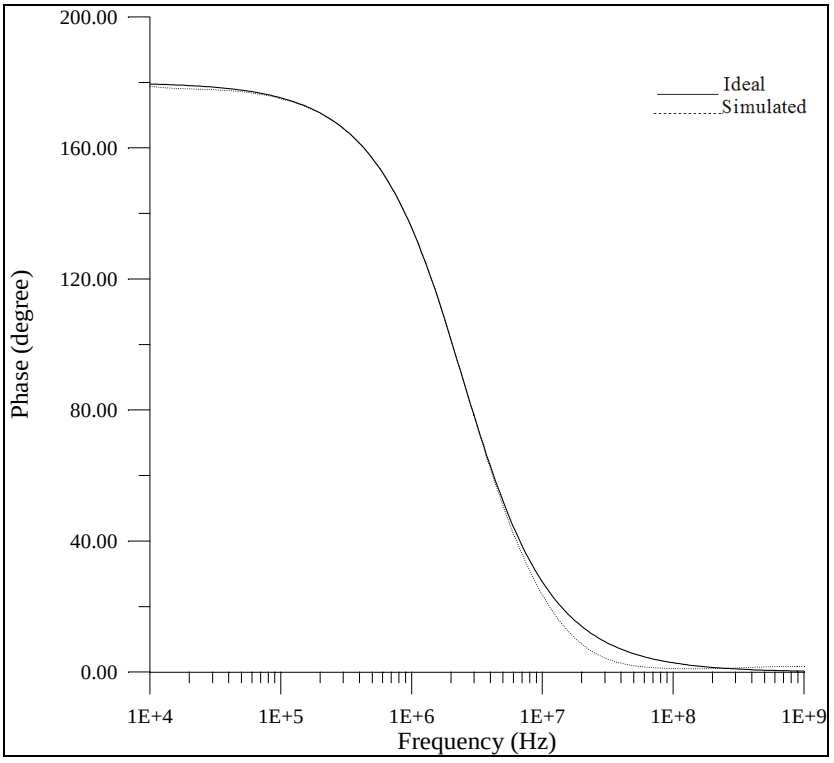


Figure 3. 3 : Phase response of all-pass filter operating in voltage mode

For different bias current values 5µA, 10µA, 15µA, 20µA, 25µA and with same values of capacitors simulation is repeated. Figure 3.4 shows parametric simulation results with respect to bias currents. The corresponding center frequencies are obtained by simulation respectively; 651.780KHz, 1.2329MHz, 1.8751MHz, 2.4578MHz, and 2.9966MHz which are in good agreement with theoretical values deduced from equation (3.3): 612.134KHz, 1.2242MHz, 1.836MHz, 2.448MHz and 3.060MHz, respectively.

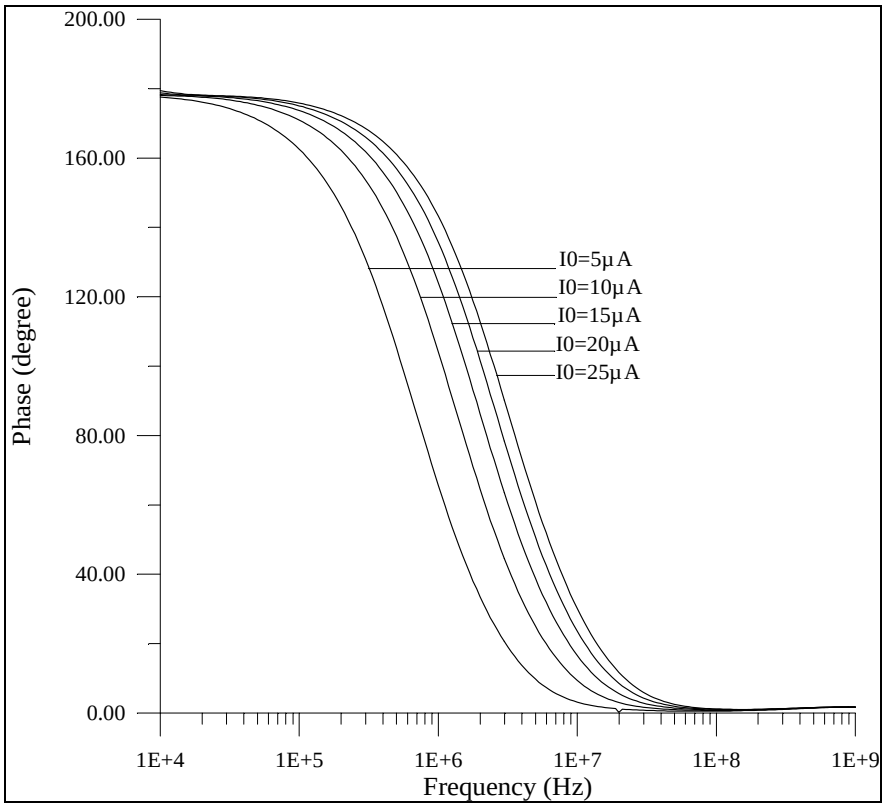


Figure 3. 4: Phase response of all-pass filter various variables of control current

Finally, a sinusoidal signal at 2.448MHz frequency is applied to input of the filter to obtain time domain response. This causes 102ns time delay at the output of the filter corresponding 90° phase difference. It is the same as theoretical values.

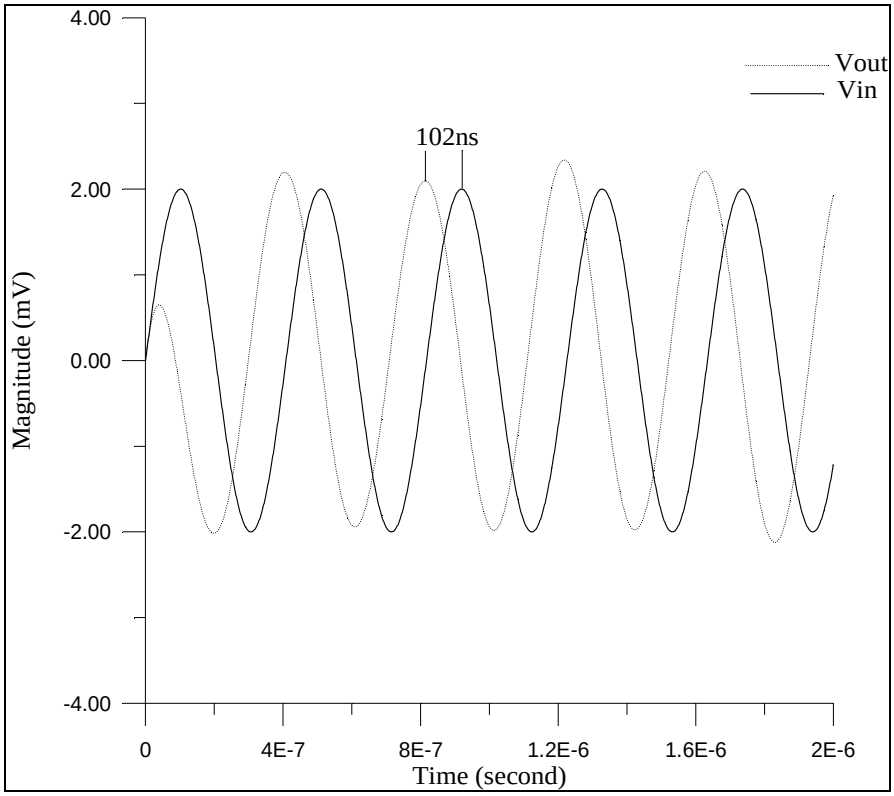


Figure 3.4 : Time domain response of all-pass filter when V_{IN}=2sin(2π2448000t)mV

3.1.2 First Order Allpass Filter In Current Mode

The first order allpass filter in current mode is represented in Figure 3.5. It consists of a dual output second generation current conveyor, a dual output second generation current controlled current conveyor, and a capacitor. In this filter there are two output ports that one of them is inverting and other one is noninverting output.

The transfer functions of the filter construction are described by

$$\frac{I_{AP+}}{I_{in}}(s) = \frac{s - \frac{1}{R_x C}}{s + \frac{1}{R_x C}} \tag{3.7}$$

$$\frac{I_{AP-}}{I_{in}}(s) = -\frac{s - \frac{1}{R_x C}}{s + \frac{\alpha}{R_x C}} \tag{3.8}$$

where I_{AP+} is noninverting output and I_{AP-} is inverting output.

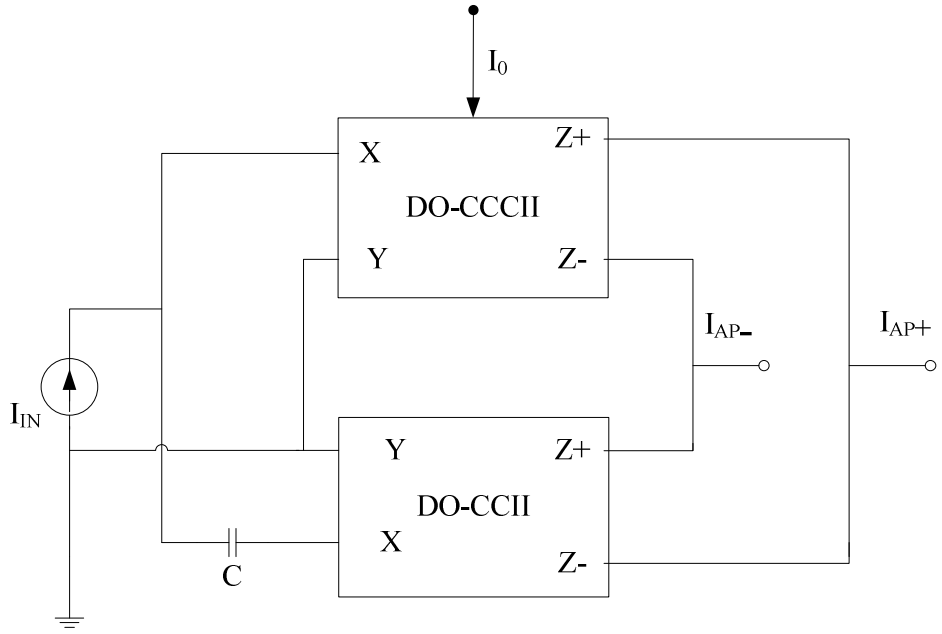


Figure 3.5 : First Order Allpass Filter In Current Mode

Center frequency of the filter for both outputs is

$$w_0 = \frac{1}{R_x C} = \frac{2I_o}{V_T C} \tag{3.9}$$

where I_0 is bias current of the dual output CCCII and V_T is thermal voltage approximately 26mV. The phase responses of the filter can be expresed as

$$\Phi_1(\omega) = 180 - 2\arctan(\omega C R_X) \tag{3.10}$$
$$\Phi_2(\omega) = -2\arctan(\omega C R_X) \tag{3.11}$$

where equation (3.10) for noninverting output and equation (3.11) for inverting output of the filter.

The filter transfer functions and phase equations are modified when nonideality conditions are considered;

$$\frac{I_{AP+}}{I_{in}}(s) = \frac{s - \dfrac{\alpha_1}{\alpha_2 R_x C}}{s + \dfrac{1}{R_x C}} \tag{3.12}$$

$$\frac{I_{AP-}}{I_{in}}(s) = -\frac{s - \dfrac{\alpha_1}{\alpha_2 R_x C}}{s + \dfrac{1}{R_x C}} \tag{3.13}$$

$$\Phi(\omega) = 180 - \arctan\left(\frac{\alpha_2 \omega C R_X}{\alpha_1}\right) - \arctan(\omega C R_X) \tag{3.14}$$

$$\Phi(\omega) = -\arctan\left(\frac{\alpha_1 \omega C R_X}{\alpha_2}\right) - \arctan(\omega C R_X) \tag{3.15}$$

where α_1 and α_2 are current track errors of dual output CCCII and dual output CCII, respectively.

The first order allpass filter operating in current mode in Figure 3.5 is simulated using PSpice simulation program. The dual output CCCII is simulated using the bipolar implementation circuit in Figure 2.21 with the typical parameters of the bipolar transistors NR100N and PR100N and DC supply voltage ±3V. The dual output CCII is simulated using the bipolar implementation circuit of dual output CCCII in Figure 2.21 by giving a high value I_0 ,with the typical parameters of the bipolar transistors NR100N and PR100N, and DC supply voltage ±3V as same as dual output CCCII. Capacitor value is chosen as 150pF and the bias current I_0 for dual output CCCII is applied 20μA to the circuit that makes parasitic resistance R_X 650Ω. Under these conditions gain and phase response of the filter are shown in Figure 3.6 and Figure 3.7, respectively. Theorically the center frequency with these

values of bias current , capacitor value is 1.632MHz. In simulation results, center frequency at inverting output is 1.718MHz and center frequency at noninverting output is 1.620MHz.

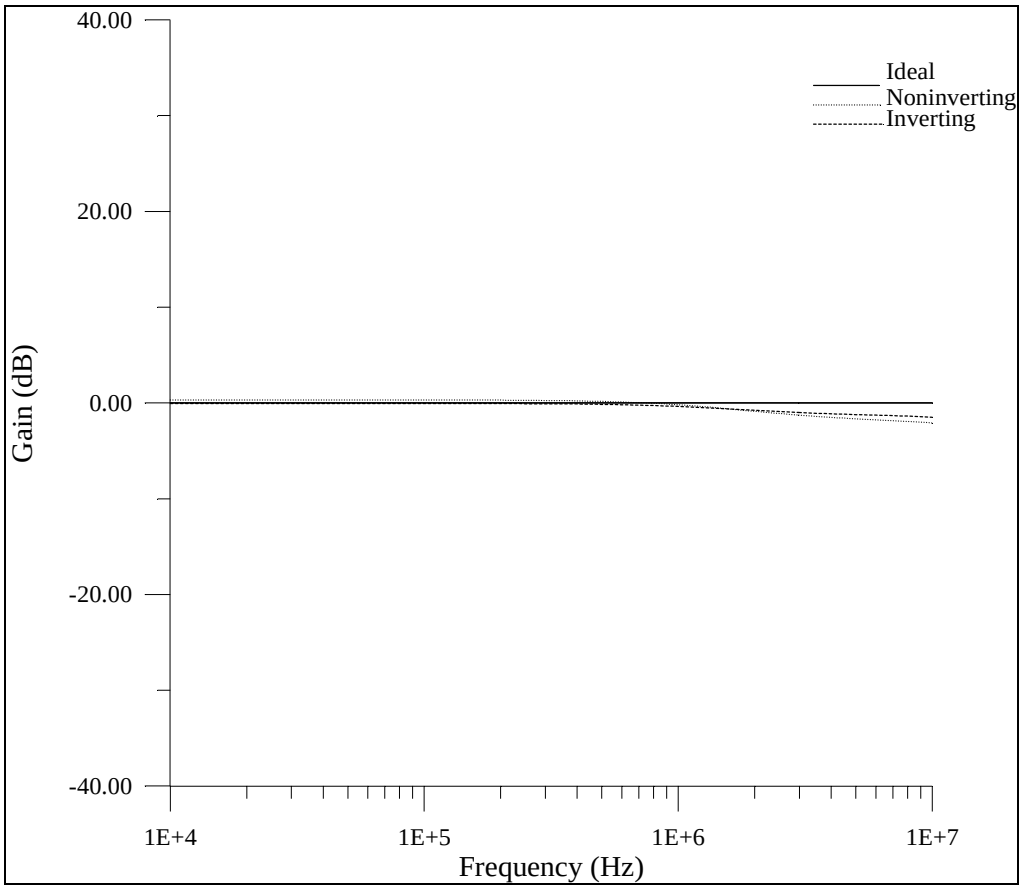


Figure 3.6 : Gain response of the all-pass filter operating in current mode

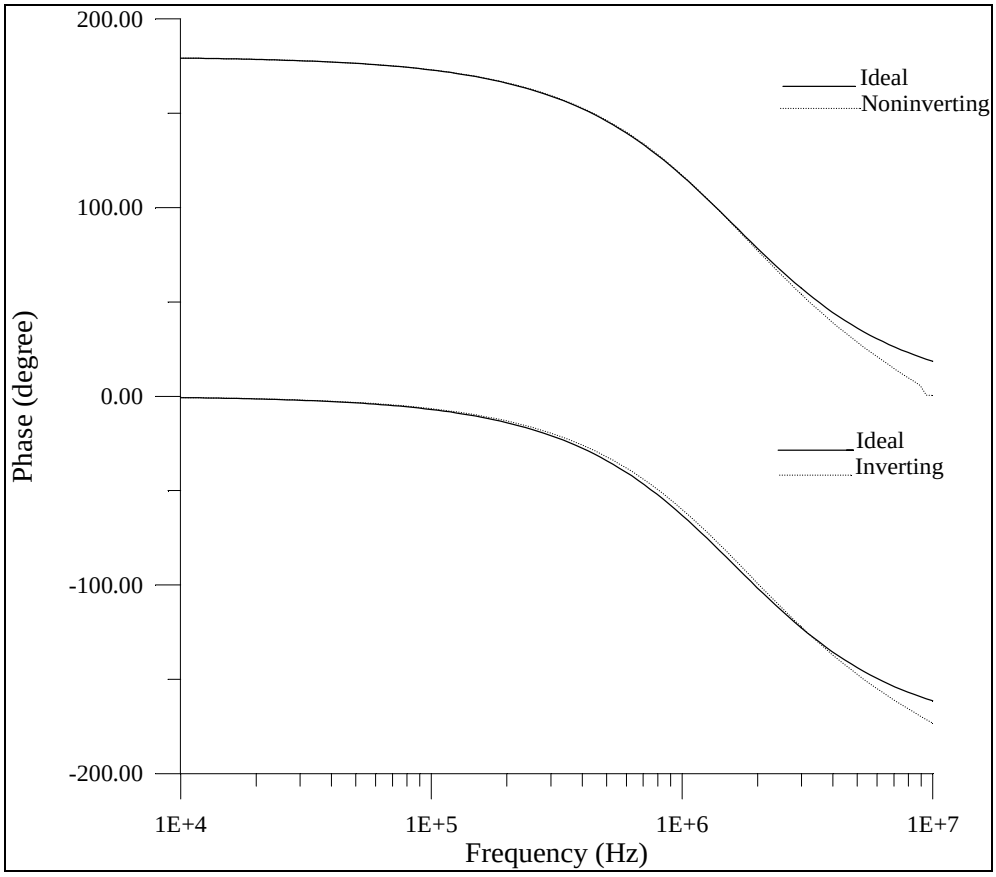


Figure 3. 7 : Phase response of all-pass filter operating in current mode

Parametric simulation is done for different bias current values 10µA, 15µA, 20µA, 25µA and with same values of capacitor. The corresponding center frequencies are obtained by using formulas 816.179KHz, 1.224MHz, 1.632MHz, and 2.04MHz respectively. At the inverting output center frequencies which are 826.541KHz, 1.227MHz, 1.620MHz, and 2.005MHz and at the noninverting output center frequencies that are 876.064KHz, 1.301MHz, 1.718MHz, and 2.127MHz are measured in order to bias currents.

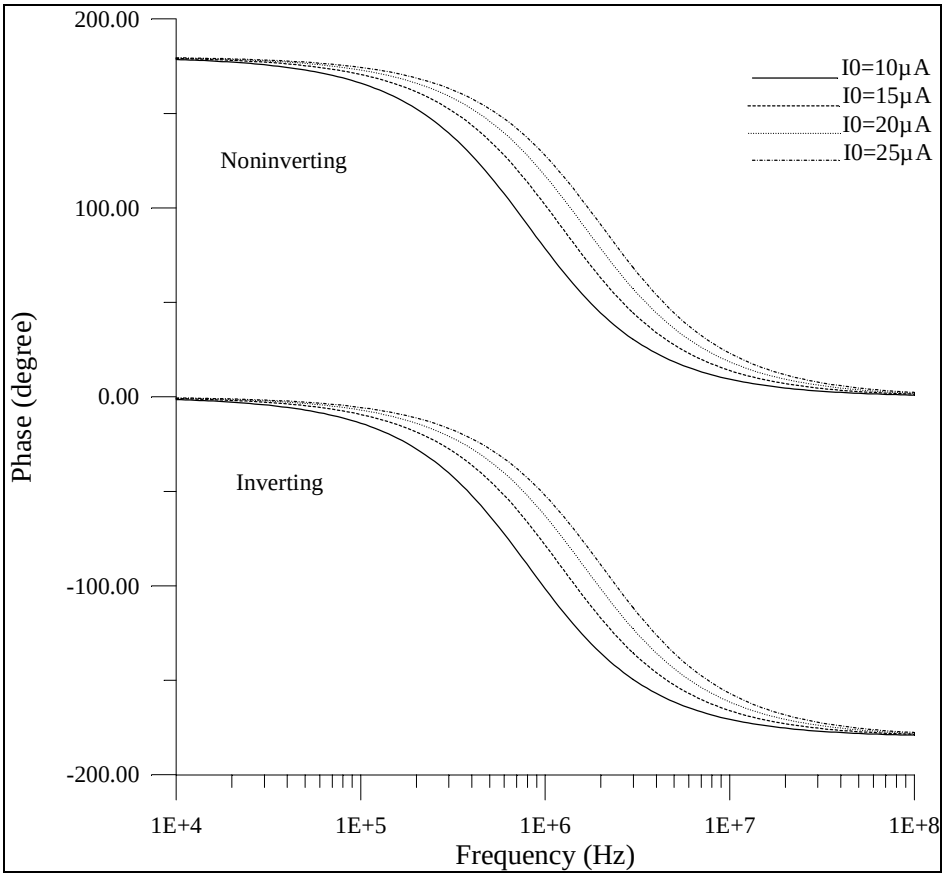


Figure 3.8 : Phase response of all-pass filter various variables of control current

When a sinusoidal signal at 1.632MHz frequency is applied to input of the filter to obtain time domain response. This causes 155.6µs time delay at the inverting output and 461.04µs time delay at the noninverting output of the filter. These time delays correspond 91.52º and 271.2º phase difference while their theoretical results must be 90º and 270º, respectively.

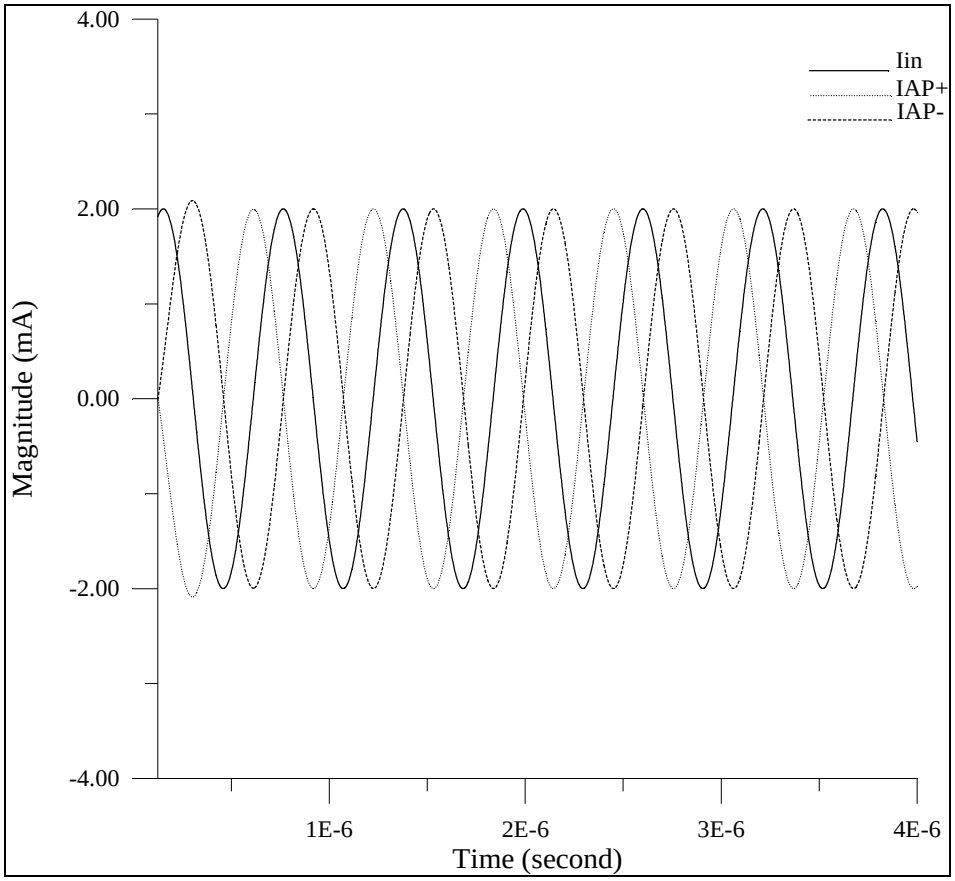


Figure 3.9 : Time domain response of all-pass filter when I_{IN}=2sin(2π1632000t) mA

3.1.3 Second Order Bandpass Filter

The second order bandpass filter is represented in Figure 3.10. It is consists of a positive current controlled current conveyor, two capacitors and a resistor.

The transfer functions of the filter construction are described by

$$\frac{V_{out}}{V_{in}}(s) = \frac{\frac{2s}{C_2 R_X}}{s^2 + s(\frac{1}{C_1 R_1} + \frac{2}{C_2 R_X}) + \frac{2}{C_1 C_2 R_1 R_X}} \qquad (3.16)$$

where R_X is parasitic resistance of CCCII+. Gain, center frequency, phase response, and bandwidth of the filter can be written as

$$K = \frac{2C_1R_1}{2C_1R_1 + C_3R_X} \tag{3.17}$$

$$w_0 = \sqrt{\frac{2}{R_xC_1C_2R_1}} = \sqrt{\frac{4I_o}{V_TC_1C_2R_1}} \tag{3.18}$$

$$\Phi(\omega) = 90 - \arctan\left(\frac{C_2R_X + 2C_1R_1}{2 - w^2C_1C_2R_XR_1}\right) \tag{3.19}$$

$$BW = \frac{2}{R_xC_2} + \frac{1}{R_1C_1} \tag{3.20}$$

where K is gain, w_0 is center frequency, and BW is bandwidth of the filter.

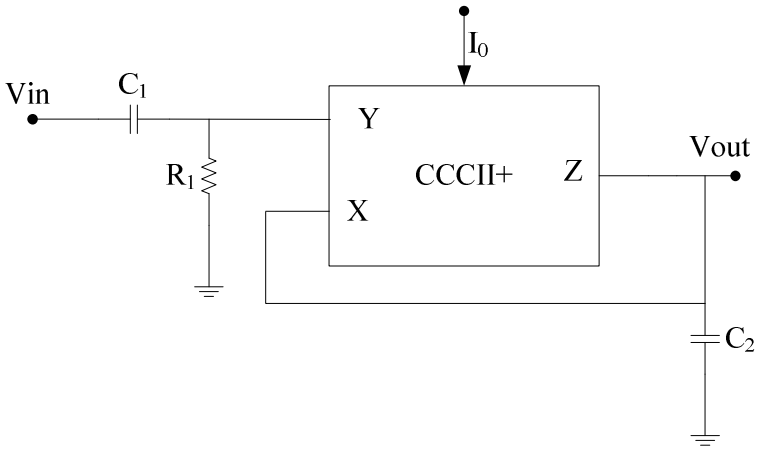


Figure 3.10 : Second order bandpass filter

If nonideality of CCCII is considered, equations of gain center frequency, phase response, and bandwidth are modified as;

$$K = \frac{(\beta + \alpha)2C_1R_1}{2C_1R_1 + C_3R_X} \tag{3.21}$$

$$w_0 = \sqrt{\frac{(1+\alpha)}{R_xC_1C_2R_1}} = \sqrt{\frac{2I_o(1+\alpha)}{V_TC_1C_2R_1}} \tag{3.22}$$

$$\Phi(\omega) = 90 - \arctan\left(\frac{C_2R_X + (1+\alpha)C_1R_1}{(1+\alpha) - w^2C_1C_2R_XR_1}\right) \tag{3.23}$$

$$BW = \frac{(1+\alpha)}{R_xC_2} + \frac{1}{R_1C_1} \tag{3.24}$$

The second order bandpass filter in Figure 3.10 is simulated using PSpice simulation program. The CCCII is simulated using the bipolar implementation circuit in Figure 2.21 with the typical parameters of the bipolar transistors NR100N and PR100N and DC supply voltage ±3V. Both capacitors' values are chosen as 150pF, R_1 resistors is 1300Ω, and the bias current I_0 for dual output CCCII is applied 10μA that makes parasitic resistance R_X 1300Ω. When V_{IN} is a 2mV AC source simulation is realized and gain response phase response of the filter are obtained as shown in Figure 3.11 and Figure 3.12, respectively under these conditions. Theoretically and ideally the center frequency with these values is 1.15425MH, gain is 0.666, and bandwidth is 2.2448MHz In simulation results, center frequency is 1.505MHz, gain is 0.655.and bandwidth is 2.343MHz.

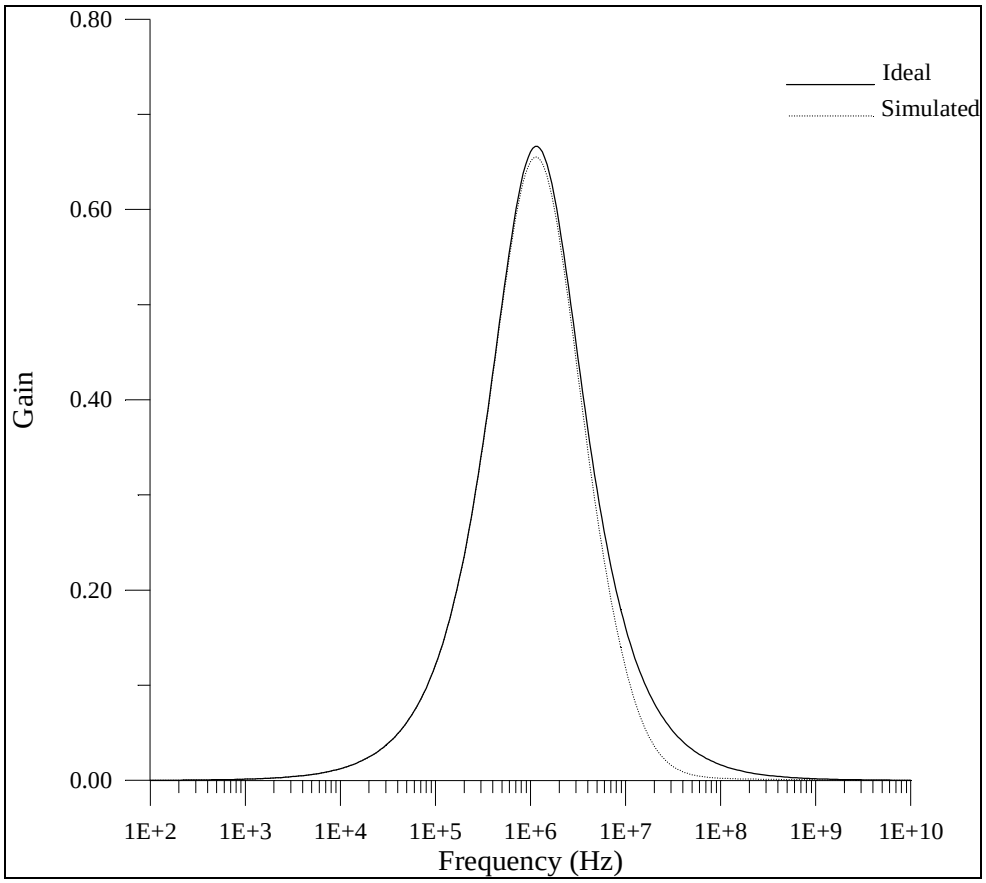


Figure 3.11 : Gain response of the second order bandpass filter

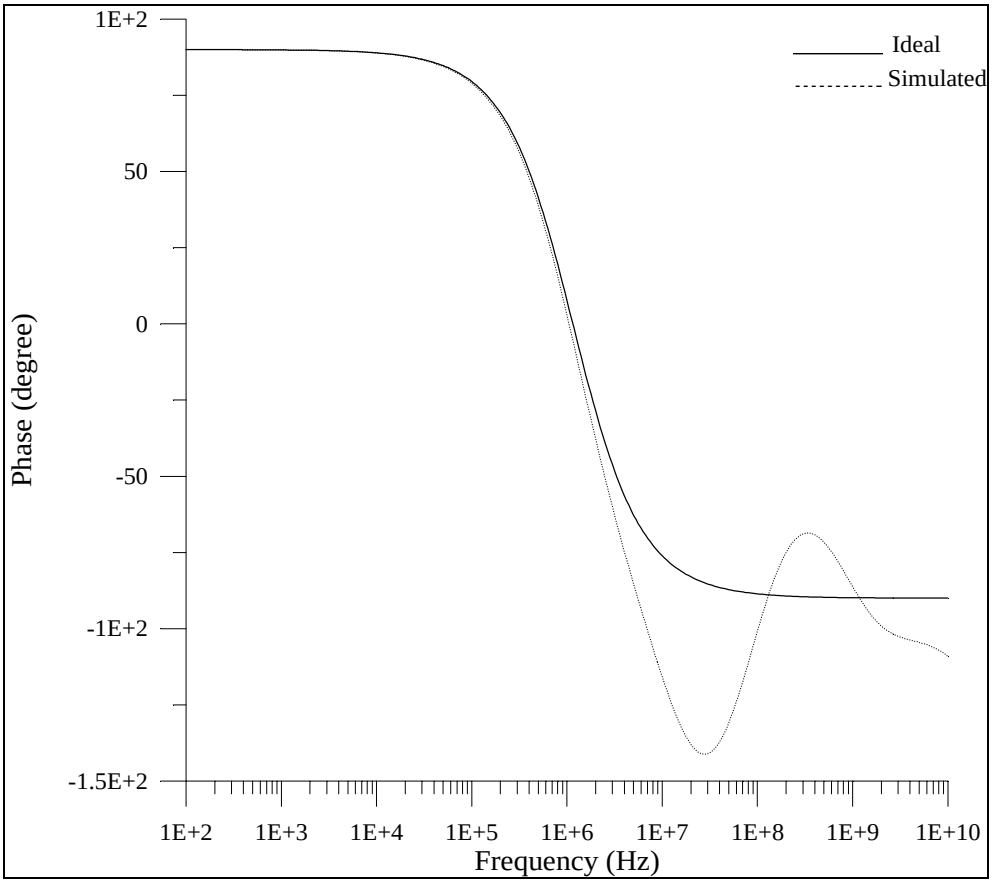


Figure 3.12 : Phase response of the second order bandpass filter

3.2 Oscillator Application of current conveyors

Current conveyors are very useful to design oscillator because of their providing large bandwidth, high linearity, and wide dynamic range to construction. Designed sinusiodal oscillator circuit which is shown in Figure 3.13 consists of a one current controlled current conveyor CCCII-, two capacitors, two resistors.

The characteristics equation of the sinusoidal oscillator can be derived by

$$s^2 C_1 C_2 R_X + s(C_2 \frac{R_X}{R_1} + C_1 \frac{R_X}{R_2} + C_1 \frac{R_X}{R_1} - C_1) + \frac{R_X}{R_2 R_1} = 0 \qquad (3.25)$$

where the R_X is parasitic resistance of the CCCII+ and depends on I_0 bias current.

The oscillation condition is

$$C_2 \frac{R_X}{R_1} + C_1 \frac{R_X}{R_2} + C_1 \frac{R_X}{R_1} - C_1 = 0 \tag{3.26}$$

Under this oscillation condition, oscillation frequencyof the sinusoidal oscillator is calculated as;

$$w_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \tag{3.27}$$

The oscillation frequency is not dependent to I_0 bias current, but oscillation condition depends on I_0.

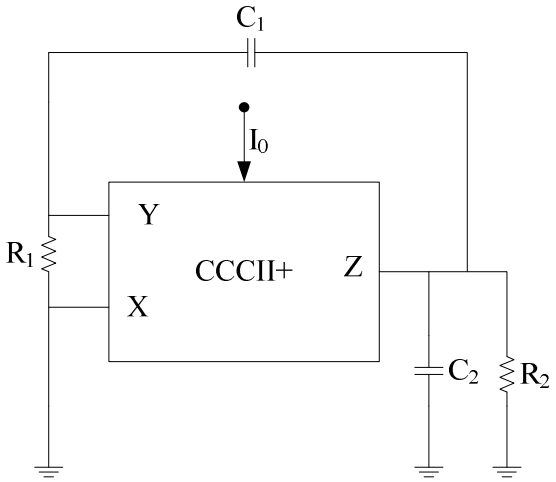


Figure 3.13 : Sinusoidal Osillator circuit

Simulation of the oscillator is realized when $C_1 = C_2 = 100\text{pF}$, $R_1 = R_2 = 1950\Omega$ and $R_X = 650\Omega$ with PSpice simulation program. Under these conditions oscilltion frequency is calculated as 816.179KHz. Figure 3.14 shows the simulated oscillation waveform of the sinusoidal oscillation wavefrom. It is achieved by using ideal circuit of the CCCII+. To measure its linearity, total harmonic distortion (THD) is measured by doing fourier analysis. THD of the oscillator circuit is % 2.82 that is good value for its linearity.

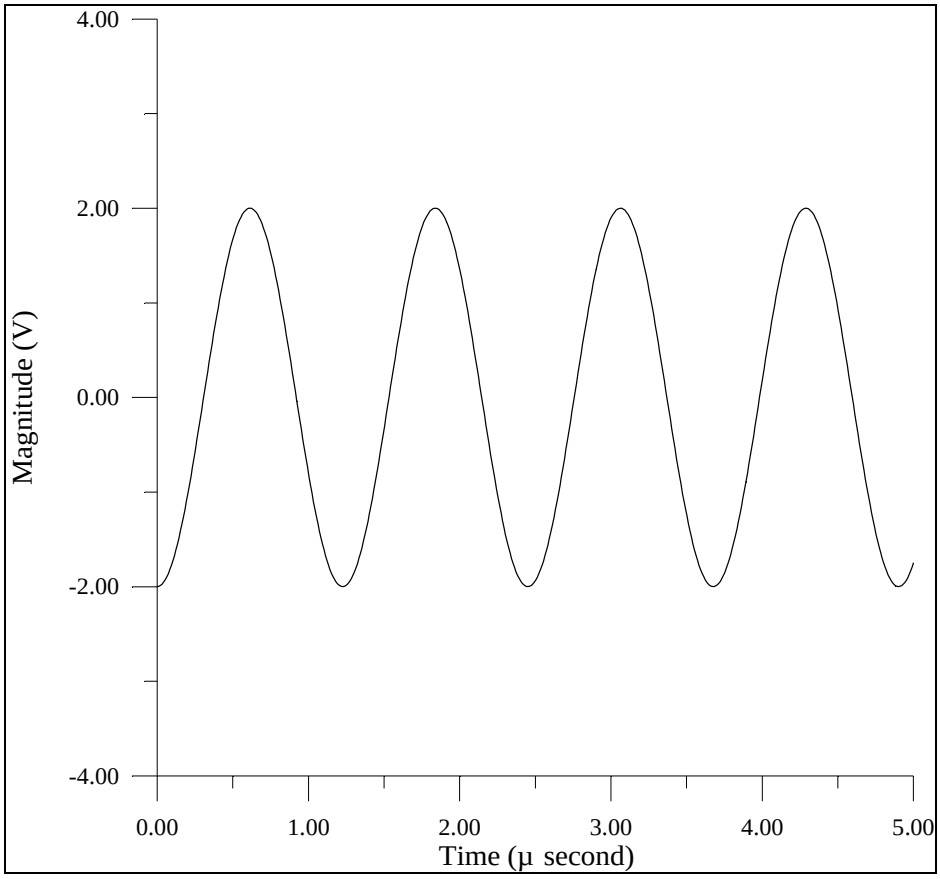


Figure 3.14 : Simulated oscillation waveform of the sinusoidal oscillator

3.3 Inductance simulation of current conveyors

Inductance realization in integrated circuits is quite ardous than other passive components like resistors or capacitors because of its cost, dimension, and mutual affect of electrical field. Due to this excuses, inductance simulations are tried to realize with opamp, OTA, and RC circuits.

Current controlled current conveyors allows applications to be extended to the domain of the electronically adjustable functions. Inductance simulation with CCCII provides tunability. Whereupon in this study an inductance simulation is done that is lossless grounded inductance whose value can be adjustable by I_0 bias current of the CCCII.

3.3.1 Lossless Grounded Inductance Simulation

The lossless grounded inductance simulation circuit is shown in Figure 3.15. It consists of two positive type CCCIIs, a negative type CCCII, and a capacitor.

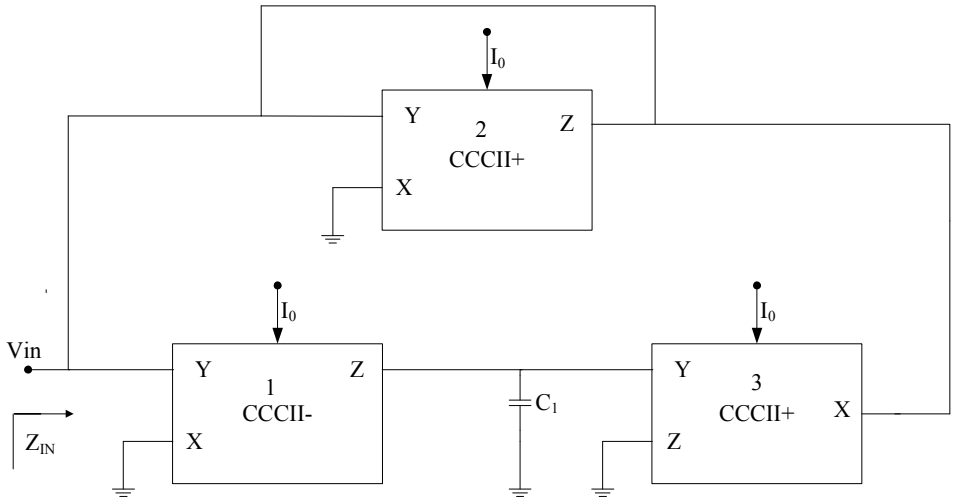


Figure 3.15 : Lossless grounded inductance simulation circuit

When a voltage is applied to the input port of the circuit, input impedance is calculated as;

$$Z_{IN} = \frac{sC_1R_{X1}R_{X2}R_{X3}}{R_{X3} - sC_1R_{X1}R_{X2} + sC_1R_{X1}R_{X3}} \tag{3.28}$$

where R_{X1}, R_{X2}, and R_{X3} are parasitic resistance of first CCCII-, second CCCII+, and third CCCII+, respectively. When R_{X2} and R_{X3} values are equal to each other, then input impedance is modified as;

$$Z_{IN} = sC_1R_{X1}R_{X2} \tag{3.29}$$

It can be easily seen that, input impedance is a inductance which depends on R_{X1} and R_{X2}. It is tunability property according to R_{X1} only because R_{X2} is included in condition.

In nonideal case input impedance equation is expressed as;

$$Z_{IN} = \frac{sC_1R_{X1}R^2{}_{X2}}{R_{X2}(\alpha_1 + R_{X1}(1-\alpha_2)sC_1)} \tag{3.30}$$

where α_1 and α_2 are current tracking errors of first CCCII and second CCCII, resprectively.

Ideal simulation of the inductance is realized with PSpice simulation program when C_1 is equal to150pF, and $R_{X1} = R_{X2} = R_{X3}$=1300Ω are choosen. Under these conditions inductance value is calculated as 253.5μH. An sinusoidal current source with 2mV amplitude at 5000KHz is applied to the input. Theoretically voltage of an inductance is defined as

$$V_L = L\frac{di}{dt} \tag{3.31}$$

With values in simulation, voltage of the inductance is 15.927mV in same frequency with current source but there is a 90° phase differences between them because derivation of sine wave is coisine wave. Current and voltage values of inductance are shown in Figure 3.16.

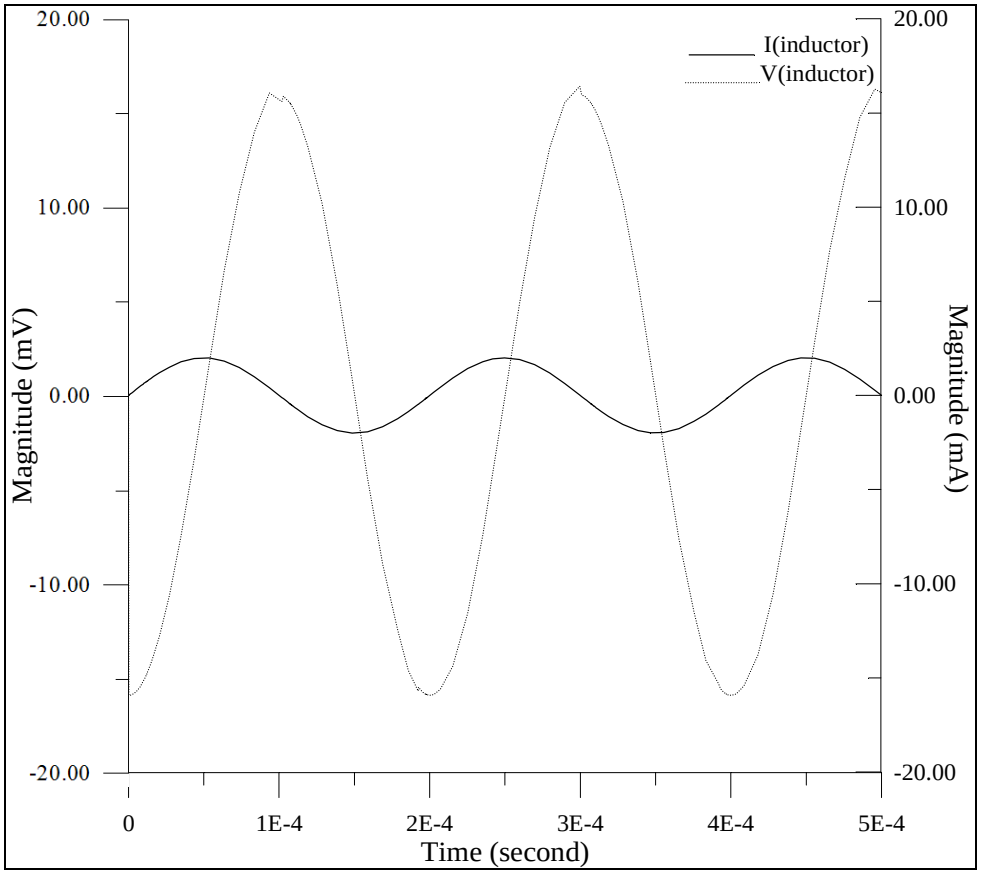


Figure 3.16 : Current and voltage waveforms of lossless inductance

For different values of parasitic resistance of CCCII-simulation is repeated under same values of when C_1, R_{X2}, R_{X2}, and input source. These vaules are 520Ω, 650Ω, 860Ω, and 1300Ω. For these values of R_{X1} inductance values are 101.4μH, 126.75μH, 167.7μH, and 253.5μH respectively. Voltage of inductances in order above are calculated as; 6.37mV, 7.96mV, 10.53mV, and 15.927mV. Simulation results which are shown in Figure 3.17 are same as theoretical results.

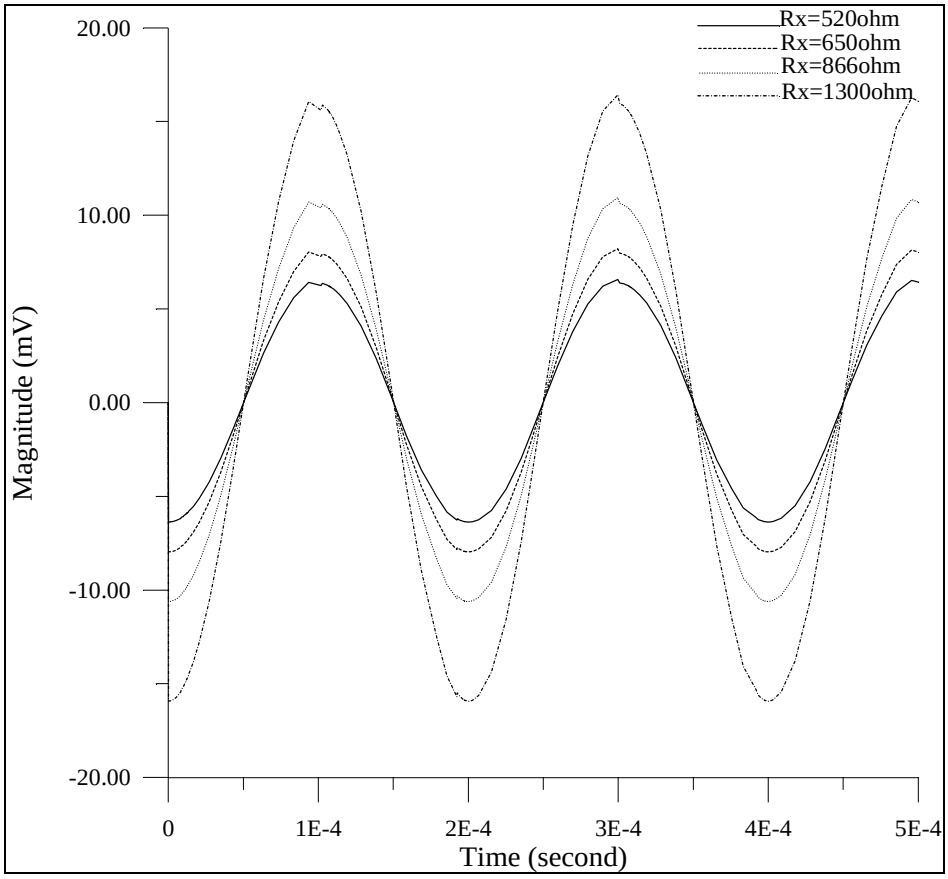


Figure 3.17 : Inductance voltages for different parasitic resistance.

CHAPTER FOUR
CONCLUSION

In this thesis, current conveyor types, their applications, and their variety over counterparts like as opamp and operational trnasconductance amplifier (OTA) are discussed. Especially; current controlled current conveyor is considered important because it has more advantages than the others.

Current mode signal processing circuits have more importance than voltage mode because of their advantages in terms of speed, bandwidth, and accuracy. In adddition, current mode functions exhibit simpler circuity and lower supply voltage capabilities. Many published papers in literature indicate an increase through current mode. And current conveyors are used to design circuits operating in current mode. In this sense, current conveyors have an advantage.

The best performance exhibited type of the current conveyors is current controlled current conveyor (CCCII). It has a parasitic resistance which depends on a bias current of CCCII. It provides electronically tunability at the functions of the circuits. By helping this property; filters, oscillators, and inductance simulations are realized in the thesis.

In this study, there are three filter applications. First of them is an allpass filter operating in voltage mode. The main advantages of this new construction are having center frequency depended on bias current, consisting of only a CCCII+ and two capacitors. In this sense, its implementation can be realized simply. Second of filters is an allpass filter operating in current mode. In this circuit, center frequency has adjustibility property due to only bias current as in first allpass filter. One of the differences between these two filters, there are two outputs in the second one that one of them is inverting output and the other one is noninverting output. The inverting output provides 180º phase difference from noninverting output that have the same transfer function as allpass filters. Another difference between these two filters is value of the components used in design. In the design of the allpass filter operating in

current mode, a DO-CCII, a DO-CCCII, and a capacitor are used. The third and last filter design is second order bandpass filter, consists of a CCCII+, a resistor and two capacitors. Its gain, bandwidth, and center frequency depends on bias current of CCCII+, so adjustment of any one cannot be done without no changing other ones. The simulations for all of the filters are done and obtained results are in good agreement with theoritical analysis.

In the oscillator circuit, a CCCII+, two capacitors, and two resistors are used. The dependency of bias current of CCCII+ exists in oscillation condition. During the simulation, fourier analysis is done to measure total harmonic distortion (THD). THD is % 2.82 so linearity of the oscillator is high.

Last simulation is a lossless inductance simulation. In the real, implementation of an inductance is difficult. In addition inductance is affected from magnetic field and its environment. In this sense, its equivalent circuits is designed with CCCIIs. In this design, two CCCII+, a CCCII-, and a capacitor are used. Lossless inductance value depends on bias current of CCCII-. By only changing the bias current, the value of the inductance can be adjustable. According to its simulation results and theoritical results, its performance approaches to ideal. It allows operating in very high frequencies in mega hertz.

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APPENDIX

The model parameters of PR100N and NR100N transistors are given below.

.MODEL PR100N PNP (IS=73.5E-018 BF=110 VAF=51.8 IKF=2.359E-3 ISE=25.1E-16 NE=1.650 BR=0.4745 VAR=9.96 IKR=6.478E-3 RE=3 RB=327 RBM=24.55 RC=50 CJE=0.180E-12 VJE=0.5 MJE=0.28 CJC=0.164E-12 VJC=0.8 MJC=0.4 XCJC=0.037 CJS=1.03E-12 VJS=0.55 MJS=0.35 FC=0.5 TF=0.610E-9 TR=0.610E-8 EG=1.206 XTB=1.866 XTI=1.7)

.MODEL NR100N NPN (IS=121E-018 BF=137.5 VAF=159.4 IKF=6.974E-3 ISE=36E-16 NE=1.713 BR=0.7258 VAR=10.73 IKR=2.198E-3 RE=1 RB=524.6 RBM=25 RC=50 CJE=0.214E-12 VJE=0.5 MJE=0.28 CJC=0.983E-13 VJC=0.5 MJC=0.3 XCJC=0.034 CJS=0.913E-12 VJS=0.64 MJS=0.4 FC=0.5 TF=0.425E-9 TR=0.425E-8 EG=1.206 XTB=1.538 XTI=2)