DOKUZ EYLÜL UNIVERSITY

GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

CURRENT MODE ANALOG TO DIGITAL CONVERTERS BASED ON CURRENT MULTIPLICATION AND DIVISION TECHNIQUE

by

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October, 2007

İZMİR

CURRENT MODE ANALOG TO DIGITAL CONVERTERS BASED ON CURRENT MULTIPLICATION AND DIVISION TECHNIQUE

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by

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M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"CURRENT MODE ANALOG TO DIGITAL CONVERTERS BASED ON CURRENT MULTIPLICATION AND DIVISION TECHNIQUE"** completed by **YAVUZ İNCE** under supervision of **ASST. PROF. DR. ÖZGE ŞAHİN** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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CURRENT MODE ANALOG TO DIGITAL CONVERTERS BASED ON CURRENT MULTIPLICATION AND DIVISION TECHNIQUE

ABSTRACT

This thesis reports development and simulation of two analog-to-digital (AD) converters for low-power and small area applications, such as implantable telemetric biomedical recording applications. In development of these analog-to-digital (AD) converters current mode signal processing is chosen. Current mode signal processing has some advantages over voltage mode signal processing in low voltage and low power applications because of not requiring high precision resistors or capacitors. And one reason to be chosen current mode signal processing is many signal sources are current-type, such as temperature sensors, photo sensors and many others in biomedical. Processing the signal in current will not only avoid the use of a current to voltage converter but also cut down the components costs.

Current mode analog-to-digital converters use current mirrors to perform the required conversion. Therefore, the performances of the analog-to-digital converters are limited by the performance of the current mirrors. In the development of these ADCs, different types of current mirrors are used to improve. These current mirrors used have better output impedance than current mirror used in the previous designs. To decrease the complexity and power consumption clock-less architecture is chosen. By increasing the accuracy one more level is added to previous design.

Key words: Analog to digital converter, current mode approach, current mirror

AKIM ÇARPMA ve AKIM BÖLME TEKNİĞİ KULLANILAN ANALOG SAYISAL ÇEVİRİCİ

ÖZ

Bu tezde biomedikal kayıt uygulamaları ve düşük güç tüketimi uygulamaları için iki adet analog-sayısal çevirici geliştirilmesi ve simülasyonu yapılmıştır. Bu analog-sayısal çevirici geliştirilmesi sırasında akım modlu sinyal işleme yaklaşımı kullanılmıştır. Akım modlu sinyal işleme yaklaşımının düşük gerilim ve düşük güç tüketimi gerektiren durumlarda, yüksek duyarlıklı direnç ve kapasite gereksinimi olmadığı için gerilim modlu sinyal işleme yaklaşımına karşı avantajlara sahiptir. Akım modlu sinyal işleme tekniğinin seçilmesinin bir nedeni de sıcaklık, görüntü sensörleri ve biomedikaldeki sinyal kaynaklarının akım tabanlı olmasıdır. Bu alanlarda akım işleme yöntemi kullanıldığında akımdan gerilime çevirme yapılmayacaktır ve maliyeti de düşürecektir.

Akım modlu analog-sayısal çeviriciler gerekli çevirme işlemini gerçekleştirmek için akım aynalarını kullanmaktadırlar. Bu yüzden analog-sayısal çeviricilerin perfomansları kullanılan akım aynaları ile limitlidir. Yeni analog-sayısal çeviricilerin geliştirilmesinde farklı akım aynaları kullanılmıştır. Burada kullanılan akım aynaları, daha önce kullanılan akım aynalarından daha iyi bir çıkış direncine sahiptir. Karmaşıklığı ve güç tüketimini azaltmak için örnekleme devresi olmayan bir uygulama yapılmıştır. Sistemin doğruluğu artırılarak önceki tasarıma bir seviye daha eklenmiştir.

Anahtar kelimeler: Analog sayısal çevirici, akım modlu yaklaşım, akım aynaları

CONTENTS

Page

CHAPTER ONE
INTRODUCTION

Signal processing is a very important task for many applications in electronics. Electronic signals can be processed in either the analog or the digital domain. However digital signal processing is faster than analog signal processing, and some processes can only be done by digital signal processing. On the other hand, the signals that are to be processed are mainly analog. Therefore, analog-to-digital converters (ADCs) are one of the major blocks of the electronic structures.

The main requirements for an ADC are high accuracy, high conversion rate, low power consumption, and small chip area (Tezel, 1999). There are lots of techniques to satisfy these requirements, but not ADC can satisfy all requirements alone. Every technique has limitations and drawbacks. So the most convenient conversion technique should be chosen for conversion according to system. When the sensors or medical systems are dealing, provide output signals which can be very small and may have a large dynamic range; there is a need of low power, low voltage and smaller chip area. Appropriate technique should be chosen to satisfy these criteria's. Chosen ADC should dissipate low power and occupy small chip area. Considering low power and low current applications current mode signal processing has some advantages over voltage mode processing. Such as, generally current-mode circuits do not require amplifiers with high voltage gains thereby reducing the need for high performance amplifiers. At the same time, current mode circuits generally do not require either high precision resistors or capacitors and when capacitors are used to store the signal, the capacitors need not display either good ratio matching or good linearity. Consequently, current-mode circuits can be designed almost exclusively with transistors making them fully compatible with most digital processes. (Toumazou, Lidgey, Haigh 1990) Also to reduce the size of the design, and eliminate any clocked circuitry (which introduces noise in the analog circuits, and increases power dissipation), sample and hold circuitry is liked to eliminate. To catch, goal of that size and power dissipation reduction clocked circuitry and sample and hold circuitry eliminated. So chip area and power dissipation is reduced. So at

the output of the ADC there is gray coded. This gray coded output can be converted to other digital output with wanted circuitry.

According to limitations of the voltage mode processing in low power and low current applications current mode processing is chosen in this work. Also to reduce the power dissipation and chip area, clock and sample hold circuit is eliminated and gray coded output circuitry is implemented to ADC.

1.1 History of Current-Mode Algorithmic Analog-to-Digital Converters

Design of the current-mode algorithmic analog-to-digital converters started in the late 1980's. First basic current mirrors were used to copy the current in the converters. These converters had high conversion rates, occupied small area, and consumed low power. For example, the first current-mode algorithmic ADC occupied 0.4mm^2 area in a 3µm CMOS process, and achieved 200 kHz sampling rate while drawing 5mW power from a 5V supply; however, its resolution was only 6 bits which is too low for many applications (Narin & Salama 1988).

The reason of the low resolution was current mirrors, which could not copy the currents accurately. The accuracy was limited by the matching of the current mirrors and their low output resistance. Then, cascade current mirrors were used, which have higher output resistance. The accuracy of this converter was 7 bits and occupied an area of 0.76mm^2 in a 3µm CMOS process. The conversion time was 1.75µs and the power dissipation was 8.7mW (Narin& Salama 1990). Another method to overcome the errors caused by the low output resistance is using active current mirrors. An algorithmic current-mode ADC that uses active current mirrors achieves 8-bit resolution and 2µs conversion time, and it occupies an area of 0.74mm^2 in a 3um CMOS process while the power consumption is 63mW, which is too high (Narin & Salama 1990).

Later, it is observed that it is almost impossible to get more than 8-bit resolution with current mirrors, because even a device matching of 99.8 %, which is a difficult

task, results not more than 8-bit accuracy. To minimize the effect of matching on the resolution of current-mode algorithmic ADCs, dynamic current mirrors arc used in the converters. Another advantage of these converters was that they do not have to be pipelined, i.e. one bit cell can be used for generation of all the bits. These type, cyclic type, converters occupy less area and consume lower power while their sampling rate is lower.

A cyclic type converter, which was fabricated using a 3µm CMOS process, occupied 0.2mm^2 area and displayed a 10-bil resolution with a 25 kHz sampling rate. The power consumption was 3.5mW and operated from a single 5V supply, while the digital controller part was not included in the chip (Narin& Salama 1989).

Two years later in 1991 a 14-bit cyclic type converter based on dynamic current mirrors was fabricated in a 3pm CMOS process (Deval ,Roberts ,Declereq 1991). It is the highest resolution achieved up to now. But its conversion time was 175us and occupied an area of lmm^2. It consumed 2.5mW power from a 5V supply. It used a new-algorithm, which restricts die copied current between the full-scale current and half of it. It was one of the reasons that the convener accuracy was so high.

In 1994 a 10-bit pipelined convener was fabricated in a 2.4µm process (Macq & Jeppers 1994) Its sampling rate was 550ksample/s, which was very good. It occupied an area of 2.5mm: and consumed 20mW power. It used a digital correction algorithm called redundant-signed-digit (RSD), but it did not increase the resolution. The reason was that the RSD algorithm only eliminates offset error but actually other errors limit the accuracy.

In 1998 a low voltage algorithmic analog-to-digital converter is designed. The power supply of the converter was 1.5V (Narin & Salama 1988). It used a digital correction; algorithm, which is called modified reference no restoring (MRN). MRN algorithm is used to eliminate the comparison errors. The resolution of the converter was 10 bits and occupied 4mm: area in a 0.8µm n-well CMOS process. It consumed 2mW power and its sampling rate was 12ksample/s.

The technique which in this work improved and developed was firstly developed and applied by G. Rachmuth.

1.2 Research Objectives and Thesis Organization

The aim of this research is to improve ADC by using different current mirrors for biomedical applications. The ADC should be occupy small chip area and consumes low power.

To meet the requirements clock-less circuitry and current mode technique used design which is firstly introduced by G. Rachmuth is chosen. This design is developed by using different current mirrors. And by adding one level to ADC, a new ADC is designed in this work

Specific goals of this study are

1) To develop a current mode ADC using cascade end improved Wilson current mirrors. These advanced current mirrors allow the implementation of high accuracy, due to their high output impendence. And making comparison between these new ADCs

2) To improve the level of ADC by using cascade and improved Wilson current mirrors.

Chapter one is the introduction to thesis. In the Chapter Two the theoretical background information, different A/D converters and ADC performance parameters are presented. Chapter Three describes Current-Mode ADC based on Current Multiplication by using basic, cascaded and improved Wilson current mirrors for seven and eight level designs. Chapter four describes Current-Mode ADC based on Current division by using basic, cascaded and improved Wilson current mirrors for

seven and eight level designs. Chapter Five gives the experimental results of these ADCs. Chapter Six presents the conclusion.

CHAPTER TWO
FUNDAMENTALS OF CURRENT MODE ANALOG TO DIGITAL CONVERTERS

2.1 Introduction

An analog-to-digital converter quantizes an analog signal into a digital code at discrete time points. According to the sampling theorem, the input signal band is limited to half of the sampling frequency to avoid aliasing with the sample rate repeated spectra.

The continued proliferation of mixed analog-digital VLSI systems has and will ensure that the need for small size. High speed analog-to-digital converters (ADCs) will continue to grow. Due to the present dominance of digital technologies, the fabrication of the ADC must be compatible with these technologies. Current mode techniques *(i.e.* circuits in which the signal IS essentially processed in the current domain) offer a number of advantages. Due to the non-linear I-V relationship exhibited by most transistor structures, a small change in the input or controlling voltage results in a much larger change in the output current.

Consequently, for a process with a fixed voltage supply, the usable dynamic range of current mode signals is significantly larger than that of voltage mode signals. At the same time, a change in the current level flowing through any node is not necessarily accompanied by a change in the voltage level at that node. Hence the parasitic capacitances which are always present and must be charged or discharged with the changing voltage levels will not degrade the circuit's maximum operating speed .Therefore current mode circuits offer two potential advantages: improved dynamic range and improved operating speeds. In addition, circuits designed to exploit current mode techniques, offer auxiliary benefits such as simpler circuitry and lower power consumption. Consequently, current mode techniques have been used for a wide variety of signal processing circuits,

including amplifiers, multipliers, filters and digital-to analog conveners in a variety of different VLSI technologies. (Narin & Salama 1988)

2.2 Analog to digital converter types

There are a vast number of ADCs in literature; however, they can be grouped into five major categories: flash, integration, over sampling, successive approximation, and algorithmic ADCs. This section gives an overview of these approaches and explains their advantages and disadvantages.

2.2.1 Flash analog-to-digital converters

Flash ADCs use one analog comparator and one reference voltage for every quantization level from zero to full scale. Each of these reference voltages is compared with the input voltage in the same time interval. The outputs of these comparators drive an encoding logic to generate the equivalent digital value. Although these converters are very fast, they occupy very large chip area and consume very high power. Because for an N-bit converter one needs 2^N converters and voltage references. For example, one of this type ADCs achieves 10-bit resolution and 100Msample/s conversion rate; however, it dissipates 1.1W power from a 5V power supply and occupies 50mm^2 area in a 1um CMOS process. (Tezel , 1999)

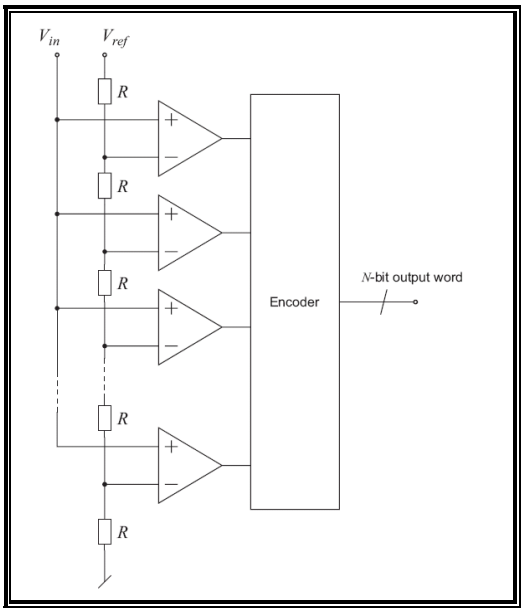

Figure 2.1 Flash converter

2.2.2 Integrating analog-to-digital converters

Integrating analog-to-digital converters use a capacitor and a constant current source. The input signal is sampled as a voltage on a capacitor. The capacitor is then discharged using a constant current source, and the discharging time gives the magnitude of the signal. These converters need high precision current sinks to linearly discharge the capacitor and very accurate counters to measure the discharging time. These type converters are not so fast, but their resolution is high. Their power consumption is lower than the flash type converters, and they occupy a smaller chip area. For example, a 14-bit integrating type ADC operates at 50 kHz and occupies 12mm^2 area in a 2um bipolar process.

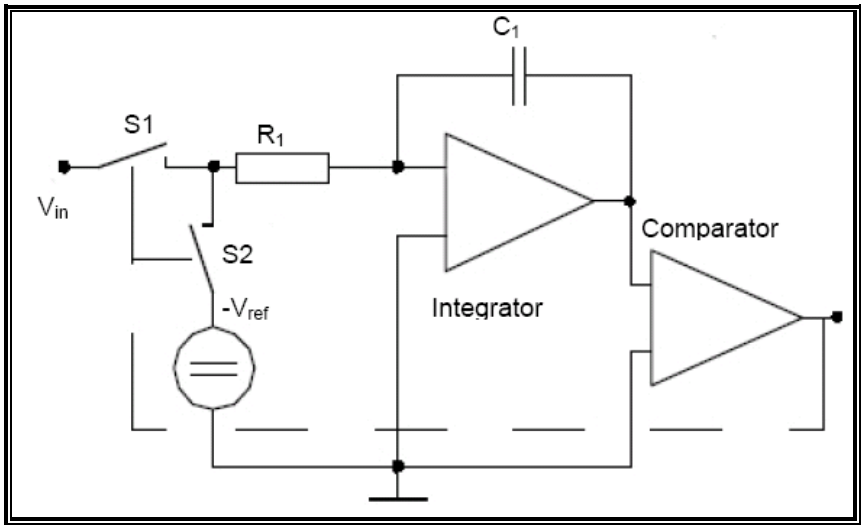

Figure 2.2 Integrating analog-to-digital converters

2.2.3 Oversampling analog-to-digital converters

Oversampling ADCs are based on the translation of high-speed, low-resolution samples of a band-limited input signal into a higher resolution, lower speed output. In an oversampling ADC the input samples are summed in an integrator that feeds its output to a comparator. The outputs of the comparator is fed serially to a digital filter and also used to control a 1-bit digital-to-analog convener (DAC) in the feedback loop, which outputs either a positive or a negative reference voltage. These type converters do not require accurate analog circuits but they use complex digital circuits to increase the resolution. They can reach up to 20-bit resolution but their conversion rate is low. Recently, a 15-bit ADC has been realized with a Nyquist rate of 2MHz. It occupies an area of $5.25mm^2$ in a 1 um CMOS process and its power dissipation is 230mW.

2.2.4 Successive approximation analog-to-digital converters

Successive approximation type analog-to-digital converters use digital-to-analog converters (DACs) to perform the conversion. In these ADCs, the input signal is compared with suitable reference voltages that arc created by the DACs, so that alter each comparison one bit is obtained. They convert the analog data to digital by N-comparisons for an X-bit converter. The DAC and the comparator

determine the speed and resolution of these type ADCs. One of these type converters was recently reported, and it achieves a l0Msample/s conversion rate and 10-bit accuracy, while dissipating 340mW power from a 5V power supply and occupying 36mm: area in a l um CMOS process (A.Tezel, 1999).

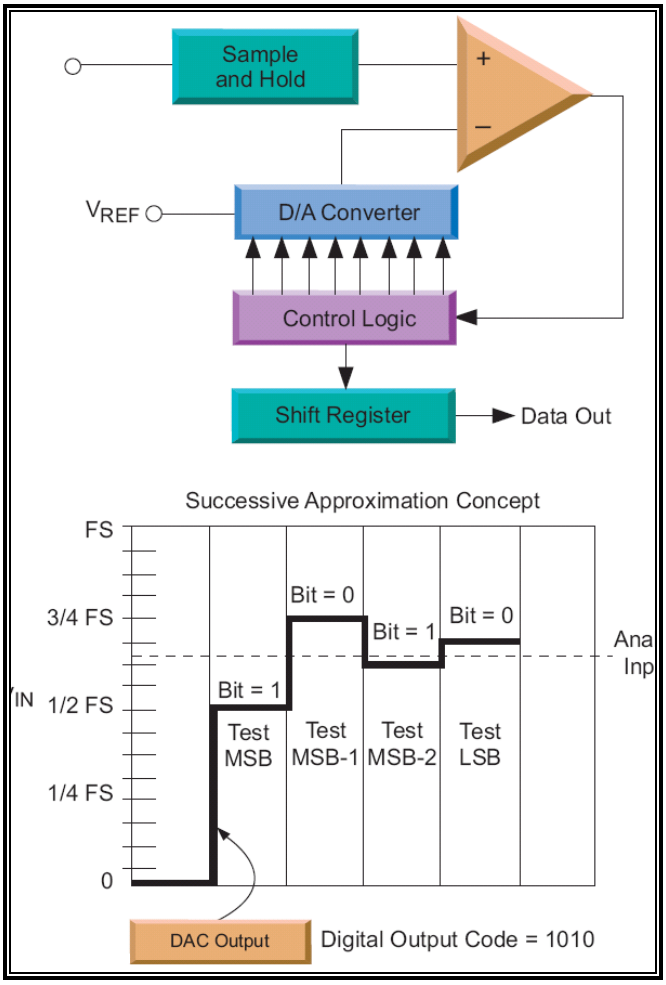

Figure 2.3 Successive approximation analog-to-digital converter

2.2.5 Algorithmic analog-to-digital converters

Algorithmic ADCs are similar to the successive approximation type ADCs with one main difference: in successive approximation ADCs, the reference signal is changed and compared to the input signal; whereas, in algorithmic ADCs, the reference signal is fixed and the input signal is processed. The input signal is

multiplied by two and compared with the reference current. If the input signal is larger that the reference signal, then the output is digital 1, otherwise it is digital 0. If the digital output is 1, then, the reference signal is subtracted from the input signal and the resulting signal is multiplied by two; or else, the input signal is multiplied by two without the subtraction operation. This process continues until the least significant bit is obtained. This type of ADCs occupies very small chip area and dissipates very low power. For example, such a high performance algorithmic ADC provides 10-bit accuracy, 550ksample/ s conversion speed, while occupying 2.5mm^2 in a 2.4µm process and consuming 20 mW power. (Tezel, 1999)

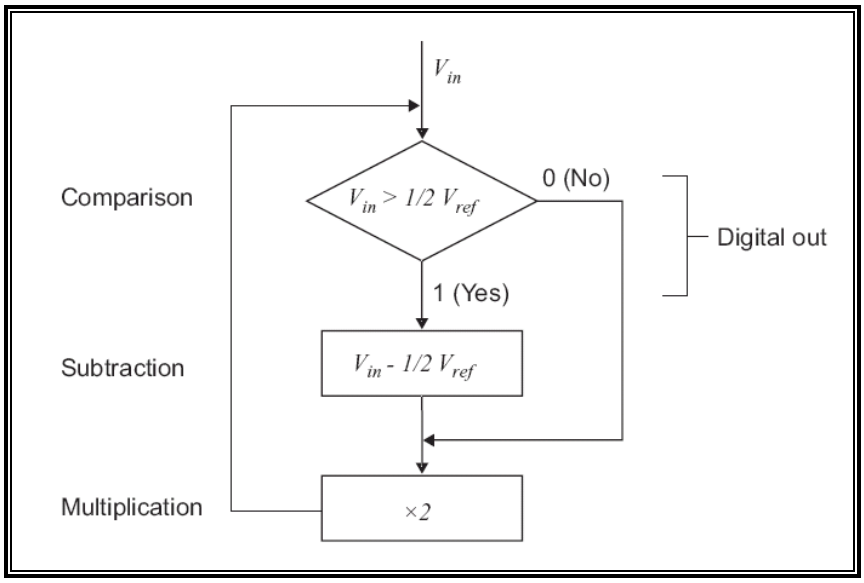

Figure 2.4 Algorithmic analog-to-digital converter

Each of the conversion techniques presents a performance trade-off, and the designer should choose the optimum approach to address the needs of the design. If high speed is required, **die** designer should sacrifice large chip area and high power consumption by choosing the flash type converters. When high resolution is needed, the integrating or oversampling ADCs should be used. But integrating type ADCs need precision components, and the oversampling method results in a large chip area, slow conversion rate, and high power consumption due to the required post-conversion processing. If a small size and low power converter is

required, the algorithmic ADC is the best choice. The drawback of this type converter is the moderate resolution and conversion rate. Therefore, there is no universal analog-to-digital conversion technique that is best suited to all situations.

2.3 Current-Mode Analog Integrated Cırcuıts

During the last 40 years, the vast majority of analog circuits have used voltages to represent and process relevant signals. However, recently, current-mode signal processing circuits, in which signals and state variables are represented by currents rather than voltages have shown advantages over their voltage-mode counterparts.

Initially, the widespread use of MOS technology, with its unique ability to accurately store and transfer voltages or charge packets, led to the development of analog integrated circuit techniques in which voltage was used as the signal. Although these techniques are quite successful in many applications, reductions in the available supply voltage and the deterioration in the performance of the analog components caused by the move to ever smaller geometries, is likely to limit their performance.

Generally current-mode circuits do not require amplifiers with high voltage gains thereby reducing the need for high performance amplifiers. At the same time, current mode circuits generally do not require either high precision resistors or capacitors and when capacitors are used to store the signal, the capacitors need not display either good ratio matching or good linearity. Consequently, current-mode circuits can be designed almost exclusively with transistors making them fully compatible with most digital processes.

Current-Mode operated circuits include advantages such as higher bandwidth, higher dynamic range, and they are more amenable to lower power supplies. Furthermore, advances in integrated circuit design have meant that state-of-the-art analog integrated circuit design is now able to exploit the potential of current-

mode analog signal processing, providing attractive and elegant solutions for many circuit and system problems. In many applications, circuits operating in the current domain will bring benefits. One reason is that many signal sources are current-type, such as temperature sensors, photo sensors and many others in biomedicine. Processing the signal in current will not only avoid the use of a current-to-voltage converter but also cut down the components' cost.

For example, a comparator for current input and voltage output can be implemented with only four MOS transistors, while in voltage domain it is impossible to realize with so few devices. In current domain, computations like addition and subtraction can be performed with just two current mirrors, while in voltage domain, these functions are very difficult to achieve for a large range of inputs. Especially in the low-voltage circuits, voltage-domain behavior will suffer due to the threshold voltage of the devices. Such difficulties can be overcome by operating in the current domain.

2.4 Effect of Output Resistance on the ADC Performance

Finite output resistance of the current mirrors is one of the main performance limitation factors on the ADCs. Although MOS transistors have high output resistance, r_o , at saturation mode, it is not high enough to achieve high accuracy. For example, basic current mirrors can not achieve more than 6-bit accuracy. One way to get high output resistance is to increase the channel length of the device. However, this increases the device size and parasitic capacitance.

A better way to increase the output resistance is to use cascade structures. The output resistance values of the cascade current mirror and improved Wilson current mirror are much higher than that of the simple current mirror.

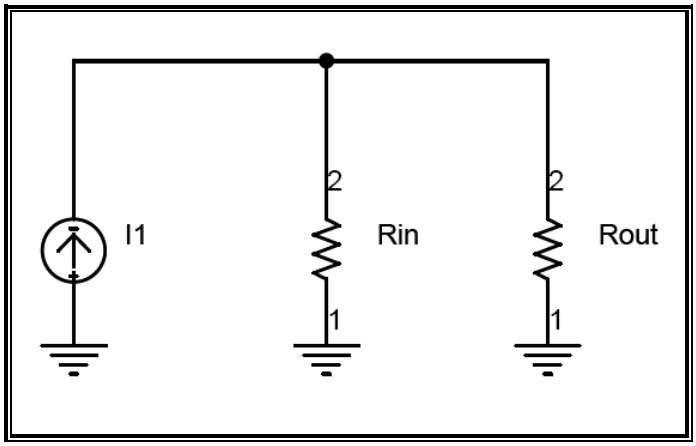

Figure 2.5 Small signal model for current mirrors

Figure 2.6 shows the small signal model for current mirrors. R_{out} and R_{in} are the output resistance and input resistance of the current mirror, respectively, and I_1 is the input current. The error current, ΔI, over input current

$$\frac{\Delta I}{Iin} = \frac{Rin}{Rin + Rout} \approx \frac{Rin}{Rout} \tag{2.1}$$

For basic current mirror this equation (2.1) becomes

$$\frac{\Delta I}{I_{in}} = \frac{1}{r_o gm} = \frac{\lambda\beta(V_{GS}-V_T)^2}{2\beta(V_{GS}-V_T)} = \frac{\lambda(V_{GS}-V_T)}{2} \tag{2.2}$$

where gm is the transconductance. V_{GS} is the gate to source voltage of the mirroring transistor, and V_T is the threshold voltage. The maximum error occurs when V_{GS} is maximum.

$$V_{GSMAX} = \frac{V_{DD} + V_T}{2} \tag{2.3}$$

If we insert r_o gm

$$\frac{\Delta I}{I_{in}} = \frac{\lambda\left(\frac{V_{DD}+V_T}{2} - V_T\right)}{2} = \frac{\lambda(V_{DD}-V_T)}{2} \tag{2.4}$$

The maximum resolution that can be obtained is

$$N = -\frac{ln\left(\frac{\lambda(V_{DD}-V_T)}{2}\right)}{ln2} - 1 \tag{2.5}$$

Assuming that V_{DD} =5V, λ= 0.02 V^{-1} and V_τ = 0.75 V then N= 5.55, i.e. 5-bit accuracy.

For cascade current mirror, the current error over input current becomes,

$$\frac{\Delta I}{Iin} = \frac{2}{r_o^2 gm^2} = \frac{\lambda^2(V_{GS}-V_T)^2}{2} \tag{2.6}$$

V_{GSMAX} of cascade minor is the same as V_{GSMAX} of basic current mirror.

$$\frac{\Delta I}{Iin} = \frac{\lambda^2\left(\frac{VDD-VT}{2}\right)^2}{2} = \frac{\lambda^2(VDD-VT)^2}{8} = \frac{1}{2}\left(\frac{\lambda(VDD-VT)}{2}\right. \tag{2.7}$$

$$N = -\frac{ln\left[\frac{1}{2}\left(\frac{\lambda(V_{DD}-V_T)}{2}\right)^2\right]}{2} - 1 \tag{2.8}$$

According to the calculations above, the accuracy of basic current mirror is limited by the finite output resistance(Tezel , 1999)

2.5 Effect of Device Mismatches

Device mismatches is another important drawback of current mirrors. Even with very large device sizes and careful layout drawing, it is almost impossible to reach a matching better than 0.2%. The mismatch errors are inevitable, but some current mirrors are less sensitive to device matching than the other ones.

The device mismatches can be classified into two categories; threshold voltage, V_T mismatches and β mismatches.

$$\beta = \frac{\mu C_o W}{L} \tag{2.9}$$

Where μ is the carrier mobility, C_o is the gate oxide capacitance per unit area, W is the device width and L is the device length. β mismatches are equal for each of the current mirror type.

$$N = \frac{ln\left(\frac{\beta}{\Delta\beta}\right)}{ln2} - 1 \tag{2.10}$$

Where N is the accuracy of the ADC in bits, and Δβ is the β difference between the mirroring transistors. A β mismatch of 0.2% results in a maximum ADC accuracy of 8 bits.

V_T mismatches is inversely proportional to the dynamic range of the current mirror type. Table 2.2 shows the limitations of β and V_T mismatches, and finite output resistance on the ADC accuracy implemented with the two current mirror types assuming that β and V_T mismatch is 0.2%, V_{DD}=5v. and V_T=0.75V. The dynamic range of the basic current mirror is high; therefore, V_T mismatch error limits the ADC accuracy to 8 bits.

$$N = 1.44\ ln\left[\frac{V_{DD} - V_T}{\Delta V_T}\right] - 3 \qquad (2.11)$$

Where, ΔV_T is the threshold voltage difference between the mirroring transistors. The dynamic range of cascade current mirrors is low, and V_T mismatch error limits the ADC accuracy to 7 bits.

2.6 ADC PERFORMANCE SPECIFICATIONS

ADC performance specifications are generally categorized in two ways: DC accuracy and dynamic performance. Most applications use ADCs to measure a relatively static, DC-like signal (for example, a temperature sensor or strain-gauge voltage) or a dynamic signal (such as processing of a voice signal or tone detection). The application determines which specifications the designer will consider the most important

2.6.1 DC Accuracy

Many signals remain relatively static, such as those from temperature sensors or pressure transducers. In such applications, the measured voltage is related to some physical measurement, and the absolute accuracy of the voltage measurement is important. The ADC specifications that describe this type of accuracy are offset error, full-scale error, differential nonlinearity (DNL), and integral nonlinearity (INL). These four specifications build a complete description of an ADC's absolute accuracy.

The transfer function of an ADC is a plot of the voltage input to the ADC versus the code's output by the ADC. Such a plot is not continuous but is a plot of 2N codes, where N is the ADC's resolution in bits. If you were to connect the codes by lines (usually at code-transition boundaries), the ideal transfer function

would plot a straight line. A line drawn through the points at each code boundary would begin at the origin of the plot, and the slope of the plot for each supplied ADC would be the same as shown in Figure 2.6.

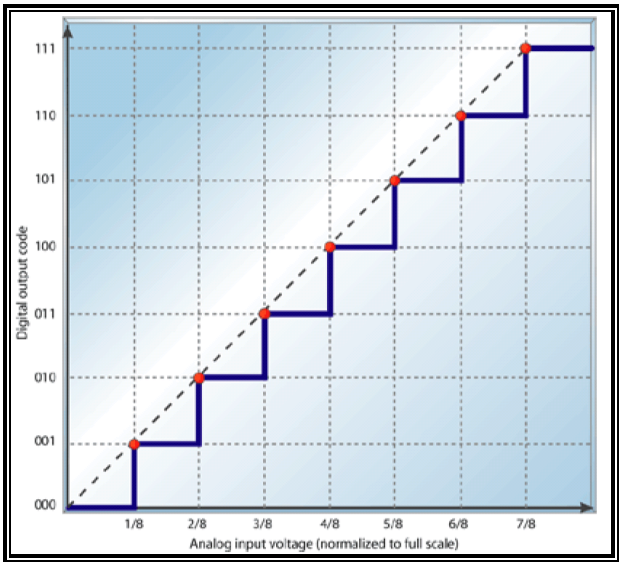

Figure 2.6 the ideal transfer function of ADC

Figure 2.6 depicts an ideal transfer function for a 3-bit ADC with reference points at code transition boundaries. The output code will be its lowest (000) at less than 1/8 of the full-scale (the size of this ADC's code width). Also, note that the ADC reaches its full-scale output code (111) at 7/8 of full scale, not at the full-scale value. Thus, the transition to the maximum digital output does not occur at full-scale input voltage. The transition occurs at one code width—or least significant bit (LSB)—less than full-scale input voltage .

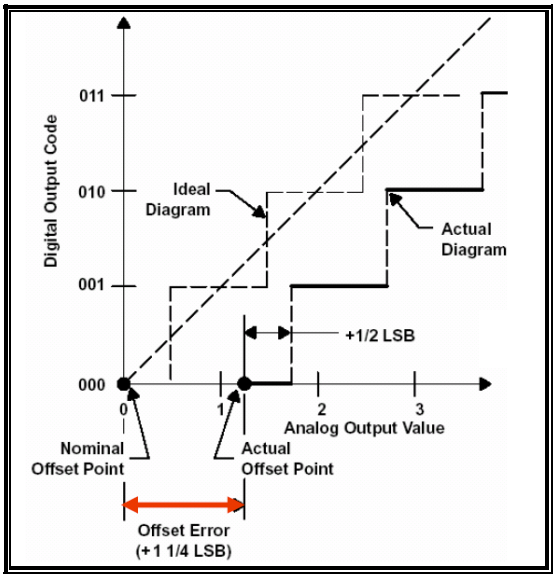

Figure 2.7 the transfer function with an offset of - 1/2 LSB

The transfer function can be implemented with an offset of - 1/2 LSB, as shown in Figure2.7. This shift of the transfer function to the left shifts the quantization error from a range of (- 1 to 0 LSB) to (- 1/2 to +1/2 LSB). Although this offset is intentional, it's often included in a data sheet as part of offset error (see section on offset error). Limitations in the materials used in fabrication mean that real-world ADCs won't have this perfect transfer function. It's these deviations from the perfect transfer function that define the DC accuracy and are characterized by the specifications in a data sheet. The DC performance specifications described have accompanying figures that depict two transfer function segments: the ideal transfer function (solid, blue lines) and a transfer function that deviates from the ideal with the applicable error described (dashed, yellow line). This is done to better illustrate the meaning of the performance specifications.

2.6.1.1 Offset error, full-scale error

The ideal transfer function line will intersect the origin of the plot. Offset error can be observed as a shifting of the entire transfer function left or right along the input voltage axis, as shown in Figure 2.8.

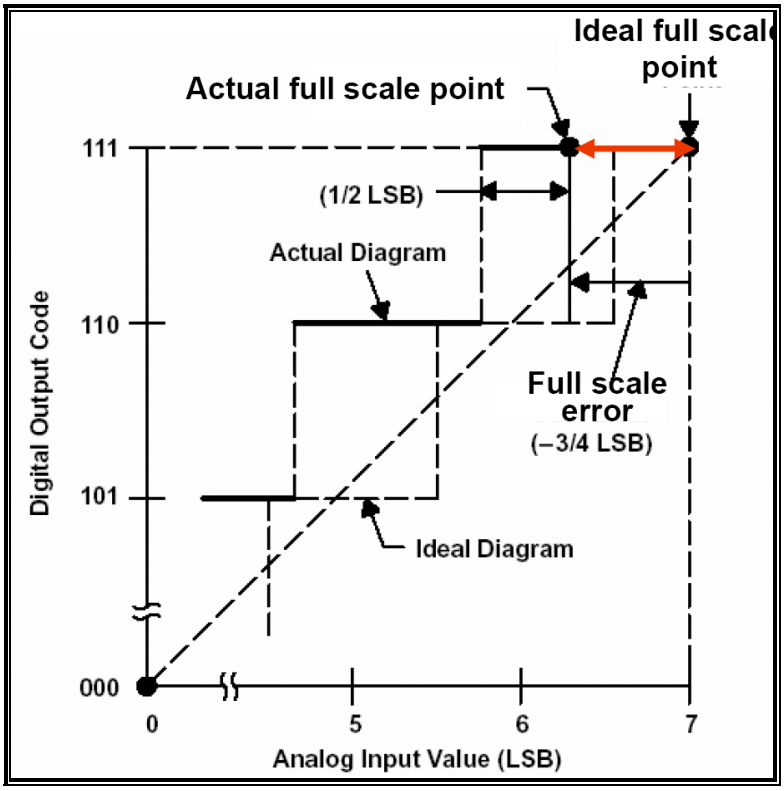

Figure 2.8 Full-scale error of ADC

Full-scale error is the difference between the ideal code transition to the highest output code and the actual transition to the output code when the offset error is zero. This is observed as a change in slope of the transfer function line as shown in Figure2.8. A similar specification, gain error, also describes the nonideal slope of the transfer function as well as what the highest code transition would be without the offset error. Full-scale error accounts for both gain and offset deviation from the ideal transfer function. Both full-scale and gain errors are commonly used by ADC manufacturers.

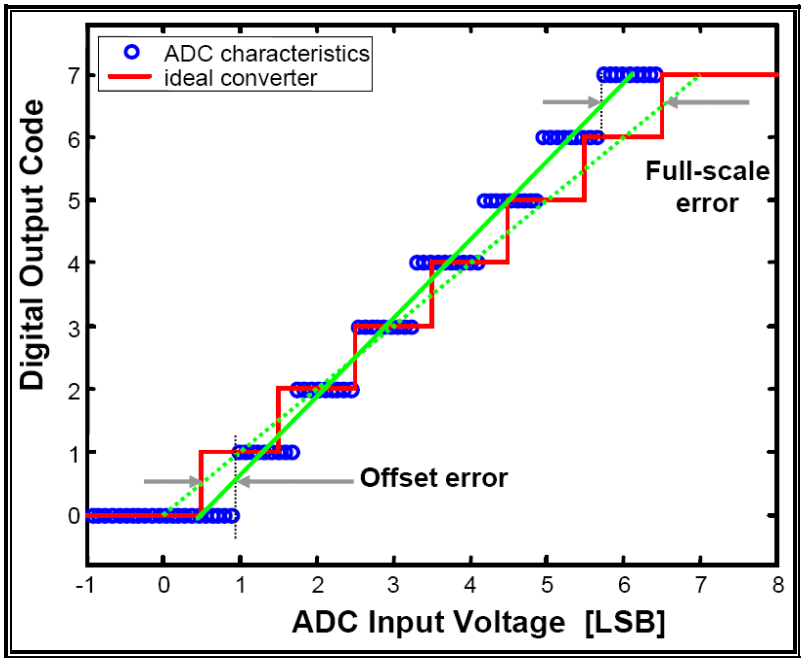

Figure 2.9 Off-set and full scale error of ADC

2.6.1.2 Nonlinearity

Ideally, each code width (LSB) on an ADC's transfer function should be uniform in size. The difference in code widths from one code to the next is differential nonlinearity (DNL). The code width (or LSB) of an ADC is shown in Equation 2.12.

$$\mathbf{LSB} = \frac{V_{ref}}{2^N} \tag{2.12}$$

The voltage difference between each code transition should be equal to one LSB, as defined in Equation 2.12. Deviation of each code from an LSB is measured as DNL. This can be observed as uneven spacing of the code "steps" or transition boundaries on the ADC's transfer-function plot. In Figure 2.10, a selected digital output code width is shown as larger than the previous code's step size. This difference is DNL error. DNL is calculated as shown in Equation 2.13.

$$DNL = \frac{(V_{n+1} - V_n)}{V_{LSB}} \tag{2.13}$$

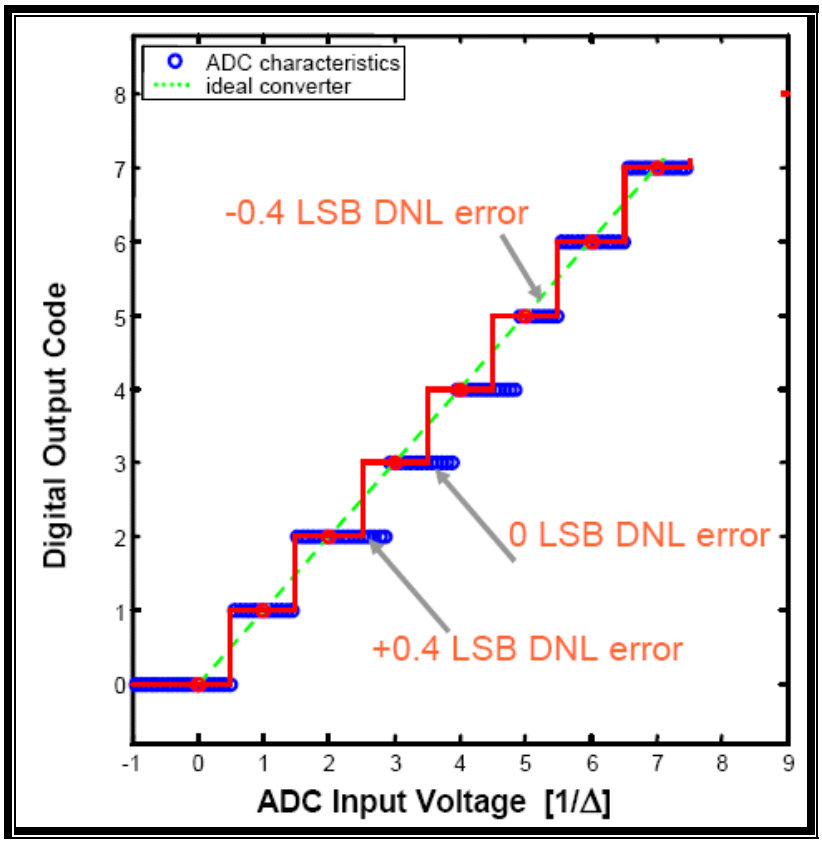

Figure 2.10 DNL error of ADC

The integral nonlinearity (INL) is the deviation of an ADC's transfer function from a straight line. This line is often a best-fit line among the points in the plot but can also be a line that connects the highest and lowest data points, or endpoints. INL is determined by measuring the voltage at which all code transitions occur and comparing them to the ideal. The difference between the ideal voltage levels at which code transitions occur and the actual voltage is the INL error, expressed in LSBs. INL error at any given point in an ADC's transfer function is the accumulation of all DNL errors of all previous (or lower) ADC codes, hence it's called integralnonlinearity. This is observed as the deviation from a straight-line transfer function, as shown in Figure 2.11.

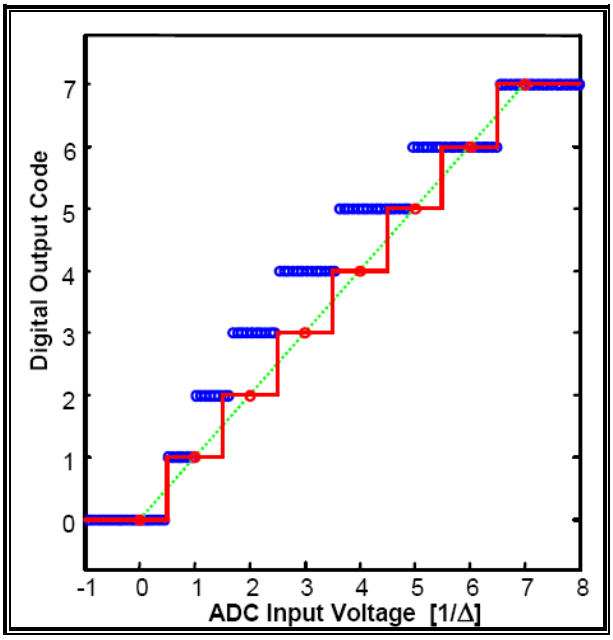

Figure 2.11 INL error of ADC

CHAPTER THREE
CURRENT-MODE ADC BASED ON CURRENT MULTIPLICATION TECHNIQUE

Like the name of the approach, technique is based on the multiplication of the reference signal and comparing these references with the input signal. This approach is similar to flash converter. Principle of the conversion is simple; so it is easy to implement. This approach was first used by G.Rachmut than H. Helble improved the system. Before this study, only simple current mirrors and seven conversion levels were used with this approach. With this study previous design which was 7 level and simple current mirrors was improved, by using improved Wilson current mirrors and cascade current mirrors.

Another characteristic of the system is its operation in subthreshold domain. For this reason, the analog-to-digital converter used within the system has to operate in subthreshold regime. A problem with subthreshold circuits is that systems operating in this mode are both low power and slow. Consequently, the need for a subthreshold current mode A/D converter is due to the specifications which need energy efficiency. However, the most important drawback of using system in subthreshold region is being slower than other solutions.

3.1 Principle of Operation

Principle of the operation is similar to the flash conversion. But the reference is not divided by using resistors. The reference current is copied by using current mirrors. And as a result different current levels are done. In the beginning the reference current is multiplied by the factor of desired level. According to number of levels LSB is I_{ref} and MSB become N times I_{ref}. Here is the N denotes the level of conversion. If eight conversion levels are desired than N becomes eight.. Basic conversion algorithm can be expressed as follows.

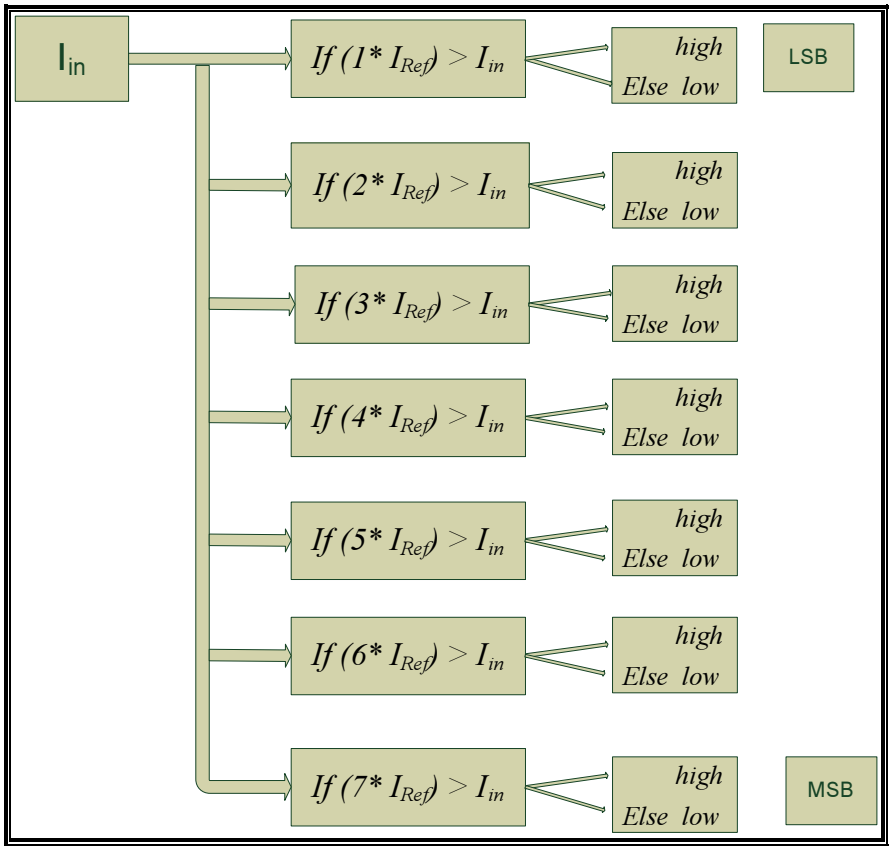

Figure 3.1 Principle of Current Multiplication Technique

Being calculated by linear multiplication of levels, the related conversions become linear. Linear conversion characteristic of this type ADC is one of the most important features.

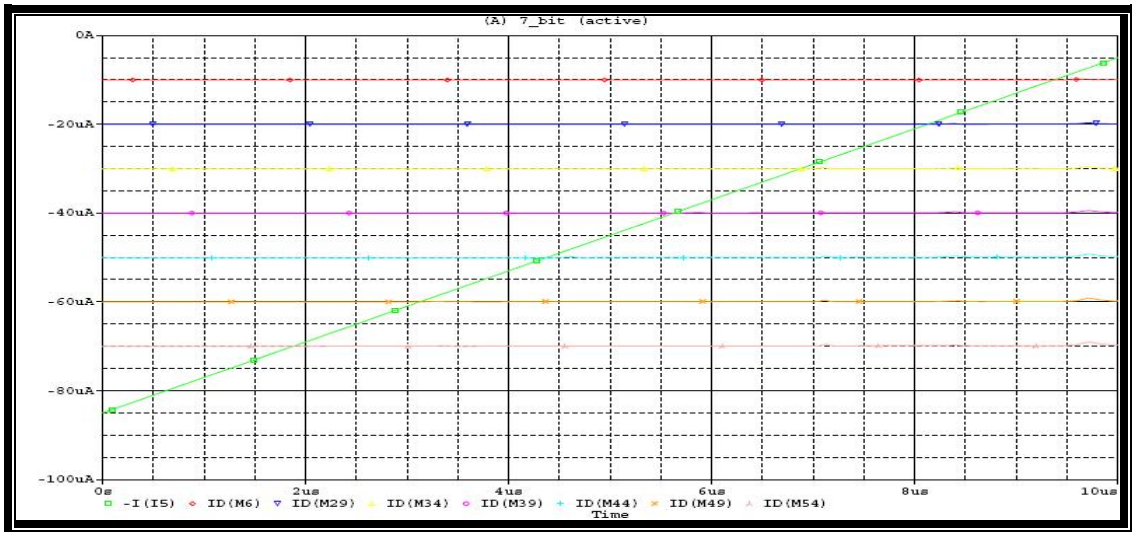

Figure 3.2 linear conversion levels of the seven bit ADC

Figure 3.2 shows the linear conversion levels of the seven bit ADC. The reference current is 10 µA, having seven levels subsequent levels are multiplication of the reference and goes 20 µA, 30 µA...

3.2 Current mode ADC based on Current Multiplication Technique using simple current mirrors

The current-mode analog-to-digital conversion technique has been known for many years as a conversion method that can take advantage of relatively simple hardware to produce ADCs. A current mode conversion is performed as shown in Figure 3.3. The input signal, I_{in} which can take on any value, I_{ref}, is the reference current the circuit shown below is only one bit of the conversion.

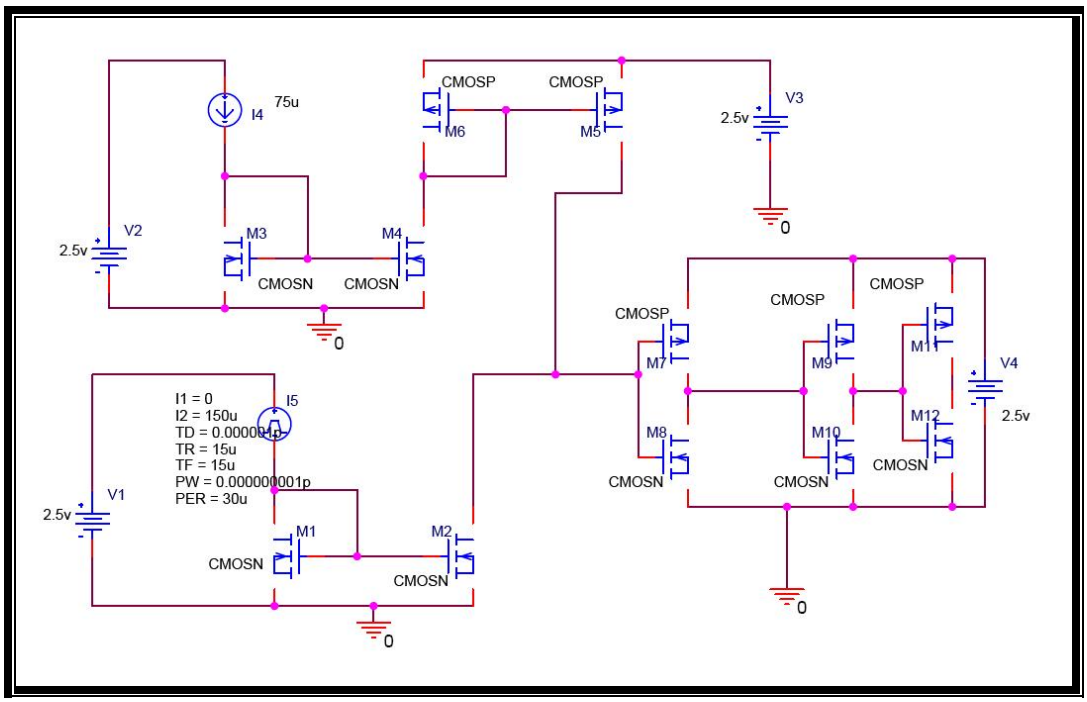

Figure 3.3 Single level of Simple current mirrors used ADC

Here the current source I_5 denotes the reference current I_{ref} and I_4 denotes the input signal I_{in}. I_{ref} is mirrored by an *n*-mirror to isolate the converter from the outside world. To transform the current sink into a current source, the current gets mirrored again but this time a *p*-mirror is used. Neglecting the current mirror error,

due to device variances caused by production tolerances, the current should still have the exact same value as the reference current had before it was mirrored twice.

The other input to the cell, I_{in}, also passes trough an *N*-mirror first, transforming it into a current sink. It has the same value as I_{in} had, but the sign changes. This node is connected to the drain of the *p*-type transistor of the mirror which provides the isolated I_{ref} in the form of a current source. In addition, the input of a CMOS current comparator is connected to this node as well. It is supposed to switch from low to high when the input current (the current sink) becomes bigger than the reference current (the current source).

To meet these requirements, the existing comparator design had to be extended by adding a third inverter stage to the two existing ones. It inverts the signal after the second stage a third time, so that the comparator output switches when the absolute value (I_{in}) of the current sink becomes bigger than the absolute value (I_{ref}) of the current source. SPICE experiments showed the usage of only a single inverter stage in the comparator would principally work as well but suffers from an extreme comparison speed loss by at least ten magnitudes. Since this is not acceptable for the target application, it was decided to choose the three inverter design for this project. (Helbe, 2004)

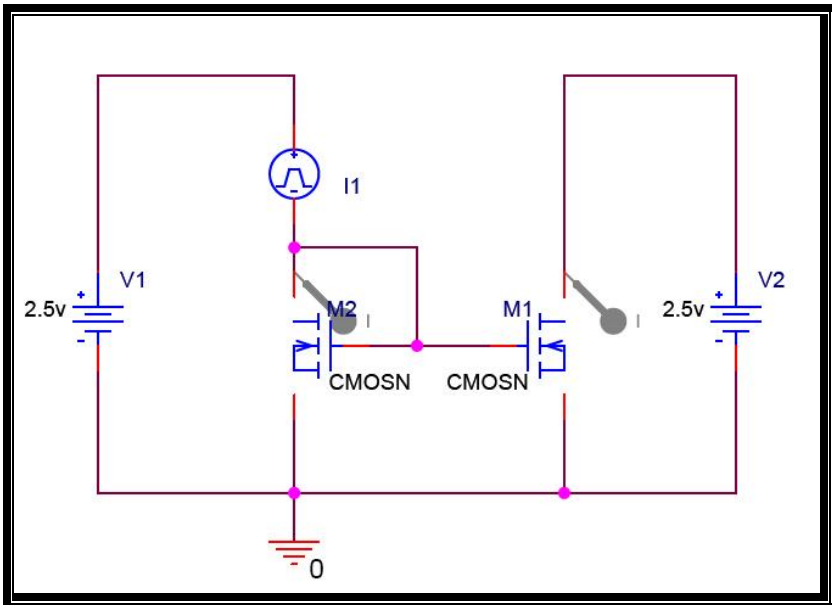

Figure 3.4 A simple CMOS current mirror

A simple CMOS current mirror is shown in figure 3.4, in which it is assumed that both transistors are in the active region. If the finite output impedances of the transistors are ignored, and it is assumed that both transistors are the same size, then M_1 and M_2 will have the same current since they both have the same gate-source voltage, V_{gs}. However, when finite output impedance is considered, whichever transistor has a larger drain-source voltage will also have a larger current.

In addition, the finite output impedance of the transistors will cause the small-signal output impedance of the current mirror, that is, the small-signal impedance looking into the drain of M_1, to be less than infinite. To find the output impedance of the current mirror, r_{out}, the small-signal circuit is analyzed after placing a signal source, v_x, at the output node. Then by definition, r_{out} is given by the ratio v_x/i_x, where i_x is the current flowing out of the source and into the drain of M_1. (Johns&Martin, 1997)

$$I_{Ref} = I_1 = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{Th})^2 (1 + \lambda V_{DS1}) \tag{3.1}$$

$$I_{out} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS1} - V_{Th})^2 (1 + \lambda V_{DS2}) \tag{3.2}$$

Which enable to express the output current, I_{out} *as* a function of I_{in}, $V_{out\ and}$ V_{DS1} to simplify algebraic calculations, we assume the last term equals to zero. Thus, V_{Gs1} is directly derived from the former equation and after substitution in the letters it gives;

$$I_{out} = I_{Ref}\frac{(W/L)_2}{(W/L)_1}(1 + \lambda V_{out}) \tag{3.3}$$

MOS is considered individually before starting calculation of the simple current mirror output impendence. M_1 is diode connected and that I_{jn} does not exist in the small-signal model; I_{in} was replaced with an open circuit because it is an independent current source. A low-frequency small-signal model is used for M_2, (i.e., all the capacitors are ignored in the model). This small-signal model can be further reduced by riding the Thevenin-equivalent circuit. The Thevenin-equivalent output voltage is 0 since the circuit is stable and contains no input signal. This circuit's Thevenin-equivalent output impedance is found by applying a test signal voltage, v_y, at v, and measuring the signal current, i_y , as shown in figure 3.5.

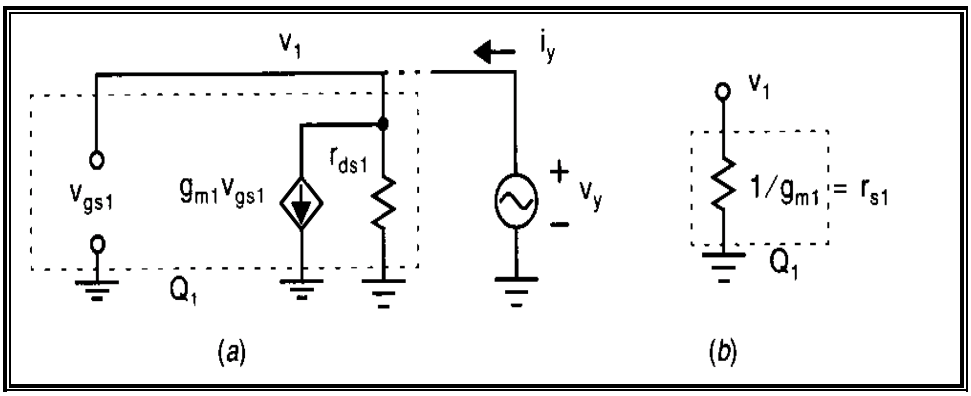

Figure 3.5 a- small signal model of CMOS b- Equivalent small signal model

Here, the current i_y is given by

$$i_y = \frac{v_y}{r_{ds1}} + g_{m1}v_{gs1} = \frac{v_y}{r_{ds1}} + g_{m1}v_y \tag{3.4}$$

Recalling that the output impedance is given by v_y/i_y, the output impedance equals $l/g_{m1||}$ $r_{dsl.}$ Because typically $r_{dsl}>>1/g_{m1}$. The output impedance is approximately $l/g_m i$ (which is also defined to be r_{s1}), which results in the equivalent model shown in Figure 3.5 .

Using the simplified small-signal model for the overall current mirror, as shown in Figure 3.6, where v_{gs2} has been connected to ground via a resistance of $l/g_m 1$- Since no current flows through the l/g_{ml} resistor, v_{gs2} equals 0 no matter what voltage level v_x is applied to the current-mirror output. This should come as no surprise, since MOS transistors operate unilaterally at low frequencies. Thus, since $g_{m2}V_{gS2}$ = 0, the circuit is simplified to the equivalent small-signal model shown in Figure 3.5. The small-signal output impedance, r_{out1}, is simply equal to r_{ds2}. (Johns&Martin, 1997)

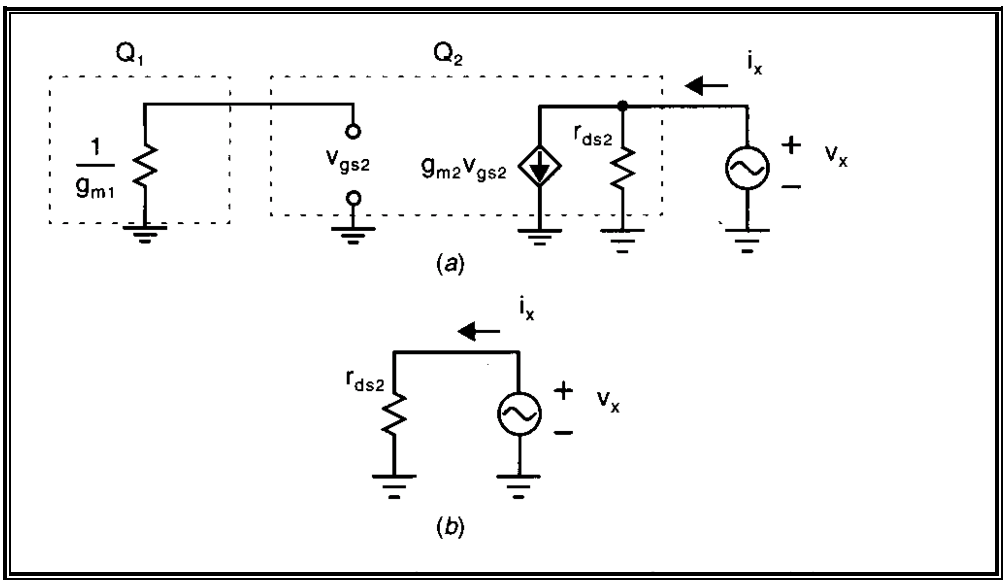

Figure 3.6 a- Small signal model of simple current mirror b- Simplified small signal model

Figure 3.7 shows the entire circuitry which is necessary for the seven level current mode A/D converters. It is composed of seven of the bit cells from Figure 3.3. Since every stage of the comparator requires its own copy of I_{in}, it has to be copied seven times. The copies are obtained by connecting the gates of *n*-MOS transistors to the node which drives the gate of the second transistor in the *n*-mirror for I_{in}. They form the I_{in} input network which can be identified on the left hand side

of the schematic in Figure 3.7. Since they are all part of an *n*-type current mirror, their drains are in a second connection line connected to the ground node. The source of each I_{in} is copied by the transistor directly connected to the comparator input of the corresponding bit cell. For the input of the second bit cell, I_{Ref} times two is required. It is obtained by taking a copy of I_{Ref} from the first cell and then doubling it in the *n*-mirror of bit cell number two. The current doubles because the gates of two transistors of the same dimensions are connected in parallel.

For the input of bit cell number three, three times I_{ref} is required. Since two can not be divided by three, doubling does not work again. But, according to Kirchhoff's current law, making one copy of 2 * I_{ref} and one copy of I_{ref} itself and adding them together results in 3 * I_{ref}. Four times I ref can be obtained by making a copy of 2 * I_{ref} and doubling it as done in bit cell number two. Five times I ref can be obtained by making one copy of 2 * I_{ref} and one copy of 3 * I_{ref} and adding them together. Six times I ref again is obtained by doubling a copy of 3 * I_{ref} as done before in the case of bit cell number two and four. Finally, seven times I_{ref} is obtained by adding a copy of 6 * I_{ref} to a copy of I_{ref}. (Helbe, 2004)

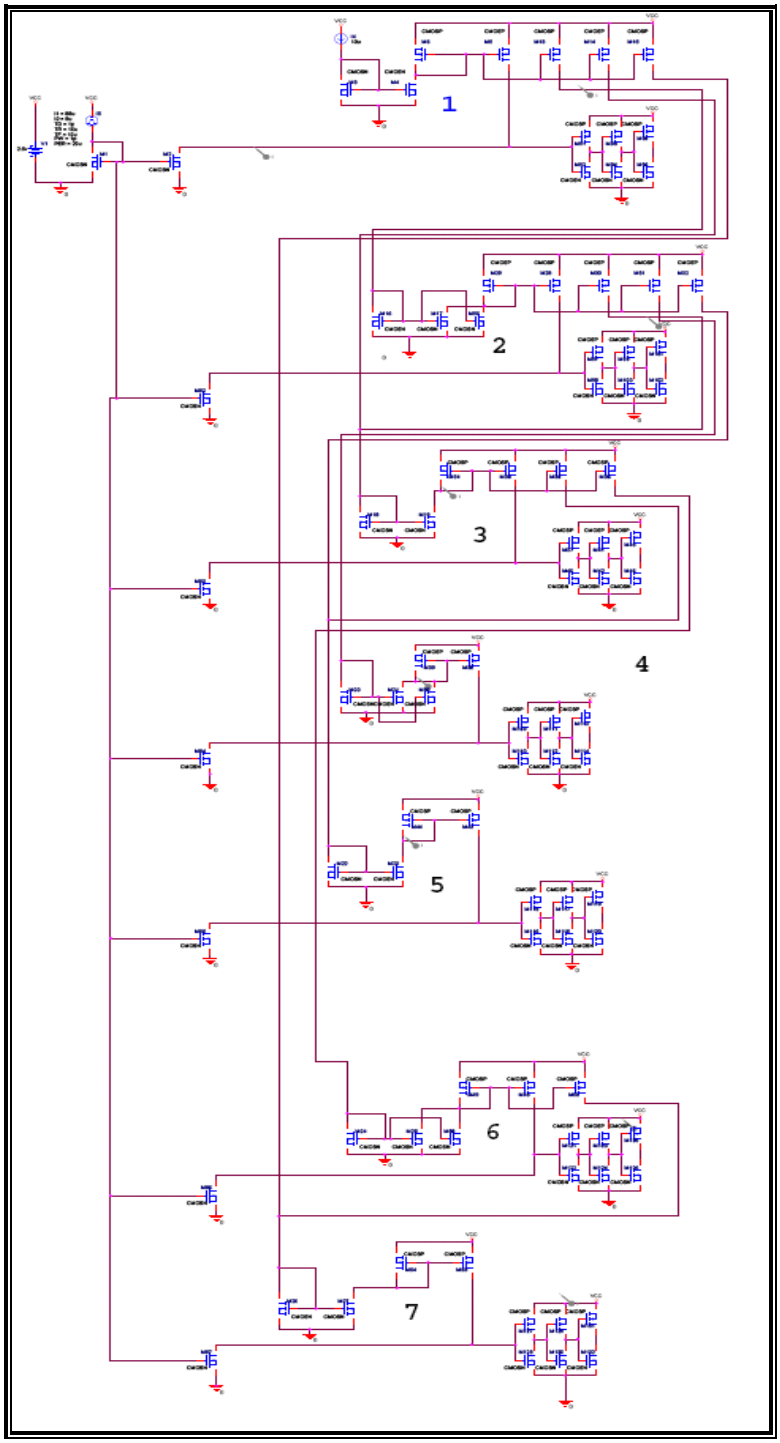

Figure 3.7 Seven level current mode ADC using simple current mirrors

Current mode ADC, designed by basic current mirror has advantages beside of its advantages. Disadvantages of this design are caused because of the used current mirror type. Basic current mirrors have some deficiencies; can be listed as follows:

1. One of the most important deviations from ideality is the variation of the current-mirror output current with changes in voltage at the output terminal. This effect is characterized by the small-signal output resistance R_0, of the current mirror. A Thevenin-equivalent model of the output of the current mirror includes R_0 in parallel with a current source controlled by the input current. The output resistance directly affects the performance of many circuits that use current mirrors. For example, the common-mode rejection ratio of the differential amplifier depends directly on this resistance, as does the gain of the active-load circuits.

Increasing the output resistance reduces the dependence of the output current on the output voltage and is therefore desirable. Generally speaking, the output resistance increases in practical circuits when the output current decreases. Unfortunately, decreasing the output current also decreases the maximum operating speed. Therefore, when comparing the output resistance of two current mirrors.

2. Another important error source is the gain error, which is the deviation of the gain of a current mirror from its ideal value. The gain error is separated into two parts:

-The systematic gain error

-The random gain error.

The systematic gain error, *e*, is the gain error that arises even when all matched elements in the mirror are perfectly matched and will be calculated for each of the current mirrors presented in this section. The random gain error is the gain error caused by unintended mismatches between matched elements.

3. When the input current source is connected to the input terminal of a real current mirror, it creates a positive voltage drop V_{IN}, which reduces the voltage available across the input current source. Minimizing V_{IN} is important because it simplifies the design of the input current source, especially in low-supply applications. To reduce V_{IN} current minors sometimes have more than one input terminal.

4. A positive output voltage, V_{OUT}, is required in practice to make the output current depending mainly on the input current. This characteristic is summarized by the minimum voltage across the output branch. V_{OUT}(min). The output device(s) to operate in the active region is very high. Minimizing Vout(min) maximizes the range of output voltages for which the current-mirror output resistance is almost constant. (Gray&Meyer, 2004)

Because of these deficiencies usage of the simple current mirrors are limited. Finite output resistance of the simple current mirrors is the main limitation regarding to its accuracy in the current mode ADC design. To overcome these deficiencies other current mirrors are developed. This currents mirror's output impedances are much bigger than simple current mirror. So accuracy of the current mode ADC can be increase rapidly. But also by making output impedance, we also lose some dynamic range of the ADC. Because Simple current mirror's dynamic range is better than other current mirrors.

In this work, by using Cascade Current Mirror and Improved Current Mirrors, the improvement of the current mode ADC is observed.

3.3 Current mode ADC based on Current Multiplication Technique using Cascade Current Mirrors

Finite output resistance of the current mirrors is one of the main performance limitation factors on the ADCs. Although MOS transistors have high output resistance, Rout, at saturation mode, but it is not high enough to achieve high accuracy. One way to increase the output resistance is to use cascade structures.

A cascade current mirror is shown in Figure 3.8. The output impedance looking into the drain of Q_2 is simply r_{ds2}, which is seen using an analysis very similar to that which was used for the simple current mirror. Thus, the output impedance can immediately be derived by considering Q_4 as a current source with a source-

degeneration resistor of value r_{ds2}. Making use of Equation 3.6 and noting that Q_4 is now the cascade transistor rather than Q_2, we have

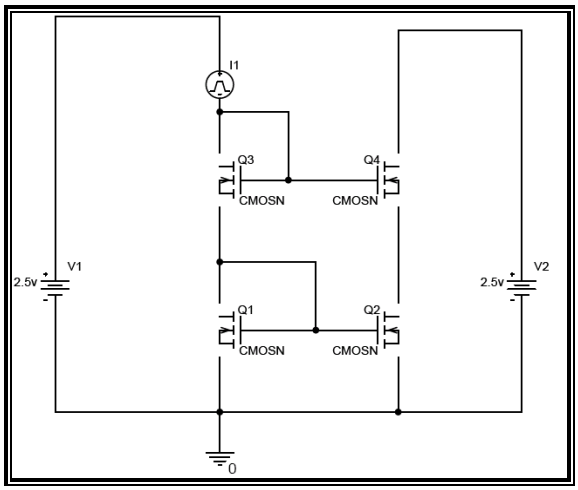

Figure 3.8 a cascade current mirror

$$r_{out} = r_{ds4}[1 + R_s(g_{m4} + g_{s4} + g_{ds4})] \tag{3.6}$$

Where now $R_s = r_{ds2}$. Therefore, the output impedance is given by

$$\begin{aligned} r_{out} &= r_{ds4}[1 + r_{ds2}(g_{m4} + g_{s4} + g_{ds4})] \\ &\cong r_{ds4}[1 + r_{ds2}(g_{m4} + g_{s4})] \\ &\cong r_{ds4}(r_{ds2}g_{m4}) \end{aligned} \tag{3.7}$$

Thus, the output impedance has been increased by a factor of $g_{m4}r_{ds2}$, which is an upper limit on the gain of a single-transistor MOS gain-stage, and might be a value between 10 and 100, depending on the transistor sizes and currents and the technology being used. This significant increase in output impedance can be instrumental in realizing single-stage amplifiers with large low-frequency gains.

There is a disadvantage in using a cascade current mirror; it reduces the maximum output-signal swings before transistors enter the triode region. (Johns&Martin, 1997)

According to above calculations the output impendence of the current mirrors can be improved. By changing the current mirrors in the ADC design, it is desired to develop the accuracy. In the previous design only simple current mirrors were used, so the performance is limited by the capabilities of simple current mirrors. The design of the cascade ADC design is similar to simple current mirrors. All the simple current mirrors are changed to the cascade current mirrors. Here is the one cell of the cascade current mirror.

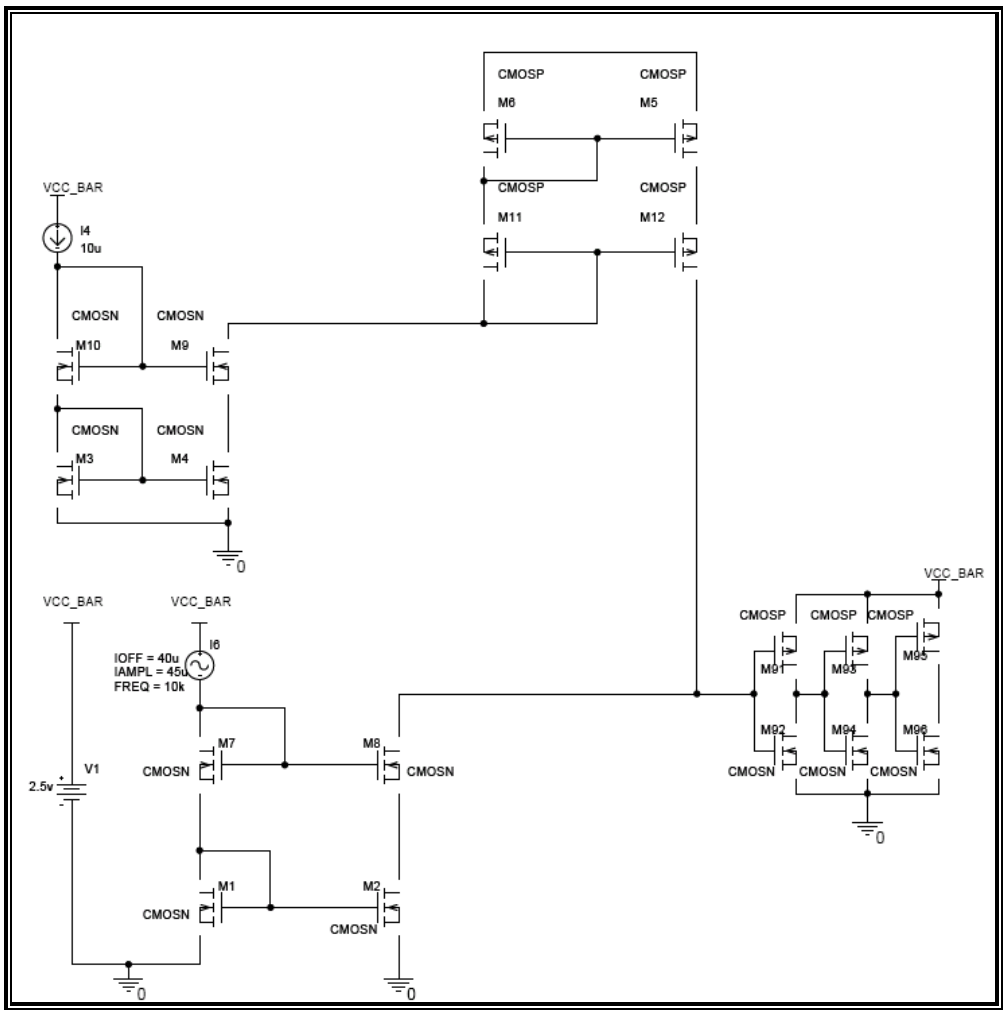

Figure 3.9 a cell of the multiplying ADC using cascade current mirrors.

Figure3.9 shows the first bit cell of the multiplying converter by using cascade current mirrors. I_{Ref} is mirrored by an *n*-mirror (M_1,M_2,M_7,M_8) which is also designed by using cascade current mirrors to isolate the converter from the outside world. To transform the current sink into a current source, the current gets mirrored

again but this time a *p*-mirror (M_5, M_6, M_{11}, M_{12}) is used. Neglecting the current mirror error, due to device variances caused by production tolerances, the current should still have the exact same value as the reference current had before it was mirrored twice.

The other input to the cell, I_{In}, also passes trough an N-mirror (M_1, M_2, M_7, M_8) first, transforming it into a current sink. It has the same value as I_{In} had, but the sign changes. This node is connected to the drain of the p-type (M_5, M_6, M_{11}, M_{12}) transistor of the mirror which provides the isolated I_{Ref} in the form of a current source. In addition, the input of a CMOS current comparator is connected to this node as well. It is supposed to switch from low to high when the input current (the current sink) becomes bigger than the reference current (the current source). It inverts the signal after the second stage a third time, so that the comparator output switches when the absolute value (I_{In}) of the current sink becomes bigger than the absolute value (I_{Ref}) of the current source.

Figure3.10 shows the whole circuitry which will be use for cascade multiplying ADC design it is composed of seven cells from Figure 3.9. Since every stage of the comparator requires its own copy of I_{In}, it has to be copied seven levels and has to be copied eight levels times for eight level designs. For observation we also improved to design to eight levels. The copies are obtained by connecting the gates of n-MOS transistors to the node which drives the gate of the second transistor in the n-mirror for I_{In}. They form the I_{In} input network which can be identified on the left hand side of the schematic in Figure3.10. Since they are all part of an n-type current mirror, their drains are in a second connection line connected to the ground node. The source of each I_{In} copy transistor directly connects to the comparator input of the corresponding bit cell.

For the input of the second bit cell, I_{Ref} times two is required. It is obtained by taking a copy of I_{Ref} from the first cell and then doubling it in the n-mirror of bit cell number two. The current doubles because the gates of two transistors of the same dimensions are connected in parallel. For the input of bit cell number three, I_{Ref} times three is required. Since two can not be divided by three, doubling again does not

work. But, according to Kirchhoff's current law, making one copy of 2 * I_{Ref} and one copy of I_{Ref} itself and adding them together results in 3 * I_{Ref}. Four times I_{Ref} can be obtained by making a copy of 2 * I_{Ref} and doubling it as done in bit cell number two. Five times I_{Ref} can be obtained by making one copy of 2 * I_{ref} and one copy of 3 * I_{Ref} and adding them together. Six times I_{Ref} again is obtained by doubling a copy of 3 * I_{Ref} as done before in the case of bit cell number two and four. Seven times I_{Ref} is obtained by adding a copy of 6 * I_{Ref} to a copy of I_{Re}f. And finally eight times I_{Ref} is obtained by adding a copy of 7 * I_{Ref} to a copy of I_{Ref}. The last stage is added with our new design.

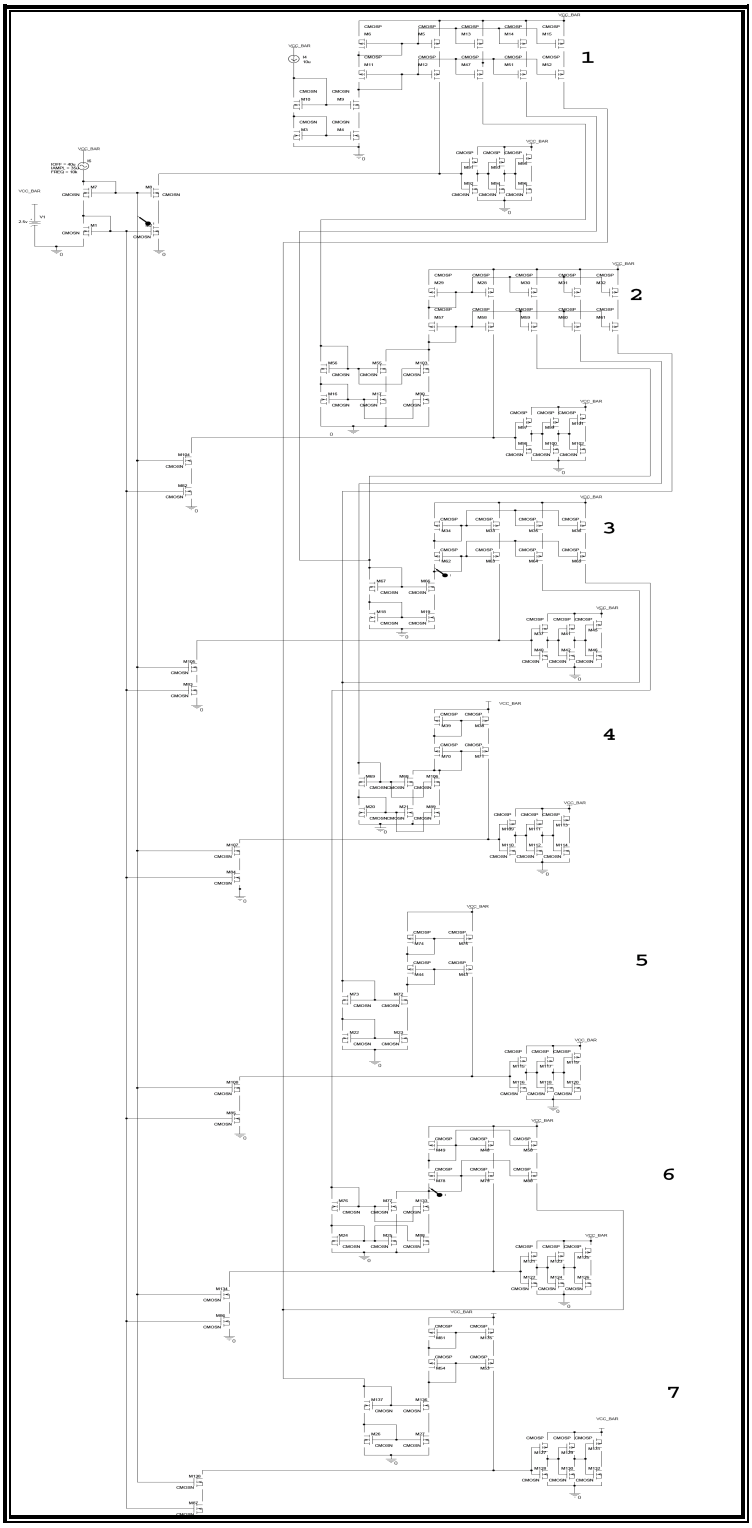

Figure 3.10 seven level ADC which cascade current mirrors are used

Figure3.10 is made by cascade current mirrors and there are 7 levels. In order to see the effect of using cascade current mirrors, one level is added to this design. (Figure 3.11)

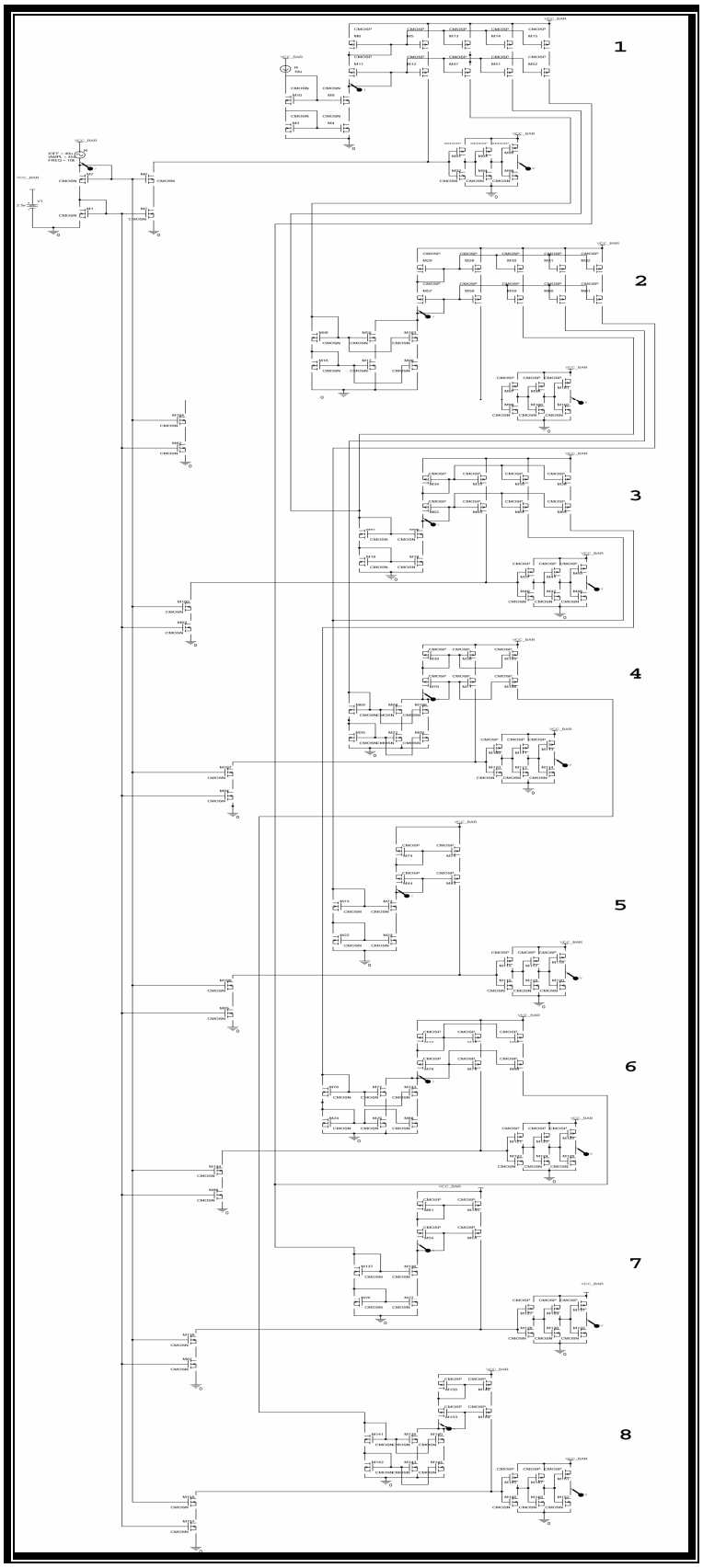

Figure 3.11 8- level ADC which cascade current mirrors are used

3.4 Current mode ADC based on Current Multiplication Technique Improved Wilson Current mirrors

One way of to improve current mirror output resistance is to use improved Wilson current mirrors. Improved Wilson current mirror (figure 3.12) is an example of using shunt-series feedback to increase the output impedance (Sedra, 1991). Basically, Q_2 senses the output current and then mirrors it to $I_{4,}$ which, in turn, is subtracted from the input current. $I_{in.}$ Note that I_{in} must precisely equal I_{in}; otherwise the voltage at the gate of Q_3, Q_4 would either increase or decrease, and the negative feedback loop forces this equality. This feedback arrangement increases the output impedance by an amount equal to 1 plus the loop gain. Assuming all devices are matched, the output impedance without the feedback due to Q_1, Q_3 would be $2r_{ds4}$; taking into account that Q_4 has source degeneration equal tol/g_{m2} which is responsible for the 2 factor. The loop gain is approximately given by

$$A_L \cong \frac{g_{m1}(r_{ds1} \parallel r_{in})}{2} \tag{3.7}$$

Where r_{in} is input impedance of biasing current source, I_{in}. The factor of 1/2 is due to the voltage attenuation from the gate of Q_4 to its source, caused by the source degeneration of the diode-connected G_2. Assuming r_{jn} is approximately equal to $r_{ds1.}$

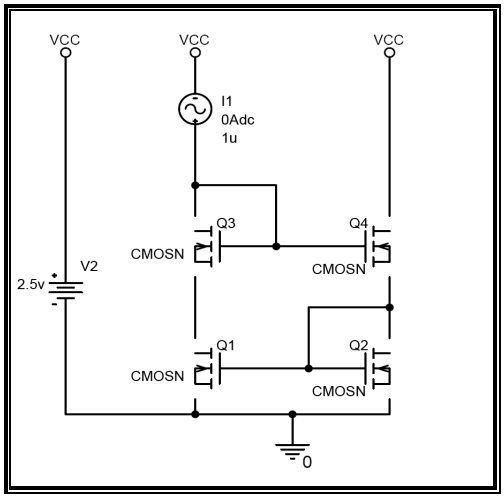

Figure 3.12 improved Wilson current mirror

Then the loop gain is

$$A_L \cong \frac{g_{m1} r_{ds1}}{4} \tag{3.8}$$

And the output impedance is therefore given by

$$r_{out} \cong 2r_{ds4} \frac{g_{m1}(r_{ds1} \parallel r_{in})}{2} \cong r_{ds4}\left(\frac{g_{m1} r_{ds1}}{2}\right) \tag{3.9}$$

which is roughly one-half the output impedance for that of a cascade current mirror. For this reason, the cascade current mirror is often preferred over the Wilson current mirror. In terms of output voltage swing, the minimum allowed voltage across the current mirror, before Q_4 enters the triode region, is $2V_{eff} + V_{in}$, which is similar to the of the cascade current mirror.

The principle of the ADC which improved Wilson current mirrors is used, is very similar with cascade current mirror.

Figure 3.12 shows the first bit cell of the multiplying converter by using improved Wilson current mirrors. I_{Ref} is mirrored by an *n*-mirror (M_1, M_2, M_7, M_8) which is also designed by using improved Wilson current mirrors to isolate the converter from the outside world. To transform the current sink into a current source, the current gets mirrored again but this time a *p*-mirror (M_5, M_6, M_{11}, M_{12}) is used. Neglecting the current mirror error, due to device variances caused by production tolerances, the current should still have the exact same value as the reference current had before it was mirrored twice. But with this design for I_{in} ,improved Wilson current mirror can not be used. Improved Wilson current mirrors are used in I_{ref} and changing I_{ref} current sink to source.

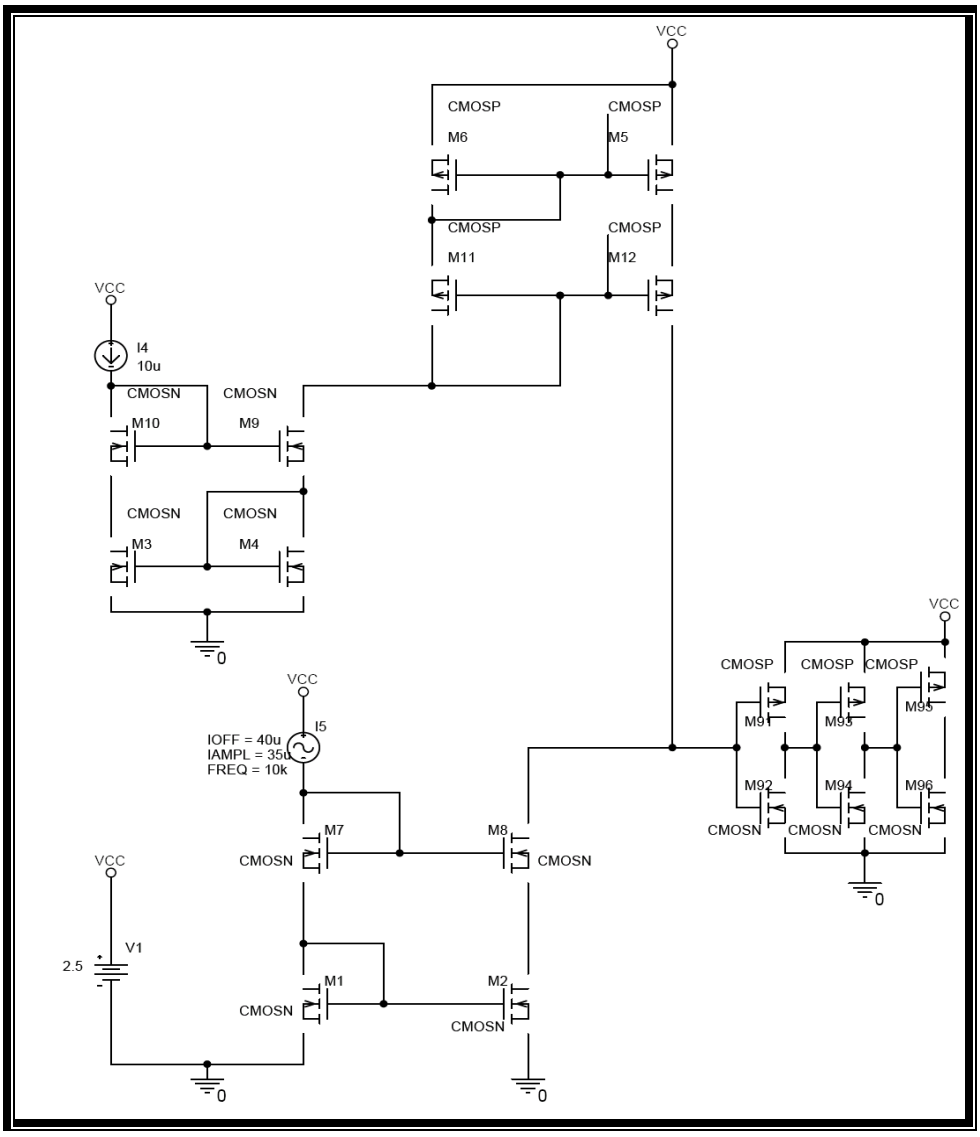

Figure 3.13 one cell of the multiplying converter by using improved Wilson current mirror

The other input to the cell, I_{In}, also passes trough an N-mirror (M_1,M_2,M_7,M_8) first, transforming it into a current sink. It has the same value as I_{In} had, but the sign changes. This node is connected to the drain of the p-type (M_5,M_6,M_{11},M_{12}) transistor of the mirror which provides the isolated I_{Ref} in the form of a current source. In addition, the input of a CMOS current comparator is connected to this node as well. It is supposed to switch from low to high when the input current (the current sink) becomes bigger than the reference current (the current source). It inverts the signal after the second stage a third time, so that the comparator output switches when the absolute value (I_{In}) of the current sink becomes bigger than the absolute value (I_{Ref}) of the current source.

Figure 3.14 shows the whole circuitry which will be use for improved Wilson current mirror ADC design It is composed of seven cells from Figure 3.14. Since every stage of the comparator requires its own copy of I_{In}, it has to be copied seven levels and has to be copied eight times for eight level design. For observation eight level design developed and simulated (figure 3.15). The copies are obtained by connecting the gates of n-MOS transistors to the node which drives the gate of the second transistor in the n-mirror for I_{in}. They form the I_{in} input network which can be identified on the left hand side of the schematic in Figure 3.14. Since they are all part of an n-type current mirror, their drains are in a second connection line connected to the ground node. The source of each I_{In} copy transistor directly connects to the comparator input of the corresponding bit cell.

For the input of the second bit cell, I_{Ref} times two is required. It is obtained by taking a copy of I_{Ref} from the first cell and then doubling it in the n-mirror of bit cell number two. The current doubles because the gates of two transistors of the same dimensions are connected in parallel. For the input of bit cell number three, I_{Ref} times three is required. Since two can not be divided by three, doubling again does not work. But, according to Kirchhoff's current law, making one copy of 2 * I_{Ref} and one copy of I_{Ref} itself and adding them together results in 3 * I_{Ref}. Four times I_{Ref} can be obtained by making a copy of 2 * I_{Ref} and doubling it as done in bit cell number two. Five times I_{Ref} can be obtained by making one copy of 2 * I_{ref} and one copy of 3 * I_{Ref} and adding them together. Six times I_{Ref} again is obtained by doubling a copy of 3 * I_{Ref} as done before in the case of bit cell number two and four. Seven times I_{Ref} is obtained by adding a copy of 6 * I_{Ref} to a copy of I_{Ref}. And finally eight times I_{Ref} is obtained by adding a copy of 7 * IR_{ef} to a copy of I_{Ref}. The last stage is added with our new design. This structure is similar with cascade design, only the difference is; used current mirrors.

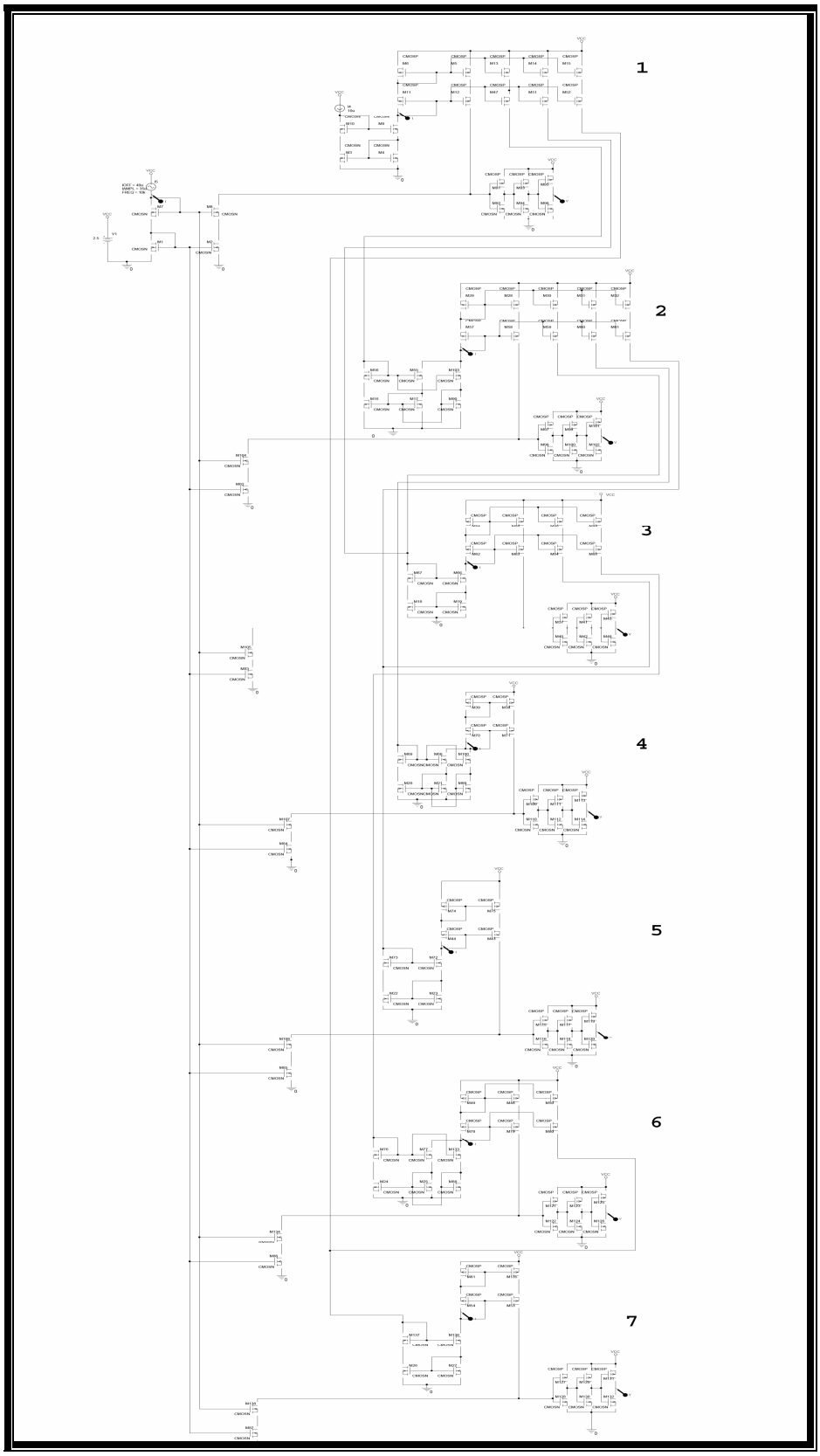

Figure 3.14 7-level ADC using improved Wilson current mirrors

Like cascade structure, 8-level ADC design is also developed with improved Wilson current mirrors.

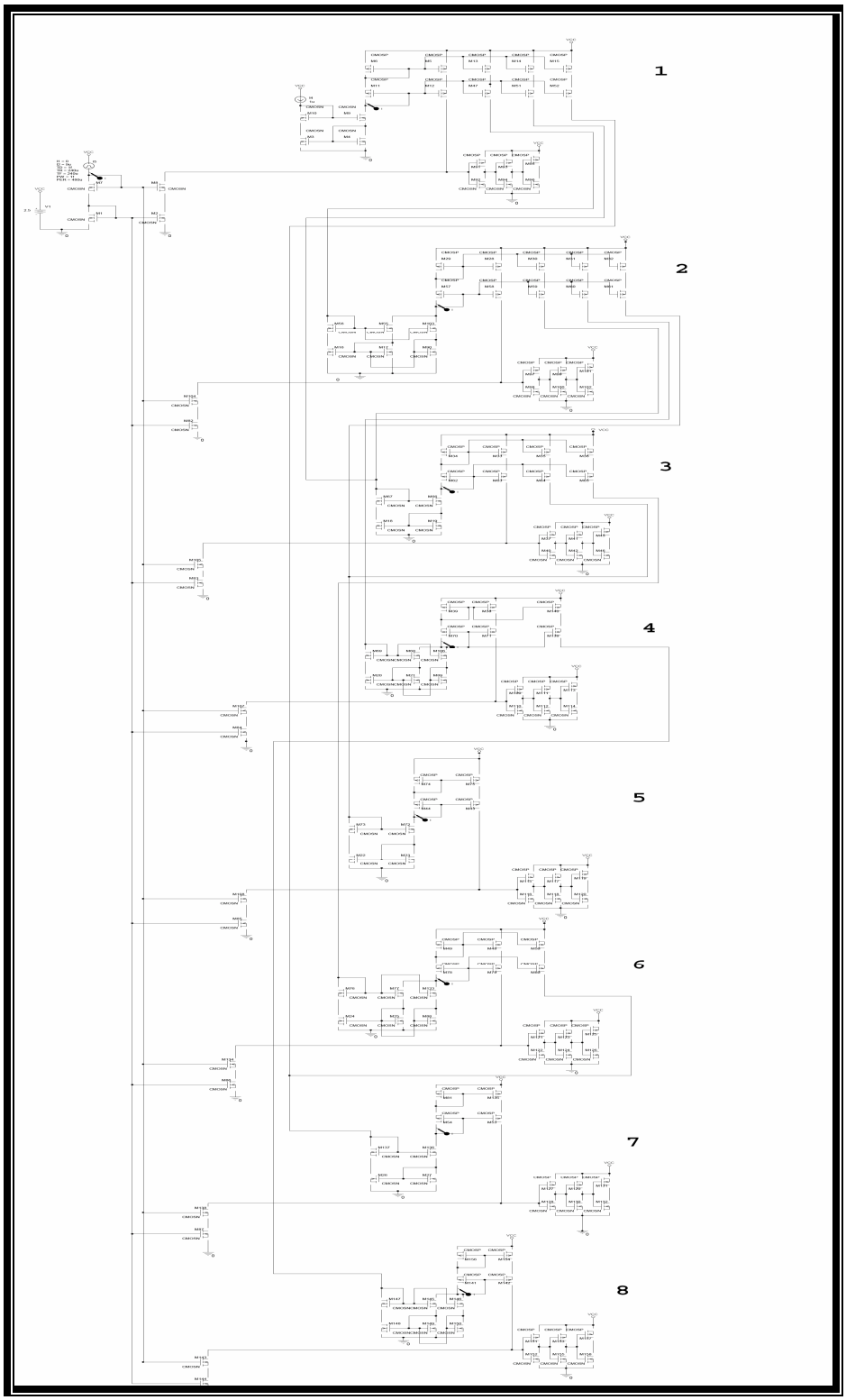

Figure 3.15 8-level ADC using improved Wilson current mirrors

CHAPTER FOUR
CURRENT-MODE ADC BASED ON CURRENT DIVISION

Unlike current multiplication technique, this technique is based on to divide the reference current into specified values. This technique is first used by G.Rachmuth and improved by H.Helble. In this work; the current mirror types are changed, and observed. Similar to current multiplication based approach, this A/D converter must also be capable of operating at low voltages whilst having a resolution in the single micro amperes range. Another requirement is to have seven bits thermometer code as output of the converter cell.

Main characteristic of the system is its operation in subthreshold domain. For this reason, the analog-to-digital converter used within the system has to operate in subthreshold regime. A problem with subthreshold circuits is that systems operating in this mode are both low power and slow. Consequently, the need for a subthreshold current mode A/D converter is due to the specifications which need energy efficiency. However, the most important drawback of using system in subthreshold region is being slower than other solutions.

4.1 Principle of Operation

The idea behind this converter is to divide a reference current by a number of different divisors to obtain a linear increasing set of currents to which the input current can be compared. While I_{Ref} represents the full scale input of the converter, the LSB is, in this case, is always 1/7 * I_{Ref}. This brings us back to the principle of operation of the voltage mode flash converter, where a chain of equal resistors divides a reference voltage into N voltages which increase by the value of the LSB from stage to stage. The design is also about a flash architecture, in which a copy of the current which we want to convert is fed directly to a comparator. Therefore, for each bit of the thermometer code a separate comparator is required. (Helbe, 2004)

Improvements over its on multiplication based competitor are primarily expected with regard to its operation speed and linearity. In contrast to the multiplication technique, current division can be accomplished using Ohm's law. To do so, the reference current simply has to be copied several times with current mirrors and then split up again into fractions by using current mirrors. The algorithm which follows this principle looks like this for bit one to bit seven: (Helbe, 2004)

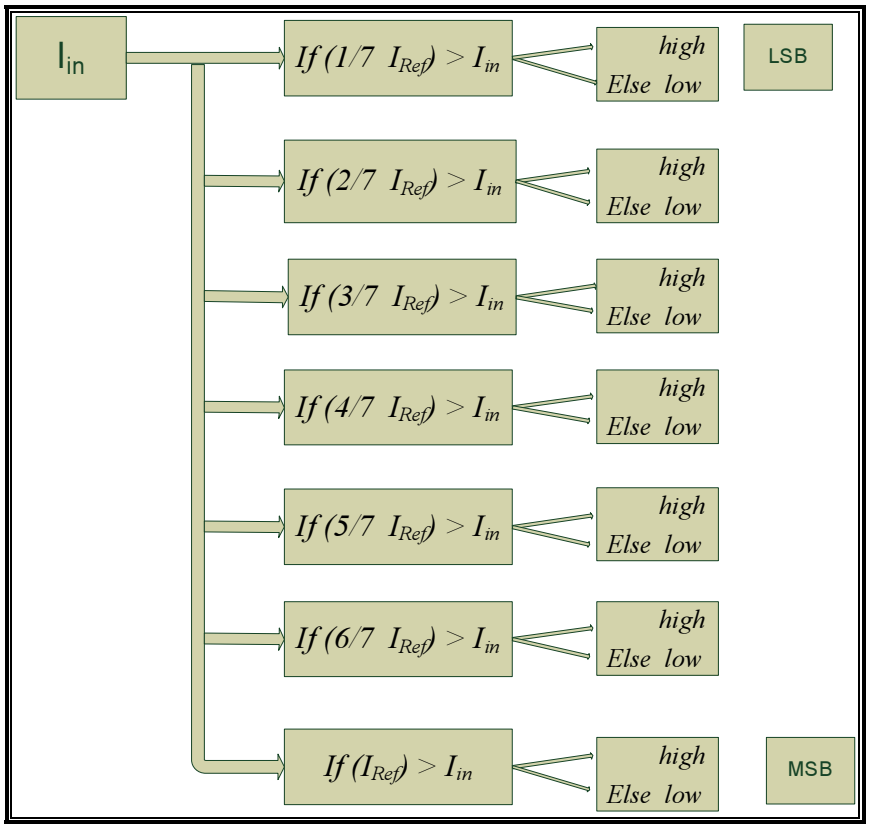

Figure 4.1 Principle of Current division technique

These levels are calculated according to seven level design, previous design is extended and added one level more so the total level become eight. So each level became 1/8 of the reference current.

4.2 Current mode ADC based on Current Division Technique using simple current mirrors

Current division ADC is made up of three n-mirrors, two p-mirrors and one comparator. I_{Ref} is mirrored by an n-mirror first, followed by a p-mirror. Thus its value is unchanged at this point and can be compared directly to the reference current to determine the logical state of bit seven. When I_{In} is raised from zero to full scale, one bit after another will go from low to high. If a comparator with three inverters had been used, their logic values would have changed from high to low for the same simulation. (Helbe, 2004)

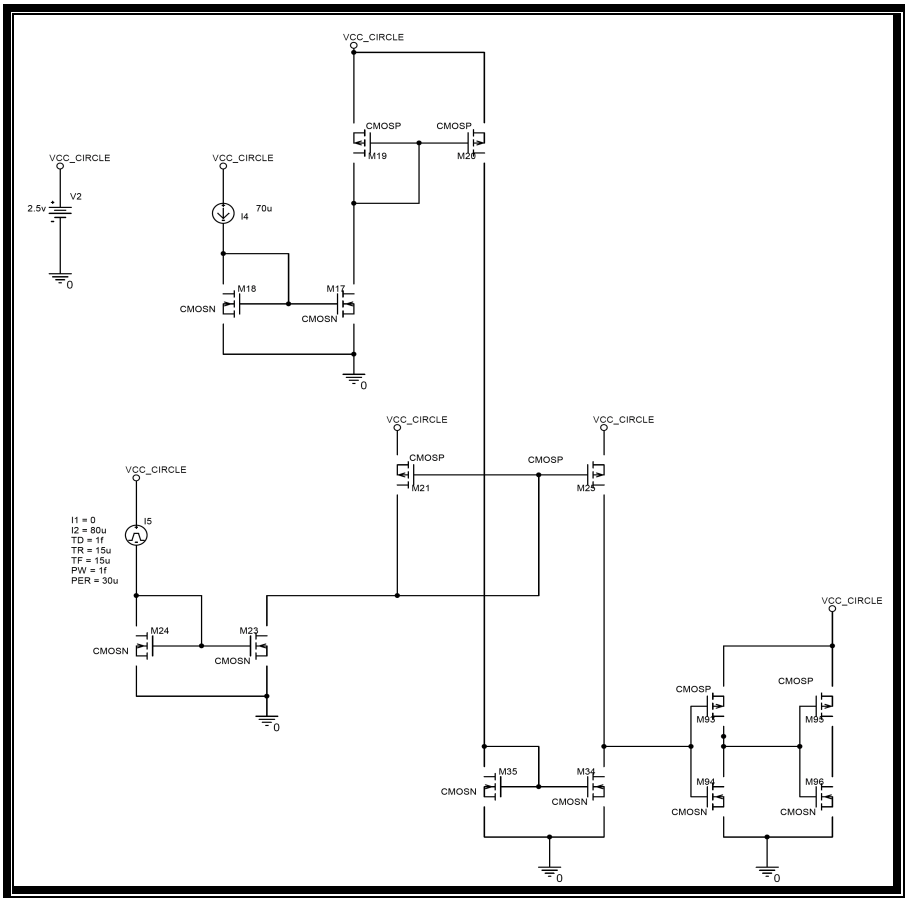

Figure 4.2 single bit cell of current division ADC using simple current mirrors

The design as a whole, as shown in Figure 4.3(bigger size of this drawing is given in appendix), performs a series of static current divisions to generate seven different current levels to which the input current can be compared to. This can be explained using the I_{In} current copy chain which is made up of one n- and one p-mirror. The p-mirror has seven transistors connected in parallel, so that it provides seven identical copies of the input current in the form of a current source. Each current source is connected to a separate comparator.

The division of I_{Ref} is slightly more complicated. Consider a copy of $I_{Ref,}$ as seen in the single bit cell in Figure 4.1; this current is then split into seven equal parts by connecting it to seven parallel connected n-mirrors, functioning as current sinks. Assuming that these seven parallel n-mirrors all have exactly the same electrical properties, the current will inevitably spilt up into seven identical portions, following Kirchhoff's current law. For bit number one (the LSB), it is sufficient to compare this current directly to I_{Ref}. For the second bit, two of the LSB currents have to be added together and then be compared to I_{Ref}. Same rules apply to the currents which are formed to determine the logical state of bit three, four, five and six. For the seventh bit, I_{In} is directly compared to $IR_{ef.}$ This comes from the fact that seven LSB currents added together sum up to $I_{Ref.}$ Due to the fact that it is more accurate, size, and power efficient to use just one n-mirror instead adding together the current output of seven of them, this appears to be the best solution. (Helbe, 2004)

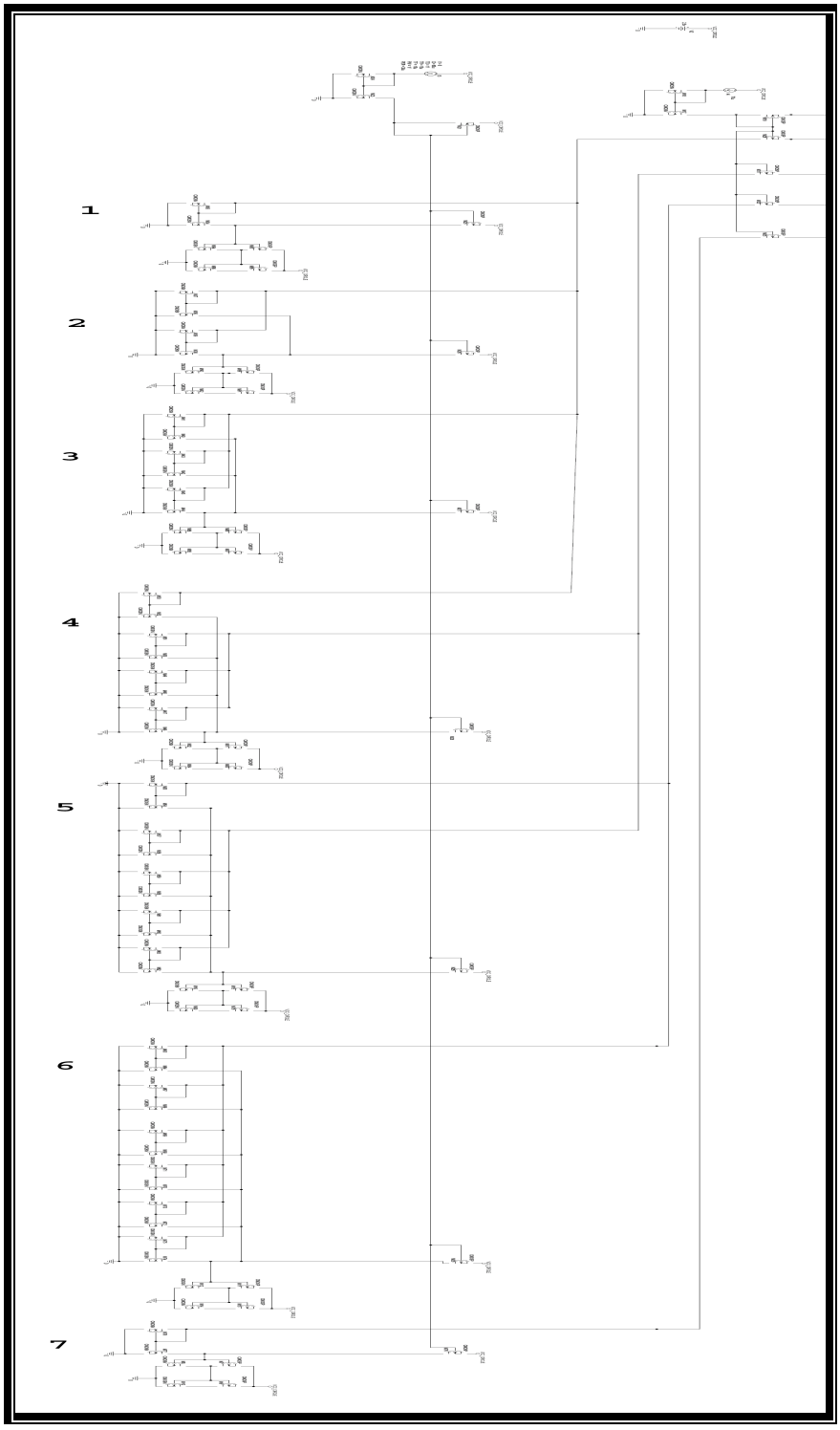

Figure 4.3 7-level ADC based on current division technique using simple current mirrors

As it was made with current multiplication technique, the design was extended and one more level is added to see the differences. In the eight level designs, eight current levels were supposed to **divide current to eight levels.** (In appendix there is bigger size of this drawing)

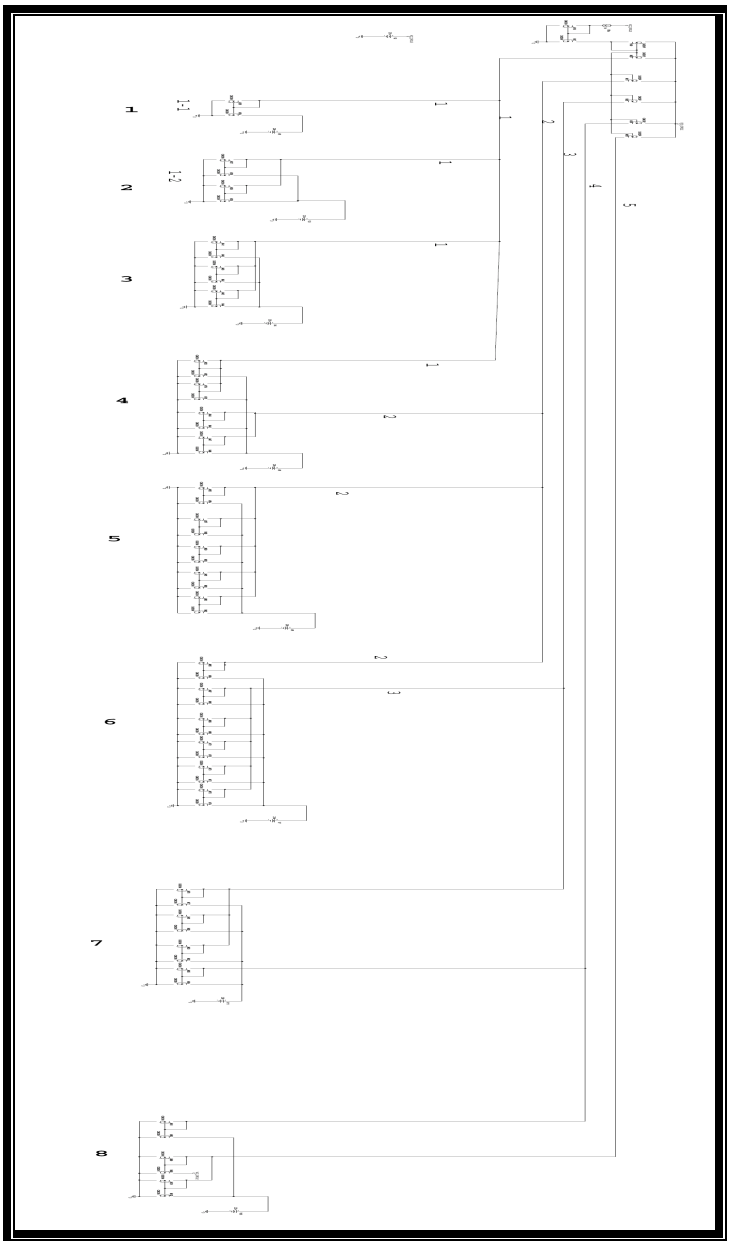

Figure 4.4 8-level ADC based on current division technique using simple current mirrors

4.3 Current mode ADC based on Current Division Technique using simple Cascade Current Mirrors

As it was mentioned in the previous chapter, finite output resistance of the current mirrors is one of the main performance limitation factors on the ADCs. Although MOS transistors have high output resistance, R_{out}, at saturation mode, but it is not high enough to achieve high accuracy. One way to increase the output resistance is to use cascade structures. Like it was done with current multiplication technique, simple current mirrors are changed to the cascade current mirrors in simple current mirror design.

As impedance of the cascade current mirrors are calculated in the previous chapter; output impedance is much higher than the simple current mirrors. One cell of the cascade ADC is shown figure 4.5.

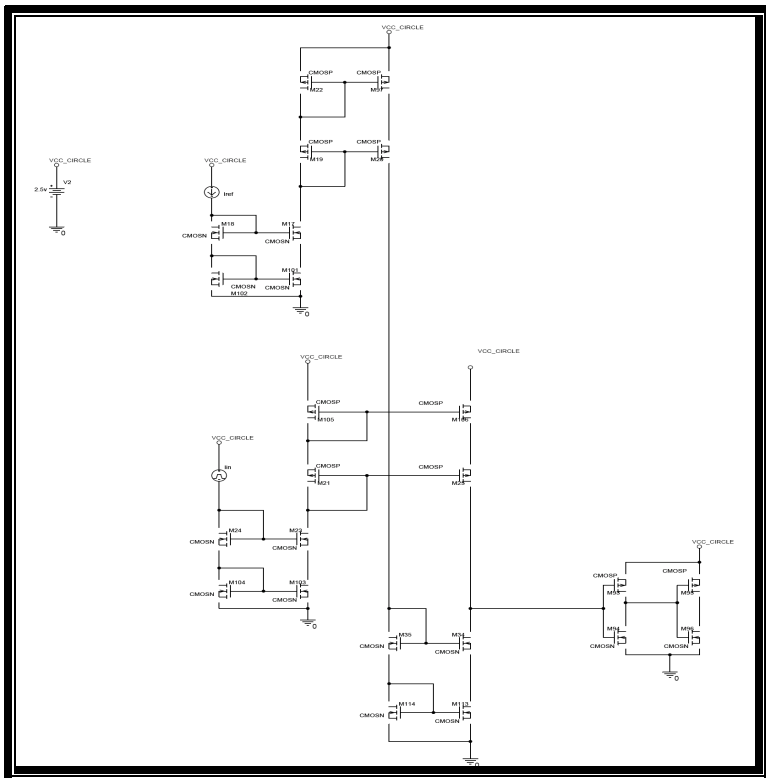

Figure 4.5 single bit cell of current division ADC using cascade current mirrors

Current division ADC is made up of three n-mirrors, two p-mirrors and one comparator. I_{Ref} is mirrored by an n-mirror first, followed by a p-mirror. But here, unlike the previous section all current mirrors are cascade topology. These currents can be compared directly to the reference current to determine the logical state of bit seven. When I_{In} is raised from zero to full scale, one bit after another will go from low to high.

Whole circuit used in this work is shown in figure 4.6 (In appendix there is bigger size of this drawing) for 7-level design.

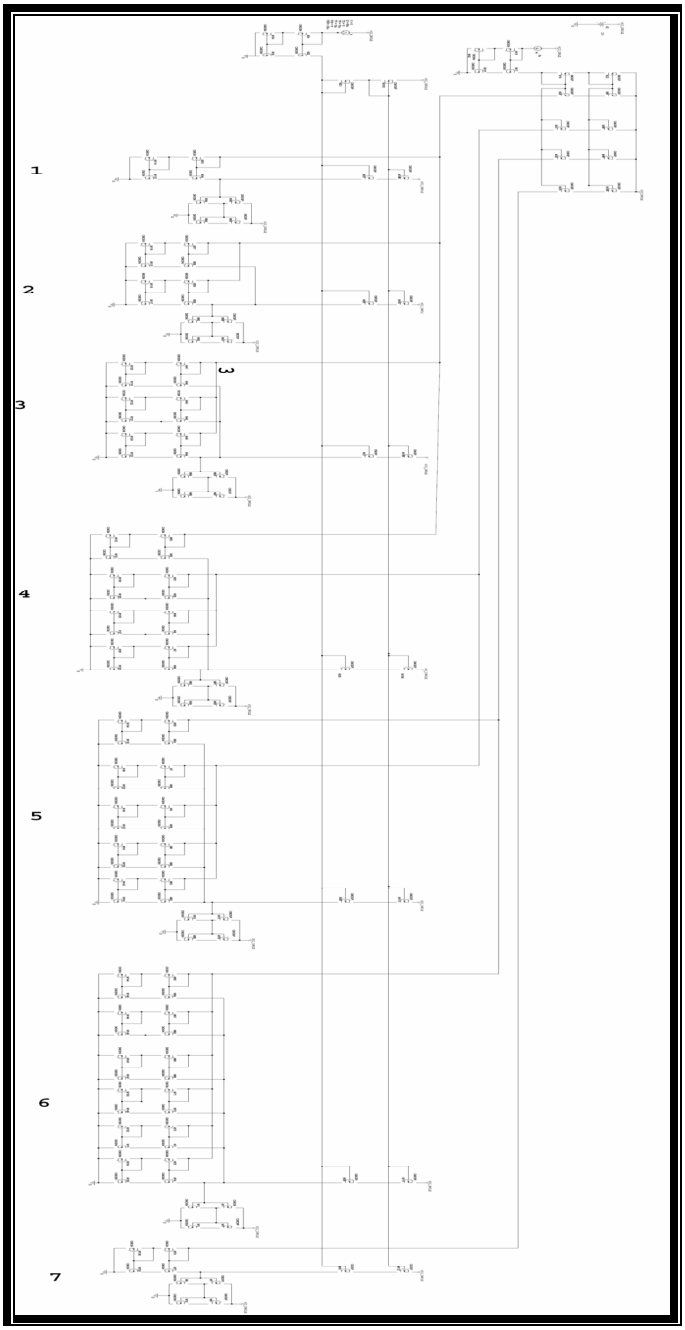

Figure 4.6 7-level ADC based on current division technique using cascade current mirrors

The design which is used for 8-level ADC is shown figure 4.7. (In appendix there is bigger size of this drawing)

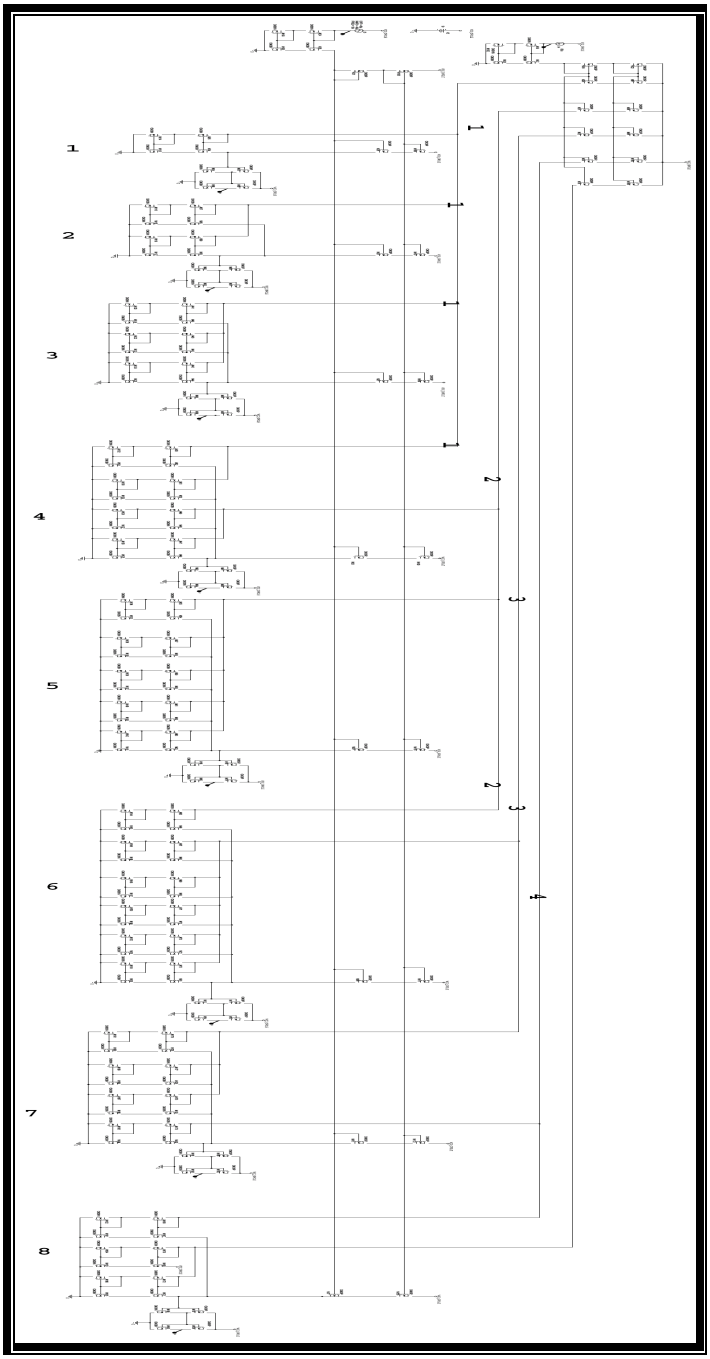

Figure 4.7 8-level ADC based on current division technique using cascade current mirrors

4.4 Current mode ADC based on Current Division Technique using simple Improved Wilson Current Mirrors

One way of to improve the output impedance is to use improved Wilson current mirrors. Improving the output impedance of the current mirror, dynamic range is decreasing.

As impedance of the Improved Wilson current mirrors are calculated previous chapter; output impedance is much more bigly than the simple current mirrors. One cell of the Improved Wilson ADC is shown figure 4.8. (In appendix there is bigger size of this drawing)

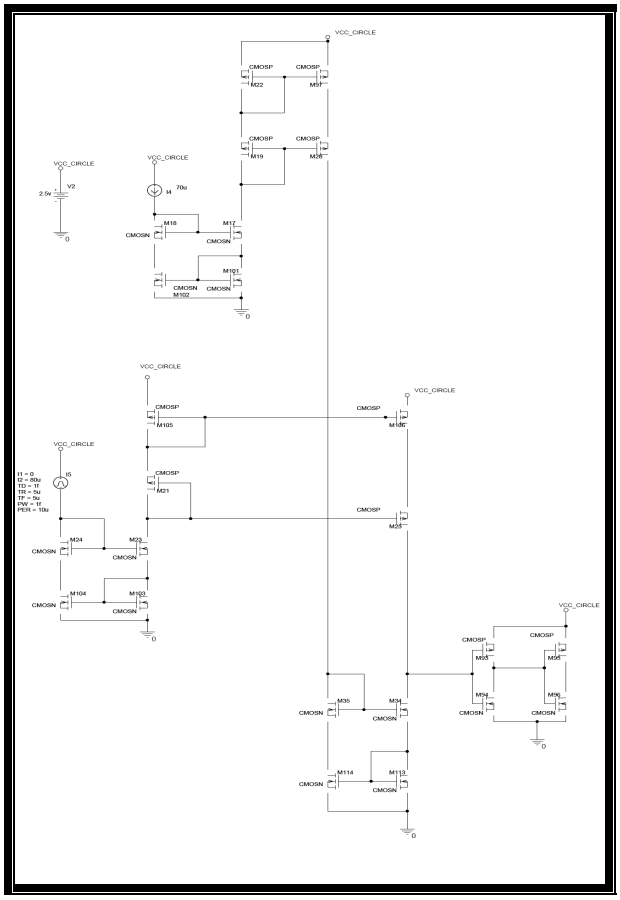

Figure 4.8 single bit cell of current division ADC using Improved Wilson current mirrors

Current division ADC is made up of three n-mirrors, two p-mirrors and one comparator. I_{Ref} is mirrored by an n-mirror first, followed by a p-mirror. But here despite of the previous section all current mirrors are Improved Wilson topology. These currents can be compared directly to the reference current to determine the logical state of bit seven. When I_{In} is raised from zero to full scale, one bit after another will go from low to high.

Whole circuit used in this work is shown in appendix for seven level and eight level designs.

CHAPTER FIVE
RESULTS OF SIMULATIONS

In previous chapters, analog to digital converters are introduced. In this chapter the test results of these Converters are shown. All tests are simulated by using OrCAD 10.5, and the transistor models are got from MOSIS library. Transistor models used in simulations are attached in the appendix

In the result section, 7-level analog to digital converter results are shown at first and than 8-level converter results are given.

5.1 7-Level A/D Converters based on Current Multiplication Technique

7-level analog to digital Converters based on current multiplication technique was firstly made by H. Helble in 2004 by using basic current mirrors. Firstly this reference design is simulated, after that design; our new design which Cascade current mirrors and improved Wilson current mirror used analog to digital Converters are simulated.

5.1.1 Basic Current Mirror used 7-Level A/D Converters based on Current Multiplication Technique

7-level design which was introduced in section 3.2 by H. Heble is simulated in this section. In this design, basic current mirrors are used as a current mirror. The dynamic range of the simple current mirrors are good but being relatively low output impendence to Cascade and improved Wilson current mirrors; the accuracy of the simple current mirror is low.

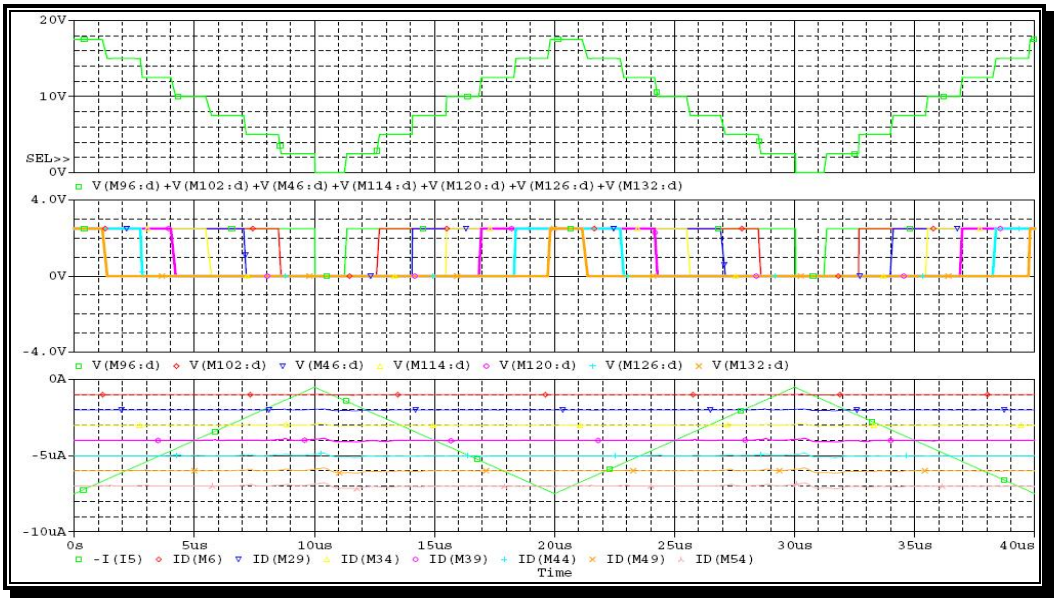

Figure 5.1 Simple current mirror used converter output

In Figure 5.1 the output of the simple current mirror used converter is shown. Here the reference level of the converter is 1µA and this reference current multiplied up to seven in each level and compared with the saw tooth input. Frequency of the input signal is 100 kHz. The output of the comparator is shown at the top of Figure5.1.

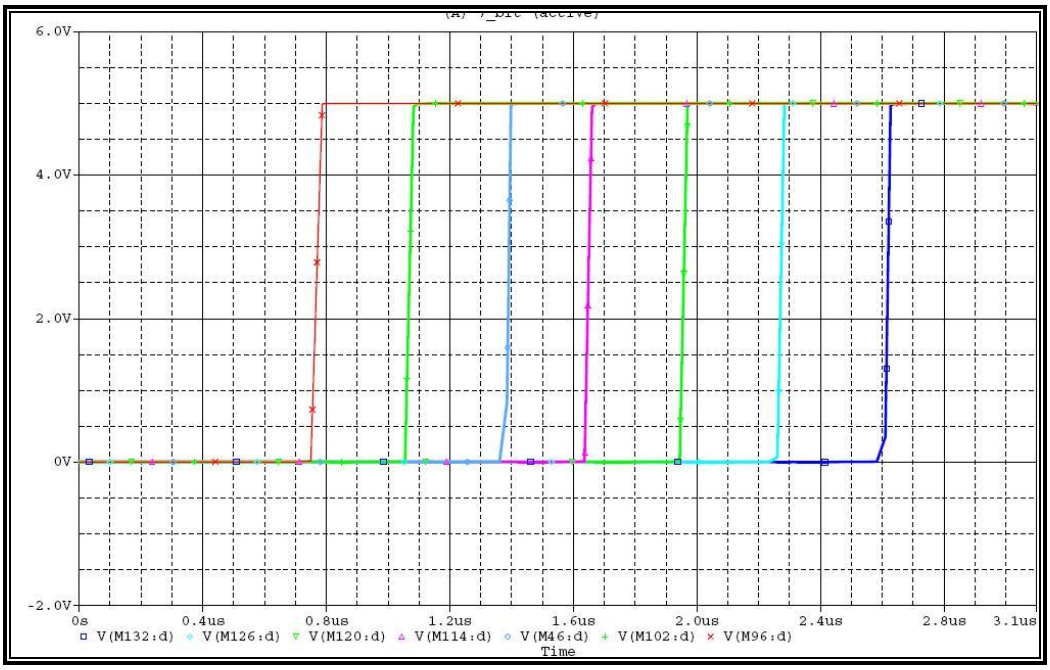

Figure 5.2 Transitions from low to high for Simple current mirror used converter

In Figure 5.2 the bits from one to seven is shown. Bits are switched from low to high. The linearity of the system can be seen by looking at the distance at which the switching takes place. But also the DNL and INL of the system are calculated in the last section. But the linearity of the system looks good by looking of the distance.

The sequence of the output levels are shown in Figure5.3 which gives output for the saw tooth input at 100 kHz.

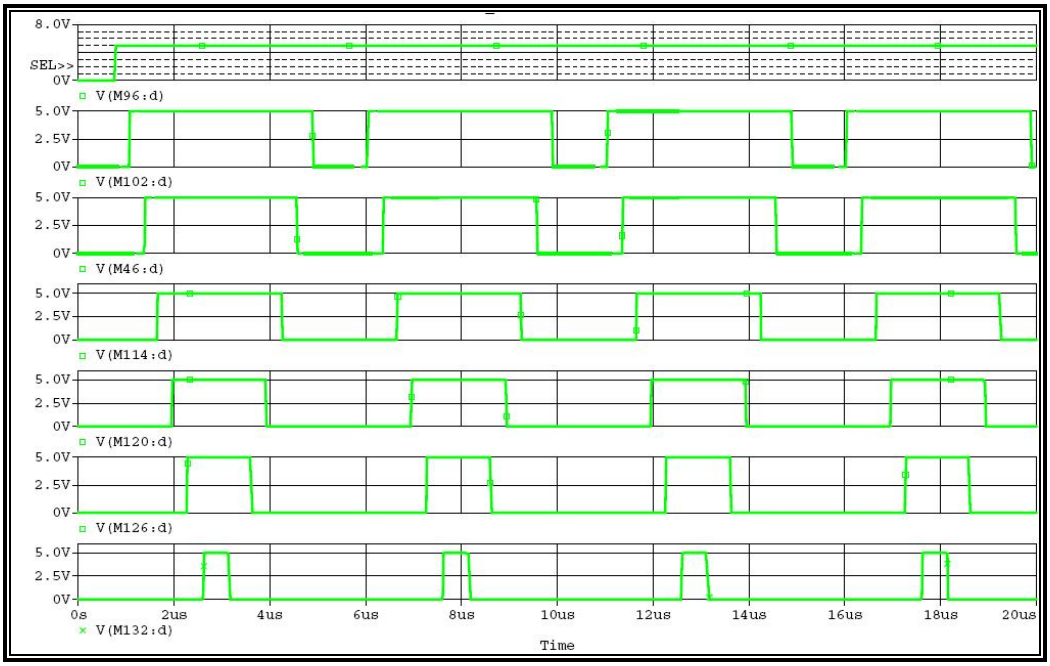

Figure 5.3 Output of simple current mirror used ADC

5.1.2 Cascade Current Mirror used 7-Level A/D Converters based on Current Multiplication Technique

In this section, cascade current mirrors used 7-level analog to digital converters are simulated. Dynamic ranges of the cascade current mirrors are relatively low than simple current mirrors as explained in section 3.2. But the output resistances of the cascade current mirrors are better than simple. The theory is introduced in section 3.3. Here is the result of our design in which cascade current mirrors are used.

In the test conditions; the reference current and frequency are changed and the converters are tested.

In Figure5.4 output of the converter, reference currents and input saw tooth current are shown. Here the input current's max value is 9µA and the min value is 0 µA. Reference current is 1µA. Being multiplied seven here we have seven level for comparison to input current. Because of the switching there are some oscillations on the reference current. These oscillations also related about the parasitic capacitance of the MOS transistors. Here the frequency is 500 kHz.

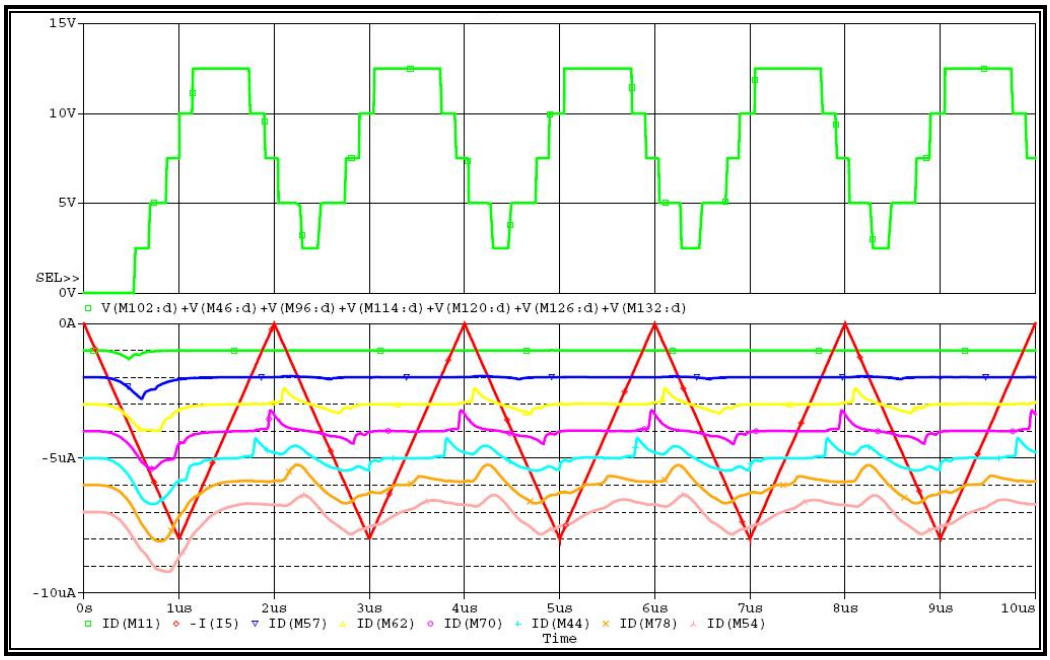

Figure 5.4 Output of cascade mirror used ADC for 500 kHz saw tooth input

In Figure 5.5, the reference frequency is changed to 200 kHz but the signal amplitudes kept constant. Here is the result is similar to the previous result. Because of the parasitic capacitance and the oscillations there are some missing bits at the output of the converter. At high frequencies and low current levels some missing codes are observed with this analog to digital converters.

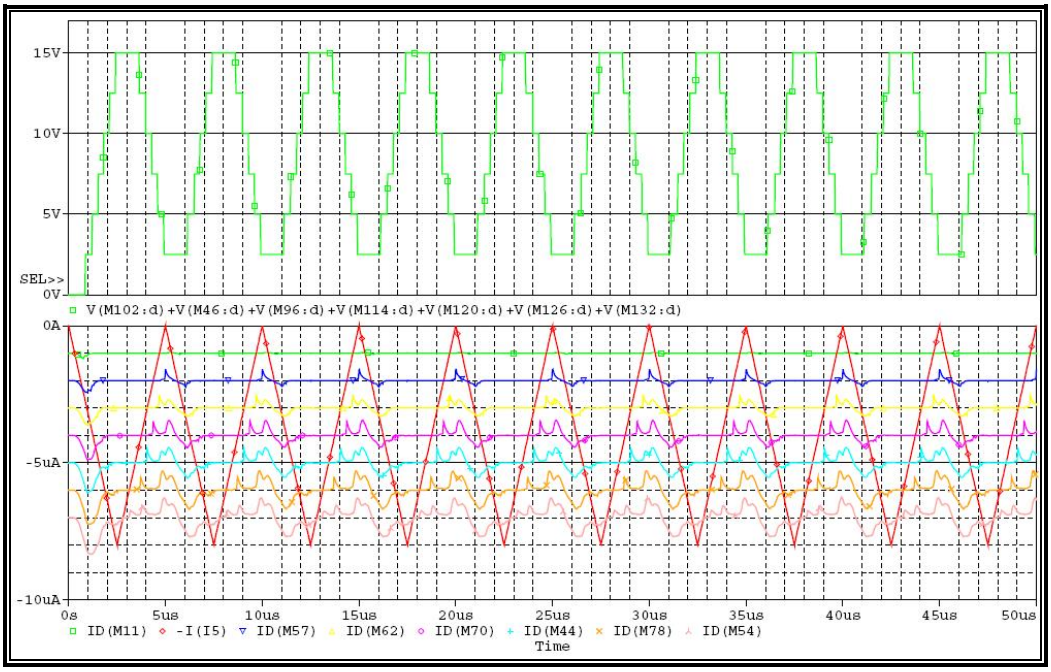

Figure 5.5 Output of cascade mirror used ADC for 200 kHz saw tooth input

In Figure5.6, the reference current is selected as 100 kHz. When the output is observed there are no missing codes and also the linearity of the converter is better than the simple current mirrors. Also the oscillations on the reference currents are decreased by increasing the frequency. This shows the effect of the parasitic capacitances (and dimension of the transistor) on bandwidth.

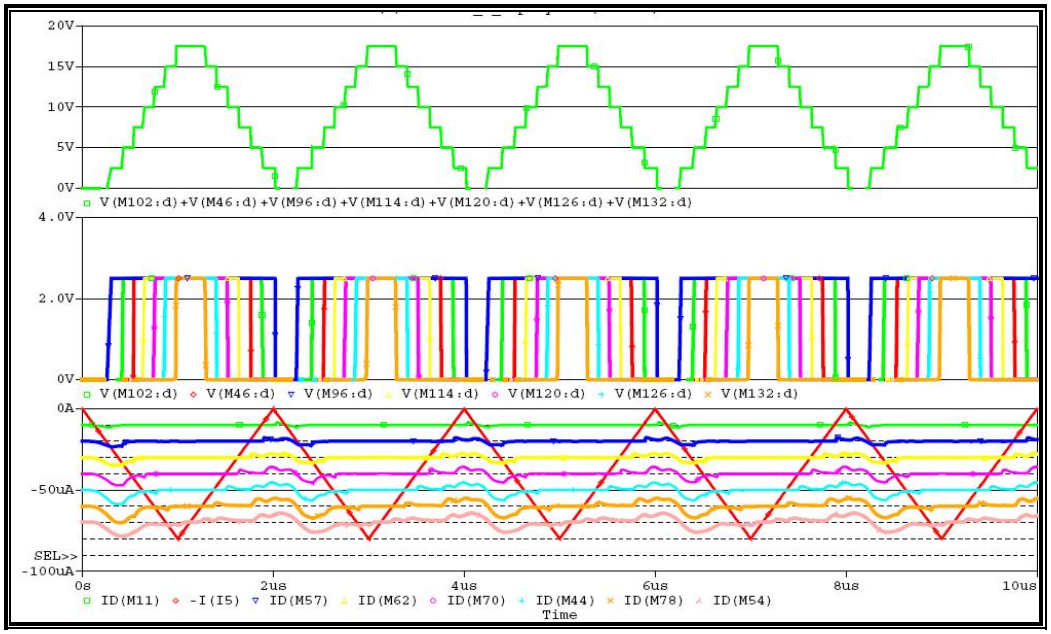

Figure 5.6 Output of cascade mirror used ADC for 100 kHz saw tooth input

In Figure5.6, the average power consumption of the converter is shown. Test was simulated when the Vcc is 2.5V and frequency is 500 kHz. The average power consumption is 7mW. This is very convenient for low power applications.

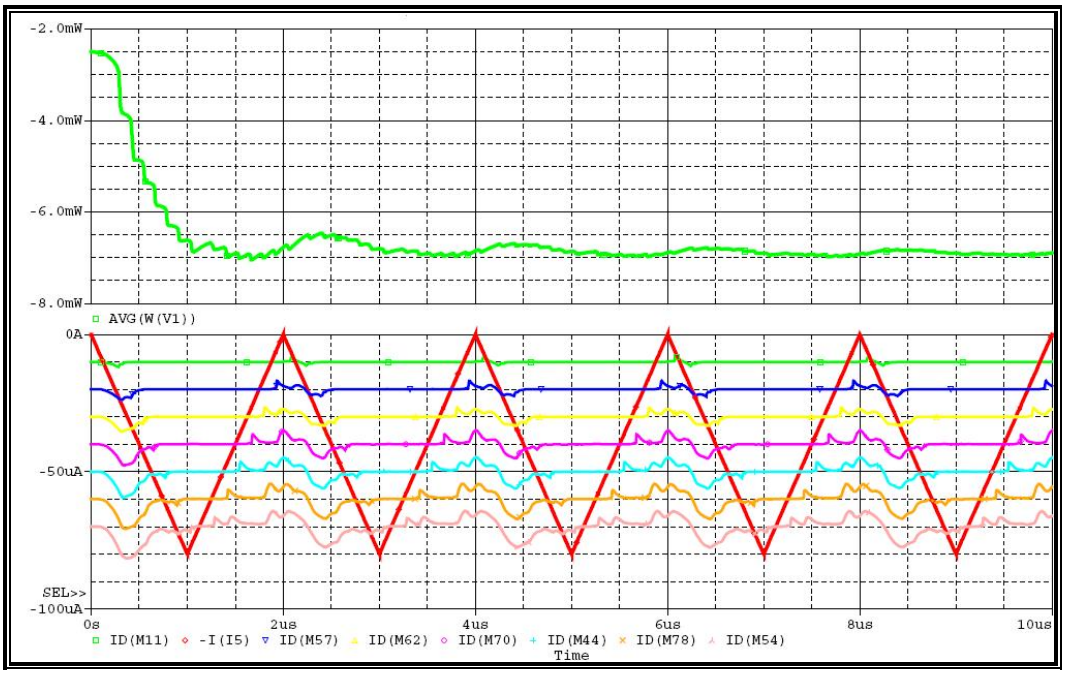

Figure 5.6 Output of cascade mirror used ADC for 500 kHz saw tooth input.

In Figure 5.7, the frequency of the signal is 50 kHz. And the power consumption of the converter is decreased to 3.8mW. This is also expected result.

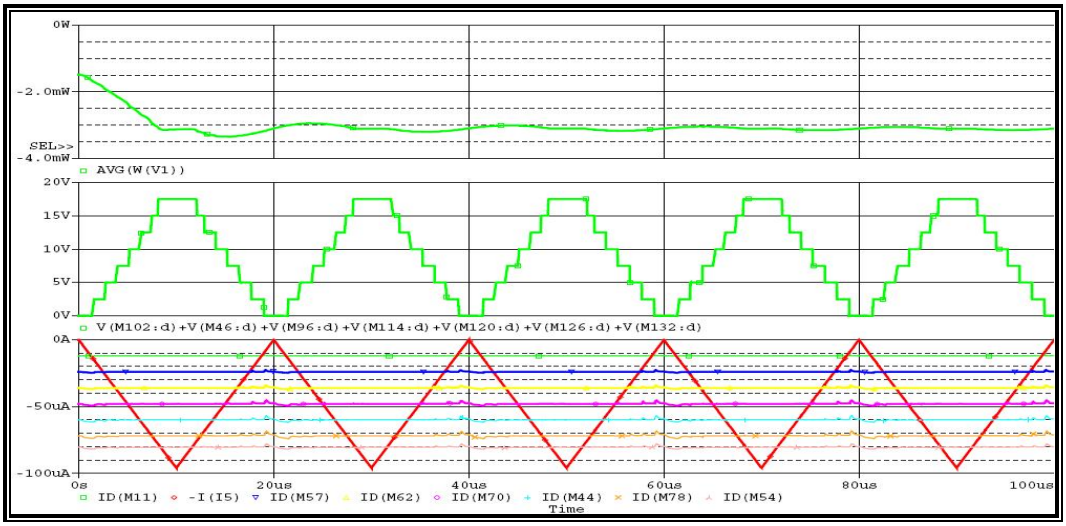

Figure 5.7 Output and power consumption of cascade mirror used ADC for 50 kHz saw tooth input.

5.1.3 Improved Wilson Current Mirror used 7- Level A/D Converters based on Current Multiplication Technique

In Figure 5.8 the output of the 7-level converters are shown which improved Wilson current mirrors are used. The input current is a 500 kHz saw tooth and oscillating between 0 and 8 µA. Like cascade current mirrors at the high frequencies and low current values there some missing codes at the output of the converter.

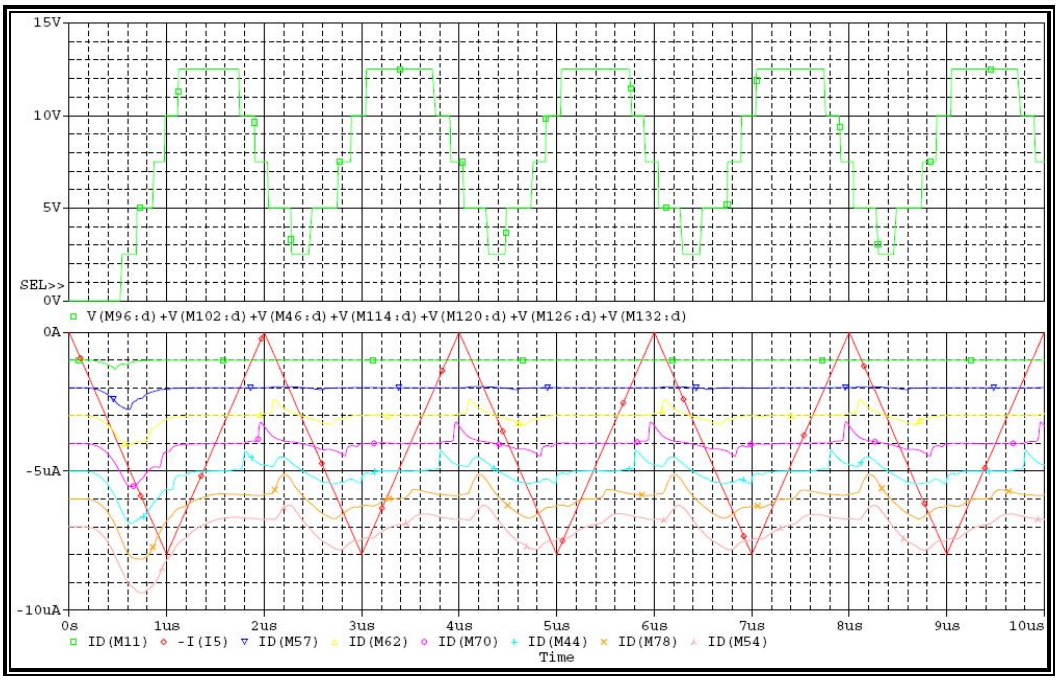

Figure 5.7 Output of improved Wilson current mirrors mirror used ADC for 500 kHz saw tooth input

In Figure 5.8, the input signal's frequency is decreased to 100 kHz. Although the frequency is decreased, there are some oscillations on the reference currents because of the switching.

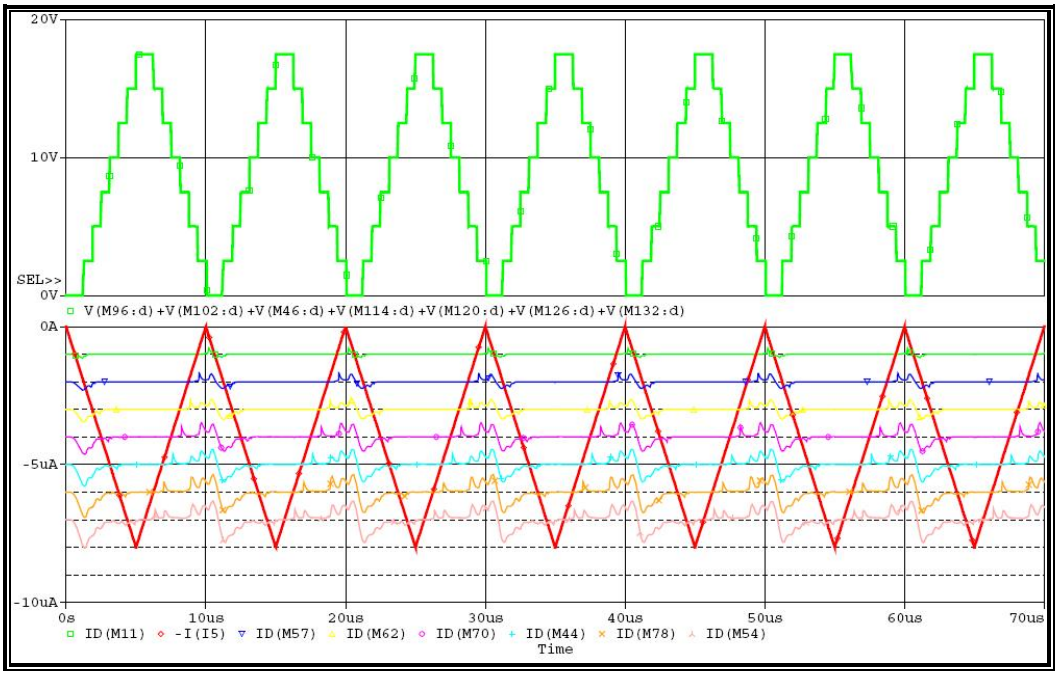

Figure 5.8 Output of improved Wilson current mirrors mirror used ADC for 100 kHz saw tooth input

Power consumption of the converter is shown in Figure5.9. Power consumption is 3.8mW when the frequency is 100 kHz and Vcc is 2.5V.

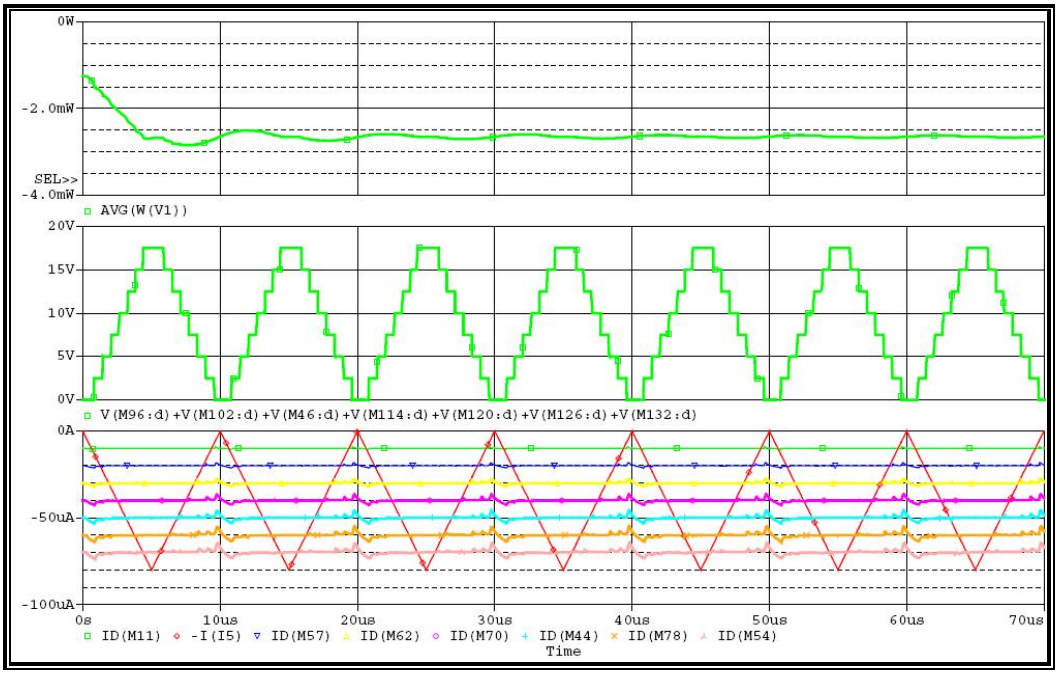

Figure 5.9 Output and power consumption of improved Wilson current mirror used ADC for 100 kHz saw tooth input.

5.2 7-Level A/D Converters based on Current Division Technique

7-level analog to digital converter based on current multiplication technique was introduced in section 4.2. In this section the designed circuits are simulated. In the simulations OrCAD 10.5 and MOSIS models are used. MOSIS model of the transistors are attached in the appendix section.

In the previous design only simple current mirrors were used and the circuit simulated only up to 5 kHz. In our work we extended the used current mirror types. We also design the circuit by using Cascade current mirrors and Improved Wilson current mirrors.

5.2.1 Basic Current Mirror used 7-Level A/D Converters based on Current Division Technique

Basic current mirrors used analog to digital converters previously only tested up to 5 kHz. In Figure 5.10 the reference current is 700nA so each level is 100nA and frequency is 100 kHz.

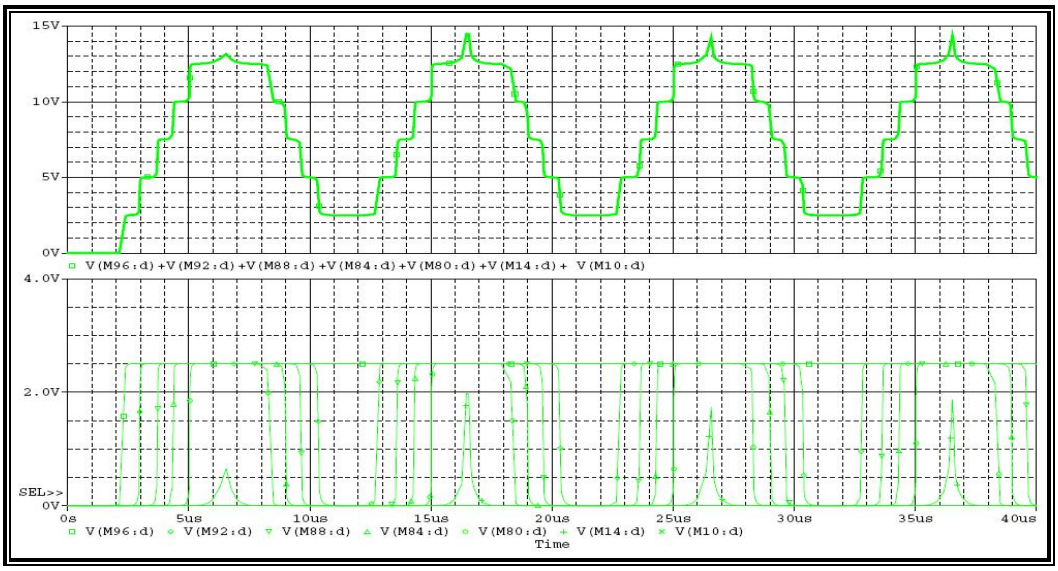

Figure 5.10 Output of basic current mirror used 7-level analog to digital converter based on current division technique for 100 kHz saw tooth input

When the input signal is changed to 8 µA saw tooth with frequency 500 kHz. (Figure 5.11) We got better shape. But also there are till have some missing codes. The linearity of converter also seems not adequate for making a conversion in this frequency.

Figure 5.11 shows the out puts of the converter at 500 kHz and the input signal is 0 to 9 µA saw tooth. Both accuracy and linearity is not enough for adequate conversion. Test results are justify the previous design made by H.Helble.

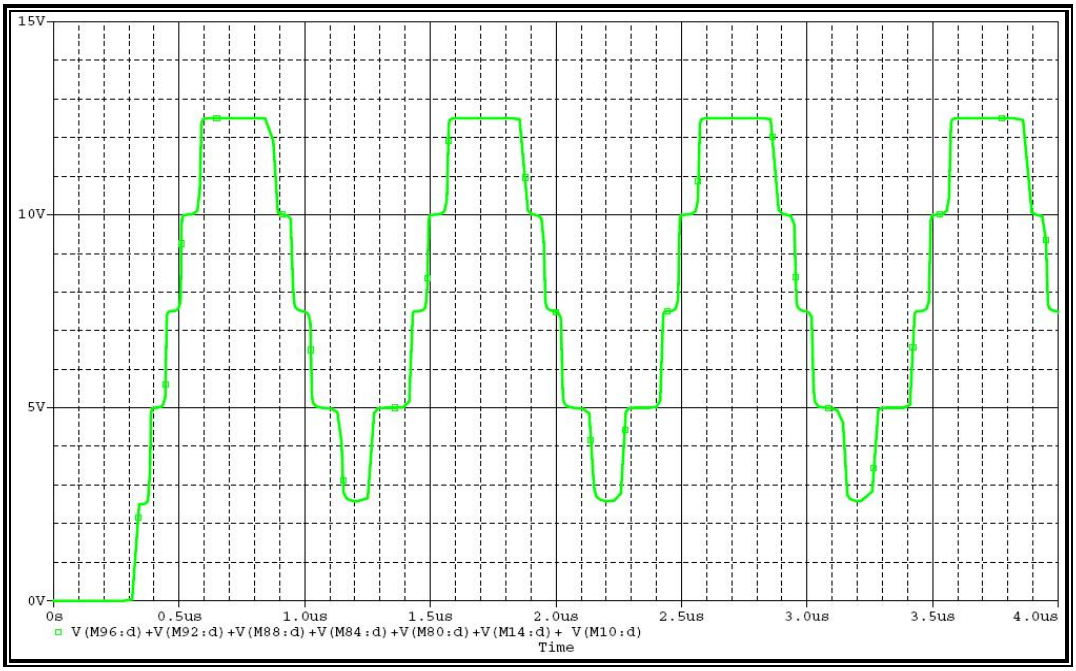

Figure 5.11 Output of basic current mirror used 7-level analog to digital converter based on current division technique for 500 kHz saw tooth input

Figure5.12 shows each output of the analog to digital converter. In the bottom of the Figure shows the LSB and top graph shows the MSB of the converter. Here the input signal is 0 to 8 µA saw tooth. And frequency is 500 kHz.

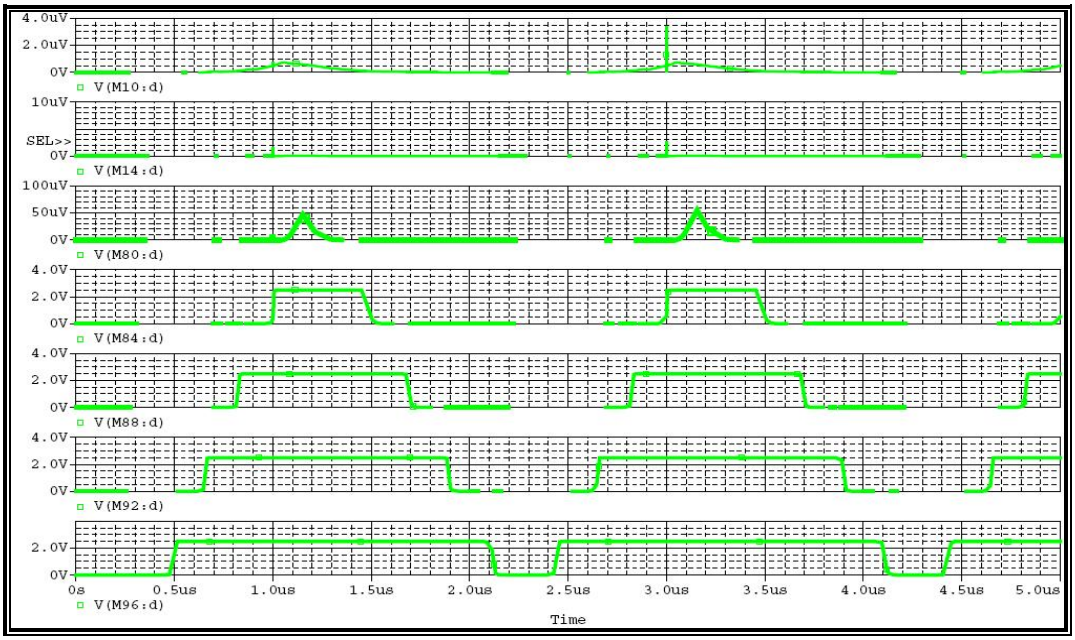

Figure 5.12 Bits of basic current mirror used 7-level analog to digital converter based on current division technique for 500 kHz saw tooth input

Figure 5.13 shows the output bits of the converter. In this simulation input signal is 0 to 80 µA and the reference current is 70 µA. So the each level is 100 µA. In Figure 5.13, the graph on the bottom shows the LSB and top graph shows the MSB. In this simulation the frequency of the input signal is decreased to 100 kHz.

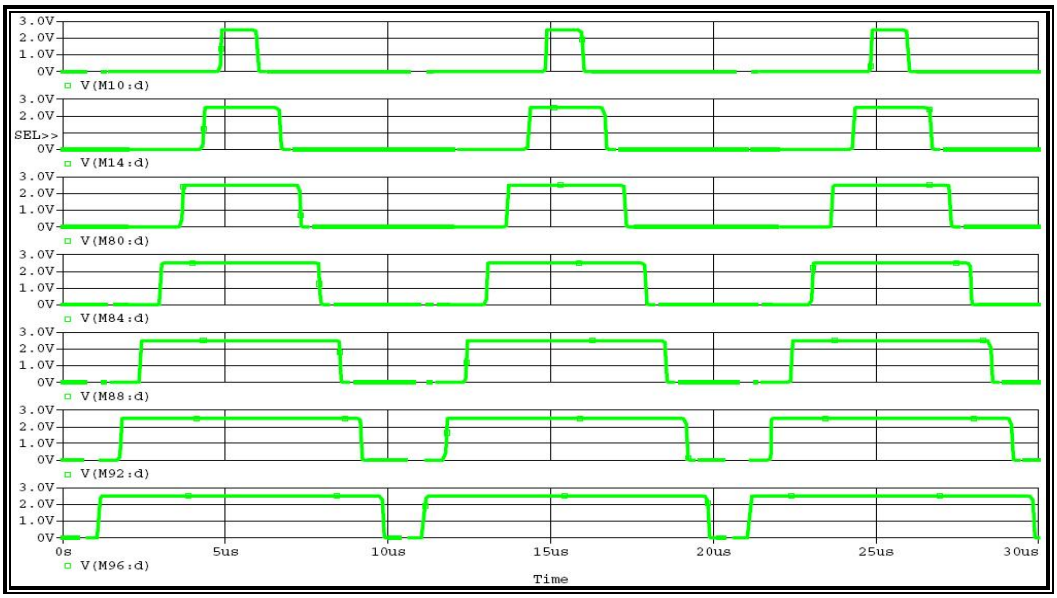

Figure 5.13 Bits of basic current mirror used 7 level A/D converter based on current division technique for 100 kHz saw tooth input

5.2.2 Cascade Current Mirror used 7-Level Analog to Digital Converters based on Current Division Technique

Being having better output impedance than the simple current, cascade current mirrors are used to improve the design. In Figure 5.14 shows the output of the cascade current mirror used analog to digital converter. The input signal is 0 to 8 µA, 500 kHz saw tooth. The top graph shows the power dissipation of the circuit, in the middle the input signal and bottom graph output of the converter.

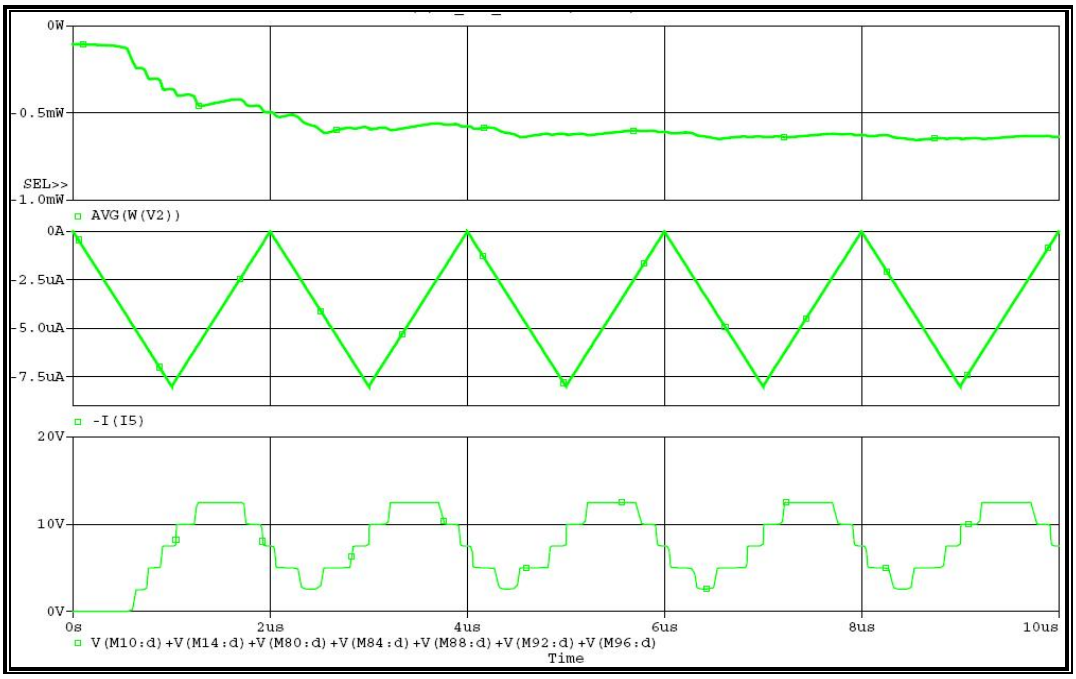

Figure 5.14 Outputs and power consumption of cascade current mirror used 7-level A/D converter based on current division technique for 500 kHz saw tooth input

Last graph of the Figure 5.14 shows the missing codes of converter. The conversion frequency is high and the reference current is low to keep transistor in subtreshold region.

In Figure 5.15, input signal's frequency is decreased to 200 kHz. So the conversion can be made properly. Although converter makes the conversion properly linearity of the system is not good enough. But power dissipation of the system is

lower than the current multiplying technique. So this type of a system is more adequate for low power applications.

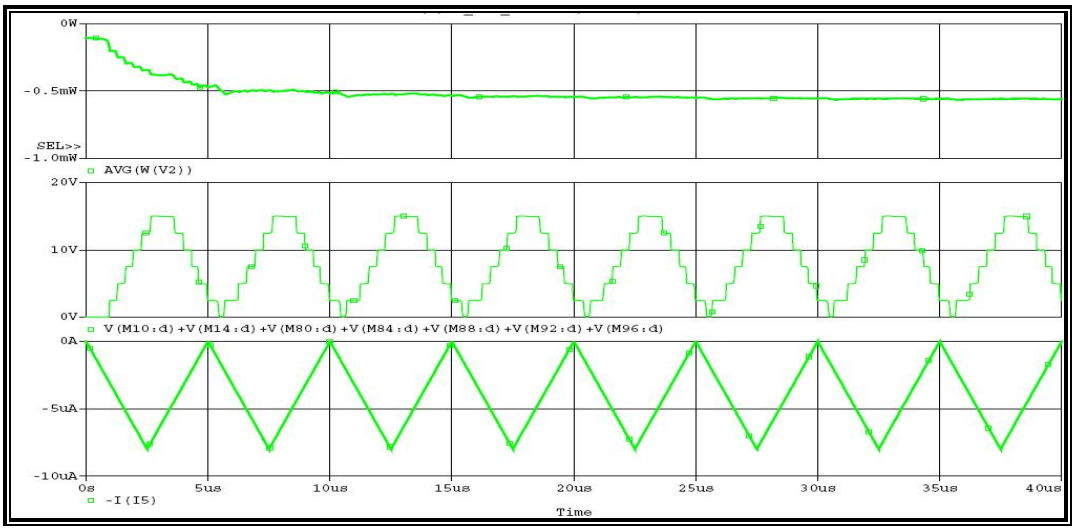

Figure 5.15 Outputs and power consumption of cascade current mirror used 7 level analog to digital converter based on current division technique for 200 kHz saw tooth input

Figure 5.16 shows the system tested with input signal 0 to 80 µA saw tooth. Power dissipation is nearly half the current multiplying technique. Figure 5.16, graph in the middle shows the converter output of the design.

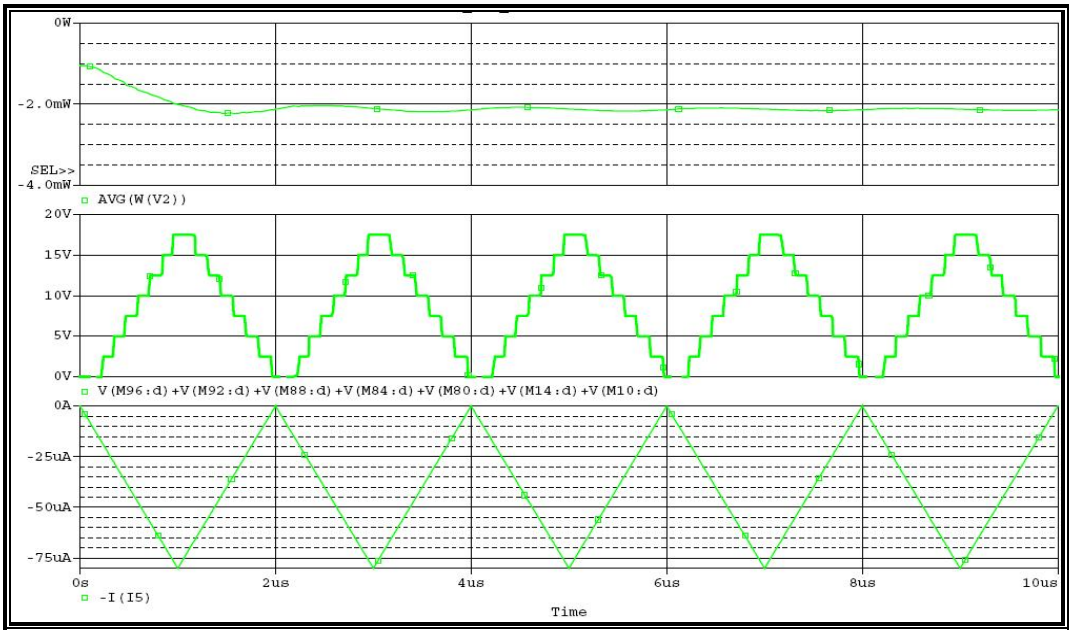

Figure 5.16 Outputs and power consumption of cascade current mirror used 7 level analog to digital converter based on current division technique for 500 kHz saw tooth input

5.2.3 Improved Wilson Current Mirror used 7-Level A/D Converters based on Current Division Technique

Like cascade current mirrors, the output impedance of the improved Wilson current mirror is better than simple current mirrors. Figure 5.17 shows the transition of the each bit from low to high. The first signal indicates the first bit (LSB) and the last signal indicates the last bit (MSB). Transition time between the forth bit and the third bit is to long considering the other transitions. And the time between second and third level is short. System's linearity is no good enough to implement this technique with this type of current mirror with these parameters.

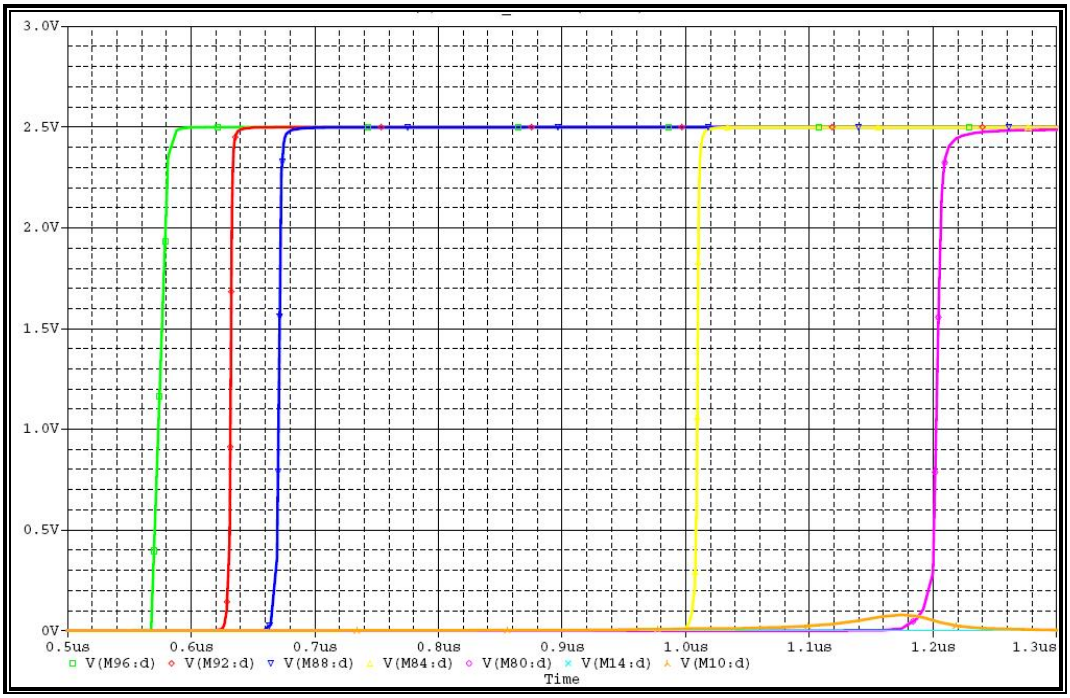

Figure 5.17 Transitions of bits from low to high for Improved Wilson current mirror used 7 level analog to digital converter based on current division technique

In Figure 5.18; input signal, output of the converter and power dissipation of the analog to digital converter. Power dissipation of the system is nearly 2 mW. In the middle graph missing codes and non linear output is shown.

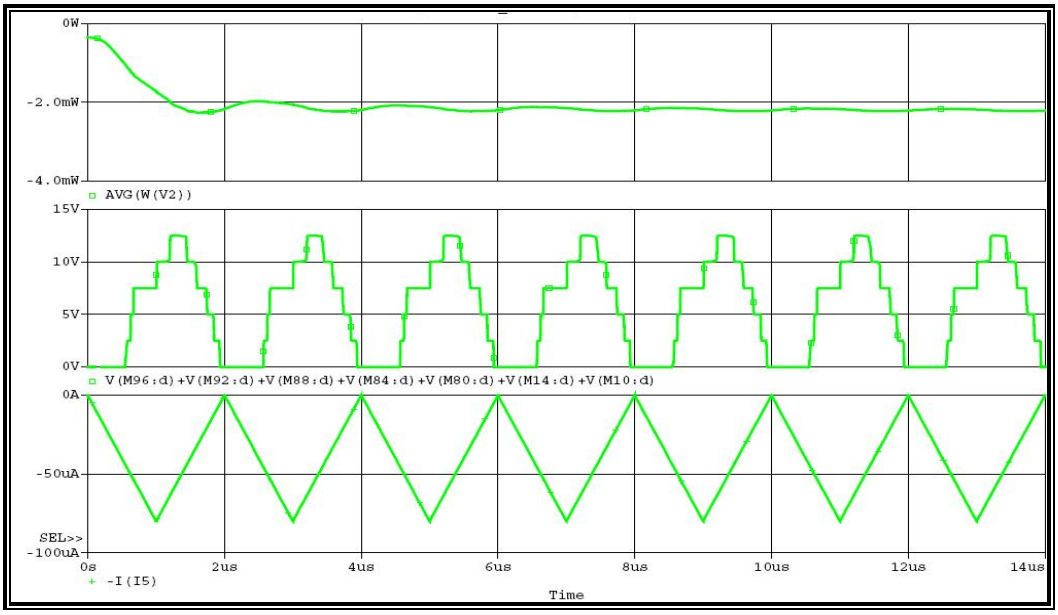

Figure 5.18 Output and power dissipation of Improved Wilson current mirror used 7 levels analog to digital converter based on current division technique

Figure 5.19 shows the transitions form low to high when the in put current is 0 to 80 µA with 100 kHz frequency and reference current is 70 µA. The un-linearity is also same. Like Figure 17, here the first signal indicates the LSB and the last signal indicates the MSB. Transition time between third bit and the forth bit is long. This causes missing codes and un-linear situation in the conversion.

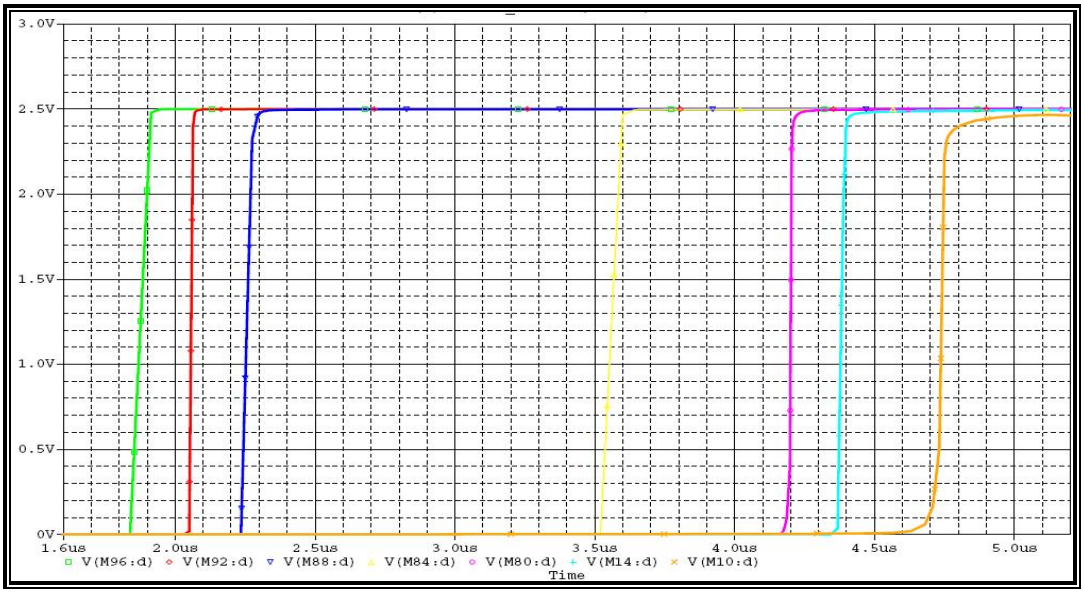

Figure 5.19 Transitions of bits from low to high for Improved Wilson current mirror used 7 level analog to digital converter based on current division technique for 100 kHz saw tooth input

Figure 5.20 shows the outputs of the system when the input is 100 kHz and 80 µA peak to peak. The linearity is low and there are some missing codes.

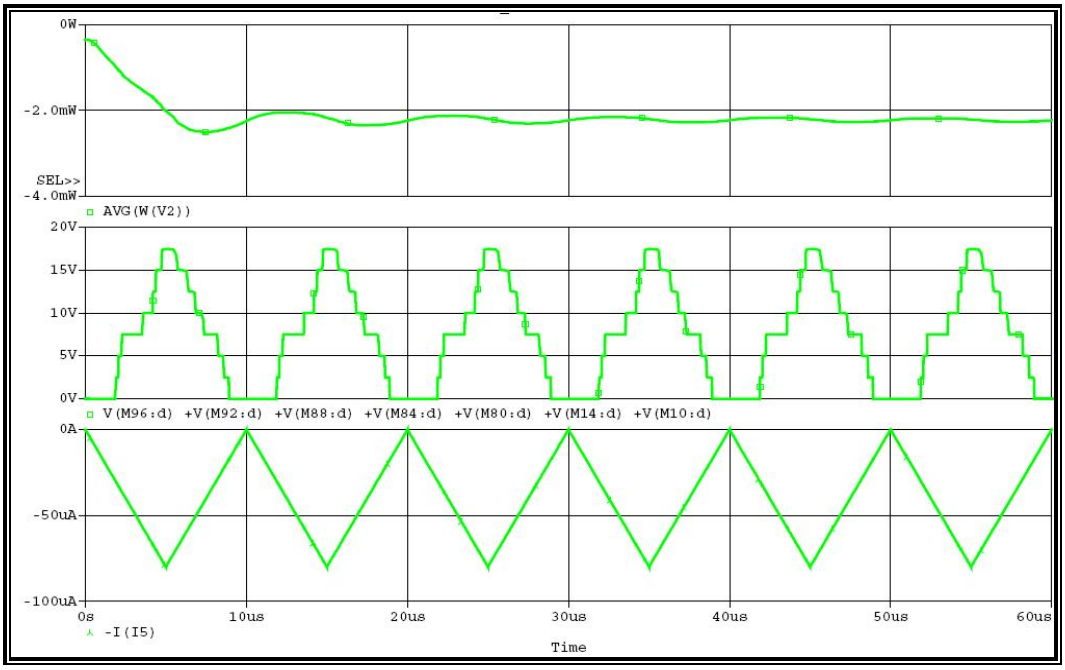

Figure 5.20 Output and power dissipation of Improved Wilson current mirror used 7 level analog to digital converter based on current division technique 100 kHz saw tooth input.

5.3 8-Level A/D Converters based on Current Multiplication Technique

7-level design of the converter is performed in the previous section. To improve our design, one level is added to our cascade and improved Wilson current mirror designs. Adding one level to analog to digital converter increased the power dissipation of the system. In these simulations OrCAd 10.5 version and MOSIS models are used. First simple current mirror used design simulated than go on with other designs used cascaded and improved Wilson.

5.3.1 Basic Current Mirror used 8-Level A/D Converters based on Current Multiplication Technique

Figure 5.21 shows the output of 8-level analog to digital outputs. Input signal of the converter is 0 to 9 µA, 100 kHz saw tooth. And each comprising level is 1uA. Comparison is made in the range 0 to 8 µA. In Figure 21 shows the each output of the bits.

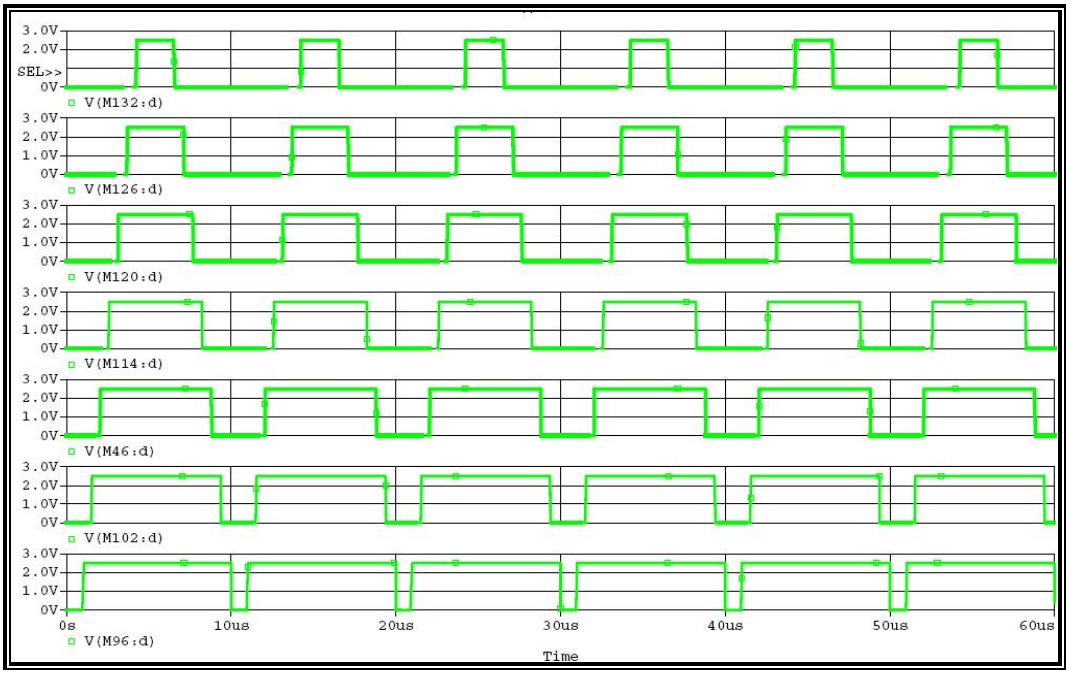

Figure 5.20 Output bits of simple current mirror used 8-level analog to digital converter based on current multiplication technique for 100 kHz saw tooth input.

The graph in the bottom shows the LSB , the graph on the top shows MSB of the converter. Linearity of the system is good. Also the INL and DNL of the system are calculated.

5.3.2 Cascade Current Mirror used 8-Level A/D Converters based on Current Multiplication Technique

Figure 5.22 shows the output of the cascade current mirror used design. Input signal of the system is 500 kHz, 9 µA peak to peak saw tooth. Bottom graph in the Figure 5.22 shows the reference currents and input signal. Like 7-level design, on the reference currents there are some oscillations because of the switching and parasitic capacitance. So these capacitances make system bandwidth low. Graph on the top shows the converter output. There are some missing codes at the output.

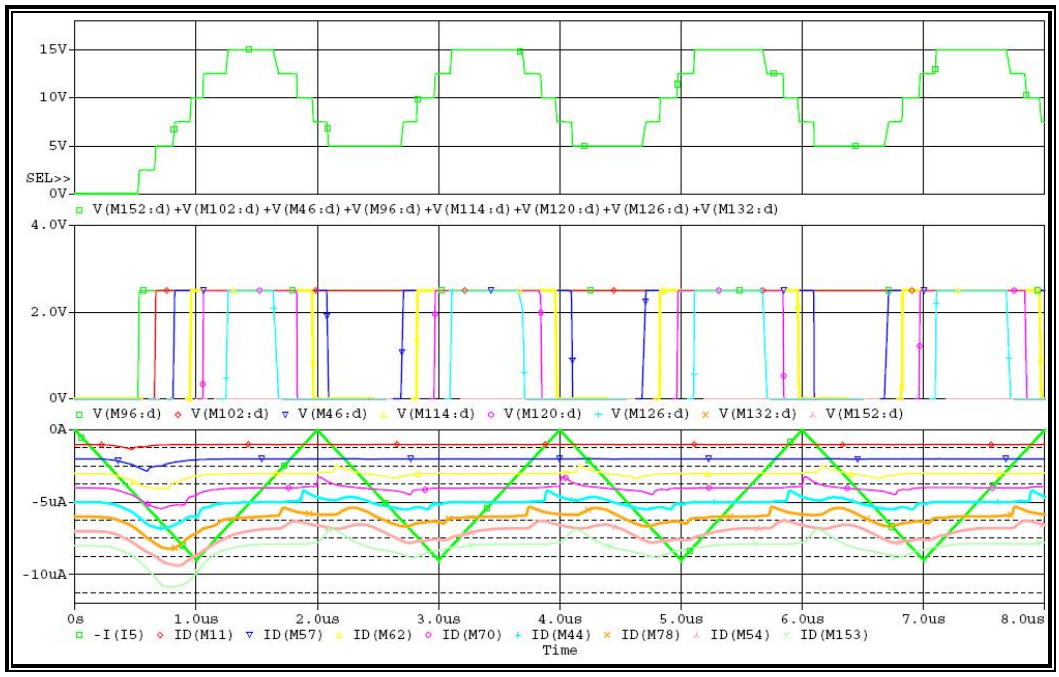

Figure 5.22 Output of cascade current mirror used eight level analog to digital converter based on current multiplication technique for 500 kHz saw tooth input.

Figure 5.23 shows the output, when the frequency is 500 kHz and input signal is 90 µA peak to peak. Oscillations on the reference currents are seem to be smaller but the scale is different from the Figure 22. There are still some oscillations on the reference currents. Being the reference currents high with this level there is no missing codes. Power dissipation of system is approximately 4mW.

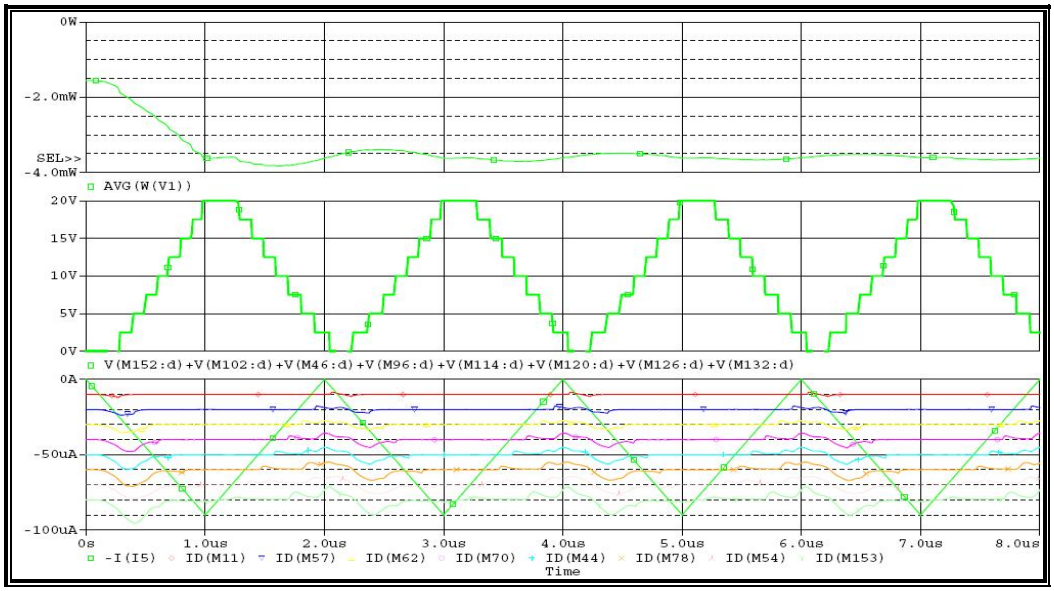

Figure 5.23 Output of cascade current mirror used eight level analog to digital converter based on current multiplication technique for 500 kHz saw tooth input.

5.3.3 Improved Wilson Current Mirror used 8-Level A/D Converters based on Current Multiplication Technique

Improved Wilson current mirror used analog to digital converter outputs are shown in Figure 5.24.

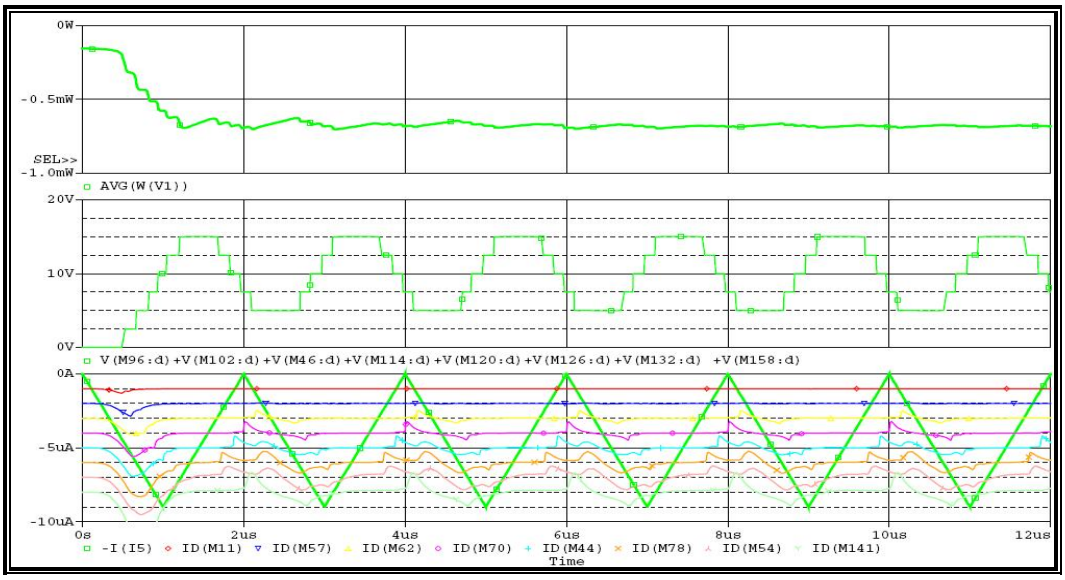

Figure 5.24 Output and power consumption of Improved Wilson current mirror used 8 level analog to digital converter based on current multiplication technique for 500 kHz saw tooth input.

In Figure 5.24; input signal, reference currents are shown in the bottom. The input signal is 500 kHz, 9 µA peak to peak saw tooth. A reference currents oscillation causes the problem at the output of the converter. This is shown in the middle graph. There are some missing codes. And also these missing codes cause missing transitions and decreasing the power dissipation.

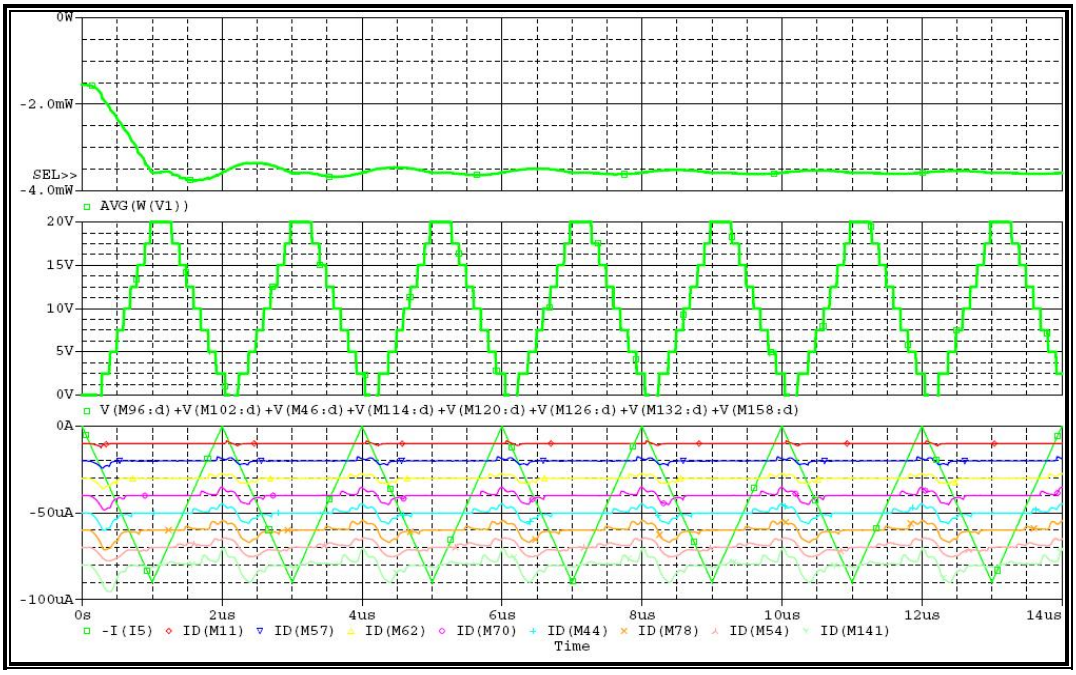

Figure 5.25 Output and power consumption of Improved Wilson current mirror used 8 level analog to digital converter based on current multiplication technique for 500 kHz saw tooth input.

Figure 5.25 shows the system with the increased peak to peak input signal. Here input signal's peak to peak value is 90 µA. Because of the parasitic capacitance of the MOS transistor and switching there are some oscillations. But this time power dissipation is increased to 4mW.

Input signal's frequency and peak to peak vale is changed and tested in the Figure 5.26. In this simulation input signal's frequency is 100 kHz and peak to peak value is 90 µA. The oscillations on the reference currents are decreased by decreasing frequency. And the linearity becomes better with these reference currents. Power dissipation of the system is 3.8mW.

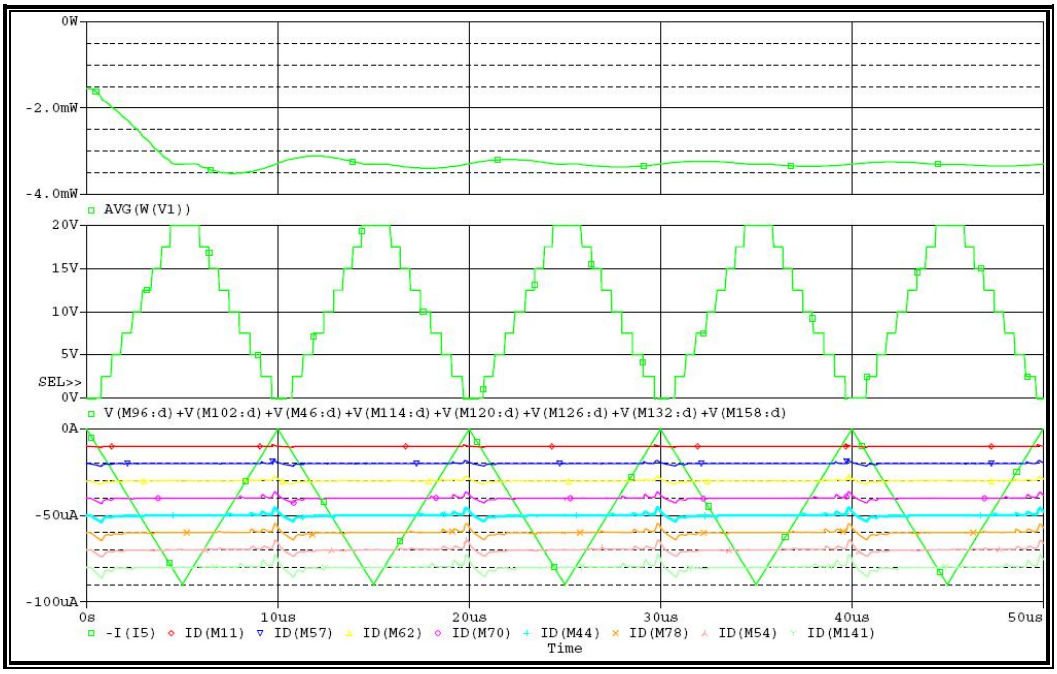

Figure 5.26 Output and power consumption of Improved Wilson current mirror used 8 level analog to digital converter based on current multiplication technique for 100 kHz saw tooth input.

5.4 8-Level A/D Converters based on Current Division Technique

8-level analog to digital converters based on current multiplication technique is introduced in section3.4. Simulations are performed with OrCAD 10.5. MOSIS transistor models are used in simulations. First we start simulations with simple current mirror used design and performed different inputs. Than same inputs are supplied to cascade mirror and improved Wilson current mirror used designs.

5.4.1 Basic Current Mirror used 8-Level A/D Converters based on Current Division Technique

Basic current mirror used 8-level design's results are shown in Figure. At the first test input signal's frequency is 500 kHz and the amplitude is 9 µA peak to peak. Similar to the 7-level design output of the converter has some missing codes with this input. Reference current is 8 µA. According to topology which we used in our design each level has 1uA resolution. Power consumption of the circuit is seemed

low but the rest of the circuit does not work properly. So all switching does not perform these decreases the switching losses and power dissipation on the transistors.

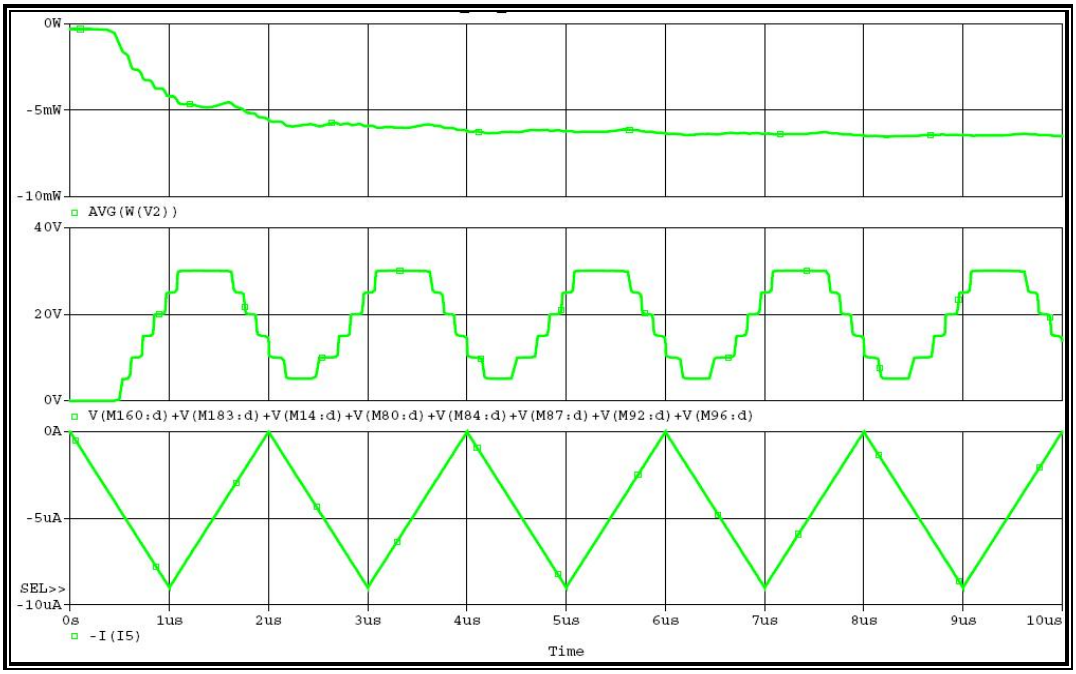

Figure 5.27 Output and power consumption of basic mirror used 8 level analog to digital converter based on current division technique for 500 kHz saw tooth input.

In Figure 5.28, the input signal is changed to 9uA peak to peak and 100 kHz. With this input there are no missing codes at the output of the converter. Also the power dissipation is 3.8mW

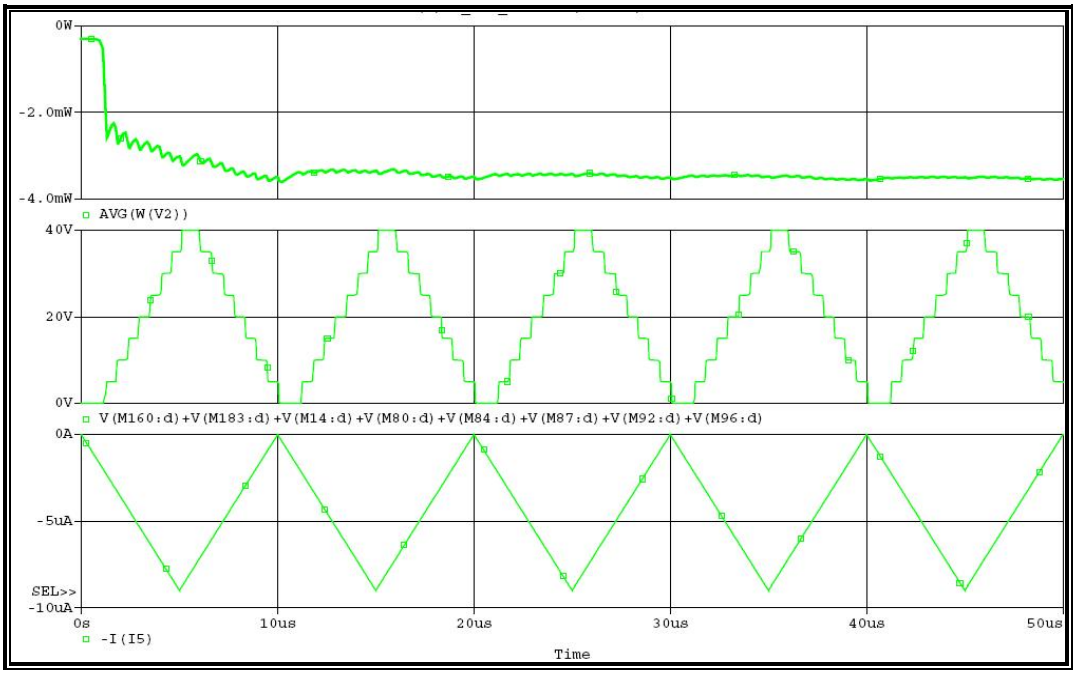

Figure 5.28 Output and power consumption of basic mirror used 8 level analog to digital converter based on current division technique for 100 kHz saw tooth input.

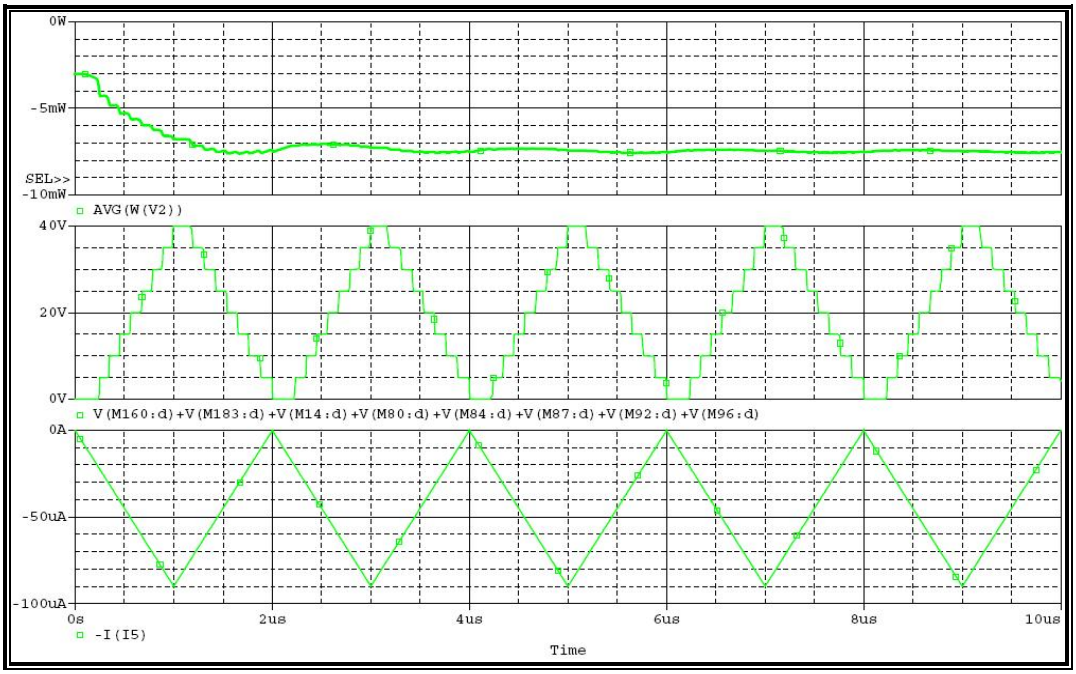

Figure 5.29 Output and power consumption of basic current mirror used 8 level analog to digital converter based on current division technique for 500 kHz saw tooth input and Vcc is 5V

In Figure 5.29 and Figure 5.30, Vcc is increased to 5V for different frequencies. This causes to double the power dissipation of the system. The linearity of the system is not effected by the change of the supply.

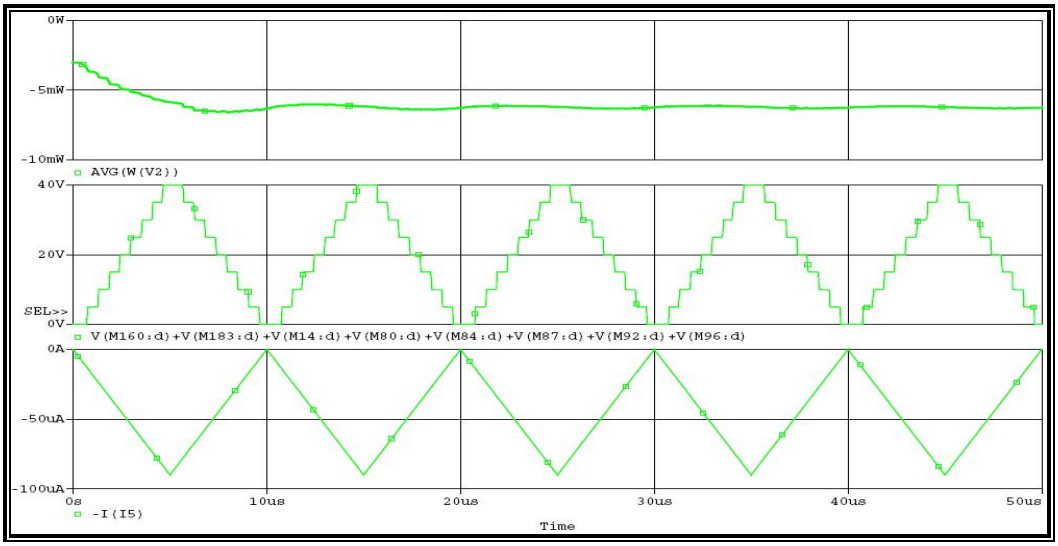

Figure 5.30 Output and power consumption of basic current mirror used 8-level analog to digital converter based on current division technique for 100 kHz saw tooth input and Vcc is 5V

5.4.2 8-Level Cascade Current Mirror used A/D Converters based on Current Division Technique

Cascade mirrors used analog to digital converter results are shown in Figure 31. The input signal is 9 µA peak to peak and 500 kHz saw tooth in Figure 5.31. In Figure 5.31 power consumption, output of the converter and input signal waveform are shown.

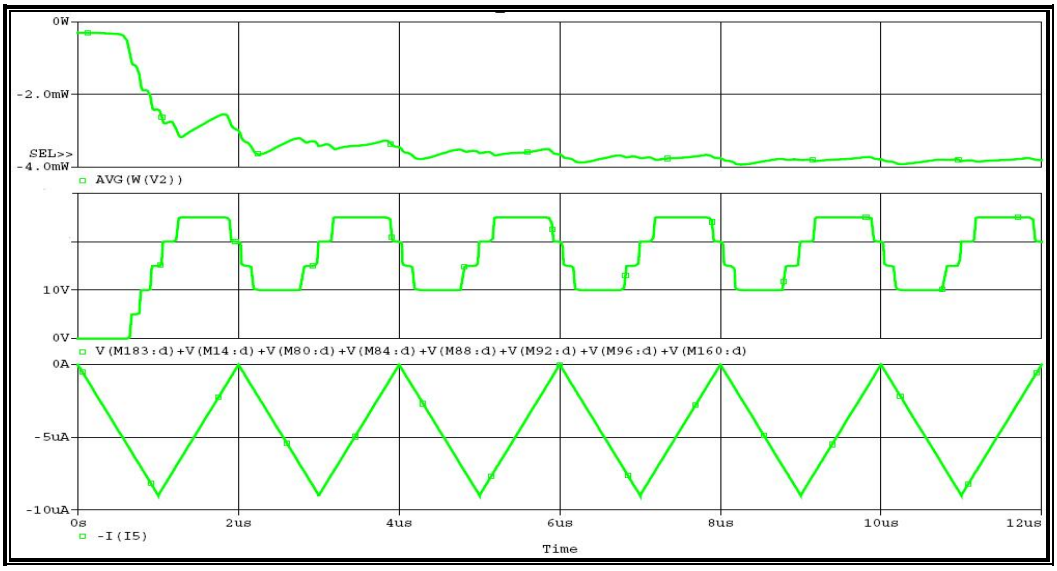

Figure 5.31 Output and power consumption of cascade current mirror used 8 level analog to digital converter based on current division technique for 500 kHz saw tooth input

Graph in the middle shows the converter output of the system. From this graph some missing codes can be seen. In Figure 5.32 shows the bit transitions from low to high. The first signal indicates the LSB and the last signal indicates the fifth bit of the converter. Because of the error some bits are not switched. This is effect of parasitic capacitances.

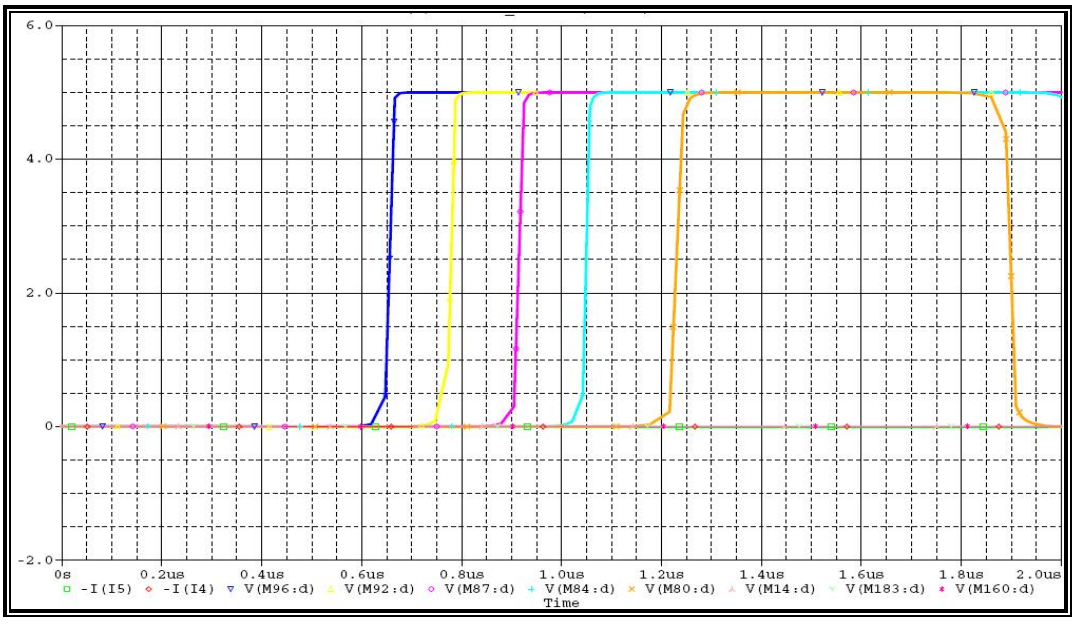

Figure 5.32 Bit transitions from low to high of cascade current mirror used 8 level analog to digital converter based on current division technique for 500 kHz saw tooth input .

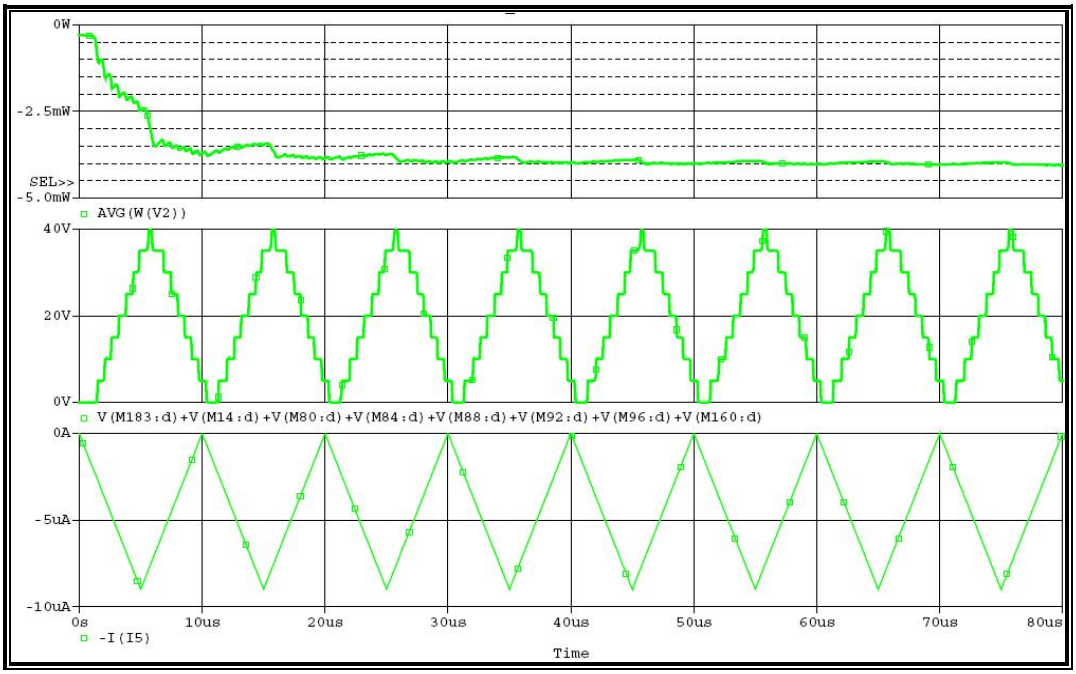

Figure 5.31 Output and power consumption of cascade current mirror used 8 level analog to digital converter based on current division technique for 100 kHz saw tooth input

In Figure 5.32, the input signal's frequency decreased to 100 kHz. Decreasing the frequency gives better switching results. Considering the 7-level design bandwidth of the 7 level design is better then the 8-level design.

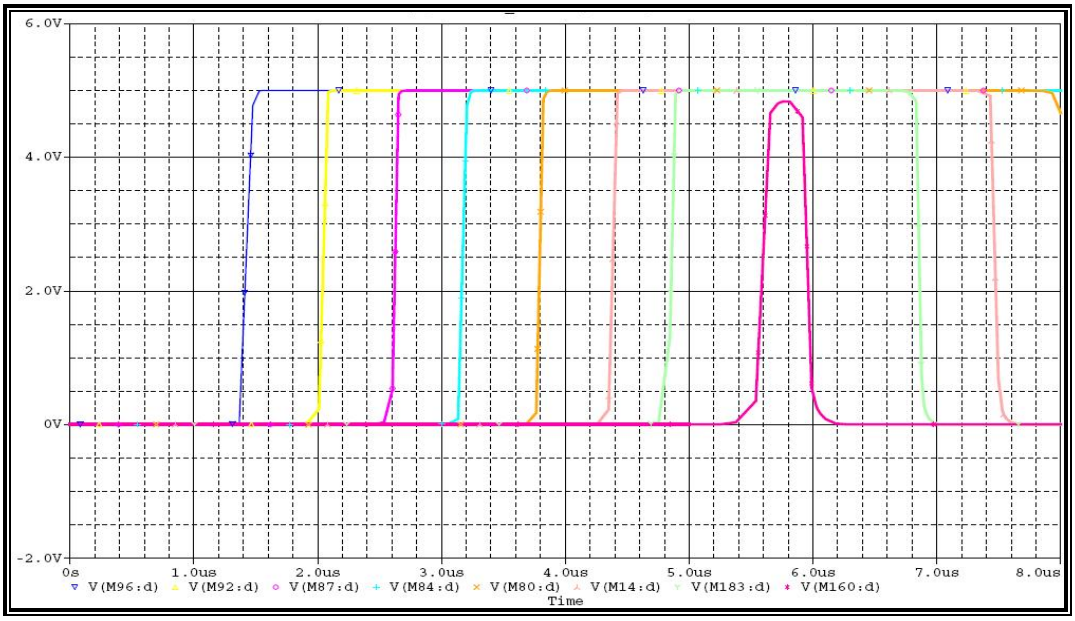

Figure 5.33 Bit transitions from low to high of cascade current mirror used 8 level analog to digital converter based on current division technique for 200 kHz saw tooth input .

5.4.3 8-Level Improved Wilson Current Mirror used A/D Converters based on Current Division Technique

Improved Wilson current mirrors used design's output is shown in Figure 5.34. These are the bit of the converter. The input signal is 90 µA peak to peak 200 kHz saw tooth. Signal in the left indicates LSB of the converter and signal in the right indicates the MSB of the converter. as it shown form the Figure transition time between third bit and forth bit is longer than others. And transition time between forth bit and fifth bit is shorter than others. Transitions times from high to low are better than the low to high.

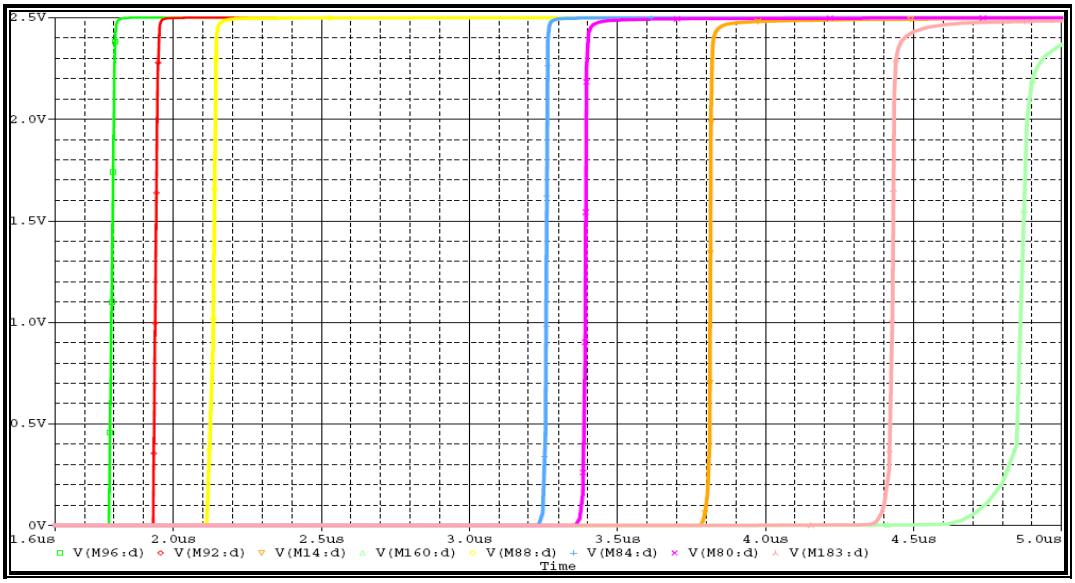

Figure 5.34 Bit transitions from low to high of Improved Wilson current used eight level analog to digital converter based on current division technique for 200 kHz saw tooth input .

In Figure 5.35, transitions times from high to low is shown. Signal in the left indicates the MSB of the converter; signal in the right indicates the LSB of the converter. Transition time between seventh bit and sixth bit is shorter than the others but this is not as bad as transition time from low to high. In Figure 36, the reference is shown currents for conversion. Each level is exactly 10 µA as expected.

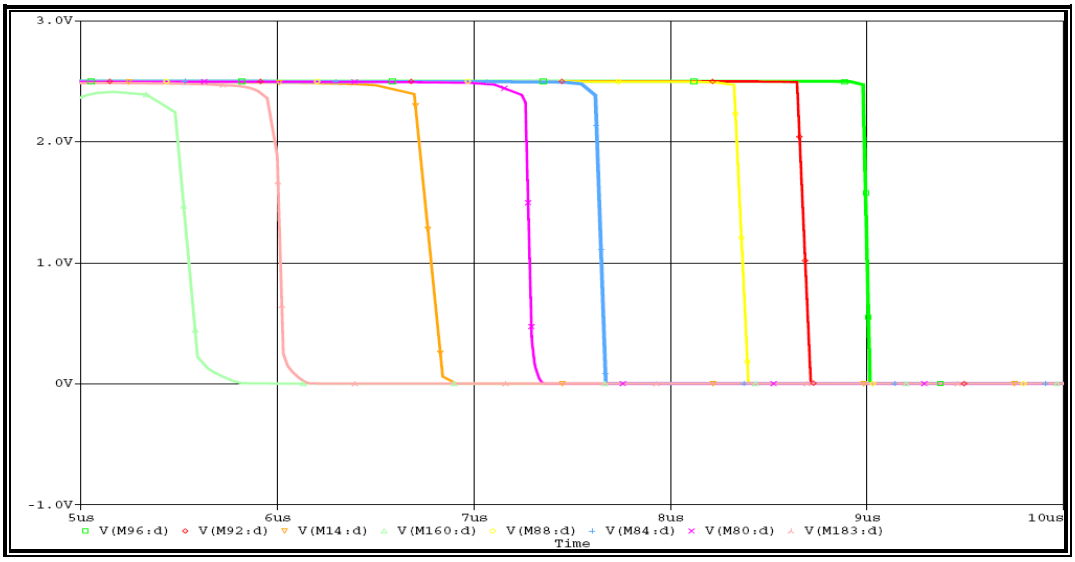

Figure 5.35 Bit transitions from high to low of Improved Wilson current used eight level analog to digital converter based on current division technique for 200 kHz saw tooth input .

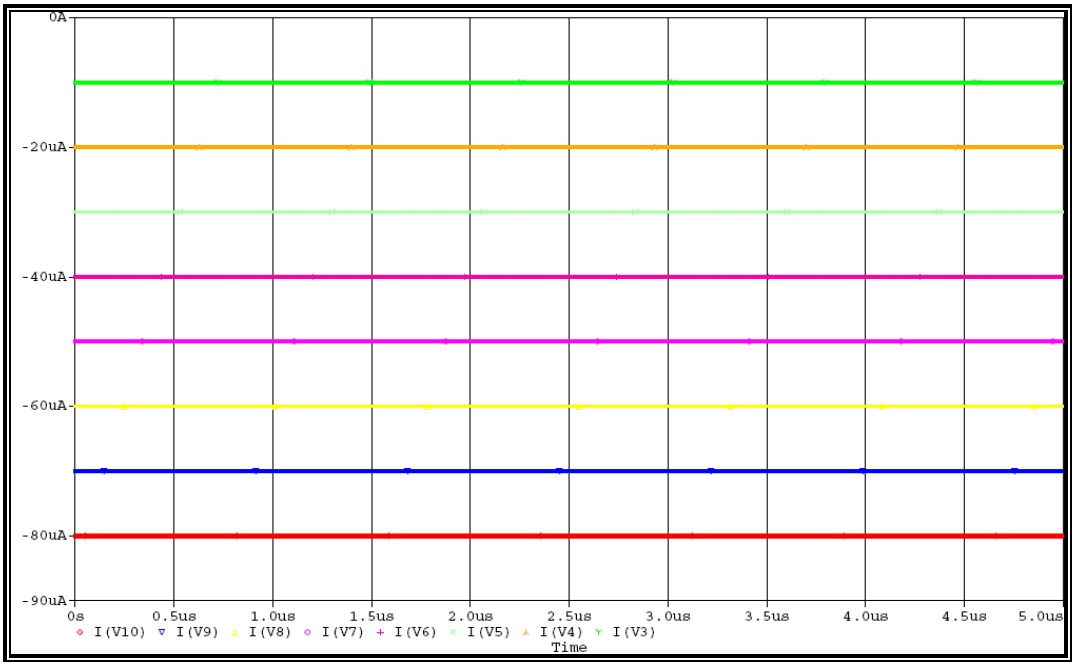

Figure 5.36 Reference currents of Improved Wilson current mirror used eight level analog to digital converter based on current division technique for 80uA

In Figure 5.37; Output, input and the power consumption of the converter is shown. In Figure 5.36, reference currents are shown. Linearity of the converter is not good because of the not equal transition times. In Figure 5.38, reference currents

for 80pA are shown. There are little deviations in such a low current levels. Power consumption of the circuit is nearly 2.2mW.

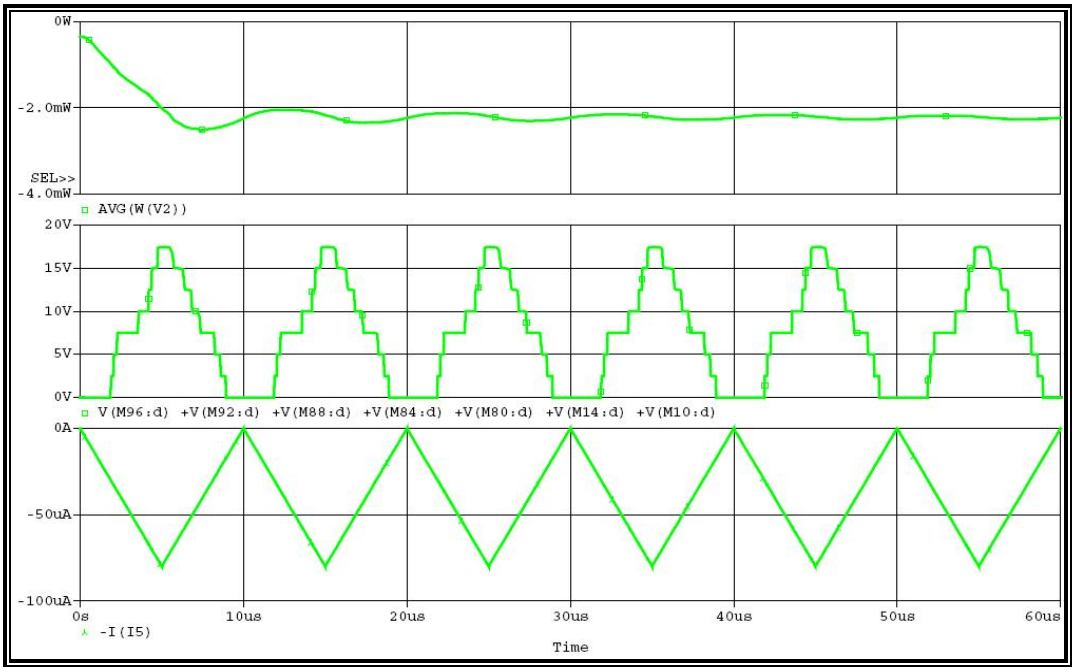

Figure 5.37 Output and power consumption of Improved Wilson current mirror used 8-level analog to digital converter based on current division technique for 100 kHz saw tooth input

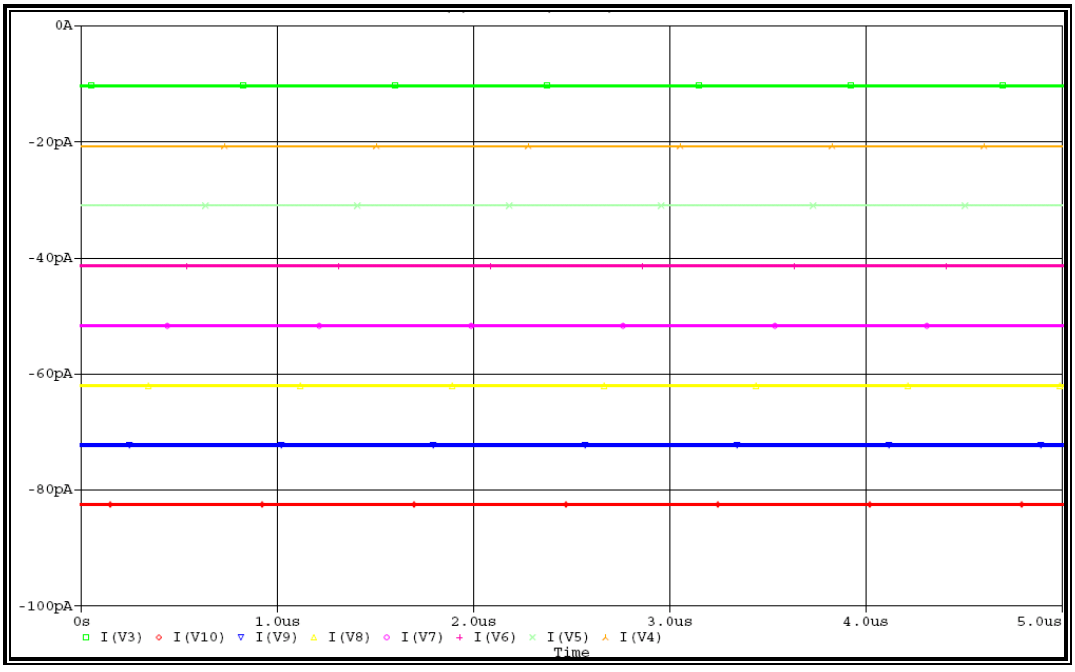

Figure 5.38 Reference currents of Improved Wilson current used 8-level analog to digital converter based on current division technique for 80pA

5.4 INL and DNL RESULTS

The integral nonlinearity is the difference between the ideal and measured code transition levels after correcting for static gain and offset. Integral nonlinearity is usually expressed as a percentage of full scale or in units of LSBs. Differential nonlinearity (DNL) is the difference, after correcting for static gain, between a specified code bin width and the ideal code bin width, divided by the ideal code bin width. Maximum INL and DNL of the ADCs are calculated. In Figure 5.39 INL and DNL results for seven bit ADC based on current multiplication technique.

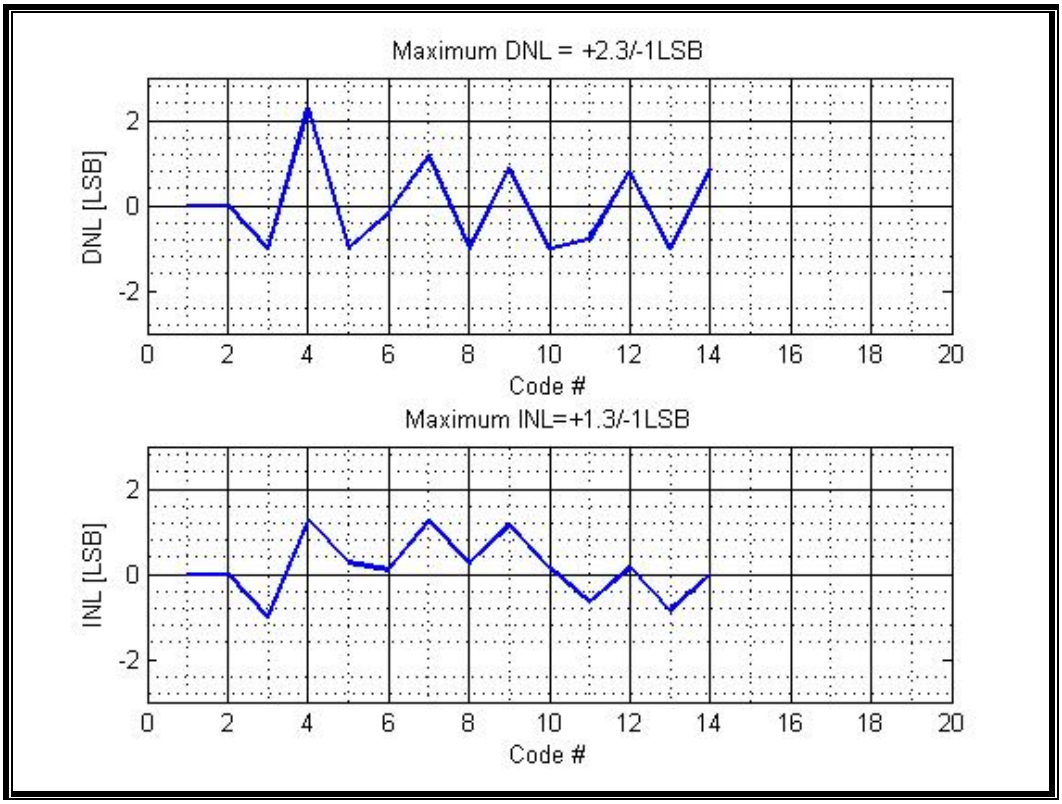

Figure 5.39 INL and DNL results seven level ADC based on current multiplication technique.

INL and DNL results of other ADCs are listed below table 5.1

Table 5.1 INL and DNL results of ADCs

	Max INL	Max DNL
Seven level ; basic current mirror used ADC based on Current Multiplication Technique	1.3 lsb	2.3 lsb
Eight level ; basic current mirror used ADC based on Current Multiplication Technique	1.6 lsb	1.1 lsb
Seven level ; basic current mirror used ADC based on Current Division Technique	2.1 lsb	1.9 lsb
Eight level ; basic current mirror used ADC based on Current Division Technique	2.1 lsb	1.6 lsb
Seven level ; Cascode current mirror used ADC based on Current Multiplication Technique	0.6 lsb	1.2 lsb
Eight level ; Cascade current mirror used ADC based on Current Multiplication Technique	1.6 lsb	1.4 lsb
Seven level ; Cascade current mirror used ADC based on Current Division Technique	1.6 lsb	1.5 lsb
Eight level ;Cascade current mirror used ADC based on Current Division Technique	1.9 lsb	1.2 lsb

INL improvement of using cascade mirrors can be seen from the table 5.1. 7-level design which is used basic current mirror; INL value is 1.3 lsb and 7-level design which cascade current mirror used design 0.6lsb. As a result for high frequencies cascade and improved Wilson current mirrors are more eligible than simple current mirrors.

CHAPTER SIX
CONCLUSION

In this study, a current-mode analog-to-digital conversion concept, based on current multiplication and current division technique was analyzed and developed. This technique is firstly introduced by G. Rachmuth and developed by H. Helble in 2004. Therefore, the performance of the ADC is limited by the current mirrors. Previous designs which made by G. Rachmuth and H. Helble were realized by using simple current mirrors. One technique to improve accuracy of the ADC is using Cascade and Improved Wilson current mirrors. High output impedance of Cascade and Improved Wilson current mirrors makes ADC accuracy better. Simulation results show that by using cascade current mirrors and improved Wilson current mirrors, accuracy of the ADC can be improved. By improving accuracy, previous design is improved and a new ADC is developed in this study. There were seven conversion levels in the previous design.

ADCs are designed and simulated, including basic, cascade, and improved Wilson current mirrors. Their limitations on mirroring accuracy are investigated. It is verified with calculations that the main accuracy limitations, i.e., finite output resistance and device mismatches By changing the current mirrors used in previous design, new ADCs are developed having eight conversion levels. In the previous design ADC is tested under condition 25nA reference current and 5 kHz frequency. In this study, these conditions are improved to 100 kHz by changing the reference current to 8µA. This system was first designed to be used in medical cases and low power needed systems. To reduce the size of the design in further, and eliminate any clocked circuitry, which introduces noise in the analog circuits, and increases power dissipation. New designs also fulfill these requirements by having 3.8mW (current multiplication technique) and 2mW (current division technique) power consumptions. Current division technique has low power consumption but its accuracy and linearity is worse than the current multiplication technique in lower current values. INL and DNL are calculated in Chapter Five, Results part. The INL

and DNL results show the improvement in linearity. These are the key parameters for DC performance of the ADCs.

These new current multiplication and current division ADC techniques are simple to implement and improve. In this study, the dimensions of the transistors are kept same with the previous design which made by H.Helble.

Current mode approach is not very new approach in theory but it is new for application. There have not been many designs based on current mode approach. In some ways, current mode approach has some advantages according to voltage mode approach; such as dealing with sensors and low voltage applications. As a future work, conversion levels of ADCs can be improved. As it is calculated and can be seen from the simulations; main problems in current mode ADCs are low output impedance and device mismatches. The speed of the system can be increased by improving match of the transistors and optimizing the dimensions of MOS transistors. Moreover, VLSI implementation can be realized.

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APPENDICES

APPENDIX A. MOSIS PARAMETRIC TEST RESULTS

RUN: T22Y VENDOR: AMI

TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5N

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.93	volts
SHORT	20.0/0.6			
Idss		450	-246	uA/um
Vth		0.68	-0.91	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.72	-0.96	volts
Vjbkd		11.6	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.59	V^0.5
K' (Uo*Cox/2)		58.5	-18.9	uA/V^2
Low-field Mobility		470.97	152.16	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask and etch bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL
SCN_SUBM (lambda=0.30)	0.00
AMI_C5	0.00
SCN (lambda=0.35)	-0.10

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.4	105.1	22.0	1095	38.7	0.09	0.09	ohms/sq
Contact Resistance	56.5	134.9	15.7		24.9		0.78	ohms
Gate Oxide Thickness	139							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	817	809	ohms/sq
Contact Resistance	0.73			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	423	730	86		30	15	10	40	aF/um^2
Area (N+active)			2478		35	15	11		aF/um^2
Area (P+active)			2388						aF/um^2
Area (poly)				942	49	15	9		aF/um^2
Area (poly2)					45				aF/um^2
Area (metal1)						29	12		aF/um^2
Area (metal2)							34		aF/um^2
Fringe (substrate)	312	253			69	53	36		aF/um
Fringe (poly)					57	36	28		aF/um
Fringe (metal1)						54	33		aF/um
Fringe (metal2)							49		aF/um
Overlap (N+active)			207						aF/um
Overlap (P+active)			291						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.86	volts
Vinv	2.0	2.47	volts
Gain	2.0	-19.70	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		95.01	MHz
D256_WIDE (31-stg,5.0V)		151.13	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.48	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		0.99	uW/MHz/gate

COMMENTS: SUBMICRON
T22Y SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Apr 9/02
* LOT: T22Y WAF: 1102
* Temperature_parameters=Default

```
.MODEL CMOSN NMOS (                                 LEVEL   = 49
+VERSION = 3.1           TNOM    = 27           TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17       VTH0    = 0.6695207
+K1      = 0.8694489     K2      = -0.0917188   K3      = 25.6919711
+K3B     = -7.3653322    W0      = 1E-8         NLX     = 1E-9
+DVT0W   = 0             DVT1W   = 0            DVT2W   = 0
+DVT0    = 2.7518708     DVT1    = 0.4157316    DVT2    = -0.1405757
+U0      = 459.4342532   UA      = 1E-13        UB      = 1.522944E-18
+UC      = 1.874362E-11  VSAT    = 1.487444E5   A0      = 0.5981684
+AGS     = 0.1306288     B0      = 2.521977E-6  B1      = 5E-6
+KETA    = -4.514909E-3  A1      = 7.33129E-5   A2      = 0.4029659
+RDSW    = 1.564889E3    PRWG    = 0.027362     PRWB    = 0.0392247
+WR      = 1             WINT    = 2.520232E-7  LINT    = 3.653372E-8
+XL      = 0             XW      = 0            DWG     = -1.17306E-8
+DWB     = 5.311566E-8   VOFF    = -5.688886E-4 NFACTOR = 1.0780094
+CIT     = 0             CDSC    = 2.4E-4       CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0213525    ETAB    = -1.275836E-3
+DSUB    = 0.2490912     PCLM    = 2.5868986    PDIBLC1 = -0.2902944
+PDIBLC2 = 2.407506E-3   PDIBLCB = -0.0307296   DROUT   = 0.6175306
+PSCBE1  = 5.55857E8     PSCBE2  = 5.346571E-5  PVAG    = 0
+DELTA   = 0.01          RSH     = 82.4         MOBMOD  = 1
+PRT     = 0             UTE     = -1.5         KT1     = -0.11
+KT1L    = 0             KT2     = 0.022        UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11     AT      = 3.3E4
+WL      = 0             WLN     = 1            WW      = 0
+WWN     = 1             WWL     = 0            LL      = 0
+LLN     = 1             LW      = 0            LWN     = 1
+LWL     = 0             CAPMOD  = 2            XPART   = 0.5
+CGDO    = 2.07E-10      CGSO    = 2.07E-10     CGBO    = 1E-9
+CJ      = 4.190399E-4   PB      = 0.99         MJ      = 0.4442523
+CJSW    = 3.25452E-10   PBSW    = 0.1          MJSW    = 0.1159885
+CJSWG   = 1.64E-10      PBSWG   = 0.1          MJSWG   = 0.1159885
+CF      = 0             PVTH0   = 0.0362863    PRDSW   = -50.9170356
+PK2     = -0.0310644    WKETA   = -0.0155136   LKETA   = 2.178067E-3     )
*
.MODEL CMOSP PMOS (                                 LEVEL   = 49
+VERSION = 3.1           TNOM    = 27           TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17       VTH0    = -0.9287413
+K1      = 0.5450549     K2      = 9.985989E-3  K3      = 7.6456595
+K3B     = -0.6035863    W0      = 1E-8         NLX     = 1.676263E-8
+DVT0W   = 0             DVT1W   = 0            DVT2W   = 0
+DVT0    = 1.8819638     DVT1    = 0.5382275    DVT2    = -0.158632
+U0      = 218.8230822   UA      = 3.047014E-9  UB      = 1E-21
+UC      = -5.19775E-11  VSAT    = 1.752811E5   A0      = 0.8858636
```

```
+AGS      = 0.1542562      B0      = 5.925993E-7    B1      = 2.749323E-6
+KETA     = -3.260539E-3   A1      = 9.450969E-5    A2      = 0.3
+RDSW     = 2.987038E3     PRWG    = -0.0250945     PRWB    = 2.090247E-4
+WR       = 1              WINT    = 2.984848E-7    LINT    = 5.097201E-8
+XL       = 0              XW      = 0              DWG     = -1.762771E-8
+DWB      = 2.326045E-8    VOFF    = -0.068173      NFACTOR = 0.8423144
+CIT      = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB    = 0              ETA0    = 0.2336514      ETAB    = -0.0788196
+DSUB     = 1              PCLM    = 2.1941068      PDIBLC1 = 0.0489779
+PDIBLC2  = 3.799792E-3    PDIBLCB = -0.05041       DROUT   = 0.2314605
+PSCBE1   = 5.12196E9      PSCBE2  = 5E-10          PVAG    = 0
+DELTA    = 0.01           RSH     = 105.1          MOBMOD  = 1
+PRT      = 0              UTE     = -1.5           KT1     = -0.11
+KT1L     = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1      = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL       = 0              WLN     = 1              WW      = 0
+WWN      = 1              WWL     = 0              LL      = 0
+LLN      = 1              LW      = 0              LWN     = 1
+LWL      = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO     = 2.91E-10       CGSO    = 2.91E-10       CGBO    = 1E-9
+CJ       = 7.269487E-4    PB      = 0.9581537      MJ      = 0.4963302
+CJSW     = 2.719314E-10   PBSW    = 0.99           MJSW    = 0.3106279
+CJSWG    = 6.4E-11        PBSWG   = 0.99           MJSWG   = 0.3106279
+CF       = 0              PVTH0   = 5.98016E-3     PRDSW   = 14.8598424
+PK2      = 3.73981E-3     WKETA   = 5.032394E-3    LKETA   = -4.435939E-3    )
*
```

APPENDIX B. BASIC CURRENT MIRROR USED SEVEN LEVEL A/D CONVERTERS BASED ON CURRENT MULTIPLICATION TECHNIQUE

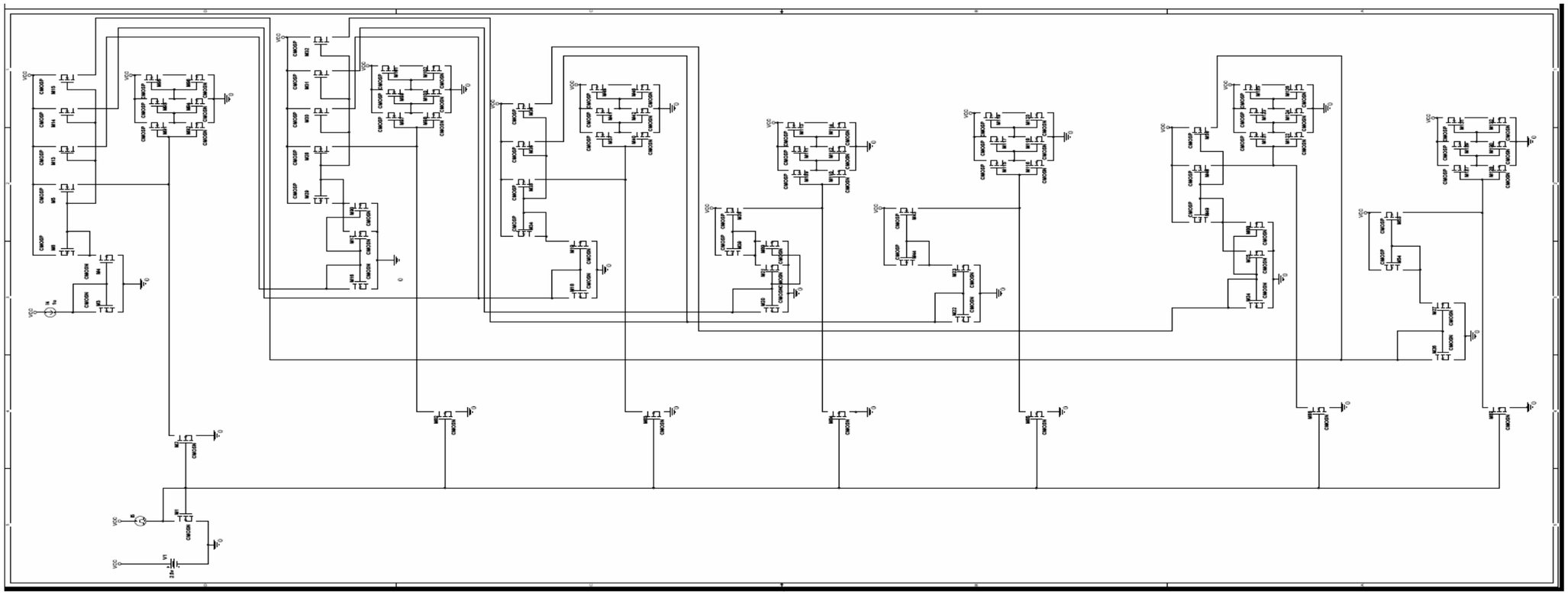

Figure Appendix: Basic Current Mirror used Seven Level A/D Converters based on Current Multiplication Technique

APPENDIX C. CASCADE CURRENT MIRROR USED SEVEN LEVEL A/D CONVERTERS BASED ON CURRENT MULTIPLICATION TECHNIQUE

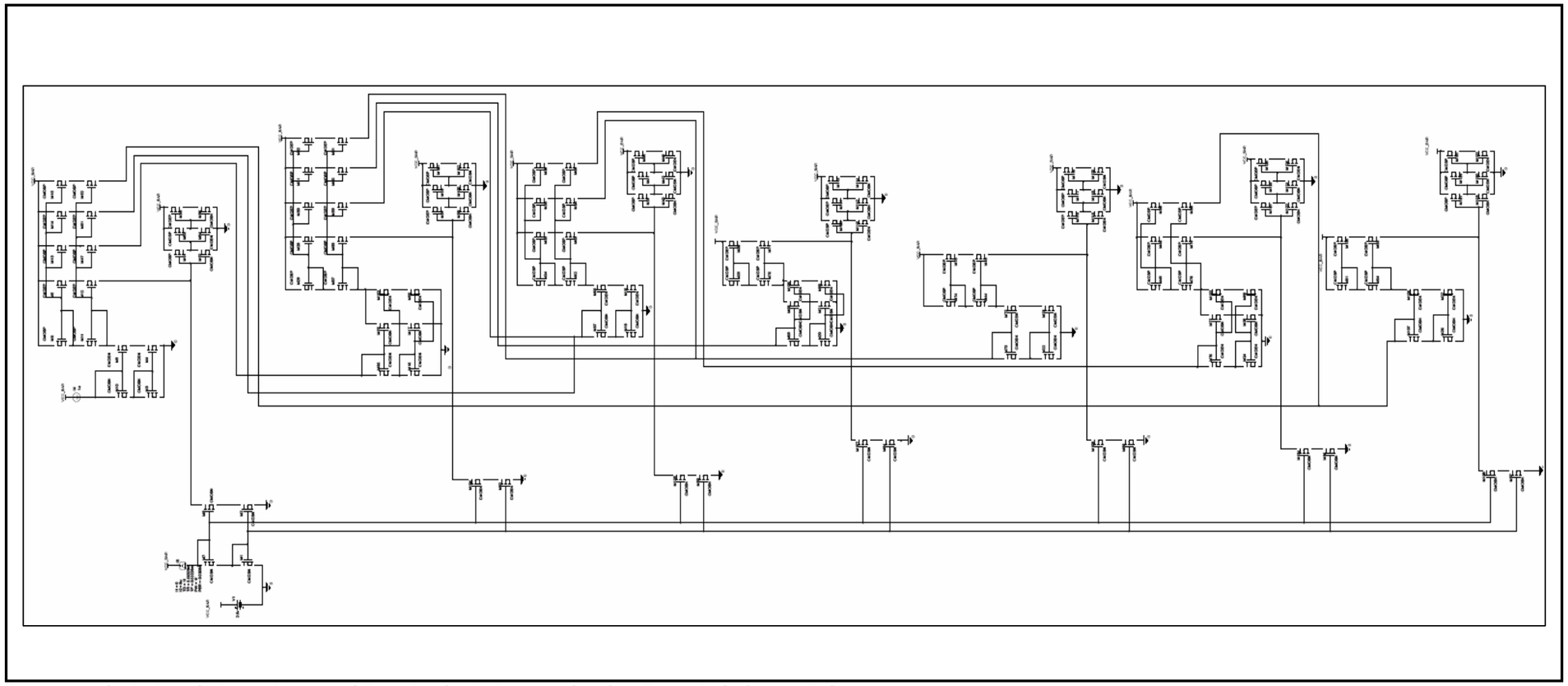

Figure Appendix B: Cascade Current Mirror used Seven Level A/D Converters based on Current Multiplication Technique

APPENDIX D. IMPROVED WILSON CURRENT MIRROR USED SEVEN LEVEL A/D CONVERTERS BASED ON CURRENT MULTIPLICATION TECHNIQUE

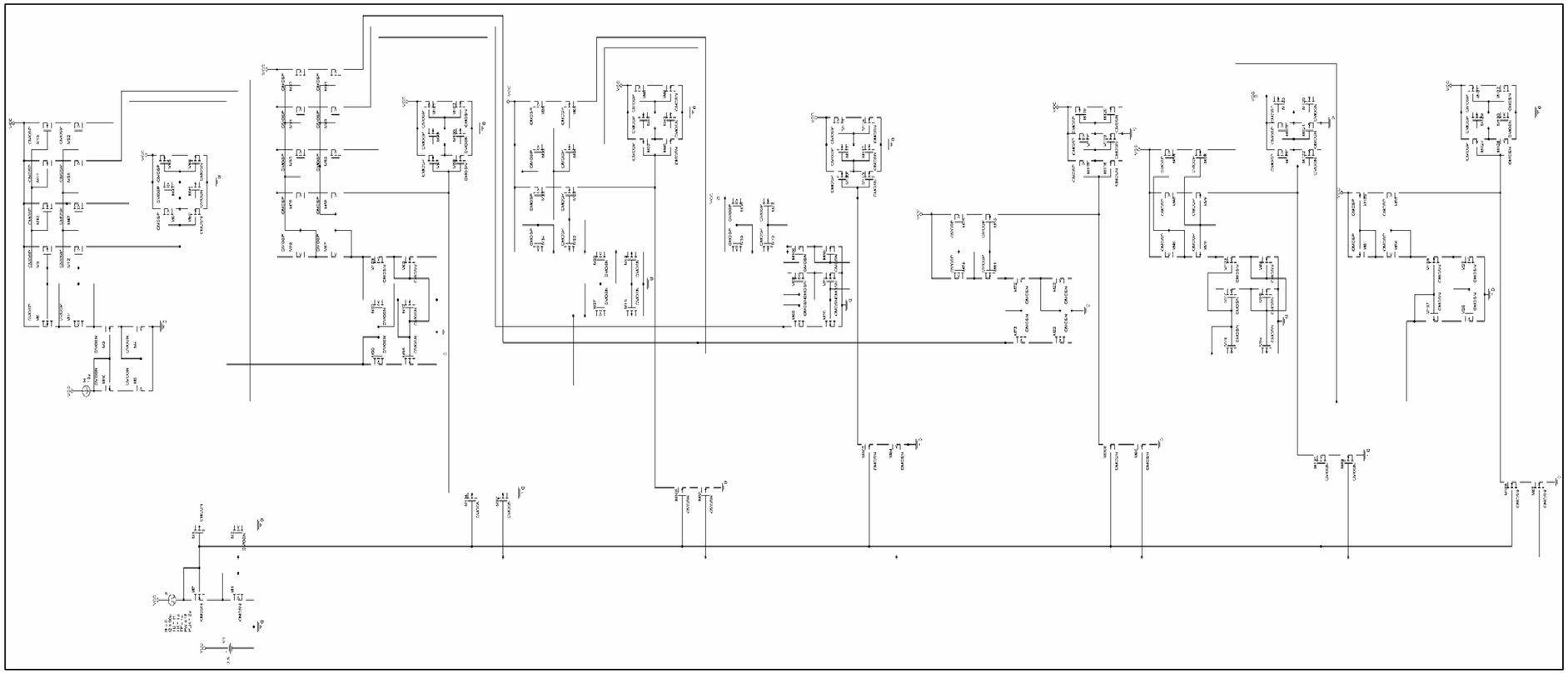

Figure Appendix D: Improved Wilson Current Mirror used Seven Level A/D Converters based on Current Multiplication Technique

APPENDIX E.1 BASIC CURRENT MIRROR USED SEVEN LEVEL A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

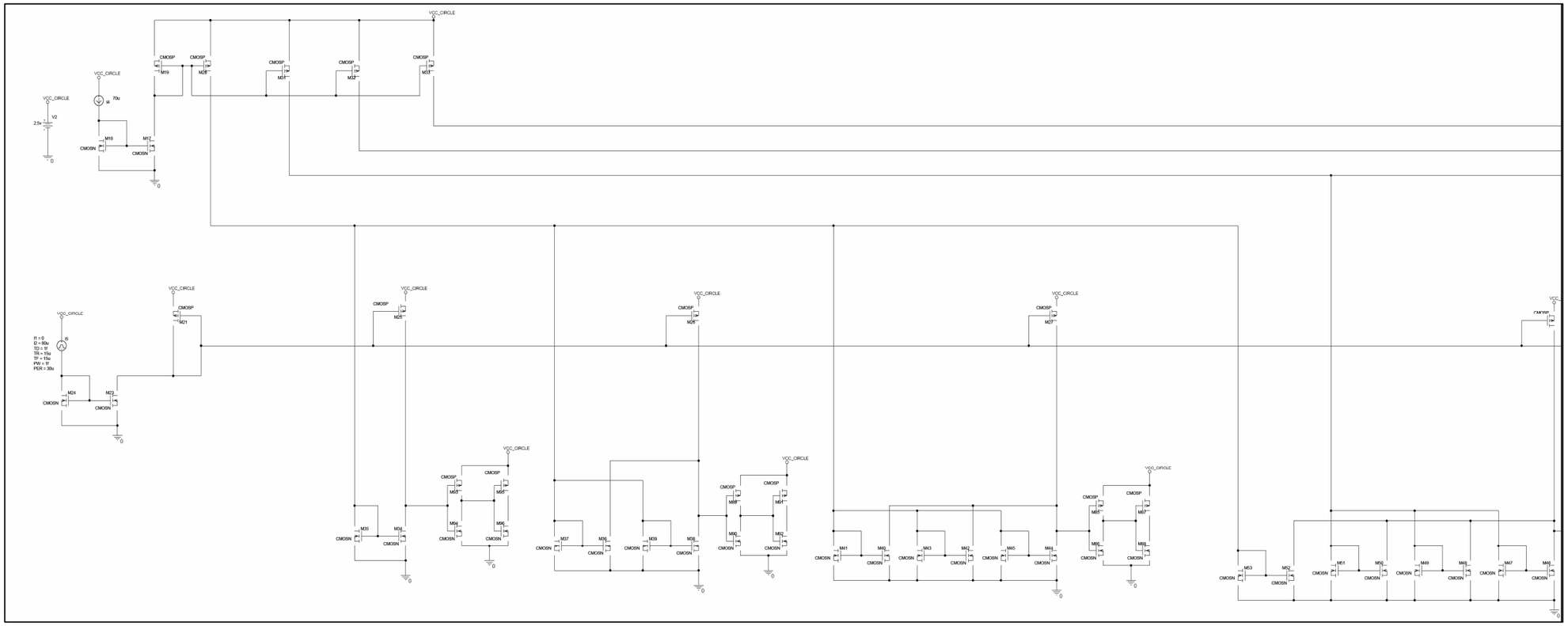

Figure Appendix E.1: Basic Current Mirror used Seven Level A/D Converters based on Current Division Technique

APPENDIX E-1 BASIC CURRENT MIRROR USED SEVEN LEVEL A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

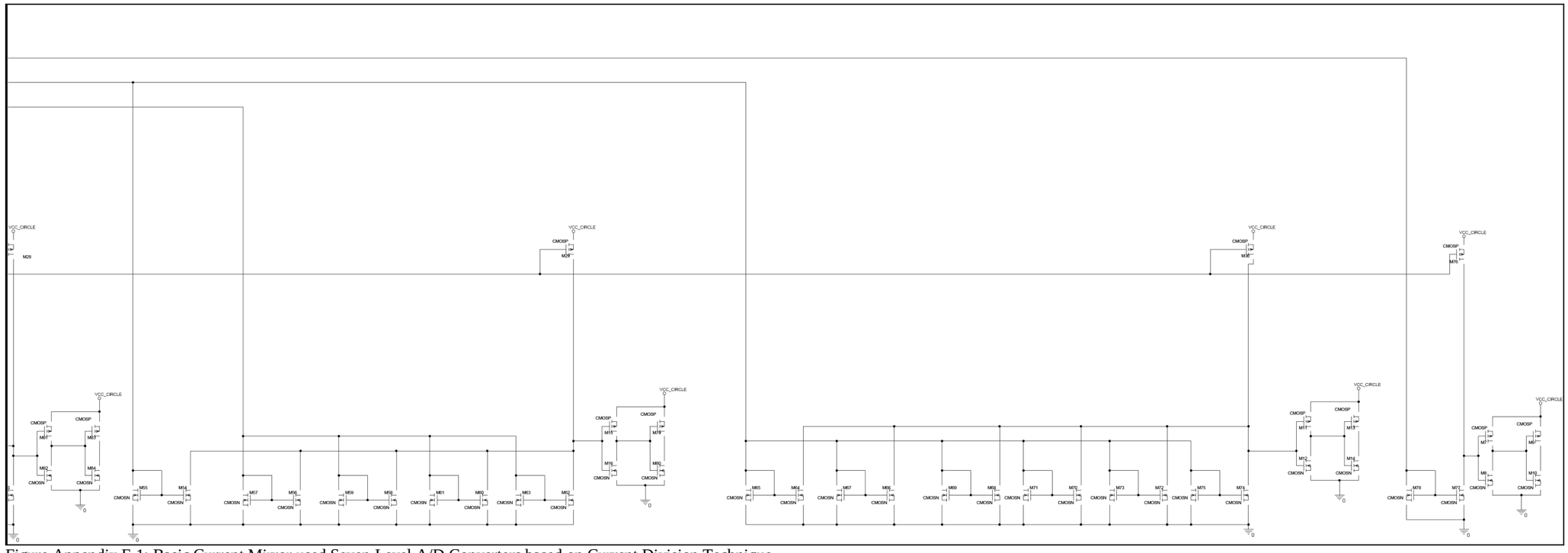

Figure Appendix E.1: Basic Current Mirror used Seven Level A/D Converters based on Current Division Technique

APPENDIX E-2 BASIC CURRENT MIRROR USED SEVEN LEVEL A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

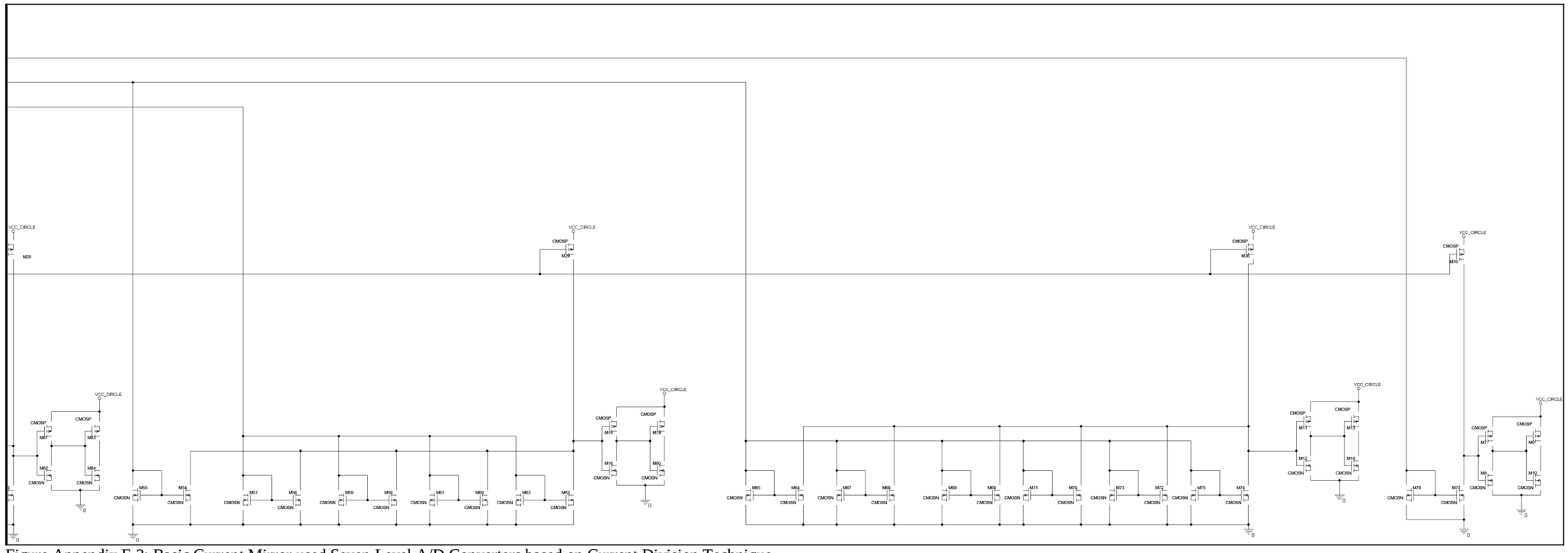

Figure Appendix E.2: Basic Current Mirror used Seven Level A/D Converters based on Current Division Technique

APPENDIX F.1 CASCADE CURRENT MIRROR USED SEVEN LEVEL ANALOG TO DIGITAL CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

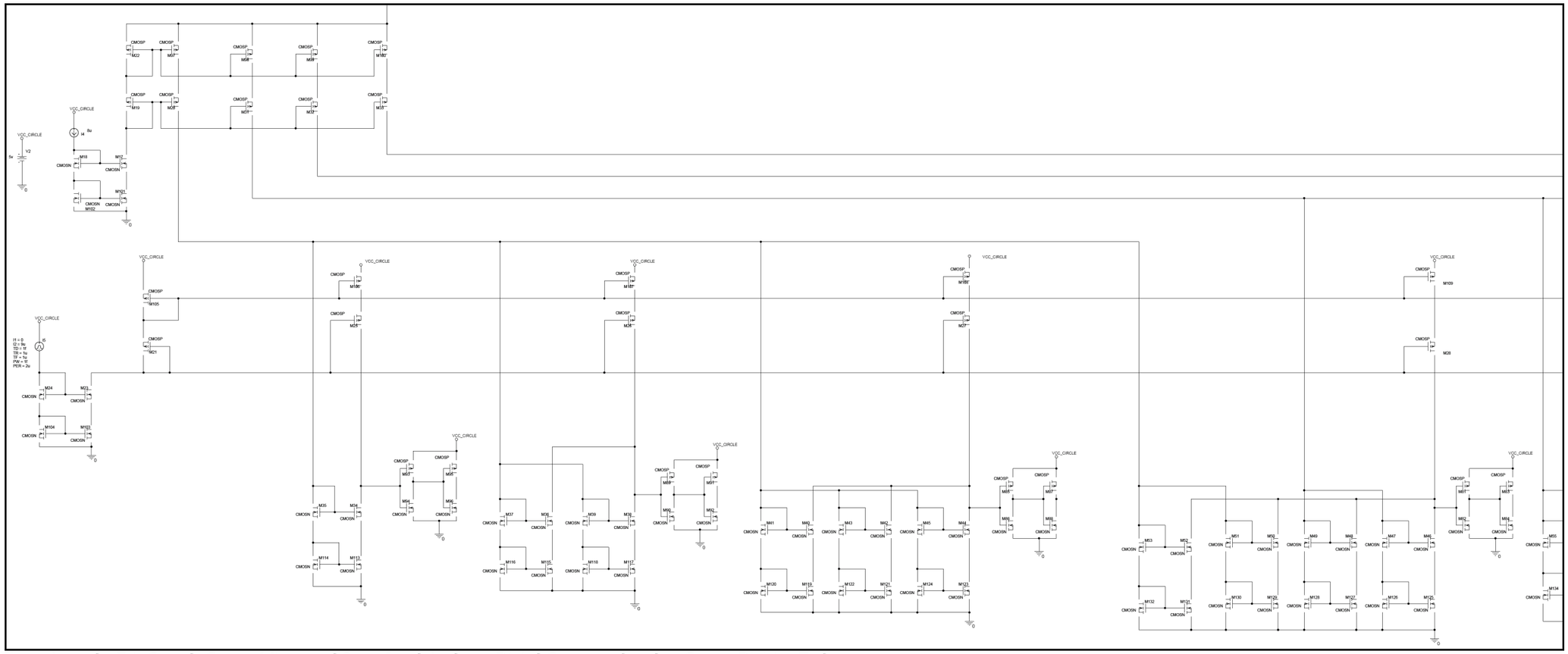

Figure Appendix F.1: Cascade Current Mirror used Seven Level Analog to Digital Converters based on Current Division Technique

APPENDIX F.2 CASCADE CURRENT MIRROR USED SEVEN LEVEL ANALOG TO DIGITAL CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

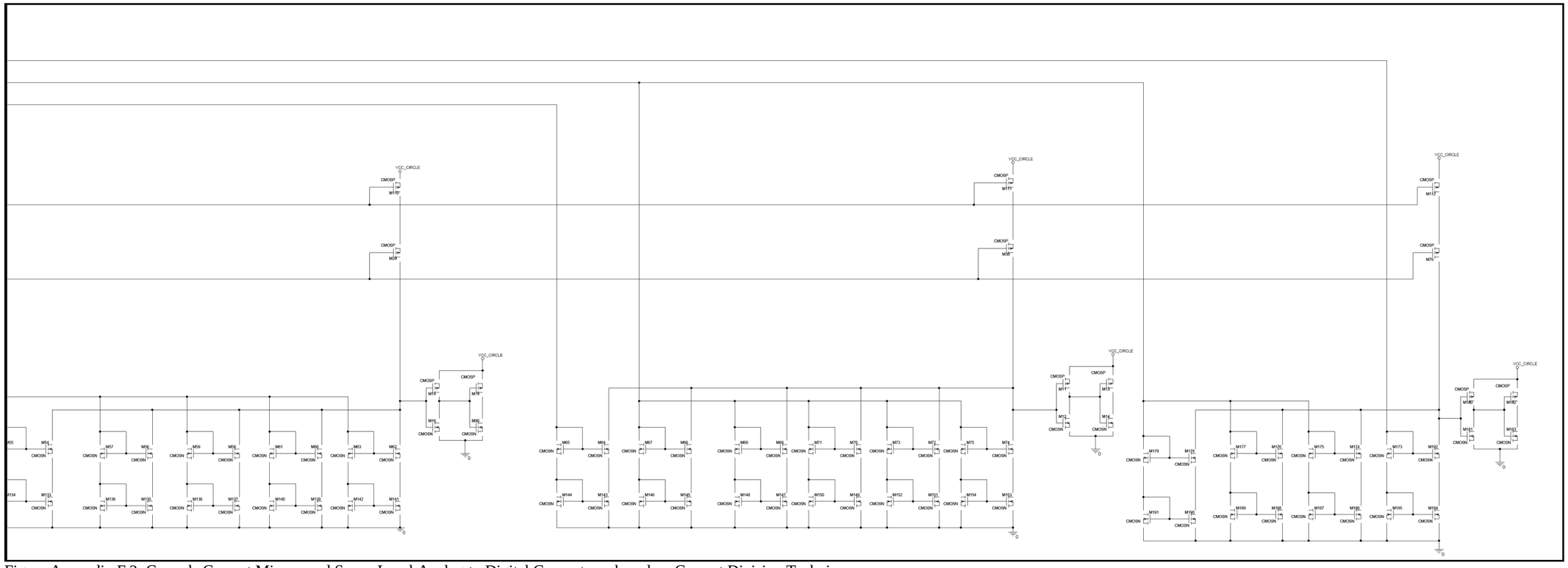

Figure Appendix F.2 :Cascade Current Mirror used Seven Level Analog to Digital Converters based on Current Division Technique

APPENDIX G.1 IMPROVED WILSON CURRENT MIRROR USED SEVEN LEVEL A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

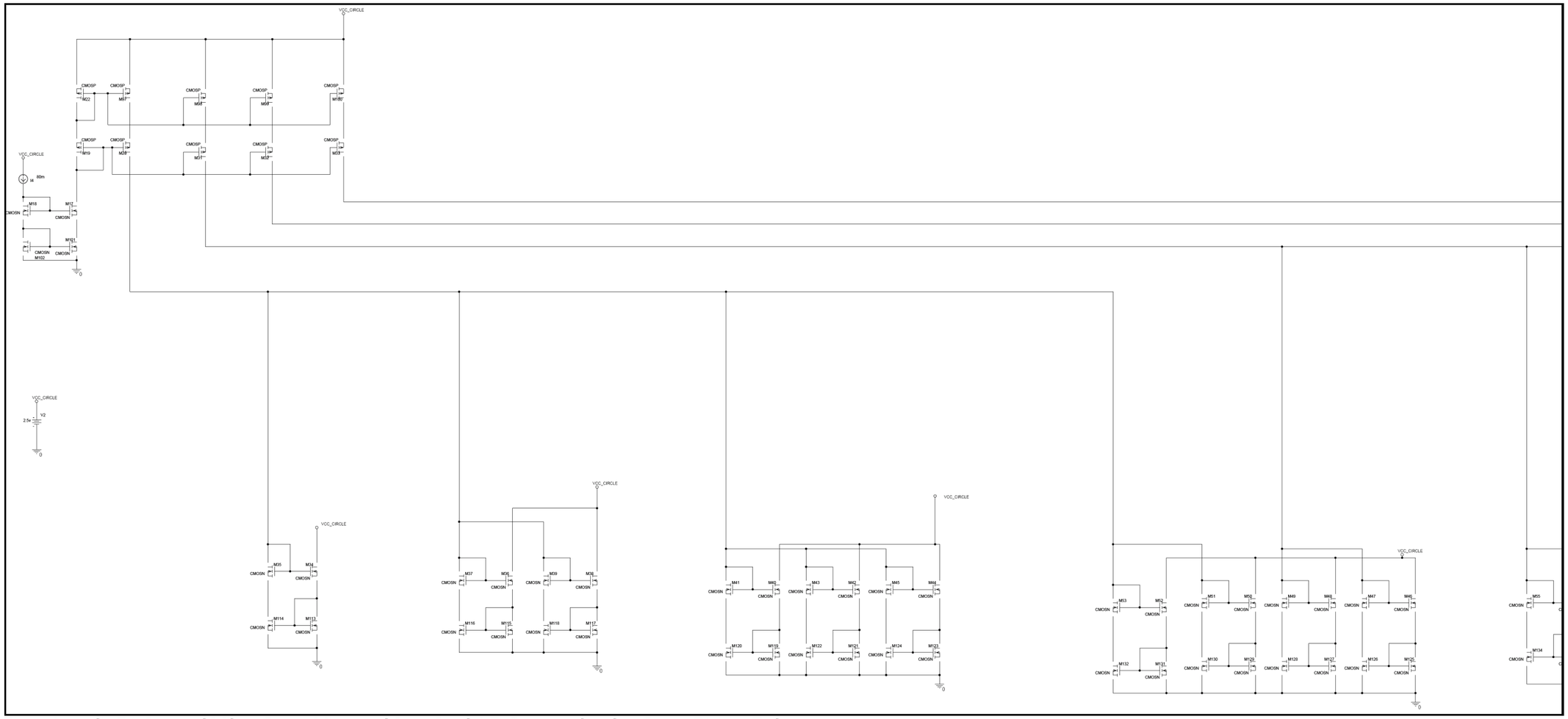

Figure Appendix F.1: Improved Wilson Current Mirror used Seven Level A/D Converters based on Current Division Technique

APPENDIX G.2 IMPROVED WILSON CURRENT MIRROR USED SEVEN LEVEL A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

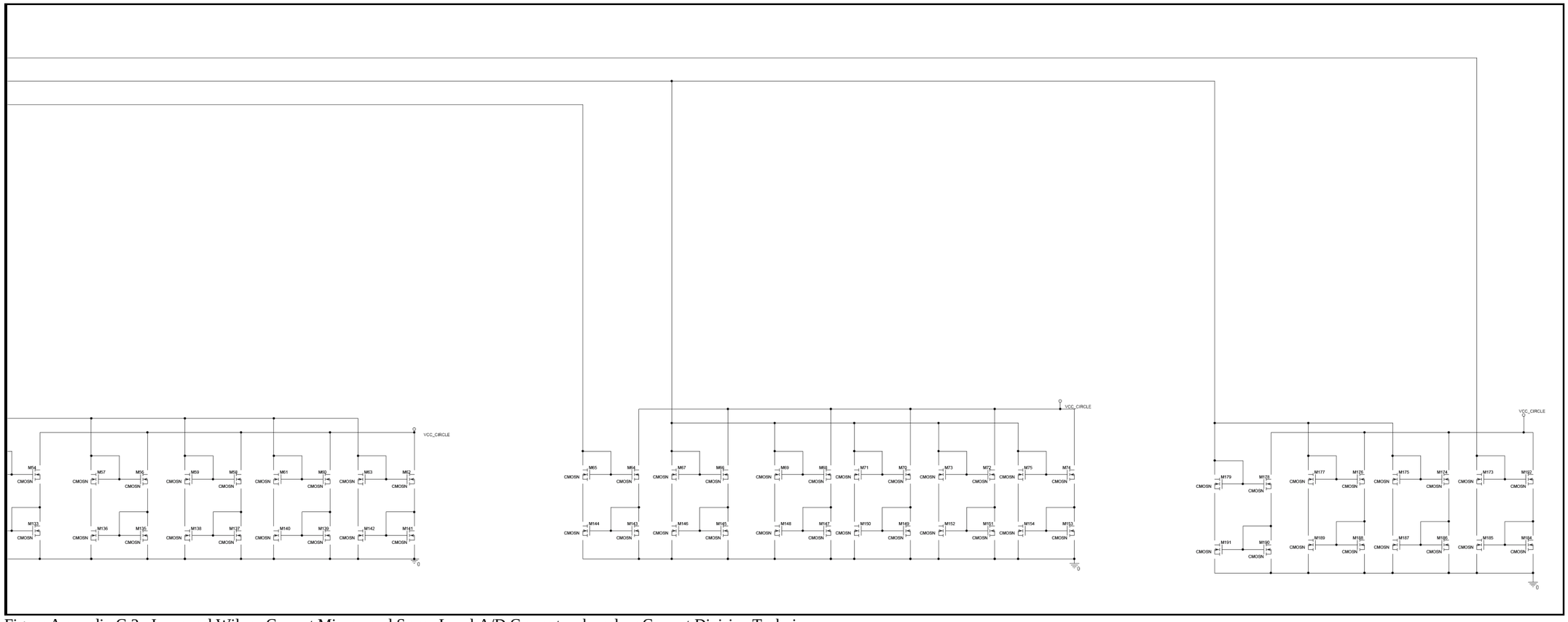

Figure Appendix G.2 : Improved Wilson Current Mirror used Seven Level A/D Converters based on Current Division Technique

APPENDIX H. BASIC CURRENT MIRROR USED EIGHT LEVEL A/D CONVERTERS BASED ON CURRENT MULTIPLICATION TECHNIQUE

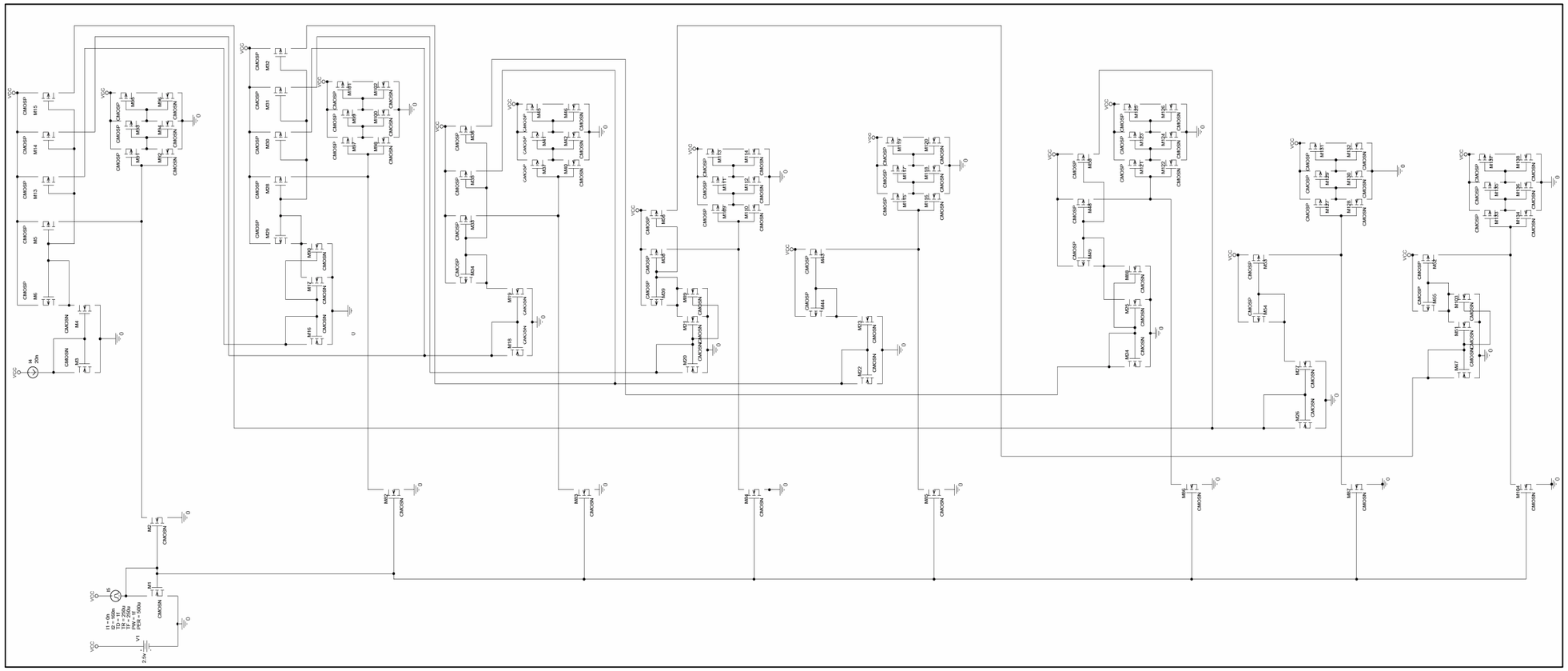

Figure Appendix H: Basic Current Mirror used Eight Level A/D Converters based on Current Multiplication Technique

APPENDIX I

CASCADE CURRENT MIRROR USED EIGHT LEVEL A/D CONVERTERS BASED ON CURRENT MULTIPLICATION TECHNIQUE

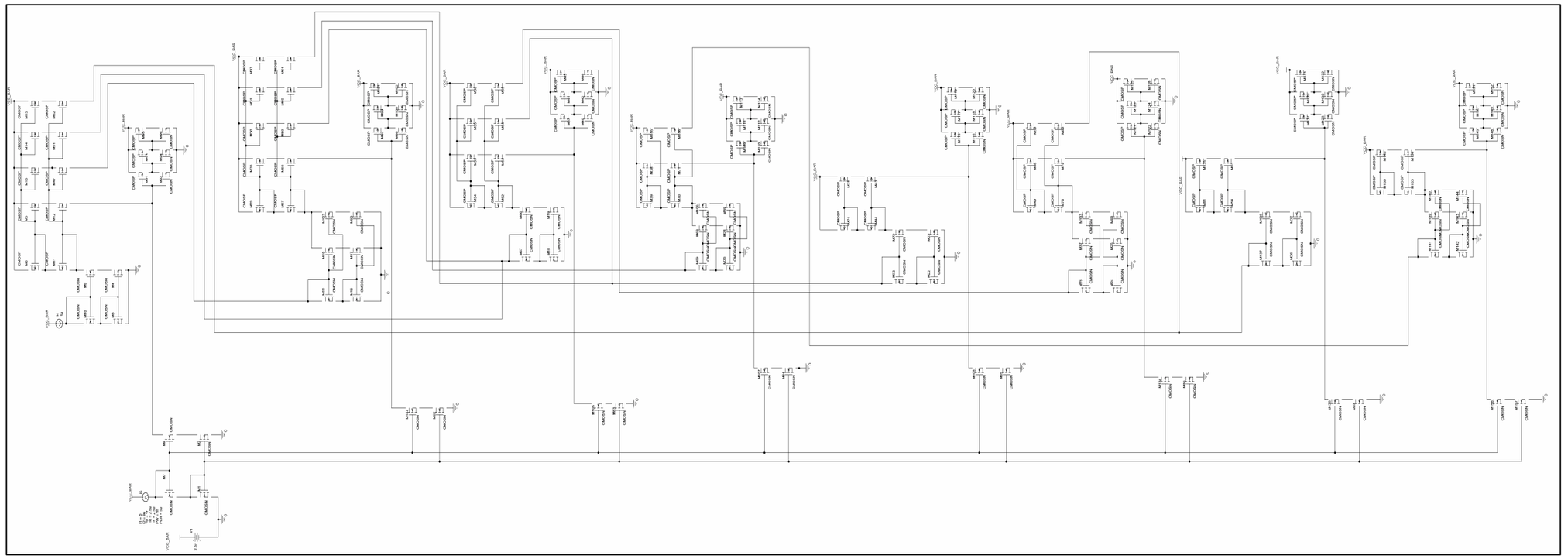

Figure Appendix I: Cascade Current Mirror used Eight Level A/D Converters based on Current Multiplication Technique

APPENDIX J

IMPROVED WILSON CURRENT MIRROR USED EIGHT LEVEL A/D CONVERTERS BASED ON CURRENT MULTIPLICATION TECHNIQUE

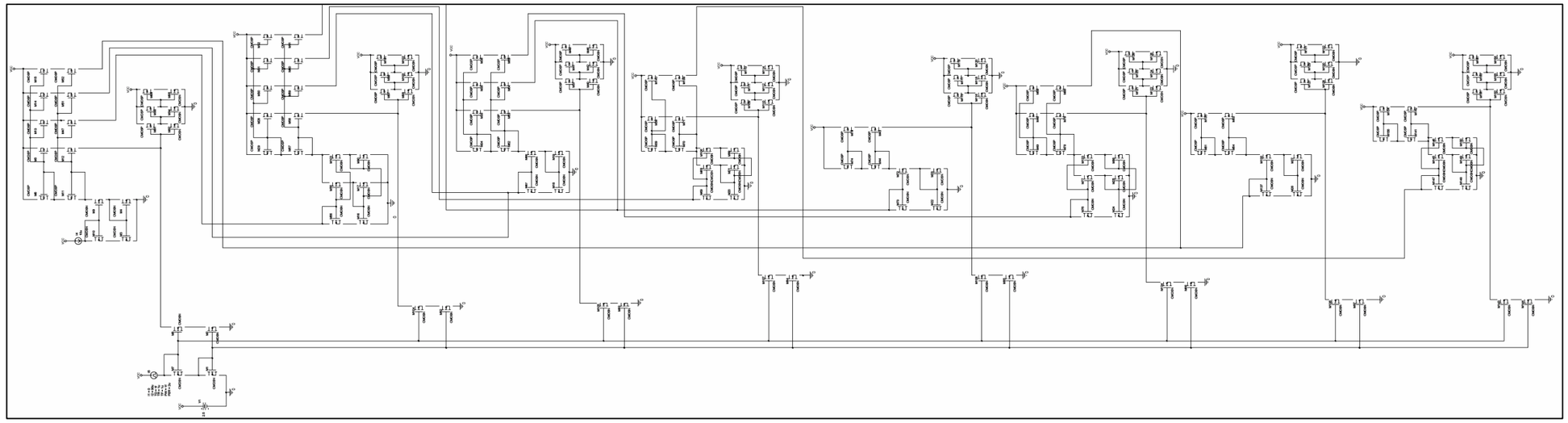

Figure Appendix J: Improved Wilson Current Mirror used Eight Level A/D Converters based on Current Multiplication Technique

APPENDIX K.1

BASIC CURRENT MIRROR USED EIGHT LEVEL A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

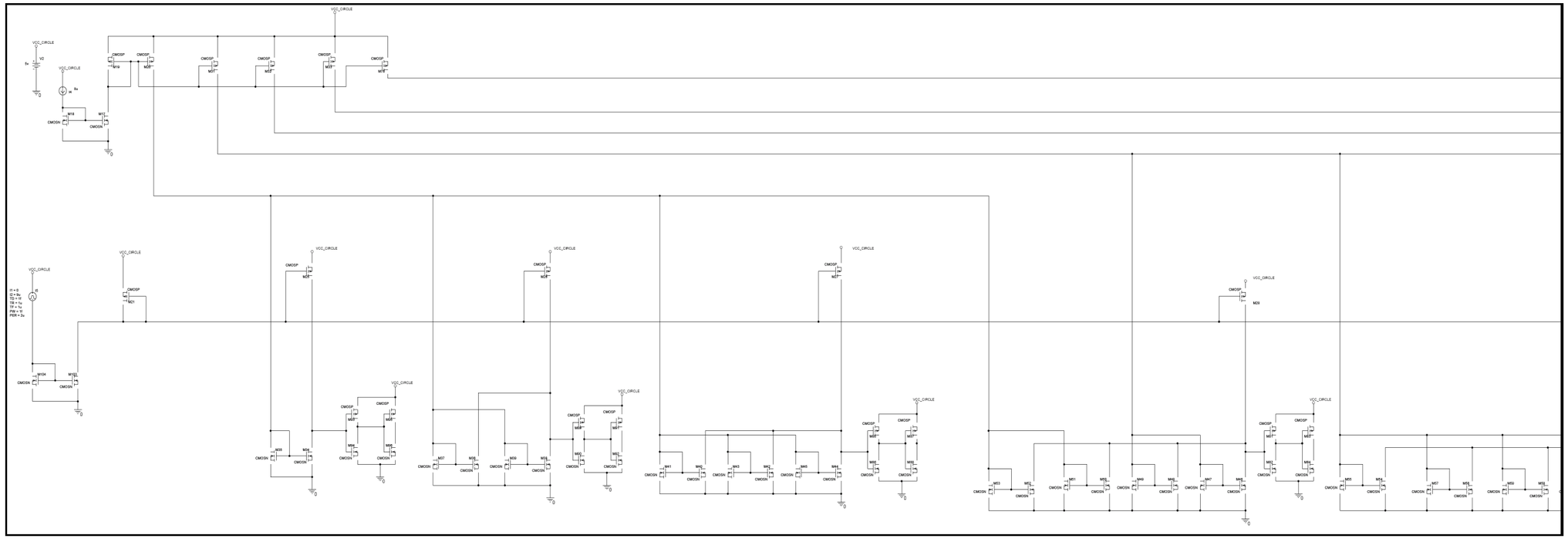

Figure Appendix K.1 : Basic Current Mirror used Eight Level A/D Converters based on Current Division Technique

APPENDIX K.2

BASIC CURRENT MIRROR USED EIGHT LEVEL A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

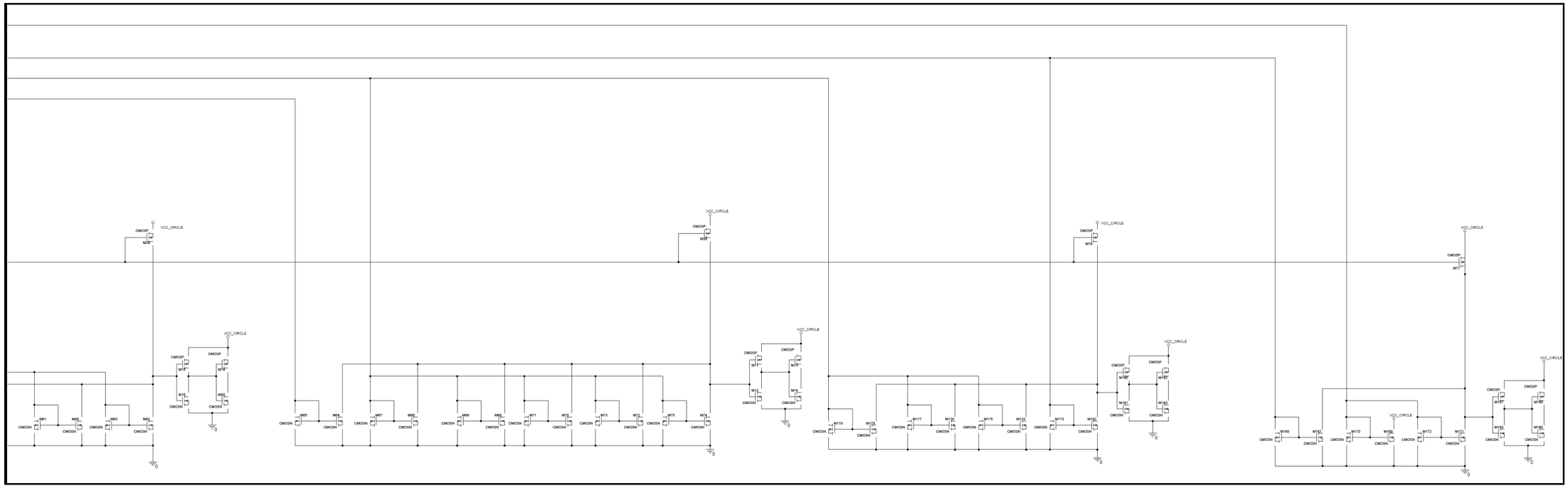

Figure Appendix K.2 : Basic Current Mirror used Eight Level A/D Converters based on Current Division Technique

APPENDIX L.1

EIGHT LEVEL CASCADE CURRENT MIRROR USED A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

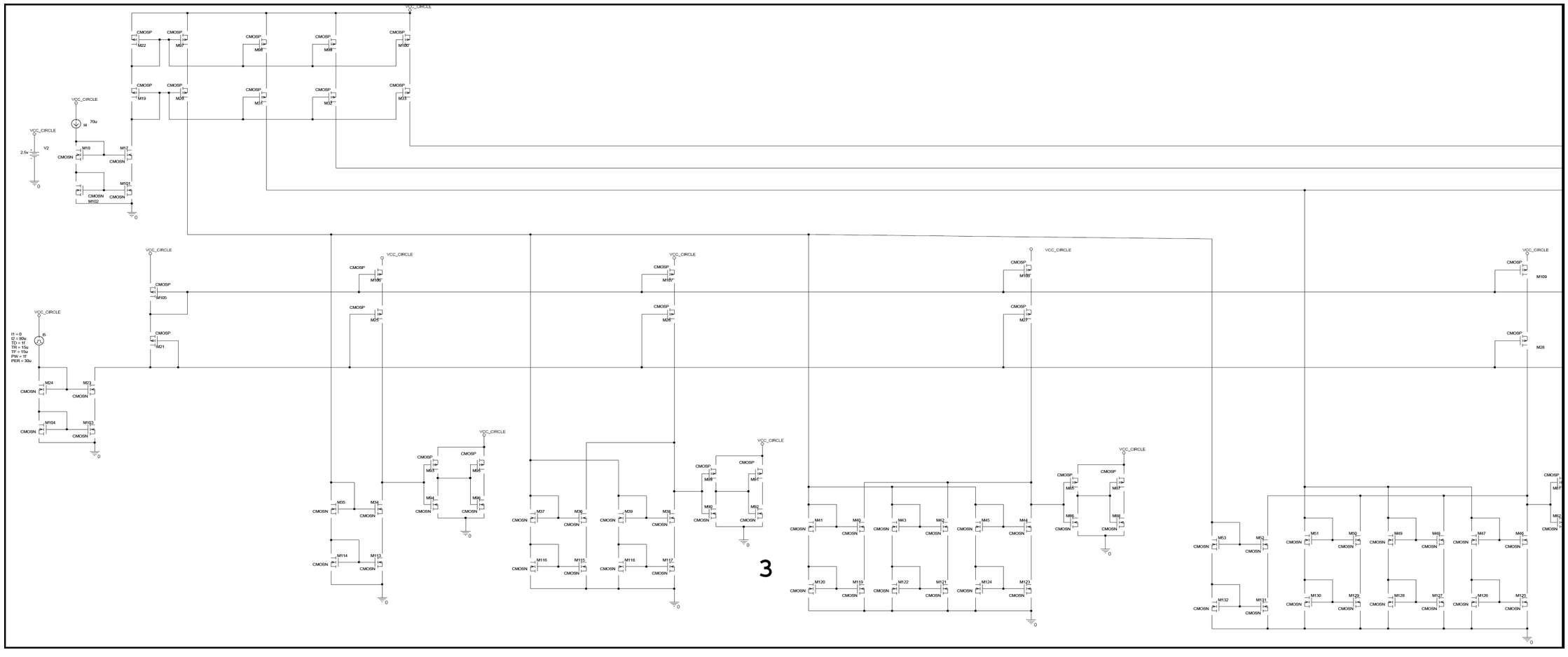

Figure Appendix L.1: Eight Level Cascade Current Mirror used A/D Converters based on Current Division Technique

APPENDIX L.2

EIGHT LEVEL CASCADE CURRENT MIRROR USED A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

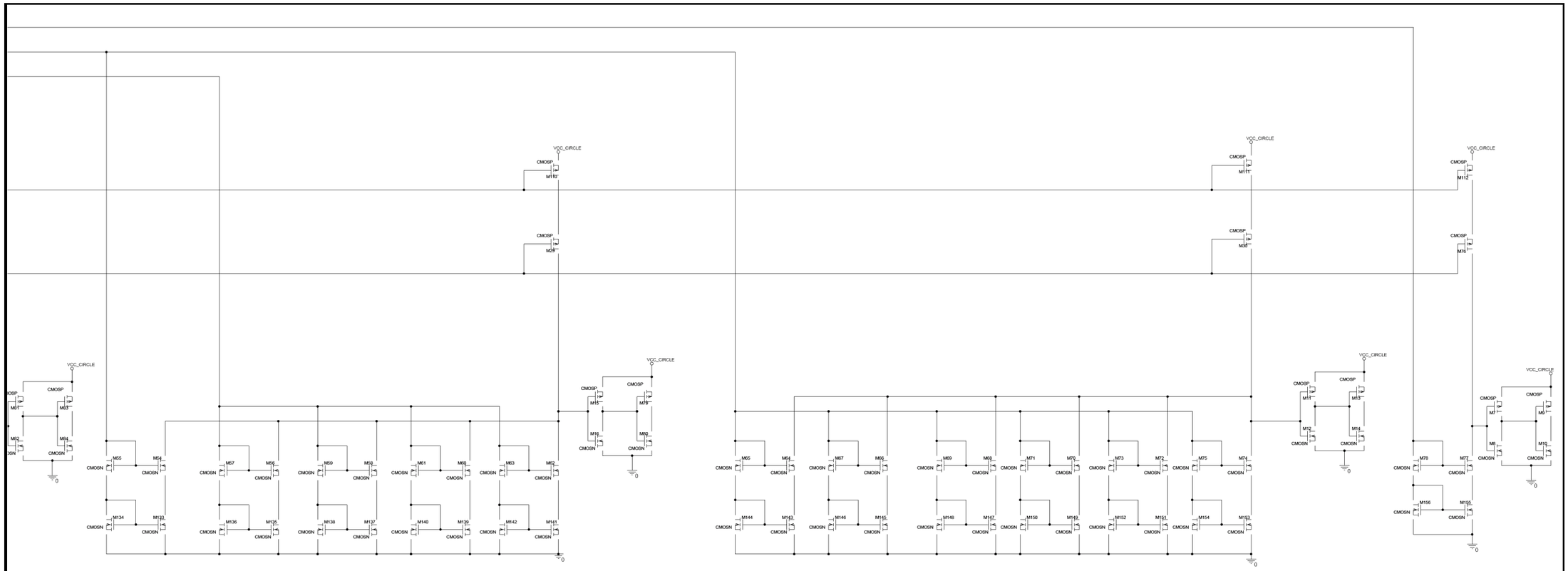

Figure Appendix L.2: Eight Level Cascade Current Mirror used A/D Converters based on Current Division Technique

APPENDIX M.1

**EIGHT LEVEL IMPROVED WILSON CURRENT MIRROR USED A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

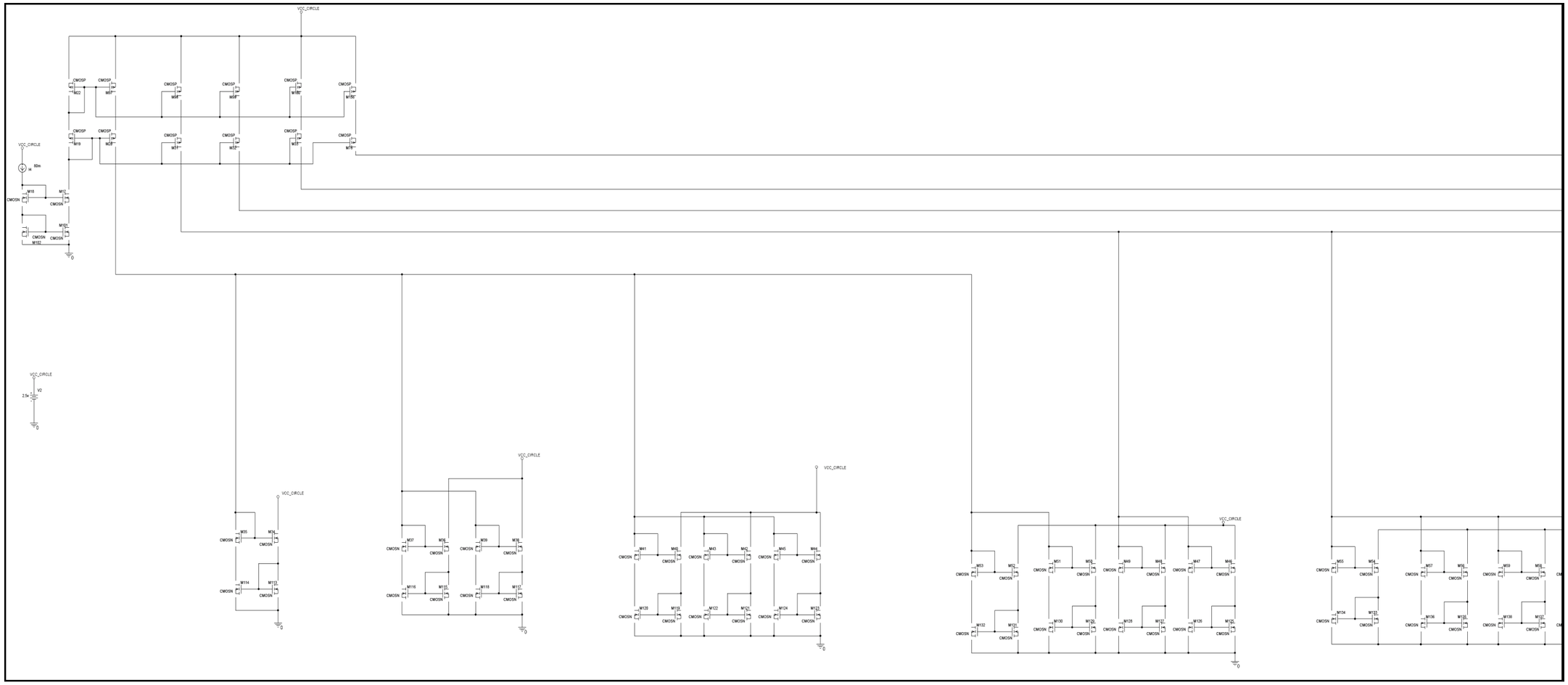

Figure Appendix M.1: Eight Level Improved Wilson Current Mirror used A/D Converters based on Current Division Technique

APPENDIX M.2

EIGHT LEVEL IMPROVED WILSON CURRENT MIRROR USED A/D CONVERTERS BASED ON CURRENT DIVISION TECHNIQUE

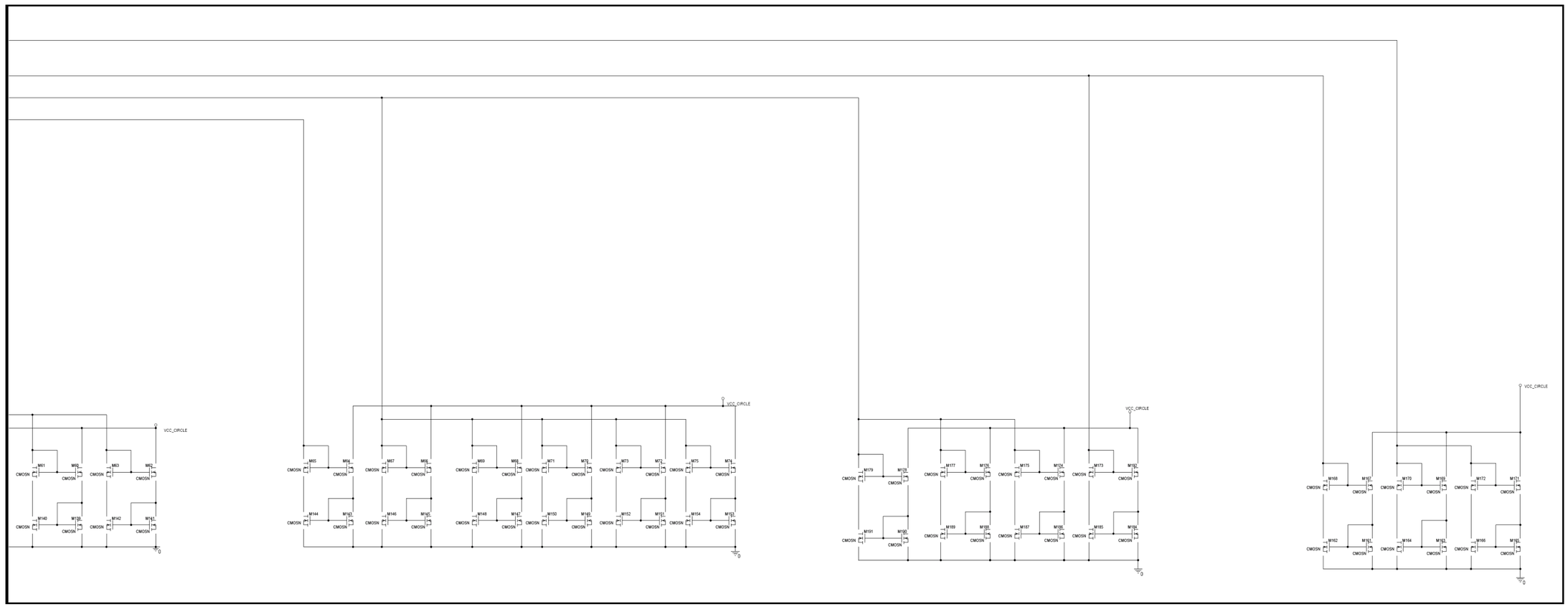

Figure Appendix M.2: Eight Level Improved Wilson Current Mirror used A/D Converters based on Current Division Technique