NEW ALGORITHM FOR JACQUARD CONTROL SYSTEMS AND ITS APPLICATIONS

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By

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ABSTRACT

NEW ALGORITHM FOR JACQUARD CONTROL SYSTEMS AND ITS APPLICATIONS

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In this thesis, to renew control systems and softwares of the current weaving machines existing in Gaziantep Industry is aimed. Therefore, the proper hardware to the contemporary technology has been produced and the software that supports this hardware has been regenerated.

The new software and hardware that have been produced solved many problems that current systems had and made them more contemporary and smooth.

As a first step, the type of the loom that this study has been applied on is Wilton, the brand of electronic jacquard that this loom uses is Takemura and its brand is Schöner. In the future work, this study will be able to be applied on Staubli brand electronic jacquards and Van de Wiele brand looms that use Bonas type electronic jacquards. Furthermore, this study with new features added will also be able to be applied on other weaving sectors (the weaving machines that have electronic jacquards) such as, towel, fabric, kilim etc..

Key words: Jacquard Control System, carpet weaving machine, Gaziantep Industry, carpet, Takemura, Schöner, Bonas, Staubli.

ÖZ

JAKAR KONTROL SİSTEMLERİ İÇİN YENİ ALGORİTMA VE UYGULAMALRI

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Bu tezde, şu an Gaziantep sanayisinde bulunan halı dokuma makinelerinin kontrol sistemlerinin ve yazılımlarının yenilenmesi amaçlanmıştır. Böylece, modern teknolojiye uygun donanım üretilmiş ve de bu donanımı destekleyen yazılımda yeniden oluşturulmuştur.

Yapılan yeni yazılım ve donanım, şu anki sistemlerde bulunan birçok eksik ve sorunlu noktayı çözüme kavuşturmuş ve de mevcut sistemleri daha modern ve sorunsuz hale getirmiştir.

İlk etapta, çalışmanın uygulandığı halı dokuma makinesinin tipi, Wilton, kullandığı elektronik jakar markası, Takemura ve de markası Schöner' dir. Bu çalışma, daha sonraki dönemlerde, Staubli marka elektronik jakar kullanan halı dokuma makinelerine ve de Bonas Marka elektronik jakar kullanan Van De Wiele marka halı dokuma makinelerine de uygulanabilecektir. Ayrıca, bu çalışma, eklenen yeni özelliklerle, havlu, kumaş, kilim vb. diğer dokuma sektörlerine de (dokuma makinesinde elektronik jakar bulunan) uygulanabilecektir.

Anahtar kelimeler: Jakar Kontrol Sistemi, halı dokuma makinesi, Gaziantep Sanayisi, halı, Takemura, Schöner, Bonas, Staubli

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Special thanks are due to my family, my mother, my father, my brother, my sister and my nieces for their never ending support and patience.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

In this chapter, a historical approach to the weaving is presented, development of weaving and its contribution to civilization are reviewed, invention and improvements of jacquard mechanism are briefly summarized. In the following sections, concept of electronic jacquards and selection boxes are introduced and introduction of jacquard control systems are given, the problems of current systems and need for this study, contribution of the study, flowing steps of the study are represented and finally, organization of the thesis is demonstrated.

1.2 History of Weaving

Weaving is the oldest art of mankind. Nobody knows how the concept of weaving began. The loom was created to hold the flexible materials rigid while being woven. The history of the loom goes back to the history of the man. The first looms were stakes in the ground with the fiber, also known as the warp, stretched between them. Looms gained more efficiency after the invention of heedle, a device which lifted each warp, or group of warps, thread. Lifting warp threads created a shed. A crosswise thread known as weft was passed through the shed. The weft was placed in a shuttle for convenience. Little else was done to automate the loom until the invention of the Jacquard Attachment. The jacquard loom impacted the world of weaving and even inspired the development of the personal computer [1].

The predecessor of the Jacquard loom, the draw loom, was invented in the East Asia. Primarily used for silk weaving places in Europe in the middle ages. The draw loom could produce intricately woven fabric. By raising individual warp threads, which

were gathered into groups, a pattern was created in the woven cloth. A cord was attached to each of these groups of threads and an assistant, called a draw boy, sat on the top of the loom and pulled the correct cords to create the pattern. The draw boy was told which cords to rise by a master weaver who sat at the loom threw the shuttle to create the woven material. Since draw boys could make mistakes, attempts were made to automate the work of the draw boy. In the 17th century a mechanical draw boy was invented. The mechanical draw boy allowed the assistant to stand on the floor instead of sitting on top of the loom. However, with the mechanical draw boy mistakes could still be made so a search began for an automatic mechanism, which would eliminate the need for an assistant by performing all of the functions of a draw boy. In 1725, a man named Basile Bouchon added a device called a selection process to the mechanical draw boy. A roll of paper, which was perforated according to the pattern to be woven, controlled the selection process. This device eliminated errors but still required an assistant. Other additions and improvements were made and in 1745, Jacques de Vaucanson mounted a selection box above the loom in which hooks, attached to individual heddles, passed through needles and were raised by a metal bar. This mechanism served as a foundation for the Jacquard attachment [4].

1.3 Process of Weaving

In general, weaving involves the interlacing of two sets of threads at right angles to each other: the warp and the weft (see Figures 1.1 and 1.2) The warp are held taut and in parallel order, typically by means of a loom, though some forms of weaving may use other methods. The loom is warped (or dressed) with the warp threads passing through heddles on two or more harnesses. The warp threads are moved up or down by the harnesses creating a space called the shed. The thread is wound onto spools called bobbins. The bobbins are placed in a shuttle which carries the weft thread through the shed. The raising/lowering sequence of warp threads gives rise to many possible weave structures from the simplest plain weave (also called tabby), through twills and satins to complex computer generated interlacings.

Both warp and weft can be visible in the final product. By spacing the warp more closely, it can completely cover the weft that binds it, giving a *warpfaced* textile such as rep weave. Conversely, if the warp is spread out, the weft can slide down and

completely cover the warp, giving a *weftfaced* textile, such as a tapestry or a Kilim rug. There are a variety of loom styles for hand weaving and tapestry. In tapestry, the image is created by placing weft only in certain warp areas, rather than across the entire warp width [2]. Figure1.1 and 1.2 show the warp and weft individually.

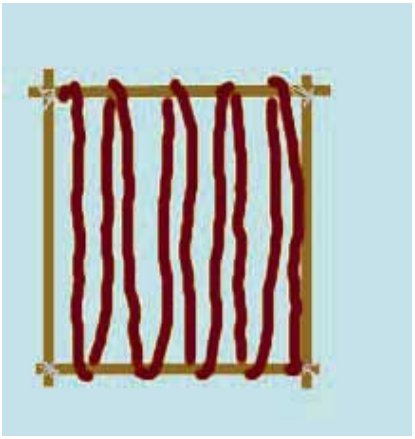


Figure 1.1 Warp

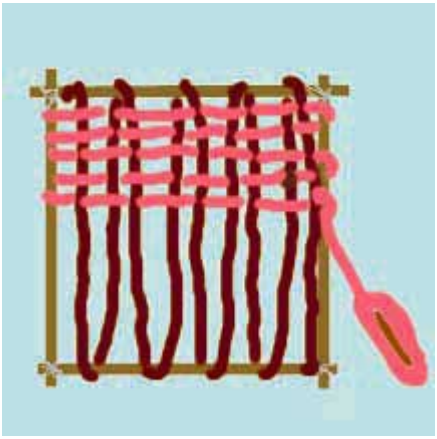


Figure 1.2 Weft

There are five basic mechanisms describing the total action of weaving. They are as follows;

a) Mechanism 1: The let off motion distributes the warp to the loom.
b) Mechanism 2: A warp shedding mechanism moves the warp yarn up and down according to the weave pattern.
c) Mechanism 3: Filling insertion system introduces the filling between the openings of the warp yarns (also called shed) carried out by the shedding mechanism.

Filling glass products are basically inserted with modern picking systems:

- Air jet
- Rapier
- Projectiles
- Needle (loom for narrow fabrics)

d) Mechanism 4: A reed moved by the beat up motion beats the filling between the warp yarns against the fabric in formation.

e) Mechanism 5: A Fabric take up regulates the filling density and the fabric is wound onto a tube on the loom or with a seperate winding device.

1.4 History of the Jacquard Automated Loom

In consequence of the Industrial Revolution, the late 18th century had witnessed a considerable expansion in the automation of processes that had once been the preserve of small groups of highly skilled workers employed in so-called `cottage industries'. The textile industry was one sphere were industrialization had rendered obsolete such skills. Whereas, prior to the development of mechanical looms and weaving machines, lengths of fabric had to be woven slowly by hand, the advent of powered tools for carrying out this task meant that quantities of fabric could be mass-produced at a far quicker rate than previously, thereby reducing its expense. There was one area, however, where the new machines could not compete with skilled manual workers. In the generation of cloth containing anything other than a plain (or at best extremely simple) woven pattern. The Jacquard Loom provided a solution to this problem so that, with it in use, extremely intricate patterns and pictures could be automatically woven into cloth at much the same rate as a plain length of fabric could be generated. Image a world where all clothes were made from a single cloth color?

The key idea behind Jacquard's loom was to control the action of the weaving process by interfacing the behavior of the loom to an encoding of the pattern to be reproduced. In order to do this Jacquard arranged for the pattern to be depicted as a group of holes punched into a sequence of pasteboard card. Each card contained the same number of rows and columns, the presence or absence of a hole was detected mechanically and used to determine the actions of the loom. By combining a tape of cards together the Jacquard loom was able to weave (and reproduce) patterns of great complexity, e.g. a surviving example is a black and white silk portrait of Jacquard woven under the control of a 10,000 card program. Jacquard's invention of the punched card is now recognized as important largely because of the influence it had on other developers of computing machinery utilizing his punch card concept [3].

1.5 Jacquard Attachment

In 1804, Joseph Marie Jacquard created the attachment to the draw loom which now bears his name, Jacquard worked in the silk weaving industry in Lyons, France. The attachment, placed on top of a loom, contained several important parts: harness cords, the hooks, the comber board, the weights, the cards, the square cylinder, and the needles (see Figure1.3).

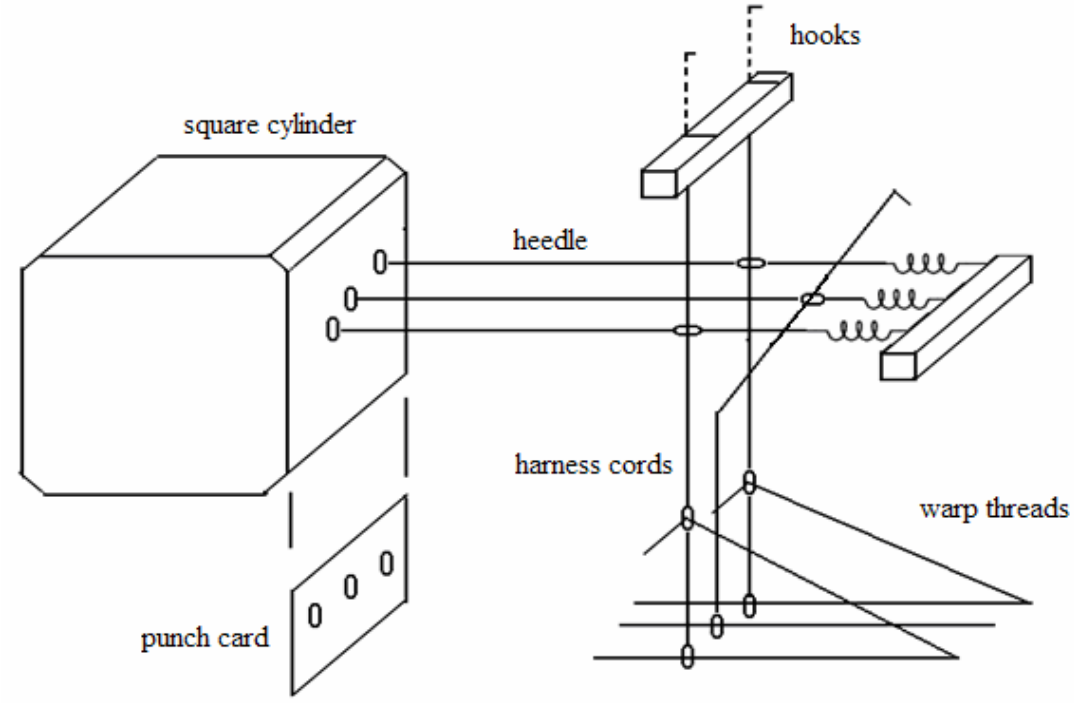


Figure 1.3 Schematic of jacquard mechanism

The harness cords were attached to each individual heddle containing a warp thread. These cords were suspended from the bottom of the hooks. The cords passed through a board, known as the comber board, which hung above the heddles and kept the harness cords in place. Weights were attached to the bottom of the heddles in order to keep them under tension. A series of cords were punched with the pattern, which was to woven. When there was a hole in the card, the needle went through the hole and raised the thread. There was one card for every weft thread used in the creation of the pattern. The square cylinder rotated one-quarter turn each time that the master weaver pressed the treadle. Intricate pattern could be created on the Jacquard loom

without the use of a draw boy. Each Jacquard mechanism should contain any number of hooks for the heddles. Some had about two hundreds, others over one thousand [4].

1.6 Impact of Jacquard Attachment

The creation of the Jacquard attachment had many consequences. Immediately after its invention, Joseph Marie Jacquard became unpopular since his invention put draw boys out of work. Not making any money on his invention, he slid into poverty. Eventually, Napoleon awarded him a pension on the condition that all of his patients would revert to the city of Lyons. At one point, Jacquard had to flee Lyons for his life and his looms were destroyed. In 1826 the first Jacquard loom came to America. Many housewives quit weaving at home and sent their wool to the weaving mill to be woven in fancy patterns on a Jacquard loom. The Jacquard looms eventually became widely accepted and many are still used in textile mills today. Besides the immediate effects of Jacquard's invention on weaving, the invention influenced the makers of the first computer. The Jacquard attachment is a computer in the sense that it uses a binary system to create woven designs. The same binary system appears in computers in the forms of 1s and 0s. In the Jacquard attachment the holes correspond to "1s" and the places without holes correspond to "0s". The cards act as a program telling the loom which threads to rise to create the pattern. Charles Babbage, in 1842, used a system of punch cards similar to Jacquard's the basis of operation for his calculating engine. Babbage's calculating engine was considered as the first mechanical computer. His engine influenced Hermann Hollerith who built a punch card to process the 1890 United States Census. Holllerith started his own company called the Hollerith Tabulating Company, which eventually became IBM [5].

The history of the Jacquard loom was as complex as machine itself. Jacquard improved upon inventions, which came before him and created a machine, which would influence many generations that followed. The Jacquard loom did nothing that could not be done with more difficulty on the draw loom. Jacquard's attachment was a simply substitute for the strenuous job of a draw boy. Still, Jacquard's invention was a major step toward the automation found in today's textile mills and it inspired designers of the first computers with its use of a punch card system of information

storage [4]. Figure 1.4 shows the Punch Card Loom of 19th century, from the collection of science museum, London. Figure 1.5 is a Punch Card Loom of 18th century, from Deutsches Museum, Munich.

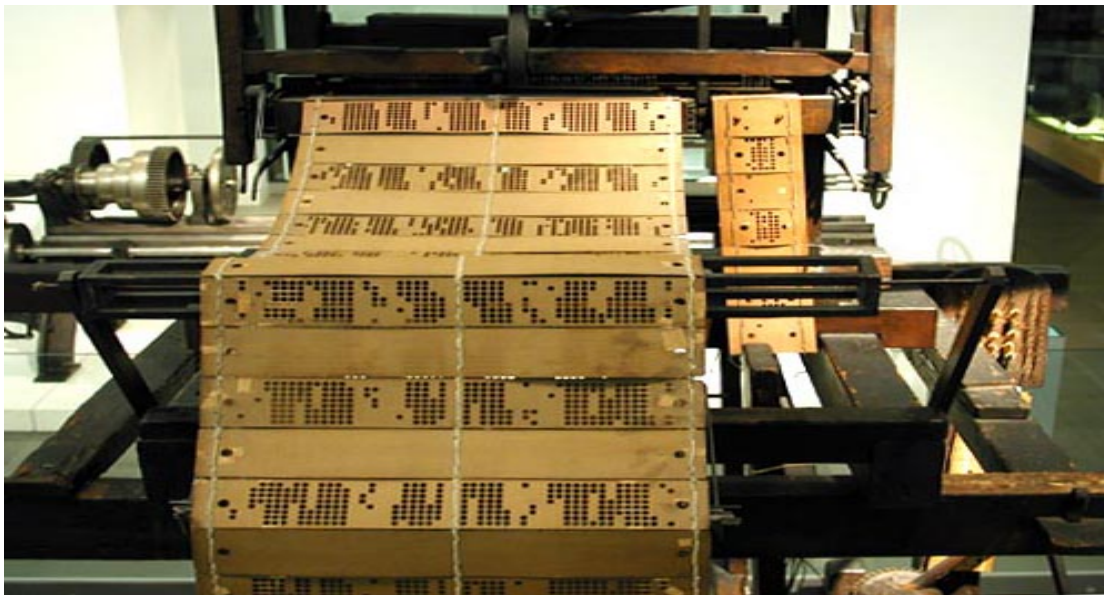


Figure 1.4 Punch card mechanism

Figure 1.5 Punch card loom

1.7 Electronic Jacquards

The term "Jacquard" is not specific or limited to any particular loom, but rather refers to the added control mechanism that automates the patterning [6].
By the introduction of the jacquard mechanism, controlled by a computer, rate and capacity of the looms are considerably increased. Pattern change becomes a pure software issue. This allows more flexibility in the production. Electronic jacquard mechanism has replaced classical punch pattern feeding mechanism by a roller mechanism. In this mechanism the yarn threads are directly controlled; the mechanical efficiency is very high when compared with that of the classical jacquard mechanism [4]. Figure 1.6 shows a carpet loom with electronic jacquard

Bonas Machine Company Ltd. launched the first electronic Jacquard at ITMA, Milan in 1983. Although the machines were initially small, modern technology has allowed Jacquard machine capacity to increase significantly, and single end warp control can extend to more than 10,000 warp ends. This avoids the need for repeats and symmetrical designs and allows almost infinite versatility. The computer-controlled machines significantly reduce the down time associated with changing punched paper designs, thus allowing smaller batch sizes. However, electronic Jacquards are costly and may not be required in a factory weaving large batch sizes, and smaller designs. The larger machines allowing single end warp control are very expensive, and can only be justified where great versatility is required, or very specialized design requirements need to be met. For example, they are an ideal tool to increase the ability and stretch the versatility of the niche linen Jacquard weavers who remain active in Europe and the West, while most of the large batch commodity weaving has moved to low cost areas.

Linen products associated with Jacquard weaving are linen damask napery, Jacquard apparel fabrics and damask bed linen.

Jacquard weaving of course uses all sorts of fibers and blends of fibers, and it is used in the production of fabrics for many end uses. Research is under way to develop layered and shaped items as reinforcing components for structures made from composite materials [6].

Figure 1.6 A carpet loom with electronic jacquard

1.8 Selection Box (SB)

Selection box is collection of soleneoids. It replaces the punch card mechanism into PC controlled electronic jacquard mechanism. Each hole position in the punch card is assigned to a certain solenoid, thus forming a matrix of soleneoids. Selection box in the electronic jacquard mechanism would have exactly the same function as the punch card in a punch card mechanism. The prime difference is that the solenoid matrix is driven by a PC to feed the pattern to the jacquard mechanism [4]. Since selection boxes are the parts of electronic jacquards where the electrical signals are transformed to mechanical movements. They can be called as the *heart* of electronic jacquards. More detailed information about selection boxes and solenoids will be given for understanding the working principles of an electronic jacquard.

1.8.1 Selection Box Types

Selection Boxes are sized according to size and type of a loom on which the SBs are to be attached. Some selection boxes do not base on solenoids matrix technology. They adopt *Bimorph Actuators* that means actuators utilizing Piezoelectric material in order to achieve small displacement under electric potential in place of conventional solenoids. With those selection boxes, high speed and more stable operation is ensured.

SBs are classified according to their paper fed systems. They are namely for endless paper, cut paper and vincenzi types. They are highlighted shortly in following sections [4].

1.8.1.1 Selection Boxes for Endless Paper

They are attachable to any type of jacquard loom for endless paper. They are also attachable to high speed jacquards with a running speed of more than 400 rpm. They exhibit their best performance especially when attached to looms (for carpets, curtains and raschel lace for endless paper) containing more than one jacquard [4]. Figure 1.7 shows a selection box for endless paper. Connections of solenoids to a selection box for endless paper can be seen in Figure 1.9.

1.8.1.2 Selection Boxes for Vincenzi Pitch

They are only systems in the world that are attachable to jacquards with the vincenzi pitch (4mm) they are widely used through the world, especially for jacquard weaving and carpets. They are conveniently designed in such a manner that one controller (PC) controls more than one head. They are best suited for piece types of carpet having symmetrical patterns.

In coordination with CAD, weaving of specially ordered carpets with full repeat patterns can be performed immediately [4]. Figure 1.7 shows a selection box vincenzi pitch.

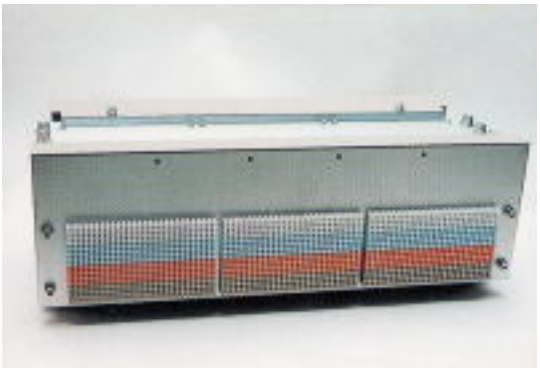


Figure 1.7 Selection box for endless paper

Figure 1.8 Selection box for vincenzi pitch

Figure 1.9 Connections of solenoid cards on a connector box installed on a selection box for endless paper

1.8.1.3 Selection Boxes for Cut Paper

They are attachable to any type of jacquard loom for cut paper. They provide easier maintenance. Needles size ranges from 400 to 1320. Figure 1.10 shows a selection box for cut paper [4].

Figure 1.10 Takemura jacquard for cut paper

1.9 Jacquard Control System

It is the general name of the system including electronic cards and the control unit that transfers the design information to the jacquards in respect of the software generated before and existing in the industrial PC. Figure 1.11 shows the schematic view of a Jacquard Control System. Processing steps of any jacquard control system are;

1- Desired design is generated by the designators by using any design software and save as bitmap (BMP) format.
2- Design generated by the designators are converted to the format that jacquard controller utilizes, by using other softwares.
3- Converted design data is loaded to the jacquard controller by using floppy disks or a special type of magnetic disk called as “zip disk” that may have capacity up to 100 MBs.
4- Design datas are transmitted to the jacquard driver and by the help of the transformation of electrical signals to mechanical movements in solenoids existing in selection boxes, weaving process realizes.

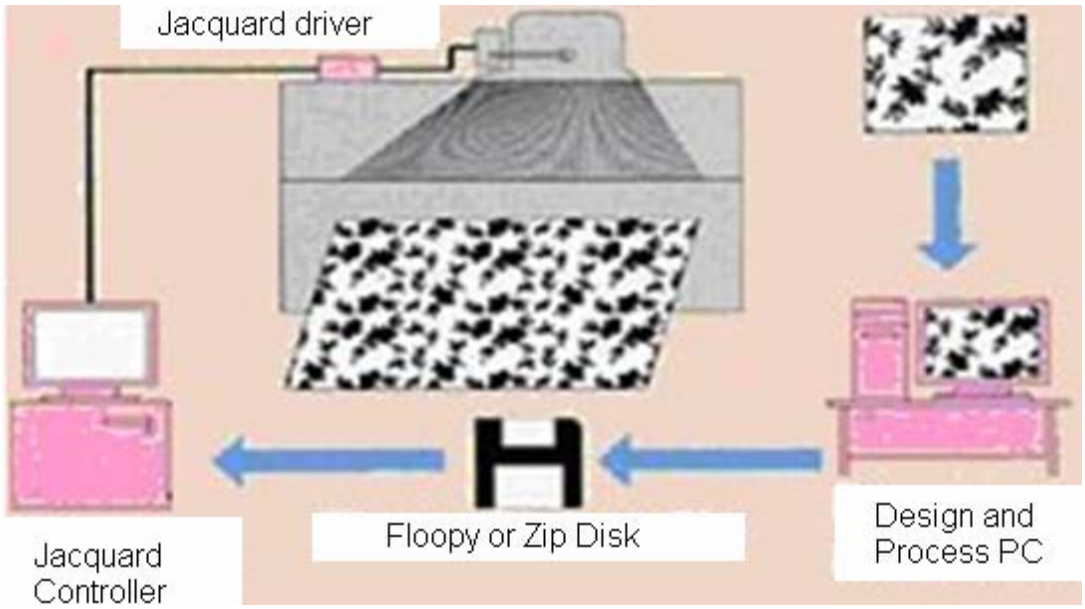


Figure 1.11 Schematic view of a Jacquard Control System

Different looms that use jacquard control systems can be seen in Figures 1.12 and 1.13.

Figure 1.12 Schleicher Jacquard

Figure 1.13 Van De Wiele with Bonas Jacquard

1.10 The Problems of Current Carpet Looms and Needs for This Study

Although the textile industry contributes great to the global income in Turkey, it is not a level which matches full capacity of the country. Cotton is a prime material of textile products. Turkey has a considerable manufacturing potential of cotton. An important portion of our export are the textile products. There are thousands of middle-sized firms operating in the sector. They contribute considerably to our annual income.

In textile machinery, our country is strongly dependent upon the abroad. Machines with latest technology are hard to install because of financial problems and infra structure of the sector. They are very expensive for most of the producers. Great portion of the production is still carried out with the existing conventional machines. They have, of course, very old technology. This situation causes the firms produce with less quality and in turn loss their position in the market. They are not able to compete with foreign vendors using high technology machines. In order to overcome this problem, textile machines still in production must either be replaced with new

ones or be brought to the latest technological level. This must be performed at an expense of minimum resources.

Exporting new machines with the latest technology requires high amount of capital. Most of our firms are not able to invest so much on the machines, simply because they can not afford such an investment. On the other hand, the option of modernization of existing machines is open. Especially in the textile machine, where the latest technological development lies on the electronic and control side, however, radical improvement has been achieved in recent years. If we look at the situation in our country, we see that there are thousands of looms in production. More than ninety percent of them are old machines.

Now, in old type of machines, operating systems such as DOS 6.22 (the ones that have Schleicher jacquards, it can be seen in Figure 1.15), OS9 (the ones that have Bonas jacquards, it can be seen Figure 1.16) and text screen controller (can be seen in Figure 1.14) that do not have support by the producers are being used. These operating systems do not support the storage devices such as CD, USB memory etc. Moreover, they do not support the wireless web standards such as IEEE 802.11. that may provide us to be able to transfer datas by using wireless communication. Now, the magnetic medias such as floppy or zip disks are being used to store the data. Because of the unreliability of the magnetic medias, serious problems such as loss of time and defective products may be yielded. In addition, statistical information about the production can not be stored in these systems. The systems such as statistical process control, database applications and business flow management can not be applied to these systems because of the inflexible software structure.

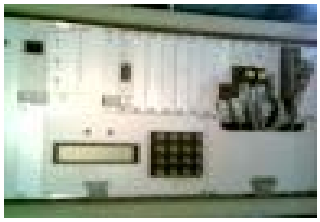


Figure 1.14 Text Screen Controller

Figure 1.15 DOS 6.22, Schleicher Jacquard

Figure 1.16 OS9

The designs that have high quality can not be stored in one disk and this situation causes another problem. Loading process can be done by uniting the design in the machine after the design data is divided into two or more parts by appropriate computer programs. Furthermore, the graphical user interface is not sufficient for the operator, loading process of can not be applied to these machines. Operator has to enter the number of the product each time after he stops the machine. This process that is being done by the operator sometimes causes to yield unexpected and defective products and time loss.

1.11 Contributions of the Study

The new software and hardware that have been produced in this study are able to overcome all of these problems mentioned above. Even though the study seems to be focused on the carpet sector, it can also be used for the machines that use the electronic jacquards, to weave fiber, towel etc.

The most important contribution of the study, as it can be easily guessed, economically, the firms in our country will not have to waste their own resources by purchasing equipments such as a special type of ethernet card providing communication between and jacquard and its contoller, other electrical components on the jacquard controller and maintenance fees from foreign brands.

More accurate results, especially about the percentages of gains that were obtained can surely be yielded in 1.5 or 2 years later than this study has been finished. It is hard to determine how exactly (by the numbers) this product will contribute the industrial sector in a short time.

1.12 Flowing Steps of the Study

Steps of the flowing of the study can be listed as;

1- Current systems were examined and found out the absences and incapable points of them.
2- Software and hardware were simultaneously designed for the solutions of the needs of current systems examined.

3- Step of production was processed without losing anytime right after the design of hardware and software.
4- Software and hardware designed were simulated and tested in laboratory conditions. In case of any failure, failed point was corrected and processed to next step.
5- The new system regenerated together with the design and production of hardware and software were installed on a real loom.
6- After the new system was installed on a real loom, some statistical datas such as practical speed and efficiency that can help us to estimate the needs that may be wished by the weaving sector in the future

Flow chart about the processing steps of the study can be seen in Figure 1.17.

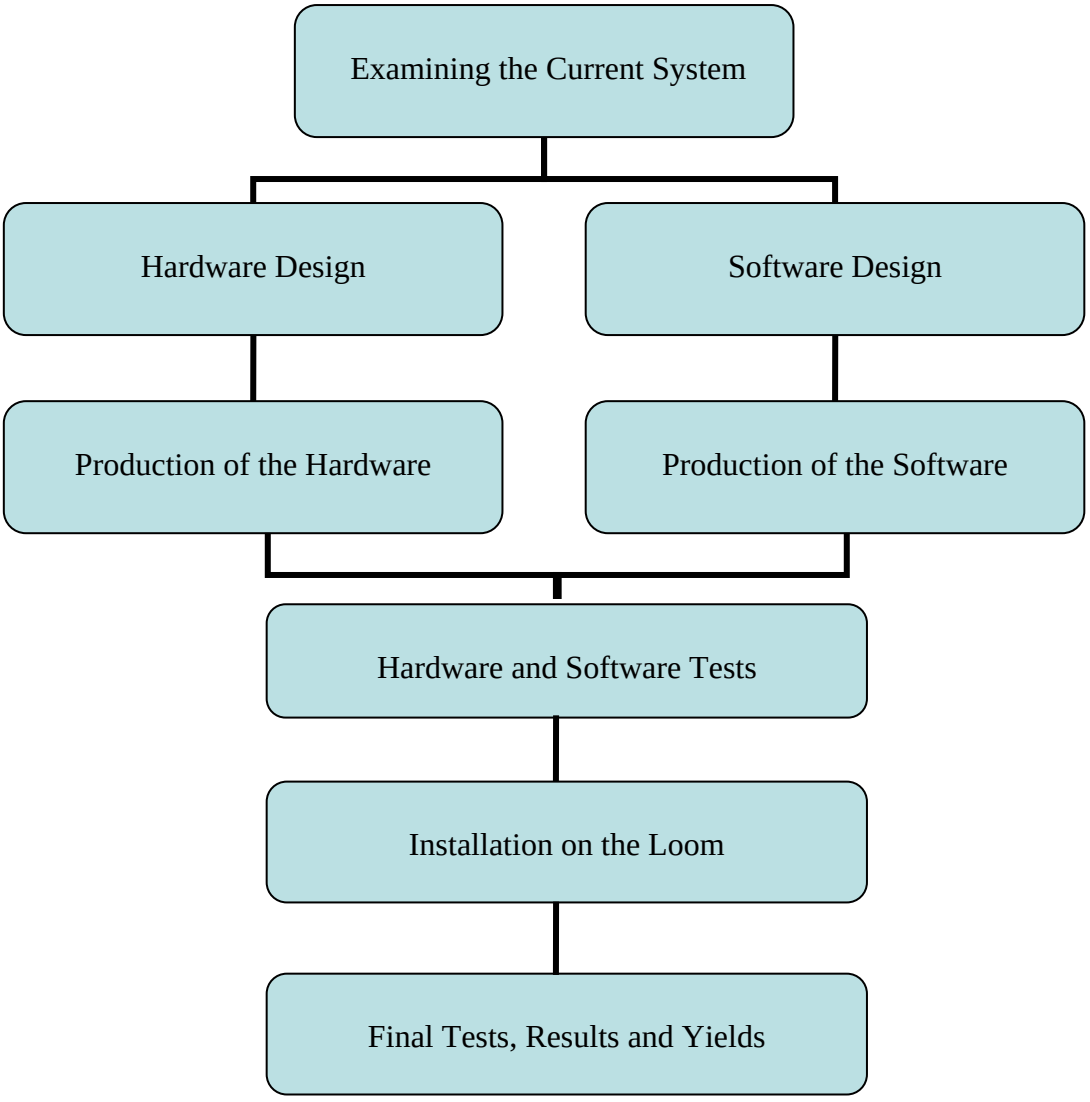


Figure 1.17 Flow chart of the entire study

1.13 Organization of the Thesis

As a guide to the study reported in this thesis, we can make following classifications. Chapter two includes the fundamentals of design and production of the hardware used in this study.

In chapter three, the software called “Weaving Control System” and providing the communication between jacquard mechanism and computer are described in details.

In chapter four, all hardwares connections that are necessary for the communication and signalization of them will be fully represented.

In chapter five, last chapter of the thesis, conclusions of the study will be demonstrated.

CHAPTER 2

HARDWARE

2.1 Introduction

In this chapter, the hardware that provides the communication between software called “Weaving Control System” and weaving machine will be represented in details. To begin with, the reasons making this kind of hardware necessary for the current weaving industry will be given. In the following sections, some useful information together with some definitions will be given for better understanding the subject. As final steps, design and production of the hardware will be represented in details.

2.2 The Needs for a New Hardware for Current Systems

For the current systems, jacquard installed on the weaving machine communicates with its control unit via an Ethernet card plugged on it. In Turkey standards, Since there doesn’t exist many enough qualified people working on the maintenance for these electronic cards that may cost up to thousand of euros/dollars, broken cards may be thrown away or may be used as spare parts for other possible failures that may occur on these cards. The circumstance that we are so helpless about maintenance about these cards forces us to design, produce and maintain our own electronic card and adapt it to the current systems. Together with the production of our own hardware, our industry will obtain a product that we may produce, develop, control and maintain it anytime and as we wish, but the most important of benefit that we will obtain is that we will not have to waste our own resources by purchasing foreign brands.

2.3 Selection of Proper Communication Protocol for the Hardware

In this section of Chapter 2, firstly, the definition of bus will be made and the types of it will be defined. General and most familiar communication protocols will be presented and the most proper one will be selected for the hardware and it will be represented in details in Appendix-B.

2.3.1 Bus and Bus Types

"A **bus** is a set (group) of parallel lines that information (data, addresses, instructions, and other information) travels on inside a computer. Information travels on buses as a series of electrical pulses, each pulse representing a "1" bit or a "0" bit (there are trinary, or three-state, buses, but they are rare)" [10].

The bus consists of three main parts:

a) Control Lines
b) Address Lines
c) Data Lines

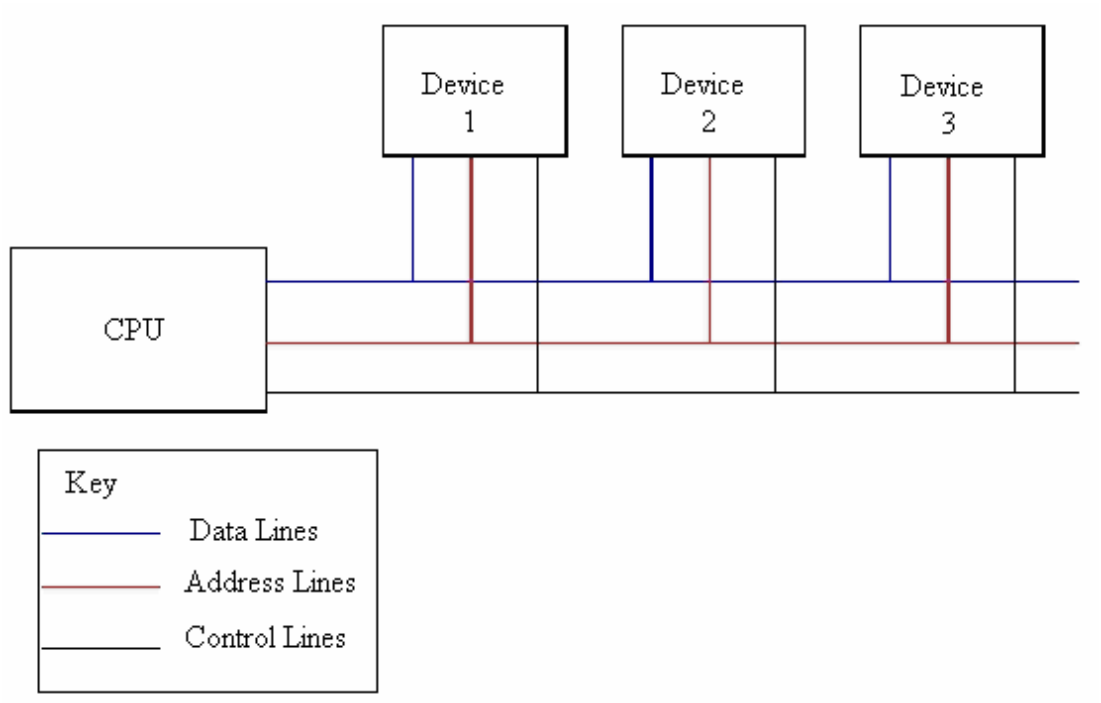


Figure 2.1 How devices are attached to a generic bus

Control lines allow the CPU to control which operations the devices attached should perform, I.E. read or write. A **control bus** is (part of) a computer bus, used by CPUs for communicating with other devices within the computer. While the address bus carries the information on which device the CPU is communicating with and the data bus carries the actual data being processed, the control bus carries commands from the CPU and returns status signals from the devices, for example if the data is being read or written to the device the appropriate line (read or write) will be active (logic zero).

Address lines allow the CPU to reference certain (Memory) locations within the device. An **address bus** carries address information. In most processors, memory is connected to the processor with separate address and data buses. The processor places the requested address in memory on the address bus for memory or the memory controller (if there is more than one chip or bank of memory, there will be a memory controller that controls the banks of memory for the processor). If the processor is writing data to memory, then it will assert a write signal and place the data on the data bus for transfer to memory. If the processor is reading data from memory, then it will assert a read signal and wait for data from memory to arrive on the data bus.

The meaningful data which is to be sent or retrieved from a device is placed on to **data lines**. A **data bus** carries data. Most processors have internal data buses that carry information inside the processor and external data buses that carry information back and forth between the processor and memory.

2.3.2 Some Useful Definitions about Bus

The **size** or **width** of a bus is how many bits it carries in parallel. Common bus sizes are: 4 bits, 8 bits, 12 bits, 16 bits, 24 bits, 32 bits, 64 bits, 80 bits, 96 bits, and 128 bits.

The **speed** of a bus is how fast it moves data along the path. This is usually measured in Megahertz (MHz) or millions of times a second.

The **capacity** of a bus is how much data it can carry in a second. In theory this is determined by multiplying the size of the bus by the speed of the bus, but in practice there are many factors that slow down a bus, including wait cycles (waiting for memory or another device to have information ready).

2.4 Steps of Hardware Design

That the communication between jacquard and control unit uses 16-bit data length at most for data transmission forces us to design an I/O card that has at least 8-bit length for data transmission and reception that can operate with a buffer mechanism that can buffer 16-bit data in 8-bit data packages. Since the design data and control signals from the jacquard operate simultaneously, it must accomplish the both processes simultaneously. Therefore we can conclude that there must be two devices independent from each other operating on the same I/O card and that one of them is charged for data transmission and other one is charged for data reception. And also, these two devices must be able to be controlled by another component on the same I/O card. To these features of the I/O card, that it should have the timing property can be added too, it would be useless if the timing of any system could not be controlled and if we couldn't create delays between adjacent datas. Finally, it must not cause any problems for other components operating on the same computer such as sound card and video card.

2.4.1 Coordination and Control of All Signals

All complex electronic systems need a component operating as a brain of entire system such as microprocessors, PICs and other programmable devices. In the coordination and control of the system designed in this study, PCI 9052 chip has been used to cover this need for this study.

The PCI 9052 provides a compact high-performance PCI bus target (slave) interface for adapter boards. The PCI 9052 is designed to connect a wide variety of local bus designs to the PCI bus and allow relatively slow local bus designs to achieve 132MB/sec burst transfers on the PCI bus. Even though we may not need the speeds in the range of tens MHz in the transmission speed of datas from the computer to the

jacquard control system for weaving process, it will be quite good if the speed of reception of data from the jacquard to the computer is high. No matter how slow the data signals received from the jacquard system are, PCI 9052 chip can achieve the acceleration of any data task, and transmit datas to the computer with respect to the speed of the oscillator connected to its Local Bus Clock input, (up to 40 MHz in non-multiplexed mode)LCLK. In this study, a 10 MHz oscillator has been used for the system to operate synchronously together with the other components that have maximum 10 MHz clock rate.

2.4.1.1 Configuration of PCI 9052 Chip

There are two important points in the configuration of PCI 9052 chip;

1. Length of the data bus that will be used in terms of bits.
2. Operation mode (Multiplexed or non-multiplexed mode)

In the selection of the length of the data bus in terms of bits, since 8255 chips have been used in this study for input and output interfaces of the system and also, since these chips use 8-bit length data bus, this situation forces us to use 8-bit length data bus. To be able to configure PCI 9052 chip for 8-bit data bus, it is enough to connect the byte enables of PCI 9052 chip, LBE#1 and LBE#0 to the system address bus. If these pins are connected to the system address bus (LA1 and LA0) and LBE#3 and LBE#2 are unconnected, PCI 9052 chip will use the least significant 8 bits of whole data bus, LAD [7:0], for the data bus. LAD [7:0] refers to that the bits from 7^{th} one to 0^{th} one are configured as data bus bits and the length of the data bus is 8 in terms of bits.

In the selection of operation mode of PCI 9052, as a beginning, it is useful to understand the terms, “multiplexed and non-multiplexed modes”. Briefly, if the address bus can also be used for the data bus too, this mode is called multiplexed mode, if it is not, it is called non-multiplexed mode. For example, PCI 9052 chip has 32-bit address and 32-bit address bus. Instead of using data bus independent from address bus, we may divide address bus into two parts as 16-bit data bus and 16- bit address bus or 8-bit data bus and 24-bit address bus (totally 32 bits). Selection of the

bus mode completely depends on the user but that the maximum operation speed of PCI 9052 chip is 8 MHz must not be forgotten in multiplexed mode. If the MODE input of PCI 9052 chip during the operation of it is logic 1, PCI 9052 chip operates in multiplexed mode, if it is logic 0, it operates in non-multiplexed mode. In this study, it has been used in **non-multiplexed** mode (to operate it in 10 MHz) that means the system uses buses (data and address buses) on different data channels.

The PCI 9052 contains a serial EEPROM interface, used to load configuration information. This is useful for loading information unique to a particular adapter (such as Network ID, Vendor ID, and chip selects). Since PCI 9052 chip requires 93LC46A/B type serial EEPROMs, 93LC46B type serial EEPROM has been used for proper configuration of PCI 9052 chip. More information about the configuration of 93LC46B chip can be found in Appendix-D

During power up, PCI RST# signal resets default values of the PCI 9052 internal registers. In return, the PCI 9052 outputs the local reset signal (LRESET#) and checks for existence of the serial EEPROM. If a serial EEPROM is installed, and the first 16-bit word is not FFFF, the PCI 9052 loads the internal registers from the serial EEPROM. Otherwise, default values are used. The PCI 9052 configuration registers can be written only by the optional serial EEPROM or PCI host processor. During the serial EEPROM initialization, the PCI 9052 response to PCI target accesses is RETRYs.

2.4.2 Parallel Interface Units of the I/O Card

In the selection of devices for data transmission and reception Intel's 8255 chip is quite sufficient for our application. Intel 8255 chip is a Parallel Interface Unit that has three configurable I/O ports that each of them has 8-bit length and one data bus having 8-bit length. To be able to configure 8255 chip as input or output, related datas must be loaded to its control register (for more detailed information about Intel 8255 chip, Appendix-E can be seen) Table 2.1 is utilized to configure 8255 chip.

Table 2.1 8255 Control Register Configuration

Control Word [Hex(Dec)]	Port A	Port B	Port C
80H (128)	OUT	OUT	OUT
82H (130)	OUT	IN	OUT
85H (133)	OUT	OUT	IN
87H (135)	OUT	IN	IN
88H (136)	IN	OUT	OUT
8AH (138)	IN	IN	OUT
8CH (140)	IN	OUT	IN
8FH (143)	IN	IN	IN

Since we need one device for input and another one for output, Table 2.1 shows that we should write “80H” to the first 8255 chip’s control register to configure it as “all ports of it as output” and “8FH” to the second 8255 chip’s control register to configure it as “all ports of it as input.”

2.4.2.1 Data Transmission

How easy to configure an 8255 chip was described in section 2.4.2. It can be obtained by writing “80H” to the control register of it. According to the principles of 8255 chip, the signal on $\overline{RD}$ input of it must be logic 1 during entire process of it. If this input is held logic 1 during the process, any data does not pass to the data bus from the ports of 8255 chip and “the direction of data flow always realizes from data bus to ports of it.”

2.4.2.2 Data Reception

We have learned that to be able configure the 8255 chip’s all ports of it as input, “8FH” value must be written to the control register of it. According to the principles of 8255 chip, the signal on $\overline{WR}$ input of it must be logic 1 during entire process of it. If this input is held logic 1 during the process, any data does not pass from data bus to the ports of 8255 chip and “the direction of data flow always realizes from the ports of it to the data bus.”

2.4.3 Timing of the System

There must be a subsystem that can slow down or generate delay for the whole system or that can generate enable inputs for the other components of the system. Briefly, this subsystem must adjust all timing specifications of the whole system. The necessity of a timer or a counter can be covered by 8254 timer/counter chip. This chip is capable of producing 0 or 1 at its OUT pin according to the value that is saved into its count register regarding to the clock frequency it is operating. The terms, time and count, even though they seem different terms than each other, they can be admitted same terms in digital systems. For example, let's assume that the operating frequency of timer/ counter is 10 MHz and 04H value is saved in the count register of the timer/counter. This configuration refers to that our chip will produce logic 0 at the OUT pin of it during 4 clock pulses operating under 10 MHz speed. After 4 clock pulses, the chip will produce logic 1 at the output of it. This situation can be commented in two ways as described below;

- If frequency is 10 MHz its period is 100 ns from the equation (timer sense);

$$t = 1/f \qquad \text{(Eqn. 2.1)}$$

So the total delay in the producing necessary OUT pin of the chip is

$$4*100ns=400ns \qquad \text{(Eqn.2.2)}$$

or

- Delay is 4 clock pulses that have 10MHz speed. (counter sense)

Since two comments refer to the same sense in the operating of the chip, it must not be surprising to name this chip counter or timer.

Since the desired count value can written to the count registers of it via data bus of it, data bus bits of the chip must be connected to the system data bus, when the chip is selected my multiplexer that will be discussed in the next chapter, data bus of the system will belong to timer/counter chip. Therefore, the value desired to be counted can be saved to the chip or the current value of the chips can be read from the chip. For further information about 8254 chip, Appendix-E can be seen.

Timer chip is especially necessary to generate delay between adjacent pile datas in this study.

2.4.4 Selection of Necessary Chip

There must be a subsystem existing on the I/O card that can do switching between the chips. In any study of designing hardware, since that more than one chip operates simultaneously is not necessary. Any system that can enable only one chip to operate at one time is proper for our need. In the design of this sub system, 74138 Multiplexer/Decoder chip has been used for the correct operation. A digital multiplexer is a combinational circuit that selects binary information from one of many lines and directs it to a single output line [9]. According to the principles of operation of multiplexer, if G_2 is logic 1, multiplexer produces 1s at the output pins of it (Y_0, Y_1…Y7) independent from other inputs, G_1 and select inputs. If G_1 is logic 0, multiplexer produces 1s at the output pins of it (Y_0, Y_1…Y7) independent from other inputs G_2 and select inputs. Because of this reason, G_1 input is connected to +5V (as it can be seen in Table 2.2) since it can accept +5V as logic 1 signal. It is easy to understand that we can name G_1 and G_2 inputs as enable inputs. If we assume that system sends the necessary commands to enable inputs for normal operation (G_1 is logic 1 and G_2 is logic 0) multiplexer produces 0 at the output pin of corresponding combination of select inputs. Assume that, CBA=010 and G_1G_2=10. The decimal equivalent of 010 is 2 and this means that multiplexer produces logic 0 at Y_2 pin. (For more information about multiplexer, Appendix-E can be seen.) That logic 0 is produced at Y_2 pin of multiplexer means that 8254 (Timer) is active other ones are passive. Since the chip select (CS') input is complemented by the input pin itself, logic 0 triggers the chip, not logic 1. Although 74245 (Octal Bus Transceiver) chip does not have a CS input, since $\overline{E}$ (enable) input of it operates in the same way, there are no conflicts in the operating of the switching system.

Normally, $G_2 = G_{2A} + G_{2B}$ but since we want the selection to be dependent on only the CS' input of PCI 9052 chip. G_{2B} input of multiplexer is grounded and this connection causes the signal at the pin G_2 to be dependent on only G_{2A} since we may conclude that;

$G_2 = G_{2A} + G_{2B}$ (logic 0) $\rightarrow$ $G_2 = G_{2A}$ (Eqn.2.3)

Table 2.2 Truth table of switching between the chips via multiplexer

+5V	PCI 9052 CS'	Select inputs			1^{ST} 8255 CS'	2^{ND} 8255 CS'	8254 CS'	74245 $\overline{E}$
G_1	G_2	C	B	A	Y_0	Y_1	Y_2	Y_3
1	1	X	X	X	1	1	1	1
1	0	0	0	0	0	1	1	1
1	0	0	0	1	1	0	1	1
1	0	0	1	0	1	1	0	1
1	0	0	1	1	1	1	1	0

2.4.5 Base Addressing

In computing, a **base address** is an address serving as a reference point ("base") for other addresses. In other words, it is the starting point for other addresses for the same hardware. To be able to transmit the base address data, there must be another subsystem as it is in the selection of the necessary chip, manual or automatically that can allocate the base address on operating system installed on the computer. When the operating systems executes this procedure, any hardware on the computer can not use the same base address and all devices on the computer can operate on their own data channels without any problem. If the operating systems allocated the same base addresses for different devices, since the same address buses would be used by the different devices, there would be many situations that are not expected such as fatal failures on the devices. The subsystem designed for the base addressing of the I/O card can be seen in Figure 2.2

In the operation of subsystem in Figure 2.2, as it can be seen it is a simple circuit to understand the principles of the operations of it. Firstly, it is better to understand the operation of "Octal Bus Transceiver (74245)" chip. As it can be seen in Table 2.3 if both of DIR and $\overline{E}$ input are logic 0, the all datas on bus B are transmitted to the bus A. In other words, the datas on bus B_n are transmitted to bus A_n. If $\overline{E}$ input is logic 0

and DIR input is logic 1, the datas on bus A_n are transmitted to bus B_n. (n=0, 1,…7) but $\overline{E}$ input is logic 1, the chip is isolated and does not let any buses to be transmitted.

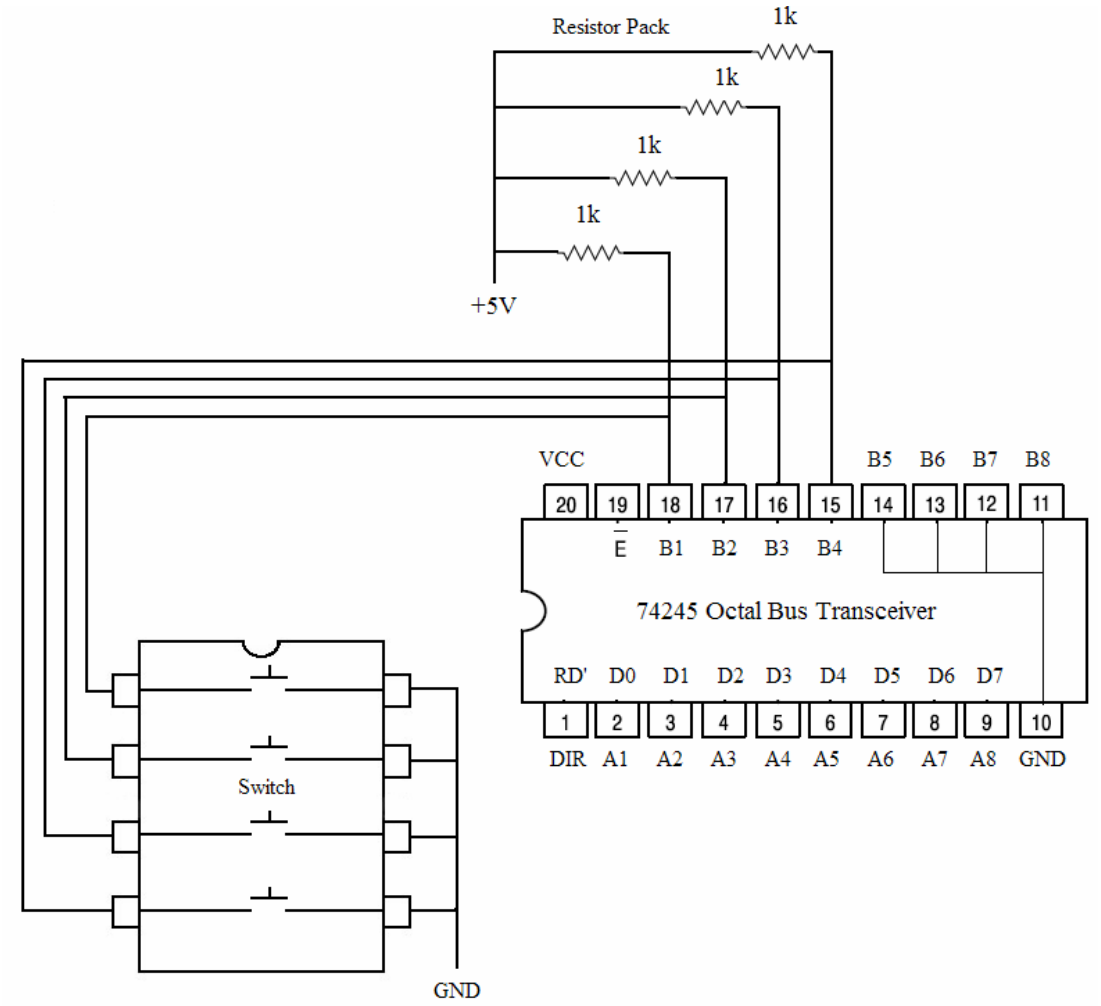


Figure 2.2 Subsystem for base addressing

Table 2.3 Truth table of octal bus transceiver

INPUTS		OUTPUT
$\overline{E}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

$\overline{E}$ input of the 74245 chip is connected to 74138 (multiplexer) for chip selection. Since that 74245 chip is selected is assumed, there is no need to show in Figure 2.2. DIR input of the chip is connected to the RD' input of the system to READ the data on data bus and transmit the related data (base address data) to the computer.

When one of the pins of the switch is closed manually, corresponding bit of that pin is grounded and logic 0 data is transmitted to the B bus of 74245 chip. If the pin remains open, the logic 1 data is transmitted to the B bus via resistor pack as shown in Figure 2.2. The last four bits of the chips are grounded since we do not need so many base address combinations. Only first four bits of B bus are combinational. Even this type of connection provides us sixteen different base address combinations. When the conditions, that $\overline{E}$ input is logic 0 (chip is selected), RD' input is logic 0 and PCI bus is on address phase are satisfied, the base address datas are transmitted to the system data bus (D_0, D_1,….D_7, D_0 is the least significant bit.) firstly and they are accepted as addresses instead of datas since the entire system is on address phase. The terms address and data phases are described in section B.2.3.3.1 under the title Frame Pin (FRAME#) in Appendix-B.

2.4.6 Warning Light Emitting Diodes

There are sixteen light emitting diodes (LEDs) independent from each other on I/O card that emit light when data exists on the ports, P1A and P2A of it. P1A refers to the A port of 1st 8255 chip and P2A refers to A port of 2nd 8255 chip. Since these LEDs are connected to the ports of I/O card in parallel, they do not have any affect on the operation of the system. They are just for warning the user about the data existence. If the data exists any pin of these ports (logic 1) this signal is sensed by the inverter gate in 7405 chip and inverted to 0V (logic 0). Therefore the current passes through the resistor and leads the LED to emit light since there is a voltage difference between two ends of the LED. If no data exists, 0V is inverted by inverter gate in 7405 chip to 5V but since there will be no voltage difference between the inverter output and voltage source on the first pin of resistor pack, no current flows and LED does not emit any light. Related subcircuits can be seen in Figures 2.3 and 2.4.

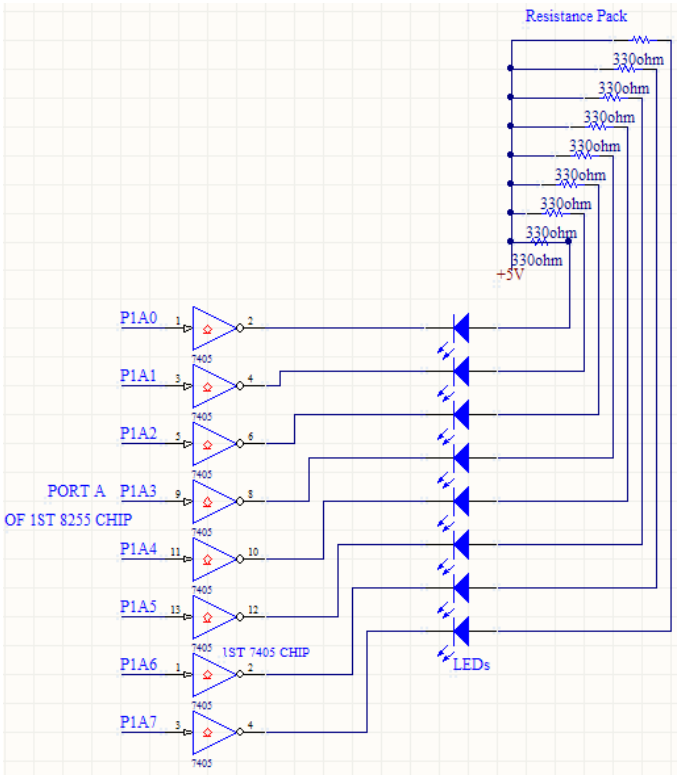


Figure 2.3 Circuit diagram of warning LEDS for P1A port of 1st 8255 chip

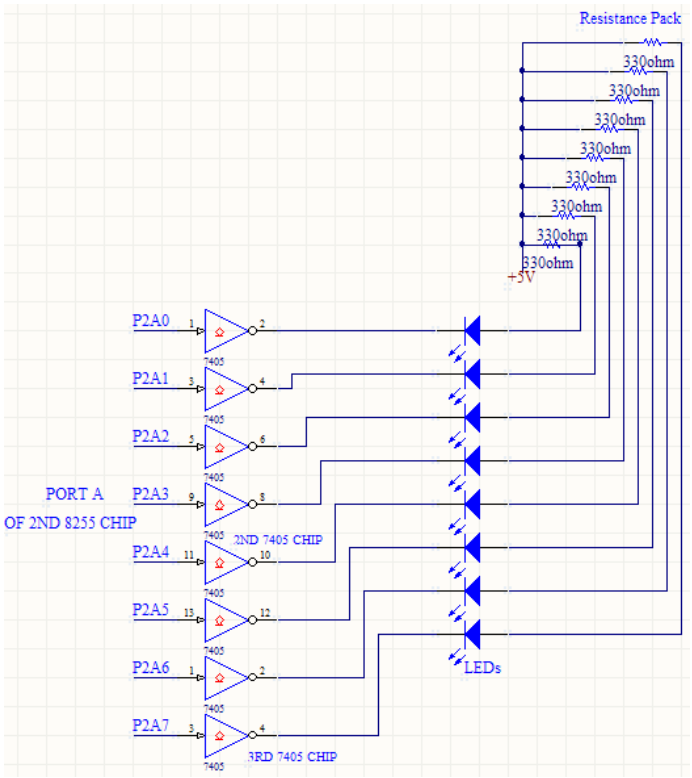


Figure 2.4 Circuit diagram of warning LEDS for P1A port of 2nd 8255 chip

2.4.7 Synchronizing All Components

That all components operate in synchronous speed is very important issue since that the all components can be controllable is desired. For a circuit that has components operate in different speeds, it is really hard to design and control the subcircuits existing on the I/O card. This situation causes the design to be formed much more difficult than the design that has synchronous components existing on it. To able to achieve the procedure of synchronizing the circuit, the main component, PCI 9052 must be configured as "first effected device from local bus clock." Since that selected 8255 and 8254 chips that operate in 10 MHz speed, a proper *crystal oscillator* should be connected to local bus clock input of PCI 9052 chip. By the help of this connection of crystal oscillator to local bus clock input of PCI 9052 chip, the I/O card operates in 10 MHz (maximum) in a synchronous form. If such a configuration hadn't been done, since 8254, 8255 and PCI 9052 chips would operate in different speeds, there will many mismatchings between square waves carrying datas. Hence, desired data wouldn't be transmitted/received to/from to correct path in desired duration.

2.4.8 Decoupling Electrical Networks of the I/O Card

Decoupling of electrical networks is the method that decouples an electrical network from another one by using decoupling (bypass) capacitor.

Sometimes, for various reasons, a power supply supplies an AC signal superimposed on the DC power line. Such a signal is often undesirable in the powered circuit. A decoupling capacitor can prevent the powered circuit from seeing that signal, thus decoupling it from that aspect of the power supply circuit.

To decouple a subcircuit from AC signals or voltage spikes on a power supply or other line, a bypass capacitor is often used. A bypass capacitor is to shunt energy from those signals or transients past the subcircuit to be decoupled, right to the return path. For a power supply line, a bypass capacitor from the supply voltage line to the power supply return (neutral) would be used [14].

2.4.8.1 Placement of Decoupling Capacitors to the Circuit

A transient load decoupling capacitor should usually be placed as close as possible to the device requiring the decoupled signal. The goal is to minimize the amount of line inductance and series resistance between the decoupling capacitor and that device, and the longer the conductor between the capacitor and the device, the more inductance there is. [13]. In the I/O card designed, it is quite sufficient to place 0,1μF (as often used) ceramic capacitors as close as possible to the integrated circuits to decouple them from other signals and connections of the circuit. Since there are ten ground and ten supply connections of PCI 9052 chip, to use 5, it is enough to use 1 decoupling capacitor for each two ground and power connections.

A power supply decoupling bypass capacitor should be placed as close to the voltage/current source as possible. The idea is to minimize the line inductance and series resistance between the capacitor and the supplied devices. In our study, it is sufficient to place 10μF (as often used) polarized capacitors as close as possible to the source pins of PCI connector to decouple the voltage sources that we have used on the whole system from other signal on the I/O card.

As shown in Figure 2.5, any capacitor that has capacitance value may be used between 0.01 μF and 0.1 μF for transient load decoupling and for power supply decoupling, any capacitor that has capacitance value between 10 μF and 100 μF may be used.

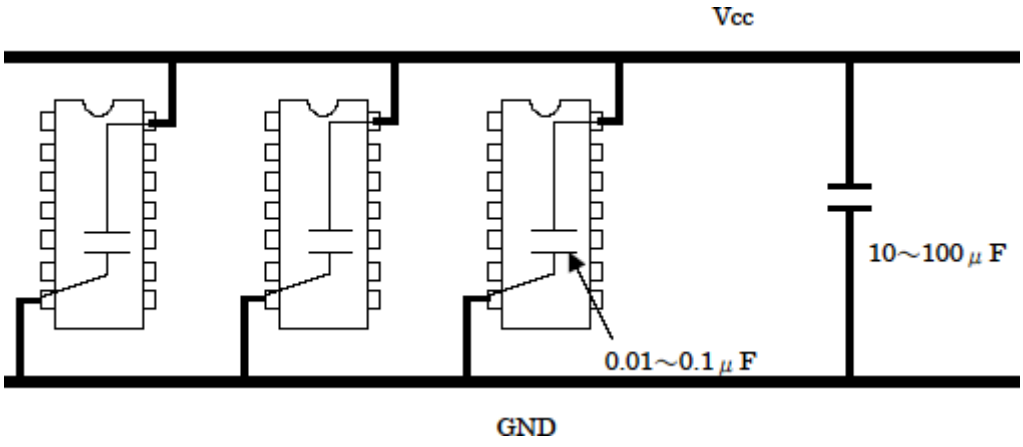


Figure 2.5 Connection of decoupling capacitors to any system

2.4.9 Artwork of the I/O Card

In this subsection of chapter two, the I/O card was designed in a few steps such as arranging and placing components on board, routing trace widths and spacing and corners of tracks. In the artwork of the I/O card, Altium Designer Ver. 6.9 program was utilized.

2.4.9.1 Arranging the Components on the Board

Before routing any connections, components of entire I/O card must be placed on the board. Where the components are located on the board and where they are in relation to each other can affect the how the circuit performs, how easy it is to route the traces, and how convenient it is to test and repair the finished board [15]. According to the signal relations mentioned in design steps, placement of all components of the I/O card has been formed as shown in Figure 2.6.

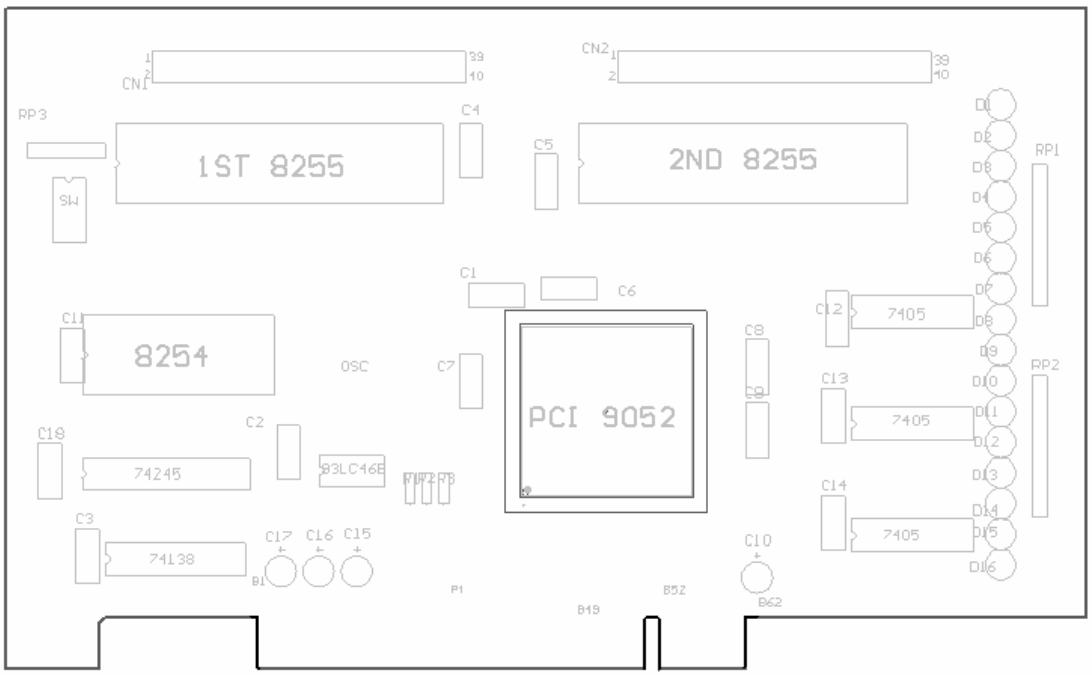


Figure 2.6 Placement of all components on the board of the I/O card

2.4.9.2 Routing Trace Widths and Spacing

The first thing that can be regarded about the routing trace widts and spacing between the traces is that trace width and spacing depend on the current that the traces must carry.

As a general rule, **the widest traces and widest spacing can be used, while still achieving the layout and board size desired.** When the traces are widely spaced, we are less likely to find unwanted short circuits caused by incomplete etching or solder bridging between traces. Wide traces can also reduce electrical noise problems because of their lower impedance.

As with copper wire, the amount of current a PC board trace can safely carry is a function of its cross-sectional area. Thick wide traces can carry more current than thin, narrow ones. Table 2.4 shows the amount of current that traces of varying widths and thickness can safely carry [15].

Table 2.4 Maximum currents for different trace widths

Weight of copper foil ($oz./\ ft^2$)	Trace width (in.)	Maximum current (amps)
0.5	0.005	0.13
	0.01	0.5
	0.02	0.7
	0.03	1.00
1	0.005	0.5
	0.01	0.8
	0.02	1.4
	0.03	1.9
2	0.005	0.7
	0.01	1.4
	0.02	2.2
	0.03	4.00

When that the maximum current that PCI 9052 chip dissipates is 130 mA is regarded, even though it has 10 ground and 10 power connections. A track width having 0.01 inch (0.254) wide can be used for data transfers for our design. That maximum operating current of 8255 and 95LC46B chips are individually 1mA and 20 mA can be given for a better illustration proving that we do not need such thick tracks for the board. For ground and power connections, it is sure that thicker tracks are necessary since they are connected to nearly all components and that they carry higher currents than other tracks such as data tracks do. For the selection of track width of power and ground connections, especially for tracks close to the PCI connector, 0.3 inch (0.762 cm) wide tracks have been used for this study. In some parts of ground and power connections of the board that around 0.2 inch wide tracks have been used can be observed.

Narrow closely spaced traces do have some advantages. They require less room on the board, and they can be routed between IC (integrated circuit) pads more easily. Spacing between traces becomes more critical when there are large voltage differences between traces [15]. Table 2.5 shows recommended spacings for traces according to their difference in peak voltages.

Table 2.5 Minimum trace spacings for uncoated traces

Voltage difference between traces (DC or AC peak voltages)	Minimum spacing between traces
0-50	0.015in.
51-150	0.035in.
151-300	0.050in.
301-500	0.100in.
500+	0.0002in./volt

When the Table 2.5 and that the maximum voltages that I/O card supports are +12V and -12V are regarded, even 0.015 in. (0.0381mm) spaced tracks will cause no problems on the board. On the board of the I/O card, the minimum space between adjacent tracks is 0.25mm for the lines that has voltage maximum +5V (for data

lines) and minimum space between two adjacent lines that has +12V and -12V voltage levels is 0.45mm.

2.4.9.3 Corners of the Traces

If a variety of PC boards is examined, that the traces make sharp, 90 degrees corners, while others use angled (chamfered) corners, and still others use rounded corners can be observed easily. Rounded and or angled corners conserve board space and less likely to form solder bridges with adjacent traces or pads. In addition, the copper foil is less likely to crack or lift from a rounded trace. In most circuits, rounded corners can prevent the reflections and radiation losses that can occur with square corners. [15]. If we draw an analogy between the electrons passing through the trace of a voltage line and a car going on the way, it is hard to turn the corner for both of them if the corner is vertical, but the corner is rounded or angled, it is easier for both of them to turn it than it is for them on vertical corners. We can easily conclude that it is better to use angled traces for our design on the board of I/O card. In Figures 2.7 and 2.8, two random screen-shots from the board of I/O card illustrate how rounded corners for traces are used in the routing of the traces.

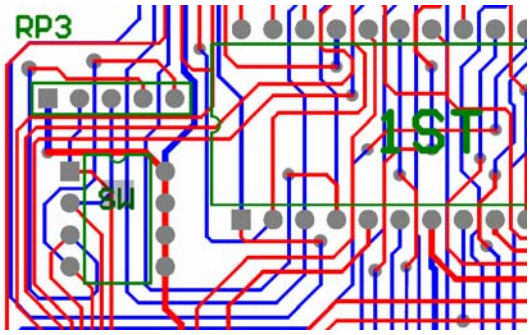


Figure 2.7 A view from left top corner of the board

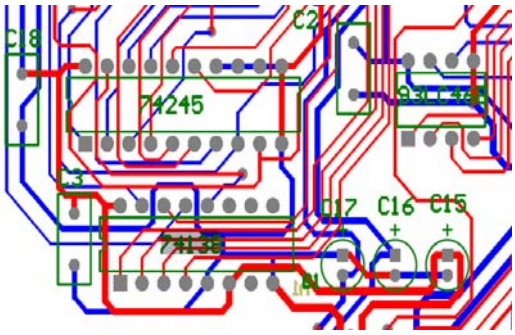


Figure 2.8 A view from left bottom of the board

Since there is not enough space on one layer of the board for all connections, this situation forces us to route the tracks on two layers of the board. The red lines on the board represent the tracks on the top layer and blue ones represent the tracks on the bottom layer of the board of the I/O card. Connections between layers on a double-

sided board have been made with *vias*, or feed-throughs, which are small, drilled holes that terminate in small pads on both sides of the board. Completed view of the board of the I/O card can be seen in Figure 2.9.

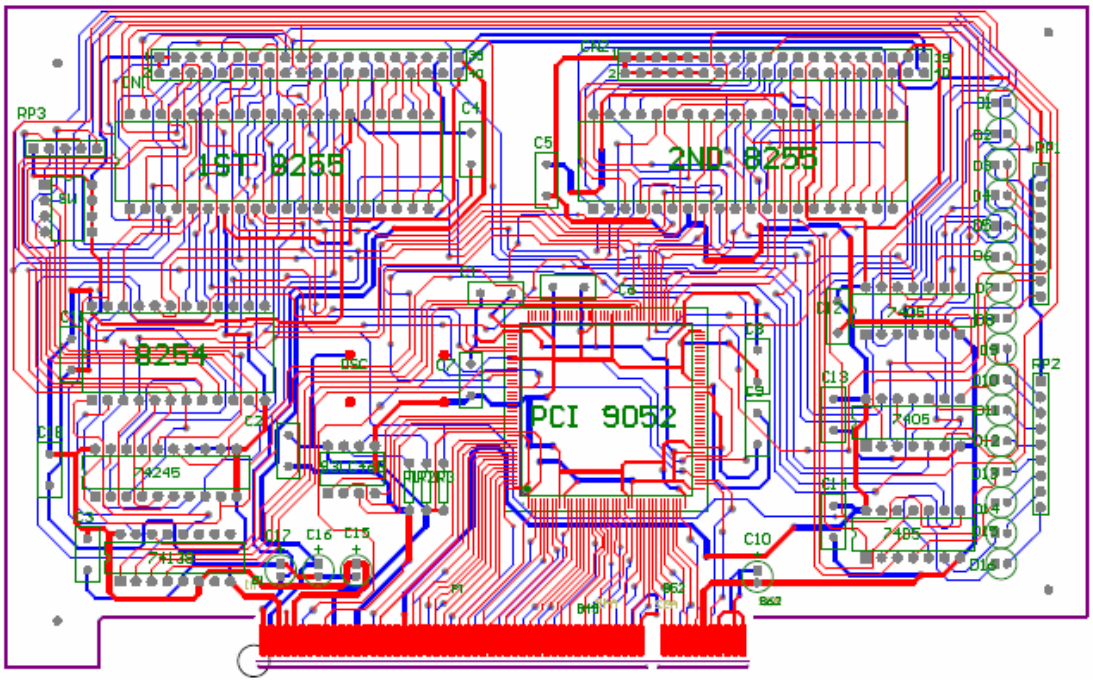


Figure 2.9 Complete view of the board of the I/O card

2.5 Production of the I/O Card

In this section of chapter two, production steps of the I/O card designed will be discussed in details.

2.5.1 Printing the Artwork

To be able to transfer design to the board, the first thing that should be done is to transfer the voltage traces of the I/O card to the board, to be able to achieve this procedure, gerber files of both layers, top and bottom layers must be obtained as fabrication outputs via Altium Designer. Gerber files of both layers of the I/O card can be seen in Figures 2.10 and 2.11.

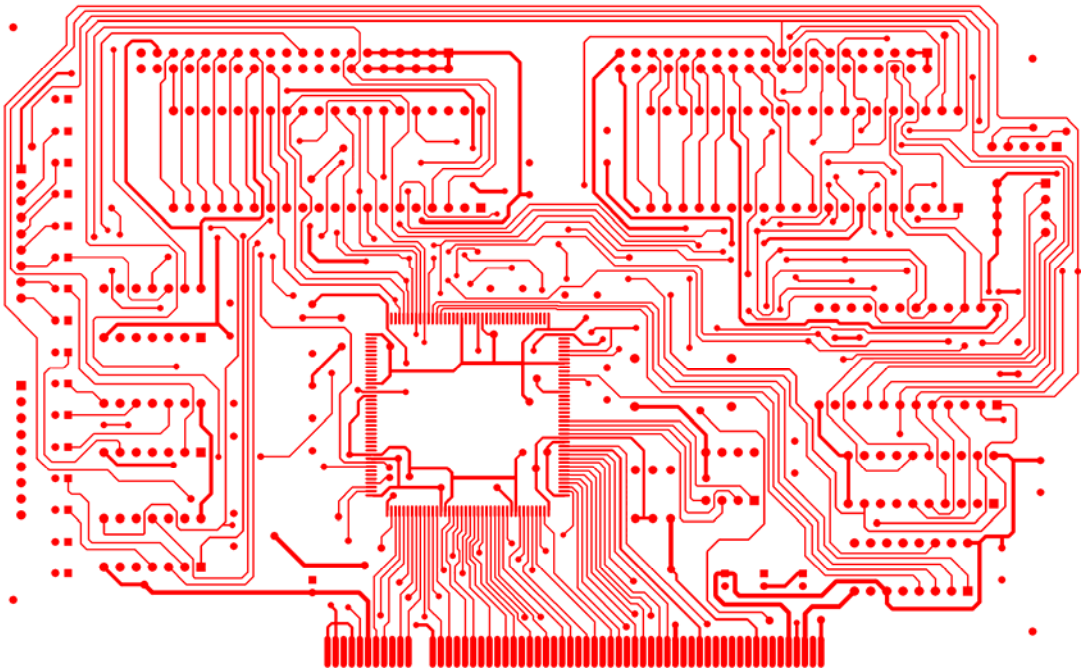


Figure 2.10 Gerber file of top layer of the I/O card

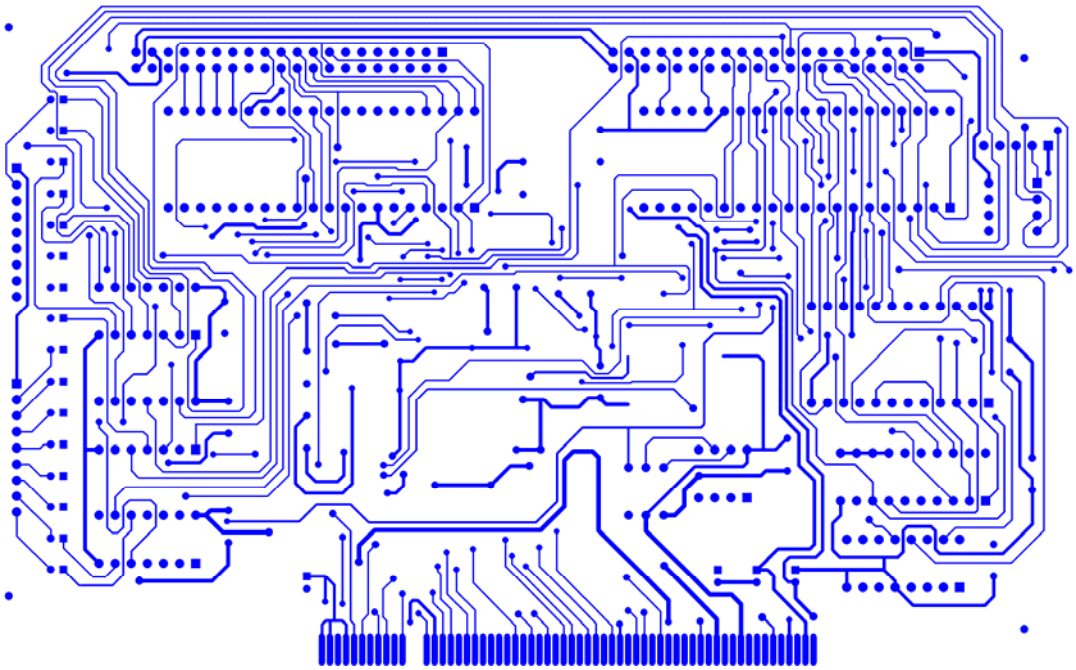


Figure 2.11 Gerber file of bottom layer of the I/O card

After the gerber files of the design via Altium Designer is obtained, these fabrication outputs must be printed by a high quality laser printer, preferably 1200 dpi or more

to a dry transparent film. Printer output of top layer gerber file can be seen in Figure 2.12.

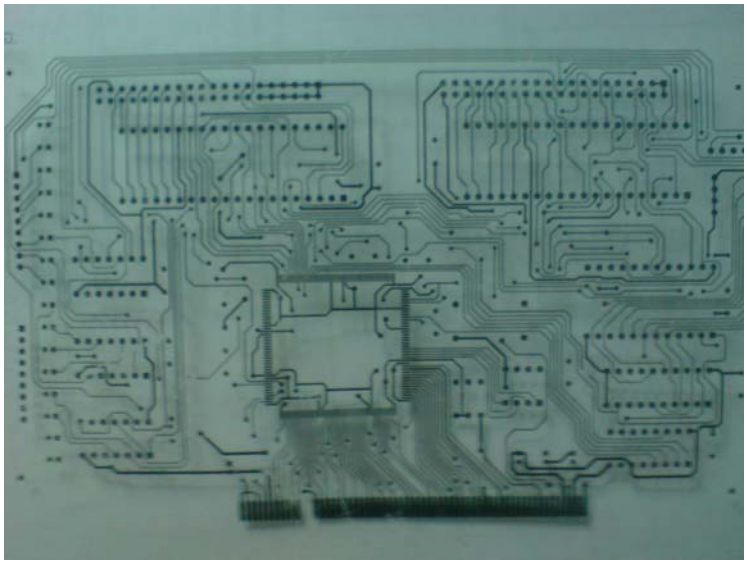


Figure 2.12 Laser printer output of top layer gerber file

2.5.2 Exposing the Artwork onto the Board (Image Transfer)

The next step in manufacturing the I/O card is the transfer of original artwork pattern to the copper surface on the card. The first thing that should be done to transfer the image to the board is to tape the both gerber outputs on both layers of the PCB board very carefully. In the production of the PCB of this study, it is good to use a dry transparent film which is sensitive to ultraviolet light (200–500 nm). The application of the photoresist is carried out in a machine called the exposure unit that can be seen in Figure 2.13. The photoresist is heated to about 110 °C and then pressed to the copper surface of the board. The photoresist may be of positive or negative type. In case of the positive photoresist, the polymerized resist is soluble in the liquid developer and it requires artwork in the form of a positive. The negative type photoresist gets polymerized with ultraviolet light and becomes insoluble in the developer. Here the artwork is in the form of a negative. The coated board is exposed to the ultraviolet light. The resist is then developed, leaving those portions of the copper which are to be retained on the board and is covered by the resist.

Overexposing is a problem if the opaque areas on the transparency don't completely block light, because areas that should be protected from light will begin to expose slightly. Overexposing can also allow light to leak under the edges of the artwork, resulting in thinner traces and smaller pads on a positive-acting board.

Figure 2.13 UV Exposure unit

2.5.3 Etching the Board

In the etching step, our final board is created by removing exposed copper, leaving the artwork drawn in copper on the bare board.

To etch, immerse the board in an enchant, a chemical bath that removes the exposed copper from the board. In this study, ferric chloride and ammonium persulfate mixture solution has been used. During the etching process, a chemical reaction causes the copper to dissolve in the etching solution. Top view of the I/O card after etching can be seen in Figure 2.14.

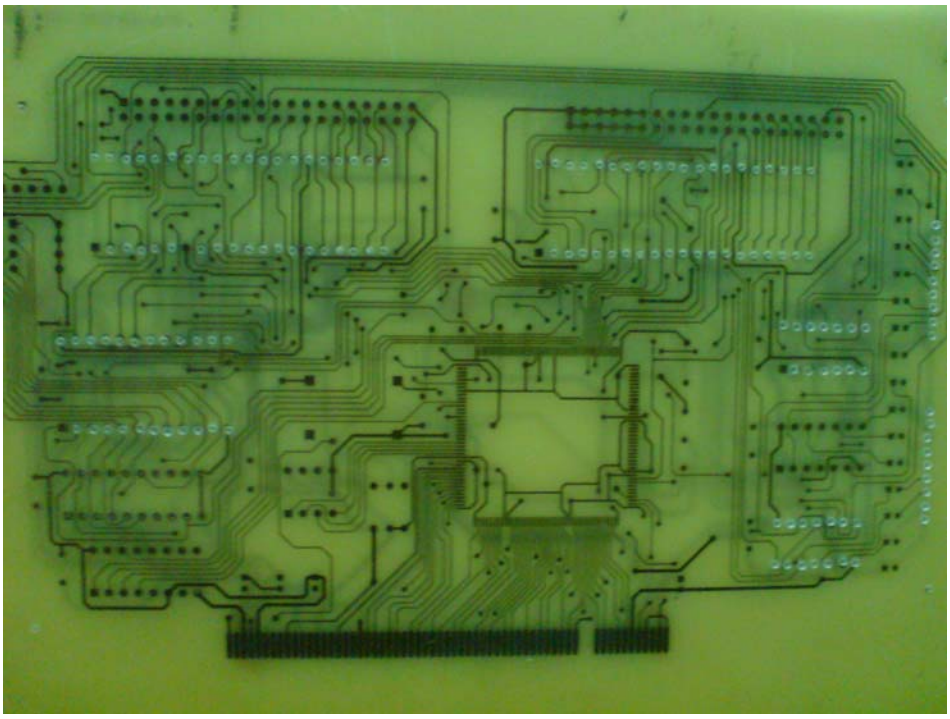


Figure 2.14 Top view of the board after etching process

2.5.4 Drilling the Board

Next step is to drill the proper holes for the through hole components (all components excluding PCI 9052 chip since it is surface mount component) existing on the I/O card. For this study, an automated drilling system has been used that uses the drill files, another fabrication outputs of Altium Designer program.

A drill file is a text file that describes the location, size and depth of of every hole to be drilled in the board. The drill file is read by the automated drilling system using computer base which uses the information to drill the holes automatically. An automated drilling system from Excellon Automation Company can be seen Figure 2.15.

Figure 2.15 An automated drilling system from Excellon Automated Company

2.5.5 Coating the Board

The base metal conductor used in the fabrication of printed circuit boards is copper. Copper is chosen because of its excellent properties as a conductor of heat and electricity. However, it quickly oxidizes in the presence of air and water. If the copper surface on the printed circuit board is not coated or treated with a protective agent, the exposed area would rapidly become unsolderable. Therefore, all printed circuit boards necessarily use some form of a surface finish on the exposed pads to which electronic components are to be soldered [16].

Steps of spray coating that have been applied on the I/O card can be listed as;

- Board is cleaned.
- Protected areas like terminal pins, connectors are masked off or removed.
- Coating is applied using a spray process on both sides of the PCB and its edges.
- Coating is cured using oven according to the coating type.
- Masking is removed and any removed parts are reassembled.
- Board undergoes full production testing to ensure functionality of board is not affected by the process.

2.5.6 Soldering the Components of the I/O Card to the Board

Soldering the components onto the board of the I/O card is the last step of all ones.

Soldering is the process in which two or more metal items are joined together by melting and flowing a filler metal into the joint, the filler metal having a relatively low melting point [17].

In this step of production, the components are placed to the locations adjusted before regarding the electrical relations between each other. After the components of the I/O card have been placed. They have been soldered on the bottom layer of the board since it easier to fix by soldering the components to the board on the bottom layer and all the components of the I/O card are on the top layer.

Since PCI 9052 chip is a surface mount component, there doesn't exist any hole to fix this chip on the board of I/O card. Therefore, it must be soldered to the board by using hot air method. In this method, after PCI 9052 chip is fixed to the board manually and applying compress onto it by hand. Hot air is applied to the pins of the chip and that it is fixed to the board is provided. The I/O card designed can be seen in Figure 2.16.

Figure 2.16 Top view of the I/O card after all production steps

2.6 General Properties of the I/O Card

We can list the properties of the I/O card after all design and production steps as given below;

- 32 bit PCI bus addressing.
- 8 bit data bus (in non-multiplexed mode).
- Plug and Play feature. (By the help of the driver that will be described in Appendix-D.)
- 6 configurable I/O ports that each of them has 8 bits (48 I/O lines). 3 ports of 1st 8255 (A, B and C ports) device are connected to channel 1 (CN1) and 3 ports of 2nd 8255 (A, B and C ports) chip are connected to channel 2 (CN2). Pin assignments of each channel can be seen in Tables 2.6 and 2.7.
- Maximum 10 MHz operating speed.

In the translation of the meanings of the data and voltage pins on the channels, in the representation "P*XYZ*", "P" refers to the port, "*X*" refers to the number of the channel (1 or 2), "*Y*" refers to the port of the corresponding 8255 chip (A, B and C) and finally, "*Z*" refers to the number of the corresponding bit (0, 1, 2, 3, 4, 5, 6 and 7). For example, P1B6 refers to 6th bit of B port of 1st 8255 chip of the 1st channel. (7th bit is the most significant one and 0th is the least significant one.)

Additionally, I/O card is capable of yielding +5V, -5V, +12V, -12V voltage supply connections at the pins of it for additional subcircuits that may be connected to the whole weaving system. Especially, how important +12 V voltage supply is will be discussed in the operation of optocouplers for sensor signalizations in Chapter four.

Table 2.6 Pin Assignments for CN1 connector

Pin	Function	Pin	Function
1	GND	2	GND
3	GND	4	P1A3
5	P1A1	6	P1A2
7	CLK0	8	P1A0
9	GATE0	10	OUT0
11	OUT2	12	CLK2
13	CLK1	14	GATE2
15	OUT1	16	GATE1
17	P1A5	18	P1A4
19	P1A7	20	P1A6
21	P1C6	22	P1C7
23	P1C4	24	P1C5
25	P1C1	26	P1C0
27	P1B7	28	P1C2
29	P1B6	30	P1C3
31	P1B5	32	P1B0
33	P1B4	34	P1B1
35	P1B3	36	P1B2
37	+5V	38	-5V
39	+12V	40	-12V

Table 2.7 Pin assignments for CN2 connector

Pin	Function	Pin	Function
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	GND	8	GND
9	GND	10	GND
11	GND	12	GND
13	P2A0	14	P2A1
15	P2A2	16	P2A3
17	P2A4	18	P2A5
19	P2A6	20	P2A7
21	P2C7	22	P2C6
23	P2C5	24	P2C4
25	P2C0	26	P2C1
27	P2C2	28	P2B7
29	P2C3	30	P2B6
31	P2B0	32	P2B5
33	P2B1	34	P2B4
35	P2B2	36	P2B3
37	+5V	38	-5V
39	+12V	40	-12V

CHAPTER 3

SOFTWARE

3.1 Introduction

In this chapter, the software called “Weaving Control System” that provides the communication between the computer and the jacquard control system will be represented in details. First of all, the subject, why this kind of software is necessary for the current weaving industry is given. In the following sections, the content, flow diagram, processing steps and the general structure of the software together with some code blocks (in Appendix-C) will be demonstrated with some details. As a next step, the detailed algorithm about the process of weaving will be given step by step in the form of flow charts. Finally, the process of Weaving Control System is illustrated with an example carpet weaving.

3.2 The Needs for a New Software for the Current Systems

As demonstrated in the introduction chapter, the designs are still transferred to the old weaving machines by using 3.5” floppy disks. This kind of magnetic medias such as floppy disks cause distortions and defective products on carpet weaving. Furthermore, copying design data from floppy disk to the weaving machine is a time wasting procedure since the transfer rate of magnetic medias are quite low. High quality design data can not fit into the floppy disks that have low data capacity and this situation causes the defective products as well. Nowadays, these high quality designs can be loaded to the weaving machines by dividing the design data into many parts and unite in the weaving machine by using some other softwares and this situation causes additional time wasting. Since the current systems do not have a real “Human Machine Interface” system, the multiple designs loading process can not be

achieved by the operator. All the problems stated above will be overcome by the software called as “Weaving Control System”.

3.3 The Content of the Weaving Control System

Briefly, the purpose of the software called Weaving Control System is to transmit the related job order data to the weaving machine in a way faster and safer than the current systems do and keep the weaving machine under the control in software sense. To be able to achieve this task, the software converts the pile data to the proper format for the weaving machine and transmits it to the jacquard memory by regarding characteristical information set before of the weaving machine. During the weaving process, the software communicates with jacquard and continues to this procedure until the current job order is finished and repeats the same procedure for next each pile.

3.4 General Process of Weaving Control System

1. Desired widths(s) and part(s) of carpets (these may be some things else that use jacquard system such as fabric and towel) are formed.
2. The designs can be added to the streets by clicking right button on the mouse of the computer and the number of per design that will be woven is entered by the operator. As a result of these datas entered by the operator, that how many wefts each part has and how long the weaving process lasts with respect to the estimated speed can be seen on the operator window.
3. When the weaving process begins, some statistical datas such as total process time, elapsed time are saved by regarding practical weaving speed obtained from quantity of wefts processed per minute.
4. When the job order is completed or stopped, a new job order maybe started or the weaving process can be started from a different weft of the same job order.

A detailed flow diagram can be seen in Figure 3.1 as shown below for a better understanding the general processing steps of Weaving Control System.

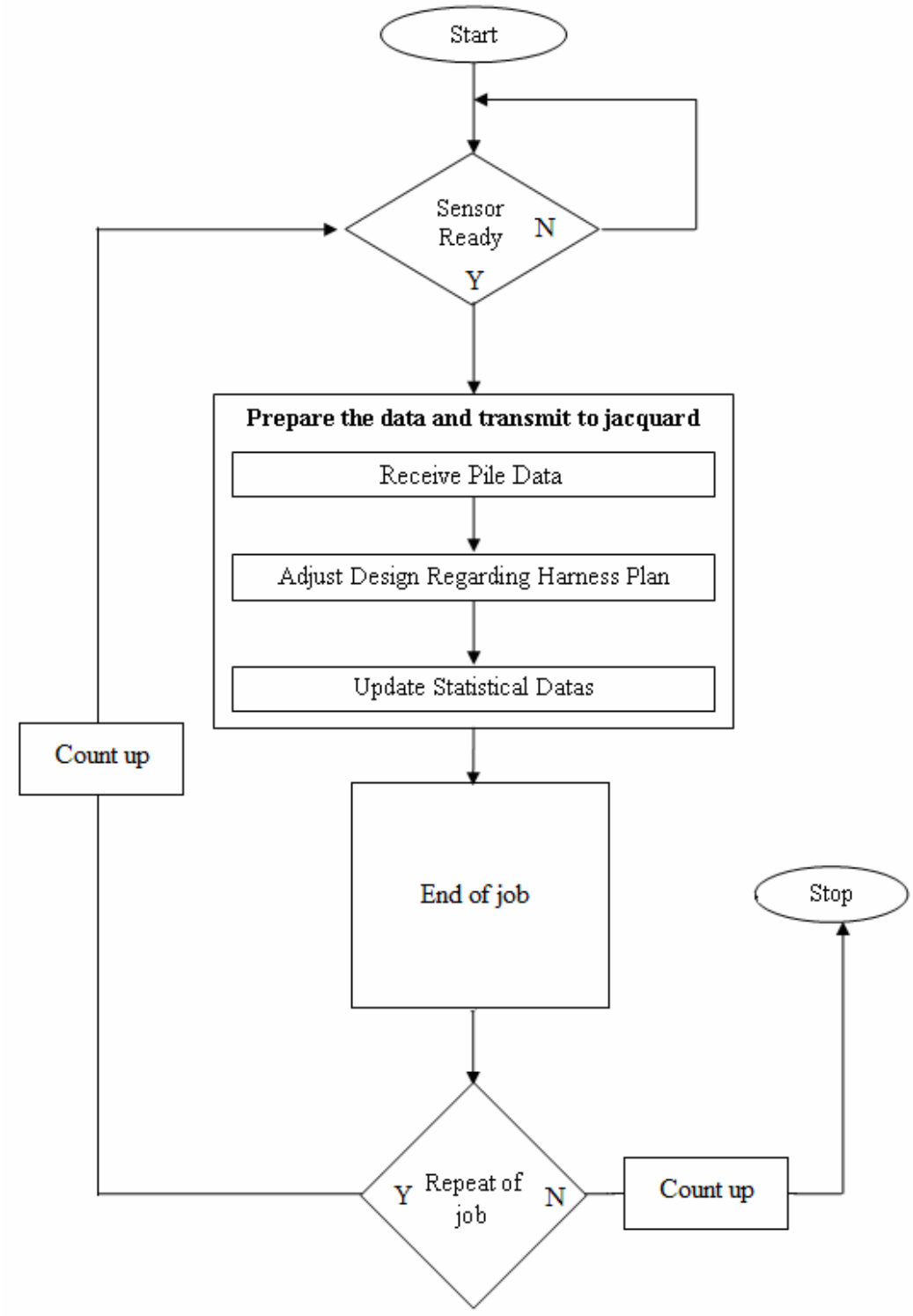


Figure 3.1 General flow diagram of Weaving Control System

"Y" and "N" refer to Yes and No individually.

3.5 Configuration of the Weaving Control System

These are some settings such as folder settings to direct the related files used by Weaving Control System to the correct paths and some specific settings to make Weaving Control System focus on the weaving machine and jacquard types. Unless these settings are set since there will be no default parameters or values, Weaving Control System can never be started. These settings should be first things that must be done as soon as the Weaving Control System is installed on the system.

3.5.1 Folder Settings

First settings that should be done in the Weaving Control System configuration are folder settings. In these settings, related folders (folders that store the datas about weaving process) should be directed to the related paths for a proper weaving process. In case of mismatching situation between the folders used by Weaving Control System and the paths, a failure occurs in running of Weaving Control System and it can never be started. (It also warns the operator with a warning message) Folder settings can be reached by the marked part in red on the first window of Weaving Control System as shown in Figure 3.3 in the window that will be opened after clicking “Ayarlar” button. Folder settings window can be seen in Figure 3.2.

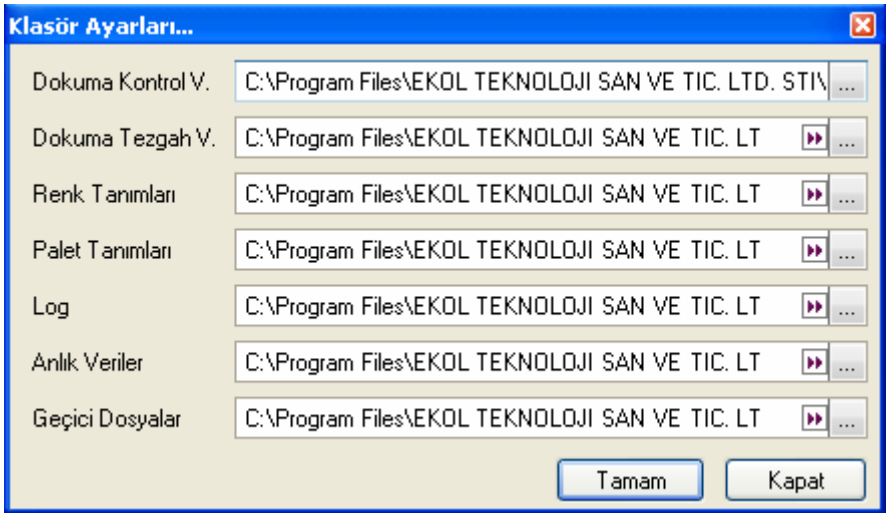


Figure 3.2 Folder settings window

Folder settings should be as given below;

1. Dokuma Kontrol V. (Weaving Control Datas): C:\Program Files\EKOL TEKNOLOJI SAN VE TIC. LTD. STI\Dokuma Kontrol Sistemi\Data\
2. Dokuma tezgah V. (Weaving Machine Datas): C:\Program Files\EKOL TEKNOLOJI SAN VE TIC. LTD. STI\Dokuma Kontrol Sistemi\Machine\
3. Renk tanımları (Color Order Definition): C:\Program Files\EKOL TEKNOLOJI SAN VE TIC. LTD. STI\Dokuma Kontrol Sistemi\ColorOrderDefinition\
4. Palet tanımları (Palette Definitions): C:\Program Files\EKOL TEKNOLOJI SAN VE TIC. LTD. STI\Dokuma Kontrol Sistemi\ColorPalette\
5. Log (Log): C:\Program Files\EKOL TEKNOLOJI SAN VE TIC. LTD. STI\Dokuma Kontrol Sistemi\Log\
6. Anlık veriler (Instant Datas): C:\Program Files\EKOL TEKNOLOJI SAN VE TIC. LTD. STI\Dokuma Kontrol Sistemi\Temp\
7. Geçici Dosyalar (Temporary Files): C:\Program Files\EKOL TEKNOLOJI SAN VE TIC. LTD. STI\Dokuma Kontrol Sistemi\Temp\

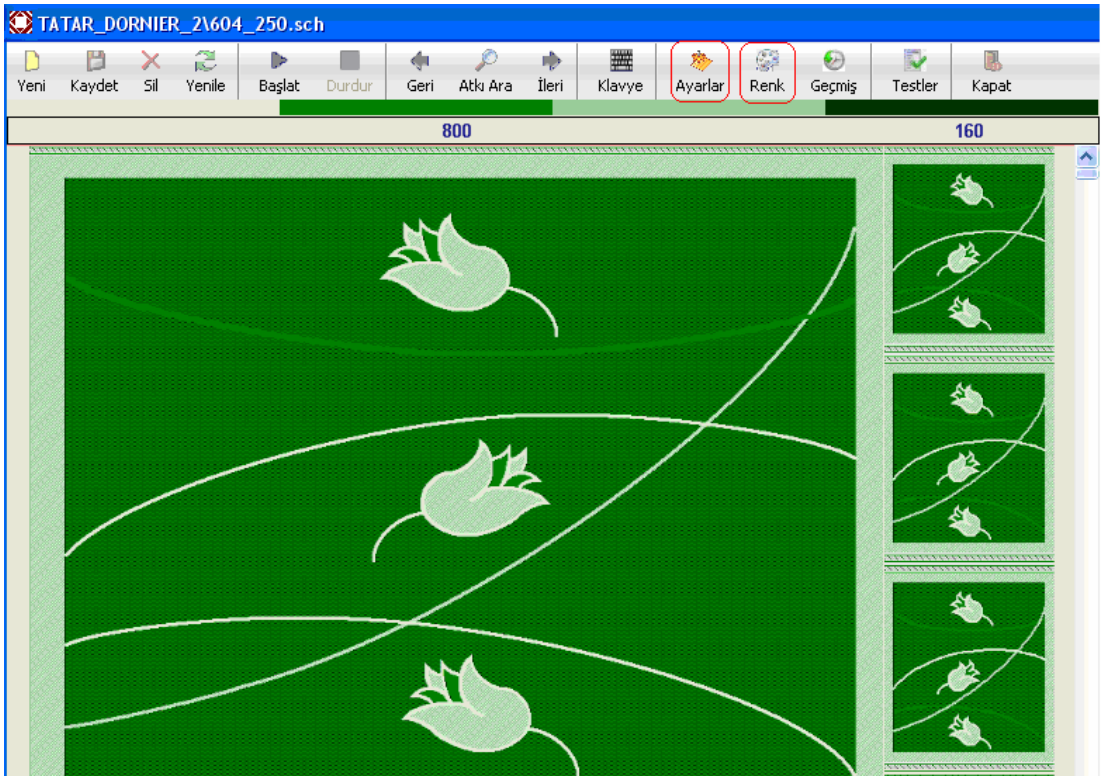


Figure 3.3 First Window of Weaving Control System with a random design

Sub folders; Data, Machine, ColorOrderDefinition, ColorPalette, Log are spontaneously generated together with the installation of Weaving Control System, but "Temp" folder is Window's own Temp one and not generated again together with the installation.

Since Weaving Control System has mostly been designed for Industry of Turkey, all the labels and other titles that can be seen on the windows of Weaving Control System are in Turkish. Necessary translations (from Turkish to English) will be done for a better understanding.

3.5.2 Weaving Machine Specifications

In this part of Weaving Control System, specifications of the weaving machine in details as shown in Figure 3.5 should be entered to the proper blanks manually and by directing the related folder to the correct paths that Weaving Control System utilizes. This window can be reached by clicking the button marked in red as shown Figure in 3.4 in the first window of Weaving Control System.

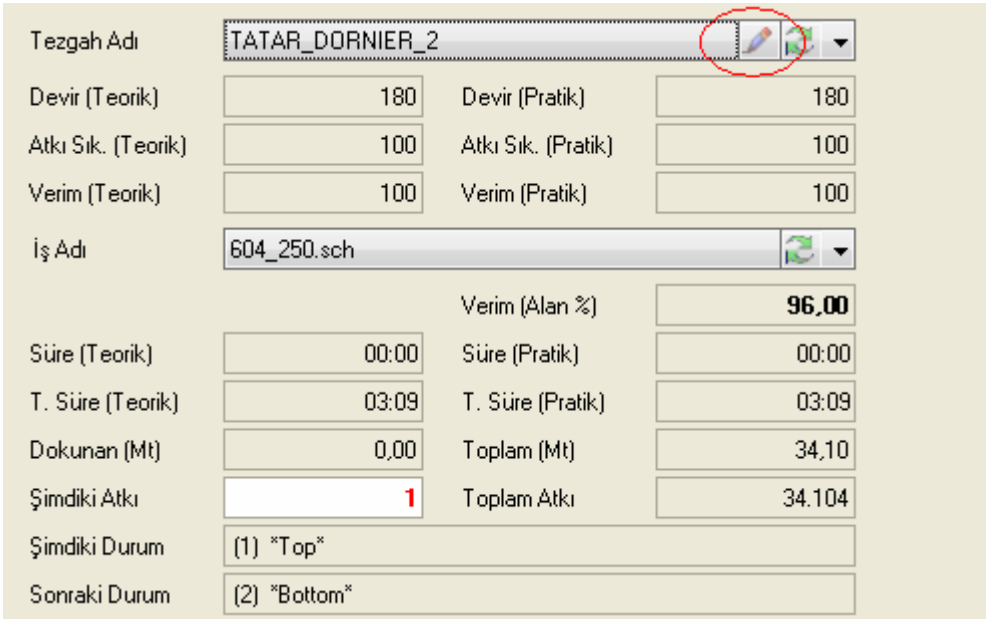


Figure 3.4 Another view of first window of Weaving Control System to reach weaving machine specifications window

In Figure 3.4, also, some statistical datas can be seen about the processing of the weaving such as theoretical datas, (speed of the weaving machine in terms of rpm, efficiency, and total time) practical datas (speed of the weaving machine in terms of rpm, efficiency, and total time) that are yielded and the situation of the current weft according to the weaving type.

Specifications of the weaving machine can be listed as;

1. Name of the weaving machine
2. Name of the operator
3. Operator password
4. IP Number of the weaving machine
5. Total number of grids in the reed of the weaving machine
6. Number of grids of the reed in the weaving machine per meter
7. Number of colors (number of threads in different colors that weaving machine has loaded on its creel.)
8. Space (unused grids) on the left (in terms of the weaving machine's grids)
9. Space (unused grids) on the right (in terms of the weaving machine's grids)
10. Space for cutting material being woven (in terms of the weaving machine's grids.)
11. Number of the wefts in 10cms (theoretical and practical)
12. Ground file (standard weaving data for the unused grids on the left and right)
13. Data for harness plan
14. Color order definitions
15. Job orders file path (*.pdf, *.sch)
16. Design file path (*.bmp)
17. Processed file path (*.ekj)
18. Weaving type (such as 1/1, ½, ⅓)
19. Maximum length of job order (length of the material being woven in meters)
20. Weaving speed of the weaving machine (RPM)
21. Efficiency of the weaving machine as can be found as;

Efficiency = ((Practical Speed/Theoretical Speed)*100) (Eqn. 3.1)

As it should be done in folder settings, process of directing the related files to the correct paths should be done in weaving machine specifications as well. These settings should be as given below;

1. İş D. Yolu(*.bmp) (Job File Path): C:\Program Files\EKOL TEKNOLOJI SAN VE TIC. LTD. STI\Dokuma Kontrol Sistemi\DKSveri\Is\
2. Desen D. Yolu(*.ekj) (Design File Path): C:\Program Files\EKOL TEKNOLOJI SAN VE TIC. LTD. STI\Dokuma Kontrol Sistemi\DKSveri\BMP\

.ekj is a special type of data format that can be obtained from the conversion of .bmp image file to digital datas and invented by Ekol Teknoloji.

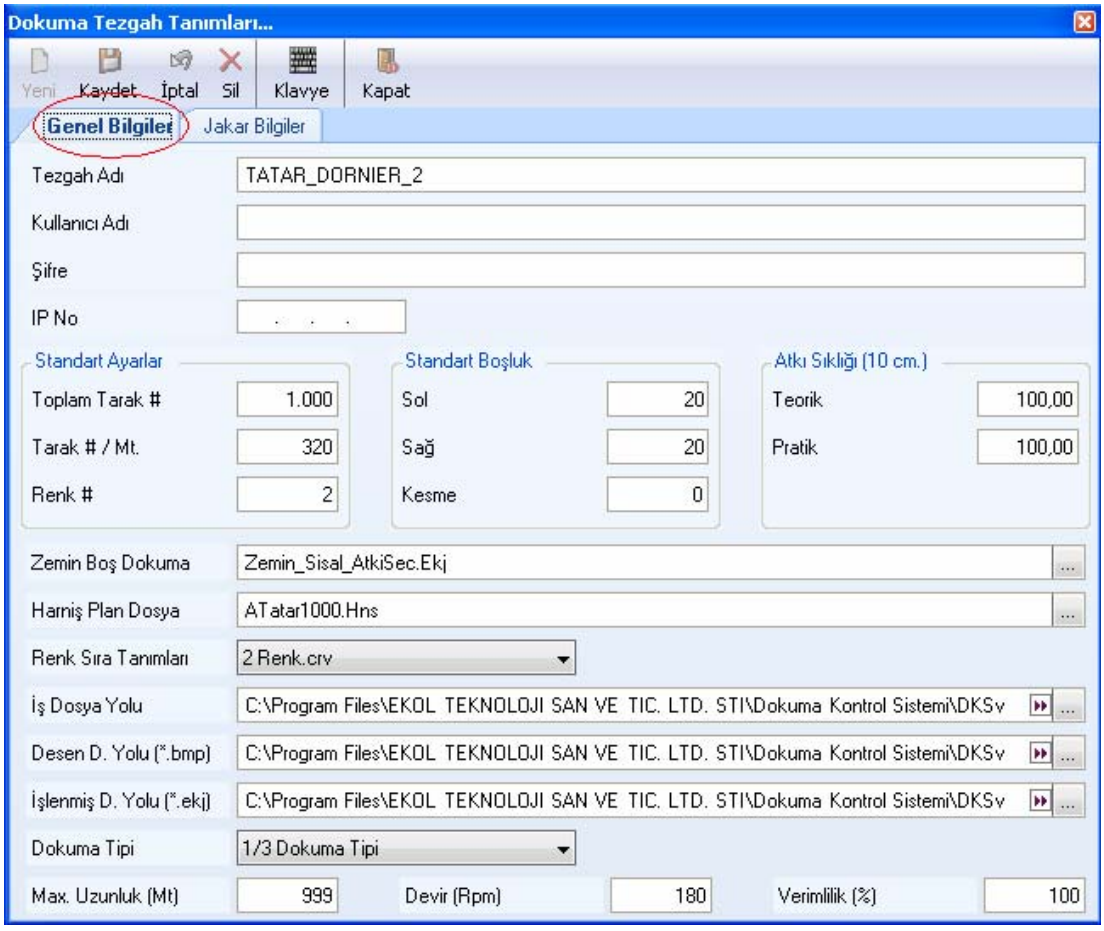


Figure 3.5 Weaving machine specifications window

3.5.3 Jacquard Specifications

In this part of configurations, as the settings are done for weaving machine, they should be done for the jacquard that is installed on the weaving machine since weaving machine and jacquard can be regarded as machines independent from each other. These settings are;

1. Name of the weaving machine
2. Type of the jacquard on the weaving machine (only Takemura type for 1.0 release of Weaving Control System)
3. Number of solenoid cards on each jacquard portion (A, B, C, as can be seen in Figure 3.6.)
4. Number of solenoids (piezoelelectric materials) on each electronic card
5. Number of the wefts skipped in pick finding
6. Type of transmitting data (left to rite, right to left)
7. Maximum triggering time (In case of any failure situation, it is the term that defines the maximum duration lasting in seconds for stopping working of weaving machine after Weaving Control System stops communication and sending data to the jacquard. As a standard, this period of time is 39 seconds but by the help of the Weaving Control System, this duration will be able to be adjusted.)

Figure 3.6 shows the related window of the Weaving Control System for jacquard specifications.

Transmitting data from left to right or right to left is an important selection, since to define the first solenoid card as starting reference. If the reference is defined as “from left to right” data is transmitted from left to right and continue to be transmitted to the other solenoid cards and each portion of jacquard in the same order but if it is selected as “from right to left”, in contrast to former procedure given, data is transmitted from right to left and continue to be transmitted in the same order.

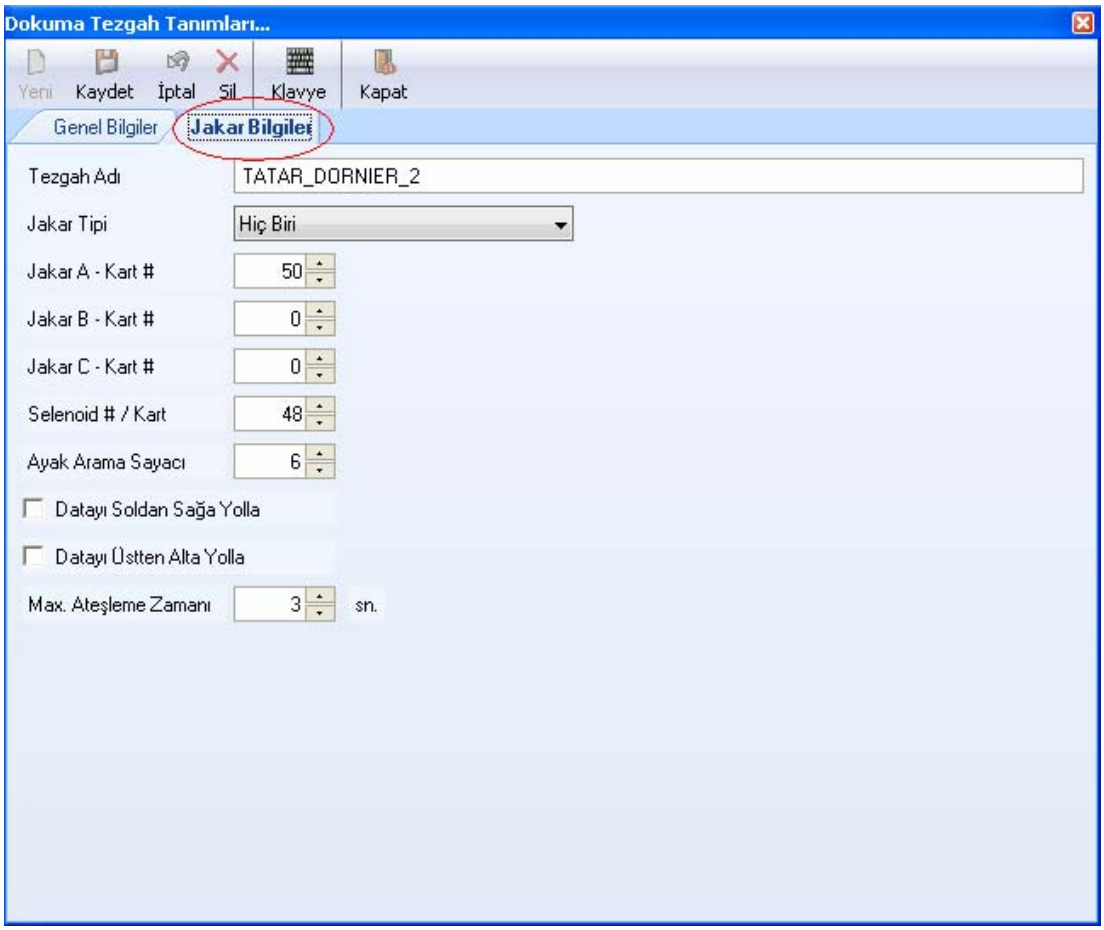


Figure 3.6 Jacquard specifications window

If the self-stopping system wouldn't exist, since weaving machine would not be able to get new design data from Weaving Control System or any communication software, the jacquard would continually process the same pile and defective product would be obtained.

Even though the jacquard type option seems selectable in the Version 1.0 of Weaving Control System. Jacquard type is fixed as Takemura type jacquard for first release of Weaving Control System but in the following versions of it, it will be configured for different types of jacquard such as Bonas and Schleicher types of jacquard.

According to weaving machine and jacquard specifications entered by the operator, weaving process can be started for the job orders that have been generated before or new ones.

3.6 Job Order Files

In computer science, *Job* is the unit of work that a computer operator (or a program called a job scheduler) gives to the operating system. *Job order* is the order that is given to the operating system by the program running together and *job order files* can be easily defined as all the files related to the same job order.

3.6.1 Street (Part) Files (*.pdf)

In weaving terminology, a *street* can be defined as the place that the weaving process takes place and the carpets or the other things (towel, fabric etc.) that are being woven can be observed. As by the well known definition of the street, we can see materials being woven on the street as if the cars are going on a road. It can product up to 8 different side to side carpet designs on the weaving machine but *the number of grids of the reed that are added to each part must be equal to the number of the grids of that part*. The content of the street file includes;

1. Number of the parts
2. Number of the grids on the left
3. Number of the grids of the parts
4. The unused grids at the end of the part (in terms of number of the grids).
5. Number of the grids of all parts

In Figure 3.7, upper view of the reed of the weaving machine that has 2 parts can be seen, one of them has 800 grids and other one has 160 grids and this reed has 320 unused grids of space on the right and the left (160 grids for each side). Even though the weaving machine normally has a width of 1280 grids. At the end of this chapter, an example about carpet weaving process will be given.

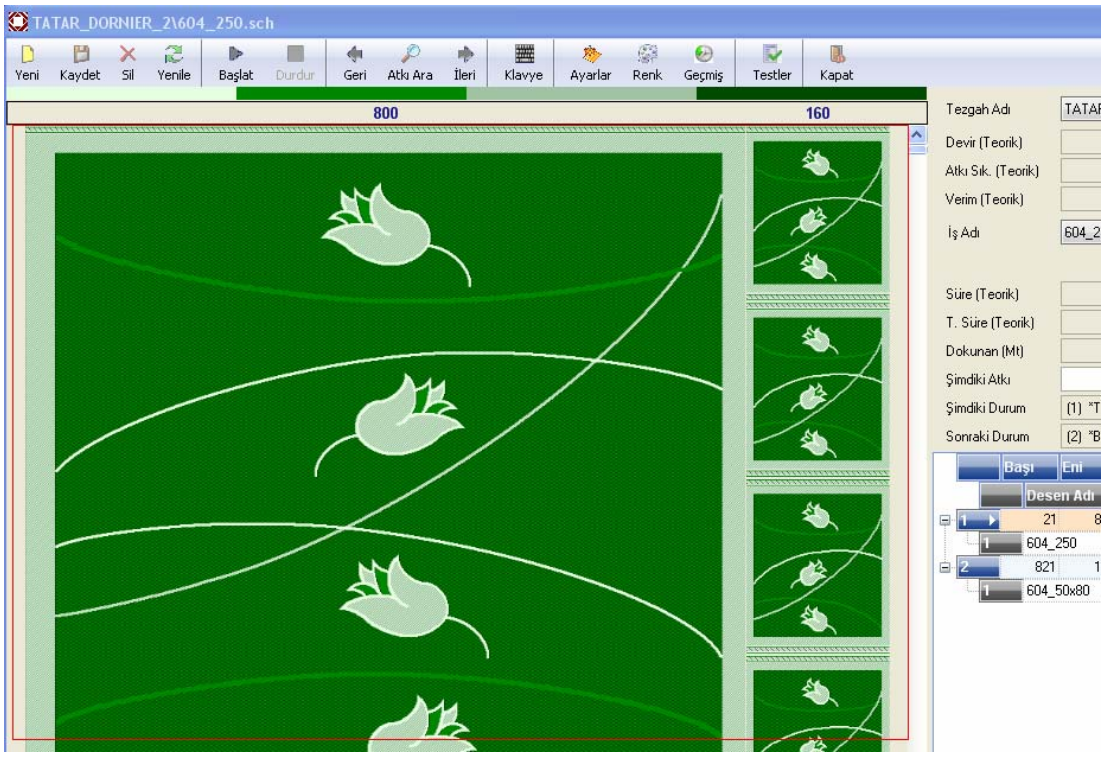


Figure 3.7 A sample view of the reed with two streets (marked in red rectangle)

3.6.2 Job Files (*.sch)

Different designs up to 32 (all of them must have *same* width in terms of grids) can be added to each street that is defined in the street file. The content of the job file includes;

1. Number of the parts
2. Street file
3. Total number of the grids of the part
4. Number of the grids of the part*number of the colors of the weaving machine
5. Number of the wefts of each design (including the space (unused grids at the beginning and the end)
6. The space (unused grids) at the beginning of each design (in terms of the grids)
7. The space (unused grids) at the end of each design (in terms of the grids)
8. The name of each design
9. Number of repeats for each design

We can easily conclude that the maximum number of different designs that can be woven simultaneously is 256. From the equation;

8 different designs side to side*32 different designs on the same street = 256 different designs (Eqn.3.2)

3.6.3 Processed Design Files (*.ekj)

It is the form of design data converted from bitmap format to color-reed matrice. The content of the processed file includes;

1. Number of the grids of the part*Number of colors of the weaving machine
2. Weft number
3. Pile information. For each noose, it means that the length of pile as data in terms of bytes can be found as given below

(Number of grid of the part*Number of the colors of the weaving machine-1)/8+5 (Eq. 3.3)

Equation 3.2 was found by experimental methods not by any analytical ones.

4. Number of total wefts

3.7 Other Files

These are other files that Weaving Control System utilizes during the weaving process.

3.7.1 Color Palette Files

It is the file formed from color information and used for generating the “Color Order File”. Figure 3.8 shows the configuration window for color palette. Purpose of color palette files is that operator selects how many and what colors of threads will be used in the weaving. To form this file, operator firstly picks the color palette from the drop-down list that includes some information such as what kind of palette and how many colors it has. After the palette is picked, desired colors are picked from the row

corresponding to the color palette picked before. If the operator can not find the desired color on the corresponding row, he may use Red Green Blue (RGB) standard to form the desired color. After this file is generated by the operator, the weaving machine can not use different colors than the ones operator picks. Color palette window can be reached by clicking the button “Renk” on the first window of Weaving Control System in Figure 3.3

There is an important point that must not be ignored; operator must choose the colors on the palette according to the colors of the threads loaded on the creel of the weaving machine. Briefly, operator must check the colors of the threads firstly, and then he must form the color palette.

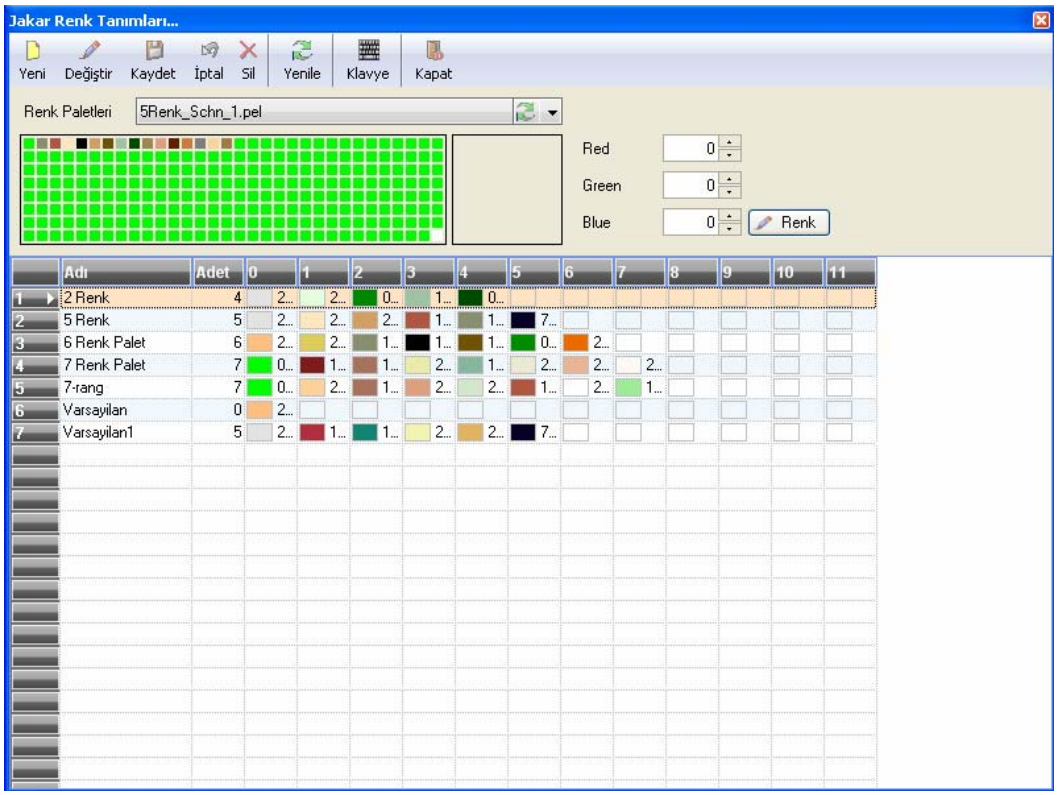


Figure 3.8 Color palette window

3.7.2 Color Order Files

It is the file used for redrawing the design according to the colors loaded on the weaving machine and including the color information. In case of that the desired

colors for the weaving process does not exist on the weaving machine, Weaving Control System selects the most similar colors to the desired colors from the colors loaded on the weaving machine.

3.7.3 History Files

There are two types of history files that store the necessary datas about the weaving process.

3.7.3.1 Main History Files

Main history files store the general information about the weaving process given below.

1. Beginning of weaving (exact time of the beginning of the weaving process)
2. Ending of weaving (exact time of the ending of the weaving process)
3. Weaving machine failure

3.7.3.2 History Files for Calculating Efficiency

These are the files that use the datas about variables given below;

1. Forming the design
2. Changing the design
3. Beginning of weaving
4. Stopping weaving
5. Forward pick finding
6. Back pick finding

and also use the datas about variables given below together with ones given above to calculate the efficiency of the weaving machine.

1. Elapsed time of the weaving

2. The pile currently being woven
3. Measured speed of the weaving machine
4. Expected speed of the weaving machine
5. Number of total wefts

Even though forward pick finding is possible in the sense of software, it is senseless to use forward pick finding in real applications, back pick finding is used to correct the defective part of the carpet being woven and return to the correct weft. Since anybody and any machines can not estimate that the fault may occur in the forward steps of the weaving, there is no need to use the forward pick finding feature of the software in case of any possible failure.

Average speed and speed versus time graphics are plotted for each job order by using these datas and these datas are also used to calculate an accurate efficiency of the weaving machine. A sample graphic (speed versus time) that has been plotted by Weaving Control System can be seen in Figure 3.9.

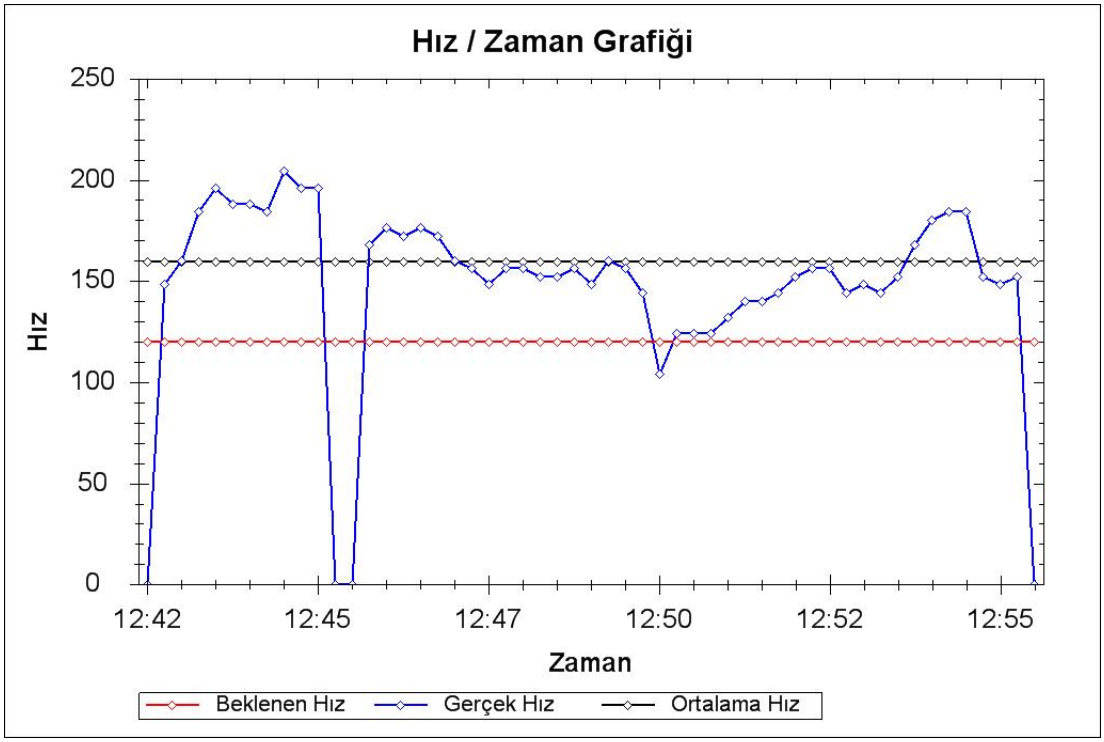
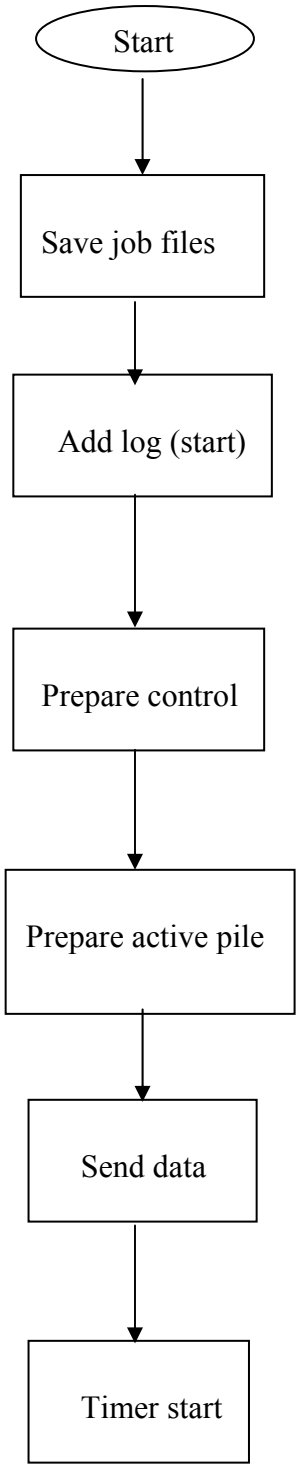


Figure 3.9 A sample graphic with its variables (speed versus time)

3.8 Algorithm Steps of the Process of Weaving

3.8.1 Starting the Process of Weaving



⇒ Process starts manually by the operator by using Weaving Control System.

⇒ For the job, job files, .pdf and .sch are created in RAM of the computer and saved in hard drive of it.

⇒ For the current job, the log file that holds the datas such as, type of weaving, total weft, speed of weaving are added to the current job files.

⇒ States of the sensor, T2 is checked and if its state is logic 1, T1 sensor is allowed to send the related pile data. (T2 sensor can be regarded as the enable signal generator.).

⇒ After enable signal is received from sensor T2, with the signal from T1 (logic 1) active pile data is prepared and sent to the jacquard.

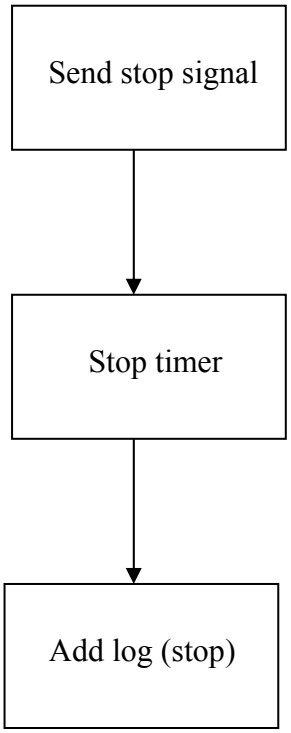
⇒ Related pile data prepared before is sent to the jacquard.

⇒ Timer is started to create a delay between two adjacent pile datas.

Figure 3.10 Flow chart of starting the process

In the log step of the starting the process of weaving step, log file is created together with the starting the process of weaving and also updated since the starting of the weaving is also an event that occurs during the process of weaving. It is important that the log file is generated together with the starting of the weaving since it would cause the weaving process to slow down if it was generated after the weaving process starts.

3.8.2 Stopping the Process of Weaving



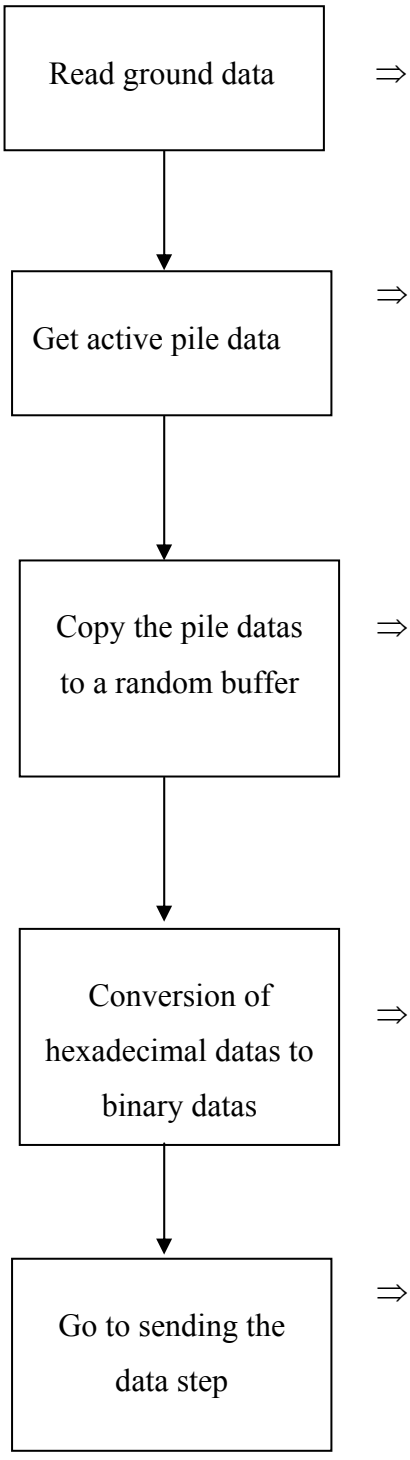
⇒ Stop signal is sent by the operator by using Weaving Control System as it is in the start step.

⇒ Timer is stopped to avoid the process to continue.

⇒ Log file is updated since the weaving machine is stopped and log file is updated in every different events as it is updated in the starting process.

Figure 3.11 Flow chart of stopping the process

3.8.3 Preparing the Pile Data



⇒ Ground data for cloth that will be woven under the carpet is read from ground file to mask with design file.

⇒ Active pile datas are read from all street and ground files.

⇒ Pile datas are buffered to do a comparison with ground file. The size of pile datas must be equal to the size of ground file for the weaving process to begin. Otherwise it never starts.

⇒ After the previous step is succeed, hexadecimal datas are converted to binary ones for the sending data step.

⇒ Datas have been prepared for sending datas step.

Figure 3.12 Flow chart of preparing the pile data

3.8.4 Sending the Pile Data to the Jacquard

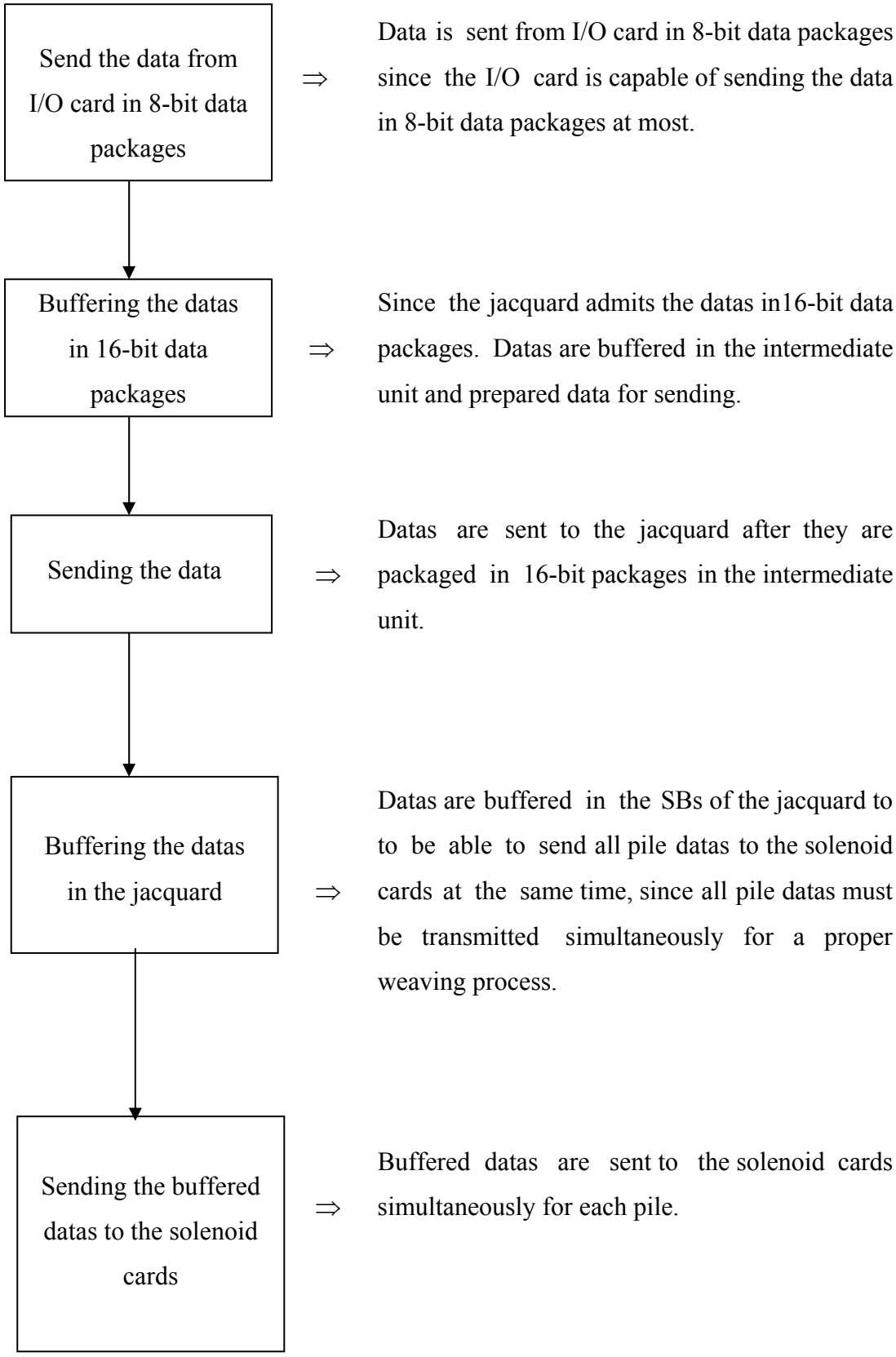
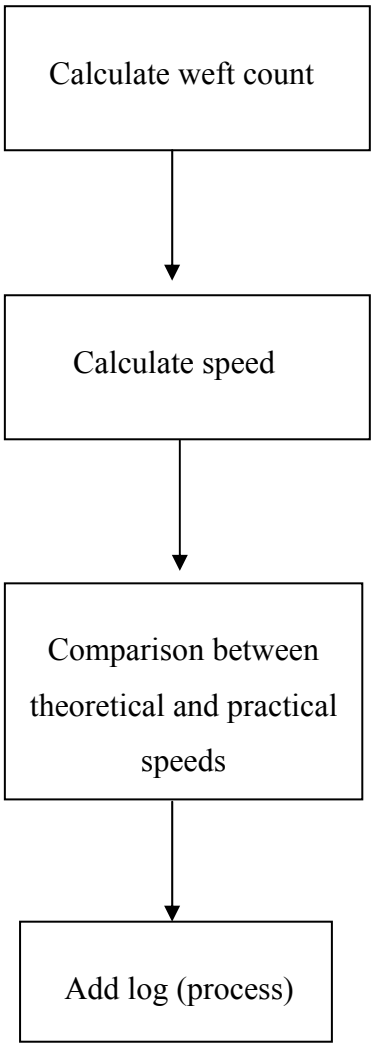


Figure 3.13 Flow chart of sending the data

3.8.5 Holding the Statistical Datas



⇒ Count of the weft is obtained from the weft counter by using sensor signal, every logic 1 signal received from T1 sensor increases the count of weft.

⇒ Speed of weaving is calculated in terms of wefts woven per min.

⇒ Comparision is made between theoretical or expected and practical speeds. Together with the datas obtained, efficiency of the weaving is calculated.

⇒ Log file is updated with the information about about the efficiency of weaving.

Figure 3.14 Flow chart of holding the statistical datas

Even though the steps of the process of weaving can be divided into sub flow charts and algorithms as given in section 3.8 since a whole process of weaving can yield sudden changes in the process, the steps of the weaving process may change the orders in the processing steps.

3.9 An Example on Weaving Control System

To be able to understand the operation of the weaving the carpet by using Weaving Control System, firstly, it is good to be familiar with the properties of the loom and the jacquard studied on.

Table 3.1 Properties of the loom used in the example (also for the study)

Weaving type: Wilton	Branch name: Schöner
Grids per meter in the reed: 320	Maximum number of colors: 6
Number of needles: 7680	Weaving wide: 4 meters
Number of the grids in the reed: 1280	Power of the loom: 60 KW/h
Weaving speed: 125 wefts/min	Number of wefts per 10 cms: 100
Production year: 1996	

Table 3.2 Properties of the jacquard used in the example (also for the study)

Type of the jacquard: Takemura SBS	Number of solenoid cards: 288
Number of solenoids on each card: 28	

As it can be seen in Figure 3.15, there are 3 streets on the whole reed that were created by the operator manually. In the first street, there is 1 carpet that has a width of 640 grids and lenght of 1900 wefts, in the second street, there are 3 carpets that each of them has a width of 256 grids and length of 818 wefts and in the third street, there are 2 carpets that each of them has a width of 256 grids and length of 888 wefts.

By an easy calculation;

1280-(640+256+256)=128 grids of the whole reed are left unused on the rite (Eq.3.4)

On the part left unused, the cloth is woven different than carpet since there is not a design on that part. Furthermore, in the view of the example, some parameters of the weaving procees can be observed by the operator such as, efficiency of the loom, efficiency of the available area, practical speed of the loom, number of total wefts that are being wowen during entire process and for each process etc. As it can be

seen on the same figure, a transparent curtain is warning the operator to indicate which weft of streets is being woven. And also, this curtain is going down by 1 pixel in per two wefts since the weaving type is chosen as ½. All related datas about the weaving process can be seen by view of the entire reed in Figure 3.15.

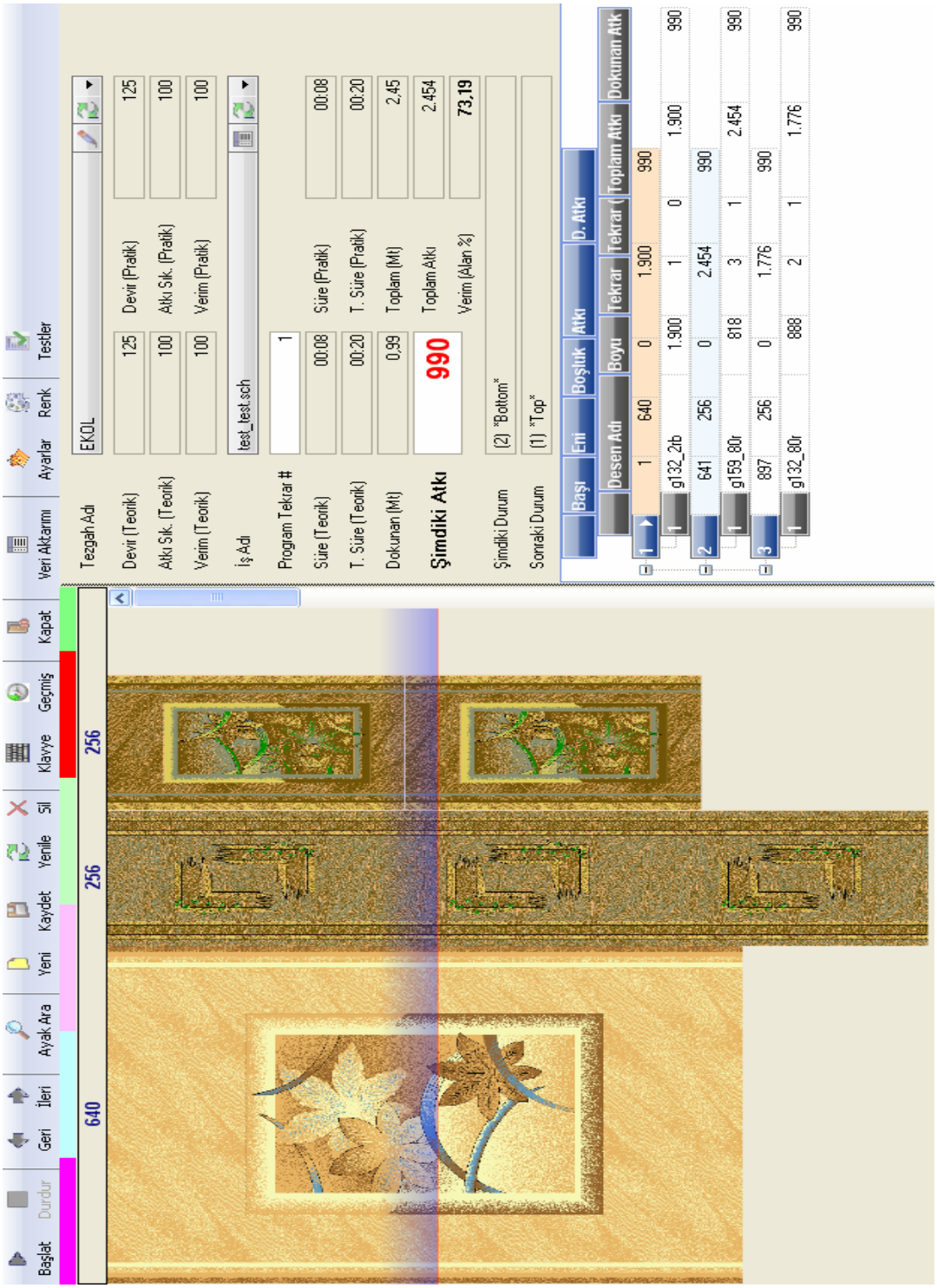


Figure 3.15 Top of view of the reed of the example

CHAPTER 4

SIGNALIZATION AND DATA FLOW OF ENTIRE SYSTEM

4.1 Introduction

In this chapter of the study, the signalization and data flow of entire system will be explained. Communication signals together with intermediate hardwares that are connected to the new system will be given in details and also individual features of each hardware that have been utilized during the study will be represented as well. Finally, the summary of signalization of entire system will be described.

4.2 Communication Signals Connections between I/O Card and Jacquard

In this section of the last chapter, communication signals connections between I/O card and jacquard will be represented. Diagram of these signals can be seen in Figure 4.1. As mentioned in chapter 3, first port (P1) of the hardware designed is configured as “output” that means all design datas are transmitted from this port to the jacquard and second port (P2) is configured as “input” to be able to receive the datas from photo sensors. Therefore, the direction of data flow may be realized in two ways;

1. From computer (I/O card) to the jacquard for transmitting design data and some control signals such as stop signal.
2. From weaving machine to the computer for transmitting the signals from photo sensors for the operations such as counting the number of weft and generate enable signals for the weaving process.

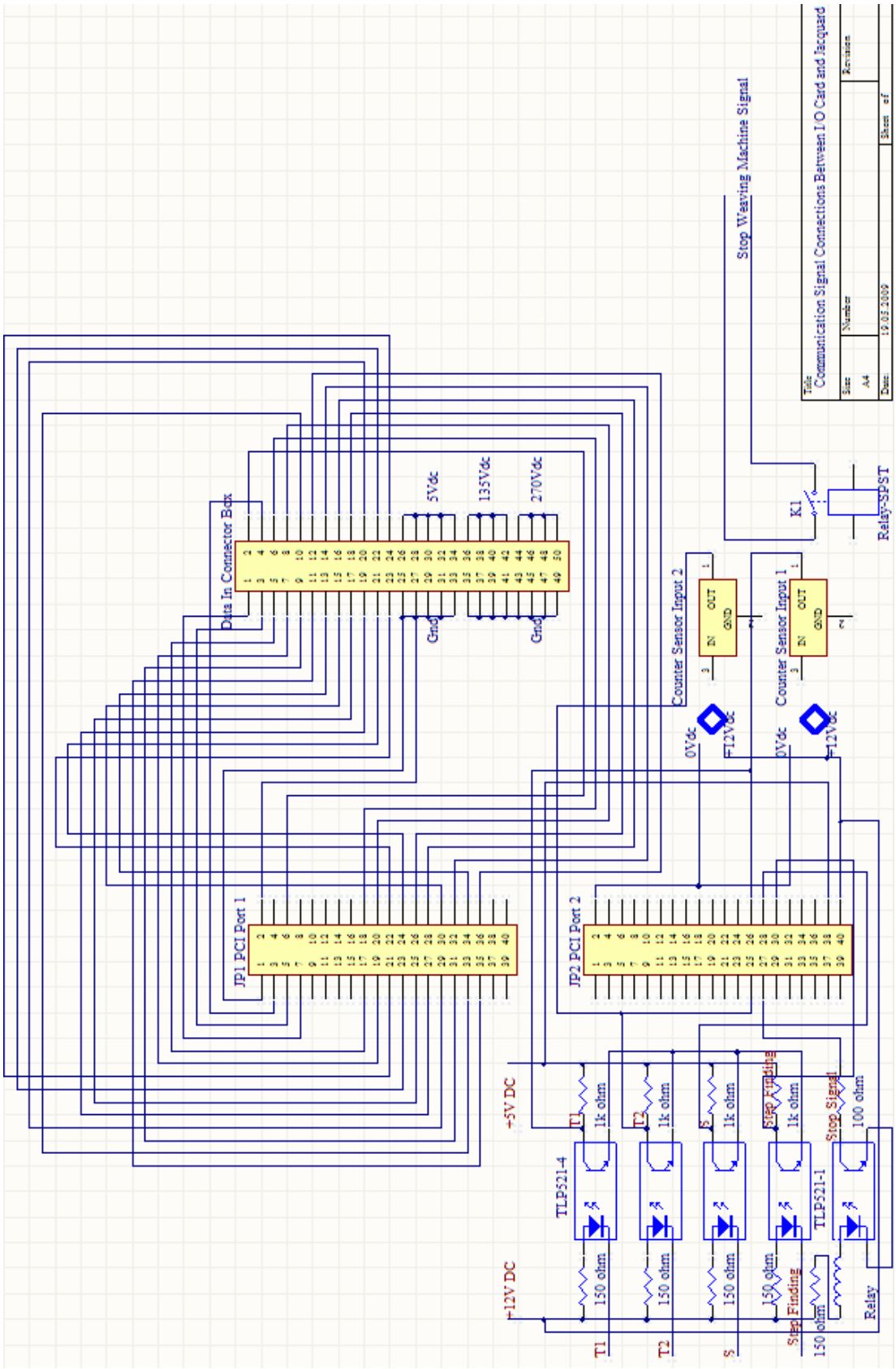


Figure 4.1 Signals connections between I/O card and jacquard

According to the principles of jacquard mechanism, the photo sensors, T1 and T2 are used to provide a proper communication between jacquard mechanism and software being used. These photo sensors are activated by an iron bar operating together with the weft engine. While the weft engine is ON, it rotates the iron bar that activates the sensors. Since this bar makes circles around itself, it passes through the space that already exists in the middle of the sensors and when it *firstly* passes through the space of the second one (T2) and *secondly* passes through the space of the first one (T1). Hence, software receives the signal that it must send the necessary data of the related pile and content of counter of weft is increased by 1, otherwise it never sends the data and weaving process does not realize. In Figure 4.2, a simulation mechanism for the sensors that works with a little electrical engine can be seen. In this simulation, whether the jacquard mechanism and Weaving Control System can operate properly or not by using sensor signals is intended.

Figure 4.2 T1 and T2 sensors with an electrical engine to simulate the mechanism

The type of the photo sensors utilized in this study is EE-SX67Q and utilize the voltage that they need to operate properly on the pin of the I/O card that yields +12 V. It is obvious that if the optocouplers hadn't been used in this study since the sensors would have generated a +12V level as a communication signal, I/O card designed in this study would have been damaged by the voltage being generated by the sensors. Even though the I/O card is capable of yielding a +12V level for any purpose, it is not capable of receiving a signal having +12V level as a communication one. It **must** be +5V.

To be able to stop the weaving machine by using stop signal via Weaving Control System; when the stop signal is transmitted, this signal is sensed by the optocoupler and transmitted as a +12V signal level that energizes a relay. As a result of energizing of relay, another signal is sent to the PLC system of weaving machine that means "stop the weaving machine."

4.2.1 Why Optocoupler?

In electronics, an **optocoupler** (or **optical isolator**, **opto-isolator**, **photocoupler**, or **photoMOS**) is a device that uses a short optical transmission path to transfer a signal between elements of a circuit, typically a transmitter and a receiver, while keeping them electrically isolated, since the signal goes from an electrical signal to an optical signal back to an electrical signal, electrical contact along the path is broken [6]. A simple optocoupler can be seen in Figure 4.3.

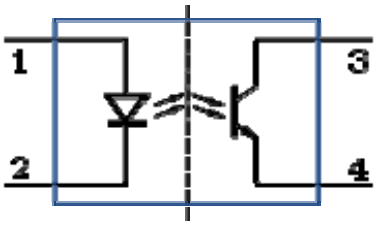


Figure 4.3 Optocoupler

Why optocoupler is used in this study is to be able to keep the presence (+12V) or absence (0V) of the communication signals generated by the sensors in +5V or 0V

levels and isolate the I/O card from the jacquard mechanism in case of any damageful failure that may occur. Types of optocouplers utilized are TLP521-4 and TLP521-1 and in the representation of optocouple package, TLP521 refers to type of optocouplers and the number after dash refers to how many of them there are in the package.

4.2.2 Transformation from Electrical Signals to Mechanical Movements

At this point, one of the most important issues is probably to transform the data signals to mechanical movements. In jacquard systems, to be able to achieve this transformation, piezoelectricity feature of some materials is benefited. *Piezoelectricity* is the ability of some materials (notably crystals and certain ceramics, including bone) to generate an electric potential in response to applied mechanical stress. This may take the form of a separation of electric charge across the crystal lattice. If the material is not short-circuited, the applied charge induces a voltage across the material. The word is derived from the Greek piezo or piezein, which means to squeeze or press.

The piezoelectric effect is reversible in that materials exhibiting the *direct piezoelectric effect* (the production of electricity when stress is applied) also exhibit the *reverse piezoelectric effect* (the production of stress and/or strain when an electric field is applied) [7].

It can easily be concluded that to transform the electrical signals to mechanical movements, reverse piezoelectric effect on piezomaterial should be used. For this process, one pole of the piezoelectric material is kept constant at +135V and this situation forces the movement to be dependent on only the other pole of it. Voltage signal that carries the data is applied to the Darlington Transistor for switching. If the voltage applied is;

- 0V (logic 0), Darlington Transistor is in OFF state that means no switching, it applies 0V to the other pole of piezoelectric material that means no data and no movement (even though a current passes through the piezoelectric material), steady position remains, as shown in Figure 4.4

- 5V (logic 1), Darlington Transistor is in ON state that means switching exists, it applies 270V to the other pole of piezoelectric material that means data exists, movement realizes and piezoelectric material shifts to left, as shown in Figure 4.5

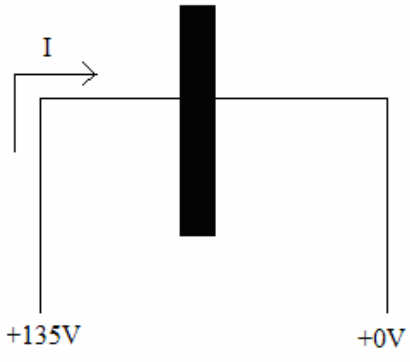


Figure 4.4 Steady position

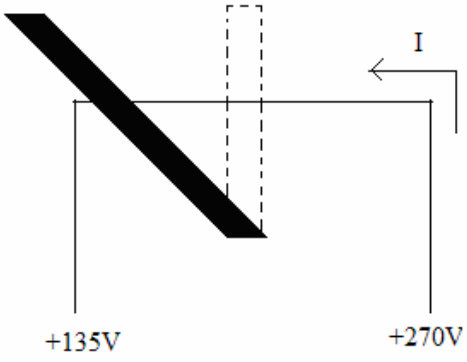


Figure 4.5 Shift left

In Figures 4.4 and 4.5, black and thick lines represent the piezoelectric material under the effect of the current passing through the circuit.

It can be easily concluded that the direction of the movement of the piezoelectric material is determined by the *direction of the current.* In Figure 4.7, locations of piezoelectric materials in a solenoid card can be seen and also that the piezoelectric material is keeping its steady position (on the right, but it keeps the plastic part pinned on it on the right since the plastic part is also pinned to a pivot point) when it is off. (Figure 1.9 can also be seen to understand better the principles of solenoid cards)

If we try to describe the data in mechanical sense; we have learned that when the data exists, plastic part on the piezoelectric material shifts *right.* By this movement, pins in different (see Figure 4.10) colors and also stressed by a spring mechanism enter into the holes showed in Figure 4.6. Therefore, the weaving procedure described in section 1.5 for punch cards realizes for solenoid cards as well. We can easily say that the “sense of weaving for electronic jacquards and mechanic ones are the same.” The holes on the punch cards do the same job of what the holes on solenoid cards do.

Figure 4.6 Crossection of a solenoid card and its holes on it

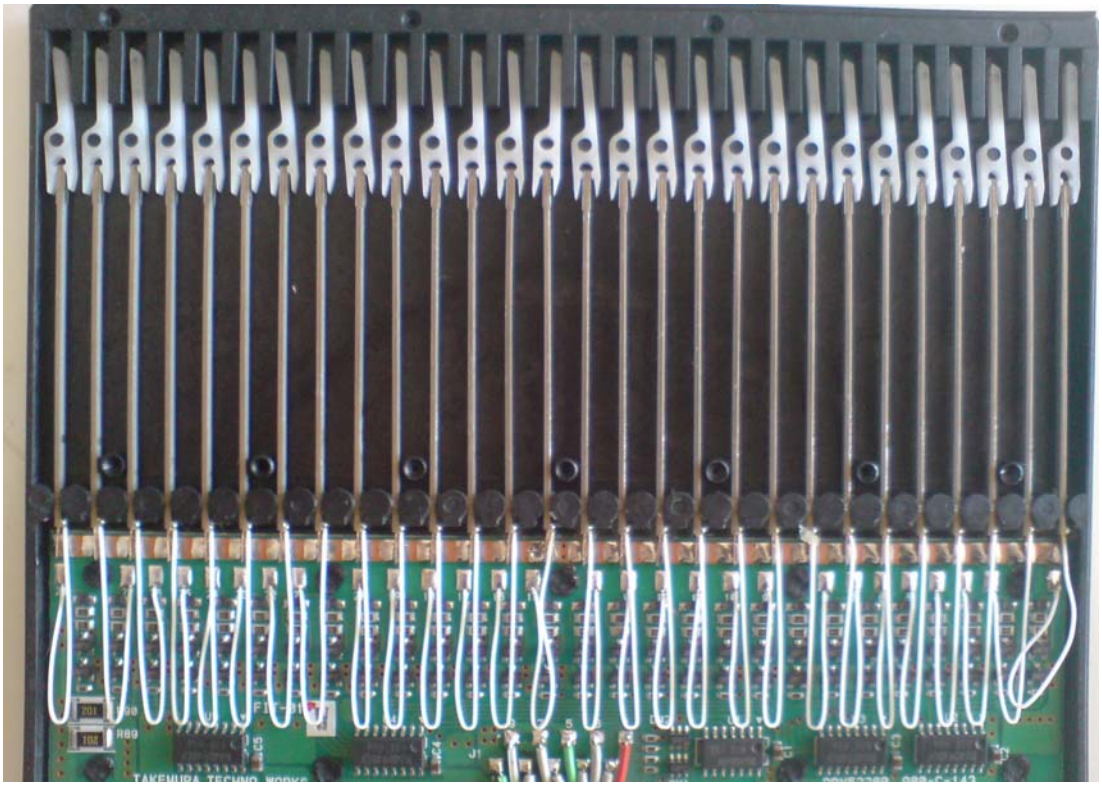


Figure 4.7 Inner view of a solenoid card

4.2.3 Data Transfer to Solenoid Cards

The first thing that can be said about the type of data transfer to solenoid cards is that it is *serial transfer*. This serial transfer is provided by the shift *registers* existing in 4094 integrated circuits that have 8 shift registers in the same package. A digital system is said to operate in a serial mode when the information is transferred and manipulated one bit at a time. The content of one register is transferred to another by shifting the bits from one register to the other one. The information is transferred one bit at a time by shifting the bits out of the source register into the destination register [9]. In Figure 4.8, serial data transfer can be seen with shift registers. In this figure, the outputs, Q1, Q2, Q3, and Q4 refer to the signals that are transmitted to the Darlington Transistor for switching operation.

Shift register is a register capable of shifting its binary information either to the right or to the left. The logical configuration of shift register consists of a chain of flip-flops connected in cascade, with the output of one flip-flop connected to the input of the next flip-flop. All flip-flops receive a common clock pulse that causes the shift from one stage to the next.

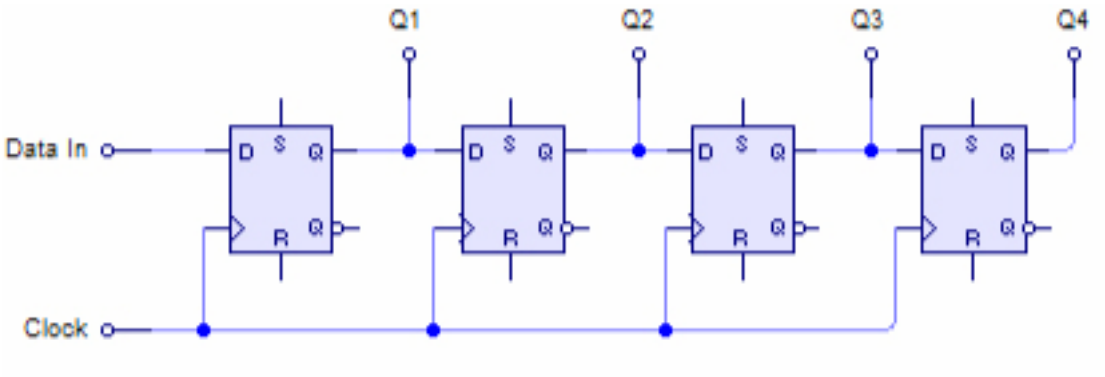


Figure 4.8 Serial data transfer with shift registers

The truth table of D flip-flop being used in serial transfer process can be seen in Table 4.1. It shows that the next state of the flip-flop is independent of the present state since Q (t+1) is equal to input D whether Q is equal to 0 or 1. This means that an input pulse will transfer the value of input D into the output of the flip-flop independent of the value of the output before the pulse was applied. The truth table shows clearly that Q (t+1) is equal to D [9].

D flip-flop also has S (set) and reset (R) master inputs for further and more complicated applications. Since we don't need these inputs in our study, they may be unconnected and also since these inputs do not receive any signals, they don't cause any problems in the operating of the flip-flops. Related truth table about the master inputs of D flip-flop can be seen in Table 4.2.

Table 4.1 Truth table of D flip-flop

Q (t)	D	Q (t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Table 4.2 Truth table of master inputs

S	R	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	No Change

4.3 Summary of Signalization of Entire System

If we try to understand the principles of the signalization of entire system with a random data (from computer to the weaving machine) by following the path it is following as enumerated below;

1. The random data is transmitted by the help of Weaving Control System and using the output port of the I/O card.
2. This data is transmitted to an intermediate unit to transmit this *parallel* data together with the necessary voltages 0V, +5V, +135V, 270V for the correct operation of solenoid cards as mentioned before. (Buffering the datas from 8 bits to 16 bits also realize in this section.)
3. Data and other voltages are transferred to the connector box by the help of the connector cable, as shown in Figure 4.9.
4. Datas are transferred to solenoid cards with respect to the sense of the software.
5. Mechanical movement realizes or not depending on whether the bits of data is logic 0 or logic 1.

Figure 4.1 can be seen again to follow better the procedure given above.

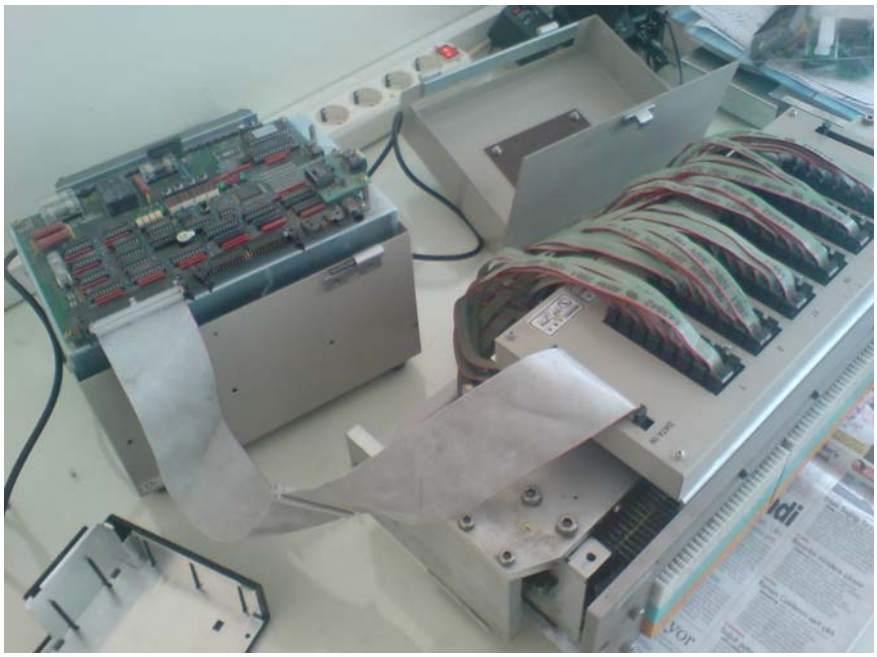


Figure 4.9 Connection of intermediate unit to the connector box

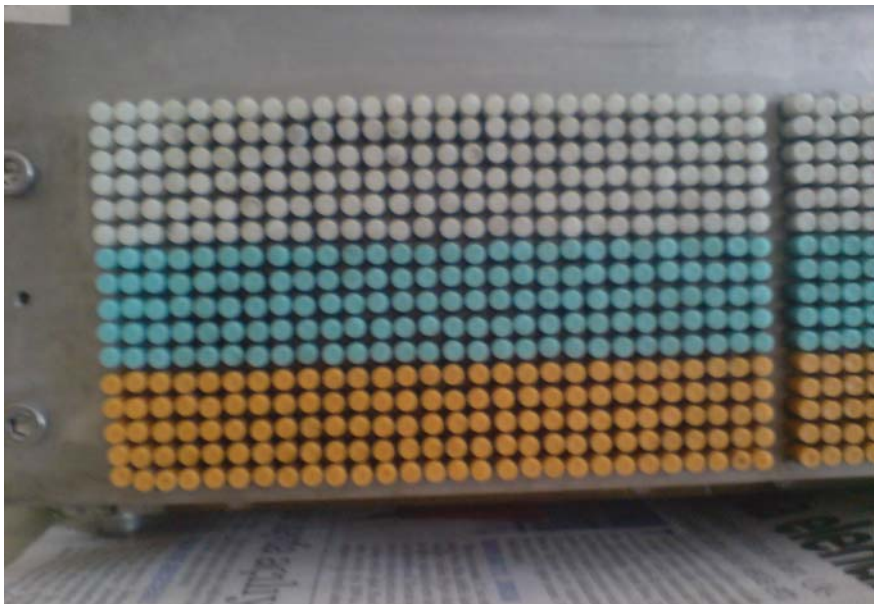


Figure 4.10 Front view of 1/3 portion of selection box for endless paper

Each solenoid card has 28 piezoelectric materials in it as shown in Figure 4.7 and it can be easily understood that each piezoelectric material represents one bit (from the information given before). If we observe the front view of a selection box for endless paper we can see that there are 28 pins in each column of pins in colors white, light

blue and orange and there are 16 rows in 1/3 portion of selection box, so it is the best way to transfer the pile data to the solenoid cards in the form of 16 by 8 matrices by using the array feature of the software as it can be seen in Figure 4.12. after three groups of pile datas (16 by 8) are transferred to the solenoid cards, for the fourth groups of pile datas, last four pins of 1st 1/3 portion and first four pins of 1/3 portion of 1st selection box form another group of pile datas and go on in this way for the 3rd portion too. To transmit the pile datas data to the other selection boxes of the jacquard, another connector cable is used to transmit it from the "Data Out" port of the first selection box as, shown in Figure in 1.9 to "Data In" port of second one and goes on. From the information given above, an equation about the capacity of the data that is necessary to control all the piezoelectric materials;

- 1 solenoid card has 28 piezoelectric materials = Data capacity of it is 28 bits
- 28*16 = 448 bits in 1/3 portion of selection box for endless paper (Eq.4.1)
- 3*448 = 1344 bits are needed to control a selection box for endless paper (entire of it can be seen in Figure 4.11) (Eq.4.2)
- Since the design data is transmitted in 8-bit packages to the jacquard
- 1344/8 = 168 means that 168 clock pulses are needed to control all the bits (piezoelectric materials) of a selection box for endless paper (Eq.4.3)

Since the calculations can be done for selection box for endless paper and used in this study, different calculations should be done for different types of selection boxes given in chapter 1 in details.

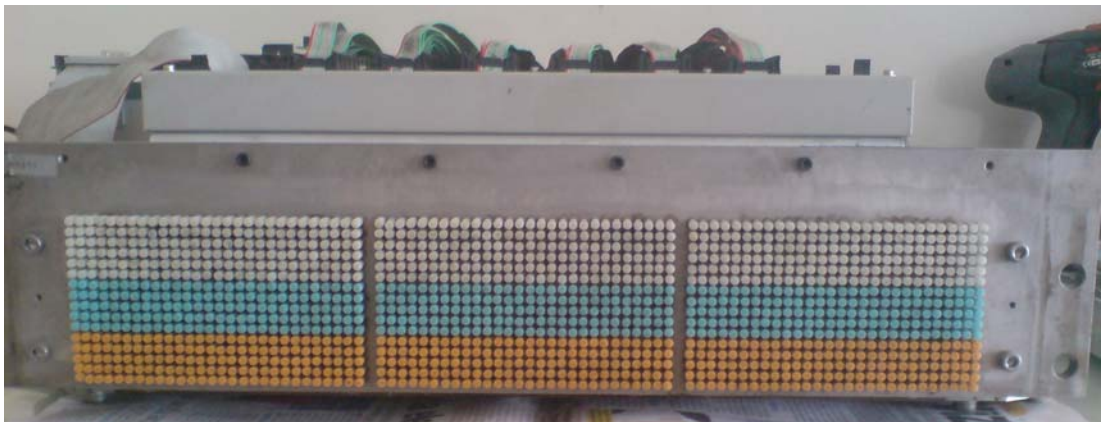


Figure 4.11 Entire front view of the selection box for endless paper

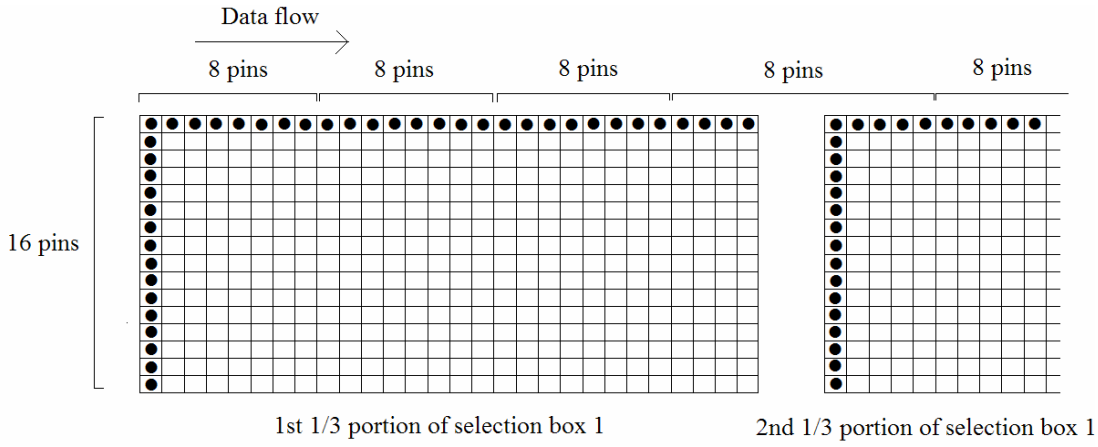


Figure 4.12 Data flow in one selection box

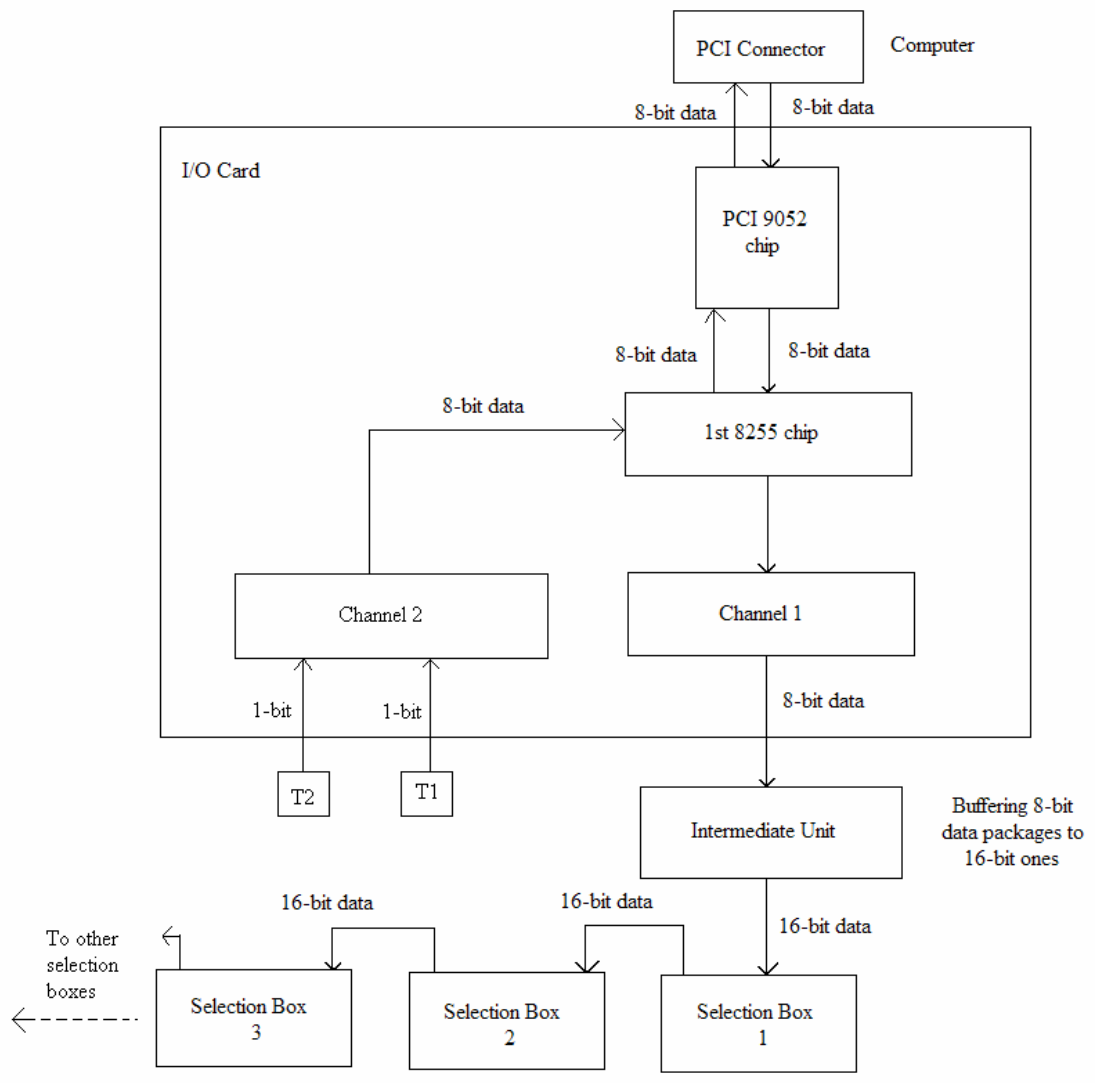


Figure 4.13 Flow of design data for whole system with three selection boxes

Weaving process does not start until the data buffer of the selection box 3 is completely is loaded with design datas. When the data buffer of selection box 3 is completely loaded with design datas, related pile datas are transmitted to solenoid cards and weaving process realizes. Flow of design data for whole system with three selection boxes can be seen in Figure 4.13 more detailed.

CHAPTER 5

CONCLUSIONS

As a result of this study, after the laboratory tests of the new jacquard control system, control mechanism of a Wilton carpet weaving machine that uses Takemura type jacquard has been renewed. Installation of this product has been realized on a factory in Gaziantep and the new system is currently working properly.

In the hardware step of the study, a new hardware that is easily compatible to all modern computer systems has been produced since it uses PCI bus on the computer motherboard. PCI bus type card has especially been selected since this type of bus is sufficiently fast (data transmission/reception) on all applications and that even 10 year old computer motherboards, there are 3 PCI bus slots at least and this situation doesn't cause the problems such as, absence of empty data slots for other components of the computer. Even though the I/O card is produced for this study, since it is programmable it can also be used for any other engineering applications.

In the software step of the study, a new software that is compatible to the new computer systems has been produced. In old systems, it wasn't possible to monitorize the steps of the weaving process. The software installed on these systems is formed by a DOS screen that includes command structures on it. It wasn't even possible to use a mouse to direct the cursor on the user screen. In the new system formed by the software produced in this study, a much more modern user interface is available that the operator can see even each weft of the carpet being woven. While the weaving is processing, a transparent curtain will go down together with the weaving of the carpet to point the step of weaving. Briefly, a new software that is much more user friendly and easier to use has been produced.

In the future work, this study is being planned to apply to Van De Wiele brand weaving machines that use Bonas type jacquards and Schönner brand weaving machines that use Staubli type jacquards with extra modifications on the study. Furthermore, the new system will be able to be configured for different weaving structures and different weaving sectors such as fabric, towel and kilim.

Since this study is focused on the industrial sector, more accurate results by the numbers are being expected in 1 or 2 years after the study is completed. The most important result is that product is supposed to reduce dependency to foreign brands. It is estimated that it will increase the efficiency of weaving, decrease the defective product in a big amount and also, since the system including hardware and software is under our control, also a big decrease in spending money in spare parts is expected.

In Gaziantep, around 250 weaving machines need this modification on their control systems. Same type of weaving machines also exist in İstanbul, Bursa, Kayseri, Denizli, Tekirdağ, Çorum, Manisa and Uşak. Number of these machines are nearly 200 and also this product can also be exported to İran, Özbekistan, Suriye and Ürdün. An estimated number of these weaving machines in these countries are 1500.

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APPENDIX-A

GLOSSARY

Altium Limited

An Australian based software company that provides PC-based electronics design software for engineers.

Bitmap

IBM and Microsoft format specifications for image files.

Bimorph Actuator

Actuators utilizing piezoelectric material in order to achieve small displacement under electric potential.

Bonas Machine Company Ltd.

A designer and manufacturer of electronic jacquards.

CAD (Computer Aided Design)

It is the use of computer technology for the design of objects, real or virtual.

Clock Pulse

The signal (generated by oscillators) used to synchronize the operations of an electronic system.

Connector Box (weaving)

The name of the platform that solenoid cards are connected.

Creel

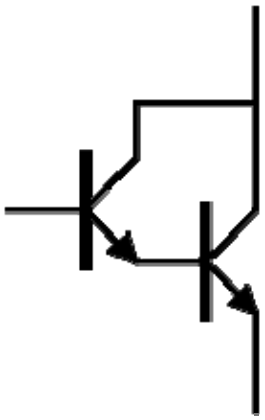
A platform onto which different colors of threads are placed.

Crystal Oscillator

A is an electronic circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency.

Darlington Transistor

A compound structure consisting of two bipolar transistors (either integrated or separated devices) connected in such a way that the current amplified by the first transistor is amplified further by the second one.



Decoupling Capacitor

A capacitor used to decouple one part of an electrical network (circuit) from another. Noise caused by other circuit elements is shunted through the capacitor, reducing the effect they have on the rest of the circuit.

Dos (Disk Operating System)

It is a shorthand term for several closely related operating systems that dominated the IBM PC compatible market between 1981 and 1995, or until about 2000.

.pdf

Abbreviation of Path Definition File.

.sch

Abbreviation of scheme

DPI (Dots Per Inch)

A measure of spatial printing or video dot density, in particular the number of individual dots that can be placed within the span of one linear inch (2.54 cm.)

Ethernet

A family of frame-based computer networking technologies for local area networks (LANs).

Flip-flop

The circuit that can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states.

Gerber file

A file format used by printed circuit board manufacturing machines to layout electrical connections such as traces, vias, and pads (the component "footprints" on the PCB).

IEEE 802.11

It is a set of standards carrying out wireless local area network (WLAN) computer communication in the 2.4, 3.6 and 5 GHz frequency bands.

Jacquard (weaving)

A shedding mechanism attached to the loom that gives individual control of up to several hundred warp threads and thus enables large complex designs to be produced.

Harness (weaving)

A group of cords and their attachments, from the hooks of the machine downwards that control the lifting of the warp threads.

IP (Internet Protocol) Number

A numerical identification and logical address that is assigned to devices participating in a computer network utilizing the Internet Protocol for communication between its nodes.

ITMA (International Textile Machinery Association)

It is the world's largest international textile machinery, is recognised as the 'Olympics' of the textile machinery industry.

Log (Data Logging)

It is the practice of recording sequential data, often chronologically.

Loom

A weaving machine that produces cloth.

Microsoft Visual Studio

An Integrated Development Environment (IDE) from Microsoft that can be used to develop console and graphical user interface applications along with Windows Forms applications, web sites, web applications, and web services in both native code together with managed code for all platforms supported by Microsoft Windows, Windows Mobile, Windows CE, .NET Framework, .NET Compact Framework and Microsoft Silverlight.

Microprocessor

It is the device that incorporates most or all of the functions of a central processing unit (CPU) on a single integrated circuit (IC).

Microsoft .NET Framework

A software framework that can be installed on computers running Microsoft Windows operating systems.

Noose

A loop at the end of a rope in which the knot slides to make the loop collapsible.

OS9

It is a family of real-time, process-based, multitasking, multi-user, Unix-like operating systems.

Plug and Play

A term used to describe the characteristic of a computer bus, or device specification, which facilitates the discovery of a hardware component in a system, without the need for physical device configuration, or user intervention in resolving resource conflicts.

PCB (**Printed Circuit Board**)

It is used to mechanically support and electrically connect electronic components using conductive pathways, or traces, etched from copper sheets laminated onto a non-conductive substrate.

PIC (Peripheral Interface Controller)

PIC is a family of Harvard architecture microcontrollers made by Microchip Technology, derived from the PIC1640[1] originally developed by General Instrument's Microelectronics Division

PLC (Programmable Logic Controller)

A digital computer used for automation of electromechanical processes, such as control of machinery on factory assembly lines, amusement rides, or lighting fixtures.

Punch Card

It is a flexible write-once medium that encodes, most commonly, 80 characters of data. Groups or "decks" of cards form programs and collections of data.

Q (t+1)

Next state of Q (t) in respond to one clock pulse.

Reed

Comb-like feature thread passing through which the warp ends pass.

Schleicher

A german company that produces weaving machines.

Sensor

A device that measures a physical quantity and converts it into a signal which can be read by an observer or by an instrument.

Pick Finding

It is the process that is necessary to be able to find the correct weft number, in case of any failure in weaving.

Van de Wiele

A belgian company that produces weaving machines.

Warp

The lengthways threads of woven fabric.

Weave

Formation of fabric by interlacing the warp and weft threads.

Weft

The horizontal yarns that interlace at right angles with the vertical warp threads.

Windows

Operating systems for IBM compatible PC developed by Microsoft.

Windows Vista

A line of operating systems developed by Microsoft for use on personal computers.

APPENDIX-B

COMMON BUS STANDARDS AND PCI OVERVIEW

B.1 Common Bus Standards

ISA (Industry Standard Architecture) is a bus system for IBM PCs and PC clones. The original standard, from 1981, was an 8 bit bus that ran at 4.77 MHz. In 1984, with the introduction of the IBM AT computer (which used the 80286 processor, introduced by Intel in 1982), ISA was expanded to a 16 bit bus that ran at 8.3 MHz. An electronic card that uses ISA bus can be seen in Figure B.1

Figure B.1 An electronic card that uses ISA bus

VL bus (VESA Local bus) is created in 1992 by the Video Electronics Standards Association for the Intel 80486 processor. The VL bus is 32 bits and runs at 33 MHz. The VL bus requires use of manually set jumper switches. An electronic card that uses VL bus can be seen in Figure B.2

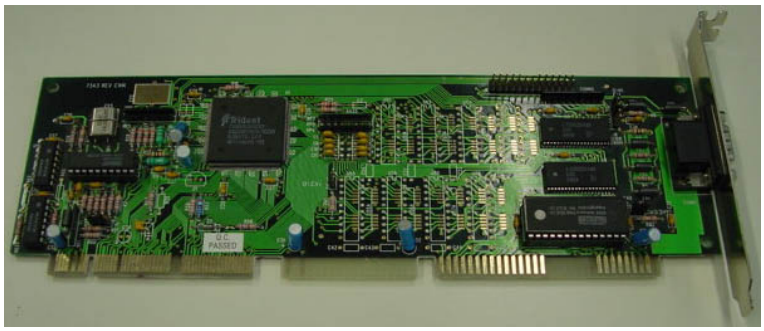


Figure B.2 A graphic card that uses VL bus

PCI (Peripheral Component Interconnect) is a bus created by Intel in 1993. PCI is available in both a 32 bit version running at 33 MHz and a 64 bit version running at 66 MHz. PCI supports automatic configuration (for “plug and play”). PCI automatically checks data transfers for errors. PCI uses a burst mode, increasing bus efficiency by sending several sets of data to one address. An electronic card that uses PCI bus can be seen in Figure B.3

Figure B.3 An electronic card that uses PCI bus

PCI-X revised the conventional PC standard by doubling the maximum clock speed (from 66 MHz to 133 MHz) and hence the amount of data exchanged between the computer processor and peripherals. Conventional PCI supports up to 64 bits at 66 MHz (though anything above 32 bits at 33 MHz is only seen in high-end systems) and additional bus standards move 32 bits at 66 MHz or 64 bits at 33 MHz. The theoretical maximum amount of data exchanged between the processor and peripherals with PCI-X is 1.06 GB/s, compared to 532 MB/s with standard PCI. PCI-X also improves the fault tolerance of PCI allowing, for example, faulty cards to be reinitialized or taken offline. An electronic card that uses PCI-X bus can be seen in Figure B.4

Figure B.4 An electronic PCI-X (PCI Express) card

AGP (Accelerated Graphics Port) was created by Intel to increase performance by separating video data from the rest of the data on PCI I/O buses. AGP is 32 bits and runs at 66 MHz. AGP 2X double pumps the data, doubling the amount of throughput at the same bus width and speed. AGP 4X runs four sets of data per clock, quadrupling the throughput. An electronic card that uses AGP bus can be seen in Figure B.5

Figure B.5 An AGP type of electronic card

The main difference among the several types of bus is in the number of bits that can be transmitted at a time, and in the operating frequency used. Nowadays the two fastest types of PC expansion bus are the PCI and the AGP. Transfer rates and some other properties of those buses are shown below [10].

Table B.1 Comparison of the common bus types in a few aspects

Bus Type	Number of Bits	Clock Speed	Data Per Clock Cycle	Max.Transfer Rate
ISA	16 Bit	8Mhz	1	16 MB/s
ISA	32 Bit	8Mhz	1	32 MB/s
VL-BUS	32 bit	25 MHz	1	100 MB/s
VL-BUS	32 bit	33 MHz	1	132 MB/s
PCI	32 bit	33 MHz	1	132 MB/s
PCI	64 bit	33 MHz	1	264 MB/s
PCI	64 bit	66 MHz	1	512 MB/s
PCI	64 bit	133 MHz	1	1 GB/s
AGPX1	32 bit	66 MHz	1	266 MB/s
AGPX2	32 bit	66 MHz	2	533 MB/s
AGPX4	32 bit	66 MHz	4	1 GB/s
AGPX8	32 bit	66 MHz	8	2 GB/s
PCI-X 64	64 bit	66 MHz	1	533 MB/s
PCI-X 133	64 bit	133 MHz	1	1 GB/s
PCI-X 266	64 bit	133 MHz	2	2 GB/s
PCI-X 533	64 bit	133 MHz	4	4 GB/s

PCI-X, PCI type slots exist in the contemporary computers. Even though the computer hardware technology improves in unbelievably speeds. A proper base for the PCI-X slots hasn’t been formed yet for the modern machines used for the

industrial applications. PCI-X slots are used for the graphic cards requiring for high resolution nowadays and it can not be said that they are really necessary for providing the communication between computer and industrial machines. Since PCI-X is a newer bus standard compared to PCI, a substructure has not been formed yet to be able to realize big projects about its architecture and usability.

In current applications in industrial sector, ISA type electronic cards are being used too, but since they have lower data transmission rate compared to PCI and the current computers do not have ISA type slots, these reasons force us to design the an electronic card that uses PCI type slot.

B.2 PCI Bus

In this section of Appendix B, a brief overview of PCI will be presented and the details of PCI bus protocol will presented as a next and final step.

B.2.1 PCI Overview

The PCI Local Bus is a high performance bus for interconnecting chips, expansion boards, and processor/memory subsystems. It originated at Intel in the early 1990s as a standard method of interconnecting chips on a board.[saved] It was later adopted as an industry standard administered by the PCI Special Interest Groups, or “PCI SIG” Under the PCI SIG the definition of PCI was extended to define a standard expansion bus interface connector for add-in boards.

PCI was first adopted for use in personal computers in about 1994 with Intel's introduction of the "Saturn" chipset and "Alfredo" motherboard for the 486 processor. With introduction of chipsets and motherboards for the Intel Pentium processor, PCI largely replaced earlier bus architectures such as EISA, VL, and Micro Channel. The ISA bus has initially continued to co-exist with PCI for support of legacy" add-in boards that don't require the high performance of the PCI bus. But as legacy boards are redesigned, PCI is expected to completely replace ISA as well.

B.2.2 PCI Bus Protocol

PCI is synchronous bus architecture with all data transfers being performed relative to a system clock (CLK). The initial PCI specification permitted a maximum clock rate of 33 MHz allowing one bus transfer to be performed every 30 nanoseconds. Later, PCI specification extended the bus definition to support operation at 66 MHz, but the vast majority of today's personal computers continue to implement a PCI bus that runs at a maximum speed of 33 MHz.

PCI implements a 32-bit multiplexed Address and Data bus (AD[31:0]). It architects a means of supporting a 64-bit data bus through a longer connector slot, but most of today's personal computers support only 32-bit data transfers through the base 32-bit PCI connector. At 33 MHz, a 32-bit slot supports a maximum data transfer rate of 132 Mbytes/sec, and a 64-bit slot supports 264 Mbytes/sec.

The multiplexed Address and Data bus allows a reduced pin count on the PCI connector that enables lower cost and smaller package size for PCI components. Typical 32-bit PCI add-in boards use only about 50 signals pins on the PCI connector of which 32 are the multiplexed Address and Data bus. PCI bus cycles are initiated by driving an address onto the AD[31:0] signals during the first clock edge called the *address phase*. The address phase is signaled by the activation of the FRAME# signal. The next clock edge begins the first of one or more *data phases* in which data is transferred over the AD [31:0] signals.

In PCI terminology, data is transferred between an *initiator* which is the bus master, and a *target* which is the bus slave. The initiator drives the C/BE[3:0]# signals during the address phase to signal the type of transfer (memory read, memory write, I/O read, I/O write, etc.). During data phases the C/BE[3:0]# signals serve as byte enable to indicate which data bytes are valid. Both the initiator and target may insert wait states into the data transfer by deasserting the IRDY# and TRDY# signals. Valid data transfers occur on each clock edge in which both IRDY# and TRDY# are asserted.

A PCI bus transfer consists of one address phase and any number of data phases. I/O operations that access registers within PCI targets typically have only a single data

phase. Memory transfers that move blocks of data consist of multiple data phases that read or write multiple consecutive memory locations. Both the initiator and target may terminate a bus transfer sequence at any time. The initiator signals completion of the bus transfer by deasserting the FRAME# signal during the last data phase. A target may terminate a bus transfer by asserting the STOP# signal. When the initiator detects an active STOP# signal, it must terminate the current bus transfer and re-arbitrate for the bus before continuing. If STOP# is asserted without any data phases completing, the target has issued a *retry*. If STOP# is asserted after one or more data phases have successfully completed, the target has issued a *disconnect*.

Initiators arbitrate for ownership of the bus by asserting a REQ# signal to a central arbiter. The arbiter grants ownership of the bus by asserting the GNT# signal. REQ# and GNT# are unique on a per slot basis allowing the arbiter to implement a bus fairness algorithm. Arbitration in PCI is "hidden" in the sense that it does not consume clock cycles. The current initiator's bus transfers are overlapped with the arbitration process that determines the next owner of the bus.

PCI supports a rigorous auto configuration mechanism. Each PCI device includes a set of configuration registers that allow identification of the type of device (SCSI, video, Ethernet, etc.) and the company that produced it. Other registers allow configuration of the device's I/O addresses, memory addresses, interrupt levels, etc.

Although it is not widely implemented, PCI supports 64-bit addressing. Unlike the 64-bit data bus option which requires a longer connector with an additional 32-bit of data signals, 64-bit addressing can be supported through the base 32-bit connector. *Dual Address Cycles* are issued in which the low order 32-bits of the address are driven onto the AD [31:0] signals during the first address phase, and the highorder 32-bits of the address (if non-zero) are driven onto the AD [31:0] signals during a second address phase. The remainder of the transfer continues like a normal bus transfer.

PCI defines support for both 5 Volt and 3.3 Volt signaling levels. The PCI connector defines pin locations for both the 5 Volt and 3.3 Volt levels. However, most early PCI systems were 5 Volt only, and did not provide active power on the 3.3 Volt

connector pins. Over time more use of the 3.3 Volt interface is expected, but add-in boards which must work in older legacy systems are restricted to using only the 5 Volt supply. A "keying" scheme is implemented in the PCI connectors to prevent inserting an add-in board into a system with incompatible supply voltage.
Although used most extensively in PC compatible systems, the PCI bus architecture is processor independent. PCI signal definitions are generic allowing the bus to be used in systems based on other processor families.

PCI includes strict specifications to ensure the signal quality required for operation at 33 and 66 MHz. Components and add-in boards must include unique bus drivers that are specifically designed for use in a PCI bus environment. Typical TTL devices used in previous bus implementations such as ISA and EISA are not compliant with the requirements of PCI. This restriction along with the high bus speed dictates that most PCI devices are implemented as custom ASICs.

The higher speed of PCI limits the number of expansion slots on a single bus to no more than 3 or 4, as compared to 6 or 7 for earlier bus architectures. To permit expansion buses with more than 3 or 4slots, the PCI SIG has defined a *PCI-to-PCI Bridge* mechanism. PCI-to-PCI Bridges are ASICs that electrically isolate two PCI buses while allowing bus transfers to be forwarded from one bus to another. Each bridge device has a "primary" PCI bus and a "secondary" PCI bus. Multiple bridge devices may be cascaded to create a system with many PCI buses.

B.2.3 PCI Signal Descriptions

In this section, mission of each pin of PCI bus will be represented individually in details.

B.2.3.1 System Pins

B.2.3.1.1 Clock (CLK)

Clock provides the timing reference for all transfers on the PCI bus. All PCI signals except reset and interrupts are sampled on the rising edge of the CLK signal. All bus

timing specifications are defined relative to the rising edge. For most PCI systems the CLK signal operates at a maximum frequency of 33 MHz. Revision 2.1 of the PCI specification defined a 66 MHz operating mode, but this mode is not yet widely implemented. To operate at 66MHz, both the PCI system and the PCI add-in board must be specifically designed to support the higher CLK frequency. Add-in boards indicate to the system if they are 66 MHz capable through the M66EN signal. A 66 MHz system will supply a 66 MHz CLK if the add-in board supports it, and supply a default 33 MHz CLK if the add-in board does not support the higher frequency. Likewise, if a system is capable of providing only a 33 MHz clock, then a 66 MHz add-in board must be able to operate using the lower frequency. The minimum frequency of the CLK signal is specified at 0 Hz permitting CLK to be "suspended" for power saving purposes.

B.2.3.1.2 Reset (RST#)

Reset is driven active low to cause a hardware reset of a PCI device. The reset shall cause a PCI device's configuration registers, state machines, and output signals to be placed in their initial state. RST# is asserted and deasserted asynchronously to the CLK signal. It will remain active for at least 100 microseconds after CLK becomes stable.

B.2.3.2 Address and Data Pins

B.2.3.2.1 Address and Data Phase Pins (AD[31:0])

Address and Data are multiplexed onto these pins. AD[31:0] transfers a 32-bit physical address during "address phases", and transfers 32-bits of data information during "data phases". An address phase occurs during the clock following a high to low transition on the FRAME# signal. A data phase occurs when both IRDY# and TRDY# are asserted low. During write transactions the initiator drives valid data on AD[31:0] during each cycle it drives IRDY# low. The target drives TRDY# low when it is able to accept the write data. When both IRDY# and TRDY# are low, the target captures the write data and the transaction is completed. For read transactions the opposite occurs. The target drives TRDY# low when valid data is driven on

AD[31:0], and the initiator drives IRDY# low when it is able to accept the data. When both IRDY# and TRDY# are low, the initiator captures the data and the transaction is completed. Bit 31 is the most significant AD bit. Bit 0 is the least significant AD bit.

B.2.3.2.2 Bus Command and Bus Enable Pins (C/BE [3:0] #)

Bus Command and Byte Enables are multiplexed onto these pins. During the address phase of a transaction these signals carry the bus command that defines the type of transfer to be performed. Table B.2 shows a list of valid bus commands. During the data phase of a transaction these signals carry byte enable information. C/BE [3]# is the byte enable for the most significant byte (AD[31:24]) and C/BE[0]# is the byte enable for the lease significant byte (AD[7:0]). The C/BE [3:0]# signals are driven only by the initiator and are actively driven through the all address and data phases of a transaction.

Table B.2 Valid bus command codes

C/BE[3:0]#	Command Types
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

B.2.3.2.3 Parity Pin (PAR)

Parity is even parity over the AD [31:0] and C/BE [3:0]# signals. Even parity implies that there is an even number of '1's on the AD [31:0], C/BE [3:0]#, and PAR signals. The PAR signal has the same timings as the AD [31:0] signals, but is delayed by one cycle to allow more time to calculate valid parity.

B.2.3.3 Interface Control Pins

B.2.3.3.1 Frame Pin (FRAME#)

Cycle Frame is driven low by the initiator to signal the start of a new bus transaction. The address phase occurs during the first clock cycle after a high to low transition on the FRAME# signal. If the initiator intends to perform a transaction with only a single data phase, then it will return FRAME# back high after only one cycle. If multiple data phases are to be performed, the initiator will hold FRAME# low in all but the last data phase. The initiator signals its intent to perform a *master initiated termination* by driving FRAME# high during the last data phase of a transaction. During a *target initiated termination* the initiator will continue to drive FRAME# low through the end of the transaction.

B.2.3.3.2 Initiator Ready Pin (IRDY#)

Initiator Ready is driven low by the initiator as an indication it is ready to complete the current data phase of the transaction. During writes it indicates the initiator has placed valid data on AD [31:0]. During reads it indicates the initiator is ready to accept data on AD [31:0]. Once asserted, the initiator holds IRDY# low until TRDY# is driven low to complete the transfer, or the target uses the STOP# signal to terminate without performing the data transfer. IRDY# permits the initiator to insert wait states as needed to slow the data transfer.

B.2.3.3.3 Target Ready Pin (TRDY#)

Target Ready is driven low by the target as an indication it is read to complete the current data phase of the transaction. During writes it indicates the target is ready to accept data on AD [31:0]. During reads it indicates the target has placed valid data on the AD [31:0] signals. Once asserted, the target holds TRDY# low until IRDY# is driven low to complete the transfer. TRDY# permits the target to insert wait states as needed to slow the data transfer.

B.2.3.3.4 Stop Pin (STOP#)

Stop is driven low by the target to request the initiator terminate the current transaction. In the event that a target requires a long period of time to respond to a transaction, it may use the STOP# signal to suspend the transaction so the bus can be used to perform other transfers in the interim. When the target terminates a transaction without performing any data phases it is called a *retry*. If one or more data phases are completed before the target terminates the transaction, it is called a *disconnect*. A retry or disconnect signals the initiator that it must return at a later time to attempt performing the transaction again. In the event of a fatal error such as a hardware problem the target may use STOP# and DEVSEL# to signal an abnormal termination of the bus transfer called a *target abort*. The initiator can use the target abort to signal system software that a fatal error has been detected.

B.2.3.3.5 Lock Pin (LOCK#)

Lock may be asserted by an initiator to request exclusive access for performing multiple transactions with a target. It prevents other initiators from modifying the locked addresses until the agent initiating the lock can complete its transaction. Only a specific region (a minimum of 16 bytes) of the target’s addresses is locked for exclusive access. While LOCK# is asserted, other non-exclusive transactions may proceed with addresses that are not currently locked. But any non-exclusive accesses to the target's locked address space will be denied via a retry operation. LOCK# is intended for use by bridge devices to prevent deadlocks.

B.2.3.3.6 Initialization Device Select (IDSEL)

Initialization Device Select is used as a chip select during during PCI configuration read and write transactions. IDSEL is driven by the PCI system and is unique on a per slot basis. This allows the PCI configuration mechanism to individually address each PCI device in the system. A PCI device is selected by a configuration cycle only if IDSEL is high, AD [1:0] are "00" (indicating a type 0configuration cycle), and the command placed on the C/BE [3:0]# signals during the address phase is either a "configuration read" or "configuration write". AD [10:8] may be used to select one of up to eight "functions" within the PCI device. AD[7:2] select individual configuration registers within a device and function.

B.2.3.3.7 Device Select Pin (DEVSEL#)

Device Select is driven active low by a PCI target when it detects its address on the PCI bus. DEVSEL# may be driven one, two, or three clocks following the address phase. DEVSEL# must be asserted with or prior to the clock edge in which the TRDY# signal is asserted. Once DEVSEL# has been asserted, it cannot be deasserted until the last data phase has completed, or the target issues a target abort. If the initiator never receives an active DEVSEL# it terminates the transaction in what is termed a *master abort*.

B.2.3.4 Arbitration Pins (Initiator Only)

B.2.3.4.1 Request Pin (REQ#)

Request is used by a PCI device to request use of the bus. Each PCI device has its own unique REQ# signal. The arbiter in the PCI system receives the REQ# signals from each device. It is important that this signal be tri-stated while RST# is asserted to prevent a system hang. This signal is implemented only be devices capable of being an initiator.

B.2.3.4.2 Grant Pin (GNT#)

Grant indicates that a PCI device's request to use the bus has been granted. Each PCI device has its own unique GNT# signal from the PCI system arbiter. If a device's GNT# signal is active during one clock cycle, then the device may begin a transaction in the following clock cycle by asserting the FRAME# signal. This signal is implemented only be devices capable of being an initiator.

B.2.3.5 Error Reporting Pins

2.3.3.5.1 Parity Error Pin (PERR#)

Parity Error is used for reporting data parity errors during all PCI transactions except a "Special Cycle". PERR# is driven low two clock periods after the data phase with bad parity. It is driven low for a minimum of one clock period. PERR# is shared among all PCI devices and is driven with a tri-state driver. A pull-up resistor ensures the signal is sustained in an inactive state when no device is driving it. After being asserted low, PERR# must be driven high one clock before being tri-stated to restore the signal to its inactive state. This ensures the signal does not remain low in the following cycle because of a slow rise due to the pull-up.

B.2.3.5.2 System Error Pin (SERR#)

System Error is for reporting address parity errors, data parity errors during a Special Cycle, or any other fatal system error. SERR# is shared among all PCI devices and is driven only as an open drain signal (it is driven low or tri-stated by PCI devices, but never driven high). It is activated synchronously to CLK, but when released will float high asynchronously through a pull-up resistor.

B.2.3.6 Interrupt Pins (INTA#, INTB#, INTC#, INTD#)

Interrupts are driven low by PCI devices to request attention from their device driver software. They are defined as "level sensitive" and are driven low as an open drain signal. Once asserted, the INTX# signals will continue to be asserted by the PCI

device until the device driver software clears the pending request. A PCI device that contains only a single function shall use only INTA#. Multi-function devices (such as a combination LAN/modem add-in board) may use multiple INTX# lines. A single function device uses INTA#. A two function device uses INTA# and INTB#, etc. All PCI device drivers must be capable of sharing an interrupt level by chaining with other devices using the interrupt vector.

B.2.3.7 Cache Support Pins (Optional)

These pins are architected to permit cacheable memory to be implemented on a PCI bus. They transfer status information between the bridge/cache and the target of the memory request. If a PCI transaction results in a hit on a "dirty" cache line, the bridge/cache will signal "snoop backoff" to the cacheable target. As a result, the target will issue retries on all accesses to the modified cache line until the bridge/cache completes a writeback operation. The target will then permit the access to complete.

These cache support pins are rarely if ever implemented in today's PCI systems. For performance reasons, cacheable memory is typically coupled very closely with a host processor bus that runs at a higher frequency than PCI.

B.2.3.7.1 Snoop Backoff Pin (SBO#)

Snoop Backoff indicates a hit to a modified line when asserted. When SBO# is deasserted and SDONE is asserted, it indicates a "CLEAN" snoop result.

B.2.3.7.2 Snoop Done Pin (SDONE)

Snoop Done indicates the status of the snoop for the current access. When deasserted, it indicates the result of the snoop is still pending. When asserted, it indicates the snoop is complete.

B.2.3.8 Additional Pins

B.2.3.8.1 Present Pins (PRSNT [1:2]#)

Present signals are used for two purposes: 1) to indicate that an add-in board is physically present, and 2) to indicate the power requirements of an add-in board. These are static signals that are either grounded or left open on the add-in board. Table B.3 shows the encoding of these signals.

Table B.3 Encoding of present signals

PRSNT1#	PRSNT2#	Add-in Board Configuration
Open	Open	No board present
Ground	Open	Board present, 25W maximum
Open	Ground	Board present, 15W maximum
Ground	Ground	Board present, 7.5W maximum

B.2.3.8.2 Clock Running Pin (CLKRUN#)

Clock Running is an optional signal used to facilitate stopping of the CLK signal for power saving purposes. CLKRUN# is intended only for the "mobile" environment where power consumption is critical. It is not defined on the PCI connector used for regular add-in boards. CLKRUN# is driven as an open drain signal. The PCI system drives CLKRUN# low when it is propagating a normal CLK signal. It releases CLKRUN# so it floats to a high level via a pull-up resistor as a request to stop the CLK for a specific PCI device. The device may then pulse CLKRUN# low to indicate to the system that it should continue to drive CLK, or allow CLKRUN# to remain high as confirmation that CLK can be stopped. If the CLK has been stopped and a PCI device wants to resume normal operation, it drives CLKRUN# low as a request that the system should start driving CLK again.

B.2.3.8.3 66 MHz Enable Pin (M66EN)

66MHZ Enable is left "open" or disconnected on add-in boards that support operation with a 66 MHz CLK, and grounded on add-in boards that support operation with only a 33 MHz CLK. 66MHz systems place a pull-up resistor on this signal to detect if the add-in board is 66 MHz capable. If the signal is high, a CLK with a maximum frequency of 66 MHz is supplied. If it is low, a CLK with a maximum frequency of 33 MHz is supplied. 33 MHz systems attach this signal to ground. 66 MHz operation will take place only if both the system and the add-in board support it.

B.2.3.9 64-Bit Bus Extension Pins (Optional)

B.2.3.9.1 Address and Data Phase Pins (AD[63:32])

Address and Data are multiplexed on the same pins and provide 32 additional bits when operating in a 64-bit bus environment. During data phases these bits transfer an additional 32-bits of data when both REQ64# and ACK64# are asserted. During address phases, when a Dual Address Cycle is being issued and the REQ64# signal is asserted, these bits transfer the upper 32-bits of the address.

B.2.3.9.2 Bus Command and Byte Enable Pins

Bus Command and Byte Enables are multiplexed onto the same pins and provide 4 additional bits when operating in a 64-bit bus environment. During data phases these bits transfer byte enables for the upper 32-bits of the data bus (AD[63:32]) when both REQ64# and ACK64# are asserted. During address phases, when a Dual Address Cycle is being issued and the REQ64# signal is asserted, these bits transfer the bus command.

B.2.3.9.3 Request 64-Bit Transfer Pin

Request 64-bit Transfer is asserted low by the initiator to indicate it desires a 64-bit transfer. This signal is driven with the same timings as FRAME#.

B.2.3.9.4 Acknowledge 64-Bit Transfer Pin

Acknowledge 64-bit Transfer is asserted low by a target as an indication that it has decoded its address as the target of the current access, and is capable of performing a 64-bit transfer.

B.2.3.9.5 Parity Upper DWORD Pin

Parity Upper DWORD is the even parity bit that protects AD [63:32] and C/BE [7:4]#.

B.2.3.9.6 JTAG/Boundary Scan Pins (Optional)

PCI devices may optionally support JTAG/Boundary Scan as defined in IEEE Standard 1149.1, *Test Access Port and Boundary Scan Architecture*. JTAG allows components installed on a PCI add-in board to be exhaustively tested by serially scanning test patterns through each component. TCK (test clock), TDI (test data input), TDO (test output), TMS (test mode select), TRST# (test reset) signals are defined by the JTAG standard. If JTAG is not implemented by an add-in board, the TDI and TDO signals must be connected to preserve the scan path.

B.2.3.10 PCI Connector Pinout

Three types of add-in boards may be implemented: "5 Volt add-in boards" include a key notch in pin positions 50 and 51 to allow them to be plugged only into 5 Volt system connectors. "3.3 Volt add-in boards" include a key notch in pin positions 12 and 13 to allow them to be plugged only into 3.3 Volt system connectors. "Universal add-in boards" include both key notches to allow them to be plugged into either 5 Volt or 3.3 Volt system connectors. Universal boards must be able to adapt to operation at either signaling level.

Since the integrated circuits on the hardware designed utilizes +5V level and the electronic sensors that have been used in the further steps of the study utilizes +12V level, *5 Volt add-in boards* has been used in the design of the hardware. Table B.3

shows the pinout configuration of +5V system environment. On the table B.4, Side A represents the top layer of the electronic card and Side B represents the bottom layer of the electronic card.

Table B.4 +5V system environment

5V System Environment					
Pin	**Side A**	**Side B**	**Pin**	**Side A**	**Side B**
1	-12V	TRST#	**32**	AD[17]	AD[16]
2	TCK	+12V	**33**	C/BE[2]#	+3.3V
3	Ground	TMS	**34**	Ground	FRAME#
4	TDO	TDI	**35**	IRDY#	Ground
5	+5V	+5V	**36**	+3.3V	TRDY#
6	+5V	INTA#	**37**	DEVSEL#	Ground
7	INTB#	INTC#	**38**	Ground	STOP#
8	INTD#	+5V	**39**	LOCK#	3.3V
9	PRSNT1#	Reserved	**40**	PERR#	SDONE
10	Reserved	+5V (I/O)	**41**	+3.3V	SBO#
11	PRSNT2#	Reserved	**42**	SERR#	Ground
12	Ground	Ground	**43**	+3.3V	PAR
13	Ground	Ground	**44**	C/BE[1]#	AD[15]
14	Reserved	Reserved	**45**	AD[14]	+3.3V
15	Ground	RST#	**46**	Ground	AD[13]
16	CLK	+5V (I/O)	**47**	AD[12]	AD[11]
17	Ground	GNT#	**48**	AD[10]	Ground
18	REQ#	Ground	**49**	Ground	AD[09]
19	+5V (I/O)	Reserved	**50**	Connector Key	
20	AD[31]	AD[30]	**51**	Connector Key	
21	AD[29]	+3.3V	**52**	AD[08]	C/BE[0]#
22	Ground	AD[28]	**53**	AD[07]	+3.3V
23	AD[27]	AD[26]	**54**	+3.3V	AD[06]
24	AD[25]	Ground	**55**	AD[05]	AD[04]
25	+3.3V	AD[24]	**56**	AD[03]	Ground
26	C/BE[3]#	IDSEL	**57**	Ground	AD[02]
27	AD[23]	+3.3V	**58**	AD[01]	AD[00]
28	Ground	AD[22]	**59**	+5V (I/O)	+5V (I/O)
29	AD[21]	AD[20]	**60**	ACK64#	REQ64#
30	AD[19]	Ground	**61**	+5V	+5V
31	+3.3V	AD[18]	**62**	+5V	+5V