**UNIVERSITY OF GAZİANTEP**
**GRADUATE SCHOOL OF**
**NATURAL & APPLIED SCIENCES**

# ELECTRICAL AND MAGNETORESISTIVE CHARACTERISTICS OF ELECTRODEPOSITED SCHOTTKY DIODE SYSTEMS

**Ph. D THESIS**
**IN**
**ENGINEERING PHYSICS**

BY
**GÜLSEN (GÜLER) ŞAHİN**
**JAN 2010**

# Electrical and Magnetoresistive Characteristics Of Electrodeposited Schottky Diode Systems

**PhD Thesis**
**in**
**Engineering Physics**
**University of Gaziantep**

**Supervisor**
**Prof. Dr. Ömer Faruk BAKKALOĞLU**

**by**

**Gülsen (GÜLER) ŞAHİN**

**Jan 2010**

## ABSTRACT

## ELECTRICAL AND MAGNETORESISTIVE CHARACTERISTICS OF ELECTRODEPOSITED SCHOTTKY DIODE SYSTEMS

ŞAHİN (GÜLER), Gülsen
Ph.D. in Engineering Physics Department
Supervisor: Prof. Dr. Ömer Faruk BAKKALOĞLU
January 2010, 104 pages

In this study, by using *n*-Si substrate with (100) orientation, 300-400 μm thickness and 3-4 Ωcm resistivity and phosphorus doped, thin film Schottky diode systems (Ni/*n*-Si SBDs and Co/*n*-Si SBDs which are electrochemically formed on *n*-type Si) are constructed and characterized. In the electrical characterization of these diodes, the current-voltage (*I-V*), the capacitance-voltage (*C-V*) and the conductivity-voltage (*G-V*) measurements are done. In addition, the magnetoresistive properties of these systems are investigated.

We have determined laterally homogeneous barrier heights (BHs) of the electrodeposited Ni/*n*-Si and Co/*n*-Si SBDs by the help of the linear relationship between the effective BHs and the ideality factors which is experimentally and theoretically confirmed.

The homogeneity or the uniformity of the Schottky BH is an issue with important implications on the theory of Schottky BH formation and important ramifications for the operation of Schottky barrier diodes and contacts. Thus, provided semiconductor substrate is well characterized, the homogeneous Schottky BH may be obtained even from the *I-V* characteristics of one contact. For this purpose, the Co/*n*-type Si SBDs with a doping density of about $1.22 \times 10^{15}$ $cm^{-3}$ and Ni/*n*-type Si diodes with a doping density of about $1.25 \times 10^{15}$ $cm^{-3}$ are prepared and the linear region with large BHs is used. The electrical characteristics of Ni/*n*-type and Co/*n*-Si structures were compared with each other at the room temperature.



**Key Words**: Silicon, Schottky Barrier Diodes, Barrier inhomogeneity, Electrodeposition Method, Magnetoresistance

# ÖZET

## ELEKTRODEPOLAMA YÖNTEMİYLE YAPILAN SCHOTTKY DİYODLARIN ELEKTRİKSEL VE MAGNETORESİSTANS ÖZELLİKLERİNİN İNCELENMESİ

ŞAHİN (GÜLER), Gülsen

Doktora Tezi, Fizik Mühendisliği, Gaziantep Üniversitesi
Danışman: Prof. Dr. Ömer Faruk BAKKALOĞLU
Ocak 2010, 104 pages

Bu çalışmada, (100) doğrultusunda büyütülmüş, 300-400μm kalınlıklı ve 3-4 Ωcm öz dirençli ve Fosfor katkılı *n*-Si kullanarak, elektrodepolama yöntemiyle oluşturduğumuz Ni/*n*-Si and Co/*n*-Si Schottky diyotların elektriksel ve magnetoresistans özellikleri incelendi. Bu diyotların elektriksel karakteristikleri, akım-voltaj (*I-V*), kapasitans-voltaj (*C-V*), ($C^{-2}$-*V*), iletkenlik-voltage (*G-V*) yardımıyla belirlendi. Ayrıca bu sistemlerin magnetoresistans özellikleri araştırıldı.

Elektrodepolama yöntemiyle oluşturduğumuz Ni/*n*-Si and Co/*n*-Si Schottky diyotların yanal homojen bariyer yükseklikleri etkin BH'leri ve idealite faktörleri arasındaki lineer ilişki yardımıyla belirlendi.

Schottky bariyer yüksekliğinin oluşum teorisinde, Schottky bariyer yüksekliğinin özdeşliği ve homojenliği önemli bir konudur ve Schottky bariyer diyot ve kontakların oluşumunda önemli bir daldır. Böylece yarıiletken madde iyi karakterize edilip homojen Schottky bariyer yüksekliği, tek bir kontağın *I-V* karakteristiklerinden de elde edilebilir. Bu amaçla, yaklaşık 1,22x $10^{15}$ $cm^{-3}$ katkı yoğunluklu Co/*n*-tip Si SBD lar ve yaklaşık 1,25x $10^{15}$ $cm^{-3}$ katkı yoğunluklu Ni/*n*-tip Si diyotlar hazırlandı ve büyük BH lı lineer bölge kullanıldı. Ni/*n*-tip Co/*n*-Si yapılarının elektriksel karakteristikleri oda sıcaklığında birbiriyle karşılaştırıldı.

**Anahtar kelimeler:** Silisyum, Schottky bariyer diyot, Bariyer inhomojenliği, Elektrodepolama yöntemi, Manyetorezistans

## ACKNOWLEDGEMENTS

This work is advanced by the supervision of Prof. Dr. Ömer Faruk Bakkaloğlu. I would like to express my great thanks to him for his guidance, advice and suggestions.

The co-operation and support of Prof. Dr. Abdülmecit Türüt (Atatürk University) were very valuable who provided me the opportunity of studying in the laboratories of Atatürk University.

My gratitude also goes to Dr. Şükrü Karataş (The University of Sütçü İmam) for his effort in reorganizing the results section and Dr. Metin Bedir for his interest and support in the construction of such a work.

I would further like to thank to Dr. Ömer Güllü (The University of Batman) who contributed in making the measurements.

My special thanks go to my family for their understanding and encouragement.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

## LIST OF SYMBOLS

| | |
|---|---|
| A | The effective diode area ($cm^2$) |
| $A^*$ | The Richardson constant |
| $C$ | The Schottky capacitance |
| $E_c$ | Energy of the conduction band |
| $E_f$ | Fermi energy |
| $E_g$ | Energy bandgap |
| $f(E)$ | The Fermi-Dirac (probability) distribution function |
| $g_c(E)$ | The density of state in the conductivity band |
| H | The coercieve field |
| $h$ | The planck constant |
| $I_0$ | Saturation current |
| $J$ | Current density |
| k | The Boltzmann constant |
| $m_n$* | The effective mass of the *n*-type semiconductor |
| $n$ | Ideality factor (forward slope factor, depends upon metal-semiconductor interface) |
| $N_D$ | The donor concentration of *n*-type semiconductor substrate |
| $q$ | The electronic charge |
| $R_S$ | Series resistance |
| T | The absolute temperature |
| $V_a$ | Applied voltage |
| $V_{bi}$ | Built in potential |
| $V_d$ | Diffusion potential |
| $\Phi_{bn}$ | The barrier height of a metal-semiconductor Schottky diode |
| $\Phi_{b0}$ | Asymtotic value of $\Phi_{bn}$ at zero electric field |
| $\Delta\Phi$ | The Schottky barrier lowering |
| $\Phi_m$ | The work function of the metal |
| $\Phi_s$ | The work function of the semiconductor |
| $\chi_s$ | The electron affinity of the semiconductor |
| $\varepsilon_s$ | The dielectric constant of the semiconductor |
| $\varepsilon_0$ | The dielectric constant of vacuum |
| $\rho$ | Resistivity |
| $\rho(x)$ | The space charge density |
| $\psi(x)$ | The potential function |
| $Q$ | In the semiconductor the charge density for unit area |

# CHAPTER 1

## GENERAL INTRODUCTION

The metal-semiconductor (MS) contact is one of the most widely used rectifying contacts in the electronic industry [1,2]. Due to the technological importance of metal-semiconductor structures, a full understanding of the nature of the electrical characteristics of Schottky barrier diodes (SBDs) in this system is of great interest. Metal-semiconductor Schottky contacts are frequently used in integrated circuits, e.g. as gates in MESFETs or MOSFET, in light detectors and as solar cells. Schottky barrier diodes (SBDs) are among the simplest MS contacts devices [3-11]. Metal-semiconductor (MS) Schottky contacts are still being investigated and has attracted much attention during recent years [3,4]. The popularity of such studies rooted in their importance to the insulator layer between metal and semiconductor, because the existence of such an interfacial insulator layer converts MS diodes to MIS type diodes and can have strong influence on the device characteristics as well as the interface states density, Schottky barrier height and ideality factor [12-20].

It is well known that, unless specially fabricated, a Schottky barrier diode (SBD) possesses a thin interfacial native oxide layer between the metal and the semiconductor. The existence of such an insulating layer can have a strong influence on the diode characteristics as well as a change of the interface state charge with bias which will give rise to an additional field in the interfacial layer [21,22]. Therefore, the interfacial layer and the interface states play an important role in the determination of the barrier height. Consequently, it has been concluded that the barrier height determined from the *I-V* characteristics is controlled by the interface states energy distribution in equilibrium with the semiconductor and the applied voltage under forward bias condition.

Depending on the characteristics of the interface, the metal-semiconductor contacts can be a Schottky barrier or an ohmic contact. Because of nonlinear current

voltage characteristics Schottky barrier has rectifying properties. Rectifiers can be obtained by the deposition of a thin film of a metal on the surface of a semiconductor.

The most important feature characterizing a SBD is its barrier height (BH). In spite of the numerous applications of Schottky barriers, the factors controlling the BH are not completely understood [3-12,23]. The barrier height (BH) is likely to be a function of the interface atomic structure, and the atomic inhomogeneties at metal-semiconductor (MS) interface which are caused by grain boundaries, multiple phases, facets, defects, a mixture of different phases etc. [7,8].

Due to the performance and stability of metal semiconductor structures which are of great importance to the electronic devices [3,4,24], although these devices have been studied extensively, a satisfactory understanding in all details has still not been achieved. Because there is a continuing need for faster and more complex systems for the information age, existing semiconductor devices are being studied for improvement, and new ones are being invented [3,4,24-26]. As it is stated above, the interface states play an important role on determination of Schottky barrier height and other characteristic parameters and these can affect device performance, stability and reliability [4,21,22,27]. Thus, barrier height, ideality factor, series resistance ($R_S$) and interface states density values ($N_{SS}$) at metal-semiconductor structures play an important role in the determination of the main parameters of the structures. These parameters give useful information concerned with the nature of the device. When voltage is applied across the MS device, the combination of the interfacial insulator layer, depletion layer and the series resistance of the device will share applied voltage.

Usually, the forward bias *I-V* characteristics are linear in the semi-logarithmic scale at low voltages, but deviate considerably from linearity due to the effects of parameters such as the series resistance $R_S$, the interfacial layer and interface states at sufficiently large applied voltage. The parameter $R_S$ is only effective in the downward-curvature region (non-linear region) of the forward *I–V* characteristics at sufficiently high applied voltage, but parameters such as the ideality factor $n$ and barrier height $\Phi_b$, are effective in both the linear and non-linear regions of these characteristics, accompanying the change of the SBH [28,29].

Si is an important integral for the very-large-scale integration (VLSI) circuits in many applications. Due to very high melting point of some metals, the electrodeposition process is sometimes prefered for the contact fabrication. The characterization of electrodeposited Co-Si contacts reveals that the resulting Schottky barrier is superior to those fabricated by other metallization techniques [30]. Moreover, it provides the possibility of depositing film structures different from those produced from other techniques as well [31]. Although the work function of Co is lower than that of usually used metals such as Ni, Au and Pt; Cobalt is more interactive than these metals for Schottky contact fabrication by electrodeposition method.

I can actually be said that the properties of thin films play a vital role in all electrical and optical devices. The optical and electrical properties of films strongly depend on growth method and growth conditions.

Several other techniques along with electrodeposition have been used so far to grow different types of thin films, among these techniques are evaporation [32], sputtering [33], molecular beam epitaxy [34] and spraying pyrolysis [35]. Electrodeposition is a cheap easy method to use and it is usable in the deposition of several different types of materials, e.g. metals, semiconductors, polymers etc. [36].

Among the different methods available for metallization of Si surfaces, vacuum deposition is preffered as the usual metallization method while electrodeposition is preffered due to its valuable advantages such as the possibility of metal deposition at low temperature with low costs [37-40]. With this technique, metallic systems such as Ni, Co etc. which are very difficult to be evaporated by the vacuum deposition can easily be formed. Although a conducting substrate is required in electrodeposition of metals, semiconducting substrates, such as suitably doped Si, provide a better alternative to metallic conductive substrates because the conductivity of semicondoctor substrates could be good enough to allow the electrodeposition and would not short circuit during the transport measurements due to the relatively higher resistivity of Si and the formation of the Schottky barrier between the metal films and Si substrate.

Although magnetic microstructures are electrodeposited directly on patterned Si wafers of various substrate resistivities, the electrical behavior of the resulting structures has not yet fully been investigated [30]. Moreover, the electrodeposition of metallic thin films directly onto Si could lead to the easy integration of SBDs and other systems like Giant negative magnetoresistance (GMR) sensors with Si-based electronics [41-45]. Schottky barriers (SBs) between magnetic metals and semiconductors are particulary useful for suppressing substrate leakage currents in magnetoresistance measurements. Furthermore, hot electron spin valve transistors require high quality SBs for their operation [42-45]. Some theories such as thermionic emission, diffusion etc. are present to explain the Schottky barrier effect [3]. The confirmations of these theories are based on the experimental results [46-57]. According to Mönch [46], the homogeneous BHs rather than effective BHs of individual contacts or mean values should be used to discuss theories on the physical mechanism that determine the BHs of the MS contacts. Thus, provided the semiconductor substrate is well characterized then the homogeneous Schottky BH may be obtained even from the *I-V* characteristics of one contact [46].

In this study, the main interest is given to the investigation of the electrical properties of the electrodeposited metal/semiconductor systems. Therefore, the thin film Schottky diode systems of Ni/*n*-Si SBDs and Co/*n*-Si SBDs are constructed and characterized. As mentioned above, due to the difficulty in the evaporation of Ni and Co by the vacuum deposition, we preferred the electrodeposition technique to construct these systems. In the electrical characterization of these diodes, the current-voltage (*I-V*), capacitance-voltage (*C-V*), conductivity-voltage (*G-V*) measurements are done, and some parameters like laterally homogeneous barrier heights (BH) of these electrodeposited SBD's are determined by the help of the linear relationship between effective BHs and ideality factors which is experimentally [46-55] and theoretically [56,57] confirmed. The electrical characteristics of Ni/*n*-type and Co/*n*-Si structures were compared with each other at room temperatures. The statistical distribution of the characteristics parameters of the structures was made by means of the Gaussian function. As is well-known, the homogeneous or uniform of the Schottky BH is an issue with important implications on the theory of Schottky BH formation and important ramifications for the operation of Schottky barrier diodes and contacts [46, 57, 58].

As a second interest in this thesis, the magnetoresistive properties of Ni and Co (which are ferromagnetic at room temperature) grown on *n*-type Si substrate are investigated.

The magnetoresistance is defined as the change in the resistivity of the magnetic film when an external magnetic field is applied. The magnetoresistance of magnetic film of Fe, Ni, Co and their alloys are generally anisotropic. When the magnetic field is applied parallel to the current, an increase in the resistivity is observed while decrease in the resistivity is observed when the magnetic field is applied perpendicular to the current. The anisotropic magnetoresistance (AMR) and giant magnetoresistance (GMR) effects are used in sensor technology and therefore continue to be of great interest [44]. The GMR was first discovered in antiferromagnetically coupled ultrathin multilayers of ferromagnetic and nonmagnetic metals [45]. The GMR effect is defined as a decrease in resistance from the level in the zero field state in which the magnetizations of adjacent ferromagnetic layers are antiparallel due to a weak anti-ferromagnetic coupling between layers to a lower level in which the magnetizations of the adjacent layers align due to an applied external field. When the magnetizations of the ferromagnetic layers are parallel there is less magnetic scattering because the spin of the electrons of the nonmagnetic metal align parallel or antiparallel with an applied magnetic field in equal numbers.

# CHAPTER 2

# SCHOTTKY BARRIER CONTACTS

## 2.1 Introduction

A Schottky Barrier diode is a contact between a metal and a semiconductor which has rectifying properties. To consider the characteristic parameters of Schottky diodes, a proper contact is needed. There is a charge transporting between the metarials when the metal is brought into contact with the semiconductor until the electrochemical potantials equalize. When the work function of metal is bigger than the semiconductor in *n*-type contacts, a rectifier contact occurs. When the work function of semiconductor is bigger than the metal in *n*-type contacts, an ohmic contact occurs.

## 2.2 Literature Survey

The first serious research about the usefulness of the electrical conductivity properties of metal and semiconductors and using them in the electronic circuits by applying contacts is made by Braun in 1874 [59].

Braun in 1895 used Schottky diodes as detector. In the Second World War period, with the developments of microwave radars, Schottky diodes are used as frequency transformers and as diodes of microwave detector. The metal-semiconductor field effective transistor is found in 1964 by Baird [60].

Schottky found barrier lowering because of image force in the metal-vacuum systems [61]. After 50 years from this, in 1964, this situation is confirmed by Sze and co-workers in the metal-semiconductor contacts [62]. In 1930s the rectifying theory of which fundamental principle bases the carrier diffusion event from the energy barrier is improved by Schottky and Spenke [63]. Crowel and Sze in 1965 brought in the diffusion theory of Schottky and thermionic emission theory of Bethe as a single theory [64].

The first studies on the interface layer in Schottky diodes were made by Cowley and Sze [65], who obtained their estimates from an analysis of barrier heights with different metallization as a function of the metal work function. Card and Rhoderick in 1971 [16] examined the effects of the interface layer on the ideality factor of the forward bias *I-V* characteristics. Tseng and Wu [66] analysed the effect of the presence of an interfacial layer on the behaviour of Schottky barrier diodes.

Electronic properties of a Schottky diode are characterized by its barrier height and ideality factor parameters. An ideality factor value is determined from the forward bias *I-V* characteristics. A barrier height value is obtained from experimental linear relationship between barrier heights and ideality factors. Mönch claimed that these two parameters can differ from diode to diode because of inhomogenity of barrier height [46].

The famous Schottky-Mott rule [67,68] predicts the barrier height to be equal to the difference between the electron affinity of the semiconductor and the work function of the metal.

Jeong et al. in 1991 worked for increasing barrier height in Au-InP Schottky diode by using a thin Phospour-nitrit ($P_3N_5$) interface layer occured by "Direct Photochemical Vapor Deposition Process" method and $PCl_3$ and $NH_3$ gas mixture. They obtained barrier height as 0.81 eV in their works [69].

Türüt et al. ascertained the interface layer, interface states and *I-V* and *C-V* characteristics concerning on the constant charges in interface, barrier height, ideality factor and interface state densitities in the Al/p-Si Schottky diodes with/without interface [70]. Szatkowski and Sieranski showed with experimental results that the interface states can effect the voltage-capacitance characteristics in 1992 [71].

In another study Türüt et al. investigated the thermal stability of the Schottky barrier height of Cr-Ni-Co alloy Schottky Contacts on an MBE *n*-GaAs substrate using current-voltage (*I-V*) and capacitance-voltage ($C^{-2}$-*V*) techniques after thermal annealing for 5 min. in an $N_2$ atmosphere at several temperatures in the 200-600 $^0$C range. In that study, the autors showed that the Schottky barrier formation was determined by the complicated mixture of phases at the interface resulting from

chemical reactions between the metal contact and GaAs or the thin native oxide layer on the surface of the GaAs. Thus, it was also shown that the Cr-Ni-Co/MBE *n*-GaAs contacts were thermally stable and maintained good Schottky characteristics after annealing at temperatures as high as 600 $^0$C for 5 min [72].

Karataş et al. in a study worked on the temperature dependence of the characteristic parameters of the H-terminated Sn/*p*-Si (100) Schottky contacts. They measured the current-voltage (*I-V*) characteristics of Sn/hydrogen-terminated p-Si Schottky contacts in the temperature range of 150-400 K. In that study it was shown that the occurrence of a Gaussian distribution of than BHs is responsible for the decrease of the apparent BH, the increase of the ideality factor and non-linearity in the activation energy plot at low temperature. They concluded that the temperature dependent *I-V* characteristics of the device can be successfully explained on the basis of a thermionic emission mechanism with Gaussian distribution of the BHs [18].

In another study Karataş et al. worked on the analysis dependence on temperature of basic electrical parameters on Zn/*p*-Si Schottky diodes. They concluded that the ideality factor ($n$) and the series resistance ($R_S$) of diode is strongly connected to temperature and decrease with increase in the temperature [73].

T. Kılıçoğlu et al., have fabricated Au/*n*-Si Schottky Barrier diodes (SBDs) with and without thin native oxide layer to explain whether or not the native oxide layer is effective on some electronic parameters such as, ideality factor, barrier height (BH), series resistance, interface state density and rectifying ratio. After obtaining the values of these parameters they concluded that the values of all electronic parameters of Au/native oxide/*n*-Si metal-insulater-Semiconductor (MIS) SBDs except for the rectifying ratio are higher than the values of the reference sample (MS). This was attributed to the presence of the native oxide layer [74].

F. Dağdelen and A. Aydoğdu studied the electronic properties of the Ni/*n*-type complex semiconductor/Ag Schottky diodes made by metal evoporation method. From Schottky diodes measurements, diode parameters are determined by two different methods; Ku method and Cheung method. According to the results of the Ku method, the ideality multipliers and barrier heights of the diode were found as 2.62, 2.78, 2.51, 2.05 and 0.92 eV, respectively. And the ideality multipliers and

barrier heights of the diode from the results of the Cheung method were obtained as 2.63, 2.05, 1.33, 2.14 and 0.98, 0.91, 0.88, 0.91 eV, respectively [75].

A new Schottky diode, Al/*p*-GaSe, was presented in the study of Wen-Chang Huang et al. It showed an effective Schottky barrier height of 0.94 eV with an ideality factor of 1.24 at the 400 $^{0}$C annealed diode. The contact interface of the diode was passivated after thermal annealing. The passivation gave rise to a lower reverse leakage current and a better ideality factor [76].

It was shown that non-ideal behavior in the SBDs could be quantitatively explained by assuming specific distribution of nanometer-scale interfacial patches (small regions) with lower BH than the junctions main BH [56,57]. In such cases, the current across the MS contact may be greatly influenced by the presence of the BH inhomogeneity [5,8,13,55-57,77-79]. Some authors have also been able to account for much of the observed nonideal behavior by assuming certain distributions of microscopic barrier heights for the different diodes [5,8,13,56,57,77-80]. Tung and coworkers [56,57] have modeled imperfect Schottky contacts by assuming lateral variations of the barrier height. They found larger ideality factors and smaller effective barrier heights when they increased the inhomogeneity of barriers. Thus, it has been pointed out that the BH inhomogeneity model may also be used to explain the linear relationship between effective BHs and ideality factors that is often observed on sets of the identically prepared diodes [46-57].

The demands for the fabrication of low cost SBDs, the terrestrial solar cells and other metal-semiconducting devices have recently enhanced the interest in the preparations of these systems by electrodeposition techniques. Therefore, this technique is extensively used in industrial production as an inexpensive method of large scale thin film deposition [81]. Electrodeposition has also been successfully employed in the preparation of many elemental semiconductors in thin film form, with most of the effort being put into Ge and Si elemental semiconductors, CdS, CdSe, CdTe, ZnSe and ZnTe II-VI compounds; GaAs, GaP, InP [82]. The application of the electrodeposition in the preparation of metal layers on these particular semiconductors has gained considerable interest, since Bhattacharya's first attempt in 1983 [83].

Kiziroglou et al. fabricated Ni-Si Schottky barriers by electrodeposition using Ni on *n*-Si substrates and presented *I-V*, *C-V* and low temperature *I-V* measurements. They revealed a high quality Schottky barrier with extremely low reverse leakage current. They showed the results to fit an inhomogeneous barrier model for thermionic emission over a Schottky barrier proposed by Werner and Guttler [J.H. Werner, H.H. Guttler, Barrier inhomogeneities at Schottky contact, J. Appl. Phys. 69 (3) (1991) 1522-1533]. A mean value of 0.76 V and a standard deviation of 66 mV was obtained for the Schottky barrier height at room temperature with a linear bias dependence. X-ray diffraction and scanning electronmicroscopy measurements revealed a polycrystalline Ni film with grains that span from the Ni-Si interface to the top of the Ni layer. The variation in Ni orientation was suggested as a possible source of the spatial distribution of the Schottky barrier height [84].

Also Kiziroglou et al. fabricated the electrodeposited Ni-Si contacts and studied the transport mechanisms through the formed Schottky barrier because of the particular interest of current transport at Schottky barriers for spin injection and detection in semiconductors. They used high doped Si to enable tunneling currents. Then they interpreted the results using tunneling theory for Schottky barriers and recent models for spatially distributed barrier height. It was shown that, contrary to the case of low doped Si where thermionic emission dominates, tunneling is the dominant mechanism for reverse and low forward bias for highly doped Si. An exponential reverse bias *I-V* behavior with negative temperature coefficient is reported. An explanation can be found on the rapid decrease of the reverse bias *I-V* slope with the temperature predicted by Padovani and Stratton for thermionic field emission in conjunction with the increase of the Schottky barrier height with the temperature suggested for spatially distributed barrier heights [85].

In another study, Kiziroglou et al. used electrodeposition to fabricate magnetic microstructures directly on patterned *n*-type Si wafers of various substrate resisitivities. They characterized the Ni-Si Schottky barrier and found to be of high quality for relatively low Si resisitivities (1-2 μΩ-cm), with extremely low reverse leakage. It was shown that a direct correlation exists among the electrodeposition potential, the roughness, and the coercivity of the films. They also concluded that the

electrodeposition of magnetic materials on Si might be a viable fabrication technique for magnetoresistance and spintronics applications [30].

M. Ahmetoğlu et al. in their works reported the electrical characteristics of the Schottky diodes formed by electrodeposition of copper on *n*-Si (111) from 0.2 M $CuSO_4 5H_2O$ + 0.5 M $H_3BO_3$ (pH=2.0) solution. Electrical measurements have been carried out at room temperature. Cu/*n*-Si diode current-voltage characteristics displayed low reverse-bias leakage currents and average barrier heights of 0.59 ± 0.02 eV and 0.67 ±0.02 eV obtained from both *I-V* and *C-V* measurements at room temperature, respectively [86].

Ö. Güllü., et all have investigated the electrical characteristics, such as current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements of identically prepared crystal violet/*p*-Si Organic/Inorganic (OI) Schottky structures formed by evaporation of organic compound solution to directly p-Si semiconductor substrate. They have seen a diode-to-diode variation although the diodes were all identically prepared: the effective barrier heights ranged from 0.6 ± 0.1 to 0.8 ± 0.1 eV, and the ideality factor from 1.6 ± 0.4 to 3.5 ± 0.4. Also they have plotted the barrier height versus ideality factor plot for the OI devices. Lateral homogeneous BH was calculated as a value of 0.7 eV from the observed linear correlation between BH and ideality factor, which can be explained by laterally inhomogeneities of BHs. The values of barrier height and acceptor doping concentration yielded from the reverse bias *C–V* measurements ranged from $0.7 \pm 0.1$ to $1.3 \pm 0.1$ eV and from $(4.7 \pm 0.8) \times 10^{14}$ to $(8.1 \pm 0.8) \times 10^{14}$ $cm^{-3}$, respectively. The mean barrier height and mean acceptor doping concentration from *C–V* characteristics has been calculated 1.0 eV and $5.9 \times 10^{14}$ $cm^{-3}$, respectively Thus, modification of the interfacial potential barrier for metal / Si diodes has been achieved using a thin interlayer of the methyl violet organic semiconductor; this has been ascribed to the fact that the methyl violet interlayer increases the effective barrier height by influencing the space charge region of Si [87].

S. Duman et al., concerned on the barrier-height inhomogeneity in identically prepared Ni/*n*-type 6H-SiC Schottky diodes and concluded that, even though the diodes had identically been prepared, they revealed different BHs and ideality factors. This behaviour was attributed to spatial variations of the BHs. The experimental BHs

were observed to decrease linearly as a function of the increasing ideality factor. The Gaussian fits of the experimental SBH distributions obtained from the *C–V* and *I–V* characteristics yielded mean SBH values of 1.27 and 0.93 eV, respectively [88].

## 2.3 Semiconductors

### 2.3.1 Introduction

A semiconductor is classified as a material between metals and insulators. Its electrical conductivity lies between those of a conductor and an insulator. The conductivity of a semiconductor material is closely dependent on its temperature and can be varied under an external electrical field. Semiconductors are used to build devices of modern electronics, including radio, computers, telephones, and many others. Some examples of semiconductor devices are transistor, many kinds of diodes including Schottky diodes, rectifiers, and digital and analog integrated circuits. Solar photovoltaic panels are made of semiconductors that directly convert light energy into electrical energy.

In a metal, the electric current is carried by the flow of electrons. In semiconductors, the electric current can be carried either by the flow of electrons or by the flow of positively-charged “hole”s in the electron structure of the material, or it is carried by both mechanisms.

Silicon is a basic element that is used to create most semiconductors commercially. A pure semiconductor is often called an “intrinsic” semiconductor. Some “impurities” are added into semiconductor material to change its conductivity, or ability to conduct. This process is called “doping”.

### 2.3.2 Silicon

Silicon is the most common metalloid which has the symbol Si and atomic number 14. Its atomic mass is 28.0855. The electronic configuration of silicon is $1s^2 2s^2 2p^6 3s^2 3p^2$. Although silicon is a tetravalent metalloid, which means it has four valence electrons, and is in the same group as carbon, it is less reactive than carbon. As the eighth most common element in the universe by mass, silicon very rarely occurs as the pure free element in nature, but is more widely found as various forms of silicon dioxide (silica) or silicates.

Among other semiconductors, silicon is most widely used element in semiconductor technology and therefore more information is available about the properties of devices constructed from this element [89].

### 2.3.3 Doping

The property of semiconductors can easily be changed by introducing impurities into their crystal lattice that makes them most useful for electronic devices. When impurites are added into semiconductors, their electrical properties such as their resistivites may easily be modified because the solute impurity atoms have different valence characteristics from the solvent atomic lattice. The process of adding controlled impurities to a semiconductor is known as doping. The amount of impurity, or dopant, added to an intrinsic (pure) semiconductor varies its level of conductivity. Doped semiconductors are often referred to as extrinsic [89].

### 2.3.4 Dopants

The materials chosen as suitable dopants are classified as either electron acceptors or donors. The selection of dopants depends on the atomic properties of both the dopant and the material to be doped. A donor atom incorporated into the crystal lattice donates weakly-bound valence electrons to the material, creating excess negative charge carriers. The conduction of electricity is done by these weakly-bound electrons which can move about in the crystal lattice relatively freely in the presence of an electric field. The donor atoms create some states under, but very close to the conduction band edge. Electrons at these states can be easily excited to conduction band, becoming free electrons, at room temperature. An acceptor incorporated into the crstal lattice produces a hole which is a place into which an electron can easily be accepted. Semiconductors doped with donor impurities are called *n*-type, while those doped with acceptor impurities are called *p*-type. The *n* and *p*-type descriptions indicate the type of majority carriers responsible mainly for the electrical conduction. The opposite carrier is called the minority carrier, which exists due to thermal excitation at a much lower concentration compared to the majority carrier.

Let us consider silicon as an example: The pure semiconductor silicon has four valence electrons. For silicon, the most common dopants are the elements of group III and group V. Group III elements have three valence electrons and therefore they act as acceptors when added to silicon. Group V elements have five valence electrons, which allow them to act as a donor. Therefore, a silicon crystal doped with boron (an element of group III) creates a *p*-type semiconductor whereas one doped with phosphorus (an element of group V) results in an *n*-type material [3].

## 2.4 Metals

### 2.4.1 Introduction

Metals form one of the three groups of elements along with semi-metals and nonmetals in the periodic table of elements. In metals, atoms are sometimes considered as a lattice of positive ions embedded into a cloud of delocalized electrons. The atoms in metals are arrenged in a crstal structure ( e.g, FCC, BCC and HCP). They have peculiar characteristics as distinguished by their ionization and bonding properties. Atoms in metals are bound together by their outer valence electrons by metallic bound. The metallic bonds are responsible for the free movement of the valance electrons, which make these electrons not belong to a particular atom but shared by many atoms. On the periodic table, they lie on the left side of a diagonal line drawn from boron (B) to polonium (Po) that separates the metals from the nonmetals. Most elements on this line are semi-metals and on the right side of this line are nonmetals; i.e., elements to the lower left are metals; elements to the upper right are nonmetals. According to the band theory of elements, metals have overlapping conduction bands and valence bands in their electronic structure. A very little energy is required to excite an electron from valance band to conduction band. The thermal energy is sufficiently enough for this excitation. Therefore at room temperature metals are good conductors but insulators are bad conductors which have a big energy gap between valance and conduction bands. Thermal energy is not sufficient for the electrons to overcome this energy gap to excite to the conduction band in insulators. Semiconductors have a smaller energy gap than that of insulators and some electrons are easily excited to the conduction band and they are responsible for the electric energy transportation in semiconductors at room temperature [89].

### 2.4.2 Nickel

Nickel is a chemical element which has a chemical symbol Ni and its atomic number is 28. The electronic configuration of nickel is $1s^2 2s^2 2p^6 3s^2 3p^6 4s^2 3d^8$. Nickel has a silvery-white apperance. It is one of the four ferromagnetic elements at about room temperature. It is less reactive than cobalt and iron and can not get easily oxidised. It belongs to the transitional metals and is hard and ductile [89].

### 2.4.3 Cobalt

Cobalt is a hard, grey metal. Its symbol is Co and atomic number 27. The electronic configuration of cobalt is $1s^2 2s^2 2p^6 3s^2 3p^6 4s^2 3d^7$. Cobalt is a ferromagnetic metal at room temperature. Pure cobalt is not found in nature, but compounds of cobalt are common in nature [89].

## 2.5 Electrodeposition

In simple terms, electrodeposition is the process by which suitable materials are deposited on electrically conducting substrates by the action of an electric current. Electrodeposition can be carried out by galvanostatic (constant current) or potentiostatic (constant potential) method in a two or three electrode cell. Depending on the bath composition and the current or potential applied, a single layer or a set of multilayers of metallic thin films can be deposited on suitable substrates under suitable conditions. Generally a conducting sustrate is required for electrodeposition, however a semiconducting material with enough conductivity can also be used as substrate. Therefore electrodeposition method is frequently emloyed to form metallic contact on a semiconductor [82].

## 2.6 Diodes

### 2.6.1 Introduction

In electronics, a diode is a two-terminal device. The characteristics of a diode are those of a switch that can conduct electric current in only one direction. One therefore can use a diode to convert an ac signal into a direct one.

The directionality of current flow most diodes exhibit is sometimes generically called the rectifying property. A circuit condition that allows an electric current to pass in one direction is called forward biased connection. A condition that blocks the current in the opposite direction is called the reverse biased connection. Thus, the diode can be thought of as an electronic version of a check valve.

### 2.6.2 Transistor

In electronics, a transistor is a three layer semiconductor device consisting of eiither two n- and one p- type layers of material or two p- and one n- type of material. The first one is called an npn transistor , while the latter is called a pnp transistor. A transistor is used to amplify or switch electronic signals. A voltage or current applied to one pair of the transistor's terminals changes the current flowing through another pair of terminals. Because the controlled (output) power can be much larger than the controlling (input) power, the transistor provides amplification of a signal. The transistor is the fundamental building block of modern electronic devices, and is used in radio, telephone, computer and other electronic systems. Some transistors are packaged individually but most are found in integrated circuits.

### 2.6.3 Schottky Barrier Diodes

#### 2.6.3.1 Introduction

Schottky Barrier diode is a contact between a metal and a semiconductor which has rectifying properties. The rectification of Schottky Barrier is reported first by Braun in 1874.

A Schottky diode can be formed by the connection of a metal to a doped semiconductor layer. A Schottky junction (or Schottky barrier) is formed at the junction of the metal layer and the doped semiconductor layer. Typically, a separate metallization layer is insulatively disposed over the substrate to provide an electrical contact to the Schottky contact layer. Optionally, a separate diffusion barrier layer can be interposed between the metallization layer and the underlying Schottky contact layer to prevent interdiffusion of the metallization layer with the Schottky contact layer and the semiconductor substrate. Schottky diodes have a metal-semiconductor transition as their basic structure and whose basic electronic properties are defined by this transition. A Schottky diode is formed from a semiconductor-metal combination which is chosen such that a depletion zone arises at the boundary surface. The current-voltage characteristic of this arrangement depends on the polarity of the applied voltage. A Schottky diode is characterized by a low turn-on voltage, fast turnoff, and nonconductance when the diode is reverse biased. To create a Schottky diode a metal-silicon barrier must be formed. In order to obtain the proper characteristics for the Schottky diode, the barrier metal is likely different than the metal used in other process steps such as metal ohmic contacts. When forward biased, a Schottky diode provides a low-resistance current path and, when reverse-biased, a high-resistance current path. On the other hand, the metal contact, which is formed on the heavily-doped region, has a current-to-voltage (*I/V*) relationship that is linear or resistive. A Schottky diode is primarily a majority carrier device. Under many circumstances (primarily low injection conditions), current is conducted primarily by majority carriers. As a consequence, Schottky diodes often have faster switching times than *p-n* junction diodes of comparable size. The voltage-current characteristics of Schottky diodes are very similar to the voltage-current characteristics of *p-n* junction diodes. Schottky diodes can be switched from one state to another, either from on to off or from off to on much faster that *p-n* junction

diodes. The performance of the Schottky diode is typically gaged by the product of its series resistance and its junction capacitance. This product must be minimized for the best performance to be achieved. Unguarded Schottky diodes typically have poor reverse leakage and poor breakdown characteristics. To improve leakage characteristics, high performance Schottky diodes are provided with junction guard rings. Guard rings provide excellent breakdown characteristics in both forward and reverse bias. Schottky diode is an important power device and used extensively as output rectifiers in switching-mode power supplies and in other high-speed power switching applications, such as motor drives, switching of communication device, industry automation and electronic automation and so on.

Schottky diodes are widely used as voltage rectifiers in many power switching applications, such as switching-mode power supplies, electric motor, switching of communication device, industry automation and electronic automation. The use of a Schottky diode generally allows integrated circuits to have greater speed because it is a majority carrier device [90].

#### 2.6.3.2 Barrier Formation

To consider the characteristic parameters of Schottky diodes, a proper contact is needed. There is a charge transporting between the metarials when the metal is brought into contact with the semiconductor until the electrochemical potantials equalize [91]. When the work function of metal is bigger than the semiconductor in *n*-type contacts, a rectifier contact occurs.

#### 2.6.3.3 Metal / *n*-type Semiconductor Rectifier (Schottky) Contact

When the metal is brought into contact with the semiconductor an equilibrium state occurs because of the charge transporting and the Fermi level of both materials become equal. The donors in the semiconductor are ionized at room temperature. In the rectifier contact state the electrons flow from the semiconductor into the metal.

There will be a dipol level in the contact region because of the new charge distribution. A potential barrier prevents the electron flowing from the opposite side which is relevant to the energy-band diagram. This case is shown in Figure 2.1. $\Phi_m$ is the work function of the metal, $\Phi_s$ is the work function of the semiconductor, $\chi_s$ is

the electron affinity of the semiconductor, corresponds to the energy separation between the vacuum level and the conduction band edge of the semiconductor [92].

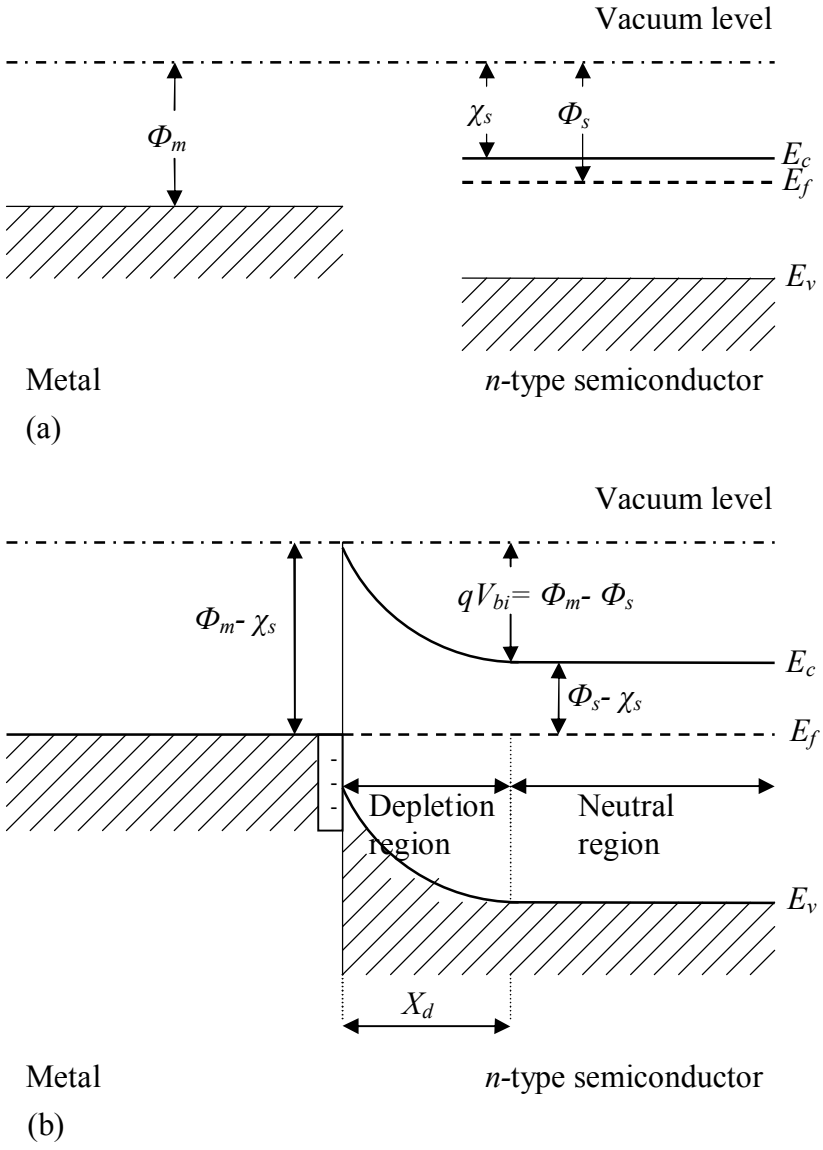



Figure 2.1 (a) The energy band diagrams of the metal and the semiconductor before the contact (b) The energy band diagram after the contact

Before the contact the Fermi level of the semiconductor is bigger than that of the metal. After the contact the Fermi level of the semiconductor is lowered. Electrons must be transferred from semiconductor to metal, creating a depletion region in the near surface of the semiconductor and excess negative charge on the metal side while the flowing electrons leave ionized donors behind.

Energy levels of the both materials equalize. As a result because of the dipol level, a potential barrier occurs in the surface. The height of this barrier is ($\Phi_m$-$\Phi_s$) in the semiconductor side and ($\Phi_m$-$\chi_s$) in the metal side. It is also expressed as:

$$qV_{bi\ (dif)} = \Phi_m\text{-}\Phi_s \tag{2.1}$$

where $V_{dif}$ potential measured due to the metal surface is the diffusion potential. Because of the ionized donors there will be positive charges in the semiconductor side of the contact and these positive charges are at rest, thus the surface level of the contact is called as space charge level. Because of the potential barrier in the contact, the surface level is called as barrier level. The thickness of this level (d) is depended on the concentration of the charges and the value of diffusion potential. When the energy gained by the electrons with thermal way is big enough to exceed the potential barier, an equal and in the opposite side leakage current ($I_o$) pass across from the contact.

If $-V$ voltage is applied on the semiconductor, the barrier height doesn't change for the electrons that will flow from metal into the semiconductor, so the current of the electrons doesn't change also. But on the semiconductor side, conductivity band increases by $qV$ and the barrier height decreases by $qV$ for the electrons that will flow into the metal.

Thereby, the current flow from the metal into the semiconductor increaes by *exp(qV/ kT)*. In this case, the net current occured is;

$$I = I_o\left[\exp\left(\frac{qV}{nkT}\right) - 1\right],\ I \text{ is positive.} \tag{2.2}$$

This bias is called forward bias ($V>>kT/q$).

When $+V$ voltage applied on the semiconductor side, conductivity band decrease by $qV$ and the barrier height on the semiconductor side increases by $qV$, net current tends to $-I_o$ value. This bias is called reverse bias ($V<<kT/q$).

### 2.6.3.4 The Effects on The Schottky Barrier Height

The barrier height in an ideal metal-semiconductor contact is given as:

$$\Phi_{bn} = \Phi_m - \chi_s \tag{2.3}$$

where $\Phi_m$ is the work function of the metal contact, $\chi_s$ is the electron affinity of the semiconductor (the energy difference between the base of the conduction band and the vacuum level). Some effects can make deviations in the Schottky barrier height that given in the equation (2.3) i.e. the emission current in the cathode increases with increasing in the field forces. This effect is called as Schottky effect and expresses that the work function of the cathode depends on the surface field force. An electron in the dielectric at a distance $x$ from the metal surface causes an electrical field. The field lines will be perpendicular to the metal surface and same with that of the $+e$ image charge localised at a distance $x$ from the metal surface to the inside. The force effects on the electron that caused from the influence of Coulomb and the image charge is called as the image force and expressed as:

$$F = \frac{-e^2}{4\pi\varepsilon_S(2x)^2} = -Ee \tag{2.4}$$

while the potential can be found as:

$$-\Phi(x) = +\int_x^\infty E dx = \int_x^\infty \frac{e}{4\pi\varepsilon_S 4(x)^2} dx = \frac{-e}{16\pi\varepsilon_S x} \tag{2.5}$$

where $x$ is the integral variable and for $x = \infty$ we accepted the potential as zero. The potential is given in the equation (2.5) where the external electrical field is zero. If the external electrical field is different from zero, then equation will be

$$-\Phi(x) = \frac{-e}{16\pi\varepsilon_S x} - Ex \tag{2.6}$$

The equation (2.5) will lose its validity for the small values of $x$ and while $x$ goes the zero, $-\Phi(x)$ approaches to $\infty$. The second term in the equation expresses the quantity in the decreasing in the potential barrier because of the external field.

This decreasing in the potential barrier is called as Schottky effect or the

lowering with the image force. We obtain the Schottky barrier lowering $\Delta\Phi$ with the condition of

$$\frac{d[e\Phi(x)]}{dx} = 0 \tag{2.7}$$

and $X_m$, the maximum barrier as:

$$X_m = \sqrt{\frac{e}{16\pi\varepsilon_S E}} \tag{2.8}$$

**2.6.3.5 Current Transmission With Thermionic Emission in the Schottky Diodes**

The procedure of the electron transmission over the potential barrier in the Schottky contact is explained with the thermionic region emission theory. From a hot surface the oscillation of the carriers because of the thermal energy is known as thermionic emission.

In the metal-semiconductor Schottky diodes, thermionic emission theory is based on exceeding the potential barrier by the carriers with enough thermal energy, from the semiconductor to metal or from the metal to semiconductor.

In the Schottky diodes, the current provided by majority carriers. In the metal *n*-type semiconductor Schottky diodes, the electrons (in the metal/*p*-type semiconductor Schottky diodes holes) provide the current. While forming the thermionic emission theory to apply Maxwell-Boltzmann approach and not to be affected from the thermal equilibrium state, it is accepted that the potential barrier belongs to rectify contact is bigger than kT energy and the carrier collisions in the depletion region are very small. In the Figure 2.2, a $V_a$ forward bias voltage applied at the Schottky contact is seen [92].

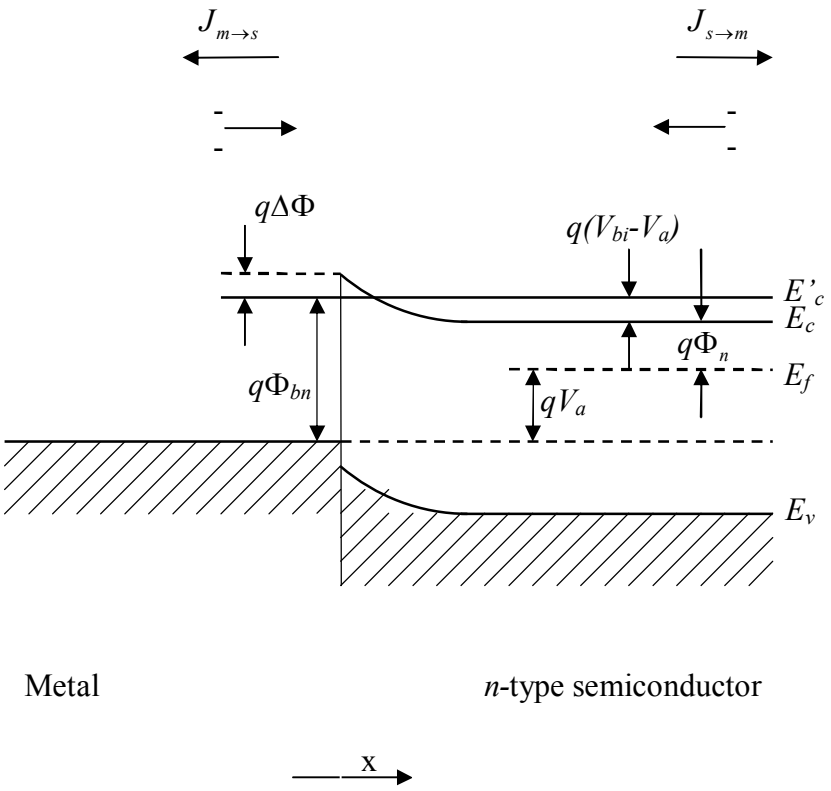



Figure 2.2 The energy-band diagram of the image decreasing effect in the metal-semiconductor Schottky diode under the forward bias

Here $J_{s\to m}$ is current density from the semiconductor to the metal and $J_{m\to s}$ is that from the metal to the semiconductor. $J_{s\to m}$ current density is a function of the concentration of the electrons which have a velocity enough to exceed the barrier in $x$ way. Thus,

$$J_{s\to m} = q\int_{E_c}^{\infty} v_x dn \tag{2.9}$$

can be written [3]. Here $E'_c$ is the minimum energy needed for the thermionic emission in the metal, while $v_x$ is the velocity in the drift way. Increasing concentration of the electrons is given as;

$$dn = g_c(E)f(E)dE \tag{2.10}$$

Here $g_c$ *(E)* is the density of state in the conductivity band and *f(E)* is the Fermi-Dirac (probability) distribution function. By applying Maxwell-Boltzmann approach, for the concentration of the electrons,

$$dn = \frac{4\pi(2m_n^*)^{3/2}}{h^3}\sqrt{E-E_c}\exp\left[\frac{-(E-E_f)}{kT}\right]dE \tag{2.11}$$

is obtained, where $m_n$* is the effective mass of the *n*-type semiconductor and *h* is the planck constant.

The ($E$-$E_c$) energy is accepted as the kinetic energy of the free electron, then

$$\frac{1}{2}m_n^* v^2 = E - E_c \tag{2.12}$$

$$dE = m_n^* v dv \tag{2.13}$$

and

$$\sqrt{E-E_c} = v\sqrt{\frac{m_m^*}{2}} \tag{2.14}$$

is obtained.

When the equation (2.11) is rewritten by using these results,

$$dn = 2\left(\frac{m_n^*}{h}\right)^3 \exp\left(\frac{-q\Phi_n}{kT}\right)\exp\left(\frac{-m_n^* v^2}{2kT}\right)4\pi v^2 dv \tag{2.15}$$

is obtained. This equation gives the number of electrons per unit volume which have the velocities between $v$ and $v + dv$. If the velocity is seperated into its components, $v^2 = v_x^2 + v_y^2 + v_z^2$ is obtained. The equation (2.9) can then be written as,

$$J_{S\to m} = 2q\left(\frac{m_n^*}{h}\right)^3 \exp\left(\frac{-q\Phi_n}{kT}\right)\int_{-\infty}^{\infty} v_x \exp\left(\frac{m_n^* v_x^2}{2kT}\right)dv_x \int_{-\infty}^{\infty}\exp\left(\frac{-m_n^* v_y^2}{2kT}\right)dv_y$$
$$\int_{-\infty}^{\infty}\exp\left(\frac{-m_n^* v_z^2}{2kT}\right)dv_z \tag{2.16}$$

Also for the minimum $v_{ox}$,

$$\frac{1}{2}m_n^* v_{ox}^2 = q(V_{bi} - V_a) \tag{2.17}$$

can be written. $v_{ox}$ is the minimum velocity needed for the electrons to exceed the potential barrier in $x$ direction. Using the minimum velocity condition $v_x \rightarrow v_{ox}$, and the variable changes and $v_x dv_x = \left(\frac{2kT}{m_n^*}\right)\alpha d\alpha$ as follows:

$$\left(\frac{-m_n^* v_x^2}{2kT}\right) \equiv \alpha^2 + \frac{q(V_{bi} - V_a)}{kT} \tag{2.18a}$$

$$\left(\frac{-m_n^* v_y^2}{2kT}\right) \equiv \beta^2 \tag{2.18b}$$

$$\left(\frac{m_n^* v_z^2}{2kT}\right) \equiv \gamma^2 \tag{2.18c}$$

The expression in the equation (2.16) becomes

$$J_{s\rightarrow m} = J_{x\rightarrow\infty} = 2q\left(\frac{m_n^*}{h}\right)^3\left(\frac{2kT}{m_n^*}\right)^2 \exp\left(\frac{-q\Phi_n}{kT}\right)\exp\left[\frac{q(V_{bi} - V_a)}{kT}\right]$$

$$x\int_0^\infty \alpha \exp(-\alpha^2)da \int_{-\infty}^{\infty}(-\beta^2)\int_{-\infty}^{\infty}(-\gamma^2)d\gamma \tag{2.19}$$

When the last expression is integrated,

$$J_{s\rightarrow m} = \left(\frac{4\pi q m_n^* k^2}{h^3}\right)T^2 \exp\left[\frac{-q(\Phi_n + V_{bi})}{kT}\right]\exp\left(\frac{qV_a}{kT}\right) \tag{2.20}$$

or

$$J_{s\rightarrow m} = \left(\frac{4\pi q m_n^* k^2}{h^3}\right)T^2 \exp\left[\frac{-q(\Phi_{bn})}{kT}\right]\exp\left(\frac{qV_a}{kT}\right) \tag{2.21}$$

are obtained.

As seen in Figure 2.2 $\Phi_n + V = \Phi_{bn}$ and when voltage applied is zero $J_{m\to s}$ and $J_{s\to m}$ are entirely the same. That is,

$$J_{m\to s} = \left(\frac{4\pi q m_n^* k^2}{h^3}\right) T^2 \exp\left[\frac{-q(\Phi_{b0})}{kT}\right] \tag{2.22}$$

Net current density in the junction becomes

$$J = J_{s\to m} - J_{m\to s} \tag{2.23}$$

Obviously, the net current density is

$$J = \left[A^* T^2 \exp\left(\frac{-q\Phi_{bn}}{kT}\right)\right]\left[\exp\left(\frac{qV_a}{kT}\right) - 1\right] \tag{2.24}$$

Here $A^*$ is the Richardson constant for the thermionic emission and given as,

$$A^* = \frac{4\pi q m_n^* k^2}{h^3}$$

For a general condition, the expression (2.24) can be written as,

$$J = J_0\left[\exp\left(\frac{qV_a}{kT}\right) - 1\right] \tag{2.25}$$

Here $J_0$ is known as reverse saturation current density and express [3] as;

$$J_0 = A^* T^2 \exp\left(\frac{-q\Phi_{bn}}{kT}\right) \tag{2.26}$$

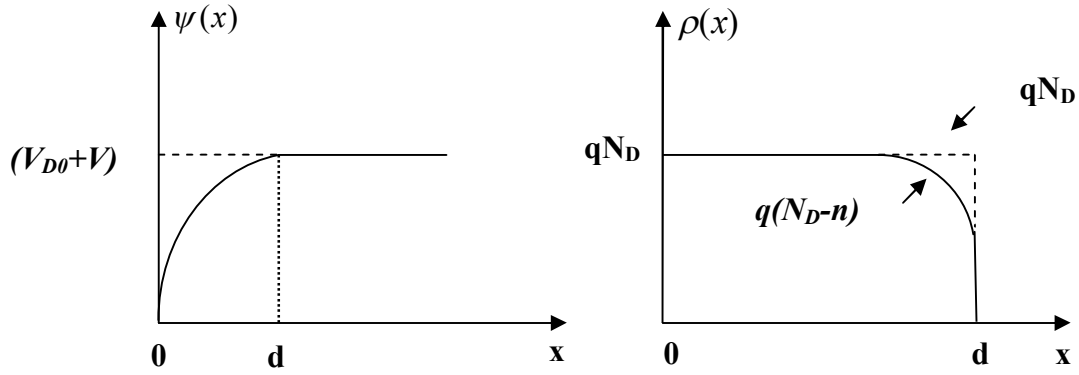
When we give attention to the Schottky barrier height decreasing with the image force and defining $\Phi_{bn}$ as $\Phi_{bn} = \Phi_{b0} - \Delta\Phi$, then the equation (2.26) can be written as

$$J_0 = A^* T^2 \exp\left(\frac{-q\Phi_{bn}}{kT}\right)\exp\left(\frac{q\Delta\Phi}{kT}\right) \tag{2.27}$$

$\Delta\Phi$ change in the barrier height will increase with increase in electrical region or the reverse bias voltage [92].

### 2.6.3.6 The Schottky Capacity in the Metal-Semiconductor Schottky Diodes

Depletion region (dipol level) in the metal-semiconductor contact structures act like a capacitor with the space charges in the semiconductor side and surface charges in the metal side. When the voltage increased in the state of reverse bias, the width of the depletion region increases. If there is an important hole density in the semiconductor close to the metal, because of the coincidence of the new Fermi level with the Fermi level in the metal, hole density decrease.




(a) (b)

Figure 2.3 (a) potential distribution (b) Charge distribution of the metal/*n*-type rectifying contacts dependent to the state

The capacity of the Schottky region will change because of this charge exchange. For these properties, Schottky diodes can be used as variable capacitor with voltage control. To find the capacity of the Schottky region, the Poisson equivalent of the potential distribution at the barrier layer of the diode, can be expressed as [91];

$$\nabla^2\psi(x)=\frac{d^2\psi}{dx^2}=-\frac{\rho(x)}{\varepsilon_s\varepsilon_0} \tag{2.28}$$

where $\varepsilon_s$ is the dielectric constant of the semiconductor, $\varepsilon_0$ is the dielectric constant of vacuum, $\rho(x)$ is the density of space charge dependent to the state. The density of space charge can be written as [4];

$$\rho(x) = q(N_D - n) \tag{2.29}$$

where $N_D$ is the donor concentration of *n*-type semiconductor substrate. *n* is the density of the electron in the conduction band of the semiconductor. The graphs of the potential function $\psi(x)$ and the space charge density $\rho$ (x) dependent to the state are shown in Figure 2.3.

Let $V_D$ refer to the diffusion potential of barrier layer and -*V* refer to the potential applied to the contact. As a result $N_D >> n$, since $q(V_D\text{-}V) >> kT$ in the $0 \le x \le d$ . So, for *n*-type semiconductor we can write as;

$$\rho(x) \cong qN_D \tag{2.30}$$

When this equation is used in the Poisson equation,

$$\frac{d^2\psi}{dx^2} = -\frac{qN_D}{\varepsilon_s \varepsilon_0} \tag{2.31}$$

is obtained.

The solution of this last equation can be looked for in these conditions:

1) for $x = 0$ $\psi(x) = 0$

2) for $0 \le x \le d$ $\psi(x) = V_{D0} \pm V$

3) for $x = d$ $\frac{d\psi(x)}{dx} = 0$

For the equation (2.31), with the 3rd condition, when we integrate, we can obtain the electric field of depletion region.

$$E(x) = -\frac{d\psi(x)}{dx} = \frac{qN_D}{\varepsilon_s \varepsilon_0}(x - d) \tag{2.32}$$

by the integrating equation (2.32) with the 1st condition.

$$\psi(x) = -\frac{qN_D}{\varepsilon_s \varepsilon_0}(\frac{1}{2}x^2 - xd) \tag{2.33}$$

is obtained. When the solution of this last equation with the 2nd condition is made;

$$d = [\frac{2\varepsilon_s \varepsilon_0}{qN_D}(V_{D0} \pm V)]^{\frac{1}{2}} \tag{2.34}$$

is obtained, which is the width of the Schottky region, where $V_{D0}$ is the diffusion potential at the zero voltage. For $V>0$, the contact is reverse bias, for $V<0$ it is forward bias. In the semiconductor the charge density for unit area is given by

$$Q = qN_D d \tag{2.35}$$

By using (2.34) and (2.35) equations

$$Q = [2\varepsilon_s \varepsilon_0 qN_D(V_{D0} \pm V)]^{\frac{1}{2}} \tag{2.36}$$

is obtained. The Schottky capacity is defined as the exchange of the $Q$ charge according to the voltage which has the equivalent (2.36). So the capacity can be written as;

$$C = \frac{\partial Q}{\partial V} \tag{2.37}$$

and from (2.36) and (2.37) equations

$$C = [\frac{\varepsilon_s \varepsilon_0 qN_D}{2(V_{D0} + V)}]^{\frac{1}{2}} \tag{2.38}$$

or

$$C = \frac{\varepsilon_s \varepsilon_0}{d} \tag{2.39}$$

can be found. As seen, the capacity of depletion region is inverse proportional with voltage applied and the width of the Schottky region and directly proportional with donor density.

### 2.6.3.7 Cheung Functions and Determining the Characteristics of Schottky Diode

Cheung presented (1986) a different model for calculation of Schottky diode parameters with the forward bias *I-V* characteristics of metal-semiconductor contact structure [93].

When the current density (*J*) found from thermionic emission is multiplied by the effective area "*A"* of the diode, the total current in the diode:

$$I = A \cdot J = \left[ AA^{*}T^{2} \exp\left( \frac{-q\Phi_{bn}}{kT} \right) \right] \left[ \exp\left( \frac{qV_a}{kT} \right) - 1 \right] \tag{2.40}$$

is obtained. In this equation if $qV_a \gg kT$ , 1 can be ignored. In practice all the voltage applied doesn't fall into the depletion region, so there will be deviations from the ideal state. To express these deviations, we should use constant (*n*), ideality factor. In this case, current equation will be:

$$I = A \cdot J = \left[ AA^{*}T^{2} \exp\left( \frac{-q\Phi_{bn}}{kT} \right) \right] \left[ \exp\left( \frac{qV_a}{nkT} \right) \right] \tag{2.41}$$

The part $IR_S$ of ($V_a$) voltage applied drops on the series resistance, so, when we take:

($V_a \rightarrow V_a$ - $IR_S$ ) instead of $V_a$ we obtain

$$I = A \cdot J = \left[ AA^{*}T^{2} \exp\left( \frac{-q\Phi_{bn}}{kT} \right) \right] \left[ \exp\left( \frac{q(V_a - IR_S)}{nkT} \right) \right] \tag{2.42}$$

when we take the logarithm of the last equation and solve according to $V_a$,

$$V_a = \left( \frac{nkT}{q} \right) \ln\left( \frac{I}{AA^{*}T^{2}} \right) + n\Phi_{bn} + IR_S \tag{2.43}$$

is obtained. If the differentiation of the equation according to $\ln I$ is made:

$$\frac{dV_a}{d(\ln I)} = \frac{nkT}{q} + IR_S \tag{2.44}$$

is obtained. The graph of $dV/d(\ln I)$ versus $I$ in the equation (2.44) is a line and the slope of this line gives $R_S$, series resistance. The ideality factor ($n$) can be found from the intersection point of this line with the vertical axis (Cheung and Cheung, 1986). The potential barrier height $(\Phi_{bn})$ can be defined from a $H(I)$ function as;

$$H(I) = V_a - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{2.45}$$

From equations (2.43) and (2.44)

$$H(I) = n\Phi_{bn} + IR_S \tag{2.46}$$

is obtained. If the graph of $H(I)$-$I$ is drawn, the slope of the line obtained gives ($R_S$) series resistance. $q\Phi_{bn}$ barrier height can be found from the intersection point of the line with $H(I)$ axis**.**

### 2.6.4 Metal / *n*-type Semiconductor Ohmic Contacts

Let a metal and a semiconductor be in a contact state in the case of ($\Phi_m < \Phi_s$ ). $\Phi_m$ is the work function of the metal, $\Phi_s$ is the work function of the semiconductor. Before the contact is establihed, the Fermi level of the semiconductor is lower than the metals, as ($\Phi_s - \Phi_m$). The energy band diagram of the metal and semiconductor before the contact is shown in Fig.2.4.a. [92]. Here $\chi_s$ is the electron affinity of the semiconductor.

After the contact in the thermal equilibrium state, an electron flowing occurs from the metal into the semiconductor and in this case the *n*-type of the semiconductor surface increases. In this phase in the semiconductor surface, the electrons make a surface charge layer. Again the electrons sepeared from the metal, left a surface charge layer behind and thus a diode layer occurs in the contact region. This case is shown in Fig.2.4.b. [92]. If a positive $+V$ voltage applied into the metal side, there will be a barrier for the electrons flowing to the metal from the semiconductor and the electrons easily flow in this direction. (Fig. 2.4.c) [92].

If a $+V$ voltage applied to the semiconductor side, because of the extremely doping state of the semiconductor the barrier height of which the electrons meet will be very low, so that the electrons flow easily from the metal into the semiconductor

(Fig. 2.4.d) [92]. As a result in such a contact, the electrons move easily to both side. The contacts occured in this way called ohmic contacts. When a $+V$ voltage applied to the ohmic contact, the potential will scatter to whole of the body. When a $-V$ voltage applied to the metal, because of the transition of the electrons from the metal into the conductivity band of the semiconductor, these contacts are called the enjection contacts [94].

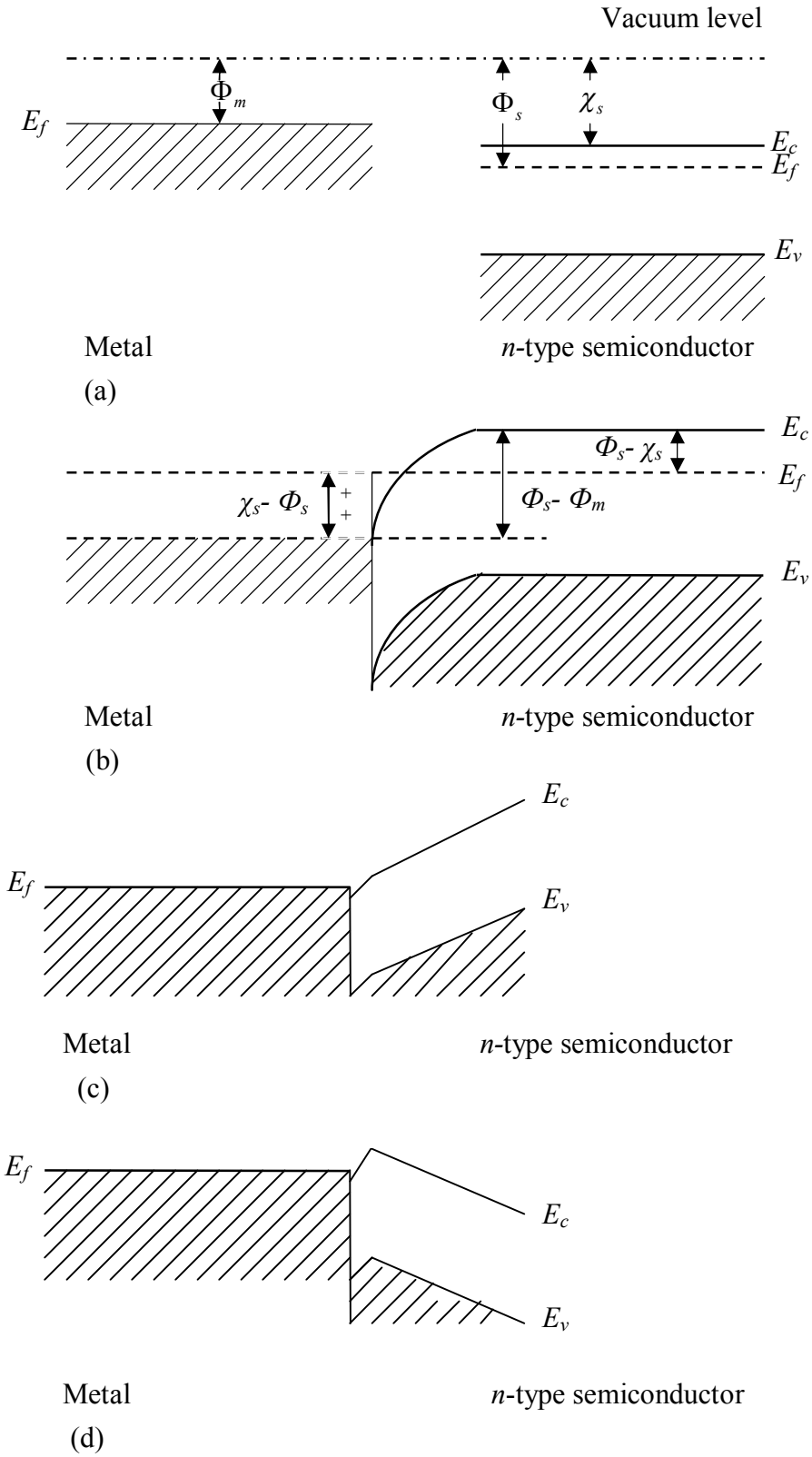



Figure 2.4 The energy band diagram of metal/*n*-type semiconductor ohmic contact for $\Phi_m < \Phi_s$ (a) Before the contact (b) After the contact (c) under the reverse bias (d) under the forward bias

## 2.7 Magnetoresistance

Magnetoresistance is defined as an influence on electron motion by an external magnetic field. The applied magnetic field increases the scattering probability of conduction electrons within the materials and subsequently result in an increase in resistance. When the effect depends on the relative orientation of magnetisation vector with respect to current direction, the effect is called anisotropic magnetoresistance. This efect occurs in all metals but it is strongest in magnetic metals. The resistance of metal gets the lowest value when the magnetisation vector is at $90^o$ and the highest when the magnetisation is at $0^o$ to the current direction. The origin of the anisotropic effect comes from the spin orbit coupling [95].

The giant magnetoresistance was discovered in 1988 in multilayer systems. The giant magnetoresistance depends on the relative orientation of the magnetisation vectors of the magnetic layers. When the magnetisation vectors of layers are antiferromagnetically coupled the resistance gets the highest value while it gets the lowest one when the magnetisation vectors are ferromagnetically coupled [45]. The giant magnetoresistance effect also exists in heterogeneous alloys with ferromagnetic granules (like Co) embedded in a non-magnetic metal (like in Ag) [96]. The characteristics of magnetoresistance observed in these heterogeneous systems are similar to those observed in the multilayer structures. In both cases the maximum resistance occurs when the field is equal to the coercieve field Hc, at which the net magnetisation is zero .

# CHAPTER 3

# EXPERIMENTAL TECHNIQUES

## 3.1 Introduction

In this chapter, first, the electrodeposition technique for the production of the magnetic Ni and Co films on *n*-Si semiconducting wafer is introduced. Then, the experimental set up is described for the electrodeposition of these films. Finally, the experimental procedure is presented for magnetoresistance measurement.

## 3.2 Electrodeposition Method

Electrodeposition is a low-temperature, cost effective, and particularly attractive method for its vital role in the fabrication of self-assembled metallic nanostructures where line-of-sight techniques do not work and it is tested as a useful alternative to physical obtention methods for metallic thin films [97-101]. Many metallic thin films such as Cu, Co and Ni and their alloys have already been electrodeposited directly on *n*- or *p*-type silicon substrates. The direct deposition of metallic films on a semiconducting substrate without a seed layer makes the integration of an efficient, inexpensive and convenient method possible with the the silicon technology [98].

In general, the main concerns in the practical application of electrodeposition can be summarized as follows;

- Chemical and electrochemical stability are required for the solvent and cathode elecrode which is used as substrate. Depending on the final product, aqueous or nonaqueous solutions are used as an electrolyte and the deposition quality is strongly affected by the purity of the solution.

- The characteristics of the substrates such as the stability, surface conditions and morphology are the determining factors for initial and subsequent deposition. The substrate may vary from being a liquid metal to a single crystal.
- The electrical resistivity of deposited layers should be low enough to allow the current density to remain in the optimum range, and before electrodeposition any existing surface oxide must be removed by reaction with the solvent.
- Although deposition can be achieved under constant current, constant potential or by other means involving pulsed current or voltage, the current density level must remain within the pre-defined values, depending on the materials involved.
- Doping during the electrodeposition and post-deposition treatments is often needed to improve the characteristics of the films [82].

### 3.2.1 Experimental set-up of Electrodeposition System

The electrodeposition of a metallic coating onto an object is achieved by putting a negative charge on the object to be coated and immersing it into a solution (in other words, the object to be plated is made as the cathode of an electrolytic cell) [100-101]. Metal or semiconductor material can be deposited on the cathode. Schematic diagram of the electrodeposition systems shown in Figure 3.1.

According to the Faraday's rule, the amount of deposit is proportional to the total amount of charge which passes during the depositing. This rule is employed to determine thin film thickness, as in the following expression;

$$G / A = j\ t\ E\ \alpha \qquad (g\ cm^{-2}) \tag{3.1}$$

Where G / A is weight deposited per unit area, J is the current density, t is the time and α is the current efficiency which is the ratio of the experimental to theoretical weight deposited and E is elecric field. It can generally be expected to be between unity and 0.5. This equation can be written in a slightly different form to give the rate of deposition. If a thickness L is deposited in time t, then the rate of deposition L / t is given by

$$L / t = ( j E \alpha ) / \rho \qquad (cm / sec) \tag{3.2}$$

where ρ is the film density [82].

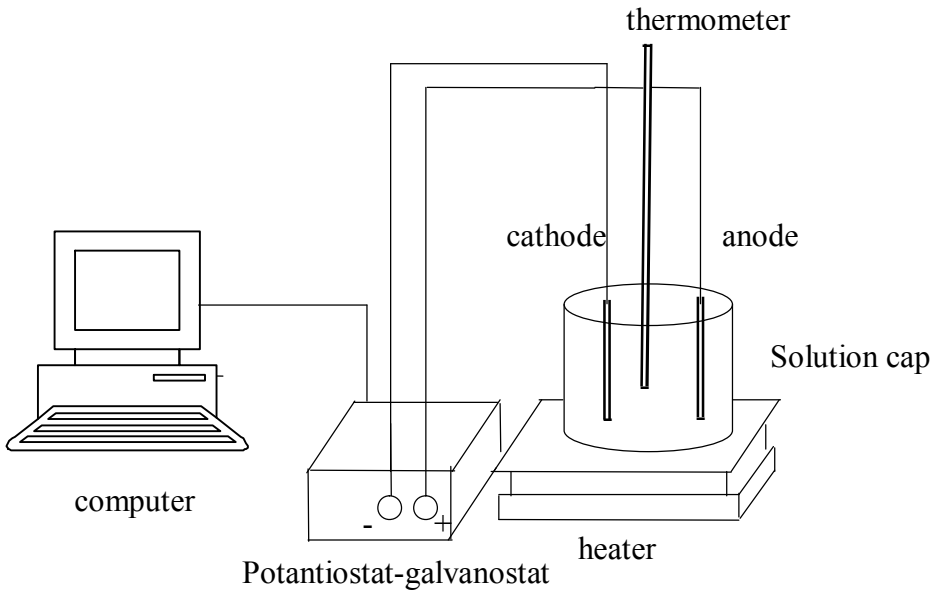



Figure 3.1 The schematic diagram of the electrodeposition system

Our system is controlled by computer during the electrodeposition process to provide a constant potential or a constant current for a certain period of time. A magnetic heater can be used to stir and to control the temperature of the chemical solution if required.

### 3.3 Growth Mechanism of the Thin Films by Electrodeposition Method

Metal deposition on semiconductor surfaces or metalization plays an important role in the electronics industry [102-105] as it is a key step in many applications. The characterization of electrodeposited Ni-Si contacts reveals that the resulting SB is superior to those fabricated by other metallization techniques [106-108].

Electrochemical deposition occurs when ions in a solution become part of the surface of an electrode by accepting electrons and becoming neutral. In this manner, metalic thin films can be deposited on an electrode by passing current through the solution. Several factors in electrodeposition influence the performance and quality of the produced semiconducting thin films [82].

These factors are as follows;

a. The properties of substrate
b. The composition of solution
c. Current density
d. The pH value of solution
e. Deposition time
f. Stiring rate
g. Solution temperature

The applied potential or current during deposition process.

### 3.4 Preparation of the Substrate

The used *n*-type Si wafer was (100) oriented. To take an efficient result in performing diode, wafers should be cleaned from organic and mechanic impurity. Thus, we chemically cleaned substrate using RCA cleaning procedure by following the process below:

- The wafer was boilt in $NH_4OH+H_2O_2+6H_2O$ 10 minutes.
- Boilt in $HCl+H_2O_2+6H_2O$ 10 minutes.
- The native oxide on the front surface of the substrates was removed in $HF:H_2O$ (1:10) solution.
- Rinsed in de-ionized water for 30 seconds.

### 3.5 Fabrication of Schottky Diodes

At first to make an ohmic contact to the dull surface of the substrate, the heater is washed with %10 HCl, then cleaned with deionized water and dried. After that it is put in place in vacuum apparatus and fired to be ready. Then the substrate is put in the vacuum apparatus to the table which has a proper height for the ohmic contact as its dull surface looks down.

As a result of the vacuum process, when the pressure drops to $10^{-5}$ torr level, gold-antimony alloy (Au %99 - Sb %1) which is put on the heater after drying is evaporated. After waiting a period making reverse process, air is given to the vacuum apparatus and by taking out the substrate from the vacuum apparatus and putting it in the quartz cirucible pota chemically cleaned, then heated for 3 minutes in the oven at $420^0$C. The diagram of the oven system used for annealing is shown in the Figure 3.2. By this way the ohmic contact process is completed.

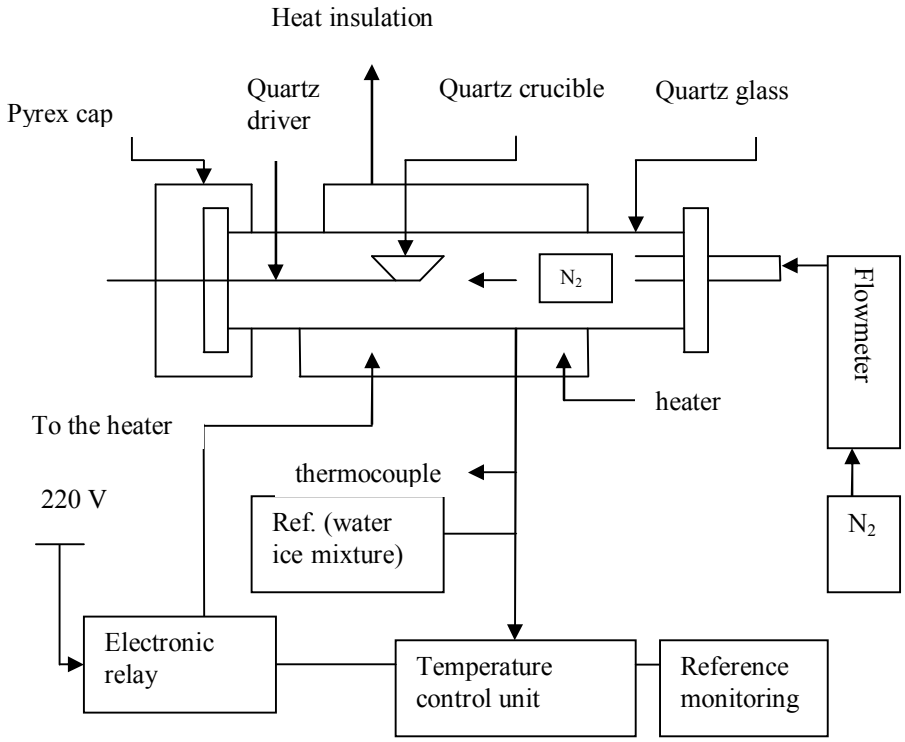



Figure 3.2 The diagram of the oven and control unit for the ohmic contact thermal process

### 3.6 The Development of the Nickel Layer on the *n*-type Silicon Wafer

The Schottky contacts were formed on the front face of the *n*-Si as dots with diameter of about 1 mm by the galvanostatic electrodeposition of Ni. Acid resistant adhesive tape was used to mask off all the substrate except for the deposition area. The electrodeposition of Ni films on *n*-type Si substrate has been carried out at room temperature from an aqueous electrolyte containing 1M Ni sulphate and 0.5M boric acid. The *n*-Si substrate was used as cathode while a Pt plate was anode. A current density of 3 $mA/cm^2$ was maintained between the two electrodes as seen in Figure 3.3. Film thickness was determined as 150 nm by deposition time.

During the deposition process positively charged $Ni^{+2}$ ions are accelerated under the influence of the applied potantial towards the cathodic electrode.

By taking into account these results, to produce good quality Ni film on *n*-Si by the galvanostatic growth method, the following deposition conditions should be considered:

- pH : 4
- Deposition time : 80s
- Applied current : $3mA/cm^2$
- Solution temperature : Room temperature
- Stiring rate : No

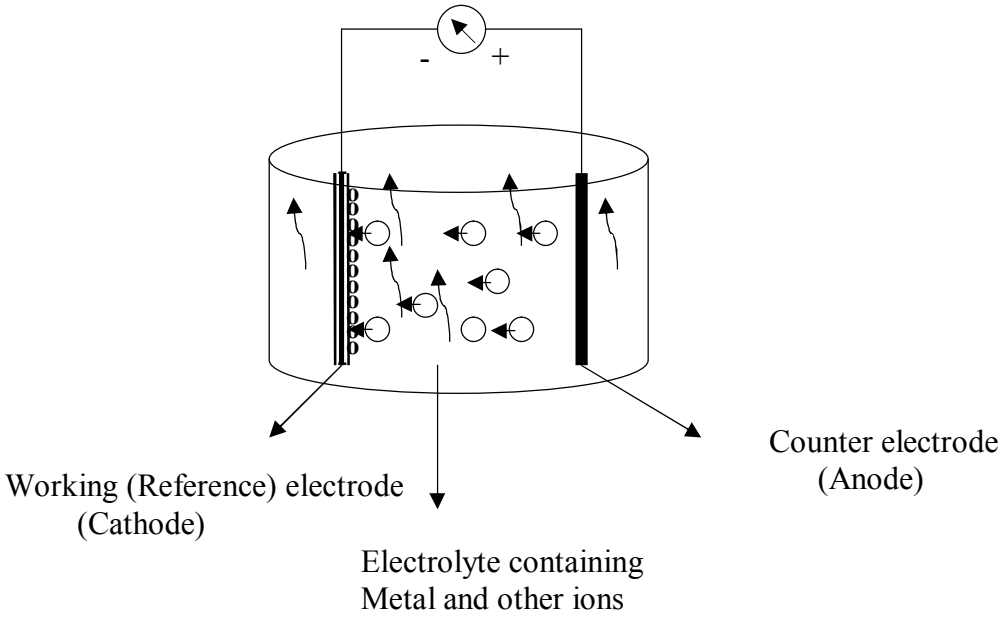



Figure 3.3 The schematic representation of a set-up for electrodeposition

### 3.7 The Development of the Cobalt Layer on the *n*-type Silisyum Wafer

The Schottky contacts were formed on the front face of the *n*-Si as dots with diameter of about 1 mm (the diode area= $7.85 \times 10^{-3}$ $cm^2$) by the galvanostatic electrodeposition of Co. Acid resistant adhesive tape was used to mask off all the substrate except for the deposition area. The electrodeposition of Co films on *n*-type Si substrate has been carried out at room temperature from an aqueous electrolyte containing 1M Co sulphate and 0.5M boric acid. The *n*-Si substrate was used as cathode while a Pt plate was anode. A current density of 3 $mA/cm^2$ was maintained between the two electrodes as seen in Figure 3.3. Film thickness was determined as 150 nm by deposition time.

During the deposition process positively charged $Co^{+2}$ ions are accelerated under the influence of the applied potantial towards the cathodic electrode.

By taking into account these results, to produce good quality Co film on *n*-Si by the galvanostatic growth method, the following deposition conditions should be considered:

- pH : 4
- Deposition time : 80s
- Applied current : 3mA/cm$^2$
- Solution temperature : Room temperature
- Stiring rate : No

### 3.8 Experimental Procedure of the Magnetoresistance

As described above in the parts 3.6 and 3.7, the electrodeposition of Ni and Co films on on the front face of *n*-type Si substrate has been carried out at room temperature from an aqueous electrolyte containing 1M Ni sulphate and 0.5M boric acid for Ni electrodeposition, 1M Co sulphate and 0.5M boric acid for Co electrodeposition by the galvanostatic method. Acid resistant adhesive tape was used to mask off all the substrate except for the deposition area. The deposited film area for Co and Ni was 4mmx4mm. The *n*-Si substrate was used as cathode while a Pt plate was anode. A current density of 3 mA/cm$^2$ was maintained between the two electrodes. All the film thicknesses were determined as 150 nm by deposition time. The bath pH was 3 for Co and Ni electrodeposition films.

The magnetoresistance measurements were done using the Van der Pauw technique with four spring loaded contacts. The MR effect was calculated from the relation of MR % = $\{[R(H_{MR})-R(H_{MR}=0)]/R(H_{MR}=0)\}$x100 where $R(H_{MR})$ and $R(H_{MR}=0)$ are the resistances with and without the external magnetic field $H_{MR}$ respectively. The MR measurements of the electrodeposited films were performed in the longitudinal (LMR) and transverse (TMR) geometries as described in Figure 3.4.

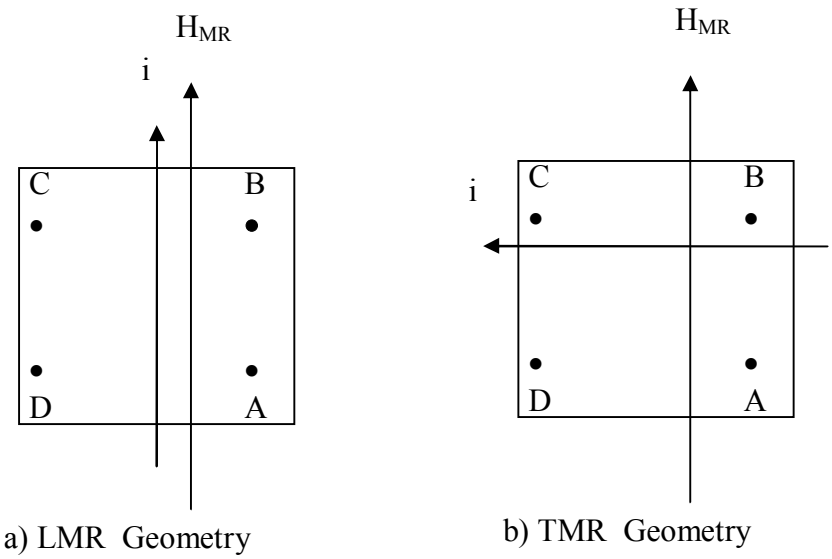



Figure 3.4 Longitudinal (LMR) and transverse (TMR) geometries

# CHAPTER 4

# MEASUREMENTS AND RESULTS

## 4.1 Measurement Techniques

In this section, the electrodeposited magnetic Nickel-*n*-type Si and Cobalt/*n*-type Si Schottky barriers are characterized. In the electrical characterization of these diodes, the current-voltage (*I-V*), capacitance-voltage (*C-V*), conductance-voltage (*G-V*) measurements are done. In addition the magnetoresistive properties of these systems will be investigated.

The current-voltage (*I-V*) characteristics were measured using a Keithley 487 Picoammeter/Voltage Source at room temperature and in the dark. Capacitance–voltage characteristics were measured using a HP model 4192A LF impedance analyser at room temperature and in the dark.

### 4.1.1 Current-Voltage Measurement

The schematic representation of the structure of a metal-semiconductor junction which consists of a metal contacting a piece of semiconductor and the sign convention of the applied voltage and current are shown in Figure 4.1, where $x_d$ is the depletion layer width.

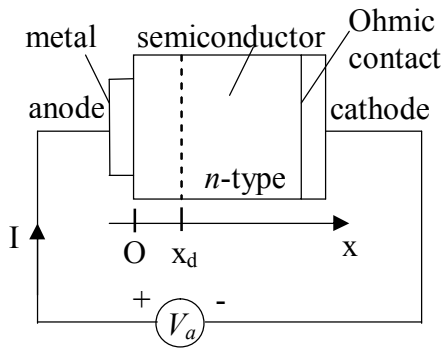



Figure 4.1 Structure and sign convention of a metal-semiconductor junction

#### 4.1.1.1 Forward Characteristics

From $J = J_0$ ($e^{qv/kT}$-1) one can predict the ideal forward and reverse *I-V* Characteristics of a Schottky barrier diode. In the forward direction [3] with $V>3kT/q$,

$$J = A^*T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right)\exp\left[\frac{q(\Delta\Phi + V)}{kT}\right] \tag{4.1}$$

where $\Phi_{b0}$ is the zero- field asymtetic barrier height. A* is the effective Richardson constant, and $\Delta\Phi$ is the Schottky barrier lowering. The ideality factor *n* is given by

$$n \equiv \frac{q}{kT}\frac{\partial V}{\partial(\ln J)} \tag{4.2}$$

and $\Phi_{bn}$ is given as

$$\Phi_{bn} = \frac{kT}{q}\ln\left(\frac{A^{**}T^2}{J_S}\right) \tag{4.3}$$

The relation between *J* and *V* is shown in Figure 4.2.

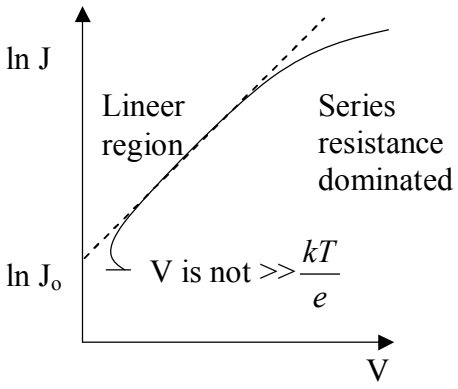



Figure 4.2 *I-V* Characteristics of a forward biased Schottky diode

#### 4.1.1.2 Reverse Characteristics

In the reverse direction the dominant effect is due to the Schottky barrier lowering [3], or

$$J_R \cong J_S \quad (\text{for } V_R > 3kT/q)$$

$$= \text{A**T}^2 \exp\left(-\frac{q\Phi_{bn}}{kT}\right)\exp\left(+\frac{q\sqrt{q\varepsilon/4\pi\varepsilon_S}}{kT}\right) \tag{4.4}$$

If the barrier height $q\Phi_{bn}$ is reasonably smaller than the band gap such that the generation-recombination current in the depletion–layer is small in comparison with the Schottky emission current will increase gradually with the reverse bias as given by Eq. (4.4).

For most of the practical Schottky diodes, however, the dominant reverse current component is the edge leakage current which is caused by the sharp edge around the periphery of the metal plate. This is similar to the junction curvature effect.

### 4.1.2 Capacitance-Voltage Measurement

The barrier height can also be determined by the capacitance measurement. When a small ac voltage is superimposed upon a dc bias, charges of one sign are induced on the metal surface and charges of the opposite sign in the semiconductor. The relationship between $C$ and $V$ is given by [3]

$$C \equiv \frac{\partial Q_{SC}}{\partial v} = \sqrt{\frac{q\varepsilon_S N_D}{2\left(V_{bi} - V - \frac{kT}{q}\right)}} = \frac{\varepsilon_S}{W} \text{ farad/cm}^2 \tag{4.5}$$

$$\Phi_{bn} = V_{bi} + V_n + \frac{kT}{q} - \Delta\Phi \tag{4.6}$$

where $Q_{SC}$ is the space charge per unit area of the semiconductor, $C$ is the depletion layer capacitance per unit area, $\Delta\Phi$ is the Schottky barrier lowering, $N_D$ is the doping

concentration of *n*-type semiconductor, $W$ is the depletion width, $V_i$ is the voltage intercept, and $V_n$ the depth of the Fermi level below the conduction band which can be computed if the doping concentration is known [3].

### 4.1.3 Magnetoresistance Measurements

The magnetoresistance measurements of the metal thin film samples prepared in this study are performed in two configurations using a home made electromagnet as seen in Figure 4.3 and 4.4:

**1.** With the longitudinal magnetoresistance (LMR) geometry in which the magnetic field is applied parallel to the current direction in thin film plane, Fig.4.3(a).

**2.** With the transverse magnetoresistance geometry (TMR) in which the magnetic field is applied perpendicular to the current direction in thin film plane Fig.4.3(b)

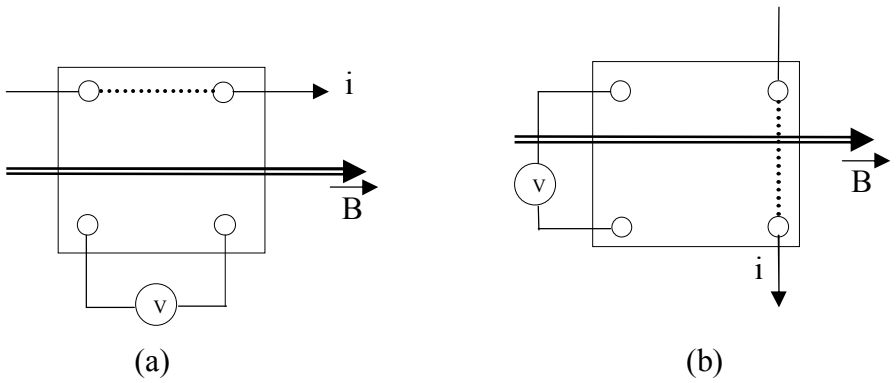
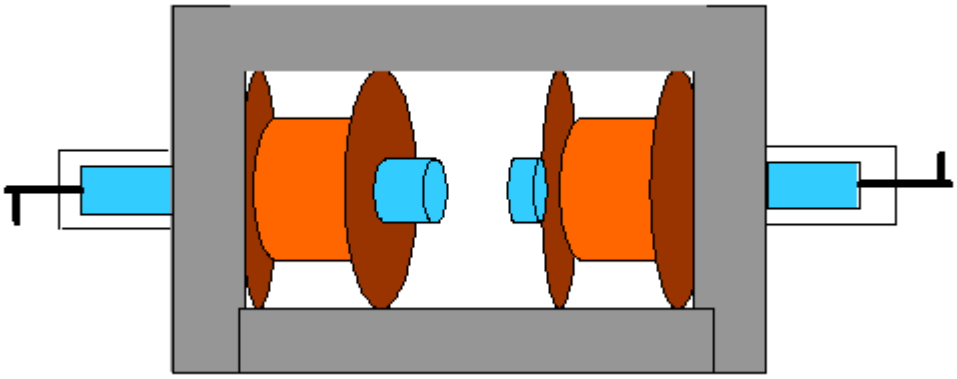
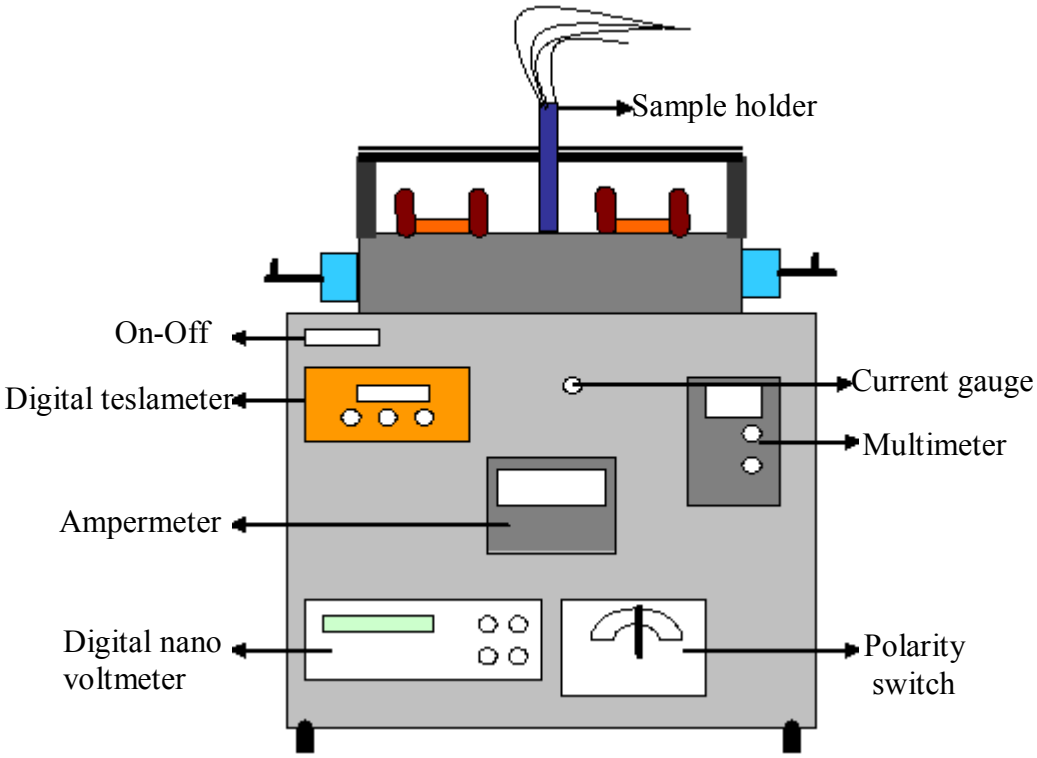



Figure 4.3 The geometrical configurations for (a) LMR and (b) TMR measurements



(a)




(b)

Figure 4.4 A laboratory set-up for magnetoresistance measurements. Illustration of the home made electromagnet (a) top and (b) front view [82].

# CHAPTER 5

# RESULTS AND DISCUSSION

## 5.1 Current-Voltage Measurement Results of the Schottky Diodes

In this study, an (100) oriented *n*-type Si substrate is used which has a thickness of 300-400 μm, a resistivity of 3-4 Ω-cm, and a mobility ($\mu_n$) of 1450 $cm^2$/V-sn and $N_C = 2.08x10^{18}$ $cm^{-3}$ for T = 300 K .

When the equations below are used to calculate the donor density and Fermi level:

$$N_D = 1/q\mu_n\rho \tag{5.1}$$

$$N_D = N_C \exp(-E_F/kT) \tag{5.2}$$

$N_D$ is the donor concentration of *n*-type semiconductor substrate. $N_D$ and $E_F$ are obtained as $N_D = 1.437x10^{15}$ $cm^{-3}$- $1.078x10^{15}$ $cm^{-3}$ and $E_F$=0.205-0.209 *eV* for the *n*-type Si.

The forward current-voltage characteristics of the Schottky structure can be described by the following relation [3,4,10,109-111],

$$I = I_o \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \tag{5.3}$$

where,

$$I_o = AA^*T^2\exp\left(-\frac{q\Phi_b}{kT}\right) \tag{5.4}$$

is the saturation current, $\Phi_b$ is the Schottky barrier height (SBH), $V$ is the definite forward-bias voltage, $A$ is the effective diode area ($A$=7.85 x $10^{-3}$ $cm^2$), $k$ is the Boltzmann constant ($k$= 8.625 x $10^{-5}$ *eV/K*), $T$ is the absolute temperature (T=300 K), $A^*$ is the Richardson constant for *n*-type Si ($A^*$ = 112 $Acm^{-2}K^{-2}$) [3,112,113]. The

ideality factor of Schottky contact from Eq. (5.3) is obtained in the slope of straight line region of the forward-bias logarithmic characteristics of *I-V* through the relation;

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \tag{5.5}$$

where $n$ is a measure of conformity of the diode to pure thermionic emission for an ideal Schottky barrier diode of $n = 1$. However, $n$ has usually a value greater than unity. This value indicates that the effect of the series resistance in the linear region is important. The underlying cause for $n > 1$ can be due to an interfacial layer, barrier height inhomogeneity or image-force lowering which is voltage dependent [3,4,25,26]. Furthermore, the interfacial native oxide layers can inevitably formed by water or vapour adsorbed onto the surface of the semiconductor substrate, [3,4,113] before making barrier diode on the front surface of the *n*-type Si substrate. Fig. 5.1 shows the dark forward and reverse bias *I-V* characteristics of one of the electrodeposited Ni/*n*-Si Schottky contacts respectively. From Eq. (5.4) the barrier height, $\Phi_b$ is given by;

$$\Phi_b = \frac{kT}{q}\ln\left(\frac{A^* A T^2}{I_0}\right) \tag{5.6}$$

Using Eqs (5.5) and (5.6), as explained above, the values of the ideality factor ($n$) and the barrier height ($\Phi_b$) of the Ni/*n*-Si Schottky contacts were found as 1.10 and 0.69 eV, respectively. Moreover, at high currents there is a deviation which has been clearly shown to depend on parameters such as the interfacial layer thickness, the interface states density and series resistance, as one would expected [114,115].

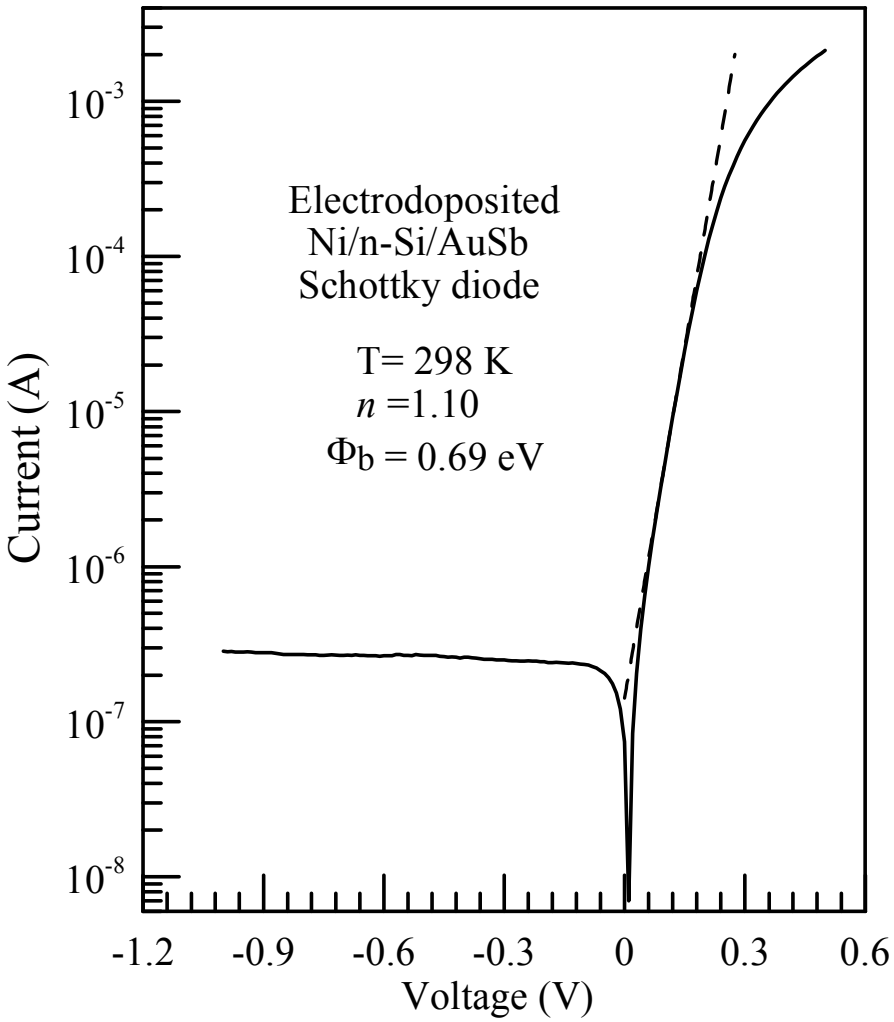



Figure 5.1 The experimental forward and reverse bias current versus voltage characteristics of one of the dots of the electrodeposited Ni/*n*-Si Schottky barrier diodes at the room temperature

21 dots (Schottky contacts) for the Ni/*n*-Si were fabricated on the same *n*-type Si semiconductor substrate by electrodeposition of Ni. Fig. 5.2 shows the dark forward and reverse bias *I-V* characteristics of the electrodeposited Ni/*n*-Si Schottky contacts respectively.

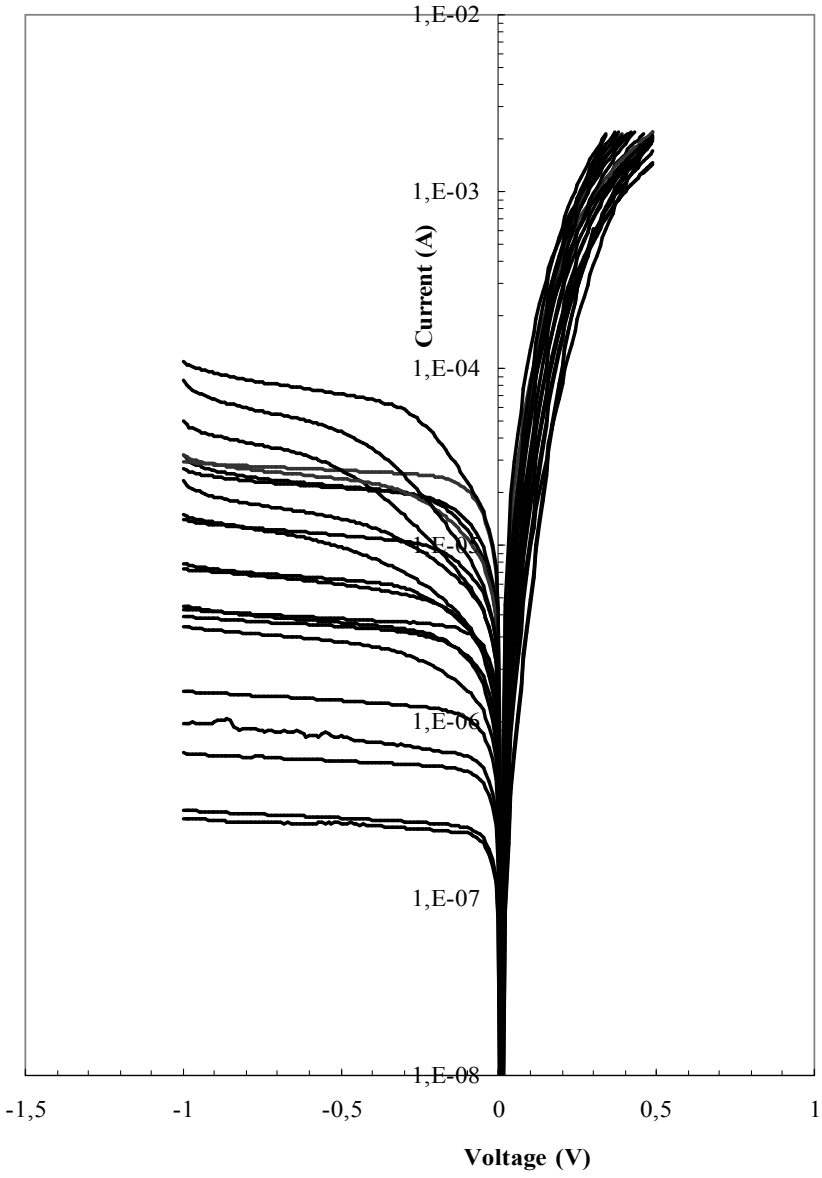



Figure 5.2 Forward and reverse bias current versus voltage characteristics of the electrodeposited Ni/*n*-Si Schottky barrier diodes at the room temperature

According to the thermionic emission theory, the reverse current of an ideal Schottky diode should saturate at the value of the expression in Eq. (5.4). As can be seen, the reverse bias *I-V* characteristics of the device exhibit an good saturation. The barrier height for the electrodeposited Ni/*n*-Si/AuSb SBDs obtained from the forward bias current-voltage characteristics has varied from 0.58 eV to 0.70 eV, and the ideality factor *n* obtained has varied from 1.10 to 1.66.

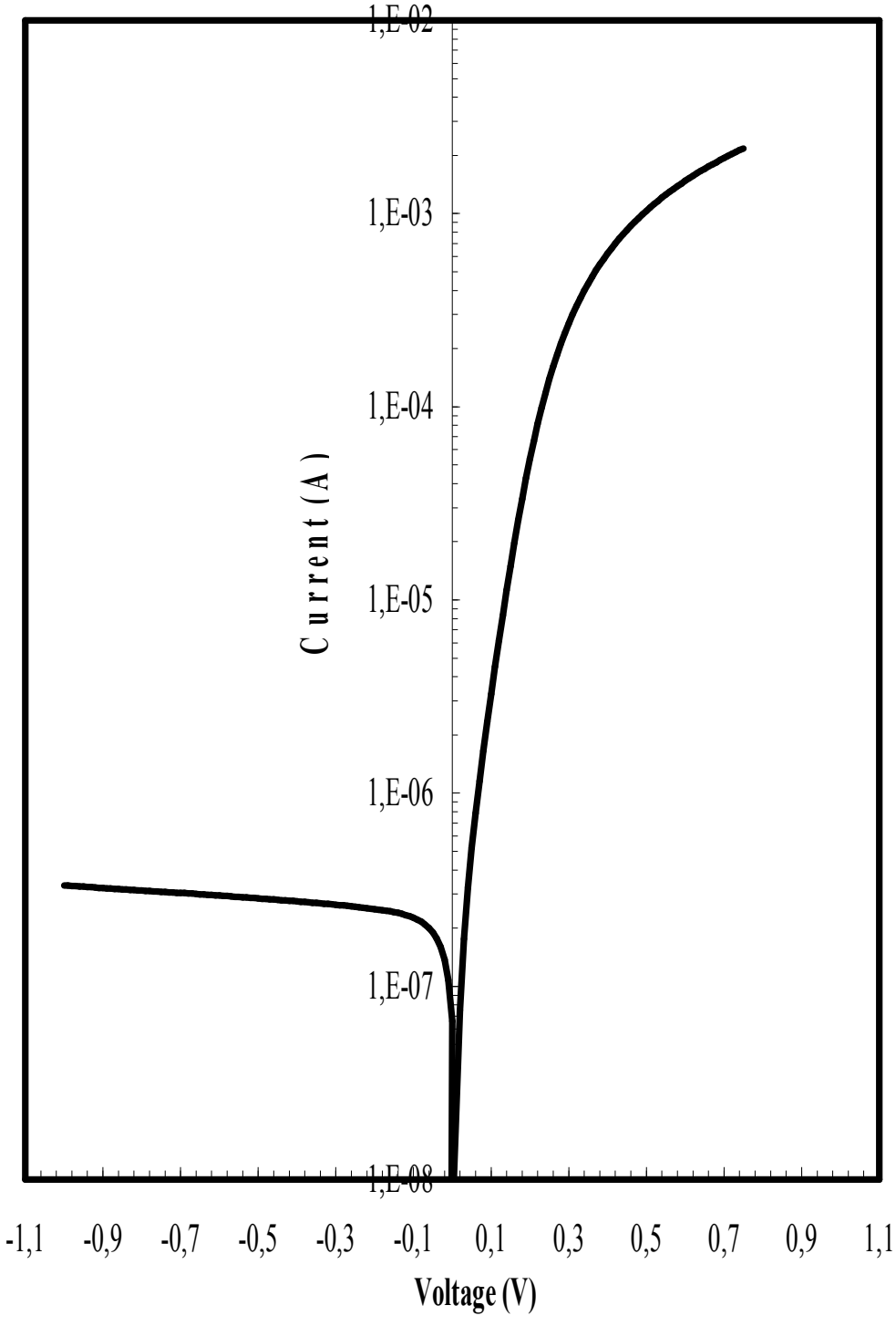



Figure 5.3 The experimental forward and reverse bias current versus voltage characteristics of one of the dots of the electrodeposited Co/*n*-Si Schottky barrier diodes at the room temperature

The ideality factor (*n*)of Co/*n*-Si/AuSb Schottky barrier diode is calculated using Eq. (5.5) from the linear region of the forward-bias *I-V* plots in Fig. 5.3 and is found to be 1.19. The value of the barrier height of the Co/*n*-type Si Schottky barrier diode is found to be 0.70 eV from the y-axis intercepts of the semilog forward bias *I-V* plots with the help of Eq. (5.4). It should be known that $\Phi_b$ is the diode potential barrier that exists at the interface between metal and semiconductor layers.

10 dots (Schottky contacts) for the Co/*n*-Si were fabricated on the same *n*-type Si semiconductor substrate by electrodeposition of Co. The forward bias and reverse bias current-voltage characteristics of the Co/*n*-Si (MS) Schottky structure at 300 K (room temperature) are given in Fig. 5.4.

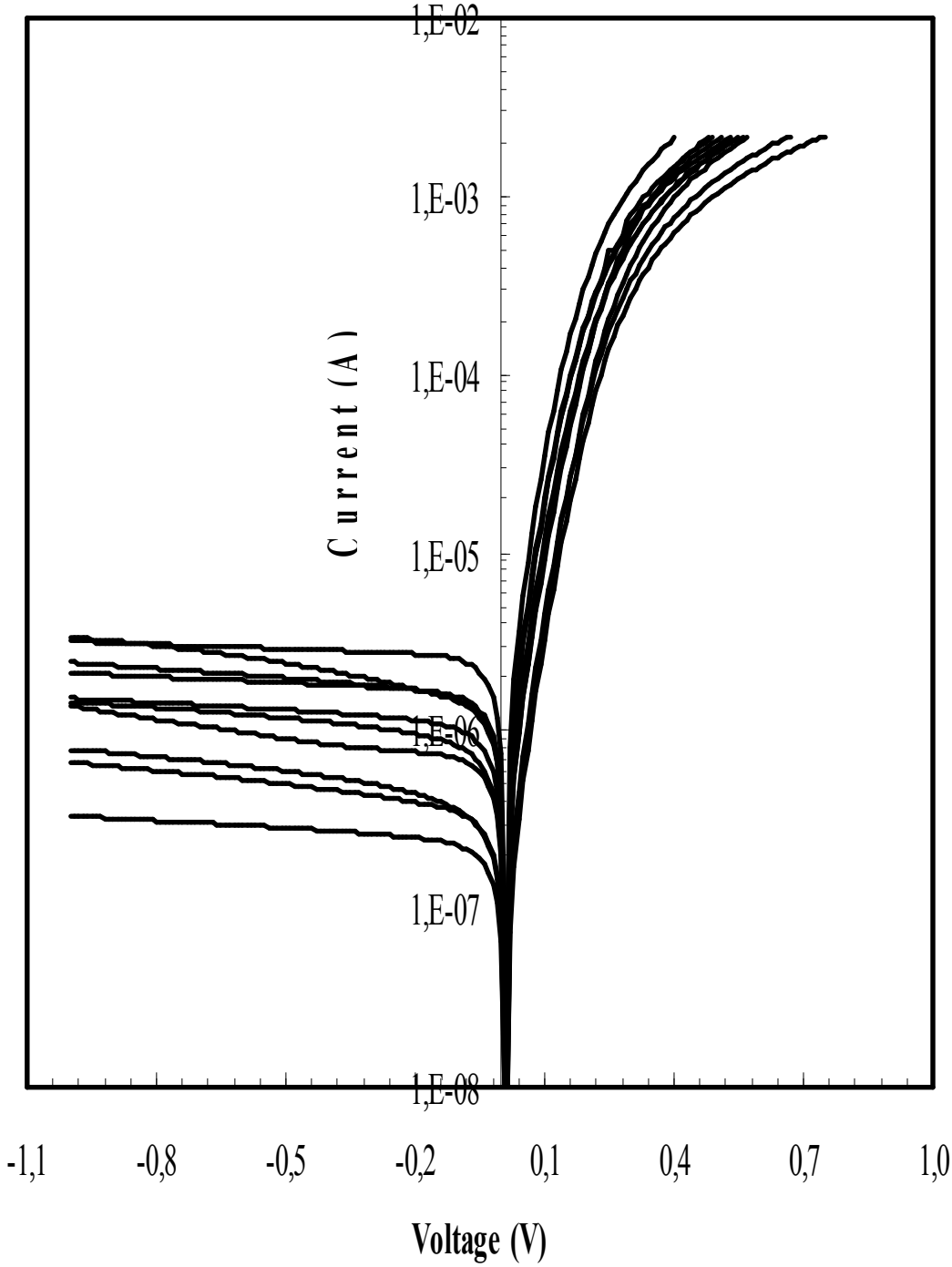



Figure 5.4 The experimental forward and reverse bias current versus voltage characteristics of the 10 electrodeposited Co/*n*-Si Schottky barrier diodes at the room temperature

As can be seen from Fig. 5.4, the Co/*n*-type structure shows the rectifying behaviour and reverse current curve indicates a good saturation. The values of the

barrier height ($\Phi_b$) and the ideality factor ($n$) of the Co/$n$-type Si Schottky contact have varied from 0.63 to 0.70 eV from the extrapolated experimental saturation currents ($I_0$), and ideality factor ($n$) from 1.18 to 1.26 from the slope of the linear region of the semilog-forward bias $I$–$V$ characteristics measurements, respectively.

The calculated values of these parameters for Ni/$n$-type Si Schottky contacts are given in Table 5.1.

Table 5.1 The various parameters of the Ni/*n*-Si structure obtained from *I–V* characteristics at room temperatures

| **Ni/*n*-Si Schottky Contacts** | **İdeality Factor, *n*** | **Barrier height, Φ (eV)** | **Saturation current, $I_0$ *(A)*** |
|---|---|---|---|
| Point 1 | 1.37 | 0.64 | 8.50E-07 |
| Point 2 | 1.58 | 0.60 | 4.77E-06 |
| Point 3 | 1.66 | 0.59 | 9.22E-07 |
| Point 4 | 1.55 | 0.60 | 6.77E-06 |
| Point 5 | 1.54 | 0.60 | 5.70E-06 |
| Point 6 | 1.48 | 0.61 | 1.76E-06 |
| Point 7 | 1.25 | 0.63 | 2.05E-06 |
| Point 8 | 1.29 | 0.62 | 3.02E-06 |
| Point 9 | 1.24 | 0.64 | 1.70E-06 |
| Point 10 | 1.42 | 0.60 | 2.01E-06 |
| Point 11 | 1.18 | 0.66 | 2.01E-06 |
| Point 12 | 1.27 | 0.62 | 1.58E-06 |
| Point 13 | 1.23 | 0.64 | 2.41E-06 |
| Point 14 | 1.12 | 0.68 | 1.49E-07 |
| Point 15 | 1.16 | 0.66 | 2.52E-06 |
| Point 16 | 1.14 | 0.67 | 1.48E-06 |
| Point 17 | 1.10 | 0.69 | 3.66E-06 |
| Point 18 | 1.10 | 0.70 | 1.26E-07 |
| Point 19 | 1.56 | 0.58 | 1.04E-06 |
| Point 20 | 1.20 | 0.63 | 6.22E-07 |
| Point 21 | 1.27 | 0.61 | 4.71E-07 |

When we look at the table 5.1, the ideality factors are obtained between 1.10 and 1.66, the barrier heights are between 0.58 and 0.70 and the saturation current is

obtained betwen $1.26x10^{-7}$ and $6.77x10^{-6}$ . From the ideality factors, it can be said that Ni/*n*-type Si Schottky diode nearly shows the property of an ideal diode.

The calculated values of the Co/*n*-type Si Schottky contacts are given in Table 5.2.

Table 5.2 The various parameters of the Co/*n*-Si structure obtained from *I–V* characteristics at room temperatures

| **Co/*n*-Si Schottky contacts** | **İdeality Factor, *n*** | **Barrier height, Φ (eV)** | **Saturation current, $I_0$ *(A)*** |
|---|---|---|---|
| Point 1 | 1.19 | 0.70 | 1.13E-07 |
| Point 2 | 1.25 | 0.66 | 4.53E-07 |
| Point 3 | 1.25 | 0.65 | 7.54E-07 |
| Point 4 | 1.19 | 0.69 | 1.59E-07 |
| Point 5 | 1.27 | 0.65 | 8.85E-07 |
| Point 6 | 1.24 | 0.67 | 3.86E-07 |
| Point 7 | 1.18 | 0.69 | 1.50E-07 |
| Point 8 | 1.24 | 0.65 | 7.63E-07 |
| Point 9 | 1.26 | 0.63 | 1.50E-06 |
| Point 10 | 1.21 | 0.67 | 3.90E-07 |

As seen in the table 5.2, the obtained values for the ideality factors are between 1.18 and 1.27, for the barrier heights, between 0.63 and 0.70 for saturation current, betwen $1.13x10^{-7}$ and $1.50x10^{-6}$. From the ieality factors, it can be said that Co/*n*-type Si Schottky diode also nearly shows the property of an ideal diode.

## 5.2 Calculation of the Electronic Parameters of Schottky Diodes by the Cheung Method

The series resistance is a very important parameter of Schottky diode. The resistance of the Schottky contact is the total resistance value of the resistors in series and resistance in semiconductor device in the direction of current flow. The Schottky diode parameters as the barrier height $\Phi_b$, the ideality factor $n$ and the series resistance $R_S$ were also obtained using a method developed by Cheung and Cheung [93]. The Cheung's functions can be written as follows:

$$\frac{dV}{d(\ln I)} = IR_S + n\frac{kT}{q} \tag{5.7}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{5.8}$$

and

$$H(I) = IR_S + n\Phi_b \tag{5.9}$$

where $\Phi_b$ is the barrier height extracted from the lower-voltage part of forward $I$–$V$ characteristics. The $dV/d(\ln(I))$ plot is a straight line region where dominates the series resistance. (Fig. 5.5, 5.6) and (Fig. 5.7, 5.8), represent d$V$/dln($I$) and H($I$) vice versa current, respectively, for the Ni/$n$-type Si Schottky structure at room temperature. (Fig. 5.9, 5.10) and (Fig. 5.11, 5.12), represent d$V$/dln($I$) and H($I$) vice versa current, respectively, for the Co/$n$-type Si Schottky structure at room temperature.

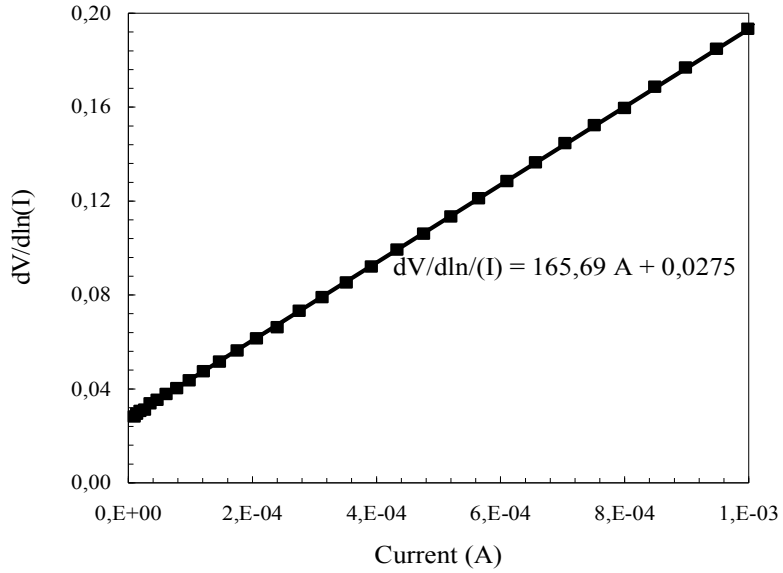



Figure 5.5 An experimental *dV/d*ln*(I)* vs *I* plot obtained from forward bias current-voltage characteristics of the Ni/*n*-type Si Schottky structure at the room temperature

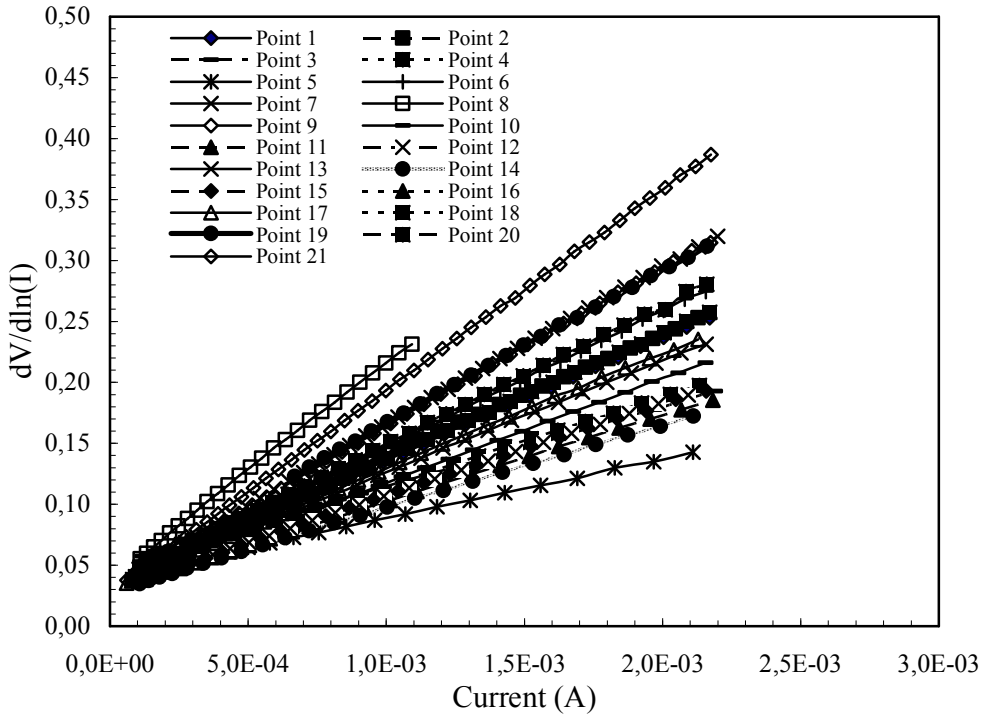



Figure 5.6 The experimental *dV/d*ln*(I)* vs *I* plots obtained from forward bias current-voltage characteristics of the Ni/*n*-type Si Schottky structure at the room temperature

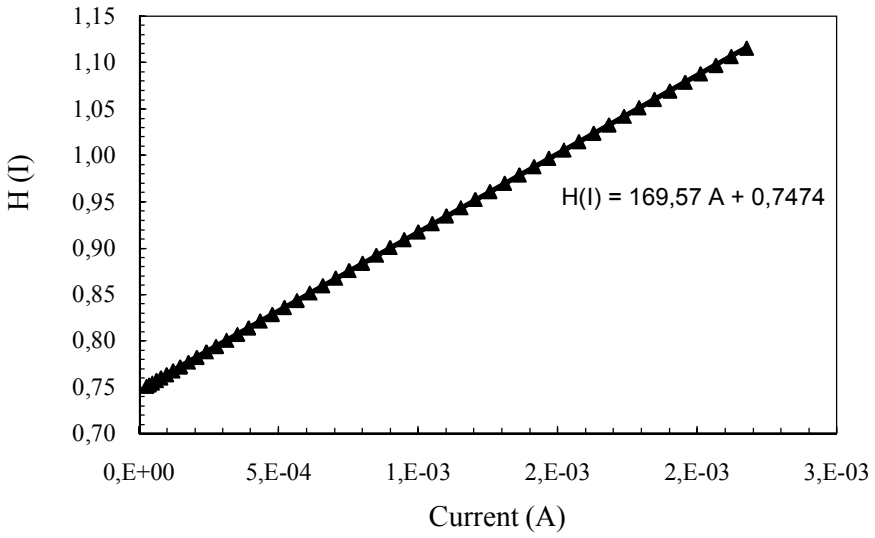



Figure 5.7 An experimental H(*I*) vs *I* plot obtained from forward bias current-voltage characteristics of the Ni/*n*-type Si Schottky structure at the room temperature

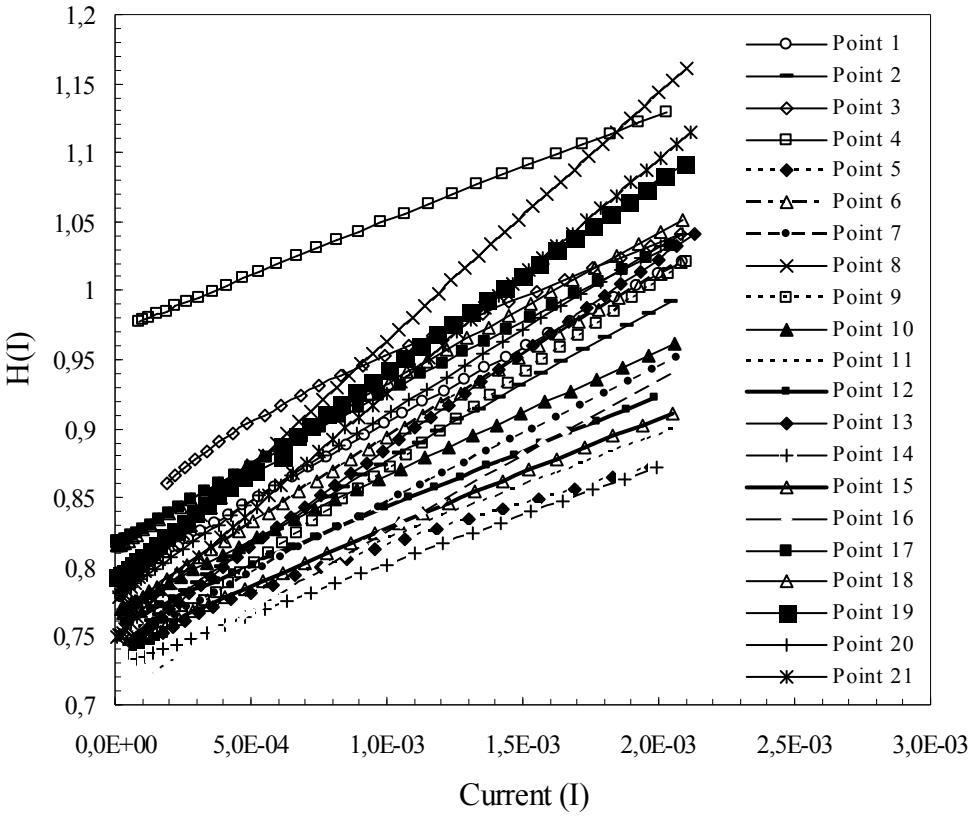



Figure 5.8 The experimental H(*I*) vs *I* plots obtained from forward bias current-voltage characteristics of the Ni/*n*-type Si Schottky structure at the room temperature

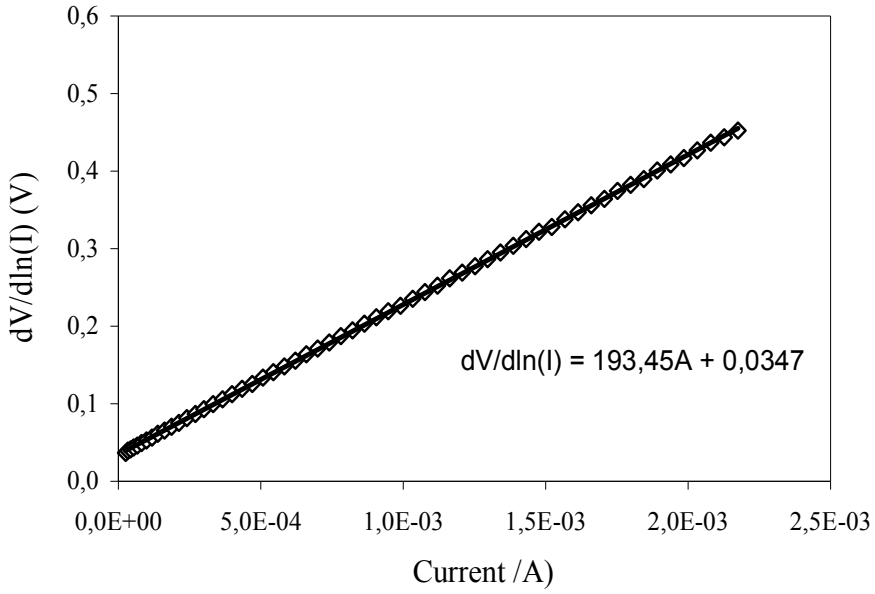



Figure 5.9 An experimental $dV/d\ln(I)$ vs $I$ plot obtained from forward bias current-voltage characteristics of the Co/*n*-type Si Schottky structure at the room temperature

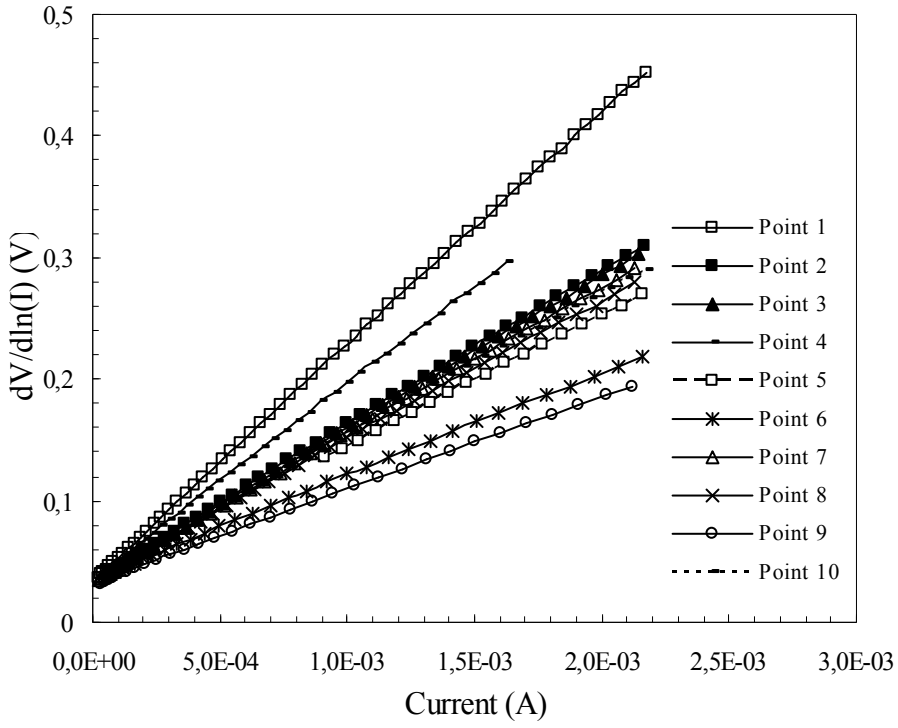



Figure 5.10 The experimental $dV/d\ln(I)$ vs $I$ plots obtained from forward bias current-voltage characteristics of the Co/*n*-type Si Schottky structure at the room temperature

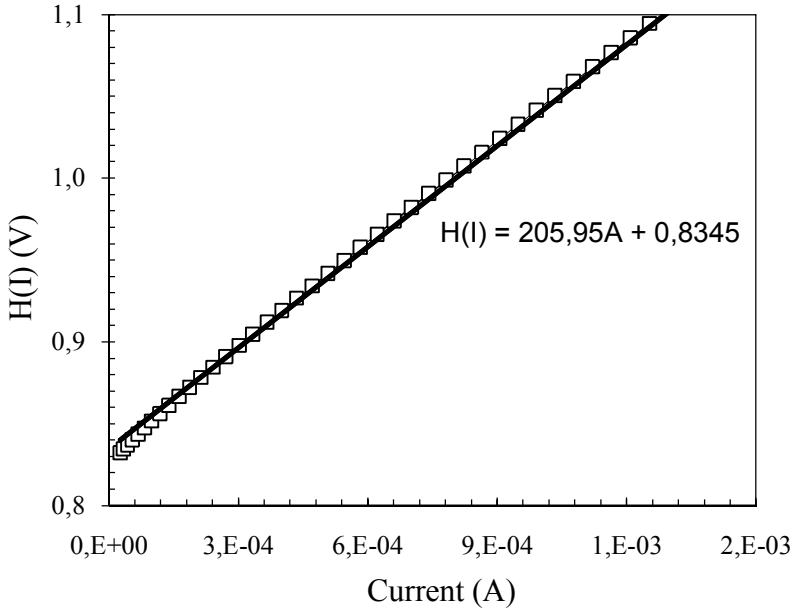



Figure 5.11 An experimental H(*I*) vs *I* plot obtained from forward bias current-voltage characteristics of the Co/*n*-type Si Schottky structure at the room temperature

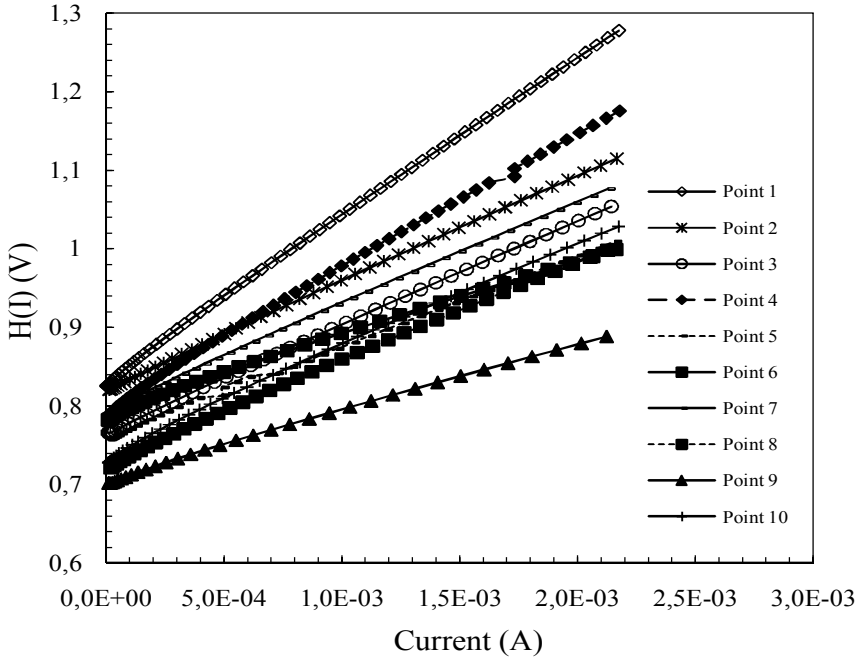



Figure 5.12 The experimental H(*I*) vs *I* plots obtained from forward bias current-voltage characteristics of the Co/*n*-type Si Schottky structure at the room temperature

Equation (5.7) should give a straight line for the data in the downward-curvature region of the forward bias *I-V* characteristics. Thus, the slope and *y*-axis intercept of a plot of $dV/d\ln(I)$ versus *I* plot will give $R_S$ and $nkT/q$, respectively. The plots associated with these functions are given in Figs. 5.5,5.9. The values of ideality factor and series resistance from Eq. (5.7) are found to be 1.06 and 165.69 Ω for 21$^{st}$ dot of the electrodeposited Ni/*n*-Si Schottky barrier diodes and 1.34 and 193.62 Ω for 1$^{st}$ dot of the electrodeposited Co/*n*-Si Schottky barrier diodes. As can be seen in Figs.5.1, 5.3 and Figs.5.5, 5.9 (for $dV/d\ln(I) - I$), it can clearly be seen that there is relatively difference between the values of *n* obtained from the downward curvature regions of forward bias $I - V$ plots and from the linear regions of the same characteristics. The reason of this difference can be attributed to the existence of effects such as the series resistance and the bias dependence of the Schottky contact according to the voltage drop across the interfacial layer and change of the interface states with bias in this concave region of the $I - V$ plot.

In the same way, the barrier height and series resistance values are calculated from Fig.5.7 and 5.11 and using Eq. (5.9) (from plot of $H(I) - I$), the barrier height value and series resistance value are found to be 0.59 eV and 169.57 Ω for 21$^{st}$ dot of the electrodeposited Ni/*n*-Si Schottky barrier diodes and 0.71 and 205.95 Ω for 1$^{st}$ dot of the electrodeposited Co/*n*-Si Schottky barrier diodes. It can be seen obviously that the value of $R_S$ obtained from the $H(I) - I$ plots is closely in agreement with the value obtained from the $dV/d\ln(I) - I$ plot.

That is, the $R_S$ values obtained from the Cheung functions are in agreement with each other due to consistency of Cheung functions.

Table 5.3 The series resistance parameters of the Ni/*n*-Si structure obtained from *I–V* characteristics at room temperatures

| **Ni/*n*-Si Schottky Contacts** | **Series resistant, $R_S$ (Ω) *(dV/dlnI)-I*** | **İdeality Factor, n *dV/dlnI)-I*** | **Series resistant, $R_S$ (Ω) *H(I)-I*** | **Barrier height, Φ (eV) *H(I)-I*** |
|---|---|---|---|---|
| Point 1 | 101.83 | 1.30 | 109.64 | 0.57 |
| Point 2 | 99.053 | 1.62 | 114.43 | 0.47 |
| Point 3 | 64.077 | 1.99 | 82.583 | 0.52 |
| Point 4 | 73.653 | 1.59 | 85.05 | 0.48 |
| Point 5 | 48.312 | 1.56 | 59.8 | 0.49 |
| Point 6 | 113.82 | 1.23 | 119.72 | 0.52 |
| Point 7 | 94.325 | 1.18 | 98.85 | 0.59 |
| Point 8 | 175.5 | 1.18 | 181.01 | 0.60 |
| Point 9 | 128.13 | 1.58 | 137.12 | 0.58 |
| Point 10 | 86.55 | 1.18 | 90.478 | 0.54 |
| Point 11 | 72.155 | 1.14 | 75.026 | 0.63 |
| Point 12 | 76.813 | 1.16 | 80.232 | 0.59 |
| Point 13 | 132.1 | 1.24 | 139.41 | 0.60 |
| Point 14 | 97.212 | 1.20 | 102.57 | 0.73 |
| Point 15 | 68.486 | 1.10 | 69.918 | 0.62 |
| Point 16 | 76.901 | 1.14 | 79.727 | 0.65 |
| Point 17 | 104.64 | 1.23 | 111.36 | 0.64 |
| Point 18 | 105.4 | 1.19 | 110.68 | 0.74 |
| Point 19 | 125.97 | 1.57 | 136.78 | 0.51 |
| Point 20 | 116.11 | 1.23 | 123.1 | 0.65 |
| Point 21 | 165.69 | 1.06 | 169.57 | 0.59 |

When looked at the Table 5.3, ideality factors are obtained between 1.06 and 1.99, barrier heights between 0.47 and 0.74 and series resistances are betwen 48.312 and 175.5 from the (*dV/d*ln*I)-I* graphs and between 59.8 and 181.01 from *H(I)-I*.

Table 5.4 The series resistance parameters of the Co/*n*-Si structure obtained from *I–V* characteristics at room temperatures

| **Co/*n*-Si Schottky Contacts** | **Series resistant, $R_S$ (Ω) *(dV/dlnI)-I*** | **İdeality Factor, n *dV/dlnI)-I*** | **Series resistant, $R_S$ (Ω) *H(I)-I*** | **Barrier height, Φ (eV) *H(I)-I*** |
|---|---|---|---|---|
| Point 1 | 193.62 | 1.34 | 205.95 | 0.71 |
| Point 2 | 128.69 | 1.28 | 136.57 | 0.66 |
| Point 3 | 127.34 | 1.21 | 135.38 | 0.61 |
| Point 4 | 160.44 | 1.4 | 174.82 | 0.67 |
| Point 5 | 108.23 | 1.4 | 115.04 | 0.60 |
| Point 6 | 85.475 | 1.36 | 99.37 | 0.64 |
| Point 7 | 122.43 | 1.25 | 135.08 | 0.67 |
| Point 8 | 116.39 | 1.28 | 130.56 | 0.59 |
| Point 9 | 77.274 | 1.25 | 87.84 | 0.56 |
| Point 10 | 119.32 | 1.36 | 137.57 | 0.61 |

As seen in the table 5.4, the ideality factors are obtained between 1.21 and 1.40, the barrier heights between 0.56 and 0.71 and the series resistances are betwen 77.274 and 193.62 from the (*dV/d*ln*I)-I* graphs and between 87.84 and 205.95 from *H(I)-I*.

As can be seen from the data, the effective Schottky barrier heights (SBHs) and the ideality factors (*n*) from *I-V* characteristics varied from diode to diode even if they are identically prepared. This finding indicates that the potential barriers at real MS interfaces depend much more strongly on the applied voltage than predicted by the image-force effect for ideal contacts. Therefore, it is common practice to take averages [46-50].

Figure (5.13) and (5.14) show the statistical distribution of BHs from the forward bias *I-V* plots of the Ni/*n*-Si Schottky barrier diodes (21 dots) and Co/*n*-Si Schottky barrier diodes (10 dots) respectively.

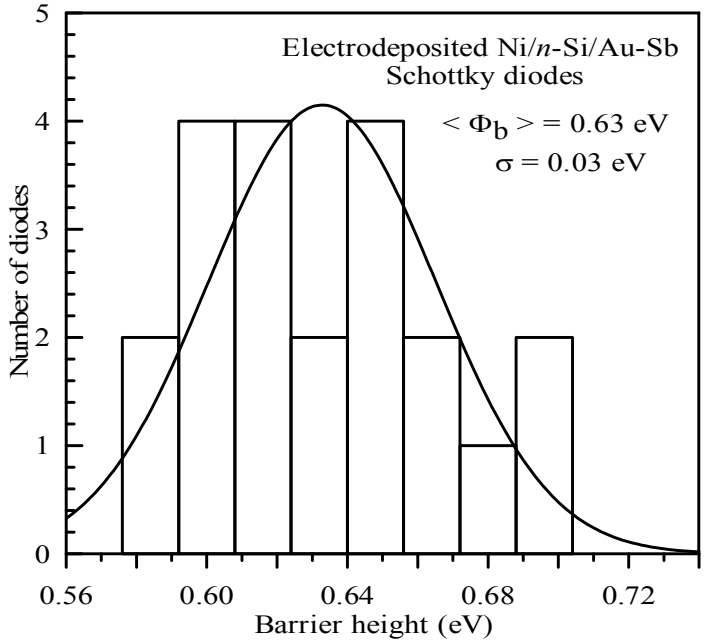



Figure 5.13 Gaussian distribution of the barrier heights from the forward bias *I-V* characteristics of the Ni/*n*-type Si Schottky barrier diodes at the room temperature. The Gaussian fits yields $\overline{\Phi}_b = 0.63$ eV and $\sigma = 30$ meV for the barrier heights

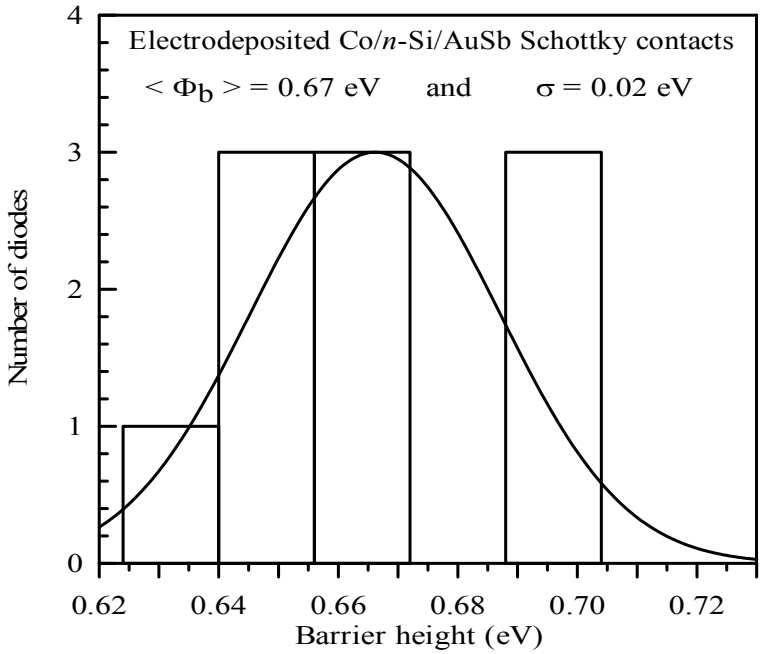



Figure 5.14 Gaussian distribution of the barrier heights from the forward bias *I-V* characteristics of the 10 electrodeposited Co/*n*-type Si Schottky barrier diodes at the room temperature. The Gaussian fits yields $\overline{\Phi}_b = 0.67$ eV and $\sigma = 0.02$ eV for the barrier heights

The experimental distributions of the effective BHs were fitted by the Gaussian function. The statistical analysis yielded a mean BH value of 0.63 eV with a standard deviation of 30 meV for the Ni/*n*-Si SBDs. The statistical analysis yielded a mean BH value of 0.67 eV with a standard deviation of 20 meV for the Co/*n*-Si SBDs.

In the distribution of the ideality factors from the forward bias *I-V* characteristics of the Ni/*n*-type Si and Co/*n*-Si Schottky contacts (Figs. 5.15 and 5.16), the Gaussian fit yields a mean ideality factor value of 1.33 with a standard deviation of 0.18 and 1.23 with a standard deviation of 0.03 respectively.

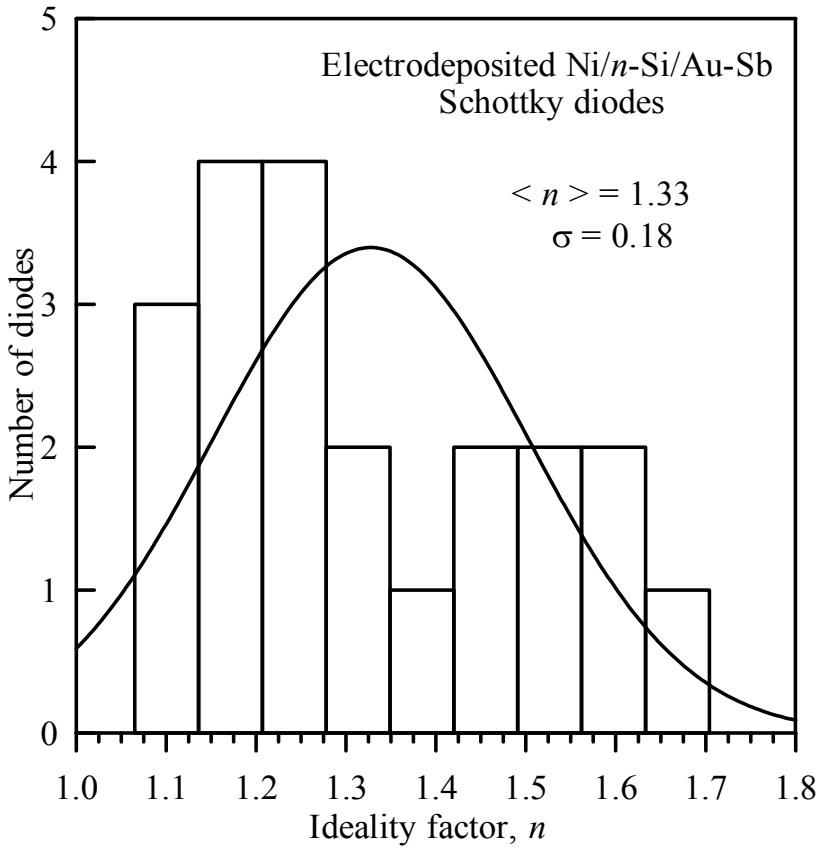



Figure 5.15 Gaussian distribution of ideality factors from the forward bias *I-V* characteristics of the electrodeposited Ni/*n*-type Si Schottky barrier diodes at the room temperature. $\overline{n} = 1.33$ eV and $\sigma = 0.18$ for the ideality factors

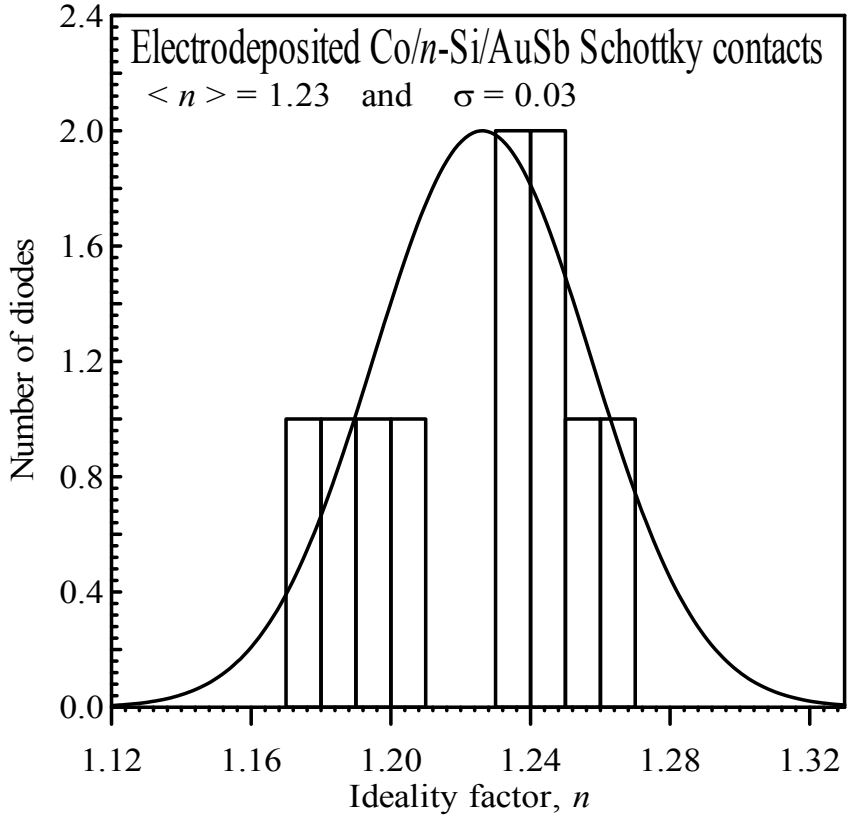



Figure 5.16 Gaussian distribution of the ideality factors from the forward bias *I-V* characteristics of the electrodeposited Co/*n*-type Si Schottky barrier diodes at the room temperature. $\overline{n} = 1.23$ eV and $\sigma = 0.03$ for the ideality factors

When we consider the image force lowering of the Schottky barrier, we obtain an ideality factor value of 1.008 for the electrodeposited Ni/*n*-Si SBD with the mean effective BH of 0.63 eV. The free carrier concentration of the used Si is approximately $1.25 \times 10^{15}$ $cm^{-3}$ at room temperature. Thus, the inhomogeneities may play an important role and have to be considered in the evaluation of experimental *I-V* characteristics.

## 5.3 Capacitance-Voltage (*C-V*) Measurements of the Samples Under the Constant Frequency

The capacitance-voltage *(C-V)* characteristic is one of the fundamental properties of the Schottky diode. The capacitance-voltage *(C-V)* measurements of the samples are taken between -0.95 V and 1 V at $f$ = 1MHz. The *C-V* graphs at $f$ = 1MHz of the samples are given in Figures 5.17-5.20 and the diffusion potentials obtained from these graphs are given in Table 5.5 and 5.6.

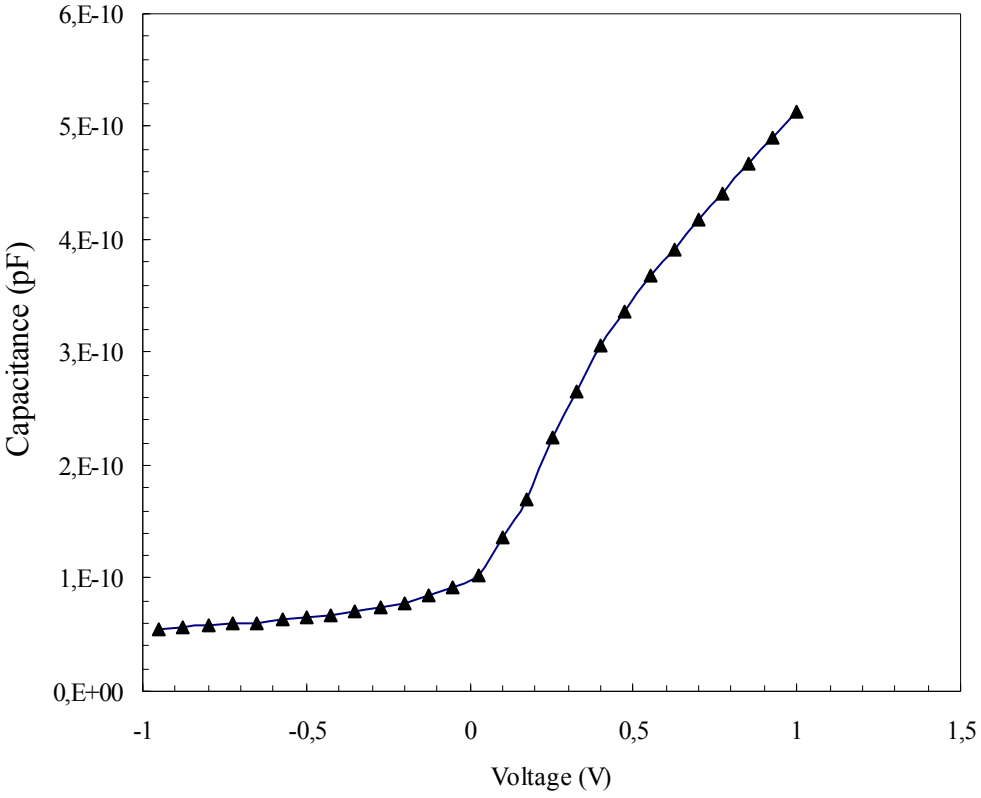
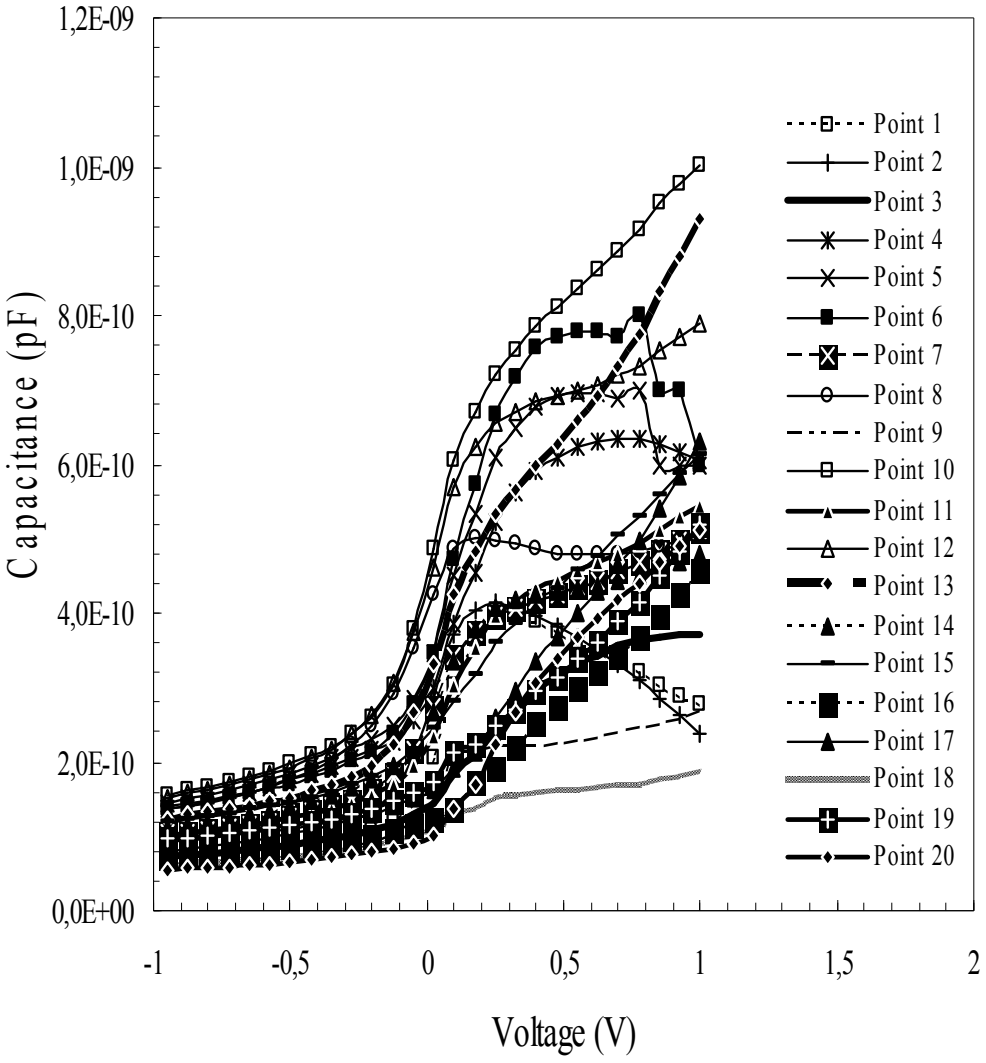



Figure 5.17 The experimental *C-V* characteristics of one of the dots of the electrodeposited Ni/*n*-Si Schottky barrier diodes

Fig




*C-V* characteristics of the electrodeposited Ni/*n*-Si Schottky barrier diodes

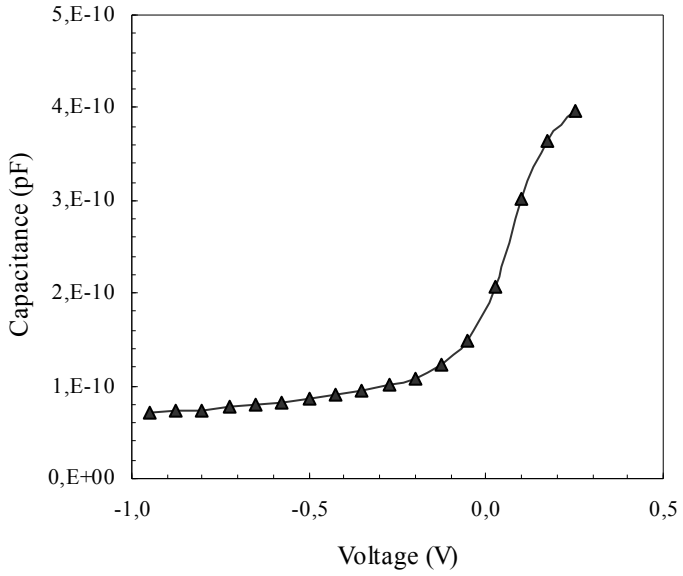



Figure 5.19 Experimental Capacitance-Voltage (*C-V)* characteristics of one of the dots of the electrodeposited Co/*n*-Si Schottky barrier diodes

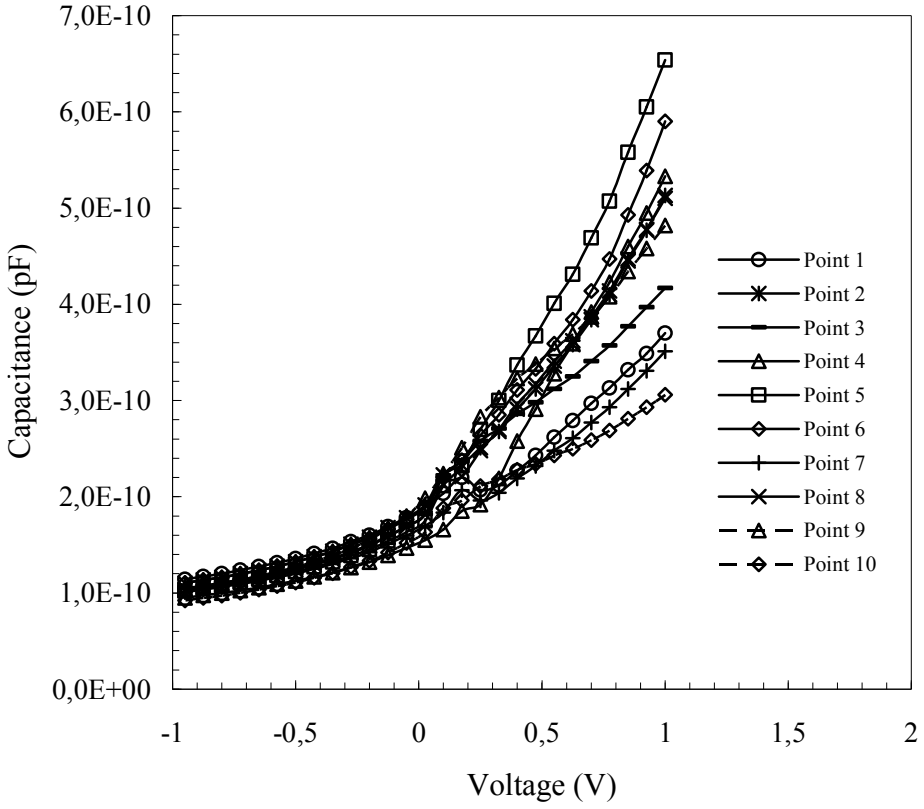



Figure 5.20 The experimental *C-V* characteristics of the electrodeposited Co/*n*-Si Schottky barrier diodes

As can be seen from Figs. 5.17-5.20, the *C-V* characteristics in the SBDs show an increase of capacitance with the increasing forward voltage. If measurements are carried out at sufficiently high frequencies, the charge at the interface states cannot follow an ac signal. This will occur when the time constant is too long to permit the charge to move in and out of the states in response to an applied signal. Thus, in the Schottky barrier diode, the depletion layer capacitance can be expressed as [3,4]

$$\frac{1}{C^2} = \frac{2(V_d + V)}{q\varepsilon_S A^2 N_D} \tag{5.10}$$

The slope of the reverse bias $C^{-2}$-$V$ plot can also be given by

$$\frac{d(C^{-2})}{dV} = \frac{2}{N_D A^2 q\varepsilon_S} \tag{5.11}$$

When equation (5.10) is differentiated according to $V$ and solved due to $N_D$ for a diode,

$$N_D = 2/q\varepsilon_0\varepsilon_S A^2 \frac{dV}{d(C^{-2})} \tag{5.12}$$

is obtained.

$\frac{dV}{d(C^{-2})}$ in this equation, is obtained from the slope of the line in $C^{-2}$-$V$ graph, as shown in the Eq. (5.11), then donor density is obtained for each diode. From the equation (5.1) donor density was calculated as between $N_D$ = 1.437x10$^{15}$ cm$^{-3}$-1.078x10$^{15}$ cm$^{-3}$. From the equation (5.12) donor density of Ni/*n*-Si Schottky barrier diode calculated as between $N_D$ = 8.44x10$^{14}$ cm$^{-3}$- 3.77x10$^{15}$ cm$^{-3}$ and for Co/*n*-Si Schottky barrier diode it is calculated as between $N_D$ = 1.22x10$^{15}$ cm$^{-3}$- 3.50x10$^{15}$ cm$^{-3}$.

$$C_2 = \frac{1}{n_{CV}} = \frac{2}{N_D A^2 q\varepsilon_S [d(C^{-2})/dV]} \tag{5.13}$$

where $C_2$ is the inverse of the ideality factor $n_{CV}$, $A$ is the area of the Schottky barrier diode, $V_d$ is the diffusion potential at zero bias and is determined from the

extrapolation of the linear $C^{-2}$-$V$ plot to the $V$ axis, that is, it is the intercept voltage $V_0$; $\varepsilon_s$ is the dielectric constant of the semiconductor (=11.8 for Si) [3,4], $\varepsilon_0$ is the dielectric constant of vacuum (8.85x10$^{-14}$ F/cm), $q$ is the electronic charge, and $N_D$ is the doping concentration. The plots of $C^{-2}$-$V$ as a function of reverse bias voltage are linear that indicates the formation of SDs [40]. The diffusion potential or built-in potential is usually measured by extrapolating $1/C^2$-$V$ plot to the $V$-axis. The barrier height $\Phi_{CV}$ from the $C$-$V$ measurement is defined by

$$\Phi_{CV} = V_d + \frac{kT}{q} + kT\ln\left(\frac{N_C}{N_D}\right) - \Delta\Phi_b \tag{5.14}$$

$$= V_{d0} + E_F - \Delta\Phi_b, \tag{5.15}$$

where $\Delta\Phi_b$ is the image force correction and $E_F$ is the Fermi energy measured from the conduction band edge in the neutral region of $n$-Si and can be calculated knowing the carrier concentration. Figs. 5.21-5.24 show the reverse bias $C^{-2}$-$V$ (1.0 MHz) characteristics of the Ni/$n$-Si and Co/$n$-Si Schottky barrier diode. By applying the slope of the $C^{-2}$-$V$ plot shown in Fig. 5.21 and 5.22 to Eq. (5.13), the values of $1/C_2$=$n$=1.47, and the doping concentration $N_D$ = 1.25x10$^{15}$ cm$^{-3}$ for Ni/$n$-Si Schottky barrier diode and $n$ = 1.02 and $N_D$ = 1.25x10$^{15}$ cm$^{-3}$ for Co/$n$-Si Schottky barrier diode are obtained. According to Eq. 5.15 the measured barrier height $\Phi_{CV}$ is 0.80 eV for the Ni/$n$-Si SBD and $\Phi_{CV}$ is 0.76 eV for the Co/$n$-Si SBD. As has been seen, the $C^{-2}$-$V$ curve gives the $\Phi_b^{CV}$ value higher than those derived from $I$-$V$ measurements as expected. Because barrier heights deduced from two techniques are not forever the same. The reason for the discrepancy between the measured $I$-$V$ and $C$-$V$ Schottky barrier height (SBH) is clear. The difference between barrier heights obtained from $I$-$V$ and $C$-$V$ measurements is mainly due to inhomogeneities.

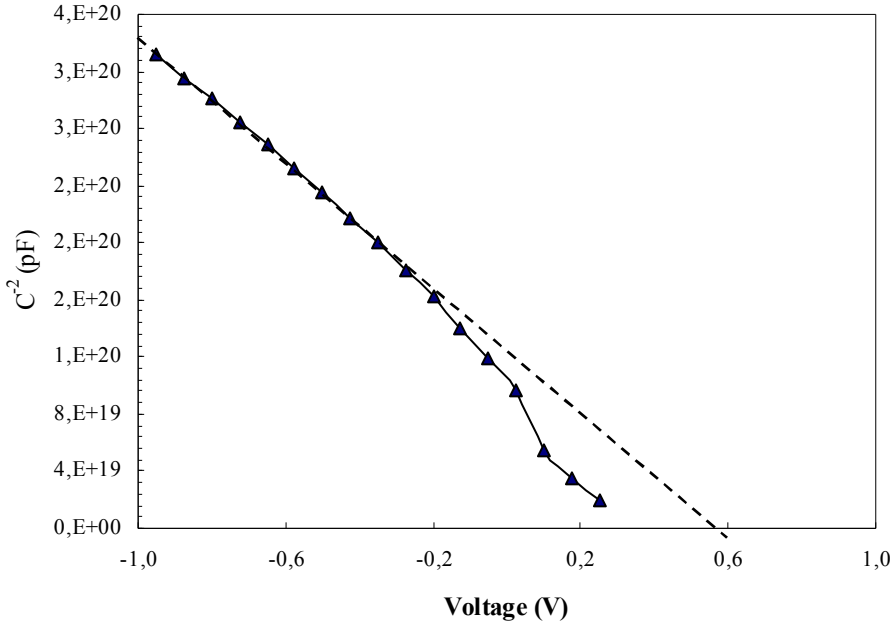



Figure 5.21 The experimental $C^{-2}$-$V$ characteristics of 10$^{th}$ dot of the electrodeposited Ni/*n*-Si Schottky barrier diodes at a frequency of 1.0 MHz and the room temperature

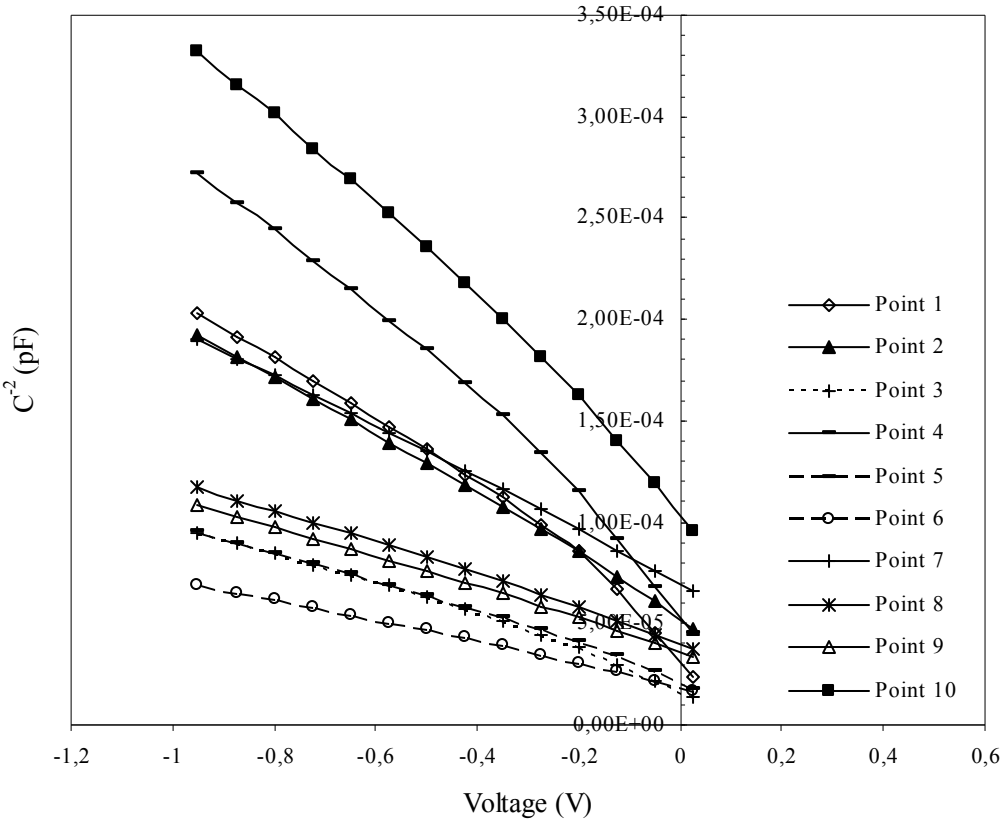



Figure 5.22 The experimental $C^{-2}$-$V$ characteristics of the 10 electrodeposited Ni/*n*-Si Schottky barrier diodes at a frequency of 1.0 MHz and the room temperature

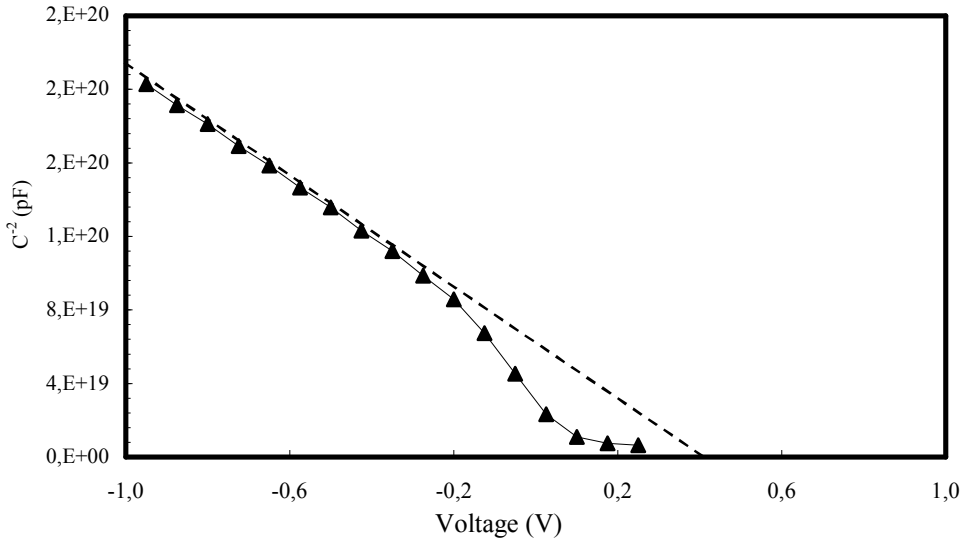



Figure 5.23 The experimental $C^{-2}$-$V$ characteristics of the 1st dot of the electrodeposited Co/*n*-Si Schottky barrier diodes at a frequency of 1.0 MHz and the room temperature

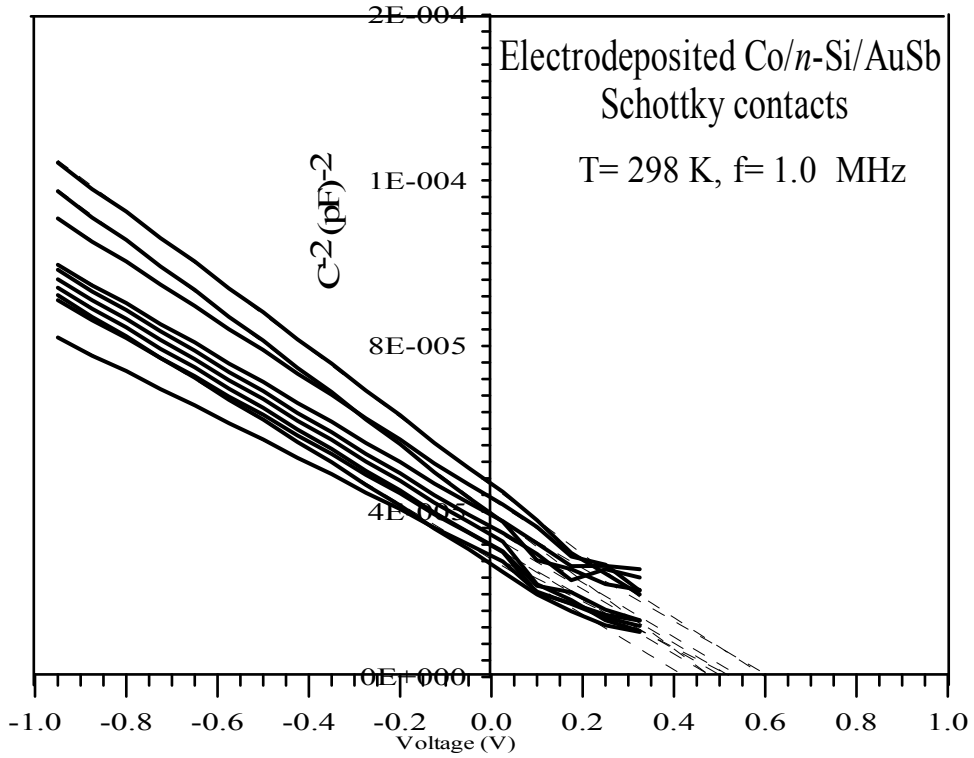



Figure 5.24 The experimental $C^{-2}$-$V$ characteristics of the 10 electrodeposited Co/*n*-Si Schottky barrier diodes at a frequency of 1.0 MHz and the room temperature

Table 5.5 The various parameters of the Ni/*n*-Si structure obtained from *C–V* characteristics at a frequency of 1.0 MHz and room temperature

| **Ni/*n*-Si Schottky Contacts** | **$V_0$ (eV)** | **$V_d$ (eV)** | **$\Phi_b$ (eV)** |
|---|---|---|---|
| Point 1 | 0.42 | 0.445 | 0.64 |
| Point 2 | 0.40 | 0.425 | 0.62 |
| Point 3 | 0.44 | 0.465 | 0.64 |
| Point 4 | 0.43 | 0.455 | 0.66 |
| Point 5 | 0.47 | 0.495 | 0.67 |
| Point 6 | 0.48 | 0.505 | 0.67 |
| Point 7 | 0.59 | 0.615 | 0.80 |
| Point 8 | 0.54 | 0.565 | 0.74 |
| Point 9 | 0.52 | 0.545 | 0.72 |
| Point 10 | 0.51 | 0.535 | 0.80 |

Table 5.6 The various parameters of the Co/*n*-Si structure obtained from *C–V* characteristics at a frequency of 1.0 MHz and room temperature

| **Co/*n*-Si Schottky Contacts** | **$V_0$ (eV)** | **$V_d$ (eV)** | **$\Phi_b$ (eV)** |
|---|---|---|---|
| Point 1 | 0.42 | 0.445 | 0.80 |
| Point 2 | 0.48 | 0.505 | 0.79 |
| Point 3 | 0.50 | 0.525 | 0.71 |
| Point 4 | 0.52 | 0.545 | 0.81 |
| Point 5 | 0.54 | 0.565 | 0.69 |
| Point 6 | 0.56 | 0.585 | 0.76 |
| Point 7 | 0.58 | 0.605 | 0.73 |
| Point 8 | 0.58 | 0.605 | 0.68 |
| Point 9 | 0.59 | 0.615 | 0.79 |
| Point 10 | 0.60 | 0.625 | 0.77 |

As seen from Tables 5.5 and 5.6, the value of $\Phi_{b(C\text{-}V)}$ for the Ni/*n*-Si Schottky contacts ranges from 0.62 to 0.80 eV. The value of $\Phi_{b(C\text{-}V)}$ for the Co/*n*-Si Schottky contacts ranges from 0.68 to 0.81 eV. The barrier heights obtained from *C-V* characteristics are higher than that obtained from *I-V* characteristics.

As can be seen from these tables, the experimental effective BHs obtained from the *C-V* characteristics differ from diode to diode. Therefore, as mentioned above, their averages should be taken [46,48,49,116,117,118].

Figure 5.25 and 5.26 show the statistical distribution of BHs from the reverse bias $C^{-2}$-$V$ plots of the same diodes.

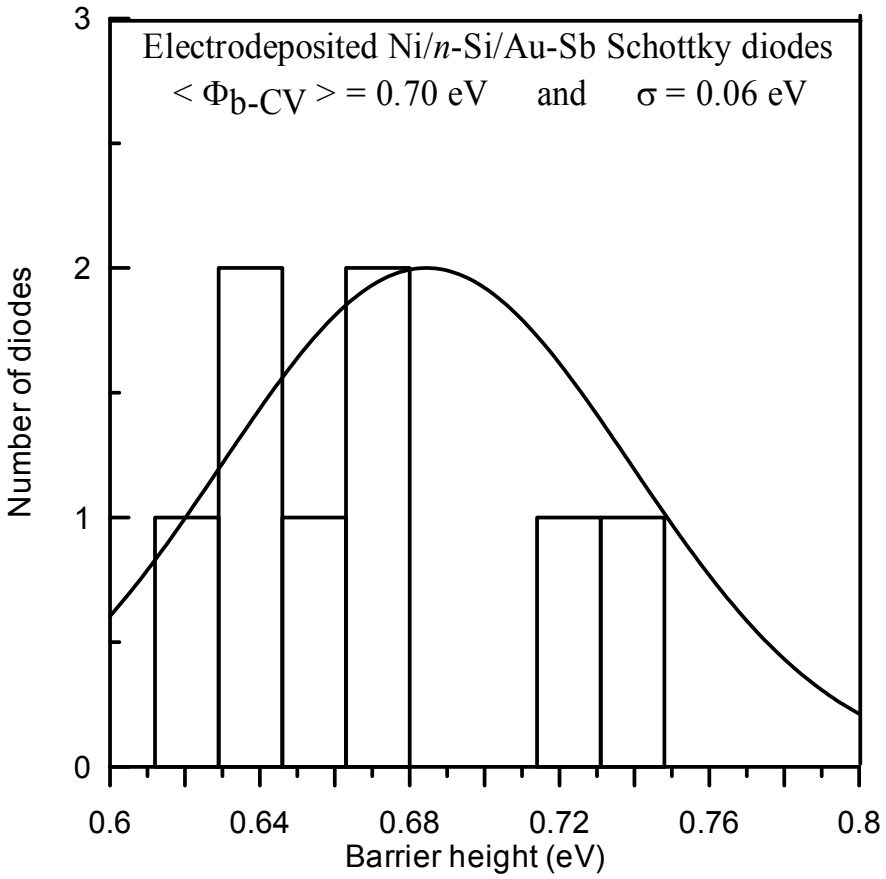



Figure 5.25 Gaussian distribution of the barrier heights from the reverse bias $C^{-2}$-$V$ characteristics of the 10 electrodeposited Ni/*n*-type Si Schottky barrier diodes at the room temperature. $\overline{\Phi}_b = 0.70$ and $\sigma = 0.06$ for the barrier heights

The experimental distributions of the effective BHs were fitted by the Gaussian function. At first, let us consider the *I*-*V* BHs. The statistical analysis yielded a mean BH value of 0.63 for Ni/*n*-Si and 0.67 eV for Co/*n*-Si with a standard deviation of 0.03 and 0.02 eV respectively. In the distribution of the BHs from the reverse bias $C^{-2}$-$V$ characteristics of the Ni/*n*-Si SDs at 1.0 MHz (Fig. 5.25), the statistical analysis yielded a mean BH value of 0.70 eV with a standard deviation of 0.06 eV.

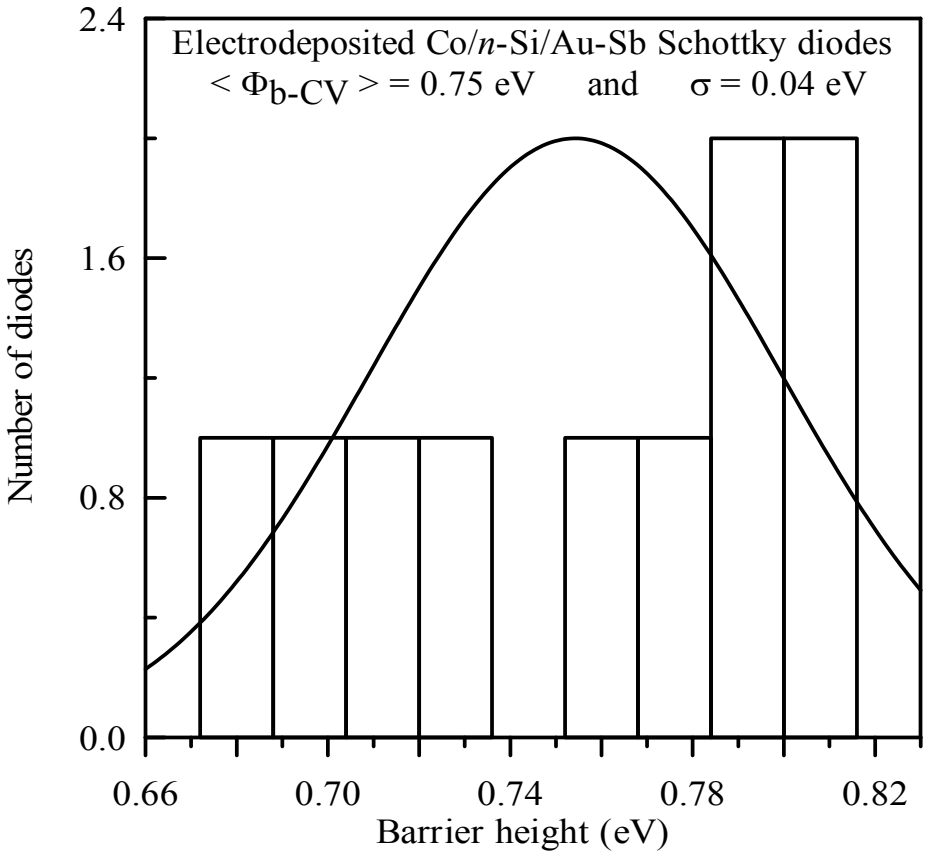



Figure 5.26 Gaussian distribution of the barrier heights from the reverse bias $C^{-2}$-$V$ characteristics of the 10 electrodeposited Co/$n$-type Si Schottky barrier diodes at the room temperature. $\overline{\Phi}_b = 0.75$ and $\sigma = 0.04$ for the barrier heights

In the distribution of the BHs from the reverse bias $C^{-2}$-$V$ characteristics of the Co/$n$-Si SDs at 1.0 MHz (Fig. 5.26), the statistical analysis yielded a mean BH value of 0.75 eV with a standard deviation of 0.04 eV. The difference between the mean SBH values obtained from $C^{-2}$-$V$ and $I$-$V$ (0.07 for the Ni/$n$-Si SDs and 0.08 for the Co/$n$-Si SDs) characteristics is larger than the image-force lowering value of 0.013 eV for this device. The image-force lowering value for the barrier height was determined by using Eq. (3.31) according to reference [3]. Due to the different nature of the $C^{-2}$-$V$ and $I$-$V$ measurement techniques, barrier heights deduced from them are not always the same. When the difference in SBH approaches zero, the potential profiles approach a uniform barrier height.

## 5.4 Conductivity -Voltage (*G-V*) Measurements of the Samples Under the Constant Frequency

Conductivity-voltage (*G-V*) measurements of the samples are taken between -0.95 V and 1 V at $f$ = 1MHz. The *G-V* graphs of the samples are shown in the figures between Figures (5.27) - (5.30). When we look at these figures, there is no change in the conductivity under the reverse bias with voltage. So this shows rectifying property of the diode clearly.

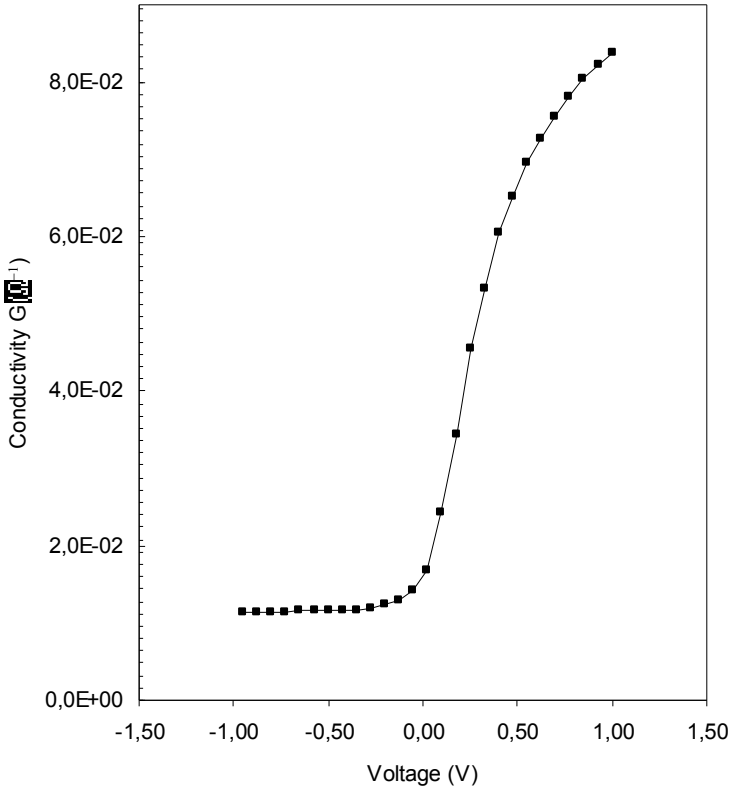



Figure 5.27 Reverse bias and forward bias *G-V* characteristics of the 6$^{th}$ dot of the electrodeposited Ni/*n*-Si Schottky barrier diodes

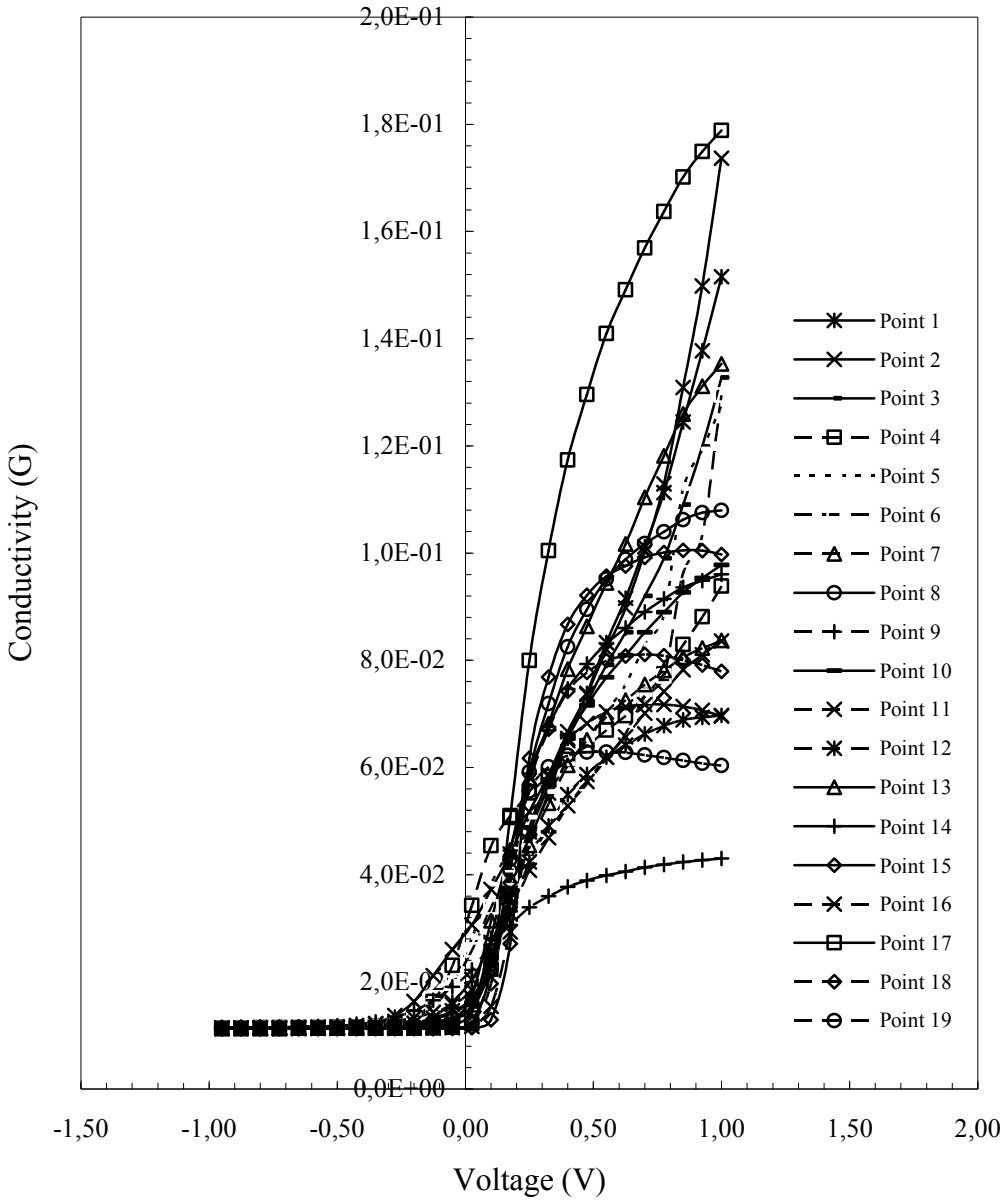



Figure 5.28 Reverse bias and forward bias *G-V* characteristics of the electrodeposited Ni/*n*-Si Schottky barrier diodes

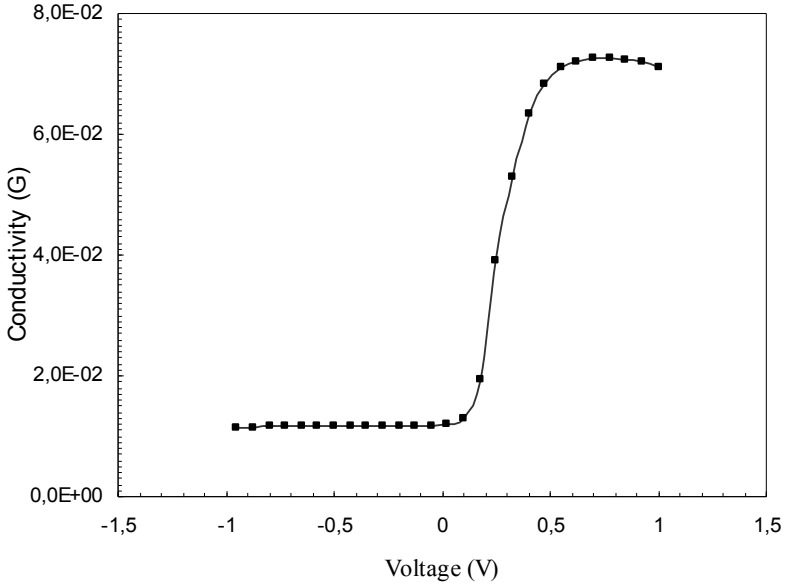



Figure 5.29 Reverse bias and forward bias *G-V* characteristics of the 1st dot of the electrodeposited Co/*n*-Si Schottky barrier diodes

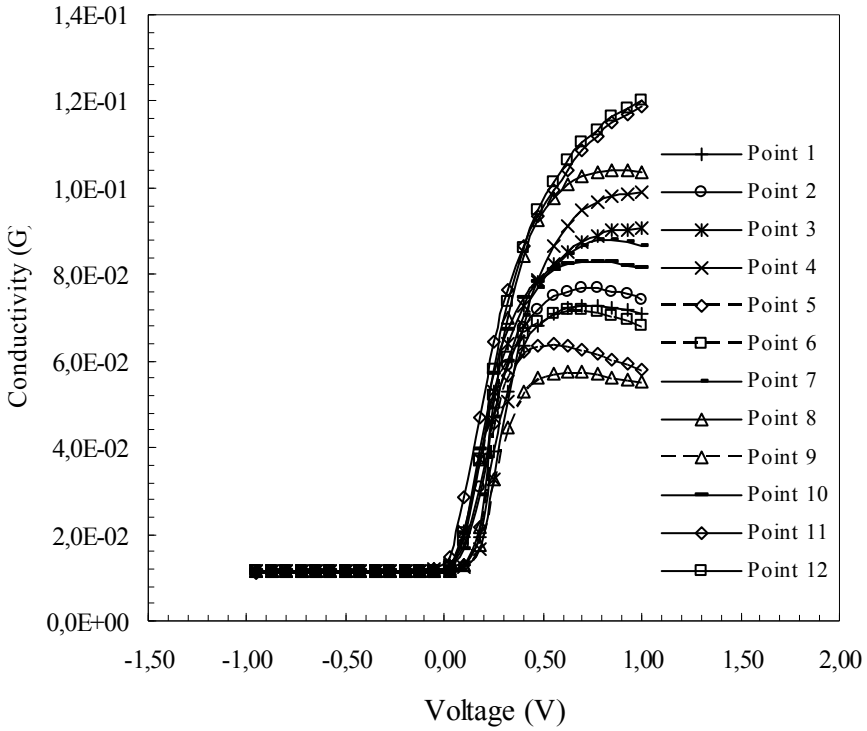



Figure5.30 Reverse bias and forward bias *G-V* characteristics of the electrodeposited Co/*n*-Si Schottky barrier diodes

## 5.5 Magnetoresistance of Co and Ni Films

The anisotropic magnetoresistance (AMR) effect in the electrodeposited pure Co and Ni films is reported to be 4.8% and 3% respectively [119].

The distribution of magnetic domains has a great influence on the resistance of magnetic metal films. When the magnetic domains are aligned parallel by a magnetic field, the resistance of the sample changes to a maximum (positive or negative) value depending on the MR measurement geometry. When the magnetic field is removed, the residual (remanent) magnetisation determines the new resistance state of the sample which usually differs by a small amount from the resistance value of the initial demagnetised state [119]. The systems of Ni and Co are the typical examples of the magnetic metal systems showing this behaviour. If there is a preferred axis within the sample in the demagnetised state, no or little MR effect is expected to be detected when it is measured with a magnetic field applied along that axis. On the other hand, the resistivity measured in a magnetic field applied perpendicular to the preferred axis is quadratic in the field. Thus the anisotropic MR effect is a measure of sample anisotropy or domain magnetisation distribution [120].

The MR measurements on our Co and Ni films are shown in Figures 5.31 and 5.32. The measurements of magnetoresistance were started with the magnetisation vectors initially aligned at $90^{o}$ with respect to the current direction and done in a complete reversal cycle of magnetic field application between ±200Oe. As we observe from Figures 5.31 and 5.32, the magnetoresistance value of Co samples remains stacked in a region of around 4% while the magnetoresistance of Ni reduces to a value close to zero when the magnetic field is brought to the initial zero value. This means that the initial zero magnetic field state of the Co sample is not regained back after we reduce the magnetic field to zero value (Figure 5.31). The resistance of the Co film does not therefore change much in a subsequent MR measurement which is done with a magnetic field applied along the same direction as the previous measurement. We ascribe this behaviour to the remanent magnetisation, i.e., to the magnetic moments pinned mostly at the easy axes along or around the direction of the magnetic field applied in the MR measurement. However the resistance value of the initial zero magnetic field state of Ni film is mostly regained back after we reduce the magnetic field to zero (Figure 5.32) which may be attributed to the magnetic

moments returning to the initial orientations along their initial easy axes. These effects are observed in both LMR and TMR measurement geometries (Figures 5.31 and 5.32).

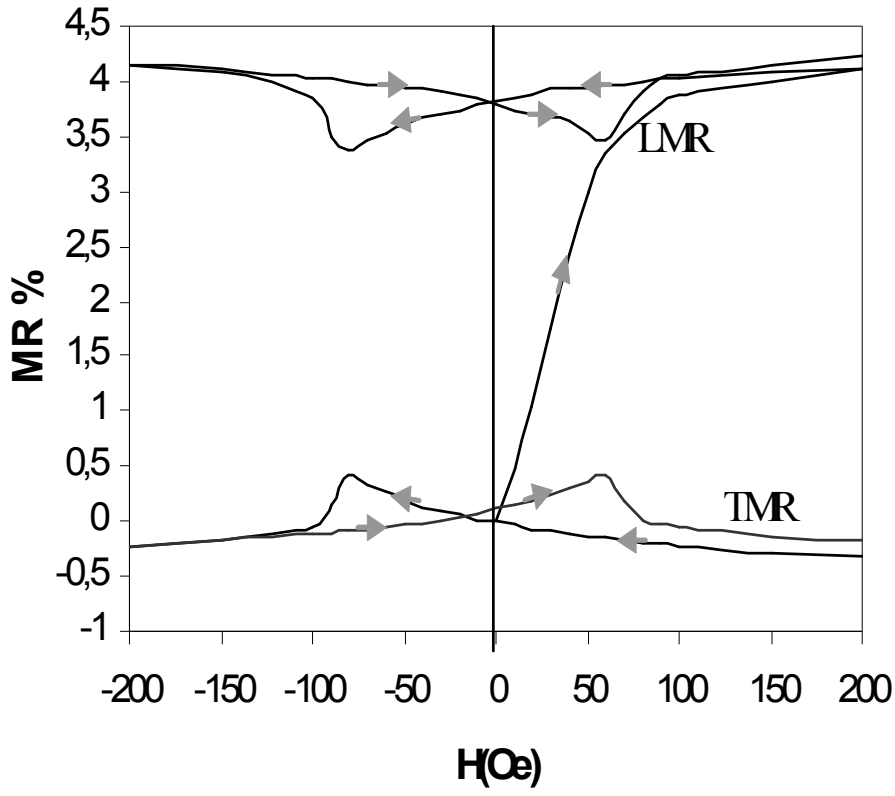



Figure 5.31 AMR of Co films

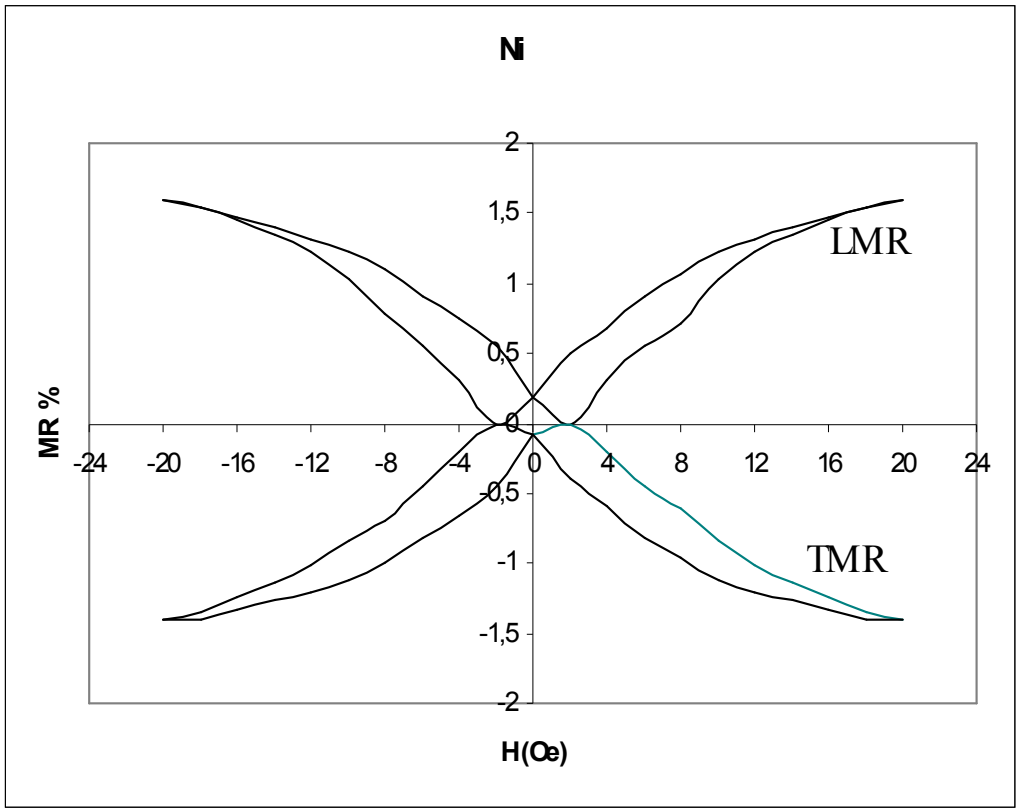



Figure 5.32 AMR of Ni Films

# CHAPTER 6

# CONCLUSIONS

In this study, by using *n*-Si substrate with (100) orientation, 300-400 μm thickness and 3-4 Ω-cm resistivity and phosphorus doped, we obtained Ni/*n*-Si SBDs and Co/*n*-Si SBDs by electrodeposition method. We have investigated electrical properties of Ni/*n*-type Si Schottky structure (MS) and Co/*n*-type Si Schottky structure (MS) using current-voltage (*I-V*) and (*C-V*) and conductance-voltage (*G-V*) measurements at room temperature. The electrodeposition was shown to result in higher SB heights compared with evaporation.

The purpose of this study is to obtain the Schottky diodes with high barrier heights by using electrodeposition method and to confirm the linear relationship between effective BHs and ideality factors experimentally, due to barrier inhomogeneity. For this purpose, ohmic contacts were made dull surface of *n*-Si substrate. Than, Ni and Co films are deposited on the *n*-Si by electrodeposition method. Thus, we obtained a lot of metal-semiconductor (MS) diodes. After taking *I-V, C-V, G-V* measurements for each diode prepared, the graphs of these measurements are drawn and the characteristics are evaluated. In addition the magnetoresistive properties of these systems are investigated.

The ideality factors (*n*) of the substrate are calculated from the slope of the straight line region of the forward bias ln*I-V* characteristics. The barrier heights ($\Phi_{IV}$) are calculated from $I_0$ saturation current density which the linear part of the semi-logarithmic forward bias *I-V* characteristics intercepted the vertical axis. The values of diode parameters such as ideality factor, series resistance ($R_S$) and barrier height were obtained from *I-V* measurements using Cheung's method. In general, the ideality factors obtained from Cheung functions are bigger than those obtained from the slope of the linear part of the forward bias of the *lnI-V* graphs. This is because, the data of the part that inclines downwards that refers to the big values of the

voltage is affected by both series resistance and interface states, but the data of the linear part are affected by only the interface states in the Cheung's method.

Some of the diode parameters obtained by *I-V* graphs are given in a table in the fifth chapter. As seen in the Table 5.1, the ideality factors of the Ni/*n*-Si diodes are changing between 1.10 and 1.66, the barrier heights are changing between 0.58 and 0.70. As can be seen in the Table 5.2, the ideality factors of Co/*n*-Si diodes are between 1.18 and 1.27, the barrier heights are found between 0.63 and 0.70. As seen from the tables, the ideality factors of the *n*-type MS diodes are close to the ideal. The deviation from the ideality is because of the interface states that caused from natural oxide level of semiconductor surfaces in the production process and the barrier height inhomogeneity. In the ideal state, there is no oxide level in the semiconductor surface and no natural oxide level in the process of Schottky contact production [78,121].

As determined by Wittmer and Freeouf, the diodes that have a thin interface level show electrically ideal Schottky diode properties. Their barrier heights are close to the Schottky-Mott value [121]. This case is compatible with the experimental results obtained as we mentioned above, so we can say that these diodes fit to the thermoionic emission model. Song at al. [78] reported that the non-uniformity in the thickness of the oxide level on the semiconductor and inhomogenity in the density of the interface charge and also again inhomogenity in the composition of the interface oxide level can cause to the inhomogenic property of the semiconductor surface, and thus to the barrier height inhomogeneity [78].

The ideality factors and barrier heights are calculated from *C-V* characteristics. Carrier density and diffusion potential at high frequency (1MHz) are obtained from $C^{-2}$-*V* curves. As seen in the table 5.5, the barrier heights of the Ni/*n*-Si diodes are changing between 0.62 and 0.80 eV, the diffusion potentials ($V_D$) are changing between 0.425 and 0.615, the carrier densities ($N_D$) between $8.44 \times 10^{14}$ $cm^{-3}$ and $3.77 \times 10^{15}$ $cm^{-3}$. As seen in the Table 5.6, the barrier heights of Co/*n*-Si diodes are found between 0.68 and 0.81, the diffusion potentials ($V_D$) are changing between 0.445 and 0.625, the carrier densities ($N_D$) = $1.22 \times 10^{15}$ $cm^{-3}$ and $3.50 \times 10^{15}$ $cm^{-3}$.

As well-known it is very difficult to obtain the Schottky diodes with the wanted barrier height and low ideality factor. Because metal and semiconductor interface is sensitive to the preparing process of the surface. The Schottky barrier heights and the ideality factors have varied from diode to diode. Therefore, it is common practice to take averages [46-50]. In our statistical analysis for the Ni/*n*-Si SBDs a mean BH value of 0.63 eV with a standard deviation of 30 meV, a mean ideality factor value of 1.33 with a standard deviation of 0.18 are found. In addition, the statistical analysis yields the mean effective SBH 0.70±0.06 eV for these devices from the *C-V* characteristics. The Gaussian fits of the experimental BH distributions of the Co/*n*-Si SBDs obtained from the *I-V* and $C^{-2}$-*V* characteristics have yielded e mean BH values of 0.67 and 0.75 eV, respectively. The statistical analysis yields the mean effective SBH = 0.67±0.02 eV and the mean ideality factor =1.23±0.03 for these devices from the *I-V* characteristics. In addition, the statistical analysis yields the mean effective SBH 0.75±0.04 eV for these devices from the *C-V* characteristics. It was shown that high quality barriers are obtained using Si with low resistivity, and with very low reversed leakage, and therefore, this study opens up the way for the investigation of electronic effect on Si and consequently for the exploitation of all the benefits of Si technology.

Figures 6.1 and 6.2 shows the experimental barrier heights versus the ideality factors plot of the electrodeposited Ni/*n*-Si and Co/*n*-Si Schottky barrier diodes at room temperature.

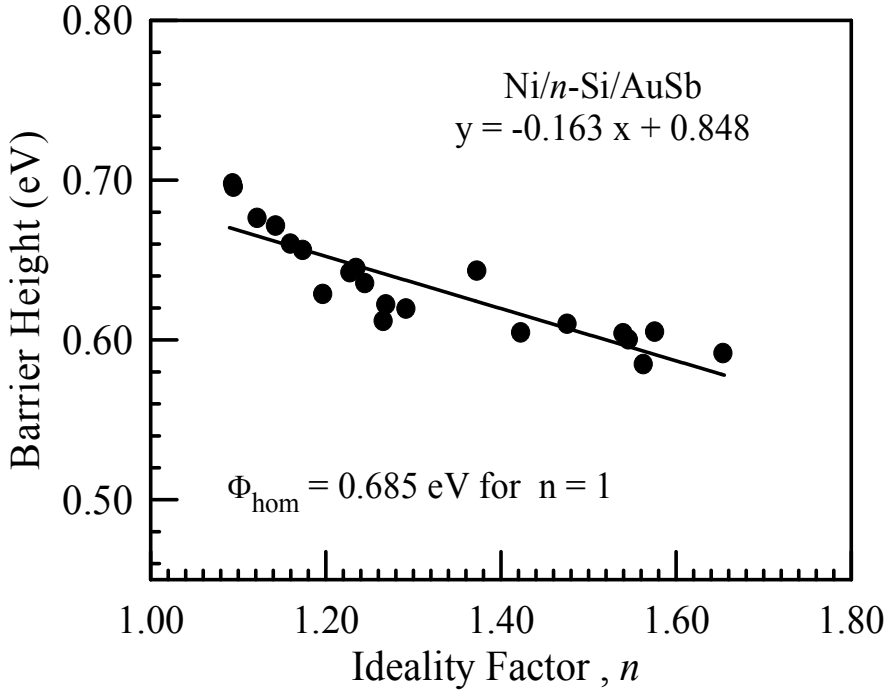



Figure 6.1 The experimental barrier height versus ideality factor plot of the electrodeposited Ni/*n*-Si/Schottky barrier diodes at the room temperature

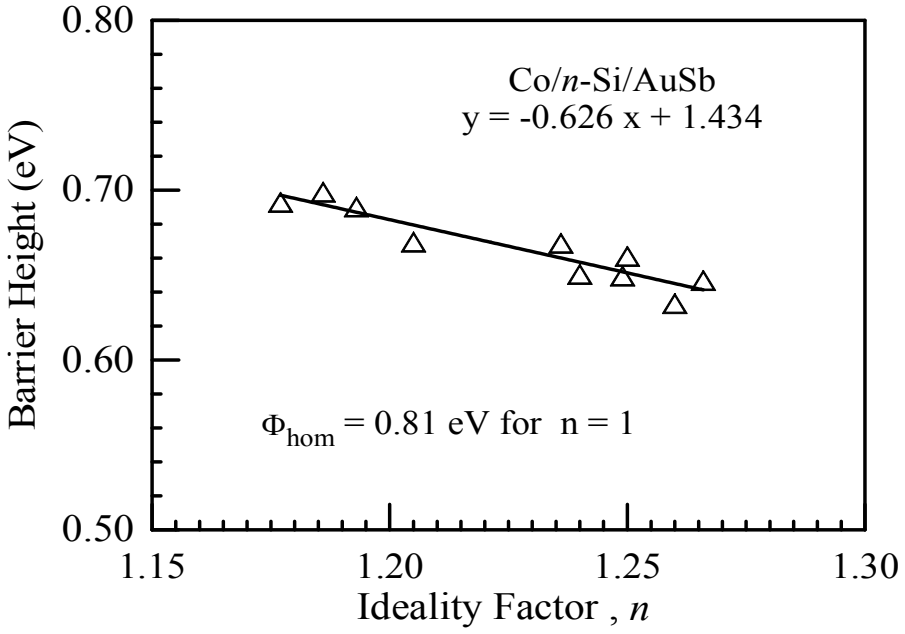



Figure 6.2 The experimental barrier height versus ideality factor plot of the electrodeposited Co/*n*-Si/Schottky barrier diodes at the room temperature

As can be seen from Figures 6.1 and 6.2, there is a linear relationship between experimental effective BHs and ideality factors of the electrodeposited Ni/*n*-Si and Co/*n*-Si Schottky contacts. That is, the barrier heights become smaller as the ideality factors increase. This finding may be attributed to lateral barrier inhomogeneities of in Schottky diodes [46,48,49,51,52,57,113,116,117]. It has been mentioned that higher ideality factors among identically prepared diodes were often found to accompany lower observed barrier heights. A laterally homogeneous barrier height value of 0.69 eV for the electrodeposited Ni/*n*-Si SBDs and 0.81 eV for the electrodeposited Co/*n*-Si Schottky contacts were obtained from the linear relationship between the experimental effective BHs and the ideality factors that can be explained by lateral inhomogeneities, in Figures 6.1 and 6.2.

The homogeneous BH of 0.69 eV for the electrodeposited Ni/*n*-Si SBD formed by us is close to the value of 0.71 eV by Kiziroglou et al. [30]. In addition, the homogeneous barrier height value of 0.69 eV is larger than value of 0.67 eV given for the vacuum-deposited *n*-Si SBD in ref. [4]. Furthermore, the homogeneous BH of 0.81 eV for the electrodeposited Co/*n*-Si MS formed by us is close to value of 0.82 eV by Sağlam et al. Forment et al. [37] reported that the barrier height was higher for the electrochemically deposited contacts than for the vacuum evaporated one. They [37] assumed that the difference in barrier height between electrochemically deposited and evaporated contacts can be explained by the presence of a dipole layer containing oxygen at the metal-semiconductor interface of the electrochemically formed contacts. Moreover, as mentioned in [46], the homogeneous BHs rather than effective BHs of individual contacts or mean values should be used to discuss theories on the physical mechanism that determine the BHs of the MS contacts. Thus, provided the semiconductor substrate is well characterized then the homogeneous Schottky BH may be obtained from the *I-V* characteristics of even one contact [46].

As can be seen above, the mean BH value of 0.63 eV for the electrodeposited Ni/*n*-Si SBD and 0.67 eV for the electrodeposited Co/*n*-Si SBD from the statistical distribution of SBHs are smaller than the lateral homogeneous BH value of 0.69 eV for the Ni/*n*-Si SBD and 0.81 eV for Co/*n*-Si obtained from the linear relationship between the experimental effective BHs and ideality factors. Forment et al. [37] obtained an average value of 0.883 eV using BEEM to measure local BHs on a

nanometer scale for Au/n-GaAs SBDs. Leroy et al. [52] measured an average BH of 0.819 eV of the whole contact for Au/n-GaAs SBDs using conducting probe-AFM, instead of local nanometer-scale BHs. They concluded that a lower average of effective BH was obtained due to averaging over the whole contact. That is, the later BH value given by Leroy et al. [52] is because it is the lower barriers that carry the highest currents and hence dominate in the integration of the current over the total contact area, which is measured with conducting probe-AFM. Likely, we obtained a mean BH value of 0.63 eV smaller than the lateral homogeneous BH value of 0.69 eV because we made the measurements of the current over the total contact area. We would find a mean BH value near to the lateral homogeneous BH value of 0.69 eV if we used BEEM which gives the local BHs. However, the histograms in Figures 5.13-5.16 disregard the pronounced correlation between the effective BHs and ideality factors [52].

The high values of *n* can be attributed to the presence of a wide distribution of low-SBH patches which are occurred by laterally barrier inhomogeneous. The lateral inhomogeneous distribution of barrier heights at the interface may be caused by grain boundaries, multiple phases, facets, defects, a mixture of different phases etc. [46,48,49,51,52,57,116,117]. Ideality factors between 1.01 and 1.02 can be expected due to image force lowering of the Schottky barrier at the interface. Our data clearly show that the diodes have ideality factors that are considerably larger than the value determined by the image-force effect only. Therefore, these diodes are patchy [46,116,118]. The larger values of ideality factors are attributed to secondary mechanisms at the interface [3,4,8,48,56,78,122]. For example, interface defects may lead to a lateral inhomogenous distribution of barrier heights at the interface which then results in larger ideality factors, and the charge transport across the interface only is no longer due to thermionic emission. As seen from the explanations above, the inhomogeneities may play an important role and have to be considered in the evaluation of experimental *I-V* characteristics. Furthermore, the high values of *n* can also be attributed to the presence of a wide distribution of low-SBH patches caused by laterally barrier inhomogeneous.

Conductivity is given as:

$$G = \frac{dI}{dV} \tag{6.1}$$

When we look at the figures between (5.27) - (5.30) we see no change in the conductivity under the reverse bias with voltage. So this shows rectifying property of the diode clearly.

As a result of our MR measurements which are shown in the Figures 5.31 and 5.32, when the magnetic field is brought to the initial zero value the magnetoresistance value of Co samples remains stacked in a region of around 4% but the magnetoresistance of Ni reduces to a value close to zero. This means that the initial zero magnetic field state of the Co sample is not regained back after reducing the magnetic field to zero value. The resistance of the Co film does not therefore change much in a subsequent MR measurement which is done with a magnetic field applied along the same direction as the previous measurement. We ascribe this behaviour to the remanent magnetisation, i.e., to the magnetic moments pinned mostly at the easy axes along or around the direction of the magnetic field applied in the MR measurement. However the resistance value of the initial zero magnetic field state of Ni film is mostly regained back after we reduce the magnetic field to zero which may be attributed to the magnetic moments returning to the initial orientations along their initial easy axes. These effects are observed in both LMR and TMR measurement geometries.

## REFERENCES


[1] Liang, GR., Cui, TH. and Varahramyan, K. (2003). Fabrication and electrical characteristics of polymer-based Schottky diode. *Solid-State Electronics*, **47**, 691

[2] Horvath, ZsJ., Adam, M., Szabo, I., Serenyi, M. and Van Tuyen, V. (2002). Modification of Al/Si interface and Schottky barrier height with chemical treatment. *Applied Surface Science,* **190,** 441

[3] Sze, S.M. (1981). *Physics of semiconductor devices.* (2nd ed.). New York: Wiley.

[4] Rhoderick, E.H. and Williams, R.H. (1988). *Metal-semiconductor contacts.* Oxford: Clarendon Press.

[5] Jones, F.E., Hafer, C.B., Wood, R.G., Danner, M., Lonergan. (2001). *Journal of Appied Physics,* **90**, 1001

[6] Saha, A.R., Chattopadhyay, S., Das, R., Bose, C. and Maiti, C.K. (2006). Determination of the interface properties of Ni-silicided strained-Si/SiGe heterostructure Schottky diodes using capacitance-voltage technique. *Solid-State Electronics*, **50**, 1269

[7] Karataş, Ş. and Altındal Ş. (2005). Analysis of *I–V* characteristics on Au/n-type GaAs Schottky structures in wide temperature range. *Materials Science and Engineering B,* **122**,133

[8] Chand, S. and Kumar, J. (1996). Evidence for the double distribution of barrier heights in $Pd_2Si$/n-Si Schottky diodes from *I - V – T. Semiconductor Science and Technology*, **11**, 1203

[9] Tung, R.T. (2001). Recent advances in Schottky barrier concepts. *Material Science and Engineering*, R **35**, 138

[10] Karataş, Ş. (2005). Comparison of electrical parameters of Zn/p-Si and Sn/p-Si Schottky barrier diodes. *Solid State Communications*, **135**, 500

[11] Dimitruk, N.L., Borkovskaya, O.Yu., Dimitruk, I.N., Mamykin, S.V., Horvath, Zs. J. and Mamontova, I.B. (2002). *Applied Surface Science,* **190**, 455

[12] Hudait, M.K. and Kruppanidhi, S.B. (2000). *Solid-State Electronics*, **44**, 1089

[13] Werner, J.H. and Guttler, H.H. (1991). Barrier inhomogeneities at Schottky contacts. *Journal of Applied Phys*ics, **69**, 1522

[14] Singh, A., Reinhardt, K.C.and Anderson, W.A. (1990). *Journal of Applied Physics,* **68**, 3475

[15] Chattopadhyay, P.and Daw, A.N. (1986). On the current transport mechanism in a metal-insulator-semiconductor-(MIS) diode. *Solid-State Electronics*, **29**, 555

[16] Card, J.C. and Rhoderick, E.H. (1971). *Journal of Physics D,* **4**, 1589

[17] Hattori, K. and Torii, Y. (1991). A new method to fabricate Au/n-type InP Schottky contacts with an interfacial layer. *Solid-State Electronics*, **34**, 527-531

[18] Karataş, Ş., Altındal, Ş., Türüt, A. and Özmen, A. (2003). Temperature dependence of characteristic parameters of the H-terminated Sn/p- Si (100) Schottky contacts. *Applied Surface Sciences*, **217**, 250

[19] Akkal,B., Benamara, Z., Bideux, L. and Gruzza, B.(1999). Electrical characterization of the Au/InP(100) and Au/InSb/InP(100) structures. *Microelectronics Journal*, **30**, 673

[20] Chin, V.W.L., Green, M.A. and Storey, J.W.V. (1990). Evidence for multiple barrier heights in p-type PtSi schottky-barrier diodes from I-V-T and photoresponse measurements. *Solid-State Electronics,* **33**, 299

[21] Hanselaer, P.L., Laflere, W. H., Van Meirhaeghe, R. L. and Cardon, F. (1984). Current voltage characteristic of Ti-pSi metal-oxide-semiconductor diodes. *Applied Physics*, **56**, 2309

[22] Hanselaer, P. et al. (1986). The influence of a HF and an annealing treatment on the barrier height of p- and n-type Si MIS structures. *Applied Physics ,* **39**, 129

[23] Hökelek, E. and Robinson, G. Y. (1981). *Solid-State Electronics*, **99**, 24

[24] Loscutoff, P. W. and Bent, S. F. (2006). Reactivity of the Germanium Surface: Chemical Passivation and Functionalization. *Annual Review of Physical Chemistry*, **57**, 467

[25] Kwok, K.K. (1995). *Complete Guide to Semiconductor Devices.* New York: McGraw-Hill.

[26] Tyagi, M.S. (1991). *Introduction to Semiconductor materials and Devices*. New York: John Wiley.

[27] Rhoderick, EH. (1978). *Metal-Semiconductor Contacts*. Oxford University Press.

[28] Akkılıç, K., Aydın, M.E., Uzun, I. and Kılıçoğlu, T. (2006). The Calculation of Electronic Parameters of an Ag/chitin/n- Si Schottky barrier diode. *Synthetic Metals*, **156**, 958

[29] Akkılıç,K., Uzun, I. and Kılıçoğlu, T. (2007). The calculation of electronic properties of an Ag/chitosan/n-Si Schottky barrier diode. *Synthetic Metals*, **157**, 297

[30] Kiziroglou, M. E., Zhukov, Alexander A., Abdelsalam, M., Li, X., de Groot, P. A. J., Bartlett, P.N. and de Groot, C. H. (2005). Electrodeposition of Ni-Si Schottky barriers. *IEEE Transactions on Magnetics*, **41**, 10, 2639

[31] Zaman H et al. (1997). *IEEE Transactions on Magnetics,* **33**, 3517

[32] Neamtu, J., Volmer, M. and Coraci ,A. (1999). Magnetoresistive properties and microstructure of NiFe thin films and NiFe(*t*/Cu(*s*)/NiFe(*t*) multilayer films. *Thin Solid Films,* **343**, 218

[33] Hutchings, J.A., Newstead, K., Thomas, M.F., Sinclair, G., Joyce, D. E. and Grundy, P.J. (1999). Magnetic anisotropy in Ni/Fe and Fe/Cu/NiFe multilayers. *Journal of Physics: Condensed Matter,* **11**, 3449.

[34] Raquet, R., Viret, M., Warin, P., Sondergard, E. and Mamy, R. (2001). Negative high field magnetoresistance in 3d ferromagnets. *Physica B*, **294**, 102

[35] Chynoweth, T.A. and Bube, R.H. (1980). Electrical transport in ZnCdS films deposited by spray pyrolysis. *Journal of Applied Physics*, **51**, 3, 1844.

[36] Bakkaloğlu, Ö.F., Karahan, İ.H., Efeoğlu, H., Yıldırım, M., Çevik, U. and Yoğurtçu, Y.K. (1998). Magnetic studies on electrodeposited $Cu_{1-x}Co_x$ alloy films. *Journal of Magnetism and Magnetic Materials,* **190**, 193.

[37] Forment, S., Van Meirhaeghe, R. L., De Vrieze, A., Strubbe, K. and W. Gomes, P. (2001). A comparative study of electrochemically formed and vacuum-deposited n-GaAs/Au Schottky barriers using ballistic electron emission microscopy (BEEM). *Semiconductor Science and Technology,* **16**, 975.

[38] Bao, Z. L. and Kavanagha, K. L. (2006). Epitaxial Bi/GaAs diodes via electrodeposition. *Journal of Vacuum Science and Technology B,* **24**, (4) 2138.

[39] Eftekhari, A. (2003). Improving Cu metallization of Si by electrodeposition under centrifugal fields. *Microelectronic Engineer*, **69**, 17.

[40] Saxena, V. and Prakash, R. (2000). Effect of steric hinderance on junction properties of poly (3-alkylthiophene)s based schottky diodes. *Polymer Bulletin, 45, 267.*

[41] Pattanaik, G.R., Pandya, D.K. and Kashyap, S.C. (2001). Giant magnetoresistance in Cu–Co films electrodeposited on n-Si. *Journal of Magnetism and Magnetic Materials,* **234**, 294-298

[42] Monsma, D. J., Lodder, J. C., Popma, T. J. A., and Dieny, B. (1995). Perpendicular hot electron spin-valve effect in a new magnetic field sensor: The spin-valve transistor. *Physical Review Letters,* **74**, 26, 5260–5263

[43] Van Dijken, X. J. S. and Parkin, S. S. P. (2003). Comparison of magnetocurrent and transfer ratio in magnetic tunnel transistors with spin-valve bases containing Cu and Au spacer layers. *Applied Physics Letters*, **82**, 5. 775–777

[44] Zang, H. and Wang, W. (2003). Microfabrication and test of a magnetic field sensor using electrodeposited thin film of giant magnetoresistive $(Cu/Co)_x$ multilayers *Microsystem Technologies*, **9**, 436.

[45] Baibich, M.N., Broto, J.M., Fert, A., Nguyen Van Dau, F., Petroff, F., Etienne, P., Creuzet, G., Friederich, A. and Chazelas, J. (1988). Giant Magnetoresistance of (001)Fe/(001)Cr Magnetic Superlattices. *Physical Review Letters,* **61**, 2472.

[46] Mönch, W. (1999). Barrier heights of real Schottky contacts explained by metal-induced gap states and lateral inhomogeneities. *Journal of Vacuum Science and Technology B*, **17**, 1867

[47] Mönch, W. (2001). *Semiconductor Surfaces and Interfaces*. (3rd ed.). (Springer, Berlin), 389, 421, 485.

[48] Im, H. J., Ding, Y., Pelz, J. P. and Choyke, W. J. (2001). Nanometer-scale test of the Tung model of Schottky-barrier height inhomogeneity. *Physical Review*, 64, (7), 075310

[49] Kampen, T. U. and Mönch, W. (1995). Lead contacts on Si(111):H-1×1 surfaces. *Surface Science,* **490**, 331-333

[50] Akkılıç, K., Aydın, M. E., and Türüt, A., (2004). The Effect of Series Resistance on the Relationship Between Barrier Heights and Ideality Factors of Inhomogeneous Schottky Barrier Diodes. *Physica Scripta, 70, 364*

[51] Çetin, H., Şahin, B., Ayyıldız, E. and Türüt, A. (2004). The barrier-height inhomogeneity in identically prepared H-terminated Ti/p-Si Schottky barrier diodes. *Semiconductor Science and Technology*, 19, 1113

[52] Leroy, W.P., Opsomer, K., Forment, S. and Van Meirhaeghe, R.L. (2005). The barrier height inhomogeneity in identically prepared Au/n-GaAs Schottky barrier diodes. *Solid-State Electronics,* **49**, 878

[53] Altındal, S., Kanbur, H., Tataroglu, A. and Bulbul, M.M. (2007). The barrier height distribution in identically prepared Al/p-Si Schottky diodes with the native interfacial insulator layer ($SiO_2$). *Physica B,* **399**, 146

[54] Akkılıç, K., Türüt, A., Çankaya, G. and Kılıçoğlu, T. (2003). Correlation between barrier heights and ideality factors of Cd/n-Si and Cd/p-Si Schottky barrier diodes. *Solid State Communications,* **125**, 551

[55] Doğan, H., Yıldırım, N., Türüt, A., Biber, M., Ayyıldız, E. and Nuhoğlu, C. (2006). Determination of the characteristic parameters of Sn/n-GaAs/Al–Ge Schottky diodes by a barrier height inhomogeneity model. *Semiconductor Science and Technology,* **21**, 822

[56] Tung, R. T. (1992). Electron transport at metal-semiconductor interfaces: General theory. *Physical Review Letters B*, 45, 13509

[57] Sullivan, J. P., Tung, R.T., Pinto, M.R. and Graham, W.R. (1991). Electron transport of inhomogeneous Schottky barriers: A numerical study. *Journal of Applied Physics,* **70**, 7403

[58] Schmitsdorf, R F., Kampen, T U and Mönch, W. (1997). Explanation of the linear correlation between barrier heights and ideality factors of real metal-semiconductor contacts by laterally nonuniform Schottky barriers. *Journal of Vacuum Science and Technology B,* **15,** 1221

[59] Braun, K.F. (1874). *Physical Chemistry*, **153**, 556

[60] Torrey, H.C. and Whitmer, C.A. (1948). *Crystal Reectifers*. Mc Graw Hill.

[61] Schottky, W. (1914). *Physics*. 215

[62] Sze, S.M., Crowell, C.R. and Kahng, D. (1964). Photoelectric Determination of the Image Force Dielectric Constant For Hot Electrons in Schottky Barriers *Journal of Applied Physics*, **35**, 2534

[63] Schottky, W. and Spenke, E. (1939). *Wiss Veroff Semeis-Werken,* **18**, 225

[64] Crowell, C.R. and Sze, S.M. (1996). Current transport in metal-semiconductor barriers. *Solid-State Electronics*, **9**, 1035

[65] Cowley, A.M. and Sze, S.M. (1965). Surface States and Barrier Height of Metal-Semiconductor Systems. *Journal of Applied Physics,* **36**, 3212

[66] Tseng, H.H. and Wu, C.Y. (1987). *Solid-State Electronics*, **30**, 383

[67] Schottky, W. (1938). *Naturwiss,* **26**, 843

[68] Mott, N.F. (1938). The contact between a metal and an insulator or semiconductor. *Proceedings of the Cambridge Philosophical Society*, **34**, 568-572

[69] Jeong, H.Y., Kim, G.T., Kim, S.T., Kim, K-II. and Chung, W.J. (1991). *Journal of Applied Physics*, **69**, 6699

[70] Türüt, A. and Sağlam, M. (1992). Determination of the density of Si-metal interface states and excess capaticance caused by them. *Physica B*, **179**, 285

[71] Szatkowski, J. and Sieranski, K. (1992). ). Simple interface-layer model for the nonideal characteristics of the Schottky-Barrier diode. *Solid-State Electronics*, **35**, 1013

[72] Türüt, A., Gümüş, A., Sağlam, M., Tüzemen, S., Efeoğlu, H., Yalçın, N. and Missous, M. (1998). Thermal stability of Cr-Ni-Co alloy Schottky contacts on MBE *n*-GaAs. *Semiconductor Science and Technology.* 13

[73] Karataş, Ş. and Altındal, Ş. (2005). Analysis Dependence on Temperature of Basic Electrical Parameters on Zn/ p-Si Schottky Diodes. *KSU Journal of Science and Engineering,* 8(1)

[74] Kılıçoğlu, T. and Asubay, S. (2005). The effect of native oxide layer on some electronic parameters of Au/n-Si/Au-Sb Schottky barrier diodes. *Physica B,* **368**, 58-63

[75] Dağdelen, F. and Aydoğdu, A. (2006). Electronic Properties of the Ni/n- type Complex Semiconductor / Ag Schottky diodes. *Science and Engineering Journal of Fırat Univercity,* **18**, (3), 291-295

[76] Huanga, W.C., Sub, S.H., Hsuc, Y.K., Wangd, C.C. and Changc, C.S. (2006). *Superlattices and Microstructures,* **40**, 644-650

[77] Rossi, R.C. and Lewis, N.S. (2001). Investigation of the Size-Scaling Behavior of Spatially Nonuniform Barrier Height Contacts to Semiconductor Surfaces Using Ordered Nanometer-Scale Nickel Arrays on Silicon Electrodes. *Journal of Physical Chemistry B*, **105**, (17), 12303

[78] Song, Y.P., Van Meirhaeghe, R.L., Laflére, W.H. and Cardon, F. (1986). *Solid - State Electronics,* **29**, 633

[79] Zhu, S., Van Meirhaeghe, R. L., Detavernier, C., Cardon, F., Ru, G., Qu, X. and Li, B. (2000). *Solid-State Electronics,* **44**, 663

[80] Osvald, J. (2006). Series resistance influence on intersecting behaviour of inhomogeneous Schottky diodes *I–V* curves. *Solid-State Electronics,* **50**, 228

[81] Başol, B.M. (1988). *Solar Cells,* **23**, 69-88

[82] Bedir, M. (2002). Growth of Semiconducting and Conducting Thin Films and Investigation on Their Electrical, Magnetical and Optical Properties. *Thesis Ph.D.* University of Gaziantep.

[83] Bhattacharya, R.N. and Rajeshwan, K.(1985). *Journal of Applied Physics,* .**58**, (9) 3590-3593

[84] Kiziroglou, M. E., Zhukov, A.A., Li, X. Gonzalez, D.C., de Groot, P.A.J., Bartlett, P.N. and de Groot, C.H. (2006). Analysis of thermionic emission from electrodeposited Ni-Si Schottky barriers. *Solid State Communications*, **140**, 508-513

[85] Kiziroglou, M. E., Li, X. Zhukov, A.A., de Groot, P.A.J. and de Groot, C.H. (2008). Thermionic field emission at electrodeposited Ni-Si Schottky barriers. *Solid-State Electronics,* **52**, 1032-1038

[86] Ahmetoğlu (Afrailov), M., Alper, M., Şafak, M., Ertürk, K., Gürpınar, B., Kocak, F. and Hacıismailoğlu, C. (2007). Electrical properties of n-Si / Cu Schottky diodes formed by electrodeposition. *Journal of Optoelectronics and Advanced Materials,* **9**, 4 818-821

[87] Güllü, Ö., Barış, Ö., Biber, M. and Türüt, A. (2008). Laterally inhomogenous barrier analysis of the methyl violet/p-Si organic/ inorganic hybrid Schottky structures. *Applied Surface Science,* **254**, 3039-3044

[88] Duman, S., Doğan, S., Gürbulak, B. and Türüt, A. (2008). The barrier-height inhomogeneity in identically prepared Ni/n-type 6H-SiC Schottky diodes *Applied Physics A,* **91**, 337-340

[89] Smith, W.F. (1990). *Principles of Materials Science and Engineering.* (McGraw-Hill-Singapore).

[90] SILICA VALLEY.com 02, january 2007

[91] Ziel, A.V. (1968). *Solid State Physical Electronics*. Prentice-Hall, New-Jersey. 245.

[92] Akkılıç, K. (2002). Si Tabanlı Sn metali ile oluşturulan ince arayüzey doğal oksit tabakalı ve tabakasız Schottky diyotların idealite faktörleri ile engel yükseklikleri arasındaki lineer ilişkinin araştırılması. *Thesis Ph.D.*, University of Dicle.

[93] Cheung, S.K. and Cheung, N.W. (1986). Extraction of Schottky diode parameters from forward current-voltage characteristics. *Applied Physics Letters.* **49**, 85

[94] Andrews, J.M. and Lepselter, M.P. (1970). Reverse current-voltage characteristics of metal-silicide Schottky diodes. *Solid-State Electronics*, **13**, 1011

[95] McGuire, T.R. and Potter, I. (1975). *IEEE Transactions on Magnetics*, **11**, 1018

[96] Xiao, J.Q., Jiang, J.S. and Chien, C.L. (1992). Giant magnetoresistance in nonmultilayer magnetic systems. *Physical Review. Letters,* **68**, 3749

[97] Switzer, Jay A. and Moffat, Thomas P. (2006). Gordon Research Conference on Electrodeposition. Colby-Sawyer College New London, NH.

[98] Pasa, A. A. and Schwarzacher, W. (1999). Electrodeposition of Thin Films and Multilayers on Silicon. *Physica status solidi* (a). **173**, 1. 73-84 WILEY-VCH Verlag Berlin GmbH, Fed. Rep. of Germany.

[99] Bartlett, P. N., Ghanem, M. A., Hallag, I. S. E., de Groot, P. and Zhukov, A. (2003). "Electrochemical deposition of macroporous magnetic networks using colloidal templates.," *Mater, Journal of Materials Chemistry*, **13**, 2596–2602

[100] Schlesinger, M. and Paunovic, M. (editors). (2000). *Modern Electroplating* (4th ed.). Wiley, New York.

[101] Paunovic, M. and Schlesinger, M. (1998). *Fundamentals of Electrochemical Deposition*. Wiley, New York.

[102] Blum, W. (1952). *J. Electrochemical Society* , **99**, 31C

[103] Dettner, H.W., Elze, J. and Raub, E. (1966). *Handbuch der Galvanotechnik.* Carl Hanser Verlag, München.

[104] McKinney, B.L. and Faust, C.L. *J.* (1977). *Electrochemical Society,* **124**, 379C

[105] Landolt, D., *J.* (2002). Electrodeposition Science and Technology in the Last Quarter of the Twentieth Century. *Electrochemical Society*, **149**, S9

[106] Zhao, Q. T., Breuer, U., Rije, E., Lenk, S. and Mantl, S. Tuning of NiSi/Si Schottky barrier heights by sulfur segregation during Ni silicidation. *Applied Physics Letters*, **86**, 062 108, 2005

[107] Spiegel, A. (2003). *Electrochemical Investigation of Ion Implanted p-Si*. p.6, THÈSE N$^{O}$ 2783.

[108] Dhingra, S ., Shrma, R. and George, P. J. (1999). Selective Deposition of a Thin Copper Film for Metallization on Silicon by the Chemical Bath Process. *Solid-State Electronics,* **43**, 2231

[109] Karataş, Ş., Altındal, Ş. and Çakar, M. (2005). Current Transport in Zn/p- Si (100) Schottky Barrier Diodes at High Temperatures. *Physica B,* **357**, 386

[110] Karataş, Ş. and Türüt, A. (2006). The Determination of Electronic and Interface State Density Distributions of Au/n-type GaAs Schottky Barrier Diodes *Physica B,* **381**, 199

[111] Kumar, S., Katharria, Y. S., Kumar, S. and Kanjilal, D. (2006). Temperature Dependent Barrier Characteristics of Swift Heavy Ion Irradiated Au/n-Si Schottky Structure. *Journal of Applied Physics*, **100**, 113723

[112] Keffous, A., Siad, M., Mamma, S., Belkacem, Y., Lakhdar Chaouch, C., Menari, H., Dahmani, A. and Chergui, W. (2006). *Applied Surface Science*, **218**, ( 2003) 337

[113] Güler, G., Güllü, Ö., Bakkaloğlu, Ö. F. and Türüt, A. (2008). Determination of lateral barrier height of identically prepared Ni/n-type Si Schottky barrier diodes by electrodeposition. *Physica B,* **403**, 2211-2214

[114] Şahin, B., Çetin, H. and Ayyıldız, E. (2005). The effect of series resistance on capacitance–voltage characteristics of Schottky barrier diodes. *Solid State Communications,* **135**, 490

[115] Ebeoğlu, M.A., Temurtaş, F. T. and Öztürk, Z. Z. (1998). *Solid-State Electronics,* **42**, 23

[116] Ohdomari, J. and Tu, K.N. (1980). *Journal of Applied Physics*, **51**, 3735

[117] Akkılıç, K., Kılıçoğlu, T. and Türüt, A. (2003). Linear correlation between barrier heights and ideality factors of Sn/n-Si schottky diodes with and without the interfacial native oxide layer. *Physica B,* **337**, 388

[118] Sağlam, M., Cimili, F.E. and Türüt, A. (2004). Experimental determination of the laterally homogeneous barrier height of Au/*n*-Si Schottky barrier diodes *Physica B,* **348**, 397

[119] Bozorth, R.M. (1993 ed.). *Ferromagnetism*. *IEEE* Press. 746.

[120] Handley, R.C.O'. (1999). *Modern Magnetic Materials Principles and Applications*. John Wiley and Sons, Inc. 575.

[121] Wittmer, M. and Freeouf, J.L. (1992). Ideal Schottky diodes on passivated silicon. *Physical Review Letters*, **69**, 2701

[122] Doğan, H., Korkut, H., Yıldırım, N. and Türüt, A. (2007). Prediction of lateral barrier height in identically prepared Ni/*n*-type GaAs Schottky barrier diodes. *Applied Surface Science,* **253**, 7467

## CURRICULUM VITAE

## PERSONAL INFORMATION

Surname, Name: Şahin (Güler) Gülsen
Nationality: Turkish (TC)
Date and Place of Birth: 18 January 1975 , Adana
Marital Status: Married
Phone: +90 0533 216 0259
email: gsahin@adiyaman.edu.tr

## EDUCATION

| Degree | Institution | Year of Graduation |
|---|---|---|
| MS | University of Dicle, Physics | 2000 |
| BS | University of Dicle, Education of Physics | 1997 |
| High School | Adıyaman High School | 1992 |

## WORK EXPERIENCE

| Year | Place | Enrollment |
|---|---|---|
| 2003- Present | University of Adıyaman | Research Assistant |
| 1998-2003 | University of Dicle | Research Assistant |
| 1997-1998 | Diyarbakır | Teacher |

## FOREIGN LANGUAGES

English

## PUBLICATIONS

1. Güler, G., Güllü, Ö., Bakkaloğlu, Ö.F. and Türüt, A. (2008). Determination of lateral barrier height of identically prepared Ni/n-type Si Schottky barrier diodes by electrodeposition. *Physica B,* **403**, 2211-2214

2. Güler, G., Güllü, Ö., Karataş, Ş. and Bakkaloğlu, Ö.F. (2009). Analysis of the series resistance and interface state densities in metal semiconductor structures. *Journal of Physics:Conference Series,* **153**, 012054

3. Güler, G., Güllü, Ö., Karataş, Ş. and Bakkaloğlu, Ö.F. (2009). Electrical Characteristics of Co/n-Si Schottky Barrier Diodes Using $I - V$ and $C - V$ Measurements. *Chinese Physics Letter*, **26**, 6, 067301

4. Güler, G., Karataş, Ş., Güllü, Ö. and Bakkaloğlu, Ö.F. (2009). The analysis of lateral distribution of barrier height in identically prepared Co/*n*-Si Schottky diodes. *Journal of Alloys and Compounds,* **486**, 343–347

5. Güler, G., Karataş, Ş. and Bakkaloğlu, Ö.F. (2009). Annealing temperature effect on electrical characteristics of Co/p-type Si Schottky barrier diodes. *Physica B: Physics of Condensed Matter*, **404**, 8-11, 1494-1497

6. Çelik, Ö., Kılıçoğlu, T., Akkılıç, K., Güler, G. and Aydın, M.E. (2001). Investigation of The Interface State Density of p-Si\Anodic Oxide\Al Structures Optained by Application of Various Constant Voltages. *Fizika J*, **6**, 4, 77-79

7. Maskan, A. and Güler, G. (2004). Kavram Haritaları Yönteminin Fizik Öğretmen Adaylarının Elektrostatik Kavram Başarısına ve Elektrostatiğe Karşı Tutumuna Etkisi. *Çağdaş Eğitim*, **309**, 34-40

**REFERENCE PROCEEDINGS**

1. Güler, G., Aydın, M.E., Akkılıç, K. and Kılıçoğlu, T. Farklı Sabit Akım Uygulayarak Oluşturulan p-Si\$SiO_2$\Al Yapılarının Özelliklerinin Araştırılması. Turkish Physical Society II. National Condenced Matter Physics Congress. 22-24 June 2000 University of Atatürk Erzurum-Turkey

2. Kılıçoğlu, T., Ebeoğlu, M.A., Öztürk, Z.Z., Aydın, M.E., Akkılıç, K. and Güler, G. Sabit Akım Uygulayarak Oluşturulan p-Si\$SiO_2$\Al Yapının Özelliklerinin Araştırılması. Turkish Physical Society 19$^{th}$ Physical Congress. 26-29 September 2000,University of Fırat, Elazığ-Turkey

3. Güler, G., Özek, N. and Yaprak, G. 1999-2001 ÖSS Fizik Sınav Sorularının Bilişsel Gelişim Seviyelerinin İncelenmesi, Dershane ve Liselerde Sorulan Soruların Bilişsel Gelişim Seviyeleriyle Karşılaştırılması. Turkish Physical Society 21$^{st}$ Physical Congress. 11-14 September 2002 SDU. Isparta-Turkey

4. Güler, G., Güllü, Ö., Karataş, Ş. and Bakkaloğlu, Ö.F. The determination of electrical characteristics of Co/n-Si Schottky contacts. Turkish Physical Society 25$^{th}$ international Physical Congress. 25-29 August 2008 Bodrum-Turkey

5. Güler, G., Güllü, Ö., Karataş, Ş. and Bakkaloğlu, Ö.F. Annealing Temperature Dependent of Electrical Properties of Ni/p-Si (100) Schottky Diodes. Turkish Physical Society 25$^{th}$ international Physical Congress. 25-29 August 2008 Bodrum-Turkey

6. Güler, G., Güllü, Ö., Karataş, Ş. and Bakkaloğlu, Ö.F. Analysis of the series resistance and interface state densities in metal semiconductor structures. International Conference On Superconductivity and Magnetism (ICSM2008) Antalya- Turkey