JUNE 2017 M.Sc. in Electrical and Electronics Engineering HUSNAIN UL HASEEB KAZMI

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CASCADED H-BRIDGE MULTILEVEL CONVERTER BASED D-STATCOM

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ELECTRICAL AND ELECTRONICS ENGINEERING

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Assist. Prof. Dr. Ahmet Mete VURAL

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Husnain Ul Haseeb Kazmi

ABSTRACT

Cascaded H-Bridge Multilevel Converter Based D-Statcom

Husnain Ul Haseeb Kazmi

M.Sc. in Electrical-Electronics Engineering

Supervisor: Assist. Prof. Dr. A. Mete VURAL

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The aim of this thesis is to study the power quality of electrical power system based on Cascaded H-Bridge multilevel converter D-STATCOM. The power system simulation has been done in computer software. Modulation technique used is Space Vector Pulse Width Modulation, because of its advantages over other techniques. But the problem of this technique is implementation, due to its complexity for high number voltage levels. Mostly power quality is affected by the types of loads connected at the distribution level of electrical power systems or by any type of faults. Inductive type of loads connected to the system creates a small dip in the power quality which should not be compromised. It can be seriously harmful for both the power system and for the consumers of power. Different type of compensation devices are used to sort out this problem. One of the compensation devices is D-STATCOM which is connected in parallel to the system near to the distribution point to overcome the power quality problems. D-STATCOM can absorb as well as inject the reactive power to keep system at steady state.

Keywords: Distribution static synchronous compensator (D-STATCOM); Space vector pulse width modulation (SVPWM); Distribution series capacitors; Multilevel cascaded H-bridge inverter, Voltage sags.

ÖZET

Kaskat H-Köprü Çok Seviyeli Çevirgeç Tabanli D-Statkom

Husnain Ul Haseeb Kazmi

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Danışman: Yrd. Doç. Dr. Ahmet Mete VURAL

Haziran 2017, 57 sayfa

Bu tezin amacı kaskat H-köprü çok seviyeli çevirgeç tabanlı D-STATKOM tabanlı elektrik güç sisteminin güç kalitesini çalışmaktır. Güç sistemi benzetimi bilgisayar yazılımında yapılmıştır. Diğer modülasyon tekniklerine göre avantajlarından ötürü kullanılan modülasyon tekniği Uzay Vektör Darbe Genişlik Modülasyonudur. Fakat bu tekniğin problemi yüksek sayıdaki gerilim seviyelerinin karmaşıklığı yüzünden uygulamasındadır. Çoğu kez güç kalitesi elektrik güç sistemlerinin dağıtım seviyesindeki bağlanan yük çeşitlerinden veya arıza türlerinden dolayı etkilenir. Sisteme bağlanan endüktif tipteki yükler güç kalitesinde göz ardı edilmemesi gereken küçük azalmalar oluştururlar. Bu durum hem güç sistemi hem de güç tüketicileri için ciddi anlamda zarar verici olabilir. Bu problemi gidermek için farklı tipte kompanzasyon cihazları kullanılmaktadır. D-STATKOM, kompanzasyon cihazlarının bir türüdür ve güç kalitesi problemlerini gidermek için dağıtım noktasının yanında sisteme paralel bağlanır. D-STATKOM, sistemi durgun-hal koşullarında tutmak için reaktif gücü absorbe veya enjekte edebilir.

Anahtar Kelimeler: Dağıtım statik senkron kompanzator (D-STATKOM); Uzay vektör darbe genişlik modülasyonu (SVPWM); Dağıtım seri kapasitörler; Çok seviyeli kaskat H-köprü evirici; Gerilim düşümleri.

Dedicated to My Father, My Mother, My brother and Sisters and Noor-us-Saba

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LIST OF SYMBOLS/ABBREVIATIONS

FACTS	Flexible AC Transmission Systems
UPFC	Unified Power Flow Controller
IPFC	Interline Power Flow Control
SVC	Static Var Compensator
STATCOM	Static Synchronous Compensator
D-STATCOM	Distribution Static Synchronous Compensator
SVPWM	Space Vector Pulse Width Modulation
SVM	Space Vector Modulation
GTO's	Gate Turn Off
VSC	Voltage Source Converter
TCSC	Thyristor Controlled Series Capacitor
TCPS	Thyristor Control Phase Shifters
TCR's	Thyristor Control Reactor
TSSR	Thyristor Switched Series Reactor
TSSC	Thyristor Switched Series Capacitor
MLI	Multilevel Inverter
APOD	Alternative Phase Opposition Disposition
PD	Phase Disposition
PS	Phase Shift
THIPWM	Third Harmonic Injection Pulse Width Modulation
PSPWM	Pure Sine Pulse Width Modulation
DBPWM	Dead Band Pulse Width Modulation
SIC	Super Imposed Carrier
PWM	Pulse Width Modulation
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
NPC	Neutral Point Clamped
CHB	Cascaded H-Bridge

CC	Capacitor Clamped
FC	Flying Capacitor

CHAPTER 1

1.1 Introduction

Nowadays electrical energy is one of the basic requirements in almost every field of life, whether it is home or it is office. Day by day the technical advancements are making impact on this world. Almost in every field there is interference of automation, robots, and industries. To fulfill the input requirements for these we need a good quality power. There are some factors which can affect the power quality of electrical power systems e.g. the variable loads, faults in lines etc. These situations are very critical if they last longer, even in seconds. If oscillations in the power systems are not damped effectively then the results can create an increase in the magnitude of these oscilations, which can destabilize the system and can be very harmful. Stability of the electrical power systems is one of the big concerns for the operation and control of the electrical power systems.

To get control on the instabilities of the power systems some compensation devices should be attached to the system, these can be connected in series or in parallel. In power electronics these devices are called Flexible Alternating Current Transmission Systems (FACTS). These devices are fundamentally power electronics apparatuses which are very valuable for increasing the transmission ability in the power system. The good advantage of these devices is that they give control to several parameters in the power transmission system network [1].

This type of power electronics devices can boost the dependability in the power systems network, they also back/help the voltage with improved control of their constraints like reactive power flow, voltage and current, phase angle [2]. FACTS devices can develop good dynamic performance and can also uplift the dependability of power electronics based systems and boost power flow control of the network [3]. FACTS devices vary basically in two categories such as in series, or in parallel, or in

the mixture of both series and parallel. Fundamentally there are two types to shunt connected compensator devices, (1) is Static VAR Compensator (SVC) and (2) is Static Synchronous Compensator fact devices. Some of the science scholars had shown that when a parallel (shunt) connected FACTS compensator devices such as SVC or STATCOM are installed at the mid of transmission line system then they can double the steady state power transfer ability of a line as compared to the original generated one. Basically parallel (shunt) compensation device provides a good quality real power handling ability of the transmission line in a extra economic price than constructing another transmission line of same or more capability. Shunt compensation devices (FACTS) offer simple control and the good reactive power help to the power transmission system [4]. Because of economic factor, it is very difficult to install the shunt controller devices in all the buses of transmission lines, so it is very important as well as effective to find the finest position and proportions of supplementary compensator by bearing in mind the calculations and design of stable state of the power system [5].

1.2 Motivation of Thesis

Power quality is always a big deal in transmission system, this cannot be compromised if so, it can harm the both generation and load side. In this thesis, work was done to improve the power quality and to control some of the parameters, like voltage, phase angle, current, active or reactive power. FACTS devices were introduced to help in transmission of good quality power. In this thesis one of the parallel FACTS device is used which is the Distribution Static Synchronous Compensator (D-STATCOM). It will be discussed in detail in chapter 3.

1.3 Contribution of Thesis

The contribution of D-statcom in the transmission system is very effective and has a good value. It can be said that it is a low cost power supplement, which strengthens the signal up to the destination. Gives an upper hand to control the system’s output. In this task modulation scheme for the converter is SVPWM. Three level space vector pulse width modulation has been implemented on the converter side which will be explained in detail in Chapter 4.

1.4 Overall Summary of the Thesis

This thesis is organized in 6 chapters in total.

Chapter 1: This chapter is about a short introduction of the thesis and the task which is done in it. It also informs about the type of FACTS device which will be used in the whole process and type of modulation scheme.

Chapter 2: This chapter explains about the work done in the past. A short background and what type of work done and its effects and who and when did he/she did it.

Chapter 3: In this chapter type of inverters and their topologies are discussed. Moreover the FACT device is discussed in detail.

Chapter 4: This chapter explains about the modulation technique which has been used in this task.

Chapter 5: This chapter shows the results of the modeling and simulation of the power system. Some case studies are also studied to check the performance of system.

Chapter 6: In this last chapter conclusion has been explained and some ideas for the future work are shown.

CHAPTER 2

LITERATURE SURVEY

2.1 Introduction

Electrical power systems history start from the day when first electrical system was installed to transmit the energy. Ever since that day power quality and its long range effective transmission is under research. Millions of people around the world are work in this field to improve and provide good quality power to the consumer systems.

2.2 Short Literature Analysis

The article "Quality of power in the Electronics age" written in 1980's by john Douglas a science writer states briefly about the power quality importance and its impact on the electrical systems. He in this document stated that how voltage dips can affect the computer system, the households, and how costly almost 1Billion $ was used to spend to avoid power disruptions through the plans which were to install underground lines and setting the power transmission poles far away from the traffic.[6]

In another outline of power distributor's responsiveness and worries about the power quality problems/issues some researchers enlightened the importance of good quality of power transmission. The necessity for transporting a good quality of electricity is required and electric practicalities are taking measurements to offer the improved power requisite by their clients. Based on superior power excellence plans being applied by electrical utilities and in the survey showed by TVPPA, conclusion can be determined that good power feature is an increasing anxiety to the electrical utilities and asks for larger usefulness care of power suppliers have to deal with power transmission quality associated issues on a repetitive basis. Furthermore, these problems are related with all end user types and are created around alike by utilities and clients. [7]

In early 1980's it was found that in France, for telecommunication systems, some transistor based inverters were used separately to provide the best efficiency and reliability and the quasi square wave [8]. These type of inverters were the basic power quality maintainers. By the time passed and researched done to improve the quality of power introduced some other type of power converters and compensation devices.

In late times of 1980's the "Electrical Power Research Institute" expressed the idea of Flexible Alternative Current Transmission System's (FACTS) which consists of different controllers for power electronic control and movement and conduction voltage and alleviate active instabilities [9]. Normally, the basic purposes of FACTS devices are to surge the working ability of power transmission line and to regulate the flow of power. Hingorani and Gyugyi [10] and Hingorani [11], [12] suggested idea of FACTS devices. Edris *et al.* [13] suggested explanations and some terms for various FACTS regulators. Basically till now two categories for recognition of electronical power based FACTS controllers are present: one consists predictable or conventional reactors and thyristor-switched capacitors, and quadrature tap changer transformers, the second one consists gate turn-off (GTO's) thyristor-switched converter for voltage source converters (VSCs). The first category has stemmed in the Static Var Compensators (SVC), the Thyristor- Controlled Series Capacitors (TCSC), and the Thyristor-Controlled Phase Shifters (TCPS) [14], [15]. The second group has made the Static Synchronous Compensators (STATCOM), the Static Synchronous Series Compensators (SSSC), the Unified Power Flow Controllers (UPFC), and (IPFC) the Interline Power Flow Controllers [16 - 19]. The two basic collections of FACTS controller have clearly unlike performance and operating characteristics. The thyristor controlled group consists of reactor and capacitor banks with fast solid-state switches in customary series or in the parallel circuit engagements. The thyristor based switches govern the on and off periods of the reactors and fixed capacitor banks and thus comprehend a flexible reactive impedance. The main thing is that except to losses, they can't interchange the real active power to the system. The Voltage source Converters category of FACTS controllers set works self-commutated DC to AC converters, by means of GTO thyristors, or IGBT's who have ability to produce internally inductive reactive and capacitive power to help transmission line for compensation, lacking the use of capacitors/reactors banks. This type of converters with energy storage devices can also interchange real-power with the system, in adding

to the individually manageable reactive power. This VSC can be used consistently to manage transmission lines impedances, voltage and angle by giving reactive shunt compensations, series compensations, and phase shifts, or to manage directly the reactive power and real-power flow in the line [19]. The research article shows a new structure of secondary voltage control idea which can be helpful to the Slovenian power systems is intended. The Slovenian power system has a maximum load of 1700 MW and contains some 30 generating units. They work as an isolated generating corporations, which would in addition to energy, deal the power systems additional services too. Different isolated power systems regarding to generation, it would be of benefit to comprehend the reactive power control systems improved to the group structure. [9]

2.3 Impact of Task Done

The task of this thesis is to model and simulate a three phase D-STATCOM for power quality enhancement. The modulation scheme to be used is SVPWM. The idea of the process is to control the parameters for the good grade output which is done by D-STATCOM. It is the well-known compensation device for the system to control and make good impact on the system.

CHAPTER 3

INVERTERS AND D-STATCOM

3.1 Introduction

High power electrical drives are one of the most working areas in development and research of power electronics devices for the last decade. As the technology advanced the needs of industrial power increased, which pushed in the development of new converter technologies, new semiconductors for power, and different control technologies. Applications of high power requirement with high power semiconductors e.g IGBT's, IGCT's GTO's also have the currents and voltages at high level. At this series of connected semiconductors converters, it is hard to handle. Due to this difficulty and some other problems multilevel inverters family was introduced.

3.2 Multilevel Inverters (MLI's)

Multilevel voltage source inverters are the growing attention in the engineering in the direction of power conversions at intermediate voltage levels for high power applications [20]. Multilevel power converters are being increasing adopted because of their advantages. The applications can be divided into two basic parts; large motor drives and power systems applications. In the power system applications, there are further two categories which are divided into series and shut connected devices. Some of examples are STATCOM [21], [22], UPFC [23], SVC, SSSC and TCRs etc.

3.2.1 Advantages and Disadvantages of MLI's

The MLI's converters are basically array based power semiconductors and the capacitor based voltage sources which generate stepped output waveforms. The process of commutation of switches in inverters allows the summation of voltage levels of capacitors which reach more high voltage level at output as compared to two level inverters. Some of the interesting features of multilevel level inverters are as follows [24].

- MLI's have lower voltage pressure (stress) on switching device.
- Harmonic distortion is very low at output.
- Distortion in current is very less.
- MLI's operate at low switching frequency.
- Electromagnetic interference is less.

There are more advantages of MLI's which can be studied in literature. Beside advantages, the typical disadvantages of MLI's are the large number of power semiconductor switches to deal with, more capacitors involved, multiple DC sources, DC voltage balancing difficulty problem and the complication of control system.

3.2.2 Basic Operating Diagram of MLI

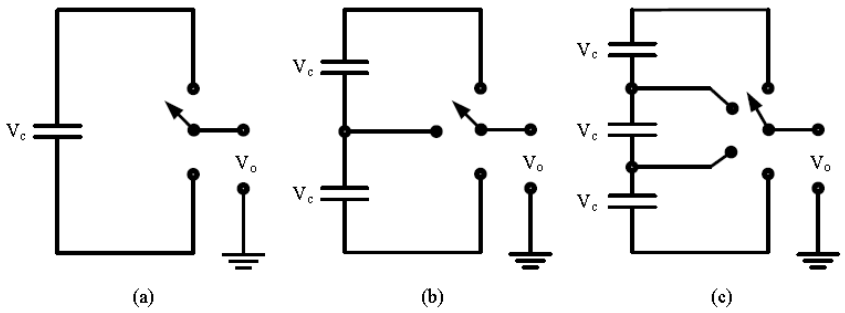

Figure 3.1 Basic operation diagram of MLI's [24]

In figure 3.1 (a) there are two possible output voltage values i.e 0 and Vc. In figure 3.1 (b) b output voltage can have 3 possible values. i.e. 0, Vc and 2Vc. In the figure 3.1 (c) we can see that output voltage can have 4 possible states i.e. 0, Vc, 2Vc, 3Vc. This process can be extended for more levels. Total number of output voltage level shows the level number of inverter. In the figure 3.1 "*n"* is 2, 3, 4 respectively. If "*n*" is greater than 2 then the inverter is said to be MLI inverter.

3.3 Different Topologies for MLI's

Basically there are three main topologies of MLI's

1. Neutral Point Clamped (NPC) (Diode Clamped) [25]
2. Capacitor Clamped (Flying Capacitors) [27]

3. Cascaded H-Bridge (CHB) [29] [26]

Lai *et al* [30] has described the working of all these topologies and explained the detailed comparison in his work. A short overview of these topologies is also explained below.

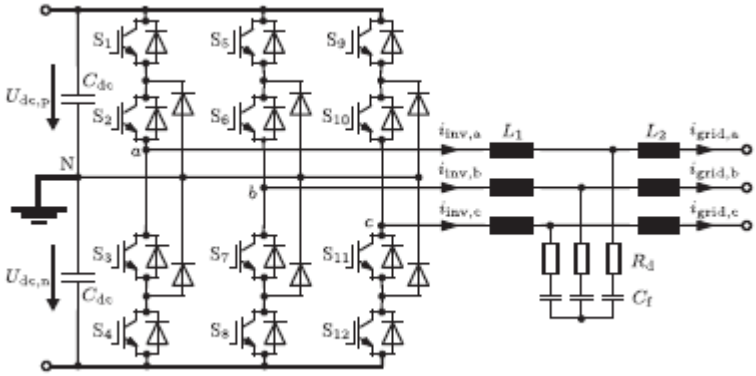

Figure 3.2 Three-phase neutral-point-clamped (3L-NPC) converter [46]

3.3.1 Neutral Point Clamped Topology (NPC)

The Neutral-point clamped topology is shown in figure 3.2, it can also be called as a diode clamped topology. In theory for the NPC inverter "*n*" can be any integer value possible. The main known advantage of this kind of topology is that it needs only one DC source as similar to two level inverter. But the number of power converters increase. The figure 3.2 shows the three levels topology. When "*n*" > 3, diodes in the inverter have different values, form 1/(n-1) to (n-2)/(n-1) times the Vdc. The other main disadvantage of NPC inverters is the fluctuation of its DC-link voltage in capacitors. It becomes a bit difficult to balance DC link voltage when the number of levels are increased as it is shown in the table 3.1.

Table 3.1 The number of components required in NPC topology

Level number	Capacitors no	Switches	Diodes
3	2	12	6
4	3	18	9
5	4	24	12
.	.	.	.
.	.	.	.
.	.	.	.
N	*(n-1)*	*6(n-1)*	*3(n-1)*

3.3.2 Capacitor Clamped Topology

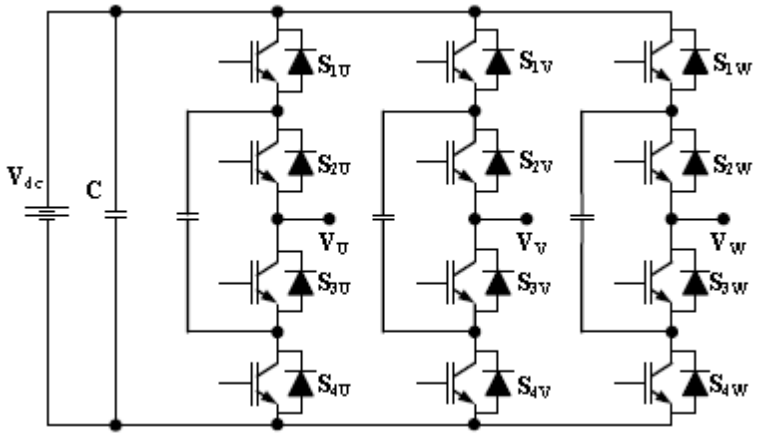

Figure 3.3 Three Levels of capacitor clamped topology [47]

This topology has also second name known as flying capacitor topology. In this topology voltage clamping is done because of flying capacitors at each phase. Figure 3.3 shows the 3-level FC topology. In this topology voltage production is more flexible than the NPC. But this topology also has the voltage balancing problem because of multiple capacitors involved. The highest drawback of this topology is that it needs a huge number of capacitors e.g. for the n-level capacitor clamped inverter needs a least

of *(3n-5)* independent capacitors. The use of large number of bulky capacitors, most of which need pre-charge circuit, along with the voltage balancing problem of its Capacitors inhibit the industrial use of this topology.

3.3.3 Cascaded H-Bridge Topology (CHB)

In this topology, the H-Bridges are added to each other in every phase to increase the number of levels. The output voltage wave is much better as the number of CHB's increase.

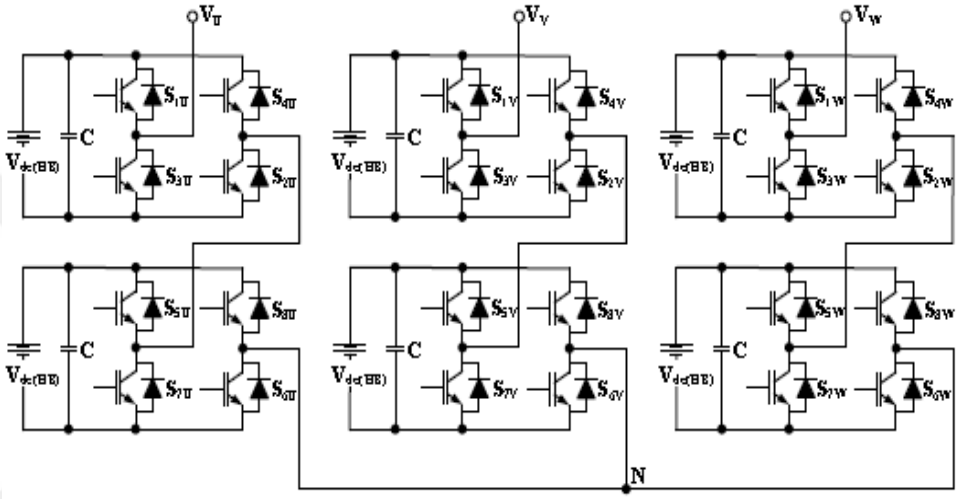

Figure 3.4 Five levels of Cascaded H-Bridge Inverter topology [47]

Figure. 3.4 shows 5-level CHB topology. It involves two alike H-bridges in each phase. In *n*-level topology, *(n-1)/2* identical H-Bridges are used in every phase. Identical H-bridges lead to decrease in cost which is a smart feature of this topology. Though, voltage level varies at every bridge. As it has isolated DC link capacitors so this is the big advantage of this topology, it does not have voltage unbalancing problem.

Table 3.2: Comparison of MLI Topologies

Topologies	Diode Clamped	Flying Capacitors	Cascaded H-Bridges
Number of Power semiconductor switches	*2 (n-1)*	*2 (n-1)*	*2(n-1)*
Number of clamping diodes per phase	*(n-1)(n-2)*	0	0
Number of DC bus/source capacitor	*(n-1)*	*(n-1)*	*(n-1)/2*
Number of balancing capacitors required	O	*(n-1)(n-2)/2*	0
Unbalancing of voltage level	medium	High	low
Use in systems	Motor drive systems , STATCOM	Motor drive systems , STATCOM	Motor drive system , fuel cells, PV, battery systems

3.4 Different Control Techniques for MLI's

Demand for power converters is increasing as the time passes, as of MLI's which are appropriate to high voltage systems, high-power or medium power uses, multilevel converters are drawing the devotion of science researchers. MLI's attain high voltage switching by series of voltage steps with in the rating of electrical power devices. The most significant difficulties in controlling a MLI's is to get a flexible amplitude and sinusoidal output using simple control techniques. Performance of any MLI has an effect on harmonic reduction which depends on switching strategy. In the voltage

source type inverters with multi levels there are different Pulse Width Modulation control structures established and analyzed [2][41].

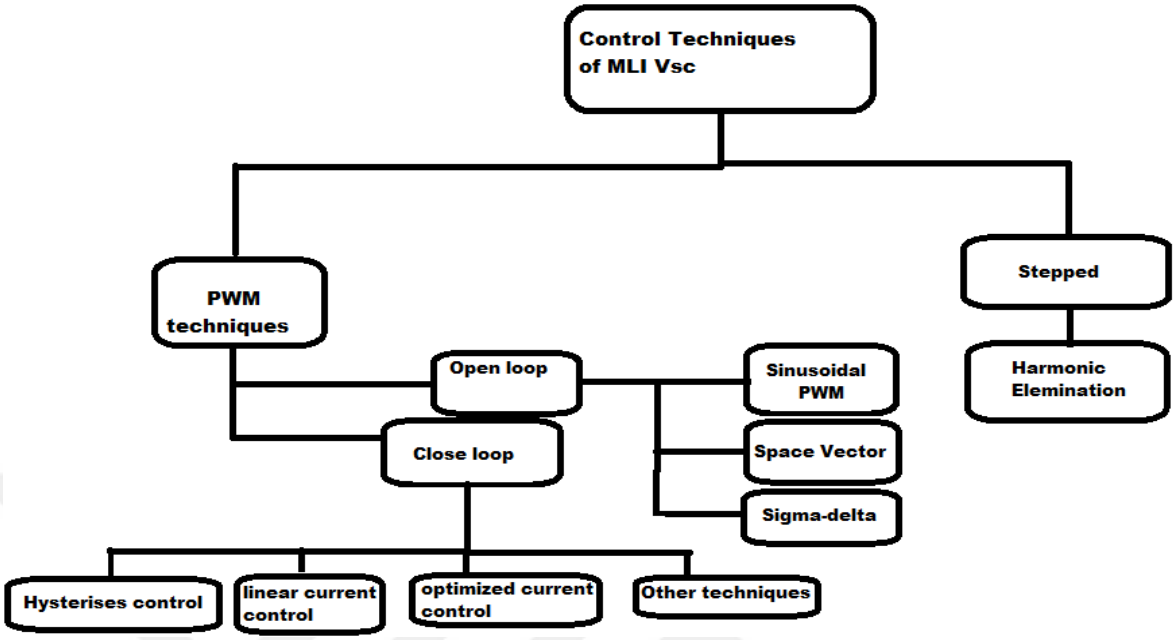

Figure 3.5 control techniques for MLI's

In the figure 3.5 it can be seen that control techniques can be divided into two basic schemes, PWM and Stepped. Further PWM is divided into open and close loop. Here some of the open loop techniques are discussed which are SPWM, SVPWM, and sigma-delta. SPWM can be divided into two forms, modulating and carrier signal. Multicarrier PWM entails the natural sampling of the reference or the modulation signals with carrier signals, normally triangular type waveforms [31]. Further they can be characterized like this:-

- Alternative phase opposition disposition: (APOD) which needs individually of (*n*-1) carriers waveforms for "*n*" levels phase wave to be phase moved from alternative by 180 degree alternatively.
- Phase disposition (PD) is almost same to APOD, just carriers are in phase here.
- Hybrid (H) is the combination of disposition techniques and phase shift multicarrier PWM.

- Phase shifted (PS) technique employs all carriers appropriately phase shifted.

- Super imposed carrier (SIC) is like carrier modulation technique, in this just single carrier signal is used and the amplitude is same as PD method.

For modulating signal SPWM can be ordered according to modulating signal into PSPWM (pure sine), DBPWM (dead band) and THIPWM (third harmonic injection).

- PSPWM is widely accepted technique because of sinusoidal output waveform, in this a triangular wave is matched with sinusoidal reference wave known as modulation signal. [32]

- THIPWM is a method to expand the gain of PWM by injecting third harmonic [33]

- Space vector PWM technique has some advantages with respect to reduced motor losses and ease of generation [34]. In multilevel inverters, space vector modulation (SVM) recognizes every switching state in a complex (α, β) plane. Then a reference phasor revolving in the (α, β) space at the central frequency which is sampled in between the switching period, the next adjacent 3 inverter switching states are chosen by the duty cycles calculated. One of the most significant benefits of SVPWM is that it is also appropriate for digital signal processor (DSP). And it also improves DC bus operation, commutation losses reduces, and total harmonic distortion (THD) is very low. SVPWM is discussed in detail in Chapter 4.

3.5 Power Quality Problems

FACTS devices are used for voltage stabilization, power factor improvement, reactive power compensation and harmonic reduction. There are different types of power quality complications which can effect performance or sometimes they can damage the equipment too. Some of the power quality difficulties/problems are as follows.

- Voltage Sag: It can be defined that the reduction of voltage magnitude due to any fault or it can occur due to the variations in inductive load.

- Voltage swell: This type of power quality problem can occur when the capacitors are energized or if the inductive load is disconnected.

- Voltage harmonics: These are the deviations and distortions in the sinusoidal waveforms of the voltage and current, and mostly caused by rectifiers or non-linear loads.

- Voltage unbalance: It is caused by incorrect distributions of single phase loads. Basically it is variation in magnitude and phase angle of voltage in three phase system.

To solve these kind of power quality problems, FACTS devices are used with the power systems. FACTS are represented by group of power electronics devices. These perform same function like transformer tap changer, phase-shift transformers, reactive compensators etc. Basically FACTS devices can be divided into two parts. Older ones were based on thyristor valve and the latest are the VSC's. According to the connection type FACTS devices, there are two categories, series and shunt connection devices [35]. Basic purpose of parallel/shunt devices is to provide reactive power compensation and voltage support to the lines or loads [36].

3.6 Types of Compensation Devices

According to connection, there are two types of devices. Shunt and series connected devices. Series connection devices are (SSSC) Static synchronous series Compensator, (TCSR) Thyristor controlled series reactor, (TCSC) Thyristor controlled series capacitor, (TSSR) Thyristor switched series reactor (TSSC) Thyristor switched series capacitor. Shunt compensation devices are (STATCOM) and (SVC). In this thesis Statcom is used with SVPWM, which is explained in the related chapter.

3.7 D-STATCOM

D-STATCOM is principally a parallel coupled device which is connected near to distribution side to control the variations caused by load. It has overwhelmed the

synchronous condenser because of its lower cost, improved dynamics, operation and maintenance cost is also lower [37]. D-STATCOM provides as well as absorbs reactive power in AC networks. The VSC controls the interchange of reactive power between the AC system and DC voltage device through the leakage reactance of a transformer. The difference between STATCOM and D-STATCOM is that STATCOM is used at the generation level to control reactive power at generation and to provide voltage support, while D-STATCOM is used at the distribution side near load for voltage control and upgrading of the power factor. It is also helpful in eliminating the total harmonic distortions, voltage sags and swells [38]. Furthermore, it can act like a shunt active filter to reduce voltage and current harmonics.

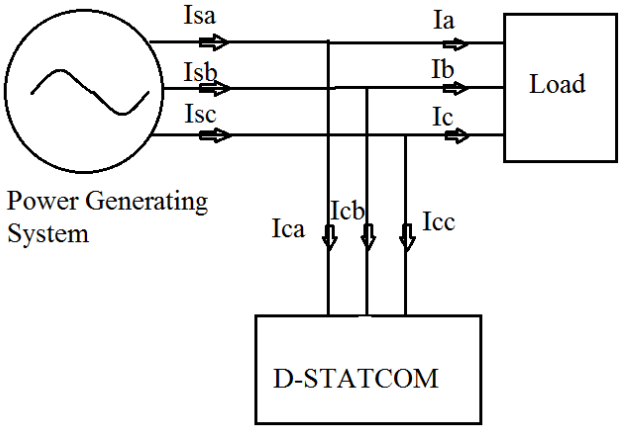

Figure 3.6 Basic structure of D-STATCOM [35]

3.7.1 Components of D-STATCOM

The main components of D-STATCOM are same as the STATCOM. It comprises of a VSC, and a DC source (capacitor or batteries) a filter for reducing the ripples because of switching of power semiconductors, coupling transformer to connect with AC system and the control block for parameters.

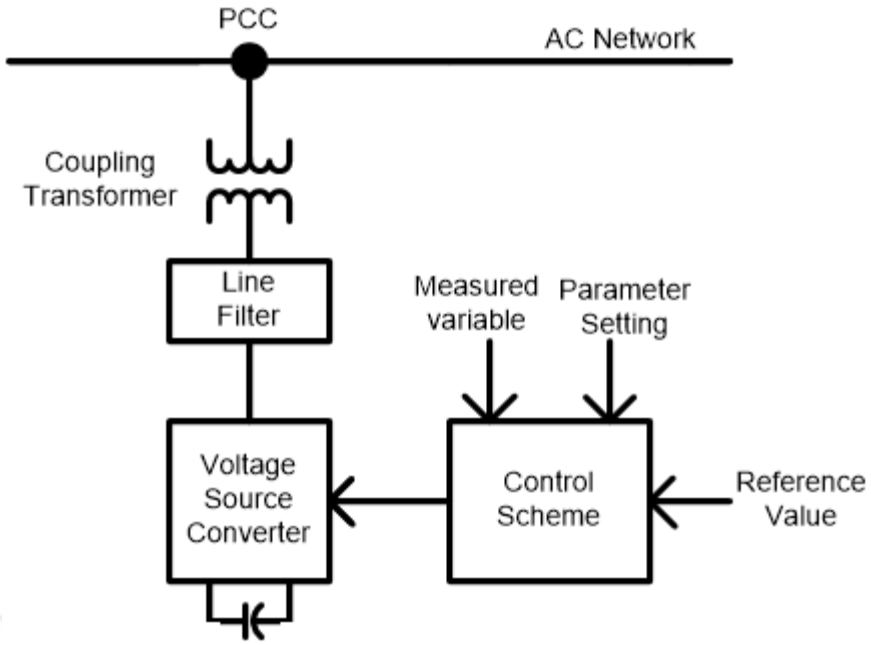

Figure 3.7 Schematic Representation of the D-STATCOM [37]

In the figure 3.7 VSC converts the DC voltage of the DC source in to AC output wave form. This voltage is maintained in a specified phase angle and magnitude to generate the required reactive power. DC source in this D-STATCOM is a capacitor. LC filters are added to eliminate the distortions, and harmonics for reducing the ripples because of the switching of the power semiconductors. Coupling transformers are used to synchronize with AC system through reactance. The control block is a part where fault is detected, or a change in system is detected, voltage sag and swell of system.

3.8 Internal Structure of D-STATCOM

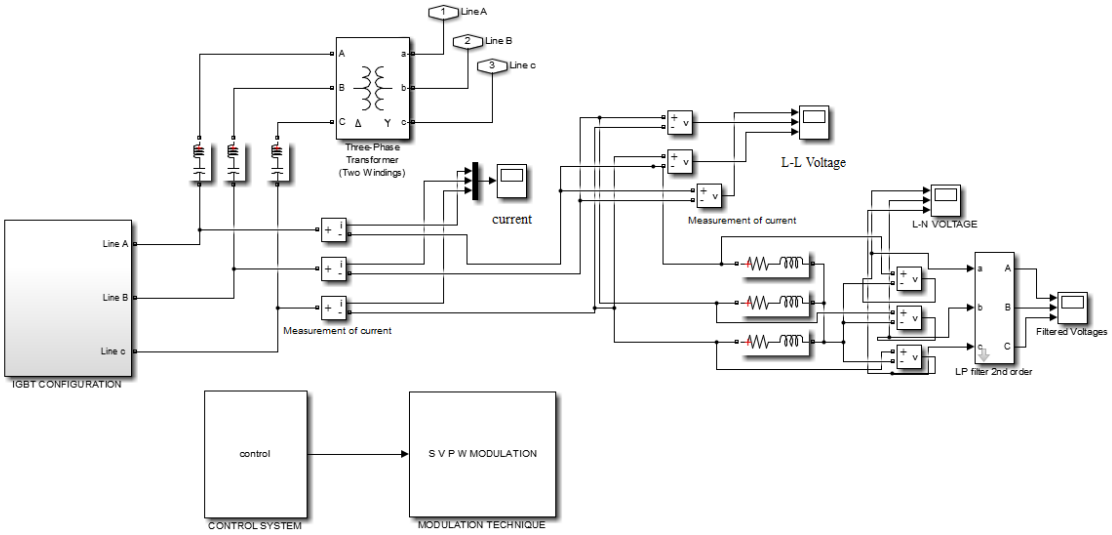

Figure 3.8 Internal structure of D-STATCOM

Inside the D-STATCOM there are three parts, first one is the power inverter type, which is Cascaded H-Bridge. In this electrical power system three level H-Bridge is used. Second part is the Control system of D-STATCOM, which is discussed in Section 3.9. And the third part is the SVPWM part.

3.9 Control System of D-STATCOM

The main task of the controller is to detect the variations in the system due to faults or due to the variations in the load. It also works for computation of parameters, voltages, and generation of the pulses for the converter.

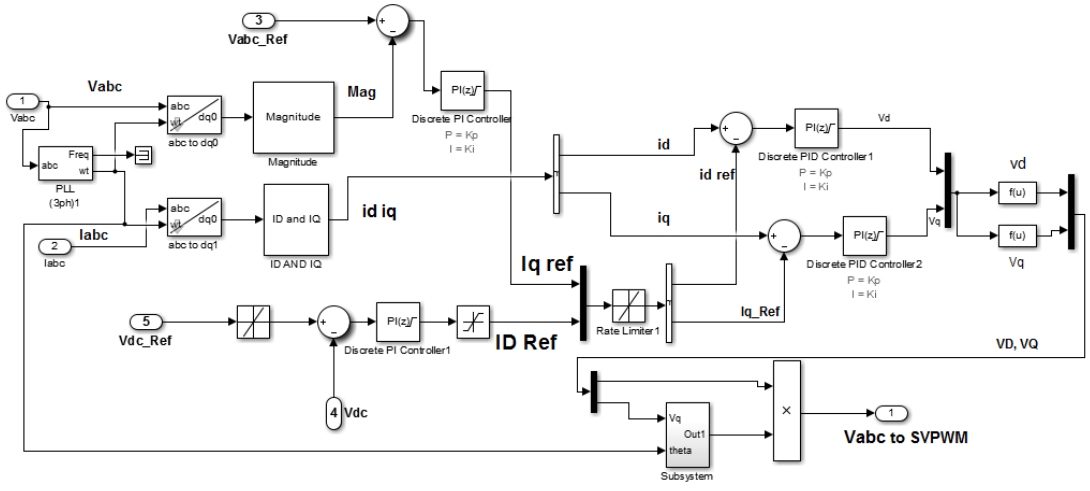

Figure 3.9 Control system for D-statcom

The three phase a, b, c signals of voltage and current are first converted to two-phase DQ frame system with the abc to dq converter. After conversion Vabc gives the magnitude and from the current we get Id and Iq. Then from the magnitude compared with reference Vabc through PI controllers we get Iq_ref. And Id_ ref is obtained by the computation of Vdc_ref and Vdc. Then these are used to obtain Vd and Vq. Which is then converted to Vabc. Results are shown in Chapter 5.

CHAPTER 4

SPACE VECTOR PULSE WIDTH MODULATION

4.1 Introduction to SVPWM

Space vector pulse width modulation (SVPWM) technique is formerly created as a vector style to the normal pulse width modulation technique for the inverters. SVPWM is an alternate method for obtaining the output voltage, little bit better than the ordinary sinusoidal pulse width modulation technique. Normally SVPWM technique is done by rotating the main reference vector around 360^{o} state diagram. Generally this is divided into six main basic sectors and then the sectors are further divided into small parts which will be discussed in detail in this chapter. SVPWM technique is being widely used for lower number of level of inverters. It is bit hard to implement for higher level because this method is very complex at multilevel due to its highly complex computation and calculations.

4.2 Concept of SVPWM.

SVPWM technique involves a vector moving around with constant amplitude and with constant frequency which is obtained from the three phase sinusoidal inputs. The moving vector is rotated in stationary constant d-q coordinate plane and made to replicate its corresponding three phase rotating vector via d-q (2 phase) frame. This whole process is known as 3 phase to 2 phase coordinate transformation system.

In this study full H-bridge inverter topology consisting of four switches for each phase is used to create three-levels of output voltage waveform. Cascaded h-bridge multi-level inverter contains of sequence networks of “n” full h-bridge topology. Figure 4.1 shows the formation of cascaded multilevel inverter. The total output voltage of multi-

level inverters can be given as in equation 4.1: [39]

$$V_0 = V_{out,1} + V_{out,2} + V_{out,3} + \cdots + V_{out,n} \tag{4.1}$$

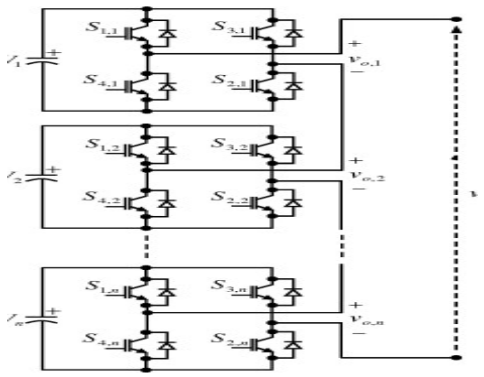

Figure 4.1 Cascaded multilevel inverter [32]

4.3 Principle of SVPWM

The basic model of a general 3 phase voltage source PWM inverters is presented in Figure. 4.2 there are 6 power switches S1 to S6 which give the output levels. These are measured by the switching variables a, a′, b, b′, c and c′. First when the upper first transistor is switched to on, i.e., when a, b or c is 1, the equivalent lower second transistor is switched to off condition, i.e., the equivalent a′, b′ or c′ is 0. Therefore, the "off" and the "on" states of the upper transistors S1, S3 and S5 can be used to conclude the output voltages.

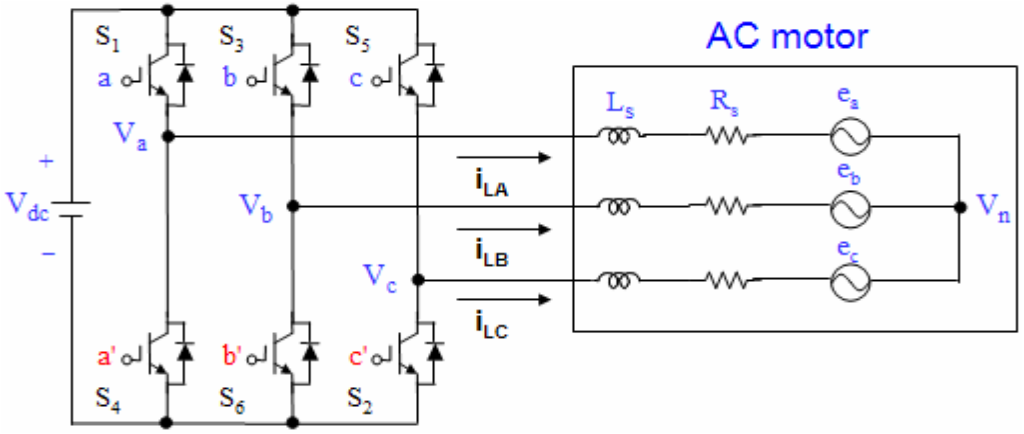

Figure 4.2 General three-phase inverter. [45]

The connection between the variable switching vector [a, b, c]^t and the line-to-line voltage vector [Vab Vbc Vca]^t is given in the following:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{4.2}$$

Also, the connection between the variable switching vector [a, b, c]^t and the phase-voltage vector [Va Vb Vc]^t can be stated below.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{4.3}$$

As shown in equations 4.2 and 4.3 about the transformation which is corresponding to an orthogonal prediction of [a, b, c]^t on the double dimensional vertical to the vector [1, 1, 1]^t (the corresponding d-q space) in a 3-dimension coordinate system. In the result, 2 zero vectors and 6 non zero vectors are probable. 6 working active voltage (V1 to V6) form the border/axes of a hexagonal as portrayed in Fig.4.2. The angle amongst any neighboring 2 non-zero vectors is 60 degrees. In the meantime, 2 zero vectors (V0 and V7) are at the beginning/origin and put on “zero” voltage to the load. These 8 vectors are entitled the basic simple space vectors and are represented by V0 to V7.

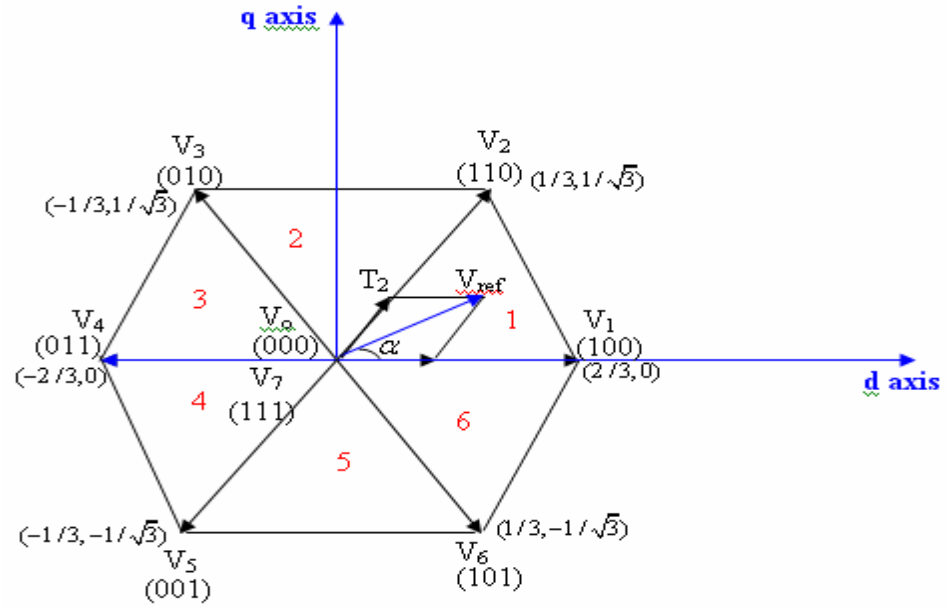

Figure 4.3 Basic 6 sectors and switching vectors [45]

As illustrated in figure. 4.3, total 8 likely groupings or mixtures of "on and off" arrangements for the 3 upper power device switches and combinations of lower power device switches are totally opposed. According to the above matrixes the 8 switching vectors, give phase voltages(line to neutral) at output, and line voltage according to VDC are predicted in Table 4.1 which displays the 8 voltage vectors of inverter from (v0 – v7).

Table 4.1 Switching vectors, phase voltages and output line to line voltages

Voltage Vectors	Switching Vectors			Line to Neutral Voltage			Line to Line Voltage		
	a	b	C	Van	Vbn	Vcn	Vab	Vbc	Vca
V0	0	0	0	0	0	0	0	0	0
V1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V2	1	1	0	1/3	1/3	-2/3	0	1	-1
V3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V4	0	1	1	-2/3	1/3	1/3	-1	0	1
V5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V6	1	0	1	1/3	-2/3	1/3	1	-1	0
V7	1	1	1	0	0	0	0	0	0

The similar conversion can be implemented on the wanted output voltage to get the required reference/orientation voltage vector Vref in two d-q plane. The task of space vector PWM technique is to estimate the reference/orientation voltage vector Vref using the 8 switching forms. One modest technique of calculation is to produce the middling output of the inverter in short periods, T (time) to be the similar as that of Vref in the short period.

4.4 Steps for Implementation of SVPWM

First of the main step is to generate three phase voltage

Where,

$$V_{REF} = V_a + V_b + V_c \tag{4.4}$$

$$V_a = V_m \sin(\omega t) \tag{4.5}$$

$$V_b = V_m \sin\left(\omega t - \frac{2\pi}{3}\right) \tag{4.6}$$

$$V_c = V_m \sin\left(\omega t + \frac{2\pi}{3}\right) \tag{4.7}$$

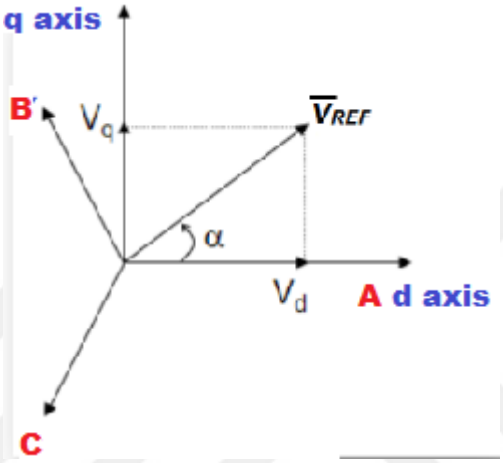

Figure 4.4 Relation of (a b c) to d-q frame

In 2 frame coordinate system V_{REF} will be as

$$V_{ref} = V_d + V_q \tag{4.8}$$

Due to this transformation V_{ref} of three phase is directly converted to 2 phase d-q frame as shown in the above figure.

So

$$V_d = V_a + V_b \cos\left(\frac{2\pi}{3}\right) + V_c \cos\left(\frac{4\pi}{3}\right)$$

$$= V_a - \left(\frac{1}{2}\right) V_b - \left(\frac{1}{2}\right) V_c$$

$$= V_a + \left(\frac{1}{2}\right) V_b$$

$$= \left(\frac{3}{2}\right) V_a \tag{4.9}$$

$$V_q = V_a \cos\left(\frac{3\pi}{2}\right) + V_b \cos\left(\frac{\pi}{6}\right) + V_c \cos\left(\frac{5\pi}{6}\right)$$

$$= 0 - \left(\frac{\sqrt{3}}{2}\right) V_b - \left(\frac{\sqrt{3}}{2}\right) V_c$$

$$= \left(\frac{\sqrt{3}}{2}\right)(V_b - V_c) \tag{4.10}$$

And in Matrix form as,

$$\begin{bmatrix} \overrightarrow{V_d} \\ \overrightarrow{V_q} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{4.11}$$

After this Vref magnitude and its respective angle (α) is calculated.

$$\overrightarrow{V_{ref}} = \overrightarrow{V_d} + \overrightarrow{jV_q} = \sqrt{\overrightarrow{V_d{}^2 + V_q{}^2}} \tag{4.12}$$

$$\alpha = \tan^{-1}\left(\frac{\overrightarrow{V_q}}{\overrightarrow{V_d}}\right) \tag{4.13}$$

This “α” is used to recognize the sector of in which the orientation voltage vector is moving. This is an important part of SVPWM because according to the sector the corresponding switching sequence and switching time is calculated. The pointing of sector where reference voltage vector is situated is simple because of angle identification. Depending on the reference angle, voltage sectors can be found as per the table given below.

Table 4.2 Estimation of sectors according to rotating vector

Sector no	Degree
i.	$0<\alpha\leq 60^{o}$
ii.	$60^{o}<\alpha\leq 120^{o}$
iii.	$120^{o}<\alpha\leq 180^{o}$
iv.	$180^{o}<\alpha\leq 240^{o}$
v.	$240^{o}<\alpha\leq 300^{o}$
vi.	$300^{o}<\alpha\leq 360^{o}$

Now next step to determine duration time T1, T2, T0

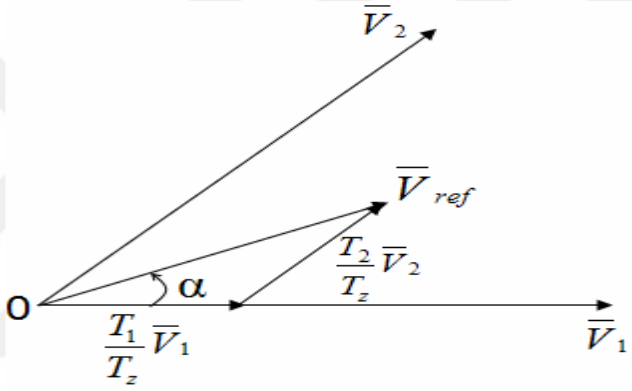

Figure 4.5 Reference voltage vector as of adjacent vectors in the sector 1

For calculation of switching time in sector 1 is given as follows:

$$\int_0^{T_z}\bar{V}_{ref}=\int_0^{T_1}\bar{V}_1dt+\int_{T_1}^{T_1+T_2}\bar{V}_2dt+\int_{T_1+T_2}^{T_z}\bar{V}_0$$

$$\therefore T_z\,.\bar{V}_{ref}=(T_1\,.\bar{V}_1+T_2\,.\bar{V}_2)$$

$$\Longrightarrow T_z\,.\left|\bar{V}_{ref}\right|.\begin{bmatrix}\cos\alpha\\ \sin\alpha\end{bmatrix}=T_1\,.\,\frac{2}{3}\,.\,V_{dc}\,.\begin{bmatrix}1\\0\end{bmatrix}+T_2\,.\,\frac{2}{3}\,.\,V_{dc}\,.\begin{bmatrix}\cos(\frac{\pi}{3})\\ \sin(\frac{\pi}{3})\end{bmatrix}\qquad(4.14)$$

$$(where, 0\leq\alpha\leq 60^{0})$$

$$\therefore \mathrm{T_1}=\mathrm{T_z}\,.\,\mathrm{a}\,.\,\frac{\sin(\frac{\pi}{3}-\alpha)}{\sin(\frac{\pi}{3})}\qquad(4.15)$$

$$\therefore T_2 = T_z \,.\, a \,.\, \frac{\sin(\alpha)}{\sin(\frac{\pi}{3})} \tag{4.16}$$

$$\therefore T_0 = T_z - (T_1 + T_2), \left(where, T_z = \frac{1}{f_z} \; and \; a = \frac{|\overline{V}_{ref}|}{\frac{2}{3}V_{dc}} \right) \tag{4.17}$$

For general switching time calculation at any given sector can be given by [42]

$$\therefore T_1 = \frac{\sqrt{3} \,.\, T_z \,.\, |\overline{V}_{ref}|}{V_{dc}} \left(sin\frac{\pi}{3} \; \alpha + \frac{n-1}{3}\pi \right)$$

$$= \frac{\sqrt{3} \,.\, T_z \,.\, |\overline{V}_{ref}|}{V_{dc}} (sin\frac{n}{3}\pi - \alpha)$$

$$= \frac{\sqrt{3} \,.\, T_z \,.\, |\overline{V}_{ref}|}{V_{dc}} (sin\frac{n}{3}\pi \; cos\alpha - cos\frac{n}{3}\pi \; sin\alpha) \tag{4.18}$$

$$\therefore T_2 = \frac{\sqrt{3} \,.\, T_z \,.\, |\overline{V}_{ref}|}{V_{dc}} (\sin(\alpha - \frac{n-1}{3}\pi))$$

$$= \frac{\sqrt{3} \,.\, T_z \,.\, |\overline{V}_{ref}|}{V_{dc}} (-cos\alpha \,.\, sin\frac{n-1}{3}\pi + sin\alpha \,.\, cos\frac{n-1}{3}\pi) \tag{4.19}$$

$$\therefore T_0 = T_z - T_1 - T_2, \begin{pmatrix} where, n = 1 \; through \; 6 \; (that \; is \; sector \; 1 \; to \; 6) \\ 0 \leq \alpha \leq 60^0 \end{pmatrix}$$

The Space Vectors chosen and the times for switching are planned, the next level stage is to organize probable orders for switching. Normally the switching order scheme for any specified Vref is not specific, but it should meet the main two necessities to reduce the device switching frequency [43].

a) The changeover from one switching value to the succeeding should involve only 2 switches in the same inverter phase/leg, one being switched “ON” and other should be switching “OFF”.

b) The change of V*ref* stirring from one sector in the space vector plan to the next needs no or least number of switches.

The next step is to conclude the switching time of each transistor (S1 to S6)

Table 4.3 Switching time calculation for sectors.

Sector	Upper switches (S_1, S_3, S_5)	Lower switches (S_4, S_6, S_2)
1	$S_1 = T_1 + T_2 + T_0/2$ $S_3 = T_2 + T_0/2$ $S_5 = T_0/2$	$S_4 = T_0/2$ $S_6 = T_1 + T_0/2$ $S_2 = T_1+T_2+T_0/2$
2	$S_1 = T_1 + T_0/2$ $S_3 = T_1 + T_2 + T_0/2$ $S_5 = T_0/2$	$S_4 = T_2 + T_0/2$ $S_6 = T_0/2$ $S_2 = T_1+T_2+T_0/2$
3	$S_1 = T_0/2$ $S_3 = T_1 + T_2 + T_0/2$ $S_5 = T_2 + T_0/2$	$S_4 = T_1+T_2+T_0/2$ $S_6 = T_0/2$ $S_2 = T_1 + T_0/2$
4	$S_1 = T_0/2$ $S_3 = T_1 + T_0/2$ $S_5 = T_1 + T_2 + T_0/2$	$S_4 = T_1+T_2+T_0/2$ $S_6 = T_2 + T_0/2$ $S_2 = T_0/2$
5	$S_1 = T_2 + T_0/2$ $S_3 = T_0/2$ $S_5 = T_1 + T_2 + T_0/2$	$S_4 = T_1 + T_0/2$ $S_6 = T_1+T_2+T_0/2$ $S_2 = T_0/2$
6	$S_1 = T_1 + T_2 + T_0/2$ $S_3 = T_0/2$ $S_5 = T_1 + T_0/2$	$S_4 = T_0/2$ $S_6 = T_1+T_2+T_0/2$ $S_2 = T_2 + T_0/2$

Single phase cascaded multi-level converter topologies are generally described as below.

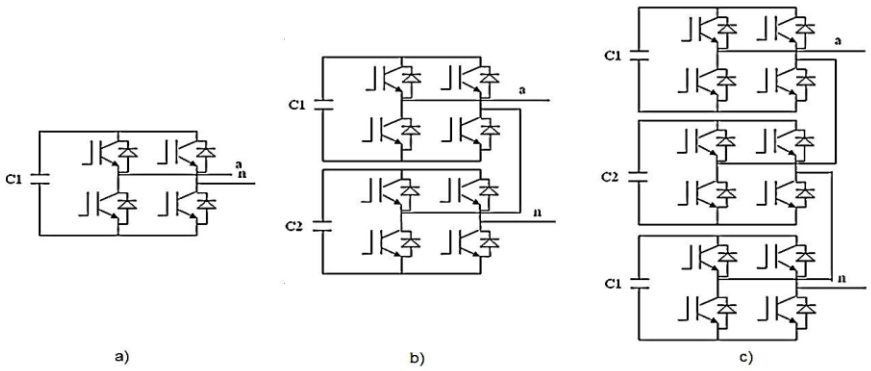

Figure 4.6 Single phase cascaded 3 level (a), 5 level (b), 7 level (c) inverter topologies respectively.[40]

Three phase of cascaded H Bridge inverter topology is shown below in figure 4.6

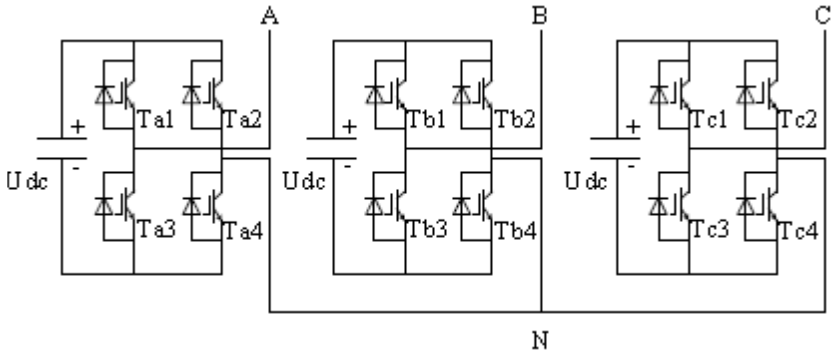

Figure 4.7 Three phase Cascaded H Bridge [40]

The basis six sectors are from V1 to V6 are always same in any number of levels. The difference in levels brings in the complexity of switching vectors. As the number of switching state vectors increase the difficulty level of implementation in SVPWM increases. Locating a Vref voltage vector in increasing number of levels is difficult. We can estimate the switching vectors by (n^3). Where "n" is the number of levels. [44] [45]

E.g. For 2 levels SVPWM we will have (2^3) = 8 switching states.

For 3 levels SVPWM we will have (3^3) = 27 switching states.

For 5 levels SVPWM we will have (5^3) = 125 switching states.

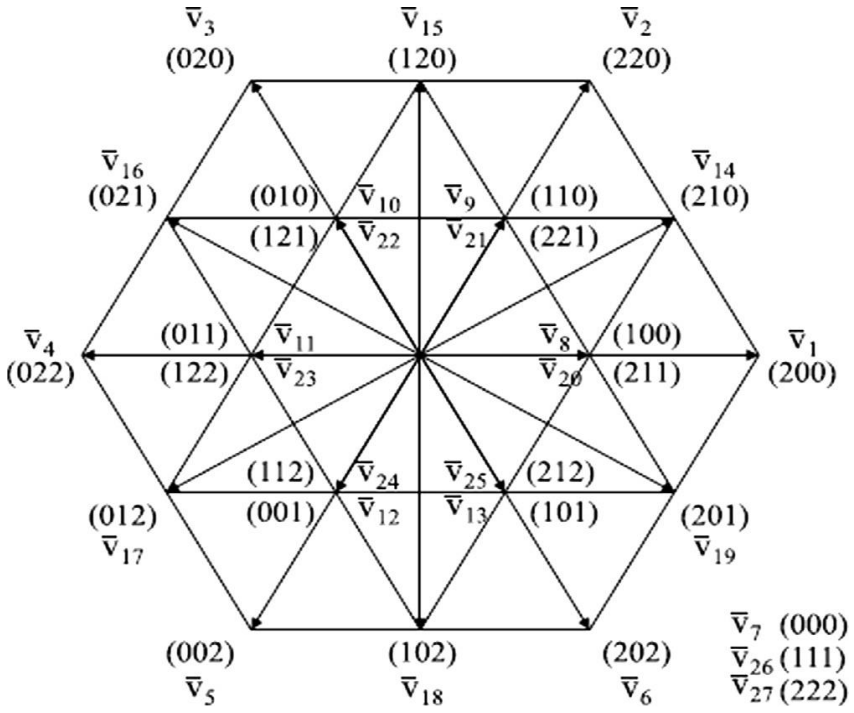

Figure 4.8 Basis switching states of 3 level SVPWM

Calculation of switching time interval is same like 2 levels of SVPWM.

In the figure above we have 27 number of switching states (3^3=27). Vector V7, V26 and V27 are at origin with zero magnitude.

The general representation of space voltage vectors can be expressed as shown in fig 4.8.

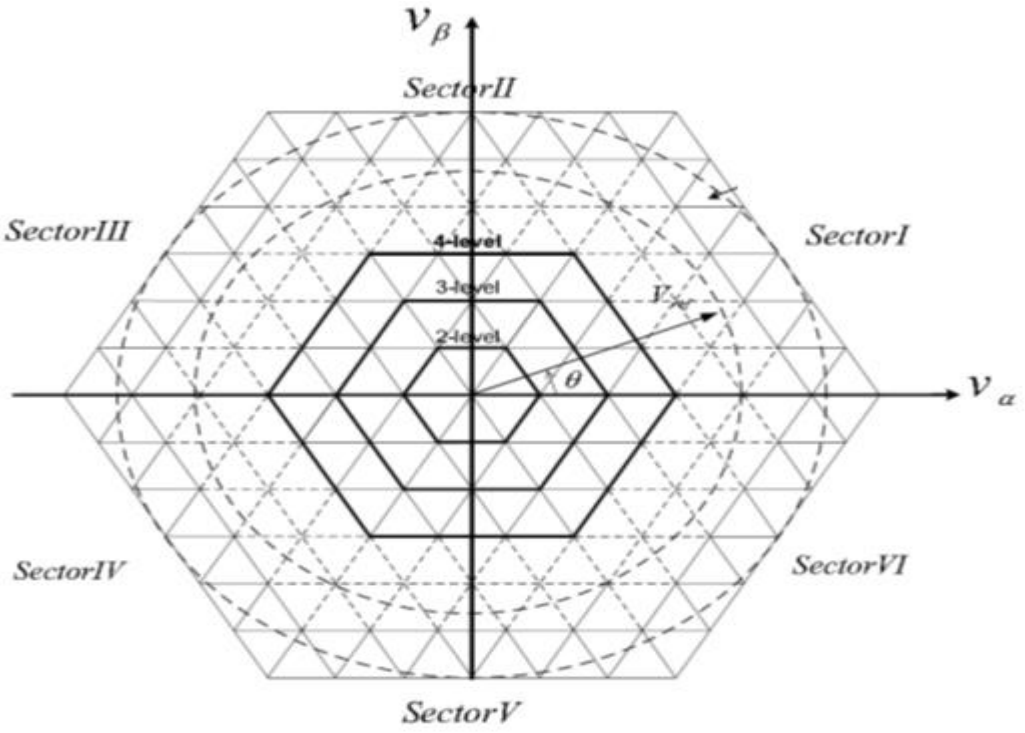

Figure 4.9 The general diagram of multi-level Space Voltage vector

CHAPTER 5

CASE STUDIES AND SIMULATION RESULTS

5.1 Simulation Model

The modulation and simulation of the power system has been implemented using a computer software. Firstly three phase generation system is made with the help of programmable voltage source and it is connected with the three wire transmission system which has been connected to the load. Between the generation of power and the load, a transformer is connected with D-STATCOM, for the power flow control. The total number of three busses are used. The whole simulation model is shown in figure 5.1.

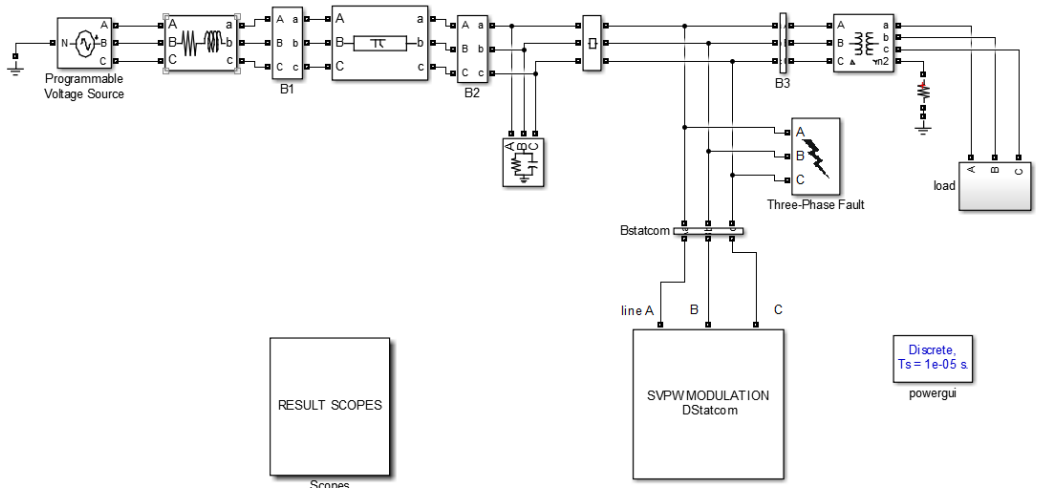

Figure 5.1 Main simulation model of system

5.2 D-STATCOM Analysis and Behavior

In this case study results are analyzed while reference voltage is kept at 1pu and Vdc is at 2600. These are the rated values of the system. Set points variations for the programmable voltage source are between 0 - 10%.

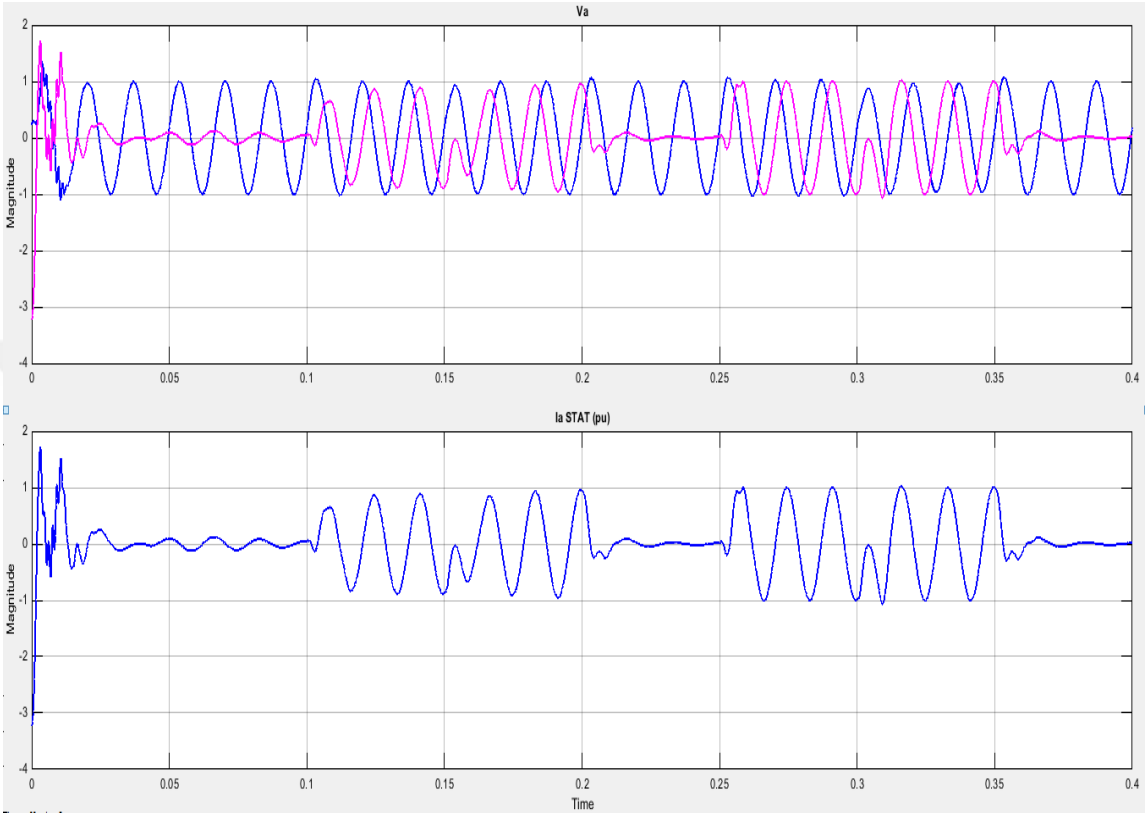

Figure 5.2 Voltage and Current of D-STATCOM

Figure 5.2 shows the phase A voltage and variation of current of the D-STATCOM. In this test the load is kept at constant value so that there should be no effect on the system by the variation of load. To check D-STATCOM behavior some step changes to the voltage are applied at the generator side and they are between 0 to 10%. Vref and the voltage at B3 are initially set at 1pu, so that there should be no difference and D-STATCOM should not react to the system. When the step change is applied at 0.1s as an increment in per unit value, D-STATCOM detects the difference to the reference and performs accordingly, which is shown in the figure 5.3.

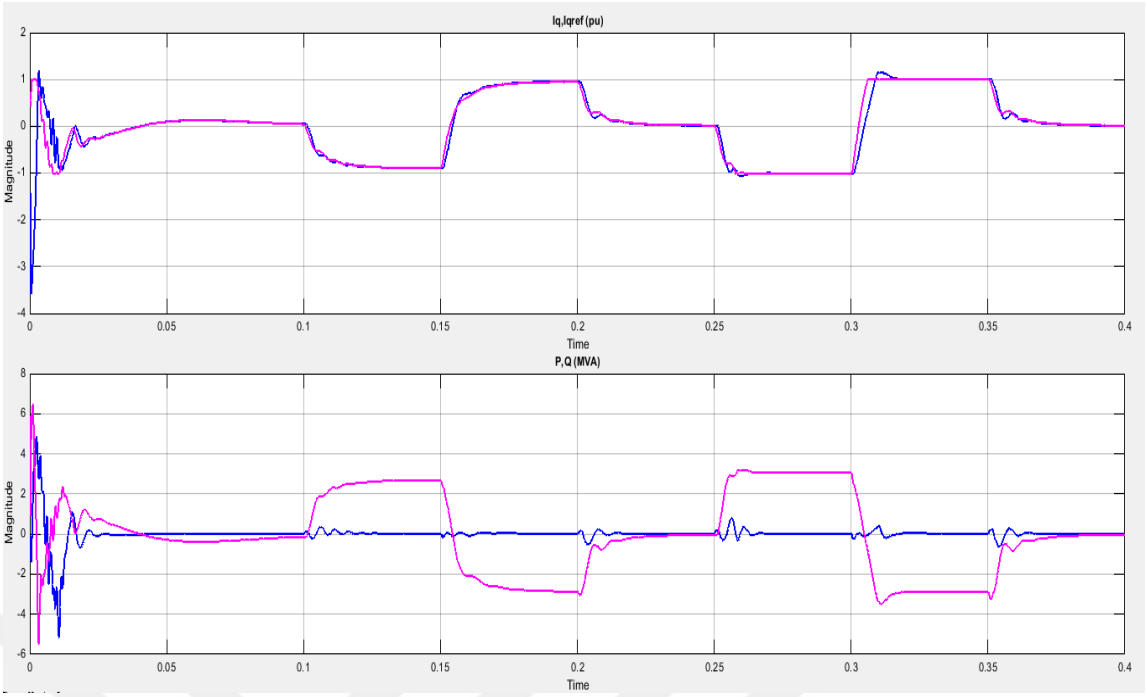

Figure 5.3 Id and Iq (ref) and P, Q (MVAR) injected

From Figure 5.3, it can be seen that when the system generation and reference voltage are same there is no interaction of D-STATCOM. But at time t=0.1s when the generation voltage is increased from the reference voltage the D-STATCOM reacts by absorbing the reactive power to keep it stable. Until voltage of source is more than reference voltage, D-STATCOM keeps absorbing the reactive power. As it can be seen that during the absorption of reactive power Id and Iqref are negative and the injected power Q is in positive nearly to the +2.5MVAR. When the system voltage is set under the reference voltage at t=0.15 it can be seen that Id and Iq change from negative to positive. This explains that system needs reactive power to maintain Vref at 1pu value. The reactive power also changes and value is nearly -2.5MVAR.

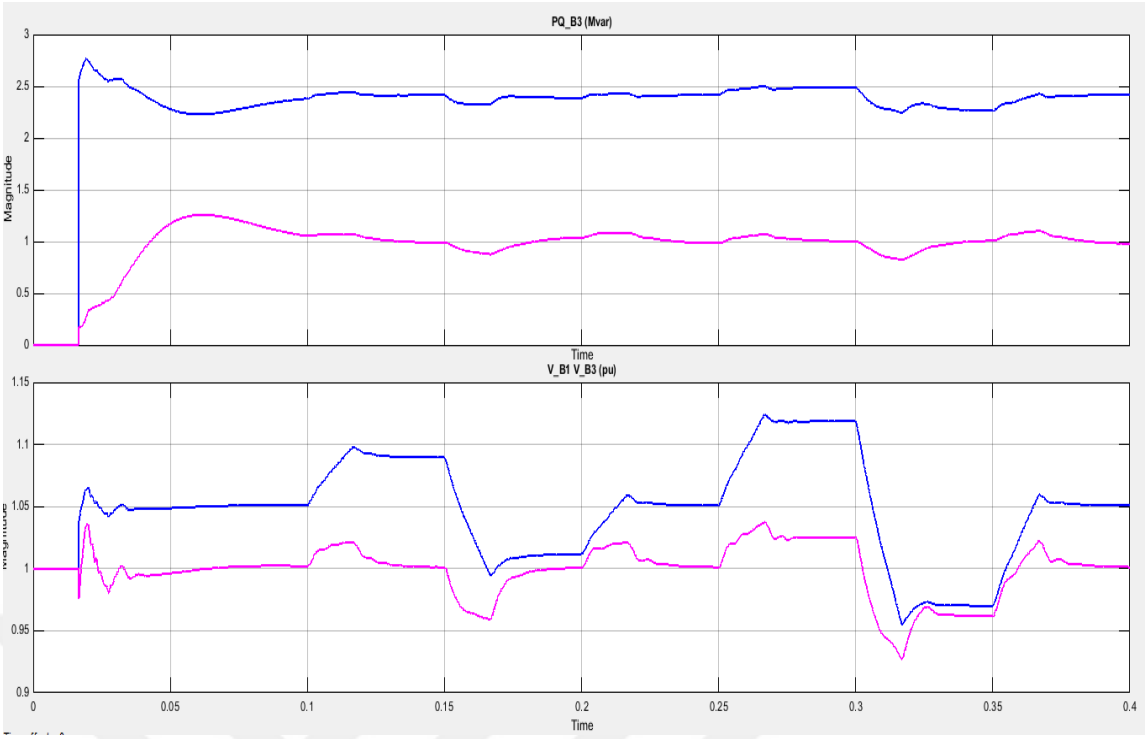

Figure 5.4 (a) P, Q of Bus 3 (b) Voltage of Bus 1 and Bus 3

Figure 5.4 shows the parameter Bus 3 which is connected to the load. It is shown that the power at the Bus 3 is almost stable due to the correction of D-STATCOM. The second graph shows the voltage of Bus 1 compared to the voltage of Bus 3. As it was stated in the figure 5.4 that the voltage levels were set to be 1pu it can be seen in the figure 5.4 that Bus 1 and Bus 3 start at 1pu.

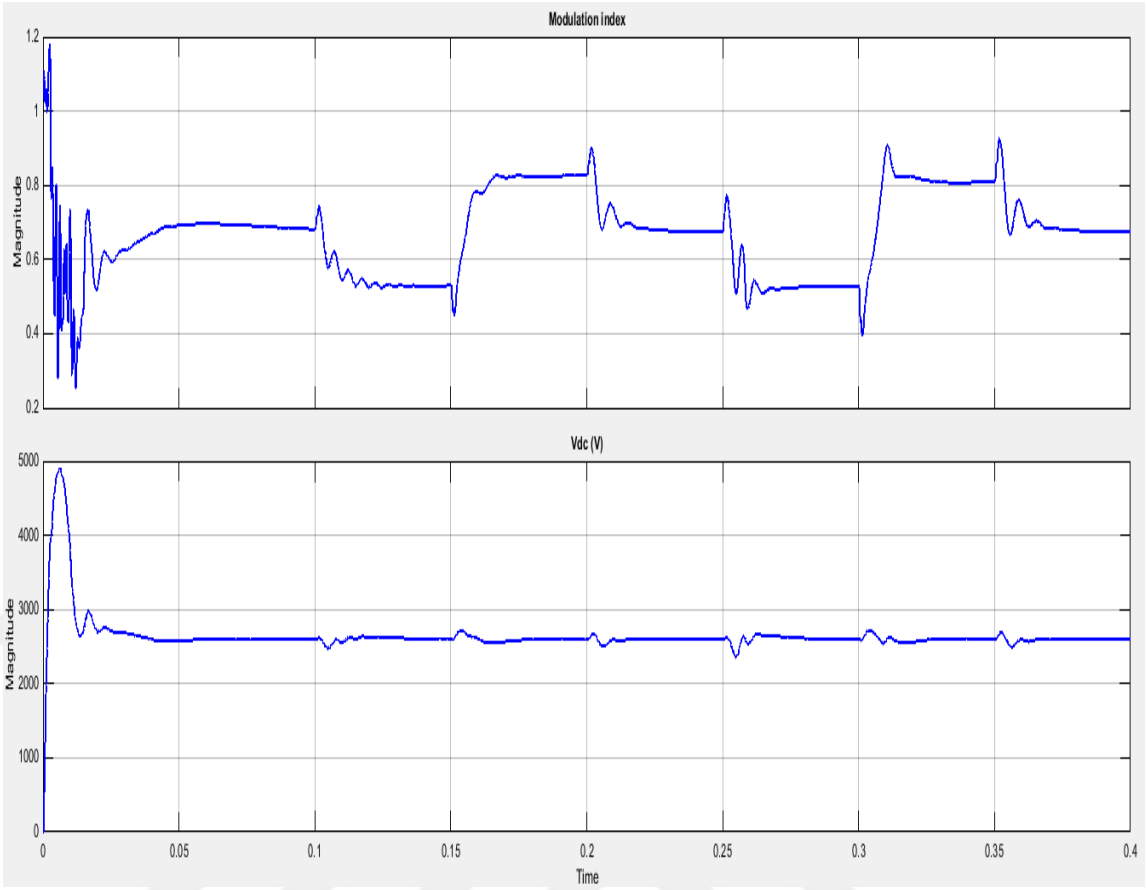

Figure 5.5 (a) Modulation index (b) Vdc of system =2600

Figure 5.5 shows the variation in modulation index with respect to time. It can be seen during the increment of source voltage form t = 0.1 to t=0.15 the modulation index decreases. And when the source voltage decreases form set value the modulation index increases. Vdc is set to be at 2600V and it can be seen almost stable.

Figure 5.6 shows the five levels of line to neutral (phase) voltage of space vector pulse width modulation based output of D-STATCOM.

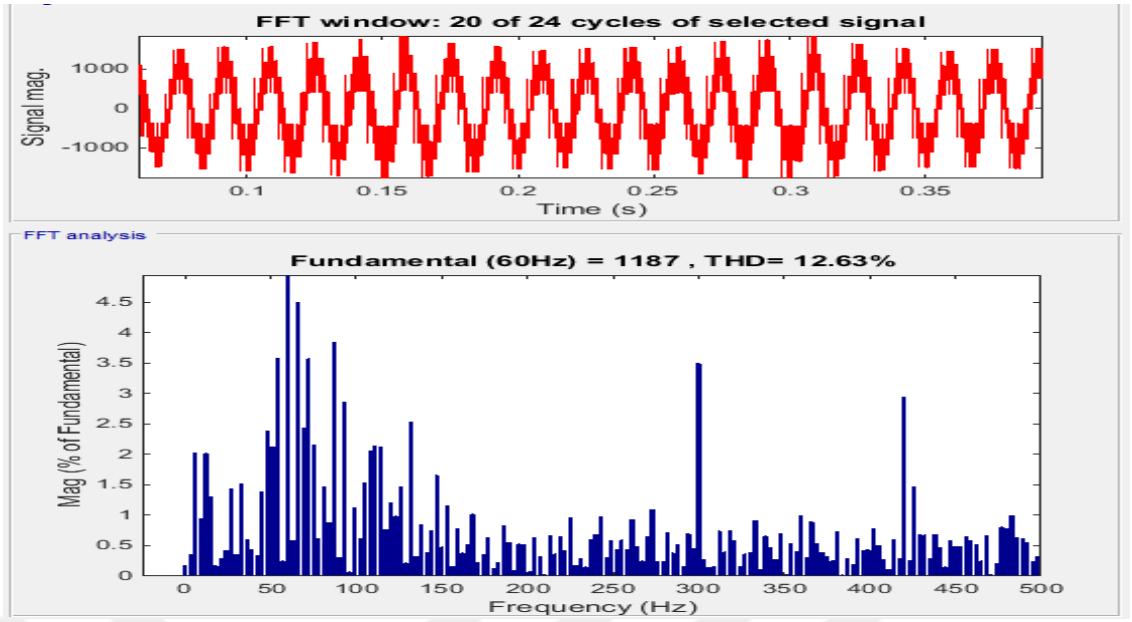

Figure 5.6 (a) Line-to-neutral voltage of SVPWM (b) THD of line to neutral voltage of SPVWM

Figure 5.7 shows the three levels of Line to line voltage of the SVPWM output and its THD.

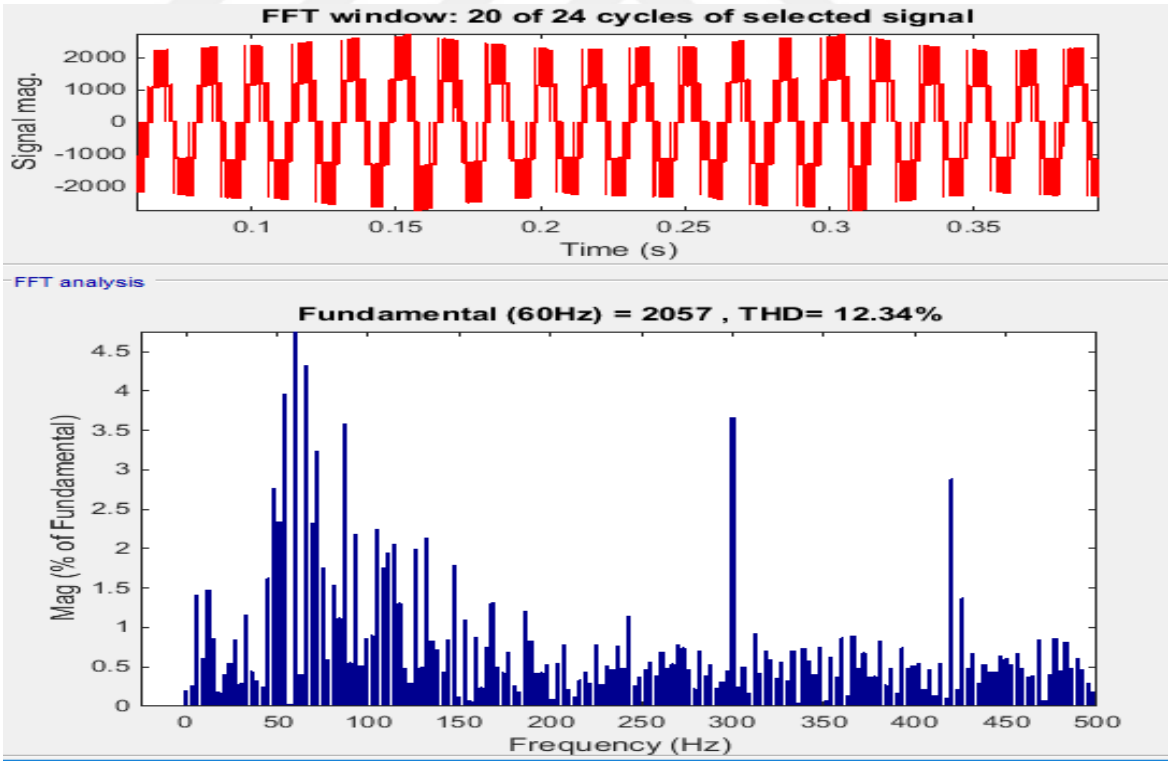

Figure 5.7 (a) three level line to line voltage of SVPWM (b) THD for line to line voltage

5.3 Case study 1: Behavior of system without D-Statcom

Figure 5.8 shows the test of simulation without D-STATCOM. In this test D-Statcom is bypassed to analyze the response of system at Bus 3 on distribution side,

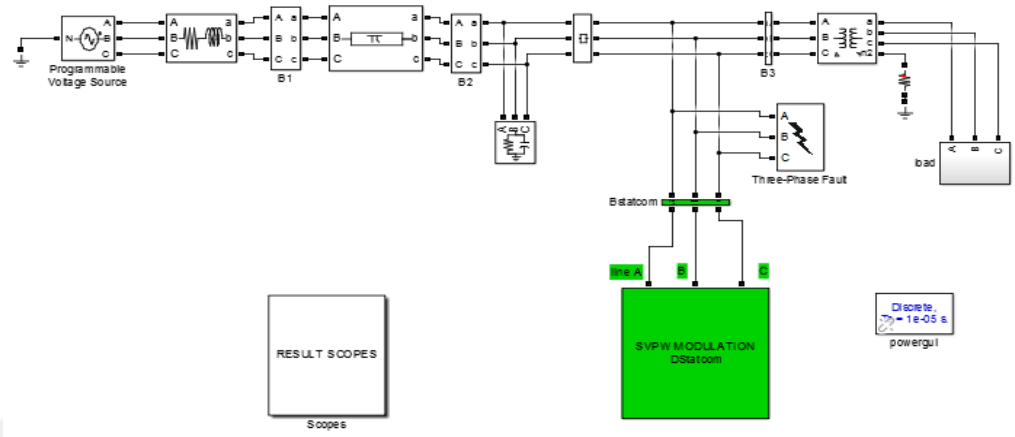

Figure 5.8 System when D-statcom is bypassed

In figure 5.8 Vref is as usual set to 1pu and Vdc is 2600v and small step changes are applied at generation side to check the behavior at distribution side.

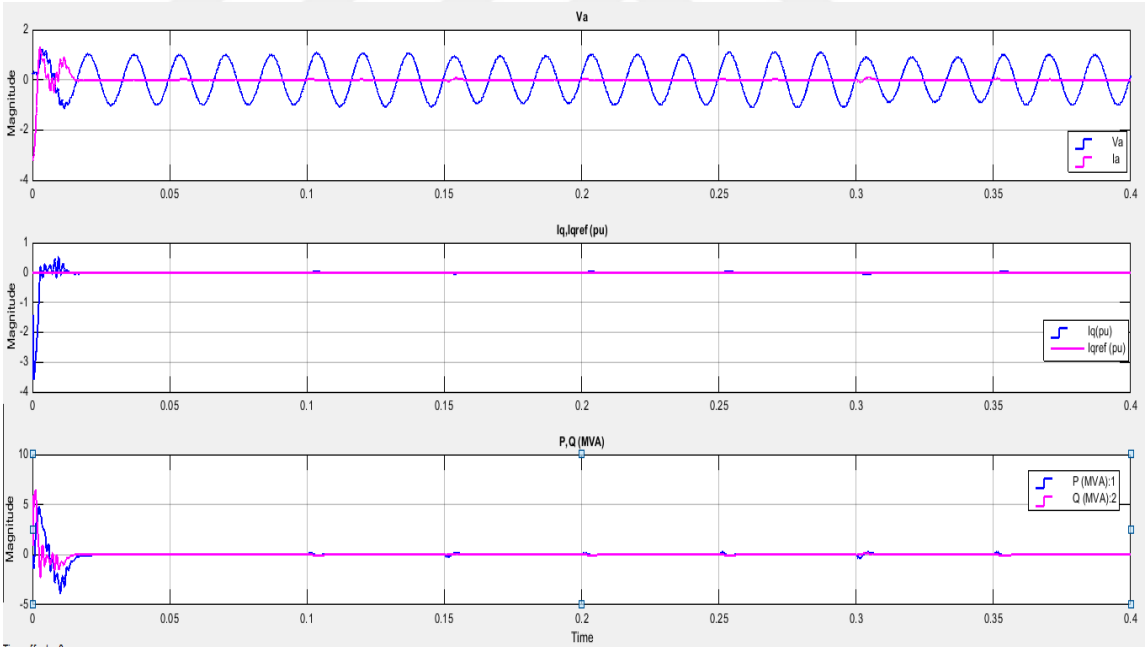

Figure 5.9 (a) Voltage and current of D-STATCOM (b) Iq and Iq (ref) of D-STATCOM (c) P, Q of the D-STATCOM

In Figure 5.9 (a) it can be seen that when there is no compensation device connected then there is no current flow in the D-STATCOM. Pink line shows that there is no

current flow. In Figure 5.9 (b) and (c) graphs Id and Iq (ref) and the injected Power Q of D-STATCOM are at zero, because compensation device is bypassed.

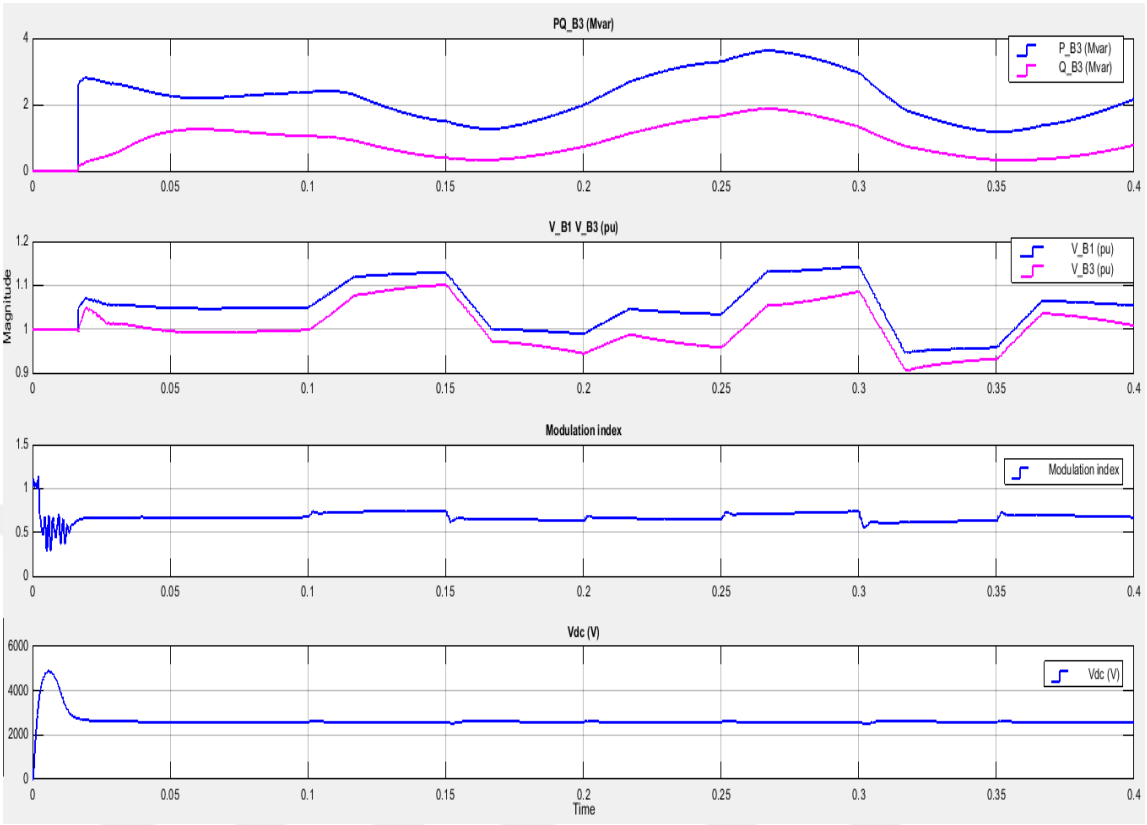

Figure 5.10 (a) Bus_3 P, Q (Mvar) (b) Comparison of Bus 1 Voltage and Bus 3 (c) Modulation index

Figure 5.10 (a) and (b) shows that system response is not good, it has big variations. Power P, Q at bus 3 is not stable because system has no compensation device. The last graph shows the modulation index which is also below the level.

5.4 Case Study 2: When Vref is more than 1pu

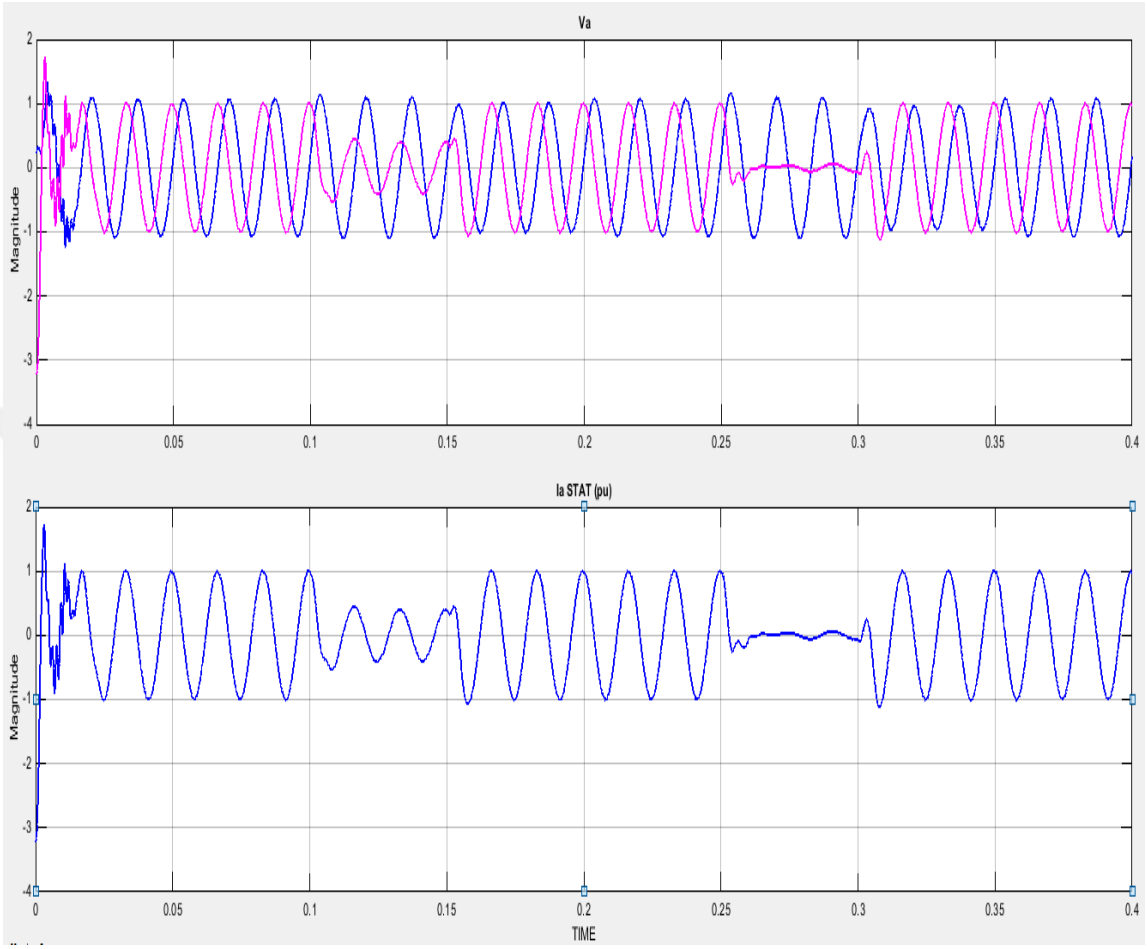

Figure 5.11 voltage and current of Statcom at Vref > 1pu

In figure 5.11 Voltage and current are shown. As we can see that in this figure statcom is operating from the start. But in figure 5.2 at t=0.02s statcom current was close to zero, because Vref was (1) equal to the per unit value. So Statcom did not react to absorb or to provide power. Here in this case study the set points from t=0 to t=0.1 are set to 1pu, but as we increased the Vref 09% from 1pu the statcom detects the difference and compensates.

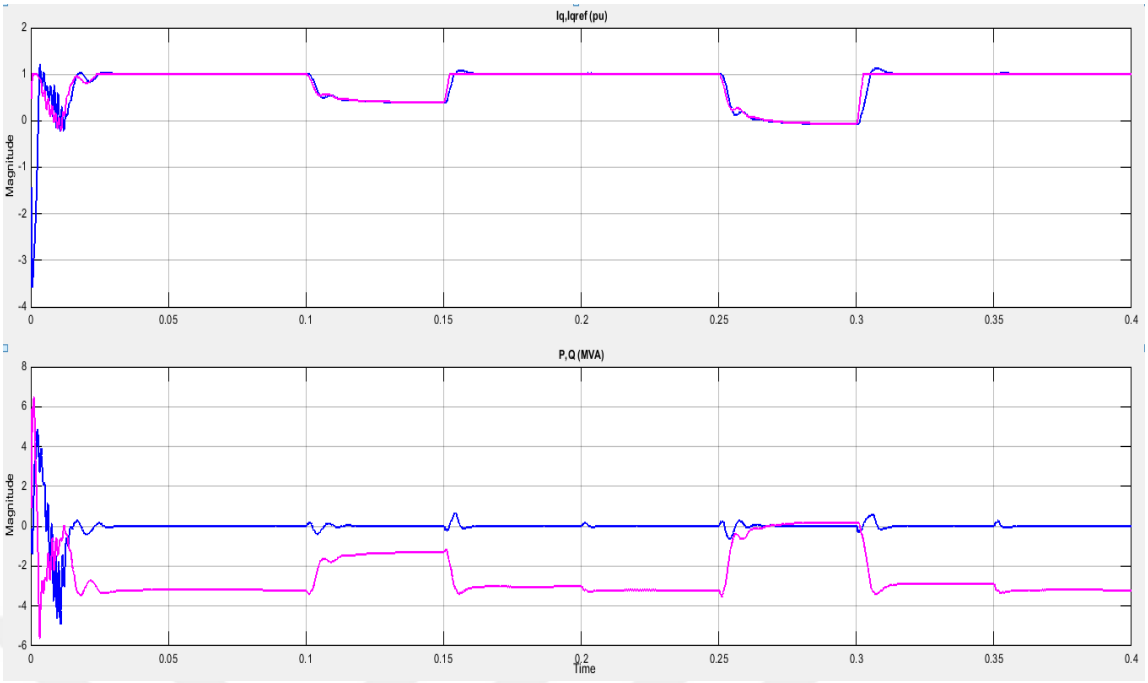

Figure 5.12 (a) Id and Iq pu of D-statcom (b) P, Q of D-statcom

Figure 5.12 shows that up to t=0.1s Id and Iq are at 1pu value because of difference in generating set point and given Vref. At t=0.15s when the set point value is increased 06% from 1pu we can observe that the difference decreased between Vref and set point. When the difference is low D-STATCOM generates less reactive power and id and iq comes close to zero form 1pu value. At t=0.25 when the difference in set point at generation side and the given Vref are same to each other, the Id and Iq ref are at zero. Actually here from t=0.25 to t=0.3 Vref and generation set point are equal, so D-statcom neither absorbs nor provides the reactive power which can be seen in the graph b. As it can be seen that the Q is in negative from the start which means D-statcom is continuously generating the Reactive power.

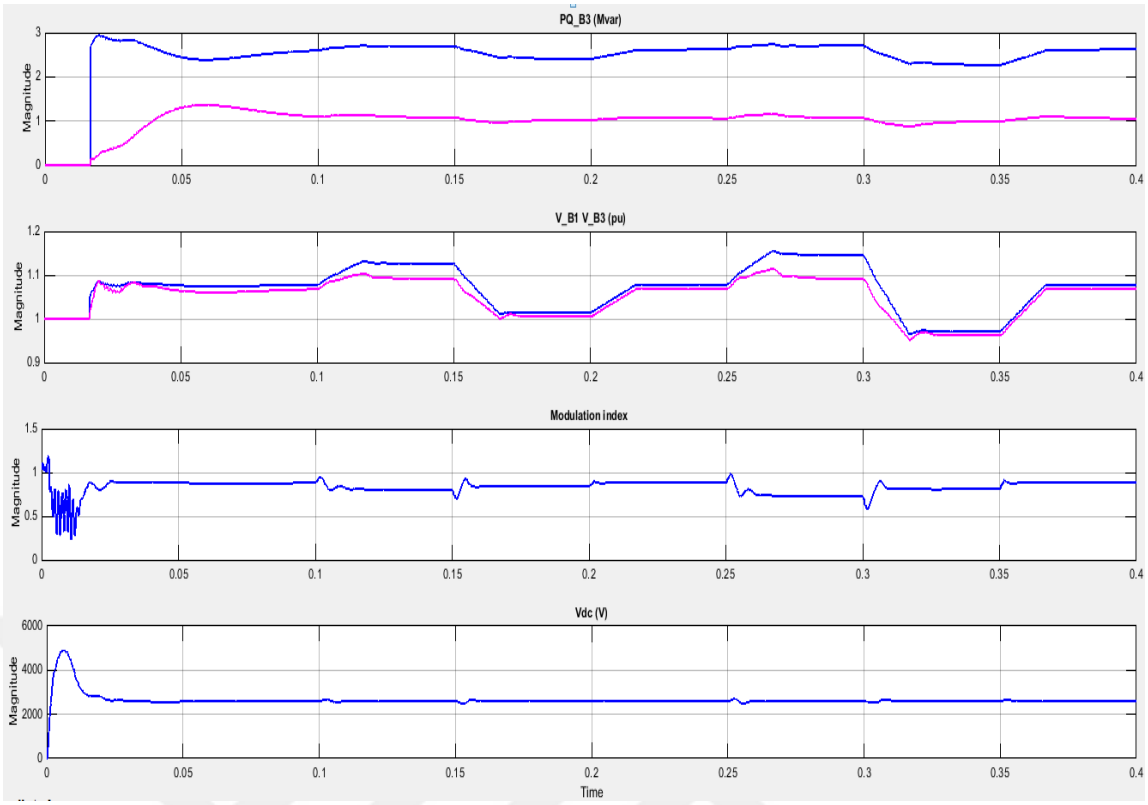

Figure 5.13 (a) power P and Q of Bus 3 (b) voltage comparison to Bus 1 and Bus 3

(c) Modulation index (d) Vdc with respect to time

Figure 5.13 (a) shows that the system is working properly in stable mode, even when Vref is increased from 1pu value. The variations in the graph are not so different the normal working D-STATCOM. Figure 5.13(b) shows the voltages of bus 1 and bus 3 which are nearly same after the compensation. Figure 5.13 (c) shows the modulation index. Modulation index increases in capacitive mode as compared to inductive mode. Figure 5.13(d) shows the Vdc with respect to time.

5.5 Case study 3: When Vref is less then 1pu

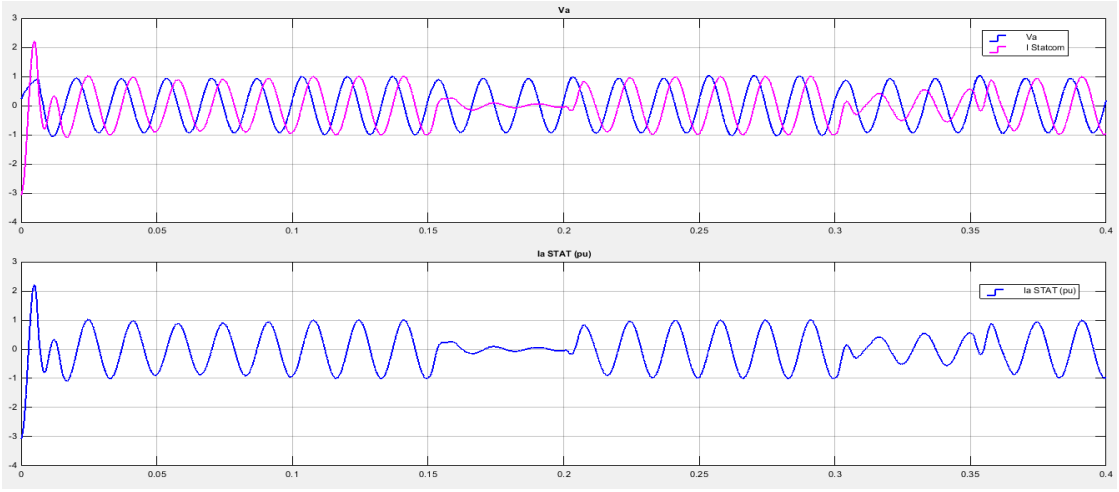

Figure 5.14 Voltage and Current at Vref>1

Figure 5.14, it can be seen that from t=0s to t=0.15s current of statcom is almost at 1pu. The reason for this is that from t=0 to t=0.1 source is at 1 pu but Vref is below 1 with difference of 06% which means from the start D-STATCOM is absorbing the reactive power and is in inductive mode.

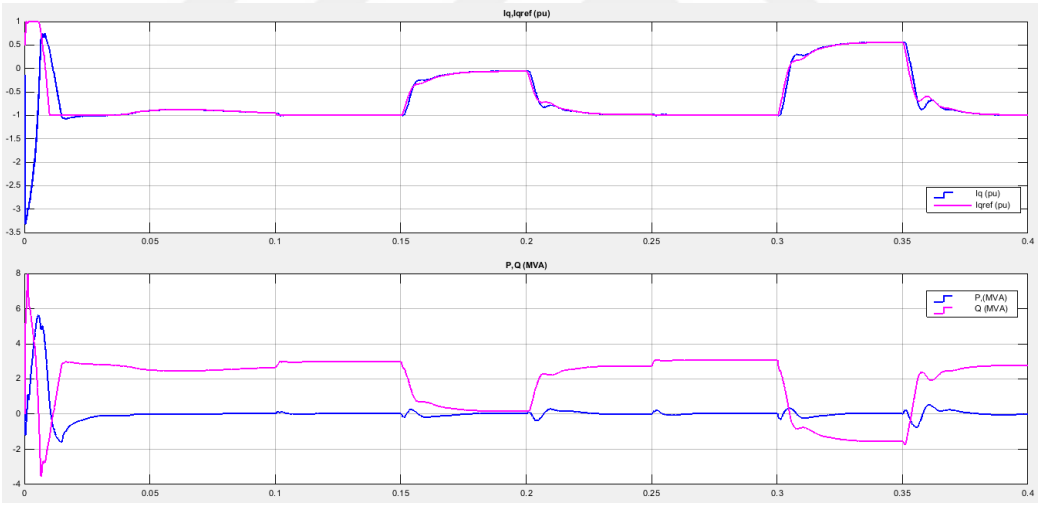

Figure 5.15 (a) Id and Iq (b) Power P, Q (Mvar)

Figure 5.15 shows that from the beginning D-STATCOM is in inductive mode and absorbing the reactive power until t=0.15s. At t=0.15 when set point also decreases from 1pu and it is close to Vref the D-STATCOM starts decreasing the absorption until Vref and set point are equal.

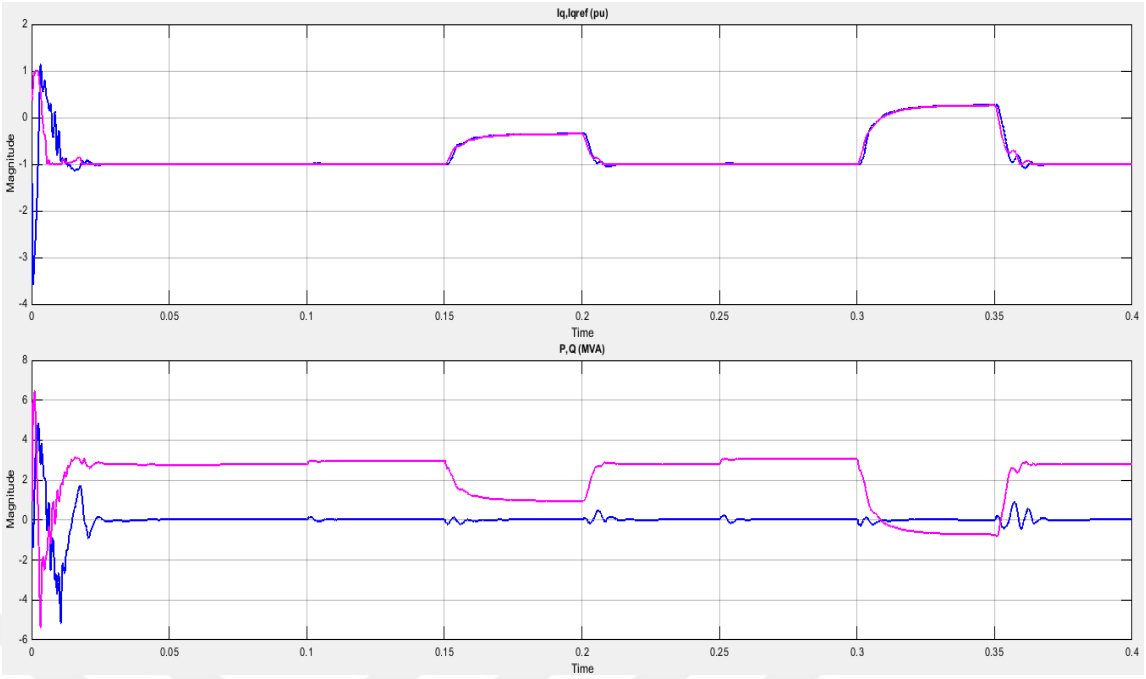

Figure 5.16 (a) Id and Iqref at Vref<1 (b) P, Q (Mvar)

Figure 5.16 it can be seen that t=0.3 D-STATCOM starts going towards the capacitive mode and the reactive power Q starts coming down form almost +3MVAR and goes up to -1MVAR.

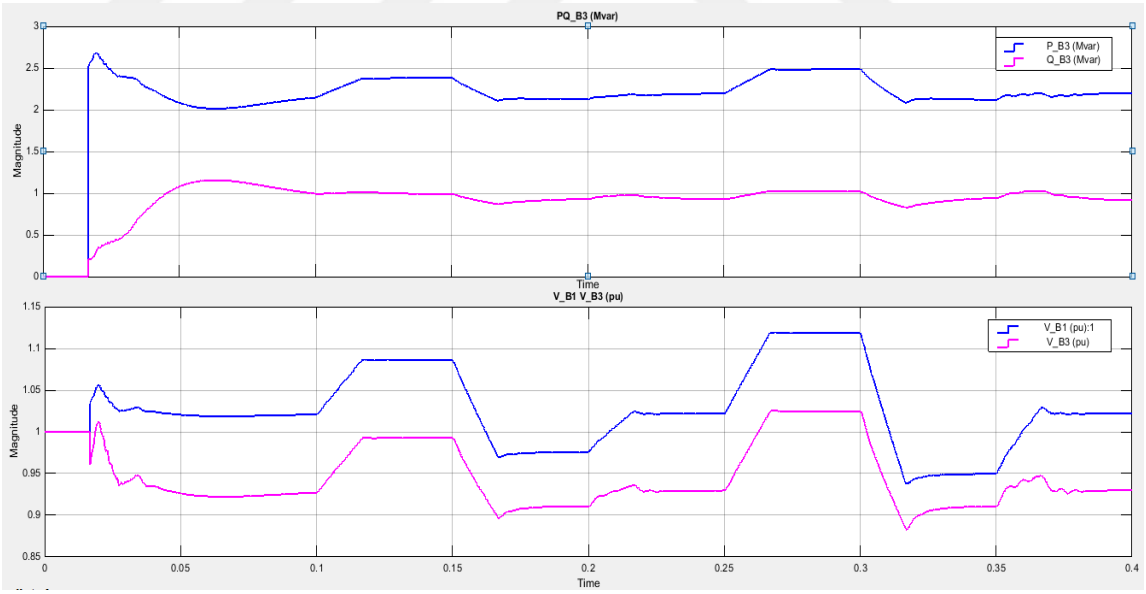

Figure 5.17(a) Power P, Q of Bus 3 (b) Voltage of Bus 1 and 3

Figure 5.17 (a) and (b) shows power of bus 3 and the voltage of Bus1 and Bus3.

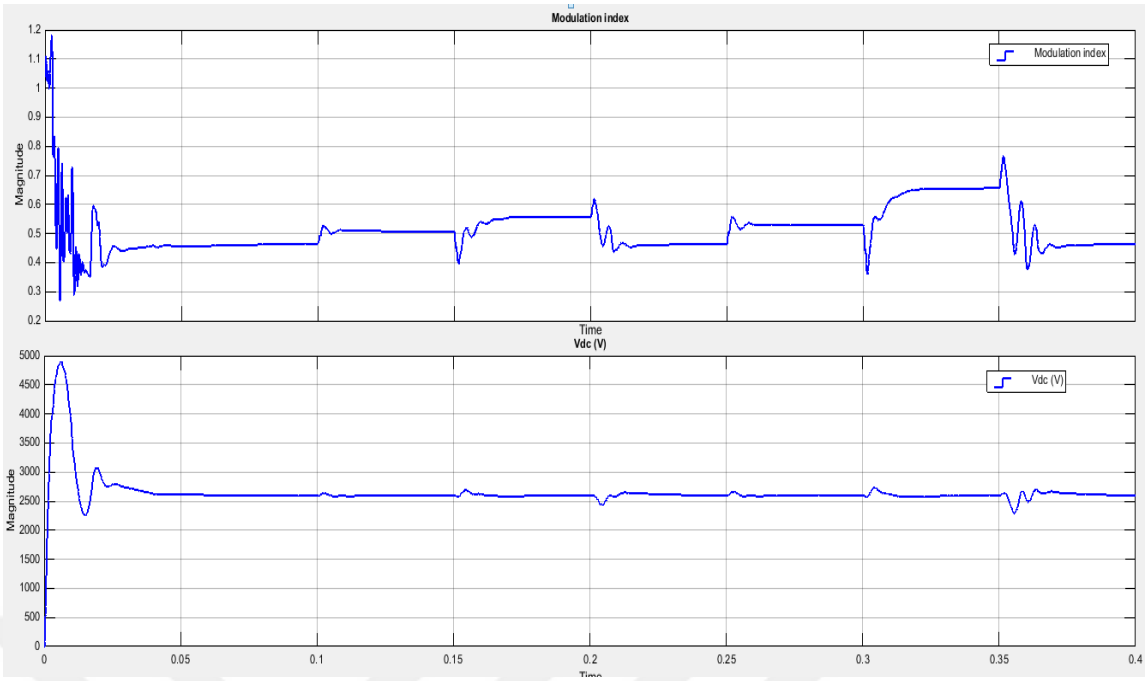

Figure 5.18 (a) Modulation index (b) Vdc

Figure shows the variation of modulation index with respect to time which is low at start, because source set point is already greater then Vref, form t=0.3 to t=0.35 index increases a bit because set point and Vref are close to each other (below 1).

5.6 Case study 4: When Vdc is changed from nominal voltage (2900v)

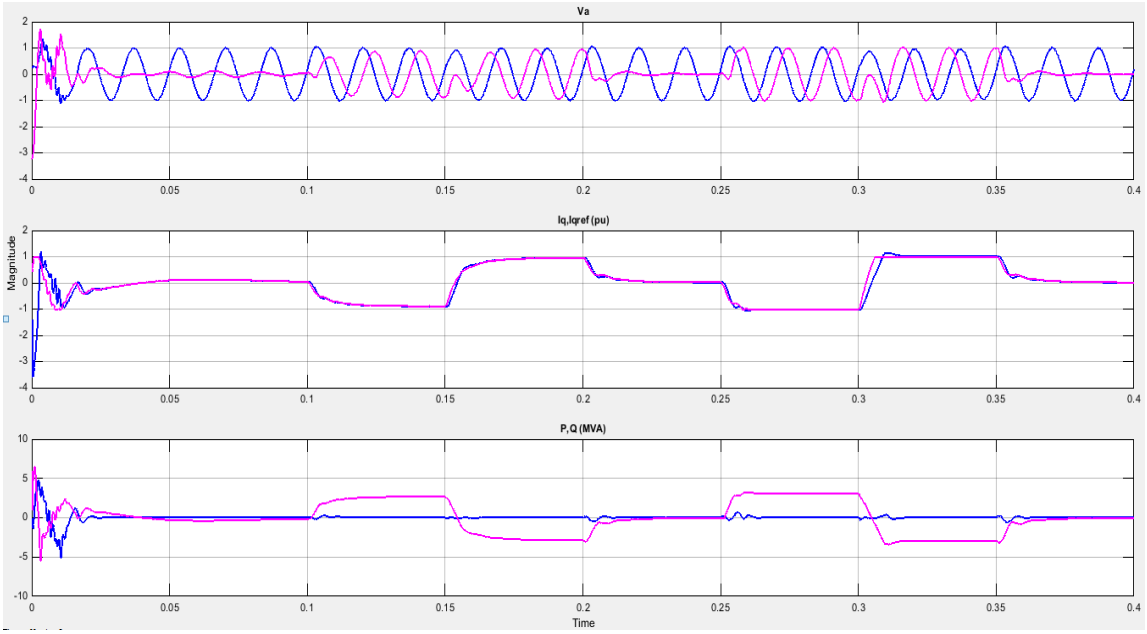

Figure 5.19 (a) Voltage and Current of D-STATCOM (b) Id and Iq ref (pu) (c) Power P, Q (MVAR)

Figure 5.19 explains the effect of change in voltage level of DC power. It can be seen that all the results are almost the same as in the normal operation of D-STATCOM. In

the Figure 5.20 it can be seen that all the other parameters are at good level and are almost same and D-statcom is performing ok. The only thing which is changed is the DC voltage source level.

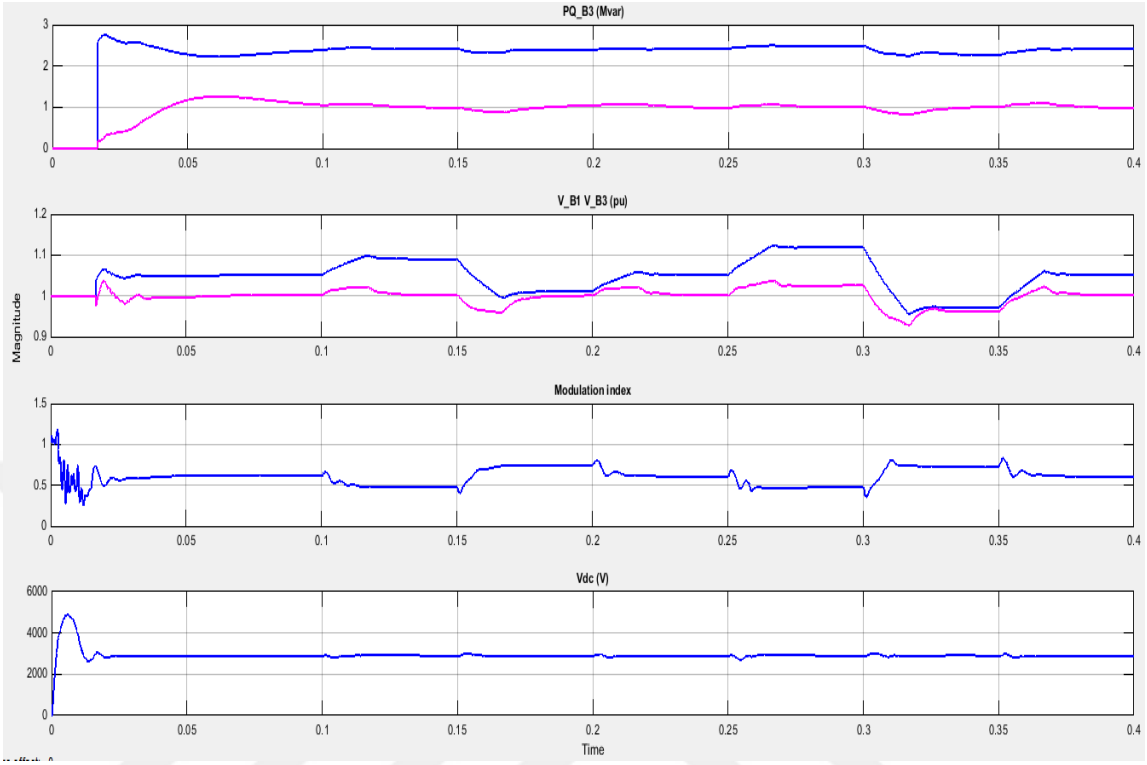

Figure 5.20 (a) P, Q of bus 3. (b) Voltage of bus1 and bus 3 (c) Modulation index (d) Vdc= 2900v

5.7 Case Study 5: Single phase to ground fault

Another case study was done to observe the effect of D-statcom on the power system. The figure below 5.21 shows the voltage and current of the D-Statcom. Blue line is the voltage level, and at t=0.05s a single phase to ground fault was created up to t=0.12s. It can be seen that from the applied time based fault, voltage level is down to 0 (zero). After the fault time is finished voltage is recovered to 1pu. In the second part of figure current should be almost zero up to t=0.1s in normal conditions if there is no problem, but instead of zero the compensation device starts reacting to the voltage change. The other two phases were working ok so the D-statcom fluctuates the reactive power because of lack of phase A.

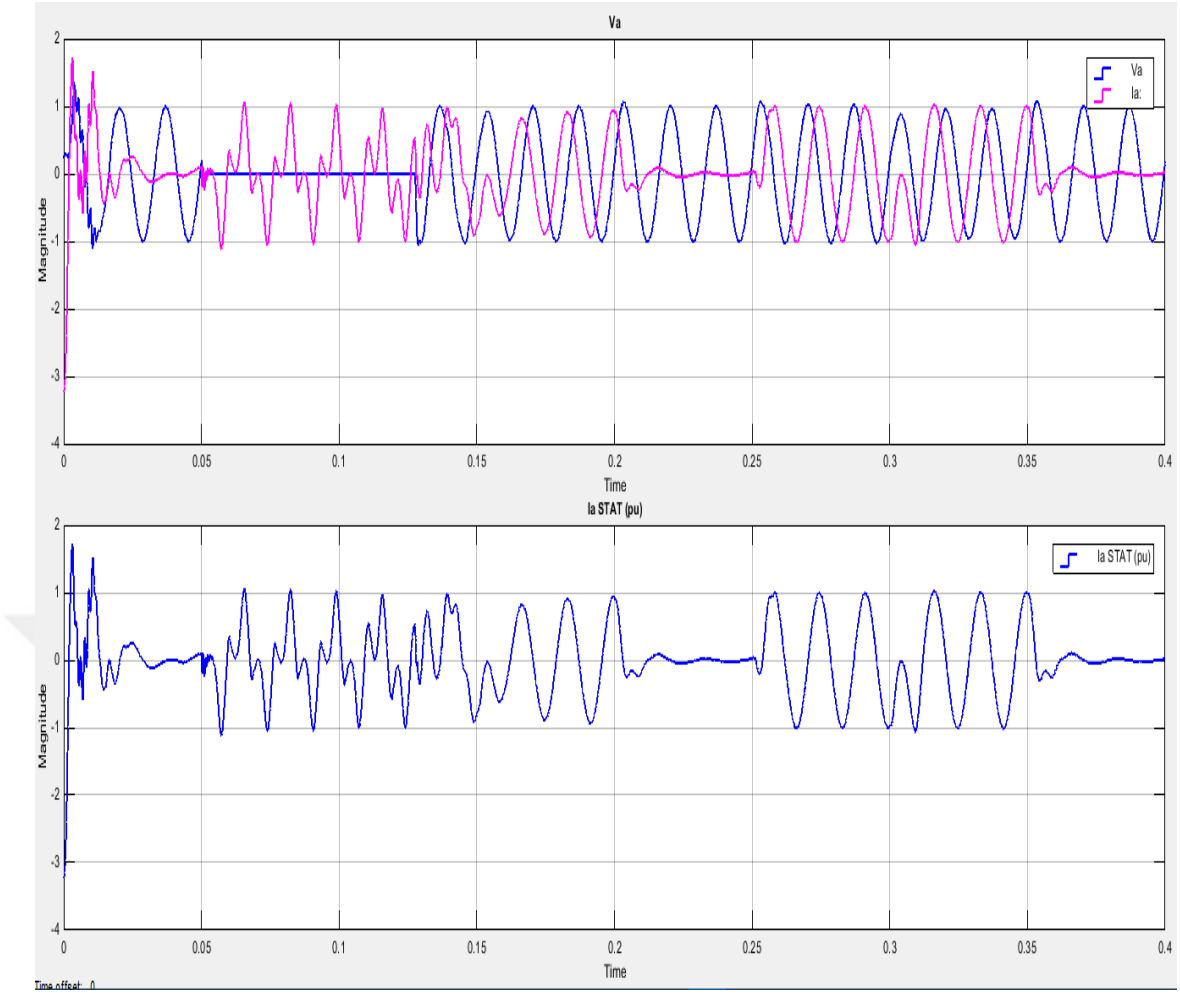

Figure 5.21(a) Voltage and current (b) Current Statcom

Figure 5.22 we can see that Id and Iq ref are fluctuating from t=0.05s to t=0.12s, because of one phase which is in fault condition at the said time. In normal conditions this should be working according to the set points of generation. But here in the second part it can be seen that pink line is below zero level. Which explains that D-STATCOM is working in capacitive mode, because of lack of voltage level at generation side.

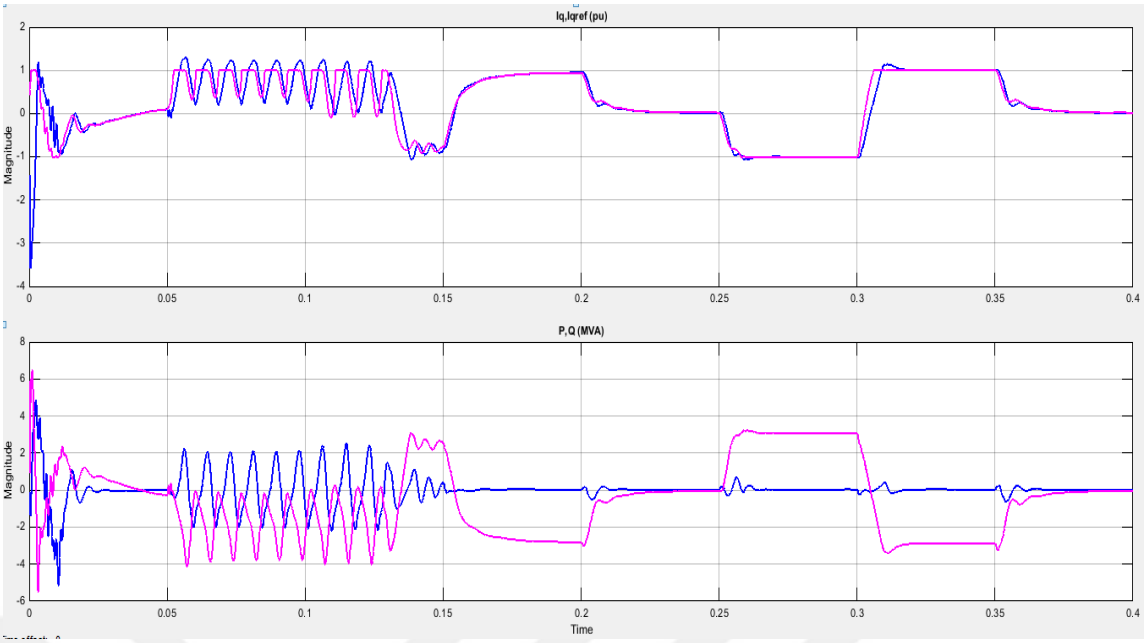

Figure 5.22 (a) Id and Iq (pu), (b) Power P, Q (MVA)

Figure 5.23 shows that a phase during the fault time effects the power at bus 3 on load side. Voltage level of Bus 1 and Bus 3 from t=0.05s to t= 0.12s has more difference than each other. In the modulation index graph, during the fault time we can see the effect of fault, index almost reaches to 1. Due to this fault Vdc is also not stable.

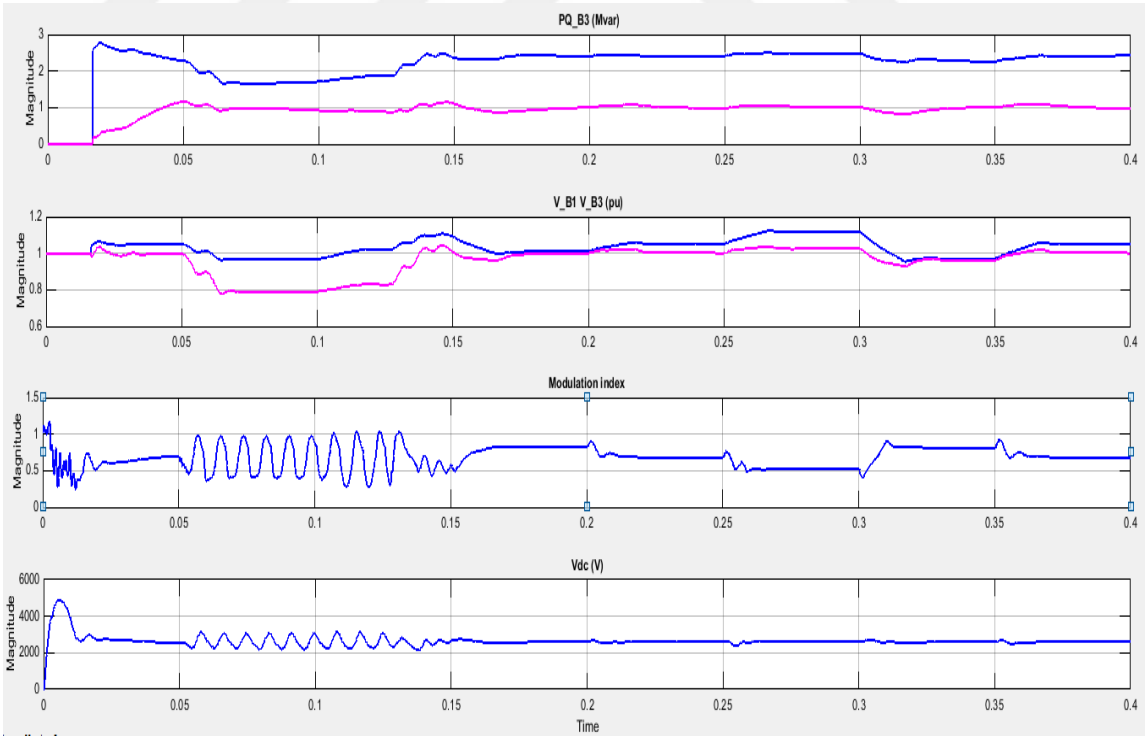

Figure 5.23 (a) P, Q bus 3 (b) Voltage bus 1 and bus 3 (c) Modulation index (d) Vdc

5.8 Case Study 6: Three phase to ground fault

The next case study was done by creating the three phase fault. The fault time was same as in above test. We can see in the figure 5.24 that voltage is 0 between t=0.05s to t=0.12s. But in the Figure 5.24 (b) we can see that there is current flow in the D-STATCOM.

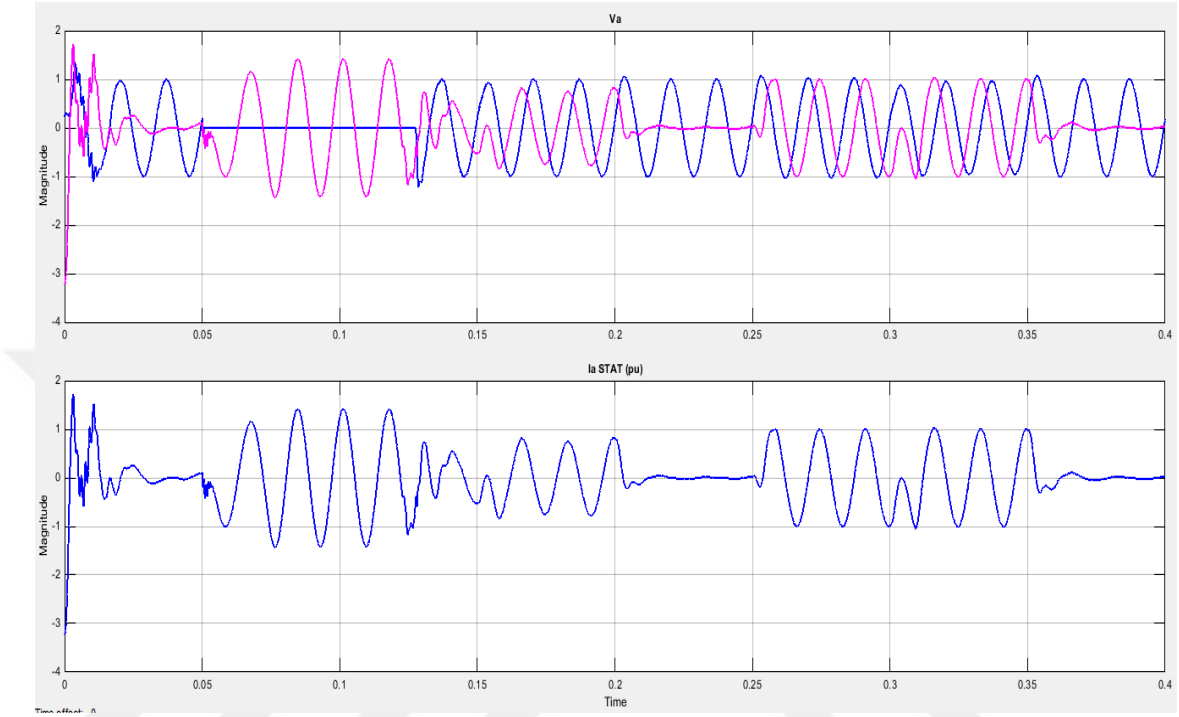

Figure 5.24 (a) Voltage and Current D-STATCOM (b) Ia D-STATCOM

Figure 5.25 (a) we can see that Iq and Iq ref are at 1pu level and when the fault time ends, D-STATCOM starts working as normal device. In Figure 5.25 (b) P, Q of D-STATCOM are at same level 0, because of all three phases down to ground.

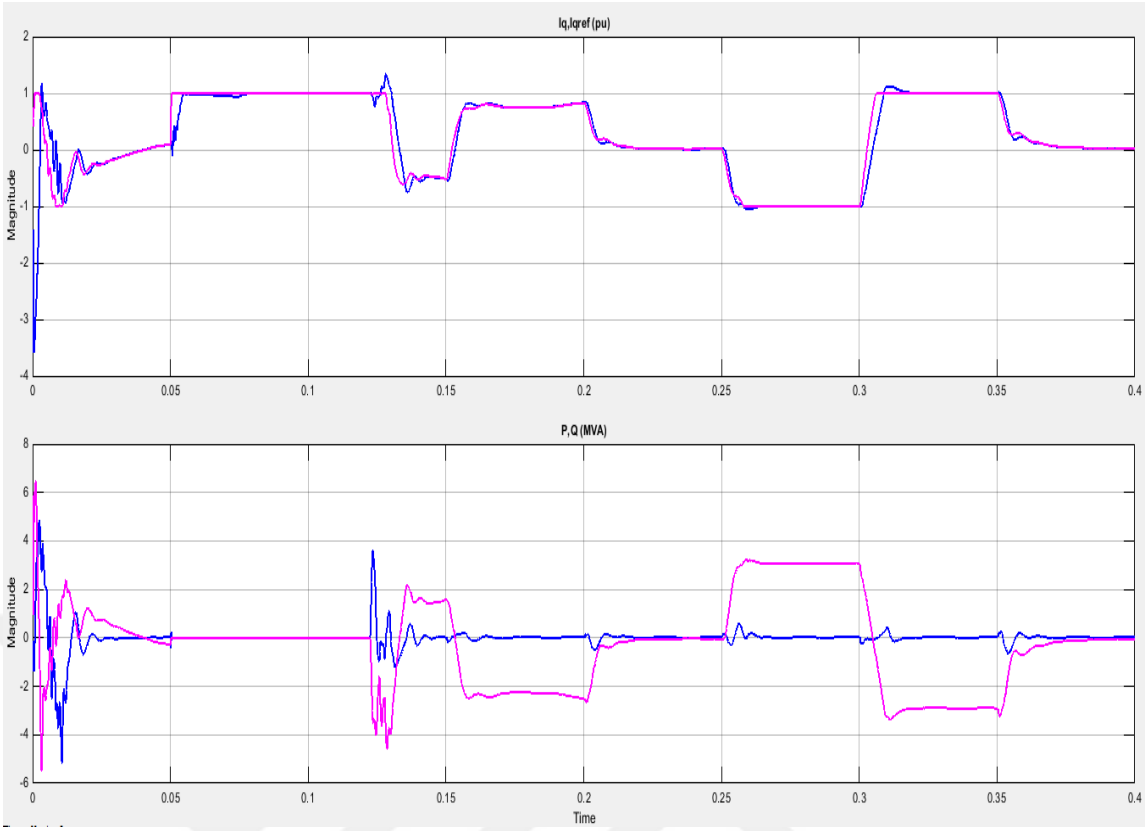

Figure 5.25 (a) Id and Iq ref (pu). (b) Power P, Q (MVAR)

Figure 5.26 shows the effect of all three phases down to ground, in (a) we can see that when the fault time starts the Bus 3 power P and Q both come down to zero. And after the time ends both powers are restored. Which means that compensation device is working properly. In Figure 5.26 (b) we can see when fault occurs the pink line which is related to bus 3 goes down. But the Bus 1 voltage is almost at the same position. This is because the fault is at D-STATCOM Bus, which will not affect Bus 1.

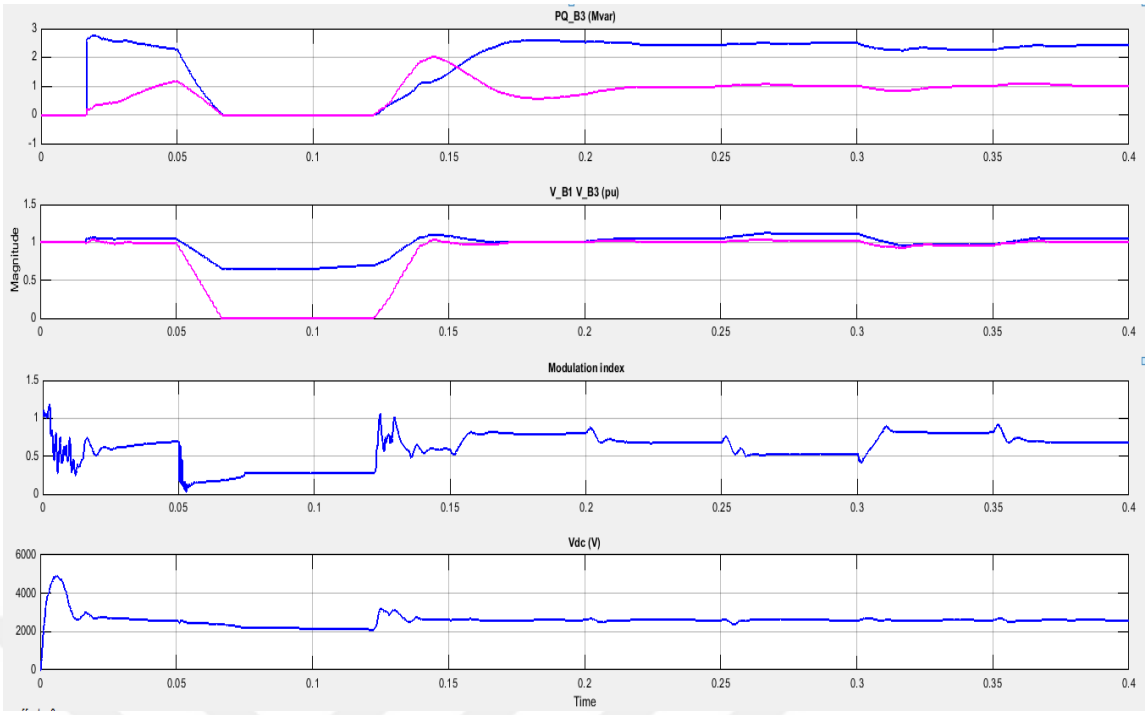

Figure 5.26 (a) Power P, Q bus 3 (b) Voltage bus 1 and bus 3 (c) Modulation index (d) Vdc

In Figure 5.26 (c) we can see that the modulation index varies during the three phase fault time. Which can be seen that it has gone down and nearly to zero during the whole time. As the modulation index is effected Vdc voltage level also decreases to a small value with respect to time.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Description of conclusion

The work done in this thesis is to enhance the power quality of the power system with D-STATCOM. When the load varies, it creates some instabilities in transmission system which can damage both generation and distribution side. To overcome this problem a D-STATCOM is added to the power system in parallel. D-STATCOM reacts to the changes in the desired quality and work for the stabilization of the power system by providing or by absorbing the reactive power.

Study on case 1 was done without the connection of D-statcom which clearly showed at Bus 3 that the system is very unstable and dangerous for generation and load units. When the load is varied the power quality is compromised without any compensation device. Then in second case reference voltage was changed above the 1pu and then the system performance was observed. It can be concluded that D-STATCOM reaction time is very good and one other quality of D-STATCOM is that it can absorb as well as provide the reactive power. In the second case as Vref is more then set point 1pu so it works in capacitive mode and generates the reactive power. By operating in capacitive mode it stabilizes the system power quality.

Case study 3 explains the compensators behavior when the Vref is set below the nominal 1pu value. Which means that the system has some extra power and the compensator has to absorb it. From the start D-STATCOM is in inductive mode and keeps absorbing extra power until a change occurs. In the next case 4 all the other parameters were set to the nominal value and change was made in DC voltage. In this case it can be concluded that changing the Vdc value does not affect the working of D-STATCOM while absorbing or generating the reactive power. If D-STATCOM is

in inductive or in capacitive mode, it will keep operating according to the generation and Vref, independent of Vdc.

In the case study 5 a single phase to ground fault has been applied to observe the performance of D-STATCOM. In the results it can be seen that during the fault time also, D-STATCOM performs fairly good. It tries to accommodate the fault currents by reacting accordingly. It generates the reactive power to adjust the fault in the line. In the last case study a three phase fault has been applied and the results taught that during the three phase fault there is no power flow in D-STATCOM.

6.2 Ideas for future work

In the future some other ideas can be tested to observe and study the power quality.

Firstly modulation scheme can be combined to any other modulation scheme to observe the performance for a hybrid modulated system.

In this work 3 level SVPWM has been done and in future the number of levels can be increased for multiple voltage levels.

Different type of control techniques can be tried and studied to get improved power quality.

Some other compensation devices can be combined to observe the behavior of system.

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