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M.Sc. in Electrical and Electronics Engineering

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MODULAR MULTILEVEL CONVERTER BASED HIGH VOLTAGE DIRECT CURRENT TRANSMISSION SYSTEM

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Modular Multilevel Converter Based High Voltage Direct Current Transmission System

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Supervisor

Assist. Prof. Dr. Ahmet Mete VURAL

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Hakam Muayad YOUSIF

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Hakam Muayad YOUSIF

ABSTRACT

MODULAR MULTILEVEL CONVERTER BASED HIGH VOLTAGE DIRECT CURRENT TRANSMISSION SYSTEM

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The modular multilevel converter is a trending topology for voltage source converters of high voltage direct current transmission that makes it possible bulky electrical energy transfer over very long distances. In this work, an MMC based VSC-HVDC transmission system was designed, modeled, and simulated for balanced 3-phase operation. The time-domain simulations were based on semiconductor level switching. The MMC-HVDC transmission system was considered between two huge big generation centers to provide a control of DC power flow from one center to another. At the same time, reactive power or AC voltage at the terminals of each MMC station was also regulated for stable operation. MMC was designed using five half-bridges at each arm. So there exists 60 semiconductor IGBT switches for one MMC. A reliable modulation technique for the switching of IGBT switches has also been decided and verified in this thesis. The dynamic responses of the controllers of the MMC based VSC-HVDC transmission system have also been analyzed and verified in this work.

Keywords: HVDC, High Voltage Direct Current Transmission, MMC, Modular Multilevel Converter, VSC, voltage source converter.

ÖZET

MODÜLER MULTILEVEL KONVERTÖRÜ YÜKSEK TABANLI DOĞRUDAN GERİLİM GERİLİMİ İLETİM SİSTEMİ

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79 sayfa

Modüler çok seviyeli çevirgeç çok uzak mesafeler boyunca çok fazla miktarlardaki elektrik enerjisinin transferini mümkün kılan gerilim kaynaklı çevirgeçler için trend topolojidir. Bu çalışmada MMC tabanlı bir VSC-HVDC iletim sistemi dengeli 3-faz işletim için tasarlanmış, modellenmiş ve benzetim çalışmaları yapılmıştır. Zaman-domeni benzetim çalışmaları yarıiletken seviyesindeki anahtarlamaya dayalıdır. MMC-HVDC iletim sistemi iki büyük üretim merkezi arasında bir merkezden diğerine DC güç akışının denetimine imkan verecek şekilde düşünülmüştür. Aynı zamanda da, her bir MMC istasyonundaki reaktif güç veya AC gerilim kararlı bir işletim için düzenlenmiştir. MMC her kolda beş adet yarım-köprü olacak şekilde tasarlanmıştır. Böylece her bir MMC'de 60 adet yarıieltken IGBT anahtarı bulunmaktadır. Bu tezde, IGBT anahtarlaması için güvenli bir modülasyon tekniğine de karar verilmiş ve doğrulanmıştır. Bu çalışmada, MMC tabanlı VSC-HVDC iletim sisteminin denetleyicilerinin Dinamik tepkileri de analiz edilmiş ve doğrulanmıştır.

Anahtar kelimeler: HVDC, Yüksek voltajlı doğru akım iletimi, MMC, Modüler Çok Seviye Dönüştürücü, VSC, voltaj kaynağı dönüştürücü.

Dedicated to

My dear mother, father, my wife and children & A best future for my country

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LIST OF SYMBOLS/ABBREVIATIONS

HVAC	high voltage alternating current
HVDC	high voltage direct current
HV	high voltage
DC	direct current
FACTS	flexible alternating current transmission systems
AC	Alternative current
IGBT	insulated gate bipolar transistor
GTO	gate turn-off thyristor
MMC	modular multilevel converter
BJT	bipolar junction transistor
MOSFET	metal-oxide-semiconductor field-effect transistor
IEICE	Institute of Electronics, Information and Communication Engineers.
MOSFRT	Pressure at the inlet compressor
VSC	voltage-source converter
PWM	Pulse Width Modulation
PD-PWM	Phase disposition pulse width modulation
PV	photovoltaic
CCC	Capacitor Commutated Converters
CSC	Current Source Converters
Ud	output voltage
SVM	Space Vector Modulation
THI	Third Harmonic Injection
N, n	Number of: level, capacitor

NPC	Neutral-Point Clamped
FCC	flying capacitor converter
SM	submodules
T1	IGBT1
T2	IGBT2
D1	Diode1
D2	Diode2
Vc	voltage in the submodule capacitor
V_dc	DC link voltage
V_{rm}	arm voltage
S_{sm}	Switching state of each of arm submodules
I_{circ}	circulating current
i_p	upper arm current
i_o	lower arm current
$\mathbf{P_{ac}}$	active power
$\mathbf{Q_{rc}}$	reactive power
V	Voltage
I	current
FFM	Fundamental Frequency Modulation
$\mathcal{F}_k$	harmonic of an n-level phase voltage
α_i	firing angle
SHE	Selective Harmonic Elimination
APOD	phase opposition disposition
PD	phase disposition
LS	Level shift
POD	Phase Opposition Disposition
PS	Phase shift

f	frequency
f_{ceq}	switching frequency
f_c	Carriers frequency
THD	harmonic distortion
D_n	individual harmonic distortion
I_f	AC power generator current
V_o:	AC power generator Voltage
id	active current
iq	reactive current
F_c	cut off frequency
L_{eq}	equivalent impedance parameter for current control
L_{gq}	grid equivalent inductance
L_{rm}	the filter inductance
R_{eq}	equivalent resistance parameters for current control
R_{gq}	grid equivalent resistance
R_{rm}	filter resistance
R_{rc}	regular active damping coefficient
R_{ad}	active damping

CHAPTER 1

GENERAL OVERVIEW

1.1. Introduction

Over the years, the electricity between distant regions has been transmitted over HVAC (high voltage alternating current) transmission lines, which means the two signals (current and voltage) on these lines transfer a wave-like pattern over the transmission lines and are consistently altering direction. In contrast to an AC transmission line, there is a trending technology that uses HVDC (high voltage direct current) transmission line to transmit electricity, in which the voltage and current aren't time varying, which means that they don't vary as energy is transmitted. DC electricity has the zero-frequency, constant electrons motion from negative (-) charge to positive (+) charge area [1].

The infrastructure of electrical power systems has changed fast from central generating stations with HV transmission grids to be multi- generating systems that feed same HV transmission grids. Moreover, lifting restrictions in the power field and beginning the area that intended to distribute electrical power resources that is more cost-effective to supplying all customers with sufficient power. This rapid transformation and lifting restrictions allow to power system engineers to utilize some power electronics solutions such as HV DC and FACTS systems in order to transmit and distribute the electrical energy. Conversely, the growing and improvement in semiconductor switches as well as improvement in transient properties has been effected on development the proper strategies for HVDC systems. HVDC transmission includes several technological and economic advantages greater than standard AC

transmission that make the technology of HVDC represent an alternative choice to the usage of AC transmission [2].

An example of recently HVDC transmission lines is the Clean Line projects that got power from renewable power resources. These renewable resources are AC power generators, and these electrical powers have been transmitted via collecting lines. These lines then have been connected to a substation that collected power and the voltage converted from collector lines voltage to be common voltage (for example 345KV). Then, the power will be converted from AC to DC. The process of converting called rectification. This process utilized power electronic switches such as (IGBT), (GTO), (IGCT), etc. The Self commutation offer a four-quadrant operation that give much flexibility in operation, this allows to control both reactive and real powers at the AC terminals for each VSC. [3, 4].

This provides large number of voltage levels that will be regenerated as AC signal in second station with low degree of distortions, in addition, the large number of voltage levels give a benefit of need just small filters or even no need to filters. An additional advantage belonging to the large number of voltage levels that it possible to adopted to lower switching frequency to decrease the losses of semiconductor switching. This rising in converter topologies offers several benefits to the HVDC systems including: low distortion levels, flexibility, modularity, and increased the efficiency. The MMC power stages must be made effectively along with a pulse generating structure for semiconductor switches. Furthermore, the external controllers need to be designed to providing reliable steady-state operation as well as dynamic response [5].

This work intends make a reliable HVDC system in which the converter circuits are designed based on MMC topology which enable to regenerate AC signal that is very closely to original AC waveform and this minimizes considerably the quantity of harmonics on the AC output terminal.

1.2.Brief History of HVDC Systems

Throughout the earliest half of the twentieth century, HVAC transmission had achieved such a ripeness that it had become the most common choice for designing meshed high-voltage transmission systems. The battle of using DC or AC in transmission electricity was mostly left behind and the common opinion was that fundamentally all transmission line must be depending on HVAC overhead lines. In certain cases, however, HVAC transmission couldn't be used. A couple of this kind of cases are interconnections of unsynchronized AC grids and very long transmissions over the sea. The mercury arc valve was developed by Peter Cooper Hewitt in 1902. It was utilized as a rectifier for electroplating for treatment metal surface, battery charging and dc motors speed control. The usage was, however, limited to voltages under a lot of kilovolts due to issues with backfire (arc-back) phenomenon in which the valve runs in the opposite direction in case the applied voltage is negative [6].

Developing direct current (DC) transmission returns to the 1930's and it has been a powerful technology after the first serious installations in 1954. Historically during the past 40+ years, DC tasks have been shown to give considerable electrical, environmental and economic advantages when transmitting power over very long distances, in which there is a huge veritable growth in the use of DC to engage energy resources in remote sections of the region and provide the energy to people in many greatly populated locations. By using this modern technology, the earliest mercury arc valve HVDC transmission system has been put in service in 1954. This approach is 96 km in long and was able to transmitted 20MW/100kV over a single-cable link with sea return linked the Gotland island with the mainland of Sweden. During 1940's an identical task has also been started in Germany, but due to the war the work wasn't placed into operation in Germany. Rather, the apparatus was transferred to the Soviet Union and bring into operation nearly at the same time as the Gotland-mainland HVDC link. This became the beginning of the mercury arc valve HVDC transmitting era, which survived till the mid-1970s [1].

The mercury arc valves could possibly effectively match the transformation tasks, hut the costly of the valves along with drawbacks including: reliability problems, limited capability of voltage handling, and issues concerning the dealing with of the

toxic mercury prevented a large continuing development of the technology. Beginning from the contrivance of the thyristor in 1950 by the research group headed by William Shockley, the technology of power semiconductor has been developed in parallel with the high-voltage mercury arc valves. The earliest commercially ready thyristor had been released in 1956 by General Electric. In 1960s the development high-voltage thyristor valves for application of HVDC transmission began, where the first thyristor-based HVDC link had been used in 1972 which is name Eel River link in Canada that done by General Electric. From 1977 no new systems based mercury arc valve had been installed. The thyristor era was began, and due to somewhat reliability, efficiency, and low cost, the technology of thyristor-based HVDC transmission has continuous increase from the time its release 40 years ago [7].

The technology of semiconductor has been also utilized for some other power conversions tasks than HVDC transmission. Previously during the early years of the mercury arc valve, rectifiers have been used for dc motors speed control. Through the period 1950s and 1960s, each transistor and thyristor technology have been developed, including: BJTs (bipolar junction transistors), GTO (gate turn-off) thyristors and the (MOSFETs)metal-oxide-semiconductor field-effect transistors) that all have been used for variable-speed motor drives [6].

After serious research tasks by Becke and C. F. Wheatley Jr. through 1980's on “power MOSFRT " that lead to fabricate what today is called the insulated-gate bipolar transistor (IGBT). Together with that research, Baliga have been stead same approach, that has been released in 1982 in Procedures of the IEICE, and the developed device was known as "insulated gate rectifier'. The concept of insulated gate means the fact that the device gate is produced in a similar manner as in a MOSFRT, by using an oxide layer. This simply means that the device is voltage controlled, compared with a BJT that needs a base current so long as the unit carries out a major current. The advantage of using a voltage-controlled is related to the fact that power consumption of the gate driver is significantly less than for a current-controlled device This might look unimportant, however in HV converters the gate drivers run at highly voltages, and giving the required supply voltage at many hundreds of kilovolts isn't insignificant task [8, 9].

IGBT are switch quicker than the BJT and GTO that means it can be reduce the switching losses or it make possible to use switching frequency. In addition, the IGBT required a lower gate-power, which is considered the significant reason why the IGBT used rather than BJT or GTO in motor-drive applications through 1990's. In the late 1990s, the IGBT has been available to applications of voltage-source converter (SVC) based HVDC. The earlier improvement stage had included a number of technology steps. Firstly, a packaging technique was developed, this technique give ability to series-connected slacks of IGBTs. Next development was the passive elements along with gate driver for simultaneous switching of all IGBTs in the stack [10].

In 1997, the first VSC based HVDC transmission has been used practically by ABB in Hiillsjbn. Sweden, which was a test system for research uses. The first commercial transmission link based on IGBT-HVDC was provided in 1999, this was the modern Gotland link (in Sweden) that interconnecting Gotland region with the mainland. The converters were 2-level VSCs with pulse width modulation (PWM) AC voltages. In several ways these types of latest HVDC converters place a new standard for which an HVDC' transmission system would achieve. A big difference between IGBT-HVDC transmission and thyristor-HVDC transmission is the great controllability that will come from the fact that IGBT are unable to just turn on a current at a specific instant, similar to the thyristor. Additionally, it can turn off a current at a required instant. As a result, an IGBT-based HVDC' converter has the ability to independently controlling the reactive and active power. Specially for weakly grids, this is extremely advantageous since the ac-side voltage could be controlled effectively by inserting (or extracting) instantly a controlled level of reactive power. Another advantage is the fact that IGBT-based converters will be able to operate without the existence of generators on the ac side (black-start capability) [1].

By using IGBT technique, the HVDC application area generally has been increased to cover several cases that thyristor-based HVDC cannot be employed. On the other hand, the concern of using two-level VSC technique is the fact that the converter losses are significantly higher than for thyristor-based converters, this due to approximately Fifteen times higher switching frequency required for 2-level IGBT VSCs compared to the thyristor converters. Over a decade different methods to

minimize the switching losses have been reviewed, however, no serious improvements have been in view before modular multilevel converter (MMC) come to takes place. Even though the Rainer Marquardt was gives the concept of MMC at international conferences in 2003, only a few people observed that this technique would certainly replace the overall HVDC transmission area till around 5 years later. MMC allows lower switching frequencies for every device, meaning the IGBTs could be improved for lowest transmission losses. The Power devices utilized for HVDC transmission should be manufactured for lowest losses but this requires accurate trade-offs, specifically between low ON-state voltage drops and fast switching [6].

1.3.Organization of Thesis

The thesis is divided into six chapters as follows: -

- **Chapter One & Two:** give a background and an introduction of this research. It explained the most approach in the field of explosive detection. It also discusses the fundamental of these approaches and it's mainly used in explosive detection, with describes the research aim. Furthermore, this chapter reviews the study context offering a brief background from the investigation related domains.

- **Chapter Three**: provides a general review of HVDC techniques and the fundamental of these approaches and it's used in power transmission system. Additionally, this chapter explains the most modulation topologies that used with HVDC and the benefit of each method in addition to power controlling strategies that can be used with each approaches.

- **Chapter Four:** illustrates the steps of designed HVDC system based on MMC and power controlling model for HVDC

- **Chapter Five**: gives the results and summarizes a brief decision about this work presented.

- **Chapter Six:** presents the conclusions, and suggestions for the future work that may improve the performance of the project.

CHAPTER 2

LITERATURE SURVEY

2.1 Introduction

In the last decade, many investigators have studied the MMC based HVDC, and an intense research has been done to take place every aspect of the system.

2.2 Related Works

Hagiwara et al. (2009) [11], presented an algorithm for voltage balancing regarding the capacitors per phase-leg. This control was implemented by adding a balancing element to the modulation index for each sub-module.

Antonopoulos et al (2009) [12], proposed an approach to reduce circulating current and stabilize the voltage of converter arm. The procedure was dependent on controlled stored energy within the converter, and a couple of control loops have been added to make sure the operation is stable.

In 2010, Angquist et al [13], proposed a facilitation of reduce the circulating current through utilized open-loop method for the evaluation of the arm energy, were its result appeared it have a higher stability. In same year, Guan et al (2010) [14], researched the voltage ripples in the capacitors which related to circulating current component reason

Rohner et al (2010) [15], explains that MMC technique is highly attractive and MMC topology for high-voltage and medium voltage applications. A new PWM has been presented and evaluated. The PWM modulated for an arbitrary range of voltage levels. Based on this PWM strategy, the semiconductor losses have been calculated, and the loss distribution is illustrated that this model got low losses in power.

Mahendran (2013) [16], described the MMC possibilities to utilized as a possible interface between the photovoltaic (PV) panels and grid. He has been proposed an enhanced SVLM approach depending on the PD-PWM. This approach can provide (N + 1) and (2N + 1) level outputs in the MMC, and can perform the dynamic balance compensation controlled the SM capacitor voltage balance without modifying the reference signal.

Çiftçi (2014) [17], specifies the proper carrier based PWM switching along with controlling technique for MMC drives. The project gave the characterization of several phase-shifted and level-shifted carrier based PWM strategies with regards to switching pulse patterns and resulting voltage waveforms for both level (2N+1) and (N+1) output phase voltages. Additionally, the MMC control approaches based on PWM has been analyzed and the performances of various control approaches has been tested in part of: efficiency, circulating current AC component, SM capacitor voltage ripple, output harmonics distortion as well as other considerations in the same switching count concept.

Gayithri, Geetha (2014) [18], and Çiftçi, Hava (2015) [19], used PD-PWM approach to develop the gating pulse generation for a MMC. They designed the controllers by utilizing PI controller to controlled the active power and current. The tested results of controller show that it was capable of tracking the step changes in the reference value through a 0.2 msec time delay.

Haddioui (2015) [20], studied the present modulation approaches. His work suggested the improving solutions that can offer minimizing the switching frequency, improving the capacitor voltage balancing, and regularly distributing the losses over power switches.

2.3 Place of Work in The Literature

In this thesis, an MMC based VSC-HVDC system has been modeled, designed, and simulated for balanced operation with 3-phase. The modular multi-level converter has been positioned in-between two large separate generation centers. The model also includes loads as well as conventional high voltage AC lines. Semiconductor-based time-domain simulations have been carried out in simulation environment. The stages of the work can be summarized as below:

Initially, MMC topologies, the types of power stage have been designed, and the switching modulation strategies have been investigated in the literature for guidance to the work. MMC based VSC-HVDC systems were also investigated for their controllers. At first, the MMC was designed with a suitable level number and a DC link voltage. Secondly, MMC was coupled to a three-phase balanced bus of an example power system using series reactors to test its internal and external control algorithms using standard proportional integral controllers. The four quadrant operation provides independent real and reactive power injection from/to the power system and it was tested and verified. Next, two MMCs were connected at their DC terminals with a long DC transmission line to form a MMC based VSC-HVDC transmission system. The location of the VSC-HVDC transmission system in the example power system was decided to provide two-way real power flow control at AC terminals of both converters. The long DC transmission line was also modeled, suitable for time-domain simulations. The dynamic responses of the controllers of the MMC based VSC-HVDC system were obtained from the time-domain simulation results. They were evaluated and conclusions were drawn at the end of the study. Next, an efficient modulation strategy for the switching of semiconductor switches was decided and tested.

CHAPTER 3

THEORETICAL BACKGROUND OF HVDC TECHNOLOGY

3.1 Introduction

In this chapter, some theoretical concepts of HVDC systems and related techniques are explained.

3.2 HVDC Technology

The HVDC which is also known as (an electrical super highway) or (power super highway), is the electric power transmission system that uses DC for bulk electrical power transmission rather than typical transmission system that uses high voltage alternating current (AC). The main advantages of using HVDC transmission instead of conventional three-phase AC transmission can be summarized as follows: Reducing transmitting loss, the ability to transmit extra power through a similar right of way, the capability to interconnect systems which are not synchronized or utilizing various frequencies, long distance water crossing capability, and short-circuit current limitation [21].

The major advantage of HVDC transmission over AC transmission is that the HVDC transmission has capability to accurately control active power transfer over the DC line. This function is limited in AC transmission; thereby FACTS devices are required to enhance this function. Furthermore, HVDC transmission is relatively cheaper when compared with classical AC transmission across a 50 km long of underground or submarine cables or when the overhead lines are longer than 800 km. Figure 3.1 illustrates the cost estimation of AC transmission compared with DC transmission [22].

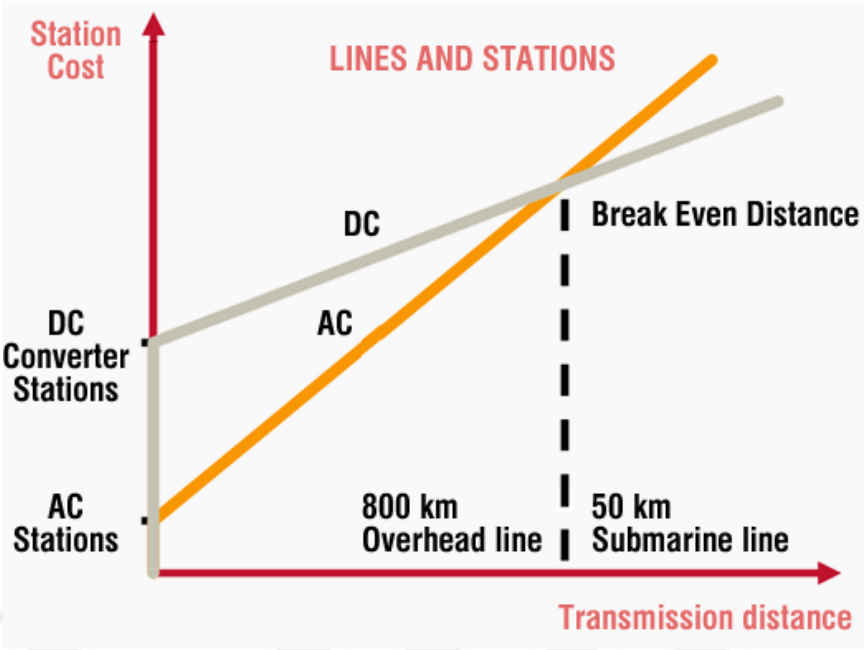


Figure 3.1: Cost estimation of AC vs DC transmission [22].

The basic procedure that occurs in an HVDC system is the transformation of the AC electrical current to the DC electrical current at transmitter (rectifier), and from DC electrical current to AC electrical current at receiver (inverter). There are three methods for this transformation [23]:

3.2.1 Natural Commutated Converters:

These type of converters is mainly utilized in HVDC systems to date. The element that allows this conversion process is the thyristor, a controlled semiconductor, that could carry highly currents value (about 4000 A) and it can work with high voltages up to 10 kV. From strategy for linking the thyristors in series, it gives the ability to create a thyristor valve, that is capable of functioning at higher voltages (several hundred of kV). The thyristor valve can operate at net frequency in between 50 Hz or 60 Hz. By control angle, it can change the level of bridge DC voltage. This capability makes the transmitted power to be controlled quickly and efficiently [24].

3.2.2 Capacitor Commutated Converters (CCC):

An amelioration in the commutation based on thyristor, the concept of CCC is described as the usage of commutation capacitors rather than in series in between the thyristor valves and converter transformers. The commutation capacitors enhance the performance of commutation failure of the converters once linked to poor networks.

3.2.3 Forced Commutated Converters:

This kind of converters offers a range of benefits, such as: Independent control of reactive and active power, power quality and passive networks feed (without generation). The valves of such converters are made by semiconductors having the ability not just to turn-on but also turn-off, which is called the Voltage Source Converters (VSC). Two different types of semiconductors are already employed in the VSCs [25]:

1- The Gate Turn-Off Thyristor, which symbolizes it as (GTO)

2- Insulated Gate Bipolar Transistor which symbolizes it as (IGBT).

These two types are usually used in commercial applications from early 1980's. The converter operation is achieved by PWM that gives the possibility to generate any amplitude or phase angle by modifying the PWM pattern, which have been done almost instantly. As a result, the PWM gives the possible ways to control both the reactive and active power separately from each other. This makes the PWM VSC to be a near ideal factor in the transmission network. At a system point of view, it works as a generator or motor with no mass which might control active and reactive power close instantly. Moreover, it doesn't redound to the short-circuit power because the AC current could be controlled [1].

3.3 Basic VSC Topologies

VSC is a good alternative for smart power grid that could provide a large amount of controllable power into the existing AC grid. The use of VSC is the state-of-the-art method of converting and transmitting electrical power. Traditionally,

Current Source Converters (CSC) have been preferred in HVDC transmission because of lower losses and higher transmission capabilities. But due to recent advancements in component design, VSCs are now used in numerous power electronic applications, and give several benefits. Some of these are [26]:

- Easier bidirectional power flow
- Faster response because of active switches (IGBTs)
- Better control of active and reactive power

The application of the IGBT, which is a self-commutated semiconductor device, makes many different topologies suitable for VSC. There are many different solutions of VSC such as two-level, non-multi-level, and multi-level converters which have been available in terms of harmonic spectrum, commutation inductance, DC capacitor volume, costs, and footprint [27].

The standard, unprocessed AC output waveform associated with a VSC is dependent upon the topology of the converter. About three typical types of topology that is ideal for DC power transmission are exist, which are described as follows [28, 29]:

3.3.1 Two-Level Converter Topology

This basic topology has been commonly utilized in several applications, such as "HVDC Light" product. In this topology, the phase outlets can be connected either negative or positive DC-link terminal, which can produce a 2-level output voltage (+Ud/2, -Ud/2), can be modulated by space vector modulation (SVM) or PWM scheme. Figure 3.2 illustrates the structure of 2-level 3-phase bridge VSC [28].

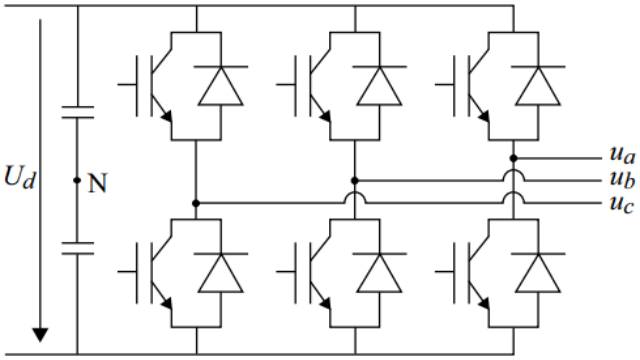


Figure 3.2: Basic structure for 2-level 3-phase VSC [28]

For applications of HVDC, a higher range (more than 100) of series linked IGBTs are needed to link in series to get the required voltage rating. The main benefit of using 2-level VSC for application of HVDC power transmission is usually a relatively basic circuit to control with several methods. The downsides of this converter when it employed for application that requires to utilize PWM to decouple the AC voltage coming from the DC voltage power. This relates to hard switching of the series string of IGBTs which will add further switching loss along with further complexity needed to dynamically share the device voltage through the switching event. The switching pattern of PWM can also cause harmonics for the output voltage, that will make a need for bulky passive filters to minimize this to appropriate levels based on the grid code [29]. Additional downsides involve poor fault performance of DC side; In case when depressed in DC voltage, in ways that the voltage ratio of AC/DC is greater than that of the over-modulation area allowed by tipplen harmonic injection (THI), AC voltage then makes the 2-level converter to rectify to DC grid and also the AC breaker should be opened. Furthermore, once the voltage of DC grid is totally reversed, the IGBT diodes are going to conduct whatever the condition of the AC side breaker and IGBTs [30].

3.3.2 Non-Modular Multilevel Topologies

The non-modular characteristics of the topology imply that the clamping diodes don't have a standard voltage rating; which means some clamping diodes should be ranked with full DC bus while others do not. By supposing that a series connected

devices are utilized to achieve this voltage rating, it is observed that for every extra level an additional component is needed. Furthermore, the split DC-Link capacitors will cause complication in voltage balancing [31].

A one model of this topology is 3 phase 3-level diode-clamped converter as illustrated in Figure 3.3. The benefits are lower switching losses and perfect simple AC waveform in comparison to the 2-level converter. If the converter is expanded to extra levels, the extra clamping diode pairs should be added as shown in Figure 3.4 for the 5-level case. The total range of diode pairs will increase rapidly with the number of levels [29]. For 1-phase case, an N-level diode clamping inverter needs (N-1) capacitors, 2(N-1) switches, and (N-1) (N-2) clamping diode [28].

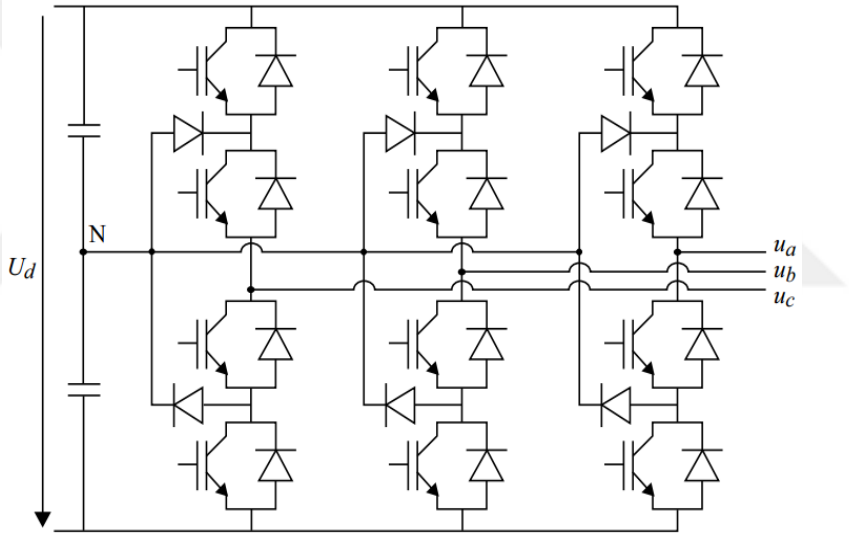


Figure 3.3: 3-level 3-phase VSC [28]

3.3.3 Multi-Level Converters Topologies

In regard to the solutions of multi-level, four most important topologies are: Diode-clamped, capacitor-clamped, cascaded H-bridge, and MMC [32].

3.3.3.1 NPC Diode Clamped Converter.

A n-level diode clamped converter consists of (n-1) capacitors within the DC bus and generates (2n-1) levels of output line voltage and (n-levels) of phase voltage. Additional characteristics involve [32, 33]:

- It requires a high voltage rating of blocking diodes.
- Irregular device rating causes various current ratings of devices.
- The output waveform offers a best harmonic content when comparison to the 2-level.
- It suffers from unbalance problem of capacitor voltage.
- The number of clamping diodes should be increased however this situation increases complexity.

An application that has used this topology implementation, is the (36MW, ±15.9kV) Eagle Pass back-to-back HVDC Light, that was put in service in September 2000, which allows to exchange power between stations of two regions: Eagle Pass in Texas and Piedras Negras in Mexico. Figure 3.4 shows the schematic of the NPC and the 3 level output waveform [34].

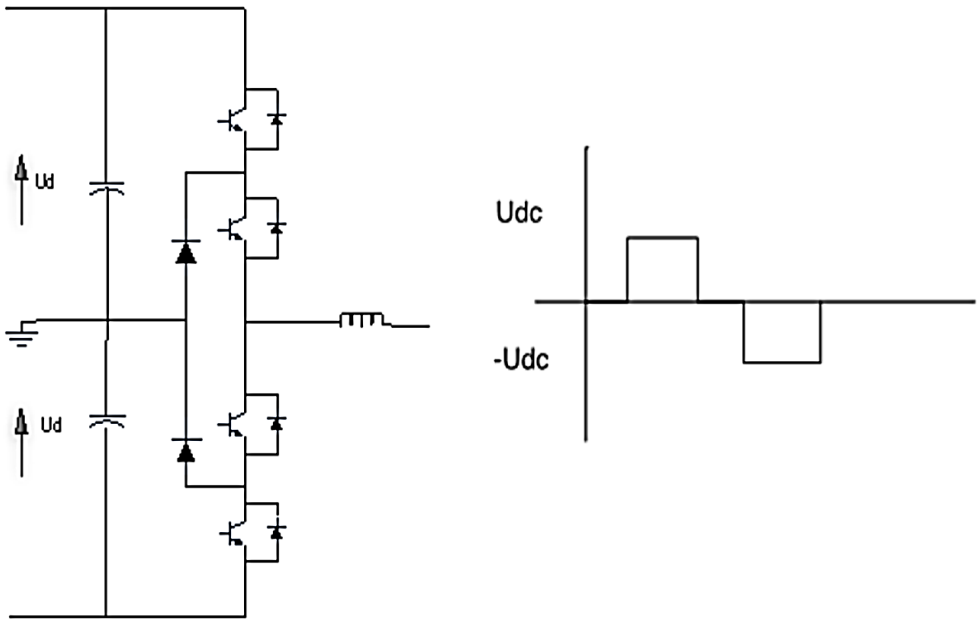


Figure 3.4: 3-level 3-phase VSC [33]

3.3.3.2 Capacitor-Clamped or Flying Capacitor Converter

Flying capacitor converter FCC has been available since 1992. Instead of diodes, the clamping capacitors provide a much more flexible topology, in which several switching combination can be resulted in the same voltage levels. When compared the capacitor clamped converter with diode clamped, the first one consists of a great number of capacitors known as ‘floating capacitors’. When the number of level increases, the amount of capacitors are also increasing. Using these high number of capacitors provides ride over capabilities through outages, however, in turn, it increases the cost and make complexity in controlling. Thus, this topology has been used in many motor drives applications. For case of capacitor clamped converter, the voltage synthesis provides much more flexibility compared to diode clamped converter. On the other hand, this topology has a disadvantage that it suffers from irregular duty problem from the switches. Figure 3.5 illustrates a single phase, 3 level capacitor clamped converter [33, 35].

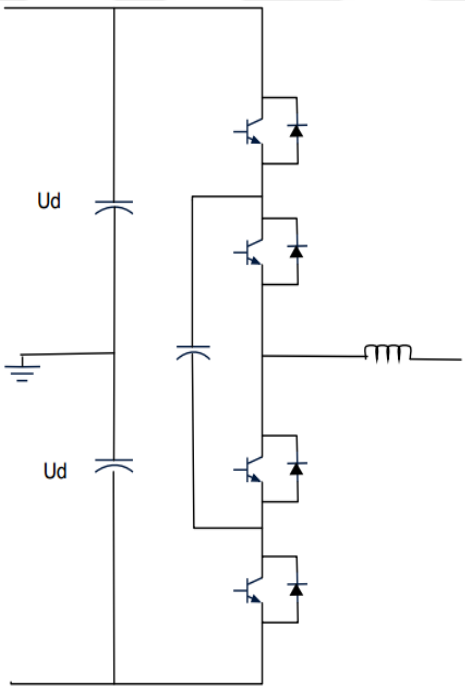


Figure 3.5: Capacitor Clamped or Flying Capacitor Converter [33]

3.3.3.3 Cascaded Multi-Level Converter

A typical strategy of VSC based multilevel is cascaded H-bridge. Even so, each H-bridge module requires a unique separated DC power supply. Single H-bridge structure is able to generate three voltage levels, these are (0, +Udc, -Udc). A sequence links of these specific bridges produces a stair case output waveform in which each step matches every individual bridge. In order to achieve greater levels for the output waveform, additional H-bridges should be linked. Usually for case of (n-level converter) it requires 1/2(n-1) H-bridges per phase. The benefits regarding this topology are those that: it needs minimal number of elements when compared to other topologies for similar voltage level needed. Furthermore, it provides a modularized circuit layout and doesn't need any further clamping capacitors or diodes. The drawback of this topology is the need for isolated DC sources which makes the design hard for higher levels. Figure 3.6 shows a single-phase cascaded H-bridge structure (one module is highlighted in grey) [28].

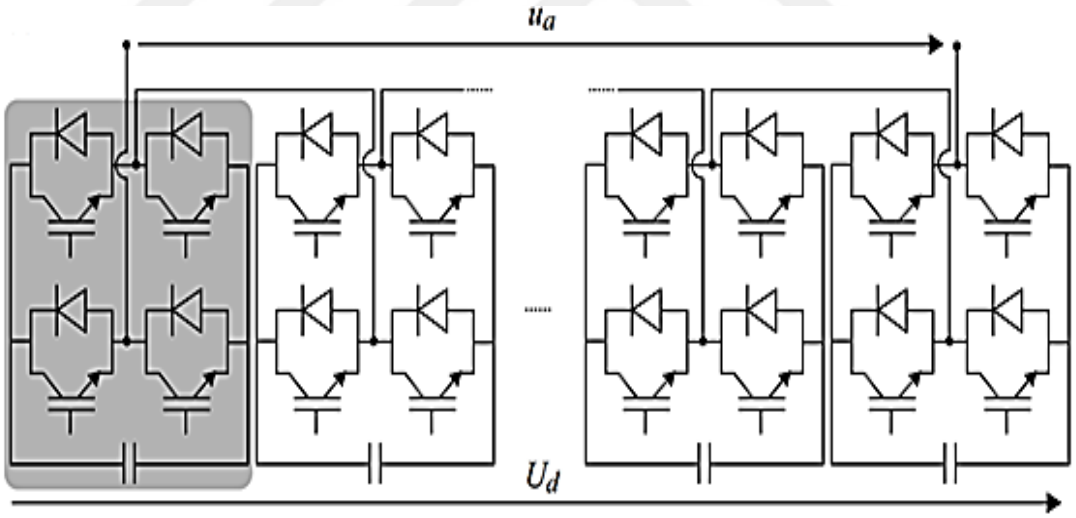


Figure 3.6: Single-Phase Cascaded H-bridge Structure [28]

3.3.3.4 Modular Multilevel Converter (MMC)

Currently, a novel topology based on VSC is known as “Modular Multilevel Converter (MMC)” has been presented. It includes a common DC-link, and do not need DC-link capacitors. In this topology, it can directly control DC-link voltage through the switching states of the submodules (SM), so it does not require any separated DC power supply as in case of cascaded H-bridge topology. The modular structure is less complicated than the cascaded H-bridge structure. Single cell consists of two switches, main and auxiliary switch. The output voltages are obtained from single structure. MMC generate (0 and +Udc) voltage levels but no (-Udc) as in cascaded H-bridge. Through the 0 level state, the capacitors charge or discharge depending upon the direction of the load current and hence a slight imbalance is created. The capacitor voltages can be controlled through process of controlling the switching-in of the various cells throughout the 0 voltage output. The arm inductances give a route for the circulating currents through the balancing process along with minimizing the inrush currents. In MMC topology, the modular nature gives a benefit as high levels and thus it can achieve higher voltages by putting cells together. For case of using higher number of SM, MMC will be operating with no need for the filters, that is a big benefit when compared with other multilevel counterparts. Figure 3.7 illustrates a MMC structure [28, 33].

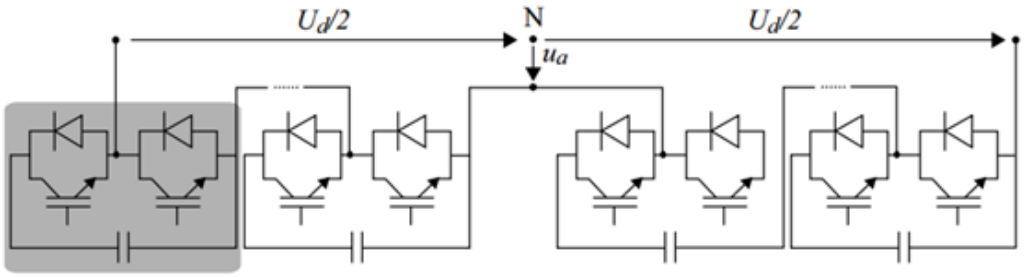


Figure 3.7: Modular Multilevel Converter Structure [28]

As discussed previously, the HVDC techniques were started from CSCs to VSCs, and far more to MMC, that has little foot print, requires a smaller filter or in some cases no need to filter. Thus, this topology is also very appropriate for offshore wind turbine applications [28].

3.4 Details of MMC Topology

MMC receives a big attention due to its modular structure that gives more advantages. Recently, MMC technology has already been used in large HVDC transmission projects, which is appropriate for high voltage structures. One example is the German offshore wind project that consists of a HVDC cable that links Norway and Denmark, [36]. Other project example is that the Trans Bay Cable project in San Francisco [37].

3.4.1 MMC Structure

The technology of MMC is composed of set of similar elements, called sub-modules (SM), as shown in Figure 3.8(a). The series of connected SMs in each phase is refers as a leg. This leg is split into lower arms and upper arms so that the quantity of the SMs in every arm is the same. Since the capacitors in the leg share a regular DC link voltage, it is not necessary to use bulky capacitors which are needed in case of two-level or NPC topology. Inductors, on the other hand, are inserted inside the arms to reduce transient currents [38].

Many SM's topologies can be considered. The main difference causes from the cell structure that can lead to numerous possible voltage levels on the SM terminal. Nevertheless, while increasing the elements, the capacitor balancing gets more challenging. In accordance with the experimental studies, the losses by switching, and the capacitor voltage balance problem, half-bridge (HB) topology is generally considered as the most appropriate topology which can be used in the SMs in cases where bidirectional power conversion is needed [39].

The half-bridge topology is constructed by two bidirectional power electronic switches (IGBT) with antiparallel diodes, and a DC capacitor. This configuration is illustrated in Figure 3.8(b) [40].

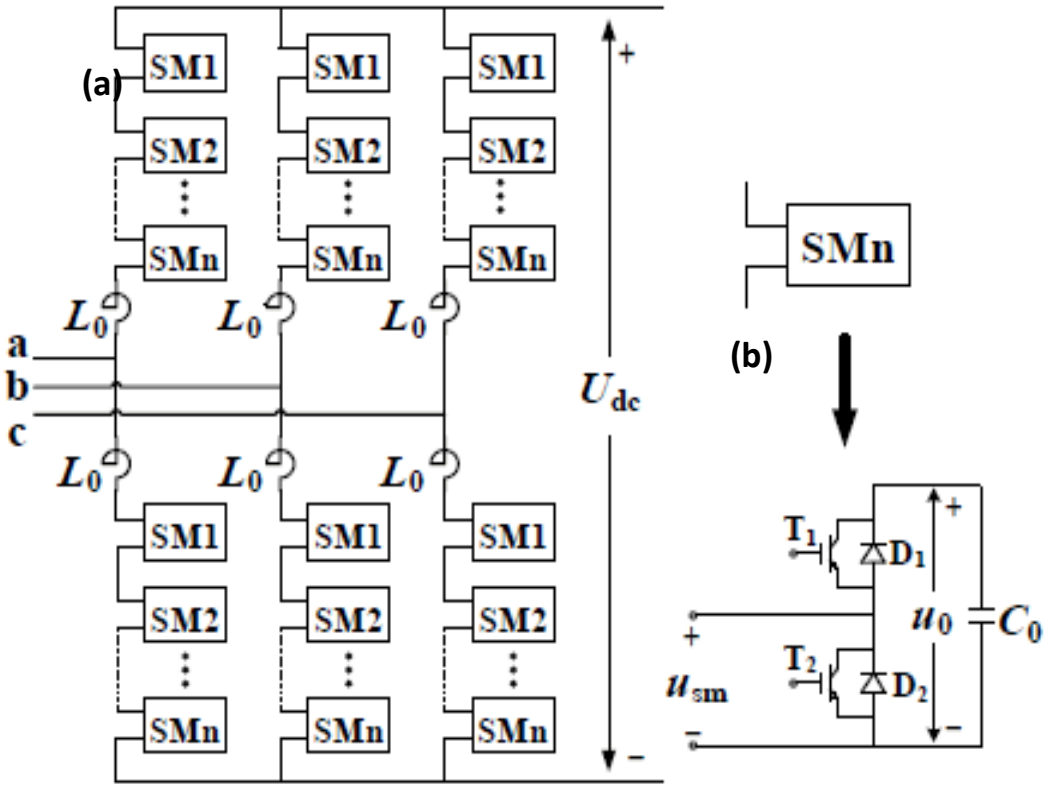


Figure 3.8: MMC Structure: (a) basic components, (b) half-bridge sub-module. [40]

The capacitors act as an energy buffer and as a voltage source. The switches achieve the status of the SM within the arm circuit and the antiparallel diodes ensure that current always flows. Figure 3.9 shows the possible states of half-bridge SM and the current paths [10]. SM has two diodes (D1 and D2) and two IGBT (T1 and T2). At a given time, only one of the HB circuits can be ON. As turning T1 off and T2 on, the SM is considered to become inserted and the SM output voltage is equal to capacitor voltage. Then the capacitor is charged when the arm current is positive and is discharged otherwise. By changing the status of the valves, in other meaning the T1 on and T2 off, the SM gives zero output voltage. In this case the capacitor is bypassed along with its voltage stays constant. As both valves will be turned off, the SM is blocked and the current flows over the diodes. Next the capacitor is only charged each time the arm current is positive. Ideally the capacitor is not discharged [40, 41].

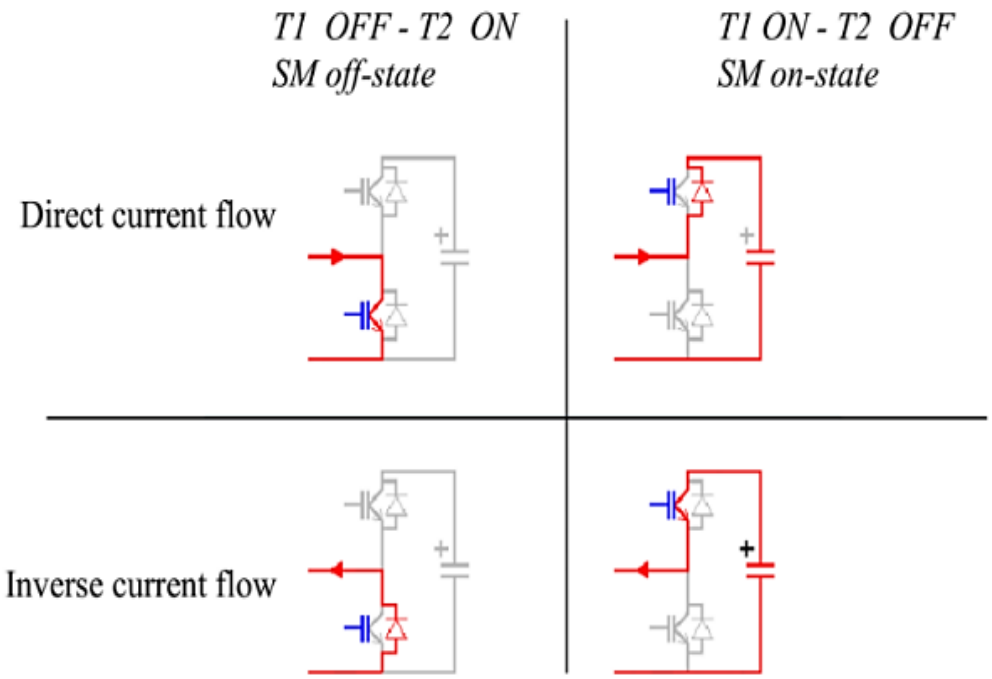


Figure 3.9: SM States and the current path [41]

For the case where SM is turned on/inserted, the circuit terminal voltage of half-bridge are equals to the voltage in the SM capacitor (SM Vc), while if it is switched off/bypassed then it will be zero. In case when both switches are OFF, the terminal voltage cannot be determined and based on the direction of the current, several voltages will occur at the terminals, in case where the both switches are ON, then the SM capacitor will be short-circuited. With regards to the states of half-bridge circuit and the SM current direction, SM capacitor is either discharged or charged. All previously discussed switching combinations and capacitor charge/discharge conditions, and half-bridge terminal voltage are illustrated in Figure 3.9 and Table 3.1[42].

Table 3.1: Switch States of a Sub-module [42]

Switch State		SM Terminal Voltage	Arm Current Polarity	Status of the Capacitor
T1	T2			
1	0	Vc	+	Charging
0	1	0	+	By-passed
1	0	Vc	-	Discharging
0	1	0	-	By-passed
1	1	Capacitor Shorted		
0	0	Open Circuit		

3.4.2 Mathematical Model of the MMC

As shown in Figure 3.10, the three-phase MMC consists of a number of 2N series connected switching cells or SMs that form a phase-leg [43].

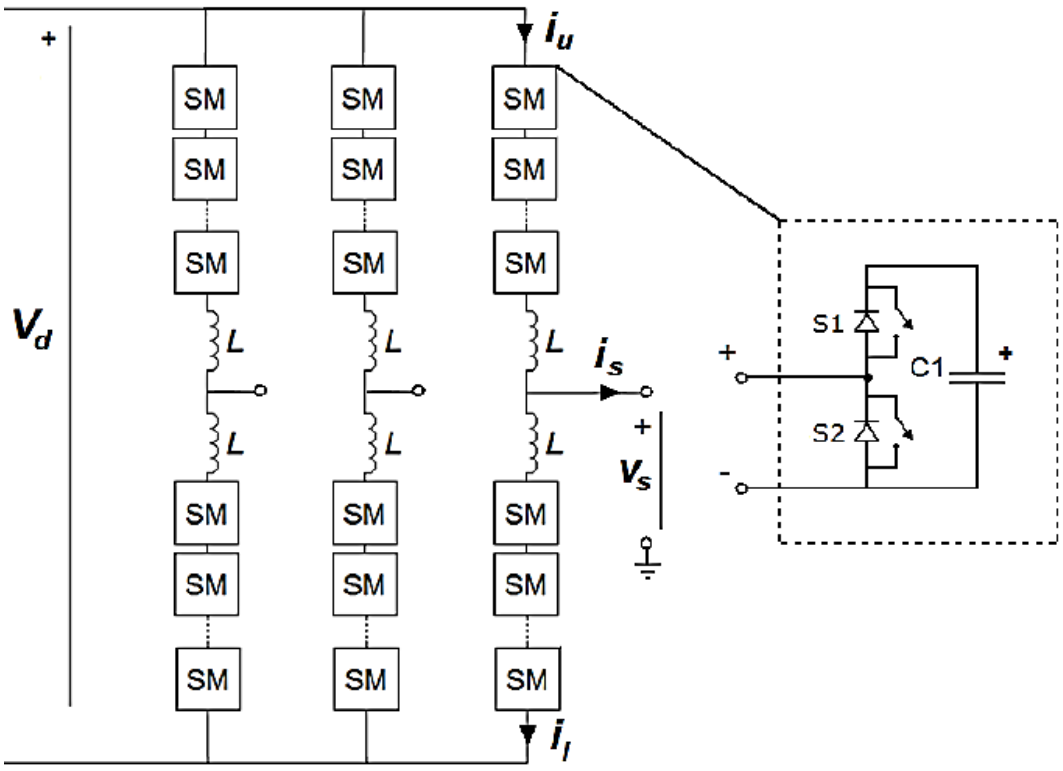


Figure 3.10: Circuit structure of MMC [43].

In the phase leg, SMs are sorted in lower and upper arms with either single coupled inductor or one inductor per arm. The SM switches are controlled in a complimentary method to ensure that at any immediate, the SM is either bypassed or connected to the arm. Every one of the arms in the converter works as a controlled voltage source, which has a variable voltage ranging from zero to Vdc. The arm voltage is determined via the switching case of the SM of arm, which can be calculated by Equation (3.1) [44].

$$V_{rm} = \sum_{i=1}^{n} S_{sm} * V_{c,sm} + L_{rm} \frac{di_{rm}}{dt} \tag{3.1}$$

The current pass through arm consisted from two parts, circulating current and the load current throughout the phase-legs in the converter, as shown in Equations (3.2) and (3.3) [44].

$$i_p = \frac{i_{ld}}{2} + I_{rc} \tag{3.2}$$

$$i_o = \frac{i_{ld}}{2} - I_{rc} \tag{3.3}$$

where $i_p$is the upper arm current and $i_o$is the lower arm current, which are both expressed as the sum of half of output (ac side) current i_{ld} and circulating current, I_{rc} that is represent the loop current that circulates over every leg of phase and the DC link. For the balanced load conditions, the DC link current is equally shared among 3-phase legs. The I_{rc} is composed of DC link current and the AC currents that related to the V_dc ripple of the phase leg and the voltage difference among different phase legs. Based on Equation (3.2) and Equation (3.3), the circulating current and the output current can be represented with respect to the currents of lower and upper arm as in Equation (3.4) and Equation (3.5) [45]:

$$i_{rc} = \frac{i_p + i_o}{2} \tag{3.4}$$

$$i_{ld} = i_p - i_o \tag{3.5}$$

The upper arm voltage and the lower arm voltage beside the circulating voltage can be evaluated by use the equations [45]

$$V_p = \frac{V_{-dc}}{2} - V_{ot} - V_{rc} \tag{3.6}$$

$$V_{lo} = \frac{V_{-dc}}{2} + V_{ot} - V_{rc} \tag{3.7}$$

$$V_{rc} = R_{rm} * i_{rc} + L_{rm} * \frac{di_{rc}}{dt} \tag{3.8}$$

The voltages summation in the arm must be equal to DC link voltage as well as the voltage must be uniformly distributed between SMs of the upper and lower arms in addition to the phase-leg. Additionally, when SM is connected within the arm, the load current passes from the capacitor generating a ripple in the SM voltage. The active power (Pac) and reactive power (Qrc) of three phase system can be calculated using equation (3.9) and (3.10) as follows [45]:

$$P_{ac} = I_1 * V_1 + I_2 * V_2 + I_3 * V_3 \tag{3.9}$$

$$Q_{rc} = \frac{1}{\sqrt{3}}((I_1 - I_2) * V_3 + (I_3 - I_1) * V_2 + (I_2 - I_3) * V_1) \tag{3.10}$$

Where, I1, I2, I3: are the current in leg 1, leg 2 and leg 3 respectively, V1, V2, V3: are the voltage in leg 1, leg 2 and leg 3 respectively.

3.4.3 MMC Switching Modulation

The switching modulation is the synchronization process with the reference voltage and frequency. The typical multi-level switching techniques are divided into two parts [34] as asynchronous and synchronous modulation strategies. These are illustrated in Figure 3.11.

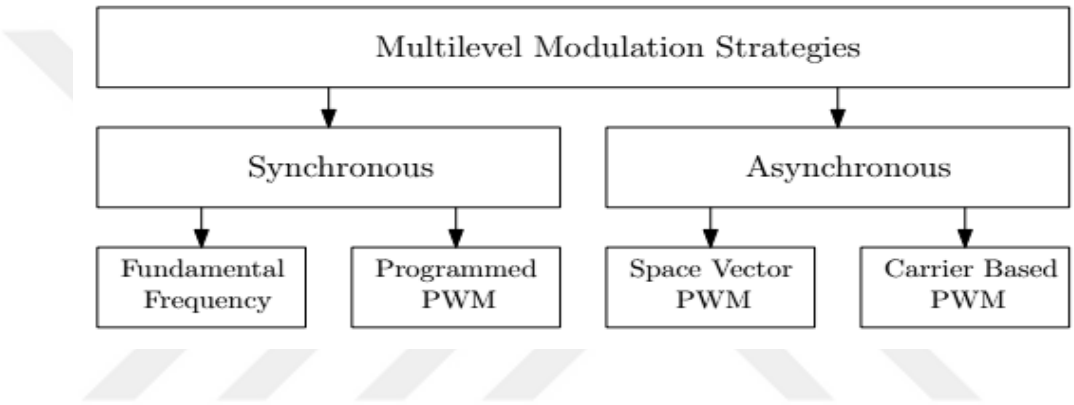


Figure 3.11: Modular Multilevel Converter Switching Methods [34]

3.4.3.1 Fundamental Frequency Modulation (FFM)

Fundamental Frequency Modulation (FFM) is a slow switching modulation that makes only one commutation per cycle. This modulation is used for slower switching semiconductors like gate turn-off thyristors (GTOs) [46].

The principle of FFM is suitable for controlling MMCs, and due to half-wave symmetry, only 0.5(n-1) firing angles can be calculated for an (n-level) converter. Because there's just only one commutation per cycle, the FFM modulation gives odd harmonic components. The harmonics for n-level phase voltage is given as: [35, 46]:

$$\mathcal{F}_k = \frac{4}{\pi k}\frac{U_{DC}}{2}\frac{2}{n-1}\sum_{i=1}^{m} cos(k\alpha_i) \tag{3.11}$$

In [47], an optimization algorithm has been presented to eliminate harmonics, in which the firing angles that lead to the minimum harmonic content have been calculated. These m firing angles are required to be calculated for every modulation index mf. Figure 3.12 illustrates the standard phase voltage in a 3-level converter, using turn-on firing angle α1. Due to symmetry, the turn-off angle is π − α1.

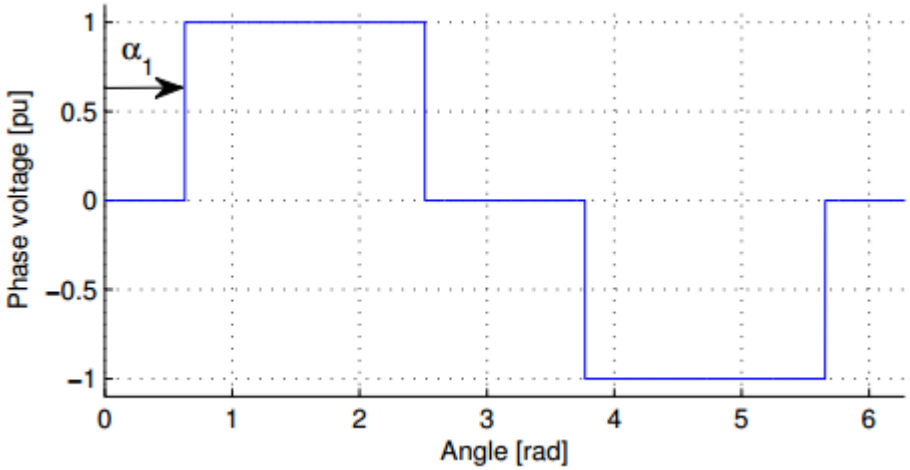


Figure 3.12: Fundamental Frequency PWM with one turn-on angle α_1 [35]

3.4.3.2 Programmed PWM

The technique of programmed PWM is a more advanced FFM, which is also known as Selective Harmonic Elimination (SHE). The procedure is to remove additional harmonic components by presenting further notches in between the turn-on and the turn off angle. Every notch is especially made to remove the required harmonic components, that is a single harmonic component for every notch angle. The more degree of angles, the more will be the voltage shape similar to the classical PWM pattern [48].

Figure 3.13 shows the addition of one notch. The width of notch and its position can be calculated in the optimizing process to minimize the harmonic components. As shown in Figure 3.13, three angles should be calculated: The original turn-on angle α_1, and the angles (α_2 and α_3) of the notch. Using Fourier analysis, the three non-linear equations are required to be solved. These are given as [35]:

$$cos(\alpha_1) - cos(\alpha_2) + cos(\alpha_3) = \frac{4}{\pi} m_a \quad (3.12)$$

$$cos(5\alpha_1) - cos(5\alpha_2) + cos(5\alpha_3) = 0 \quad (3.13)$$

$$cos(7\alpha_1) - cos(7\alpha_2) + cos(7\alpha_3) = 0 \quad (3.14)$$

where m_a is the modulation index.

Thus, from these equations, the angles are depending upon ma of the reference voltage signal, in which the 5th and 7th harmonic components can be eliminated. The 3rd harmonic isn't included due to natural elimination in symmetrical 3-phase systems [35].

Programmed PWM certainly is the most efficient way to minimize harmonic components where low switching frequency is used. The quantity of switching operations is reduced to precisely the quantity required for the specified harmonic elimination. By using this method, the switching losses are reduced. The disadvantage is the big data capacity that is required to recalculate each of the angles for every operating state, especially through transient states. Moreover, the switching losses will be raising as the number of notches are increasing [49].

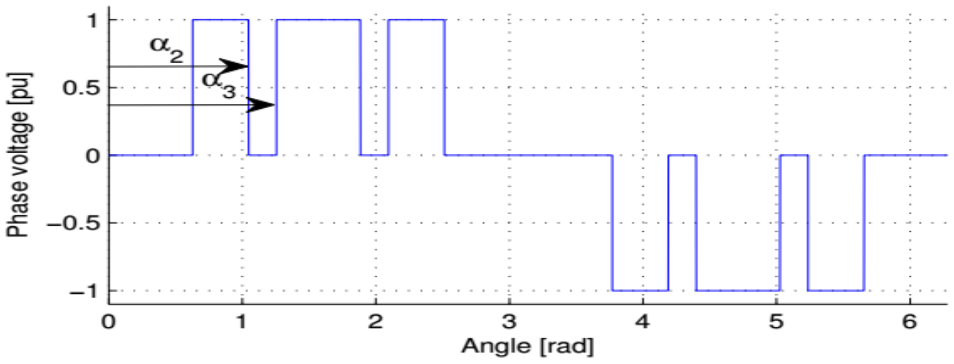


Figure 3.13: Selective harmonic elimination with Programmed PWM: Fundamental frequency output with one notch added for elimination of two harmonic components [35]

3.4.3.3 Carrier Based PWM

The Carrier Based PWM is a high frequency switching technique that is commonly considered for MMC because of acceptable performance and simplicity of the implementation. In this method, the carrier frequency is constant, in addition to this, for each switching period, the mean values of output voltage and the reference voltage are equal. To achieve this objective, a scalar method has been utilized that utilizes a reference (modulation) waveform having the desired frequency (high frequency carrier waveform) and the output voltage magnitude. The reference and the carrier magnitudes are compared to generate switching signals [17]. The general types of carrier based scalar PWM are described as follows [17]:

1- Sub-Harmonic (Level-shift) Methods

These techniques need N congruent triangular carriers becoming displaced contiguously within the total dc-link voltage (Vdc). To be able to give a circuit elements balanced exploitation that generate different voltage levels, the carriers peak-to-peak amplitudes are placed similar to one another, (Vdc/N), that is necessary but aren't an adequate condition. They have the a carrier frequency ($f_{c)}$. Carriers will not pass. Based on the phase-shift of carriers with regards to one another, the level-shift methods can be classified into three different sub-methods: the phase disposition or (PD), the phase opposition disposition or (POD) and the alternative phase opposition disposition or (APOD).

I. Phase Disposition (PD) Method

In PD method, each of the carriers are in phase. For example, a MMC having 4 SM per phase arm, the carriers of PD method are displaced in the (Vdc) band. This situation is illustrated in Figure 3.14.

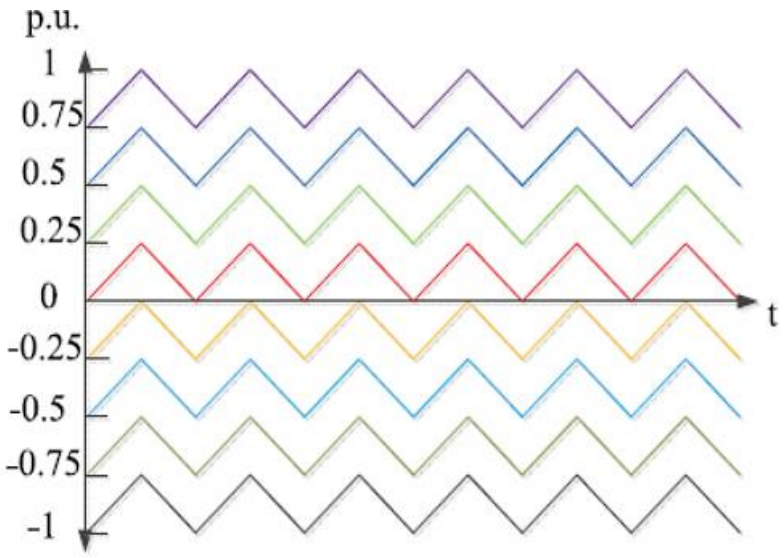


Figure 3.14: Phase disposition (PD) method [17]

II. POD (Phase Opposition Disposition) Method

In POD method, the carriers over the zero axis and under the zero axis are 180° out of phase. For example, the MMC having 4 SM per phase arm, the carriers of phase opposition disposition method are displaced in the V_dc band as shown in Figure 3.15.

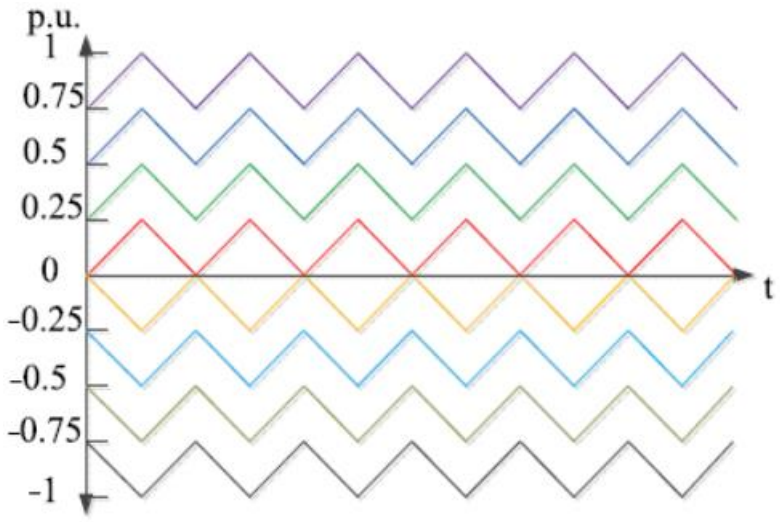


Figure 3.15: POD method [17]

III. APOD (Alternative Phase Opposition Disposition) Method

In APOD method, continuous carriers are 180 degrees out of phase. For example, an MMC having 4 SM per phase arm, the carriers of alternative phase opposition disposition method are displaced in the V_dc band as shown in Figure 3.16.

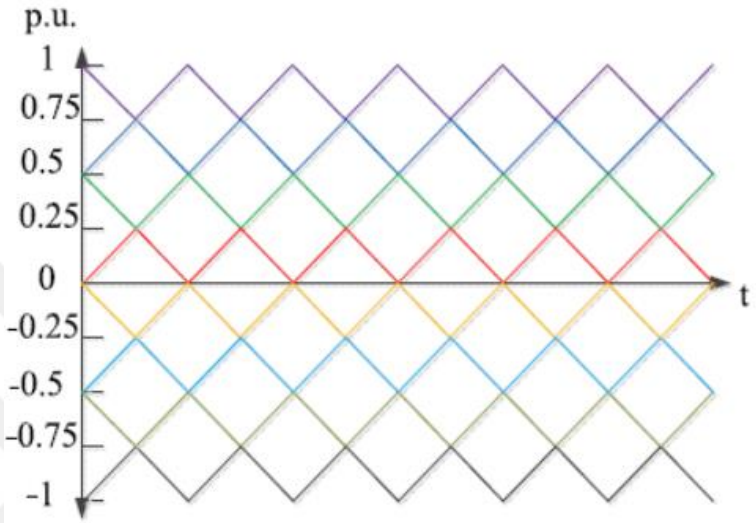


Figure 3.16: APOD method [17]

2- Carrier Disposition (Phase-shift) Method

This technique also needs N similar triangular carriers for being displaced with a (360°/N) phase-shift between each other through the total dc-link voltage; Vdc. The carriers have a frequency of f_c and peak-to-peak V_dc amplitude. Carriers pass one another. For example, the MMC having 4 SM per phase arm, the phase-shift method (PS) carriers are displaced in the V_dc band as shown in Figure 3.17.

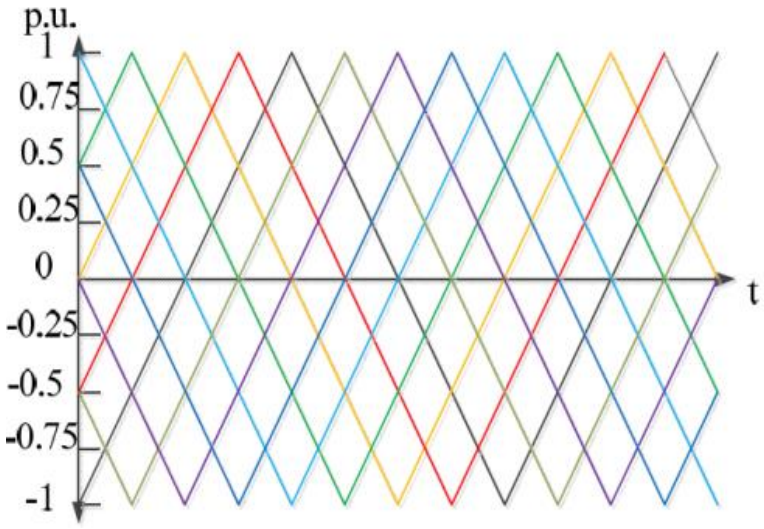


Figure 3.17: PS method [17]

Besides triangular waveforms, there are another waveform rather than triangular which is saw-tooth waveforms and it is known as "saw-tooth rotation". For example, the MMC having 4 SM per phase, carriers of saw-tooth rotation method can be illustrated in Figure 3.18.

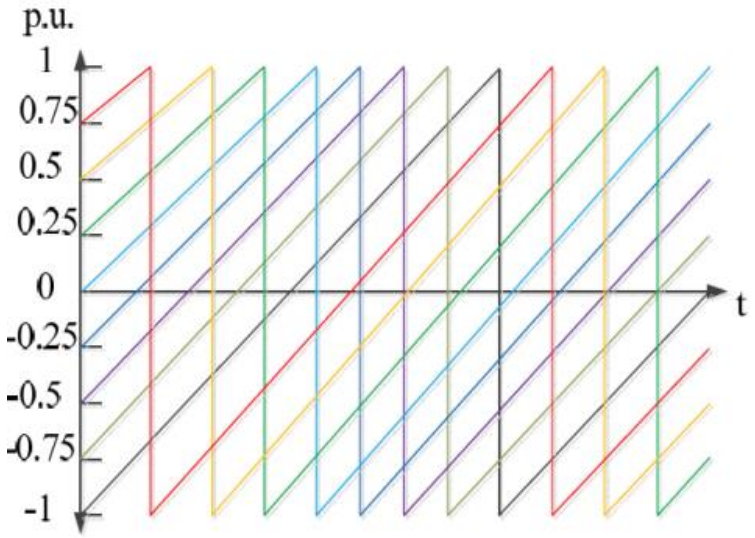


Figure 2.18: Saw tooth rotation method [17]

3.4.3.4 Space Vector PWM

The space vector modulation (SVM) strategy was prepared in the 1980s as a replacement of classical PWM [1]. The space vector modulation has been used to find the switching pulse widths, and it has come to be favored in last years, this because the today's control systems are in digital implementation. The SVM strategy, produces a vector diagram in space for every converter switching condition and the output reference has been represented by a vector. To achieve the required output voltage, the converter is driven through the related switching pulse pattern produced based on the reference vector as well as the switching condition vectors [35].

For the converter of (n-level), there are (n3) switching combinations, which leads to eight combinations for a Two-level converter. Two of those combinations are termed zero-states, this because they short-circuit the AC side of the converter. The other combinations are described as stationary vectors, and then any arbitrary output vector could be created from the stationary vectors from SV -1 to SV-6. Figure 3.19, shows the diagram for a 2-level modulation. For a 3-level converter the quantity of SV is 27 [35].

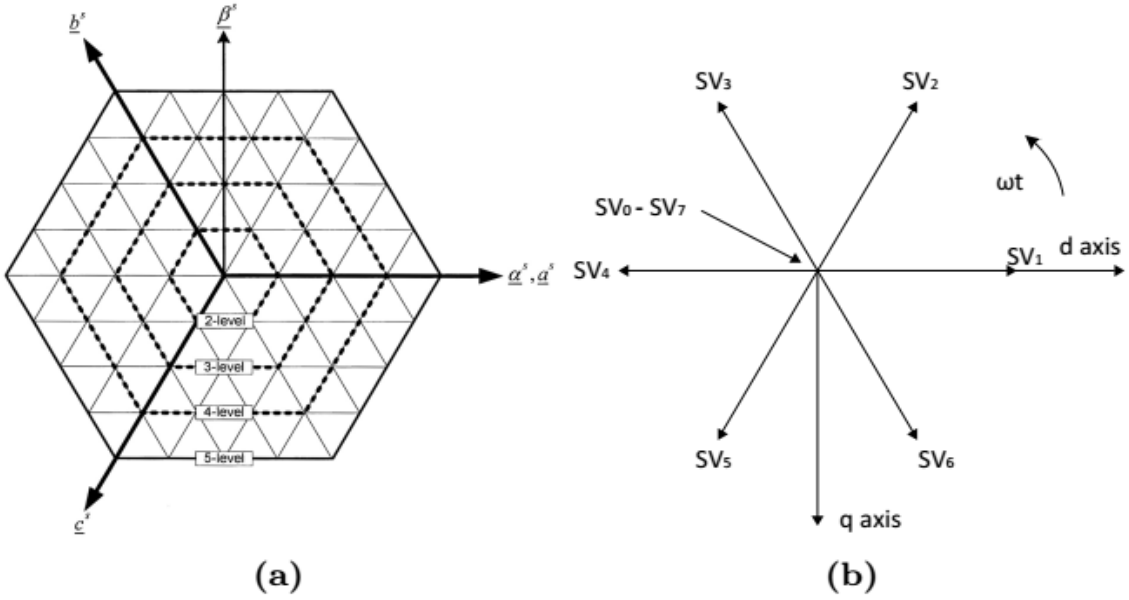


Figure 3.19: Space vector diagram: a) 5-level structure, b) 2-level SVM [35]

Because each switching state corresponds to a SV, the required output is controlled via the duty cycle for every SV. However, each SVM and carrier based scalar PWM methods might generate very similar switching pulse pattern, even so the implementation of Scalar PWM method is easier [50].

3.4.4 Carrier Sets and Number of Output Voltage Levels

For conventional 2 or 3 level converters, the level number of output voltage is fixed. However, this is not true in case of MMC. A MMC converter with N SM per arm can achieve 2N+1 or N+1 output phase-neutral voltage levels. In fact, the situation is dependent upon the "carrier sets" utilized for upper and lower phase arm switching. Two fundamental scalar pulse width modulation (PWM) methods, namely, phase and level shift are commonly utilized. Each method has N number of carriers to form a “carriers set". Switching of lower and upper MMC arms is achieved either using the same carriers set or by two different carriers sets, assuming that there's a predefined phase variation between them. The switching method, only using one set or two or more carrier’s sets for lower and upper arms leads to 2N+1 or N+1 phase-to-neutral voltage levels at the converter output [35].

3.4.4.1 Level Phase Voltages for (N+1) (2N+1) Level-shift Methods

I. PD method

For N+1 level, the PD method needs to be implemented with two various carrier sets for lower and upper arms to be able to form the phase voltage. Initially, the carriers set is organized in a similar way as expressed in 2.4.3.3. Another set of carrier has once more N identical carriers along with amplitude of (V_dc/N) and displaced contiguously in the V_dc band, starting from 0 to V_dc; nonetheless, this carrier set has a phase variation of π radians compared to the first carrier set. SM in lower and upper arms are switching with first carrier sets and second carrier sets. In such cases, output phase voltage will be (N+1) level. Figure 2.20 show the case with PD method for phase leg with 4 SM, the converter equivalent switching frequency, f_{ceq}, is equivalent to the frequency with the level-shifted carriers, as shown in Equation 3.15 [17]:

$$f_{ceq} = f_c \tag{3.15}$$

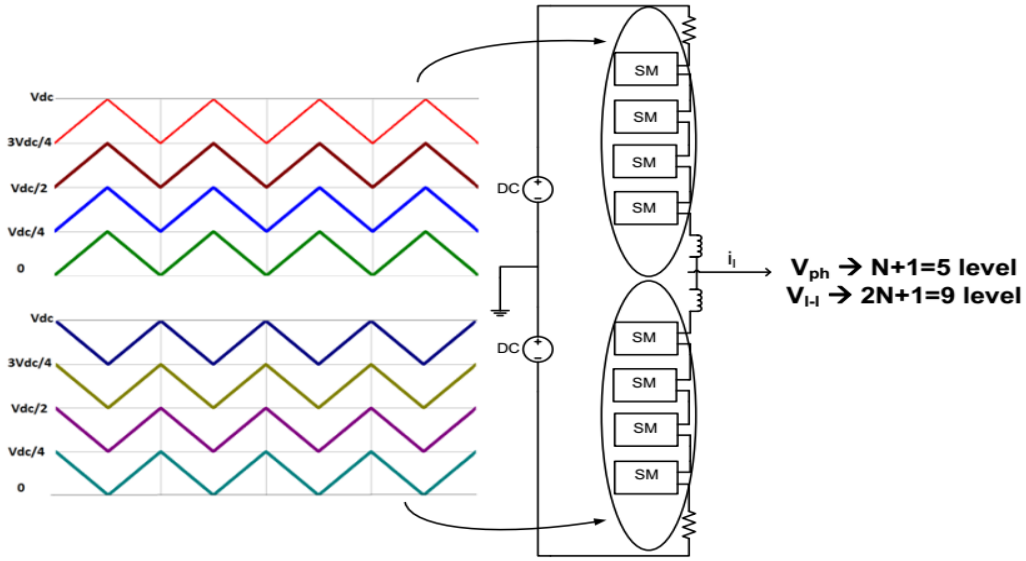


Figure 3.20: Carrier sets for PD method in case (N+1) level phase voltage [17].

For 2N+1 level, the PD method needs to be implemented with a single carrier set for both lower and upper arms to be able to form the phase voltage. Initially, the carriers set is organized in a similar way as expressed in 2.4.3.3. The SM in lower and upper arms are switching with this carrier sets. In such cases, output phase voltage will be (2N+1) level. Figure 3.21 show the case with PD method for phase leg with 4 SM, the converter equivalent switching frequency, f_{ceq}, is equivalent to two time the frequency with the level-shifted carriers, as shown in Equation 3.16 [17]:

$$f_{ceq} = 2 * f_c \tag{3.16}$$

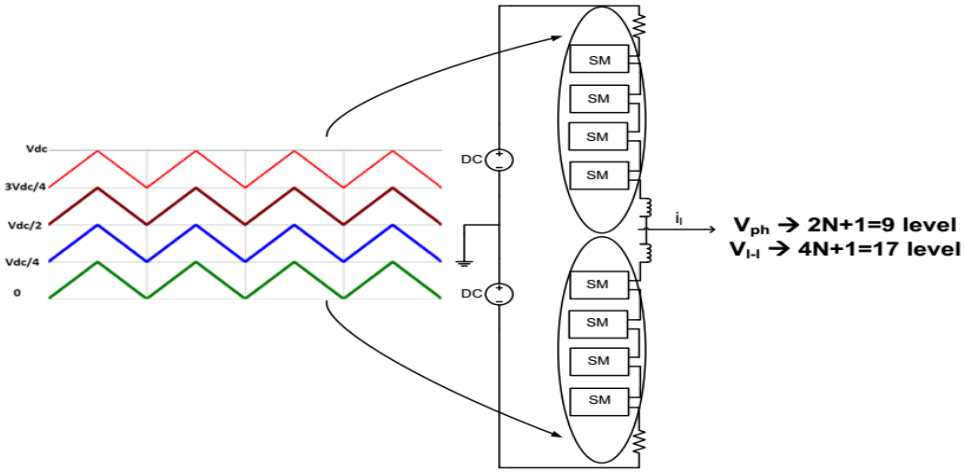


Figure 3.21: Carrier set for PD method in case 2N+1 level phase voltage of [17].

II. POD method

For N+1 level, the POD method needs to be implemented with a single carrier set for both lower and upper arms to be able to form the phase voltage. Initially, the carriers set is organized in a similar way as expressed in 2.4.3.3. The SM in lower and upper arms are switching with this carrier sets. In such cases, output phase voltage will be (N+1) level. Figure 3.22 show the case with POD method for phase leg with 4 SM, the equivalent switching frequency of converter, f_{ceq}, is equivalent to the frequency with the level phase carriers, as shown in Equation (3.15).

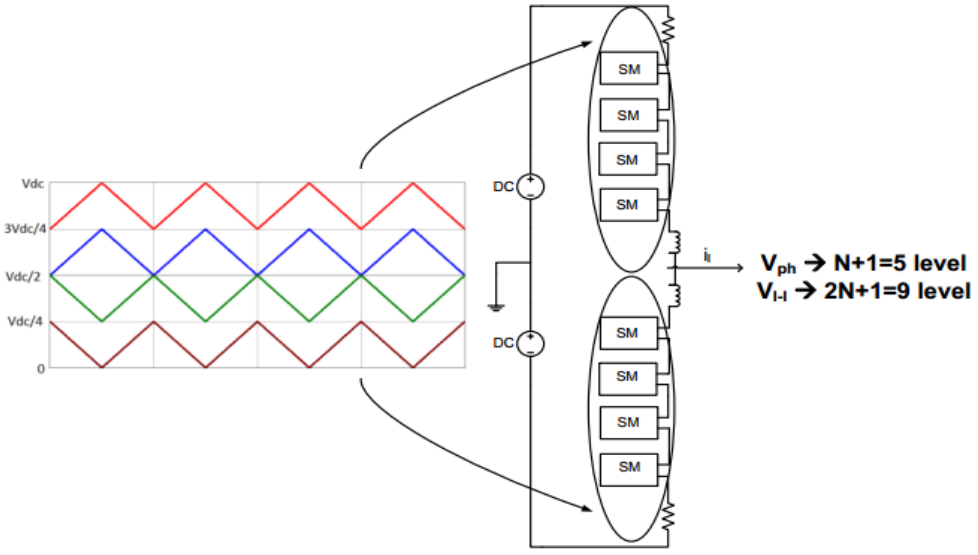


Figure 3.22: Carrier set for POD method in case (N+1) level phase voltage [17]

For 2N+1 level, the POD method needs to be implemented with two various carrier sets for lower and upper arms to be able to form the phase voltage. Initially, the carriers set is organized in a similar way as expressed in 2.4.3.3. Another set of carrier has once more N identical carriers along with amplitude of (V_dc/N) and displaced contiguously in the V_dc band, starting from 0 to V_dc; nonetheless, this carrier set has a phase variation of π radians compared to the first carrier set. SM in lower and upper arms are switching with first carrier sets and second carrier sets. In such cases, output phase voltage will be (2N+1) level. Figure 3.23 show the case with PD method for phase leg with 4 SM, the converter equivalent switching frequency, f_{ceq}, is equivalent to the frequency with the level-shifted carriers, as shown in Equation 3.16.

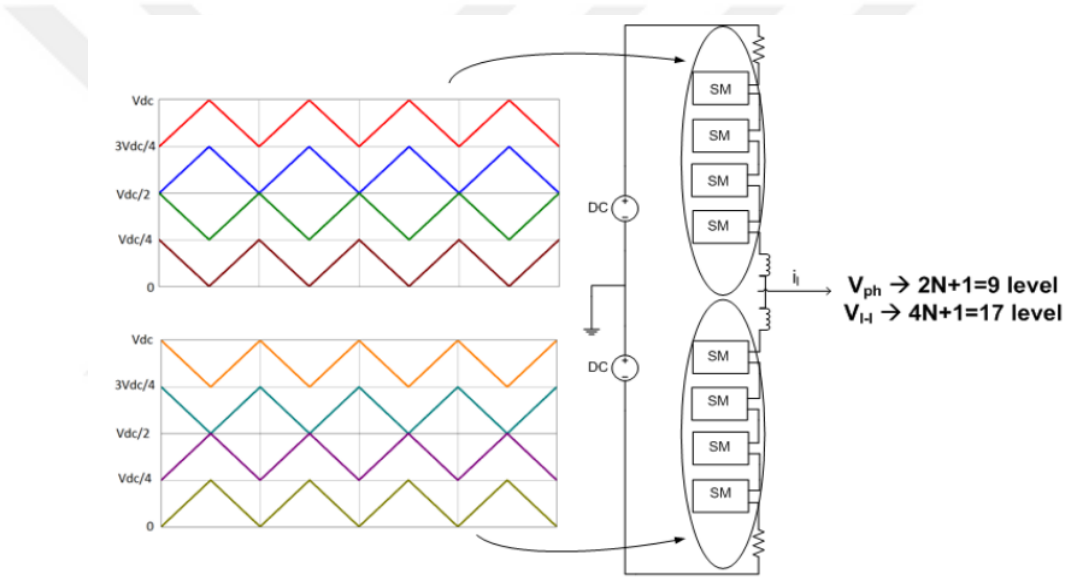


Figure 3.23: Carrier sets for POD method in case 2N+1 level phase voltage [17]

III. APOD method

For N+1 level, the APOD method needs to be implemented with a single carrier set for both lower and upper arms to be able to form the phase voltage. Initially, the carriers set is organized in a similar way as expressed in 2.4.3.3. The SM in lower and upper arms are switching with this carrier sets. In such cases, output phase voltage will be (N+1) level. Figure 3.24 show the case with APOD method for phase leg with 4 SM, the equivalent switching frequency of converter, f_{ceq}, is equivalent to the frequency with the LS carriers, as shown in Equation (3.15).

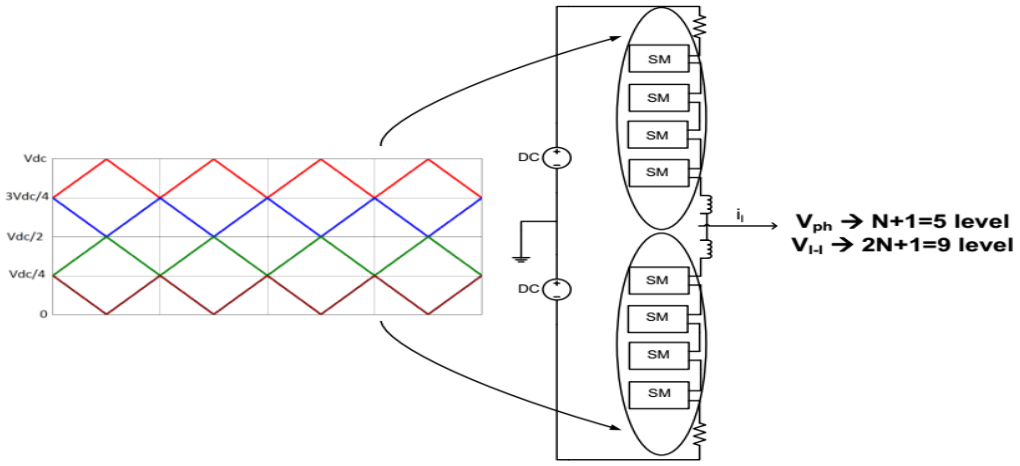


Figure 3.24: Carrier set for N+1 level phase voltage of APOD method [17]

For 2N+1 level, the APOD method needs to be implemented with two various carrier sets for lower and upper arms to be able to form the phase voltage. Initially, the carriers set is organized in a similar way as expressed in 2.4.3.3. Another set of carrier has once more N identical carriers along with amplitude of (V_dc/N) and displaced contiguously in the V_dc band, starting from 0 to V_dc; nonetheless, this carrier set has a phase variation of π radians compared to the first carrier set. SM in lower and upper arms are switching with first carrier sets and second carrier sets. In such cases, output phase voltage will be (2N+1) level. Figure 3.25 show the case with APOD method for phase leg with 4 SM, the equivalent switching frequency of converter, f_{ceq}, is equivalent to the frequency with the level-shifted carriers, as shown in Equation 3.16 [17].

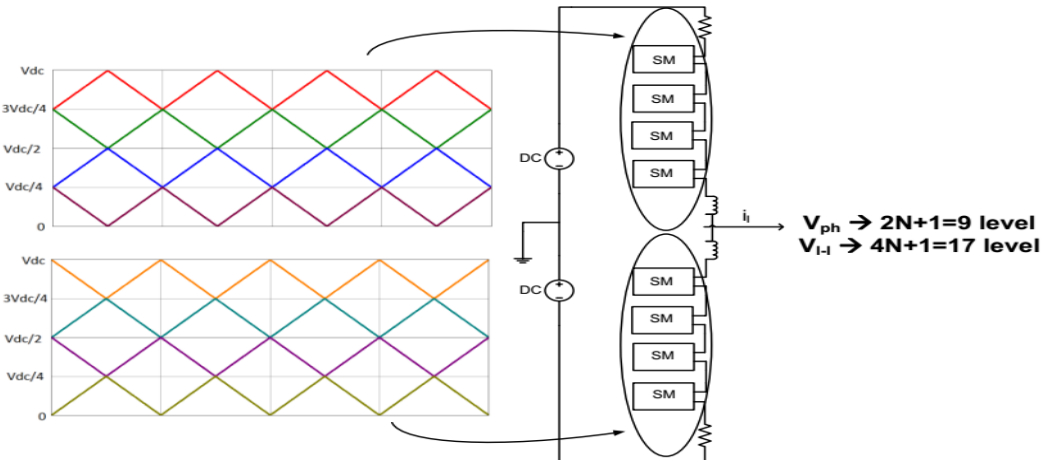


Figure 3.25: Carrier set for APOD method in case 2N+1 level phase voltage [17]

3.4.4.2 Level Phase Voltages for (N+1) (2N+1) phase-shift Methods

I. (N+1) Phase-shift Methods

For phase-shift strategy, carrier sets are organized based on N becoming even or odd. When N is odd, it should be used two different carrier sets for lower and upper arms. 1st carriers set is organized in a similar way as expressed in section 2.4.3.3. The 2nd carriers set is organized in the similar waveform, but with radians phase difference of π/N when compared with the first set. SM in lower and upper arms are switched using these 1st and 2nd sets of carrier. The output phase voltage of this case is (N+1) level. Figure 3.26 shows the case with phase-shift when N is odd (the phase leg has N=3) [20, 51]. When N is even, only one set of carrier can be used for both lower and upper arms. This set of carrier is the same as what explained in section 2.4.3.3. The SM in lower and upper arms are switched using this carrier set. The output phase voltage for this case is (N+1) level. Figure 3.27 shows the case with phase-shift method for case when leg has N=4. For both two cases, the equivalent switching frequency of converter, f_{ceq},, equals to the number of carriers times the frequency of PS carriers, that can be calculated by Equation (3.17) [17]:

$$f_{ceq} = N * f_c \tag{3.17}$$

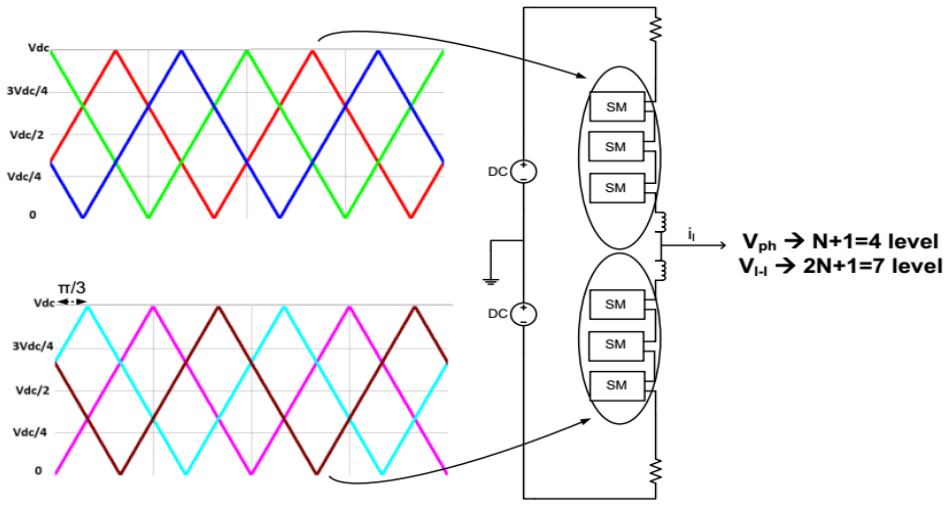


Figure 3.26: Carrier sets for phase-shift method in case of (N+1) level phase voltage with submodules of odd number [17]

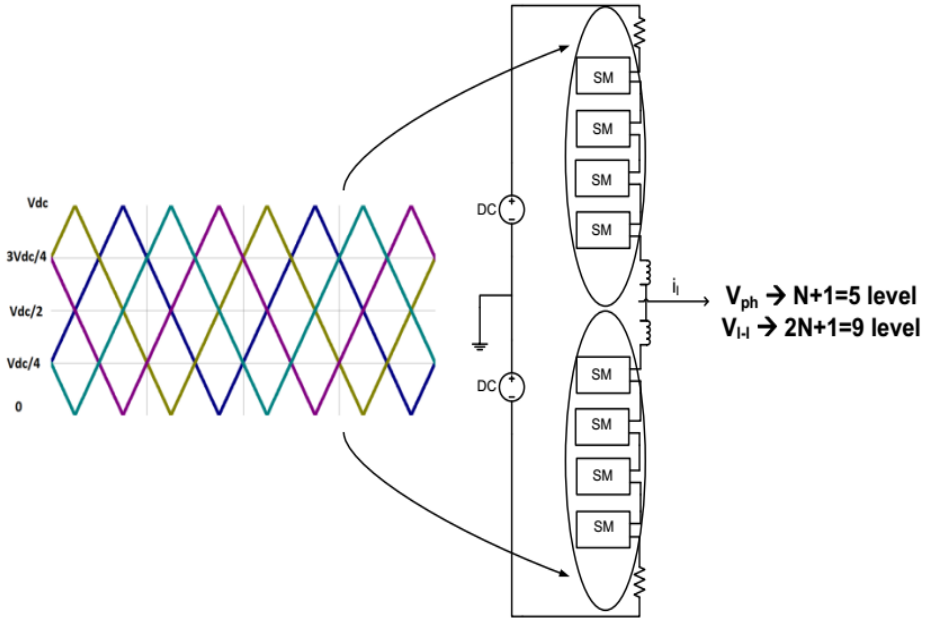


Figure 3.27: Carrier set for phase-shift method of N+1 level phase voltage of with submodules of even number [17].

II. (2N+1) Phase-shift Methods

As described in (N+1) Phase-shift Methods, there are two case odd and even. When N is odd, only one set of carrier can be used for both lower and upper arms. This set of carrier is the same as what explained in section 4.2.1.2. The SM in lower and upper arms are switched using this carrier set. The output phase voltage for this case is (2N+1) level. Figure 3.27 shows the case with phase-shift method for case when leg has N=3. When N is odd, it should be used two different carrier sets for lower and upper arms. 1st carriers set is organized in a similar way as expressed in section 4.2.1.2. The 2nd carriers set is organized in the similar waveform, but with radians phase difference of π/N when compared with the first set. SM in lower and upper arms are switched using these 1st and 2nd sets of carrier. The output phase voltage of this case is (2N+1) level. Figure 3.29 shows the case with phase-shift when N is even (the phase leg has N=4). For both two cases, the equivalent switching frequency of converter, f_{ceq},, equals to the number of carriers times the frequency of PS carriers, that can be calculated from Equation (3.18) [17].

$$f_{c\_eq} = 2N * f_c \tag{3.18}$$

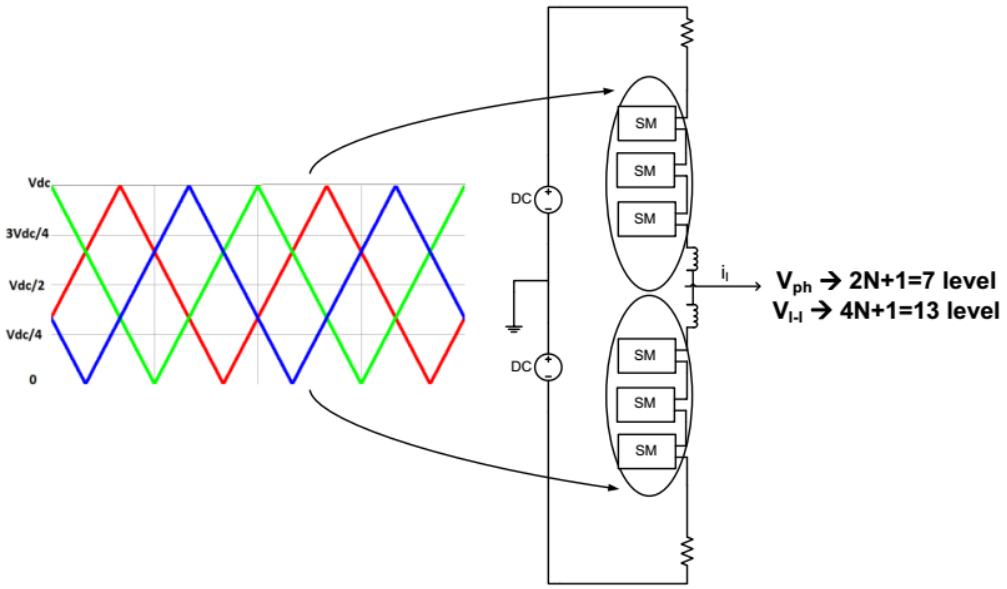


Figure 3.28: Carrier sets for phase-shift method for case of 2N+1 level phase voltage with odd number of submodules [17]

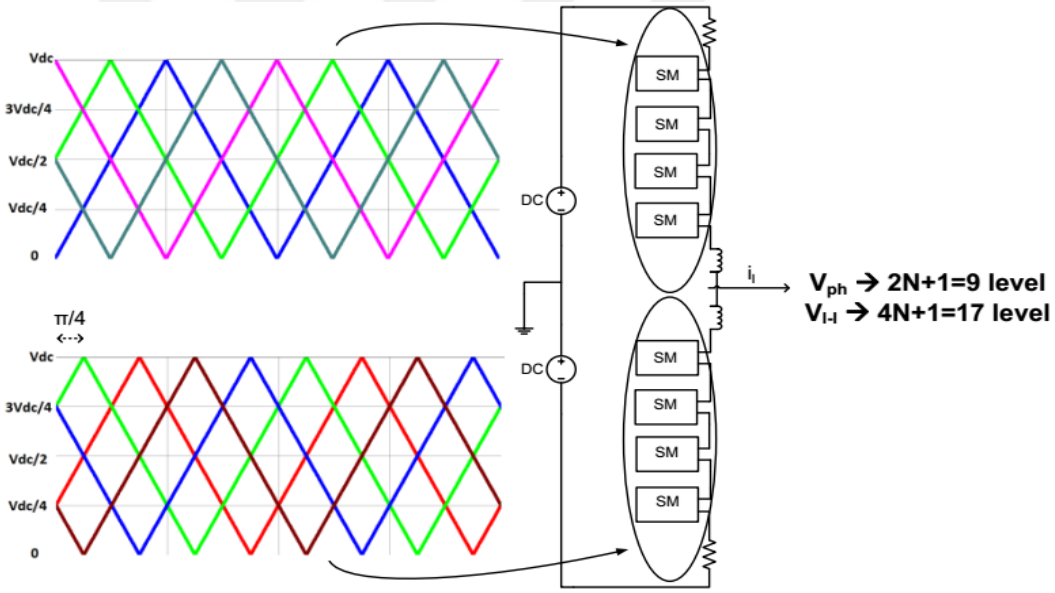


Figure 3.29: Carrier sets for phase-shift method for case of 2N+1 level phase voltage of with even number of submodules [17]

3.5 Power Quality- Standards

The IEEE Standard 519 [52] details the appropriate standards for harmonic control and power quality, which is focused on the (PCC) that is the point in the power system in which several customers or several electrical loads might be connect. This standard determines the distortion limits for various PCC voltage levels. Two essential

indexes defined in the standard which are: the individual harmonic distortion called (Dn) and the total harmonic distortion that called (THD). Dn is the percentage of the fundamental, and the THD is the square root of all individual harmonic distortions [53].

THD is the summation of total harmonic components of the voltage or current waveform in comparison with the essential component of the voltage and current wave. THD is generally computed by getting the root sum of the 1st five or six harmonics squares of the standard. In several practical cases, there's negligible error as soon as just the 2nd and 3rd harmonics are included, so long as the greater harmonics are three to five times lesser than the greatest harmonic [54]. For case that the measurement signal is related to power calculating. The THD can be calculated from equation 3.19 [54]:

$$THD(\%) = \ 100 * \sqrt{\frac{P2+p3+P4+\cdots+Pn}{P1}} \tag{3.19}$$

For case that the measurement signal is related to voltage calculating. The THD can be calculated from equation 3.20 [54]:

$$THD(\%) = \ 100 * \sqrt{\frac{V2+V3+V4+\cdots+Vn}{V1}} \tag{3.20}$$

For case that the measurement signal is related to current calculating. The THD can be calculated from equation 3.21:

$$THD(\%) = \ 100 * \sqrt{\frac{I2+I3+I4+\cdots+In}{I1}} \tag{3.21}$$

Where Pn in watts, Vn in voltage, n: is harmonic number, n = 1 is the test signal main frequency.

CHAPTER 4

HVDC SYSTEM SIMULATIONS

4.1 Introduction

This chapter presents the procedure for simulating the MMC based HVDC transmission system with five SMs per arm in the simulation platform. First, a single-phase open-loop system is designed. After the verification of this system, the control of AC-side current has been implemented for the 3-phase multi-level convertor and its closed-loop dynamic performance is verified.

4.2 System Design Method

The simulation model of the MMC based HVDC transmission system, taken from the literature is used as a base model in this study [55]. The simulation model consists of two power system works in a bi-directional way. Each system has a power source that is connected to AC grid. Two systems are connected via HVDC transmission line.

Each station of the HVDC transmission system has a MMC, which is a bi-directional VSC that interfaces the high-voltage AC and DC side of the systems. It comprises a positive and negative arm for each of the three phases. The number of SM cells of in the MMC is configured to be five per arms. Each SM is composed of one half-bridge and a DC-link capacitor. Each single phase arm has one inductor and one resistor for filtering. The DC sides of the two AC networks are connected via two DC transmission lines which are modelled using PI-section line component. The model of left-side MMC and right-side MMC are illustrated in Figure 4.1 and Figure 4.2, respectively.

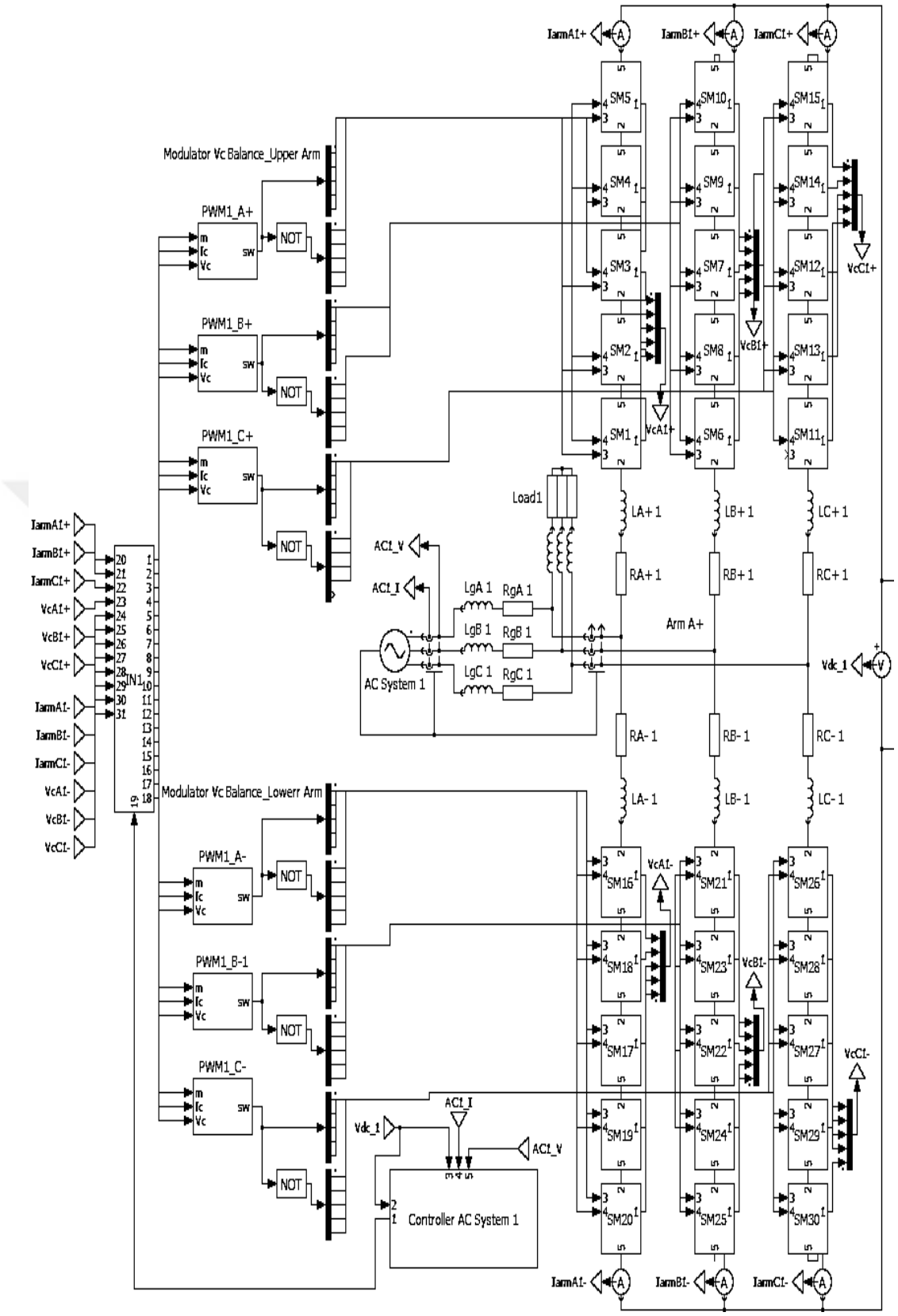


Figure 4.1: The Model of Left-Side MMC

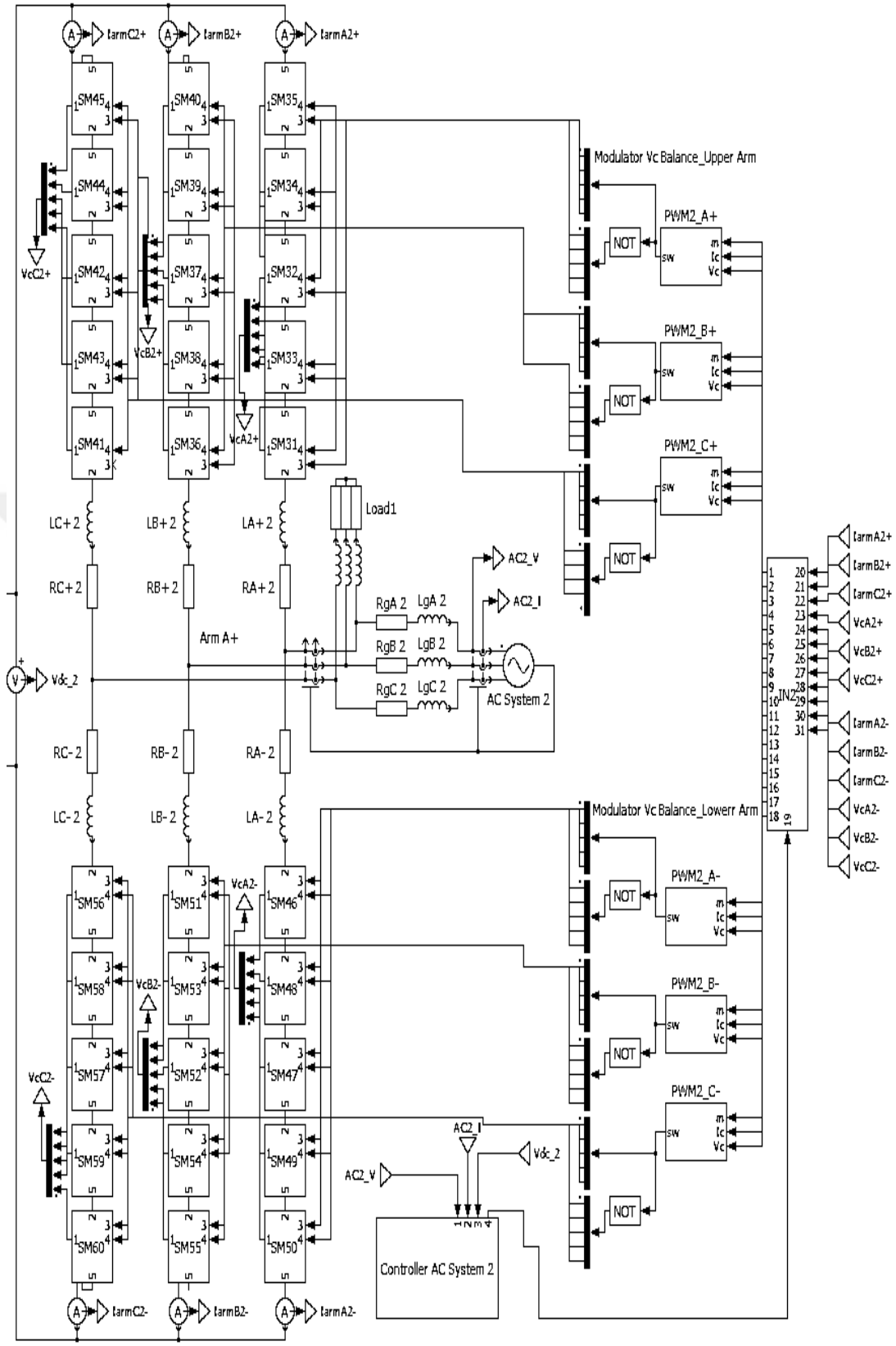


Figure 4.2: The Model of Right-Side MMC

4.3 MMC Control Scheme

The MMC upper control level composed from two loops: The controller of outer loop (PI) which adjusts the DC link voltage and produces the d-axis reference for the inner control of current loop. The interior current loop controls the d- axis and q-axis grid currents and creates the reference voltages for an MMC legs. The modulator of low level has been assigned for creating the AC voltage depending on the reference as well as active balancing of the SM voltages in same time. the SM selection algorithm, based on work described in [56], is implemented using vertically shifted carriers, ensures that the voltage among all SM of every arm is maintained at about a similar value. The magnitude of the power flow on the DC line can be controlled in both directions. In addition to this, DC link voltage can be controlled at one of the VSC side for proper converter operation.

The control strategy performed for controlled the AC-side current is dependent on d-q frame control and it is illustrated in Figure 4.3. The conversion from the stationary frame provides a cross-coupling concept. To minimize it, a decoupling concept is put into the control scheme to make sure independent voltage control and current by using the d and q axis components. As shown from Figure 4.3, we have been implemented the cross coupling effect cancellation via inner loop of the positive feedback with a gain. Additionally, we have been included the voltage feed-forward in order to acquiring excellent dynamic performance. Moreover, in case the voltage feed-forward choice is not available because of the problems in measuring, the active damping path can be added into the control scheme.

The real power control scheme, shown in Figure 4.3, consists of three controllers. These are DC-link voltage controller, active Power (id) controller and reactive Power (*iq*) controller.

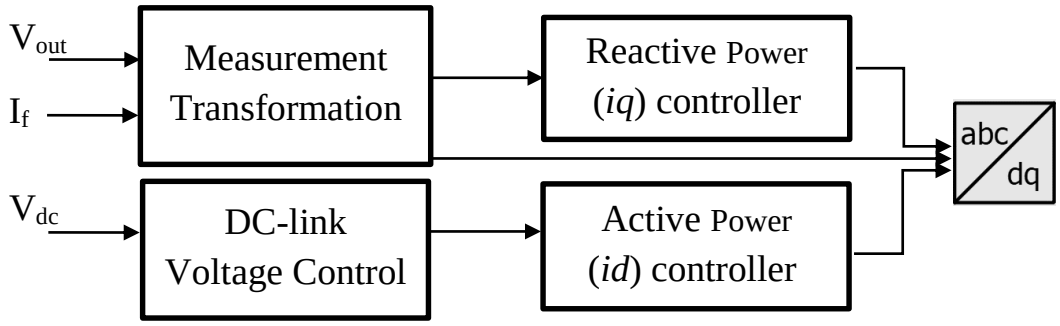


Figure 4.3: Real & Reactive power control System scheme

As seen Figure 4.3, Vout is the AC power generator voltage, If is the AC power generator current, Vdc is the generated DC link voltage. The DC-link voltage controller of system 1 (left-side MMC) is shown in Figure 4.4. It should allow good fault ride-through capability [55].

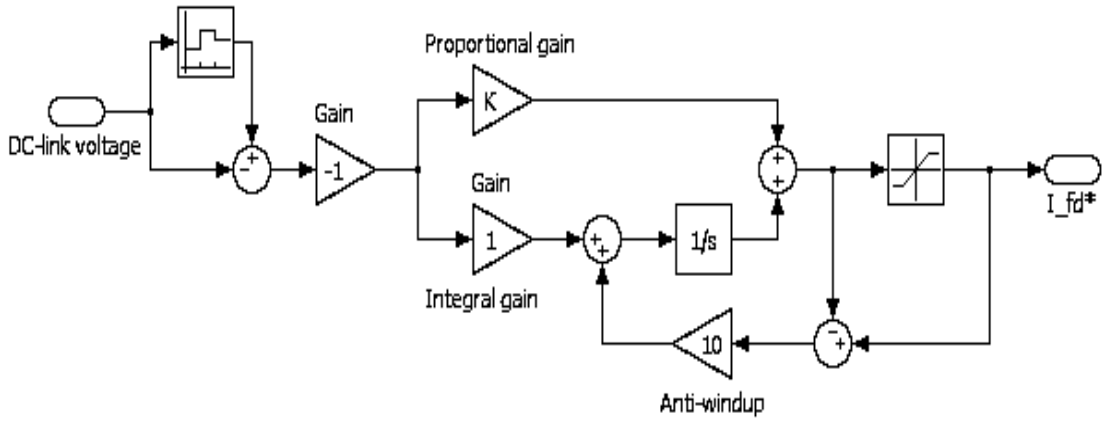


Figure 4.4: DC-link voltage Controller scheme

As shown in Figure 4.4, the DC link voltage passes through the periodic average filter, which is typically averages a continuous input signal through the certain averaging time. The output is update soon after each averaging period. This block is similar to a moving average filter in which output is processed utilizing a zero-order hold. The controller can be guided by using a reference voltage that gives ability to control the DC-link voltage limits.

The measurement transformation block diagram represents the measurement and transformation of sum voltage and arm current that are used to feed both active and reactive Power controller, as shown in Figure 4.5.

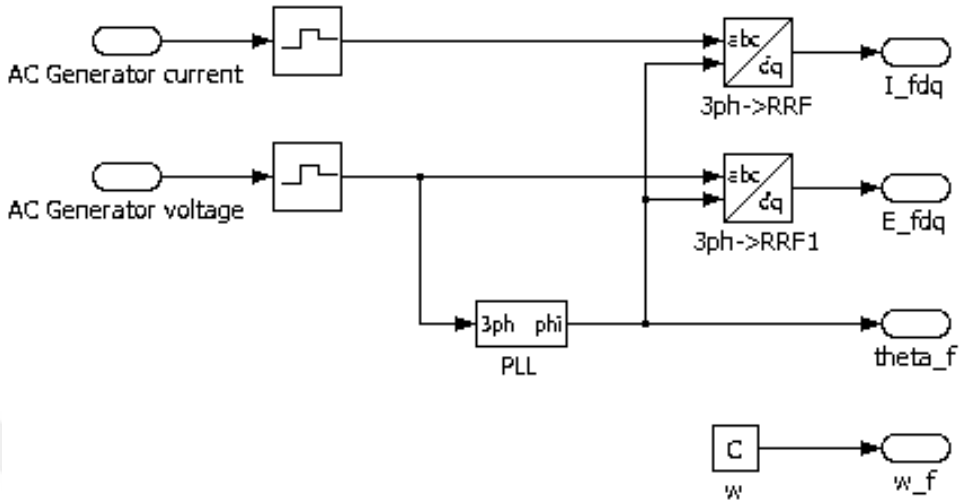


Figure 4.5: d-q transformation scheme

The active Power controller structure is shown in Figure 4.6.

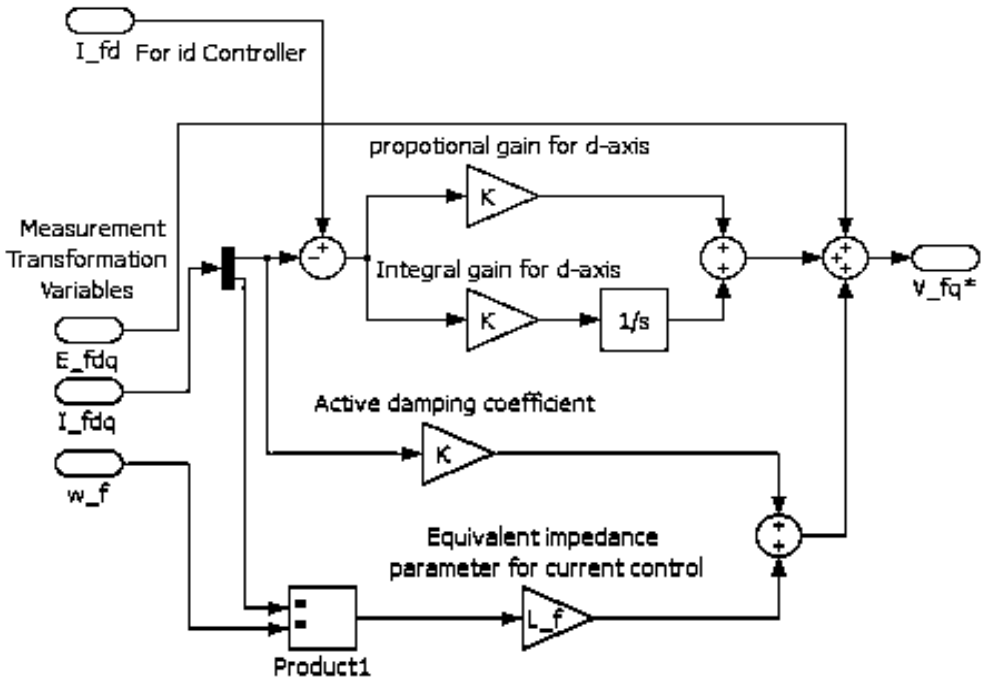


Figure 4.6: Active Power Controller

The reactive Power controller (iq) is shown in Figure 4.7.

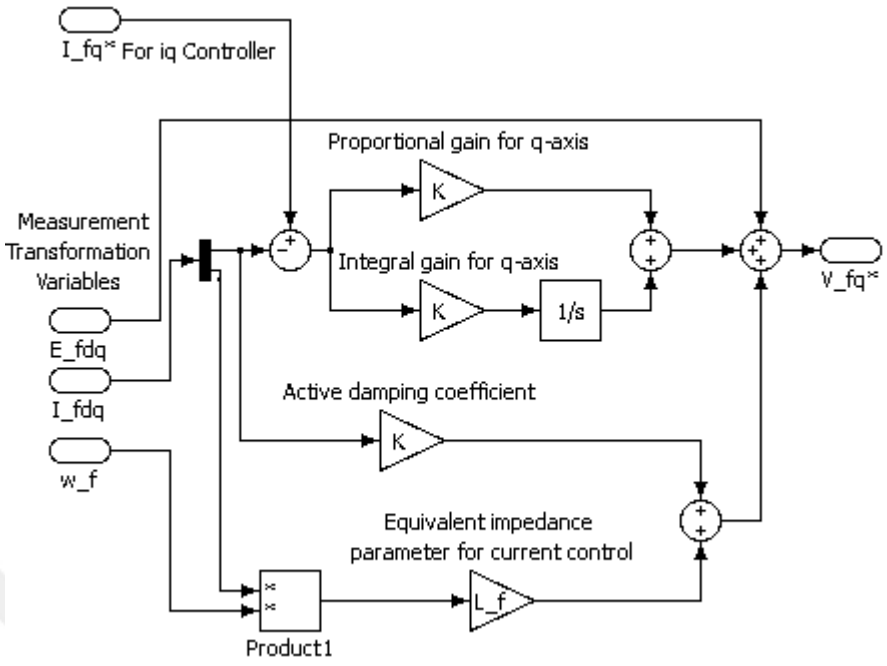


Figure 4.7: Reactive Power Controller Scheme

From Figure 4.6 and Figure 4.7, the proportional gain for d-axis and q-axis, can be calculated by equation 4.1 [55]:

$$K_{pd} = F_{cf} * L_{eq} \tag{4.1}$$

where

K_{pd}: proportional gain for d-axis and q-axis

L_{eq}: the equivalent inductance parameter for current control

F_{cf} , the cut off frequency of PI controller

The L_{eq} can be calculated from equation (4.2):

$$L_{eq} = L_{gq} + \frac{L_{rm}}{2} \tag{4.2}$$

where

L_{rm}: the filter inductance.

L_{gq}: the grid equivalent inductance

The integral gain (Kig) for d-axis and q-axis, in Figure 4.6 and Figure 4.7, can be calculated as:

$$K_{ig} = L_{eq} * (R_{eq} + R_{rc}) \quad (4.3)$$

where

R_{eq}: the equivalent resistance for current control

R_{rg}: the regular active damping coefficient

The equivalent resistance can be calculated from the equation (4.4):

$$R_{eq} = R_{gq} + \frac{R_{rm}}{2} \quad (4.4)$$

where

R_{gq}: the grid equivalent resistance.

R_{rm}: the filter resistance

The regular active damping coefficient (R_{rc}) can be calculated as:

$$R_{rc} = F_{cf} * L_{eq} - R_{eq} \quad (4.5)$$

The active damping coefficient shown in Figure 4.6 and Figure 4.7 is the negative of the regular active damping coefficient, expressed as:

$$K3 = -R_{rc} \quad (4.6)$$

Considering that effective switching frequency is often high, the SM switching loop will be very fast. This aspect is very important in order to avoid overcurrent in fault cases.

4.4 Multi Carrier PWM (MCPWM) and Capacitor Voltage Balance

As explained in Chapter 3, the strategy of carrier-based PWM is based on the comparing and contrasting the reference signal (modulating signal) with the signal of carrier. The carrier has a periodic bipolar or unipolar waveform. The switching instants are usually dependent upon the crossing points of the modulating and carrier signals. As the reference is looked at inside the carrier of waveforms range, the PWM method is considered to be a multicarrier PWM. The implementation of MCPWM in multi-cell converter method is especially useful because of the fact that each carrier could possibly be used on a certain cell that enables separate cell modulation and control. The carriers could be displaced in: Level-shifted PWM, phase-shift PWM, or hybrid of both. The Level-shifted PWM has (N-1) carrier signals using the same amplitude and frequency, in respect each carrier utilizing the feasible output voltage level produced. Depending on how the carriers are positioned, they could be with: phase disposition, phase opposition disposition, alternate phase opposition disposition. In this study we have been used phase disposition PWM method, that illustrated in Figure 4.8.

In phase disposition method, the N triangular carriers have been displaced with regards to the 0-axis that has been compared with reference signal as shown Figure 4.8. This method has lots of downsides like unequal SM capacitor ripple and therefore increased harmonic distortion on the output voltage along with a higher circulating current is often observed. To be able to overcome these downsides, an approach has been combines PD-PWM and a sort and select algorithm, in which the carriers aren't longer tied to every cell [20].

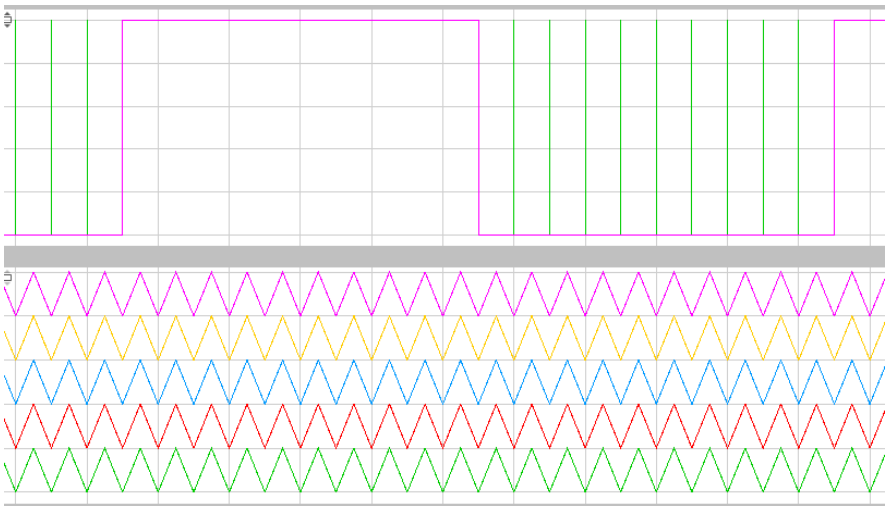


Figure 4.8: Modulator Control Signal.

The logic diagram of PD-PWM controller is shown in Figure 4.9, which is based on the algorithm available in [42]. This controller includes triangle wave generator that generates triangle wave reference depending on minimum and maximum signal value and as well as the cut off frequency. It also includes DC voltage balance that is included in C-script that responsible on voltage balance. The operation of PD-PWM controller can be summarized as follows:

1- Next each step, all of the units need to be rotated in a cyclic direction. This will stop large variations in unit voltages. This may be a challenge in comparison with the staircase modulation. Because the rotation takes place just after one-time period of the main period, but is not via any switching step.

2- From the losses point of view, the units are turned at the lowest rate possible but still are able to create a staircase equivalent output.

3- The level of carriers required for this modulation is equivalent to the number of units per leg.

4- The initialize counter block will begin within the counters in their primary value. Even when no sample time were occurred, the previous values are tested for output. Every time the sample time occurs, the counters has been increased. Every time a counter gets to maximum position it will be reduced till it reaches 0 point in which the method should be restarted with incrimination. When the reference value will be bigger than the carrier the related unit is going to be switched.

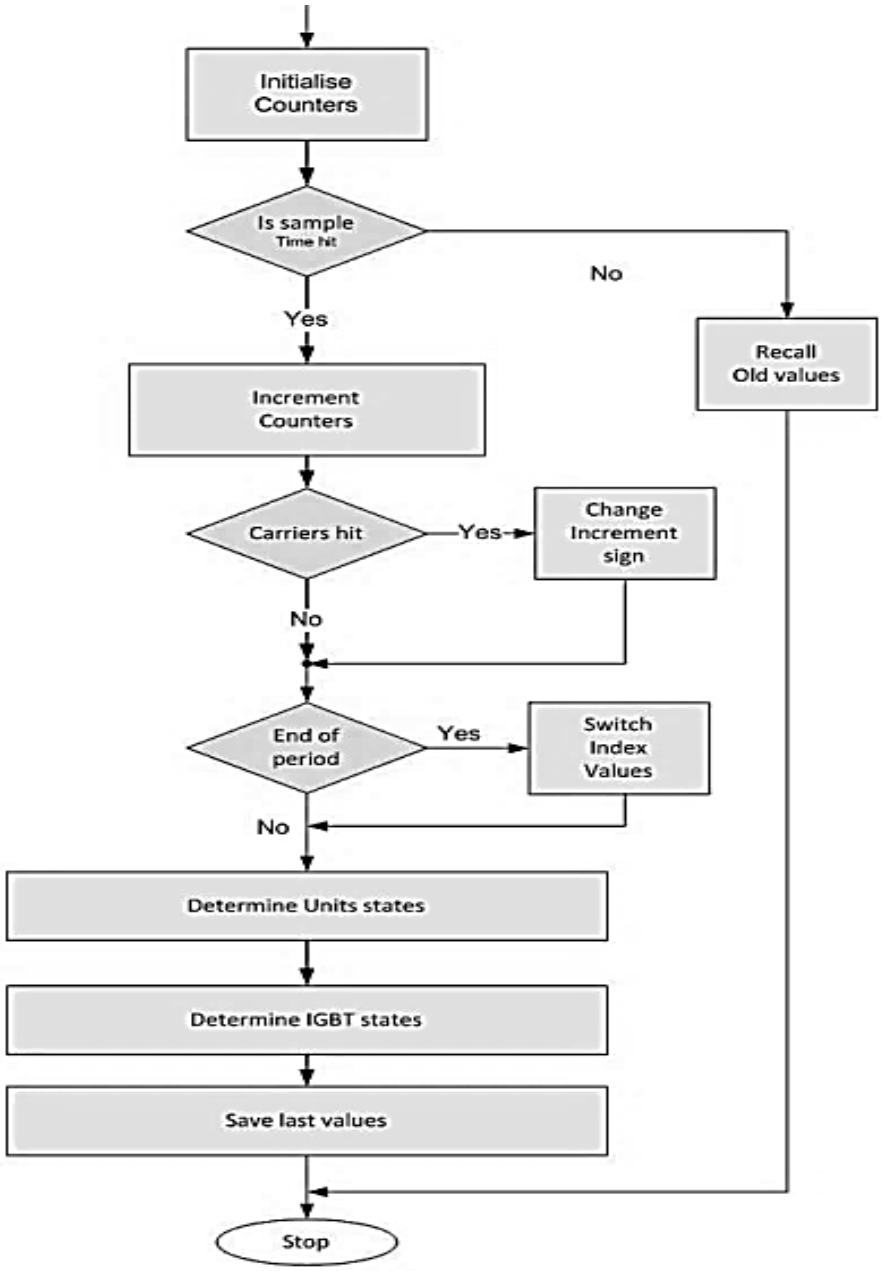


Figure 4.9: Logic diagram of PD-PWM controller [42]

CHAPTER 5

SIMULATION RESULTS

5.1 Introduction

This chapter presents simulation results validating the use of the control concepts for MMC-HVDC transmission system.

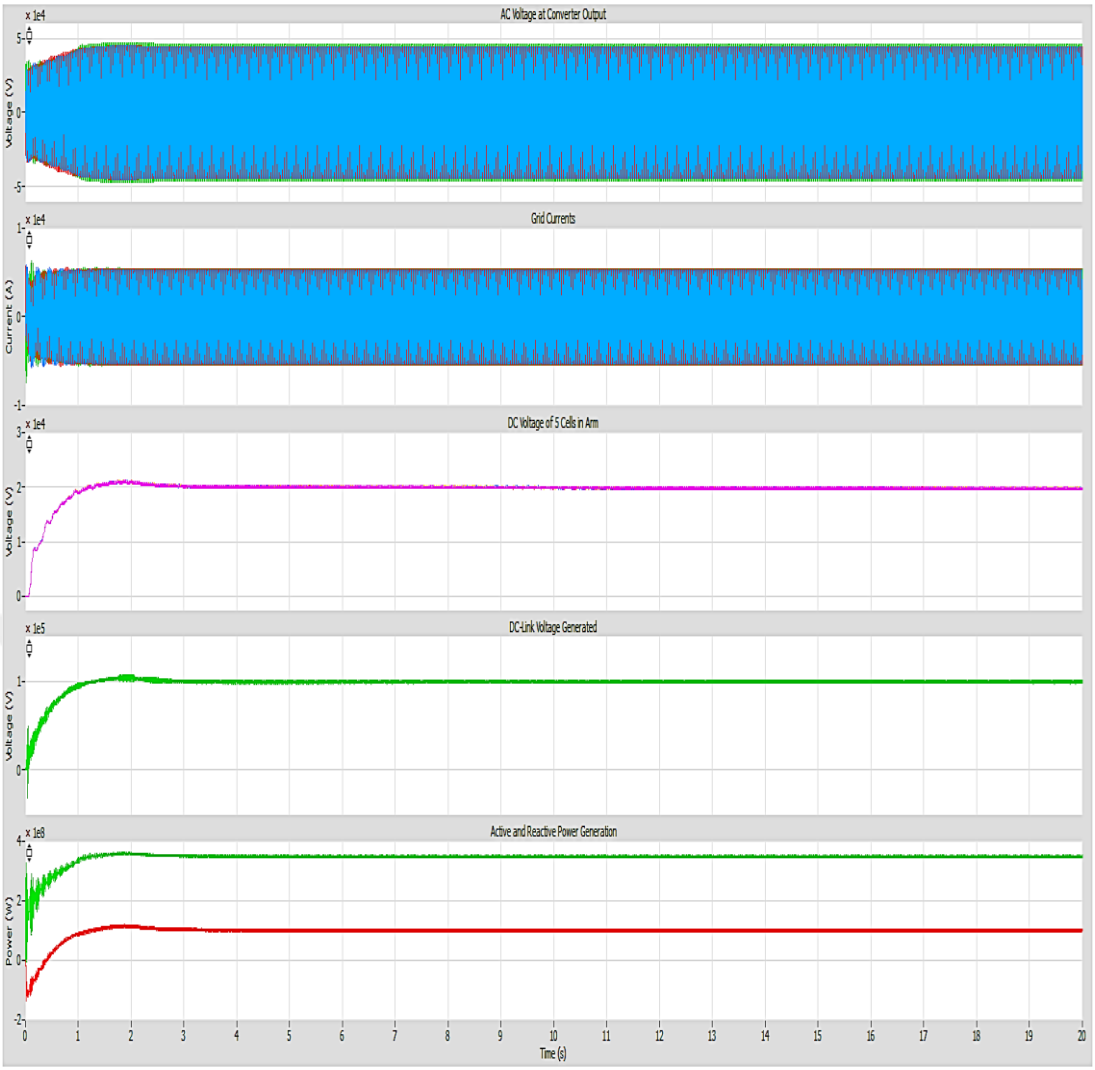
5.2 Simulation Software and Model Parameters

As described in Chapter 4, the simulation system consists of two power sources connected to AC power grid. Transmission voltage level is 136 kV with a frequency of 50 Hz and there is a phase angle offset of $\pi/4$ radians between the two generators in each system. The number of SM cells is configured to be five per arm. Each SM is composed of one half-bridge and a DC-link capacitor. Each single phase arm has one inductor and one resistor for filtering. The DC sides of the two AC networks are connected via two DC transmission lines which are modeled using PI-section line component in long distance of 500 Km. The main parameters of the system model are listed in Table 5.1.

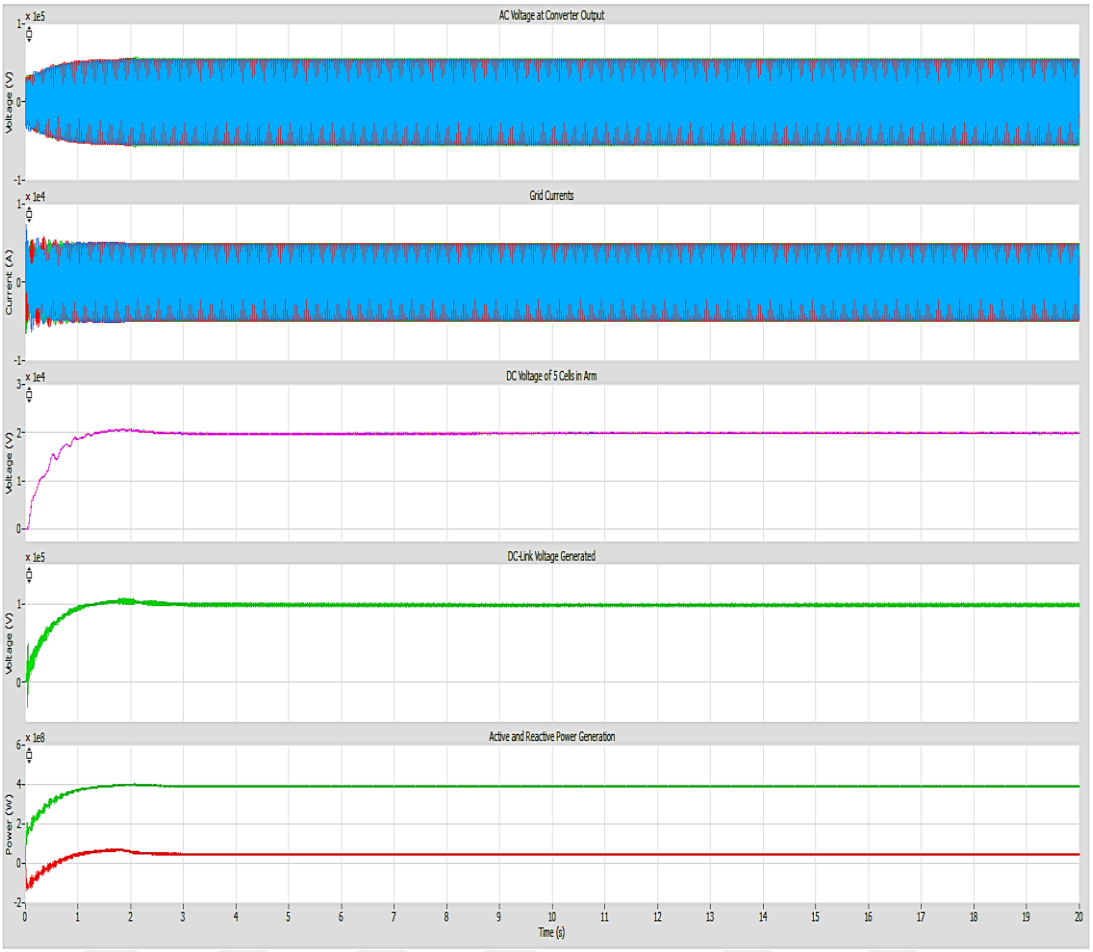
Table 5.1: Simulation parameters

Name of Parameter	Value and Unit
Power	350 (MW)
DC link voltage V_{dc}	100 (KV)
Current	5 (KA)
Peak grid phase voltage	136/sqrt(3)*sqrt(2) (kV)
Number of SM/arm	5
Grid frequency	50 (Hz)
Switching frequency	1 (KHz)
DC bus capacitance	7.2* (mF)
Filter inductance	75 (mH)
Filter winding resistance	0.1 (ohms)
Grid equivalent inductance	75 (mH)
Grid equivalent resistance	0.1 (ohms)
Load resistance	10 (ohms)
Load inductance	1 (mH)

The total simulation time has been selected to be 20 seconds to test all fault conditions and determine the time needs for system to reach its steady-state operating point. Figure 5.1 shows the simulated values of overall system parameters such as voltage, current, cell arm voltages, DC link voltage and active and reactive power of both systems 1 and 2.


AC Voltage at Converter Output
x 1e4
Voltage (V)
Grid Currents
Current (A)
DC Voltage of 5 Cells in Arm
DC-Link Voltage Generated
x 1e5
Active and Reactive Power Generation
x 1e8
Power (W)
Time (s)

(a)



(b)

Figure 5.1: The simulated waveforms: (from up to down) voltage, current, cell arm voltages, DC link voltage and active (green) and reactive (red) signals for (a) system 1, (b) system 2.

As shown in Figure 5.1, the system reaches to steady-state in around 2.4 seconds after a large startup oscillation occurred in about 0.6 seconds that is due to the resonance between arm inductor and the transmission line capacitance.

5.3 System Aspects

In order to investigated the system operation for generating power in bi-directional way, we have been made a case steady for some aspects that is important to investigated how system work and the accuracy of system. These aspects are in follows:

1- AC voltage and current

In this part we have been tested the waveforms of regenerating signal for AC voltage and current for bi-directional operation in both sides to investigate the signal stability and value of distortion that returned to accuracy of voltage and current controller in modulate DC signal to regenerate AC sign wave signal.

2- Cell arm voltages

In this part we have been tested the waveforms in MMC to investigate the accuracy of controller in modulation and guiding switching operation.

3- DC Link voltage

In this part we have been tested the waveforms of DC Link voltage that transfer through DC transmission line to determine the signal distortion and loss in two generation direction.

4- Active and reactive power

In this part we have been tested the active and reactive power generated and regenerated in both side to investigate the power stability and percentage of power loss that related to transmutation via DC transmission line and modulation process.

5- vControlling DC Link and Power generation

In this test we investigated the ability of controller to controlling DC link voltage and power generation limits and direction of generation process

6- Full Active Power Reverse

This test is based on the British grid codes which is mentioned in [51]. According to this code, the time required for full active power reverse in HVDC interconnections is 5 seconds. So this time duration has been used as a reference while testing the model.

5.3.1. Simulation Results of AC Voltage and Current

In this section, AC voltage and current waveforms have been obtained in receiver side and for both directions, then we have been compered the regenerated signal it with the original AC signal from power generator at transmitter side.

System 1 works as transmitter and system 2 works as receiver. In another words, the power generator of system 1 is activated while the power generator of system 2 is deactivated. The simulation results of voltage and current waveform at each MMC are shown in Figure 5.2 and Figure 5.3, respectively.

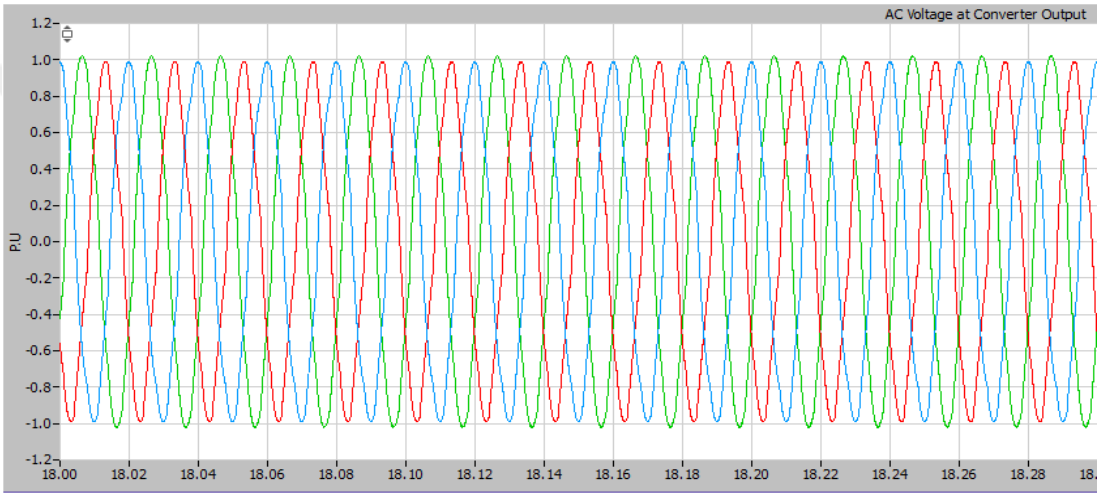


Figure 5.2: Regenerated AC voltage at system 2.

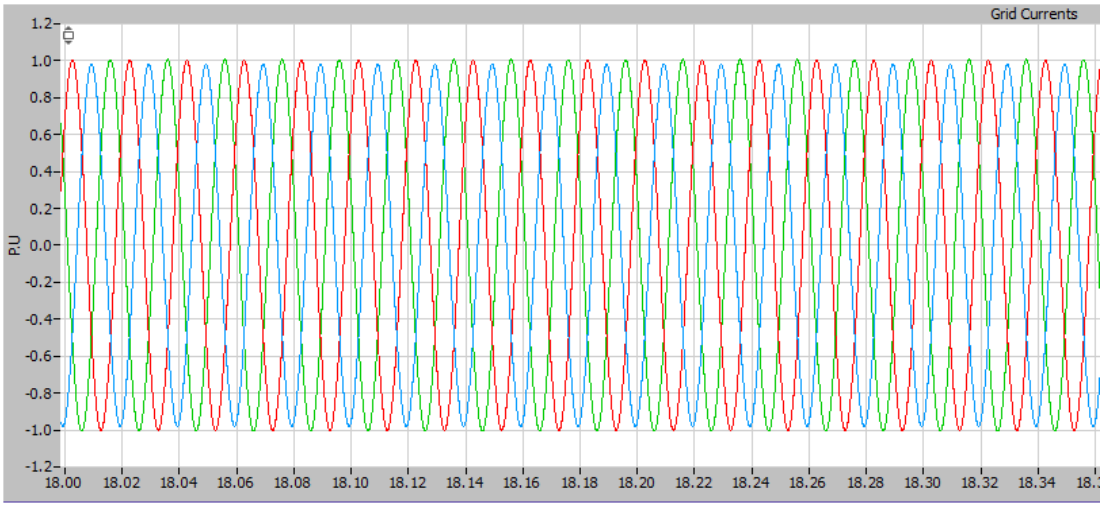


Figure 5.3: Regenerated current at AC system 2.

Now, system 2 works as transmitter and system 1 works as receiver. In another words, the power generator of system 2 is activated while the power generator of system 1 is deactivated. The simulation results of voltage and current waveform at each MMC are shown in Figure 5.4 and Figure 5.5, respectively.

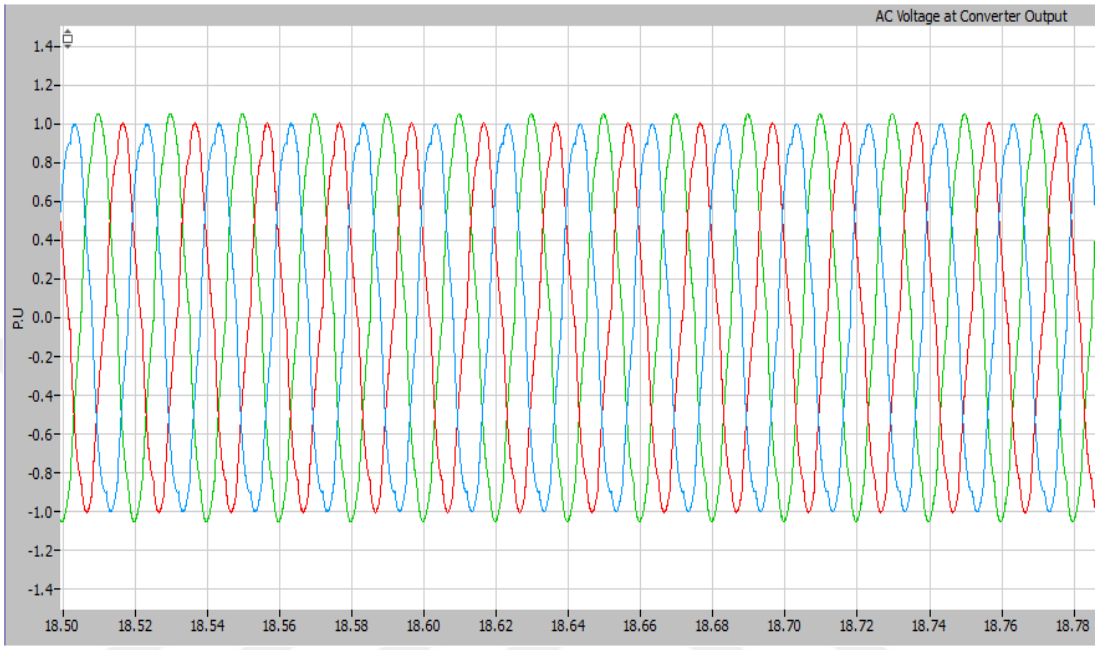


Figure 5.4: Regenerated voltage at AC system 1.

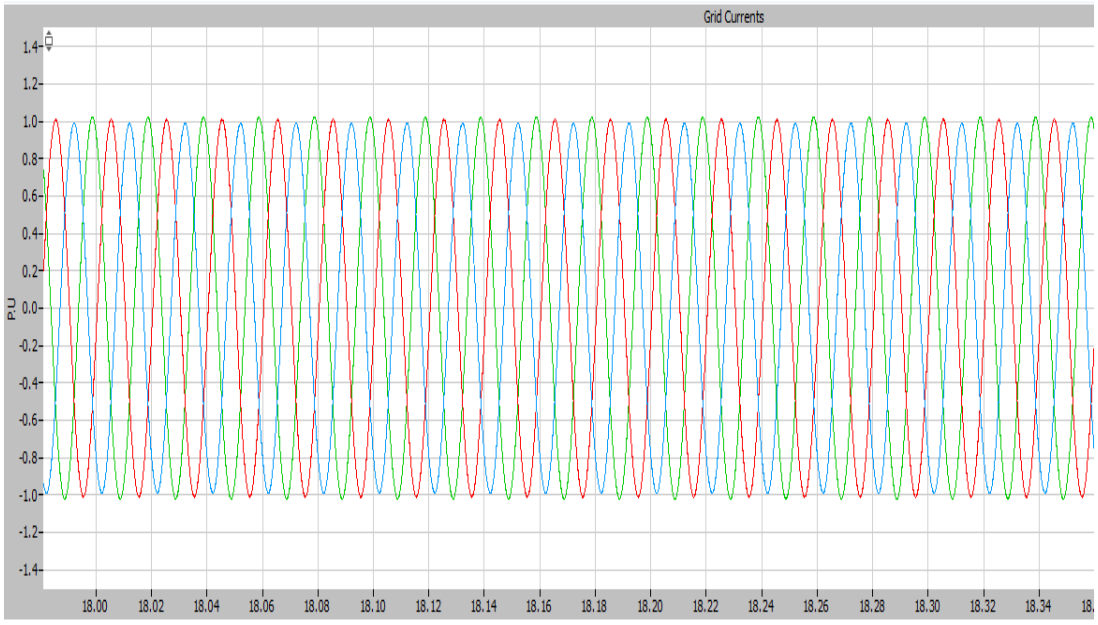
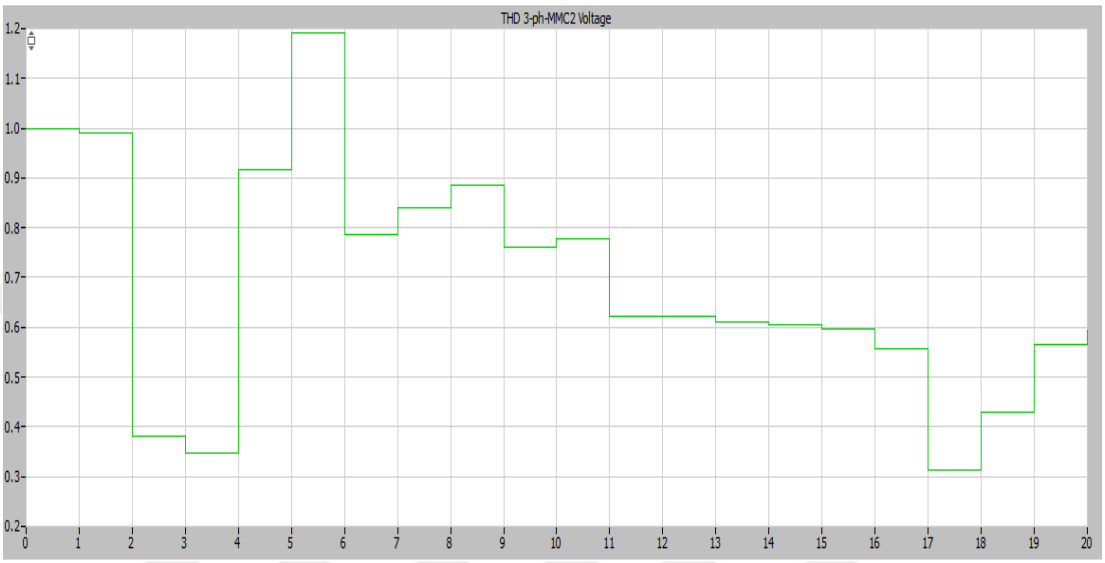
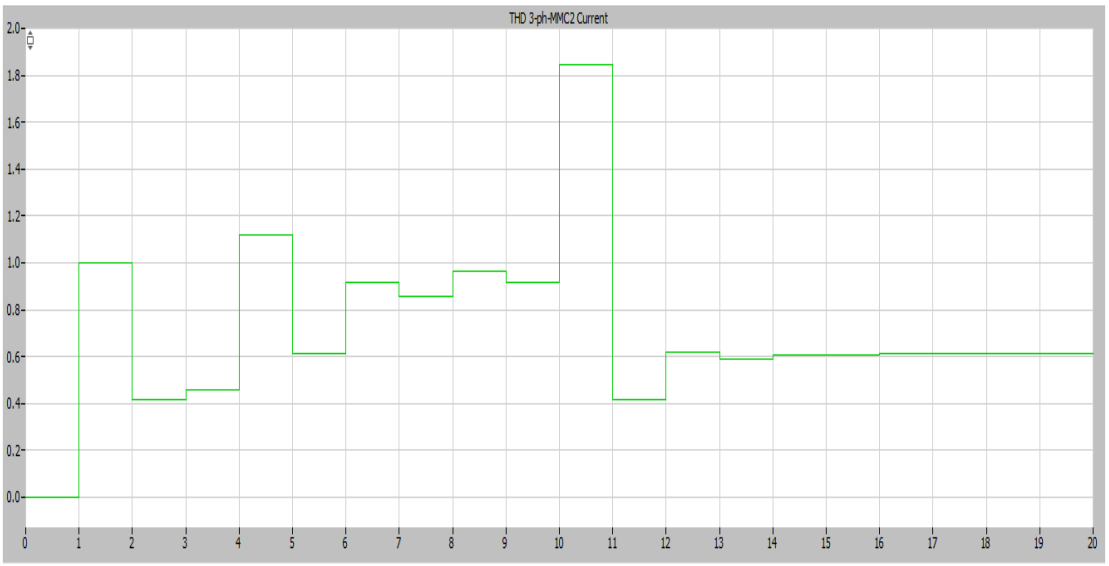


Figure 5.5: Regenerated current at AC system 1.

As seen from Figures 5.2, 5.3, 5.4 and 5.5, it is clear that the waveforms of the regenerated signals are very close to the ideal sinusoidal signal waveforms of the transmitter power generator. To quantitate, harmonic spectrum and THD values of both current and voltage are obtained. The results are shown in Figure 5.6 (a), (b) and Figure 5.7 (a), (b), respectively.



(a)



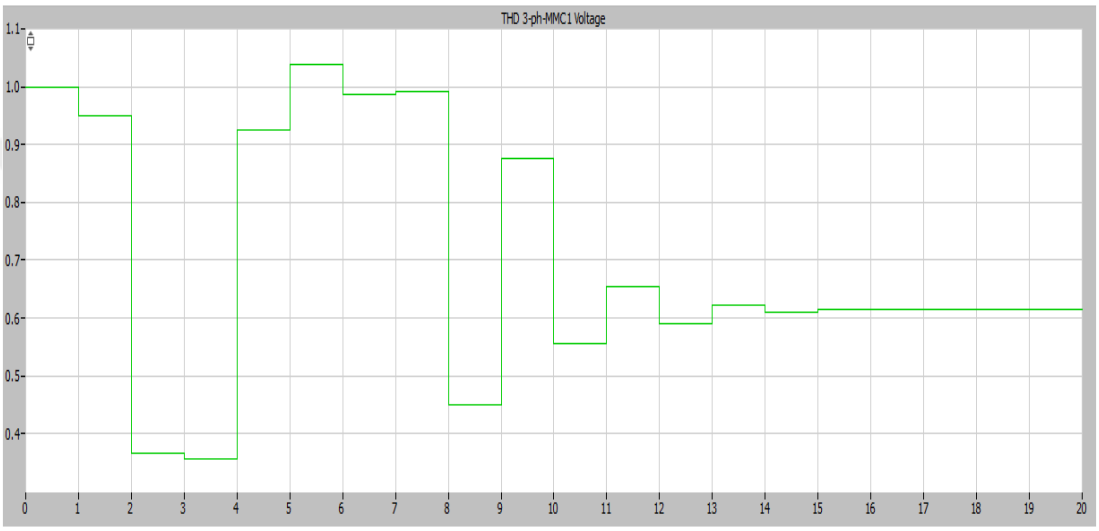
(b)

Figure 5.6: The total harmonic distortion (THD) values for regenerated signal at MMC2 output for (a) AC voltage, (b) current.

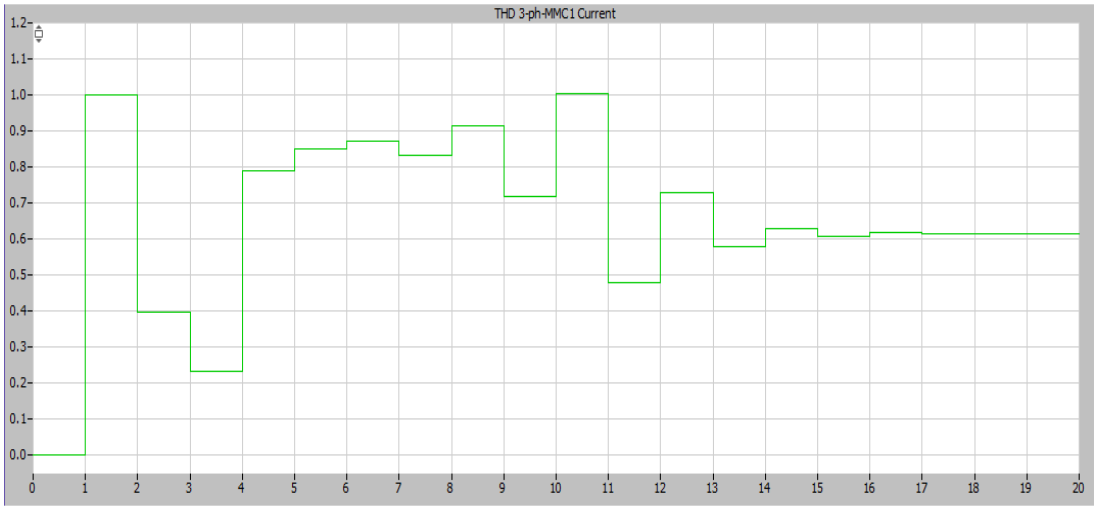
The THD value of the waveform at MMC2 are listed in Table 5.2.

Table 5.2: The total harmonic distortion (THD) values for AC voltage output and AC Grid current in MMC2 output.

Time(**S**)	T1(1s)	T2(6s)	T3(11s)	T4(16s)	T5(20s)
THD (**V**)% (50 Hz)	0.991	0.786	0.621	0.556	0.566
THD (**I**) % (50 Hz)	1	0.61	0.419	0.608	0.608



(a)



(b)

Figure 5.7: The total harmonic distortion (THD) values for regenerated signal at MMC1 output for (a) AC voltage, (b) current.

The THD value of the waveform at MMC1 are listed in Table 5.3.

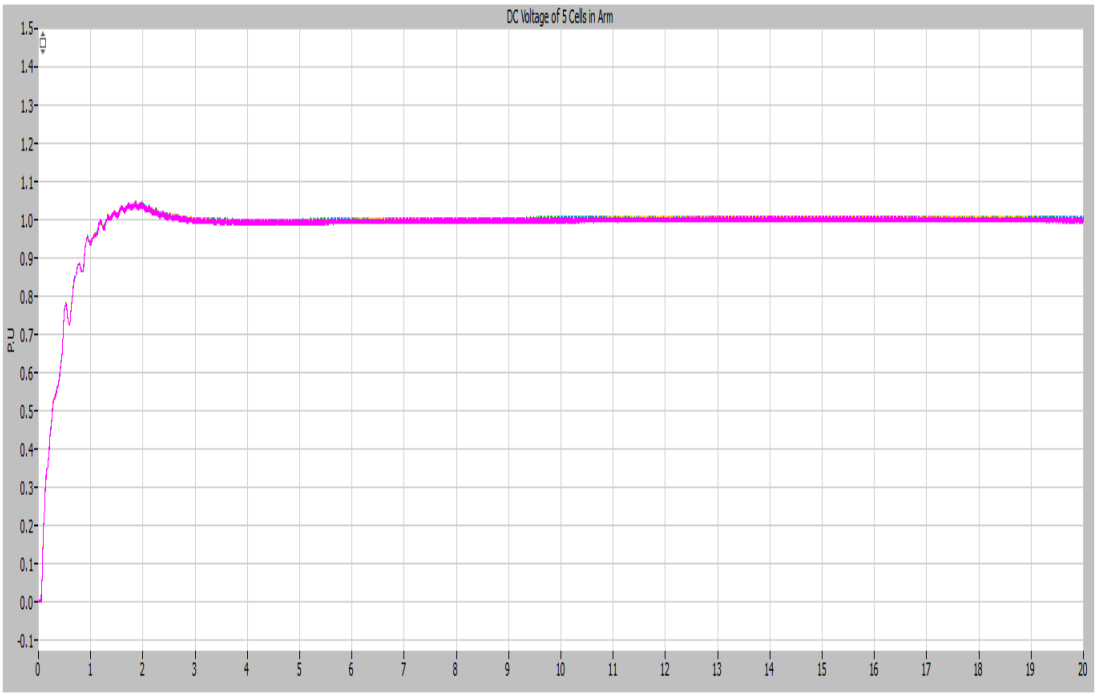
Table 5.3: The total harmonic distortion (THD) values for AC voltage output and AC Grid current in MMC1 output

Time(**S**)	T1(1s)	T2(6s)	T3(11s)	T4(16s)	T5(20s)
THD (**V**)% (50 Hz)	1	0.985	0.55	0.613	0.613
THD (**I**) % (50 Hz)	1	0.85	0.48	0.608	0.6614

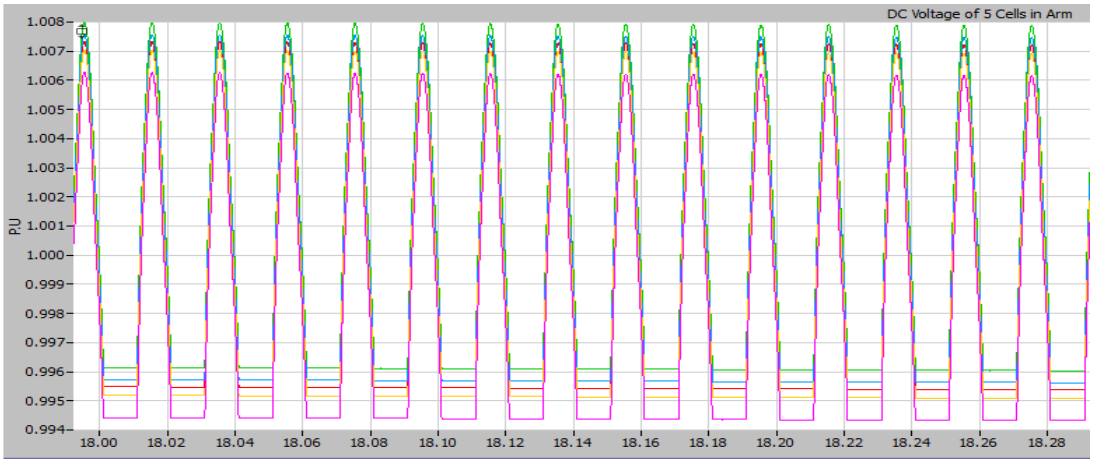
As shown from results of Table 5.2 and Table 5.3 for system 1 and system 2, respectively, it is apparent that the values are below the limits of the IEEE 519 standards.

5.3.2. Simulation Results of Cell Arm Voltages

The capacitor voltages of the 5 cells in one arm are shown in Figure 5.8.



(a)



(b)

Figure 5.8: DC voltage of five SM in the arm (a) through 20 second total simulation time (b) sub section of (0.30) second.

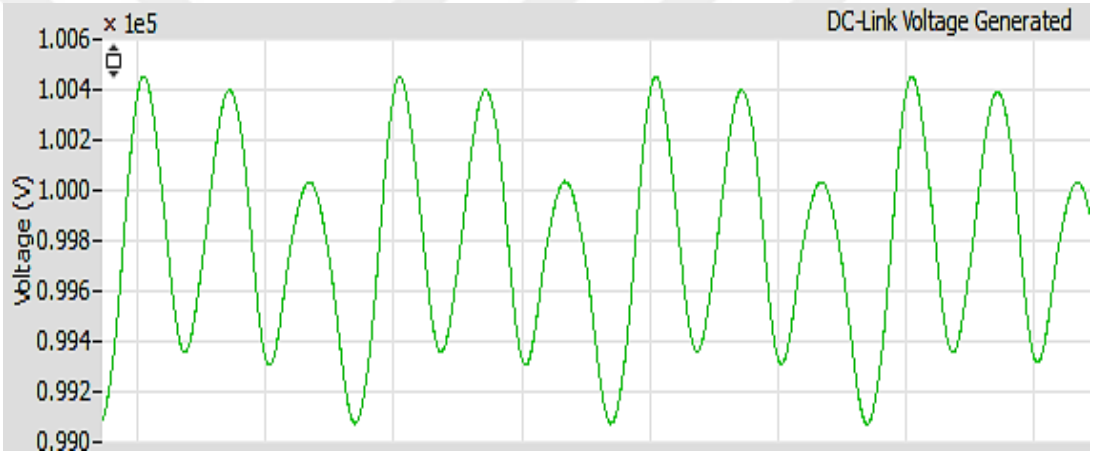
From Figure 5.8 (a), DC voltage of SM reaches to the steady-state in about 3 seconds. It is evident that each voltage of SM is very close to each other with a relatively uniform waveform shape. The ripples vary from around 19.9 kV to 20.5 kV.

These results shows that the switching strategy and the Vc balance algorithm gives the desired maximum peak to peak voltage deviation. In addition to this, uniform and low ripples in the cell waveforms in MMC are obtained. These results also confirm that there is a good choice of selecting the capacitor size of the cell. It is chosen as 7.2mF. The accurate PD PWM controller strategy for ON/OFF switching and charging/discharging is the high accuracy in modulation and maintain the value of each SM capacitor in the specific range and gives alternating ripple about (1.15%) below standard limits.

5.3.3. Simulation Results of DC Link Voltage

The DC link voltage generated in the bidirectional operation, that mean when MMC1 worked as rectification (by convert AC to DC) and transferring the DC voltage through transmission line to MMC2 that worked as inversion by convert the DC to AC again. When MMC2 worked as rectification (by convert AC to DC) and transferring the DC voltage through transmission line to MMC1 that worked as inversion by convert the DC to AC again shown in Figure 5.9.

(a)



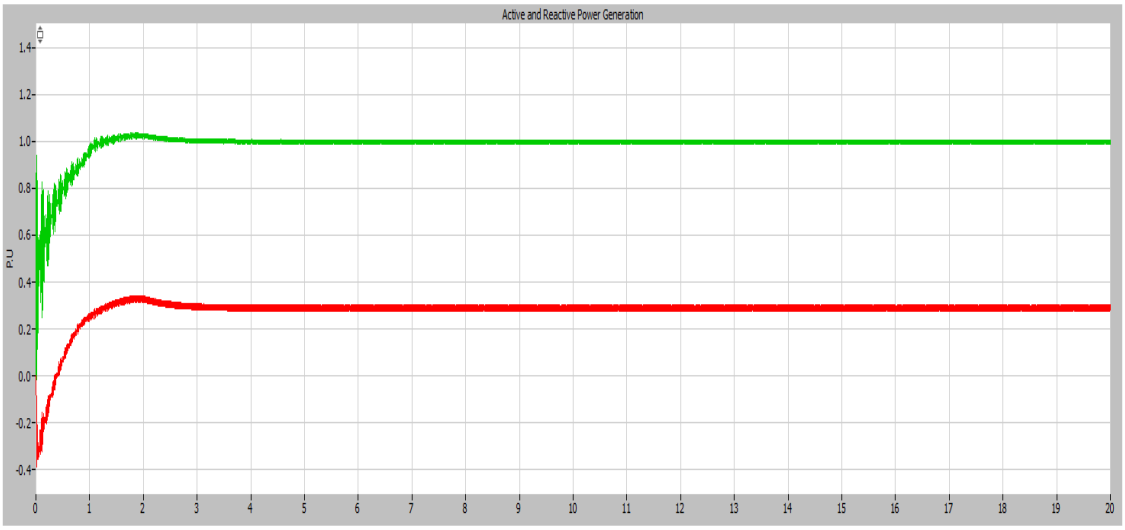
(b)

Figure 5.9: DC link voltage (a) generation through 20 second, (b) sub section of dc link voltage

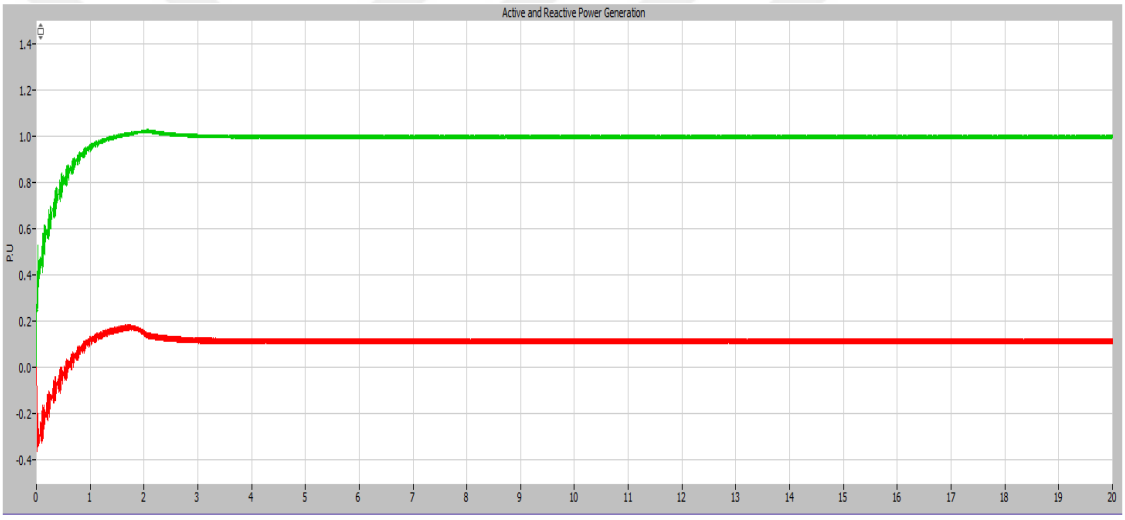
As shown in Figure 5.9 (a), the nominal DC link voltage reaches to its reference value of 100 kV in about 3.5 seconds. The variations of the DC link voltage are also shown in Figure 5.9 (b). The ripples are observed between 99 kV and 100.4 kV. This ripple is due to the charging and discharging of capacitors through power transfer.

5.3.4. Simulation Results of Active and Reactive Power

In this section, the simulation results of active and reactive power are presented for both of the systems. The simulated waveforms are shown in Figure 5.10.



(a)



(b)

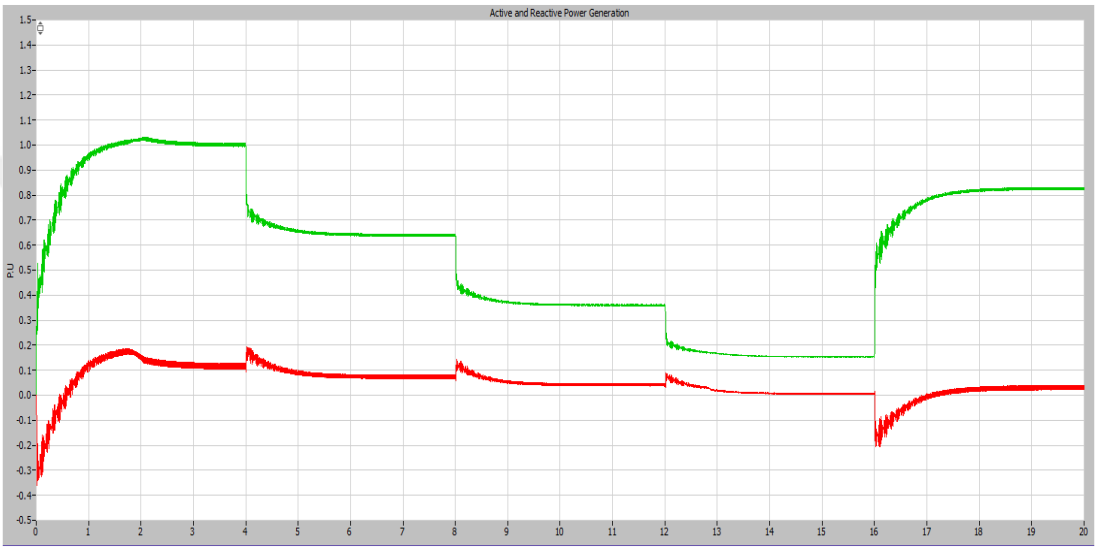
Figure 5.10: System powers: Active power (green) and reactive power (red) for system 1 (a), system 2 (b).

The oscillations observed both in active and reactive power have decreased with time and reach to steady state in about 3.5 seconds. The results show that the oscillations in power after system reach stability has a low value, where the oscillations in active power are in the range between 328.7 MW and 334.2 MW. The oscillations are between 94.4 MW and 102.8 MW in case of reactive power.

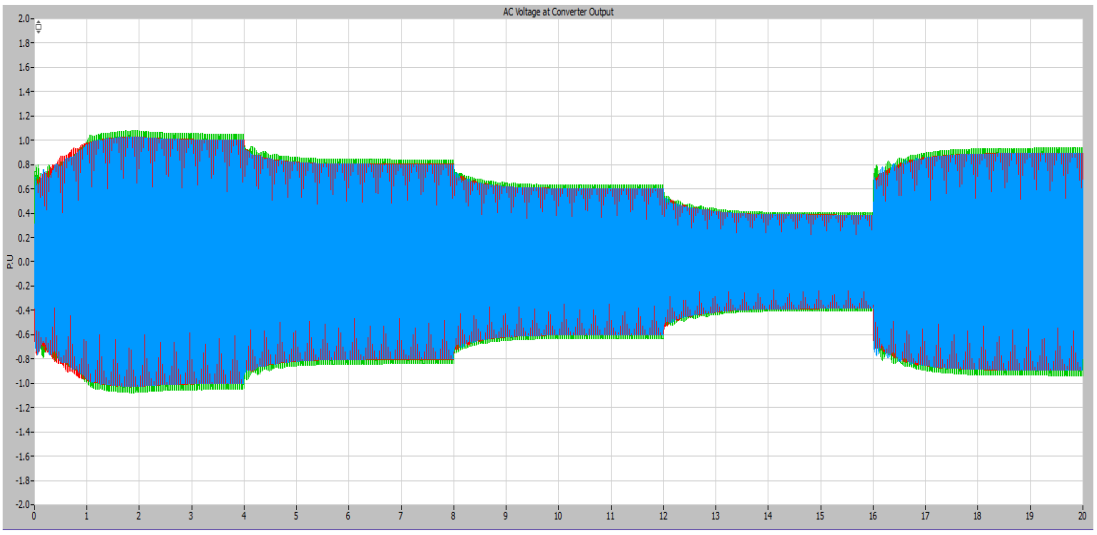
5.3.5. Controlling DC Link and Power Generation Test

In this case study, the ability of the system to work under reference value of power and DC link voltage has been tested.

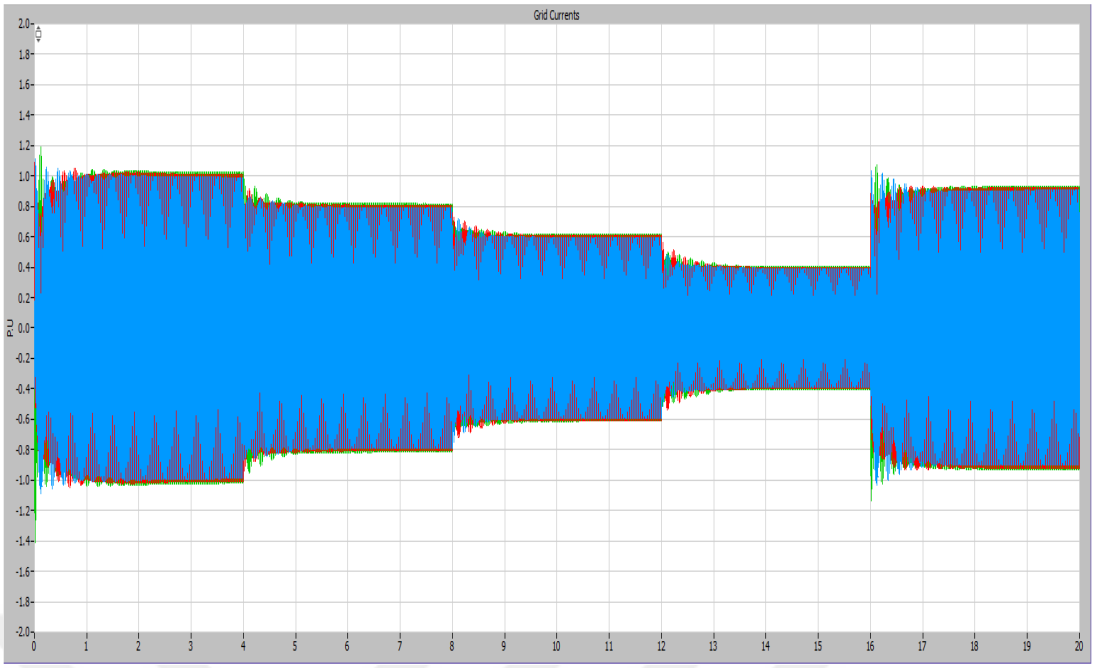
For testing the response of system for dynamic change, we have been test the response of the system to changing in power reference. For that we have been changed power reference in second (4, 8 ,12 and 16) and investigated the changed in power reading, as shown in figure 5.11.



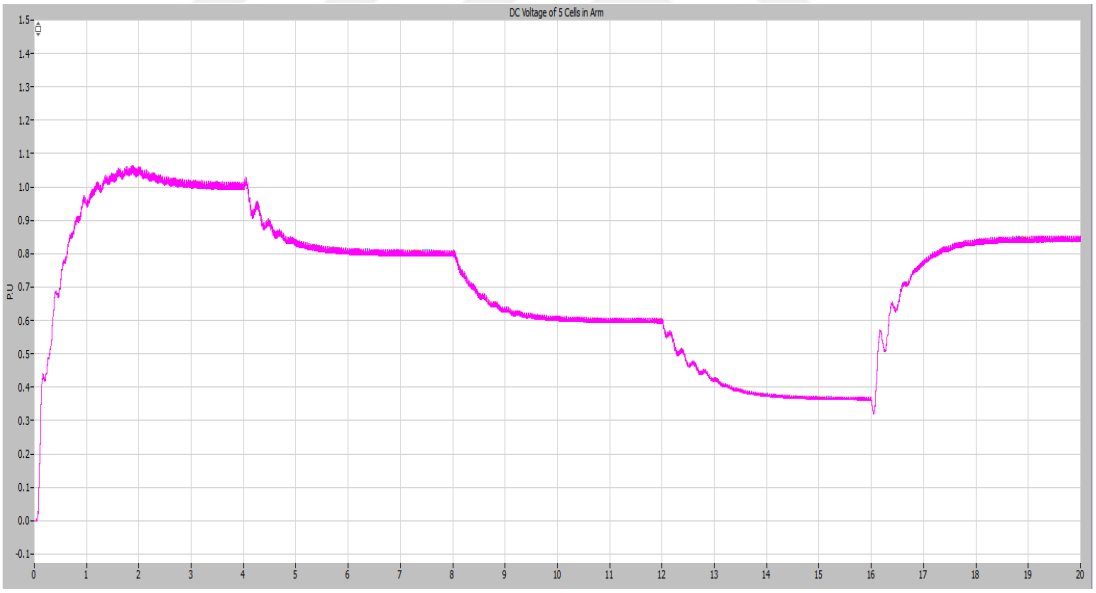
(a)



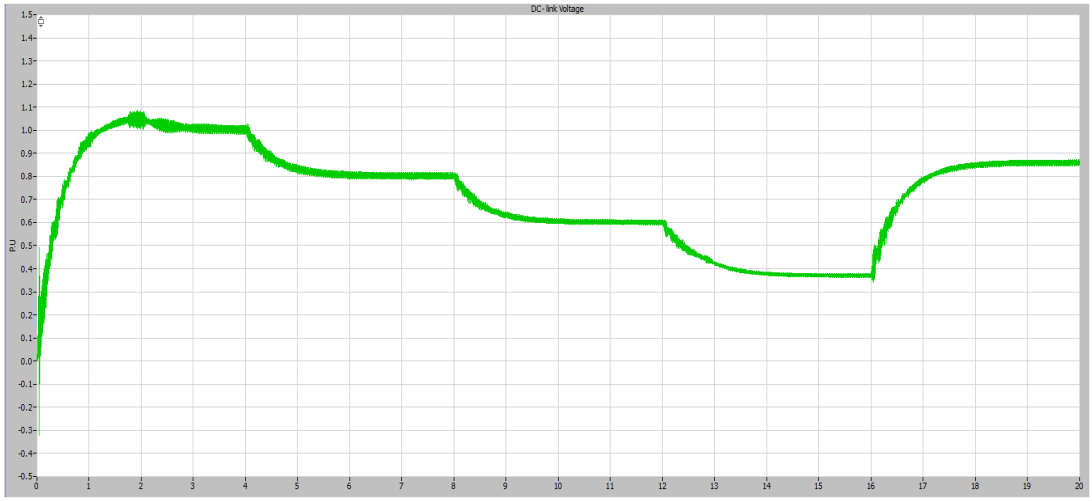
(b)



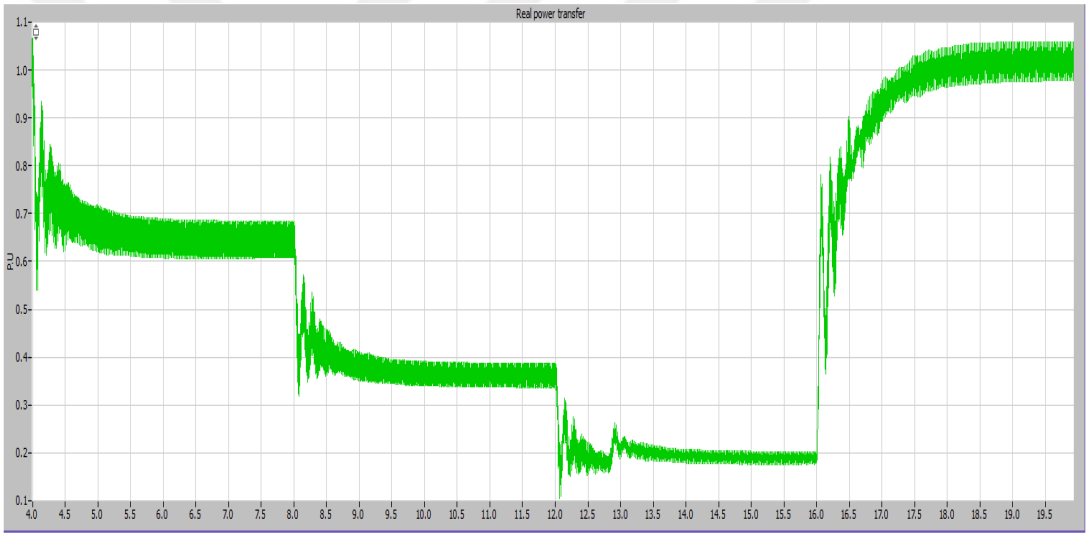
(c)



(d)



(e)



(f)

Figure 5.11: Overall HVDC control system response against changing the power reference: (a) power reference changed with time, active power (green), reactive power (red), (b) AC output voltage, (c) grid current, (d) cell voltage, (e) DC link voltage, (f) real power transfer in transmission line.

Pu is assumed value we described that each 1PU equal the maximum designed value of each measurement unit. x axis represent time while y axis represents the: power, AC output voltage, grid current, cell voltage, DC link voltage and real power in transmission line, respectively.

As shown in Figure 5.11 (a), initially AC stations have zero active and reactive power which is the starting point of system generation. The system works in normal mode (no reference power or dc voltage) and power is increased. At first, at time t = 2 seconds, power reference is set as 1 pu (or 100%) and the power drops to reach the reference value in about 0.2 seconds. At time t = 4 seconds, the reference value of the power is changed to be 0.65 pu and the system reaches to the steady-state in about 2 seconds. At time t = 8 seconds, the power reference is changed as 0.45 pu and the system reach to the steady-state in about 1.7 seconds. At time t = 12 seconds, the power reference is changed to 0.25 pu and the power drops to reach the reference value in about 1.7 seconds. Finally, the power reference is increased to 0.8 pu at time t=16 seconds and the power increases to reach the reference value in about 2 seconds.

Also, as shown from the results presented in Figures 5.11 (b), (c), (d), (e), (f), the system controllers work smoothly and efficiently with low ripple in process. It takes relatively low time to reach steady state after changing power to the desired value, which takes about 2 seconds to change from 1 PU to 0.65 PU and 1.8 seconds to change from 0.65 pu to 0.45 PU.

5.3.6. Full Active Power Reverse Test

In this test, the ability of the MMC-based HVDC transmission system on reversing active power transfer is tested and verified. The simulation results are shown in Figure 5.12.

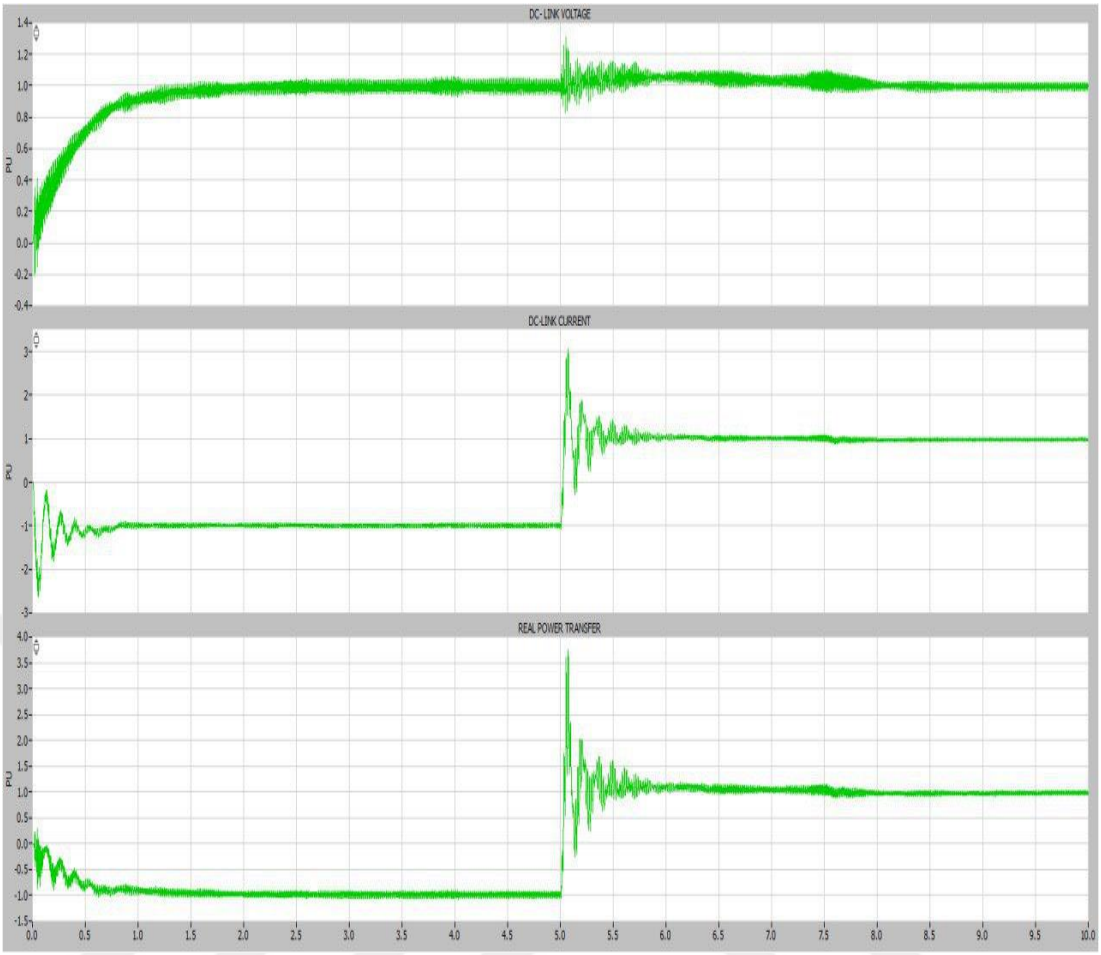


Figure 5.12: HVDC system power reverse. Upper, DC Link voltage, middle, Dc link current and the Lower, is the real power transfer in Dc link.

Pu is assumed value that describe the maximum or designed value of the parameters. x axis represent time while y axis represents the: power, AC output voltage, grid current, cell voltage, DC link voltage and real power in transmission line, respectively.

Initially system 1 is operating in inverter mode which controls the DC-link voltage, while system 2 operates in rectifier mode. It takes about 2 seconds to reach to the steady-state and the active power transfer reaches at -1.0 pu. At time t=5s, the full active power reversal is activated. Then the power changes from -1 pu to 1 pu. Now system 1 is operating in rectifier mode which controls the DC-link voltage, while system 2 operates in inverter mode. It takes about 1 seconds to reduce ripple and 2

seconds to reach to steady-state. During the whole simulation time, the DC-link voltage at both terminals closely follows the reference.

CHAPTER 6

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

6.1. Conclusions

MMC has got a big attention due to its modular structure that gives advantages as a multilevel converter. Recently, MMC technology was already used in large HVDC transmissions, which was appropriate for high voltage structures.

In this work, the simulation study of a MMC based HVDC transmission system positioned between two separate large power generation centers is performed.

MMC has five half-bridges (SM) at each arm and each half-bridges has a two bidirectional (IGBT) with antiparallel diodes, and a DC capacitor. In addition, each single phase arm has one inductor and one resistor for filtering. Thus, each MMC in total has a 6 resistors, 6 inductors, 30 half bride, 30 DC-link capacitor and (60) IGBT switches.

This MMC based HVDC transmission system can provide real power flow control and reactive power/voltage control at AC terminals of both converters independently. Moreover, real power transfer can be reversed. From the simulation studies, the following conclusions can be pointed out:

1. PD-PWM offers a good harmonic performance for regenerated wave form. This accurate controller strategy for ON/OFF switching and charging/discharging lead to high accuracy in modulation and guiding switching operation.

2. The influence of the cell capacitance on its voltage ripple has been tested. The results show that each SM voltage of is very close to each other with a relatively uniform waveform shape. These results shows that the switching strategy gives

the desired maximum peak to peak voltage deviation. In addition to this, uniform and low ripples in the cell waveforms in MMC are obtained. These results also confirm that there is a good choice of selecting the capacitor size of the cell. It is chosen as 7.2mF.

3. The AC waveforms generated by each MMC is nearly sinusoidal having low THD values which are suitable according to the IEEE 519 standards.

4. The power generation of the system can be fully controlled to make it works in desired limitation of both power and dc link limits. This give a benefit when need to operate system not in maximum load (such as let it working in 60% of its maximum power), also when the DC link transmission line are limited to work in less than the maximum dc link voltage generation so it can be controlling the value to reference to not let it exceed the dc link maximum operation voltage limits. The results show that the system controllers work smoothly and efficiently in guiding power generating with low ripple in process and relatively low time to reach steady state after changing power to the desired value.

5. The system worked in bidirectional way that can reversing active power transfer in two directions (from MMC1 to MMC 2 or vise various).

6.2. Suggestions for Future Work

MMC based HVDC is a promising technology and it is at the heart of research and development studies in power electronic area. The areas of improvement of these type of systems are available and varied.

The improvement can be achieved by Developing dynamic controls that are able to provide a broad variety of voltage conversion ratios. Experimentally verifying the developed dynamic controls and analytical models. Steady the case of using full bridge with this controller and comparing it with this controller.

REFERENCES

[1]Rudervall, R., Charpentier, J.P., Sharma, R. (2000). High Voltage Direct Current (HVDC)Transmission Systems Technology Review Paper, *Energy Week* 2000, Washington, D.C, USA.

[2]Ambrosio, R., Clay, K., DeMartini ,P., James, R., Lauby, M., Mohta, V., Moura, J., Sauer, P., Slakey, F., Lieberman, J., Tai, H. (2010). Integrating Renewable Electricity on the Grid , Report by the APS Panel on Public Affairs, *American Physical Society*.

[3]Marquardt, R., Wang, Y. (2014). Modular Multilevel Converter Fundamentals and Applications, Institute for Power Electronics and Control (IPEC), University of Bundeswehr Munich, Germany.

[4]Akhmatov, V., Callavik, M., Franck, C.M., Rye, S.E., Ahndorf, T., Bucher, M.K., Muller, H., Schettler, F., Wiget, R. (2014). Technical Guidelines and Prestandardization Work for First HVDC Grids, Power Delivery, *IEEE Transactions*, **29**,1, pp.327-335.

[5]Guan, M., Xu, Z. (2012). Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions, *IEEE Transactions*, Power Electronics, **27**(12), 4858-4867.

[6]Sharifabadi, K., Harnefors, L., Nee, H.P., Norrga, S., Teodorescu, R. (2016). Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems, Book, 1st edition, Wiley-*IEEE Press*, ISBN: 978-1118851562.

[7]Tiku, D. (2014). DC Power Transmission Mercury-Arc to Thyristor HVdc Valves, *IEEE Power & Energy Society*, Institute of Electrical and Electronics Engineers, Inc.

[8]Abu-Rub, H., Malinowski, M., Al-Haddad, K. (2014). Power Electronics For Renewable Energy Systems, Transportation And Industrial Applications, Book, *IEEE* Press, John Wiley, Sons Ltd, ISBN: 9781118634035.

[9]Vobecky, J. (2015). The current status of power semiconductors, Facta Universitatis, Series: Electronics and Energetics, **28**(2), 193-203.

[10] Nicholls, J. C. (2009). Soft-switching performance analysis of the clustered insulated gate bipolar transistor (CIGBT), PHD thesis, Emerging Technologies Research Centre, De Montfort University.

[11] Hagiwara, M., Akagi, H., (2009). Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters, Power Electronics, *IEEE Transactions* , **24**, 7, pp.1737-1746.

[12] Antonopoulos, A., Angquist, L., Nee, H. P. (2009, September). On dynamics and voltage control of the modular multilevel converter. In Power Electronics and Applications, 2009. EPE'09. 13th European Conference ,pp. **1**-10. *IEEE*.

[13] Ängquist, L., Antonopoulos, A., Siemaszko, D., Ilves, K., Vasiladiotis, M., Nee, H. P. (2010, June). Inner control of modular multilevel converters-an approach using open-loop estimation of stored energy. In Power Electronics Conference (IPEC), 2010 International (pp. 1579-1585). *IEEE*.

[14] Guan, M., Zheng, X., Huijie, L. (2010). Analysis of DC voltage ripples in modular multilevel converters, Power System Technology (POWERCON), International Conference on, October 2010.

[15] Rohner, S., Bernet, S., Hiller, M., Sommer, R. (2010). Modulation, Losses and Semiconductor Requirements of Modular Multilevel Converters, *IEEE Transactions,* Industrial Electronics, **57**, 8.

[16] Mahendran, S. (2013). IOSR Journal of Electrical and Electronics Engineering *(IOSR-JEEE)* ,**7**, 6, PP 40-51.

[17] Çiftçi, B. (2014). Selection Of Suitable Pwm Switching And Control Methods For Modular Multilevel Converter Drives, M.sc. Thesis, The Graduate School Of Natural And Applied Sciences, Middle East Technical University.

[18] Gayithri, C., Geetha, R. S. (2014). Active Power And Current Control For A Modular Multilevel Converter (MMC) Based System, *International Journal of Research in Engineering and Technology (IJRET)*, **03** Issue 06, eISSN: 2319-1163.

[19] Çiftçi, B., Hava, A.M. (2015). Performance Evaluation and Selection of PWM Switching and Control Methods for Grid Connected Modular Multilevel Converters, *IEEE Energy Conversion Congress and Exposition*, At Montreal, Canada, DOI: **10**.1109/ECCE.2015.7310172.

[20] Haddioui, M. R. (2015). Control and Modulation Strategies for MMC - Based HVDC, Master's Thesis, Aalborg University.

[21] Saeedifard, M., Iravani, R. (2010). Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System, Power Delivery, *IEEE Transactions*, **25**, 4, pp.2903-2912.

[22] Allebrod, S., Hamerski, R., Marquardt, R. (2008, June). New transformerless, scalable Modular Multilevel Converters for HVDC-transmission, Power Electronics Specialists Conference, 2008. PESC 2008 . *IEEE* , pp.174-179, 15-19.

[23] Serbia, N. (2014, Feb). Modular multilevel converters for HVDC power stations, Ph.D. Thesis, Institut National Polytechnique de Toulouse, INPT, HAL Id: tel-00945375.

[24] Davies, M., Dommaschk, M., Dorn, J., Lang, J., Retzmann, D., Soerangr, D. (2008) HVDC Plus, Basics and Principle of Operation, Siemens Energy Sector, E T PS SL/DSoe/Re, HVDC PLUS V3, Aug.

[25] Mitsubishi. (1998, Aug). Feature And Application Of Gate Turn-Offthyristors, Mitsubishi High Power Semiconductors.

[26] Bansal, R. (2017). Handbook of Distributed Generation, Electric Power Technologies, Economics and Environmental Impacts, Book, Springer, ISBN: 9783319513430.

[27] Pan. J., Nuqui, R., Srivastava, K., Jonsson, T., Holmberg, P., Hafner, Y.J. (2008, November). AC Grid with Embedded VSC-HVDC for Secure and Efficient Power Delivery, *IEEE Energy 2030*, Atlanta, USA.

[28] Meier, S. (2009). System Aspects and Modulation Strategies of an HVDC-based Converter System for Wind Farms, Phd. Thesis, Royal Institute of Technology, School of Electrical Engineering, Stephan Meier, Sweden, ISSN: 1653–5146.

[29] Andersen, B. R., Xu, L., Horton, P. J., Cartwright, P. (2002, June). Topologies for VSC transmission, Special Feature: AC/DC power transmission, Power Engineering Journal.

[30] Baek, J. W., Yoo, D.W., Kim,H. G. (2001, November-December). High-Voltage Switch Using Series-Connected IGBTs With Simple Auxiliary Circuit, *IEEE Transactions,* Industry Applications, **37**, 6.

[31] Feng Y. Review of published work and establishment of representative model and scenarios for DC fault studies, First Year Annual Report for Phd., The University of Nottingham United Kingdom-China-Malaysia.

[32] Asplund, G., Eriksson, K., Jiang, H., Lindberg, J., Pålsson, R., Svensson, K., Dc Transmission Based on Voltage Source Converters, ABB Power Systems AB, Sweden.

[33] Bonilla, C. C., Tigga, S. M. (2011). Design and performance comparison of Two-level and Multilevel Converters for HVDC Applications", Master's Thesis in Electric Power Engineering, Department of Energy and Environment, Division of Electric Power Engineering, Chalmers University of Technology, Sweden.

[34] ABB, The Eagle Pass 36 MW back-to-back HVDC Light installation is a voltage source converter (VSC) supported tie interconnecting transmission grids in Texas and Mexico, ABB Company, link: http://new.abb.com/systems/hvdc/references/eagle-pass.

[35] Iversen, T. M., Gjerde, S. S., Undeland, T. (2013, September). Multilevel converters for a 10 MW, 100 kV transformer-less offshore wind generator system. In Power Electronics and Applications (EPE), 2013 15th European Conference on (pp. **1**-10). *IEEE*.

[36] ABB, (2015). ABB Commissions Norway-Denmark HVDC Transmission Link, offshorewind, link: http://www.offshorewind.biz/2015/01/12/abb-commissions-norway-denmark-hvdc-transmission-link/.

[37] Trans Bay Cable Technology , Trans Bay Cable LLC, link: http://www.transbaycable.com/about-the-cable/.

[38] Timofejevs, A., Gamboa, D. (2013). Control of MMC in HVDC Applications, Master's Thesis, Department of Energy Technology, Aalborg University, Denmark.

[39] Shukla, A., Nami, A. (2015). Multilevel Converter Topologiesfor STATCOMs, Springer Science + Business Media Singapore, DOI **10**.1007/ 978-981-287-281-4_2.

[40] Hu1, J., Yu, L., Zhang, Z., Jin, L. (2016). Reserch On The DC Faults In Multi-Terminal DC Transmission System Based on MMC, *International Journal of Advanced Research in Electrical*, Electronics and Instrumentation Engineering, ISSN ONLINE(2278-8875) PRINT (2320-3765), **5**, 12.

[41] Casadei, G. (2012). Modular Multi-Level Converter: Modeling, Simulation and Control in Steady State and Dynamic Conditions, Msc. Thesis, Department of Energy Technology, Aalborg University, 2012.

[42] Sandu, C., Carnu N., Costea, V. C. (2008). Medium Voltage Modular Multi-Level Inverter, Master's Thesis, Institute of Energy Technology, Aalborg University, Aalborg, Denmark.

[43] Ilves, K., Taffner, F., Norrga, S., Antonopoulos, A. (2013 September). A Submodule Implementation for Parallel Connection of Capacitors in Modular Multilevel Converters, Conference Paper in *IEEE Transactions on Power Electronics*, DOI: **10**.1109/EPE.2013.6634325.

[44] Georgios, S. K., Mihai, C., Vassilios, G. A. (2011). Analysis of Multi-carrier PWM Methods for Back-to-back HVDC Systems based on Modular Multilevel Converters, *IEEE*,**1**-61284-972-978/11/$26.00.

[45] Abun, A. (2016). Modelling of Modular Multilevel Converter Using Input Admittance Approach, Master's Thesis in Electric Power Engineering, Chalmers University of Technology, Sweden.

[46] Jovcic, D., Ahmed, K. (2015). Voltage Direct Current Transmission: Converters, Systems and DC Grids, Book, 1st edition, Wiley, ISBN: 978-1118846667.

[47] Holmes, D., Lipo, T. A. (2003). Pulse Width Modulation for Power Converters, Principles and Practice, Wiley.

[48] Bouhali, O., Berkouk, M., Francois, B., Saudemont, C., Labiod, S., (2005). Solving Harmonics Elimination Problem in Three-Phase Voltagecontrolled Inverter using Artificial Neural Networks, *J. Electrical Systems* **1**,1, pp.39-51.

[49] Du, Z., Tolbert, L. M., Chiasson, J. N., Ozpineci, B. (2008, Apr). Reduced Switching Frequency Active Harmonic Elimination for Multilevel Converters, *IEEE Transactions on Industrial Electronics*, **55**, 4.

[50] Deng, Y., Teo, K. H., Duan, C. T., Habetler, G., Harley, G. R. (2013). A Fast and Generalized Space Vector, Modulation Scheme for Multilevel Inverters, *IEEE Transactions on Power Electronics*.

[51] Gamboa, D., (2013). Control of MMC in HVDC Applications, Msc. Thesis, Department of Energy Technology, Aalborg University, Denmark.

[52] IEEE, (1993). IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, *IEEE* SM 519-1992, Institute of Electrical and Electronics Engineers, Inc, New York, USA, ISBN:**1**, 55937-239-7.

[53] Malek, B., Andov, K., Gutman, R., Mehraban, B. (2015). Harmonic Issues of AEP Welsh HVDC System, CIGRE US National Committee, Grid of the Future Symposium.

[54] Microsemi, (2015). Basic Total Harmonic Distortion (THD) Measurement, Microsemi Corporation, Application Note 30 (AN30).

[55] PLECS demo model, HVDC Transmission System with MMCs, Model Link: https://www.plexim.com/support/application-examples/ 938.

[56] Jacobson, B., Karlsson, P., Asplund, G., Harnefors, L., Jonsson, T. (2010) VSC-HVDC Transmission with Cascaded Two-Level Converters, CIGRE.