INVESTIGATION OF THE EFFECTS OF THICKNESS ON THE METAL-INSULATOR TRANSITION IN VANADIUM DIOXIDE NANOCRYSTALS, AND DEVELOPMENT OF A NOVEL VANADIUM DIOXIDE MOTT FIELD-EFFECT TRANSISTOR

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Mustafa Mohieldin Fadlelmula Fadlelseed

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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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Vanadium dioxide (VO_2) is a material that has attracted a lot of attention for its prospective potential to be utilized in the field of electrical and ultrafast optical switching in one hand, and for the fundamental physics that can be revealed through studying this strongly correlated material on the other hand. One of the most attractive qualities of VO_2 is the metal-insulator transition (MIT) which takes place slightly above room temperature in this material. Controlling such phase transition through external stimuli would open unprecedented avenues of electrical and optical applications. However, thin VO_2 nanocrystal are required to overcome the limitation imposed thought the Thomas-Fermi screening length which limits the changes and the control that external electrical stimuli would have on any crystal that exceeds this length. The screening length in VO_2 is known to be no more than 6 nm. Here, we avoided the use of epitaxial and sputtered films for the complications in such materials that arise from the stress due to lattice mismatch and the interdiffusion with substrates in epitaxial films, and the polycrystalline nature of sputtered films. In this work, vapor-phase grown VO_2 nanocrystals are used instead. One reason behind this is that unlike epitaxial films vapor-phase grown VO_2 nanocrystals can be released out of the growth substrate and transferred in order to eliminate the stress induced on the crystals due to adhesion to the substrate. The main shortcoming of this type of crystals, which is addressed thoroughly in this study, is that vapor-phase grown VO_2 nanocrystals are produced with dimensions no less than 30 nm due to the lack of thickness control in physical vapor deposition technique.

Mainly in this study, a systematic method to mill down vapor-phase grown VO_2 nanocrystals to sub-5 nm thicknesses is developed. Ar-ion milling is utilized to achieve this goal. Photoresist protection and shadowing methods are introduced and used to reveal the etch rate of VO_2 nanocrystals which is found to be equal to 3.3 $\pm$0.3 nm/min using ion-gun energy of 1 KeV with medium monatomic flux. Our results show some surface damage caused by the Ar-ions bombardment that is limited maximum to the top 5.6 nm of the surface of the etched crystals. This damage and related changes in the electrical properties in the milled crystals are completely eliminated by short duration treatment in a 37% hydrochloric acid ($HCl_{(aq)}$) solution of these crystals. The results presented here in this regards show complete recovery of the relative order of changing in resistance that accompanies the MIT of treated etched crystals when compared to their pristine form.

The last part of this study is dedicated to the investigation of implementing mill down vapor-phase grown VO_2 nanocrystals in possible prospective applications. Mainly, the use of these crystals in constructing Mott-Field Effect Transistors (Mott-FETs) is investigated. Further investigation are yet to be done in this regards in order to draw a final conclusion in the possibility of using VO_2 nanocrystals in reliable Mott-FETs. However, the results presented here along with the suggestions related to the fabrication of vapor-phase grown VO_2 nanocrystals based three-terminal devices are of a vital importance in setting directions for future works.

Keywords: Vanadium dioxide, strongly correlated materials, metal-insulator transition, argon-ion beam milling.

ÖZET

VANADYUM DİOKSİT NANOKRİSTALLERİNDE KALINLIĞIN METAL-YALITKAN FAZ GEÇİŞİ ÜZERİNE ETKİSİNİN İNCELENMESİ, VE YENİ BİR TÜR VANADYUM DİOKSİT MOTT ALAN-ETKİSİ TRANSİSTÖRÜNÜN GELİŞTİRİLMESİ

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Vanadyum dioksit (VO_2), gerek elektronik ve ultrahızlı optik geçiş uygulamalarında gösterdiği büyük potansiyel nedeniyle, gerekse güçlü etkileşim gösteren malzemelerin ardında yatan temel bilim sayesinde büyük ilgi gören bir malzeme olmuştur. VO_2'nin en çok dikkat çeken özelliklerinden bir tanesi, oda sıcaklığının hemen üstünde gösterdiği metal-yalıtkan faz geçişidir (MYG). Bu tarz bir faz geçişinin dış uyaranlar aracılığıyla kontrol altına alınmasıyla, daha önce görülmemiş bir şekilde pek çok elektronik ve optik uygulamanın kapısı aralanacaktır. Bununla birlikte, dış uyaranların kristalin üzerindeki etkisini baskılayan Thomas-Fermi perdeleme kalınlığının getirdiği sınırlamar nedeniyle, VO_2 nanokristallerinin ince bir yapıda olmaları gerekmektedir. VO_2 için bahsedilen perdeleme kalınlığının 6 nm'yi geçmediği bilinmektedir. Bu noktada, latis uyuşmazlığından kaynaklanan stres ve alttaşlar arası yaşanan difüzyon sebebiyle epitaksiyel filmlerin kullanılmasından, ayrıca çoklu-kristal yapısı sebebiyle püskürtme filmlerin kullanılmasından kaçınılmıştır. Bunun yerine, buhar-fazı yöntemiyle büyütülen VO_2 nanokristalleri kullanılmıştır. Bu olayın ardında yatan nedenlerden biri, epitaksiyel filmerin aksine buhar-fazlı büyütülen VO_2 nanokristalleri bulunduğu alttaştan kurtulabilmekte ve alttaşın kristaller üzerinde oluşturduğu stresi yok etmek amacıyla transfer edilebilmektedirler. Bu çalışmada detaylıca bahsedildiği gibi bu tür kristallerin ana eksikliği, fiziksel buhar biriktirme yönteminin kristal kalınlığını kontrol etmekteki yetersizliği sebebiyle buhar-fazlı büyütülen VO_2 nanokristallerinin boyutlarının 30 nm'den aşağı inememeleridir. Bu çalışmada, buhar-fazlı büyütülen VO_2 nanokristallerini aşındırarak kalınlıklarını sistematik bir şekilde 5 nm altına indirme yöntemi

geliştirilmiştir. Bu hedefte ar-iyon aşındırması kullanılmıştır. Fotorezist koruması ve gölgeleme efekti metodlarının devreye girmesiyle, orta seviyede monatomik akı ve 1 keV'luk enerjiye sahip iyon tabancasıyla aşındırılan VO_2 nanokristallerinin aşınma hızı 3.30.3 nm/dk olarak bulunmuştur. Bulunan sonuçlar göstermektedir ki aşındırılan kristaller üzerinde 5.6 nm'yi geçmeyecek şekilde ar-iyon bombardımanından kaynaklanan bir yüzey hasarı oluşmaktadır. Hasara uğrayan kristallerin %37'lik hidroklorik asit çözeltisi (HCL(aq)) içerisinde kısa süre bekletilmesiyle, yüzeyde oluşan hasar ve getirdiği elektriksel özelliklerdeki değişimler tamamen yok edilebilmektedir. Bu çalışmada sunulan sonuçlar aşındırılan kristallerin evvelki halleriyle karşılaştırıldığında, MYG esnasında aynı derecede değişim gösterdiklerini işaret etmektedir. Burada sunulan çalışmanın son kısmı ise, buhar-fazlı büyütülen VO_2 nanokristallerini aşındırma yöntemlerini inceleyerek ulaşılabilecek yeni uygulamalara adanmıştır. Temel olarak, Mott alan-etkisi transistörünün (Mott AET) üretiminde VO_2 kristallerinin oynayabileceği rol üzerine incelemeler yapılmıştır. Konu hakkında kesin bir yargıya varmak üzere şüphesiz daha fazla araştırma yapılmasına ihtiyaç vardır. Ancak, bu çalışmada sunulan sonuçlar ve bununla birlikte buhar-fazlı büyütülen VO_2 nanokristali kullanılarak üretilebilecek üç terminalli aygıtlar hakkında verilen tavsiyeler, gelecekteki çalışmaları şekillendirmede önemli bir rol oynayacaklardır.

Anahtar sözcükler: Vanadyum dioksit, güçlü etkileşimli malzemeler, metal-yalıtkan faz geçişi, argon iyon demeti aşındırmasıi.

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Chapter 1

Introduction

Since the invention of transistor in the late forties of last century, scaling them down became a major concern in both academia and industry due to the need of compact, high efficiency electrical devices. The miniaturization of electrical circuit components has become of a vital importance after the development of integrated circuits (IC) and the emergence of the first functional semiconductor IC by Fairchild Semiconductor in 1960. This technology is based on silicon based semiconductors known as Complementary Metal Oxide Semiconductor (CMOS) invented by Frank Wanlass of Fairchild Semiconductor in 1963 [1]. The well-known Moores Law named after the co-founder of both Fairchild Semiconductor and Intel predicted in 1975 that the number of transistors in an integrated circuit would double every two years as a revised form of his first prediction in this regards in 1965 [2]. Since then, Moore's law has been in play and had proven reliability. However, as the scaling and manufacturing techniques advance, both the fundamental and technological limits of the silicon technology are around the corner. Being able to circumventing almost all of the limitation encountered so far, either by changing the design of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which is an indispensable component of CMOS, or improving the fabrication processes allowed the realization of up to 14 nm channel length. However, achieving a sub 10 nm channel length is a goal that is surrounded by sets of both fundamental and infeasible to circumvent challenges.

Such critical limitations on the way of further miniaturization of MOSFETs are discussed in this section along with some promising alternative materials. However an overview on transistors in general and MOSFET's in particular is given beforehand in order to facilitate the understanding of these related limitations.

1.1 Overview on Transistors

Transistors in general are serving one of two purposes. Firstly as a signal amplifier in similar manner as the first transistor that emerged from Bell Labs at the end of 1947. The second function of a transistor is as an electrical switch or a signal controller. The amplification process is using Bipolar Junction Transistors (BJT) or Junction Field Effect Transistors (JFET). Where in the modern electronics, MOSFETs are used to execute logical operation. In this suction, brief overview of etch of these transistor types is given, However, in depth elaboration on MOSFETs is provided as the silicon technology scaling problems are of a direct relation with this specific type of transistors.

1.1.1 Bipolar Junction Transistors

As the name of BJT indicates, it is composed of two PN or NP junctions placed back to back with variation in the sizes of the three doped regions. Considering NPN BJT, the P channel is called the base and is used to control the current flow between the other two electrodes. The N region that is connected to the base (Forward biased), so that the depletion layer is minimized to the level that current would pass through the P channel, is called the emitter. The access electrons are allowed through the P channel to the other N region that is called the collector. Thus by passing a small base current I_B, much larger collector current I_C is obtained. The amplification magnitude can be given by the ratio of collector current to base current I_C/I_B and is known to range between 50-300 for most BJTs. The main difference between NPN and PNP BJT is that PNP operates in the reverse bias. Illustration of the above mentioned BJTs are shown

in figure 1.1.

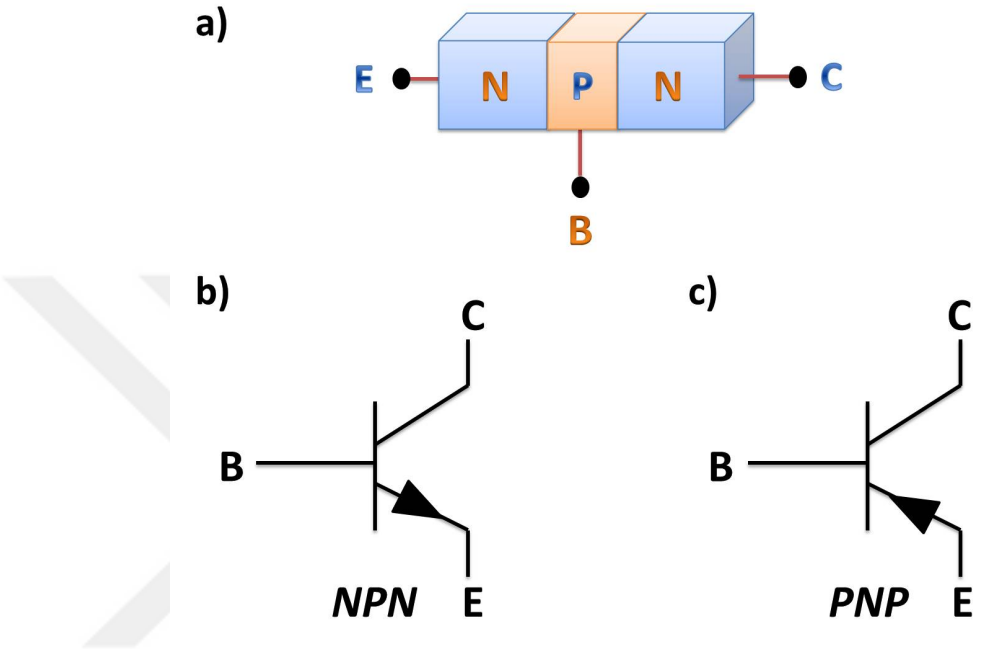


Figure 1.1: *Bipolar junction transistor schematic representation of a) NPN and schematic symbols of b) NPN BJT and c) PNP BJT.*

1.1.2 Junction Field-Effect Transistors

As for a junction field-effect transistor a N-channel JFET as an example is generally composed of a N-doped channel that is sandwiched between two highly doped P regions. The gate electrode is connected to the P regions while the the source and drain are directly connected to the opposite ends of the N channel. The main difference between BJTs and JFETs is that JFETs do not operate under biasing current as BJTs do. Considering the same N-channel JFET, the transistor would be in its fully on state when $V_{GS} = 0$, and that means a uniform channel between source and drain is formed. However, when a reverse bias is applied between gate and source (V_{GS}) the depletion layer on both sides of the channel start to grow toward the N-channel due to the high doping of the P regions, causing uniform narrowing down of the N-channel till it reaches a state where the complete region

between source and drain is blocked. Consequently, the drain source current I_{DS} is equal zero. The Voltage needed to uniformly block the channel is known as pinch-off Voltage (V_P).

Junction field-effect transistor are operating according to the following relation: (V_{GD}) = (V_{GS}) - (V_{DS}), so if a zero (V_{GS}) is considered when, for example, a 2V (V_{DS}) is applied, a -2V bias voltage is resulted in the gate-to-channel at the drain end (V_{GD}). consequently, the depletion region near the drain is wider than that at the source end. A nonuniform channel that is narrower toward the drain end would cause an increase in the electrical resistivity of the channel. Therefore, the magnitude of current passing through the channel I_{DS} is a trade-off between (V_{DS}) and the channel resistivity. Depictions of N-channel JFET under zero gate-to-source voltage are shown at both $V_{DS} = 0$ and $V_{DS} > 0$ in figure 1.2.

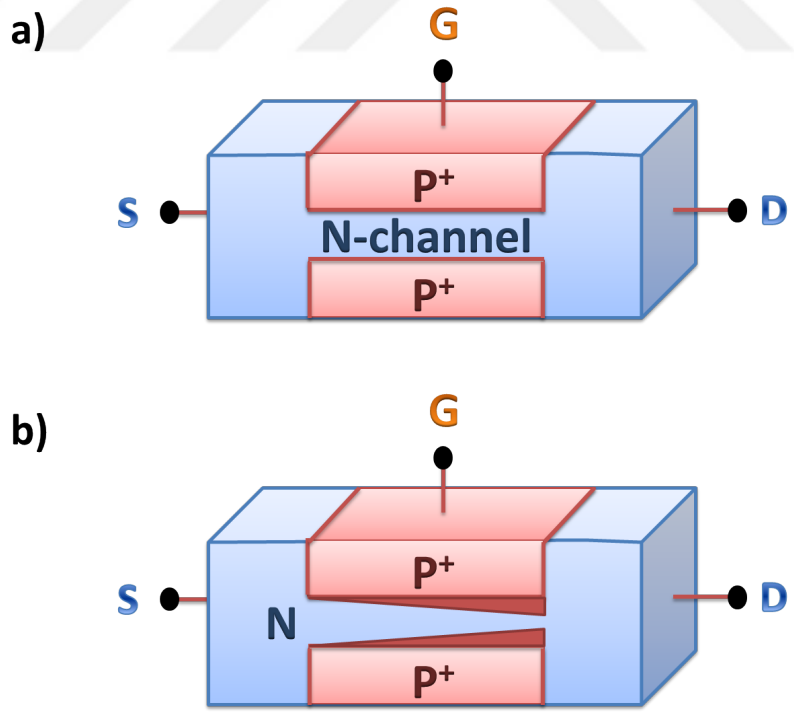


Figure 1.2: *N-channel junction field-effect transistor schematic representation in a gate to source bias (V_{GS}) = 0 when a) drain to source $V_{DS} = 0$ and of b) drain to source $V_{DS} > 0$.*

1.1.3 Metal Oxide Semiconductor Field Effect Transistors

MOSFET is the class of transistors that concerns us the most in this study, as modern transistor technology is mainly based on MOSFETs more than any other classes of transistors. The scaling problems mainly attributed to this class of transistors and they are discussed later in this chapter. Unlike BJTs, no current should pass through the gate in MOSFETs during operation, therefore a Schottky gate-contact is used. Moreover, gate and channel are set in capacitor-like configuration when considering the sandwiched dielectric material. For silicon based MOSFETs, native oxide (SiO_2) has been the best gate dielectric material due to its low trap density interface with Si, uniformity and high breakdown strength [3]. MOSFETs are constructed, taking into consideration n-channel transistor, when a p-doped silicon substrate is doped with a n-type impurities to construct the drain and source regions. These two regions are separated with the p-doped silicon body. The gate is used to inject carriers between source and drain so that a channel between the two terminals is constructed. By changing the channel type, the charge carriers can be changed as well. In a device where both types of transistors are used in a complementary manner, i.e, when one transistor is in ON state, the subsequent transistor will be in OFF state, is called complementary metal Oxide semiconductor (CMOS), and it is considered to be the back-bone of modern integrated circuits. Figure 1.3 gives a clear representation of a n-channel MOSFET.

The length of channel in a MOSFET plays a significant role in its control and operation. Apart from being important for more compacted ICs, the I-V (sourc-drain current I_D vs drain to source voltage V_D) behaviour is also partially dictated by the length of the channel. Also as mentioned above, gate voltage is another critical parameter that govern the electrical response of the whole MOSFET. Turning the attention towards the IV behaviour of such devices at this point is essential as part of scaling limitation mentioned next in this chapter is directly related to the ability of gate control on device's channel when a critical scale is reached. The minimum gate-to-source voltage V_{GS} required to induce a

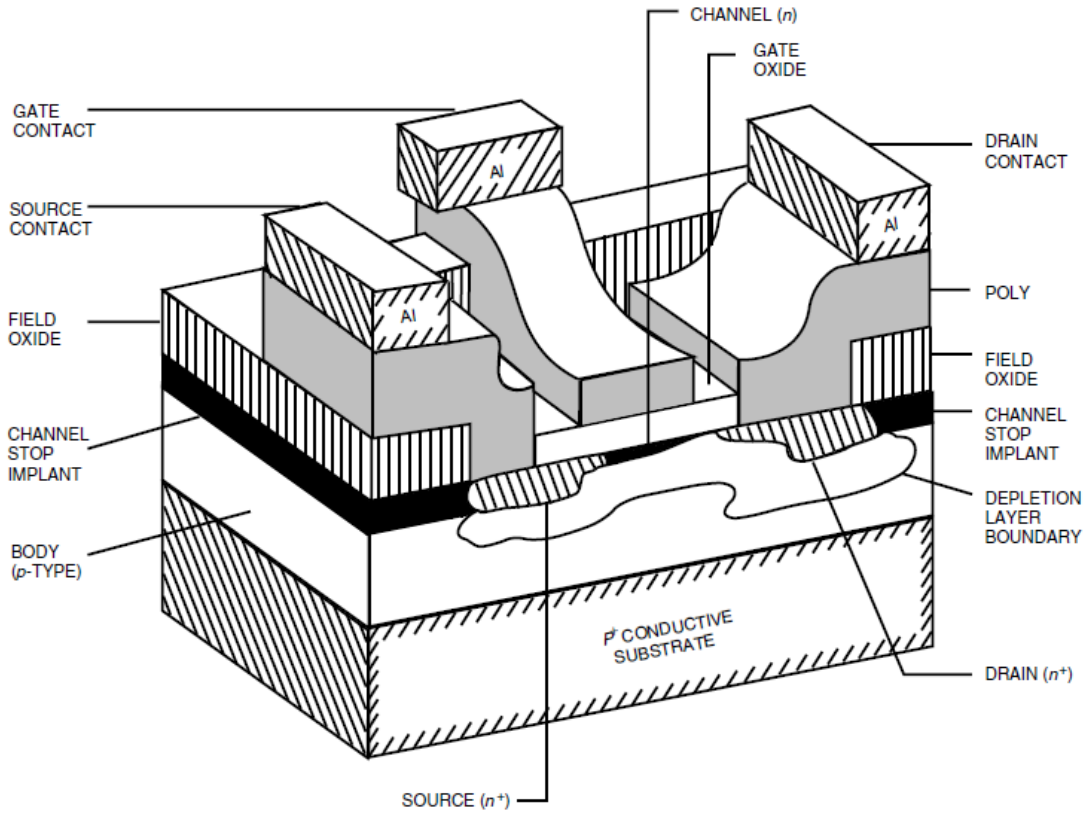


Figure 1.3: *A high performence N-channel MOSFET represented as in an integrated circuit with the field oxide used to isolate the device from other neighbor devices in the same integrated circuit. Reproduced from Ref. [4].*

conductive layer between source and drain is known as threshold voltage (V_T). At different positive V_{GS}, current passing through the n-channel I_{DS} would increase in a more dramatic manner with respect to the applied V_{DS} as higher V_{GS} is applied. However this behavior is limited by the value of voltage at which the dielectric layer starts conducting, known as the breakdown voltage (BV_{DSS}). Where For a given $V_{GS} < BV_{DSS}$, the IV curve flatten out at larger values of V_{DS} and the current flow through the channel is then becomes less responsive to the drain bias. This is know as the state of saturation of the device. As mentioned above, channel length is one reason behind the variation in saturation behaviors, however the detailed explanation of this as well as other reasons behind the saturation behavior in MOSFETs are beyond the scope of this text. Figure 1.4 is a general demonstration of the IV behaviours in MOSTFETs.

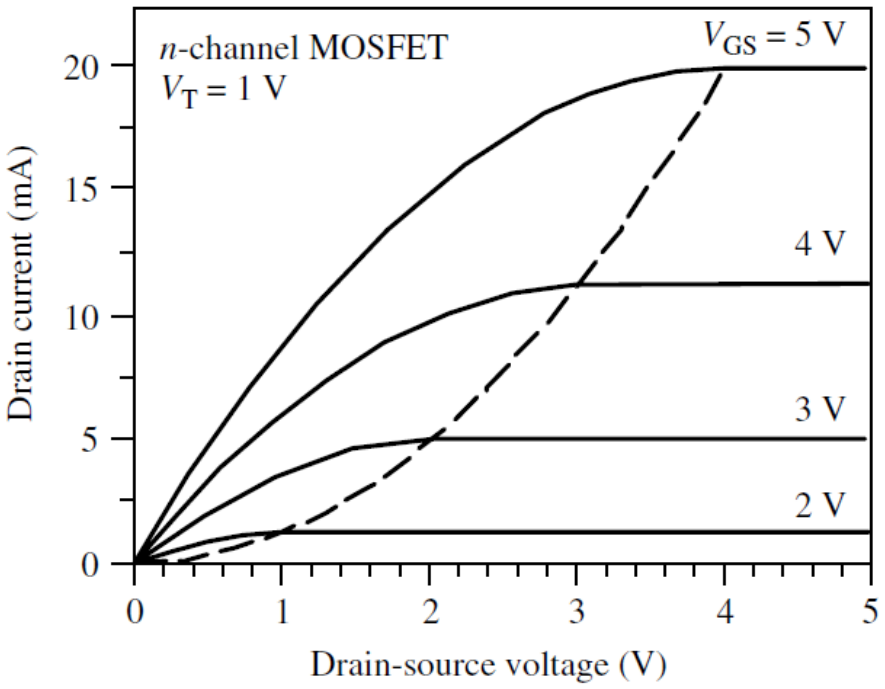


Figure 1.4: *Current vs Voltage (IV) behavior of n-channel MOSFET at various V_{GS} and threshold voltage = 1V. Reproduced from Ref. [5].*

After the general working principles of transistors in general and MOSFETs in particular have been mentioned, the understanding of the limitation hindering the further scaling of CMOS devices would be much easier. Next are discussed the most common limitations in this regard.

1.2 Silicon Technology Scaling Challenges

The types of challenges and limitations encountered due to MOSFETs scaling in CMOS devices are categorized under five main groups as reported by N. Z. Haeron et al. [6], namely physical, material related, power-thermal, technological and processes related and economical challenges. Below is the elaboration on etch of these challenges and limitations.

1.2.1 Physical Limitations

All components of MOSFET are to be scaled down when miniaturization is attempted. The dimensional scaling of some of these components below some critical limits, which we have already reached in today's silicon technology, give rise to many technical problems that reduce the reliability and limit the functionality of the final product. The most critical problem is the short-channel effect. Mainly shorter channels are desired for higher packing density as well as for faster switch and logical operations as less time is required for current to flow through the shorter channels. Nevertheless, the short-channels in devices are accompanied with some detrimental effects. The gate control over the channel behavior tends to decrease dramatically with reducing channel length as a result of the increased charge sharing between source and drain [7]. This charge sharing occurs even when V_{DS} is in its OFF state and current leakage through the channel known as drain off-current would take place [8], which is a consequence of the reduction in threshold voltage associated with drain-induced barrier lowering (DIBL) defined as the decrease in the energy barrier that the majority carriers in the source have to overcome to go through the channel [9] as represented in figure 1.5. Hot-carrier effect at increasing drain voltage is also among the effects caused by short channels.

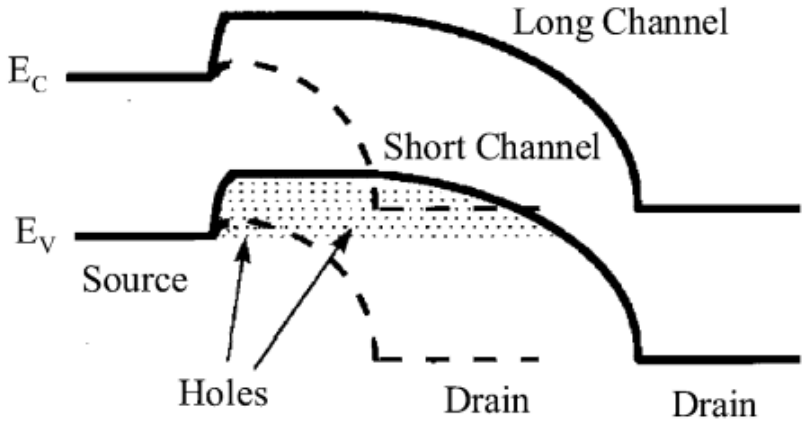


Figure 1.5: *Comparison of schematic energy band diagrams of long and short-channel in n-MOSFETs. Reproduced from Ref. [10].*

One of the most useful ways used to reduce short channel effect (SCE) is using thinner gate dielectric material [7]. It was reported that for transistors with channel length around or below 100 nm, a gate oxide thickness of 3 nm is required to circumvent the SCE [11]. This much thin gate oxide might give rise to gate leakage that would eventually cause a complete failure of the dielectric layer [12]. Moreover, further scaling would require a thinner gate oxide material, which would introduced a more critical problem due to the fact that we are approaching the fundamental limits around 1 to 1.5 nm [13].

1.2.2 Materials Limitations

As mentioned previously in this chapter, the reliability of the common gate dielectric material in MOSFETs (SiO_2) tends to reduce with reducing its thickness to the extent of reaching a breakdown in thinner films [14]. As a solution, high-K materials (relative to SiO_2) were attempted to replace the current SiO_2 gate dielectric in the 45 nm technology as they have the potential to reduce the current leakage problem [12]. However, the instability of such materials at high temperatures combined with the additional manufacturing processes required to be implemented to the current mass production processes are among the main problems that prevent the use of such materials [15]. These types of problems are example of the limitations caused by keeping the main transistor design the same while trying to implement new materials to the existing system.

1.2.3 Power-Thermal and Technological Limitations

According to D. J. Frank [16], the dynamic and static power dissipation are the two types of power dissipation in CMOS circuits. The dynamic power is not of a detrimental nature as is used in logic operations during the switching of the logic states as well as can be controlled through the supply voltage and computation rate. The static power on the other hand, that is taken place as result of leakage mechanisms within the device or circuit reduces the reliability of the whole

processor. These mechanisms by which leakage is taking place are increased in number with scaling. The term power density is used in this regard to indicate the amount of power per unit area. It was reported that for a gate length of 0.9 μm at a junction temperature $T_j = 25\,^{\circ}\mathrm{C}$, dynamic power density is around 10 W/cm^2 where the value for static power density was almost 200000 times smaller than that of the dynamic power density for the same gate length. Nevertheless, both densities increase as devices are scaled down with a drastic increase in the static power density to the extent that both the power densities would be equal for 20 nm gate length devices [16]. Figure 1.6 illustrates the relation between both the power densities with respect to gate length. The severity of this problem poses one of the greatest challenges in the way of further scaling of the CMOS devices.

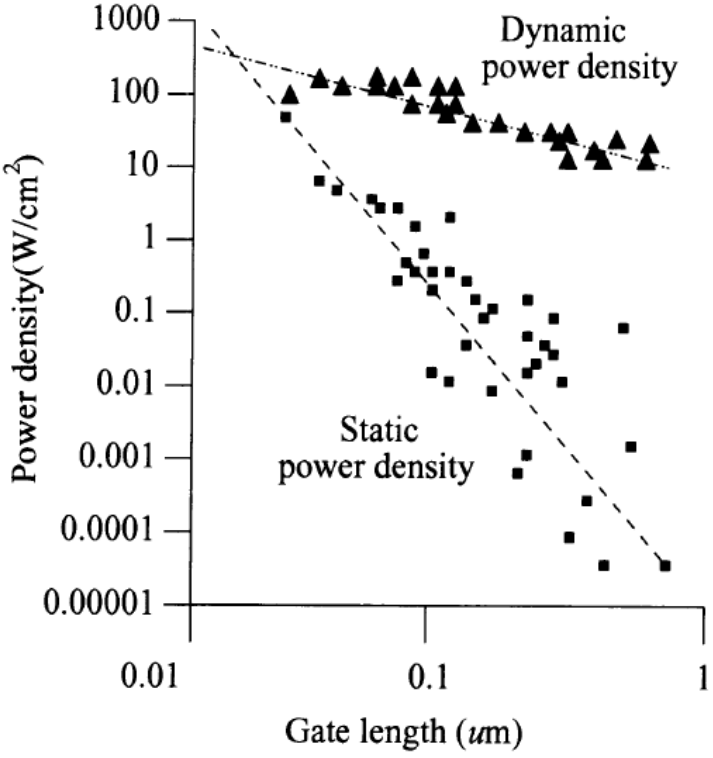


Figure 1.6: *Representation of the relation between dynamic and static power densities with respect to gate length. Reproduced from Ref. [6].*

Another constraint on the miniaturization of CMOS devices lays behind one of

the key manufacturing processes. Today's IC technology depends strongly on optical lithography for mass production. However, the resolution of this particular type of lithography depends strongly on the wavelength of the light used, apart form some other minor process-related factors. The current lithography technique is based on Ultraviolet (UV) optics. However, due to the relatively large wavelength of UV, the theoretical limitation on the spatial resolution in current photolithography hinders the further miniaturization of IC elements. Spatial resolution is a function of wavelength and numerical aperture as given in equation 1.1

$$Resolution = K\lambda/NA \tag{1.1}$$

where K is a constant that depends on the process being used. Efforts have been made in transforming the illumination light to lower wavelengths, such as Extreme Ultraviolet (EUV) and Beyond Extreme Ultraviolet (BEUV)- aiming 13.5nm and 6.8nm respectively. This is aimed at increasing the resolution. However, til their commercialization, we are limited to the current IC technologies [17, 18].

Beside all the above mentioned constraints and limitations surrounding the scaling of IC components, there is another dimension of the problem which further hinder the advancement of the current technology. Any attempts to implement new technologies to the existing industrial mass production processes of IC, would require the investment of a tremendous amount of money. The equipments and facilities costs, as well as complexities in new lithography processes are some examples of the reasons behind production cost increase [13, 19]. Nevertheless, it is clear that huge investments in this field are inevitable regardless of whether improvement of the current CMOS production technology is intended or new materials are introduced to replace the current silicon-based technology.

1.3 Promising Alternative

Many materials are being investigated as complementary or complete alternative to the current CMOS technology. Some proposals are such as carbon nanotubes field-effect transistors (CNTFETs) for their outstanding mechanical strength, thermal stability, low power consumption and high resistance to electromigration [20]. Similar proprieties are pointed out for semiconductor nanowire filed-effect transistors (NWFETs) [20]. Some other devices based on manipulation of magnetic dipole interactions such as spin field-effect transistors (SpinFEts) are also proposed for their high gain, low power consumption, high operating speed and small off-current [20, 21]. New ideas are constantly emerging to cope with the fast advancement in IC technology. Wide range of materials are investigated and numerous research are conducted world-wide in this field.

One promising class of materials that attracted a significant attention in the filed of electrical switching and logic operations is transition metal oxides or otherwise called d-electron systems. Due to the strong electron interactions owed to their electron configurations, peculiar phenomena are observed in such systems. One instance of such phenomena is the metal-insulator transition (MIT). This type of phase transition is accompanied with resistivity and structural changes within the material, that make such materials so attractive to investigate for both the understanding of the physics behind such phenomenon and for possible implementation of such materials in future electronics. The most investigated material among transition metal oxides in this regards is vanadium dioxide (VO_2) for many reasons including that it undergoes the MIT near room temperature unlike other materials in the same class. Further details on properties of VO_2 and their relation to MIT, d-electron systems and strong electrons interactions are present in the following chapter.

1.4 Motivation

The limitations encountered in miniaturization of metal oxide semiconductor field effect transistors needed for more compacted ICs and faster logic operations triggered the quest for alternative materials for further advancement in future computing technology. Many research, including this study, are motivated by this objective. As mentioned above, transition metal oxides offer attractive qualities such as MIT that can be exploited and toned in order to investigate high on/off ratio in electrical switching applications. This has already been investigated excessively in VO_2 lately. As sub-10 nm-thick single crystals of VO_2 are required due to Thomas-Fermi screening length, almost all studies conducted in this regards so far utilized epitaxial growth to obtain the required crystals. However, as such films are stressed due to lattice mismatch between the film and the substrate, those studies were not conclusive [22–24]. Moreover, inter-diffusion of vanadium and titanium at the VO_2- TiO_2 in sub-5 nm VO_2 films interferes with the quality of the films, causing further difficulties in reproducibility of obtained results [25–28]. Some other studies utilized sputtered VO_2 films instead, however investigating the effect of crystal thickness on the MIT is such films is almost impossible due to their polycrystalline nature [29, 30].

In this work, we propose the use of vapor-phase deposited free-standing VO_2 nanocrystals instead, for constricting Mott field-effect transistors utilizing MIT for electrical switching applications. However, random crystals' dimensions are produced in vapor-phase deposition, with typical minimum crystal dimensions of no less than 30 nm [31, 32]. Here we demonstrate a systematic use of argon-ion (Ar-ion) milling to produce the desired sub-10 nm-thick free-standing VO_2 nanocrystals that later are used in the ultimate goal of this study which is the attempt to demonstrate high on/off ratio VO_2 nanocrystal-based Mott field-effect transistors.

1.5 Thesis Overview

There are total of five chapters in this thesis. The first chapter is providing a general overview on transistors' history, their working principles, and the limitations hindering further miniaturization of MOSFETs in the current IC technology. The second chapter is an introduction to vanadium dioxide in general. The chapter discusses the electrical and structural properties of VO_2 and illustrates mechanisms by which the MIT takes place in VO_2 nanocrystals. The third chapter of this thesis is devoted to materials and methods used in this study. Crystal growth, etching processes, two and three-terminal device fabrication steps and all used characterization techniques are discussed in details in this chapter. Chapter four is devoted to results and discussions. All results of etch-rate study, ways to produced free-standing thinned VO_2 nanocrystals and results of electrical measurements taken from two and three-terminal devices are analyzed and discussed in this chapter. Finally, The overall conclusion of this study and future perspectives are available in the fifth and final chapter of this thesis.

Chapter 2

Vanadium Dioxide

To have a clear understanding of the reasons behind the wide range attraction to VO_2 in the research community for both fundamental and applied sciences, some concepts as well as other VO_2 related structural properties are to be discussed beforehand. Overview of d-electron system in transition metal oxides, and their relation to the emergence of strongly correlated systems and phenomena arise consequently is provided for the in-depth understanding of the behavior of such materials. Here, more attention is given to metal insulator transition on VO_2 as it is directly related to the main objective of this study.

2.1 d-Electron Systems

The electron configuration of transition metals is the main reason behind their attractive unusual and sometimes hard to explain behaviors. Proceeding using vanadium as an example when discussing transition metals would be convenient as it is the element of interest of this specific research. Also in this discussion, the inner transition metals or otherwise known as f-electron elements are excluded.

2.1.1 d-electron Elements

The naming d-electron elements is due to their partially occupied d sub-shell. Their valence electrons exist in more than one shell, explaining their several common oxidation states. Strangely, their electron configurations are not following Madelung order as usually taught from Aufbau diagram. Vanadium with an atomic number of 23 for instance has an electron configuration of $[Ar]3d^3 4s^2$ with 5 valence electrons. It is expected that 4s orbital would be occupied completely before any electrons start to occupy the expectedly higher energy 3d orbital. However, what happens in reality is totally different. In order to clarify the real condition, it is better to imagine building the neutral vanadium atom from its positive ions. Vanadium has multiple possible oxidation states, of which is the positive oxidation stat +5. Building up the neutral vanadium atom from V^{+5} would look as follows:
V^{+5}:[Ar], V^{+4}:$[Ar]3d^1$,V^{+3}:$[Ar]3d^2$
V^{+2}:$[Ar]3d^3$, V^{+}:$[Ar]3d^4$, V:$[Ar]3d^3 4s^2$
First of all, it is clear that electrons start occupying 3d orbital before the expected 4s. This is a bold indication that the 3d orbital has lower energy in this case then the 4s orbital, contrary to what Madelung order suggested. This is because what is known as "d-orbital collapse", which arises from the interplay of nuclear attraction, angular-momentum dependent centrifugal forces and imperfect shielding by the inner-core electrons [33–38]. It is clear from figure 2.1 that the energy of 3d orbital collapses below the energy of 4s for higher atomic numbers.

d-orbital collapse explains only the occupation of 3d orbital prior to 4s, however, it could lead to the false conclusion that all five valence electrons in a vanadium atom would completely fill the 3d orbital without occupying 4s orbital, given a configuration such as: $[Ar]3d^5$. However, it is well known that this is not the situation. The V^+ ion has the following electron configuration: $[Ar]3d^4$, yet the neutral form of vanadium with one more electron in the outer shell has an electron configuration that indicates further complications. The neutral vanadium atom has an electron configuration of $[Ar]3d^3 4s^2$, indicating that the last electron from the $3d^4$ moved along with the last added electron to 4s orbital. The reason

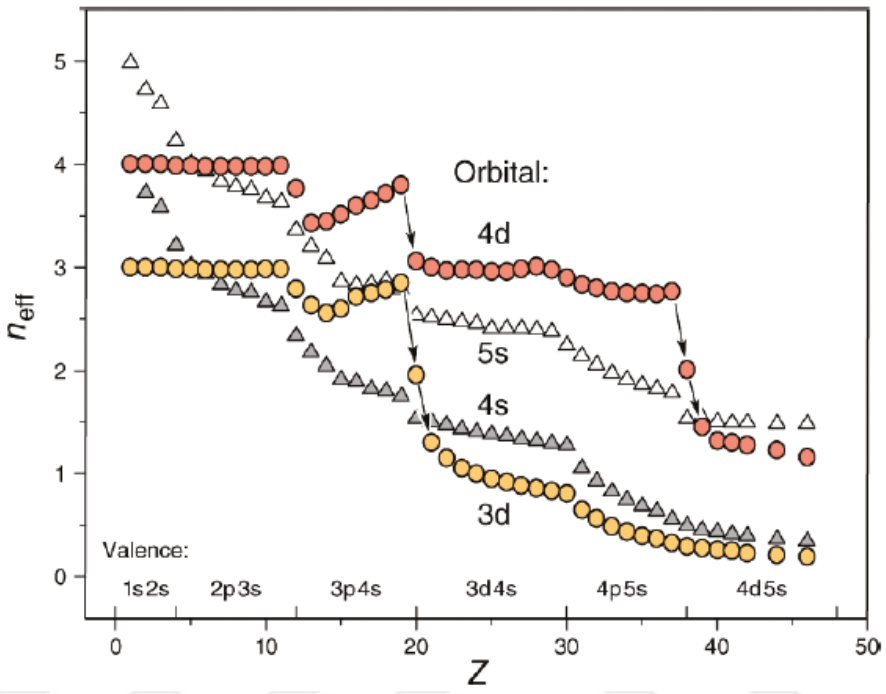


Figure 2.1: *Energetic d-orbital collapse of free neutral atoms at the beginning of the transition rows. where Z is the nuclear charge and n_{eff} is th effective quantum number representing the orbital energies ε. Reprinted with permission from [W. E. Schwarz, The full story of the electron configurations of the transitionelements,Journal of Chemical Education, vol. 87, no. 4, pp. 444448, 2010.]. Copyright [2010] American Chemical Society [39].*

behind such a behavior is that a dramatic increase in electron repulsion in the d shell is resulted from the increasing in d-orbital occupancy. When this repulsion energy is greater than the d-s orbital-energy separation, it becomes more energetically favorable to shift some of the electrons (one or two) from 3d to 4s orbital , in order to reduce the Coulomb repulsion [39]. This clearly show that it is not correct to generalize a configuration scheme for all the transition elements, rather it is a trade between the electronic Coulomb repulsion within a given d-orbital, and the d-s orbital-energy separation for each given transition element. Each element would assume more energetically stable electron configuration, regardless of the configuration of other transition elements.

2.1.2 d-Metal Compounds and Strong Correlations

When it comes to d-metal compounds, many parameters contribute to the complexity of such systems. d-metals construct different transition metal complexes as they can bond to variety of ligands. The emerging ligand p-metal d hybridization is one of the key parameters that define the properties of such complexes. It has been shown that this hybridization displays systematic trends with parent d-metal valence state and atomic number [40]. The on-site Coulomb interaction U_{dd} between the 3d electrons in the transition metal, and the charge transfer energy Δ needed to transfer an electron from the ligand p orbital to the metal 3d orbital are the other two main parameters that dictate properties of d-metal compounds [41]. The many-body nature of the valence electrons of such compounds is the reason behind why one-electron band-structure calculations fail to describe their electronic and physical properties [40].

2.1.3 Metal-Insulator Transition in d-Electron systems

One way by which parent d-metal affect the final complex electronic transport behaviors is their narrow bandwidth of d-orbital band [42–45]. This signify the electron-electron Coulomb repulsion (correlation effect) to the extent that it surpass the charge transfer energy ($U_{dd} > \Delta$), resulting in electron localization that leads to insulating transport and consequently the formation of Mott insulators [46]. This is one of the mechanisms by which a first order phase transition known as Metal-Insulator transition (MIT) in transition metal oxides takes place.

An attractive d-electron system to study strong correlation related phenomena such as MIT is vanadium dioxide, as it exhibits MIT near room temperature ($T_C \sim 65\,^{\circ}C$), accompanied with a structural phase transition [47] and a five order of magnitude change in resistivity. The electron-lattice interactions in d-systems also introduce lattice distortion, doubling the lattice constant that result in metal-metal dimerization. This distortion opens up a gap at the Fermi level, leading to the formation of what is known as Peierls insulator [48]. Both the metal-metal

dimerization and the consequently introduced band gap are shown in figure 2.2. The nature of MIT in correlated materials and the mechanism by which it takes

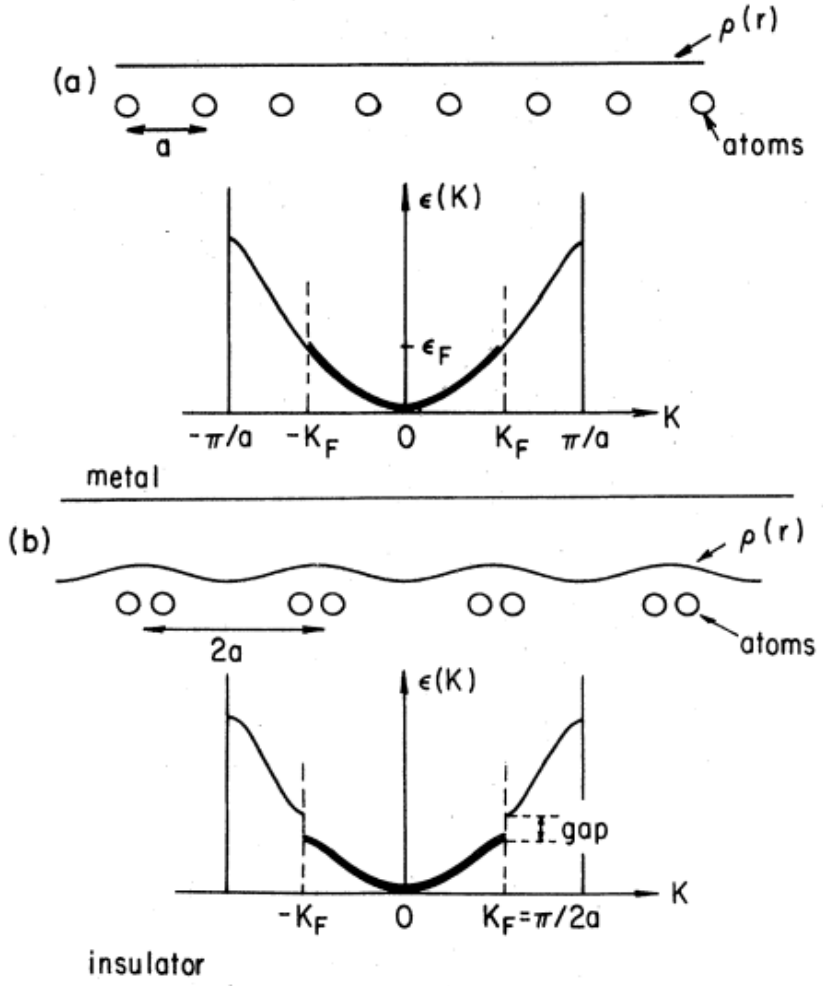


Figure 2.2: *Peierls distortion in a one-dimensional metal with a half-filled (up to the Fermi level ϵ_F) band: a) undistorted metal; b) Peierls insulator, where a is the lattice constant and $\rho(r)$ is the charge density. Reproduced from Ref. [48] with permission from the American Physical Society, License Number: 4146461335789.*

place, whether it is a Mott [49,50] or Peierls [51–53] transition, has been a subject of debate for several decades. Some studies proposed that it is a cooperation of both these mechanisms [54, 55]. However, the clear understanding of the nature of MITs in correlated systems is still incomplete and quite challenging to achieve [49, 56, 57].

2.2 Vanadium Dioxide Crystal Structures

The four oxidation states of V: +2, +3, +4, +5 are behind the wide variation on existing vanadium oxides. The near room temperature ($T_C \sim 65\,^{\circ}$C) MIT in VO_2, with V^{+4} valence, along with its stability, makes it the most attractive compound in the group. The MIT is accompanied with a structural transition from the high temperature metallic tetragonal (rutile R) phase to the low temperature insulator (monoclinic M1) phase. Uniaxial stresses introduce another monoclinic (M2) phase. The lattice of the tetragonal rutile VO_2 has a space group $P4_2/mnm$ with lattice constants $a_R \approx 4.55$ Å and $c_R \approx 2.86$ Å [58,59]. In this structure, the oxygen ions form octahedra at the center and the corners of the unit cells, where the vanadium ions occupy the interstitial sites of these octahedra. Figure 2.3 is a representation of the rutile phase structure in VO_2. Neighbouring unit cells share a common edge among their octahedra along c_R. The electrical conductivity in this structure is higher along the c-axis due to the difference in separation between vanadium ions and the off c-axis separation [61, 62].

Below T_C, dimerization of V ions start taking place along [001] direction as a result of the movement of V^{+4} away from the octahedral-interstice center due to anti-ferroelectric distortion along the rutile [110] $[1\bar{1}0]$ directions. This result in the formation of low crystal symmetry of $P4_1/c$, corresponding to the monoclinic phase [63]. There is a miner movement of the oxygen atoms accompanying this transition. The introduced optical gap of the insulating M1 phase which is around 0.59 eV [64,65]. The monoclinic phase has lattice constants of $a_{M1} \approx 5.75$ Å, $b_{M1} \approx 4.54$ Å, $c_{M1} \approx 5.38$ Å, and $\beta_{M1} \approx 122.65\,^{\circ}$ [66]. The V atoms in this phase are dimerized and configured in a zigzag-like pattern. The schematic representation of the monoclinic structure of VO_2 is present in figure 2.4. As shown in the figure, this phase exhibit an alternation in the V-V distance of around 2.65 and 3.12 Å indicated by yellow and orange arrow respectively [58, 67].

VO_2 has other possible phases such as the insulating monoclinic (M2) and the triclinic (T) phase. The M2 phase is reported to have lattice constants of $a_{M2} \approx 9.07$ Å, $b_{M2} \approx 4.54$ Å, $c_{M2} \approx 4.53$ Å, and $\beta_{M2} \approx 91.88\,^{\circ}$ and lattice

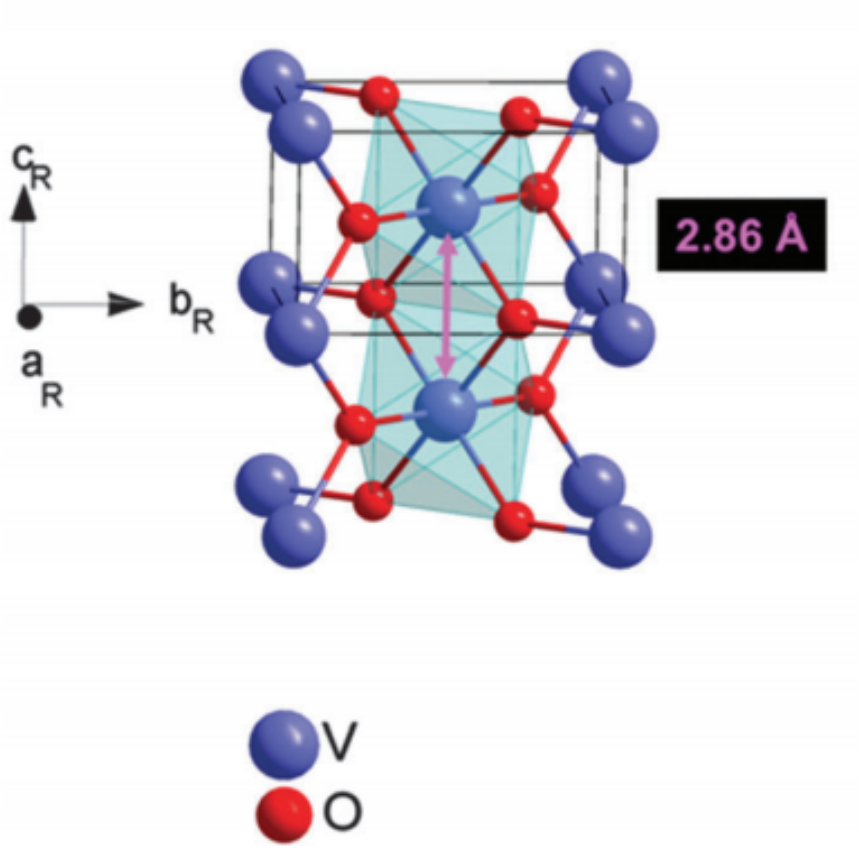


Figure 2.3: *Crystal structure of the tetragonal rutile phase in VO_2. Reproduced from Ref. [60] with permission from the PCCP Owner Societies.*

space group of c_2/m [59]. This phase can be stabilized through doping [68, 69], or straining along the c-axis [65, 70, 71]. Where as for the triclinic phase, it was reported to have lattice constants of $a_T \approx 5.71$ Å, $b_T \approx 4.49$ Å, $c_T \approx 4.53$ Å, $\alpha_T \approx 88.26\,^\circ$, $\beta_T \approx 122.50\,^\circ$ and $\gamma_T \approx 90.18\,^\circ$ [72]. An important thing to mention about the T phase is that its transition from M1 is reported to be a second order transition unlike its transition from and to the M2 phase that are both first order transitions [68]. T phase was also shown to have higher resistivity than M1 phase [73].

With this constantly expanding knowledge that we have about VO_2, it becomes more attractive to both implement it in new applications as well as study it further to reveal more interesting science. This work is combination of both these objectives, as further understanding of VO_2 is pursued and its use in a

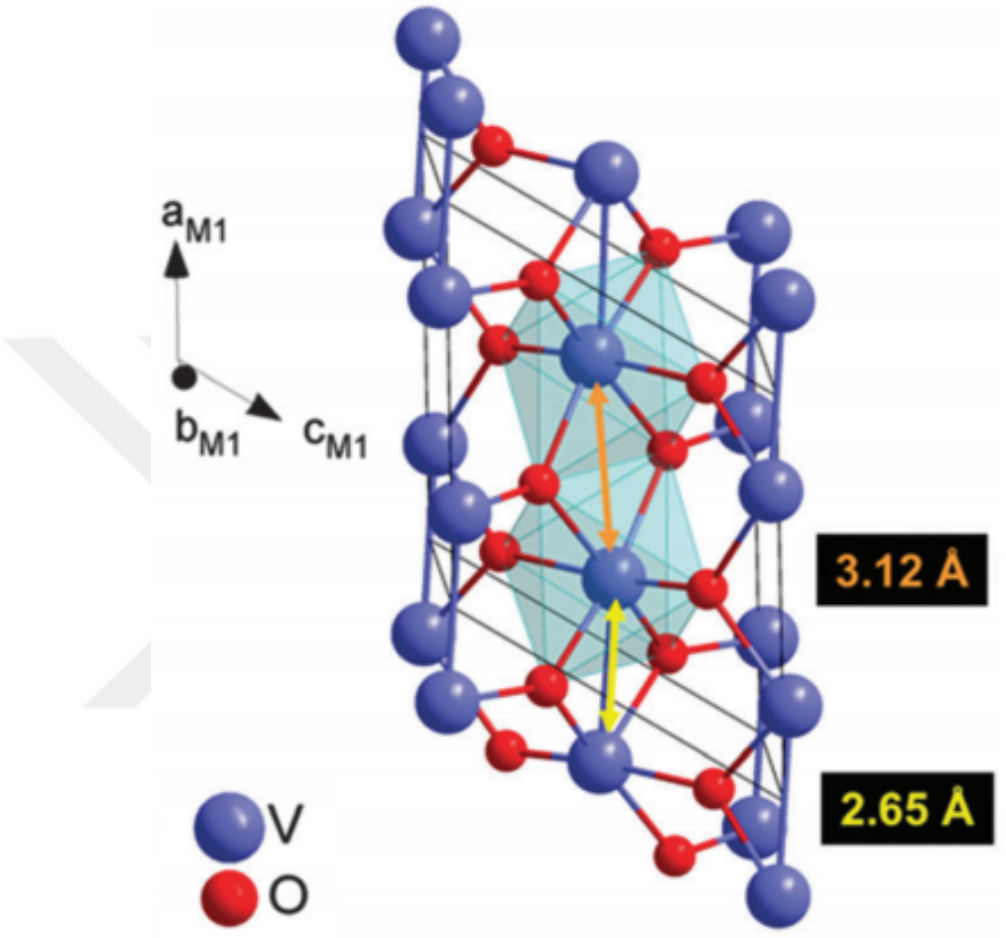


Figure 2.4: *Crystal structure of the monoclinic M1 phase in VO_2. The arrows are representation of the variation in V-V distances. Reproduced from Ref. [60] with permission from the PCCP Owner Societies.*

potential novel application is investigated.

Chapter 3

Materials and Methods

In this study many fabrication techniques and analytical methods were used in order to construct Field-effect transistors based on vapor-phase grown VO_2 nanocrystals. Many successful and unsuccessful methods were attempted, nevertheless, out of each of them some useful information were extracted. Therefore, all the fabrication techniques and analytical methods which were conducted all through the duration of this study are reported in a comprehensive order within this section.

3.1 Crystal Growth

The production of VO_2 nanowires and nanocrystals using vapor-phase transport method was first reported in 2004 by B. S. Guiton [31]. Here we use the same method of physical vapour deposition, however, almost all the parameters were modified and toned in order to produce larger cross-sections of VO_2 nanocrystals as it is presented later in this section.

As it is always the case before any growth process, selecting a right substrate is the first step. Contrary to what is reported by B. S. Guiton, we were able to produce dense wide nanobeams using SiO_2/Si substrate. The precise selection of

the thickness of the oxide layer is not of a vital importance as the crystals are transferred to different substrates in a later step after growth. The substrate used here is a p-doped (100) Si substrate with 1 μm thermal oxide on top. Another conventional step is the pre-growth cleaning of the wafer, however, it had been realized that a fully cleaned wafer will produce a range of low density to an empty substrate. Therefore, minor trace of volatile or organic materials that burn at relatively low temperatures yet leave behind high energy surfaces or nucleation sites were tested to be effective in achieving high density growth. Having realized that, we leave glove's fingerprint on substrate prior to placing it in furnace. Nevertheless, crystals produced this way have proven high quality and no signs of any contamination as is explicitly shown in the results and discussion chapter.

3.1.1 Furnace

In order to conduct the vapor-phase transport, a three zone split tube furnace (Protherm furnaces brand, made in Turkey) was utilized. As the name of the furnace indicates, it has three different zones that are separately controllable, that is each section can be set to a different ramp rates, holding intervals and temperatures. A three-dimensional representation of the furnace and relative parts are shown in figure 3.1 below. The inlet of the furnace is connected to an Argon gas tube where on the other hand the outlet is connected to a vacuum pump which maintains a low pressure environment of 1.2×10^{-2} mbar inside the furnace's tube. Furthermore, the supply of argon gas is present for some essential reasons. First of all, Ar serves as an inert environment during the critical stages of the growth. Secondly it acts as a medium by which the physical vapour of source material is transported from the boat upstream to the hot surface of the substrate downstream. One more important detail is that in order to have control on the amount of argon gas passing through the tube of the furnace, a pressure gage is connected to the outlet to serve this purpose.

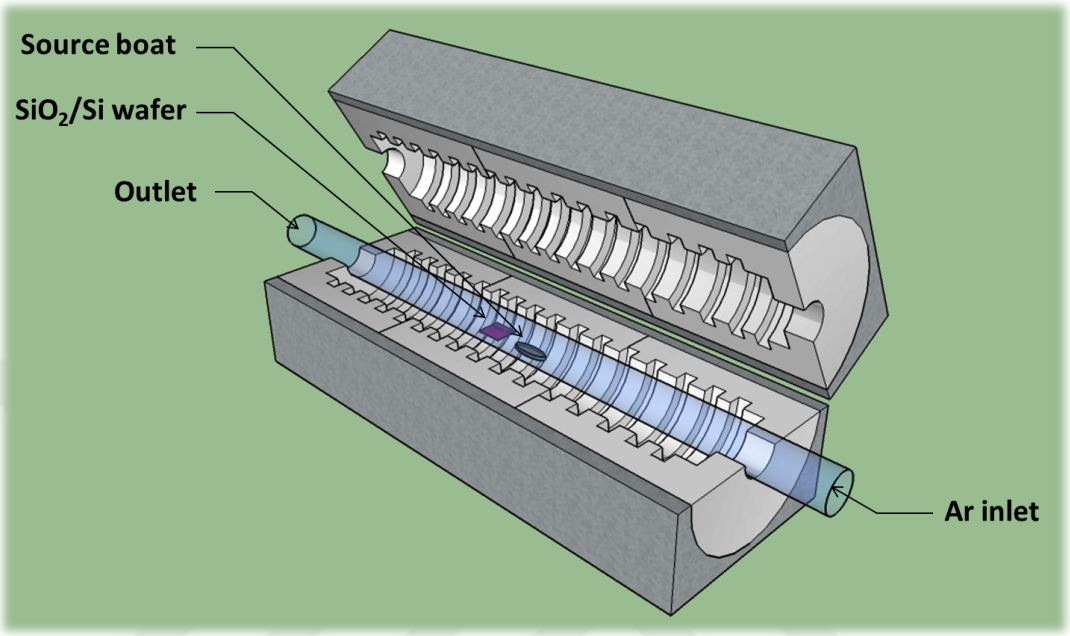


Figure 3.1: *A 3D representation of protherm furnaces brand furnace that is used for vapor-phase growth of VO_2 nanocrystals*

3.1.2 Growth Parameters

The general growth procedures start with selecting the source materials. Here, V_2O_5 in its powder form is used as the precursor material. Around 25 to 35 mg of V_2O_5 is placed in an alumina boat. The boat then placed inside the tube in a way that it will be situated toward the center of the mid-zone of the furnace. Then a SiO_2/Si substrate with a glove fingerprint is placed 1 to 2 cm from the boat downstream provided that both of them are within the borders of the mid-zone. Following, all the three zones of the furnace are set to ramp up to 850 °C within a period of 20 minutes and then hold that same temperature for more 20 to 25 minutes. At this point, the vacuum tube must be attached to the outlet end of the quartz tube and the furnace's lid must be closed. After turning the furnace's power on, Vacuum pomp must be turned on immediately, however, the vacuum valve must be opened in a very slow manner to avoid sucking up both the substrate and the source boat. The supplying of Ar gas must be done at a gas pressure around 2.5 to 3 mbar during the ramp up stage when the mid-zone temperature hits 680 °C, and should be kept running throughout the remaining

period of the growth. When the growth time is up, the Ar supply must be cut off and the lid of the furnace should be opened immediately in order to rapidly cool down the substrate. It is essential to keep the vacuum pomp running till below 250 °C in order to avoid any possible oxidation or contamination of the hot crystals. After switching off the vacuum pump, vacuum can be broken by applying Ar flow for few seconds till the vacuum tube is released out of the outlet end of the quartz tube. The complete removal of the substrate out of the quartz tube is done whenever it is comfortable to handle that tube. By the end of this step, the growth process is considered done. The only remaining thing is to inspect the quality of the growth.

3.2 Etching Process

This part of the work was the most time consuming yet the most rewarding part of all the processes done in this study as we were able to demonstrate new etching procedures that are presented for the first time. Our aim was to figure out the etching rate for the vapor-phase grown VO_2 nanocrystals to systematically etch such crystals down to thicknesses lower than the screening length. It was obvious since the beginning that in order to figure out the right etch rate of VO_2 nanocrystals, we would need sets of samples that would be etched at various durations. In each of this samples we had to create a reference point to which we can refer in order to know how much of a crystal we had etched each time. We were able to construct these required reference point on our specimens, however due to some problems and difficulties that we had encountered in this first process as is explicitly discussed later in this section, we had to come up with an alternative process that is much easier and time saving relative to the first one. Fortunately we were lucky enough to come across a valuable detail that helped us on developing a better etching process. Both methods are described in details in the following subsections.

3.2.1 Method 1: Photoresist Masking

The first method that was utilized in order to protect some parts of the etched crystals in order to refer to when measuring thickness is photo-lithography. Here, a crystal is firstly specified then its location within the substrate is marked in order to assist its finding under the mask aligner. In our case, a scratch is drawn using a diamond tip indicating the crystal position as shown in figure 3.3a. Nevertheless, the finding of the specified crystals under the photo-mask was still difficult as the objective fixed to the mask aligner has only 10x magnification with only black and white view as shown in figure 3.2. Therefore, some few picture of the position of the crystal at different magnifications under a normal light microscope had to be taken to compare to what would be seen under the mask aligner. Moreover, the specified crystal is preferred to have a wide surface dimensions in the range of few microns to reduce the difficulty of measuring the thickness difference between the etch and pristine sides of the crystal (step size).

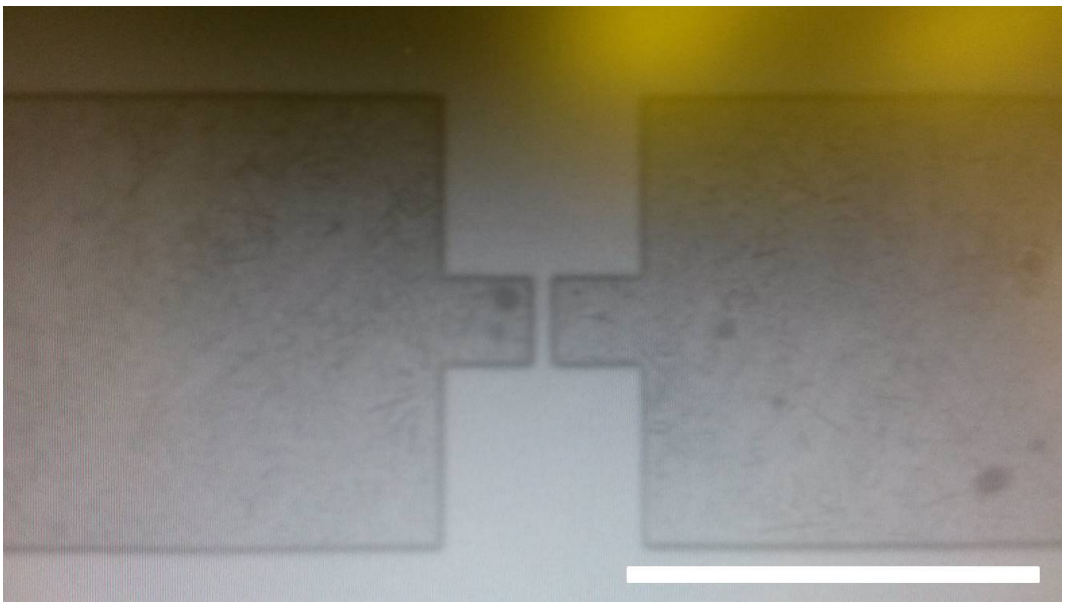


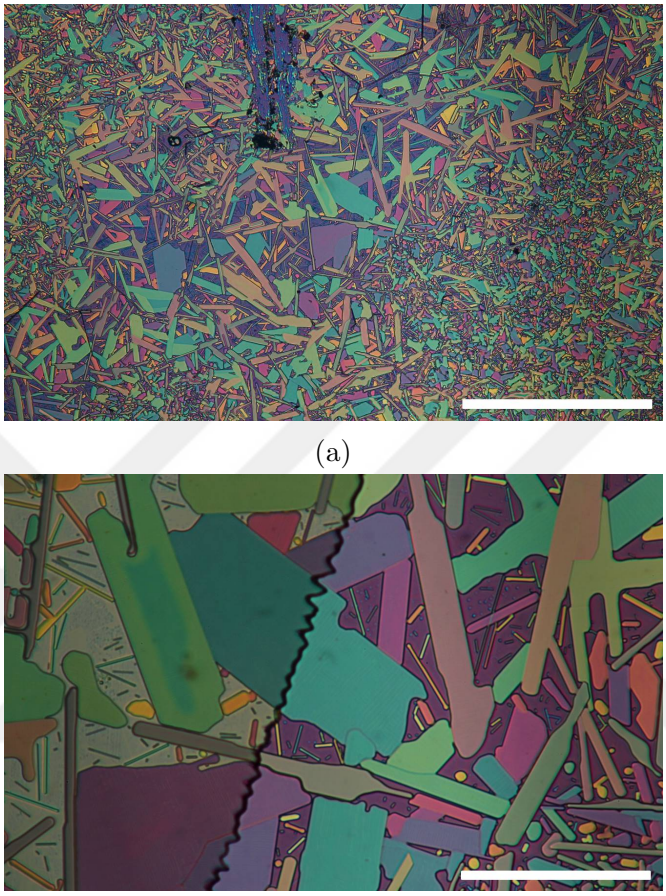
Figure 3.2: *A picture indicating the difficulty of identifying crystals below photo-mask under the 10x objective available in the mask aligner. Scale bar is* 20 μm

3.2.1.1 Optical Lithography

The photoresist that was used is AZ 5214E which is a reversal photoresist, that can be changed from being positive photoresist to negative one by adding a flood exposure (no mask) and reversal bake step respectively, however, here it is used in its positive form. The procedures start with cleaning the sample using acetone followed by isopropyl alcohol (IPA) and finally distilled (DI) water. This step is followed by a baking at 120 °C on a hotplate meant to eliminate all moisture present on sample. After that the sample is placed on a spinner and fixed down by the vacuumed surface of the sample holder. The photoresist then applied on sample in the form of drops in a uniform way. The settings of the spinner depend on the type of photoresist used. Recipes from producers can be used or process dependent recipes can be developed otherwise. As for AZ 5214E, the spinning speed is set to 6000 rpm for 50 seconds to achieve a coating film thickness of about 1.4 μm. A pre-exposure baking step at a 110 °C for 50 seconds on hotplate is required to stabilize the coating and also activate a special crosslinking agent in the resist formulation for those who are aiming to use the image reversal propriety of the resist as mentioned on the product data sheet. Afterward, the sample is ready for exposure, so mask aligner (EVG 620 Mask Aligner System) is used by placing both a proper photo-mask and sample into the equipment and then the setting of exposure parameters including the indication of substrate and photoresist thickness and exposure dose ,which is 40 mJ/cm^2 in our case, is required.

After UV light exposure, the sample is developed to reveal the patterns. AZ 400 developer is used in water diluted form at a developer to water ratio of 1:4. The optimum required time of removing the UV exposed parts of photoresist is around 50 seconds, then sample must be flushed with water in order to interrupt the developing process and avoid over development. An example of a sample that underwent this process is present in figure 3.3b. Samples are then inspected using optical microscopy.

After the sample is etched, the photoresist covering the pristine part of the



(a)

(b)

Figure 3.3: *a) Scratch using a diamond tip indicating the crystal position used to assist locating the specified crystal under mask aligner. b) Half coated crystal pre-etching for reference point establishment. Scale bars are* 40 μm *and* 200 μm *respectively*

crystal must be removed. This is known as the lift-off process where some chemicals are used to strip out that remaining layer of photoresist. When any process along the way that the sample undergoes between photolithography and lift-off is above room temperature, the removal of the photoresist becomes harder due to the chemical changes that take place in its composition. Usually acetone is enough for lift-off, however, in such cases the use of removers is required. Etching process itself is causing the heat up of samples and therefore removers are to be used. AZ 100 remover is used, and according to the producer, for not extremely high temperature processes, samples must be submerged in 80 °C heated remover for around 8 to 10 minutes to achieve the lift-off. However, in most of the

cases it was not possible to completely remove the resist, and therefore precision thickness measurements using Atomic Force Microscopy (AFM) were almost not achievable, the thing that urged the finding of alternative masking processes.

3.2.1.2 Etching Equipment and Procedures

Two different equipment were used at different stages of this study in order to mill down VO_2, namely Precision Etching Coating System (PECS) and Thermo Scientific K-Alpha X-ray Photoelectron Spectrometer (XPS) System. Due to some problems encountered using PECS as is explained below, XPS System was utilized the most throughout our experiments not only for etching but also for elemental analysis. Below is an explicit explanation of the procedures followed using both systems.

3.2.1.2.1 Precision Etching Coating System (PECS)

The use of PECS is quite simple due to the simplicity of the equipment itself. The whole process depends on few manual keys that need to be set and then the system should be observed. The system can also perform multipurpose coating, however, this is out of the scope of this work. Nevertheless, to use the etching function of the system, some equipment components that are related to the coating process have to be either disabled or shielded. The system has a thickness monitoring sensor that works to stop the coating process at the desired film thickness, which needs to be disabled before staring the etching process; otherwise the monitoring unit might permanently be damaged. Another essential detail is that if any of the coating sources is inserted into the sample chamber, etching will not take place even if the system seems like working, and therefore this might lead to deceiving conclusions.

After venting the sample chamber, the sample is placed at the middle section of the sample holder and then the (in) switch is switched back to pump the chamber. Sample stage rotation switch is turned on, to maintain uniform etch

rates all around the sample, and set at 10 rpm. Both the current supplied to the etching gun and consequently the ion beam energy are set up manually. We tend to keep these parameters fixed for all samples and only change the duration of etching to figure out the thickness change time dependency. The current supplied to power the ion gun is fixed at 100 μA and the applied beam energy is maintained at 3 KeV. However, Although some fair results were achieved using PECS, due to the instability and fluctuation on the ion beam energy during operation, the long term use of the equipment is considered to be out of question as it is not meeting the precision level required in such an advanced research. Therefore, the XPS system was a successful stable alternative to use for etching as is explained later.

3.2.2 Method 2: Shadowing Effect

As the complete removal of photoresist after the etching process is hard and its residue poses a great hinder on thickness measurement, an alternative reference point establishment technique had to be found. However, not many choices were available. The use of XPS instead of PECS for etching process was already taking place by then and test samples were deeply investigated for the in depth understanding of the accuracy of the ion etching function of the equipment. A strange profile of etched crystals draw our attention and curiosity for further investigation, and consequently led us to what we later called "The shadowing effect" as is discussed next.

3.2.2.1 X-ray Photoelectron Spectrometer (XPS)

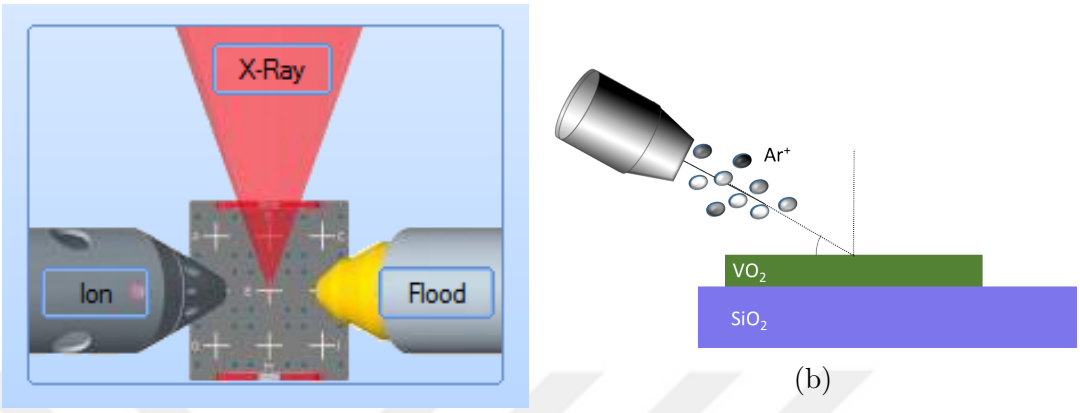
X-ray Photoelectron Spectrometry is a surface sensitive elemental identification and characterization technique. Therefore, in order to make possible the study of elements present within the body of samples (more than 3-10 nm) an Ar ion gun is available as part of the setup so that depth profile analysis can be done using the equipment. In the depth profile analysis, the surface of sample is etched

to the desired depth using the ion gun and then photoelectrons are collected for elemental identification. This step is repeated for revealing depth profile of a given sample. The elemental analysis of the XPS technique is used in this study as explained later in this section, however, the function of the setup that we mainly utilized is the ion etching.

Similar to PECS and all dry etching systems, ion gun energy as well as current supplying the gun power are some of the most important parameters to pay attention to in XPS ion etching process. The ion gun energy can be set to fixed values that range from 1 to 3 KeV for high energies and 200 KeV and 500 KeV as for low energies. As for current, there are only three available settings, namely High, Medium and Low. The etch rate of any given material is depending on what combination of these settings are chosen, apart from the material's intrinsic properties. Therefore, all samples undergoing etching for specific etch rate investigation must be conducted under the same parameters. In our case, we had chosen optimum values which are 1 KeV for ion gun energy and medium monoatomic flux all through the study provided otherwise is not indicated. Moreover, for testing smother etching side effects, lower setting values are used and they are indicated in the relevant sections. The spot size of the ion gun is ranging from 30 μm to 400 μm.

The process starts by placing the sample in the equipment's sample stage and then placing the whole stage back to the load lock. Sample is then transferred automatically to the analysis chamber where three types of guns are present. To the upper part of the sample stage when placed inside the analysis chamber is the X-ray gun fixed in an incline with respect to the stage. Where to the right of the stage is fixed the flood gun, used to discharge the analysis chamber, in a similar manner as the x-ray gun. Finally is the ion gun fixed in an angel of 32 $^\circ$ with respect to the sample stage and positioned to its left as illustrated in figure 3.4.

The position and angle of each of these guns are of vital importance as they effect the end result of analyses. Even the fixing clips should be placed in a way that they would not block the path of guns used at that specific analysis. After selecting the ion beam etch object and setting its parameters as mentioned



(a) (b)

Figure 3.4: *a) The view of guns positions with respect to sample stage taken from Avantage software. b) Schematic representation of ion gun position.*

above, the spot of sample that is desired to be etched must be assigned. However, the platter view camera has only a digital zoom option, therefore an indication mark to the position of the crystal might be required similar to the situation encountered with mask aligner. A thick well defined scratch can be identified in both equipments. After assigning the point, the process can be started.

The detailed results of this process are explicitly discussed in the results and discussion section, however, some important realizations (repetitive pattern) on etched samples related to the used XPS system must be indicated here. In one specific side of all crystals on etched samples, a step-like structure was realized as illustrated on figure 3.5. When deeply investigated, it turned out that those structures were forming on crystals' sides that are placed opposite to the location of the ion gun. This effect is later called shadowing effect and is caused by the angular projection of Ar ions in a way that crystals' bodies block the accelerating ions to reach the substrate vicinity located at the sides of crystals that are opposite to the ion gun position. This exact effect can be cause by any body on the surface of any given sample. Further elaboration on this effect is present in later chapters.

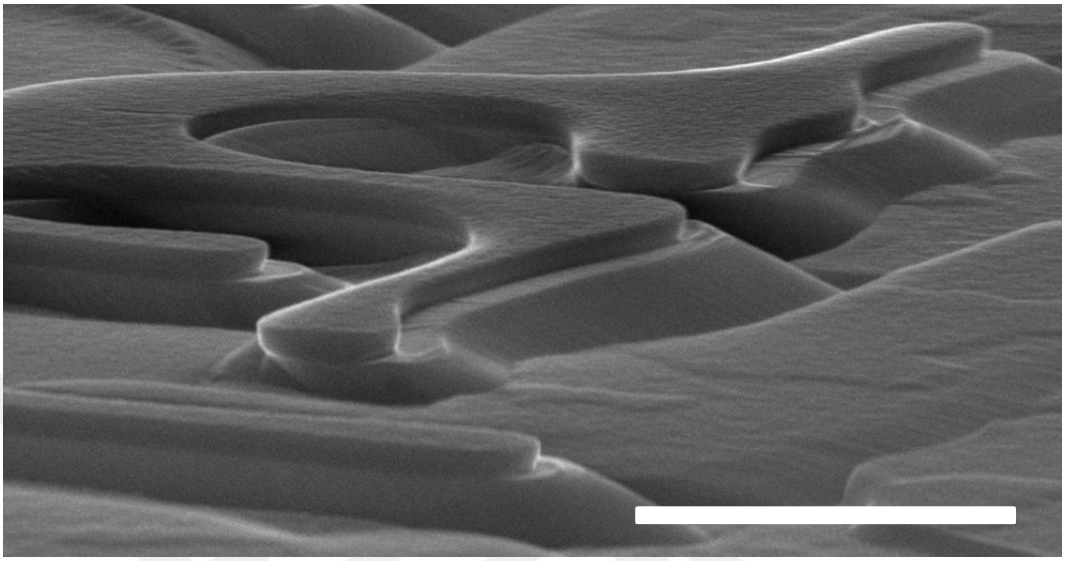


Figure 3.5: *A SEM picture showing the shadowing effect of VO_2 nanobeams due to the ion gun location in Thermo Scientific K-Alpha XPS System, The scale bar is 2 μm*

3.3 Device Fabrication

Systematic electrical measurements had to be done on VO_2 nanobeams after every step of the etching process in order to relate their electrical properties to the gradual variation in thickness up to the final desired crystal thickness. Therefore, all tested crystals had to be constructed in the form of two-terminal devices directly after growth to be able to achieve this step by step analysis. Consequently, device fabrication had been taken place in every stage of this study even before reaching the fabrication of the last three-terminal field-effect transistors. In this section we discuss the all steps of device fabrication methods and techniques.

3.3.1 Hexagonal Boron Nitrite (h-BN) Transfer

The proprieties of hexagonal Boron Nitrite (h-BN) and the reasons behind using it in both two and three-terminal devices are openly mentioned in the results and discussion. However, here the techniques used for the transfer are mentioned.

As h-BN is a graphene like material, isolating its layers is done in the same way as in graphene. In the year 2004, the mechanical exfoliation or otherwise called the repeated peeling of graphene layers out of highly oriented pyrolytic graphite using Scotch tape was reported by Andre Geim and coworkers [74]. Using this exact same technique, we were able to transfer few layers of h-BN on top of SiO_2/Si substrates. The same tape could be used effective for several times. However, to do so the tapes must be kept in an isolated place not to be contaminated. During transfer, contaminating the tapes when touching uncleaned surfaces or gloves is possible if great caution is not taken during their handling.

3.3.2 Crystal Transfer

As nucleation of VO_2 nanobeams and growth during vapor-phase transport happen at elevated temperatures, the crystals are embedded slightly into the softened SiO_2 surface. In most cases, the attempt of removing those crystals out of the oxide surface requires the etching of the top few nanometers of the oxide surface. An etchant must be used provided that it is highly selective of SiO_2 and not the VO_2 nanocrystals. The well-known wet etchant used widely in microfabrication to etch oxide films such as SiO_2 is the Buffered oxide etchant (BOE). It is a hydrofluoric acid HF diluted in a buffering agent (ammonium fluoride NH_2F) and water. HF is constructing only 7% of the whole mixture [75]. Nevertheless, it must be handled carefully as it can cause skin burns and great bone damages.

In order to facilitate the removal of crystals out of SiO_2 surface, the whole sample is dipped on BOE for few seconds and then is flushed by DI water to stop continuous etching. Then the dry sample is placed under an optical microscope stage that is placed near a motorized 3-axis micromanipulator (Marzhauser Wetzlar) as shown in figure 3.6. This manipulator has sensitivity of 25 nm and is controlled using 2-axis joystick. By fixing a 1 μm probe to the manipulator it is possible to poke crystals out of substrate and transfer them to a desired position on anther substrate. This technique is generally used to transfer VO_2 nanobeams above formally transferred h-BN for two-terminal devices. Moreover, the same

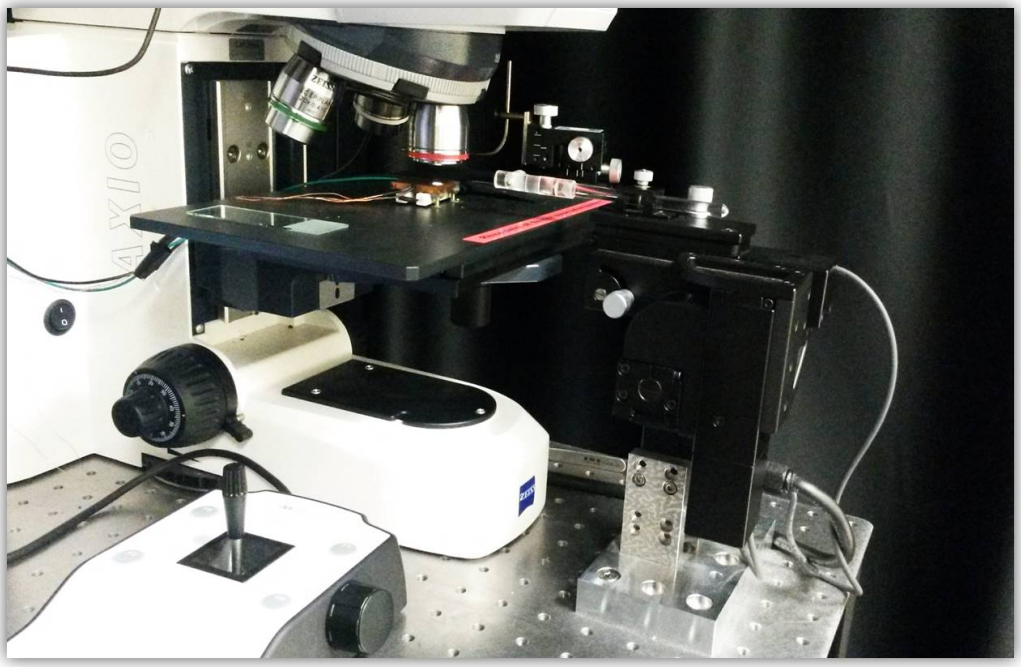
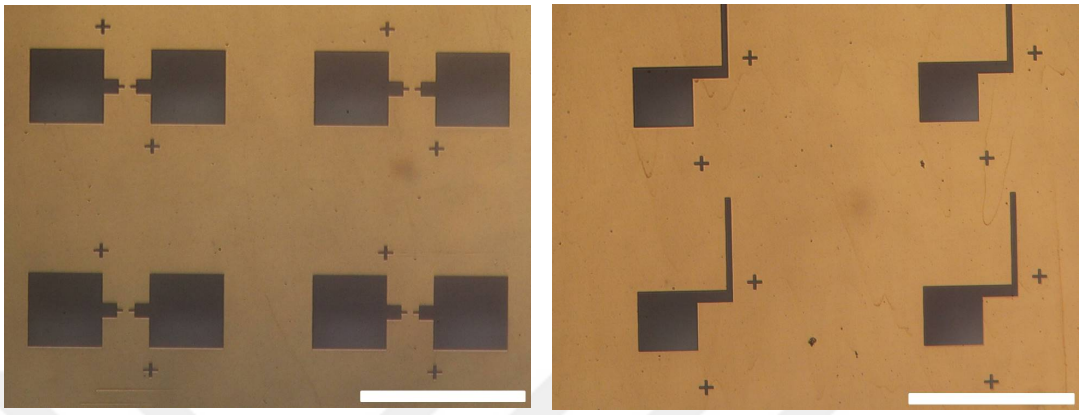


Figure 3.6: *Picture shown the Marzhauser Wetzlar micromanipulator with its 2-axis joystick located near an optical microscope*

micromanipulator is also used to place metal contacts as described later.

3.3.3 Optical Lithography for Contact Patterning

In microfabrication in general and integrated circuits fabrication in particular lithography plays a vital role. It is used here to build up both two and three-terminal devices. To avoid repetition, refer to lithography procedures mentioned on reference point construction for etching process as similar steps are used here in order to construct metal contact patterns. Moreover, the AZ 5214E is also used in its positive form during this process. A photo-mask, which is chrome coated to allow UV light only through the drawn patterns, is required. Those patterns are transferred through light to the surface of substrate with the help of photoresist. Multi-patterns mask is used throughout this work for many different purposes such as to construct metal electrodes' patterns as shown in figure 3.7.



(a) (b)

Figure 3.7: *a) Patterns used for metal contacts. b) Patterns designed for metal gate deposition. Scale bars are* 140 μm

3.3.4 Metal Deposition

To form the metal contacts and metal gates on two and three-terminal devices, metal deposition techniques are to be used. Among those techniques is thermal evaporation as well as e-beam evaporation, both stemmed from physical vapour deposition, are used the most here. In both techniques, target metals are heated to evaporation temperature under ultra-high vacuum (UHV) condition, to increase the mobility of metal particles and prevent metal oxidation, and deposited uniformly on the surface of a rotating substrate placed in the top of the evaporation chamber. However, the main difference between these two techniques is in the way the source is evaporated. In thermal evaporator system, the source metals are placed on tungsten boats connected to resistive element that is heated via electrical resistivity as current passes through it. The rate of deposition is controlled through current control. Where in e-beam evaporator, the source metal is heated using focused high energy electron beam. The electron beam is produced using hot filament and then controlled using focusing and deflecting magnets. Due to the limitation regarding the ability of resistive element to reach extremely high temperatures, refractive, low vapor pressure and high melting point metals such as titanium are evaporated using e-beam evaporator.

Another useful way that we mostly used on forming metal contacts on two-terminal devices is indium contact transfer. In this process neither the use of evaporators is required, as indium has a low melting temperature (156.6 °C), nor is lithography patterning. Equipments required to be able to place indium contacts are Peltier plate or temperature controlled stage placed under optical microscope, micromanipulator (the same one used for VO_2 crystal transfer) and indium source. The procedures start with raising up stage temperature to around 165 °C with indium source placed in top of bare substrate on the heated stage. A probe that is placed at the end of the manipulator is approached and dipped in the molten indium at 165 °C, then drawn back and upward simultaneously to get a rod-like pointed tip structure which is then moved and placed on the desired place on another substrate which is place on top of the same stage so that the indium rod would melt down and form a metal contact. All these steps are done on a live view obtained by a camera fixed to the optical microscope for easier control as shown in figure 3.8.

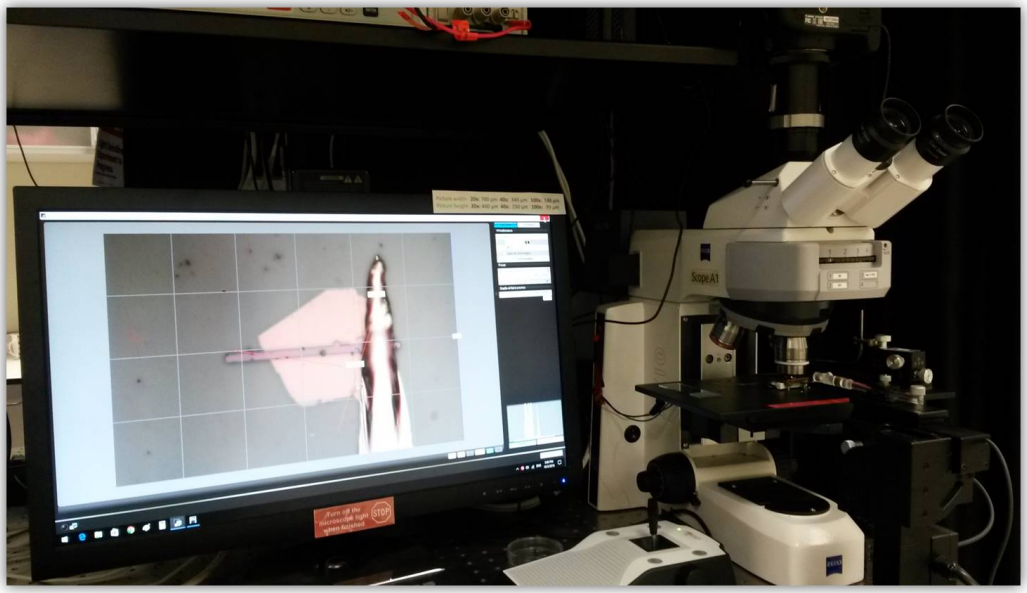


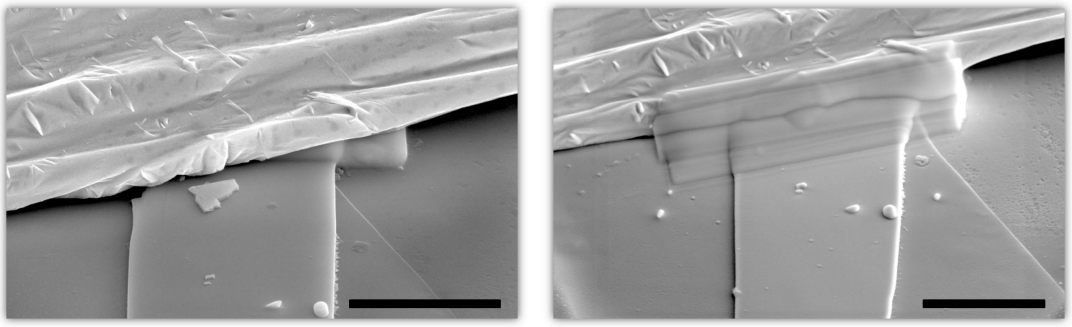
Figure 3.8: *A live view that is directly streamed from the camera connected to the microscope to a computer monitor*

3.3.5 Focused Ion Beam (FIB) Used for Indium Contact Fixation

When measuring the resistance dependency on temperature (R vs T) of VO_2 nanobeams and cross the T_c temperature the crystal structure chances form the low temperature monoclinic phase (M) to the high temperature tetragonal rutile (R). This transformation is accompanied with dimensional shrinkage of the crystals as R phase has much smaller unit cell then the M phase. Due to this dimensional change taking place on crystals as well as the softness of the indium contacts, the later tend to lose contact to crystals causing the loss of current running between the source and drain through the VO_2 channel, and consequently the malfunctioning of the whole device.

In order to overcome this problem, indium contacts fixation using Platinum (Pt) was introduced. This process is done using Focused Ion Beam (FIB) system by utilizing the Pt deposition gun available within the system. It starts by tilting the sample stage to around 56 ° in way that the Pt gun would face the side of the indium contact where it is contacting the VO_2 nanobeams as show in figure 3.9a. Then a pattern is drawn, using the patterning toll available in the FIB software, in a way that it would contain parts of both the indium contact and the nanocrystal as well as any empty space in between. The thickness of the Pt thickness is inserted to the software and the source is heated prior to the deposition. Then the Pt gun is inserted to the chamber and deposition is started. It is important to use the electron gun as a director to the deposition flow in order to avoid any harm to the crystal if otherwise ion gun is used. The optimum electron gun energy is 5 KeV and supplied by 1.6 nA. The obtained pattern is as shown in figure 3.9b.

This same technique of depositing Pt using FIB is using to fix down VO_2 nanobeams after transfer, provided that the metal contacts are going to be evaporated. The reason is that before evaporation, patterns are to be constructed to direct the evaporated metal. This Pattering is achieved through optical lithography which includes steps such as liquid photoresist application and high speed



(a) (b)

Figure 3.9: *a) Indium VO_2 nanobeams interface before Pt deposition. b) After deposition of Pt to fix down the Indium contact. Scale bars are* 3 μm

spin coating process during which freely placed VO_2 nanobeams are exposed to both unsteady flow of the liquid photoresist as well as centrifugal force exerted by the spinner. Therefore, Pt is deposited in the same manner mentioned above in order to keep the transferred nanocrystals in place throughout this process. Pt is also used to fixed crystals that are used for all types of devices that include the hydrochloric acid treatment step mentioned later.

3.3.6 Three-Terminal Devices Fabrication

The same steps mentioned above are used generally in the fabrication of three-terminal devices including crystal transfer and fixing, etching of the given crystal to the desired thickness after confirming its initial thickness using AFM. However, some extra steps are required to complete the three-terminal device configuration. The most important additional step is the removal of the conductive amorphous surface layer that emerge due to etching process. This step is crucial for the final device performance. The surface layer is removed using wet enchant. It is found that a short sample treatment using 37% hydrochloric acid ($HCl_{(aq)}$) removes the etch-introduced surface layer completely and leaves behind milled pristine VO_2 nanocrystals that are needed for three-terminal devices fabrication.

A thin flake of h-BN (no more than 4 layers) is then transferred above the

middle part of the crystal in a manner that it would cover an area a bit lager than the area the metallic gate would occupy. This h-BN flake would serve as a gate dielectric material.

Precision is required when transferring the gate dielectric h-BN flakes. It is not a random transfer as in the case for the h-BN flakes that are intended to be used as substrate for the free-standing VO_2 nanocrystals. The first step, however, is similar as exfoliated h-BN flakes are transferred onto a SiO_2 substrate. This substrate can then be used as a source for several other transfers. Now a polycarbonate film is needed to be prepared as it is going to be used for the transfer. 6% wt of Poly(Bisphenol A carbonate) granules are dissolved in 100 ml chloroform to form a solution. This solution is then poured and spread on a glass slide as film which is then left on open air to dry for one minute followed by another one minute on top of a 140 °C preheated hotplate in order to remove any remaining chloroform. The resulted dried film is then cut in the required size in order to be used for the transfer. A thin flake of h-BN is then targeted under optical microscope to be transferred. The transfer process is done with the setup that is used for both VO_2 and indium contact placement. This setup consists of an optical microscope and a micromanipulator with a sub-micron precision and a temperature-controlled stage. The polycarbonate film is then placed on top of the SiO_2 substrate that contain the targeted thin h-BN flake. The film is then precisely moved above the targeted flake using the micromanipulator. When positioning is done, the stage is then heated gradually upto 150 °C in order for the film to get attached to the flake. The film with the flake is now pilled at temperature around 100 °C. The pilled film is now attached to the manipulator tip while the sample that contains the processed VO_2 nanocrystal is placed underneath.

With the help of the optical microscope, the h-BN is aligned and placed on top of the mid-region of the VO_2 nanocrystal. After the placement of the film, it is pressed down with the probe in the surrounding of the crystal in order to reduce the effect of the film shrinkage and consequently the misplacement of the h-BN flake when the sample is heated for the second time. This second heating is done by rising the stage temperature to 150 °C in order to assure good adhesion

of the flake to the surface of the VO_2 nanocrystal and the removal of any air bubbles entrapment. After the sample is cooled down to room temperature, it is gently emerged in chloroform in order to dissolve the polycarbonate film. Usually, keeping the sample emerged in chloroform overnight would assure the complete removal of the polymer film. After this step, the device is ready for the next fabrication step which is either the placement of indium contacts or patterning the three pads of the electrodes through electron-beam lithography.

3.4 Characterization Techniques

Characterizing VO_2 nanobeams after etch process is vital to assure the conservation of the as grown crystal quality in terms of elemental and structural properties. Moreover, the monitoring of any intended or process imposed changes in the electrical properties of the nanocrystals is required. Many characterization methods such as atomic force microscopy (AFM), Raman spectroscopy, Scanning electron microscopy (SEM), transmission electron microscopy (TEM) and two point probe resistivity measurement were used to reveal relative characteristics of VO_2 nanobeams and VO_2 based devices. In this section brief explanations and overview of the ways each of the characterization techniques had been utilized is presented.

3.4.1 Atomic Force Microscopy (AFM)

Contact mode measurements were mostly conducted throughout this work. In this mode the deflection of the cantilever is kept constant using a position sensitive photodetector that registers the position of the laser light reflected from the top of the cantilever and feed that into a feedback loop which maintain the same deflection value regardless of features on the sample's surface. In order to obtain this constant deflection, force between tip and sample must be constant as well. The dominant forces between tip and sample in contact mode are repulsive Van der Waals forces. Therefore any surface features would cause variation on the tip

sample force and hence a deflection change. A piezoelectric positioning element then receives a lower or higher voltage through the feedback loop depending on the encountered feature to readjust the deflection of the cantilever. These applied voltage values are the measure for height of the features on the scanned surface. The scanning through the sample surface is done by a piezoelectric stage.

In the XE - 100E PSIA system that is used in this study, the piezoelectric stage has a maximum scanning dimensions of $45\mu m \times 45\mu m$ in the x-y plane. The type of contact probe used was silicon AFM probe with aluminum coated cantilever, resonant frequency of 13 kHz and force constant of 0.2 N/m. Samples had to be attached to the stage using two sided tape as the probe can drag the sample around due to the direct contact.

Atomic force microscopy had been mainly used for measuring as grown crystal thickness before any process is applied. Then measuring the difference in thickness between the reference point and the etched region of samples prepared for etch rate analysis. Moreover, the surface roughness of etched nanocrystals had also been measured using AFM in some cases. Although AFM has a wide range of use, they are out of the scope of this work.

3.4.2 Raman Spectroscopy

Analyses using Raman spectroscopy are based on light matter interactions. The elastic scattering of photons is referred to as Rayleigh scattering, and such photons are accounting for the vast majority of the interaction process' outcome. However, Rayleigh scattered photons do not reveal any information about the probed material. On the other hand, extreme minority of photons in the incident light are inelastically scattered. This type of scattering is known as Raman scattering and it occurs as a result of one of two different processes. When incident photons excite electrons at the ground state to a virtual state, these electrons relax back to a state with a higher energy than the ground state causing the release of photons that have lower energies when compared to the incident light. This process is known as Stokes scattering. The second scattering process takes place

when incident light excite electrons that already exist in a state higher than the ground state to a virtual state. The excited electrons then relax to the ground state releasing photons with higher energies relative to the incident photons and result in a process called anti-Stokes scattering. All the above mentioned scattering processes are illustrated in figure 3.10. The difference in energy between

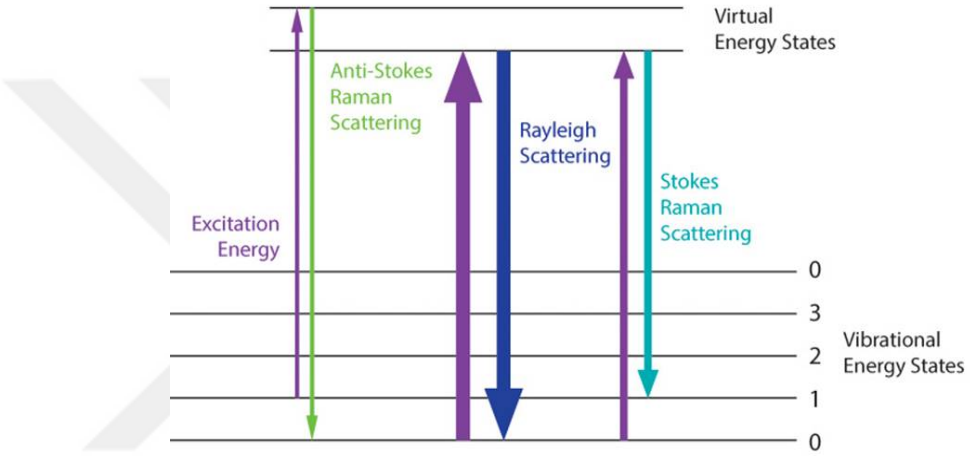


Figure 3.10: *A Jablonski diagram illustrating the both the elastic and inelastic scattering of incident light when interacted with matter. Reproduced from Ref. [76]*

incident and emitted photons matches the energy difference between two resonant states of the probed material, a quality that is characteristic of any given material. These energy differences between resonant states are independent of the incident light used.

Raman spectrometer (WITec Alpha 300) was used in every step of this project specifically to assure the quality of the VO_2 nanobeams after the milling and device fabrication processes. The incident laser light used in WITec Raman spectrometer utilized here is 532 nm. Moreover, a key parameter to keep in mind when any attempts are taking to obtain Raman spectra of VO_2 nanobeams is the intensity of the excitation laser light used. The applied laser light intensity must be much lower than the intensity which would induce a phase transition. In this work, single spectra with more than one accumulation were generally used. Relative results are shown and discussed in the results and discussion section.

3.4.3 Electron Microscopy

Many different types of analyses can be done using various equipments and modes of electron microscopy. When incident electron beam interact with matter, backscattered electrons, secondary electrons, Auger electrons, transmitted electrons, X-rays and photons are produced. Each of these can be detected separately and reveal different information regarding the probed material. Imaging, chemical and elemental analyses as well as structural analyses are some of what can be investigated utilizing electron microscopy. Moreover, modes such as energy dispersive x-ray spectroscopy (EDX) and Wavelength-dispersive X-ray spectroscopy (WDS) are used in scanning electron microscope (SEM) for elemental analysis, where modes such as high resolution transmission electron microscopy for imaging and selected area electron diffraction (SAED) for structural analysis are used in transmission electron microscopy (TEM).

Almost no sample preparation is required for samples that are to be analysed using SEM, provided that they are conductive. However, when it comes to TEM, tedious sample preparation steps are required to obtain an electron transparent sample. Mostly FIB is used to etch and transfer the part of sample that is going to be analysed to a suitable TEM grid. However, gallium doping is common in such samples as energetic gallium ions are used in ion gun available in FIB system. Therefore, in order to over come this problem in our case, VO_2 nanobeams were firstly transferred to a TEM grid as shown in figure 3.11, then fixed down to the grid using Pt that is deposited using FIB system, prior to Ar ion etching which is preformed using XPS system. In this way, a non-destructive sampling population is achieved for TEM analysis. As for SEM, It was mostly utilized as an imaging toll throughout the course of this project.

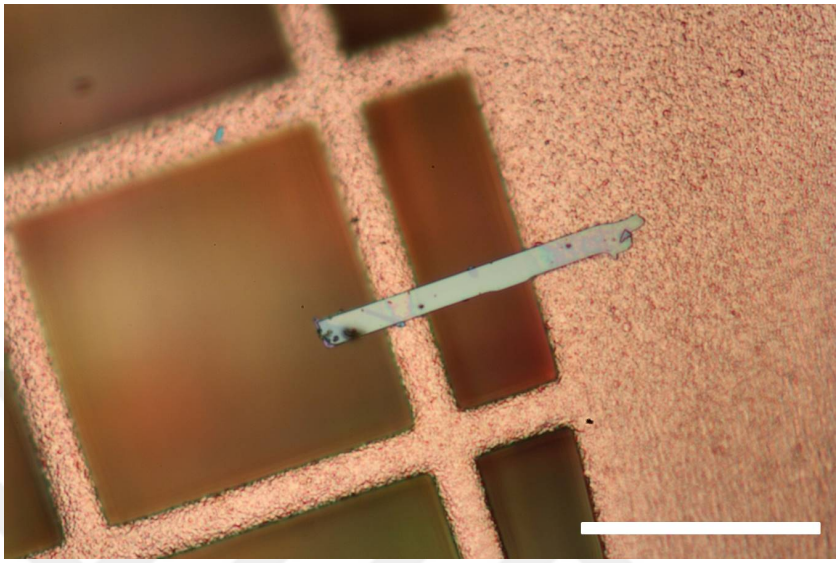


Figure 3.11: *A VO_2 crystal that is transferred on top of TEM grid. Scale bar is 40 μm.*

3.4.4 Probe Station

The probe station used here is a custom made setup which is controlled using various Labview programs for different electrical measurements. Current vs voltage (IV) and resistance vs temperature (RT) are of the measurements that can be performed using this setup. The probe station setup used in the Strongly Correlated Materials Lab (SCMLab) is shown in figure 3.12.

In order to perform RT measurement the sample's stage is made of copper plate which is connected to a Peltier plate to allow temperature control. The device to be measured is connected to a voltage divider that supplies it with only 50 mV out of the 7 V input. Due to the potential difference between the two probes, an electrical current would be drawn through the low potential probe and then amplified via preamplifier and fed back to the program in which the resistance at any given point is extracted thought the following relation:

$$R = \frac{V}{I}$$

As the the potential difference is set to a fixed value and the variation on current is extracted at any given temperature, the change in resistance is calculated and

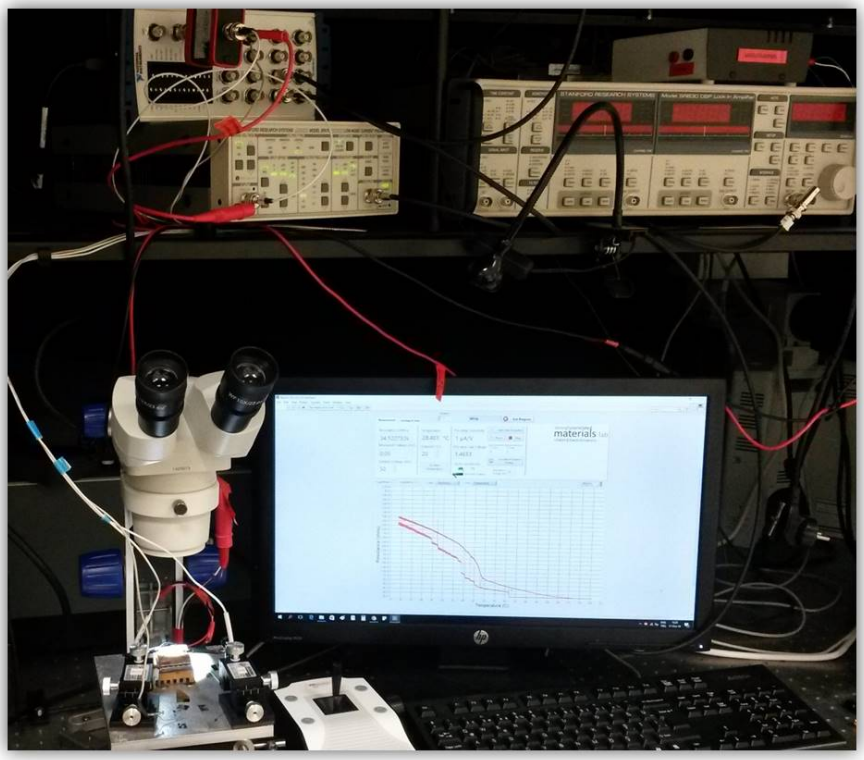


Figure 3.12: The probe station setup used for IV and RT measurements

plotted with respect to temperature simultaneously thought the software. The obtained plot can then be exported for further analysis.

As for Current vs voltage (IV) measurement, the procedures involved are straight forward. The probes are again connected to the metal contacts of the measured device. Electrical potential difference is applied between the two ends of the probes and the resulted current is then amplified and read through a specific Labview program. Any variation on the applied electrical potential difference would result on different values of current running through the device channel. The interval by which the swapping of voltage intended for IV scan is supplied to the program. The program then plots the obtained current values against the know voltage applied at every given moment to finally attain the IV curve of the measured device.

Chapter 4

Results and Discussion

In this thesis, the study of the electrical and structural qualities of vapor-phase grown VO_2 nanocrystals are intended to both assist and simplify the study of exotic phenomena in correlated systems as well as pave the way for possible future use and commercialization of VO_2 based devices. There are many reasons behind avoiding the use of bulk VO_2 in general. The domain structure, impurities and crystal defects present in such forms of materials make it almost impossible to obtain reproducible behavior of such complex structures. Consequently, thin single crystals are required for both investigation and implementation of VO_2 in modern technologies. We are mainly behind investigating the possibility of electrically stimulating the metal-insulator transition in VO_2, for demonstration of a high on/off ratio VO_2 based Mott-FET. Tuning MIT on VO_2 through different types of stimuli such as strain and doping had been reported earlier [70, 77–79]. Achieving this objective however is easier said than done. One of the obstacles in electrically stimulating MIT in VO_2 is due Thomas-Fermi screening, where most of the VO_2 body could remain unaffected by the field imposed by the gate as shown in an attempt reported by Ruzmetov, D. and colleagues [80].

Thomas-Fermi screening length (L_{T-F}) in VO_2 is known to range from 0.7 to 6.0 nm in the insulating phase [81–84]. It is calculated using the formula $L_{T-F} = \sqrt{\epsilon_0 K k_B T / e^2 n_e}$, where ϵ_0 is the dielectric permittivity, k_B is the Boltzmanns

constant, T is the temperature and e is the elementary charge. We used the range of values in the literature for the critical carrier concentration n_e and relative dielectric constant K in the insulating phase of VO_2 [27, 82, 85] in order to obtain the above mentioned L_{T-F} range.

This is a clear indication that crystals within the range mentioned above are needed to be produced in order to have a full-body induced conduction through the crystals. So far, sub-10 nm-thin crystals of VO_2 has been achieved only via epitaxial growth or sputtering methods. Many of the studies in literature in this regards utilize epitaxial films, where some others inferior in number use sputtered films. The lattice mismatch between the film and the substrate in epitaxial films, however, tarnish the quality of such films [22–24]. Further alternations in the properties of these films within the thickness range required are inevitable due to the inter-diffusion between the film and substrate that eventually overpower the original film properties as mentioned earlier [25–28]. Whereas for sputtered films, apart from their polycrystalline nature, they were found to lose conductivity below 45 nm due to film discontinuity [80, 86].

The alternative of using vapor-phase deposited VO_2 seemed attractive as such crystals can be released off substrates, and consequently have only their crystal weigh exerting a stress along their c-axis. The lack of dimensional control in vapor-phase deposition with no crystal dimensions less than 30 nm is circumvented through the introduction of well-established argon-ion milling procedures in order to obtain the required sub-10 mn free-standing VO_2 nanocrystals. The results attained using this method are discussed later in this chapter. Beforehand, the results form investigating the vapor-phase grown VO_2 nanocrystals structural qualities are first discussed, as obtaining high quality VO_2 nanocrystals is a pre-requisite for the rest of the experiments.

4.1 Quality Control of Vapor-Phase Grown VO_2 Nanocrystals

High quality crystal production is one of our first concerns as the final samples' and devices' quality is partially related to that. The crystals undergo many processes and fabrication steps before finally construct two or three-terminal devices. Degradation of the quality of such crystals along the way might be possible. Therefore, we assure the production of high quality as-grown crystals through systematic controlled growth procedures. Knowing that some other stoichiometries of vanadium oxide are possible to produce, such as V_6O_{13} [32] depending on the oxygen partial pressure, growth temperature and some other growth parameters, we control these parameter, as mention in materials and methods chapter, to assure the production of only VO_2 nanocrystals.

It is reported that the stable phase of VO_2 at room temperature (below T_C) M1 shows characteristic Raman peaks at around 190 (A_g), 222 (A_g), 258 (B_g), 306 (B_g), 337 (A_g), 388 (A_g), 496 (A_g), 608 (A_g), and 663 cm^{-1} (A_g) [87]. Figure 4.1 shows a representative Raman spectrum of one of our as-grown VO_2 free-standing nanobeams with similar M1 peaks as indicated above. As these peaks are characteristic, this spectrum is a one clear prove of the high quality of our pristine crystals.

Further confirmation of having the right stoichiometry of vanadium oxide producing VO_2, is the metal-insulator transition taking place around 65 °C. This transition is optically observable, and domains of both insulating and metallic phases can both be seen in unreleased crystals due to substrate-induced non-uniform strains. Upon the transition and due to the clamping of crystals on substrate, alternating compressive and tensile stresses are exerted on crystals. The regions under compressive strain are corresponding to the metallic phase, where the tensile strained regions are in one of the insulating phases due to the stabilization of these phases under tensile strained even for some range above T_C [88]. Phase transition can be seen to take place at 65 °C in our unreleased

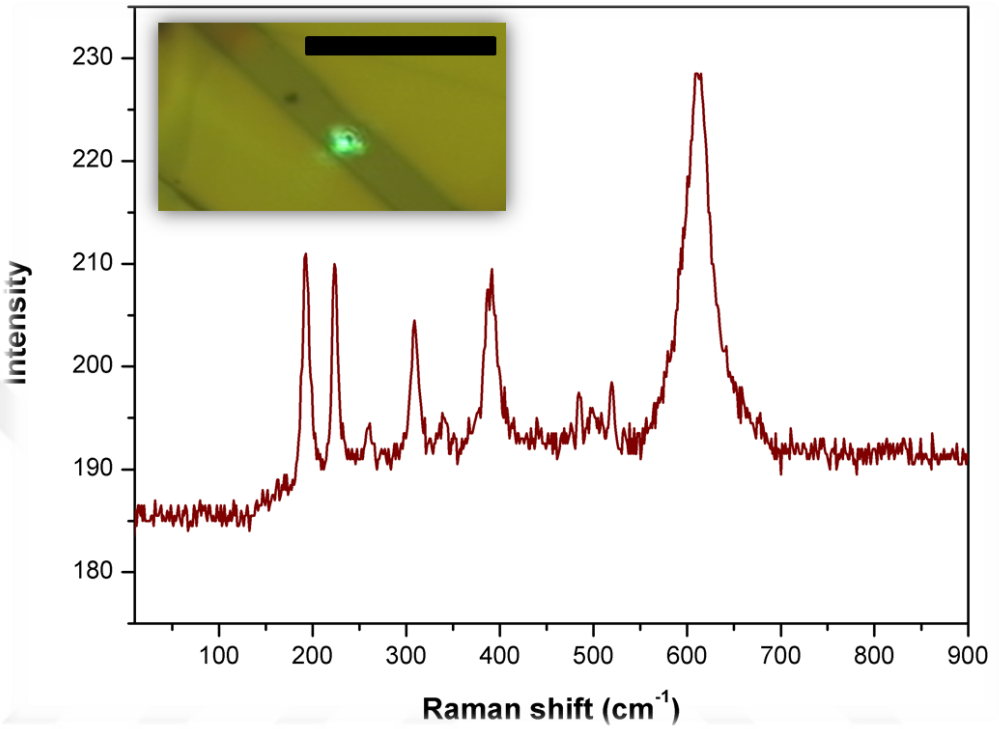


Figure 4.1: *Raman spectrum taken from a pristine VO_2 nanocrystal below T_C. The inset is an optical picture of the region from which this spectrum was obtained. Scale bar is* 10 μm.

crystals in a similar manner as shown if figure 4.2. The dark stripes in the right-side of the figure are the metallic domains that start forming upon passing T_C. Observing the starting of this transition at 65 °C is another clear evidence of our high quality VO_2 nanocrystal.

4.1.1 Etch Rate of Vanadium Dioxide Nanocrystals

To figure out the etch rate of vapor-phase grown VO_2 nanocrystals, many different crystals are to be etched for various durations. The etch rate is then extracted from the thicknesses of these crystal with respect to their etching durations. A pristine surface either on the crystal or on the vicinity of the crystal must be maintained to act as thickness reference. To do so, two main methods are used.

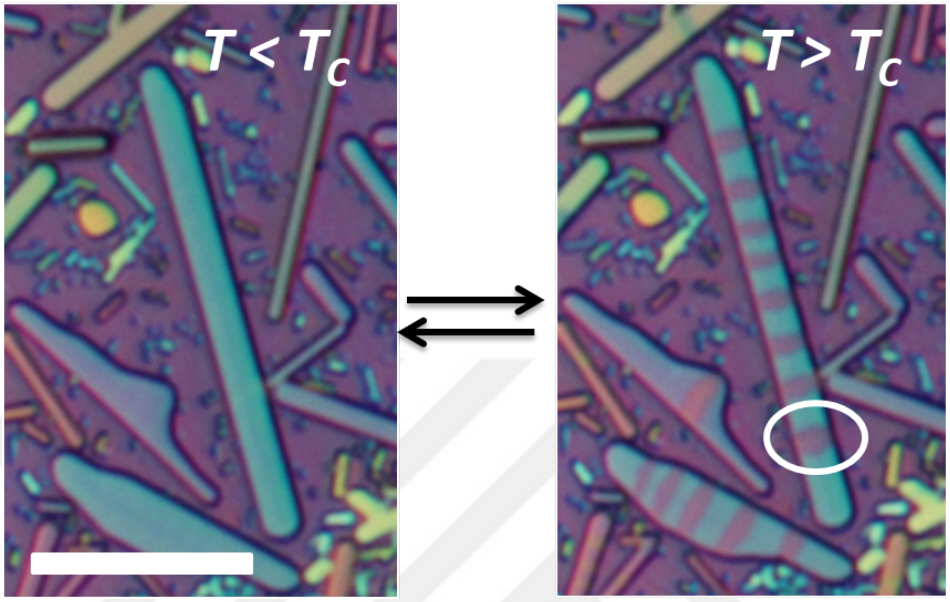


Figure 4.2: *Optical image of MIT on unreleased VO_2 nanocrystals. The left-side picture is taken below T_C, while the right one is taken right above T_C upon heating. Scale bar is* 10 μm.

First of all, photoresist is used in order to cover one part of the crystals in order to protected it during the etching process. We have realized that the durability of the photoresist used is limited to only short durations. Prolonged durations of etching (>10 minutes), using 1 KeV ion gun energy and medium monoatomic flux, tend to peel off the photoresist completely. Therefore, photoresist protection method is used for very limited number of samples on finding the etch rate of vapor-phase grown VO_2 nanocrystals, for the sake of comparison to other approaches. Figure 4.3 illustrates the three steps used to extract the VO_2 nanocrystals etch rate, when photoresist protection is used. This approached is used at 8 different samples, each etched for different duration (<10 minutes) compared to the rest of the samples. The results obtained for AFM of these samples then used along with the samples prepared with the second approach (explained next) in order to reveal the etch rate of vapor-phase grown VO_2 nanocrystals.

The second method utilizes VO_2 nanocrystals either as a mask or as ion-beam blocker. in the first case, a random crystal is transferred above the targeted crystal in order to act as a mask. The transferred crystal covers the part that

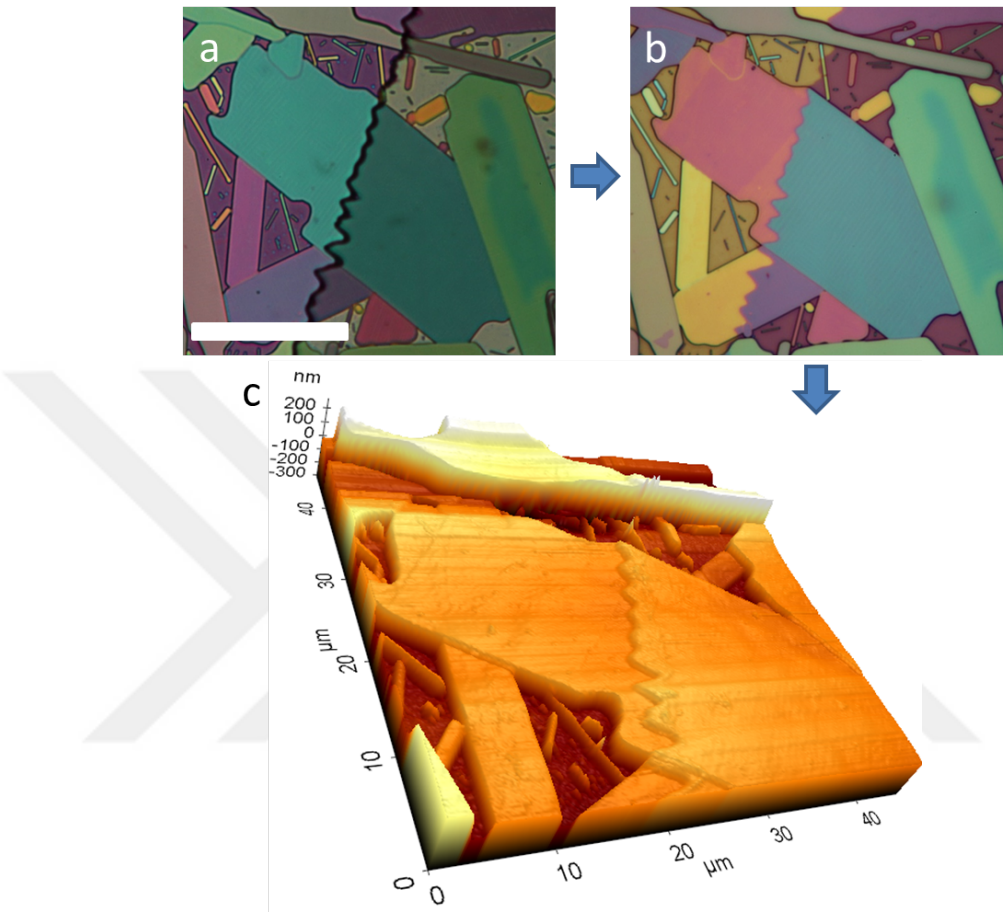


Figure 4.3: *a) Optical image of a VO_2 nanocrystals of which half its surface is protected by a layer of photoresist, prior to etching.Scale bar is* 20 μm. *b) Optical image of the same nanocrystals after 8 minutes of etching and lift-off. c) An AFM 3D topography map of the region etched on b).*

needs to be protected to act as a pristine reference surface after the etching process. Figure 4.4 is a representation of this method. On the other hand, the targeted crystal acts as a blocker of the ion-beam, and consequently protects a narrow strip of pristine SiO_2 surface due to the fact that the Ar-ion gun is targeted to the sample surface at an angle of 32 ° as explained in the materials and methods section.

The AFM measurements collected from samples etched using the methods above, for various durations are used to obtain the etch rate of vapor-phase grown VO_2 nanocrystals. A representative AFM measurement is given in figure 4.5. It turns out that the average etch rate of such crystals is 3.3 nm/min with 0.3

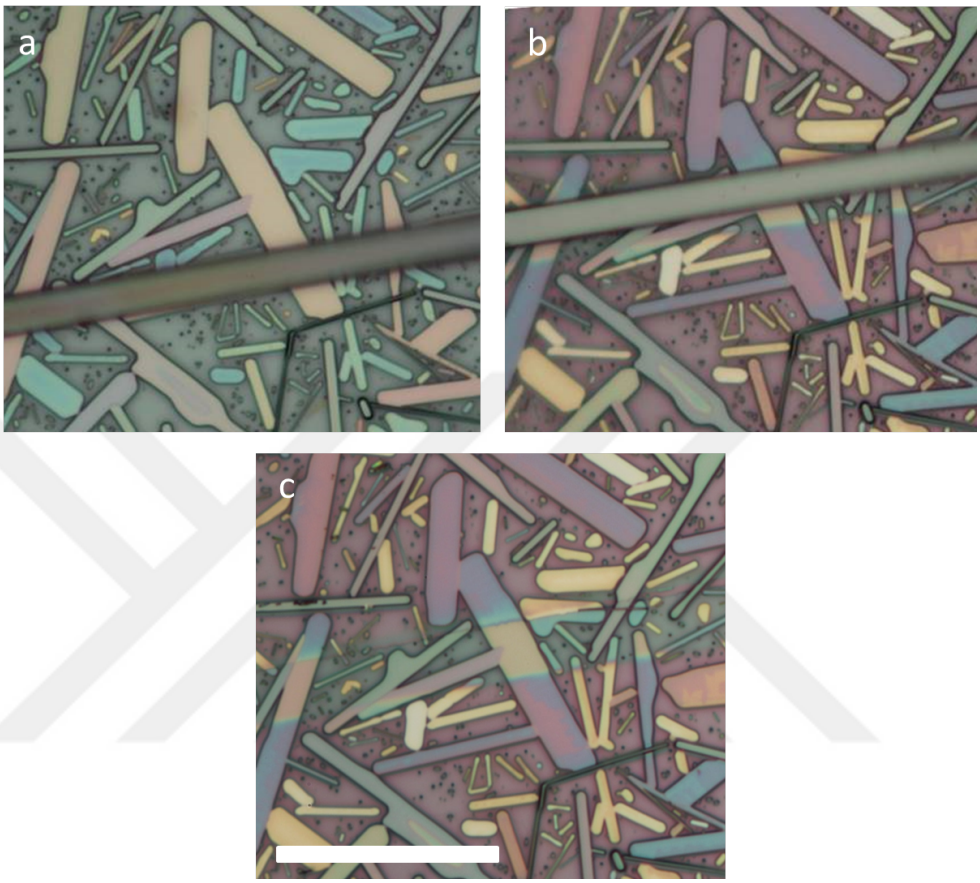


Figure 4.4: *a) Optical image of a VO_2 nanocrystals used to mask another targeted VO_2 nanocrystals prior to etching. b) Optical image of the same nanocrystals after etching. Note that the masking crystal has slid upward prior to etching. c) Optical image of the same nanocrystals after etching and removal of the masking crystal. Scale bar is* 30 μm.

nm/min error. Table 4.1 provides the average etch rates and the methods used for masking each sample used in this part of the study.

4.2 Free-Standing VO_2 Nanocrystals

In this study, the production of sub-10 nm VO_2 single crystals is required in order to pave the way to further study the effect of thickness on MIT, the quantum confinement effect in such systems, and to understand other similar strongly correlated materials along with the utilization of VO_2 nanocrystals on novel electrical

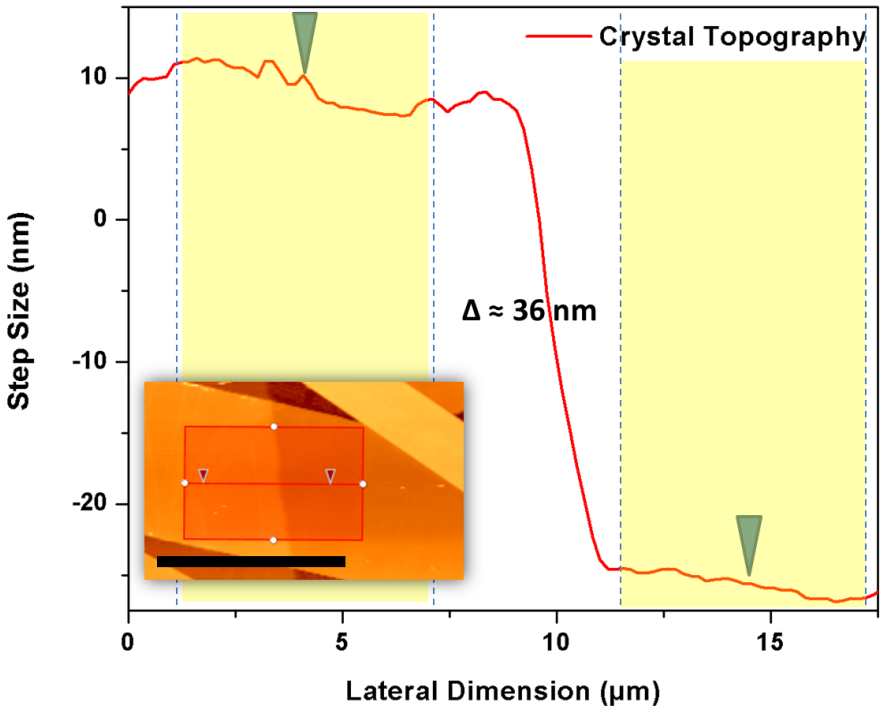


Figure 4.5: *A representative AFM area profile showing the difference in thickness between the pristine and the 10 min. etched part of a crystal. The protection method used here is photoresist protection. The 2D topography map in the inset shows the region from which the area profile in the main figure is taken. Scale bar in the inset is* 20 μm.

and ultra-fast optical switching. As mentioned before, epitaxial films are not the right choice due to many complications such as substrate induced non-uniform strains. However, even single crystals grown using vapor-phase deposition have non-uniform local strains due to substrate adherence [88] as can be clearly inferred from figure 4.2. Being aware of this fact, all of the experiments presented in this work form this point on are conducted on free-standing crystals that are released from the growth substrate (SiO_2/Si) then transferred above exfoliated hexagonal-Boron Nitride (h-BN) flakes in order to get rid of such non-uniform strains. Unlike non-uniformly strained VO_2 crystals, where metallic stripes form in the vicinity of the critical temperature, the crystals on h-BN display an abrupt phase transition, indicating that they are only uniformly strained along their c-axes. Comparison of the abrupt transition taking place on VO_2 nanocrystals on top of h-BN flakes and the gradual transition taking place on as-grown VO_2

Table 4.1: Etch rate of vapor-phase grown VO_2 nanocrystals

Sample	Masking Method	Average Etch Rate (nm/min)
Sample 1	Photoresist	3.7
Sample 2	Photoresist	3.7
Sample 3	Indium Shadowed Crystal	3.0
Sample 4	Crystal Masked	3.2
Sample 5	Crystal Masked	3.2
Sample 6	Crystal Shadowed	3.3
Sample 7	Crystal Shadowed	3.4
Sample 8	Crystal Shadowed	3.2
	Average of all samples	3.3

nanocrystals on SiO_2/Si substrate is presented in figure 4.6.

4.3 Crystal Damages Due to Ion-Milling

To check for possible damages on crystals due to Ar-ion milling, both physical and chemical alterations on crystals are investigated. Below is the separate detailed discussion of both possibilities.

4.3.1 Physical Damages of Crystals

The ion-beam energy used to etched crystals in this work is 1 KeV, as mentioned earlier. It was reported that, even at Ar-ion beam energies as low as 200 eV, surface damage is inevitable, yet it can be slightly reduced and restricted to a layer of few nanometers [89, 90]. To investigate the damage introduced to our crystals after etching for various durations, High Resolution Transmission Electron Microscope (HR-TEM) micrographs are taken from the cross-sections of these crystals.

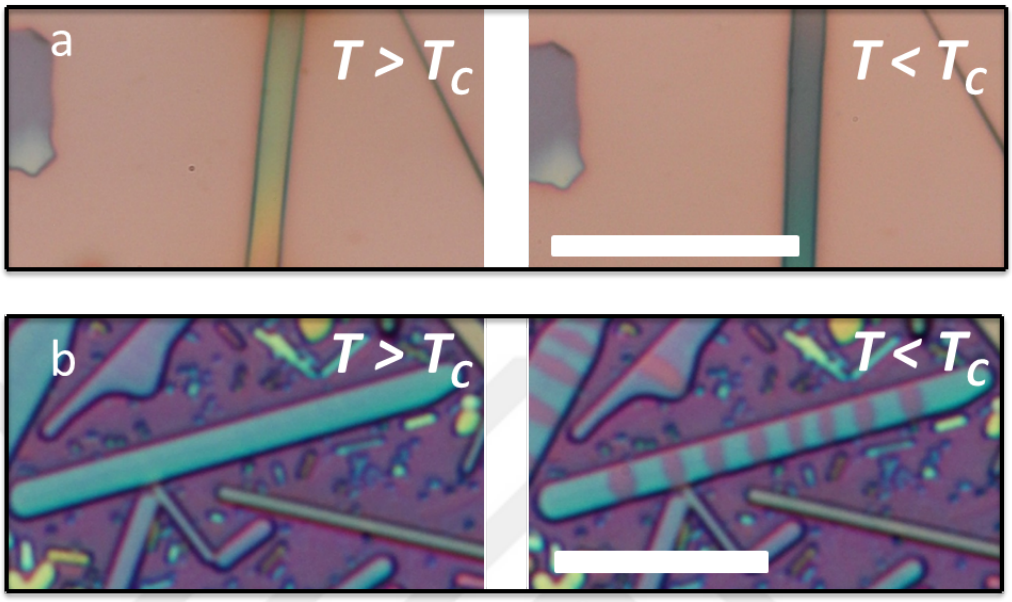


Figure 4.6: *a) Shows the abrupt transition on VO_2 nanocrystals on top of h-BN flakes upon heating above T_C. The scale bar is* 20 μm. *b) Shows the domain structure emerging upon transition on as-grown VO_2 nanocrystals on SiO_2/Si substrate due to substrate induced non-uniform strains. The scale bar is* 10 μm.

Figure 4.7 shows the HR-TEM cross-sections of three different crystals etched for 10, 28 and 40 minutes respectively, revealing the amount of damage introduced to the upper surface of the crystals. The HR-TEM micrographs show that the damaged surface is to be 4.5 nm and a bit more than 5.5 nm respectively. A Selected Area Electron Diffraction (SAED) pattern at d) taken from area shown at figure 4.7 b) shows that the body of the crystal is still single crystal.

In order to have further confirmation to the amount of damage caused by the etching process, we used Stopping and Range of Ions in Matter (SRIM) software [91] to simulate the depth of the surface damage. All parameters used in the etching process including the angle of ion gun are utilized in the simulation. Figure 4.8 demonstrates the ion penetration depth with respect to the number of ions that collide with the surface. It is clear from the figure that slight increase in the penetration depth is dependent on the logarithmic increase in the number of ions. Moreover, the final total surface damage turned out to be highly dependent on both the ion-beam energy and the rate at which this newly introduced surface

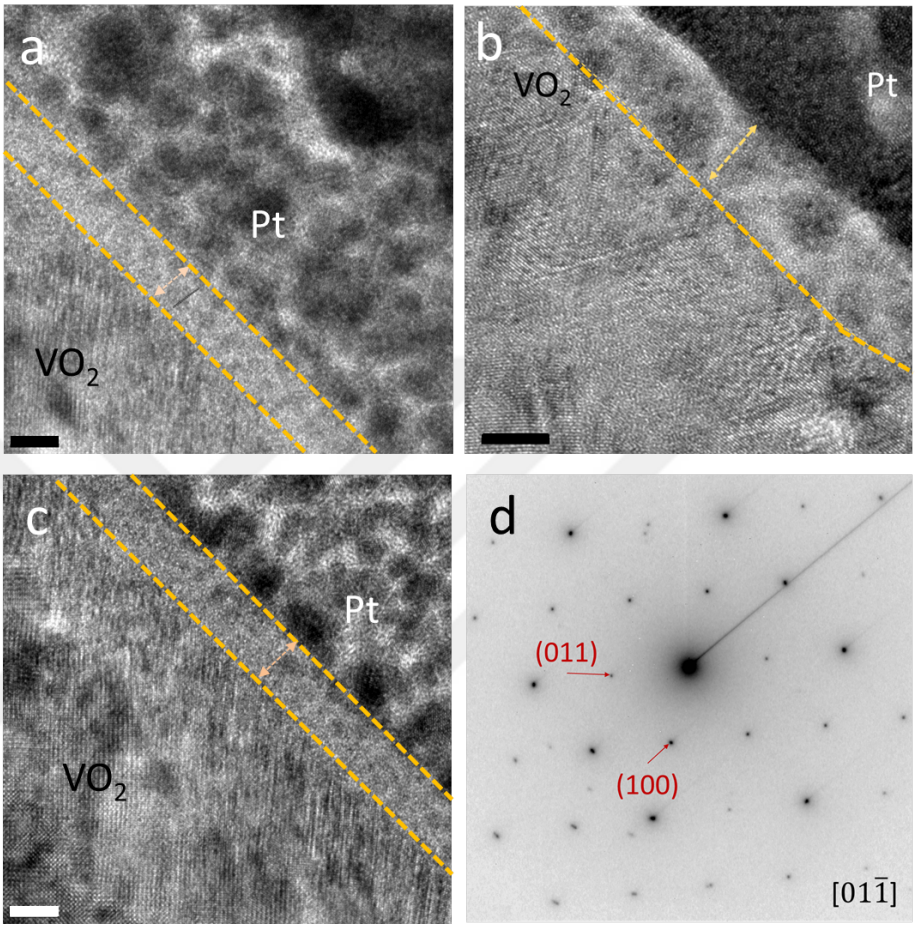


Figure 4.7: *HR-TEM images showing the surface damage due to Ar-ion bombardment of three different VO_2 nanocrystals etched for a) 10 minutes, b) 28 minutes and c) 40 minutes. The scale bar in each image corresponds to 5 nm. d) A* $[00\bar{1}]$ *zone axis indexed Selected Area Electron Diffraction pattern taken from the bulk of the crystal at b).*

layer is etched. The ion-beam energy used in our experiments leaves a small amount of damaged on the surface of the crystal. This confirm the observed damage on the HR-TEM micrographs from figure 4.7.

To further confirm the quality of the bulk of the etched crystals, we performed room temperature micro-Raman spectroscopy (532 nm laser excitation) on milled nanocrystals. It is important to note that as our crystals are on h-BN, they are in a single phase at any given temperature. Therefore, the Raman signal obtained belongs to a single phase. An initially 170 nm thick VO_2 nanocrystal is selected

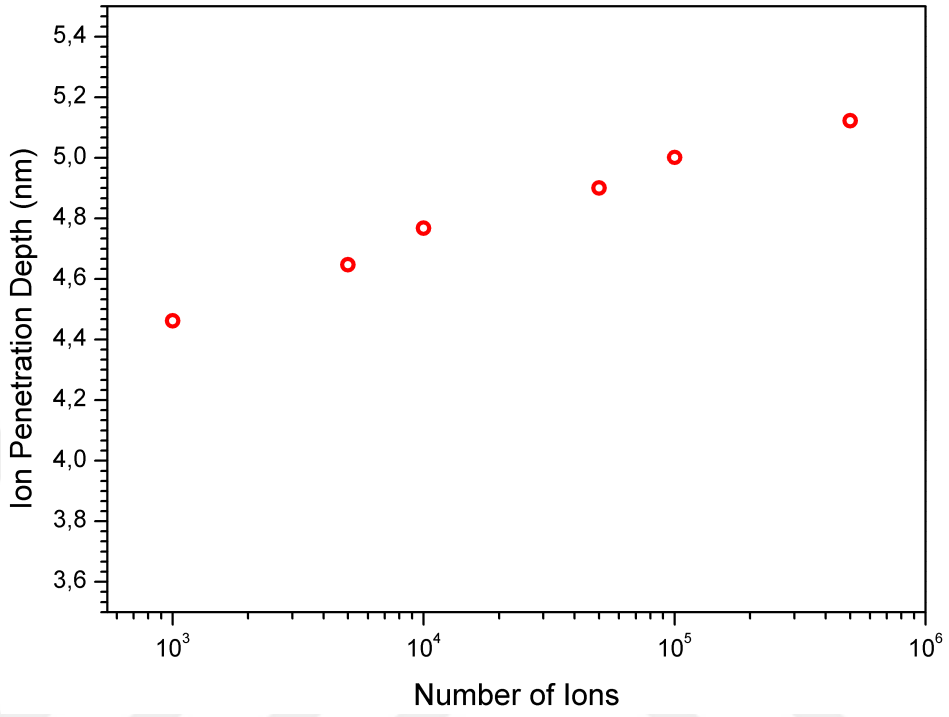


Figure 4.8: *SRIM simulation results show the ion penetration depth dependence on number of ions and consequent crystal damage.*

to do a serious of Raman measurements. The crystal is etched down to about 4 mn (excluding the damaged surface layer) in several etching steps. After each etching step, Raman spectra are taken from the crystal. These Raman spectra are given in figure 4.9. This experiment is meant to reveal the effect of gradual thickness variation on MIT, as explained later, along with the quality check of the milled crystal. The 520 cm^{-1} silicon peak becomes more pronounced as the crystal gets thinner as expected. The M1 associated peaks are marked with dark dashed lines [92]. It can be clearly seen from the long dashed lines indicating ω_{V1} (194 cm^{-1}), ω_{V2} (223 cm^{-1}) and 613 cm^{-1} that no shift on the spectra is taking place as the crystal gets thinner. Nevertheless, the ratio of intensities of ω_{V1} (194 cm^{-1}) and ω_{V2} (223 cm^{-1}) ($I_{\omega V1}/I_{\omega V2}$) changes. This change can be attributed to polarization [93]. A 90 ° rotation in the sample direction during measurement would shift the intensity of these peaks. Therefore, $I_{\omega V1}/I_{\omega V2}$ vary significantly due to change in the polarization of the excitation light [93]. Relaying on both the results obtained from TEM and Raman measurements, we can conclude that the bulk of the crystal is not affected by Ar-ion milling.

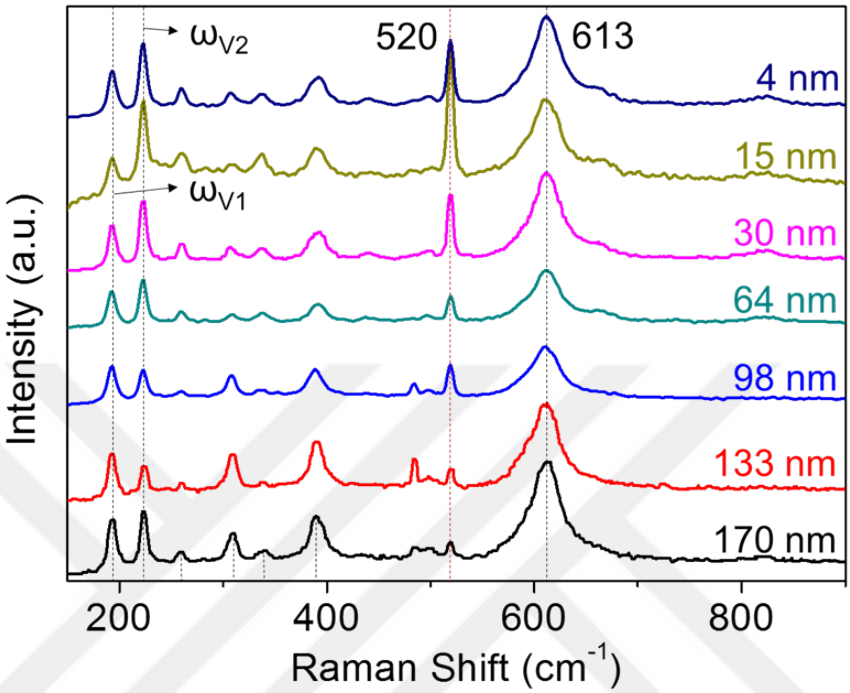


Figure 4.9: *Raman spectra taken from a VO_2 nanocrystal at various thicknesses.*

4.3.2 Chemical Alteration of Crystals

Assuring the chemical integrity of crystals after milling is also an essential step. Both changes in the chemical state of the vanadium and oxygen atoms on the surface of VO_2 nanocrystals, and the ion implantation on the surface are suspected due to the exposure of crystals to high energy Ar-ion bombardment. To investigate such possibilities, XPS analyses are carried out. To have a solid ground for comparison, the changes on vanadium 2p peak and oxygen 1s peak as well as the occurrence and/or the emergence of 2p peak of argon are investigated for three different scenarios. In the first case, a pristine VO_2 nanocrystals on h-BN on SiO_2 is surveyed for all the peaks above. In the second cause, the same sample is etched directly after the first XPS measurement, without removing the sample out of the XPS chamber, and then the possible changes on these peaks are surveyed again. In the last case, the same sample is removed out of the XPS chamber, kept under ambient conditions for three days, and then the same surveys are carried out one more time. The result of surveying vanadium 2p peaks and oxygen 1s peaks show

a distinct difference between these three cases as can be seen form the lift panel in figure 4.10. The two peaks belonging to V $2p_{3/2}$ form the XPS spectrum taken

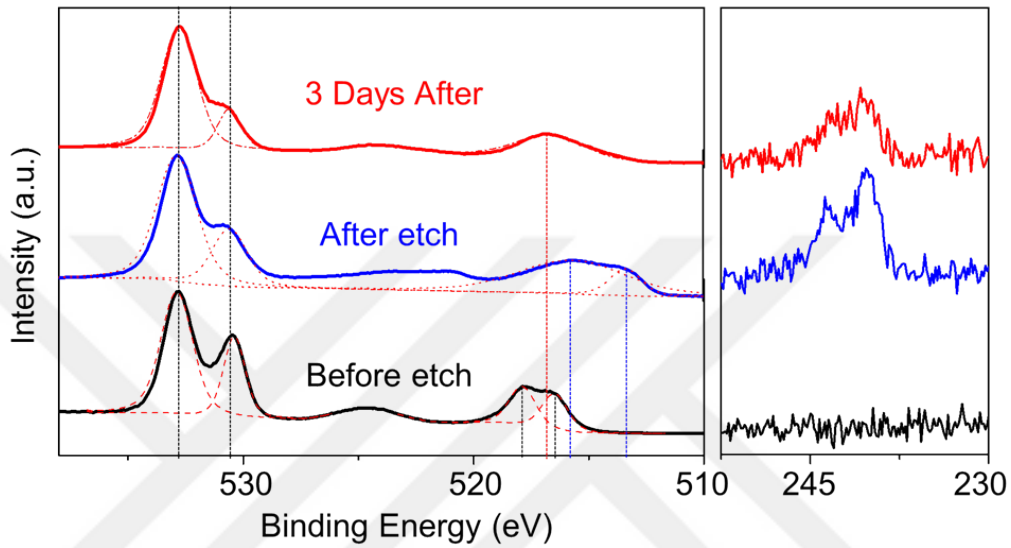


Figure 4.10: *XPS spectra around vanadium, oxygen (left panel), and argon (right panel) binding energies before etching, immediately after etching, and three days after etching.*

before etching are coming from V_2O_5 and V_6O_{13} [94], which indicate that the nanocrystal is oxidized at its surface. This is an expected thing as the used sample is grown and kept under ambient conditions few days before the analysis. The after etching (for 28 minutes) spectrum on the other hand shows the evolving of V $2p_{3/2}$ peaks into different peaks with binding energies that correspond to those of VO_2 and VO. The decrease in intensity of the O 1s (O-V) peak is an indication of a loss of some oxygen from the crystal. A single V $2p_{3/2}$ peak remains after leaving the etched sample under ambient condition for three days, which can be attributed to V_6O_{13}. The consistency of the results from these measurements with the TEM images assures that there is an amorphous surface layer poor in oxygen produced as a result of ion milling.

As for investigating Ar-ion entrapment, XPS surveying for 2p argon peak is performed at the same sample and the same time of the three cases mentioned above, as indicated in the right panel of figure 4.10. No signs of any peaks associated with argon 2p from the XPS survey taken before etching the sample.

However, after 28 minutes of etching, argon 2p peaks are clearly observed. On the other hand, the 2p peaks diminished after leaving the sample under ambient conditions for three days, implying that some of the entrapped argon has escaped. It should be noted here that, XPS collect argon related data not only from the VO_2 nanocrystal surface, but also from the surrounding SiO_2 surface as well due to large spot size of the X-ray beam. In order to confirm this, we performed an XPS analysis on milled bare SiO_2 surface, looking for 2p argon peaks. When compered the findings from both milled VO_2 on SiO_2/Si substrate to milled bare SiO_2/Si substrate, we found that argon entrapment is exactly similar in both cases as shown in figure 4.11. Consequently, we concluded that argon entrapment does not impose any threat on the novel properties of milled VO_2 nanocrystals.

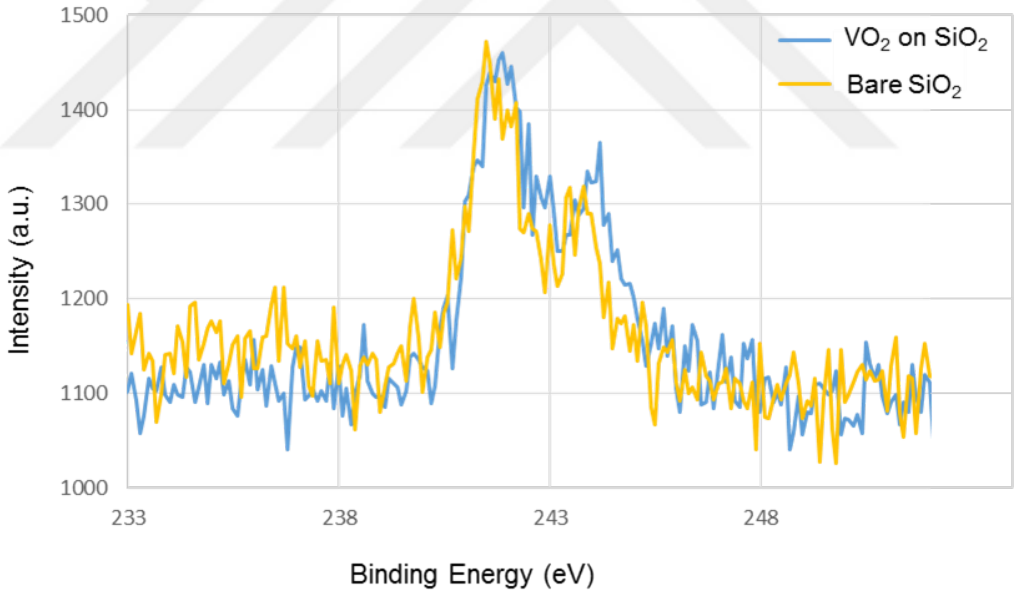


Figure 4.11: *Comparison of argon 2p XPS spectra taken from similar duration etched VO_2 nanocrystal on SiO_2/Si substrate and bare SiO_2/Si substrate. The striking similarity between the two samples' argon 2p peak is a clear evidence that most of the Ar ions are trapped on SiO_2 surface.*

4.4 Effect of Thinning and Two-Terminal Device's Structure on MIT

In order to perform electrical resistance vs. temperature measurements on vapor-phase grown VO_2 nanocrystals as they get thinner through Ar-ion milling, two-terminal devices are constructed from such VO_2 nanocrystals on h-BN flakes. Indium contacts are placed on opposite edges of the selected transferred VO_2 nanocrystal as explained in section 3.3.4. Then AFM measurement is conducted in order to determine the initial crystal thickness. It should be noted here that, crystal thickness after milling is determined from both the etch rate and the etch duration. After several etch cycles, AFM measurements are repeated in order to minimize the propagation of error in determining the crystal thickness.

As indium contacts are placed above T_C and consequently pin down the crystal in its rutile phase, a uniform stress along the crystals c-axis emanates upon cooling below T_C as larger lattice dimensions are now stabilized in the M1 phase [95]. Therefore, uni-axial compressive stress near the transition temperature (P_C) increases as the crystal get thinner, although the compressive force (F) acting on the crystal by the contacts stay constant. As a result, T_C decreases relative to the crystal thickness. The inset in figure 4.12 depicts such an effect. The term $\eta = \frac{F}{EA}$ expresses the compressive strain acting on the crystal, where E and A are Young's modulus and the cross-section area of the crystal respectively. It should be clarified here that such strain might be relieved through buckling of crystal below certain thickness depending on other relative dimensions of crystal. In order to verify the decrease on T_C due to thickness reduction, calculation of the expected T_C at given crystal thicknesses are performed using the fact that $\frac{\partial P_C}{\partial T_C} = 71MPa\ ^\circ\mathrm{C}^{-1}$ at the M1-R phase boundary [65], and then compared to measured critical temperatures T_C (form RT measurements shown in the next section) of the same crystal as shown in figure 4.12. Blue circles and red dotes in the figure indicate calculated and measured T_C respectively.

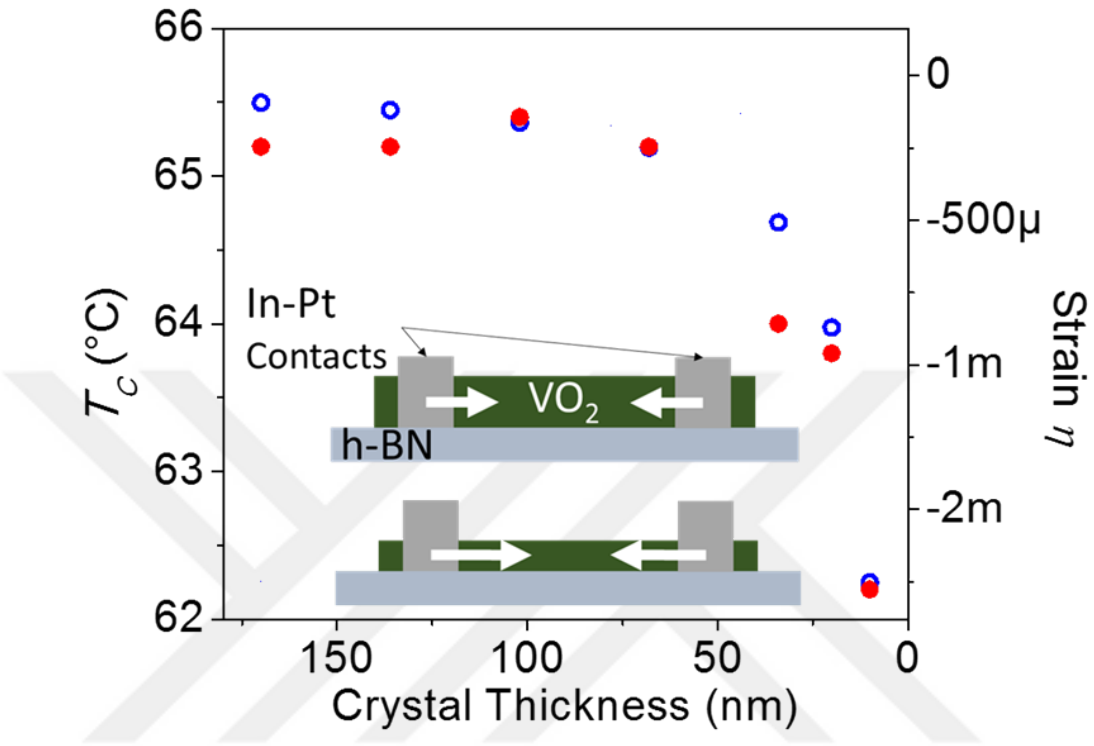


Figure 4.12: *T_C dependence on crystal thickness of a two-terminal VO_2 nanocrystal on h-BN device (with indium as contacts). Compressive strain acting on crystal due to contacts placement increase gradually with the decrease in crystal thickness. This results in a relative decrease on T_C . Calculated T_C (Blue circles) are in great agreement with measured T_C (red dotes).*

4.5 Crystal Milling-Induced Changes on Electrical Resistance vs. Temperature (RT) Measurements

The device above and other similar devices are used in this part of the study. Each device is etched to below 10 nm in several etching steps. After each etching period, the RT measurements are repeated for each device. The initial dimensions such as width (ω) and length (l) of each crystal are measured prior to etching in order to have the ability to extract the relative resistivity (ρ) of each crystal at any given thickness from the RT measurements.

Taking into consideration a single device as an example, it is noted that the overall resistance in the insulating phase of the crystal decreases drastically after the first etch period, and keep in decreasing at a much slower rate after each consecutive etch period. This effect can be seen clearly in the representative measurements in figure 4.13. An obvious explanation of such an effect is preliminarily extracted from HR-TEM images 4.7. The formation of a conductive amorphous film of vanadium oxides at the surface of VO_2 nanocrystals as a result of the Ar-ion bombardment can cause such a decrease in resistivity. The inset carton in figure 4.13 is an illustration of the formation of the amorphous film after milling. This amorphous surface film consists of VO_2, VO and probably other Magneli phases of vanadium oxides that are not resolved by the XPS analysis. For a crystal that is etched down to total thickness of 10 nm, a pristine 4

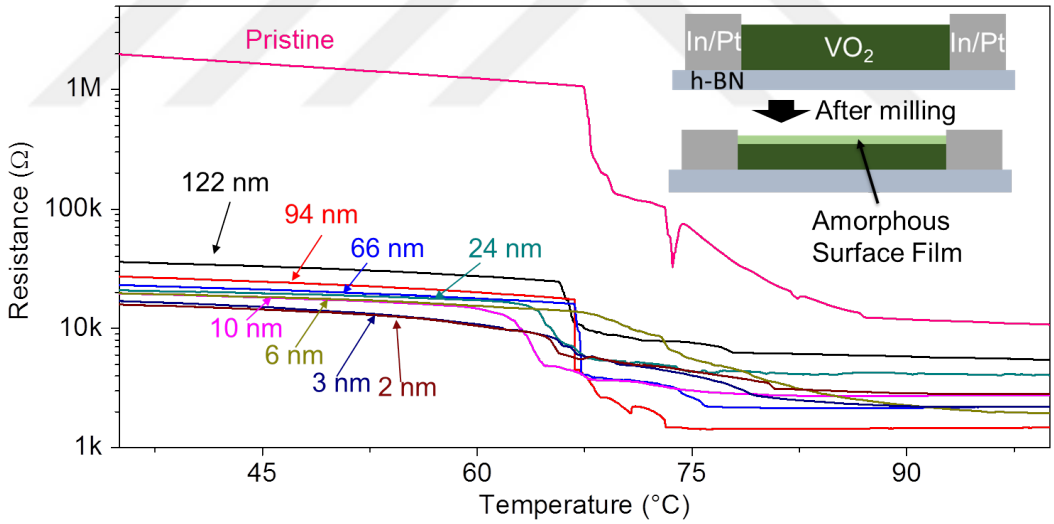


Figure 4.13: *RT measurements taken from a specific crystal that is etched for different interrupted duration down to 2 nm. The The indicated thicknesses on the graph are excluding the amorphous surface layer thickness in each case. The inset is an illustration of the formation of the amorphous surface layer due to ion milling.*

nm of crystal must still be laying underneath the amorphous film according to both the SRIM simulation results and the TEM images. To confirm this, a VO_2 nanocrystal-based two-terminal device that is etch down to around 10 nm in total has proven to undergo MIT as expected from a VO_2 nanocrystal that is uniformly strained along its rutile c-axis. Optical images available in figure 4.14 a) shows

the abrupt transition that takes place on 4 nm VO_2 nanocrystal (excluding the amorphous surface film). The rainbow colored region on the crystal at the left side of the image is an example of the buckling by which thin long crystals tend to relieve the contact induced strain as explained earlier. Figure 4.14 b) is a SEM micrograph that shows the buckled region at close proximity. The next section is dedicated to further verifying the formation of the conductive amorphous surface film through its contribution to the resistivity the crystal.

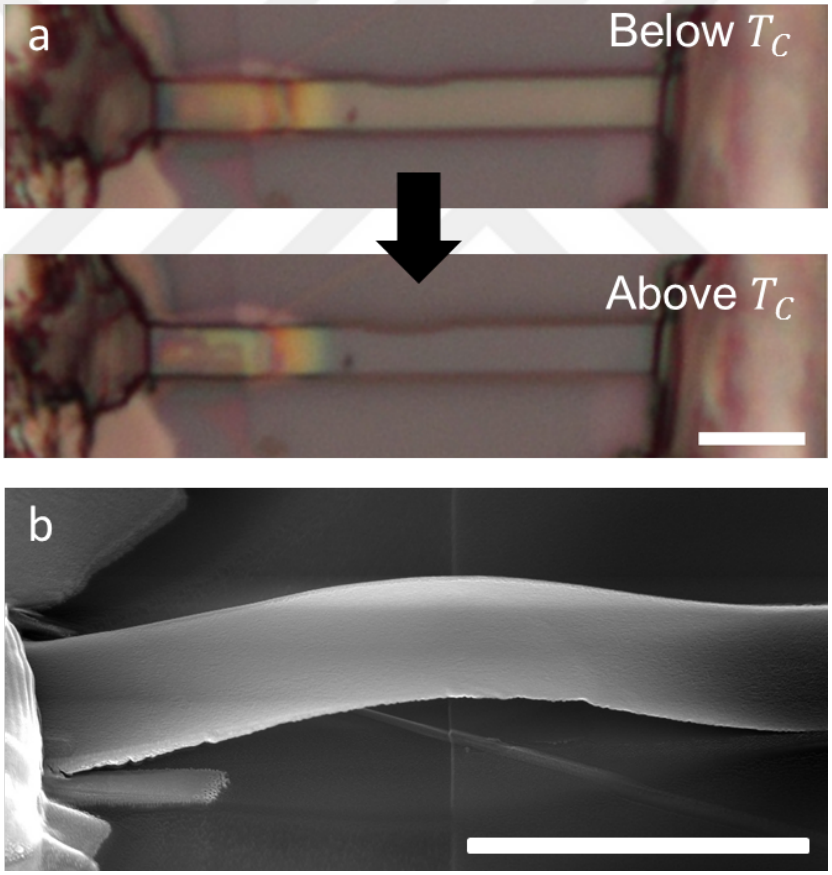


Figure 4.14: *Optical microscope images of a crystal with a total thickness of 10 nm a) below and above the transition temperature. Scale bar is* 10 μm. *The rainbow of colors that appear at the left side of the crystal is due to the buckling of the crystal around that point as shown in the SEM micrograph in b). Scale bar is* 4 μm

4.6 Resistivity of The Amorphous Surface Film

To calculate the resistivity of the amorphous surface film of a given crystal we relay on the RT measurements of the pristine crystal along with its constant dimensions. The expected resistance (R^{exp}_{VO2}) due to decrease in thickness of the crystal is then calculated assuming that uniformity of the remaining crystal. Then the resistance of the amorphous surface film R_{surf} can be extracted out from both the measured resistance (R_{total}) at that specific thickness and R^{exp}_{VO2} through the following relation: $\frac{1}{R_{surf}} = \frac{1}{R_{total}} - \frac{1}{R^{exp}_{VO2}}$, where R_{surf} can be calculated from the known width, length and thickness (t_{surf}) of the surface film. As mentioned earlier, the pristine crystal thickness is measured using AFM, where the remaining crystal thicknesses after the consecutive etch durations are determined from the etch rate and the etch duration. It should be noted that, due to an expected difference in the Ar-ion penetration depths between the pristine crystal surface and the amorphous surface film, thickness of the amorphous film may slightly increase with the increase in milling duration. However, this increase happens at very slow rates as the amorphous surface film gets etched as well. Depending on several TEM results taken from crystals that have been etched for various durations (as in figure 4.7) along with the SRIM simulations, we estimate that t_{surf} ranges from 3 nm to 5.6 nm. Based on that, the resistivity of the amorphous surface film (ρ_{surf}) at 35 °C is calculated to be 1.3 mΩ.cm as shown in figure 4.15. The resistivity values found in literature for VO and oxygen-poor Magneli phases [96, 97] are in consistence with this calculated value.

4.7 Removal of The Amorphous Surface Film

As it is clearly illustrated in section 4.5, milling process leaves behind crystals with amorphous surface films that interfere with the quality and proprieties of the pristine crystals underneath. In order to retrieve back the original proprieties of the milled crystals, removal of the process-introduced conductive surface film is a prerequisite. The micrograph in figure 4.16 shows the damage introduced to

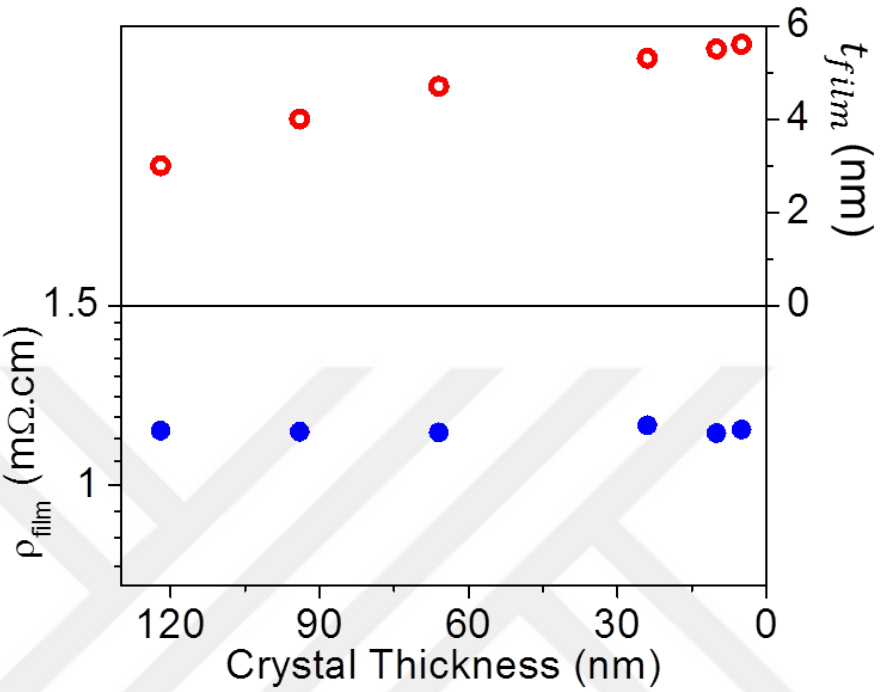


Figure 4.15: *The thickness of the amorphous surface film, t_{surf} (inferred from TEM measurements), with respect to the crystal thickness is shown in the upper panel. t_{surf} increases as the crystal is milled further. The lower panel shows how the resistivity of the amorphous surface film, ρ_{surf}, changes as the crystal is milled. ρ_{surf} is calculated from the measured resistance, crystal length and width, and t_{surf}.*

the first few nanometers of the crystal surface as a result of Ar-ion bombardment. It turned out that short duration (≤ 1 minute) of 37% hydrochloric acid ($HCl_{(aq)}$) treatment would leave behind a pristine crystal surface due to its capability of removing the amorphous surface film. Figure 4.16 shows the clear difference on the surface of the HCl treated dry-etched crystal when compared to the same crystal prior to the treatment.

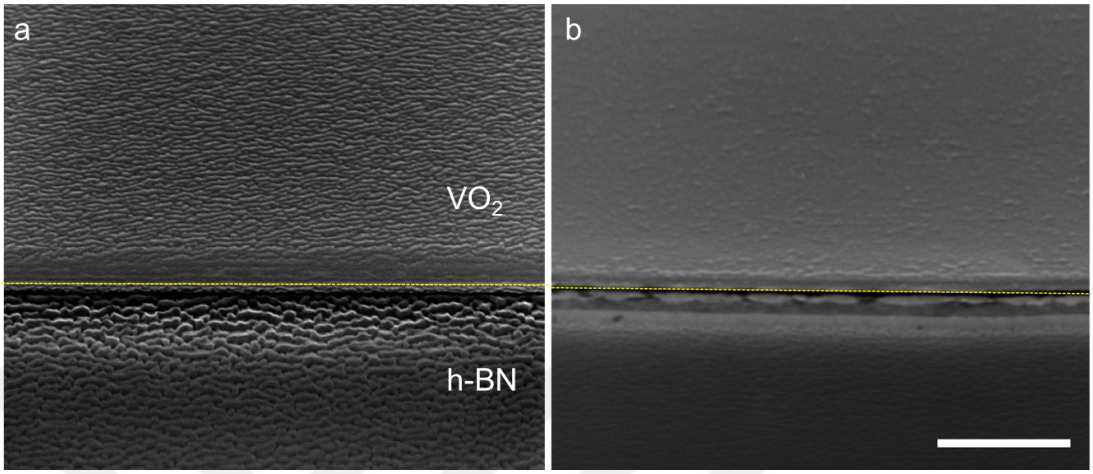


Figure 4.16: *a) SEM micrograph of a VO_2 crystal on h-BN on SiO_2 shows the surface after 10 min of etching and b) the same region after the HCl treatment. Yellow dashed line is placed to aid in distinction between VO_2 and h-BN. Scale bar is 500 nm*

4.8 Electrical Quality of The Produced Thinned VO_2 Noncrystals

As mentioned earlier, the main concern is to get reproducible pristine thinned VO_2 nanocrysals. In the previous section, the complete removal of the etching-introduced conductive surface film is illustrated. Now it is important to check whether or not the quality of pristine VO_2 nanocrysals are retrieved as well with the removal of the surface film. In order to do so, the resistance vs. temperature is measured in a selected pristine VO_2 nanocrysal after it is transferred on h-BN and constructed in a two-terminal device configuration. This crystal is then etched for 10 minutes and the resistance vs. temperature measurement is repeated again. The crystal is then dipped in $HCl_{(aq)}$ for 1 minute in order to get rid of the amorphous surface as shown in the previous section. Another resistance vs. temperature measurement is taken after the $HCl_{(aq)}$ treatment.

The relative resistance of the pristine crystal is taken as the reference for comparison. The three measurements are shown in figure 4.17. It is clear from the figure that there is a drastic decrease in the initial resistance of the etched crystal

(red line) with respect to the pristine measurement (black line) which is due to the formation of the conductive surface film. However, the measurement taken from the etched crystal after $HCl_{(aq)}$ treatment (blue line) show that the resistance of the the M1 phase is recovered due the removal of the conductive surface layer. The higher contrast in resistance that can be seen in the after $HCl_{(aq)}$ measurement when compared to the measurement taken from the pristine crystal is actually due to difference in the contact resistance. The contacts that are placed on the pristine crystal are having higher contact resistance due to surface oxidation on the VO_2 nanocrysal after growth. However, the $HCl_{(aq)}$ treatment washes away both the indium contacts and oxide or amorphous surfaces on the crystal. This result in a fresh VO_2 crystal surface. Now indium contacts are replaced on the same place of the previous contacts directly after the $HCl_{(aq)}$ treatment. This result in a lower contact resistance which is clearly observed in the metallic phase of the treated crystal.

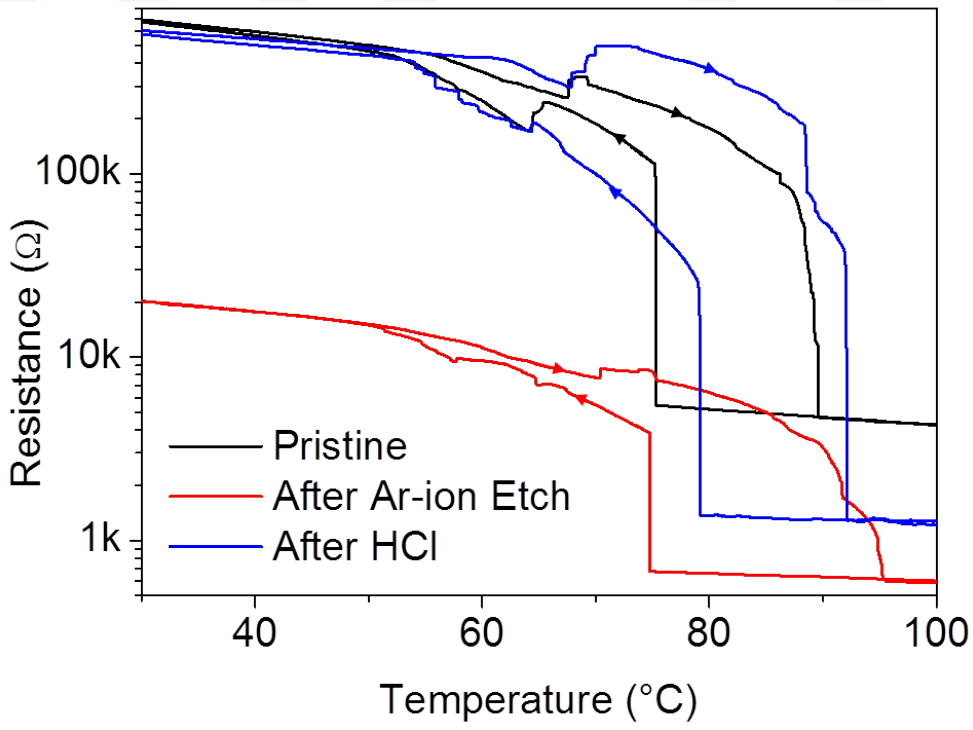


Figure 4.17: *RT measurements taken from a crystal in its pristine form (black line), after being etched for 10 minutes (red line) and after its is treated with $HCl_{(aq)}$ following the etching process (blue line).*

4.9 Electrical Measurements of VO_2 Based Three-Terminal Devices

In this section, preliminary results of electrical measurements that are taken from three-terminal devices are discussed. this part of the work still needs to be elaborated with further device's configurations and measurements. The results that are discussed here are intended to pave the way towards the demonstration of fully functional Mott-Field Effect Transistors. Manly this study was actually planned to conclude the possibility of producing a novel ultrafast Mott-FET, however, due to many obstacles that are faces specifically in the device fabrication, a final conclusion is not reached in this regards. Yet, the results we have reported so far [98], along with the results discussed in this section have already solved many of the problems that previously encountered in the way of realizing VO_2 Based Mott-FET.

The resistance of the channel of the device in figure 4.18 is extracted from many IV measurements where the potential difference between the source and drain is swapped between -100 mV to 100 mV while a specific constant gate voltage between 0 V to 14 V is applied each time. The extracted resistances are then plotted versus gate voltages in order to analyze the trend by which the resistance of the channel is changing with respect to the applied gate potential as in figure 4.19. As it is clear from the plot, the resistance of the channel is decreasing with the increasing of gate voltage . An indication of channel modulation through the control of the gate potential. The small changed in the order of magnitude of the resistance is due to the small channel area that the gate contact cover and control due to the way it is fabricated. The behaviour observed in figure 4.19, however, was not reproducible in this device as per another set of measurements taken few days after the first measurements as presented in the plot in figure 4.20.

Another device is then fabricated for further analysis. The device is shown in figure 4.21. This device is fabricated mainly to analyze the breakdown voltage of

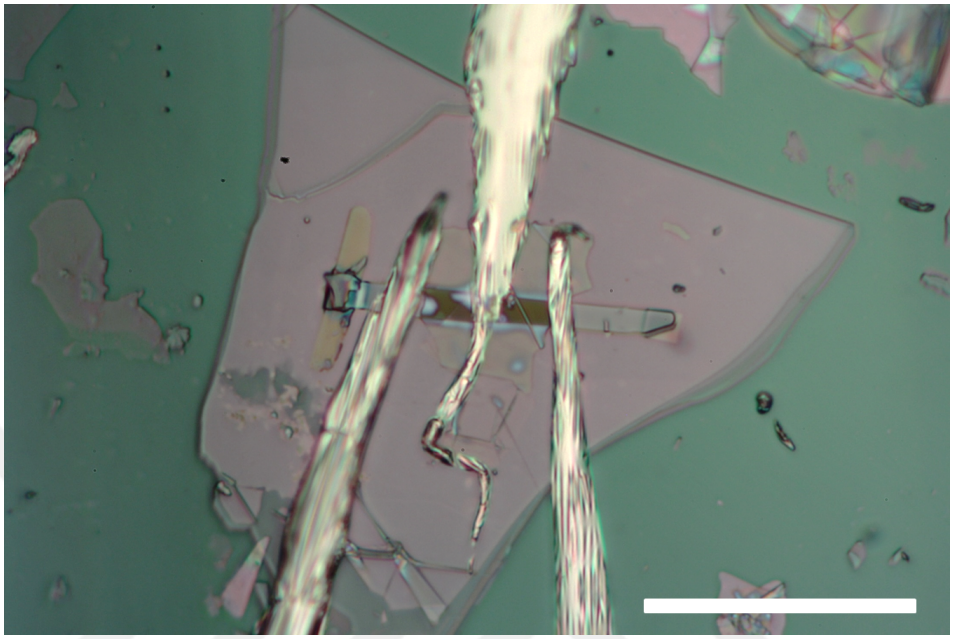


Figure 4.18: *VO_2 Based three-terminal device. Measurements in the plots in figure 4.19 and figure 4.20 are taken from this device. Scale bar is* 40 μm.

the few layers of h-BN that are used as the gate dielectric material in our devices. Gate voltages up to -12 V were then applied and changes on drain current were monitored. Dual measurement were taking and obvious hysteresis in the I_d vs. V_g measurements were observed as shown in figure 4.22. In order to confirm that this type of behavior is due to leakage, gate voltages were then plotted against gate-drain current. The same type of hysteresis were observed, confirming that the changes which are seen in the drain current with the increase in negative gate voltages are actually due to the increase in gate current as shown in the plot of gate current (I_g) vs. gate voltage (V_g) in figure 4.23. Another important conclusion to be extracted from this test is that it is essential to use fewer layers of h-BN to have better control upon the channel

After testing possible channel modulation in several three-terminal devices, the idea that the noise which is produced through the setup (in the orders of few picoamperes) might have buried down the sign of any modulation in the channel became more reasonable. To check out this possibility, channel current that might be induced through gate voltage is calculated. In this calculation, the known parameters (crystal resistivity, length, width and thickness) are used to

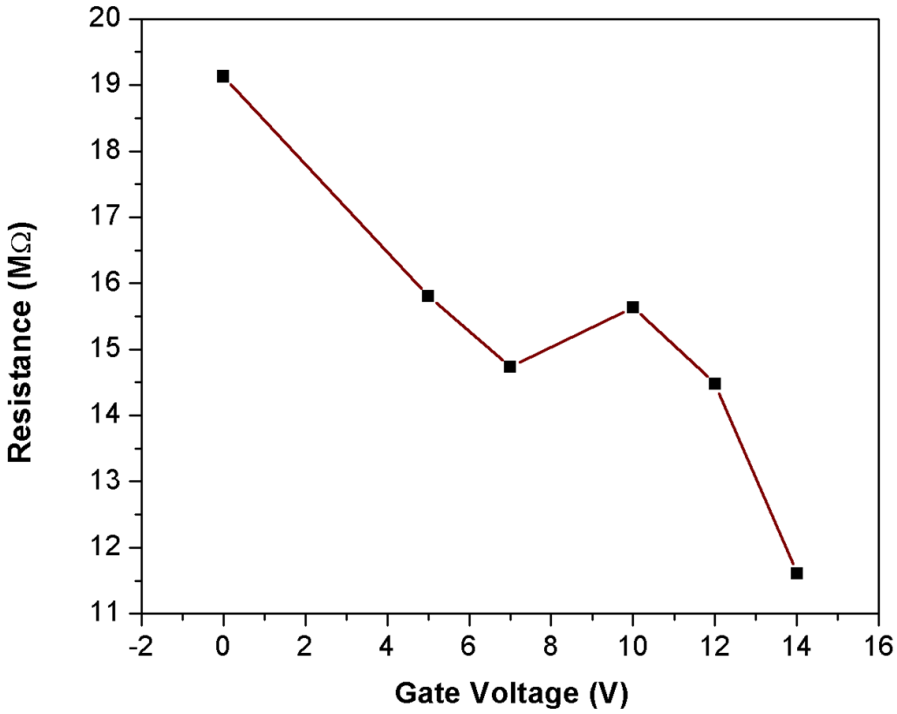


Figure 4.19: *R vs. V_g extracted from several IV measurements taken at different gate voltages from the device in figure 4.18*

calculate the total resistance of the crystal (R_{total}) using the following relation:

$$R = \rho \frac{l}{t\ \omega}$$

The total resistance of the crystal R_{total} is equal to the sum of the resistance of the crystal between the source and the gate (R_{sg}), the resistance of the crystal between the gate and the drain (R_{gd}) and the resistance of the crystal underneath the gate contact (R_g). By extracting R_g from this equation, we can now calculate the current induced through gate using Ohm's law and then verify whether it is detectable or not. The device parameters used in this calculation are as follows: Total Crystal Width (ω_{total}) = 8.5 μm, Total Crystal Length (l_{total}) = 32 μm, Source to Gate Length (l_s) = 9.4 μm, Gate to Drain Length (l_d) = 15 μm, Thickness of the crystal (t) = 5 nm, Resistivity of VO_2 crystal (ρ) $\approx$ 10 Ω.cm.

The calculated current that is expected to be induced through gate is in the order of hundreds of pA, which should have been detected in our measurements. Therefore, it is concluded from the results obtained from this device that the

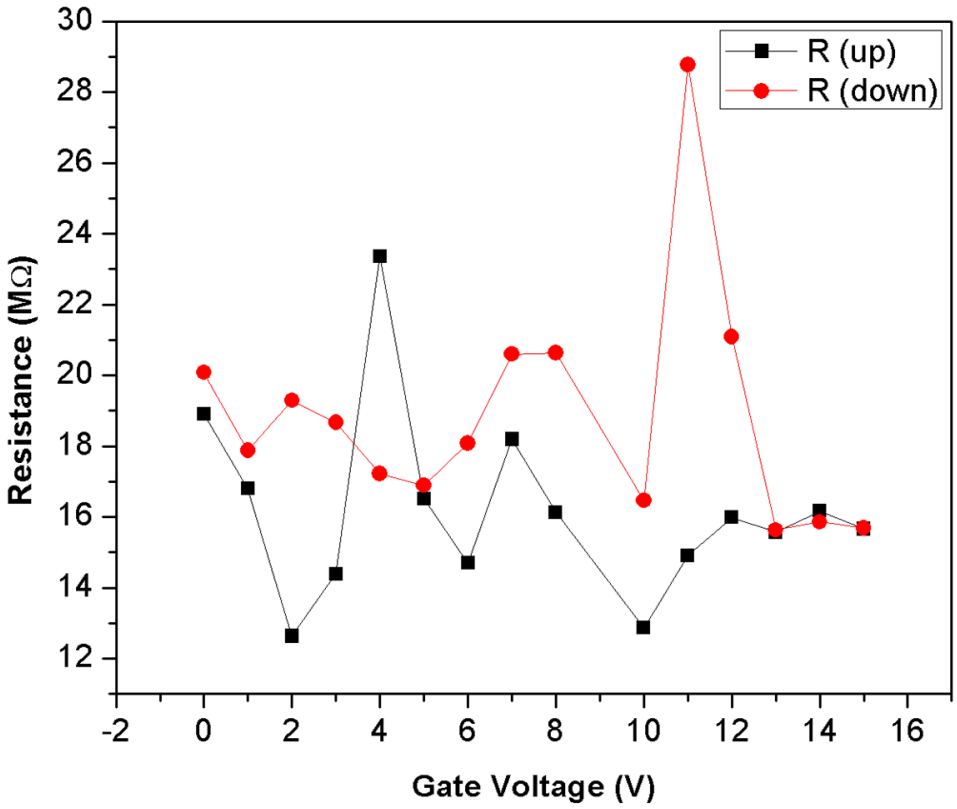


Figure 4.20: *Second set of R vs. V_g extracted from several IV measurements taken at different gate voltages from the device in figure 4.18. The trend of resistance change of the channel in these measurements is not matching the trend observed from the first measurements represented in figure 4.19*

applied gate voltage did not result in channel modulation. This part of our work is not yet conclusive. Therefore, further investigation of different device configurations are recommended to be examine in the future in order to reveal the full picture behind the possibility of fabricating functional VO_2 based Mott-FETs.

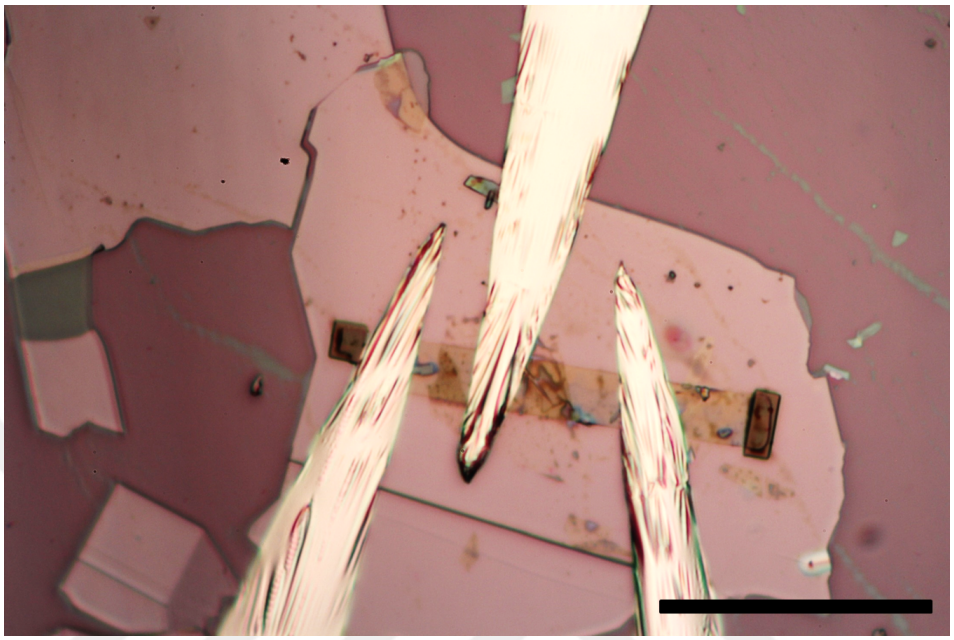


Figure 4.21: *The second VO_2 Based three-terminal device. measurements in the plots in figure 4.22 and figure 4.23 are taken from this device. Scale bar is* 40 μm.

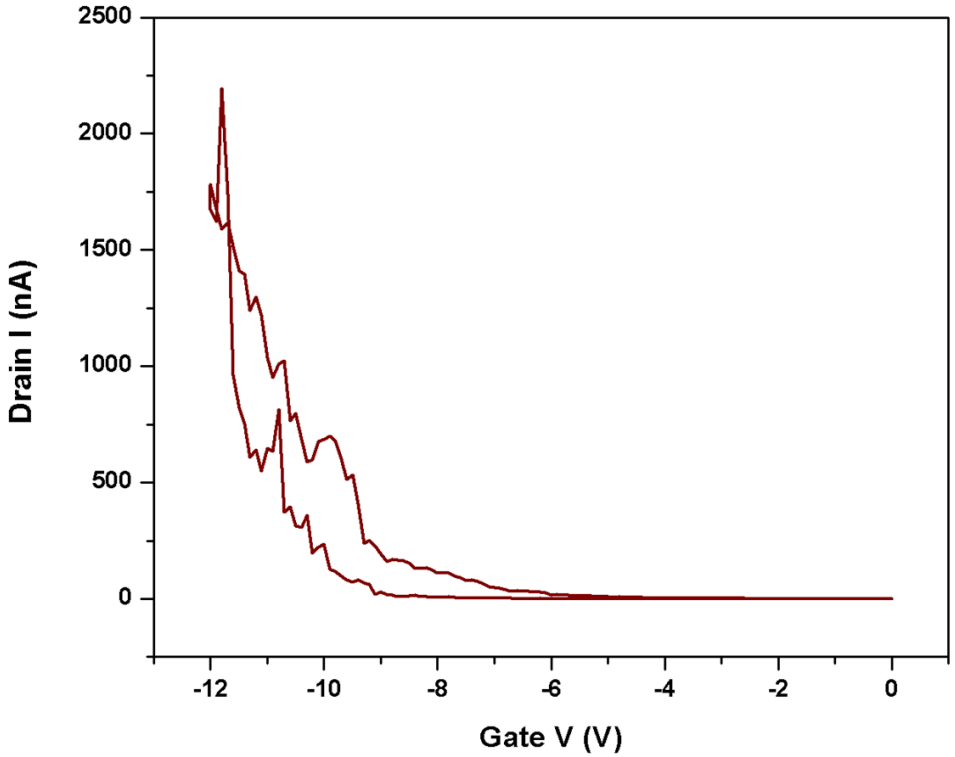


Figure 4.22: *I_d vs. V_g measurements taken at a constant V_{sd} = 100 mV, taken from the device in figure 4.21*

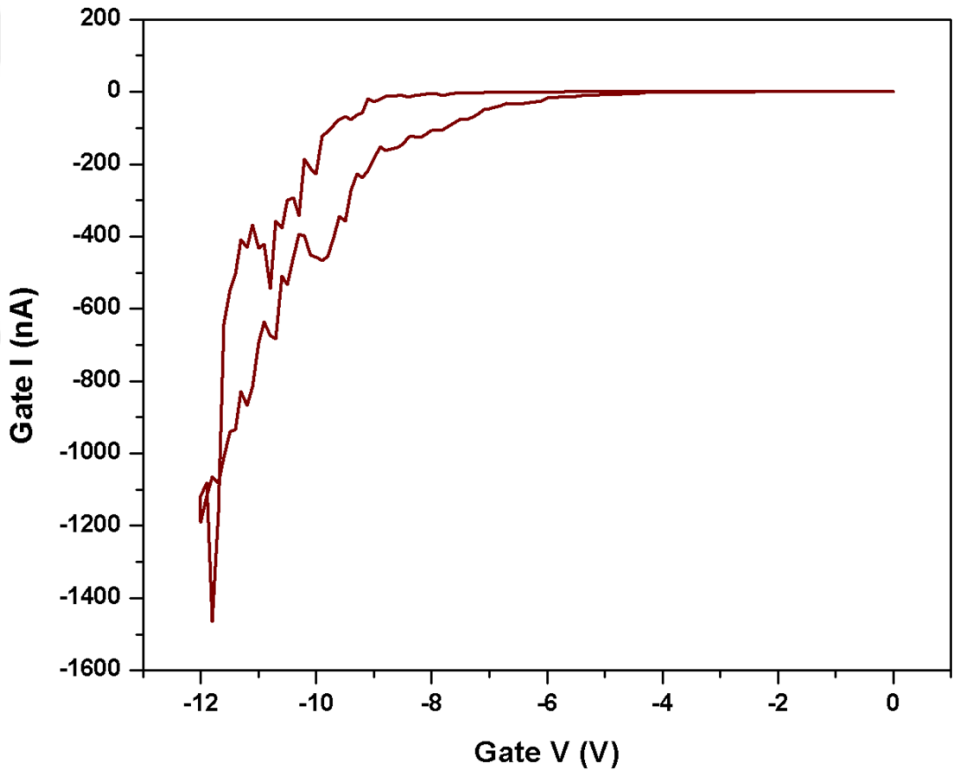


Figure 4.23: *I_g vs. V_g measurements taken at a constant V_{sd} = 100 mV, taken from the device in figure 4.21*

Chapter 5

Conclusion and Future Perspectives

In this work, most of the objectives that were set at the beginning are achieved. Many scientific research have already taken vanadium dioxide as their material of interest for its potential in the field of electrical and ultrafast optical switching in one hand, and the fundamental physics that can be revealed through studying this strongly correlated material on the other hand. One of the most attractive qualities of vanadium dioxide is the metal-insulator transition (MIT) which takes place slightly above room temperature in VO_2. To utilize this first order phase transition in applications such as transistors, thin VO_2 nanocrystal are required to overcome the limitation which is imposed by the Thomas-Fermi screening length. This indicates that external electrical stimulus in the case of VO_2 based Mott-Field Effect Transistors would only induce changes to the first few nanometers near the interface with the gate dielectric. In the case of VO_2, the screening length is known to be around 6 nm. Consequently, this imposes the limitation that thin VO_2 nanocrystals are required for both application and investigation of the physics behind exotic phenomena such as MIT. This eluded many research groups to prefer epitaxial or sputterd films of VO_2. However, for the reasons mentioned in the main text such as the stresses induced due to lattice mismatch and the interdiffusion between the film and substrate in epitaxial films and the

polycrystalline nature of sputtered films, this kind of films has been proven to be inappropriate for the applications mentioned above. Therefore, in this study we used different approach to obtain thin VO_2 noanocrystals. Random dimensions of no less than 30 nm VO_2 nanocrystals are grown using physical vapor deposition. Then these crystals are thinned down below the screening length using Ar-ion etching technique.

The first achievement of this work is the revealing of the etch rate of VO_2 using the parameters mentioned in the main text. It is found that the etch rate of VO_2 using ion-gun energy of 1 KeV is 3.3 $\pm$0.3 nm/min. This rate is revealed using the combination of the shadowing effect and the photoresist crystal protection methods along with some other side methods that are testes as well. This etch rate is then used to etch down selected VO_2 nanocrystals to the desired sub-5 nm thicknesses.

Unlike epitaxial films, vapor-phase grown VO_2 nanocrystals are possible to release out of the substrate and can be transferred to different substrates in order to eliminate the substrate-induces non-uniform stresses due to the adhesion to growth substrates. Here, we transfer VO_2 nanocrystals above exfoliated h-BN to end up with free-standing VO_2 nanocrystals. These crystals are then etched to be utilized in the study. The damage that is introduced to the top few nanometers of the crystals due to Ar-ion etching is completely removed along with its effects on the crystal quality using 37% hydrochloric acid ($HCl_{(aq)}$) treatment. Electrical measurements show the persistence of the pristine VO_2 electrical properties in the treated etched VO_2 nanocrystals. This achievement is considered to be a precursor for the demonstration of possible VO_2 based Mott-FET and the study of the effect of quantum confinement in such strongly correlated materials.

This study did not stop at this breakthrough, however, some attempts to demonstrating some possible application of the thinned pristine VO_2 nanocrystals are presented. Mainly, thee-terminal devices are fabricated using these crystals as channel material in order to provide a full picture of all fabrication challenges and suggested ways to overcome them. Also, preliminary results of electrical measurements on three-terminal devices are provided here to examine the possibility

of inducing MIT through gate control. The results provided are not conclusive in this regards. However, they can be used as reference for future works. We suggest that the area of gate coverage to be increased in order to have grater chances to induce MIT through gating. The use of e-beam lithography in pattering the contacts pads would be a better choice in order to avoid the use of indium as contact material and consequently reduce the contact resistance of these devices through evaporation of gold contacts. Also we suggest the use of fewer layers of h-BN as a dielectric material in order to reduce the threshold voltage needed to induce any modulation in the channel.

Overall, this thesis provides a systematic method to mill down vapor-phase grown VO_2 nanocrystals below 5 nm thicknesses without compromising any of their attractive properties. The outcome of this method is reproducible and reliable. This work can open the way to the study of quantum confinement in free-standing nanocrystls of other strongly correlated materials. Attempts of producing VO_2 based Mott-FET are also presented in this work.

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