FURTHER INVESTIGATIONS ON CURRENT DIFFERENCING BUFFERED AMPLIFIER

by
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CURRENT DIFFERENCING BUFFERED AMPLIFIER

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ABSTRACT

FURTHER INVESTIGATIONS ON CURRENT DIFFERENCING BUFFERED AMPLIFIER

Chapter one mentions general information about advantages of current-mode signal processing and gives circuit simulation parameters.

Chapter two presents a novel current differencer and a new current differencing buffered amplifier (CDBA) circuit which is based on this current differencer. Circuit schematics and performance results are given. Also, comparison of present study with previous designs in literature is given.

Chapter three introduces a cascadable current-mode (CM) multifunction biquadratic filter. The proposed circuit realizes all five different filter transfer functions employing only two CDBAs, while previously reported CM multifunction filters require more CDBAs and more passive component count for the same number of filter transfer function realizations. Examples for different filter transfer functions are given along with the results of circuit simulations.

CDBA-based synthetic floating inductance circuits with electronic tuning properties are introduced in chapter four. Both configurations implement a grounded capacitor, and they are fully integrable, providing the advantages of electronic tuning. Moreover, by the virtue of their impedance scaling characteristics, they offer the flexibility of representing large valued linearly tunable resistors by small modification in both circuits.

ÖZET

AKIM FARKI ALAN TAMPONLANMIŞ KUVVETLENDİRİCİ ÜZERİNE ÇALIŞMALAR

Birinci bölüm akım-modunda sinyal işlemenin avantajları ve simülasyon parametreleri ile ilgili bilgi vermektedir.

İkinci bölümde yeni bir akım farkı alıcı devre ve bu devreyi baz alan akım farkı alan tamponlanmış kuvvetlendirici (CDBA) devresi tanıtılmıştır. Devrelerin şemaları ve performans değerleri verilmiştir. Ayrıca, literatürde yayınlanmış olan diğer CDBA devreleri ile karşılaştırılması verilmiştir.

Bölüm üç kaskadlanabilir akım-modlu çok-fonksiyonlu bir biquad filtre tasarımını ele almaktadır. Sunulan devre sadece iki tane CDBA ile tüm beş filtre transfer fonksiyonunu gerçekleştirmektedir. Daha önce yayınlanmış akım-modlu filtreler daha çok sayıda CDBA ve pasif eleman gerektirmektedir. Simülasyon sonuçları ve farklı filtre transfer fonksiyonları verilmiştir.

CDBA temelli, elektronik olarak ayarlanabilen sentetik yüzen endüktans devreleri dördünce bölümde verilmiştir. İki tasarımda tamamı ile entegre edilebilen topraklanmış kapasite kullanmakta ve elektronik olarak ayarlanabilme özelliği sunmaktadır. Ayrıca, devrelerin empedans boyutlandırma özelliği sayesinde, küçük bir değişiklik ile büyük değerli lineer dirençler elde edilebilmektedir.

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α	Current gain
γ	Voltage gain
ε_p	Current tracking error for p terminal
ε_n	Current tracking error for n terminal
ε_v	Voltage tracking error
g_m	Transconductance
w_0	Natural angular frequency
AC	Alternating current
AP	All pass filter
B	Bulk of a MOS transistor
BP	Band pass filter
BS	Band stop filter
BW	Bandwidth
CCII	2nd generation current conveyor
CCCII	Current controlled 2nd generation current conveyor
CM	Current mode
CDBA	Current differencing buffered amplifier
D	Drain of a MOS transistor
DC	Direct current
IC	Integrated circuit
f_0	Natural frequency
FI	Floating inductance
FTFN	Four terminal floating nullor
G	Gate of a MOS transistor
HP	High pass filter
KHN	Kerwin-Huelsman-Newcomb (biquad filter)
L	Length of a MOS transistor
LP	Low pass filter

MOSFET	Metal oxide semiconductor field effect transistor
n	Negative input terminal of current differencer
OPAMP	Operational amplifier
OMA	Operational mirrored amplifiers
OTA	Operational transconductance amplifier
p	Positive input terminal of current differencer
Q-factor	Quality factor
S	Sensitivity
S	Source of a MOS transistor
SITO	Single input three output
SNR	Signal to noise ratio
V_{dd}	Positive power supply
V_{ss}	Negative power supply
W	Width of a MOS transistor
z	Output terminal of current differencer

1. INTRODUCTION

1.1. Advantages of Current-Mode Circuits

Originally, the term “current-mode processing” is joined to literature by Barrie Gilbert, and the first building block intended for current signal processing is the current-conveyor, published in 1968. Today, it is known that current-mode circuits such as current-mode integrators, filters, oscillators have some advantages over their voltage-mode counterparts [1].

Since the introduction of integrated circuits, the operational amplifier has served as the basic building block in analogue circuit design. Since then, new integrated analogue circuit applications have emerged and the performance requirements for analogue circuits have changed. Voltage-mode operational amplifier circuits have limited bandwidth at high closed-loop gains due to the constant gain band width product. Furthermore, the limited slew-rate of the operational amplifier affects the large-signal, high-frequency operation. A comparison of slew-rate values between two industry-standard IC, LM741 and AD844 is given in Figure 1.1. Pay attention that time axis of LM741 is in μs range while AD844 is in ns range. Calculated slew-rates are as follows: 3.71V/μs for LM741 and 1153V/μs for AD844.

One procedure for finding alternative, preferably simpler, circuit realizations is to use current signals rather than voltage signals for signal processing. MOS-transistors in particular are more suitable for processing currents rather than voltages, because the output signal is current both in common source and common gate amplifier configurations and common drain amplifier configuration is almost useless at low supply voltages because of the bulk-effect present in typical CMOS-processes [2].

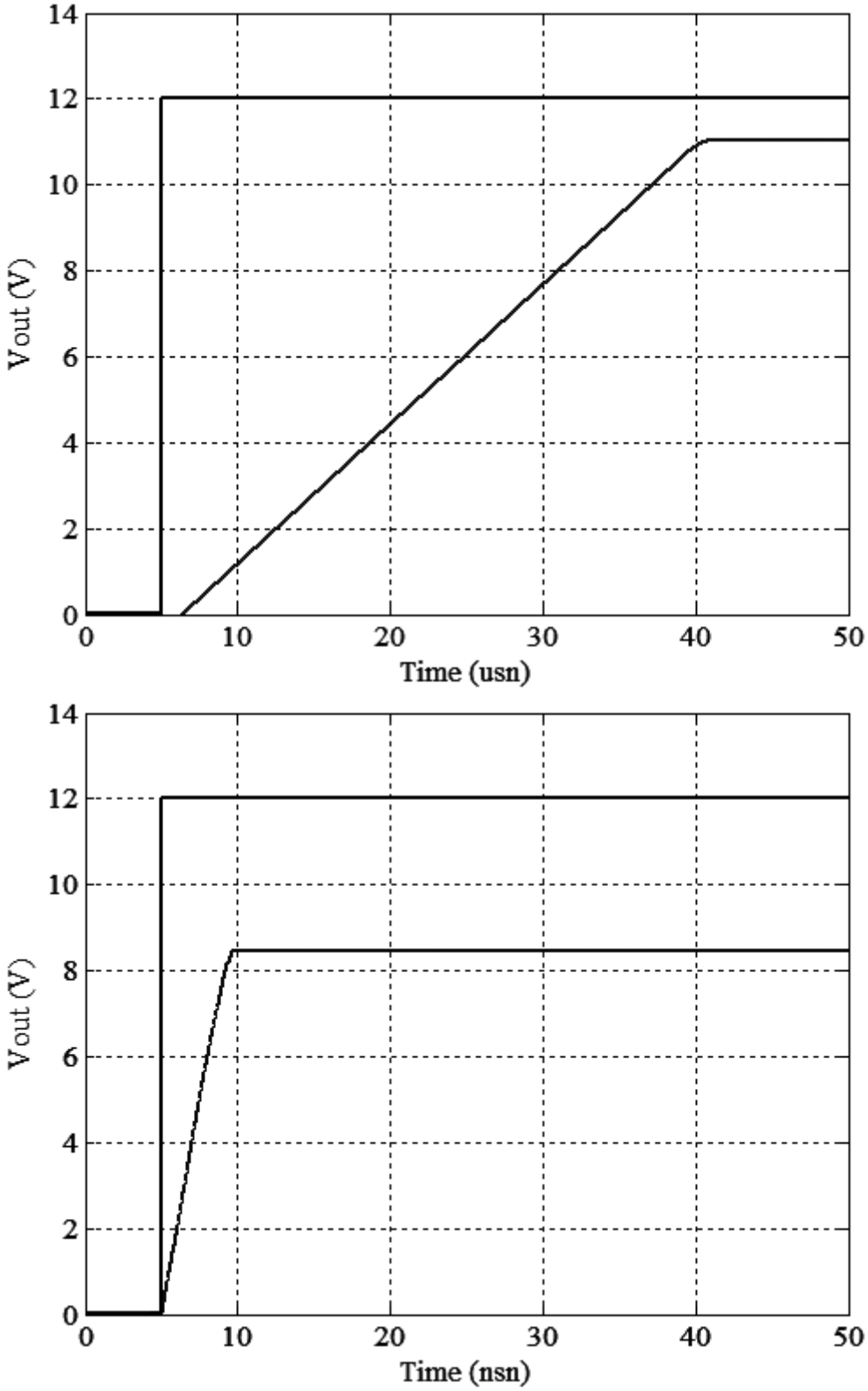

Figure 1.1. Slew-rate values of LM741 (top) and AD844 (bottom).

Moreover, MOS current-mirrors are more accurate and less sensitive to process variation than bipolar current-mirrors because with the latter the base currents limit the accuracy. Also, because of base currents, it is impossible to have 1:1 current mirroring. Therefore, at the very least, MOS-transistor circuits should be simplified by using current signals in preference to voltage signals. For this reason, integrated current-mode system realizations are closer to the transistor level than the conventional voltage-mode realizations and therefore simpler circuits and systems should result. The key to obtain better performance is to realize simpler circuits.

When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits. Current-mode circuits cannot avoid nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit techniques. Current-mode interconnection circuits in particular show promising performance.

Thus, a circuit's performance mainly depends on the number of low-impedance nodes and the way they are connected. This means complexity of a circuit is the key parameter in performance needs. As CM circuits have simple structure, they have better performance than VM circuits. But there is no gain without a drawback: CM circuits suffer from low linearity and low SNR ratios. Of course one can build complex CM circuits to achieve better linearity and high SNR ratios at the cost of lower performance.

1.2. Simulations

All circuit simulations are made with OrCAD SPICE v9.2. Level 3 TSMC 0.35μm n-well fabrication process is used. SPICE process parameters are given in Table 1.1. Power supplies used in the simulations are V_{dd}=-V_{ss}=1.8V.

Table 1.1. 0.35μm TSMC n-well process parameters.

Parameter	Value (nMOS)	Value (pMOS)
UO	436.256147	212.2319801
TOX	7.9E-9	7.9E-9
TPG	1	-1
VTO	0.5445549	-0.7140674
XJ	3E-7	2E-7
RSH	0.0559398	30.0712458
LD	3.162278E-11	5.000001E-13
ETA	0	9.999762E-4
VMAX	8.309444E+4	1.181551E+5
NSUB	1E17	1E17
PB	0.9758533	0.8152753
PHI	0.7	0.7
THETA	0.1749684	0.2020774
GAMMA	0.5827871	0.4083894
KAPPA	0.2574081	1.5
WD	7.046724E-8	1.249872E-7
CJ	1E-3	1.419508E-3
MJ	0.3448504	0.5
CJSW	3.777852E-10	4.813504E-10
MJSW	0.3508721	0.5
CGSO	2.82E-10	3.09E-10
CGDO	2.82E-10	3.09E-10
CGBO	1E-10	1E-10
DELTA	0	0
NFS	1E+12	1E+12
KP	2.055786E-4	6.733755E-5

Due to the n-well process, “B” –bulk– terminals of all nMOS transistors are shorted to the most negative power supply, namely V_{ss}; and “B” terminals of all pMOS transistors are shorted to their “S” –source– terminals. These connections can be seen in Figure 1.2. Note that, three-terminal (drain, gate and source) MOSFET symbols are used in circuit schematics to avoid complexity.

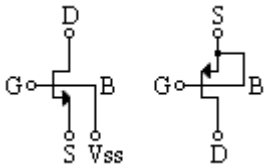

Figure 1.2. nMOS (left) and pMOS (right) transistor's "B" –bulk– terminal connections.

2. CMOS CDBA IMPLEMENTATION

In this chapter, a novel CMOS-based Current differencing buffered amplifier (CDBA) [3] structure is presented. Major advantages of the proposed circuit are its very low input terminal impedances thanks to voltage buffer architecture and large frequency bandwidth.

2.1. Proposed Circuit

CDBA is a relatively new active circuit element. The CDBA is free from parasitic input capacitances; it can operate in a wide frequency range, is suitable for current mode operation while, and also provides a voltage output. Many voltage and current mode applications using this element have already been reported in literature [4-26]. The circuit symbol of the CDBA is shown in Figure 2.1, and its terminal relationships can be described as

$$V_p=V_n=0,\ I_z=\alpha_p I_p-\alpha_n I_n,\ V_w=\gamma V_z \tag{2.1}$$

where α_p, α_n and γ are current and voltage gains, respectively, and $\alpha_p=1-\varepsilon_p$, $\alpha_n=1-\varepsilon_n$, $\gamma=1-\varepsilon_v$. Here, ε_p, ε_n are current tracking errors and ε_v is the voltage tracking error, absolute values of all last three terms being much less than unit value.

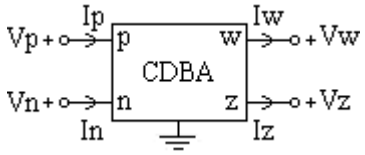

Fig. 2.1. Circuit symbol of the CDBA.

Ideally, current through z terminal follows the difference of the currents through p terminal and n terminal. Input terminals p and n are internally grounded. The difference of the input currents are converted into the output voltage V_w, therefore CDBA element can be considered as a transimpedence amplifier. The CDBA can be considered as a collection of current and voltage-mode unity gain cells, and it is free from many parasitics. Note that, input impedances of the CDBA element are zero while output impedance is infinite.

Principal schematic of the current differencing section is given in Figure 2.2. Voltage buffers provide low input impedances and also keep input terminals at virtual ground[1]. Current mirrors convey the input signals to the output terminal.

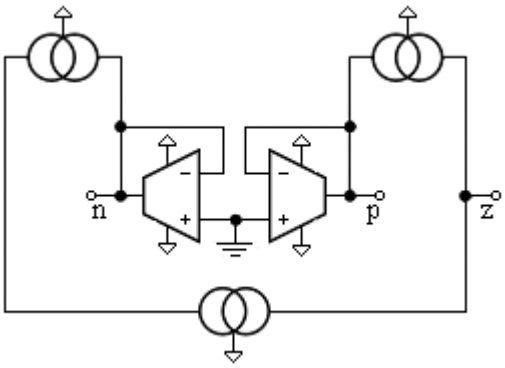

Fig. 2.2. Principle schematic of the proposed current differencer.

[1] It is called virtual since this point does not have any real electrical connection to ground. A virtual ground presents very low impedance to any signal connected to it and it therefore provides the perfect type of input for current type signal sources [27].

CMOS Transistor level schematic of current differencing section is displayed at Figure 2.3. Note that, the buffers are combined using a three-input differential amplifier section instead of using two separate voltage buffers. Positive input parts of the differential input stages of the buffers share M03 and M05 transistors and only a single transistor is used for biasing purpose. This design technique saves three transistors, one for driver transistor, one for its load and one for the bias transistor. Since driver and bias transistors could be large, considerable amount of chip area is saved, [approximately 290$(\mu m)^2$].

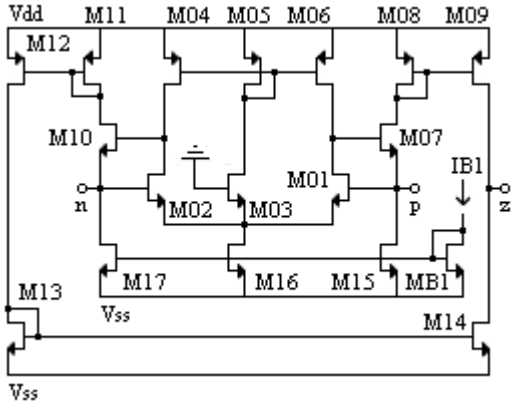

Fig. 2.3. Transistor level schematic of the proposed current differencer.

Assuming that transistors M01-M03 and M04-M06 are perfectly matched, current mirror load (M04-M06) ensures that M01-M03 transistors have the same drain current. Also, source terminals of M01-M03 transistors are tied to same node, so that their source voltages are same. Therefore, their gate voltages are forced to be at same voltage level, which causes p and n terminals to be at the same voltage level with the gate of M03, namely virtual ground. Circuit simulations show that, p and n terminals have voltage levels within ±400μV range for the entire dynamic range.

The positive input current I_p is conveyed to the output z terminal by current mirrors M08-M09, while negative input current I_n is carried to the output through M11-M12 and

M13-M14. I_p flows to z terminal and I_n flows from z terminal so that the output current at z terminal is $I_z=I_p-I_n$.

Input and output resistances of the current differencer are formulated as [28]:

$$r_p = \frac{(g_{m1}+g_{m3})\cdot(g_{d1}+g_{d3})}{g_{m1}\cdot g_{m3}\cdot g_{m7}} \tag{2.2}$$

$$r_z = 1/(g_{d9}+g_{d14}) \tag{2.3}$$

where g_{di} and g_{mi} are the drain conductance and conductance, respectively, of transistor M_i.

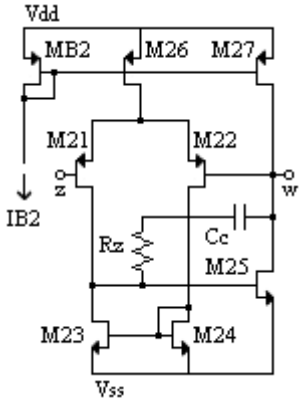

Fig. 2.4. Schematic of the Miller-OTA based buffer.

Designed buffer is a Miller-OTA with unity gain feedback. It consists of a differential amplifier (M21, M22, M23 and M24) and a common source output stage with a driver transistor of M25. There is a unity feedback between output and negative input

which guarantees low output impedance. Input of the OTA is through the gate of M21, which provides very large input impedance due to oxide structure of the gate. Feedback also increases the input impedance. Schematic of the buffer section is displayed in Figure 2.4.

Output resistance and gain of the buffer can be calculated as

$$r_w = \frac{(g_{m21} + g_{m22}) \cdot (g_{d22} + g_{d24})}{g_{m21} \cdot g_{m22} \cdot g_{m25}} \tag{2.4}$$

$$\frac{V_w}{V_z} = \frac{g_{m22}}{g_{m22} + g_{d22} + g_{d24}} \tag{2.5}$$

where g_{di} and g_{mi} are the drain conductance and conductance, respectively, of transistor M_i.

2.2. Simulation Results

Transistor aspect ratios are given in Table 1. Size of the M12 is not equal to that of the M11 to cancel the gain error. Bias current I_{B1} is chosen as 20μA. Increasing the bias current widens the bandwidth, enlarges output impedance, and increases input current range, but at the same time output impedance begins to fall at lower frequencies, input impedance enlarges, and power dissipation rises.

Table 2.1. Transistor dimensions of the current differencer (μm/μm).

Transistor	W / L
M01-M03	70/0.7
M15-M17	56/0.7
M07, M10	42/0.7
M04-M06	28/0.7
M08, M09, M11, M13, M14	10.5/0.7
M12	9.8/0.7
MB1	7/0.7

Buffer is compensated with pole-zero compensation technique. Miller capacitance used in this topology is C_c=0.2pF and lead compensation resistance is R_z=1kΩ. Transistor aspect ratios are reported in Table 2. Bias current, I_{B2} is chosen as 30μA.

Table 2.2. Transistor dimensions of the buffer (μm/μm).

Transistor	W / L
M21, M22, M28	98/0.7
M25	84/0,7
M27	77/0.7
M23, M24	14/0.7
MB2	7/0.7

Current gain simulation results are α_p=1.004 and α_n=0.991. Proposed current differencer works well above GHz range. Figure 2.5 displays the -3dB bandwidths for the current gains $I_z/(I_p-I_n)$ for I_n=0A and $I_z/(I_n-I_p)$ for I_p=0A which are at 1.25GHz and 1.07GHz, respectively. $I_z/(I_n-I_p)$ has lower bandwidth due to the fact that, negative input signal is conveyed to the output via two current mirrors while $I_z/(I_p-I_n)$ is conveyed via one current mirror. Output z terminal is grounded for this simulation.

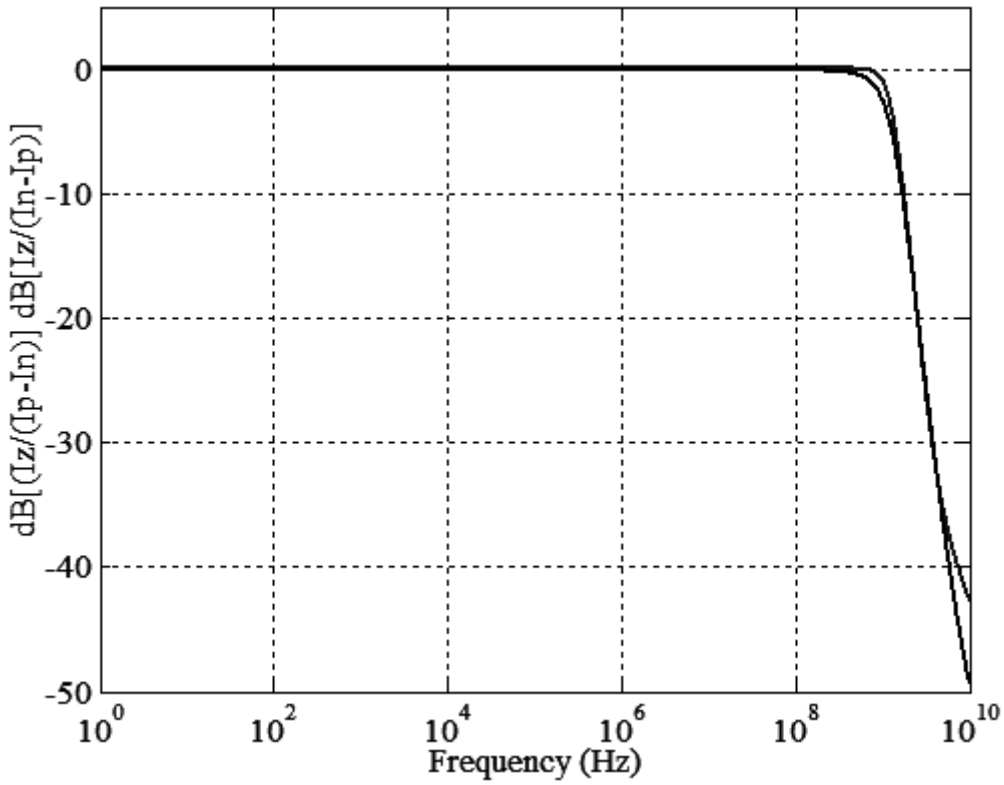

Fig. 2.5. $I_z/(I_p-I_n)$ and $I_z/(I_n-I_p)$ bandwidths of the current differencer.

DC characteristic shown on Figure 2.6 is the output current $I_z=I_p-I_n$ against the input current I_p while I_n=0A. Output z terminal is grounded for this simulation. Maximum offset current is 6.15μA for I_n=+170μA.

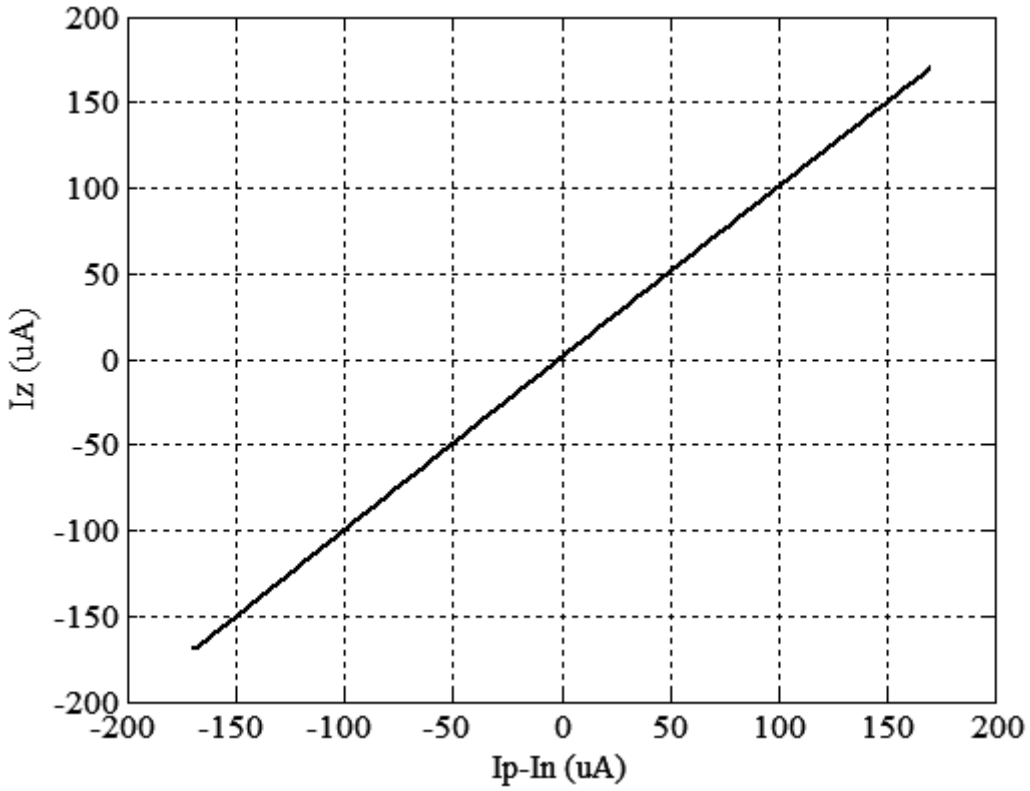

Fig 2.6. DC current tracking range simulation result.

Figure 2.7 is the simulation result of sweeping input current I_p while output z terminal is open-circuited and I_n=0A. This is the voltage that will be transferred to the output w terminal.

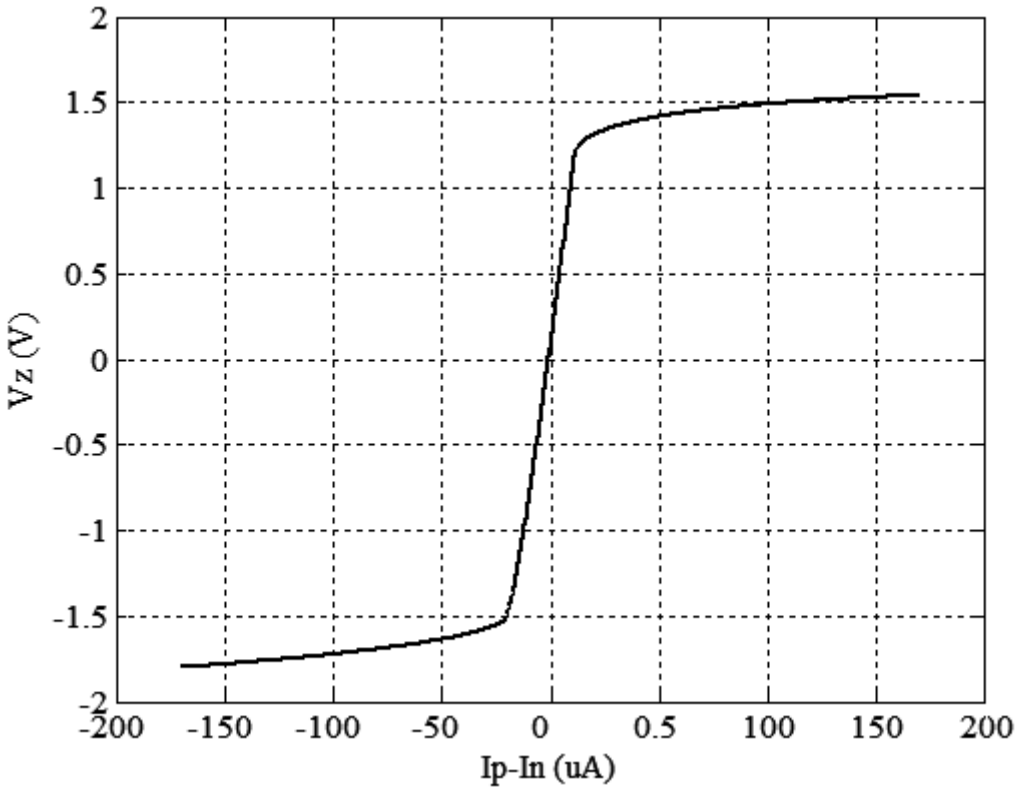

Fig. 2.7. Output voltage swing when the z terminal is open circuited.

Input impedance for p and n terminals is 1.32Ω for low frequencies while it has a peak value of 1.25kΩ at 944MHz. Output impedance is 222.5kΩ for low frequencies and starts to fall after about 30MHz. Figures 2.8 and 2.9 display input and output impedances versus frequency, respectively.

AC voltage sources V_p and V_n are connected to input terminals and output node is grounded. Let I_{Vp} and I_{Vn} be the currents flowing from the voltage sources to the input nodes of current differencer. Therefore:

$$Z_p = V_p / I_{Vp} \,,\; Z_n = V_n / I_{Vn} \tag{2.6}$$

give the input impedances. For output impedance simulation, inputs are grounded and an AC source, V_z is connected to output terminal. Therefore, output impedance will be:

$$Z_z = V_z / I_{Vz} \tag{2.7}$$

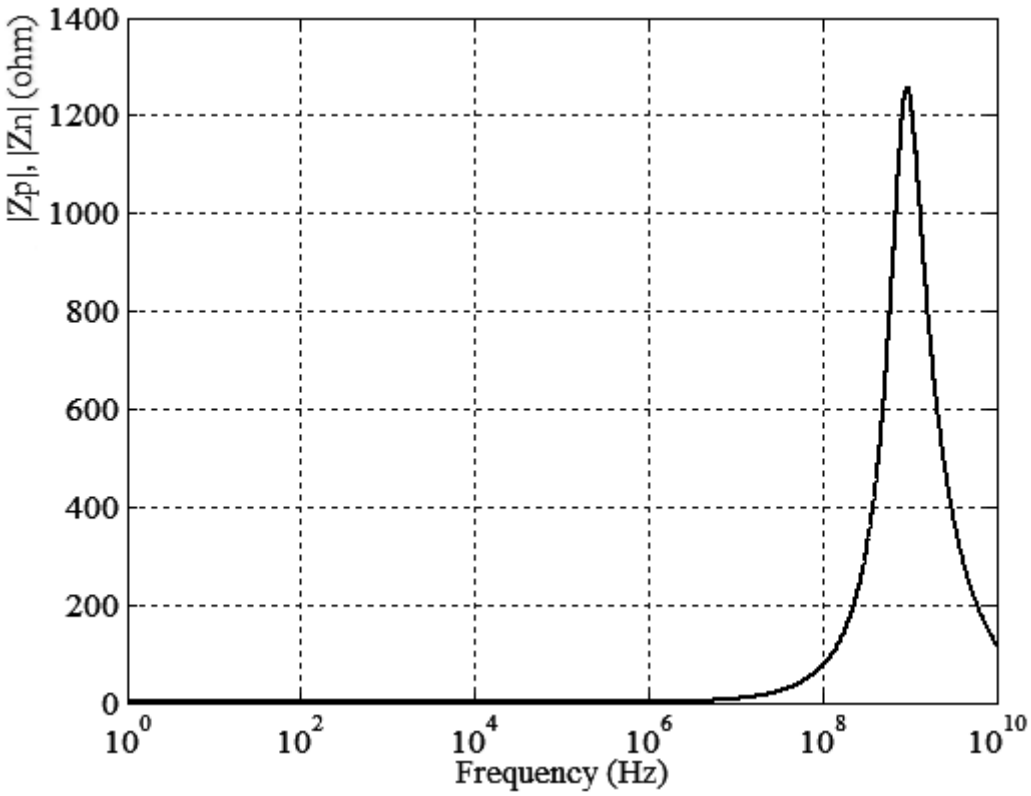

Fig. 2.8. Input impedances of terminals p and n.

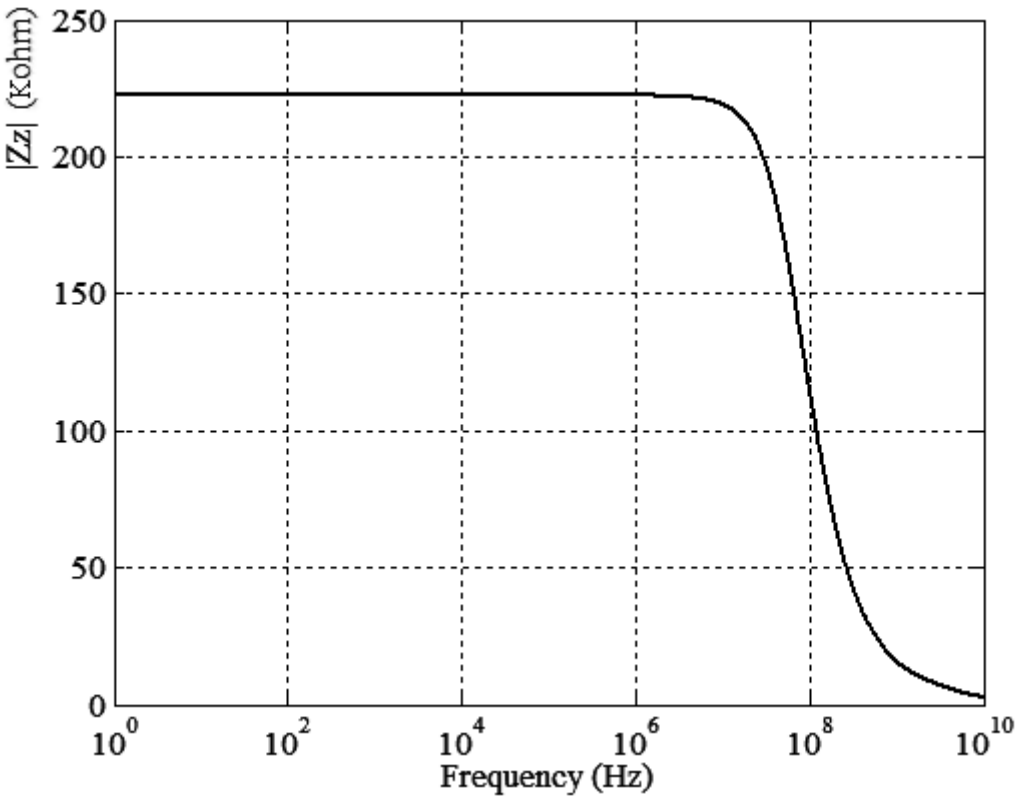

Fig. 2.9. Output impedance of current differencer.

Simulations show that, buffer can track input voltages between -1.73V and +1.63V, as seen at Figure 2.10. The offset voltage appearing at output terminal is -980μV. Voltage gain β_v is 0.9999. The -3dB bandwidth displayed in Figure 2.11 for V_w/V_z is located at 1.15GHz with a phase margin of 70˚.

Input impedance is on the order of GΩs while advantage of the unity gain feedback can be seen at the output impedance value as it has a value of 1.31Ω for low frequencies and has peak value of 555Ω at 1.68GHz, as seen in Figure 2.12.

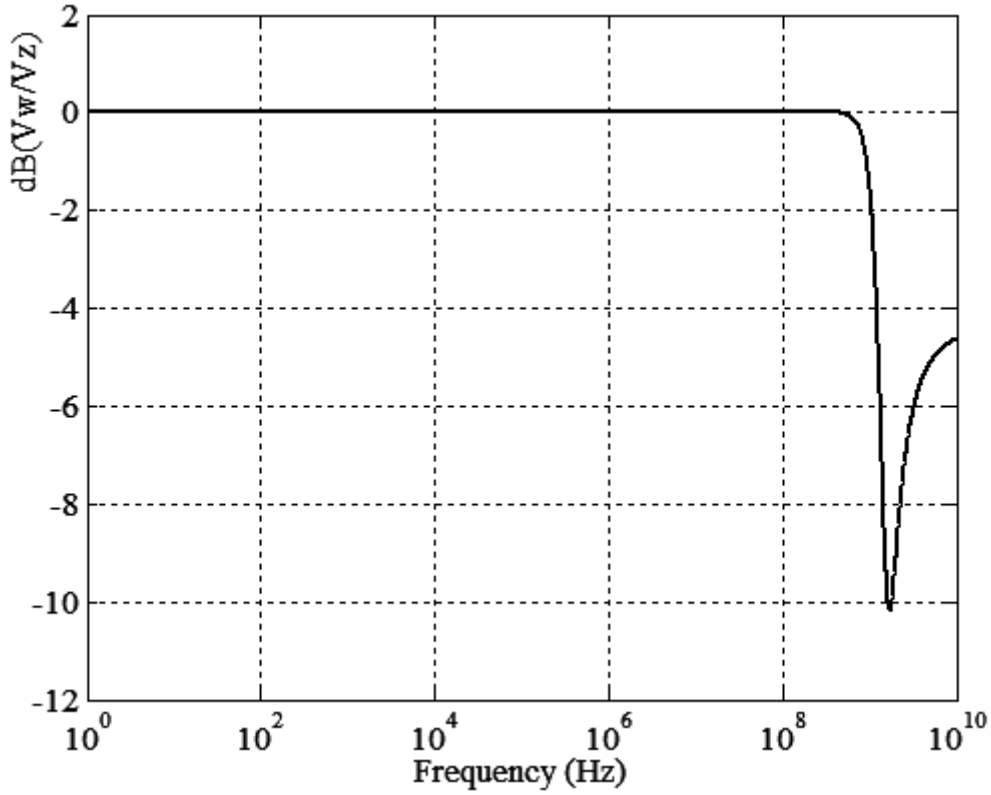

Fig. 2.10. V_w/V_z AC response of the buffer.

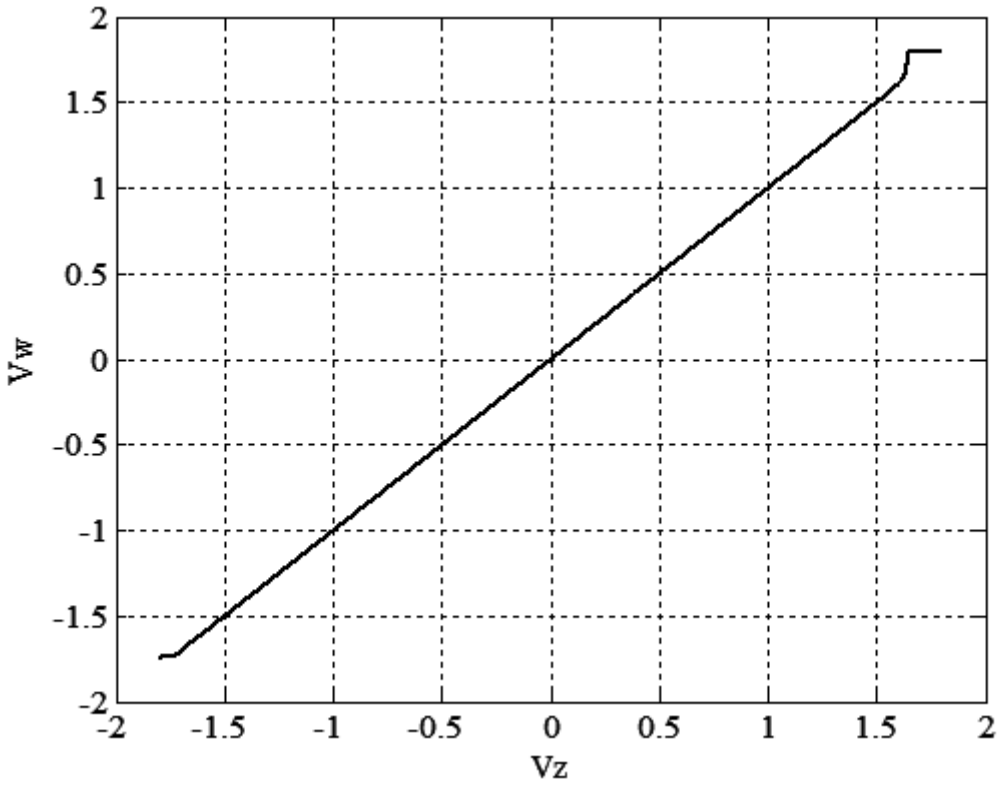

Fig. 2.11. V_w/V_z DC response of the buffer.

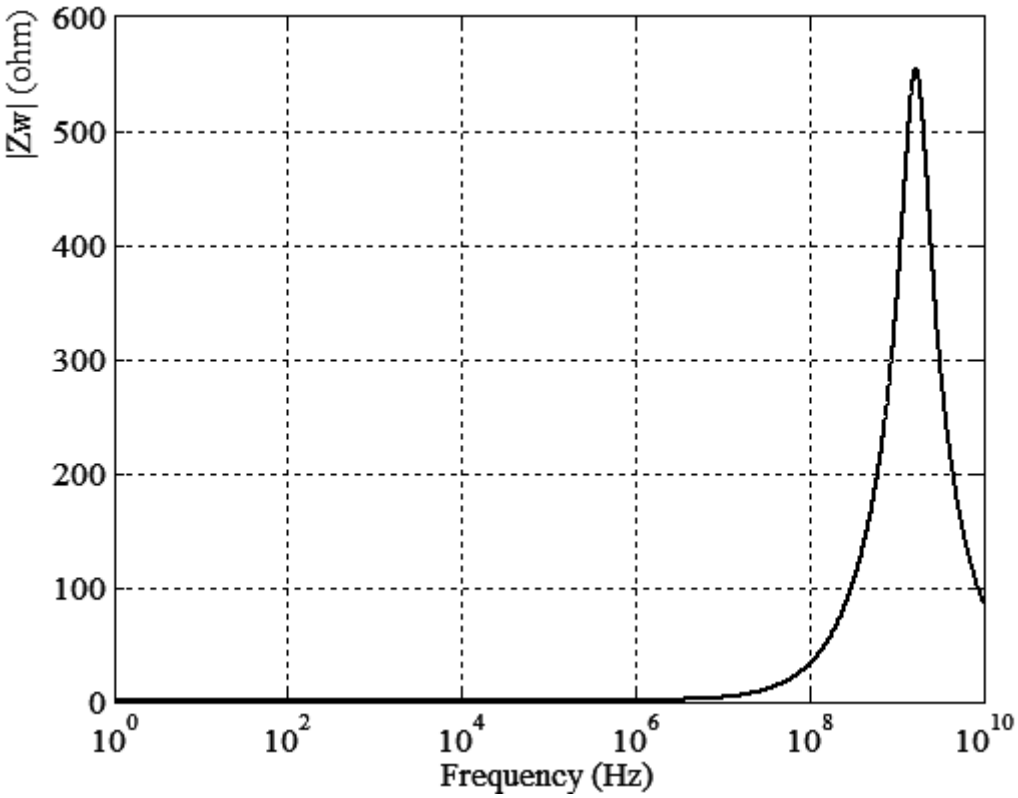

Fig. 2.12. Output impedance of voltage buffer.

2.3. Comparison with Previous Designs

Complete CDBA circuit is built using the above mentioned current differencer and Miller-OTA based buffer. Simulated power dissipation for $I_p=I_n=0A$ is 5.52mW. Figure 2.13 shows the full schematic of the design.

There are several CMOS-based CDBA designs previously published in literature [26, 29, 30]. One of these CDBA circuit designs [26] suffers from high input terminal impedances and its voltage buffer gain is much less than unity. Another work in [29] uses two second generation current conveyors (CCII) and a voltage buffer which makes the circuit very complicated and again it has large input impedances. On the other hand, the work in [30] has an advantage of low voltage operation but its bandwidth is reduced.

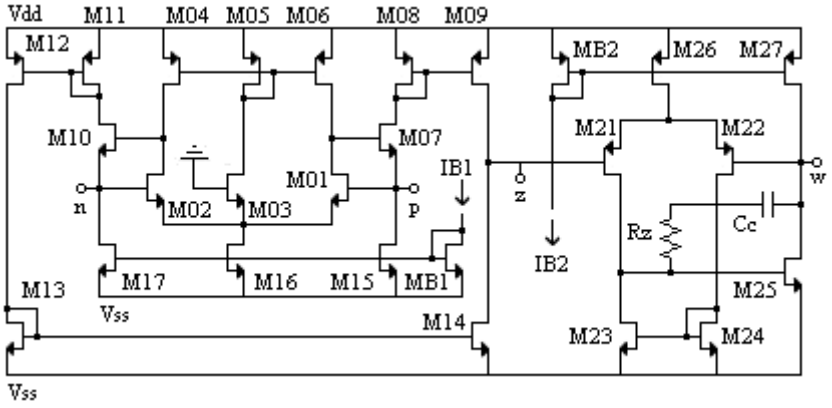

Fig. 2.13. Complete schematic of the designed CDBA.

Performance data of the new CDBA is given in Table 2.3 along with the performance data of previous realizations in literature, for comparison.

Table 2.3. Comparison of present study with other CDBA realizations.

Parameter	Toker[2] [26]	Tarım [29]	Tangsrirat [30]	Present Study
Supply voltages	±2.5V	±5V	±1.25V	±1.8V
Technology	TSMC 0.35µm	TUBITAK 3µm	HP 0.5µm	TSMC 0.35µm
Bandwidth I_z/I_p, I_z/I_n	372MHz, 255MHz	70MHz	628MHz, 642MHz	1.25GHz, 1.07GHz
Bandwidth V_w/V_z	362MHz	37MHz	432MHz	1.15GHz
Current gain α_p, α_n	0.994,1.028	0.996	0.992, 0.983	1.004, 0.991
Buffer voltage gain γ	0.88	0.9999	0.991	0.9999
Input impedance $\|Z_p\|$, $\|Z_n\|$	809Ω, 407Ω	645Ω	32Ω	1.32Ω
Output impedance $\|Z_z\|$	34kΩ	678MΩ	144kΩ	222.5kΩ
Output impedance $\|Z_w\|$	107Ω	49Ω	9Ω	1.31Ω
Power consumption (I_p=I_n=0)	10.2mW	N/A	0.98mW	5.52mW

[2] There was no simulation data for this circuit. Simulations are made for comparison using same technology with present study.

3. CURRENT MODE MULTIFUNCTION FILTER USING TWO CDBAs

3.1. Introduction

Multifunction type active filters are especially versatile, since the same topology can be used for different filter functions. In spite of the fact that numerous current mode (CM) multifunction filters are reported in literature, most of them use at least three active elements, and only few can realize all types of current transfer functions using reduced number of active elements.

Some multi-function CM filters containing CDBA elements were published in literature [7-9]. However, they employ more than two CDBAs to realize all five (LP, HP, BP, BS and AP) filter transfer functions. For example, one study [7] reports a KHN equivalent CM biquad circuit using three CDBA elements, while another one [8] describes a CM universal filter consisting of MOSFET-C integrators with single input three output (SITO) structure requiring four CDBAs for five different filter configurations. On the other hand, the work in [9] introduces a multifunction filter which realizes simultaneous LP, HP and BP filter transfer functions using two CDBAs, therefore more than two CDBAs are needed to set up a filter to realize all five filter functions.

In a recent paper [10], the realization of an nth order current transfer function by an active RC circuit involving two CDBAs is introduced. It is shown that the general current transfer function can be realized using two CDBAs. The resulting circuit has no canonical structure and reduces the number of active components considerably, in contrast to a previously reported one [11]. As an application of this general CM circuit that realizes an nth order current transfer function by an active RC circuit, the study here presents a new

current mode multifunction biquad which realizes all five filter transfer functions using only two CDBA elements, and reports the properties of this configuration.

3.2. Proposed Circuit

The current transfer function of the circuit in Figure 3.1 [10] using two CDBA elements has the following form in the case that the CDBAs are ideal.

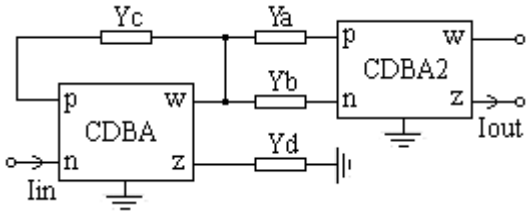

Figure 3.1. CDBA-based circuit realizing nth-order current transfer function.

$$H(s) = \frac{I_o(s)}{I_i(s)} = \frac{Y_a - Y_b}{Y_c - Y_d} \tag{3.1}$$

where Y_i are positive real admittance functions of passive two terminal elements. One of their terminals is either grounded or internally grounded.

Based upon this configuration, Figure 3.2 displays the proposed current mode, CDBA-based multifunction filter [20].

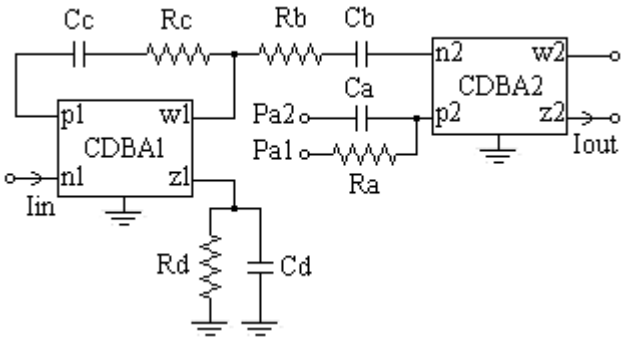

Figure 3.2. CDBA-based current mode multifunction biquad.

Note that the circuit is a low pass (LP) filter if P_{a1}, w_1 terminals are shorted together;

$$\frac{I_o}{I_{in}} = \frac{R_d}{R_a} \cdot \frac{\frac{1}{R_b C_b R_d C_d}}{D(s)} \tag{3.2}$$

where,

$$D(s) = s^2 + \left(\frac{1}{R_b C_b} + \frac{1}{R_d C_d} - \frac{1}{R_c C_d} \right) s + \frac{1}{R_b C_b R_d C_d} \tag{3.3}$$

It becomes a high pass (HP) filter in the case that P_{a2} and w_1 terminals are shorted together;

$$\frac{I_o}{I_{in}} = \frac{C_a}{C_d} \cdot \frac{s^2}{D(s)} \tag{3.4}$$

One will have a band pass (BP) filter if P_{a1} and P_{a2} terminals are disconnected;

$$\frac{I_o}{I_{in}} = -\frac{1}{R_b C_d} \cdot \frac{s}{D(s)} \tag{3.5}$$

When P_{a1}, P_{a2}, and w_1 terminals are joined, a notch (BS) filter is obtained if $R_a=R_d=2R_b$, $C_b=2C_d=2C_a$.

$$\frac{I_o}{I_{in}} = \frac{s^2 + \left(\frac{1}{R_b C_b}\right)^2}{D(s)} \tag{3.6}$$

The last configuration can be used as an all pass (AP) filter if $R_c=\infty$, $R_a=R_d=4R_b$, $C_b=4C_d=4C_a$.

$$\frac{I_o}{I_{in}} = \frac{s^2 - \frac{2}{R_b C_b} s + \left(\frac{1}{R_b C_b}\right)^2}{D(s)} \tag{3.7}$$

Note that, C_a is omitted ($C_a=0$) for the low pass configuration, R_a is omitted ($R_a=\infty$) for the high pass filter realization. On the other hand, both R_a and C_a are omitted for the band pass configuration, while R_c is omitted for the all pass case. The natural angular frequency w_o and the pole Q-factor of this filter are

$$w_0 = \frac{1}{\left(R_b R_d C_b C_d\right)^{1/2}} \tag{3.8}$$

$$Q = \frac{\left(R_b R_d C_b C_d\right)^{1/2}}{R_b C_b + R_d C_d - \dfrac{R_b R_d C_b}{R_c}} \tag{3.9}$$

It is apparent that Q can be controlled by varying R_c without affecting w_o.

3.3. Non-ideal Case

In non-ideal case, the CDBA can be characterized by

$$V_p=V_n=0,\ I_z=\alpha_p I_p-\alpha_n I_n,\ V_w=\gamma V_z \tag{3.10}$$

where α_p, α_n and γ are current and voltage gains, respectively, and $\alpha_p=1-\varepsilon_p$, $\alpha_n=1-\varepsilon_n$, $\gamma=1-\varepsilon_v$. Here, ε_p, ε_n are current tracking errors and ε_v is the voltage tracking error, absolute values of all last three terms being much less than unit value. Note that, natural frequency of this biquad is not influenced by tracking errors of the CDBA, and other w_o and Q -factor sensitivities are

$$S_{\gamma}^{\omega o} = S_{\alpha p}^{\omega o} = S_{\alpha n}^{\omega o} = S_{\alpha n}^{Q} = S_{Cd}^{Q} = 0 \tag{3.11}$$

$$S_{Rb}^{\omega o} = S_{Rd}^{\omega o} = S_{Cb}^{\omega o} = S_{Cd}^{\omega o} = -1/2 \tag{3.12}$$

$$S_{Rd}^{Q} = -\frac{R_b C_b - R_d C_d + \gamma\alpha_p R_d R_b C_b / R_c}{2[\gamma[\ _p R_d R_b C_b / R_c - (R_b C_b + R_d C_d)]} \tag{3.13}$$

$$S_{Rb}^{Q} = S_{Cb}^{Q} = -S_{Cd}^{Q} = -\frac{R_d C_d - R_b C_b + \gamma\alpha_p R_d R_b C_b / R_c}{2[\gamma[\ _p R_d R_b C_b / R_c - (R_b C_b + R_d C_d)]} \tag{3.14}$$

$$S_{\alpha p}^{Q} = S_{\gamma}^{Q} = \frac{\gamma\alpha_p R_d R_b C_b}{\gamma\alpha_p R_d R_b C_b - R_c (R_b C_b + R_d C_d)} \tag{3.15}$$

Here, for filters with complex poles, Q -factor sensitivities (3.13 - 3.15) can be minimized by proper selection of component values. On the other hand, for filters having real poles, the feedback path between w - p terminals of the CDBA vanishes. This means that two components are reduced from the configuration, further desensitizing the Q -factor of the circuit against tracking errors.

3.4. Circuit Simulations

Figure 3.3 demonstrates the results of circuit simulations for the following cases. In this simulation, we have increased the compensation capacitance of the voltage buffer due to the peaks appearing at high frequencies. Increasing the compensation capacitance decreases the bandwidth of the buffer.

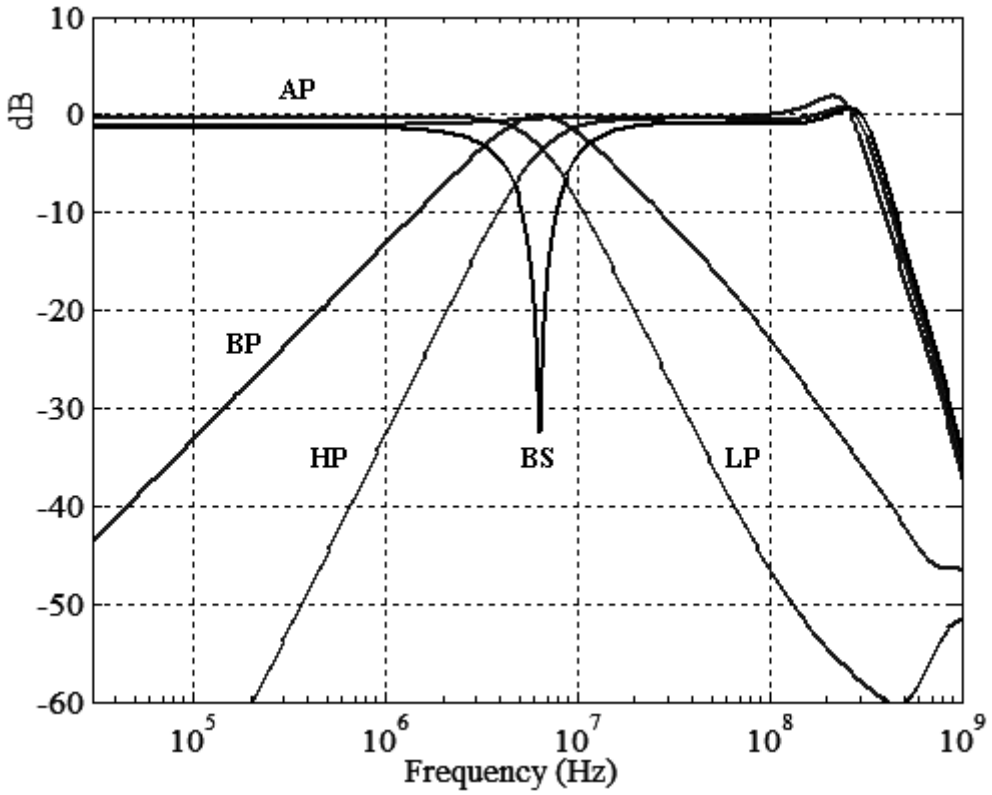

Figure 3.3. Results of circuit simulations relating bode magnitude plots for five different current transfer functions.

Table 3.1. Component values.

Filter type	Component values
Low Pass Filter, Butterworth	$C_b=C_c=7.07pF$, $C_d=14.14pF$ $R_a=R_b=R_c=R_d=2.5k\Omega$
High Pass Filter, Butterworth	$C_a=C_b=C_c=C_d=2.5pF$ $R_b=R_c=14.14k\Omega$, $R_d=7.07k\Omega$
Band Pass Filter, Butterworth	$C_b=14.14pF$, $C_c=C_d=7.07pF$ $R_b=R_d=25k\Omega$, $R_c=5k\Omega$
Notch filter, Butterworth	$C_a=C_c=C_d=1.7675pF$, $C_b=3.535pF$ $R_a=R_c=R_d=14.14k\Omega$, $R_b=7.07k\Omega$
All Pass Filter	$C_a=C_d=2pF$, $C_b=8pF$ $R_a=R_d=12.5k\Omega$, $R_b=3.125k\Omega$

All absolute w_o and Q -component sensitivities at these below-given component values are less than or equal to unity. These component values yields a characteristic frequency of f_0=6.37MHz while simulation results give a value of f_0=6.31MHz. Therefore, simulation results are in good agreement with theory. Component values for each filter configuration are given in Table 3.1.

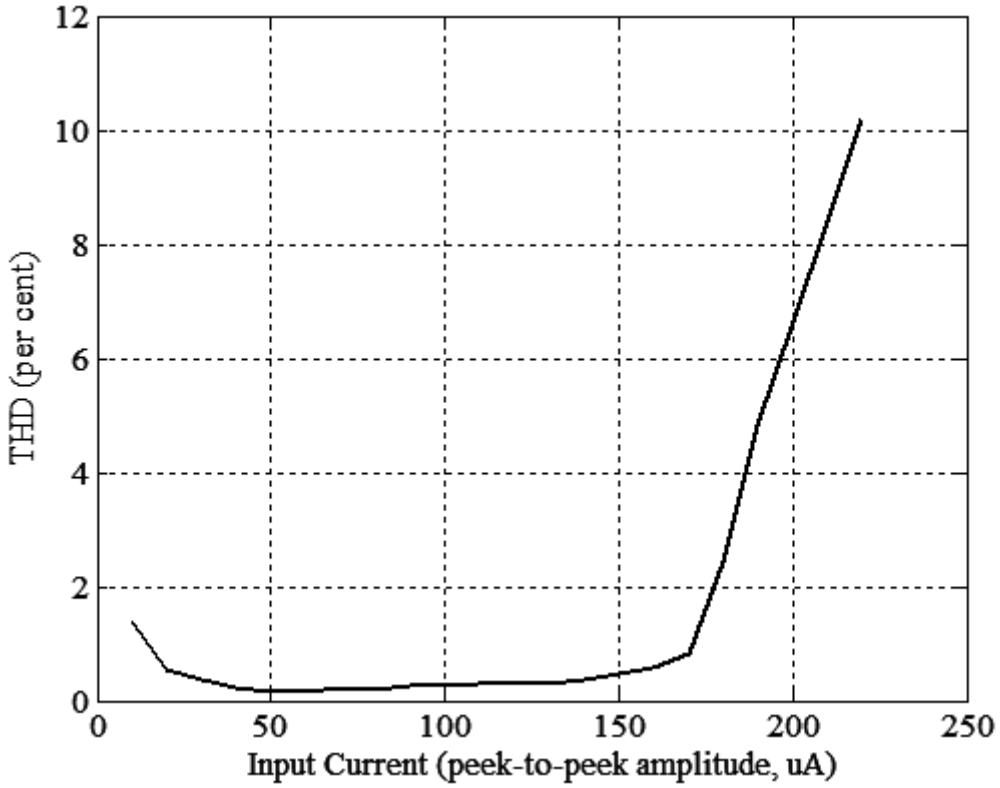

Figure 3.4. Dependence of the output harmonic distortion of BP filter on input current amplitude.

To test the input dynamic range of the filter, the simulation has been repeated for a sinusoidal input signal at f_0=6.31MHz. Amplitude of the input current is swept from 10μA to 210μA. The output harmonic distortion of BP filter is illustrated in Figure 3.4. From Figure 3.4, we see that the harmonic distortion rapidly increases if the input signal is increased beyond 170μA for the chosen CDBA implementation. This is quiet normal because maximum input current is limited at -170μA for the current differencer.

Figure 3.5 displays the effect of total harmonic distortion at output signal. Here, a sinusoidal current with peak-to-peak amplitude of 170μA and frequency of f_0=6.31MHz is used as input signal. Total harmonic distortion at this amplitude is about 0.84 per cent.

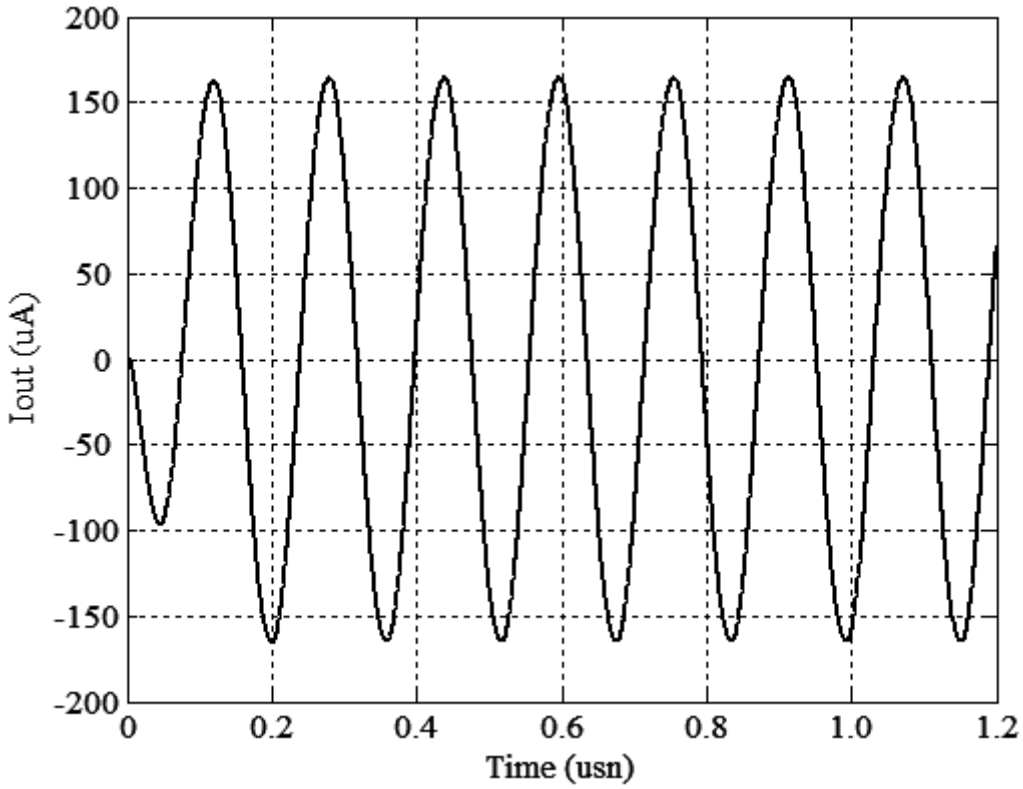

Figure 3.5. Output waveforms of the BP response.

4. CDBA - BASED SYNTHETIC FLOATING INDUCTANCE CIRCUITS WITH ELECTRONIC TUNING PROPERTIES

4.1. Introduction

Numerous synthetic floating inductance (FI) circuits using different active elements such as opamps [31], current conveyors [32, 33], four terminal floating nullors (FTFNs) [34], balanced output transconductors [35], translinear conveyors [36] and operational mirrored amplifiers (OMAs) [37] are reported in technical literature. FI circuits with grounded capacitors are preferred due to noise and stability considerations in IC implementation. In some of the previously reported current mode designs of this kind, different types of active elements are employed within the same FI circuit. For example, some [38-39] require both negative and positive types of second generation current conveyors. Another FI proposal [40] requires four pieces of current conveyors, one of them being first (CCI) and three others second generation (CCII) type, while current controlled second generation current conveyors (CCCIIs) together with conventional opamps need to be implemented in the same circuit proposed in some of the more recent papers [41-42].

However, from the point of cost reduction and ease of IC fabrication processes, it is advantageous to realize an FI circuit by employing only one type and minimum number of active elements.

In this chapter, two lossless CDBA-based FI circuits are presented [43]. The circuits provide the advantages of electronic tuning capability and full integrability. A circuit simulation example is also given to illustrate the feasibility of using the proposed synthetic FI configurations.

4.2. Circuit Description

The circuit symbol of the CDBA is shown in Figure 2.1. Assume that two matched MOSFETs operate in triode region, as shown in Figure 4.1. Their drain source currents in that region can be given as

$$I = K(V_g - V_T)(V_d - V_s) + a_1(V_d^2 - V_s^2) + a_2(V_d^3 - V_s^3) + \cdots \quad (4.1)$$

where $K=\mu.C_{ox}.w/l$ and μ, C_{ox}, w, l, and K stand for carrier mobility, channel capacitance, width and the length of the channel, and transconductance, respectively. Note that, gate voltages V_{a1} and V_{b1} are not indicated on the equivalent schematic.

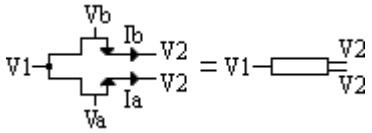

Figure 4.1. MOSFET Resistive circuit nonlinearity cancellation.

It is proven that [44], both the even and odd nonlinearities are cancelled by subtraction because the transistors have equal drain and source voltages,

$$I_a - I_b = g(V_i - V_2) \quad (4.2)$$

and

$$g=K(V_a-V_b) \tag{4.3}$$

is the conductance term. This circuit is termed as MOS resistive circuit, or simply MRC.

In order to subtract the current of MOSFETs operating in triode region, one can use the input terminals of the CDBA, since both terminals are at virtual ground potential. Note that the value of the conductance term can be positive, zero, or negative, depending upon the choice of the gate control voltages V_a and V_b.

Figure 4.2 shows the first proposed CDBA-based circuit for electronically tunable floating inductor. Note that, if the capacitor is replaced by an external resistor R, the circuit acts as a resistance multiplier, Z=kR, k>0.

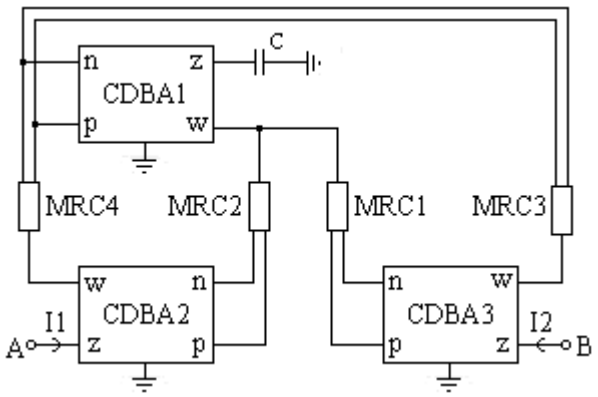

Figure 4.2. Electronically tunable, floating inductor using three CDBAs.

In order to simplify the analysis, let design parameters of MRCs be selected so that, g_1 and g_2 represent the gyration conductances for $MRC_2 \equiv MRC_3$, and $MRC_4 \equiv MRC_5$, respectively. Using (2.8) and (4.2), and by routine circuit computation, the short circuit admittance equation can be found as

$$[Y] = Z_3 g_1 g_2 \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{4.4}$$

In this equation, if $Z_3=1/sC$, and for further simplification $g_1=g_2=g$, the admittance seen between z terminals of $CDBA_1$ and $CDBA_2$ becomes

$$Y = \frac{K^2}{sC} \tag{4.5}$$

Equation (4.5) indicates that the circuit simulates an inductance

$$L = \frac{C}{\left(\mu C_{OX}\left(|V_a| - |V_b|\right)\right)^2 \left(\frac{w}{l}\right)^2} \tag{4.6}$$

which can be tuned electronically by adjusting the gate voltages of respective MOSFETs in MRCs.

Figure 4.3 shows another CDBA based tunable FI configuration. Here, $CDBA_1$ and $CDBA_2$ along with MRC1 and MRC2 constitute a gyrator circuit [26]. Therefore, a floating inductor can be synthesized easily by cascading two identical gyrators and placing a grounded capacitor C at their connection terminal. This will yield a floating inductor whose inductance is also described by equation (4.6) and can be tuned electronically by adjusting the gate voltages of respective MOSFETs in MRCs. However, this configuration requires four CDBAs.

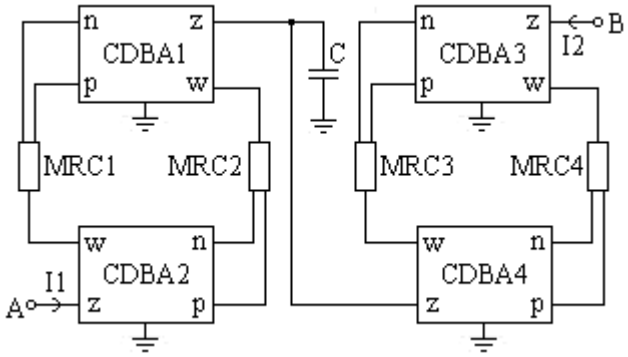

Figure 4.3. Alternative tunable, floating inductor using four CDBAs.

4.3. Simulation Results

Figure 4.4 demonstrate series resonator circuit used to test three-CDBA based FI configuration. Simulations are made using the configuration in Figure 4.4. MRCs are nMOS type transistors and their aspect ratios are W=28μm and L=0.7μm. For all MRCs V_a=1.8V and V_b=0.8V is used. Series resistor chosen to be R_s=40Ω.

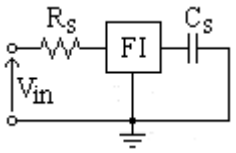

Figure 4.4. Series resonance circuit using
CDBA-based floating inductance simulator.

Three inductance values are simulated, 90mH, 900μH, and 9μH. All component values and simulation data can be seen in Table 4.1 and simulation graphics can be seen in Figure 4.5.

Table 4.1. Simulation results (for R_s=40Ω).

C	Simulated L	C_s	Calculated Frequency	Simulated Frequency	Difference (per cent)
50nF	450mH	3μF	79.1Hz	79.02Hz	0.336
		6μF	96.9Hz	96.16Hz	-0.764
		9μF	137Hz	137.46Hz	-0.101
500pF	4.5mH	30nF	7.91kHz	7.86kHz	-0.394
		60nF	9.69kHz	9.66kHz	-0.311
		90nF	13.7kHz	13.65kHz	-0.607
5pF	45μH	300pF	791kHz	785.24kHz	-0.396
		600pF	969kHz	966.55kHz	-0.253
		900pF	1370kHz	1364.58kHz	-0.729

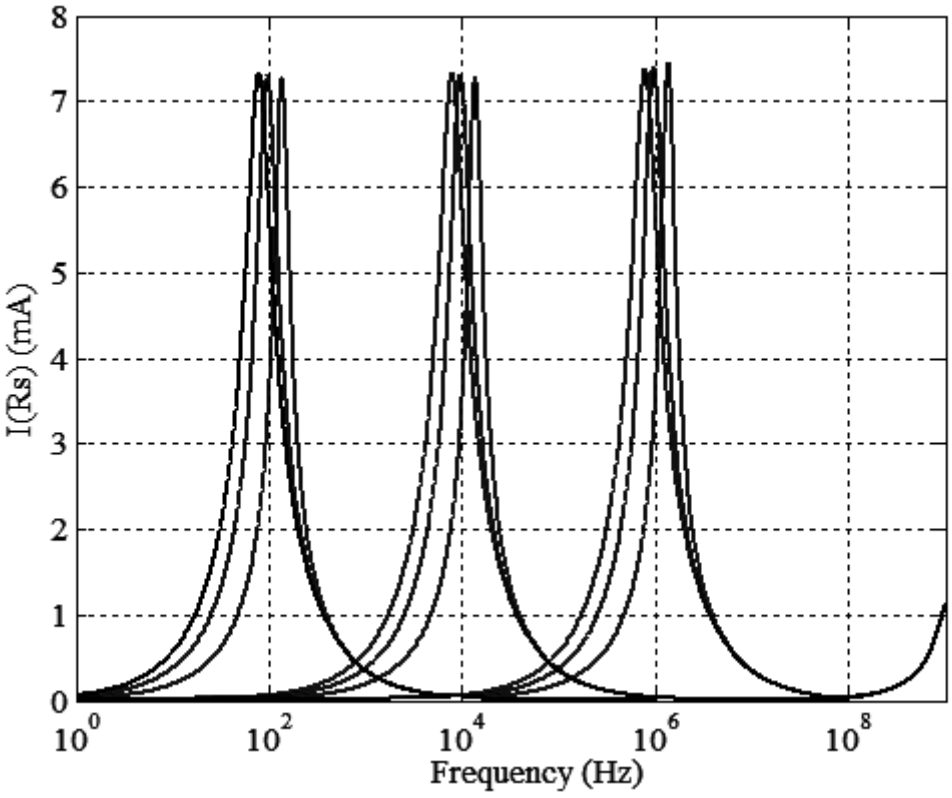

Figure 4.5. The series resonance circuit responses.

In the Figure 4.5, left curves block component values are R_s=40Ω, C=50nF, C_s=3μF – 6μF – 9μF; middle curves block component values are R_s=40Ω, C=500pF, C_s=30nF –

60nF – 90nF; right curves block component values are R_s=40Ω, C=5pF, C_s=300pF – 600pF – 900pF. It is apparent that simulation results are in good agreement with theory. Calculated and simulated natural frequencies are very close.

Figure 4.6 shows the series resonance circuit behavior for different series resistor R_s values. Changing R_s affects the quality factor of the resonance circuit. For this simulation we have used simulated 4.5mH inductance, C_s=60nF series capacitance and different values of R_s from 1Ω to 300Ω. These component values give a frequency of 9.66kHz.

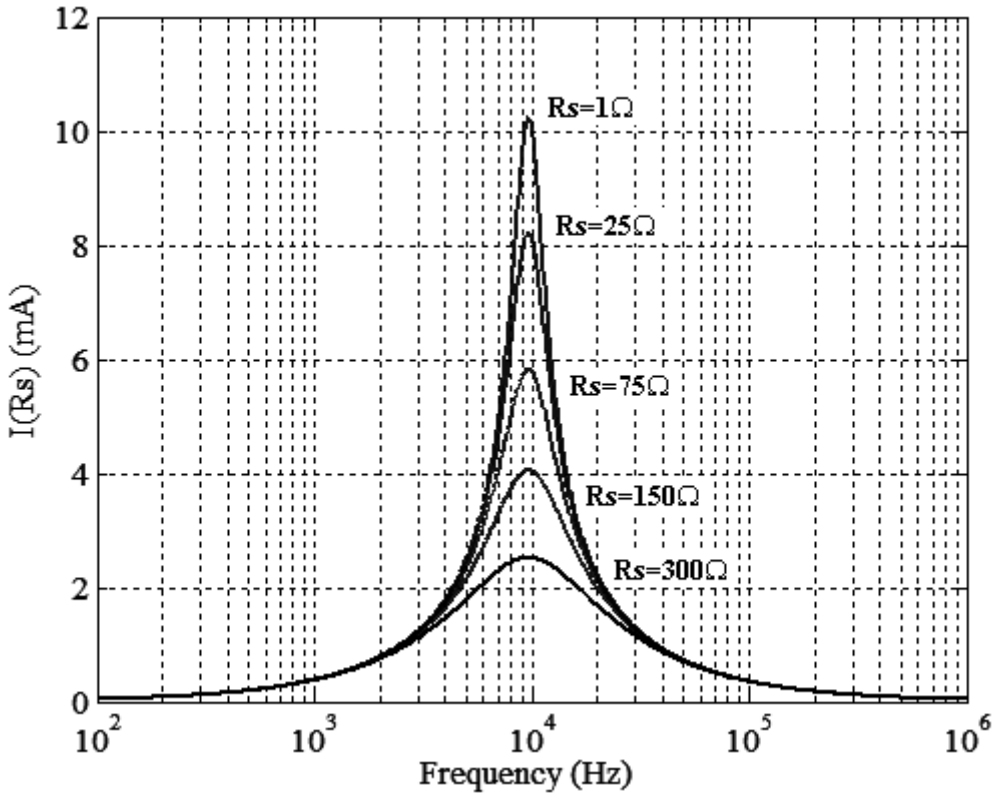

Figure 4.6. The series resonance circuit behavior for different series resistor R_s values.

Total harmonic distortion of output signal at selected frequencies of 96.16Hz, 9.66kHz and 966.55kHz are 0.04, 0.63, and 0.8 percent, respectively. For this simulation

series resistor is fixed to R_s=40Ω and 20mV peek-to-peek input sinusoidal voltage signal at the natural frequency of resonance circuits is used.

5. CONCLUSIONS

A novel current differencer and a CDBA based on this sub-circuit are studied in chapter two. Proposed CDBA has very low input and w terminal output impedances. Having a wide bandwidth allows this circuit to be used in high frequency signal processing applications.

A CM multifunction filter involving two CDBAs is introduced in chapter three. The proposed circuit has the following properties:

a) Its w_0 has small passive sensitivities, and insensitive to tracking errors of the CDBA.

b) Its Q can be controlled by varying R_c without affecting w_0 in a limited range due to low- Q of the circuit.

c) The proposed circuit permits low input impedance due to unconditionally grounded input terminals of the CDBA, which eliminates loading problem for the CM signal source.

d) This non-canonic filter can be cascaded without input-output impedance matching requirements. Note that, most cascadable filters permit cascadability due to their high output impedances. But, most of them do not exhibit low input impedance (except [45]).

e) It employs capacitors that are grounded or virtually grounded, which is an important aspect regarding integrated circuit implementation.

f) In addition to the fact that the proposed circuit employs only two active elements in realizing all five filter transfer functions, the number of passive components required is less than those of previously reported CDBA-based CM multifunction filters [7-9] for the same number of transfer function realizations.

g) This multifunction biquad configuration is a universal filter in the sense that it realizes LP, HP, BP and BS filter transfer functions.

These advantages offset the passive component matching requirement that can be easily met by today's sophisticated IC manufacturing techniques. Therefore, this proposed CM filter consisting of two CDBA elements and fewer passive components is expected to be useful in analogue signal processing applications.

CDBA-based FI simulator circuits are proposed in chapter four. These circuits are fully integrable and have voltage tuning properties. Moreover, they can be easily converted into fully integrable and linearly tunable resistance scaling circuits. Although cascaded gyrator based FI configuration requires four CDBAs, other FI circuit proposed in this study contains three CDBAs, saving one active element. In fact, FI circuits employing two active components can also be realized [32], however such circuits do not have grounded capacitors, and they are prone to noise problems. In that sense, the proposed three CDBA-based FI circuit is optimal.

Note also that, the same circuit topology can be used as a tunable linear floating resistance scaling circuit by replacing the capacitor in Figure 4.2 with an external resistor. Such circuits are very useful in integrated circuit design when large valued resistances can not be integrated due to their excessive occupation of silicon chip area,

and simple triode operation of an individual MOSFET as resistor can not provide sufficient linearity.

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